ABSTRACT

Title of dissertation: LOW PHASE NOISE CMOS PLL FREQUENCY SYNTHESIZER DESIGN AND ANALYSIS

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The phase-locked loop (PLL) frequency synthesizer is a critical device of wireless transceivers. It works as a local oscillator (LO) for frequency translation and channel selection in the transceivers but suffers phase noise including reference spurs. In this dissertation for lowing phase noise and power consumption, efforts are placed on the new design of PLL components: VCOs, charge pumps and $\Sigma\Delta$ modulators.

Based on the analysis of the VCO phase noise generation mechanism and improving on the literature results, a design-oriented phase noise model for a complementary cross-coupled LC VCO is provided. The model reveals the relationship between the phase noise performance and circuit design parameters. Using this phase noise model, an optimized $2GHz$ low phase noise CMOS LC VCO is designed, simulated and fabricated. The theoretical analysis results are confirmed by the simulation and experimental results. With this VCO phase noise model, we also design a low phase noise, low gain wideband VCO with the typical VCO gain around $100MHz/V$.

Improving upon literature results, a complete quantitative analysis of reference spur is given in this dissertation. This leads to a design of a charge pump by using a negative feedback circuit and replica bias to reduce the current mismatch which causes the reference spur. In addition, low-impedance charge/discharge paths are provided to overcome the charge pump current glitches which also cause PLL spurs.

With a large bit-width high order $\Sigma\Delta$ modulator, the fractional-N PLL has fine frequency resolution and fast locking time. Based on an analysis of $\Sigma\Delta$ modulator models introduced in this dissertation, a 3rd-order MASH 1-1-1 digital $\Sigma\Delta$ modulator is designed. Pipelining techniques and *true single phase clock* (TSPC) techniques are used for saving power and area.

Included is the design of a fully integrated 2.4GHz $\Sigma\Delta$ fractional-N CMOS PLL frequency synthesizer. It takes advantage of a $\Sigma\Delta$ modulator to get a very fine frequency resolution and a relatively large loop bandwidth. This frequency synthesizer is a 4th-order charge pump PLL with $26MHz$ reference frequency. The loop bandwidth is about $150KHz$, while the whole PLL phase noise is about $-120dBc/Hz$ at 1MHz frequency offset.

LOW PHASE NOISE CMOS PLL FREQUENCY SYNTHESIZER ANALYSIS AND DESIGN

by

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TABLE OF CONTENTS

LIST OF TABLES

LIST OF FIGURES

Chapter 1

Introduction

1.1 Motivation

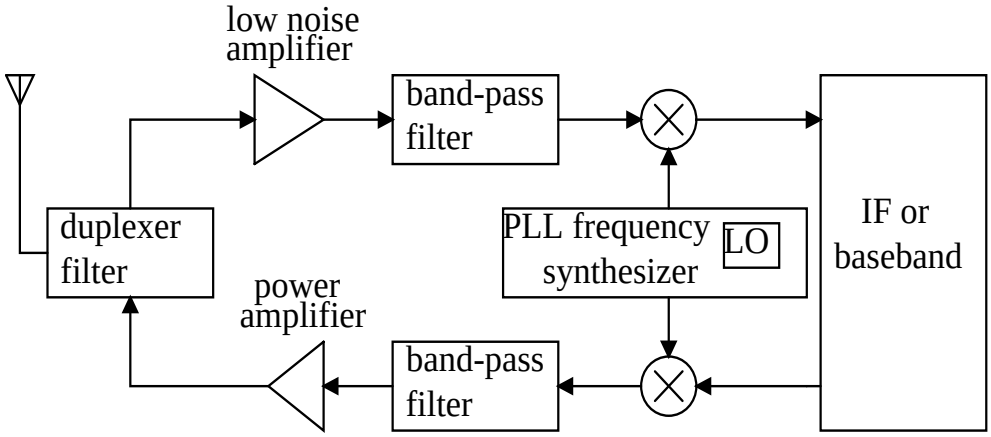


Figure 1.1: Block diagram of typical heterodyne transceiver [1]

This research focuses on the analysis and design of low noise, low power and high resolution RF PLL frequency synthesizers in CMOS technology. This is an important topic because the recent rapid growth in wireless communication has increased the demand for fully integrated, small size, low cost and low power consumption transceivers. With a constantly decreasing feature size in CMOS processes, it is possible to design a fully integrated radio-frequency (RF) front-end transceiver in CMOS technology. A Phase-locked loop (PLL) based frequency synthesizer is one of the key building blocks of a CMOS RF front-end transceiver. A frequency synthesizer is used as a local oscillator for frequency translation and channel selection

in the RF front-end of wireless transceivers. Figure 1.1 shows a generic transceiver [1]. The frequency synthesizer generates the local oscillator (LO) signals, which drive the receive and transmit mixers, converting the received signal from RF to IF or baseband signal, and similarly converting baseband or IF signal to RF for transmission.

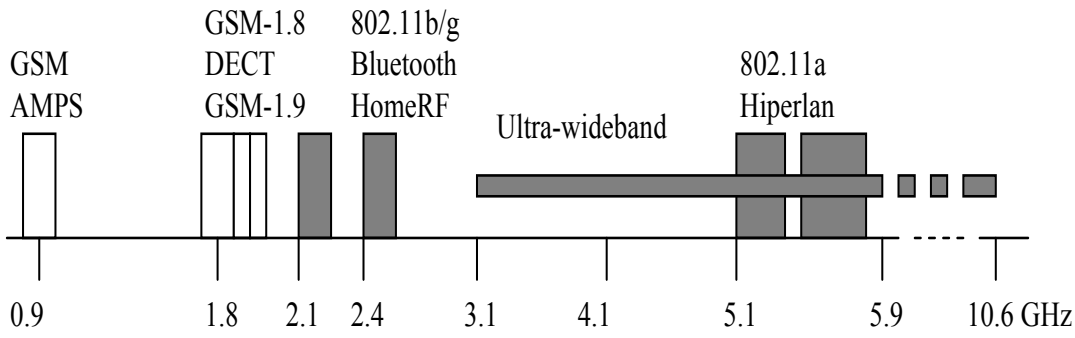


Figure 1.2: Frequency bands of wireless communication standards

Various wireless communication systems such as cordless/cellular phones, global positioning systems (GPS), and wireless local area networks (WLAN), and satellites need high quality transceivers. For different applications, there are specified wireless communication standards, such as AMPS, DECT, GSM, 802.11a/b/g WLAN, HiperLAN, Bluetooth, HomeRF, and so on. Many research efforts have been devoted to the high performance wireless tranceiver design in order to reach these standards' goals [2]-[8]. Recently a significant interest has grown in developing ultra wideband communications [9], [10], [11]. Figure 1.2 briefly illustrates the frequency band of some wireless communication standards.

With the exponentially increasing number of wireless users, more and more

channels are needed in the already scarce frequency resources. This demand has imposed much more stringent requirements on the phase noise and frequency resolution of a local oscillator. The goal to meet the requirements of the strict phase noise performance and fine frequency resolution remains a challenging research topic for the circuit designer.

PLLs are also widely used for other purposes. In optical communication systems, disk drive systems, and local area networks, PLLs are used for clock and data recovery [12], [13]. And in some complex digital systems, such as microprocessors, network routers, and digital signal processors, the clocks used at various points in the system are often synchronized through a phase locked loop to minimize clock skew [14], [15], [16]. Therefore, minimizing phase noise is very critical for improving these systems' performance.

1.2 Contributions

The main contributions of this work are briefly listed as follows:

- **Analysis of the third- and fourth-order PLL settling time**

  The frequency and time domain analyses of PLLs available in the literature are mainly based on second-order and a little on third-order approximation. But in practice the charge-pump PLLs are almost all of third- or fourth-order. The accurate frequency and time domain analyses of third- and fourth-order PLLs are presented in section 3.1. They produce more accurate results for practical high-order PLLs. The analysis results provide some guidelines for

the real design of PLLs.

- **Phase noise analysis of narrow-band and wideband LC VCOs**

  A design-oriented phase noise model for a differential cross-coupled LC VCO is proposed in section 3.3. The model combines small signal analysis and non-linear large signal concepts. By using this model, we theoretically analyze the circuit parameters' influence on the phase noise performance for both narrow band VCOs and wideband VCOs operating in a current-limited region and in a voltage-limited region, separately. Also, a narrow band LC VCO with on-chip octagonal differential inductors has been fabricated and evaluated.

- **Quantitative analysis of PLL reference spur**

  The reference spur of a charge pump PLL is even more difficult to quantitatively analyze compared to its phase noise. A complete quantitative analysis of the reference spur is given in section 3.5. Two main mechanisms - leakage current in the loop filter and current mismatch in the charge pump current source are investigated, and their contributions to spurs are analyzed independently. The resulting formulas give designers a good estimation of the reference spur level for practical PLL circuit design.

- **A CMOS charge pump circuit with improved current matching**

  In conventional charge pump design, one of the problems is the current mismatch between the up branch and down branch currents. The current mismatch causes the reference spur feedthrough. Another problem is the charge-

pump current glitches, which cause higher power level of the PLL spurs. We use a negative feedback circuit and replica bias to improve the current matching. To overcome the charge pump current glitches, low-impedance charge/discharge paths are provided. The detailed circuit is discussed in section 4.4.

- **Modelling and analysis of digital ΣΔ modulators for fractional-N PLLs**

  A digital ΣΔ modulator is used to control the instantaneous frequency division ratio for fractional-N PLL synthesizers. With an high order ΣΔ modulator, the PLL frequency resolution can be arbitrarily fine, and the loop bandwidth can be increased without deteriorating the spectral purity. The modelling and analysis of digital ΣΔ modulators are presented in section 3.6. A 3rd-order MASH ΣΔ modulator and a 3rd-order multi-bit, single loop ΣΔ modulator are chosen to analyze because the two modulators represent the extreme ends of the ΣΔ modulator topology spectrum. They are analyzed and compared in terms of DC input range, noise shaping and spurs.

- **Low power and low area design of a 3rd-order MASH digital ΣΔ modulator**

  The circuit implementation of a 3rd-order MASH digital ΣΔ modulator is discussed in section 4.5. Pipeline techniques are used to design the accumulators in a ΣΔ modulator. The pipelining deletes the critical path delay in adders. To achieve time alignment between the input and the delay carry information,

registers are used to skew the input bits. Moreover, dynamic *True Single-Phase Clock* (TSPC) techniques are used to implement the registers in a $\Sigma\Delta$ modulator for lowering power and area.

- **Implementation of a fully integrated 2.4GHz CMOS $\Sigma\Delta$ fractional-N frequency synthesizer**

  A fully integrated 2.4GHz CMOS fractional-N frequency synthesizer is designed that takes advantages of a $\Sigma\Delta$ modulator to a very fine frequency resolution and relative large loop bandwidth. A low power wideband VCO with low VCO gain (100MHz/V) and wide tuning range (1.897GHz $\sim$ 2.472GHz), a multi-modulus divider (64 $\sim$ 127), a 3rd-order MASH $\Sigma\Delta$ modulator, and other low-frequency components of a PLL to form a complete prototype synthesizer. The resulting circuit is a 4th-order charge pump PLL. The VCO voltage is 3.3V power supply, and bias current range is 2.0mA $\sim$ 2.8mA. A 26MHz reference frequency is used. The loop bandwidth is 150KHz. The whole PLL phase noise is -120dBC/Hz at 1MHz frequency offset.

1.3 Organization of Dissertation

In Chapter 2, the fundamentals of the frequency synthesizer and one key parameter, phase noise, are presented. Various frequency synthesizer architectures are discussed. Some of the existing VCO phase noise models are reviewed.

In Chapter 3, analysis of the PLL-based frequency synthesizer is covered. Various noise sources in a PLL are identified and their contributions to the closed loop

overall phase noise are derived. The PLL stability, locking time, and reference spur feedthrough are analyzed. A design-oriented phase noise model for a differential cross-coupled LC VCO is present. Two types of digital $\Sigma\Delta$ modulators for fractional-N PLLs are theoretical analyzed and compared.

In Chapter 4, a 2.4GHz fully integrated $\Sigma\Delta$ fractional-N CMOS RF frequency synthesizer is designed. It includes the LC-tuned voltage controlled oscillator, a phase frequency detector, a charge pump, a multi-modulus divider, and a MASH 1-1-1 digital $\Sigma\Delta$ modulator. The simulation and measurement results are also presented.

Finally, Chapter 5 gives a summary of our work and the future work.

Chapter 2

Frequency Synthesizers

This chapter describes some fundamentals of frequency synthesizers. First, frequency synthesizer's definition and its role in wireless communication are introduced. Then the definition of phase noise is presented and its effects on a transceiver are described. There are two types of frequency synthesizer used frequently: the direct digital frequency synthesizer and the phase-locked loop (PLL) frequency synthesizer. We will discuss them in section 2.3 and 2.4, respectively. Sections 2.5.1 gives an overview of the existing phase noise models.

2.1 Introduction

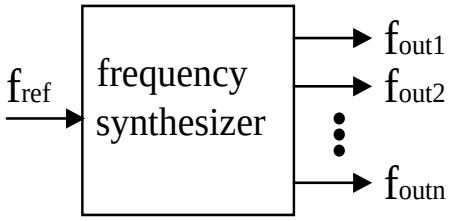


Figure 2.1: Frequency synthesizer

A frequency synthesizer is a device that generates one or many frequencies from one or few frequency sources. Figure 2.1 illustrates the input and output of a frequency synthesizer. The role of a frequency synthesizer in wireless transceiver systems is to provide the radio frequency (RF) for frequency translation as it has

been introduced in section 1.1.

2.2 Phase Noise

The ideal synthesizer produces a pure sinusoidal waveform

$$V(t) = V_0 \cos(2\pi f_0 t) \tag{2.1}$$

where V_0 and f_0 are amplitude and frequency of the signal. When amplitude and phase noise fluctuations are accounted, the waveform becomes

$$V(t) = (V_0 + v(t)) \cos(2\pi f_0 t + \phi(t)) \tag{2.2}$$

where $v(t)$ and $\phi(t)$ represent amplitude and phase fluctuations, respectively. Because amplitude fluctuations can be removed or greatly alleviated by a limiter, we concentrate on phase fluctuation effects in a frequency synthesizer output only. $\phi(t)$ represents the random phase variation and it produces phase noise. The spectral density of the phase variation is [17] p319 :

$$S_\phi(f) = \int_{-\infty}^{\infty} R_\phi(\tau) e^{-j2\pi f\tau} d\tau \tag{2.3}$$

where $R_\phi(\tau)$ is the auto-correlation of the random phase variation $\phi(t)$

$$R_\phi(\tau) = E[\phi(t)\phi(t-\tau)] = \int_{-\infty}^{\infty} \phi(t)\phi(t-\tau) dt \tag{2.4}$$

When the root mean square (rms) value of $\phi(t)$ is much less than 1 *radian*, the frequency synthesizer output signal can be written as

$$V(t) \approx V_0 \cos(2\pi f_0 t + \phi(t)) \approx V_0 \cos 2\pi f_0 t - \phi(t) V_0 \sin 2\pi f_0 t \tag{2.5}$$

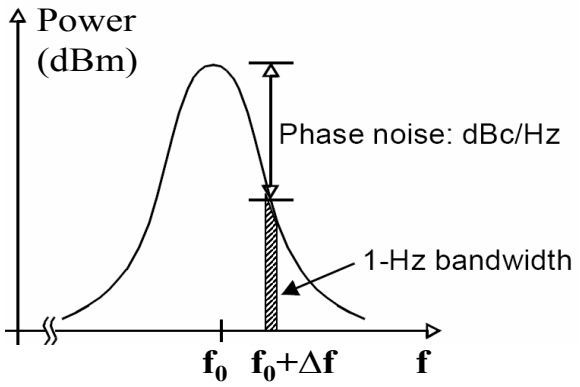


Figure 2.2: The definition of phase noise

The power spectrum density of $V(t)$ can be written as

$$S_V(f) = \frac{V_0^2}{2}\left[\delta(f - f_0) + S_\phi(f - f_0)\right] \tag{2.6}$$

It consists of the carrier power at f_0 and the phase noise at frequency offset $\Delta f = f - f_0$. The single-sideband (SSB) phase noise $L\{\Delta f\}$ is defined as the ratio of noise power in $1Hz$ bandwidth at frequency offset Δf from the carrier to the carrier power. The unit is dBc/Hz, and the "c" in the unit means carrier.

$$L\{\Delta f\} = 10 \cdot \log \frac{P_{noise}(f_0 + \Delta f, 1Hz)}{P_{carrier}} = 10 \cdot \log \frac{S_\phi(\Delta f)}{2} \tag{2.7}$$

where $P_{noise}(f_0 + \Delta f, 1Hz)$ is the noise power in 1Hz bandwidth at offset frequency Δf from the carrier frequency f_0 and $P_{carrier}$ is the carrier power. Figure 2.2 illustrates the phase noise of synthesized signal of frequency f_0.

To understand the importance of phase noise in a wireless receiver, consider the situation depicted in Fig. 2.3 [1]. The LO signal used for down conversion has a noisy spectrum. Two transmitters are present, the wanted signal with small power

and an unwanted signal in the adjacent channel with a large power level. When these two signals are mixed with the LO output, the down-converted signal will consist of two overlapping spectra. From the last line of Fig. 2.3, it is seen that the wanted signal suffers from significant noise due to the tail of the interferer.

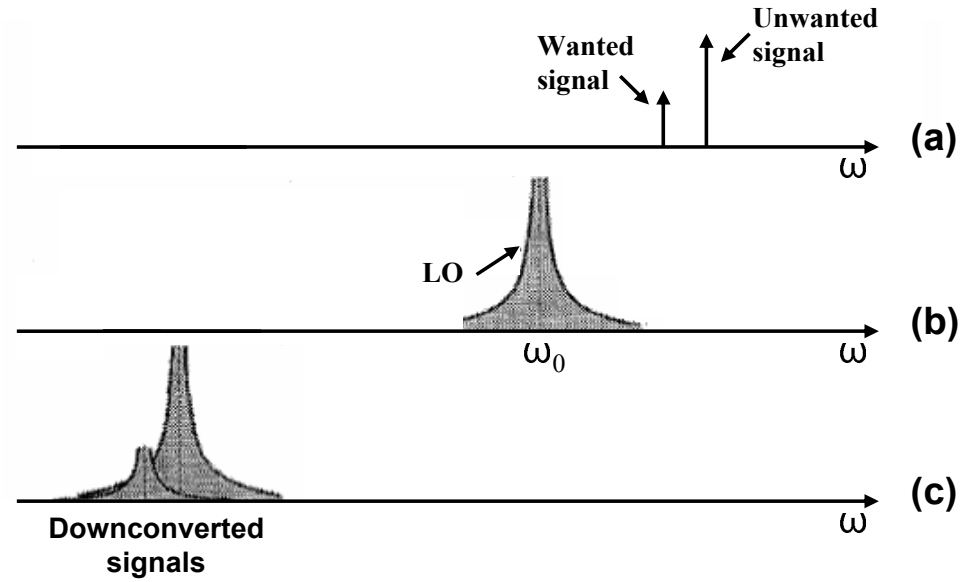


Figure 2.3: The effect of phase noise on receiver: (a) Two signals from two transmitters, (b) A local oscillator signal, (c) The two downconverted signals [1]

2.3 Direct Digital Frequency Synthesizer

Figure 2.4 shows a typical block diagram of a direct digital frequency synthesizer (DDS) [18]-[20]. It consists of a numerically controlled oscillator (NCO), a digital-to-analog converter (DAC), and a low pass filter (LPF). The NCO is made up of an adder-register pair (also known as a phase accumulator) and a ramp-to-sinewave lookup ROM. The output of the DDS is related to the phase accumulator

input by the following equation:

$$f_{out} = \frac{K}{2^N} \cdot f_{clock} \tag{2.8}$$

where N is the bit width of the accumulator and K is the accumulator's input. DDS has many advantages. For example, since there is no feedback in a DDS architecture, it is capable of extremely fast frequency switching or hopping at the speed of the clock frequency. A DDS also provides very fine frequency resolution. However a DDS has two major deficiencies. The first one is that the output spectrum of the DDS is normally not as clean as a PLL output. The noise floor of the DDS output spectrum is limited by a finite number of bits in the DAC. In order to get better DDS noise performance, various phase noise reduction techniques for DDSs have been proposed [21]-[23] recently. The second deficiency is that the DDS output frequency is limited by the maximum frequency of operation of the DAC and the digital logic. Although a high speed DDS design suitable for multi-GHz clock frequency has been reported [24], however, the power required both for the DAC and for the digital waveform computing circuitry increases approximately in proportion to its frequency.

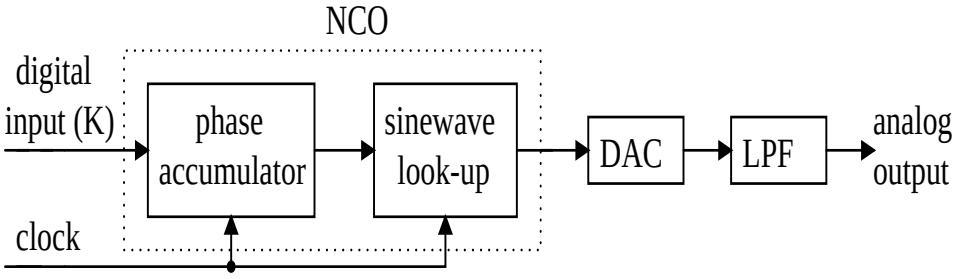


Figure 2.4: A DDS block diagram

2.4 PLL-based Frequency Synthesizer

As we have described in Fig. 1.1, a PLL frequency synthesizer is one of the key building blocks of a CMOS RF front-end transceiver. In this section, we will introduce three main PLL frequency synthesizers.

2.4.1 Integer-N PLL Frequency Synthesizer

As shown in Fig. 2.5, a basic PLL-based integer-N frequency synthesizer consists of four basic components: a phase detector (PD), a loop filter, a voltage controlled oscillator (VCO), and a programmable frequency divider [25]-[27]. The phase detector compares the phase of the input signal against the divided phase of the VCO. The output of the phase detector is a measure of the phase difference between the two inputs. The difference voltage is then filtered by the loop filter and applied to the VCO. The control voltage on the VCO changes the frequency in the direction that reduces the phase difference between the input signal and the frequency divider output.

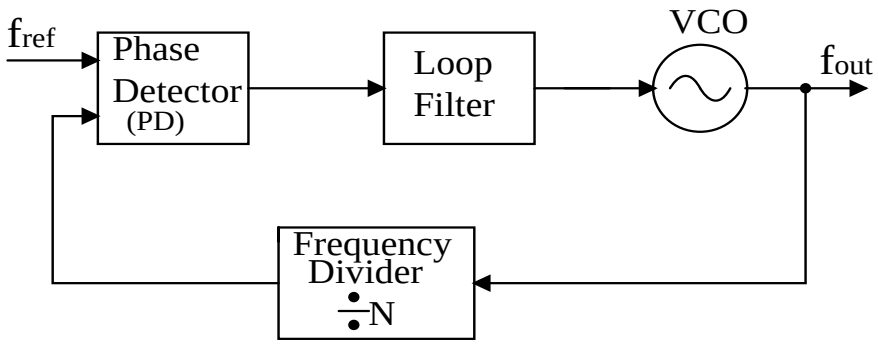


Figure 2.5: An integer-N PLL frequency synthesizer block diagram

For an integer-N synthesizer, the output frequency is a multiple of the reference frequency:

$$f_{out} = N \cdot f_{ref} \tag{2.9}$$

where N, the loop frequency division ratio, is an integer. From Eq. (2.9), the frequency resolution is equal to the reference frequency f_{ref}. Due to this limitation of the reference frequency, for narrow-band applications, the reference frequency of the synthesizer is very small. PLL stability requires that the loop bandwidth is on the order of 1/10 of the reference frequency [28]. So the small reference frequency results in a very small loop bandwidth, moreover, a very large frequency division ratio.

The conventional integer-N PLL with low reference frequency has several disadvantages. First, the lock time is long due to its narrow loop-bandwidth. Second, the reference spur (see section 3.5.1 for details) and its harmonics are located at low offset frequencies. Third, the large division ratio (N) increases the in-band phase noise associated with the reference signal, phase detector, and frequency-divider. Finally, with a small loop bandwidth, the phase noise of the VCO will not be sufficiently suppressed at low offset frequencies. So, multi-loop PLL frequency synthesizers and fractional-N frequency synthesizers are introduced to improve the performance of integer-N PLL synthesizers.

To get more insight into PLL frequency synthesizer design, we will introduce the linear PLL model and charge pump PLL in the remaining part of this subsection.

A. PLL Linear Model

A linear time-invariant PLL model is shown in Fig. 2.6. Such a model is suitable for modelling the behavior of the PLL to small perturbations when the PLL is locked. In the linear model, PD has a gain of $K_{pd}(V/rads)$, the loop filter has a transfer function $F_{lpf}(s)$, and the VCO has a gain of K_{VCO} (rads/sV). The reference signal has a phase ϕ_{ref} and the VCO output has a phase ϕ_{out}.

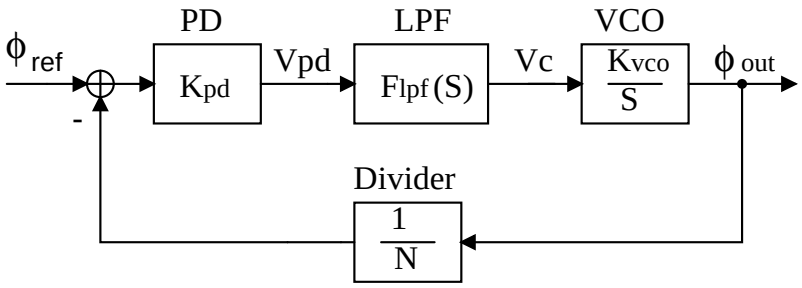


Figure 2.6: Linear time-invariant integer-N PLL model

The linear model of the PLL can be viewed as a standard feedback system with a forward transfer function, $K_{pd} \cdot F_{lpf}(s) \cdot K_{vco}/s$, and a feedback gain, $1/N$. The return ratio transfer function $G(s)$ is then

$$G(s) = \frac{K_{pd} \cdot F_{lpf}(s) \cdot K_{vco}}{N \cdot s} \tag{2.10}$$

Here we introduce an important parameter in PLL design, the **loop bandwidth** ω_c, which is defined as the frequency where the open loop gain $|G(j\omega_c)|$ drops to unity, i.e., $|G(j\omega_c)| = 1$.

The closed loop function can be written as

$$H(s) = \frac{\phi_{out}(s)}{\phi_{ref}(s)} = N \cdot \frac{G(s)}{1 + G(s)} \tag{2.11}$$

B. Charge Pump PLL

In many modern PLL, the phase detector is implemented by a tri-state phase frequency detector (PFD) combined with a charge pump (CP) [28]. This type PLL is called a charge pump PLL . The PFD can detect both the phase and frequency difference between two signals. Consequently, the PFD/CP PLL has infinite **pull-in range** irrespective of the type of filter used. **Pull-in range** is the frequency range within which a PLL can get locked from an unlocked state.

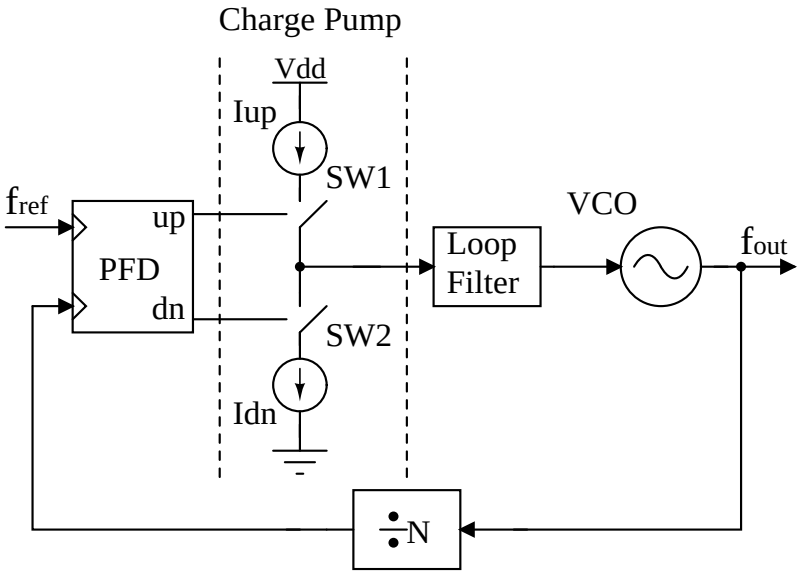


Figure 2.7: Charge pump integer-N frequency synthesizer

A simplified charge pump PLL block diagram is shown in Fig. 2.7. Its time-invariant linear model is shown in Fig. 2.8. A phase frequency detector (PFD) is a digital phase detector having *up*, *dn* output pulse signals. The charge pump consists of two switched current sources which drive the loop filter. The switches of the charge pump are controlled by the PFD output signals *up* and *dn*. The pulse

width of *up* or *dn* is proportional to the amount of phase error at the the PFD input [26]. The charge pump will charge or discharge capacitors in the loop filter when switch $SW1$ or $SW2$ is on. The VCO control voltage is proportional to the integration of phase error ϕ_e and can be written as

$$V_c(s) = \frac{I_{cp}}{2\pi} \cdot F_{lps}(s) \cdot \phi_e \tag{2.12}$$

The open loop transfer function $G(s)$ now becomes

$$G(s) = \frac{I_{cp} \cdot F_{lpf}(s) \cdot K_{vco}}{2\pi \cdot N \cdot s} \tag{2.13}$$

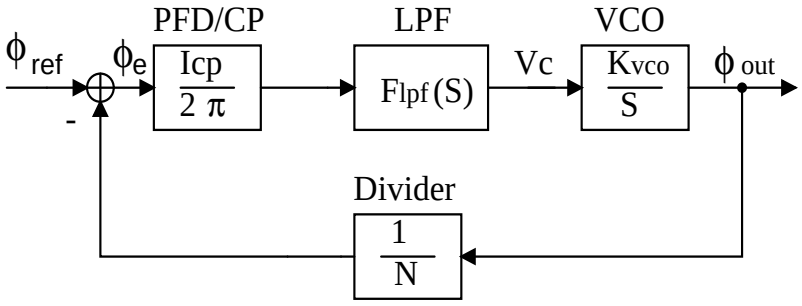


Figure 2.8: Linear time-invariant charge pump PLL model

We will use the charge pump PLL for our PLL frequency synthesizer design.

2.4.2 Multi-loop PLL Frequency Synthesizer

To avoid the large division ratio in an integer-N PLL synthesizer, two or more loops can be employed to reduce the division ratio of the whole loop. A dual-loop PLL is frequently used to improve the tradeoff among phase noise, channel spacing, reference frequency and the locking speed [29]-[31].

Some dual-loop PLL frequency synthesizer architectures are shown in Fig. 2.9. In Fig. 2.9(a), PLL1 is used to generate reference frequencies for PLL2. In Fig. 2.9(b) the output of PLL1 is up-converted by PLL2 and a single-sideband (SSB) mixer (up-conversion). PLL1 generates tunable IF frequencies, while PLL2 generates a fixed RF frequency. In Fig. 2.9(c) and 2.9(d), PLL2 and a SSB mixer (down-conversion) are used to reduce the divide ratio in PLL1.

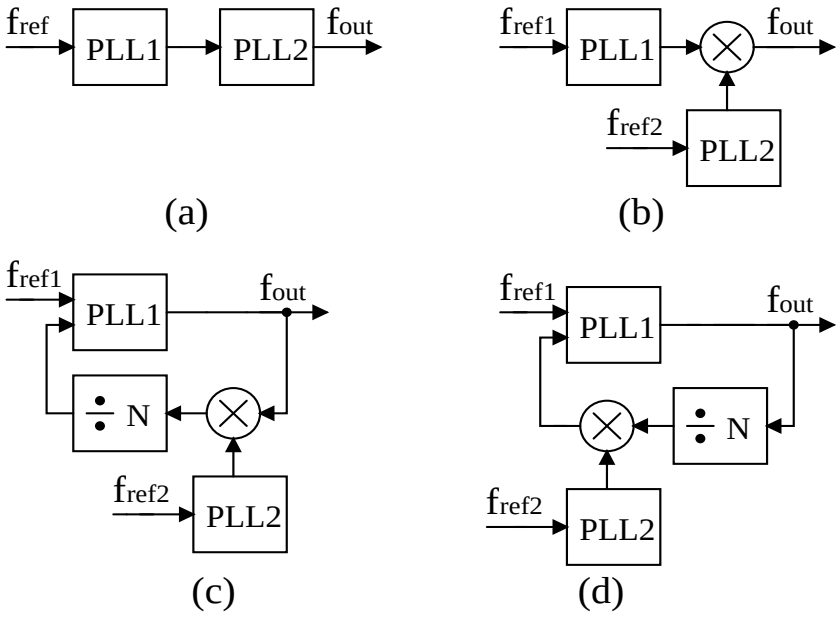


Figure 2.9: Dual loop PLL frequency synthesizers

The drawback of dual-loop PLLs is that they may require two references, and/or at least one SSB mixer, which might introduce additional phase noise [32]. Moreover, when one PLL is used as a reference for the other, the reference noise is much higher than that of crystal oscillators.

2.4.3 Fractional-N PLL Frequency Synthesizers

Fractional-N frequency synthesizers are used to overcome the disadvantages of integer-N synthesizers. In fractional-N synthesizers, fractional multiples of the reference frequency can be synthesized, allowing a higher reference frequency for a given frequency resolution.

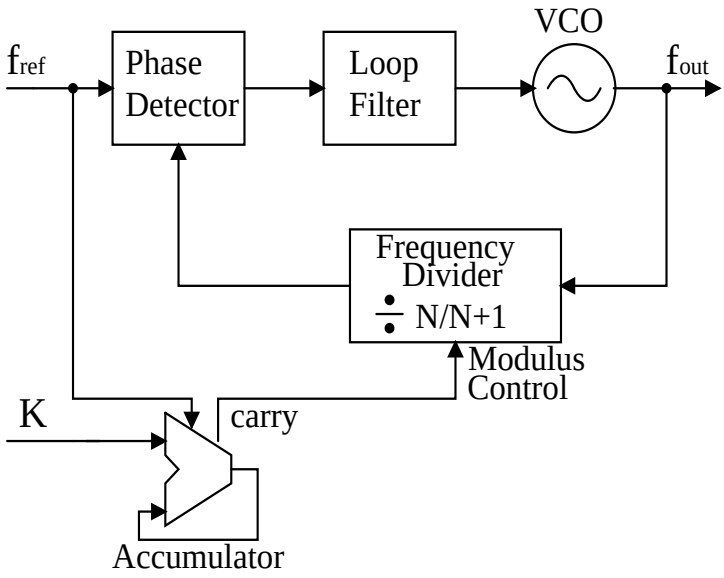


Figure 2.10: Fractional-N frequency synthesizer

In Fig. 2.10 the division modulus of the frequency divider is steered by the carry bit of a simple digital accumulator of m-bit width. The symbol $\div N/N+1$ of the divider means that the division ratio is $N+1$ when the carry bit is 1, otherwise the division ratio is N. To realize a fractional division ratio $N+F$, with $F \in [0,1]$, a digital input $K = F \cdot 2^m$ is applied to the accumulator. A carry output is produced every K cycles of the reference frequency f_{ref}, which is also the sampling frequency of the digital accumulator. This means that in 2^m clocks of reference frequency f_{ref},

the division ration is N for $(2^m - K)$ clocks, and the division ration is $N+1$ for K clocks. This results in a average division ratio N_{avg}, given by

$$\begin{aligned} N_{avg} &= \frac{(2^m - K) \cdot N + K \cdot (N+1)}{2^m} \\ &= N + \frac{K}{2^m} = N + F \end{aligned} \tag{2.14}$$

This means that a non-integer division ratio can be realized. This technique also has disadvantages. The most important one is the generation of spurs in the output spectrum due to the noise on the modulus control called pattern noise [33] in the overflow signal. This can be better understood if the accumulator is regarded as a first-order $\Sigma\Delta$ modulator [34].

$\Sigma\Delta$ modulators in fractional-N synthesis were first introduced and analyzed in [34], [35] and further refined in [36]. As the input to a first order $\Sigma\Delta$ modulator is a *DC* signal, the quantization noise is not randomized, and the output contains many spurious signals [33], [34]. With higher order modulators the switching of the divider ratio is randomized, such that the spurious signals are much lower. The more detailed description of quantization noise and $\Sigma\Delta$ modulators are given as follows.

A. Quantization Noise

A quantizer and its linear model are shown in Fig. 2.11(a) and 2.11(b), respectively [37]. The output signal $y(n)$ is equal to the closest quantized value of $x(n)$. The quantization error e(n) is the difference between the input and output value. The linear model becomes approximate when assumptions are made that $e(n)$ is an

independent white-noise signal.

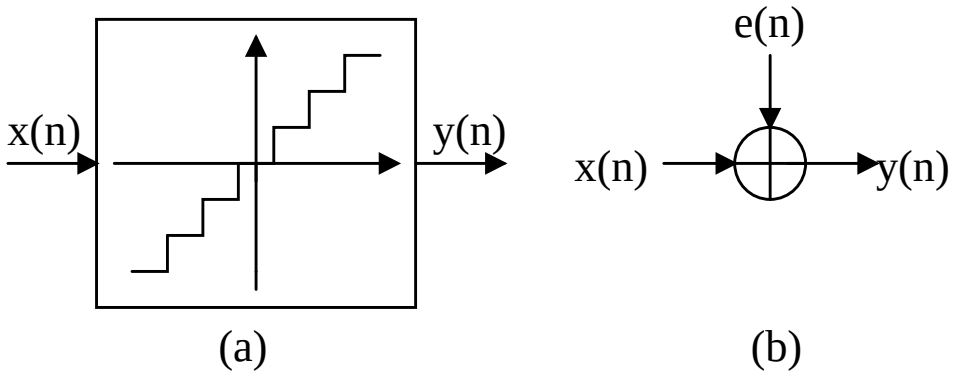


Figure 2.11: Quantizer and its linear model: (a) Quantizer, (b) Model

With the white noise assumption, the mean square of the quantization noise is given by:

$$e_{rms}^2 = \frac{1}{\Delta}\int_{-\Delta/2}^{\Delta/2} e^2 de = \frac{\Delta^2}{12} \tag{2.15}$$

where Δ is the distance between two quantization levels. If the sampling frequency is the same as the reference frequency f_{ref}, when the noise is sampled at frequency f_{ref}, all of the noise power folds into the frequency band $-f_{ref}/2 \leq f < f_{ref}/2$, with copies of this spectrum at each multiple of f_{ref}. Then the power spectrum density (PSD) of the quantization noise is:

$$S_e(f) = \frac{\Delta^2}{12 \cdot f_{ref}} \tag{2.16}$$

B. $\Sigma\Delta$ Modulator Technique

Figure 2.12 shows a a model of a first-order $\Sigma\Delta$ modulator using the quantizer of Fig. 2.11 [38]. The output of the modulator is:

$$Y(z) = z^{-1} \cdot X(z) + (1 - z^{-1}) \cdot E(z) \tag{2.17}$$

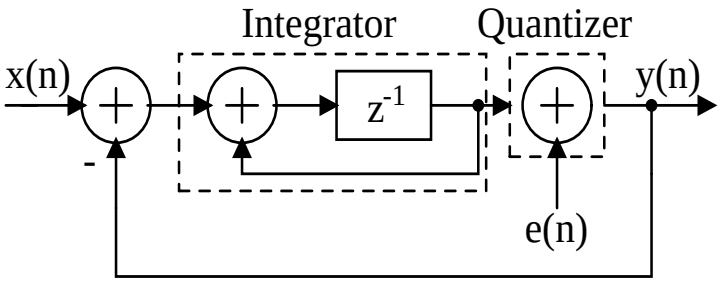


Figure 2.12: A first order ΣΔ modulator

The output is a delayed version of the input with shaped quantization noise. The operation of the first-order ΣΔ modulation of Fig. 2.12 is as follows; the input propagates to the quantizer through an integrator and the quantized output is fed back and subtracted from the input signal. This feedback forces the quantized output to track the input. The integrator shapes the quantization error with high-pass characteristic. Figure 2.13 shows an accumulator based first order sigma-delta modulator [34]. The feedback of this figure occurs implicity in the internal logic of the accumulator.

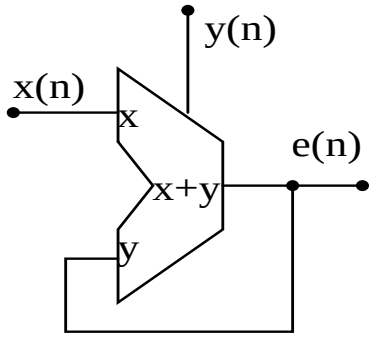


Figure 2.13: An accumulator regarded as a ΣΔ modulator [34]

For *nth*-order ΣΔ modulators, the quantization noise transfer function can be

written as [33]:

$$N_{TF}(z) = \frac{Y(z)}{E(z)} = (1 - z^{-1})^n \tag{2.18}$$

Using $z = e^{j\omega T_{ref}} = e^{j2\pi f/f_{ref}}$

Then

$$|N_{TF}(f)| = \left|1 - e^{-j2\pi f/f_{ref}}\right|^n = \left(2\sin\left(\frac{\pi f}{f_{ref}}\right)\right)^n \tag{2.19}$$

The general shapes of zero ($n = 0$), first ($n = 1$), and second ($n = 2$) order transfer function curves are shown in Fig. 2.14. From this figure, we can see that when $f < f_c$ (f_c is the loop bandwidth), the in-band noise power decreases as the noise-shaping order increases. However, the out of band noise increases for the high-order modulators. So, the $\Sigma\Delta$ modulator has noise shaping function. The out-of-band noise is filtered by the loop filter.

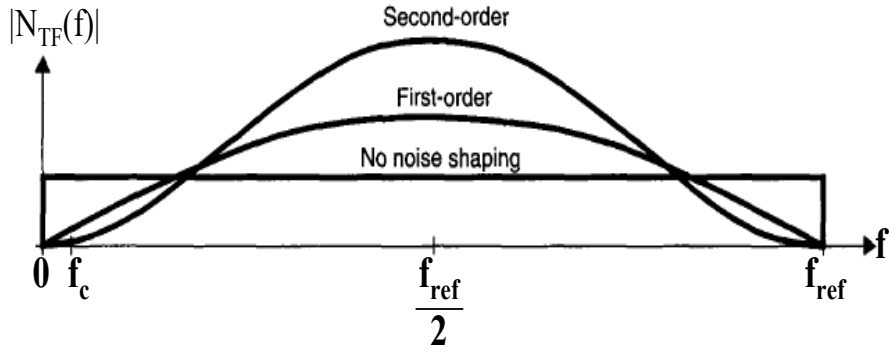


Figure 2.14: Some different order $\Sigma\Delta$ modulator transfer function

Using Eq. 2.16 and 2.19, then the PSD of the quantization noise is

$$\begin{aligned} S_f(f) &= |N_{TF}(f)|^2 \cdot S_e(f) \\ &= \frac{\Delta^2}{12 \cdot f_{ref}} \left[2\sin\left(\frac{\pi f}{f_{ref}}\right)\right]^{2n} \end{aligned} \tag{2.20}$$

C. Pipelining Technique

Adders and accumulators are the building blocks of MASH (multi-stage noise-shaping) ΣΔ modulators. In circuit design, adders or accumulators are often pipelined for saving power [39], [40]. So we will use this technique for our ΣΔ circuit design.

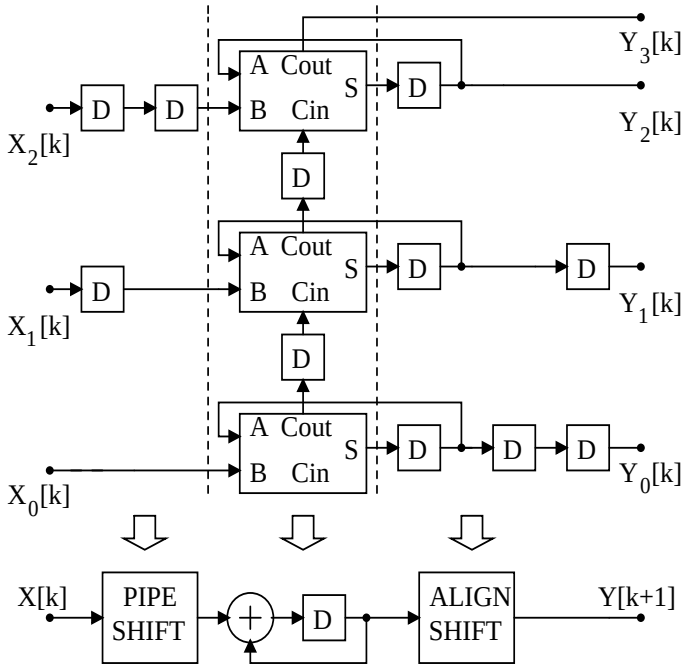


Figure 2.15: A 3-bit pipelined accumulator

The critical delay path for an adder is formed by the carry chain. The carry signal must propagate from the least to the most significant bit during each addition operation. This leads to a proportional relationship between the time required for computation and the number of bits in the adder. Pipelining of the carry path at the bit level breaks this relationship by allowing the carry information to travel through only one bit stage per clock cycle regardless of the number of bits in the adder.

Figure 2.15 shows a pipelined 3-bit accumulator, which is realized by inserting registers in the carry path. To achieve time alignment between the input and the delay carry information, registers are used to skew the input bits. We will use these pipeline techniques to realize our $\Sigma\Delta$ made of accumulators with the bit-width of 20 to make the quantization noise more randomized [33].

2.5 PLL Frequency Synthesizer Building Blocks

2.5.1 Voltage Controlled Oscillator

The VCO is a key block of a PLL frequency synthesizer. It determines the out of band phase noise performance. Commonly, both ring oscillators and LC oscillators are used in GHz range applications [41]-[46]. But the phase noise of a ring oscillators is generally not good enough in the application of narrow band wireless communication systems. LC oscillators are more attractive due to their low phase noise and low power consumption compared with that of a ring oscillator.

2.5.1.1 LC Oscillator

Figure 2.16 shows a model of a parallel LC oscillator. R_p is the equivalent parallel resistor of the LC tank, and C is a varactor, which capacitance is changed with the voltage V_c across it. The operational transconductance amplifier (OTA) has the negative input resistance of magnitude $1/G_m$, which is provided by active devices.

When $1/G_m \geq R_p$, the total resistance is zero or negative. That means when

$1/G_m = R_p$, the oscillator is in a resonance state. The resonant frequency is given:

$$\omega_0 = \frac{1}{\sqrt{L \cdot C(V_c)}} \tag{2.21}$$

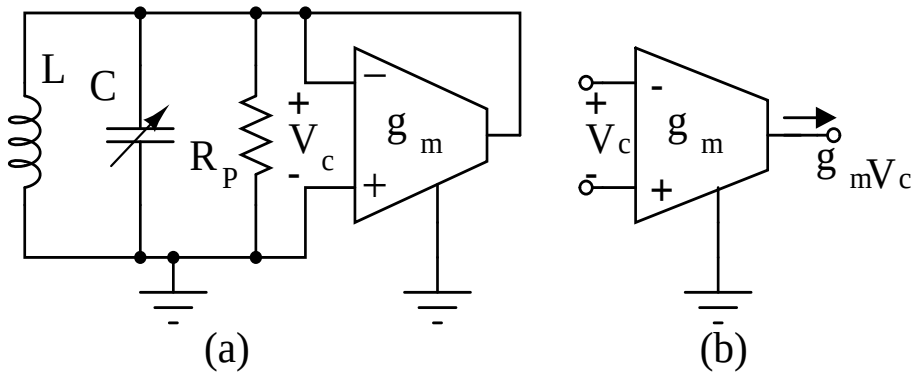


Figure 2.16: The general model of a parellel LC VCO: (a) RLC oscillator, (b) OTA

The quality factor Q of the LC tank itself is:

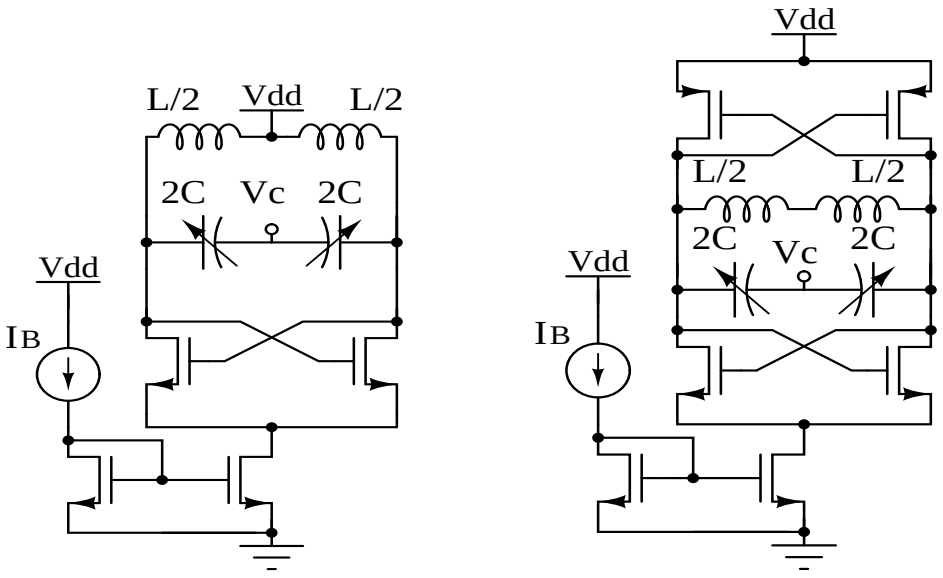
$$Q = 2\pi \cdot \frac{energy\ stored}{energy\ dissipated\ per\ cycle} = \frac{R_p}{\omega_0 L} \tag{2.22}$$

The higher quality factor Q means lower VCO phase noise. And phase noise is the most important specification in our PLL design. A good phase noise model is very important for low phase noise VCO design. In the following section, we review two of the existing LC oscillator phase noise models.

2.5.1.2 LC VCO Topologies

Cross-coupled LC oscillators play an important role in high frequency circuit design [44], [45], [48]. There are two basic types of cross-coupled pair VCO topologies as shown in Fig. 2.17. The single differential NMOS topology of Fig. 2.17(a) is

chosen to enable the oscillators to operate in the current limited region [44] for low power supply voltage. But the complementary differential topology of Fig. 2.17(b) is usually preferred in low-power applications. It exploits the same bias current with doubled efficiency compared to the structure with a single couple, when operating in the current-limited regime. So we will choose the tail-current biased complementary cross-coupled differential LC circuit for phase noise analysis.



(a) (b)

Figure 2.17: Cross-coupled pair LC VCO topologies: (a) NMOS-only cross-coupled pair, (b) NMOS-PMOS complementary pair

The LC tank quality value Q can be written as [47]:

$$Q = \frac{\omega_0 L}{r_s} \tag{2.23}$$

where r_s is the coil series resistance. With Eq. (2.22) and Eq. (2.23), then we get the equivalent parallel tank impedance as:

$$R_p(\omega_0) = Q \cdot \omega_0 \cdot L = \frac{(\omega_0 \cdot L)^2}{r_s} \tag{2.24}$$

From Eq. (2.24), we see R_p is a strong function of the oscillation frequency ω_0 and inductance L. The above equation is valid as long as the capacitive elements of the tank have a significantly higher quality factor than the inductor.

For Fig. 2.17(a), its transconductance is

$$g_m = \frac{g_{mn}}{2} = \sqrt{\frac{I_B}{2V_{ov,nmos}}} \tag{2.25}$$

where $V_{ov,nmos}$ is NMOS overdrive voltages. For Fig. 2.17(b) configuration, its conductance is $g_m = \frac{g_{mn} + g_{mp}}{2}$ [44]. Then the g_m can be

$$g_m = \frac{g_{mn} + g_{mp}}{2} = \sqrt{\frac{I_B}{2V_{ov,nmos}}} + \sqrt{\frac{I_B}{2V_{ov,pmos}}} \tag{2.26}$$

where $V_{ov,pmos}$ is the PMOS overdrive voltage. When

$$g_m = \frac{1}{R_p} = \frac{r_s}{(\omega_0 \cdot L)^2} \tag{2.27}$$

the oscillator is in a resonance state. Equaion (2.27) is the most fundamental design criterion satisfying start-up conditions for an LC oscillator. Equations (2.25), (2.26), and (2.27) indicate that there is a fundamental lower limit on the current consumption for a given transconductance and LC tank configuration. From Eq. (2.24), R_p gets larger as the resonance frequency gets larger. So, the worst-case oscillating condition occurs at the low-end of the desired frequency range. In practice, the small signal transconductance g_m is set to a value that guarantees start-up with a reasonable safety margin under worst-case conditions. Increasing g_m beyond this value generally leads to saturation contributing more noise and is thus undesirable.

2.5.1.3 *LC* VCO Phase Noise Model

A. Leeson's Model

The most well-known phase noise model is Leeson's model which was proposed by D.B. Leeson in 1966 [49]. He presented a heuristic derivation of the expected spectrum of a feedback oscillator in terms of known oscillator parameters without proof. His model is based on linear time invariant analysis.

In Fig. 2.16, when $\Delta\omega \ll \omega_0$, the impedance of the parallel RLC is easily calculated to be:

$$\begin{aligned} Z(j\omega) &= Z\left(j(\omega_0+\Delta\omega)\right) = j(\omega_0+\Delta\omega)L // \frac{1}{j(\omega_0+\Delta\omega)C} \\ &\approx -\frac{j\omega_0 L}{2(\Delta\omega/\omega_0)} = -jR_p\frac{\omega_0}{2Q\Delta\omega} \end{aligned} \tag{2.28}$$

The total equivalent parallel resistance of the tank has an equivalent mean square noise current of $\overline{i_n^2}/\Delta f = 4kT/R_p$, where k is the Boltzmann constant, and T is the absolute temperature.

Considering all noise sources rather than thermal noise, Leeson gave a multiplicative factor F. Then $\overline{i_n^2}/\Delta f = 4FkT/R_p$, and $v_n^2/\Delta f = |Z(j\omega)|^2 \cdot (\overline{i_n^2}/\Delta f)$ with the voltage leading to amplitude modulation (AM). So from Eq. (2.7), the phase noise is:

$$\begin{aligned} L\{\Delta\omega\} &= 10\cdot\log\frac{1/2\cdot\overline{v_n^2}/\Delta f}{\overline{v_{sig}^2}} \\ &= 10\cdot\log\frac{4FkTR_p}{V_0^2}\cdot\left(\frac{\omega_0}{2Q\Delta\omega}\right)^2 \end{aligned} \tag{2.29}$$

Note that the factor of 1/2 is based on the equal partition of AM and PM noise.

Finally, Leeson modified the phase noise equation as to [49]:

$$L\{\Delta\omega\} = 10 \cdot \log\left\{\frac{4FkTR_p}{V_0^2} \cdot \left[1 + (\frac{\omega_0}{2Q\Delta\omega})^2\right]\right\} \tag{2.30}$$

where an additive factor of unity inside the bracket is to account for the noise floor [47].

In Leeson's model, F is empirical, varying significantly from oscillator to oscillator. The value must be determined from measurements. With the unspecified noise factor F, the model can not predict phase noise from circuit noise analysis. We will analytically determine F in section 3.3.1.

B. Hajimiri's Non-linear time Variant Model

A more precise analysis was proposed by A. Hajimiri and T. Lee in 1998 [50]. It introduces the impulse sensitivity function (ISF or Γ) to consider the effects of nonlinearity, time-variance and cyclostationary noise. In this section, we follow the presentation of the phase noise model in [50].

ISF describes how much phase shift results from applying a unit impulse at any point in time. The phase shift response to a unit impulse can be expressed as

$$h_\phi(t,\tau) = \frac{\Gamma(\omega_0\tau)}{q_{max}}u(t-\tau) \tag{2.31}$$

where $\Gamma(\omega_0 t)$ is the ISF function, which is a dimensionless, frequency and amplitude independent periodic function with period 2π. q_{max} is the maximum charge displacement across the injected node capacitor and u(t) is the unit step function. Once the ISF has been determined, excess phase may be computed by using the

superposition integral:

$$\phi(t) = \int_{-\infty}^{\infty} h(t,\tau) i(\tau) d\tau = \frac{1}{q_{max}} \int_{-\infty}^{t} \Gamma(\omega_0 \tau) i(\tau) d\tau \tag{2.32}$$

where $i(\cdot)$ is an injected current. The ISF is periodic, so its Fourier series can be written as

$$\Gamma(\omega_0 \tau) = \frac{c_0}{2} + \sum_{n=1}^{\infty} c_n \cos(n\omega_0 \tau) \tag{2.33}$$

where the coefficients c_n are real. The injection of a sinusoidal current is written as $i(t) = I_m \cos[(m\omega_0 + \Delta\omega)t]$, where m is integer. Ignoring the terms other than $n = m$ in Eq. 2.32, then

$$\phi(t) \approx \frac{I_m c_m sin(\Delta\omega t)}{2 q_{max} \Delta\omega} \tag{2.34}$$

Performing phase to voltage conversion [50], the sideband phase noise can be given as:

$$L\{\Delta\omega\} = 10 \cdot \log \left[\frac{\frac{\overline{i_n^2}}{\Delta f} \sum_{m=0}^{\infty} c_m^2}{8 q_{max}^2 \Delta\omega^2} \right] \tag{2.35}$$

where $\overline{i_n^2}$ is the spectral density of the input noise current, and $\Delta\omega$ is the frequency offset from the carrier frequency ω_0.

Hajimiri's ISF function provides a good way if modelling phase noise. But it has some practical difficulties. First, a current impulse as a δ function of time has to be injected into a circuit node in a simulation in order to obtain its phase response. However, only a current with finite amplitude and time duration can be simulated. Second, in order to compute the ISF for a circuit node at time t, small time steps have to be taken to insure accuracy and a long time is needed to allow the circuit to settle to its steady state after the impulse is injected. As the circuit complexity

grows, the complete computation for all the ISFs becomes so time-consuming that it eventually becomes impossible.

To understand the phase noise mechanism, an appropriate noise model is very important in the design and optimization of the cross-coupled pair LC VCOs. In our research, we will provide a generalized linear phase noise model for a complementary LC VCO in section 3.3.1 by improving some literature analysis results of Kong in [51] and of Rael&Abidi in [52]. The model combines linear small signal analysis and non-linear large signal concepts. It is possible to predict the phase noise performance using the proposed model from circuit parameters.

2.5.2 Frequency Dividers

The frequency divider is one of the building blocks of a PLL frequency synthesizer that operates at high frequency. It converts the oscillator high output frequency to a lower frequency which can be compared to a reference source. So, the divider can see the full frequency range of a PLL from several hundred kHz to several GHz.

For a low power design, it is desirable to use an asynchronous divider structure to minimize the amount of circuitry at high frequencies. The dual-modulus approach achieves such a structure, and has been successfully used in many high speed, low power designs [54]-[56]. The multi-modulus divider is an extension of the popular dual-modulus topology. The ripple counter contained in the dual-modulus prescaler is replaced with a cascade of $\div 2/3$ dividers to form a multi-modulus prescaler [57], [58].

2.5.2.1 The Dual Modulus Divider

A fully programmable two-modulus divider usually consists of a two-modulus prescaler, a programmable counter (P), and a swallow counter (S), as shown in Fig. 2.18.

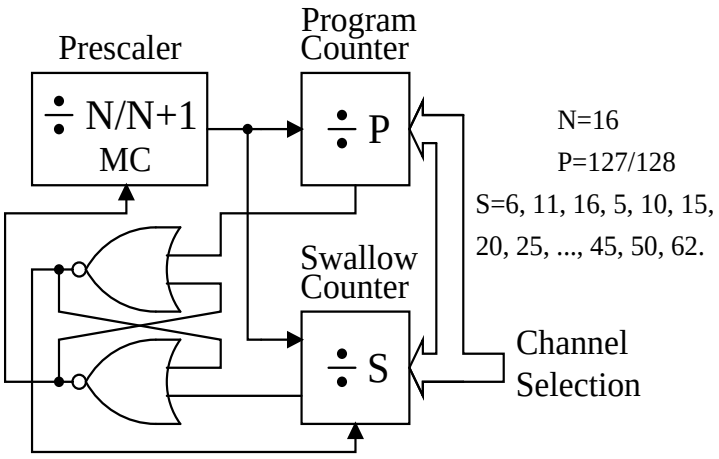


Figure 2.18: A full frequency divider with a dual-modulus prescaler and two counters

The dual-modulus prescaler divides the input frequency by either N or $N+1$. The output of the prescaler serves as the input of counter P and counter S. At the beginning, the prescaler divides by $N+1$. When the S counter reaches the number S, it then changes the prescaler control bit to set the prescaler division to N. The P counter continues counts until a number P is reached. Then both S and P counters are reset, and the division process is restarted. So in a complete cycle of the full divider, the prescaler has divided S times by $N+1$ and $P-S$ times by N. The overall division number becomes:

$$(N+1)\cdot S + N\cdot(P-S) = P\cdot N + S \tag{2.36}$$

If S is a variable between 0 and $N-1$, the complete range of division numbers

can realized. For proper reset by the P counter, P must be larger than the largest value of S. Usually the prescaler is implemented by source coupled logic (SCL) while the P and S counter are implemented by CMOS logic.

2.5.2.2 A Multi-Modulus Divider

The dual-modulus prescaler can be extended to realize multi modulus prescalers that are capable of frequency division over a large, contiguous range. The asynchronous $\div 2$ sections of the dual modulus prescaler are replaced with $\div 2/3$ dividers. The programmable multi-modulus prescaler is depicted in Fig. 2.19. The modular structure consists of a chain of $\div 2/3$ divider cells connected like a ripple counter.

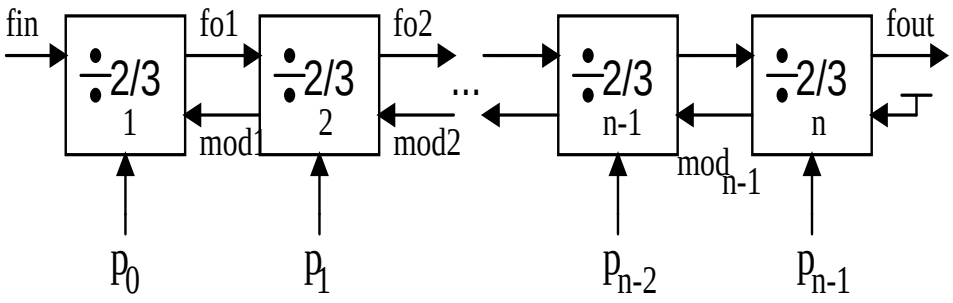


Figure 2.19: A multi-modulus prescaler

The programmable prescaler operates as follows. In a division period, the last cell on the chain generates the signal mod_{n-1}. This signal then propagates "up" the chain, being reclocked by each cell along the way. An active *mod* signal enables a cell to divide by 3 in a division cycle, provided that its programming input p is set to 1. If the programming input is set to 0 then the cell keeps on dividing by

2. Despite the state of the p input, the *mod* signal is reclocked and output towards the higher frequency cells. Division by 3 adds one extra period of each cell's input signal to the period of the output signal. Hence a chain of n $\div 2/3$ dividers provides a division ratio in a complete cycle as:

$$2^n + 2^{n-1} \cdot p_{n-1} + 2^{n-2} \cdot p_{n-2} + \cdots + 2 \cdot p_1 + p_0 \tag{2.37}$$

Where p_0, p_1, $\cdots$, p_{n-1} are the binary programming values of the cells 1 to n, respectively. The equation shows that this design increases the range of divide values to all integers between 2^n and $2^{n+1} - 1$.

2.5.2.3 Logic Implementation of the Prescaler Cells

The dual-modulus and multi-modulus prescalers are made of $\div 2$ and/or $\div 2/3$ dividers. In this section, we will give the logic implementation of these $\div 2/3$ dividers.

A. $\div 2/3$ Divider for the Two-Modulus Prescaler

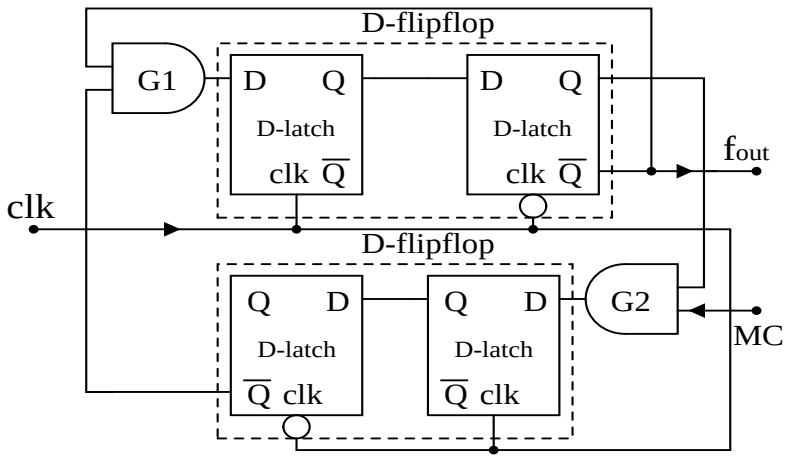


Figure 2.20: The logic implementation of $\div 2/3$ divider for the dual-modulus prescaler

Figure 2.20 shows the logic implementation of ÷2/3 divider for the two-modulus prescaler. It is made of two D-flipflops and two AND gates. When the control signal MC=0, the first flipflop is isolated from the second one. Therefore, the divider has only one state variable Q1 and divides by two. When MC=1, there are two state variables, Q1 and Q2, and divides by three.

B. ÷2/3 Divider for the Multi-Modulus Prescaler

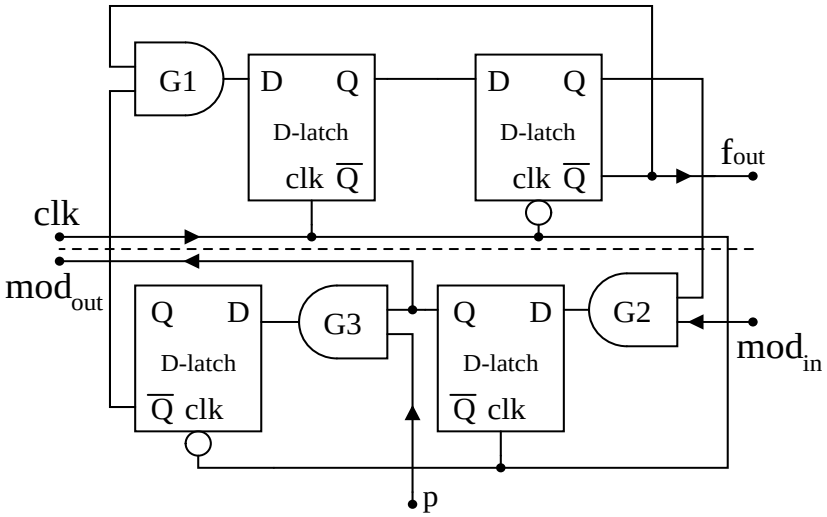


Figure 2.21: The logic implementation of ÷2/3 divider for the multi-modulus prescaler

The ÷2/3 dividers used in the multi-modulus prescaler is similar to that used in the dual-modulus prescaler, except that there is one more AND gate ($G3$) added, as shown in Fig. 2.21. The frequency of the input signal *clk* either is divided by 2 or by 3, upon control of the mod_{in} and p signals. The divided clock signal is output to the next ÷2/3 cell in the chain. The mod_{in} signal becomes active once in a division

cycle. At that moment, the state of the p input is checked, and if $p = 1$, the cell divides by 3. If $p = 0$, the divider stays in $\div 2$ mode. From Fig. 2.21, we can see the bottom part reclocks the mod_{in} signal, and outputs it to the preceding cell in the chain of the multi-modulus prescaler.

2.5.3 Phase Frequency Detector and Charge Pump [26], [28]

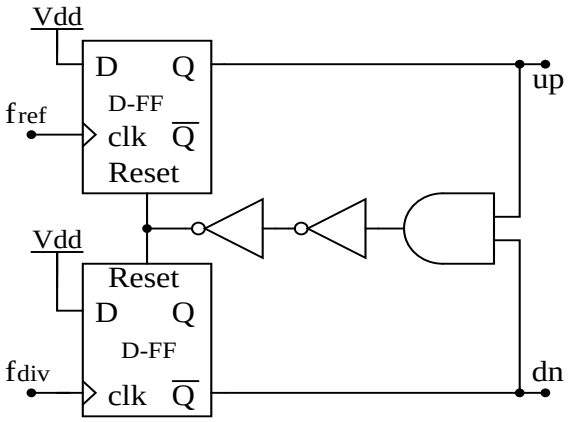


Figure 2.22: The block diagram of phase frequency detector

Figure 2.22 shows the block diagram of the phase frequency detector. The two D-flipflops are falling edge-triggered and their D input is connected to Vdd. The clock of the upper D-flipflop is connected to the reference frequency, f_{ref}, and the lower D-flipflop is clocked with the output of the frequency divider, f_{div}. If the falling edge of f_{ref} arrives before the falling edge of f_{div}, output up is set to speed up the VCO. On the other hand, if the falling edge of f_{div} arrives prior to the falling edge of f_{ref} that means the VCO frequency is faster than the reference frequency and dn is set to slow down the VCO. In either condition the falling edge of the late signal activates the AND gate and two inverters to reset both up and dn. The next

cycle starts with the next falling edge of f_{ref} or f_{div}.

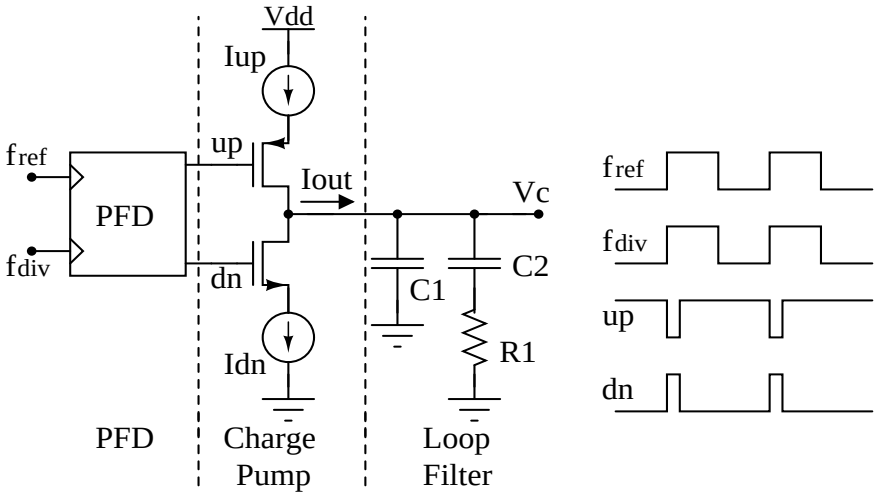


Figure 2.23: Periodic disturbance of VCO control line due to charge pump activity

A charge pump generally consists of two current sources that are switched on and off at the proper instances in time, as shown in Fig. 2.7 and Fig. 2.23. In order to avoid the dead-zone problem [26], the PFD outputs *up* and *dn* produce a narrow pulse at every phase comparison instant even if the input phase difference is zero. In the ideal case, the two pulses would have identical and opposite shapes, and the gate-drain overlap capacitance of $SW1$ and $SW2$ would be equal, resulting in complete cancellation of the feedthrough of the pulses to the charge pump output. In practice, neither of these is true. The non-idealities of a charge pump cause the reference spur on the VCO output. We will give the detailed explanation in section 3.5.1.

Chapter 3

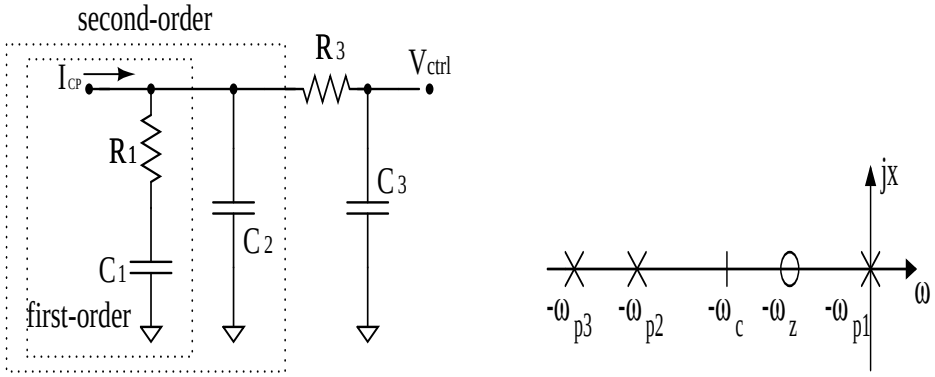
Analysis of PLL Frequency Synthesizer

In this chapter, the analysis of the PLL frequency synthesizer is presented. First, a linearized frequency domain model is analyzed according to PLL order in section 3.1. The PLL parameter effects on PLL loop bandwidth and stability are characterized. Various noise sources in a PLL are identified and their contributions to the closed loop overall phase noise are derived in section 3.2. Then a design-oriented phase noise model for complementary cross-coupled-VCO is developed in section 3.3, based on some literature analysis results in [51] and [52]. With the VCO noise model, we theoretically analyze phase noise for both narrow band and wide band VCOs. To confirm the proposed VCO phase noise model, a complementary cross-coupled LC VCO is designed. The effects of the charge pump non-idealities to reference spur are analyzed, and a new charge pump circuit is designed in section 3.5. Finally, the influence of $\Sigma\Delta$ modulators on the spectral purity of the fractional-N frequency synthesizer is investigated, and the PLL frequency synthesizer phase noise due to a $\Sigma\Delta$ modulator block is derived in section 3.6.

3.1 Linear PLL Model Analysis

The linear model for a charge pump PLL is shown in Fig. 2.8. In this section, we will analyze in detail the linear model according to the PLL order. The order of

the PLL is the number poles of the loop filter plus one due to the fundamental pole of the VCO.



(a) (b)

Figure 3.1: A third-order passive loop filter for a charge-pump PLL: (a) Schematic, (b) The transimpedance pole-zero plot

Figure 3.1(a) shows a passive third-order loop filter for a charge pump PLL. C_1 produces the first pole at the origin for the type-II PLL [26]. Together with C_1, R_1 is used to generate a zero for the loop stability. C_2 is used to smooth the control voltage ripples and to generate the second pole ω_{p2}. R_3 and C_3 are used to generate the third pole ω_{p3} to further suppress reference spurs and the high-frequency noise in $\Sigma\Delta$-PLLs. The transimpedance (V_{ctrl}/I_{cp}) of the third-order passive loop filter is:

$$\begin{aligned} Z_{lf}(s) &= \frac{1}{s(C_1+C_2+C_3)} \cdot \frac{1+sR_1C_1}{1+s\dfrac{R_1C_1(C_2+C_3)+R_3C_3(C_1+C_2)}{C_1+C_2+C_3}+s^2\dfrac{R_1R_3C_1C_2C_3}{C_1+C_2+C_3}} \\ &= \frac{1}{s(C_1+C_2+C_3)} \cdot \frac{1+s/\omega_z}{(1+s/\omega_{p2})(1+s/\omega_{p3})} \end{aligned} \tag{3.1}$$

The pole-zero location of the third-order loop filter's transimpedance are illustrated in Fig. 3.1(b). In the following subsections, The second order PLL is introduced first. Based on the second order PLL, we will analyze third- and fourth-order PLLs.

3.1.1 Second Order PLL [25], [26]

For the first order loop filter outlined in Fig. 3.1(a), its impedance is:

$$Z_{lf}(s) = R_1 + \frac{1}{sC_1} = R_1\frac{1+sR_1C_1}{sR_1C_1} = R_1\frac{\omega_z + s}{s} \tag{3.2}$$

Where $\omega_z = 1/(R_1C_1)$ is the zero for the loop stability. The pole is located in the origin, $\omega_{p1} = 0$. From Fig. 2.8, the PLL open loop gain is:

$$G_{2nd}(s) = \frac{K_{pd}K_{vco}R_1}{Ns}\cdot\frac{1+sR_1C_1}{sR_1C_1} = K\cdot\frac{1+sR_1C_1}{s^2R_1C_1} \tag{3.3}$$

where

$$K = \frac{K_{pd}K_{vco}R_1}{N} \tag{3.4}$$

When $|G_{2nd}(j\omega_c)| = 1$, we get the open loop bandwidth as:

$$\omega_c = \sqrt{\frac{K^2 + K\sqrt{K^2+4\omega_z^2}}{2}} \tag{3.5}$$

And the phase margin is $\phi_m = \tan^{-1}(\frac{\omega_c}{\omega_z})$. The second order PLL is always stable [26]. With the open loop gain function, the the closed-loop gain of the second-order PLL is:

$$\begin{aligned} H_{2nd}(s) &= N\cdot\frac{K(s+\omega_z)}{s^2+Ks+K\omega_z} \\ &= N\cdot\frac{2\zeta\omega_n s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \end{aligned} \tag{3.6}$$

where $\zeta = \frac{1}{2}(\sqrt{\frac{K}{\omega_c}})$ is the damping factor, and $\omega_n = \sqrt{K\omega_z}$ is the undamped natural frequency. The step response for this system in the time domain can be written as [26]:

$$y(t) = \begin{cases} N \cdot \left[1 - e^{-\zeta\omega_n t}\left(\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right)\right] & 0 < \zeta < 1 \\ N \cdot \left[1 - e^{-\omega_n t}(1-\omega_n t)\right] & \zeta = 1 \\ N \cdot \left[1 - e^{-\zeta\omega_n t}\left(\cosh(\omega_n t\sqrt{\zeta^2-1}) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh(\omega_n t\sqrt{\zeta^2-1})\right)\right] & \zeta > 1 \end{cases} \tag{3.7}$$

Now we suppose at time zero ($t = 0$), the divider modulus changes from N to $N + k$, and $k \ll N$. The output frequency is then equal to:

$$\begin{aligned} F_{out}(s) &= \frac{G_{2nd}(s)}{1 + \frac{G_{2nd}(s)}{N+k}} \cdot F_{in}(s) \approx \frac{G_{2nd}(s)}{1 + \frac{1}{N}G_{2nd}(s)} \cdot (1 + \frac{k}{N})F_{in}(s) \\ &= H_{2nd}(s) \cdot (1 + \frac{k}{N})F_{in}(s) \end{aligned} \tag{3.8}$$

The term $(1 + \frac{k}{N})F_{in}$ can be viewed as a step change in the reference frequency from f_{ref} to $f_{ref}(1 + \frac{k}{N})$. According to Eq. (3.7), we have:

$$f_{out}(t) = \begin{cases} \left[1 - e^{-\zeta\omega_n t}\left(\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right)\right](N+k)f_{ref} & \\ & 0 < \zeta < 1 \\ \left[1 - e^{-\omega_n t}(1-\omega_n t)\right](N+k)f_{ref} & \zeta = 1 \\ \left[1 - e^{-\zeta\omega_n t}\left(\cosh(\omega_n t\sqrt{\zeta^2-1}) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh(\omega_n t\sqrt{\zeta^2-1})\right)\right](N+k)f_{ref} & \\ & \zeta > 1 \end{cases} \tag{3.9}$$

Modifying Eq. (2.9) due to the normalized frequency error $\varepsilon(t)$, then the output frequency can be expressed as:

$$f_{out}(t) = (1 \pm \varepsilon(t))(N+k)f_{ref} \tag{3.10}$$

From Eq. (3.9) and (3.10), the normalized frequency error can be written as:

$$\varepsilon(t) = \begin{cases} e^{-\zeta\omega_n t}\left(\cos\left(\omega_n t\sqrt{1-\zeta^2}\right) - \frac{\zeta}{\sqrt{1-\zeta^2}}\sin\left(\omega_n t\sqrt{1-\zeta^2}\right)\right) & 0 < \zeta < 1 \\ e^{-\omega_n t}(1-\omega_n t) & \zeta = 1 \\ e^{-\zeta\omega_n t}\left(\cosh(\omega_n t\sqrt{\zeta^2-1}) - \frac{\zeta}{\sqrt{\zeta^2-1}}\sinh(\omega_n t\sqrt{\zeta^2-1})\right) & \zeta > 1 \end{cases} \tag{3.11}$$

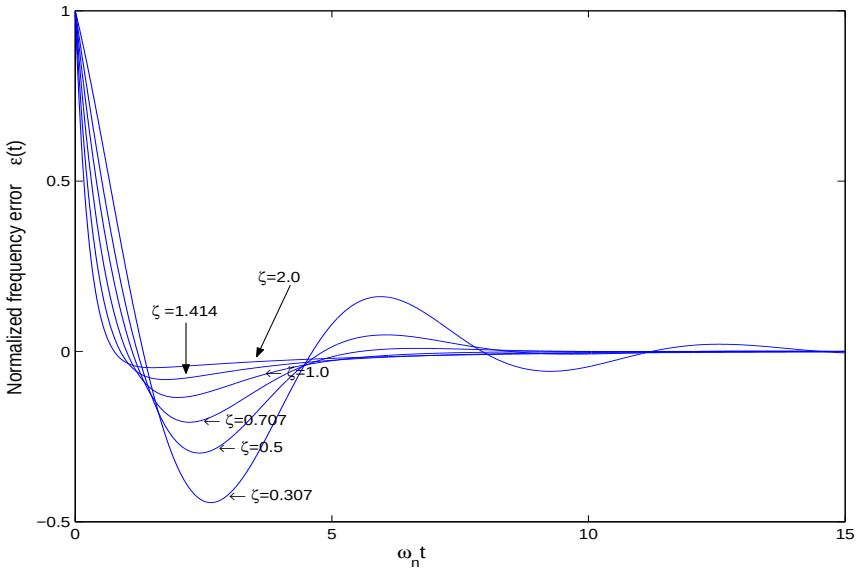


Figure 3.2: Second order PLL frequency error varying with settling time and damping factor

From Eq. (3.11), the normalized frequency error $\varepsilon(t)$ changes with the normalized settling time $\omega_n t$ and the damping factor ζ is shown in Fig. 3.2. It is under-damped for $0 < \zeta < 1$, critically-damped for $\zeta = 1$, and over-damped for $\zeta > 1$.

The second order PLL has only R_1 and C_1 making up the loop filter. Its control voltage has big ripples. So the second order PLL is not used in practice, leading to the third or fourth order PLLs being used in practice.

3.1.2 Third Order PLL

The additional pole of a third order PLL provides more spurious suppression. However, the extra lag associated with the pole introduces a stability issue. Thus the loop filter must be designed carefully to provide the required filtering while maintaining loop stability.

For the second-order passive loop filter as shown in Fig. 3.1(a), the transimpedance is:

$$Z_{lf}(s) = R_1 \frac{1 + sR_1C_1}{sR_1(C_1 + C_2) + s^2R_1C_1R_1C_2} = R_1 \frac{1 + s/\omega_z}{s(1 + s/\omega_{p2})/\omega_z} \cdot \frac{b-1}{b} \tag{3.12}$$

where $b = 1 + C_1/C_2$, and the second pole is:

$$\omega_{p2} = \frac{1}{R_1 \frac{C_1C_2}{C_1+C_2}} = b\omega_z \tag{3.13}$$

According to Eq. (3.4), the open loop gain is:

$$G_{3rd}(s) = K \cdot \frac{1 + s/\omega_z}{s^2(1 + s/\omega_{p2})/\omega_z} \cdot \frac{b-1}{b} \tag{3.14}$$

The open-loop phase-margin is:

$$\phi_m = \phi_z - \phi_{p2} = \tan^{-1}(\frac{\omega_c}{\omega_z}) - \tan^{-1}(\frac{\omega_c}{\omega_{p2}}) \tag{3.15}$$

For the maximum phase margin by differentiating Eq. (3.15), we have

$$\omega_c = \sqrt{\omega_{p2}\omega_z} = \omega_z\sqrt{b} \tag{3.16}$$

Substitute Eq. (3.16) to Eq. (3.15), then the maximum phase margin is

$$\phi_m = \tan^{-1}\sqrt{\frac{\omega_{p2}}{\omega_z}} - \tan^{-1}\sqrt{\frac{\omega_z}{\omega_p 2}} = \tan^{-1}\frac{b-1}{2\sqrt{b}} \tag{3.17}$$

The maximum phase margin is exclusively determined by the capacitor ratio b. Figure 3.3 shows the maximum phase margin as a function of $b = 1 + C_1/C_2$ in a third order PLL.

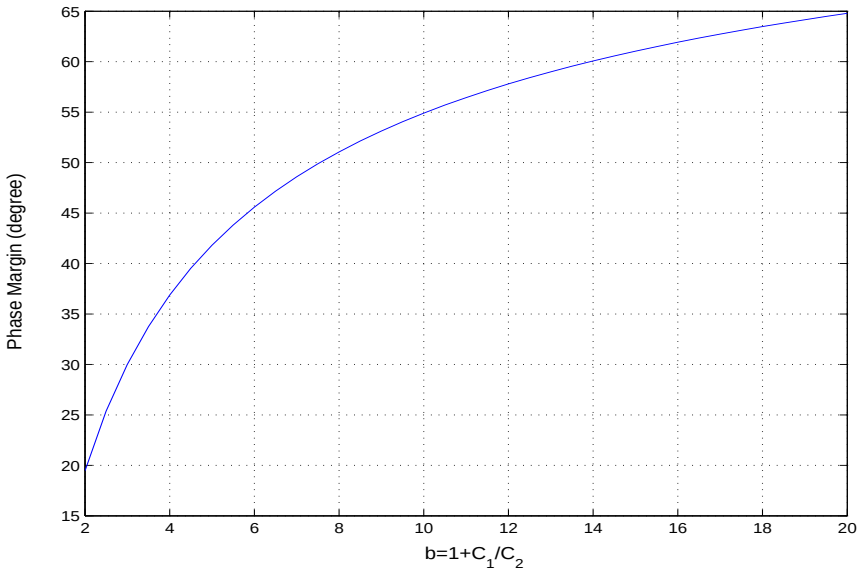


Figure 3.3: Maximum phase margin varying with $b = 1 + C_1/C_2$ in a 3rd-order PLL

Usually $C_1 \gg C_2$. With the maximum phase margin and Eq. (3.14), the PLL open loop bandwidth is simplified as:

$$\omega_c = K \cdot \frac{b-1}{b} = K \cdot \frac{C_1}{C_1 + C_2} \approx K \tag{3.18}$$

From Eq. (3.14), the third order PLL closed-loop function is:

$$H_{3rd}(s) = N \cdot \frac{1 + s/\omega_z}{1 + s/\omega_z + s^2/(\omega_z\omega_c) + s^3/(\omega_z\omega_c\omega_{p2})} \tag{3.19}$$

When the loop bandwidth is chosen for maximum phase margin, by using Eq. (3.13) and Eq. (3.16), Eq. (3.19) becomes:

$$H_{3rd}(s) \quad = \quad N \cdot \frac{\omega_c^3 + \sqrt{b}\omega_c^2 s}{(s + \omega_c)[s^2 + (\sqrt{b} - 1)\omega_c s + \omega_c^2]}$$

$$= \quad N \cdot \frac{(2\zeta+1)\omega_n^2 s + \omega_n^3}{(s+\omega_n)(s^2+2\zeta\omega_n s+\omega_n^2)} \tag{3.20}$$

where $\zeta = (\sqrt{b}-1)/2$ is the damping factor and $\omega_n = \omega_c$ is the natural frequency.

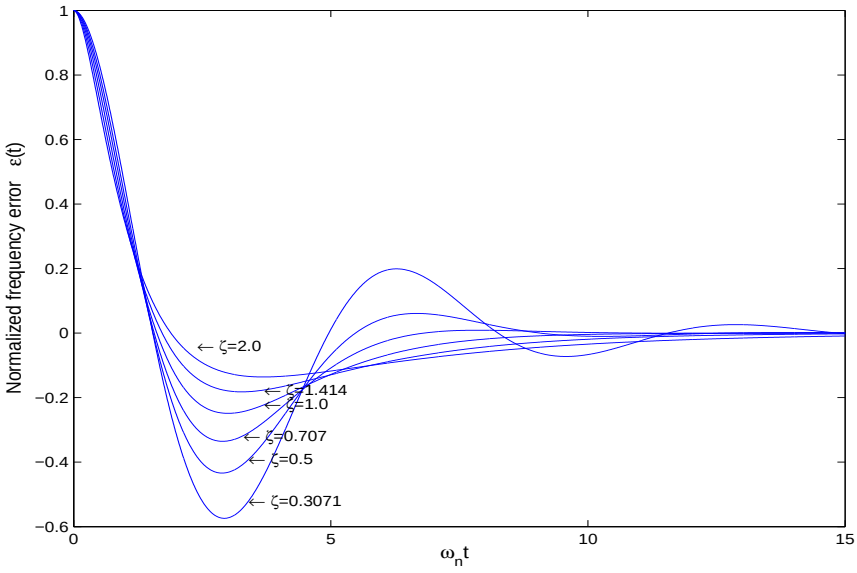


Figure 3.4: Third order PLL frequency error varying with the settling time and damping factor

From Eq. (3.8), (3.10), and (3.20), the normalized frequency error of a third order charge-pump PLL is derived as:

$$\varepsilon(t) = \begin{cases} \frac{1}{\zeta-1}\left(\zeta e^{-\omega_n t} - e^{-\zeta\omega_n t}\cos(\omega_n t\sqrt{1-\zeta^2})\right) & 0<\zeta<1 \\ e^{-\omega_n t}\left(1+\omega_n t-\omega_n^2 t\right) & \zeta = 1 \\ \frac{1}{\zeta-1}\left(\zeta e^{-\omega_n t} - e^{-\omega_n t}cosh(\omega_n t\sqrt{\zeta^2-1})\right) & \zeta > 1 \end{cases} \tag{3.21}$$

Figure 3.4 shows the normalized frequency change with the normalized settling time and damping factor. For the third-order PLL, ω_n and ζ can be mapped to ω_c and ϕ_m. So, according to Eq. (3.21), the locking time, which is normalized by a factor of ω_c, is plotted against ϕ_m with different relative frequency error ($\varepsilon = 10^{-3}$, 10^{-4}, and 10^{-5}) is shown in Fig. 3.5.

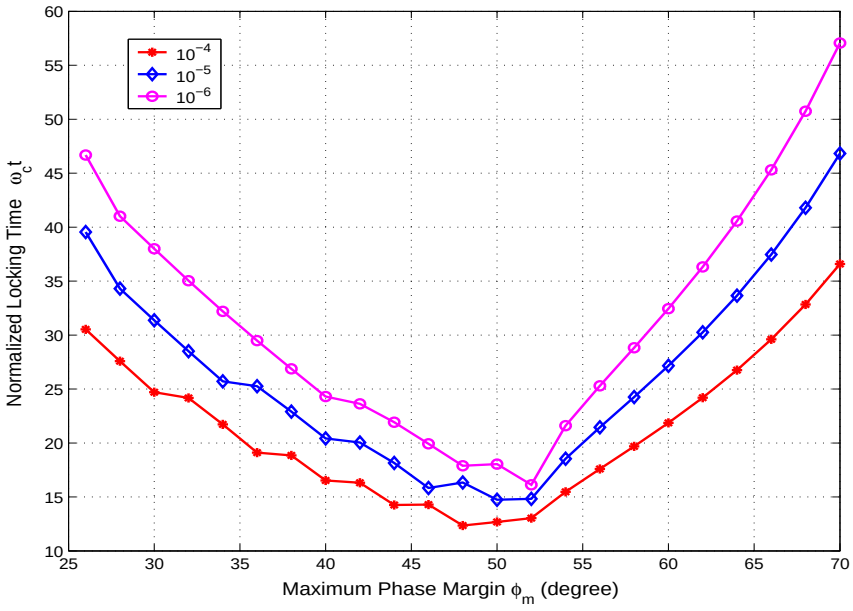


Figure 3.5: Third order PLL locking time varying with phase margin

In a third order PLL, the combination of the phase margin and loop bandwidth defines the characteristics of the loop. To further reduce the spur without decreasing the loop bandwidth and hence increasing the settling time, an additional pole needs to be added to the loop. This additional pole increases the PLL order to four.

3.1.3 Fourth Order PLL

For the third-order passive loop filter in Fig. 3.1(a), the transimpedance is given in Eq. (3.1). We rewrite it here:

$$\begin{aligned} Z_{lf}(s) &= \frac{1}{s(C_1+C_2+C_3)} \cdot \frac{1+sR_1C_1}{1+s\dfrac{R_1C_1(C_2+C_3)+R_3C_3(C_1+C_2)}{C_1+C_2+C_3}+s^2\dfrac{R_1R_3C_1C_2C_3}{C_1+C_2+C_3}} \\ &= \frac{1}{s(C_1+C_2+C_3)} \cdot \frac{1+s/\omega_z}{(1+s/\omega_{p2})(1+s/\omega_{p3})} \end{aligned} \tag{3.22}$$

Here we define $\omega_{p2} = b\omega_z$, and $\omega_{p3} = k\omega_{p2}$. Usually, $C_1 \gg C_2$, $C_1 \gg C_3$ and $R_1 > R_3$. The two non-zero poles can be written:

$$\omega_{p2} = b\omega_z \approx \frac{1}{R_1(C_2 + C_3)} \tag{3.23}$$

$$\omega_{p3} = k\omega_{p2} = kb\omega_z \approx \frac{(C_2 + C_3)}{R_3 C_2 C_3} \tag{3.24}$$

The open loop gain is:

$$G_{4th}(s) = K \cdot \frac{C_1}{C_1 + C_2 + C_3} \cdot \frac{1 + s/\omega_z}{s^2/\omega_z(1 + s/\omega_{p2})(1 + s/\omega_{p3})} \tag{3.25}$$

The open-loop phase margin is:

$$\phi_m = \phi_z - \phi_{p2} - \phi_{p3} = \tan^{-1}(\frac{\omega_c}{\omega_z}) - \tan^{-1}(\frac{\omega_c}{\omega_{p2}}) - \tan^{-1}(\frac{\omega_c}{\omega_{p3}}) \tag{3.26}$$

For the maximum phase margin by differentiating Eq. (3.26), we have

$$\frac{1/\omega_z}{1 + (\omega_c/\omega_z)^2} = \frac{1/\omega_{p2}}{1 + (\omega_c/\omega_{p2})^2} + \frac{1/\omega_{p3}}{1 + (\omega_c/\omega_{p3})^2} \tag{3.27}$$

Substitute $\omega_{p2} = b\omega_z$ and $\omega_{p3} = k\omega_{p2}$, Eq. (3.27) becomes

$$\frac{1}{\omega_c^2 + \omega_z^2} = \frac{b}{\omega_c^2 + b^2\omega_z^2} + \frac{kb}{\omega_c^2 + k^2 b^2 \omega_z^2} \tag{3.28}$$

From Eq. (3.28), we get

$$A\omega_c^4 + B\omega_z^2\omega_c^2 + C\omega_z^4 = 0 \tag{3.29}$$

Where $A = 1 - b - kb$, $B = -(k^2 + k)b^3 + (1 + k^2)b^2 - (1 + k)b$, and $C = kb^3(kb - k - 1)$.

Solving Eq. (3.29), we get

$$\omega_c = \sqrt{-\frac{B}{2} + \frac{\sqrt{B^2 - 4AC}}{2A}} \cdot \omega_z \tag{3.30}$$

let

$$D = \sqrt{-\frac{B}{2} + \frac{\sqrt{B^2 - 4AC}}{2A}} \tag{3.31}$$

then $\omega_c = D \cdot \omega_z$. Now, the maximum phase margin is:

$$\phi_m = \tan^{-1}(D) - \tan^{-1}(\frac{D}{b}) - \tan^{-1}(\frac{D}{kb}) \tag{3.32}$$

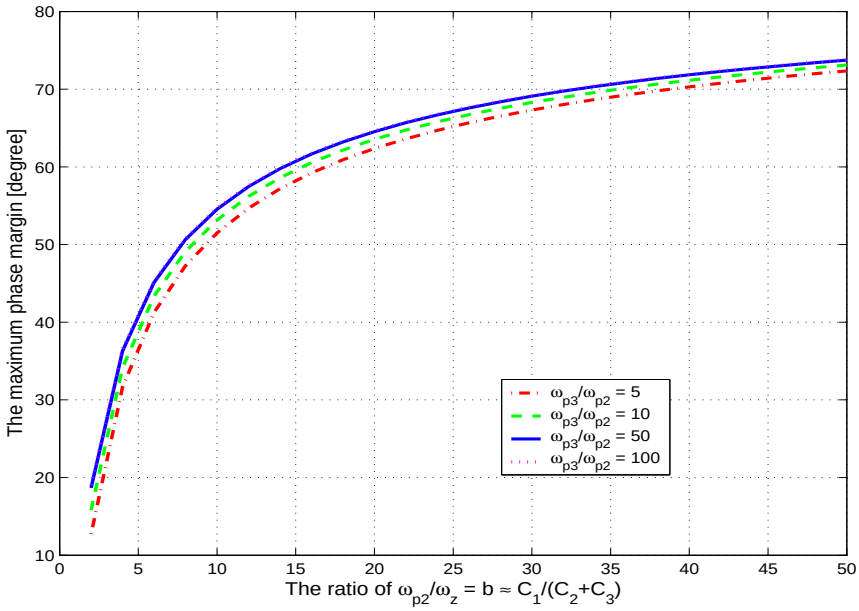


Figure 3.6: Maximum phase margin varying with the ratio $b = \frac{\omega_{p2}}{\omega_z}$, and $k = \frac{\omega_{p3}}{\omega_{p2}}$ in a 4th-order PLL

Figure 3.6 shows the maximaum phase margin as a function of $b = \omega_{p2}/\omega_z$ and $k = \omega_p 3/\omega_p 2$ in a fourth order PLL. From this figure, we can see when the ratio of ω_{p3} to ω_{p2} is larger than 10, the ratio has little influence on the maximum phase margin. Then, the PLL system can be simplified as a third order PLL.

When the frequency is equal to the loop bandwidth ω_c, $|G_{4th}(j\omega_c)| = 1$. Equa-

tion (3.25) becomes:

$$K \cdot \frac{C_1}{C_1 + C_2 + C_3} \cdot \frac{\sqrt{1 + (\frac{1}{D})^2}}{\omega_c \cdot \sqrt{1 + (\frac{D}{b})^2} \cdot \sqrt{1 + (\frac{D}{bk})^2}} = 1 \tag{3.33}$$

Let

$$E = \frac{\sqrt{1 + (\frac{D}{b})^2} \cdot \sqrt{1 + (\frac{D}{bk})^2}}{\sqrt{1 + (\frac{1}{D})^2}} \tag{3.34}$$

then from Eq. (3.33)

$$K \cdot \frac{C_1}{C_1 + C_2 + C_3} = E \cdot \omega_c. \tag{3.35}$$

With the maximum phase margin, the open loop gain of Eq. (3.25) can be written:

$$G_{4th}(s) = E \cdot \omega_c \cdot \frac{1 + s/\omega_z}{s^2/\omega_z(1 + s/\omega_{p2})(1 + s/\omega_{p3})} \tag{3.36}$$

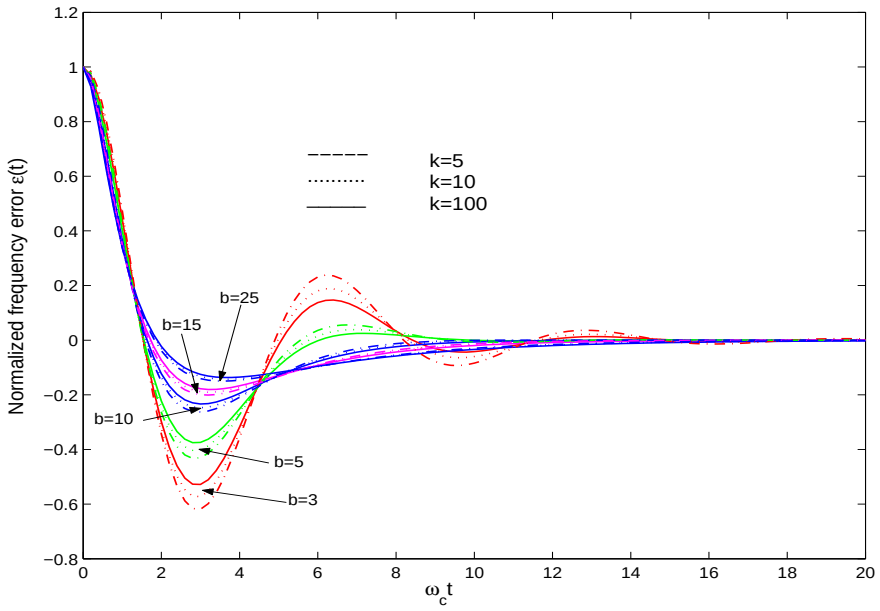


Figure 3.7: Fourth order PLL frequency error varying with settling time, the ratio $b = \frac{\omega_{p2}}{\omega_z}$, and $k = \frac{\omega_{p3}}{\omega_{p2}}$

Then the closed loop gain with the maximum phase margin can be expressed as:

$$H_{4th}(s) = \frac{N \cdot (1 + s/\omega_z)}{1 + s/\omega_z + s^2/(\omega_z\omega_c E) + s^3(1/(\omega_{p2}\omega_z\omega_c E) + 1/(\omega_{p3}\omega_z\omega_c E)) + s^4/(\omega_{p2}\omega_{p3}\omega_z\omega_c E)} \tag{3.37}$$

Substitute $\omega_z = \frac{\omega_c}{D}$, $\omega_{p2} = \frac{b}{D} \cdot \omega_c$, and $\omega_{p3} = \frac{bk}{D} \cdot \omega_c$, Eq. (3.37) becomes

$$H_{4th}(s) = N \cdot \omega_c^3 \cdot \frac{b^2 kE}{D^2} \cdot \frac{s + \dfrac{\omega_c}{D}}{s^4 + s^3(1+k)\dfrac{b}{D}\omega_c + s^2\dfrac{b^2k}{D^2}\omega_c^2 + s\dfrac{b^2kE}{D^2}\omega_c^3 + \dfrac{b^2kE}{D^3}\omega_c^4} \tag{3.38}$$

If we know b and k, we can calculate the value of D and E. With Eq. (3.8), (3.10) and (3.38), the normalized frequency error of a fourth-order PLL system can be calculated by **Matlab**. The normalized frequency error of a fourth-order charge-pump PLL is shown in Fig. 3.7.

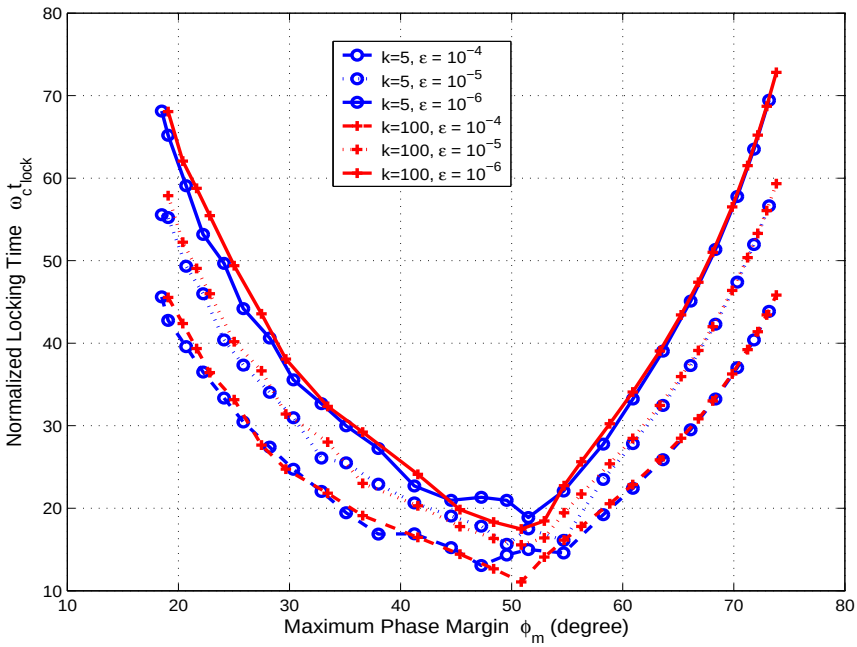


Figure 3.8: Fourth order PLL locking time varying with phase margin

According to Eq. (3.32), the phase margin ϕ_m can be calculated with known b and k. And according to Eq. (3.8), (3.10) and (3.38), the normalized locking time ($\omega_c t_{lock}$) can be calculated with known b, k, D, E, and frequency error ϵ. The normalized locking time of a fourth-order PLL, is plotted against ϕ_m with different relative frequency error ($\epsilon = 10^{-3}$, 10^{-4}, and 10^{-5}) and the ratio $k = \omega_{p3}/\omega_{p2}$ as shown in Fig. 3.8.

Higher order PLLs are rarely used because the phase margin is reduced with more poles. We do not analyze them in this dissertation.

3.2 Noise in Phase-locked loops

The noise model of charge pump PLL synthesizer is shown in Fig. 3.9. The noise sources can represent either the noise created by the blocks due to intrinsic noise sources (thermal, shot, and flicker noise sources), or the noise coupled into the blocks from external sources, such as from power supplies, the substrate, etc. For the reference, the divider and the VCO block, only phase noise is sensed at the point where the noise is injected. Those noise are denoted as $\phi_{ref,n}$, $\phi_{div,n}$, $\phi_{vco,n}$. On the other hand, current noise $i_{cp,n}$ is sensed for PFD/CP, and voltage noise $v_{lpf,n}$ is for the low pass filter. In addition, for an integer-N PLL we further model the divider phase noise by the prescaler phase noise $\phi_{pres,n}$, and the low frequency divider phase noise $\phi_{counter,n}$. The low frequency divider is made of a program counter and a swallow counter as shown in Fig. 3.9.

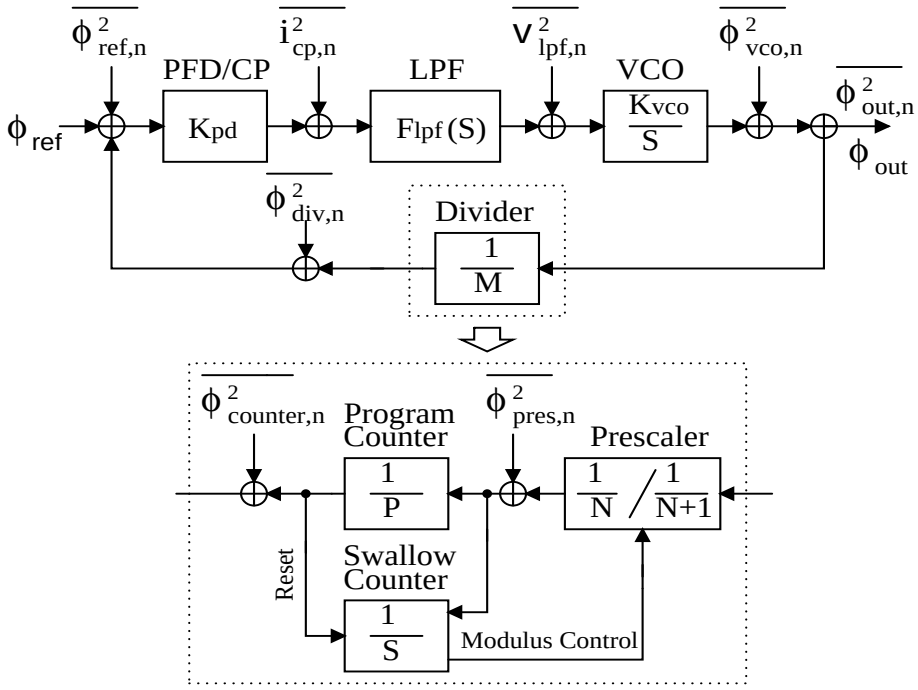


Figure 3.9: The noise model of a charge pump PLL

According to Fig. 2.8 and Eq. (2.10), the transfer function from the various noise sources to the PLL output noise can be expressed as follows.

$$\frac{\phi_{out,ref}(s)}{\phi_{ref,n}(s)} = N \cdot \frac{G(s)}{1+G(s)} = \frac{NK_{pd}K_{vco}F_{lpf}(s)}{Ns + K_{pd}K_{vco}F_{lpf}(s)} \tag{3.39}$$

$$\frac{\phi_{out,cp}(s)}{i_{cp,n}(s)} = \frac{N}{K_{pd}} \cdot \frac{G(s)}{1+G(s)} = \frac{NK_{vco}F_{lpf}(s)}{Ns + K_{pd}K_{vco}F_{lpf}(s)} \tag{3.40}$$

$$\frac{\phi_{out,lpf}(s)}{v_{lpf,n}(s)} = \frac{K_{vco}}{s} \cdot \frac{1}{1+G(s)} = \frac{K_{vco}}{s(Ns + K_{pd}K_{vco}F_{lpf}(s))} \tag{3.41}$$

$$\frac{\phi_{out,vco}(s)}{\phi_{vco,n}(s)} = \frac{1}{1+G(s)} = \frac{1}{Ns + K_{pd}K_{vco}F_{lpf}(s)} \tag{3.42}$$

$$\frac{\phi_{out,div}(s)}{\phi_{div,n}(s)} = -N \cdot \frac{G(s)}{1+G(s)} = \frac{-NK_{pd}K_{vco}F_{lpf}(s)}{Ns + K_{pd}K_{vco}F_{lpf}(s)} \tag{3.43}$$

where $\phi_{out,ref}$, $\phi_{out,cp}$, $\phi_{out,lpf}$, $\phi_{out,vco}$, and $\phi_{out,div}$ are the PLL output phase noise caused by the reference, the PFD/CP, the low pass filter, the VCO, and the divider, respectively. $K_{pd} = I_{cp}/2\pi$ is the gain of the phase frequency detector.

Because $F_{lpf}(s)$ is a low pass filter, we can get that the transfer functions

$\frac{\phi_{out,ref}(s)}{\phi_{ref,n}(s)}$, $\frac{\phi_{out,cp}(s)}{i_{cp,n}(s)}$, and $\frac{\phi_{out,div}(s)}{\phi_{div,n}(s)}$ are low pass filters with a gain of N at frequencies below the loop bandwidth. This means the noise contributions from the reference, PFD/CP, and divider are referred to the output enhanced in effect by N at low offset frequencies from the carrier, and suppressed at high offset frequencies from the carrier. The transfer function $\frac{\phi_{out,vco}(s)}{\phi_{vco,n}(s)}$ is a high pass filter. This means that the noise from the VCO at lower frequencies can be corrected by the relatively fast PLL. But at high frequencies, the loop is not fast enough and is essentially an open loop. The transfer function $\frac{\phi_{out,lpf}(s)}{v_{lpf,n}(s)}$ is a band pass filter. Therefore, at low frequencies the noise of the PLL is contributed by input, PFD/CP, LPF, divider, and VCO, but the noise from the VCO is diminished by the gain of the loop. At high frequencies, the main noise of the PLL is that of the VCO.

The reference and loop filter are usually made from off-chip discrete components. Their noise can be easily modelled with good accuracy. The noise from PFD/CP, divider, and VCO are more difficult to predict for their on chip implementation. The total PLL phase noise can be expressed as:

$$\begin{aligned}\overline{\phi^2_{out,n}(s)} &= \overline{\phi^2_{out,ref}(s)} + \overline{\phi^2_{out,pfd/cp}(s)} + \\ &\quad \overline{\phi^2_{out,lpf}(s)} + \overline{\phi^2_{out,vco}(s)} + \overline{\phi^2_{out,div}(s)} \end{aligned} \tag{3.44}$$

where $\overline{\phi^2_{out,ref}(s)}$, $\overline{\phi^2_{out,pfd/cp}(s)}$, $\overline{\phi^2_{out,lpf}(s)}$, $\overline{\phi^2_{out,vco}(s)}$, and $\overline{\phi^2_{out,div}(s)}$ are noise power spectral densities of reference, PFD/CP, LPF, VCO, and divider, respectively.

With the system level analysis, we will give our theoretical analysis for each PLL block in the following parts of this chapter.

3.3 CMOS LC VCOs

The voltage controlled oscillator (VCO) and the prescaler operate at the highest frequency of a frequency synthesizer. However, the VCO is more critical since the phase noise of the VCO determines the out of band noise of the synthesizer. The VCO performance in terms of phase noise and tuning range determines basic performance characteristics of a transceiver. The current trend toward multiband multistand transceivers and broadband systems has generated interest in VCOs that simultaneously achieve very wide tuning range and low phase noise performance [60]-[62].

With a given loop bandwidth ω_c, from Eq. (3.16) and Eq. (3.35) we have the following equations for PLL loop with a second order and third order low pass filter, respectively.

$$\omega_c = \frac{K_{pd}K_{vco}}{N} \cdot \frac{R_1 C_1}{C_1 + C_2} \tag{3.45}$$

$$\omega_c = \frac{K_{pd}K_{vco}}{N} \cdot \frac{R_1 C_1}{C_1 + C_2 + C_3} \cdot \frac{1}{E} \tag{3.46}$$

Where R_1, R_2, C_1, C_2, and C_3 are LPF parameters. E can be found with the given R_1, R_2, C_1, C_2, and C_3 in Eq. (3.34). From Eq. (3.45) and Eq. (3.46), we get that the product of $K_{pd}K_{vco}$ is constant for fixed LPF parameters. With the same loop filter parameters and divider number, Eq. (3.40) and Eq. (3.41) are proportional to K_{vco}. The relations also can be described as [63]:

$$\overline{\phi^2_{out,pfd/cp}} \propto I_{cp} \cdot (K_{vco})^2 \propto K_{vco} \tag{3.47}$$

$$\overline{\phi^2_{out,lpf}} \propto K^2_{vco} \tag{3.48}$$

So by decreasing K_{vco}, the PLL output noise due to the PFD/CP and LPF contributions is dramatically decreased. That results in an overall PLL phase noise decrease. Moreover, for a practical PLL, the noise from the preceding stages of the frequency synthesizer inevitably injected into the VCO control input, therefore the lower K_{vco} is very critical for the PLL output phase noise.

For a wideband VCO design, a single varactor device with a steep C-V characteristic can be used to achieve a wide frequency range and typically has sufficiently high Q as that it does not degrade the phase noise performance of the VCO. But this design can result in an excessively high VCO gain K_{vco}. So, a wideband VCO must properly limit the overall VCO gain.

In section 3.3.1, a design-oriented phase noise model is presented that takes into account the non-linearity of the active element. Based on the VCO phase noise model, we will analyze phase noise for both narrowband and wideband VCOs by using the circuit parameters in section 3.3.2. To confirm the VCO phase noise model, a basic complementary cross-coupled LC VCO is designed in section 3.3.3. Our goal is to design a widband VCO, so we will theoretically analyze the switched-capacitor wide range tuning method and discuss VCO constant output level control scheme in sections 3.3.4 and 3.3.5, respectively.

3.3.1 A Model for a Complementary Cross-coupled LC VCO Phase Noise Analysis

In Kong's [51] and Rael&Abidi's [52], the LC VCO phase noise model are provided. But these two models focus on the single cross-coupled LC VCO. As we stated before, we use a complementary cross-coupled LC VCO in our design. Improving on the literature results in [51] and [52], we provide a phase noise model for the complementary cross-coupled LC VCO in this section.

Figure 3.10 shows the noise sources in the complementary oscillator. From this figure, we can see thermal noise sources in LC oscillators are from tank, differential pairs and current tail.

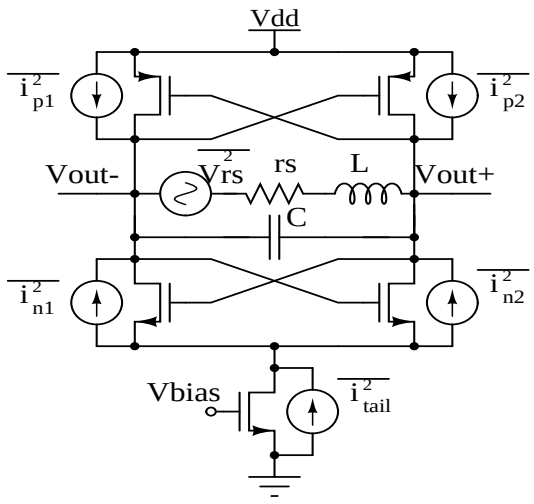


Figure 3.10: Complementary LC oscillator with noise sources

A. Phase Noise from the Tank

Phase noise from the tank (inductor and varactors) can be obtained from the

calculation in section 2.5.1 in Lesson's Model [49]:

$$Z(j\omega) = -jR_p \frac{\omega_0}{2Q\Delta\omega} \tag{3.49}$$

$$L\{\Delta\omega\} = \frac{4kTR_p}{A_0^2} \cdot (\frac{\omega_0}{2Q\Delta\omega})^2 \tag{3.50}$$

Where A_0 is the differential output voltage peak amplitude (V_{out+}/V_{out-}). Owing to filtering in the LC circuit, a square wave of current creates a sinusoidal voltage across the resonator. The peak amplitude A_0 in the current limited regime (in this operation regime, the output voltage peak amplitude increases as the tail current increases [44]) can be written as:

$$A_0 = \frac{4}{\pi} I_B R_p \tag{3.51}$$

where I_B is the bias current. The voltage drives the differential pairs into switching and thus sustains the oscillation.

B. Phase Noise from the Differential Pairs

From Fig. 3.10, we can see there are 4 noise sources of 4 differential pair transistors, $\overline{i_n^2} = \overline{i_{n1}^2} = \overline{i_{n2}^2}$, and $\overline{i_p^2} = \overline{i_{p1}^2} = \overline{i_{p2}^2}$. The transistor noise densities are $\overline{i_n^2}/\Delta f = 4kT\gamma g_{mn}$ and $\overline{i_p^2}/\Delta f = 4kT\gamma g_{mp}$. Where γ is around 2/3 for a long channel device, and is between 2 to 3 for a short channel device [47]. And, g_{mn} and g_{mp} are transconductances for nMOS and pMOS transistors, respectively. For a simple stationary model, the total differential noise power due to the four cross-coupled transistors can be written as:

$$\overline{i_{o,n}^2}/\Delta f = \frac{1}{4}(\overline{i_{n1}^2} + \overline{i_{n2}^2} + \overline{i_{p1}^2} + \overline{i_{p2}^2})/\Delta f = \frac{1}{2}(\overline{i_n^2} + \overline{i_p^2})/\Delta f = 4kT\gamma(\frac{g_{mn} + g_{mp}}{2}) \tag{3.52}$$

The phase noise due to differential pair transistors is

$$L\{\Delta\omega\} = \frac{\overline{i_{o,n}^2} \cdot |Z(j(\omega_0 + \Delta\omega))|^2}{A_0^2/2} = \frac{4kT\gamma R_p^2}{A_0^2}(g_{mn} + g_{mp})(\frac{\omega_0}{2Q\Delta\omega})^2 \tag{3.53}$$

Actually, the noise from the differential pair transistors is not stationary. The output noise is white and cyclostationary because of the periodic changes in currents and voltage of the active devices [44]. We use a similar method for the mixer noise model in [64] for our VCO phase noise calculation. In [64], the power spectral density of the output current noise due to one switch transistor is:

$$\overline{i_{o,n}^2}/\Delta f = 4kT\gamma\frac{I_B}{\pi A_0} \tag{3.54}$$

So, the phase noise due to four differential pair transistors is

$$L\{\Delta\omega\} = 4 \cdot \frac{\overline{i_n^2}/\Delta f \cdot |Z(\omega_0 + \Delta\omega)|}{A_0^2/2} = \frac{32kT\gamma R_p^2}{\pi A_0^3}(\frac{\omega_0}{2Q\Delta\omega})^2 \tag{3.55}$$

C. Phase Noise from the Tail Current

The switching differential pairs commutate and upconvert low-noise frequencies into two correlated AM sidebands around the fundamental. But noise frequencies around the second harmonic downconvert close to the oscillation frequency, and upconvert to around the third harmonic, where they are rejected by the bandpass characteristic of the LC tank. For noise injected at $2\omega_0 \pm \omega_m$, we can see

$$\cos\omega_0 t \cdot \cos(2\omega_0 \pm \omega_m)t = \frac{1}{2}(\cos(\omega_0 \pm \omega_m)t + \cos(3\omega_0 \pm \omega_m)t)$$

The downconvered noise is decomposed into half AM and half PM sidebands around the oscillation frequency ω_0. We know the bias transistor current noise is $\overline{i_{n,tail}^2}/\Delta f = 4kT\gamma_{bias} \cdot g_{m,bias}$. From Eq. 3.49, we have the tank impedance. So

according to Eq. (3.51) we get that the output noise $\overline{v_{o,n}^2}$ due to the bias current noise is:

$$\overline{v_{o,n}^2}/\Delta f = \left(\frac{4}{\pi}\right)^2 \cdot \overline{i_{n,tail}^2}/\Delta f \cdot |Z(j(\omega_0+\Delta\omega))|^2 = \left(\frac{4}{\pi}\right)^2 \cdot 4kT\gamma_{bias} g_{m,bias} \cdot R_p^2 (\frac{\omega_0}{2Q\Delta\omega})^2 \tag{3.56}$$

Then, the phase noise due to the tail transistor noise is:

$$L\{\Delta\omega\} = \frac{\overline{v_{out}^2}/\Delta f}{\frac{1}{2}A_0^2} = \frac{128kT\gamma_{bias} g_{m,bias} R_p^2}{\pi^2 A_0^2} \cdot (\frac{\omega_0}{2Q\Delta\omega})^2 \tag{3.57}$$

By adding Eq. (3.50), (3.53), and (3.57), we get that the total phase noise of the LC oscillator by the simple stationary model is:

$$L\{\Delta\omega\} = \frac{\overline{v_{out}^2}/\Delta f}{\frac{1}{2}A_0^2} = \frac{4kTR_p}{A_0^2} \cdot (\frac{\omega_0}{2Q\Delta\omega})^2 \cdot (1 + R_p\gamma(g_{mn}+g_{mp}) + \frac{128}{\pi^2} R_p \gamma_{bias} g_{m,bias}) \tag{3.58}$$

By adding Eq. (3.50), (3.55), and (3.57), we get the total phase noise of this LC oscillator by the cyclostationary model is:

$$L\{\Delta\omega\} = \frac{\overline{v_{out}^2}/\Delta f}{\frac{1}{2}A_0^2} = \frac{4kTR_p}{A_0^2} \cdot (\frac{\omega_0}{2Q\Delta\omega})^2 \cdot (1 + \frac{8I_B R_p \gamma}{\pi A_0} + \frac{128}{\pi^2} R_p \gamma_{bias} g_{m,bias}) \tag{3.59}$$

In the equation of Leeson's model, Eq. (2.29), the total excess output noise factor F is an unspecified noise factor. In our equation, the factor F of the complementary cross-coupled differential oscillator can be derived from Eq. (3.58) or Eq. (3.59) by comparing with Eq. (2.29).

In our simple stationary model, the F is:

$$F = 1 + R_p\gamma(g_{mn}+g_{mp}) + \frac{128}{\pi^2} R_p \gamma_{bias} g_{m,bias} \tag{3.60}$$

While in our cyclostationary model, the F is:

$$F = 1 + \frac{8I_B R_p \gamma}{\pi A_0} + \frac{128}{\pi^2} R_p \gamma_{bias} g_{m,bias} \tag{3.61}$$

In the next section, we will use our phase noise model to analyze phase noise in the narrowband and wideband VCOs.

3.3.2 Phase Noise Analysis for the Narrowband and Wideband VCOs

For the differential cross-coupled LC oscillator shown in Fig. 2.17, its working area is separated into two operational regimes in [44]. In the current-limited regime, the tail current I_B is periodically commutated between the left and right sides of the tank. Thus, the resulting fundamental amplitude is directly proportional to I_B and R_p, where higher harmonics of the commutated current are attenuated by the bandpass profile of the LC tank. As I_B is increased from its minimum value satisfying start-up conditions, the tank amplitude increases linearly. Eventually, the amplitude saturates and the oscillator enters the voltage-limited regime. Operating an oscillator in the voltage-limited regime is generally undesirable because the added power consumption no longer increases the amplitude and is thus recognized as a waste of power [44]. We will analyze phase noise in the two operating regimes.

To gain insight into the VCO phase noise, we consider the simplified case of a generic complementary cross-coupled LC oscillator in Fig. 2.17(b). Using the simple phase noise model, Equation (3.58) can be re-arranged as:

$$L\{\Delta\omega\} = kT \cdot \frac{R_p^2}{A_0^2 \cdot Q^2} \cdot (\frac{\omega_0}{\Delta\omega})^2 \cdot (1/R_p + \gamma(g_{mn} + g_{mp}) + \frac{128}{\pi^2}\gamma_{bias} g_{m,bias}) \quad (3.62)$$

In the current-limited regime, g_{mn}, g_{mp}, and $g_{m,bias}$ are proportional to $\sqrt{I_B}$. Applying Eq. (3.51), Eq. (3.62) can be written as:

$$L\{\Delta\omega\} = kT \cdot \frac{1}{I_B^2} \cdot \frac{1}{Q^2} \cdot (\frac{\omega_0}{\Delta\omega})^2 \cdot \left\{1/R_p + \left[\left(\sqrt{\frac{2}{V_{ov,nmos}}} + \sqrt{\frac{2}{V_{ov,pmos}}}\right)\gamma\right.\right.$$

$$+\frac{128}{\pi^2}\gamma_{bias}\sqrt{\frac{2}{V_{ov,tail}}}\Bigg]\sqrt{I_B}\Bigg\} \tag{3.63}$$

For narrowband design, R_p does not vary appreciably over the tuning range and thus $(g_{mn}+g_{mp}) \propto \sqrt{I_B}$ is chosen to satisfy the start-up condition as we have explained in section 2.5.1.2. Under these conditions, the phase noise shows a $1/Q^2$ dependence. Due to the importance of Q, a careful optimization should consider Q as a function of L for the chosen technology and area constraints, as discussed in [65], [66]. Eq. (3.63) also shows the direct relationship between the bias current and phase noise.

In the voltage-limited regime, A_0 is saturated and expressed by $A_{o,max}$, and Eq. (3.62) can be written as:

$$L\{\Delta\omega\} = kT \cdot \frac{R_p^2}{A_{0,max}^2 \cdot Q^2} \cdot (\frac{\omega_0}{\Delta\omega})^2 \cdot \Big[1/R_p + \gamma(g_{mn}+g_{mp}) + \frac{128}{\pi^2}\gamma_{bias}g_{m,bias}\Big] \tag{3.64}$$

due to the excessive signal amplitude bringing the transconductor into its resistive region, which degrades the overall tank quality factor Q. In a narrowband design where the voltage-limited regime is reached by increasing I_B, Eq. (3.64) indicates that the phase noise must degrade since the amplitude saturates to $A_{0,max}$ while the transconductance g_{mn}, g_{mp} and $g_{m,bias}$ ($\propto \sqrt{I_B}$) keeps rising. So the boundary between the two operational regimes represents the optimum point for achieving lowest phase noise. Increasing I_B beyond this point not only wastes power, but also degrades the phase noise.

The above analysis focuses on narrowband design. In order to evaluate similar characteristics for wideband VCOs, frequency dependence must be taken into account. Here, we begin our analysis of the current-limited regime. From Eq. (3.62),

a phase noise to its frequency dependence is derived assuming a fixed current I_B,

$$L\{\Delta\omega\} = kT \cdot \frac{1}{I_B^2} \cdot \frac{r_s^2}{(\omega_0 L)^2} \cdot (\frac{\omega_0}{\Delta\omega})^2 \cdot \left[\frac{r_s}{(\omega_0 L)^2} + \left(\left(\sqrt{\frac{2}{V_{ov,nmos}}} + \sqrt{\frac{2}{V_{ov,pmos}}} \right) \gamma + \frac{128}{\pi^2} \gamma_{bias} \sqrt{\frac{2}{V_{ov,tail}}} \right) \sqrt{I_B} \right] \quad (3.65)$$

Equation (3.65) reveals that phase noise tends to improve as frequency ω_0 increases. Even in cases where r_s grows linearly with frequency. The phase noise does not degrade with the rising ω_0 because the tank amplitude in this topology grows with ω_0^2. However, wideband designs operated with fixed I_B experience significant amplitude growth as frequency increases, which eventually brings the VCO into the voltage-limited regime where phase noise is known to degrade.

We know $R_p/Q = \omega_0 L$. In the voltage-limited regime, Eq. (3.62) can be written as:

$$L\{\Delta\omega\} = kT \cdot \frac{1}{A_{0,max}^2} \cdot (\frac{\omega_0}{\Delta\omega})^2 \cdot \left[r_s + (\omega_0 L)^2 (\gamma(g_{mn} + g_{mp}) + \frac{128}{\pi^2} \gamma_{bias} g_{m,bias}) \right] \quad (3.66)$$

Equation (3.66) furthermore explains that the phase noise increases as the frequency increases.

3.3.3 A Complementary Cross-coupled VCO Design

Because inductors are very important components in LC VCO design, we will discuss the inductor design next. With inductors, a complementary cross-coupled LC VCO is designed to verify the proposed phase noise model in section 3.3.1.

3.3.3.1 Inductors

On-chip inductors for LC VCOs have been widely investigated in the literature [67]-[71]. The mostly used approach is the spiral inductor made of the metal track available in the standard digital CMOS process. A spiral inductor can be made of a single metal layer or multiple metal layers. The multi-layer series spiral inductor has been used due to its smaller chip area compared with the single layer spiral inductor. The substrate coupling effect is alleviated with smaller chip area. And sometimes it is used to reduce the series resistance of metal tracks. On the other hand for the single metal layer inductor design, the top metal is used because it is the furthest metal layer from the conductive substrate and is the thickest metal layer. The large distance to the substrate reduces the magnetic coupling with the conductive substrate. The top metal layer has the smallest resistance due to its thickness. These two factors help increase the quality (Q) factor of spiral inductors.

In our design, we choose the single layer inductor implementation. Because our LC VCO uses the cross-coupled differential pair architecture, the differential inductor structure is chosen. A differential inductor offers higher quality factor than two independent spirals in series. The differential spiral inductor layout is shown in Fig. 3.11. From this figure, the most obvious benefit for using a differential inductor is that the area of only one single inductor is needed. The common-mode impedance is reduced by the strong coupling between the windings, so common-mode noise is significantly reduced. Many differential LC oscillators use two separate inductors [3], [72]. This can lead to an increased noise, because noise components

from the substrate can not be considered as common-mode noise due to the large distance between the inductors. The strong coupling between the windings of the differential inductor enhances signal symmetry, and this can in turn improve flicker noise, because flicker noise caused by the oscillator nonlinearity is reduce by the symmetry [50].

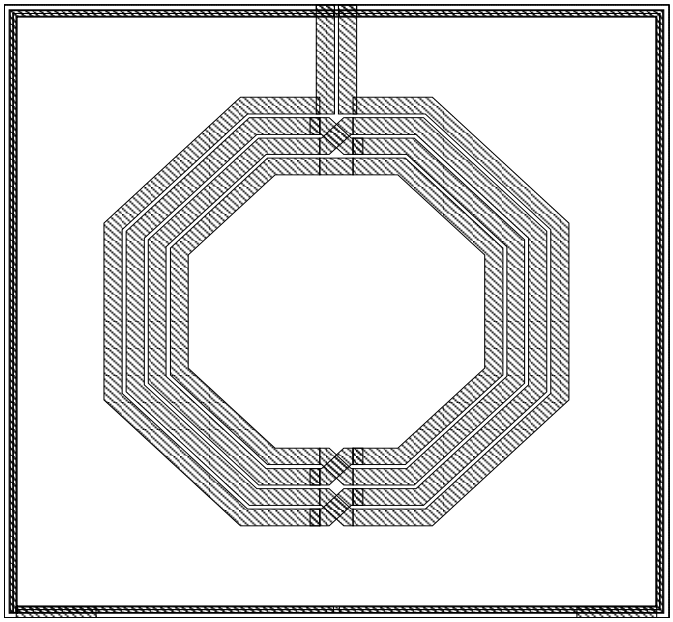
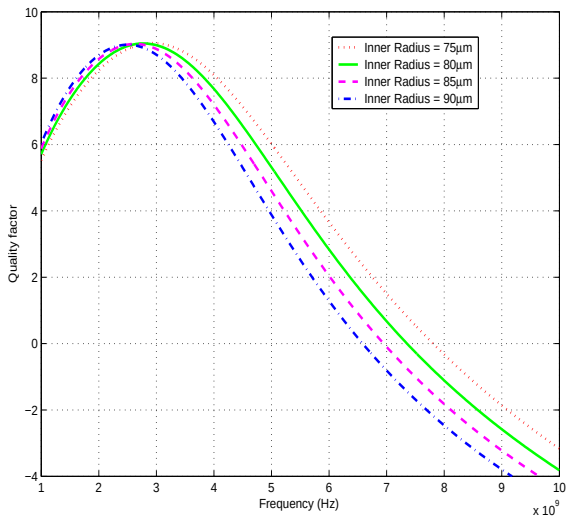
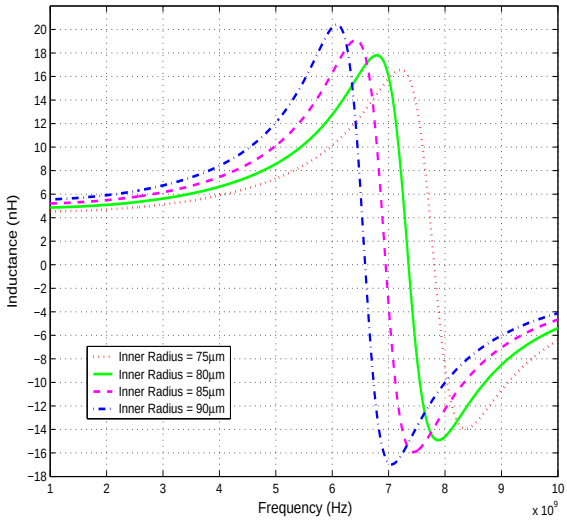


Figure 3.11: An octagonal differential inductor

As an example, the spiral inductor is built with the top metal ($Metal$ 6) tracks in TSMC0.18μm process. The thickness of $Metal$ 6 is 4.6μm. We choose two groups of inductors for simulation. One group has the metal-width as 9μm, and another group has the metal-width as 15μm. The simulated quality factor value Q and inductance L for the two groups are shown in Fig. 3.12 and Fig. 3.13, respectively. From the two group figures, we can see that the group with metal-width=15μm has a little higher Q values than those of the other group because wider metal provides

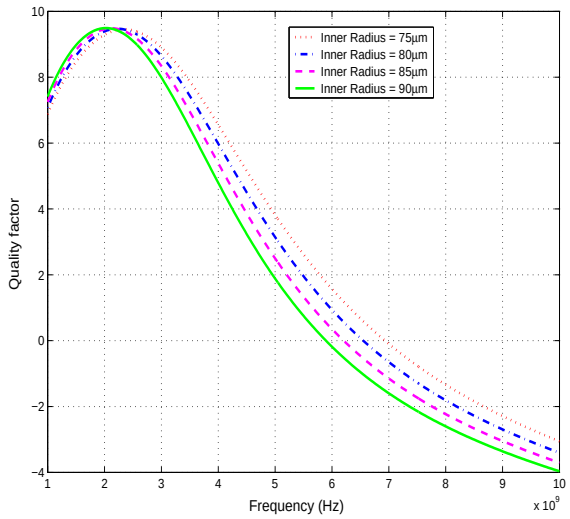


(a)

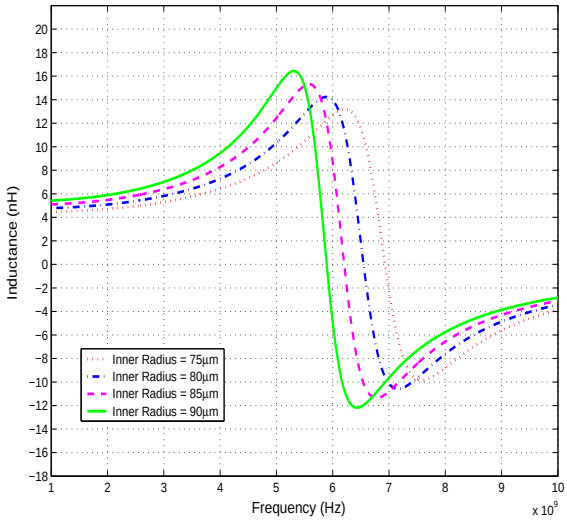


(b)

Figure 3.12: The symmetric inductor for metal-width=9μm, and metal-space=2μm: (a) Quality value, (b) Inductance



(a)



(b)

Figure 3.13: The symmetric inductor for metal-width=15μm, and metal-space=2μm: (a) Quality value, (b) Inductance

smaller resistance r_s. According to Eq. (2.23), the Q values increases as r_s decreases. However, wider metal also means larger inductance [73], as seen from Fig. 3.12(a) and Fig. 3.13(a).

3.3.3.2 A VCO Design

To confirm the phase noise model presented in section 3.3, we implement a basic complementary cross-coupled LC VCO (Fig. 2.17(b)) design in this section.

The complementary cross-coupled VCO has two main advantages compared with NMOS transistors only cross-coupled topology. First, with the additional PMOS pair, the complementary topology offers higher transconductance to compensate for the loss of the tank with less current consumption. It is more power efficient. Second, matching the PMOS and NMOS transistors, the complementary topology provides better symmetry properties of the oscillating waveform, which decreases the upconversion of $1/f$ of devices to the $1/f^3$ noise region [48], [50]. The supply voltage is 3.3V. For low power consumption and low phase noise design, we set $I_B = 2.2mA$.

From the phase noise model of Eq. (3.59), it is clear that the quality factor should be large for a good phase noise performance design. With the given quality factor, the inductance value will determine the phase noise. If we do not care about power consumption, a smaller inductor is better at the price of large current. But under a power consumption constraint, a larger inductor will be better for a given bias current. However according to Eq. (2.21), a larger inductor will reduce the

tuning range. So the differential inductor we choose has the design parameters shown in table 3.1.

Metal	Metal Width/Space	Inner Radius	Turns	Q	L	r_s
Metal6	15μm/2μm	90μm	4	9.5	5.01nH	7.8Ω

Table 3.1: Design parameters of an inductor in a complementary cross-coupled LC VCO

The tank equivalent parallel resistance $R_p = Q^2 \cdot r_s = 703\Omega$. So, the tank transconductance $g_{m,tank} \geq \frac{1}{R_p} = 1.42mS$ to meet the startup condition. If we set the startup coefficient $\alpha = 3.5$ [47]. Then the total transconductance of one NMOS and one PMOS should be $g_m = g_{mn} + g_{mp} = \alpha \cdot (2g_{m,tank}) = 9.94mS$. To reduce 1/f noise up-conversion [50], we choose $g_{mn} = g_{mp} = 4.97mS$. From these parameters and 0.18um CMOS technology parameters, $\mu_n \approx 400cm^2/VS$, $\mu_p \approx 130cm^2/VS$, and $C_{ox} \approx 5.08F/m^2$, when transistors work in saturation we get

$$\left(\frac{W}{L}\right)_n = \frac{g_{mn}^2}{I_B \cdot \mu_n C_{ox}} = 56 \tag{3.67}$$

$$\left(\frac{W}{L}\right)_p = \frac{g_{mp}^2}{I_B \cdot \mu_p C_{ox}} = 171 \tag{3.68}$$

With the minimum NMOS length=0.35μm and PMOS length=0.3μm, we get NMOS size as $\left(\frac{W}{L}\right)_n \approx \frac{21u}{0.35u}$ and PMOS size as $\left(\frac{W}{L}\right)_p \approx \frac{54u}{0.3u}$.

From the phase noise model, we also know that tail current source transconductance $g_{m,bias}$ and γ_{bias} should be as small as possible. To limit short-channel induced excess noise, the minimum length has to be avoided. For smaller $g_{m,bias}$, we will choose larger length and smaller width for the current source transistor. However, to keep the tail current transistor working in the saturation region, the

overdrive voltage of the tail transistor should be small. That results in a larger $g_{m,bias}$ when the tail current is fixed. For compromise, we choose the current bias transistor size as $W/L = 250/2$. Then the overdrive voltage $V_{ov,bias}$ is 0.43V, and the transconductance $g_{m,bias} = \dfrac{2I_B}{V_{ov,bias}} = 10.16mS$.

From Eq. (3.51), the differential output amplitude

$$A_0 = \frac{4}{\pi} I_B R_p = 1.97V \tag{3.69}$$

According to the phase noise model Eq. (3.59), with oscillation frequency $f_0 = 2GHz$ the phase noise at 1MHz offset frequency can be written as:

$$\begin{aligned} L\{1MHz\} &= \frac{kTR_p}{A_0^2 \cdot Q^2} \cdot \left(1 + \frac{8I_B R_p \gamma}{\pi A_0} + \frac{128}{\pi^2} R_p \gamma_{bias} g_{m,bias}\right) \cdot \left(\frac{2 \times 10^9}{10^6}\right)^2 \\ &= -120dBc/Hz \end{aligned} \tag{3.70}$$

In the calculation, we choose $\gamma = 2.5$ for the short channel length of the differential pair transistors, and $\gamma_{bias} = 2/3$ for the long channel length tail transistor.

The Cadence SpectreRF simulated phase noise is shown in Fig. 3.14. From the figure, we can see the phase noise is $-117dBc/Hz$ at $1MHz$ frequency offset with the oscillation frequency at $2GHz$. The phase noise simulation result is in good agreement with our analysis result in Eq. (3.70). Moreover, the simulated VCO tuning range is shown in Fig. 3.15. Its output frequency ranges from $1.871GHz$ to $2.208GHz$ when the control voltage changes from $1.2V$ to $2.7V$. The typical VCO gain K_{vco} is around $300MHz/V$.

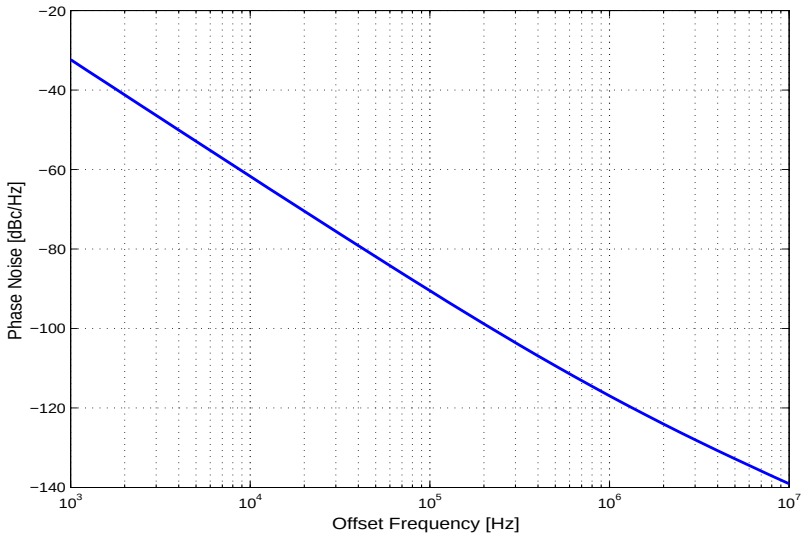


Figure 3.14: The Complementary cross-coupled LC VCO phase noise, $f_0 = 2GHz$

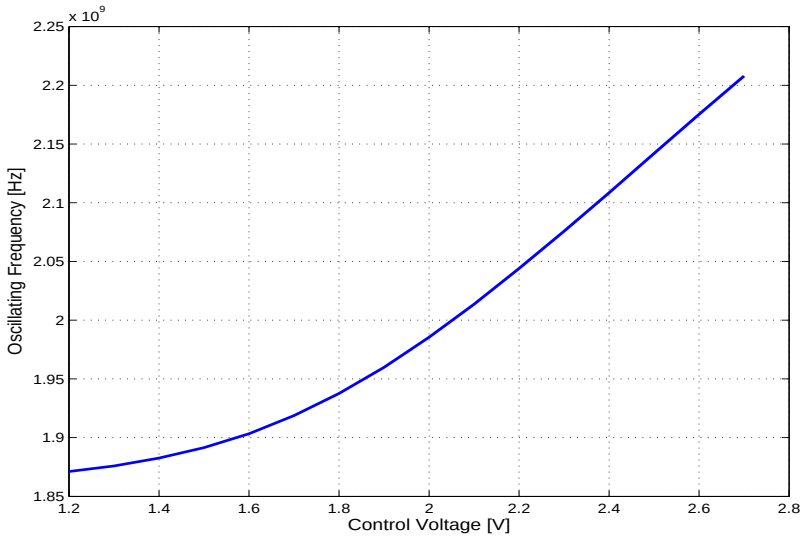
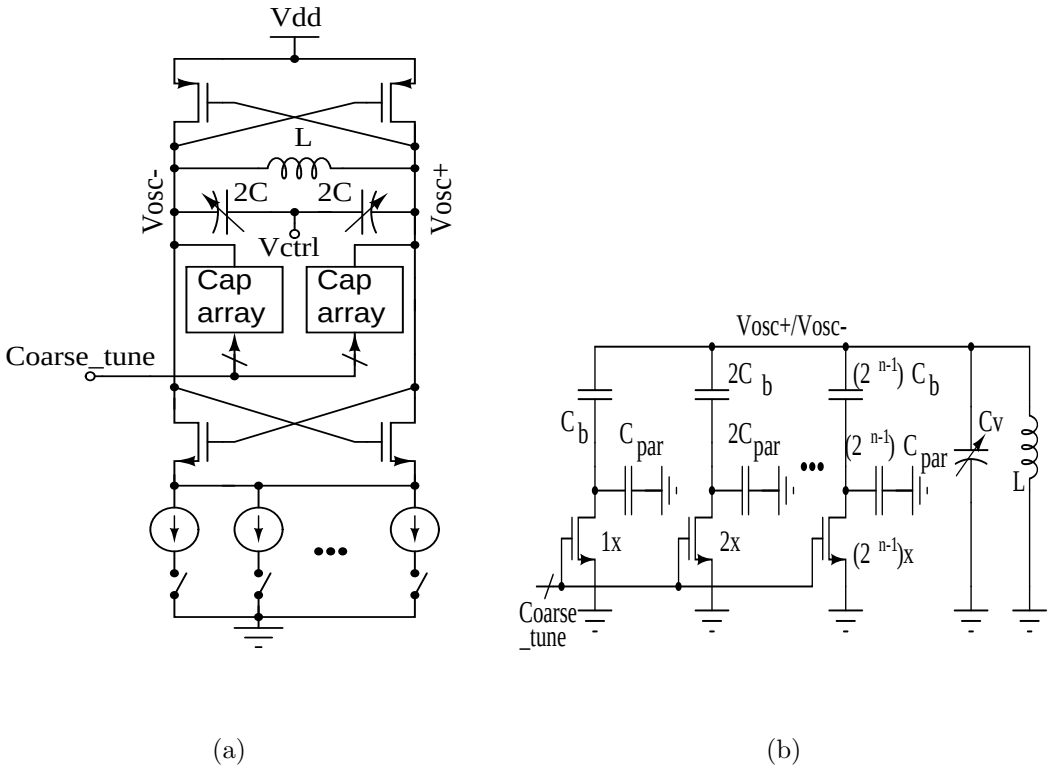


Figure 3.15: The complementary cross-coupled LC VCO tuning range

3.3.4 Wideband VCO Tuning Range Analysis

In recent years, band-switching techniques have been used extensively. These techniques have proved to be successful ways to increase tuning range and/or decrease VCO gain [61], [62].



(a) (b)

Figure 3.16: The wideband VCO: (a) The simplified VCO schematic, (b) The LC tank congifuration with the binary-weighted switched-capacitor array

The simplified wideband VCO schematic is shown in Fig. 3.16(a), and a generic binary-weighted band-switching LC tank configuration of branch size n shown in Fig. 3.16(b). The tuning range extremities can be obtained as:

$$\omega_{o,min} = [L \cdot (C_{v,max} + (2^n - 1) \cdot C_b + C_p)]^{-1/2} \tag{3.71}$$

$$\omega_{o,max} = [L \cdot (C_{v,min} + (2^n - 1) \cdot C_{b,off} + C_p)]^{-1/2} \tag{3.72}$$

Where $C_{v,max}$ and $C_{v,min}$ are the maximum/minimum varactor capacitance for the available tuning voltage range. C_b is the unit branch capacitance, and $C_{b,off}$ represents the effective capacitance of a unit branch of the array in the off state. The MOS switch in a unit branch of the array contributes a parasitic capacitance

C_{par} that is mainly composed of its drain-to-bulk junction and drain-to-gate overlap capacitors. C_p is the total lumped parasitic capacitance.

To guarantee that any two adjacent sub-bands do not overlap, the following condition must be satisfied:

$$\Delta C_v \geq \Delta C_b \tag{3.73}$$

Where $\Delta C_v = C_{v,max} - C_{v,min}$ and $\Delta C_b = C_b - C_{b,off}$.

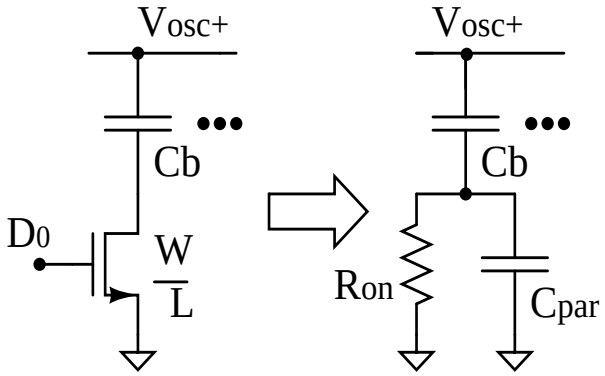


Figure 3.17: A part of switched capacitor array and its equivalent circuit

To be able to quantify the impact of lossy switches, Fig. 3.17 shows a part of a switched capacitor array and its equivalent circuit. R_{on} is the channel resistance of the unit MOS switch. From the figure, the total impedance of the equivalent circuit is:

$$\begin{aligned} Z(j\omega) &= \frac{1}{j\omega C_b} + \frac{1}{1/R_{on} + j\omega C_{par}} \\ &= \frac{R_{on}}{1 + (\omega R_{on} C_{par})^2} + \frac{1}{j\omega C_b} + \frac{\omega R^2 C_{par}}{j(1 + (\omega R_{on} C_{par})^2)} \end{aligned} \tag{3.74}$$

To avoid the LC tank Q degradation due to the switch finite channel resistance R_{on}, minimum-length MOS transistors with sufficient large size width are used. So,

$(\omega R_{on} C_{par})^2 \gg 1$. Then Eq. (3.74) can be written as:

$$Z(j\omega) = \frac{R_{on}}{1 + (\omega R_{on} C_{par})^2} + \frac{1}{j\omega C_b} + \frac{1}{j\omega C_{par}} \tag{3.75}$$

The first part is the equivalent resistance which is smaller than R_{on}. The second part and third part are equivalent two capacitor C_b and C_{par} series connected. So, only C_{par} is large enough that the total equivalent capacitance is mainly decided by the unit capacitance C_b. That means the switch size also should be large enough that C_{par} has little influence on C_b.

Moreover, we know the quality factor of an LC tank can be written as:

$$\frac{1}{Q} = \frac{1}{Q_L} + \frac{1}{Q_{var}} + \frac{1}{Q_C} \tag{3.76}$$

where Q_L, Q_{var} and Q_C are quality factors of the inductor, varactor, and switch-capacitor array, respectively. Generally the quality factor Q_{var} for the varactor can be an order of magnitude higher than Q_L. We also suppose that Q_C is much higher than Q_L [53]. Then the Q of the LC tank is primarily determined by the inductor Q_L. For the branch with C_b, its quality factor Q_C can be written as:

$$Q_C = \frac{1}{\omega_0 R_{on} C_b} = k\frac{W}{L} V_{ov} \cdot \frac{1}{\omega_0 C_b} \tag{3.77}$$

With the minimum gate length for an MOS switch, Eq. (3.77) indicates that the larger size MOS switch is needed for smaller channel resistance R_{on}, which results higher Q_C value.

From Eq. (3.75) and Eq. (3.77), larger size is necessary for MOS switches. But larger size MOS transistors bring lager off-state parasitic capacitance (for the

transistors in Fig. 3.16(b)), which will limit the tuning range. Therefore, it is very important to chose appropriate size for switches by circuit simulation.

The switched-capacitor array size n (i.e. the number of bits controlling the binary-weighted array) is also a very important design parameter for the band-switching configuration. We may expect that adding more bits to the array is beneficial to the tuning range. But actually when the size is beyond a certain number, the minimum fixed capacitance in the design prevents any further improvement to the tuning range.

3.3.5 Wideband VCO Constant Amplitude Control Scheme

The steady-state oscillation amplitude is an important design characteristic of oscillators, and can also have a significant impact on neighboring system blocks. Methods addressing this constant output amplitude typically consist of amplitude control. A conventional method of controlling the amplitude of a VCO is by means of an automatic amplitude control (AAC) loop [74], [75], where a continuous-time feedback loop provides very accurate control of the oscillation amplitude and at the same time ensures startup conditions are met. As in all feed-back systems, great care must be taken to ensure that the loop remains stable under all operating conditions. Furthermore, the presence of additional noise generators in the loop can significantly degrade the phase noise performance.

For a wideband VCO, the total tank capacitance varies over a large range as the fixed capacitors are switched in or out of the tank. That results in a wide

frequency tuning range. As the total LC tank capacitance goes from small to large, the LC oscillator frequency decreases. From Eq. (2.24), the equivalent parallel tank impedance R_p decreases too. The VCO changes from the voltage-limited regime to the current limited regime. According to Eq. (3.51), we need to increase the tail current I_B with the decreasing VCO frequency to keep the constant output swing.

According to the previous analysis, we will use an alternative amplitude control scheme to alleviate the deficiencies inherent in the conventional approach in our research. Instead of a continuous feedback loop, a calibration approach is used. The VCO amplitude is detected and compared to a reference voltage to see if the bias current needs to be adjusted by the switches shown in Fig. 3.16(a). This method has the advantage of being active only during calibration. Thus, the steady-state phase noise performance of the VCO is not affected. Furthermore, the open-loop nature of this calibration method eliminates any concerns of instability.

3.4 Frequency Divider

The divider is the main power consumption block of a PLL frequency synthesizer. The high power consumption is mainly due to the first stages (high speed part) of the frequency divider that often dissipates half of the total power. Due to the high input frequency, the high speed part of the divider can not be implemented in conventional static CMOS logic [76]. Instead, it is commonly realized in source-coupled logic (SCL), which allows higher operating frequency [77].

In this section, we will investigate the implementation aspects of a dual-

Channel number	Channel Frequency (MHz)	P-counter	S-counter	Divider Ratio	RF VCO Frequency (MHz)
1	2412	127	6	2038	2038
2	2417	127	11	2043	2043
3	2422	127	16	2048	2048
4	2427	128	5	2053	2053
5	2432	128	10	2058	2058
6	2437	128	15	20363	2063
7	2442	128	20	2068	2068
8	2447	128	25	2073	2073
9	2452	128	30	2078	2078
10	2457	128	35	2083	2083
11	2462	128	40	2088	2088
12	2467	128	45	2093	2093
13	2472	128	50	2098	2098
14	2484	128	62	2110	2110

Table 3.2: Configuration of P counter and S counter for a IEEE 802.11b/g frequency synthesizer, where $N = 16$ in $\div N/N + 1$

modulus divider in the TSMC 0.18μm CMOS process. SCL is used in the high speed part of dividers to lower power consumption. In our application, the IEEE 802.11b/g frequency divider is designed.

3.4.1 A Dual-Modulus Frequency Divider for IEEE 802.11b/g

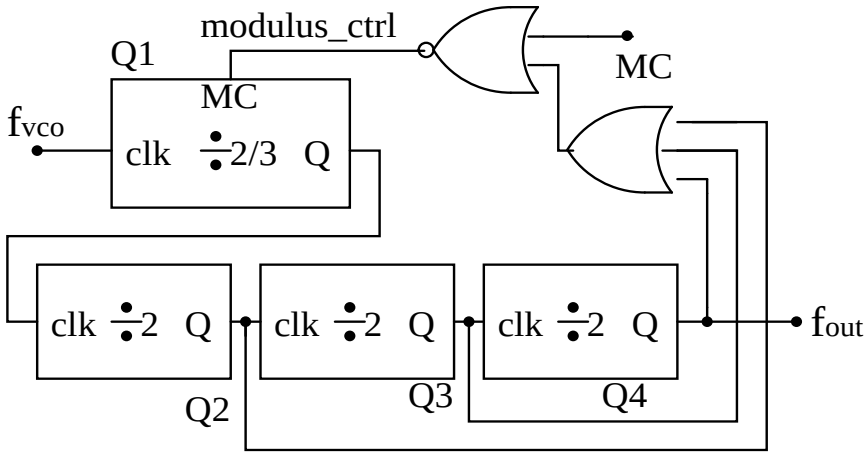


Figure 3.18: The diagram of ÷16/17 prescaler

As described in the section 2.5.2, the dual-modulus divider consists of a dual-modulus prescaler (N/N+1) followed by a program counter (P) and a pulse swallow counter (S), as shown in Fig. 2.18. The total division ratio is $PN + S$. Table 3.2 shows the 14 channel frequency allocation of the IEEE 802.11b/g standard. The *Greatest Common Factor* (GCF) is $1MHz$ for these channel frequencies. According to Eq. (2.9), the maximum reference frequency can be only 1MHz. When the **IF** LO frequency is set to 374MHz, with ÷16/17 prescaler, the configuration of the P and S counters for these 14 channels is also shown in Table 3.2.

The ÷16/17 prescaler consists of one dual-modulus ÷2/3 and three ÷2 di-

viders, as shown in Fig. 3.18. The critical condition for speed occurs when the $\div 2/3$ prescaler is supposed to divide by 3. The division by 17 is obtained by forcing $\div 2/3$ divider to divide by 3 once every 16 input transitions by the control signal MC. If the delay between the output ($Q1$) of the $\div 2/3$ divider and modulus control signal, $modulus\_ctrl$, are larger than one clock period, the circuit can not perform the correct division. However, relatively larger bias currents for the SCL D-latches in the flip-flop circuits (Fig. 3.21) means higher speed operation. In order to guarantee a correct operation of the prescaler up to 2.5GHz over process and temperature variations, the bias current of the SCL latches of the $\div 2/3$ divider is set to $750\mu A$. The differential output peak voltage is set to around 1V to drive the next stage differential circuit.

The first $\div 2$ divider stage has a maximum input frequency of 1.25GHz. Thus the speed requirements of this stage are relaxed and its power consumption can be reduced. From simulation, we set the bias current of the latches in D flipflop (Q_2 in Fig. 3.18) to $250\mu A$ to keep the differential output peak voltage at 1V. In order to decrease the white noise, the bias currents of the following two $\div 2$ dividers are also set to $250\mu A$.

Next, we introduce our design for the program counter (P) and the pulse swallow counter (S). CMOS logic ripple counters are used for both program and pulse swallow counters. Figure 3.19 shows the diagram of the program counter. The program counter generates one output pulse every 127 input pulses when the swallow counter count number is 6, 11 or 16 as described in Table 3.2. Otherwise, it generate one output pulse every 128 input pulses.

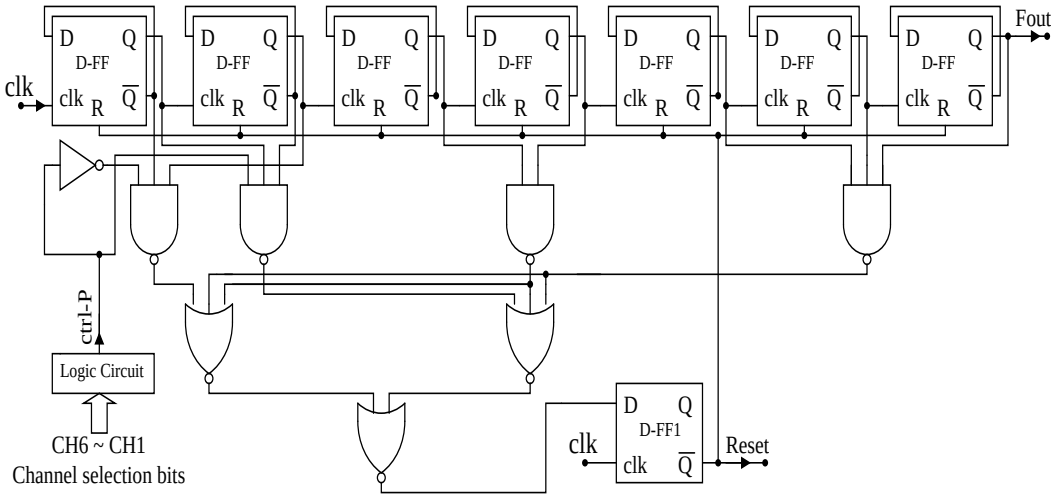


Figure 3.19: The diagram of a program counter

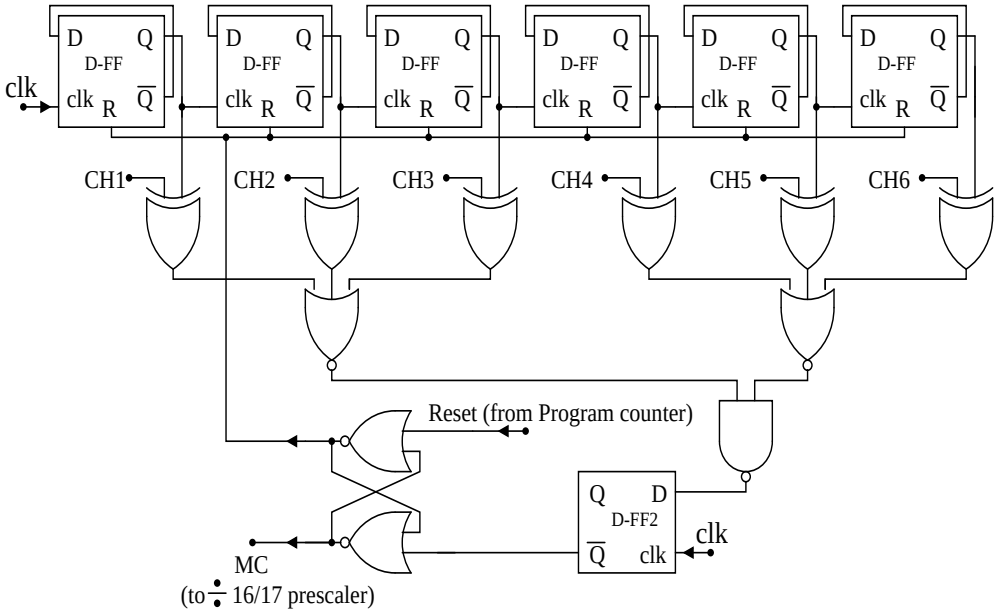


Figure 3.20: The diagram of a swallow counter

The diagram of the pulse swallow counter is shown in Fig. 3.20. The output of the swallow counter, MC, switches the division ratio of the prescaler ($\div 16/17$) and is controlled by 6 channel selection bits, $Ch1 \sim Ch6$ as shown in Fig. 3.20.

D Flipflops D-FF1 in Fig. 3.19 and D-FF2 in Fig. 3.20 are used to set and reset at the falling edge of the clock signal, clk. Therefore, the set and reset of MC are independent of the delays of the ripple counter and the logic gates.

All dividers including any CMOS logic counter are triggered by the falling edges of their input clocks, allowing a delay of as much as half of the period of the input of each divider. With this design, a race is further prevented [26].

Compared with the two-modulus divider, the main improvement for the multi-modulus divider is that its division ratio can be all the integer numbers from 64 to 127. In addition, the multi-modulus divider can function as the only block in the frequency divider. So neither a program counter nor a pulse swallow counter is necessary for multi-modulus frequency dividers compared with the structure of two-modulus dividers. The detailed circuit design of a multi-modulus divider ($64 \sim 127$) is given in section 4.3 later.

3.4.2 Source Coupled Logic

The dual-modulus and multi-modulus prescalers consist of $\div 2$ and $\div 2/3$ frequency dividers made of SCL latches and gates.

SCL is used in high-speed mixed signal environments due to its reduced switching noise, its low power dissipation at high frequencies compared to standard CMOS logic, and its immunity to common mode noise [77]. The maximum operating frequency and the required operating power of SCL can be altered by changing the DC bias condition of the gate. This mechanism enables performance versus power

trade-offs to be made during circuit operation. The standard CMOS logic utilizes the switching nature of CMOS transistors to pull its outputs toward Vdd or Vss, while SCL employs the current-steering properties of the differential pair to steer current from one part of the logic gate to another.

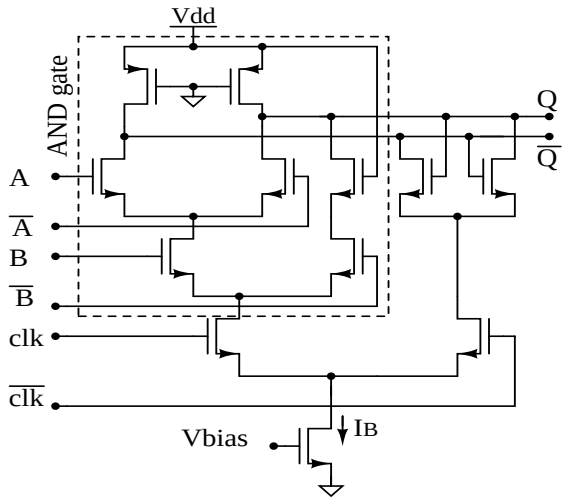


Figure 3.21: A D-latch with merged AND gate [58]

Figure 3.21 shows the circuit of a D latch merged with an AND gate (called "AND" D latch). This circuit structure can significantly increase the operating speed with less power consumption. By using the "AND" D latch, only two tail currents are needed to implement two AND gates and two D latches. In the same way, only three "AND" D latches are needed to implement six logic cells in the $\div 2/3$ divider, which is used to realize multi-modulus prescalers. Obviously, much power is saved with this "AND" D latch structure.

As we see, SCL requires DC bias currents, resulting in higher total static power dissipation compared to CMOS for frequencies lower than a few hundred megahertz, but at high frequency SCL may dissipate less total power than its CMOS equivalents.

The approximate propagation delay, τ, of the ideal SCL gate is proportional to the output signal swing by means of the relation [78]

$$\tau = \frac{C\Delta V}{I_B} \tag{3.78}$$

where C is the load capacitance on the logic gate, ΔV is the output voltage swing, and I_B is the tail current. This relationship indicates that the propagation delay can be reduced by a combination of lowering the signal swing and increasing the tail current used to charge and discharge the capacitance.

3.5 Charge Pump

Theoretically, an ideal charge-pump PLL does not suffer from reference clock feedthrough once it is locked. But in real frequency synthesis, the charge pump is the dominant block that determines the level of the reference spur (we will give the detailed explanation in section 3.5.1). Therefore, non-idealities of a charge pump should be carefully considered for circuit design.

In this section, the spectral components of the charge pump output (I_{out}) are derived first. Then, the effects of the charge pump non-idealities to reference spur are analyzed (see Eq. (3.88) and (3.92)). Later, we analyze some existing charge pump circuits. Based on the frequency spur and charge pump circuit analysis, we will give an improved charge pump circuit for our design.

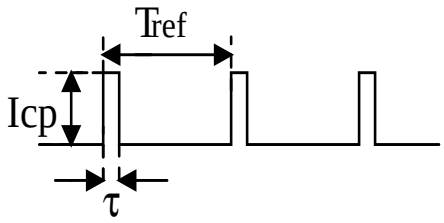


Figure 3.22: Charge pump output current pulses

3.5.1 Reference Spur Feedthrough

For an ideal charge pump, let the charge pump current be denoted as I_{cp}. The phase error between reference frequency f_{ref} and divider output frequency,f_{div}, is $\Delta\phi$. Then, the phase difference, $\Delta\phi$, is the proportion of the output current time, τ,as [59]:

$$\Delta\phi = 2\pi \cdot \frac{\tau}{T_{ref}} \tag{3.79}$$

where τ is the active time of the charge-pump output and T_{ref} is the period of the reference signal, as shown in Fig. 3.22. The Fourier series expression for a periodic train of pulses I_{out} shown in Fig. 3.22 is:

$$\begin{aligned} I_{out} &= I_{cp}\frac{\Delta\phi}{2\pi} + 2I_{cp}\frac{\Delta\phi}{2\pi}\sum_{n=1}^{\infty}\frac{\sin\left(n\pi\frac{\Delta\phi}{2\pi}\right)}{n\pi\frac{\Delta\phi}{2\pi}}\cos\frac{2\pi nt}{T_{ref}} \\ &= I_{cp}\frac{\tau}{T_{ref}} + 2I_{cp}\frac{\tau}{T_{ref}}\sum_{n=1}^{\infty}\frac{\sin\left(n\pi\tau/T_{ref}\right)}{n\pi\tau/T_{ref}}\cos\frac{2\pi nt}{T_{ref}} \end{aligned} \tag{3.80}$$

For a very small value of duty cycle $\frac{\tau}{T_{ref}} \ll 1$, $\frac{\sin(n\pi\tau/T_{ref})}{n\pi\tau/T_{ref}} \approx 1$. Eq. (3.80) can be simplified to:

$$I_{out} = I_{cp}\frac{\tau}{T_{ref}} + 2I_{cp}\frac{\tau}{T_{ref}}\sum_{n=1}^{\infty}\cos(2\pi n f_{ref}t) \tag{3.81}$$

This equation shows that the I_{out} signal comprises the fundamental and the harmonics of the reference frequency f_{ref}, and the amplitude of the spectral components of

I_{out} are twice as large as its DC value $I_{cp}\tau/T_{ref}$.

In an ideal situation the phase of the VCO would be perfectly locked and the duty cycle τ/T_{ref} of the charge pump output signal would be zero. In that case there would be no signal components at the reference nor its harmonics coming into the loop filter and therefore there would be no spectral degradation of the oscillator's output signal. In practice, however, there are two main issues which can generate reference spur.

A. Leakage Current

One of the issues in the charge pump design is the leakage current, which alters the voltage stored in capacitor C_1 of the loop filter, as shown in Fig. 3.1(a). There are several sources of leakage currents which may shift the voltage in C_1, the charge pump itself, the on-chip varactor, etc.. The phase offset due to the leakage current is usually negligible but the reference spur by the leakage current is possibly substantial in frequency synthesizers.

In Fig. 3.23(a), the pulse width of current I_{cp} to compensate the leakage current I_{leak} is:

$$\tau = T_{ref}\frac{I_{leak}}{I_{cp}} \tag{3.82}$$

when $I_{leak} \ll I_{cp}$ and $\tau \ll T_{ref}$, substitute Eq. (3.82) to Eq. (3.81), we get

$$I_{out}(t) = I_{leak} + 2I_{leak}\sum_{n=1}^{\infty}\cos(2\pi n f_{ref}t) \tag{3.83}$$

From standard modulation theory, it is known that the relationship of the peak phase deviation $\phi_p(f_m)$ to the peak frequency deviation $\Delta f(f_m)$ and the modulation

frequency f_m is given by

$$\phi_p(f_m) = \frac{\Delta f(f_m)}{f_m} \tag{3.84}$$

And, the peak frequency deviation is:

$$\Delta f(f_m) = V_{ripple}(n, f_{ref}) \cdot K_{VCO} \tag{3.85}$$

where $V_{ripple}(n, f_{ref})$ is the ripple voltage of the control voltage. The spectral components of the ripple voltage at the reference frequency f_{ref} and its harmonics can be expressed as:

$$|V_{ripple}(n \cdot f_{ref})| = 2I_{leak}|Z_f(j2\pi n f_{ref})| \tag{3.86}$$

where n ranges from 1 to ∞, and $Z_f(j2\pi n f_{ref})$ is the transimpedance function of the loop filter at the corresponding frequency.

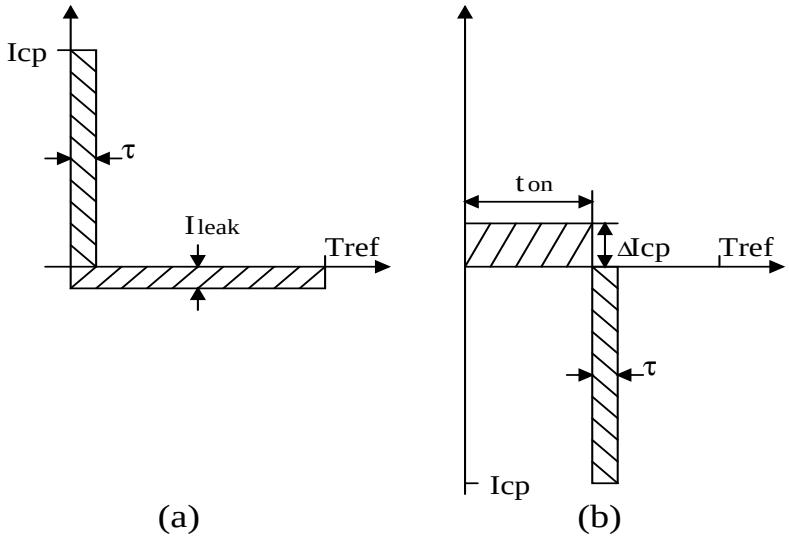


Figure 3.23: Charge pump output current in locked state due to mismatch: (a) current leakage, (b) current mismatch

Now, the peak phase deviation $\phi_p(n \cdot f_{rf})$ can be written as

$$\phi_p(n \cdot f_{ref}) = \frac{2I_{leak}|Z_f(j2\pi n f_{ref})|K_{VCO}}{n \cdot f_{ref}} \tag{3.87}$$

Each of the baseband modulation frequencies $n \cdot f_{ref}$ generates two RF spurious signals which are located at offset frequencies $\pm n \cdot f_{ref}$ from the carrier frequency f_{LO}. The amplitude of each spurious signal A_{sp} is:

$$\begin{aligned} A_{sp}(f_{LO} \pm n \cdot f_{ref}) &= A_{LO}\frac{\phi_p(n \cdot f_{ref})}{2} \\ &= A_{LO}\frac{I_{leak}|Z_f(j2\pi n f_{ref})|K_{VCO}}{n \cdot f_{ref}} \end{aligned} \tag{3.88}$$

where A_{LO} is the carrier amplitude. Therefore, we get

$$\left[\frac{A_{sp}(f_{LO} \pm n \cdot f_{ref})}{A_{LO}}\right]_{dBc} = 20\log\frac{I_{leak}|Z_f(j2\pi n f_{ref})|K_{VCO}}{n \cdot f_{ref}} \tag{3.89}$$

From Eq. (3.89), we get a conclusion that the relative amplitude of the spurious signals are determined by the transimpedance of the loop filter, by the magnitude of the *DC* leakage current, by the VCO gain and by the value of the reference frequency.

B. Mismatch in the Charge-Pump Current Sources

Another main issue is the mismatch in the charge pump current sources. Mismatch originates in the different type of devices used to implement the N-type current sources, which sink current from the output node to ground, and the P-type source which sources current from the positive supply to the output node. The current mismatch occurs in dumping the charge to the loop filter by *up* and *dn* operations. When the mismatch occurs in the charge pump, it is important to reduce

turn-on time (delay time) of the PFD that is equivalent to the minimum pulse width of the output to avoid the dead-zone [26].

Assume there is no leakage current. Let the current source mismatch of the charge pump be denoted by $\Delta I_{cp} = I_{up} - I_{dn}$, and assume $\Delta I_{cp} > 0$, as shown in Fig. 3.23(b). The pulse width of current $-I_{cp}$ to compensate this current mismatch ΔI_{cp} is:

$$\tau = t_{on} \cdot \frac{\Delta I_{cp}}{I_{cp}} \tag{3.90}$$

Usually $\Delta I_{cp} \ll I_{cp}$ and $t_{on} \ll T_{ref}$, then $\tau \ll T_{ref}$. Substitute Eq. (3.90) to Eq. (3.81), we get,

$$I_{out}(t) = \Delta I_{cp} \cdot \frac{t_{on}}{T_{ref}} + 2\Delta I_{cp} \cdot \frac{t_{on}}{T_{ref}} \cdot \sum_{n=1}^{\infty} \cos(2\pi n f_{ref} t) \tag{3.91}$$

Using a similar approach as applied to the leakage current, we get that the magnitude of the ripple voltage due to current source mismatch can be expressed as:

$$V_{mismatch}(n \cdot f_{ref}) = 2\Delta I_{cp}(n \cdot f_{ref}) \cdot \frac{t_{on}}{T_{ref}} \cdot |Z_f(j2\pi n f_{ref})| \tag{3.92}$$

Also, use the similar approach as applied to the leakage current, the spur level can be derived as:

$$\left[\frac{A_{sp}(f_{LO} \pm n \cdot f_{ref})}{A_{LO}}\right]_{dBc} = 20 \log \frac{\Delta I_{cp}(n \cdot f_{ref}) \cdot t_{on} \cdot |Z_f(j2\pi n f_{ref})| K_{VCO}}{n} \quad [dBc] \tag{3.93}$$

Eq. (3.93) shows how important it is to design the PFD and charge pump with the minimum turn-on time, t_{on}, as well as with the minimum mismatches. The minimum turn-on time is also important to reduce the inband noise contribution of the PLL to the output.

3.5.2 Analysis of CMOS Charge Pump Circuits

We will analyze three typical charge pumps as shown in Fig. 3.24 [59]. Figure 3.24(a) is the charge pump with the switch at the drain of the current mirror MOS. When the switch is turned off, the current pulls the drain of M1 to ground. After the switch is turned on, the voltage at the drain of M1 increases from 0V to the loop filter voltage held by the PLL. In the mean time, M1 has changed from the linear region to the saturation region. High peak current is generated. It is caused by the voltage difference of two series turn-on resistors from the current mirror, M1, and the switch $SW1$. On the PMOS side, the same situation occurs.

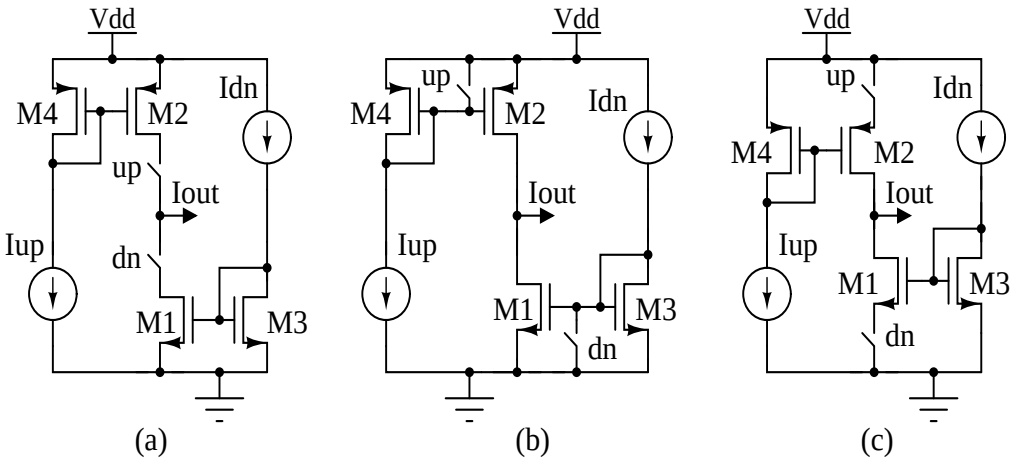


Figure 3.24: Typical charge pump circuits

To guarantee the MOS current mirrors in the saturation region, the topology with gate switches instead of drain switches is provided, as shown in Fig. 3.24(b). However, to achieve fast switching time, the bias current of M3 and M4 may not be scaled down since the transconductances of M3 and M4 affect the switching time constant. On the other hand, the gate capacitance of M1 and M2 is substantial

when the output current of the charge pump is high.

To get fast switching and save bias current, the switches located at the source of the current mirror MOSs are provided, as shown in Fig. 3.24(c). M1 and M2 are in the saturation region all the time. Different from the gate switching, the transconductances of M3 and M4 do not affect the switching time. As a result, low bias current can be used. This topology gives faster switching time than the gate switching since the switch is connected to a single transistor with low parasitic capacitance.

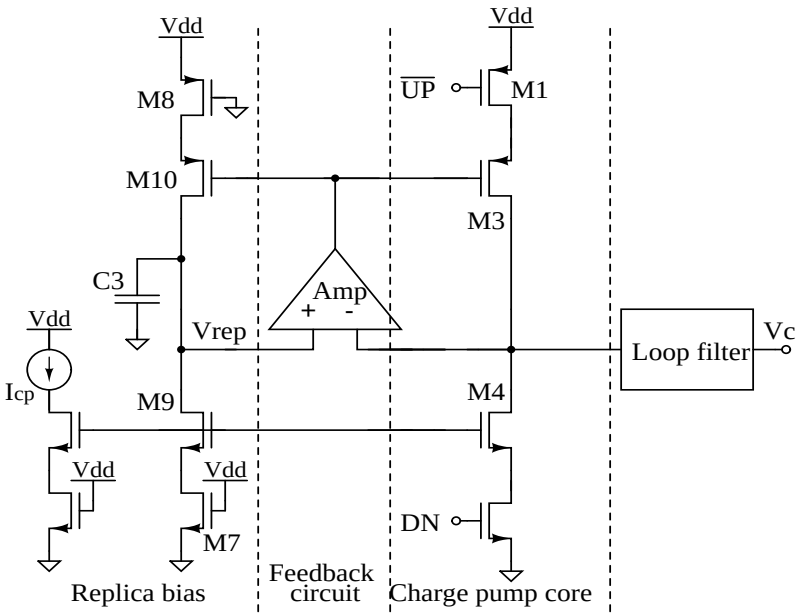


Figure 3.25: The circuit diagram of charge pump

In our design, we choose the topology as shown Fig. 3.24(c) with some improvement. We use a feedback circuit (AMP) and a replica bias to reduce the current mismatch in the *up* and *dn* branches. The new charge pump circuit is shown in Fig. 3.25. The detailed CMOS circuit will be given in section 4.4.

3.6 ΣΔ Modulators

ΣΔ noise shaping techniques have been widely used to suppress fractional spurs in fractional-N frequency synthesizers [34]-[36], [79]-[80]. In this section, first the influence of ΣΔ modulators on the spectral purity of the fractional-N synthesizer is investigated. We choose a 3rd-order MASH ΣΔ modulator (cascade 1-1-1) and a 3rd-order, multi-bit, single-loop ΣΔ modulators to study because the two modulators represent the extreme ends of the ΣΔ modulator topology spectrum. **Simulink** is used to model the two ΣΔ modulators, and **Matlab** is used to analyze their properties. Then, the PLL frequency synthesizer phase noise due to the ΣΔ modulator block is discussed, and some noise formulas are derived.

3.6.1 The MASH Modulator

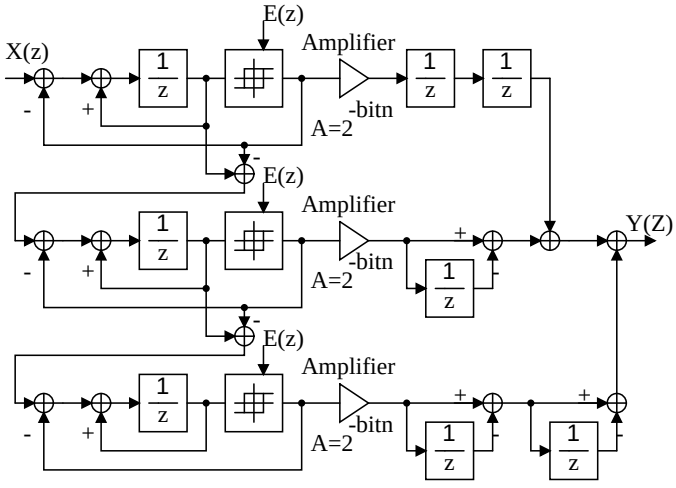
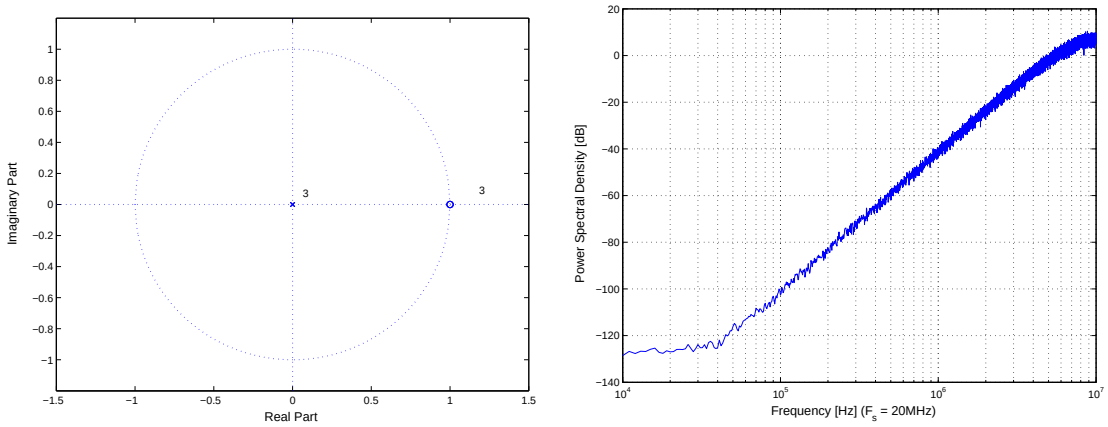


Figure 3.26: The 3rd-order MASH ΣΔ modulator Simulink Model

The simulink model of the MASH (multi-stage noise-shapping) or cascade 1-1-1 ΣΔ modulators is shown in Fig. 3.26. The MASH modulator consists of three

first-order modulators. The quantization error of the first modulator is the input of the second modulator, and the second modulator quantization error is the input of the third modulator. By adding the outputs of the three first-order modulators, the quantization error of the first and the second modulator is cancelled. The output Y has 8-levels and spread from -3 to 4 with an average between 0 and 1. The stable input range normalized to the modulator is from 0 to 1. It is inherently stable, because each first order $\Sigma\Delta$ modulator is stable.



(a) (b)

Figure 3.27: The 3rd-order MASH modulator: (a) The pole-zero plot, (b) The simulation of the output spectrum density

The signal transfer function and quantization noise transfer function (NTF) are given by [34]:

$$\frac{Y(z)}{X(z)} = z^{-3} \tag{3.94}$$

$$\frac{Y(z)}{E(z)} = (1 - z^{-1})^3 \tag{3.95}$$

where E(z) is the quantization noise associated with the third first-order modulator.

The noise transfer function contain 3 poles at the origin of the z-plane and 3 high-pass zeroes at the unit circle as shown in Fig. 3.27(a). The **Matlab** simulation was run on 2^{18} output points with the clock frequency of 20MHz. Figure 3.27(b) shows the simulated power spectrum density (PSD) of the MASH modulator output.

3.6.2 Single Stage with Multiple Feedforward

The multi-bit, single-loop ΣΔ modulator is shown in Fig. 3.28. This modulator consists of a single, 3rd-order discrete time filter with feedforward and feedback coefficients, which influence the noise transfer function NTF. Compared with the MASH architecture, the single-stage architecture has better noise shaping characteristics for dc inputs. But it is subject to instability and smaller input range. The latter limitation can be eliminated with a multi-bit quantizer as shown in Fig. 3.28.

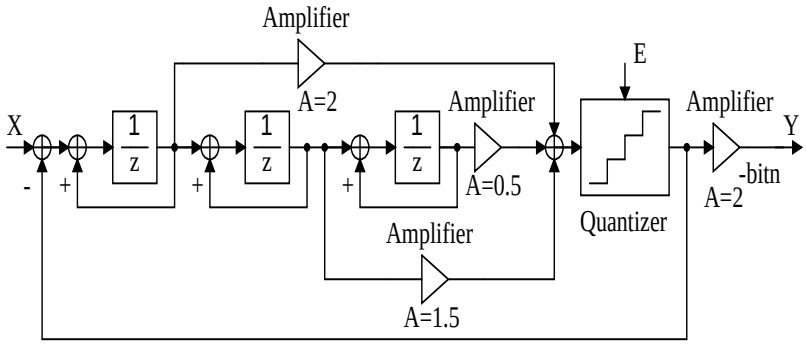


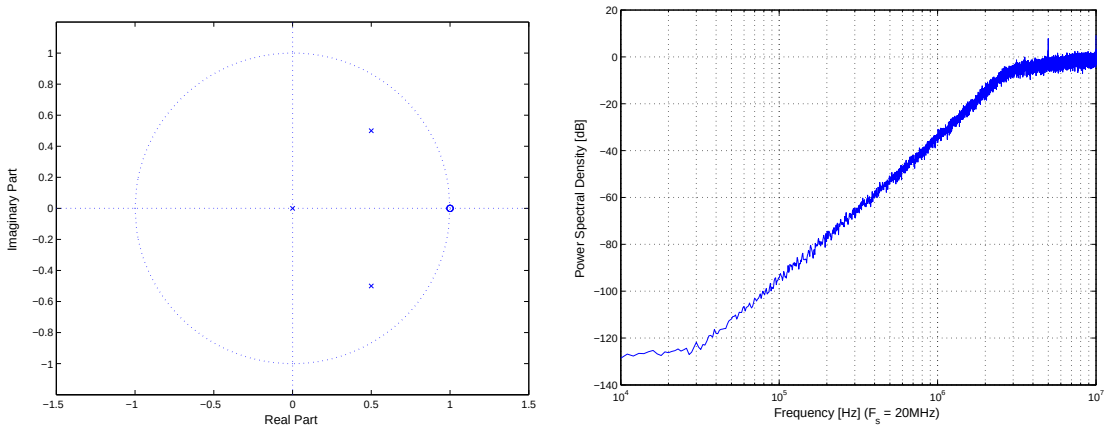
Figure 3.28: The 3rd-order multi-bit, single-loop ΣΔ modulator Simulink Model

To reduce the implementation complexity in CMOS technology, the coefficients of the feedforward and feedback are powers of two. The signal transfer function (without the quantizer) and quantization noise transfer function (NTF) are given

by:

$$\frac{Y(z)}{X(z)} = \frac{z^{-1}(2 - 2.5z^{-1} + z^{-2})}{1 - z^{-1} + 0.5Z^{-2}} \tag{3.96}$$

$$\frac{Y(z)}{E(z)} = \frac{(1 - z^{-1})^3}{1 - z^{-1} + 0.5z^{-2}} \tag{3.97}$$



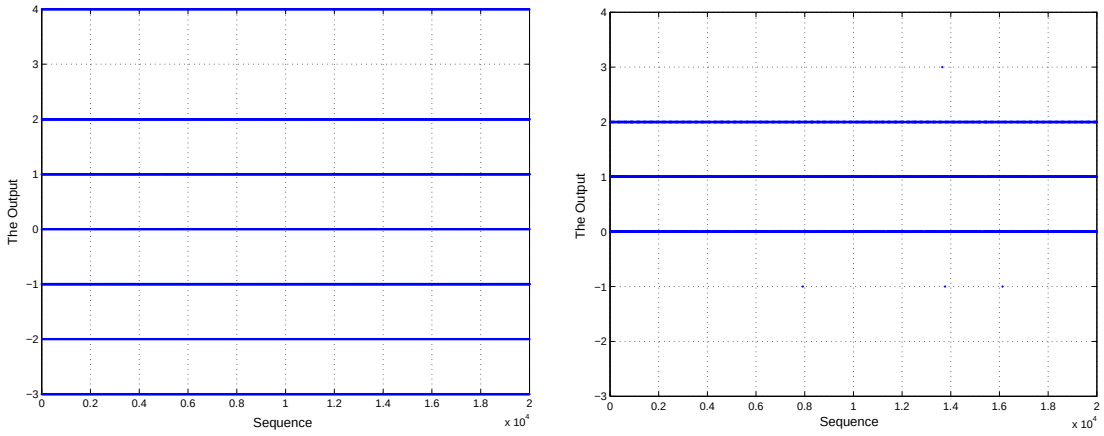
(a) (b)

Figure 3.29: The 3rd-order multi-bit, single-loop modulator: (a) The pole-zero plot, (b) The simulation of the output power spectral density

In contrast to the MASH modulator, the NTF contains 1 pole at the origin and another two symmetric complex poles inside the unit circle of the z-plane, as shown in Fig. 3.29(a). Figure 3.29(b) shows the simulated power spectral density of the multi-bit, single-loop modulator output. Although the single-loop $\Sigma\Delta$ modulator is more complex than the MASH modulator, it offers higher flexibility in terms of noise shaping. By adjusting the pole to the proper position, the quantization noise of the modulator is smoothed out. So, as shown in Fig. 3.29(b), a smooth curve results in the PSD's of the single-loop $\Sigma\Delta$ modulator.

In Fig. 3.30(a), 7 output states (7 division ratios) are employed to obtain the

wanted output for a MASH modulator in 20,000 samples (sequence in Fig. 3.30). And in Fig. 3.30(b), only 3 output states (3 division ratios) are intensively used while the other two states are used only for a limited amount of time for the single-loop modulator. So, PLL divider modulus switching is largely reduced, and the switching noise is dramatically decreased. It has better high frequency noise performance.



(a) (b)

Figure 3.30: The ΣΔ Modulator Output States: (a) MASH modulator, (b) Multi-bit, Single-loop Modulator

From the simulation results of Fig. 3.27(b), Fig. 3.29(b) and Fig. 3.30 for 3rd-order digital ΣΔ modulators, we observe that the single stage architecture is better than the cascaded one in terms of spurious content.

3.6.3 Phase Noise Due to ΣΔ Modulator Block

Discrete fractional spurs become more like random noise after ΣΔ Modulator noise shaping. The SSB phase noise of the noise-shaped fractional spurs is analyzed

as follows.

Considering the noise shapping with the mth-order MASH $\Sigma\Delta$ Modulator ($m \geq 1$), the PLL instantaneous output frequency f_{out} is always equal to the product of the instantaneous divide ratio and the reference frequency f_{ref} [36]:

$$f_{out}(z) = \left[N + \frac{K}{2^n} + (1 - z^{-1})^m E(z)\right] \cdot f_{ref} \tag{3.98}$$

The noise of the output frequency is the third term of Eq. (3.98):

$$E_{f_{out}}(z) = (1 - z^{-1})^m E(z) \cdot f_{ref} \tag{3.99}$$

According to Eq. (2.20), the noise PSD is:

$$S_{f_{out}}(z) = \frac{|(1 - z^{-1})^m f_{ref}|^2}{12 f_{ref}} = \frac{1}{12}|1 - z^{-1}|^{2m} f_{ref} \tag{3.100}$$

where the subscript f_{out} denotes the frequency fluctuations referred to the input of the divider. In order to obtain the phase fluctuations, consider the relationship between frequency ω and phase ϕ,

$$\omega(t) = 2\pi \cdot e_{f_{out}}(t) = \frac{d\phi(t)}{dt} = \frac{\phi(t) - \phi(t - T_{ref})}{T_{ref}} \tag{3.101}$$

and its z domain representation,

$$2\pi \cdot E_{f_{out}}(z) = \frac{\phi(z)(1 - z^{-1})}{T_{ref}} \tag{3.102}$$

Rearranging this expression yields

$$\phi(z) = \frac{2\pi \cdot E_{f_{out}}(z)}{f_{ref}(1 - z^{-1})} = \frac{2\pi}{(1 - z^{-1})} \cdot (1 - z^{-1})^m E(z) \tag{3.103}$$

From this equation, $E'(z) = (1 - z^{-1})^m E(z)$ is the noise output of the mth order $\Sigma\Delta$ modulator, and $\dfrac{1}{1 - z^{-1}}$ is an integrator. In the time domain, it can be

expressed as:

$$\phi(n) \quad = \quad 2\pi \cdot \{e'(n) + e'(n-1) + e'(n-2) + e'(n-3) + \cdots\} \tag{3.104}$$

And

$$e'(n) = y(n) - \overline{y} \tag{3.105}$$

where $y(n)$ is the mth order $\Sigma\Delta$ modulator output, and $\overline{y}$ is the average value of the whole set of output samples. With the sampling output $y(n)$ known, we can get $e(n)$ at each sampling time n, and we can calculate the phase $\phi(n)$ at each sampling time n. Using **Matlab**, the PSD of the $\Sigma\Delta$ modulator phase noise can be simulated.

According to Eq. (3.99), (3.100) and (3.103), the double-sideband phase noise PSD of the mth-order MASH $\Sigma\Delta$ modulator is:

$$S_{\phi}(z) = \frac{(2\pi)^2}{12 f_{ref}} \cdot |1 - z^{-1}|^{2m-2} \tag{3.106}$$

where the subscript ϕ denotes phase fluctuations. Noting that

$$|1 - z^{-1}| = |1 - e^{-j\omega T}| = 2\sin(\frac{\omega T}{2}) = 2\sin(\frac{\pi f}{f_r}) \tag{3.107}$$

the SSB phase noise PSD in the frequency domain is given by

$$\phi^2_{\Sigma\Delta}(f) = \frac{(2\pi)^2}{24 f_r} \cdot \left[2\sin\left(\frac{\pi f}{f_r}\right)\right]^{2(m-1)} \tag{3.108}$$

To find the effect of the $\Sigma\Delta$ modulator phase noise on the PLL output, a similar analysis to section 3.2 is performed. The noise from the $\Sigma\Delta$ modulator is injected into the system as shown in Fig. 3.31. Using the parameters in Fig. 2.8, $\Sigma\Delta$ modulator noise transfer function to the PLL output is given by by using G(s)

of Eq. (2.13):

$$\frac{\phi_{out,\Sigma\Delta}(s)}{\phi_{\Sigma\Delta}(s)} = \frac{G(s)}{1+G(s)} = \frac{K_{vco}K_{pd}F_{lpf}(s)}{Ns + K_{vco}K_{pd}F_{lpf}(s)} \tag{3.109}$$

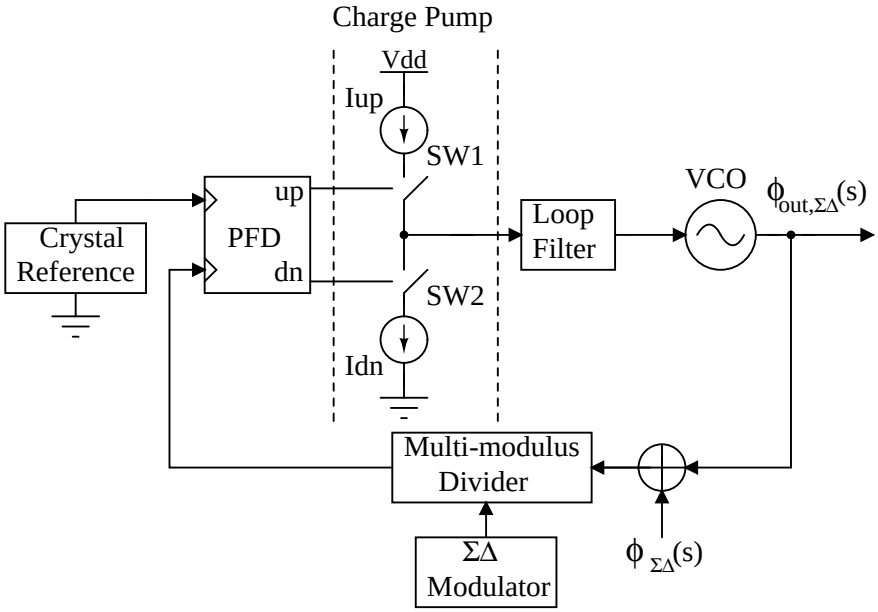


Figure 3.31: A fractional-N frequency synthesizer with a ΣΔ phase noise source added

3.7 Conclusions

This chapter presented analysis of the PLL frequency synthesizer. A linearized frequency domain model was analyzed according to its order. The PLL parameter effects on PLL dynamics and stability were characterized. Various noise sources in a PLL are identified and their contributions to the closed loop overall phase noise were derived. Then a design-oriented VCO phase noise model was developed. With the VCO noise model, we theoretically analyzed phase noise for both narrow band

and wide band VCOs. We also designed a complementary cross-coupled LC VCO to confirm the proposed phase noise model. The effects of the charge pump non-idealities to reference spur were analyzed, and a new charge pump design was given. Finally, the influence of $\Sigma\Delta$ modulators on the spectral purity of the fractional-N frequency synthesizer was investigated, and the PLL frequency synthesizer phase noise due to $\Sigma\Delta$ modulator block was derived. Based on the theoretical analysis, we will use VLSI to design a fractional-N PLL frequency synthesizer in the next chapter.

Chapter 4

Circuit Design of PLL Frequency Synthesizer

This chapter describes the detailed design and implementation of a $\Sigma\Delta$ fractional-N PLL frequency synthesizer. We begin with the PLL system design. With the system design parameters and specifications, then we focus on the PLL block design. In order to have good PLL phase noise performance, the VCO gain should be as low as possible. A wideband VCO is designed with low VCO gain in section 4.2. We also design a multi-modulus divider in section 4.3. The main issue in designing dividers is to achieve a speed as high as possible at a reasonable power consumption. *Source coupled logic* (SCL) is used for high frequency digital circuit design for saving power and lowering noise. Then, we give the circuit design of a phase frequency detector and a charge pump in section 4.4. To reduce the effect of reference spur feedthrough for good phase noise performance, we improve the charge pump design by using a feedback circuit to decrease the mismatch between the current in the *up* branch and that in the *down* branch. Later, we give the circuit design of a 3rd-order $\Sigma\Delta$ modulator in section 4.5. Pipeline techniques and *True Single phase Clock* (TSPC) techniques are used to further save power and area. Finally, we give the PLL simulation results and the measurements of a 2GHz VCO chip in sections 4.6 and 4.7, respectively.

4.1 The 2.4GHz Fractional-N PLL Frequency Synthesizer

4.1.1 Implementation

In the integer-N frequency synthesizers only integer multiplies of the reference frequency can be synthesized as we have explained in the previous chapters. Stability requirements limit the loop bandwidth to about one tenth of the reference frequency. As a result, the dynamic behavior of this type of PLL is seriously degraded in narrow band communication systems. In addition, a high division modulus N is necessary. From the noise analysis in section 3.2, the noise contributions of almost all PLL building blocks, except the VCO, are multiplied by N, so the phase noise of the PLL output becomes even worse.

In the fractional-N frequency synthesizers, fractional multiples of the reference frequency can be synthesized, allowing a higher reference frequency for a given frequency resolution. That means the loop bandwidth can be increased, without deteriorating the spectral purity. Therefore, the PLL dynamics are accelerated and the total amount of required capacitance in the loop filter can be decreased.

Figure 4.1 displays a block diagram of the $\Sigma\Delta$ fractional-N frequency synthesizer that includes the key circuits discussed in earlier chapters of this thesis. The asynchronous, 64 modulus divider supports any divide value between 64 and 127. The digital MASH $\Sigma\Delta$ modulator achieves low power operation through pipelining. The N_{offset} is used to decide the integer part of the division ratio, while the output of the $\Sigma\Delta$ modulator is used to decide the average value of the fractional part of the division ratio.

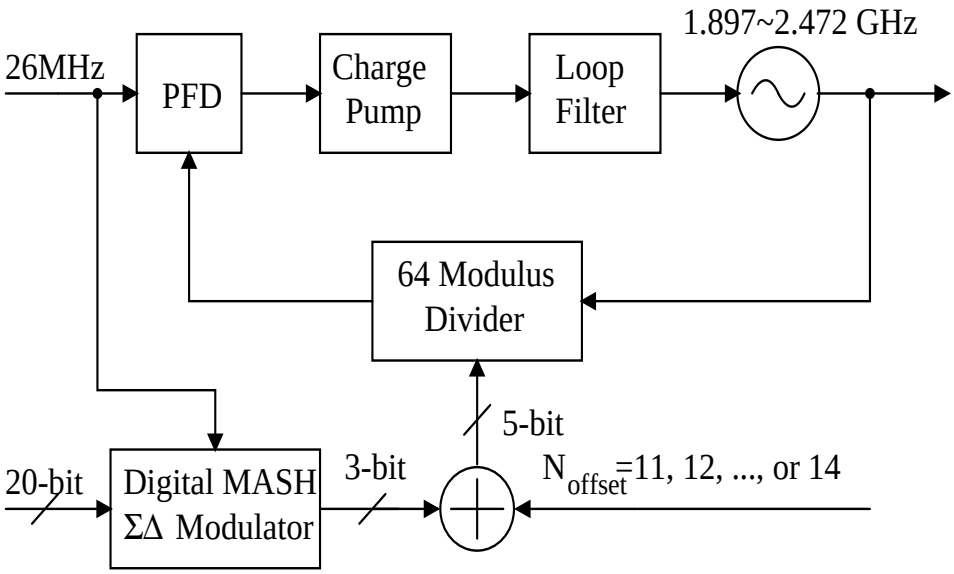


Figure 4.1: The block diagram of the 2.4GHz fractional-N PLL frequency synthesizer

To make the $\Sigma\Delta$ modulator output more randomized, the bit width of the $\Sigma\Delta$ modulator input is set to 20. As discussed in the next section, the reference frequency is chosen as 26MHz. So the smallest integer resolution can be $26MHz \times \frac{2^{13}}{2^{20}} = 203125Hz$. If the the power of 2 is less than 13, then the frequency resolution will be fractional. By choosing the division from 78 to 82, the VCO ranges from 2.028GHz to 2.132GHz, which covers IEEE 802.11 b/g RF frequency range ($2.038GHz \sim 2.110GHz$) as shown in Table 3.2.

4.1.2 Selection of Parameters

A linear frequency domain model of the fractional-N PLL frequency synthesizer is shown in Fig. 4.2. The open loop transfer function of the system consists of two poles at zero frequency, a zero at $-f_z$, a pole at $-f_{p2}$, and another pole at $-f_{p3}$. f_{p3}

occurs at a much higher frequency and therefore has little influence on the system stability.

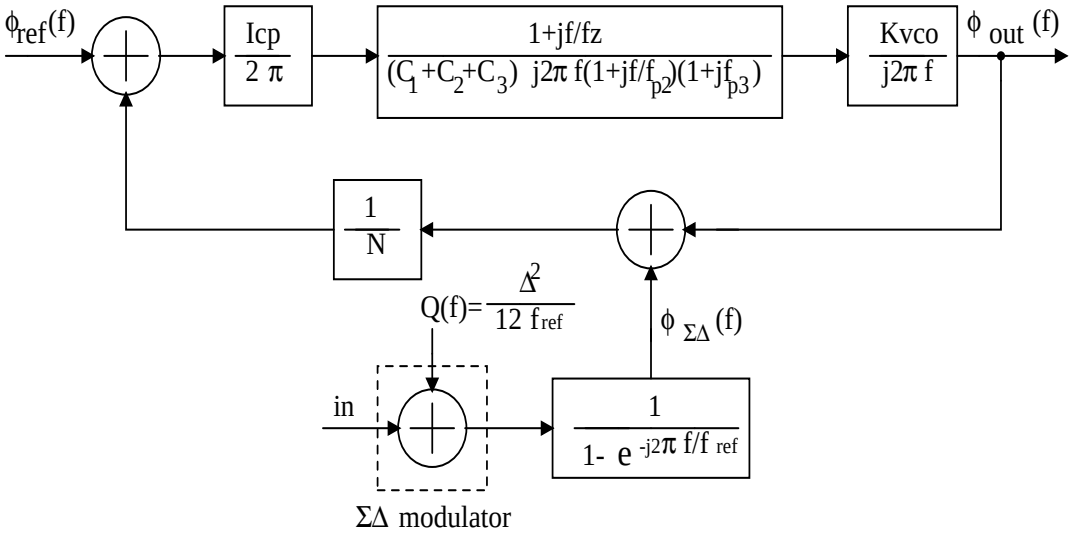


Figure 4.2: The linearized, frequency-domain model of the 2.4GHz fractional-N PLL frequency synthesizer

The PLL transfer function will be defined as $G(jf)$ and is related to the PLL parameters. By Eq. (3.1), the loop filter transfer function $F_{lpf}(jf)$ is

$$F_{lpf}(jf) = \frac{1 + jf/f_z}{(C_1 + C_2 + C_3) \cdot j2\pi f(1 + jf/f_{p2})(1 + jf/f_{p3})} \tag{4.1}$$

The above parameterization of $F_{lpf}(jf)$ allows us to express $G(jf)$ as

$$G(jf) = \frac{I_{cp}K_{vco}}{2\pi(C_1 + C_2 + C_3)N} \cdot \frac{1 + jf/f_z}{(j2\pi f)^2(1 + jf/f_{p2})(1 + jf/f_{p3})} \tag{4.2}$$

To obtain a parameterization of $G(jf)$ that achieves the fast locking time, we must select the appropriate value of the loop bandwidth f_c. The value of f_c, in turn, should be set according to the reference frequency value, f_{ref}. We assume the

loop bandwidth is $f_c = 150KHz$ for good dynamic performance. We know the loop bandwidth is on the order of one of tenth of the reference frequency [28], so that the choice of $f_{ref} = 26MHz$ seems appropriate.

The accurate locking time calculation is pretty complex. A rule of thumb equation of the estimation of locking time, T_{lock}, for a PLL is [82]:

$$T_{lock} \approx \frac{0.2}{f_c}(1 - log\frac{\epsilon}{\Delta f}) \tag{4.3}$$

where ϵ is frequency error. When the frequency difference is smaller than ϵ, the PLL is considered to be locked. Δf is the difference of the first and last channel frequency. In our case, the worst case is $\Delta f = 2110 - 2038 = 72MHz$ as seen in Table 3.2, and $\epsilon = 100Hz$.

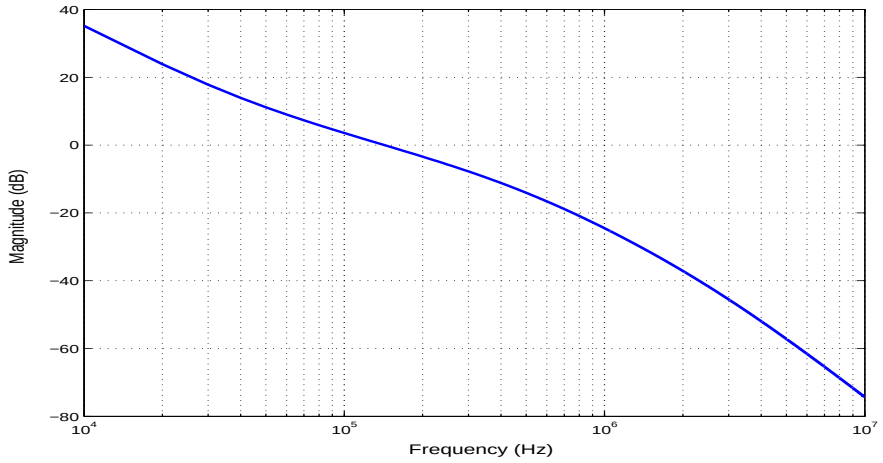
(a) For the fractional-N PLL with reference frequency $26MHz$ and the loop bandwidth $150KHz$, its locking time is calculated by Eq. (4.3) as: $T_{lock} = 9.143\mu s$.

(b) In the same way, for an integer-N PLL with the reference frequency $1MHz$ and assuming loop bandwidth $20KHz$, its locking time is calculated by Eq. (4.3) as: $T_{lock} = 68.573\mu s$.

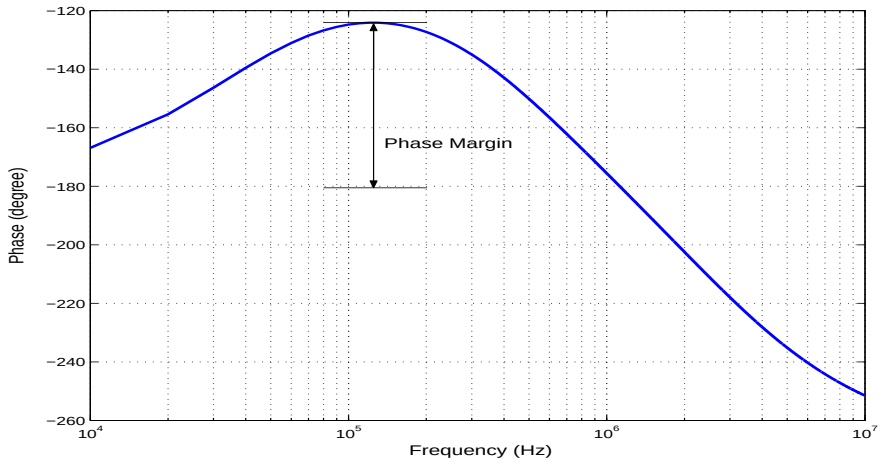
So, the fractional-N PLL has much faster locking time.

The noise-shaping slope of an mth-order MASH $\Sigma\Delta$ modulator is $20(m - 1)dB/dec$ according to Eq. (3.108), while a nth-order lowpass filter has a slope of $(-20n)dB/dec$. The total slope of the $\Sigma\Delta$ modulator and the nth-order lowpass filter together is $-20(n - m + 1)dB/dec$. To make the slope equal or lower than $-20dB/dec$, the order of the loop filter, n, must be higher than or equal to the order

of the ΣΔ modulator, m, in order to attenuate the out-of-band noise due to ΣΔ modulation. We use a 3rd-order ΣΔ modulator, so we choose a 3rd-order loop filter for our prototype design.



(a)



(b)

Figure 4.3: The fractional-N PLL open-loop: (a) Gain, (b) Phase

Given the loop bandwidth as 150kHz, to keep the PLL in a stable state, we

chose a maximum phase margin of about 58°. This gives b from Eq. (3.17). Using it in Eq. (3.13) and Eq. (3.16), we get the PLL open loop zero and pole values as:

$$f_z = 38.7kHz, \quad f_{p2} = 580.9kHz, \quad f_{p3} = 2.25MHz \tag{4.4}$$

The zero, poles, loop bandwidth, and locking time are shown in Table 4.1.

Parameter	f_z	f_{p2}	f_{p3}	f_c	T_{lock}
Value	38.7kHz	580.8kHz	2.25MHz	150kHz	$9.4\mu S$

Table 4.1: The open loop parameter settings in PLL

The VCO gain, charge pump current, the capacitor, and the resistor values must be appropriately set within the loop filter to obtain the open loop parameters specified in Table 4.1. Drawing from Chapter 3, f_z, f_{p2}, and f_{p3} are related to the parameters by the following expression:

$$f_z = \frac{1}{2\pi R_1 C_1} \tag{4.5}$$

$$f_{p2} = \frac{1}{2\pi R_1 (C_2 + C_3)} \tag{4.6}$$

$$f_{p3} = \frac{1}{2\pi R_3 C_2 C_3 / (C_2 + C_3)} \tag{4.7}$$

The reference frequency is 26MHz, and we set the divider division ratio to 79 to achieve an output carrier frequency of 2.054GHz. Low VCO gain is very important to the PLL system phase noise, so we will design the typical gain of our wideband VCO to be 100MHz/V. And we also know that the larger the charge pump current, the lower the charge pump phase noise. To keep the charge pump phase noise low,

the charge pump current is set to $50uA$. Note from Eq. (3.4) that the open loop gain is defined in terms of parameters as:

$$K = \frac{K_{pd}K_{vco}R_1}{N} = \frac{I_{cp}K_{vco}R_1}{2\pi N} \tag{4.8}$$

And at the maximum phase margin, according to Eq. (3.18) the PLL loop bandwidth f_c can be simplified to:

$$f_c \approx \frac{K}{2\pi} \tag{4.9}$$

Parameter	Value
VCO Gain	100MHz/V (Typical) 150MHz/V (Maximum)
CP Current	50uA
C_1	272pF
C_2	10pF
C_2	8.2pF
R_1	15.1kΩ
R_3	15.7kΩ
Phase Margin	58°

Table 4.2: The design parameters of the ΣΔ fractional-N PLL synthesizer

From Eq. (4.8), Eq. (4.9), and the design parameters I_{cp}, K_{VCO}, and N, we calculate R_1. R_1 value can not be made very large for low noise loop filter design. Also for this reason, the charge pump current can not be very small when the other

PLL parameters are fixed. Table 4.2 displays parameter settings that achieve the desired value of f_c, f_z, f_{p2}, and f_{p3} in Table 4.1.

In the remaining part of this chapter, we will give the detailed circuit design of the PLL blocks in this fractional-N PLL frequency synthesizer.

4.2 A Wideband LC VCO Design

In section 3.3, a phase noise model was presented for a generally cross-coupled VCO. We analyzed the wideband VCO tuning range and its constant output level control scheme. Based on the previous theoretical analysis results, a wideband LC VCO is designed with low VCO gain and a large tuning range in this section.

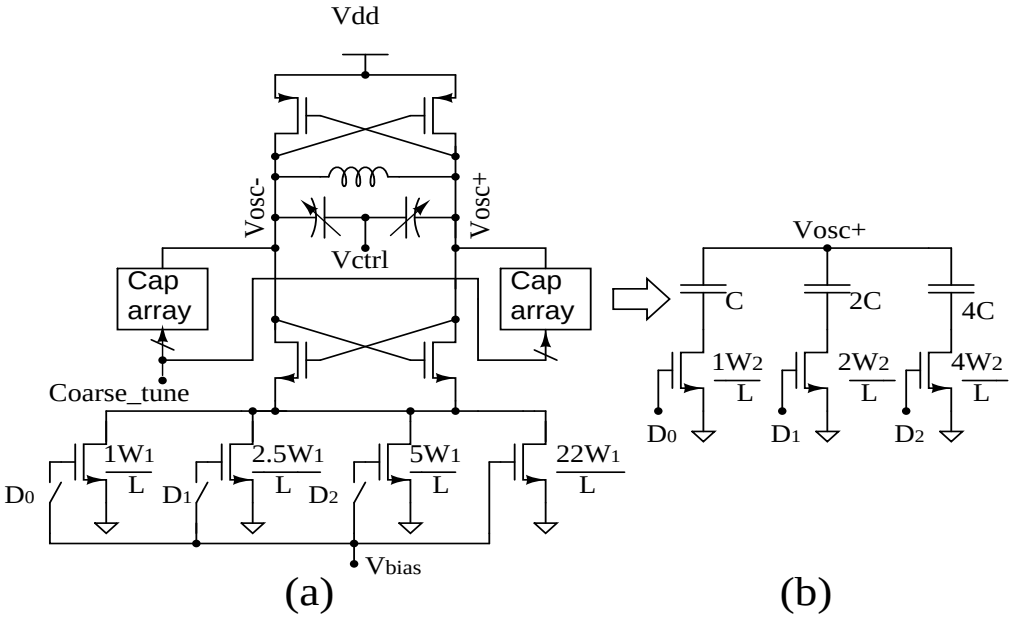


Figure 4.4: The wideband LC VCO: (a) The VCO schematic, (b) The capacitor array

4.2.1 A Wideband VCO

The schematic of the wideband VCO in our design is shown in Fig. 4.4. It is also a complementary cross-coupled structure with an additional switched capacitor bank. The W/L of the cross-coupled NMOS and PMOS devices is chosen to satisfy the oscillation startup condition at the lowest frequency of the tuning range. Because of the large frequency range for a wideband VCO, the inductance of the differential inductor should be a little smaller compared with the inductor in the VCO of section 3.3.3. So we choose the inductor in the group with the metal-width=$9\mu m$. The design parameters of the differential inductor are summarized in Table 4.3.

Metal	Metal Width/Space	Inner Radius	Turns	Q	L	r_s
Metal6	9μm/2μm	80μm	4	8.4	4.54nH	7.6Ω

Table 4.3: Design parameters of an inductor in a wideband LC VCO

In order to achieve a low tuning sensitivity K_{vco} and a relatively large frequency range, the LC tank combines a pair of small varactors and 3-bit binary weighted switched capacitor arrays. High quality factor metal-insulator-metal capacitors should be used for the switched capacitor array. With Eq. (3.73), the variable capacitance of the varactor must be larger than the variable unit capacitance of the switched capacitor array to make sure there is no gap in the whole band. According to the theoretical analysis results in section 3.3.4, the minimum-length MOS transistors with sufficiently large width are used to avoid the LC tank Q degradation due to the switch finite channel resistance. On the other hand,

we should avoid large off-state parasitic capacitance, which will limit the tuning range. So, from simulation results we choose the size parameters for the switches as $\frac{W_2}{L} = \frac{100\mu}{0.35\mu}$ (see Fig. 4.4).

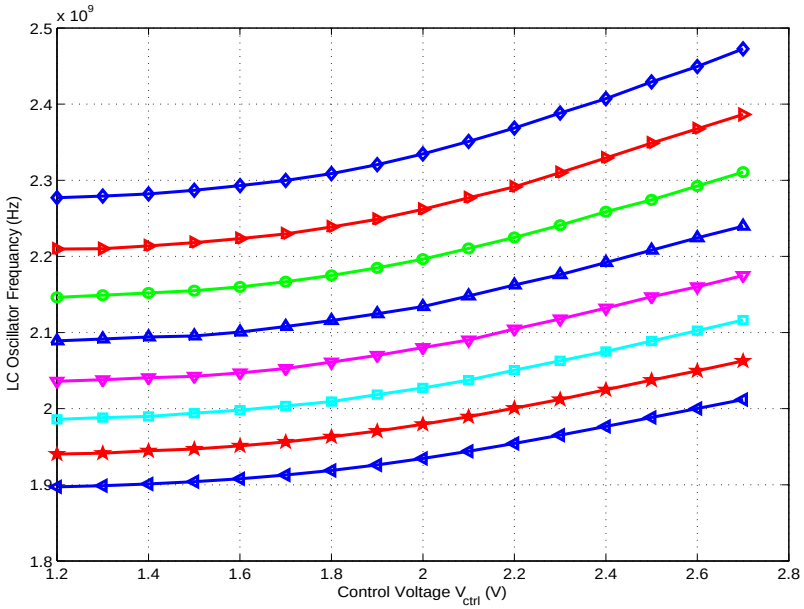


Figure 4.5: The wideband LC VCO tuning range (the curve changes from $D_2D_1D_0 = 000$ to $D_2D_1D_0 = 111$ from the top to the bottom)

Figure 4.5 shows the simulated tuning range of the wideband VCO. Table 4.4 shows the tuning range of each subband. The whole frequency range is split into 8 subbands by the switched capacitor array coarse tuning. The whole tuning range is from $1.897GHz$ to $2.472GHz$. These values are sufficient to compensate the frequency range caused by the variations of temperature and process. The typical VCO gain K_{vco} is around $100MHz/V$. Compared with the previous VCO gain of $300MHz/V$, this wideband VCO gain is much lower. That means that the wideband

VCO has better overall PLL phase noise performance according to the analysis in section 3.3.

Figure 4.6 shows the simulated wideband VCO phase noise when the oscillation frequency is $2GHz$. We can see the phase noise is $-127dBc/Hz$ at 1MHz frequency offset. It is lower than the phase noise of the VCO in section 3.3.3 because the bias current here is calibrated to 2.6mA, while the bias current of the VCO in section 3.3.3 is $2.2mA$. From Eq. (3.63) and Eq. (3.65), it is known that the larger the bias current is, the better the phase noise performance is.

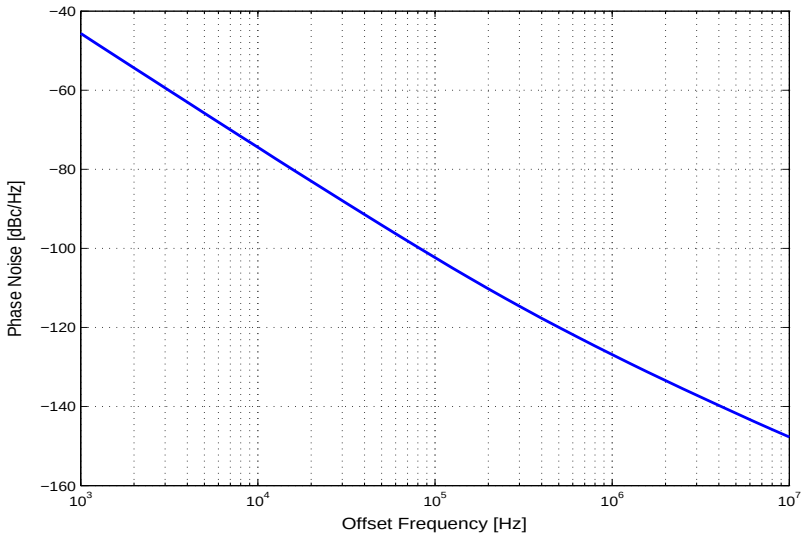


Figure 4.6: The wideband LC VCO phase noise, $f_0 = 2GHz$

4.2.2 Automatic Amplitude Control

As we have mentioned in section 3.3.5, the output swing level of the VCO is a very important specification in VCO design. The receiver and the transmitter chip

expect an LO signal of constant power. From Eq.(2.24), we know the equivalent parallel tank impedance decreases as the oscillation frequency decreases. So, we need to increase the tail current I_{Bias} with decreasing VCO frequency to keep the constant output swing by using Eq. (3.51). The tail current circuit is designed as shown in Fig. 4.4(a). It monitors the operating status of the fixed and variable capacitors and provides current to compensate the inductance variation for the constant output swing. Table 4.4 shows the VCO output swing in different subbands.

$D_2D_1D_0$	Frequency Range (GHz)	Amplitude Range (V)
000	2.277 $\sim$ 2.472	0.829 $\sim$ 0.931
001	2.209 $\sim$ 2.386	0.825 $\sim$ 0.917
010	2.146 $\sim$ 2.311	0.835 $\sim$ 0.919
011	2.089 $\sim$ 2.239	0.831 $\sim$ 0.911
100	2.036 $\sim$ 2.175	0.839 $\sim$ 0.916
101	1.986 $\sim$ 2.116	0.8436 $\sim$ 0.909
110	1.940 $\sim$ 2.063	0.846 $\sim$ 0.914
111	1.897 $\sim$ 2.012	0.845 $\sim$ 0.911

Table 4.4: Frequency and output swing of VCO at different subbands

4.3 Programmable Frequency Dividers

In this section, we will investigate the design of a multi-modulus divider. The main issue is of course to achieve a speed as high as possible at a reasonable power consumption. Source coupled logic (SCL) is used in the high speed part of dividers to lower power consumption. In our design, the IEEE 802.11b/g frequency divider (Table 3.2) is designed. The multi-modulus divider's division ratio can be all the integer numbers from 64 to 127. In addition, the multi-modulus divider can function as the only block in the frequency divider. So neither a program counter nor a pulse swallow counter is necessary for multi-modulus frequency dividers compared with the structure of two-modulus dividers.

4.3.1 Multi-Modulus Frequency Divider

As we introduced in chapter 3, a $\Sigma\Delta$ modulator and a multi-modulus divider combined together can realize an average fractional-N division ratio, $N + F$, where N is an integer and $F \in [0, 1]$.

The decimal part (F) of the division ratio of a multi-modulus divider is decided by the output of the $\Sigma\Delta$ modulator. In our design, we use a 3rd-order MASH 1-1-1 $\Sigma\Delta$ modulator. It has 3-bit outputs with 8 output levels from -3 to +4. In order to realize the $N + F$ division ratio, the multi-modulus divider should be an 8 modulus divider with division ratio $N - 3$, $N - 2$, $\cdots$, N, $\cdots$, $N + 4$.

As stated in section 4.1.1, our application is aimed at the IEEE 802.11b/g frequency synthesizer. Its RF VCO frequency ranges from $2038 \sim 2110MHz$ as

shown in Table 3.2. In our design, we chose $26MHz$ as the reference frequency. To get the required output frequency by using the multi-modulus divider, the division ratio should cover from $\frac{2038}{26} \approx 78.38$ to $\frac{2011}{26} \approx 81.15$. To realize the division ratio $78+F$, the multi-modulus divider should have all the moduli ranging from 75 to 82. Similarly, to realize $81 + F$, the multi-modulus divider should have all the moduli ranging from 78 to 85. In order to realize $78 + F$, $79 + F$, $\cdots$, $81 + F$, the multi-modulus divider should have all the moduli from $75 \sim 85$. According to Eq. (2.37), 6 asynchronous $\div 2/3$ dividers are required for this multi-modulus divider, which can realize a continuous range from 64 to 127. So our division ratio requirement is satisfied.

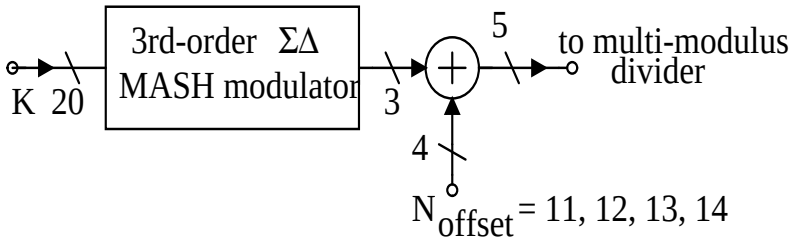


Figure 4.7: The diagram of a $\Sigma\Delta$ modulator with N_{offset}

Moduli Range	Division Ratio ($0 \leq F < 1$)	N_{offset}
75∼82	75+F	11
76∼83	76+F	12
77∼84	77+F	13
78∼85	78+F	14

Table 4.5: Configuration of N_{offset}

A third-order MASH ΣΔ modulator can only provide 8 output values, which decide the decimal value (F) of the fractional value $N + F$. In order to synthesize the total frequency range of the PLL, a 4-bit word, N_{offset} is added to the output of the ΣΔ modulator, as shown in Fig. 4.7. This resulting 5-bit word controls the divider moduli. Then all moduli between 75 to 85 are employed. Table 4.5 gives the detailed configuration of the N_{offset} number.

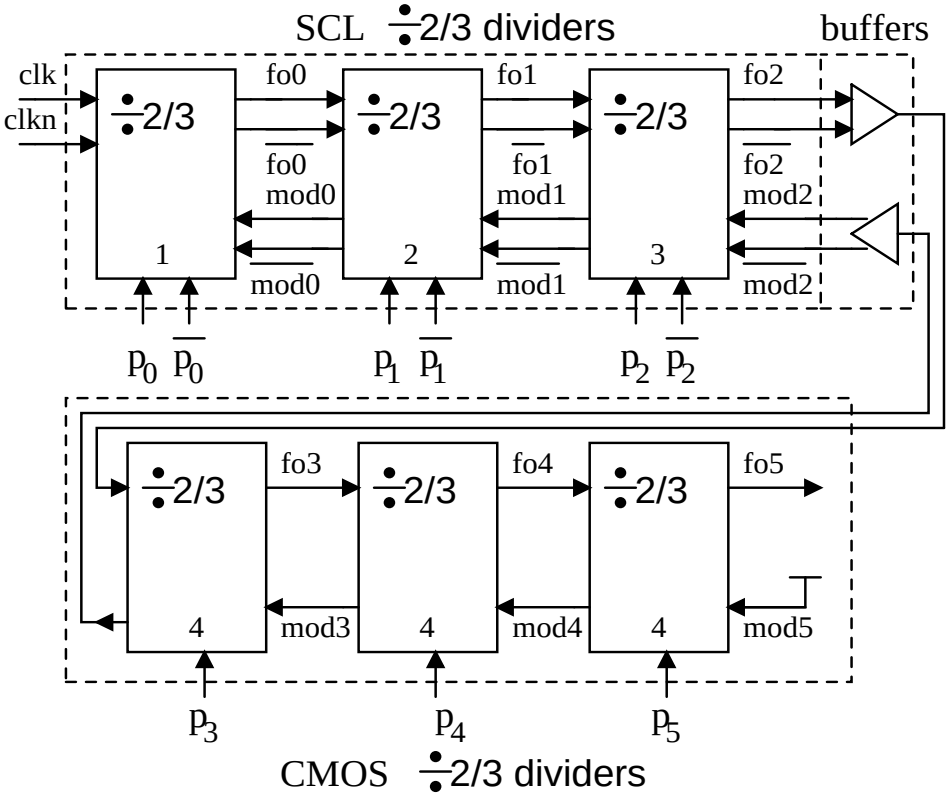


Figure 4.8: The schematic of the multi-modulus divider

The multi-modulus divider is shown in Fig. 4.8. It is a fully programmable divider, which consists of 6 asynchronously cascaded dual-modulus ÷2/3 dividers. From this figure, we can see there are two parts made of this divider. The upper

part is the high speed part, which is implemented by SCL. The lower part is the low speed part, which is implemented by CMOS logic. This implementation assures that the first stage of the multi-modulus divider runs at the high frequency of 2.5GHz.

To reach the operating frequencies of 2.5GHz, Cadence SpectreRF simulation gives the tail current in the first $\div 2/3$ divider as 750uA. With the reduced speed, 250uA tail currents are used in the second and the third $\div 2/3$ dividers to lower power consumption.

4.4 Phase Frequency Detector and Charge Pump

The phase frequency detector and charge pump are responsible for phase error to current ($\Delta\phi \rightarrow I_{out}$) conversion in PLL systems. In this section, we will give the circuit level detailed implementation of these two blocks.

4.4.1 Phase Frequency Detector

Figure 4.9 shows the circuit diagram of the phase frequency detector. The two inverters in the reset path generate enough delay to eliminate the dead zone of the charge pump [26]. As we discussed in section 3.5.1, the delay (turn-on time) of the charge pump should be as small as possible for better noise performance. The implementation of the phase frequency detector at the gate level is shown in Fig. 4.9. In order to reduce the skew between the complimentary output signals, the exclusive-or (XOR) gates are used to generate switching controls up and dn and their inverse signal $\overline{up}$ and $\overline{dn}$.

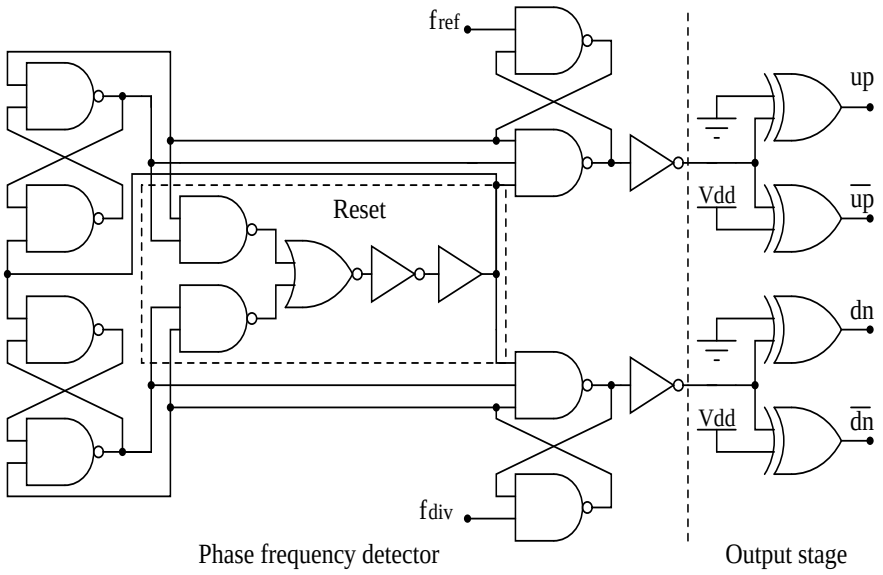


Figure 4.9: Phase frequency detector using RS latch

4.4.2 Charge Pump

As we discussed in section 3.5, in conventional charge pump design, one of the problems is the current mismatch between the up and down branches. It causes the reference spur feedthrough. Another problem is the charge pump current glitches, which cause the higher power level of the PLL spurs. Both of the problems result in increased phase noise. According to our analysis results, we choose the topology of Fig. 3.24(c) for our design. But as this topology is very simple, we should modify this circuit to make it really work.

To decrease the effects of current mismatch and charge pump current glitches, the improved charge pump circuit is shown as Fig. 3.25, which is made of the charge pump core, the feedback circuit (amplifier), and the replica bias. Its CMOS circuit is shown in Fig. 4.10. The reference current I_{CP} flows from M10 to M9 through the replica circuit, and it is mirrored to the charge pump up branch by current mirror

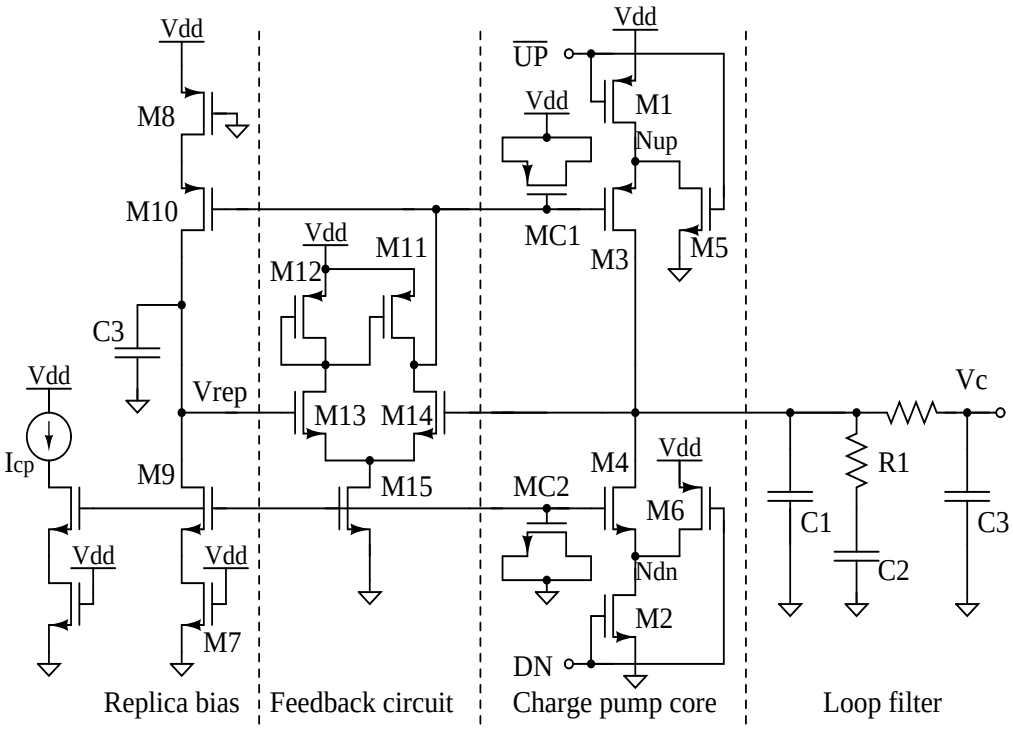


Figure 4.10: CMOS circuit of the charge pump

M3 and M10, and the charge pump down branch by current mirror M4 and M9. In order to match the two currents more precisely, three methods are adopted. First, M7 and M8 are inserted to reduce the mismatch in current mirrors due to the two current switches M1 and M2. Second, compensation of the low output impedance of the up and down current sources is done to make the current variation less sensitive to the output voltage, V_c. The up and down currents are monitored in the replica circuit. A negative feedback circuit (made by M11-M15, M9 and C3) compares the output voltage, V_c, with the replica circuit voltage, V_{rep}, to make V_{rep} follow V_c. Because of the low gain wideband VCO, the control voltage V_c is expected to vary in a small range around $Vdd/2$. Therefore, a simple differential pair (M13 and M14) is used as input stage, and it is not necessary to extend the amplifier input

and output ranges. In addition, large size transistors for current mirrors are used for better matching in circuit layout.

To overcome the charge pump current glitches, two switches M5 and M6 are used to provide low-impedance charging/discharging paths for removing the charge from nodes N_{up} and N_{dn} when up switch or down switch is turned off. The $10pF$ bypass capacitors MC1 and MC2 are added to further attenuate the glitches since they provide additional paths to ground.

4.5 ΣΔ Modulator

In section 3.6, we have studied and analyzed the MASH 1-1-1 modulator. To achieve low power design, a pipelining technique is applied to the design of the ΣΔ modulator. In addition, we also use *true single phase clock* (TSPC) techniques to implement the registers (D-flipflops) for saving power and area. The detailed circuit implementation of this ΣΔ modulator is discussed in this section.

A MASH ΣΔ modulator of any order can be pipelined. Figure 4.11 shows a pipelined, third order MASH 1-1-1 ΣΔ modulator by using the symbols introduced in Fig. 2.15. Each first order ΣΔ modulator is realized as a pipelined accumulator with feedback. In the quantization noise cancellation circuit, two delays are added to the first stage output path, and one delay is added to the second stage output path. The delays are used to compensate for the time delay incurred in the second and third stages. The output of the third stage is fed into filter $(1-D)^2$, and the delayed output of the second stage is fed into the filter 1-D. The detailed quantization noise

cancellation circuit will be described later.

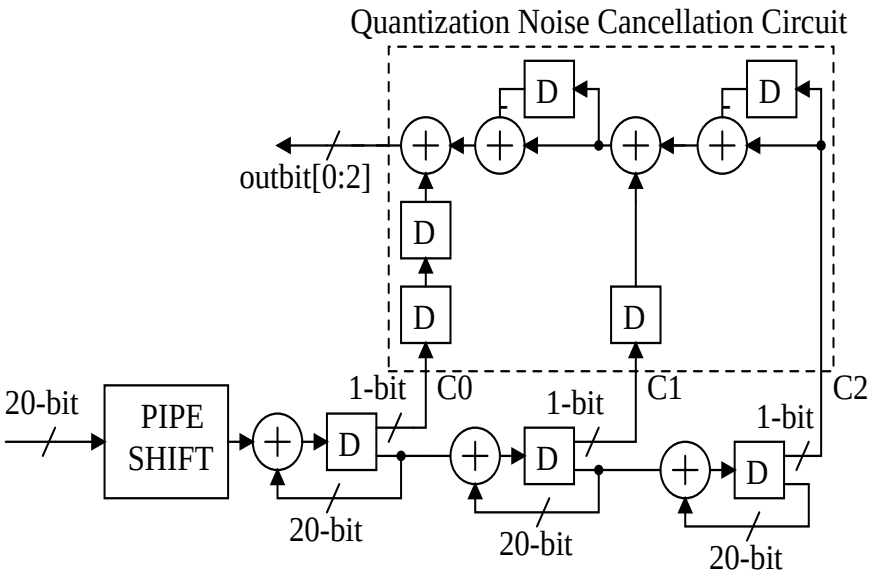


Figure 4.11: A pipelined third order digital MASH 1-1-1 modulator

The complete pipelined $\Sigma\Delta$ topology requires pipe shifting of its input data as shown in Fig. 2.15. In order to align the output data of the previous stage and the input data of the next input stage, the number of registers between each pair of adders (one belonging to the previous stage, the other belonging to the next stage) should be the same. So the registers between the first stage and the second stage, and between the second stage and the third stage can be completely eliminated in fractional-N frequency applications. We use the carry bits to control the multi-modulus divider, so the registers for aligning the output data of the third also can be completely cancelled. Therefore, only one pipe shift for the input data is left in the entire MASH structure. Without including the time alignment registers between stages and the output of the last stage, this design results in considerable savings

in area and power.

4.5.1 Quantization Noise Cancellation Circuit

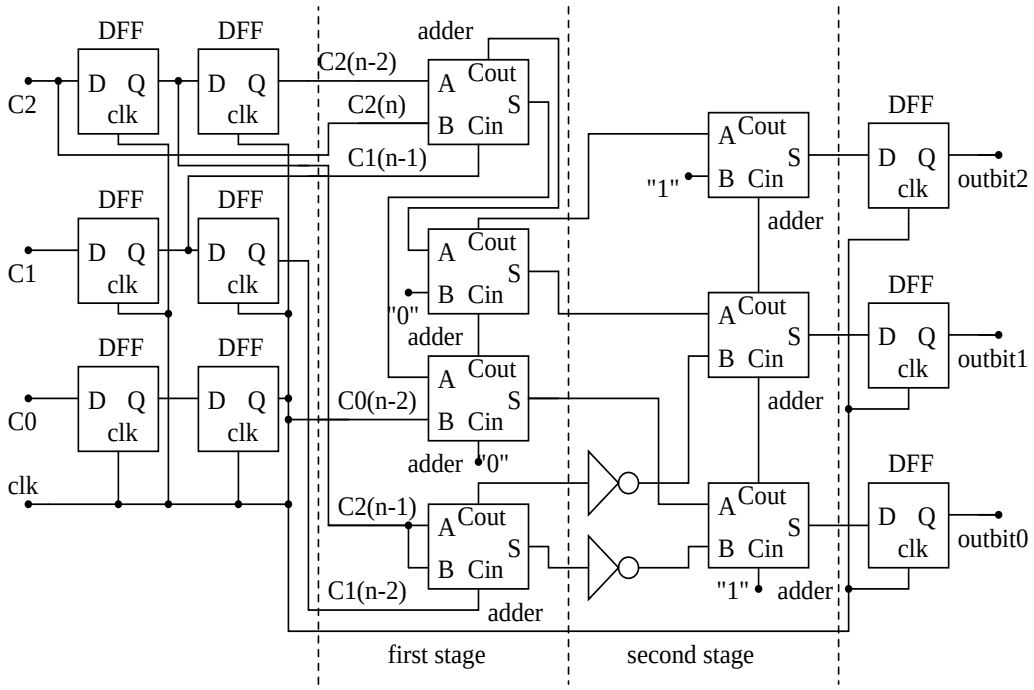


Figure 4.12: Quantization noise cancellation circuit for Fig. 4.11

Figure 4.12 shows the quantization noise cancellation circuit used in the MASH 1-1-1 of Fig. 4.11. The error cancellation circuit basically performs the following function:

$$Y(z) = C_0(z)z^{-2} + C_1(z)z^{-1}(1 - z^{-1}) + C_2(z)(1 - z^{-1})^2 \tag{4.10}$$

Where C_0, C_1 and C_2 (shown in Fig. 4.11 and Fig. 4.12) are the carry out bit of the first, second, and third accumulators, respectively. In the discrete time domain, Eq. (4.10) can be written as:

$$y(n) = C_0(n-2) + C_1(n-1) - C_1(n-2) + C_2(n) - 2C_2(n-1) + C_2(n-2) \tag{4.11}$$

There are two stages in the quantization noise cancellation circuit. The first stage performs the following add operations.

$$A(n) = C_0(n-2) + C_1(n-1) + C_2(n) + C_2(n-2) \quad (4.12)$$

$$B(n) = C_1(n-2) + 2C_2(n-1) \quad (4.13)$$

$A(n)$ is accomplished by using the top three 2-bit adders in first stage, and $B(n)$ is accomplished by the bottom 2-bit adder in the first stage, as shown in Fig. 4.12. we get that $A(n)$ can vary between 0 to 4, and $B(n)$ can vary between 0 to 3. So the range of $y(n)$ is between -3 t0 4.

output level	outbit2	outbit1	outbit0
-3	1	0	1
-2	1	1	0
-1	1	1	1
0	0	0	0
1	0	0	1
2	0	1	0
3	0	1	1
4	1	0	0

Table 4.6: Coding table for the MASH 1-1-1 output

The second stage is designed to realize $A(n)-B(n)$ to produce the final output. Two's complement of a binary number is easily performed for simple addition and substraction. So $A(n) - B(n)$ is realized by $A(n) + \overline{B(n)} + 1$. $\overline{B(n)}$ is B(n)'s inverse

binary number. We use three 2-bit adders to realize this function in the second stage. The output bits and their corresponding levels are shown in Table 4.6.

4.5.2 Mirror Adder and TSPC Register

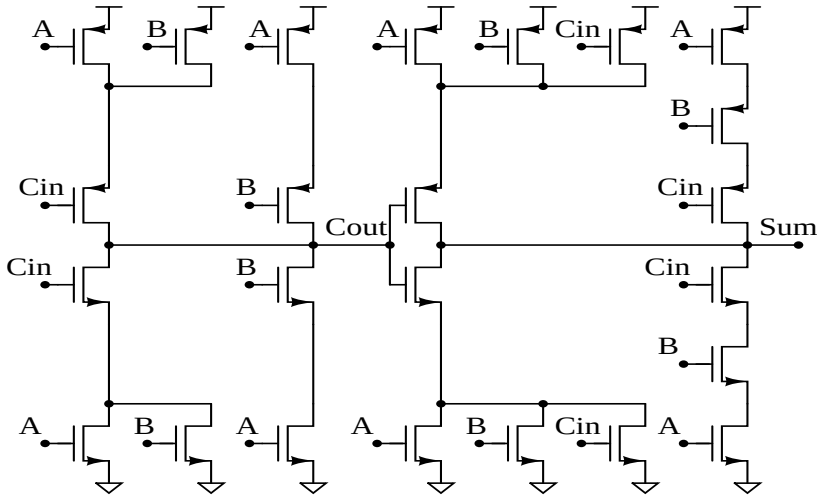


Figure 4.13: A static mirror adder circuit

The CMOS circuit for the adder used to implement the digital $\Sigma\Delta$ modulator is shown in Fig. 4.13. For PMOS transistors, their bodies are connected to the power source. And for NMOS transistors, their bodies are connected to the ground. It is a static mirror adder [81]. Generally, carry logic transistors are usually made much larger than their sum counterparts in order to speed up the carry chain. Since the carry chain has been pipelined in our circuit, there is no need for such large transistors. In the mirror adder circuit, the carry logic transistors are small, having roughly the same size as those implementing the sum logic. This design results in decreasing the area of the adder cell, which somewhat alleviates the increase in area caused by the pipelined registers.

Figure 4.14 shows the CMOS circuit of a True Single Phase Clock (TSPC) register. The TSPC technique simplifies the clocking scheme by allowing only one clock line. Moreover, it is a dynamic register. Compared with a static register, more power and area can be saved.

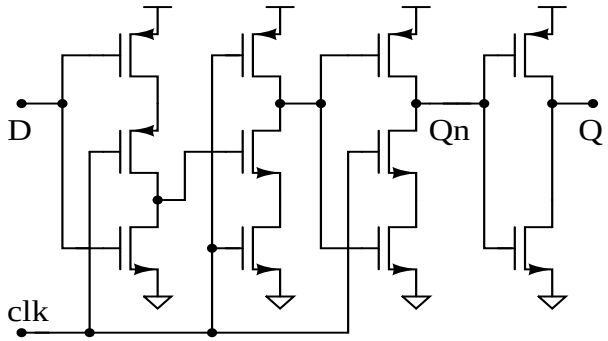


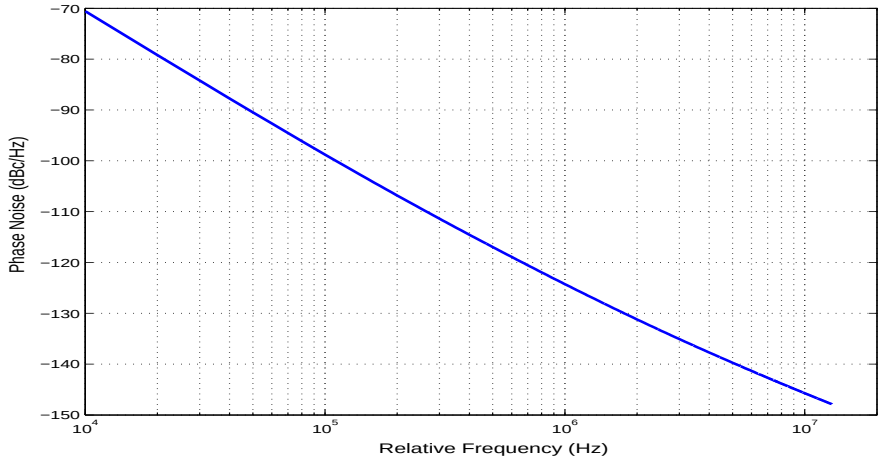
Figure 4.14: True single phase clock register circuit

4.6 Simulation Results

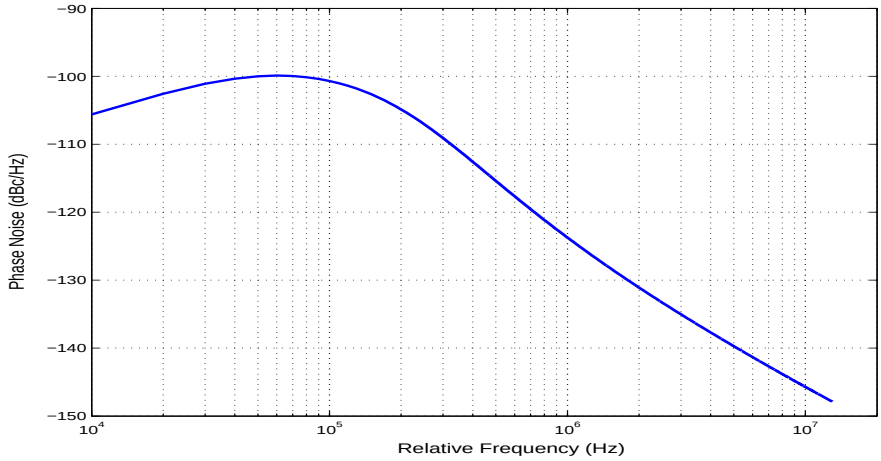
This $\Sigma\Delta$ fractional-N PLL synthesizer prototype has been simulated using data for the TSMC 0.18μm CMOS process. The design parameters of this PLL sysnthesizer are shown in Table 4.1 and Table 4.2. Cadence SpectreRF simulator is used for simulation. The phase noise of each block in the PLL is simulated separately. Matlab and Simulink tools are also used to calculate the corresponding phase noise of each block. The detailed simulation results are described as follows.

A. The VCO Block Phase Noise

Here we select the channel center frequency at $26MHz \times (78 + \frac{2^{18}}{2^{20}} + \frac{2^{17}}{2^{20}} + \frac{2^{14}}{2^{20}}) = 2038.15625MHz$. Now the average division ratio is 78.390625, and the modulator



(a)



(b)

Figure 4.15: Simulated phase noise of the VCO: (a) VCO block phase noise (b) The PLL phase noise due to VCO block

input number in binary is 01100100000000000000. With the center frequency at 2038.15625MHz, the subband of the wideband VCO should be set at $D_2D_1D_0 = 101$. The simulated VCO phase noise is shown in Fig. 4.15(a). From the figure, we can see the phase noise is -124.27 dBc/Hz at 1MHz offset frequency.

According to the transfer function of Eq. (3.42), we get the PLL output phase noise due to the VCO block as (for $s = j\omega$):

$$\overline{\phi^2_{out,vco}(s)} = \left| \frac{1}{Ms + K_{pd}K_{vco}F_{lpf}(s)} \right|^2 \cdot \overline{\phi^2_{vco,n}(s)} \tag{4.14}$$

The simulated PLL output phase noise is shown as figure 4.15(b). The comparison of the phase noise levels of Fig. 4.15(a) and Fig. 4.15(b) reveals that the VCO phase noise transfer function is a high pass filter. Therefore, the wider the loop bandwidth, the less VCO phase noise appears at the PLL frequency synthesizer output.

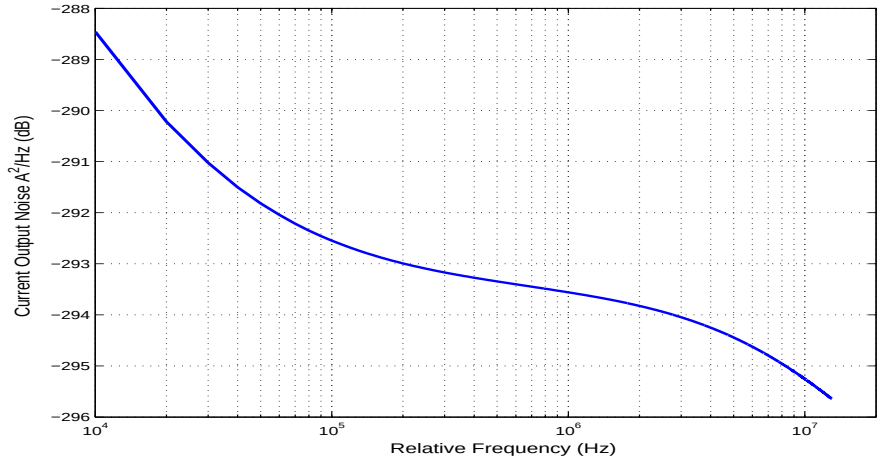
B. PFD/CP Block Current Noise

In our charge pump design, we use an amplifier circuit as feedback to reduce the output level of reference feedthrough. So, we should pay attention to the additional phase noise due to the feedback amplifier. As we know the PFD and charge pump together provide current noise in the PLL system. The simulated current noise of the PFD and charge pump together is shown in Fig. 4.16(a).

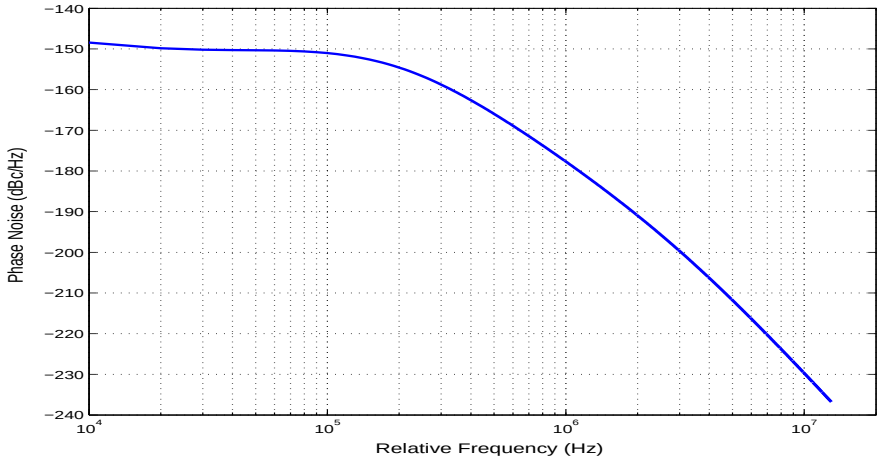
According to the transfer function of Eq. (3.40), we get the PLL output phase noise due to the PFD/CP current noise as:

$$\overline{\phi^2_{out,pfd/cp}(s)} = \left| \frac{MK_{vco}F_{lpf}(s)}{Ms + K_{pd}K_{vco}F_{lpf}(s)} \right|^2 \cdot \overline{i^2_{pfd/cp}(s)} \tag{4.15}$$

The simulated PLL phase noise is shown in Fig. 4.16(b). Compared with the PLL output phase noise caused by the VCO block of Fig. 4.15(b), the phase noise level due to PFD/CP is much lower. So, we can ignore the added amplifier's



(a)

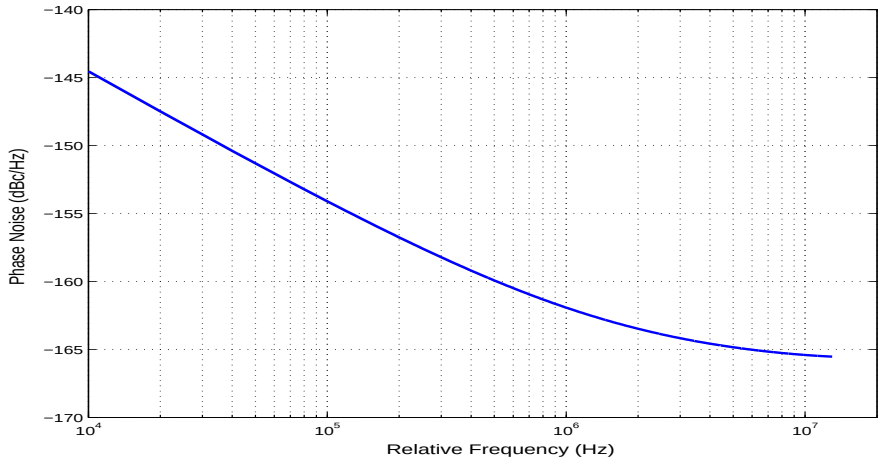


(b)

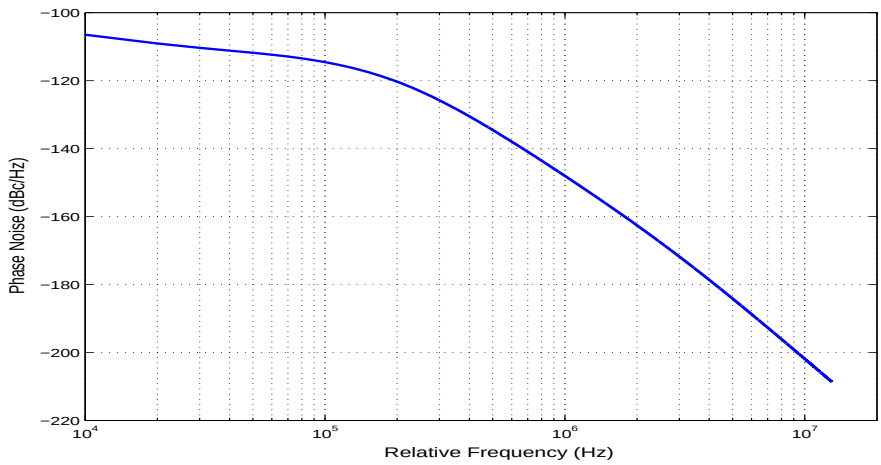
Figure 4.16: Simulated phase noise of the CP/PFD: (a) CP/PFD block output current noise (b) The PLL phase noise due to CP/PFD block

influence on the phase noise. The PFD/CP phase noise normally is the phase noise floor of a PLL system.

C. The Programmable Frequency Divider Phase Noise



(a)



(b)

Figure 4.17: Simulated phase noise of the divider: (a) divider block phase noise (b) The PLL phase noise due to divider block

If we use the integer-N PLL synthesizer, then the divide numbers are among $2038 \sim 2110$. Cadence SpectreRF simulator can not do PSS and Pnoise [83] analysis

of the whole divider at one time due to insufficient memory of our computers. In the fractional-N PLL frequency synthesizer, the combination of a ΣΔ modulator and multi-modulus divider together realizes the fractional division ratio. The channel spacing (the frequency difference between two adjacent channels) is independent of the reference frequency. By choosing 26MHz as the reference frequency, the division ratios ($78 \sim 85$) become much lower than those ($2038 \sim 2110$) in the integer-N PLL. So, we can use Cadence SpectreRF for PSS and Pnoise analysis directly. The simulated divider phase noise is shown in Fig. 4.17(a).

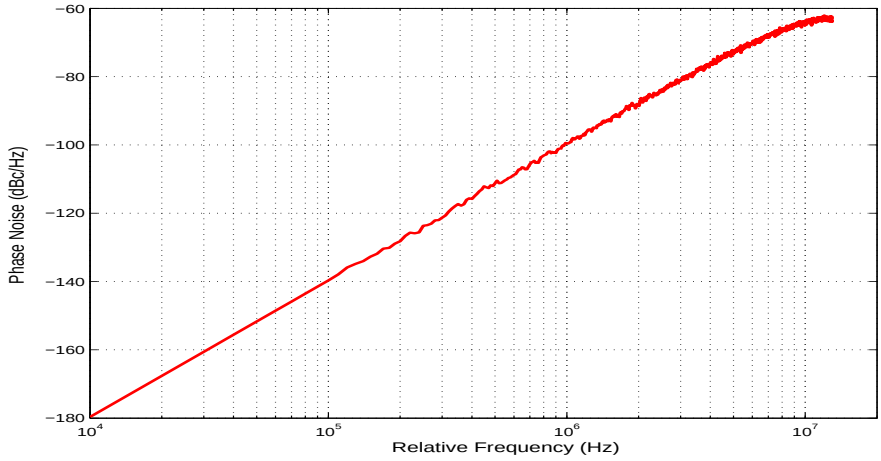
According to the transfer function of Eq. (3.40), we get the PLL output phase noise due to the PFD/CP current noise as:

$$\overline{\phi^2_{out,pfd/cp}(s)} = \left| \frac{MK_{pd}K_{vco}F_{lpf}(s)}{Ms + K_{pd}K_{vco}F_{lpf}(s)} \right|^2 \cdot \overline{\phi^2_{div,n}(s)} \tag{4.16}$$

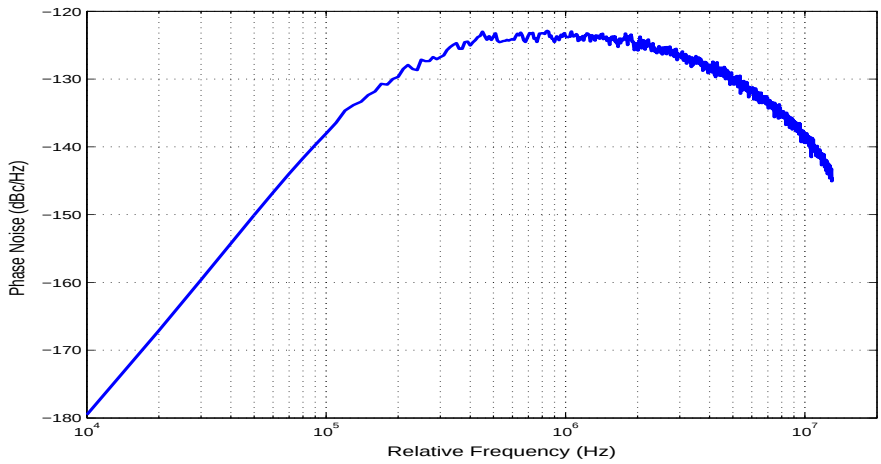
The simulated PLL phase noise is shown in Fig. 4.17(b). From this figure, we can see that the high frequency PLL phase noise due to the divider block is very low.

D. The MASH ΣΔ Modulator Phase Noise

The MASH 1-1-1 ΣΔ Modulator is chosen due to its high stability. From the Cadence and Simulink simulations of Fig. 4.11 and Fig. 3.26, respectively, we get 2^{18} output points of the modulator. The sample frequency is 26MHz. Then according to Matlab analysis results, the ΣΔ modulator output noise PSD (power spectrum density), $\overline{\phi^2_{\Sigma\Delta,n}(s)}$, is shown in Fig. 4.18(a). According to the transfer function of Eq. (3.108), we get the PLL output phase noise due to $\overline{\phi^2_{\Sigma\Delta,n}(s)}$ can be



(a)



(b)

Figure 4.18: Simulated phase noise of the 3rd-order MASH modulator: (a) ΣΔ modulator phase noise (b) The PLL phase noise due to ΣΔ modulator block

written as ($s = j\omega$):

$$\overline{\phi^2_{out,\Sigma\Delta}(s)} = \left| \frac{K_{vco}K_{pd}F_{lpf}(s)}{Ms + K_{vco}K_{pd}F_{lpf}(s)} \right|^2 \cdot \overline{\phi^2_{\Sigma\Delta,n}(s)} \tag{4.17}$$

The simulated PLL output phase noise due of the MASH ΣΔ modulator is

shown in Fig. 4.18(b). Figure 4.18(a) confirms the ΣΔ modulator noise shapping function: the higher the frequency, the higher the PSD of noise. And the high frequency noise is filtered by the loop filter as shown in Fig. 4.18(b).

E. The Overall Fractional-N PLL Synthesizer Phase Noise

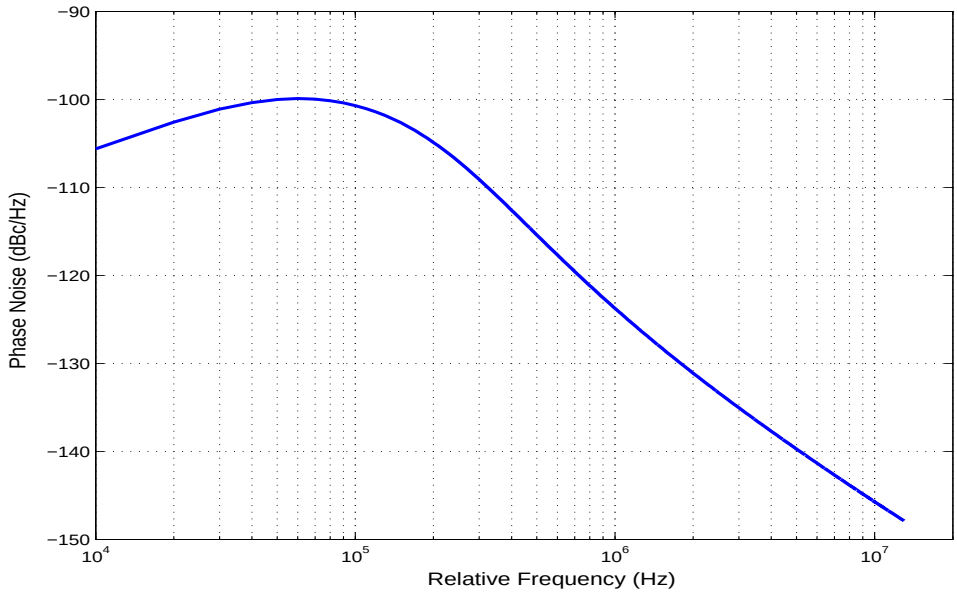
In the above, we have described in detail the simulated phase noise of the VCO, the PFD/CP, the divider, and the ΣΔ modulator in the fractional-N PLL synthesizer.

According to the linear phase noise model of Eq. (3.44), the total PLL output noise is can be expressed as ($s = j\omega$):

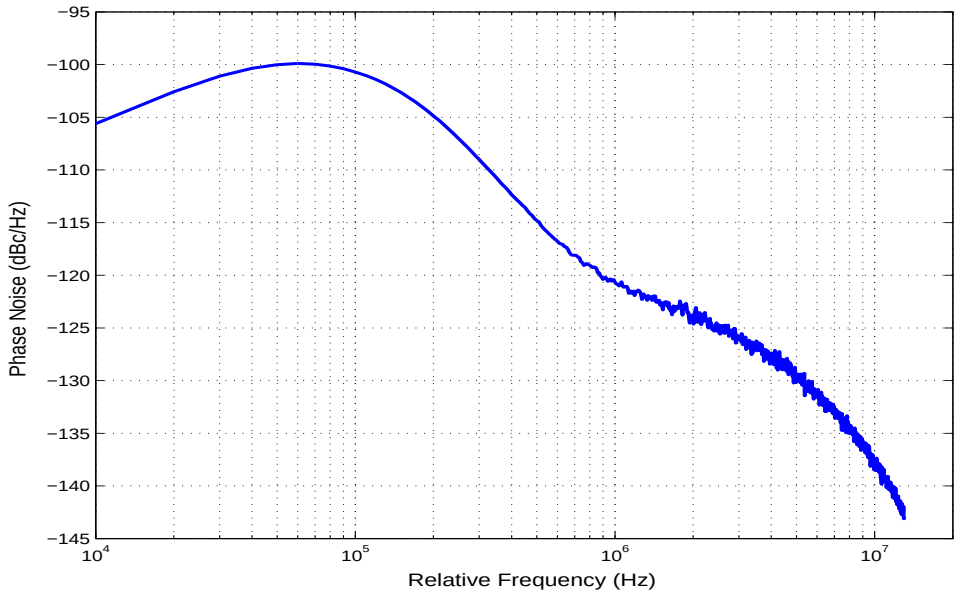
$$\overline{\phi^2_{out,n}(s)} = \overline{\phi^2_{out,vco}(s)} + \overline{\phi^2_{out,pfd/cp}(s)} + \overline{\phi^2_{out,div}(s)} + \overline{\phi^2_{out,\Sigma\Delta}(s)} \tag{4.18}$$

The simulated overall fractional-N PLL output phase noise with the ΣΔ modulator removed and in place are shown in Fig. 4.19. Comparison of Fig. 4.19(a) and Fig. 4.19(b) reveals that ΣΔ quantization noise has the dominant influence on phase noise performance at the intermediate frequencies (see section 4.1.2).

From this figure, we see that the overall ΣΔ PLL phase noise is -120.67dBc/Hz at 1MHz offset frequency. This phase noise is a little higher at 1MHz offset than that without ΣΔ modulator. Therefore, with the added ΣΔ modulator, the high frequency PLL phase noise is only a little degraded, but the PLL dynamic performance is improved a lot in the ΣΔ fractional-N PLL. As per the discussion below Eq. (4.3) in section 4.1.2, the locking time is much faster than that in an integer-N PLL with the reference frequency equal to 1MHz.



(a)



(b)

Figure 4.19: Simulated phase noise of fractional-N PLL: (a) ΣΔ modulator removed (b) ΣΔ modulator in place

4.7 The 2GHz LC VCO Measurements

A VCO chip was designed for a center frequency of $2GHz$ and fabricated in the TSMC $0.18\mu m$ CMOS process. Two NMOS source followers are used as an output buffer to drive a 50Ω measurement system. The measured results are presented here.

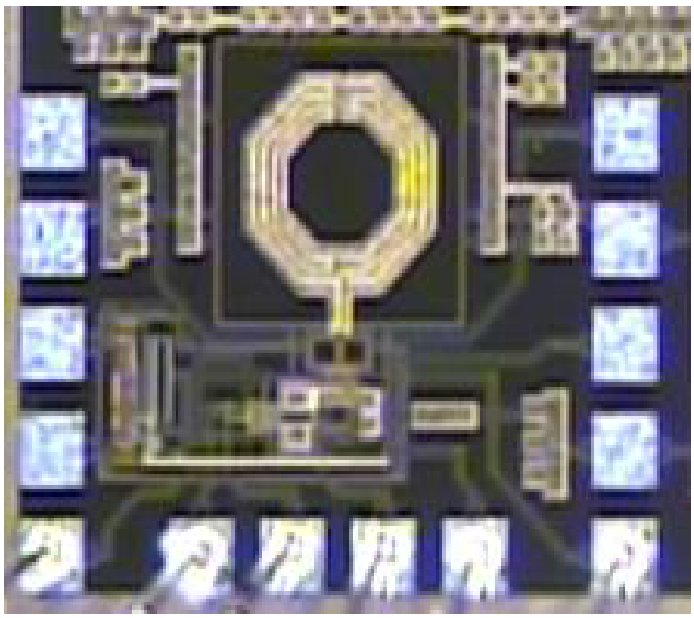


Figure 4.20: The Microphotograph of the VCO

A microphotogrph of the 2GHz VCO is shown in Fig. 4.20. The area measures $1100 \times 900\mu m^2$. The on-chip differential inductor can clearly be seen on the top. Underneath that, the tuning capacitors are placed, followed by the PMOS transistors and NMOS transistors. The inductor occupies $410 \times 410\mu m^2$, almost half of the area is contributed by the inductor coil. The rest of the die is occupied by PMOS and NMOS transistors and varactors for the VCO core, the output buffers, bandgap

reference, and the bonding pads. The VCO is encircled by double guard rings to minimize the substrate noise. The VCO core draws 2.2mA from a 3.3V power supply, thereby it consumes 7.26mW.

The VCO measured frequency tuning range with control voltage is shown in Fig. 4.21. When the control voltage changes from 1.2V to 2.7V, the center frequency changes from 1.81GHz to 2.13GHz. The measured frequency is about 150MHz lower than the Cadence SpectreRF simulation results because the parasitic capacitance has some influence on the oscillating frequency. But we find the measured frequencies match the post layout simulation results very well.

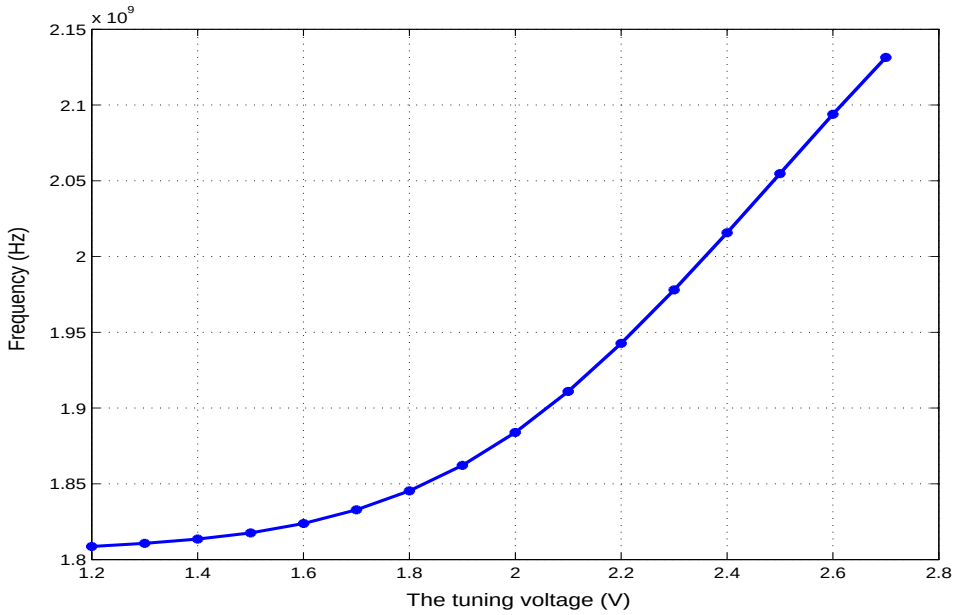


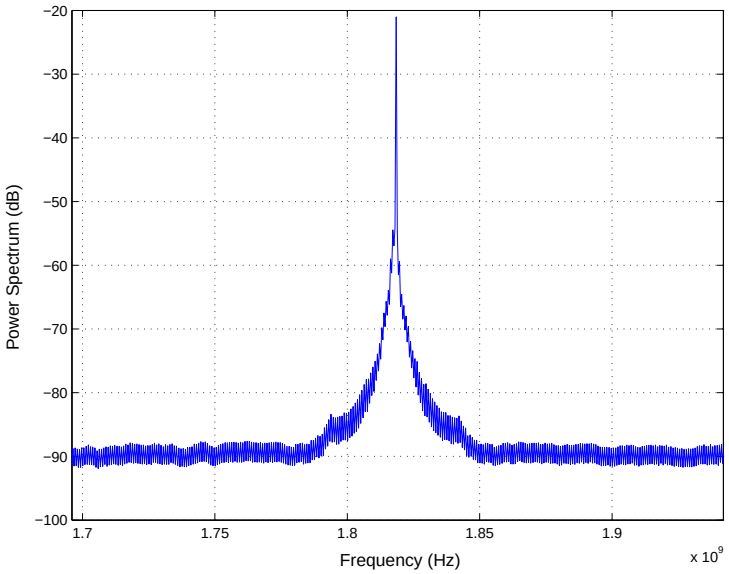
Figure 4.21: The VCO tuning range

The power spectrum of the VCO is measured by using an Agilent 8564EC Spectrum Analyzer. The measured output power spectrum is shown in Fig. 4.22.

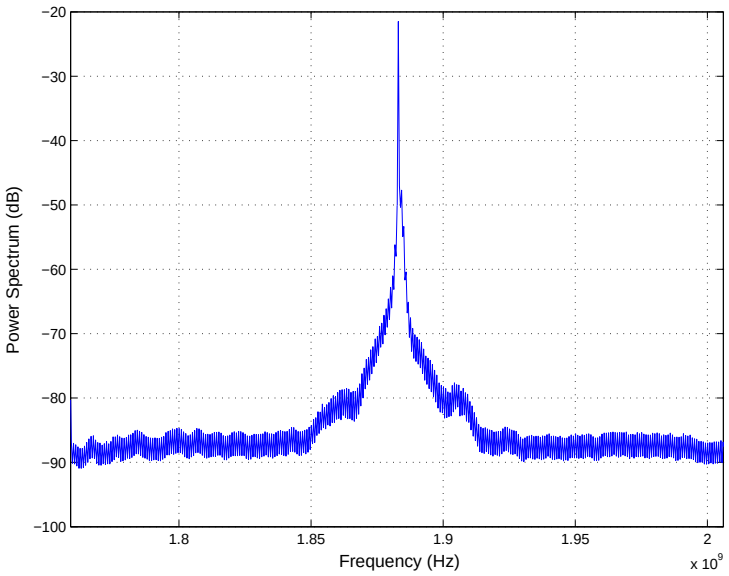
The spectra are measured with resolution bandwidth 30KHz. When the control voltage is 1.5V, the center frequency is 1.817GHz as shown in Fig. 4.22(a). And when the control voltage is 2.0V, the center frequency is 1.884GHz as shown in Fig. 4.22(b). So the VCO center frequency gets larger as the control voltage gets larger. From the figure, we see that the larger center frequency, the worse the phase noise, because both spectra are obtain at the same bias current $I_B = 2.4mA$.

4.8 Conclusions

This chapter presented the design of a 2.4GHz $\Sigma\Delta$ CMOS fractional-N frequency synthesizer, and the simulated and measured results. The frequency synthesizer is designed that takes advantage of a $\Sigma\Delta$ modulator to a very fine frequency resolution and relative large loop bandwidth. A low power wideband VCO with low VCO gain (100MHz/V) and wide tuning range (1.897GHz $\sim$ 2.472GHz), a 64/127-modulus divider, a 3rd-order MASH $\Sigma\Delta$ modulator, and other low-frequency components of a PLL form a complete prototype synthesizer. The resulting circuit is a 4th-order charge pump PLL. The VCO uses a 3.3V power supply, and the bias current range is 2.0mA $\sim$ 2.8mA. A 26MHz reference frequency is used. The loop bandwidth is 150KHz. The whole PLL phase noise is -122dBC/Hz at 1MHz frequency offset.



(a)



(b)

Figure 4.22: Measured VCO spectrum when span=250MHz, Resolution bandwidth=30KHz, and $I_{bias} = 2.4mA$: (a) Control voltage $V_c = 1.5V$, (b) Control voltage $V_c = 2.0V$

Chapter 5

Summary and Future Work

5.1 Summary

This research focuses on the design techniques of PLL-based frequency synthesizers. Using the theory and circuits developed, a 2.4GHz fully integrated $\Sigma\Delta$ fractional-N frequency synthesizer prototype is designed in TSMC 0.18μm CMOS technology. Efforts have been put on the new design of VCO, charge pump and $\Sigma\Delta$ modulator.

As stated in section 3.2, the phase noise of a voltage controlled oscillator (VCO) is the main contributor of the out of band phase noise of a frequency synthesizer. In section 3.3.1, based on the study of the VCO phase noise mechanism and improving on the literature results of Kong's [51], a design-oriented phase noise model for a complementary cross-coupled LC VCO is provided. The model combines linear small signal analysis and non-linear large signal concepts. It is used to predict the phase noise performance from circuit parameters. By using this model, we theoretically analyze the circuit parameters' influence on the phase noise performance for both narrow band VCOs and wideband VCOs operating in a current-limited region and in a voltage-limited region, separately. A $2GHz$ low phase noise CMOS LC VCO was designed and simulated in section 3.3.3 and the fabrication results are given in section 4.7. The simulation results confirm the proposed VCO phase noise model.

Due to the parasitic capacitance, the measured VCO center frequency is about 150MHz lower than the simulated VCO center frequency. The VCO gain is very critical to the overall PLL phase noise. Decreasing the VCO gain, the PLL output noise due to phase frequency detector and charge pump (PFD/CP) and low pass filter (LPF) contribution is dramatically decreased. With our LC VCO phase noise model, we also designed a low phase noise wideband VCO with the typical VCO gain around 100MHz/V and a constant output level in section 4.2.

The charge pump linearity is very important to the reference spur and the phase noise. A complete quantitative analysis of reference spur is given in section 3.5. Two main mechanisms - leakage current in the loop filter and current mismatch in the charge pump current source are investigated, and their contributions to spurs are analyzed independently. To reduce the current mismatch between the *up* branch and the *down* branch, a negative feedback circuit and replica bias are used. In addition, low-impedance charge/discharge paths are provided to overcome the charge pump current glitches caused by the charge injection.

For our design, a digital $\Sigma\Delta$ modulator is used to control the instantaneous frequency division ratio for fractional-N PLL synthesizers. With a large bit-width high order $\Sigma\Delta$ modulator, the PLL frequency resolution can be very fine, and the loop bandwidth can be increased without deteriorating the spectral purity. A 3rd-order MASH 1-1-1 digital $\Sigma\Delta$ modulator is designed in section 4.5. To achieve a low power design, pipeline techniques are used to implement the accumulators. These techniques are used to delete the critical path delay for carry information in accumulators. Moreover, *true single phase clock* (TSPC) techniques are used to

design the registers (D-flipflops) for further saving power and area.

To confirm the developed PLL blocks, a fully integrated 2.4GHz $\Sigma\Delta$ fractional-N CMOS PLL frequency synthesizer is designed. It takes advantage of a $\Sigma\Delta$ modulator to get a very fine frequency resolution and relative large loop bandwidth. The low power wideband VCO with tuning range (1.897GHz $\sim$ 2.472GHz), the new charge pump, the 3rd-order MASH 1-1-1 $\Sigma\Delta$ modulator, a 64 modulus divider (64 $\sim$ 127), and other low-frequency components of a PLL form a complete prototype synthesizer as per the block diagram in Fig. 4.1. The resulting circuit is a 4th-order charge pump PLL. A $26MHz$ reference frequency is used in this PLL frequency synthesizer. The loop bandwidth is about $150KHz$. The simulated whole PLL phase noise is -120dBc/Hz at 1MHz frequency offset.

5.2 Future Work

In our proposed LC VCO phase noise model, we only consider the devices thermal noise. Close to the VCO oscillation frequency, the slope of the phase noise spectrum is from -20 to $-30dB/dec$. This is ascribed to the upconversion of flicker noise. When the oscillator is not carefully designed, flicker noise can deteriorate the phase noise at higher offset frequencies important for communication systems. The $1/f$ noise has become an important issue in design at deep submicron levels. The physical process for the conversion of $1/f$ noise to phase noise remains unclear. In future work, $1/f$ noise in the LC VCO should be analyzed and the LC VCO phase noise model should include $1/f$ noise effects.

The multi-modulus divider is one of the main power consumption blocks in our fractional-N PLL frequency synthesizer. Further reduction of the PLL power consumption should begin with this component. A promising method is to use alternative technologies, such as advanced CMOS processes, to achieve the high speed requirements of the divider circuits at lower power levels. From an architectural standpoint, new topologies can be used for the $\div 2/3$ divider. One interesting method is to use totally different structures such as dynamic frequency dividers.

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