ABSTRACT

Title of Document: VERTICALLY INTEGRATED MODULES FOR LOW POWER EMBEDDED SENSOR SYSTEMS

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A typical embedded sensor system consists of an environmental sensor, data storage, and a control circuit (such as a microcontroller). Two main traits desired of these embedded sensor systems are small form factor and low power consumption. However, due to the diverse nature of the design and applications, monolithic solutions incorporating the three main components are often not available on a large cost effective scale.

This work describes a method of integrating heterogeneous circuit components into a single module. When combined with efficient operating algorithms the system size is reduced and lifetime is extended. Production or custom designed component chips are thinned and stacked vertically while interconnects are fabricated within the module providing a 3-D integration (3DI) of the system. A Global Positioning System (GPS) location recording sensor system is designed with the intention of applying the 3DI process to reduce its size and power consumption.

VERTICALLY INTEGRATED MODULES FOR LOW POWER EMBEDDED SENSOR SYSTEMS

By

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1. Introduction

1.1 Embedded Sensor Systems

Remote embedded sensor systems are defined as having three main components; a sensor which outputs a digital or analog stream of data taken from its environment (such as temperature, pressure, or location), a storage method such as a static or dynamic random access memory (S/DRAM) or electronically erasable programmable memory (EEPROM or flash), and a controller capable of executing a closed loop operating code such as a microcontroller (MCU) or microprocessor. The CMOS wireless revolution has enabled low cost wireless transceivers allowing for a simple means of data transfer and retrieval. Thus radio frequency (RF) transmitters are now often included in remote embedded sensor systems.

These systems are used in a diverse array of applications. An example of an embedded system is a GPS tracking unit. A small device containing a GPS sensor is affixed to a subject and records its location over a period of time. Tracking endangered species such as sea turtles is one potential use [1]. In this case, location data is collected and transmitted via sonar to a remote observer so retrieval of the device is not required. Military personnel and emergency responders are additional applications for tracking subjects. Knowledge of specific troop locations on a battlefield is invaluable in making informed decisions. The risk of casualties from friendly fire can be substantially reduced when the “fog of war” is lifted. If an emergency first responder is forced to go into a dangerous situation, their location and vital signs can be monitored remotely. If the responder comes under duress in a hazardous situation, their location and vital signs are readily available. Remote

embedded systems can also be used in monotonous applications reducing the need for human monitoring of subjects such as the weather.

The main traits desired of remote sensor systems are small size and long lifetime. With a reduced footprint the systems become less obtrusive resulting in better observations of their environment. To minimize maintenance, the system must be able to operate continuously for extended periods of time with no operator input. This requires robust operating code and a substantial battery lifetime. Designing a system with 3 Dimensional Integration (3DI) and intelligent control algorithms helps achieve the goals of small size and low power consumption.

Sensor system miniaturization can be achieved with simple means such as an ergonomic layout of a system on a printed circuit board (PCB) or using complex application specific integrated circuits (ASIC) stacked on top of each other and wire bonded to a substrate as in modern cell phones [2]. High end circuits using Silicon on Insulator (SOI) technology allow for vertical routing through the substrate to underlying circuitry [3]. The ability to stack and connect ICs directly without a PCB is a substantial benefit of SOI. The 3DI process attempts to extend this ability to standard silicon bulk integrated circuits (IC). The process provides the benefits of stacking and interconnecting circuits using the vast catalog of silicon based components available commercially off the shelf (COTS). The infrastructure for silicon chips vastly exceeds any other semiconductor technology or derivatives [4] so a vertical integration process extending to this technology would greatly increase the flexibility of embedded systems in general. Stacking chips to reduce component foot print and increase inter-chip connectivity is the goal of the 3-dimensional integration

(3DI) project. Presenting 3DI with an effective battery management algorithm to design a small, long lasting embedded system is the goal of this thesis.

1.2 3-Dimentional Integration

The 3DI process described in this work is under development for the purpose of creating a multi-chip module in which several ICs are stacked and connections are made directly through the bulk of the chip substrate. While the benefits of greater internal connectivity require specially designed circuits, the process can also be applied to production components, merging two parts into one module. An example would be the microcontroller and flash memory combination discussed later. The processes developed are divided into three main groups: wafer thinning, wafer bonding, and via production. Applications to production components also include die de-packaging, qualification and wafer re-integration.

Wafer thinning is required to reduce the chip's bulk such that fine pitch vias can penetrate through the substrate and be filled with a conductor. Thinning takes place in three phases. A coarse mechanical grind removes the majority of the bulk at a high rate. A chemical etch thins the substrate to within several microns of its target thickness. Finally a chemical mechanical polishing (CMP) step produces a clean mirror finish so the substrate can be bonded to a handle wafer or system stack.

Surface activation bonding is employed to create the system wafer stack. No bonding medium such as polyimide or benzocyclobutane (BCB) [5] is required. Instead a silicon or oxide surface layer is plasma treated to clean the surface of particles and native oxide, leaving behind an activated surface ready to accept

hydrogen or oxide bonding. When contacted with another active surface, the two wafers spontaneously bond without the use of an adhesive that could interfere with further processing.

The via etching process creates high aspect ratio vias through a silicon substrate. A highly directional magnetically coupled plasma field bombards the silicon through an oxide mask creating fine pitch (1μm) vias with an aspect ratio demonstrated at 20:1. The vias are then filled with an aluminum germanium alloy under high pressure creating an electrical connection to interconnects below.

Combining all of these processes creates a stack of various wafers or chips acting as a single module. While certain layouts and via connections are only possible with custom circuit designs, a hybrid module is also possible with production components. The majority of COTS chip packaging material dissolves in acid solutions leaving die behind. When possible die are purchased before they are packaged. These die are mapped and interconnect layouts are designed based on the pad locations. The die are then reintegrated onto a handle wafer for 3DI processing. The module is now prepared for use in embedded sensor systems.

1.3 System Design

To demonstrate the benefits of the 3DI process, a remote embedded sensor system is designed. The system is a remote Global Positioning System (GPS) Recorder Transmitter (GPS-RT) tracking unit composed of a microcontroller, programmable transceiver, flash memory, GPS module, and an accelerometer. The remote unit connects to a base station for operational maintenance and battery

charging. The use of COTS components makes it an ideal platform to examine the production applications of 3DI. Two main system components, the flash memory and the microcontroller, are de-packaged in preparation for 3DI. Each device is mapped and layout patterns are designed.

The system's many components require an effective power management algorithm. To extend the operating lifetime all components must have a power down feature. In the case of the GPS-RT, the system need only be operational during radio communication or when it is in motion with a valid position fix. Based on position and accelerometer data, the microcontroller decides which components must be active. To minimize power consumption of the microcontroller, the firmware is set up as an interrupt driven state machine which defaults to a low power sleep mode. The software's modular implementation allows for quick error recovery during extended field operations.

The following chapters present each 3DI technology and GPS-RT design choice in detail. Experimental results of novel and established processes are included. An overall description of 3DI is given to illustrate how each process fits into the system design. The relationship of software development to the GPS-RT sensor components is discussed.

2. 3-Dimensional Integration

2.1 Overview

3DI involves three processing stages; wafer thinning, wafer bonding, and via etch/fill. These stages are combined as shown in figure 2.1 to create multilayer circuits. After a base layer is prepared, wafer thinning reduces the substrate bulk of the second layer to a thickness that is penetrable by the via etch process. The process includes gluing a handle wafer to the device wafer, back grinding, chemical etch, and chemical mechanical polish (CMP), to reduce substrate thickness to 20μm.. A high degree of surface uniformity and no damage to the active circuit from heat or stress to the crystal structure are required since active devices are processed. In preparation for the bonding stage, the total thickness variation (TTV) across the surface of the wafer must be less than +/-1μm and the surface must also be virtually particle free with a maximum of 100 particles of 1μm or smaller.

After thinning, argon plasma treatment activates the substrate for surface activation wafer direct (SAWD) bonding to build the wafer stack. Plasma chemistry, exposure time, vacuum pressure and native oxide growth affect bond strength. A scanning acoustic microscope (SAM) and infra red (IR) camera detect voids in the bonding interface and measure crack propagation in fracture testing to determine bond strength.

A novel high aspect ratio (HAR) via etch process produces fine pitch (1μm) vias at a depth of 20μm. Via sidewalls must be scallop free for Al filling eliminating technologies such as Bosch deep reactive ion etching (DRIE). A passivation catalyst moderates the etch reaction to avoid sidewall pitting from focused ion bombardment

in a Trikon magnetic field=0 resonant inductance (M0RI) plasma chamber. A passivation layer is simultaneously grown along the sidewall to insulate the via from the substrate. To prevent aluminum interconnects from spiking through the sidewall and assist the via fill process, a barrier layer of titanium nitride (TiN) is deposited throughout the via. The final metallization step deposits an aluminum germanium alloy that is forced into the via by plastic deformation under high pressure. A post process CMP step planarizes the resulting metal layer for interconnect patterning. This chapter describes each of these technologies in detail along with presenting achieved process capabilities.

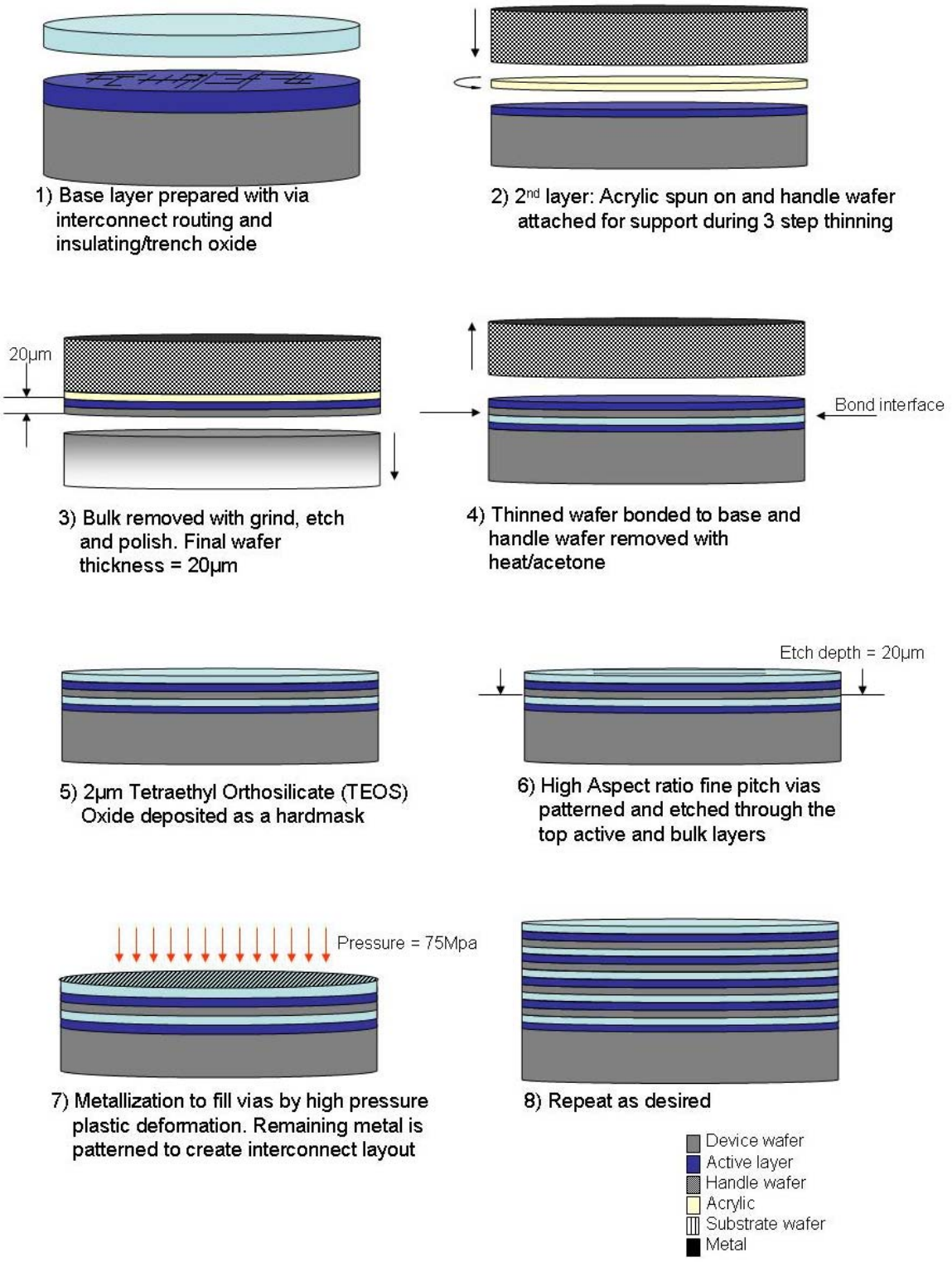

Fig 2.1. 3DI process flow

2.2 Wafer Thinning

The 20μm substrate thinness requirement imposed by the 3DI silicon via etch requires a low stress wafer thinning process. Standard production thinning methods incorporate a mechanical substrate back-grind with a diamond wheel. A coarse (350-500 grit) wheel is used for efficient removal and a fine (2000-3000 grit) wheel reduces surface roughness and removes damaged crystal planes [6]. Forces applied during the grinding process also create sub-surface defects in the wafer [7]. To prevent sub-surface damage and provide stress relief of ultra-thin (~25μm) circuits, the wafers are chemically etched after the grind. CMP produces a mirror finish on the backside of the wafer in preparation for further processing.

The three phase thinning process consists of a coarse grind, fine chemical etch, and finishing polish. Starting with a 650μm wafer, the coarse grind step removes up to 525μm with a Strassbaugh 150mm wafer grinder. The etch step uses a hydrofluoric, nitric, acetic, and sulfuric acid solution to chemically remove additional substrate bulk until the substrate is within a few microns of it's target thickness. Finally a Strassbaugh 6EC CMP tool produces a clean, mirror finish surface to prepare the wafer for further 3DI processing steps (including bonding).

Thickness measurements are taken with a Proforma 300 non contact thickness gauge. Two terminals form a parallel plate capacitor where a wafer is inserted. The change in permittivity from free space to that of the substrate is related to capacitance by:

$$C = \varepsilon \frac{A}{d}$$

where A is plate area, d is distance between plates and ε is permittivity of the substrate. The resulting capacitance is translated into a thickness measurement of the substrate with a resolution of 0.05μm. The system is calibrated with a blank silicon wafer of known thickness 672.7μm. TTV and thickness standard deviation are calculated from 5 points chosen such that the maximum and minimum thickness of the wafer are recorded. Defects such as cracks or bonding voids are not considered in thickness characterization.

2.2.1 Grinding

Low TTV and efficient bulk removal are benefits of wafer grinding [8]. When handle wafers are used (as in 3DI) the resulting TTV of the device wafer is dependant on the TTV of the handle wafer and the planarity of the bond [9]. This factor is important to consider when developing a technique for re-integrating die for batch processing. Variations in die placement will result in die thickness variations as well. Additional properties and results of die grinding are discussed in section 3.

Using industry standard 6" wafer grinding tools the substrate is thinned to approximately 125μm. Various bonding techniques (discussed in section 2.3) join the device layer to the handle wafer. Low TTV Results of back grinding are shown in table 2.1

Wafer	Bulk Removal (μm)	TTV (μm)	Bond Type
1	522	1.6	acrylic
2	522	2.3	bcb
3	453	2.2	wax
4	526	1.65	plasma
5	527	3.45	plasma
6	525	2.3	plasma
7	524	2.4	plasma

Table 2.1 Wafer Grinding Total Thickness Variation

Average starting stack thickness is 1.3mm and removal is approximately 525μm. When comparing average removal to the average TTV (2.27μm), the TTV/removal ratio is approximately 0.4%, significantly lower than chemical etch rates discussed in section 2.2.2. Surface roughness is measured with an atomic force microscope (AFM) which shows a height variation of 260nm, below the 1μm bonding requirement, and a linear scoring pattern shown in figure 2.2. Additional techniques such as electrolytic in-process dressing (ELID) have been shown to further improve the resulting TTV and mitigate surface damage [8].

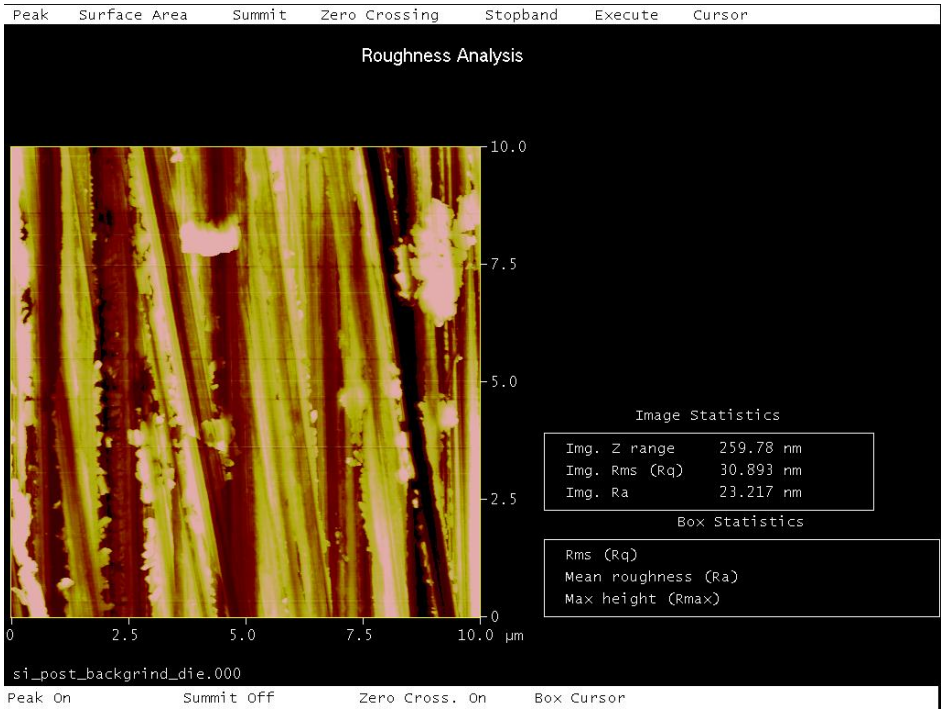

Fig 2.2. Surface roughness after mechanical grinding

2.2.2 CHEMICAL ETCHING

Various acid solutions are used to chemically etch the silicon substrate. The process uses a combination of Hydrofluoric acid (HF) and Nitric acid (HNO_3) as the reactants and Acetic acid (CH_3COOH) as a buffer. The etch chemistry is referred to as HNA. The silicon removal is an oxidation reduction reaction in which silicon is oxidized becoming SiO_2 while nitric acid loses an oxygen atom [11].

$$2Si + 4HNO_3 + 8\,HF \rightarrow 2SiO_2 + 4HNO_2 + 8HF$$

Oxidation reduction HF etch

$$2SiO_2 + 4HNO_2 + 8HF \rightarrow 2SiF_4 + 4HNO_2 + 4\,H_2O$$

HF etching of SiO_2

Several techniques exist to process with HNA including chemical bath immersion, spin/spray etchers, and meniscus etchers. Chemical bath immersion submerges a wafer into a chemical etch solution. Etching occurs on both sides of the wafer. Since wafers must be dipped into the solution, the bottom of the wafer is etched for a longer period of time resulting in a wedge shaped profile and an increase in TTV. This method is not suitable for post processing of active devices since the device side or handle wafer is etched when the stack is fully submerged. Spin/spray etchers allow a much higher degree of control. The wafer is held by a high speed rotating chuck while a nozzle sprays only the process side with the etch solution. This method protects the active layer and carefully controls the chemistry of the solution resulting in a well controlled reaction. However, 3DI systems with reintegrated die wafers create irregular surfaces at the die edges. The discontinuity disrupts fluid flow as the stream crosses the die edges resulting in radial etch striations.

The chemical etch is performed with a MATECH Wave Etch wet processing system. The main components of the system are a robotic wafer chuck, process module, rinse module, dry module, and valve matrix. The device uses diaphragm pumps to precisely meter a desired chemical mix into process liquid tanks through a valve matrix as shown in figure 2.3. A pneumatically operated circulation pump controls the fluid flow in the machine and delivers the chemical mix to the process module. The process module consists of a 180 mm x 10 mm bath in which a meniscus is formed. The height of the meniscus is constant (approximately 2mm) and limited by the flow rate of the circulator pump. Once a stable meniscus is formed, the robotic chuck pulls a wafer from a loading cassette and begins exposing the backside of the

wafer to the process mixture. A nitrogen gas curtain is formed around the chuck to prevent fumes from the reaction from etching the device side of the wafer. Once the process is completed the wafer is moved to a rinse module, similar to the process module, in which remaining process reactants are rinsed from the wafer. The meniscus is created from de-ionized (DI) water fed directly from the facility DI supply line. Contaminated rinse water is not recycled and expelled to the facility chemical drain. After the wafer is rinsed, it is spun dry and then returned to the cassette.

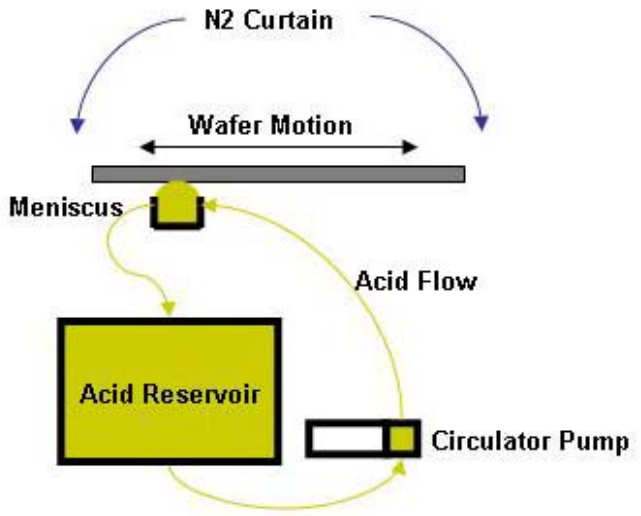

Fig. 2.3 Meniscus etcher processing diagram

In characterizing the HNA meniscus etcher, the relative acid concentrations and volume of solution was varied. Although higher temperatures increase the reaction rate, reaction temperature is maintained at 30°C for safety reasons. Since the HNA chemistry requires dislocated Si ions to react, new mixtures require a conditioning period in which the etch rate rises until the solution is saturated. The reaction begins to slow (as determined by a decrease in etch rate) as the HF reacts

with SiO_2. At a certain point the reaction rate drops by 80%-90% when there is an insufficient amount of HF to maintain the reaction as shown at the 10 minute mark of figure 2.4a. Replenishing the solution with additional HF increases the etch rate, however the new rate is currently unpredictable. The volume of HNA is related linearly to the time at which the etch rate drop off occurs. For mixtures with smaller percentages of HF, the drop in etch rate is less severe and follows a nearly linear trend (figure 2.4b).

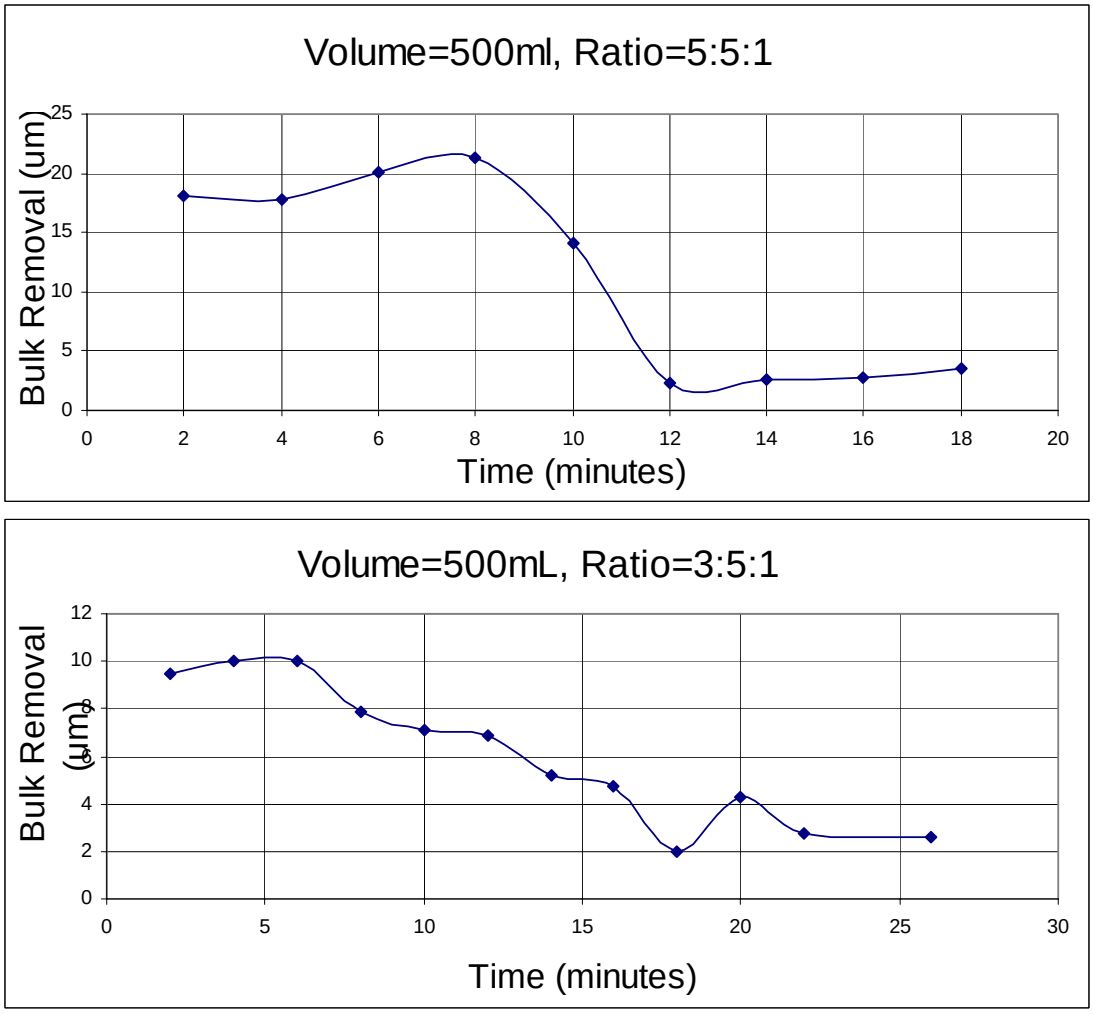

Fig 2.4 a (top),b (bottom) Wet processing removal rates. Wafer thickness is measured in 2 min and change in thickness is displayed for various etch ratio of HNA and volumes. Top: HNA=5:5:1, 500ml. Bottom: HNA=3:5:1, 500ml.

These trends are instrumental in determining etch time. Wafers must be continually etched to target thickness and cannot be measured during processing. Discontinuous etch processes (in which the wafer is rinsed, dried and measured before reaching target thickness) produce charring and burn marks across the process side of the wafer, partially due to acid residue buildup after the initial rinse (as determined by pH testing of rinse water droplets). Charring is especially severe with aggressive chemistries (high HF concentration).

TTV displays a somewhat linear trend with time as shown in figure 2.5. The best results achieved with continuous etch of die wafers show a TTV of approximately 5% of bulk removal. Target bulk removal is generally 100µm meaning a resulting TTV of 5µm after chemical etch. CMP Generally increases TTV but in this case it will be required to planarize the wafer for bonding. Additional buffers such as Sulfuric acid can potentially increase the etch quality of HNA. Characterization of the HNA reaction with sulfuric acid is required to produce a viable chemical thinning process.

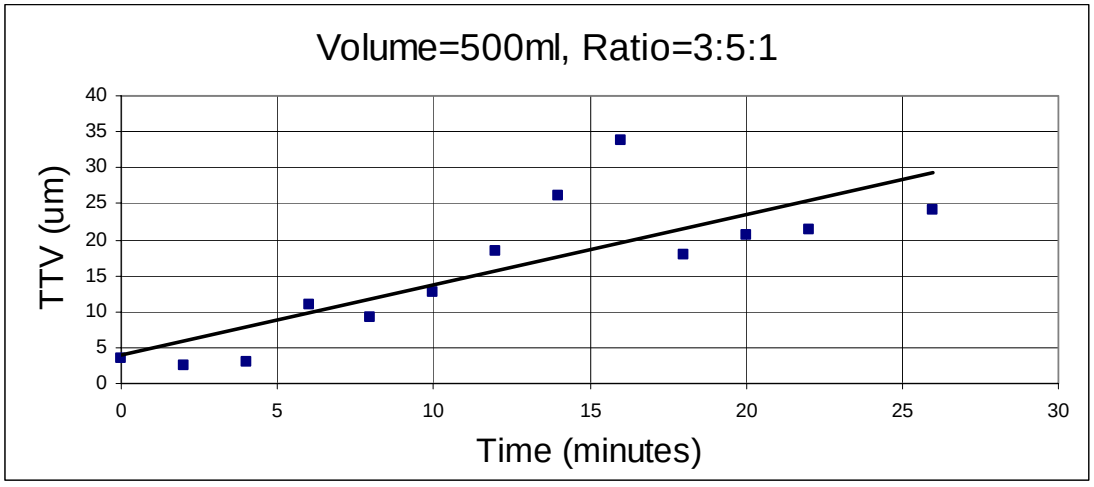

Figure 2.5 Drastic increases in wafer TTV with process time using aggressive chemistry.

To determine the etch time required to reach a target thickness; a conditioning wafer is processed for 10 minutes to initialize the reaction. The removal rate (in μm/min) is used to calculate the total required etch time. Etch rate is assumed to remain constant for 30 min for each liter of solution based on rate charts in figure 2.4. Once the etch rate drop off point is reached the solution is drained and a new batch is mixed. The remaining bulk must be removed during CMP to remove etch scarring and balance TTV.

2.2.3 Chemical Mechanical Polishing

The Strassbaugh 6EC CMP tool consists of a rotating polishing table with a nylon micro-fiber surface onto which 70nm particle alumina slurry is dispensed. The wafer is held by a rotating polishing head capable of maintaining a constant force on the wafer. To attain a high quality polished planar finish requires precise control of the polishing slurry. Most silicon polishing is done with alumina or silica based oxide slurries which tend to agglomerate into large particles and cause defects in the polished surface [13]. To avoid these defects, the slurry solution must be stabilized with a surfactant to prevent particle settling. The method of storage and circulation also plays a large role in the quality and dispersion of slurry particles in solution. Particles are counted with a Tencor Surf-Scan laser particle counter. Total particle counts and relative distribution of particle size is measured.

The backsides of single-side polish (SSP) wafers are polished (resulting in double-side polished, DSP) wafers to evaluate slurry concentrations and polishing times. A 15 minute polish at 125 RPM and 10 PSI downforce with Nalco alumina

slurry dispensed at 150mL/min produces mirror finished wafers with no visual defects. Due to improper storage and short shelf life of polishing slurry, severe agglomeration of alumina particles results in 1μm particle counts greater than 20,000 as shown in figure 2.6. To reduce particles without re-engineering slurry dispense methods, a post polishing clean with poly-acrylic acid (PAA) increases wafer hydrophilicity. A hydrophilic polished surface retains wetness so proper rinse and spin-dry operations can be performed before particles dry on the surface. Kanto CMP-MO2 (with proprietary ingredients) post-CMP cleaning solution designed to remove metal particulates along with a DI rinse in a spinner clean the wafer after CMP. Using this process reduced particle counts to fewer than 800 1μm particles, dispersed around the edge of the wafer. A clean post CMP surface is shown in figure 2.7. The particles collect on the wafer edge as water is spun off. To further clean the wafers, pre-bonding plasma treatments to remove sub-micron particles and native oxide layers are required.

Fig 2.6. Particle agglomeration on wafer surface as viewed through a Nomarsky filter. 50x magnification.

Fig 2.7. Particle reduction of PAA treated hydrophilic wafer. 50x magnification.

2.3 Wafer Bonding

The wafer bonding process is capable of joining two dissimilar substrates. High temperature (over 1000°C) annealing creates covalent bonds between two substrates. However, the high temperatures destroy the active layers in 3DI devices so an alternate mechanism is required. Various bonding agents such as benzocyclobutane (BCB) and polyimide are used in MEMS applications [14]. These bonds form at temperatures below 200°C. However, the via process (section 2.4) is incompatible with low temperature bonding mediums due to high via process temperatures delaminating the bond, increased etch depth requirements and variations in etch reactions.

Direct wafer bonding by surface activation allows sufficient bond strength for wafer grinding at low temperatures [6]. This technique is applied in optics to bond direct band-gap substrates such as InP to silicon, showcasing the versatility of surface activation in joining dissimilar substrates [15]. Silicon on insulator (SOI) technology is another example of SAWD bonding [16]. The ability to join two dissimilar substrates with no bonding medium makes surface activation an attractive technology for 3DI.

2.3.1 Wafer Direct Bonding Properties

Hydrogen bonds form when a positively charged hydrogen ion (proton) bonds with an electro-negative O, N, or F atom. This mechanism joins hydrophilic wafer surfaces at room temperature [6] in a configuration shown in figure 2.8. The wafer is then annealed at high temperatures (>1000°C) such that H is removed from the bond

interface leaving behind Si-O covalent bonds with energies equivalent to the fracture strength of the substrate. The high temperatures eliminate the possibility of performing this bond on active circuits as required by 3DI. Alternatively, plasma treatment before bonding can produce fracture strength bond energies at annealing temperatures below 400°C [17].

Plasma treatment removes the native oxide buildup and small particles that interfere with spontaneous bonding. Native oxide removal creates SiO groups at the surface of the wafer. OH groups bond to SiO bridging the gap between the wafers. Annealing takes place at 200°C for 24 hours to remove hydrogen from the interface leaving an oxide bond.

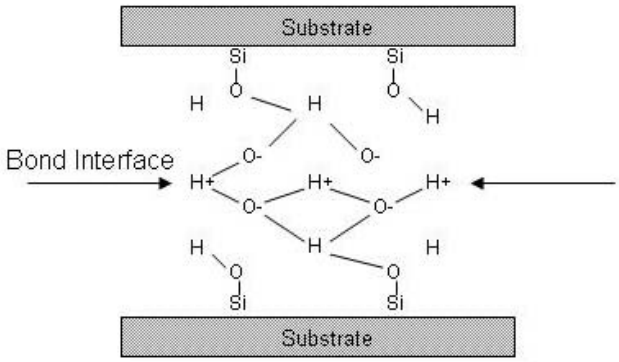

Fig 2.8 OH bonding to SiO groups after plasma activation [8].

Particles on the bonding surface create voids in the bond several orders of magnitude larger than the particle [8], significantly reducing bond strength and yield. Care must be taken during wafer handling to mitigate the introduction of particles to the bond interface. Ideally, wafers remain under high vacuum after plasma treatment and are bonded before being introduced to atmosphere to prevent particle buildup before the substrates are bonded. However, when a bonding module is not present on

the plasma etching tool, the technician' s use of a particle hood and wafer tongs reduce particle count and increase the bond yield as shown in figure 2.9.

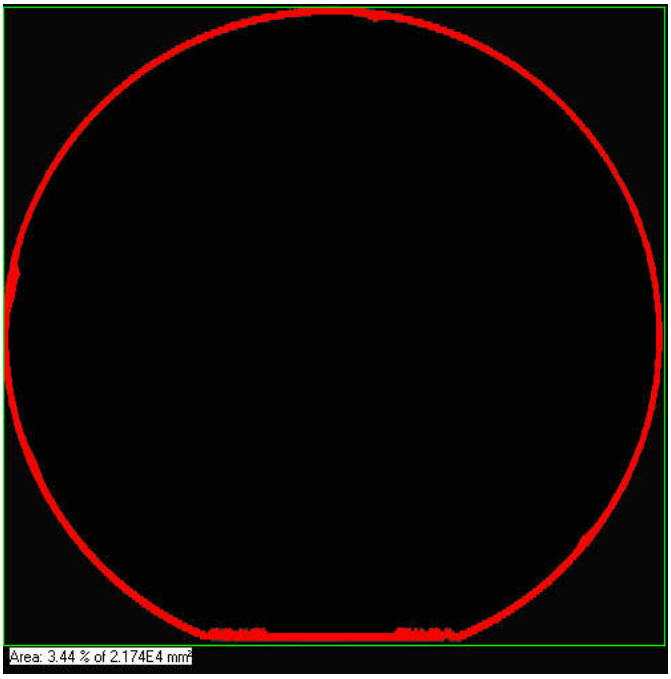

Fig. 2.9. Void free bond. Un-bonded areas appear in red. Image taken by SAM.

2.3.2 Bonding Process Conditions

Bonding wafers are sequentially exposed to Argon plasma for surface activation. The plasma is created in the M0RI chamber in which the magnetic field focuses the plasma toward the target wafer. The magnetic chamber creates a helicon plasma field with enhanced ion density over inductively coupled plasma fields. This leads to greater energies transferred to the wafer and additional bonding sites for OH groups.

Contacting the two bonding surfaces is performed in a bonding chamber. The bonding wave speed is a function of the pressure of gas that is expelled from the interface during bonding [18] so the substrates are contacted under high vacuum (1 x

10^{-5} torr). To ensure the entire surface bonds, a pressure of 4500 psi is applied for 2 minutes by two ultra-planar silicon carbide contact plates.

The number of bonds and the energy of each bond determine the bonding energy. This can be determined by a razor blade fracture test [8]. A razor blade is inserted into the bond at the edge of the wafers and a crack propagates some distance through the bond. The bonding energy is a function of crack propagation length L, wafer thickness t_w, Young's modulus E=130.2 GPa for <100> Si [19], and razor thickness t_b.

$$\gamma = \frac{3Et_w^3 t_b^2}{32L^4}$$

for wafers of the same thickness and composition. For 6 wafers bonded after 5 min exposure to Ar plasma the average bond strength was 173 mJ/m^2 shown in table 2.

After annealing at 200°C for 24 hours, significant H_2 off-gassing created voids throughout the wafer. Raising the bonding chamber temperature did not reduce this effect. There is no avenue for the H2 to diffuse out of the center of the bonding interface on blank wafers. To allow H2 to diffuse out of the bond, a trench pattern is required. This trench pattern is etched into a layer of SiO2, which ultimately provides insulation for via interconnect metallization.

Wafer	Wafer Thickness (m)	Razor Thickness (m)	Crack Length (m)	Bond Energy (J/m^2)
1	6.55E-04	4.00E-04	0.0473	0.109693395
2	6.39E-04	4.00E-04	0.0403	0.193189996
3	6.58E-04	4.00E-04	0.041	0.196899447
4	6.52E-04	4.00E-04	0.0405	0.201383801
5	6.59E-04	4.00E-04	0.044	0.149259896
6	6.55E-04	4.00E-04	0.0414	0.186820607

Table 2.2 Plasma Activation bond energies determined by fracture testing.

2.3.3 SiO_2 Bonding

To provide an avenue for H_2 to diffuse out of silicon, a trench pattern is etched into a 1500 Å layer of SiO_2. The SiO2 is deposited in a Trion plasma enhanced chemical vapor deposition (PECVD) tool at 300°C and a rate of approximately 700 Å/min. 908-35 positive photoresist recipe (Appendix A) is used to pattern a series of trenches (1µm wide at a spacing of 5mm horizontal and 2cm vertical) The oxide is etched in a $C_4F_8/CH_2/Ar$ plasma chemistry until underlying silicon is exposed and the remaining photoresist is burned off. The Argon plasma recipe described in section 2.3.

While trenches do not contribute to the bond, the off-gassing void formation is significantly reduced as shown in figure 2.10. The additional step of etching strategically placed trenches in the passivation oxide without interconnect structure interference is necessary to ensure high yield 3DI devices.

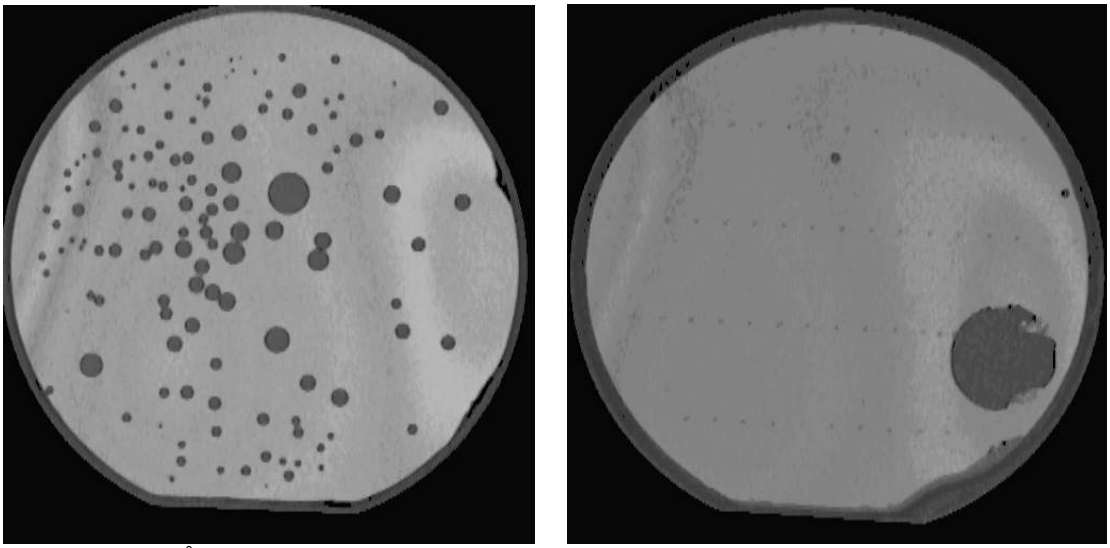

Fig 2.10 1500 Å oxide bonded wafers post baked at 150°C for 48 hour off-gassing. Light gray color indicates bonded area. Right wafer does not have trench pattern. Trenches in the left wafer eliminate the formation of bubble voids by H offgassing.

2.4 Via Etching and Filling

Bosch deep reactive ion etching (DRIE) is a preferred method of etching deep vertical sidewall features into silicon [20] for applications such as micro electro mechanical systems (MEMS). The process involves constantly switching between etch and passivation chemistries to build a protective sidewall layer that maintains a vertical etch profile. Sulfur hexafluoride (SF_6) etches silicon for several seconds after which C_4F_8 forms a Teflon-like polymer film on the substrate and within the etched gaps. When SF_6 is reintroduced, the horizontal surface passivation is removed. The sidewall passivation maintains a vertical etch profile. The frequent alternation of etch and passivation creates sidewall scallops approximately every 100 Å (depending on process parameters) [21]. The irregular sidewall prevents the buildup of a TiN barrier layer by ion sputter physical vapor deposition (PVD). The passivated vias require this TiN layer to prevent Al spiking, a short circuit when Al breaks through the passivation in an attempt to absorb Si. To eliminate scallops from the process, a novel deep silicon etch technique is presented. The new technique etches fine pitch (1μm) vias to a depth of at least 20μm with no sidewall scalloping [22]. Use of Aluminum (Al) interconnects circumvents the need for costly atomic layer deposition (ALD) and metal organic chemical vapor deposition (MOCVD) tools to fabricate plated copper interconnects [23]. A method of forcing Al alloys into an oxide passivated, TiN lined high aspect ratio via is described.

2.4.1 Scallop Free Deep Silicon Etch With Passivation

High aspect ratio via etching takes place in a Trikon Omega 201 platform with an m=0 resonant induction (M0RI) plasma chamber [22]. The process is carried out on 150mm wafers with a 2μm tetraethyl orthosilicate (TEOS) oxide coating. The substrate is patterned with the HAR photoresist recipe (Appendix A). $C_4F_8/CH_2/Ar$ plasma (with a bias power of 400 watts) is used to etch the via pattern into the TEOS layer. The M0RI chamber is powered at 600 watts to focus the plasma. The TEOS now serves as a hard mask for $SF_6/O_2/HBr$ chemistry Si bulk etch. Initial processing with this chemistry etched vias with vertical sidewalls damaged by ion bombardment as shown in figure 2.11. Insufficient verticality of mask wall profile causes ion reflections which are redirected to the side of the via from the initial vertical attack angle.

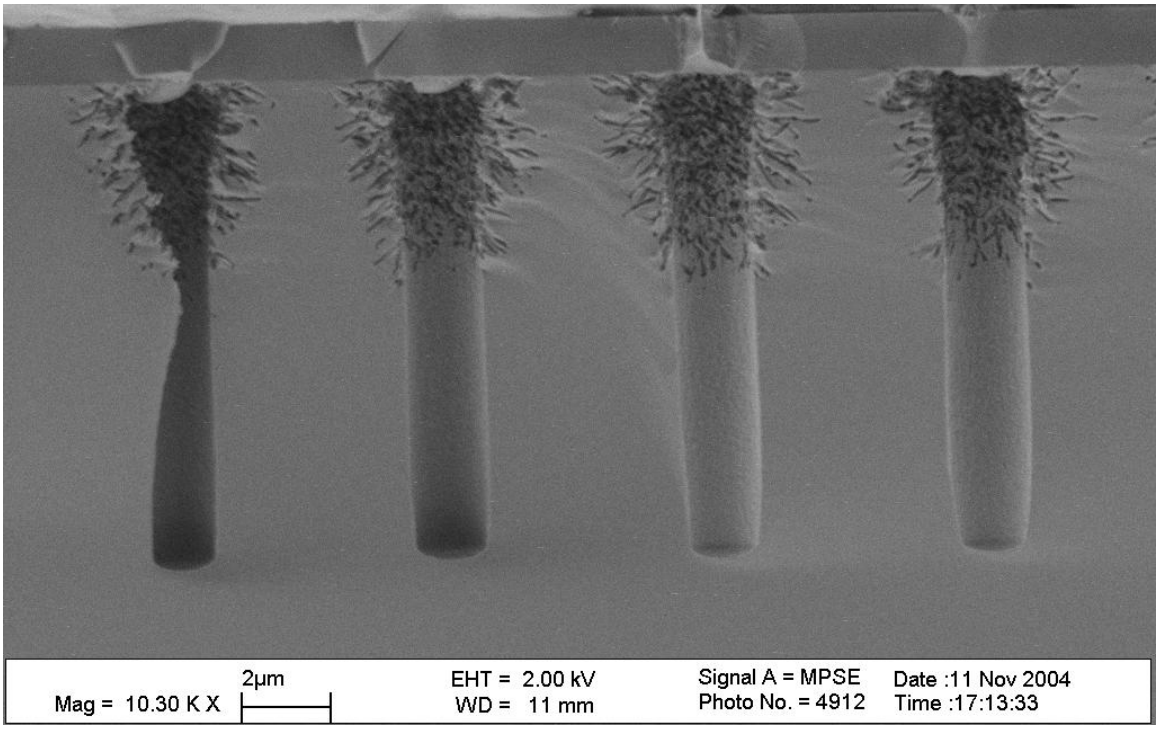

Fig. 2.11. Severe Ion bombardment during etch process after manual chamber clean and maintenance.

Introduction of SF_4 passivation gas eliminates the effect of ion bombardment. SF_4 acts as an oxide growth promoter (shown in figure 2.12) throughout the feature, protecting the sidewall and simultaneously growing insulation between the interconnect and substrate bulk. Passivation oxide also grows on the hardmask increasing the etch selectivity above 50:1 (Si:hardmask). Results of the via etch are shown in figure 2.13.

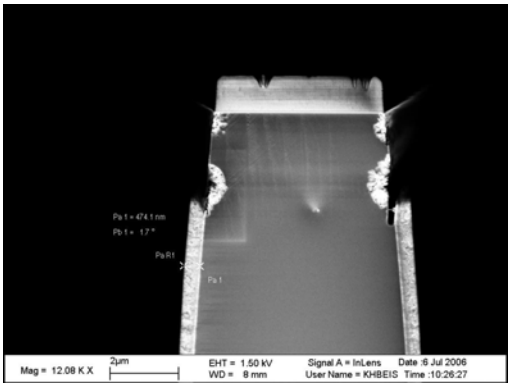

Fig. 2.12 Extreme passivation oxide growth. Sidewall oxide thickness=4740Å on a delaminated 4µm column.

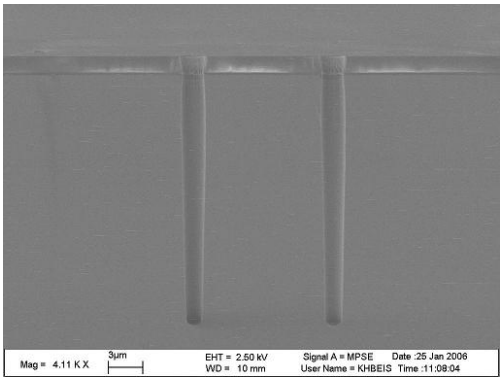

Fig. 2.13. Smooth sidewall deep fine pitch via with sidewall passivation. No process damage visible on hardmask due to high etch selectivity (dark gray top layer)

1µm via etch plasma is activated with 50 watts bias power and M0RI chamber power is increased to 2300 watts to ensure a highly directional etch. Passivation and mask species can linger in the chamber and be re-deposited on the substrate. This phenomenon is known as micro masking and results in deep (>3µm) pitting (micrograss) on horizontal surfaces [21]. The micrograss causes the wafer to appear charred and hinders metal deposition. Etch chamber oxide clean recipes are carried out after each wafer etch to eliminate the appearance of micrograss.

2.4.2 High Pressure Via Fill

Deposition and fill is carried out in a Trikon Sigma cluster tool fitted with two deposition chambers, a high temperature bake chamber, and a high pressure (forcefill) chamber. The via fill process begins with PVD of a TiN barrier layer. A 2000 Å seed layer of Ti is first deposited on the wafer surface at 400°C under high vacuum. The fine pitch deep vias are susceptible to shadow effects where Ti is deposited on the wafer surface and at the bottom of the via but not along the sidewall. The elimination of sidewall scallops is essential to achieving sufficient coverage on the floor of the via. At this point a small percentage of Ti is re-ionized and is re-deposited along the sidewall of the via in a splash effect. The same mechanism assists in the sidewall deposition of the TiN layer. TiN is facilitated by the addition of 120 sccm nitrogen gas flow during Ti deposition phase. After a 1.1μm deposition, the thickness of the sidewall barrier layer (Ti and TiN) is approximately 15nm.

Aluminum PVD builds a 3μm layer that bridges 1-2μm via gaps at 350°C under high vacuum. The vias remain under high vacuum as the wafers are transported to the forcefill chamber. The main mechanism for stress relaxation under high pressure and below the melting point of Al is dislocation glide and climb [24]. The temperature is raised to 530°C and pressure increased to 75 MPa for 10 minutes. Al fills the vias by plastic deformation as shown in figure 2.14.

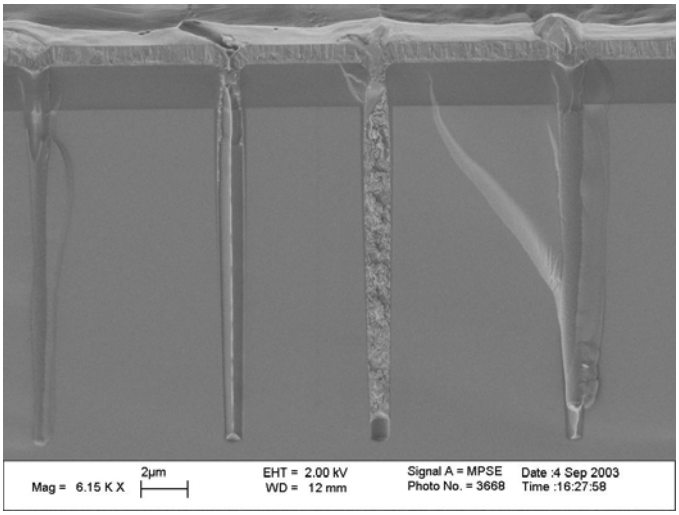

Fig 2.14. Complete Al via fill at 530 C. Discontinuity at the top of the left via and cross section of the right via is due to fracture induced during wafer cleaving.

Germanium is added during Al deposition to reduce the forcefill process temperature. Several ratios ranging from 2% - 25% were tested. The fill temperature was reduced by 130°C with an 8% Ge alloy. Higher concentrations of Ge and higher process temperatures cause precipitation from the alloy. This raises the sheet resistivity as shown in figure 2.15 and can create open circuits in the via fill as shown in figure 2.16 Via fill depth increases with Ge concentration, and forcefill time and temperature.

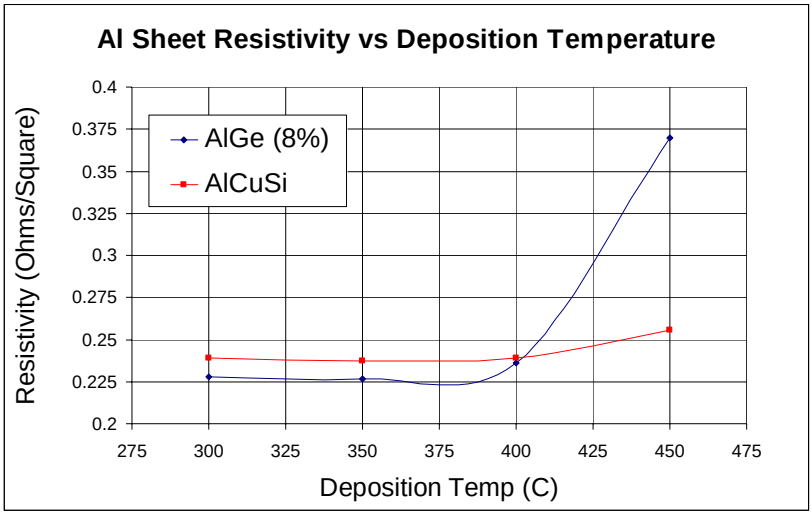

Fig 2.15Increase in sheet resistance of AlGe alloys as deposition temperature rises and Ge precipitates

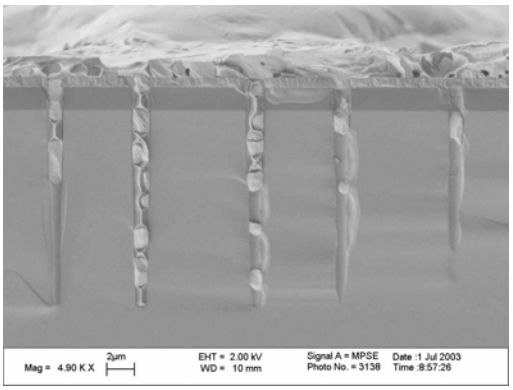

Fig 2.16 Severe Ge precipitation (25% Ge alloy). Fill temperature=450°C

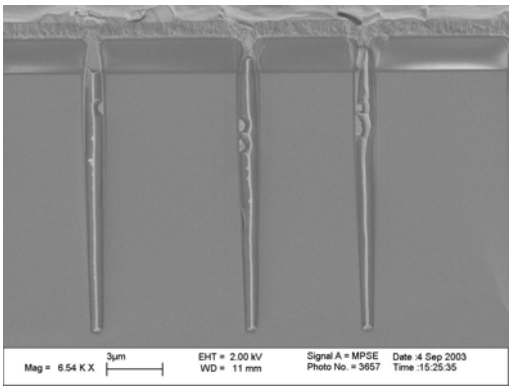

Fig 2.17 Minor Ge precipitation (8 % Ge Alloy). Fill temperature=500°C

2.5 Summary

The processes to vertically integrate a wafer stack have been presented. A three step thinning process has the capability to thin wafers to a final thickness of 20µm. TTV remains too high for bonding with surface activation. Additional characterization of chemical thinning with Sulfuric acid as a quality enhancer is required. Once the wafers are thinned, they are bonded after Ar plasma activation to bond strengths adequate to survive additional processing. Addition of a trench pattern etched in SiO_2 allows for H_2 off-gassing during bond cure phase and reducing H_2 induced voids. The via etch process has demonstrated deep fine pitch vias with scallop free sidewalls. An AlGe metallization fills the vias well below the melting point of Al. All of these processes are compatible with reintegrated die wafers.

3. Production Component Applications

3.1 Overview

To apply 3DI to standard production component chips several new processes are developed. Integrating COTS parts requires die removal from plastic packaging. Wafer reintegration places de-packed die on a handle wafer allowing discreet component circuits to be batch processed. The 3DI thinning process requires additional protective measures to reduce damage to the active devices during grinding and chemical thinning processes. From this point on the reintegrated die wafer follows the normal 3DI process flow to create a die stack. This chapter presents processing techniques which allow individual component circuits for an embedded system to be vertically integrated into a multi chip module. Integrating parts of the GPS-RT (described in chapter 4) is the final goal of applying 3DI to production components.

3.2 Die De-Packaging and Mapping

Since latest generation commercial off the shelf (COTS) ICs are not readily available as bare die in small quantities, a de-packaging process is required for test and development purposes. The component package consists of the die, a carrier such as a metal frame, wire bonds, a lead frame, and a ceramic or injection molded capsule.

COTS packages have undergone significant development to minimize damage to the die. The die is attached to a substrate with a bonding medium designed to

reduce die failure mechanisms such as vertical, horizontal, and spalling cracks [25]. The die is then wire bonded to the lead frame, most often using thermosonic bonding [26]. In this method, a gold ball with the bonding wire attached is bonded to the die pads. Ultrasonic energy combined with the capillary technique of thermocompression bonding at 150°-240°C bonds the ball to the die pad. The wire is then wedge bonded to the package lead. A plastic encapsulant fills the package and protects the die. The capsule material contains a polymer filler (65-90%), epoxy resin matrix (10-20%), crosslinker (5-10%), stress relief agents (2-5%), flame retardant (1-5%), mold release agent (0.1-1%), colorant (0.2-0.4%), catalyst , 0.2-0.3%), coupling agent (< 0.2%), and ion getters (< 0.2%) [26]. The main component (the filler) is generally some type of thermoplastic, etched by a nitric and sulfuric acid mix. With the filler removed, the package loses structural rigidity and releases the die. Wire bonds are sheared off or etched with potassium iodide, a gold etchant.

Tools such as the Nisene JetEtch incorporate pumping systems to mix and dispense the etch solution on to the package. A system of sockets and gaskets are employed to hold the package in place while the die is exposed. Such tools are essential for failure analysis since they expose the die without disturbing mechanical aspects of the system, with the exception of the encapsulating material. While access to this tool is not immediately available, the principal of etching with 90% fuming nitric acid is adapted by simply placing the component in a beaker of nitric acid for 24 hours. Nitric acid readily dissolves the plastic packaging and the adhesive used to glue the die to the pad frame. To prevent excess oxidation upon removal from the nitric acid, the acid residue is removed with isopropyl alcohol (IPA). The IPA wipe

also removes the remaining plastic residue on the surface of the die. Wirebonds do not survive the de-packaging process intact however; bonding balls remain attached to bond pads. Potassium iodide drops placed on the die remove residual gold after 20 minutes. A CC1100 radio and M25P80 flash memory used in the GPS-RT (chapter 4) are de-packaged and shown in figure 3.1

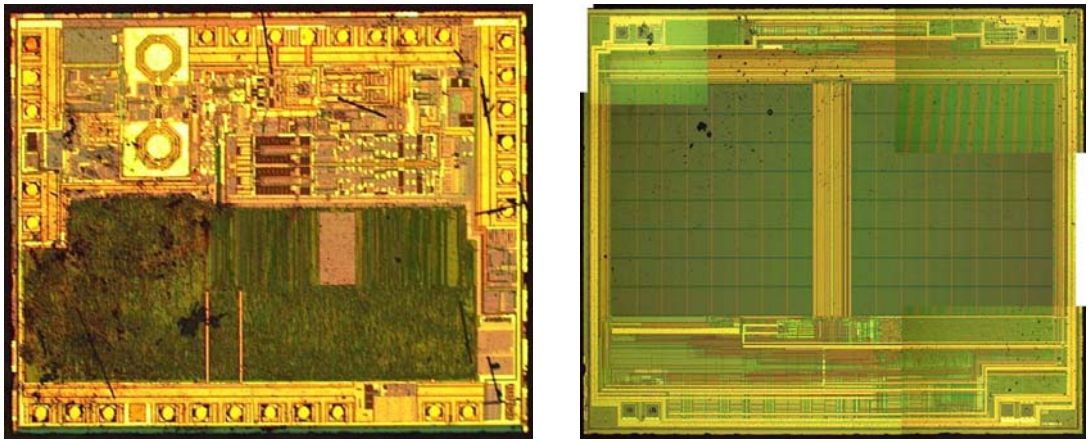

Fig 3.1 De-packaged CC1100 (left) and M25P80 (right). Each component is used in the GPS-RT (see chapter 4)

The pad dimensions and spacing are cataloged using image processing software. The resulting table is translated into a layout for die testing. When the die pad to package pin ratio is 1 to 1, ground pads found by trial and error become the key for determining the remaining pin to pad correspondence. However, components such as the Chipcon CC1100, have more pads than pins so each pad must be individually tested. A fine pad pitch prevents the use of standard DC probes so instead, probe cards which arrange 64 or more fine pitch (<50μm) pins within a 5mm x 5mm square give access to each pad. The pads are probed and integrated into test circuits to be cataloged by trial and error. The dimension and probe data is combined to derive a layout as shown in figure 3.2

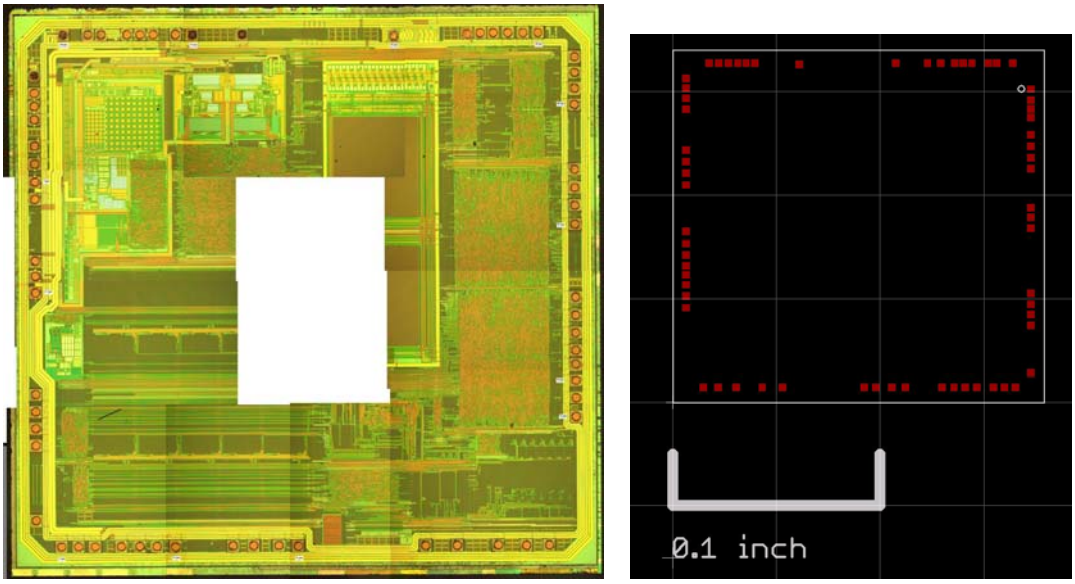

Fig 3.2. De-packaged MSP430F1612 (left) and the derived CAD layout (right)

Integrating the MSP430F1612 microcontroller and M25P80 flash memory of the GPS-RT is the final goal of applying 3DI to production components. The MSP layout dimensions are 13mm x 13 mm while the flash layout dimensions are 9mm x 5mm. Integrating the two components into a 3DI module eliminates the surface area taken by the flash. Additionally routing to the 8 pins on the flash is eliminated along with a bypass capacitor. In an example layout similar to the GPS-RT layout, the total foot print of the MSP/flash circuit is reduced from 25mm x 15mm to 14mm x 14 mm (48% size reduction) as shown in figure 3.3. Two vias and 71 mm of copper wire routing are also eliminated since all connections are now internal.

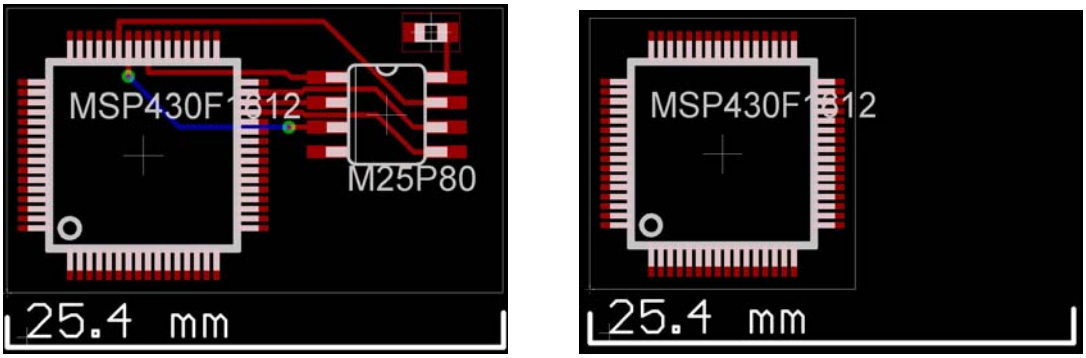

Fig 3.3 Elimination of flash memory from PCB surface when integrated into a 3DI module.

To ensure die remain functional throughout the de-packaging process, PIC16LF867a microcontrollers are programmed with a test code to demonstrate that basic functionality is retained. The program sets the PIC I/O ports to oscillate at 1.25Hz using an external RC oscillator to drive the clock. The successful test of a de-packaged PIC proves that no short circuits are created, the onboard flash memory data is retained, clock oscillators function, and I/O driver current handling abilities are unaffected (tested by using the port to drive an LED).

The de-packaged PIC program produces an output square wave at a frequency of 1.25 Hz on each I/O pin as shown in figure 3.4. A total of 25 PIC circuits were programmed and de-packaged. 17 die functioned properly when probed producing a 68% yield. However, 12 of the final 12 tests were successful suggesting the initial probing method was a source of die failure and the de-packaging process produces a higher actual yield.

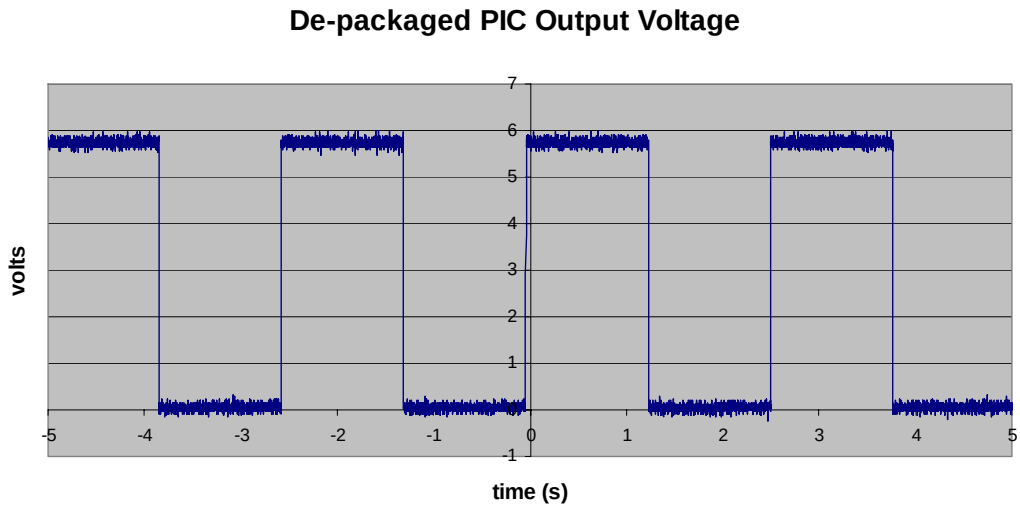

Fig 3.4. Port B voltage output of de-packaged PIC. Vcc=5.5 V, External Oscillator frequency (F_{osc}) =12MHz

3.3 Reintegrated Die Wafer (RDW)

To enable batch processing and thinning of de-packaged die as shown in figure 3.5, a method of wafer reintegration is required. The reintegration process requires a high degree of repeatability to support 3DI alignment and bonding processing. To align die a Finetech Fineplacer flip chip tool with 5µm precision is used to place die onto a handle wafer coated with adhesive.

The Finetech placer is capable of curing both heat and UV activated adhesives. Initial testing with Kaeiobond UV adhesive provided insufficient coverage when dispensed pneumatically through a nozzle as dots. Thinned die exhibit visible surface roughness similar to the 5 point dispense pattern. To eliminate this source of die TTV, a uniform spin dispensable adhesive is required.

A Humiseal acrylic adhesive is mixed with acetone (as a solvent) in a 1:1 ratio. The acrylic is dispensed on the wafer to a uniform thickness of 3µm (Appendix A). The standard patterning method with OIR 908-35 positive photoresist (PR)

caused the acrylic to crack during post bake steps due to differences in coefficients of thermal expansion. NR-1500 PY negative PR eliminates the cracking problem (Appendix A). The pattern is subject to deformation when the wafer is heated so all post bake steps are eliminated.

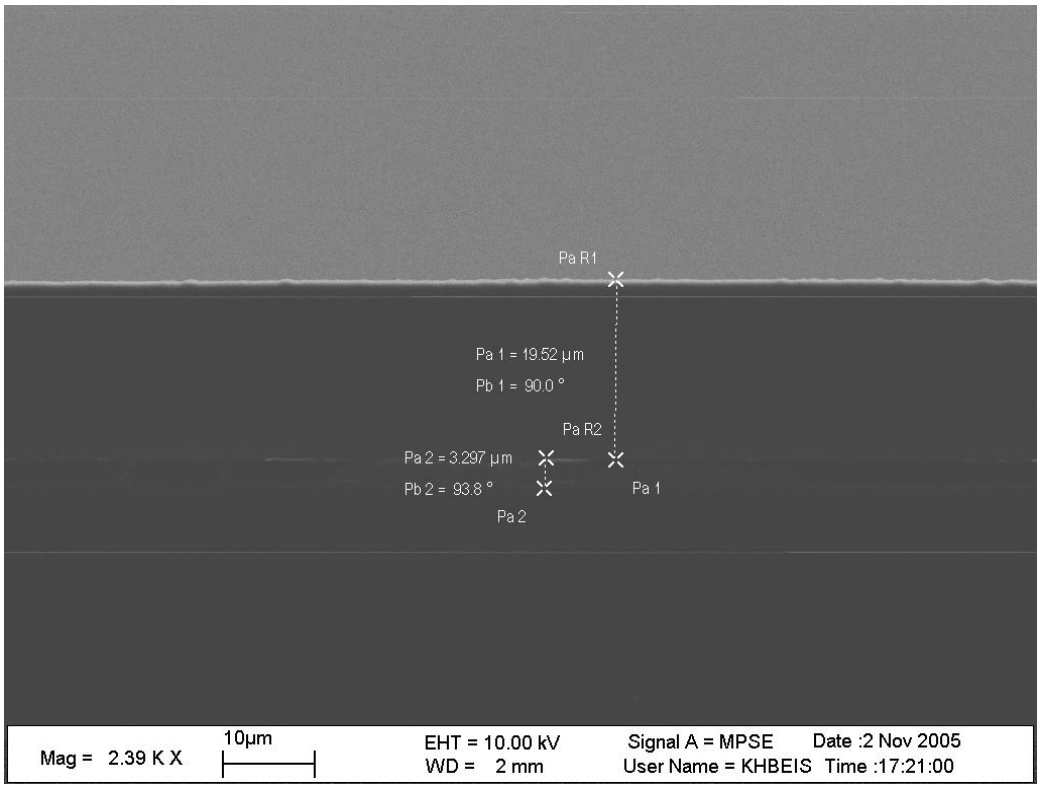

Fig 3.5. Post thinning die thickness. Pa1=19.52µm (die height), Pa2=3.3µm (acrylic thickness)

A M0RI oxide plasma etch transfers the PR pattern to the acrylic. The selectivity of the oxide plasma from the mask (PR) to the acrylic is nearly 1:1. To assure a complete etch without destroying the PR, the magnetic coupling capabilities of the M0RI focus the oxide plasma into a highly directional field ensuring an anisotropic etch. RF power is set at 2000 watts with magnetic coil inner power reduced to increase the etch reaction on the wafers outer edge. An etch time of 4 minutes produces clear features across the wafer surface without burning through the

PR and scarring the acrylic in the center of the wafer. Residual PR is burned off during die placement.

The Finetech Fineplacer has a dual camera alignment system that, with proper image calibration, can align metallized components on the acrylic handle wafer with 10μm precision. Alignment markings on each layer are shown in figure 3.6. This exceeds the resolution of the acrylic patterning step which places the lower limit on interconnect pad dimensions. Under temperatures above 130°C the acrylic reflows, further reducing the resolution of alignment marks. Full thickness die are placed on the acrylic at 130°C with a force of 20N. The force parameter is used as opposed to absolute position to ensure that die of different thicknesses are placed equal distance from the handle wafer. The reintegrated wafer is prepared for 3DI backside thinning to reduce all die to the same thickness.

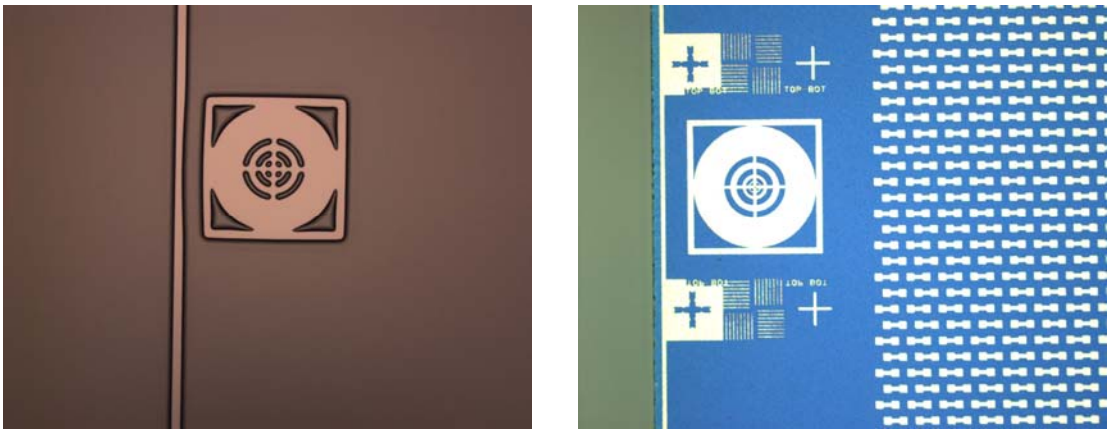

Fig 3.6 Alignment marks in acrylic (left) and metallized die test pattern (right). Slight heat deformation visible in acrylic. The target patter is 220μm in diameter.

3.4 3DI Processing

The reintegrated die wafer (RDW) process results in gaps at the die edges creating an irregular surface. The gaps cause chipping during grinding due to die sidewall impacts with the grinding wheel. Sidewall etching and undercutting occurs

during the isotropic chemical thinning. Etch reactant droplets form in the gaps causing a constant etch of the handle wafer. A gap fill process is required to mitigate these problems. Ideally, the gap fill material would have the same mechanical and chemical properties as silicon. Since Si crystal gap growth is not feasible, a viscous polymer fill is required with a melting point below that of the acrylic die adhesive to prevent alignment shifting. The fill must also be resistant to the etch chemistry to prevent damage to the handle wafer.

A test wafer coated with synthetic thermoplastic wax survives 10 minutes of direct exposure to the etch chemistry with minor etching to uncovered areas and zero etching of the wax as shown in figure 3.7. The wax is applied to the RDW before thinning takes place. The potential for chipping is reduced since the grinding wheel encounters fewer edges. After grinding, all excess wax is removed from the RDW leaving behind uniform protective barriers in the cracks between die and on exposed regions of the handle wafer.

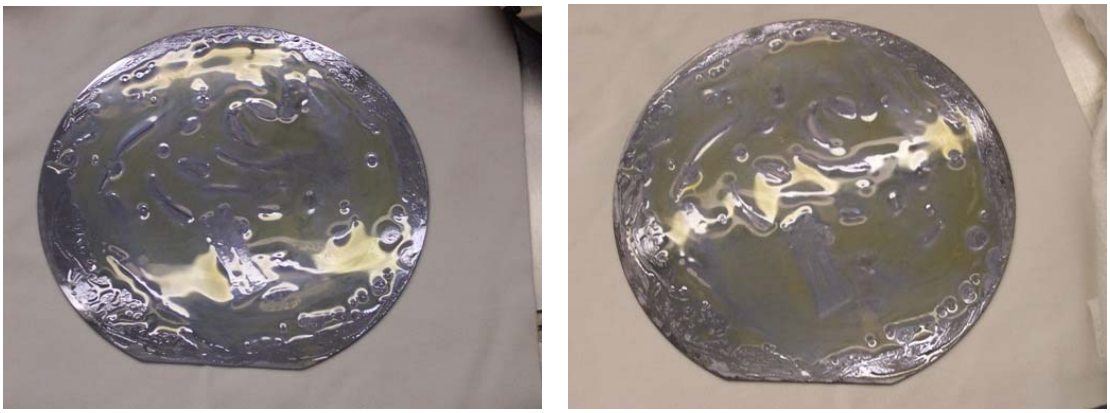

Fig 3.7. Wax resistance to 5:10:1 HNA etch chemistry. Pre etch (left) and post 10 minute etch (right).

During chemical etch, the wax fill affects the etch profile of the die. The wax prevents a uniform isotropic etch on the side of the die resulting in a lower etch rate

around the edges. Near the gap fill, etching is reduced resulting in an upward curve of up to 30µm on the die as shown in figure 3.8. These edge effects are removed and the die planarized during CMP.

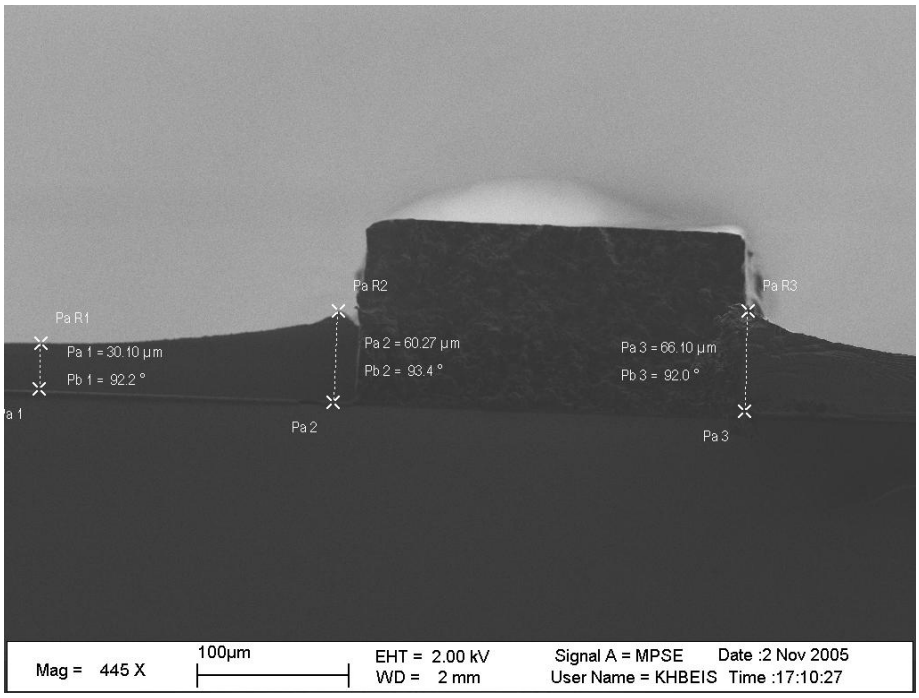

Fig. 3.8 Die etch edge effects. Edge peak height is approximately 30µm above die center height. Wax remains unaffected by etch chemistry.

As with the standard 3DI chemical etch process, the quality of etch increases dramatically when the wafer is run continuously until target thickness is reached. Removal is generally greater in the center of the wafer due to increased insulation from surrounding die. The insulation retains heat increasing the process temperature and thus the etch reaction in the center of the wafer as shown in the etch profiles of figure 3.9. The wax gap fill also contributes to die insulation. Small test chips placed in a vacant center die location were subject to over etching down to the handle wafer when surrounded with excess wax. Overall wafer TTV is reduced to <10% of material removed.

The final CMP thinning tends toward greater removal around the edge of the wafer. The edge removal is due to the rotation of the wafer on the CMP polishing table. The outer edge of the wafer rotates faster than the center leading to a higher removal rate as shown in figure 3.10. The final TTV of CMP is equivalent to that of the etch step. Coupled with a low center point from chemical thinning, the overall wafer TTV can be made to balance down to 1μm required by 3DI bonding when sufficient material is removed. The remaining 3DI process steps do not differ from those described in section 2.

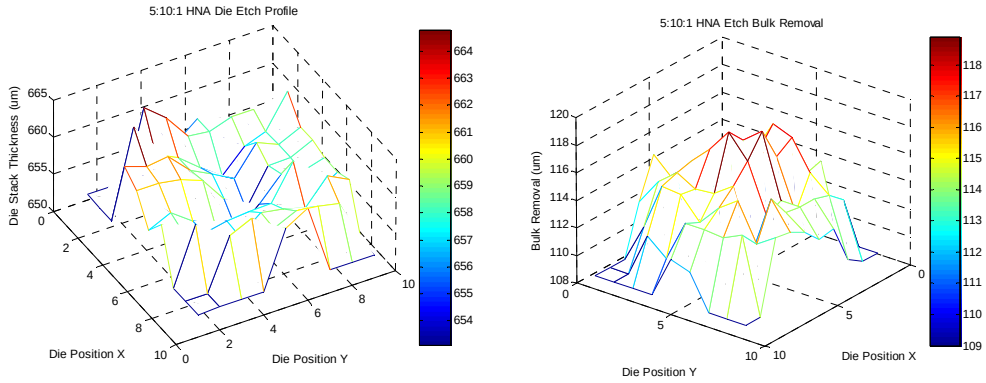

Fig 3.9. Wafer thickness after chemical etching. Center bulk removal is greater than edge removal.

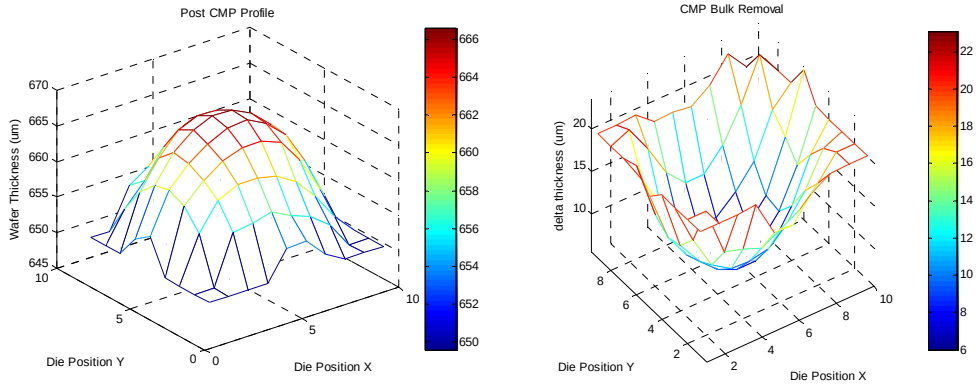

Fig. 3.10 Wafer thickness after CMP (left) shows greater removal from the wafer edge. Delta thickness shown right.

3.5 Summary

With a protective wax layer on a RDW, 3DI thinning is applied to de-packaged die in batches. Re-integration allows 3DI processing of any production component to be used in a low power embedded system. The production component applications of 3DI allow significant size reductions of embedded system PCB layouts. Additional development is necessary to determine electrical properties of interconnects through COTS chip substrates.

4. System Design

4.1 Overview

To demonstrate a low power embedded system platform that benefits from 3DI, a global positioning system recorder transmitter (GPS-RT) is developed. The system requirements are:

A) GPS data point acquisition
B) Data point retention in non-volatile memory
C) 2-way wireless communication with a basestation over a 1 mile range
D) 1 week field operating battery lifetime

To satisfy requirement D, each component chosen to fulfill requirements A-C has a low power mode in which current consumption is reduced to the order of microamperes. Power consumption is reduced when the main function of the device is shut down but basic operations such as data register retention and interrupts remain active. The microcontroller software state machine determines which devices are activated based on system interrupts. This chapter describes component selection and functionality in detail followed by an analysis of the software state machine.

4.2 Hardware

Eight integrated circuits, four voltage regulators and nearly 100 passive and interface components (switches, connectors, and jumpers) are routed together to build the GPS-RT revision B evaluation platform (the layout is shown in figure 4.1). Rev B is configurable as both a basestation and roaming unit for software development. CadSoft Easily Applicable Graphical Layout Editor (EAGLE) version 4.15 is used for

manual layout and routing of the system. The software includes schematic, PCB layout, and component editors along with configurable design rule checks (DRC) and CAM processors for gerber file generation. Each component IC is discussed in the following sections.

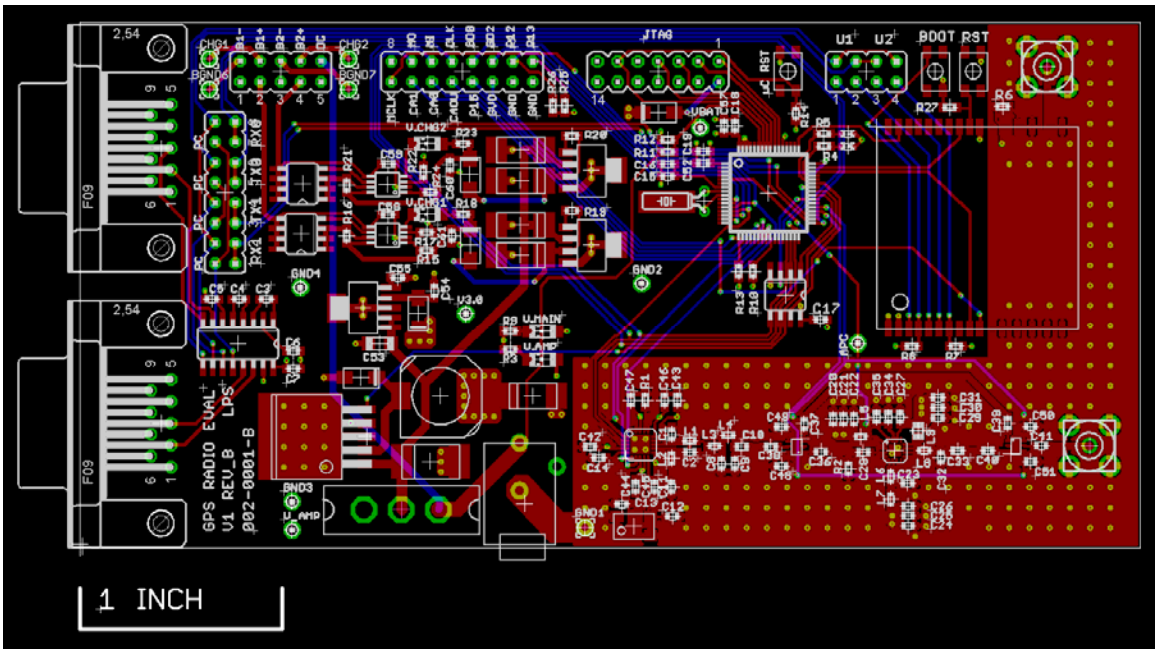

Fig. 4.1 EAGLE layout of GPS-RT rev B. Top copper shown in red, bottom copper shown in blue, vias shown in green, inner layers not visible

4.2.1 Microcontroller

Microcontrollers (MCU) are very useful devices for designing embedded systems. An extensive array of features is available for nearly every low speed mixed signal application. Operating in the low tens of megahertz, sufficient processing power is available to maintain an embedded system and perform basic data processing. Lower clock speeds also reduce power consumption due to reduced transistor switching. Additionally, many MCUs offer software configurable low

power modes in which internal circuit blocks (such as oscillators and peripherals) are shut down while retaining program data and interrupt capability.

A Texas Instruments MSP430F1612 [27] microcontroller is selected for the GPS-RT. Notable peripherals include six 8 bit I/O ports (with interrupt capability on ports 1 and 2), 12 bit A/D and D/A converters, and both a serial peripheral interface (SPI) bus and a universal synchronous asynchronous receiver transmitter (USART). The device is programmed via the IEEE 1149.1 (JTAG) specification which allows for in circuit debugging and monitoring of operating code [28]. A hardware multiplier, dynamic memory allocation (DMA), 16 bit architecture, and 125ns instruction time allow data processing at 8 MHz in addition to performing component maintenance. The system component diagram is shown in figure 4.2.

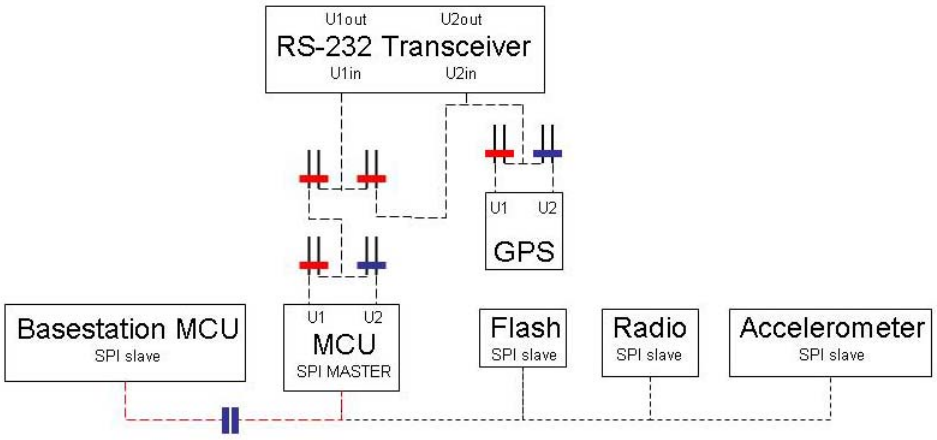

Fig 4.2. Onboard component communications diagram. Red jumpers are connected during roaming operation. The RS-232 transceiver allows the roaming unit to function as a basestation.

4.2.2 Non-Volatile Memory

Electronically erasable read only memory (EEPROM, commonly known as flash) is a solid state memory that retains data even when powered down. Bits of data are stored as a trapped charge on a floating gate of a transistor. Bits are programmed

by channel hot electron injection (CHE) [29]. A high voltage field applied to the transistor source energizes electrons to the point that some cross the oxide barrier and become trapped on the floating gate. This writes a zero to that particular gate. To erase the bit, a high negative voltage is applied to the control gate. Electrons trapped in the floating gate cross the oxide barrier to the transistor source by Fowler-Nordheim tunneling [29]. Assisted by the applied field, the electron wave function allows it to cross the barrier even without sufficient kinetic energy. The write and read functions are shown in figure 4.3

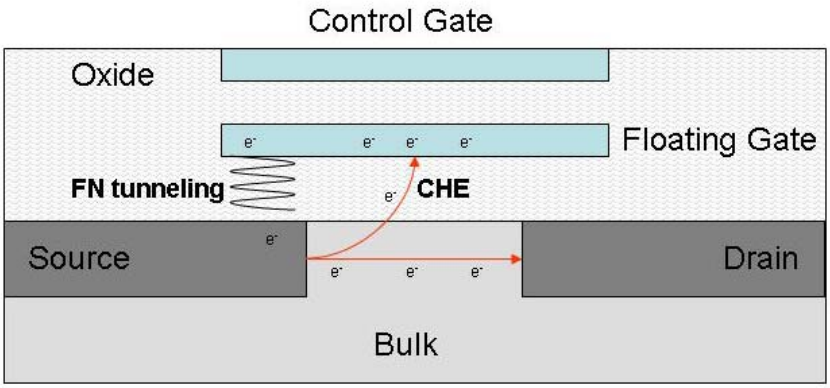

Fig 4.3. Flash memory cross section depicting program (CHE) and erase (FN) functions.

Flash memory has a limited number of write/erase cycles [30]. As defects arise in the oxide from crystal irregularities and high energy electron bombardment, the potential barrier between the floating gate and the channel is reduced and charge begins to leak. Advanced flash memory management software incorporates wear leveling functions when managing flash memory based file systems [31]. Initially, the memory is scanned for corrupt blocks to prevent write attempt failure. Use of block modification counters ensures certain sectors (such as the beginning of physical memory space) do not sustain excessive wear. Parameters such as data “freshness”

and specific block usage cycles determine which block can be erased and which should be used to store the next data set. A simpler logging method manages the GPS-RT data. As files are created and modified in memory, changes and new files are appended to the last written segment. When the data memory is filled sequentially, the first blocks are erased and new data is appended starting at the beginning of the memory space. The practicality of this method results from each data point requiring exactly 64 bytes of memory and no requirements for modifying and re-writing particular data. Since pages of memory are segmented by powers of 2, each data point will begin at the beginning of a page and subsequent points will completely fill the remaining bytes in the page. The need for de-fragmenting is eliminated and only a last address pointer is maintained.

The ST Microelectronics M25P80 [32], chosen for the GPS-RT, has 1 megabyte of physical memory. Data is programmed in 256 byte blocks and erased in 64 kilobyte sectors. In power down mode, current consumption is reduced to 1uA at a 3V supply voltage. An SPI bus provides data access with additional control pins for write protection and data transmission pause functions. Control registers enable the power down mode and report device status (i.e. write/erase progress, block protection).

4.2.3 GPS

The GPS network determines geographic location by triangulation based on distances between satellite transmitters and earthbound receivers. A digital satellite signal containing onboard satellite time and orbital data is modulated with a pseudo

random noise (PRN) number, started at a specific time (for example 12:00 am). This same PRN sequence started on the receiver at the same time (12:00 am). The PRN satellite signal arrives at the receiver approximately 67.3ms later. The exact time of flight, and subsequently distance, is calculated by determining the phase difference between the PRN sequence running on the receiver and that received from the satellite. Four satellites are required to determine a position in 3-D space. When the receiver sees 4 PRN sequences, processing engines called correlators can compare the signals and correct the errors in receiver time. Complete navigation messages (including orbital and health data for all 24 active and 4 inactive GPS satellites) are transmitted at 50 bits per second in 25 frames containing 1500 bits each shown in figure 4.4 [33]. Each frame contains satellite clock data and ephemeris along with a partial almanac. Since a receiver requires satellite location (ephemeris) to calculate position, the minimum startup time is 30 seconds (frame transmission time).

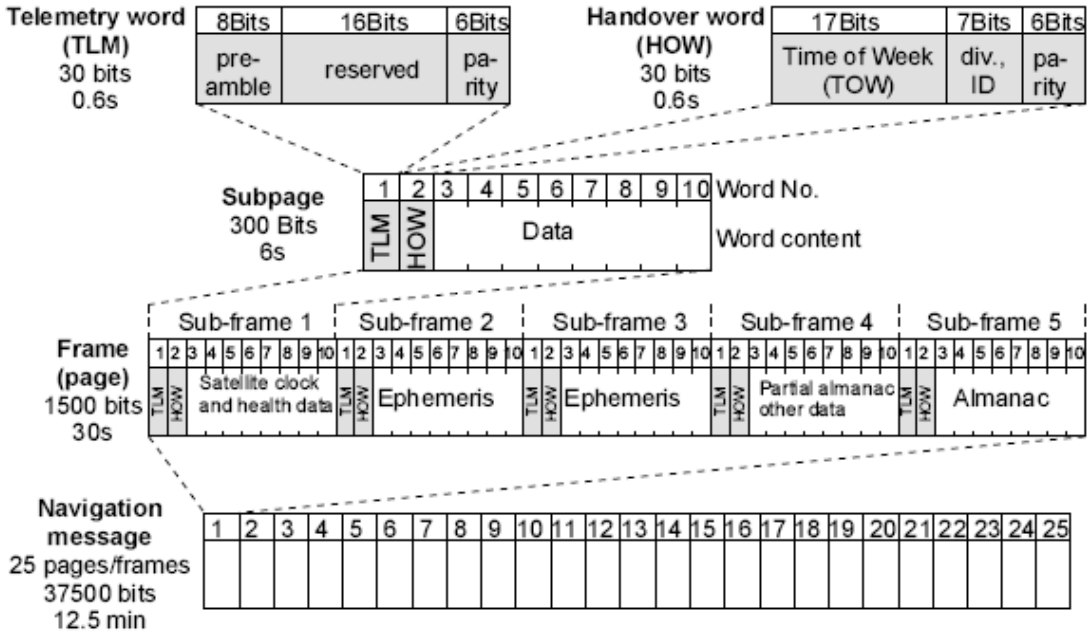

Fig 4.4. Navigation message subdivisions [34]

The vast amount of processing required to demodulate and decipher incoming signals from GPS satellites provides the largest current draw for the Ublox TIM [35] series GPS modules. To minimize current draw the system incorporates a sleep function to power down the processing unit when a GPS fix calculation is not required. In this mode, the previously acquired ephemeris and almanac data are stored in the module system RAM while processing elements are shut down. A system timer is preset to generate an interrupt which initiates the processor for signal reacquisition and position fix calculation. System current consumption on the GPS-RT rev B board is reduced by 60 mA when the GPS sleeps. Signal reacquisition upon wakeup requires 3 seconds on average (after first fix is calculated). Fast reacquisition is possible while ephemeris data stored in onboard memory is valid (up to 2 hours).

The TIM-LH module claims a 2.5m circular error probability (CEP) where 50% of fixes will represent points within a circle of radius 2.5m centered at the antenna's true position. From a 10 minute field test in a stationary location, 375 points were acquired with a maximum drift error of 6.7m latitude and 8.9m longitude. 284 points (75%) were located within the CEP assuming the true origin was located at the average of all included coordinates. When the same test was run for 2 minutes, 53 points were acquired with 52 points (98%) within the 2.5m CEP. Maximum drift errors were 8.9m latitude and 6.6m longitude shown in blue on the map of figure 4.5. The drift errors are used by the software to determine when the GPS-RT is stationary (described in section 4.3).

Fig 4.5. GPS drift data (blue) over 10 minutes. $1x10^{-5}$ degrees latitude = 1.1m. Location outlined in red.

4.2.4 RF Communication

The RF section of the GPS-RT contains three components; a transceiver, power amplifier, and RF switch. Both transmission and reception occur through the same balanced/unbalanced matching network (balun) for the transceiver. The switches are required to allow the RF signal to bypass the amplifier for receiving and close proximity transmission.

A Chipcon CC1100 [36] is the transceiver for the GPS-RT. The CC1100 is a highly configurable low power data radio capable of operating in the 300-348MHz, 400-464MHz and 800-928MHz Industrial Scientific and Medical (ISM) bands. A set

of 59 configuration registers are programmed by the microcontroller to set various operating modes.

To maintain low power operation the radio is configured to sleep when not transmitting. To receive packets, the radio periodically enters RX mode to poll for transmissions. Upon reception of a valid packet (validated when the correct number of bits are received) the radio interrupts the microcontroller and the packet is retrieved and processed in software.

Binary frequency shift keying (2-FSK) is enabled at 433 MHz with two data rates at an output power of up to 10 dBm. A 250kbps high data rate is used for efficient transmission in close proximity while the 1kpbs low data rate was found to extend the range by 50% in indoor range testing. The receiver sensitivity is -110dBm at a 1.2kbps data rate.

To boost the output power of the CC1100 and extend the GPS-RT range to 1 mile, an RFMD5110g [37] power amp capable of 33dBm output power with a 10dBm input at the desired 433MHz is used. The power amp is inserted into the output chain during transmission and bypassed during reception by two CEL UPG2009TB RF switches [38]. The switches have a high power handling capability (36 dBm) and signal isolation (28dB) and a low insertion loss (0.25dB) so the impact on receiver sensitivity is minimal. Free space attenuation is given by:

$$L_{dB} = 20\log\frac{4\pi r}{\lambda}$$

where r = transmission distance, λ= wavelength (0.693m at 433 MHz). Transmission over a 1 mile (1600m) results in a signal attenuation of 89.25dB. Theoretically the

CC1100 alone can transmit over this range since the link margin:

$$L_{margin} = TX_{power} + TX_{antennagain} + RX_{antennagain} - L_{sensitivity}$$

is 121.8 dB when a 1.8dBi ¼ wave whip antenna is used. The link margin exceeds the signal attenuation by 32dB (nearly 2 watts of output power) however, buildings and trees in the RF line of sight can attenuate the signal further by 10-20dB per obstacle [39]. In a field test, the GPS-RT successfully transmitted a signal between the coordinates: (38.9892 N, 76.9355 W), (39.0034 N, 76.94363 W), equivalent to 1818m through various obstacles (trees, buildings, etc). The measured output power of the power amp is 29.5dBm.

Layout of the RF chain is critical. The Rev B PCB has 4 layers, the top being the component layer and the closest inner layer being ground. RF and digital ground are separated. In addition to the inner ground plane a RF component ground plane encompasses the RF section. The top ground plane reduces interference by terminating field lines radiating from the RF transmission strip lines. Vias are placed at a 0.1" pitch to ensure all components tied to the top RF ground plane have a short path to the inner RF ground to minimize trace capacitance and ensure proper matching. Using the MATLAB RF toolbox for a numerical analysis of PCB dimensions, a 50 ohm trace width was designed with parameters shown in figure 4.6.

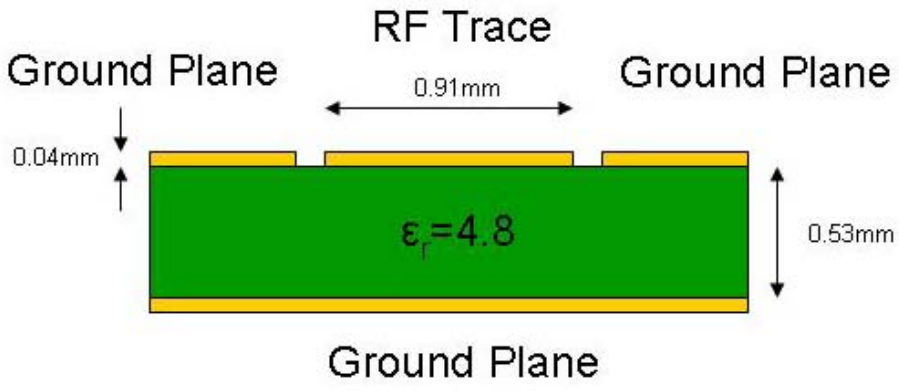

Fig. 4.6 RF trace layout on PCB

The conversion to a 4 layer board, linear path for the RF signal, and change to 3.3V switching voltage regulator for the power amp increased system power output from 24.7dBm (revision A radio layout shown in figure 4.7) to 29.5dBm (revision B radio layout shown in figure 4.8)

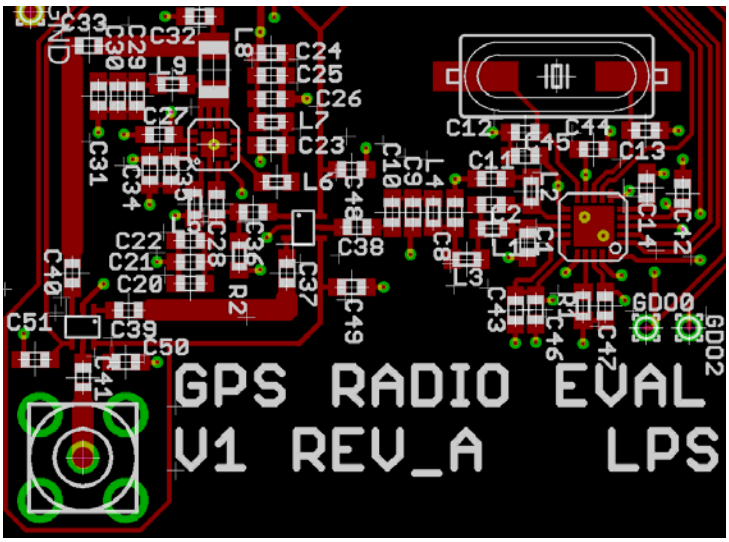

Fig 4.7. Rev. A Transceiver layout. U-turn for power amp output trace, lack of proper grounding limit maximum power and sensitivity.

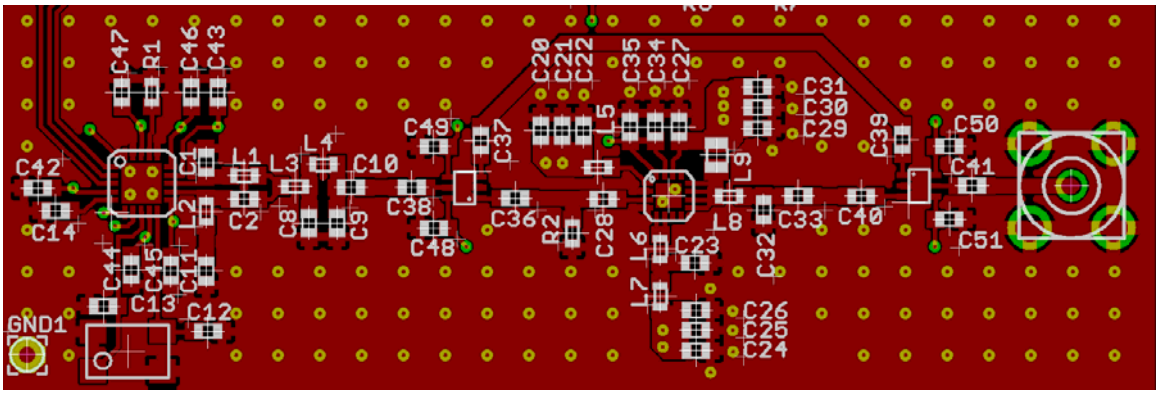

Fig. 4.8. RF transceiver layout, components outlined in white, copper shown in red, vias in green, dimensions=68mm x 22mm. Transmit path = CC1100 (far left), RF switch (center left), Power Amp (center right), RF switch to SMA connector (far left). Receive path eliminates the power amp with 50 ohm microstrip line (top).

4.2.5 Accelerometer

MEMS accelerometers contain a series of micron scale free motion cantilevers. Changes in capacitance between the cantilever and a fixed surface correspond to a force (acceleration) in the direction of the cantilevers range of motion. Arranging multiple cantilevers orthogonally allows detection of motion in three dimensions. Calculating the second integral of accelerometer output is a common method of inertial based navigation (dead reckoning). However, advanced compensation techniques are required to maintain system stability. Position errors begin to oscillate within several seconds of initial calculations [40].

An ST Microelectronics LIS3LV02DQ digital accelerometer [41] is configured as a motion sensitive interrupt source. The accelerometer includes a software configurable mode in which a high to low transition is sent to port 1 on the microcontroller when the programmable threshold acceleration is crossed. This allows the GPS to shut down completely while the system is stationary.

The LIS3 has a 16-bit resolution and the capability to measure up to 2 G's (G=acceleration of gravity=9.8 m/s^2) of acceleration in the positive or negative direction yielding a total acceleration range is 4 G's. With the accelerometer placed flat, the output should read 0G, 0G, 1G for the x, y, and z axes respectively. A test of 423 acceleration readings resulted in average values of 2.36×10^{-4}, -8.95×10^{-4}, and -1.0118 (standard deviation of 1.45×10^{-3}, 1.054×10^{-3}, 9.74×10^{-4} G) for the x, y, and z axes respectively. While the LIS3's zero-G offset is factory calibrated, stress induced by the mounting process causes the error shown in the test. Since the device is used as a motion detector and not an absolute acceleration detector, the offset is of little importance so long as it remains constant. To determine a threshold, several automobile events were characterized including normal acceleration from 0-20 mph, low speed 90 degree turns and normal deceleration from 20-0mph. Each event was found to deviate from the resting average by at least 0.1 G in both the X and Y axes. A threshold acceleration of 0.08 G (5000% of the resting average deviation) is used to determine when motion has occurred.

4.2.6 Battery Charger

Of the common battery chemistries available, lithium ion batteries provide the highest energy density. The high potential difference between the positive and negative electrodes provides a large cell voltage, approximately three times that of nickel based rechargeable [42]. Additionally, properly handled Li-ion batteries are not subject to memory effects which cause peak voltage drops abnormally fast with

repeated overcharging. Theses benefits along with the highest rechargeable battery energy density make Li-ion batteries an ideal choice for the GPS-RT.

Li-ion batteries have a carbon anode and transition metal cathode between which lithium ions are transported across an electrolyte [43]:

$$C_6 + LiM_2O_4 \xleftrightarrow{dis/charge} Li_xC_6 + Li_{(1-x)}M_2O_4$$

Where M is a transition metal (such as Mn or Co)

Rechargeable Li-ion batteries are susceptible to catastrophic failure if improper charging techniques are used. The charge reaction produces excess heat to the point of explosion when the cell voltage is exceeded. The battery also experiences swelling when forcefully over-discharged [44]. To prevent under or over voltages most consumer Li-ion batteries have built in protection systems in which monitoring circuitry opens the connection to the load or charger [42] when unsafe conditions are experienced.

The Microchip MCP7328 [45] linear charge management system for Li-ion batteries prevents damage to the battery by employing a three phase charging algorithm. The battery is first preconditioned if an under-voltage condition is detected by the sense terminal. This phase uses a low current to minimize heat dissipation in the low voltage condition. A constant current is then supplied for the main charging phase in which the battery voltage reaches the fully charged cell value of 4.2 volts. At this point the battery is restored to approximately 70% capacity [42] and a constant voltage trickle current (approximately 10% of the peak charge current) restores the battery to full capacity.

To provide the option of a 5 volt supply to the RF power amp, two battery chargers are used to recharge two batteries in parallel as shown with the red jumpers of figure 4.9. The combined voltage of two 3.6 volt cells provides 7.2 volts to the regulator.

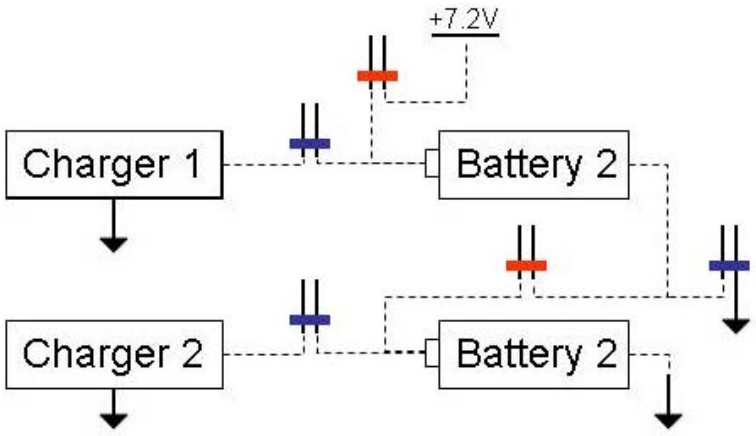

Fig 4.9 Battery Charger circuit: Blue jumpers are connected during charging mode, Red jumpers are connected during operation mode. Battery 2 is replaced with a short for 3.6V operation.

4.2.7 Voltage Regulator

The two main voltage regulator IC types are linear and switching [46]. The GPS-RT revision B uses both types to regulate system voltage. A switching regulator is used for the high current requirements of the RF power amp and a linear regulator for the remaining components. The voltage regulator also serves to prevent excess current draw which the Li-ion battery is capable of supplying to the point of destroying the circuit.

In linear regulators a voltage controlled current source (VCC) is powered by an input voltage and feedback regulated from the output. The voltage input (Vin) is connected to the collectors of a Darlington pair of NPN transistors, driven by a PNP with its collector also connected to Vin. A voltage divider at the output provides

feedback through a voltage referenced error amplifier. The feedback controls the PNP transistor providing a constant output voltage regardless of current in a steady state. Capacitors at the output terminal reduce transient effects by allowing the feedback loop more time to correct for sudden spikes in output voltage due to change in current draw.

Since the linear regulator input voltage must power two base-emitter junctions (NPN Darlington pair) and a collector-emitter junction (PNP) this topology is not ideal for a system in which battery size is a limiting factor. Low dropout (LDO) regulators modify the linear regulator to use a single transistor to reduce the voltage drop across the regulator as shown in figure 4.10. Thus a lower input voltage is required to maintain the 3V rail of the GPS-RT. The LDO regulator maintains the benefits of fast compensation for varying current loads with output sensing feedback.

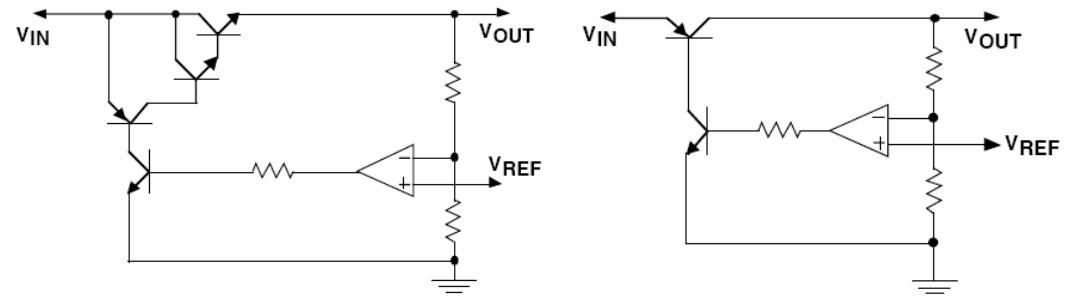

Fig. 4.10. Standard Linear voltage regulator topography (left), Low dropout linear regulator (right) [46]

To provide the high power requirements of the RF power amp, a switching regulator is used. The buck (voltage reduction) regulator also uses a transistor to control incoming voltage but instead of a linear feedback circuit, a pulse width modulated (PWM) signal feeds current into an LC circuit at the output of the regulator. A diode is connected at the voltage output to prevent current flowing to

ground when the PWM signal opens the switch to the input voltage. The LC circuit acts as a filter resulting in an output voltage equal to the peak pulse amplitude times the duty cycle. The inductor current increases and decreases with the switch closing and opening. As the current decreases with an open switch, the voltage at the diode end of the inductor decreases until the diode turns on allowing current flow from the inductor to the circuit. This topology is shown in figure 4.11

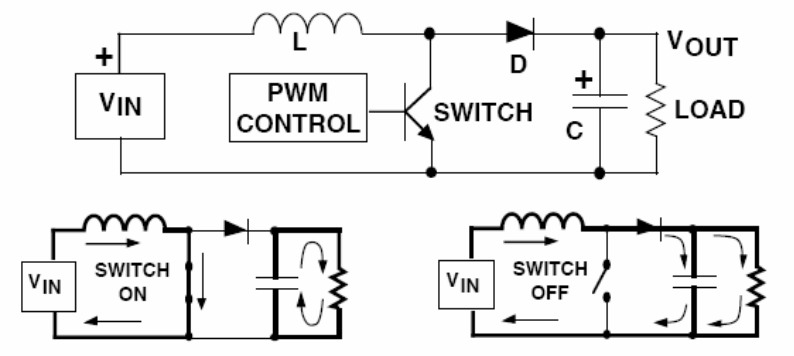

Fig 4.11. Switching regulator operation. [46]

Since the circuit continually switches, the output voltage is less stable than LDO regulators. To compensate, large value inductors and capacitors are used which in turn leads to large sized components on the circuit board. These disadvantages make the switching regulator suitable only for the evaluation circuit and RF power amp testing and result in the final assembly of revision B, shown in figure 4.12. Future revisions will include higher capacity LDO regulators.

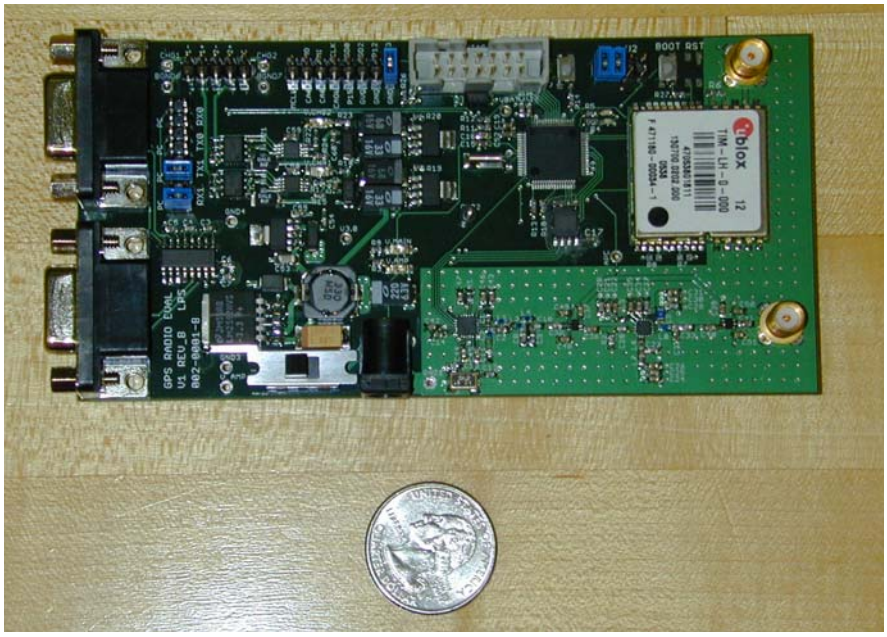

Fig 4.12. Final assembly of GPS-RT rev B.

4.3 Software

The MSP430F1612 has a program space of 55 KB flash memory with an additional 5 KB of RAM. Coupled with features such as a hardware multiplier, the vast program space allows the MCU to perform advanced processing on incoming data beyond simple storage and retrieval. This ability is essential for determining when to shut down various components. Also, time required for functions such as data transmission can be greatly reduced. Since full power RF transmission draws up to 2 amps, minimizing transmission greatly increases the systems operating lifetime.

The software is structured as an interrupt driven state machine. To provide maximum flexibility for software development, the hardware for revision B can function as either a base station (connected to a PC) or a roaming node (for logging data). While in base station mode, all components are fully powered and the user has access to each device via a command line interface (CLI) run through a serial port in a HyperTerminal program. The GPS-RT provides the processing for the text based

user interface so no native PC program is needed, aside from the standard HyperTerminal.

The roaming mode however, operates independently. The node switches between five states based on its geographic position and radio transmissions. The five main states are initialization, sleep, hibernation, transmit, and data processing shown in figure 4.13

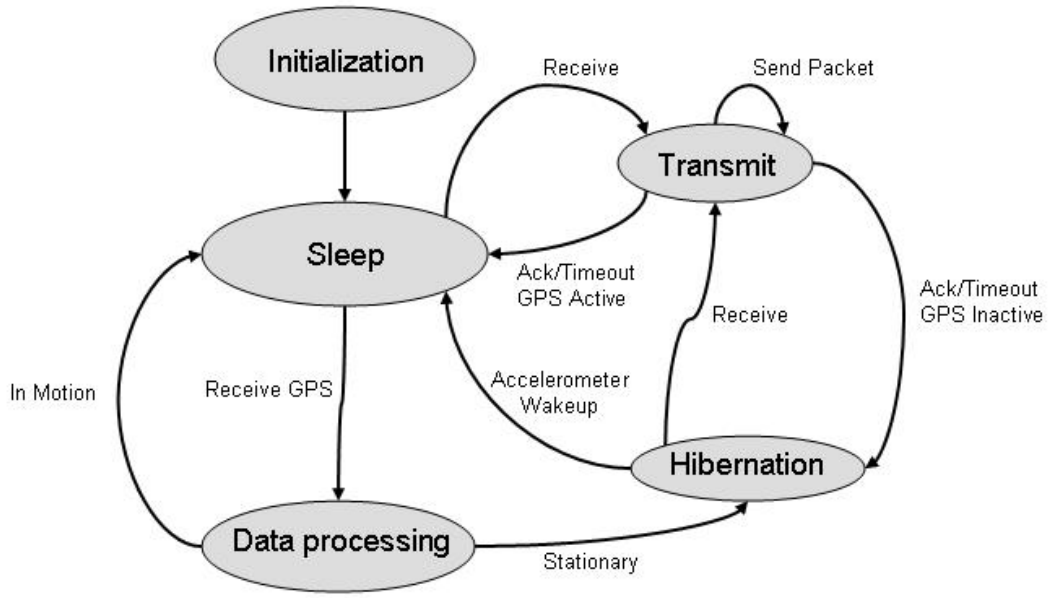

Fig 4.13. GPS-RT roaming unit state machine.

4.3.1 State Machine

The initialization state begins by configuring microcontroller peripherals. An internal 4 MHz clock and external 32 kHz watch crystal oscillator are enabled. The watch crystal maintains a low power, low speed system clock to handle interrupts when the MCU is in deep power down mode with the main 4 MHz clock idle. The

A/D converter is enabled as a battery voltage monitor and ports 1 and 2 are configured to accept interrupts.

Each component has an initialization script to set its control registers, interrupts and communication with the MCU. This stage sets the radio communication properties (operating frequency = 433 MHz, modulation = 2-FSK, packet size = 64 byte, data rate = 250KBs or 1KBs, checksum handling disabled, and valid RX confirmation mode), GPS acquisition properties (data output code = NMEA GLL position and time character string, acquisition, transmission and sleep timers), and accelerometer measurement (resting drift threshold, power down, and 3-axis enabled). The previously stored NMEA coordinates and node state logs are counted so each additional point is appended to the next available free 64 bytes.

The roaming node then enters the main sleep state where the GPS begins an acquisition and sleep cycle. GPS current consumption is reduced by 60mA when in sleep mode. Ephemeris data remains valid for up to 2 hours allowing the GPS to "hot start" and reacquire a signal in less than 5 seconds (without receiving a complete GPS frame). This time determines the lower limit for power consumption during active logging.

When a valid GPS position string is received, the MCU enters the data processing state, storing the position in memory and determining whether or not the roaming node has changed position. An initial position is stored in MCU RAM to minimize access to flash memory historical positions. Subsequent incoming positions are received and compared to the position in RAM. If new positions are within the drift range of the receiver, the timestamp on the new position is compared to the

timestamp stored in RAM. If 2 or more minutes have elapsed with new positions remaining within the established drift margin (chosen to be 5m based on the TIM-LH datasheet and acquired data), the node enters the hibernation state. If the node position has changed, processing completes and the system returns to sleep.

When the system determines position has not changed, there is no need to continue recoding GPS data and the state machine enters hibernation. To ensure an exit from this state the accelerometer is calibrated to provide the resting acceleration measurement. Adding 0.1G to this measurement results in the motion detection threshold for system wakeup. Hibernation begins with accelerometer calibration. The average of 10 x-axis readings becomes the baseline from which the motion detection threshold is calculated. If 3 sequential calibration attempts fail to establish a mean value within the drift margin, the device is determined to be in motion. The state machine exits hibernation and enters sleep mode upon accelerometer wakeup or calibration failure.

The transmission state is initiated by a radio interrupt indicating a packet has been received. Packets sent out by the base station are queries or system commands requiring a response. The base station request packets are repeated 255 times or until a response is received from the roaming node. The roaming node also requires acknowledgement for select data types including complete memory downloads and data rate switching. Other packets are sent one time and the node returns to the low power state that received the interrupt.

A command line interface (CLI) protocol is available for user base station operation. Each component can be configured from the CLI in addition to

downloading data stored in flash. The CLI includes a remote node in which each command is relayed to a roaming node, allowing for remote maintenance of all functions available during base station mode.

4.4 Summary

A low power remote embedded system was developed to store GPS data in flash memory and respond to radio requests over a 1 mile range with the goal of a 1 week operating lifetime. The GPS-RT incorporates many power saving features and accomplishes the goal of transmitting data over a 1 mile RF link. A battery solution has not been finalized so various parameters such as GPS and radio sleep time are undetermined but configurable to accommodate a 2 amp hour battery. Further improvements to the GPS-RT include a size reduction possible by combining the microcontroller and flash memory into a single 3DI module.

5. Conclusion

5.1 Summary

Standard processes adapted for 3DI include thinning and surface activation bonding. Silicon wafer thinning for SOI applications includes a mechanical grind and CMP polish. For 3DI, a backside chemical etch is introduced as a stress relief for active devices present on the topside of the wafer. The combination of excess center thinning during chemical etching and increased edge thinning during CMP can be combined to reduce overall TTV of the thinned substrate in preparation for SAWD bonding. Wafer direct Ar plasma surface activation bonding then builds a 3DI stack to be vertically interconnected.

Along with standard technologies adapted for the specific purpose of 3DI, a novel fine pitch via etching and fill process was developed. The via etching process creates 1μm diameter vias with a depth of 20μm in bulk silicon substrates. The vias are patterned in a 2μm TEOS hard mask and etched with a $C_4F_8/CH_2/Ar$ plasma chemistry. The bulk silicon is etched with a $SF_6/O_2/HBr$ plasma, with each reactive plasma magnetically focused for a vertical etch profile with high anisotropy. The use of SiF_4 as an oxide growth catalyst prevents damage to via sidewalls from ion bombardment. Simultaneously, a passivation layer is grown to prevent electrical connections from the via fill interconnect to the substrate by Al spiking. The vias are filled with an 8% AlGe alloy which endorses plastic deformation below the melting point of aluminum.

The thinning, bonding and via processes can all be applied to COTS component chips when processed as a RDW. A 90% fuming nitric acid soak removes die from plastic injection molded packaging. IPA limits post de-packaging oxidation and removes etch residue. A flip chip placing tool positions die face down on a handle wafer using a 3μm spin deposited acrylic adhesive. Gaps are filled and sidewalls are protected from thinning damage by grinding and chemical etching using a low melting point synthetic wax. Die are chemically thinned to 30μm without sidewall etching or undercutting. A thinned RDW, after cleaning, is prepared for SAWD bonding at which point standard 3DI processing of the stack continues.

The de-packaged components are all present in the GPS-RT remote low power embedded system. Components include a MCU, flash memory, GPS receiver and processing module, 1 watt radio transceiver and accelerometer. Each component was required to have a software configurable low power mode. The MCU node state machine software responds to component interrupts to select low power modes and extend battery lifetime.

5.2 Future Work

While the 3DI via process is fully capable of producing fine pitch high aspect ratio vias through silicon, resistivity measurements on via interconnects are unavailable. An intermediate testing process involving backside metallization of filled via wafers is currently under development to determine via fill yields and electrical connectivity. The thinning and bonding processes require additional characterization before integration with the via process. Successful thinning has been achieved down

to 30μm however; CMP finishing steps have not yet provided sufficient reduction of chemical die etching edge effects. Final RDW wafer TTV remains above the 1μm threshold for SAWD bonding. Excessive particle counts remain after CMP polishing requiring a more comprehensive cleaning step. Currently, a new CMP slurry dispense method is under development which will significantly reduce effects of slurry agglomeration. A successful RDW bonding process is necessary before thinned de-packaged die can be tested for electrical functionality.

The components on the GPS-RT have been evaluated and are controlled by a software state machine for low power operation. A future revision (Rev. C) is pending which separates base station and roaming node functionality. Size of the roaming node is significantly reduced. Preliminary layouts indicate dimensions of 1.25" x 3" (figure 5.1). The footprint of the Rev. C roaming unit shown in figure 5.1 is reduced by 71% over Rev. B. Additional battery monitoring code and radio power ramping will further increase the field operating lifetime of the GPS-RT. Roaming unit power consumption will be fully characterized using Rev. C.

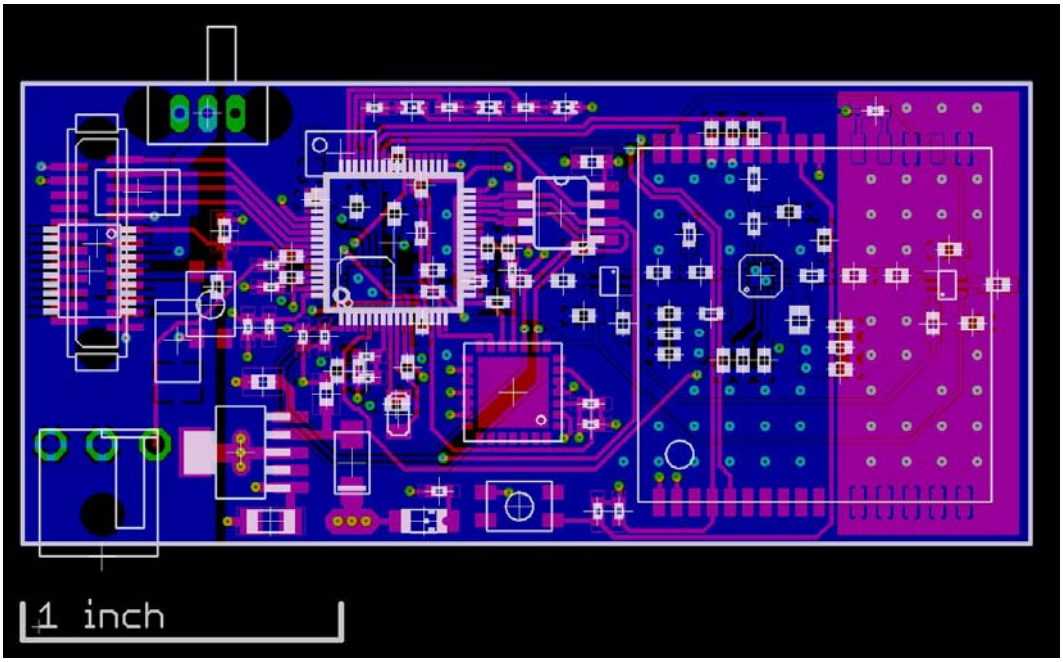

Fig. 5.1 GPS-RT revision C preliminary layout

5.3 Additional Applications

While the 3DI process can be applied to create custom multi chip modules for simple sensor systems, the fine pitch interconnects also allow for a high degree of on chip connectivity. For modern data intensive computation in which 64 bit busses are required for high speed data transfer, vertical interconnects can drastically reduce the need for routing signals to chip edges for connections to additional processors. Multiple processors can be stacked and busses routed directly through the chip. Shorter interconnect length leads to a reduction in parasitics, further increasing data transfer rates. For high end computing applications involving dozens to thousands of processors, an additional routing dimension would significantly reduce metallization requirements for common busses and power connections.

In addition to reducing circuit footprint, use of thinned die is also beneficial to flexible circuits. Instead of fiberglass PCBs, a 50μm sheet of polyimide is used as a circuit board. Preliminary metallization techniques allow the patterning of bond pads and interconnect traces. De-packaged die are flip chip bonded directly to fine pitch bond pads directly on the substrate. Coupled with emerging low profile lithium polymer battery technology, complete battery powered embedded systems are possible within a thickness of only 1mm.

5.4 Conclusion

The technologies developed in the 3DI process, its production applications, and the GPS-RT all contribute to reducing the size and power consumption of remote embedded sensor systems. 3DI technologies presented contribute to high degrees of component integration and overall compacting of system hardware. With various modifications to the process along with RDW processing, COTS components are compatible with 3DI. Integrating these components into a remote embedded system designed for low power operation greatly increases the field operating capability and applications.

APPENDIX A

Karl Suss 6” wafer spinner and contact aligner parameters for wafer dispense and exposure

2um Positive Photoresist

Static dispense: 4ml HMDS adhesion promoter
Spin: 60s, 2000rpm
Static dispense: 4ml OIR 908-35 positive photoresist
Spin: 60s, 2000rpm
Spin: 30s, 1000rpm
2mm Edge bead remover
Spin: 10s, 1000rpm
Pre-bake: 60s, 90C
Exposure: Vacuum contact, 4s, 385nm, 375W
Post-bake: 60s, 120C
Development: OPD4262, 90s
Hard-bake: 30min, 130C convection oven

HAR via 2um Positive Photoresist

Static dispense: 4ml HMDS adhesion promoter
Spin: 60s, 2000rpm
Static dispense: 4ml OIR 908-35 positive photoresist
Spin: 60s, 2000rpm
Spin: 30s, 1000rpm
2mm Edge bead remover
Spin: 10s, 1000rpm
Pre-bake: 90s, 105C
Exposure: Vacuum contact, 8s, 385nm, 375W
Post-bake: 90s, 120C
Development: OPD4262, 60s
Hard-bake: 30min, 130C convection oven

Humiseal 3um Acrylic

Static Dispense: 5ml 1:1 (Humiseal:Acetone)
Spin: 30s, 750rpm
Post-bake: 240s, 120C

3um Negative Resist

Static Dispense: 8ml AZ1500PY-NR (negative resist)
Spin: 60s, 2000rpm
Pre-bake: 60s, 90C
Exposure: Proximity Contact, 7.7s, 385nm, 375W
Post-bake: 60s, 120C
Development: RD6, 20s

BIBLIOGRAPHY

[1] Taquet et al., *Marine Ecology Progress Series*, vol. 306, pp. 295-302, 2006

[2] E. Vardaman, L Matthew, "New Developments in Stacked Die CSPs," *Proc of HDP*, pp. 29-30, 2004

[3] R. Zhang, K. Roy, D. Janes, "Architecture and Performance of 3-Dimensional SOI Circuits," *IEEE International SOI Conference*, pp. 44-45, 1999

[4] L. Mayor, *Future Fab Intl.* vol. 15, 2003

[5] I. Christianes, G. Roelkens, K. De Mesel, "Thin-Film Devices Fabricated With Benzocyclobutene Adhesive Wafer Bonding," *Journal of Lightwave Technology*, vol. 23, pp. 517-523, 2005

[6] H. Jiun, I. Ahmad, "Effect of Wafer Thinning Methods Towards Fracture Strength and Topography of Silicon Die", *Microelectronics Reliability*, vol. 46, pp 836-845, 2006

[7] Chen J, De Wolf I., "Study of Damage and Stress Induced by Backgrind in Si Wafers," *Semicond Sci Technol*, vol. 18, pp. 261-268, 2003

[8] S. S. Iyer, A. J. Auberton-Herve, *Silicon Wafer Bonding Technology for VLSI and MEMS Applications*, INSPEC, 2002

[9] K. Mitani, *Symp. on SOI Technology*, Semicon/West, p. 67, 1995

[11] M. Bachman, INRF Application Note HNA01, "Isotropic Silicon Etch Using HNA" *UCI Integrated Nanosystems Research Facility*, 2000

[13] M.R. Litchy, K. Nicholes, D.C. Grant, R.K.Singh, "Characterization of Circulated Chemical-Mechanical Polishing Slurry Particles using TwoAnalysis Methods," *Proc. of the ECS ISTC*, 2001.

[14] I. Christiaens, G. Roelkens, "Thin Film Devices Fabricated With Benzocyclobutene Adhesive Wafer Bonding" *IEEE Journal of Lightwave Technology*, vol. 23, pp. 517-523, 2005

[15] D. Pasquariello, K. Hjort, "Plasma-Assisted InP-to-Si Low Temperature Wafer Bonding" *IEEE Journal on Selected Topics in Quantum Electronics*, vol 8. pp.118-131, 2002

[16] A. Auberton-Herve, "SOI: Materials to Systems," *IEDM*, pp. 3-10, 1996

[17] H. Takagi, R. Maeda, T. R. Chung, T. Suga, "Low Temperature Direct Bonding of Silicon and Silicon Dioxide by the Surface Activation Method," *International Conference on Solid-State Sensors and Actuators*, pp. 657-661, 1997

[18] U. Gosele et al., "What Determinse the Lateral Bonding Speed in Silicon Wafer Bonding," *Applied Physics Letters*, vol. 67, pp. 863-865, 1995

[19] D. R. Franca, A Blouin, *Measurement Science and Technology*, vol. 15, pp 859-868, 2004

[20] Robert Bosch GmbH, US patent 4,855,017

[21] F. Laermer, A. Urban, R. Bosch GmbH, "Milestones in Deep Reactive Ion Etching" *International Conference on Solid-State Sensors and Actuators*, pp. 1118-1121, 2005

[22] M. Khbeis, G. Metze, K. Powell, D. Thomas, A. Pentland, J. Hutchings, "Profile Control for Deep Silicon Etch by Sidewall Passivation in High Density Plasma," *AVS 50th Symposium*, Nov 2003.

[23] G. Feng, X. Peng, J. Cai, S. Wang, "Through Wafer Via Technology for 3-D Packaging," *6th International Conference on Electronic Packaging Technology*, 2005

[24] A.G. Dirks, M.N. Webster, P. Turner, P. Rich, and D.C. Butler. *Journal of Applied Physics,* vol. 85, pp. 571-577, Jan 1999.

[25] J.M. Hu, M. Pecht, A. Dasgupta, "Design of Reliable Die Attach," *International Journal of Microcircuits and Electronic Packaging*, vol. 16, pp. 1-20, 1993

[26] D. Barker, "Wire Bond Interconnects," *UMCP course ENME693*, Fall 2004

[27] Texas Instruments SLAS368D, "MSP430x15x, MSP430x16x, MSP430x161x Mixed Signal Microcontroller," 2005

[28] IEEE 1149.1 "Standard Test Access Port and Boundary-Scan Architecture (Joint Test Action Group)", 1990

[29] A. Thean, J. Leburton, "Flash Memory: Towards Single-Electronics," *IEEE Potentials*, pp. 35-41, 2002

[30] M. Chiang, P. Lee, R. Chang, "Managing Flash Memory in Personal Communication Devices", *Proceedings of 1997 IEEE International Symposium on Consumer Electronics*, pp. 177-182, 1997

[31] H. Kim, S. Lee, "A New Flash Memory Management for Flash Storage System" *Computer Software and Applications Conference*, pp. 284-289, 1999

[32] ST Microelectronics 8495, "M25P80 8MBit, Low Voltage, Serial Flash Memory with 40 MHz SPI Bus Interface" rev 10, 2006

[33] Global Positioning System, Standard Positioning System Service, Signal Specification, 2nd Edition, 1995

[34] U-Blox GPS-X-02007, "GPS Basics Introduction to the System Application Overview"

[35] U-Blox GPS.G3-MS3-01001-B, "TIM-Lx GPS Modules", rev. B 2004

[36] Chipcon SWRS038a, "CC1100 Datasheet", rev 1.1

[37] RFMD 060620, "RF5110G Datasheet", rev A2

[38] California Eastern Laboratories, "UPG2009TP; NEC's L, S-Band 4W SPDT Switch," 2004

[39] O. Ata, "In-Building Penetration Loss Modeling and Measurement in Suburban, Urban and Dense Urban Morphologies," *Antennas and Propagation Society international Symposium*, vol 1A, pp. 779-802, 2005

[40] C. Tan, S. Park, "Sesign of Accelerometer-Based inertial Navigation Systems," *IEEE Transactions on Instrumentation and Measurement*, vol. 54, pp. 2520-2530, 2005

[41] ST Microelectronics CD00047926, "LIS3LV02DQ MEMS Inertial Sensor," rev. 1, 2005

[42] D. Salerno, R. Korsunsky, "Practical Considerations in the Design of Lithium-Ion Battery Protection Systems," *Applied Power Electronics Conference and Exposition*, vol. 2, pp. 700-707, 1998

[43] C. Simpson "Battery Charging," *National Semiconductor Design Guide F7*, 2006

[44] D. Spillman, E. Takeuchi, "Lithium Ion Batteries for Medical Devices," *14th Annual Battery Conference on Applications and Advances*, pp. 203-208, 1999

[45] Microchip DS21706A, "MCP73828 Single Cell Lithium-Ion Charge Management Controller with Charge Complete Indicator and Temperature Monitor," 2002

[46] C. Simpson “Linear and Switching Voltage Regulator Fundamentals,” *National Semiconductor Design Guide F4*, 2006