

ABSTRACT

Title of Thesis: CHARACTERIZATION OF 4H-SiC MOSFETs USING
FIRST PRINCIPLES COULOMB SCATTERING
MOBILITY MODELING AND DEVICE SIMULATION

Siddharth Potbhare
Master of Science, 2005

Thesis directed by: Professor Neil Goldsman
Department of Electrical and Computer Engineering

Detailed analysis of a 4H-SiC MOSFET has been carried out by numerically solving the steady state semiconductor Drift-Diffusion equations. Mobility models for bulk phonon scattering, surface phonon scattering, surface roughness scattering, Coulomb scattering by interface traps and oxide charges, and high field effects, have been developed and implemented. A first principles Coulomb scattering mobility model has been developed specifically to model the physics of the inversion layer in 4H-SiC MOSFETs. The Coulomb scattering model takes into account, scattering of mobile charges by occupied interface traps and fixed oxide charges, distribution of mobile charges in the inversion layer, and screening. Simulated IV curves have been compared to experimental data. Density of states for the interface traps have been extracted, and seem to be in agreement with experimental measurements. Simulations indicate that occupied interface traps in 4H-SiC MOSFETs are responsible for mobility degradation, low currents and high threshold voltages. Their effect diminishes at high temperatures due to reduction in trap occupancy, and at high gate voltages due to increased screening. At high gate voltages, surface roughness scattering plays the major role in mobility degradation in 4H-SiC MOSFETs.

CHARACTERIZATION OF 4H-SiC MOSFETs USING FIRST PRINCIPLES
COULOMB SCATTERING MOBILITY MODELING AND DEVICE SIMULATION

by

Siddharth Potbhare

Thesis submitted to the Faculty of the Graduate School of the
University of Maryland, College Park in partial fulfillment
of the requirements for the degree of
Master of Science
2005

Advisory Committee:

Professor Neil Goldsman, Chair
Professor Pamela Abshire
Professor Martin C. Peckerar

DEDICATION

To my parents

ACKNOWLEDGEMENTS

First and foremost, I would like to thank my advisor Dr. Goldsman, for all the advice and support he has given me ever since I joined his group. I thank him for this willingness to listen to whatever I had to say, and his patient guidance over the years, which has enabled me to do this work. I would like to thank Dr. Abshire and Dr. Peckerar for taking time off their busy schedules and reading my thesis, and serving on my thesis committee. I would like to say thank you to Dr. Gary Pennington for his help and invaluable inputs throughout this work. I would like to thank Mr. Aivars Lelis and his group at ARL for providing me with experimental data that was so necessary for this work. I would like to thank my parents and my family for their unvarying belief in me. Thank you to my lab-mates Akin, Amrit, Bo, Datta, Gary, Latise and Zeynep for lots and lots of fun-filled discussions on Silicon Carbide and life in general. I would also like to thank all my friends and roommates here at College Park for making this place a home away from home.

TABLE OF CONTENTS

List of Figures.....	vii
List of Tables.....	x
1. Introduction	1
1.1. Motivation.....	3
1.2. Outline.....	3
1.3. Previous work in SiC device simulation.....	5
1.4. My Approach	6
2. Drift Diffusion Modeling and Numerical Analysis	8
2.1. Drift Diffusion Model	8
2.1.1. Poisson's Equation.....	9
2.1.2. Current Equations.....	10
2.1.3. Continuity Equations.....	11
2.1.4. Steady State Drift Diffusion Model	12
2.1.5. Generation and Recombination.....	13
2.2. Numerical Methods for Drift-Diffusion Simulation of SiC MOSFETs	16
2.2.1. Boundary Conditions	16
2.2.2. Finite Difference Discretization of the Semiconductor Equations.....	22
2.2.3. Numerical Methods.....	27
2.2.4. 2D Mesh.....	31

3. Coulomb Scattering Mobility Model.....	32
3.1. Need for a Robust Coulomb Scattering Mobility Model for 4H-SiC MOSFETs	32
3.2. Deriving the quasi 2D Coulomb Scattering Rate Equation	34
3.3. Depth Dependent Coulomb Scattering Mobility Equation.....	44
3.4. Physics of the Coulomb Scattering Mobility Model.....	45
4. Complete Mobility Model and Simulation Technique for 4H-SiC MOSFET	48
4.1. Complete Mobility Model.....	49
4.1.1. Bulk Mobility	49
4.1.2. Surface Phonon Mobility	50
4.1.3. Surface Roughness Mobility	53
4.1.4. Coulomb Scattering Mobility.....	54
4.1.5. High Field Mobility.....	54
4.1.6. Total Mobility	56
4.2. Simulation Technique and Application to 4H-SiC MOSFETs.....	56
4.2.1. Interface Trap Model.....	56
4.2.2. Fixed Oxide Charge Density	65
4.2.3. 4H-SiC MOSFET Parameter Extraction Scheme	69
5. Simulation Results and Interpretations	71
5.1. Room Temperature Fits to Experimental Data	72
5.2. Room Temperature Physics of 4H-SiC MOSFETs	77
5.2.1. Interface Traps in 4H-SiC MOSFETs.....	77
5.2.2. Surface Roughness	81

5.2.3.	Total Low Field Mobility.....	83
5.2.4.	Electron Concentration and Current Density	86
5.2.5.	Comparing Coulomb Mobility and Surface Roughness Mobility.....	91
5.2.6.	Effect of Screening.....	94
5.3.	Device Performance Predictions based on Simulations.....	97
5.3.1.	Reduction of the Occupied Interface Trap Density.....	97
5.3.2.	Reduction in Surface Roughness.....	103
5.3.3.	Combined Reduction of Interface Trap Density and Surface Roughness.....	105
5.4.	Future Work	109

LIST OF FIGURES

Figure 2.1. 4H-SiC MOSFET device structure.....	17
Figure 2.2. Work function difference between n -type polysilicon gate and p -type epilayer 4H-SiC MOSFET	21
Figure 2.3. Flowchart for solving the drift-diffusion semiconductor equation system.....	30
Figure 3.1 Complex poles (p_1 and p_2) of the term inside the integral which gives the quasi-2D matrix element H_{2D} (Equation 3.11).	38
Figure 3.2. The quasi-2D scattering wavevector shown as difference between the final and the initial wavevectors.	41
Figure 4.1. Interface trap density of states for 4H-SiC MOSFET. $D_{it_{edge}} = 9.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ $D_{it_{mid}} = 4.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and $\sigma_{it} = 0.0515$	58
Figure 4.2. Fermi distribution function and the density of occupied acceptor-type interface traps at a low gate voltage of -2V.....	61
Figure 4.3. Fermi distribution function and the density of occupied acceptor-type interface traps at a gate voltage of 2V.	62
Figure 4.4. Occupation of acceptor-type interface traps by electrons at two different temperatures.....	64
Figure 4.5. Measured threshold voltage and threshold voltage calculated by excluding the effect of fixed charge density and occupied interface trap density, at different temperatures.....	67
Figure 4.6. Plot of the difference between fixed oxide charge density and the occupied interface trap density as a function of temperature, obtained from threshold voltage measurements.	68
Figure 5.1. Drain current versus gate-source voltage on a logarithmic scale, for the $200\mu\text{m} \times 200\mu\text{m}$ 4H-SiC MOSFET at room temperature, and a drain-source voltage of 0.25V.	73

Figure 5.2. Drain current versus gate-source voltage on a linear scale, for a 200 $\mu\text{m}\times$ 200 μm 4H-SiC MOSFET at room temperature, and a drain-source voltage of 0.25V.....	74
Figure 5.3. Drain current versus drain-source voltage for a 200 $\mu\text{m}\times$ 200 μm 4H-SiC MOSFET at room temperature.....	75
Figure 5.4. Interface trap density of states profile for a 4H-SiC MOSFET.....	76
Figure 5.5. Comparison of the inversion charge density (N_{inv}) and the occupied interface trap density (N_{it}) at different gate voltages, at room temperature.....	79
Figure 5.6. Coulomb scattering mobility (μ_C) plotted as a function of depth inside the semiconductor, at different gate voltages.....	80
Figure 5.7. Surface roughness mobility (μ_{SR}) plotted as a function of depth inside the semiconductor.....	82
Figure 5.8. Figure showing the comparison between the various low field mobility components at a gate-source voltage of 6V, and at room temperature.....	84
Figure 5.9. Total low field mobility (μ_{LF}) as a function of depth, at the center of the channel. Gate-source voltages range from -2V to 8V.....	85
Figure 5.10. Variation of electron concentration with depth, at the center of the channel, shown for different gate-source voltages and at room temperature.....	88
Figure 5.11. Current density variation with depth for a 4H-SiC MOSFET at room temperature..	89
Figure 5.12. Average depth of the inversion layer (Z_{avg}) plotted as a function of gate-source voltage, at room temperature.....	90
Figure 5.13. Comparison between Coulomb scattering mobility (μ_C) and surface roughness mobility (μ_{SR}) at a gate-source voltage of 2V.....	92
Figure 5.14. Comparison between Coulomb scattering mobility (μ_C) and surface roughness mobility (μ_{SR}) at a gate-source voltage of 12V.....	93

Figure 5.15. Low field drain current versus gate-source voltage characteristics for the two cases of screened and unscreened Coulomb scattering mobility models.	95
Figure 5.16. Coulomb scattering mobility plotted as a function of depth inside the semiconductor for the case of unscreened Coulomb scattering.	96
Figure 5.17. Comparison of the inversion charge density (N_{inv}) and the occupied interface trap density (N_{it}) at different gate voltages, for two different interface trap density of states profile...	99
Figure 5.18. Coulomb scattering mobility (μ_C) plotted as a function of depth inside the semiconductor, at different gate voltages, for the case of reduced interface trap densities.	100
Figure 5.19. Current density variation with depth at room temperature for a 4H-SiC MOSFET with reduced density of states of the interface traps.	101
Figure 5.20. Drain current versus gate-source voltage for a 4H-SiC MOSET at room temperature, and drain-source voltage of 0.25V.	102
Figure 5.21. Drain current versus gate-source voltage curve for a 4H-SiC MOSET at room temperature and a drain-source voltage of 0.25V.	104
Figure 5.22. Comparison of the improvement in currents due to reduction in surface roughness, and the reduction in interface trap density of states, at a gate-source voltage of 4V. A.	106
Figure 5.23. Current density variation with depth at the center of the channel in a 4H-SiC MOSFET, after reduction in the density of interface states at the band edge, and a reduction in the surface roughness, by a factor of 10 each.	107
Figure 5.24. Drain current versus gate-source voltage at room temperature, with the surface roughness and the interface trap density of states reduced by a factor of 10 each.	108

LIST OF TABLES

Table 1.1. Important physical properties of Si and polytypes of SiC	2
Table 4.1. Parameter values used for calculating the bulk mobility in a 4H-SiC MOSFET.	50
Table 4.2. Parameter values for calculating surface phonon mobility in 4H-SiC MOSFETs.	53

CHAPTER 1

1. Introduction

Silicon Carbide is fast becoming a material of reckoning for manufacturing of high temperature high power integrated circuits. In addition to a large bandgap, high thermal conductivity and a very high breakdown field, the main characteristic that sets SiC apart from other wide bandgap materials, is its ability to grow a natural oxide. Like silicon, it is possible to grow silicon dioxide on a silicon carbide substrate. This characteristic of SiC makes it easy to manufacture SiC MOSFETs and other devices which have been traditionally made using silicon. Through the years since the first integrated circuit, silicon based devices have been able to meet the need for smaller, faster, cheaper, more reliable, and more diverse electronic circuits. But all silicon based ICs have faced limitations in terms of operating temperatures ($<150^{\circ}\text{C}$) and usable power. SiC based devices and integrated circuits will work at much higher temperatures, and much higher power, as compared to Si based devices. Table 1.1 shows a comparison of the material properties of SiC and Si. Owing to its larger bandgap and superior thermal conductivity, it should be possible to use SiC based devices at temperatures up to 500°C . Also, because of the large bandgap and huge breakdown electric field, SiC devices can operate at voltages in excess of several hundred volts. A large bandgap enables very low leakage currents induced by the build-up of free charges, and thermal runaway resulting from impact ionization process. Devices are

expected to have fast switching speeds and low energy loss, even at high temperatures. SiC can drive the microelectronic revolution originated by Si, to the high temperature high power realm.

Table 1.1. Important physical properties of Si and polytypes of SiC

	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.1	2.39	2.86	3.26
Bulk Electron Mobility (cm ² /Vs)	1500	1000	300	900
Saturation Velocity (10 ⁷ cm/s)	1	2	2	2
Breakdown Field (10 ⁶ V/cm)	1	2	3	3
Thermal Conductivity (W/K·cm)	1.5	4.9	4.9	4.9
Static Dielectric Constant	11.8	9.7	9.7	9.7

Currently, the biggest challenge in development of SiC devices is low surface mobility at the SiC-SiO₂ interface. The reason for this low surface mobility has been shown to be extremely large densities of occupied interface traps at the SiC-SiO₂ interface. The earliest Si devices had high interface trap densities at the Si-SiO₂ interface. By processing refinements over the decades, very high quality SiO₂ can now be grown on Si substrates, eliminating almost all interface traps. Hence, device simulators for Si devices have little need for models for the effects of interface traps on device performance. In order to further develop SiC MOS technology, it is imperative to understand in depth, the causes for mobility degradation and the effect of various scattering mechanisms, particularly surface roughness scattering, surface phonon scattering and Coulomb scattering of inversion layer mobile charges by fixed oxide charges and occupied interface traps. Using an advanced drift diffusion MOSFET device simulator and by developing new models for interface traps and Coulombic scattering of mobile charges, I have tried to extract and isolate causes of device degradation in the various regions of device operation.

1.1. Motivation

The motivation of this thesis is to study the device performance of 4H-SiC MOSFETs using drift diffusion device simulation and to address the issues causing performance degradation in SiC MOSFETs. For this, a methodology has been developed to model the interface traps occurring at the SiC-SiO₂ interface, their occupancy, and their effects in scattering of inversion layer mobile carriers. This has been achieved by developing a comprehensive Coulomb scattering mobility model specifically for scattering by occupied interface traps, and by fixed oxide charges in SiC MOSFETs. The model has been developed from basic first principles physics of scattering of mobile charges by stationary charged scattering centers. I have tried to mold the scattering physics equations in the form of a Coulomb Mobility, which can be directly incorporated in the drift diffusion simulator. Using this new mobility model, it is now possible to separate out, and independently study the effect of the highly dense interface traps in SiC MOSFETs, and discuss whether they or some other mechanisms are responsible for the low surface mobility of these devices.

1.2. Outline

The thesis intends to address in detail the issues related to numerical simulation of SiC devices, and discuss the mobility models that have been implemented in the drift diffusion simulator to model the behavior of 4H SiC MOSFETs.

In the first chapter, I describe the current and past work that has been done in SiC device simulation. I have tried to compile a reasonably complete list of device modeling that has been carried out for SiC devices. It is followed by a short description of my approach to address the issues of SiC device modeling and simulation.

In Chapter 2, I describe the drift-diffusion model for semiconductor devices, and the numerical simulation scheme for a 4H-SiC MOSFET. The chapter describes the discretization of the semiconductor equations in steady state, the meshing scheme used to extract maximum physics of the inversion layer, the numerical methods used to solve the coupled semiconductor equations, and the various physical quantities that can be extracted from the drift diffusion model.

The new Coulomb scattering mobility model developed for 4H SiC MOSFETs is described in Chapter 3. I talk in detail about the physics of Coulomb scattering in semiconductors, and how it is very important for SiC devices. I describe the methodology of deriving a Coulomb Mobility that is easy to incorporate in a MOSFET drift diffusion simulator, from basic physics of scattering in semiconductors.

In Chapter 4, other mobility models representing various other scattering mechanisms have been described. I have included the scattering due to bulk phonons, surface phonons, surface roughness, and high lateral fields, in addition to the occupied interface trap scattering, in the device simulator. I also describe in detail, the modeling of interface trap states in SiC, and a method for extracting the fixed oxide charge density from temperature dependent threshold voltage data, in this chapter.

Finally, in the fifth chapter, I describe the simulation results for 4H SiC MOSFETs. I discuss the various device performance related results that I have extracted by comparing simulated IV curves to experimentally measured data, in this chapter.

1.3. Previous work in SiC device simulation

Zeng *et al.* [1] have shown a method of extracting energy dependent interface trap density for 6H and 4H-SiC MOSFETs in the subthreshold region of operation. Scozzie *et al.* [2] have shown the detrimental effects of interface-trapped charge on the SiC MOSFET characteristics. Arnold *et al.* [3] have shown that interface traps in SiC are responsible for decrease in transconductance, lower mobile inversion charge density and low drift mobility of inversion layer electrons. Saks *et al.* [4] have shown that severe trapping of electrons at the SiC-SiO₂ interface in 4H-SiC devices causes a reduction in the number of free electrons in the inversion layer, and also a drop in the mobility. Correlation between channel mobility and interface traps in SiC MOSFETs has also been described by Suzuki *et al.* [5][6] All these observations have been made on the basis of experiments or compact modeling of SiC devices. Physics based simulations of deep submicron 4H-SiC MOSFETs have been presented by Dubaric *et al.* [7], but the authors have assumed that there are no interface charges at the SiC-SiO₂ interface. Roschke *et al.* [8] have proposed electron mobility models for 4H, 6H, and 3C SiC, which describe the dependence of the electron mobility on doping concentration, temperature and electric field. They too, have not shown any effect of interface traps in their mobility models. Nilsson *et al.* [9][10] have described Monte Carlo and drift diffusion simulations of 4H and 6H-SiC field effect transistors. But they have only considered acoustic phonon scattering, polar and non-polar optical phonon scattering, and ionized impurity scattering. Mickevicius *et al.* [11] have carried out Monte Carlo simulations for SiC, but he has focused on phonon scattering and ionized impurity scattering. Roldán *et al.* [12] include the effect of a net interface charge in their work. However, their interface trap model is not energy dependent. But experimental measurements of interface state density of states for SiC have shown that the density of states is energy dependent. Vathulya *et al.* [13] have used an energy dependent interface state density of states model for 4H

and 6H-SiC MOSFETs, and have extracted the inversion layer mobility by fitting the current equations to experimental data. They have used compact modeling and numerical methods to solve sets of equations simultaneously to extract an average mobility. *Powell et al.* [14][15] have described in detail various mobility models for 6H SiC MOSFETs. Their mobility model incorporates the effect of scattering due to occupied interface traps. But they do not show how scattering varies with depth inside the inversion layer. Their method for dealing with screening of the scattering charge centers in deep inversion is empirical.

1.4. My Approach

My aim is to address the issue of the need for a proper comprehensive mobility model for SiC MOSFETs that can accurately model the physics of the inversion layer in SiC MOSFETs, and is simple enough to be included in a drift diffusion simulator. In addition to the usual scattering mechanisms, the mobility model should be able to describe the effect of scattering of inversion layer mobile charges by the occupied interface traps at the SiC-SiO₂ interface, fixed oxide charges distributed at the interface and in the oxide. In the process, I will be building upon the work done by others, and develop a sophisticated drift diffusion device simulator for SiC MOSFETs.

To solve this problem, I started at the basic physics of Coulombic scattering of charges. I developed a quasi 2D Coulomb scattering model, which described how inversion layer electrons are scattered by stationary charges located at the semiconductor-oxide interface, and/or some distance inside the oxide itself. Using this scattering model, I was able to write an equation for the Coulomb mobility, which was dependent on the density of occupied traps, density of fixed oxide charges, distance between the scattering charges and inversion layer mobile charges, screening of

the scattering charges by the mobile charges, and temperature. The Coulomb mobility equation was simple enough to be included in the drift diffusion modeling scheme.

In order to verify the accuracy of my model, and also to judge the importance of various scattering mechanisms in a 4H-SiC MOSFET, I compared my simulations to experimental data. To make confident predictions about the future performance capabilities of SiC MOSFETs, I first use the experimental data to calibrate my simulator. Once I have determined the proper material properties for my model, and have the comparisons of various performance degrading mechanisms, I can predict the performance of future SiC MOSFETs. My simulations also show that the interface traps lying at different energy levels inside the SiC bandgap have effects at different gate voltage levels. The interface state trap density profile extracted from simulations and comparisons with measured IV data seems to agree with values measured by experiments.

CHAPTER 2

2. Drift Diffusion Modeling and Numerical Analysis

In this chapter, I will present the drift-diffusion model which serves as the basis for the numerical simulation of a SiC MOSFET device. I begin by reviewing the drift-diffusion equations and how they are used for the specific case of simulating a MOSFET device. I will also present the discretization scheme for these equations and the numerical methods that have been used to solve them.

2.1. Drift Diffusion Model

The drift diffusion equations serve as the basic building blocks for semiconductor device modeling and can be derived directly from Maxwell's equations for electromagnetic radiation and the Boltzmann transport equation of kinetic theory. They are, in essence, equations derived from the Boltzmann transport equation by doing certain approximations. The drift diffusion equations consist of the Poisson's equation, the equations for electron and hole currents, and the current continuity equations for electrons and holes. In this section, I describe these equations in brief and then elaborate a little on the numerical methodology that is implemented to solve them for a SiC MOSFET device.

2.1.1. Poisson's Equation

The first of the drift-diffusion equations is the Poisson's equation. It relates the electrostatic potential (ϕ), to the net charge density (ρ) inside a semiconductor.

$$\bar{\nabla} \cdot (\epsilon \bar{\nabla} \phi) = -\rho \quad (2.1)$$

ρ is the net charge density and ϵ is the dielectric permittivity of the material in which the charge is present. Inside the semiconductor, the charge particle concentration consists of negatively charged electron concentrations (n), positively charged hole concentrations (p) and the ionized dopant concentrations (D). The dopants are further separated into positively charged donors (N_D^+) and the negatively charged acceptors (N_A^-). Substituting these values for the net charge density, the Poisson equation can be rewritten as:

$$\bar{\nabla} \cdot (\epsilon \bar{\nabla} \phi) = -q(n - p - D) \quad (2.2)$$

where, q is the net charge on a single electron, and

$$D = N_D^+ - N_A^- \quad (2.3)$$

The electron (n) and hole (p) concentrations are written in terms of the electron and hole quasi-Fermi levels (ϕ_n and ϕ_p).

$$n = n_i \exp\left(\frac{\phi - \phi_n}{V_T}\right) \quad (2.4)$$

$$p = n_i \exp\left(-\frac{\phi - \phi_p}{V_T}\right) \quad (2.5)$$

where, n_i is the intrinsic carrier concentration and V_T is the thermal voltage.

2.1.2. Current Equations

There are two phenomena causing current flow in a semiconductor: (i) Drift and (ii) Diffusion. Presence of an electric field in a semiconductor will cause the free electrons and holes to drift along the field lines. This method produces a current which is known as the drift current. If there is concentration gradient of the electron or hole concentrations, the electrons and holes will flow from the higher concentration region to their lower concentration region generating a current. This current is termed as the diffusion current. The contribution of carrier transport due to drift can be formulated as:

$$\vec{J}_{n,drift} = -qn\vec{v}_n \quad (2.6)$$

$$\vec{J}_{p,drift} = qp\vec{v}_p \quad (2.7)$$

where \vec{v}_n and \vec{v}_p are the drift velocities of electrons and holes respectively, due to an applied electric field. These velocities can be expressed in terms of the mobilities (μ_n and μ_p), and the applied field (\vec{E}).

$$\vec{v}_n = \mu_n \vec{E} \quad (2.8)$$

$$\vec{v}_p = \mu_p \vec{E} \quad (2.9)$$

The diffusion component of carrier transport is due to random motion and gradients in the mobile charge concentration, and is described by the following:

$$\vec{J}_{n,diff} = q\nabla(nD_n) \quad (2.10)$$

$$\vec{J}_{p,diff} = -q\nabla(pD_p) \quad (2.11)$$

D_n and D_p are the electron and hole diffusion coefficients respectively. They can be related to the electron and hole mobilities by the Einstein relations:

$$D_n = \mu_n \frac{k_B T}{q} \quad (2.12)$$

$$D_p = \mu_p \frac{k_B T}{q} \quad (2.13)$$

Here, k_B is the Boltzmann's constant, and T is the temperature.

Combining both, drift and diffusion components, the total expression for the electron and hole currents inside a semiconductor is given as:

$$\vec{J}_n = \vec{J}_{n_{drift}} + \vec{J}_{n_{diff}} = qn\mu_n \vec{E} + q\vec{\nabla}(nD_n) \quad (2.14)$$

$$\vec{J}_p = \vec{J}_{p_{drift}} + \vec{J}_{p_{diff}} = qp\mu_p \vec{E} - q\vec{\nabla}(pD_p) \quad (2.15)$$

Writing the electric field E as a gradient of the electrostatic potential, $\vec{E} = -\vec{\nabla}\phi$, the current equations can be rewritten as:

$$\vec{J}_n = -qn\mu_n \vec{\nabla}\phi + q\vec{\nabla}(nD_n) \quad (2.16)$$

$$\vec{J}_p = -qp\mu_p \vec{\nabla}\phi - q\vec{\nabla}(pD_p) \quad (2.17)$$

2.1.3. Continuity Equations

The continuity equations are based on the conservation of mobile charge. They relate the change in mobile charge concentration in time to the gradient of the current density, and the rates of generation and recombination of carriers. For electrons, the continuity equation is written as,

$$\frac{\partial n}{\partial t} = \frac{1}{q} \vec{\nabla} \cdot \vec{J}_n - R_n + G_n \quad (2.18)$$

The continuity equation for holes is given by

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \vec{\nabla} \cdot \vec{J}_p - R_p + G_p \quad (2.19)$$

where G_n and G_p are the electron and hole generation rates, R_n and R_p are the electron and hole recombination rates, and $\vec{\nabla} \cdot \vec{J}_n$ and $\vec{\nabla} \cdot \vec{J}_p$ are the net flux of electrons and holes in and out of the specific volume. The current continuity equations simply state that the total current flow into or out of a volume of space is equal to the time varying charge density within that volume plus any additions due to generation or recombination that may occur.

2.1.4. Steady State Drift Diffusion Model

In steady state, there is no net change in electron and hole concentration over time. Hence, the continuity equations for electrons and holes can be equated to zero.

$$\frac{\partial n}{\partial t} = \frac{1}{q} \vec{\nabla} \cdot \vec{J}_n - R_n + G_n = 0 \quad (2.20)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \vec{\nabla} \cdot \vec{J}_p - R_p + G_p = 0 \quad (2.21)$$

Substituting the formulae for \vec{J}_n and \vec{J}_p from the current equations in the above equations, we have,

$$\vec{\nabla} \cdot \left[-n\mu_n \vec{\nabla} \phi + \vec{\nabla} (nD_n) \right] - R_n + G_n = 0 \quad (2.22)$$

$$\vec{\nabla} \cdot \left[-p\mu_p \vec{\nabla} \phi - \vec{\nabla} (pD_p) \right] - R_p + G_p = 0 \quad (2.23)$$

Equations 2.20 and 2.21 along with the Poisson's equation (2.1) form the steady state drift diffusion system of equations. These equations are to be solved for the electrostatic potential (ϕ), the electron concentration (n) and the hole concentration (p) inside the device.

It is apparent from the above equations that the mobility, generation and recombination of electrons and holes play important roles in the physics of carrier transport in a device. I will be

describing the mobility model used for 4H-SiC MOSFET devices in detail in the next two chapters. I will briefly touch upon the generation-recombination mechanisms next.

2.1.5. Generation and Recombination

For SiC MOSFET simulation, two types of recombination mechanisms have been modeled. The recombination occurring due to trap centers (Shockley-Read-Hall) and due to direct particle recombination (Auger). The generation of particles due to impact ionization is also included.

Shockley-Read-Hall (SRH) Recombination

The capture and emission of holes and electrons by traps that reside in the mid-band energy zone is modeled using the well known Shockley-Read-Hall (SRH) mechanism of recombination. The SRH recombination rate is given by

$$R^{SRH} = \frac{np - n_i^2}{\tau_p(n + n_i) + \tau_n(p + n_i)} \quad (2.24)$$

where, τ_n and τ_p are the minority carrier lifetimes of electrons and holes respectively. The minority carrier lifetimes for SiC are in order of a few nanoseconds. They are typically around 2 orders of magnitude less than those for Si.

For a n -doped SiC slab, when there is a current flowing through the device, the electron concentration is much higher than the hole concentration ($n \gg p$). If the carrier lifetimes of electrons and holes are taken to be equal ($\tau_n \approx \tau_p$), then the SRH recombination rate can be written as

$$R^{SRH} \approx \frac{np}{\tau_p n} = \frac{p}{\tau_p} \quad (2.25)$$

At room temperature, the intrinsic carrier concentration of 4H-SiC is around $2 \times 10^8 \text{ cm}^{-3}$. For a slab of SiC doped with n -type impurity of the order of 10^{18} donor atoms per cubic centimeters, at room temperature, the hole concentration is going to be around $(10^8)^2/10^{18}$ which is approximately 10^{-30} cm^{-3} . Hence, it is easy to see that the SRH recombination rate in SiC is going to be very small (around $10^{-20} \text{ cm}^{-3}/\text{s}$).

Auger Recombination

SiC is an indirect bandgap semiconductor. Hence the probability of a direct band-to-band recombination by transfer of energy to another carrier is very small. Hence, this recombination mechanism, known as the Auger recombination is rare in SiC devices. In the direct recombination process, a free electron in the conduction band combines with a free hole in the valence band, and the net momentum of the two particle system is carried off by a third free particle, which can be an electron or a hole. The Auger recombination rate is given by

$$R^{Auger} = (np - n_i^2)(C_n n + C_p p) \quad (2.26)$$

where, C_n and C_p are the coefficients representing interactions in which the remaining carrier is an electron and a hole respectively.

Impact Ionization Generation

Generation of particles occurs when a particle with high energy collides with a bonded particle resulting in one additional free electron and one additional free hole. This type of generation is referred to as impact ionization generation. In SiC, it is seen that the free particles do not attain very high energy due to the very high bandgap. Hence, the impact ionization

generation rate is very small. The impact ionization generation rate is modeled as proportional to the carrier current density [16].

$$G^II = \frac{1}{q} (\alpha_n |\vec{J}_n| + \alpha_p |\vec{J}_p|) \quad (2.27)$$

where,

$$\alpha_{n,p} = \alpha_{n,p}^\infty \exp\left(\frac{-b_{n,p}}{|\vec{E}|}\right) \quad (2.28)$$

G^II is the net impact ionization generation rate, $a_{n(p)}$ is the per unit length generation coefficient for electrons (holes), and $b_{n(p)}$ is the electric field at which impact ionization generation becomes significant.

2.2. Numerical Methods for Drift-Diffusion Simulation of SiC MOSFETs

In this section I will describe the numerical methods used for solving the drift diffusion equations for the specific case of a SiC MOSFET device. In order to solve the coupled partial differential equations comprising the drift diffusion system of equations, a proper methodology has to be followed. The equations are solved for 2D structure, which is a section cut parallel to the channel of the MOSFET. These equations are solved for the electrostatic potential (ϕ), the electron concentration (n) and the hole concentration (p) at discrete mesh points inside the device, in the source, drain, bulk and the oxide regions. Appropriate boundary conditions for ϕ , n and p , based on the applied voltages at the various regions, are built in to the system. I will describe the boundary conditions, the meshing scheme, the discretization of the semiconductor equations, and the numerical methods used for solving the discretized system of equations.

2.2.1. Boundary Conditions

The MOSFET device structure is shown in figure 2.1. It is divided into the source, the drain, the bulk, the oxide and the interface regions, where the semiconductor equations are to be solved. The boundary regions are the regions where external voltage is applied or an artificial boundary is created.

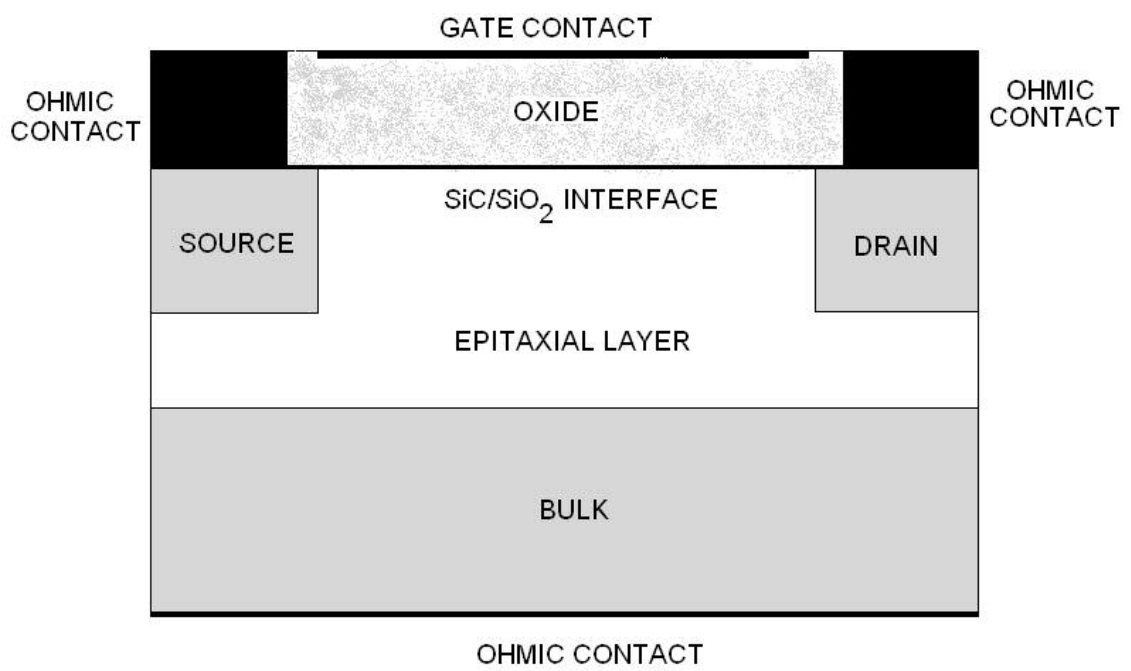


Figure 2.1. 4H-SiC MOSFET device structure

Ohmic Contact

The source, bulk and drain contacts shown in figure 2.1 are modeled as Ohmic contacts. That is, there is no resistance of the contact itself. Hence, all the voltage applied at these contacts is transferred to the semiconductor below. The boundary condition for the electrostatic potential is therefore given by

$$\phi_C = V_C + \phi_n \quad (2.29)$$

for Ohmic contacts on n -type material and

$$\phi_C = V_C + \phi_p \quad (2.30)$$

for Ohmic contact on p -type material.

Here, ϕ_n and ϕ_p are the built in potentials for n -type and p -type semiconductors in thermal equilibrium. For an n -type material with a doping of N_D^+ , the built in potential is simply

$$\phi_n = V_T \ln \frac{N_D^+}{n_i} \quad (2.31)$$

and for a p -type semiconductor doped of N_A^- , the built in potential is

$$\phi_p = -V_T \ln \frac{N_A^-}{n_i} \quad (2.32)$$

where, n_i is the intrinsic carrier concentration at temperature T and V_T is the thermal voltage.

As there is no power loss in the Ohmic contact, and the carriers are at thermal equilibrium, we can say that there exists charge neutrality in the contact volume. Hence, the total charge density is equal to zero.

$$\rho = q(p - n + D) = 0 \quad (2.33)$$

where, $D = N_D^+ - N_A^-$.

Since we are at thermal equilibrium, $np = n_i^2$. Hence, for a n -type semiconductor at the Ohmic contact,

$$p = \frac{n_i^2}{n} \quad (2.34)$$

and

$$n = \frac{D}{2} + \frac{\sqrt{D^2 + 4n_i^2}}{2} \quad (2.35)$$

Similarly, for a p -type semiconductor region at the Ohmic contact,

$$n = \frac{n_i^2}{p} \quad (2.36)$$

and

$$p = \frac{-D}{2} + \frac{\sqrt{D^2 + 4n_i^2}}{2} \quad (2.37)$$

Gate Contact

There are no mobile charge carriers inside the gate oxide. Hence, only the Poisson's equation is solved inside the oxide with the charge density taken as zero. The semiconductor equations are not solved for n and p inside the oxide; hence no boundary conditions are needed for n and p at the gate contact. The boundary condition for the electrostatic potential on the gate contact is defined as

$$\phi_G = V_G + VGB \quad (2.38)$$

V_G is the applied gate voltage and VGB is the built-in gate voltage. It is equal to the metal-semiconductor work function difference between the gate metal and the semiconductor epi-layer of the 4H-SiC MOSFET. The 4H-SiC MOSFET used for measurements has a n -type polysilicon gate doped at 10^{20} cm^{-3} and an p -type epi-layer doped at $5 \times 10^{15} \text{ cm}^{-3}$. Hence, as

shown in Figure 2.2, the work function, which is the difference between the Fermi levels of the polysilicon gate and the 4H-SiC epi-layer, can be written as

$$\begin{aligned}
 E_F^{Si} &= \chi_{Si} + \frac{E_g^{Si}}{2} - \psi_B^{Si} \\
 &= \chi^{Si} + \frac{E_g^{Si}}{2} - k_B T \ln\left(\frac{N_D^{poly}}{n_i^{Si}}\right) \\
 &= 4.06eV
 \end{aligned} \tag{2.39}$$

$$\begin{aligned}
 E_F^{4H-SiC} &= \chi^{4H-SiC} + \frac{E_g^{4H-SiC}}{2} - \psi_B^{4H-SiC} \\
 &= \chi^{4H-SiC} + \frac{E_g^{4H-SiC}}{2} + k_B T \ln\left(\frac{N_A^{epi}}{n_i^{4H-SiC}}\right) \\
 &= 6.97eV
 \end{aligned} \tag{2.40}$$

$$\Phi_{MS} = -q(E_F^{Si} - E_F^{4H-SiC}) = 2.91 \text{ V} = V_{GB} \tag{2.41}$$

Here, $\chi^{Si} = 4.05\text{eV}$, $\chi^{4H-SiC} = 3.95\text{eV}$, $E_g^{Si} = 1.1\text{eV}$, $E_g^{4H-SiC} = 3.26\text{eV}$, $N_D^{poly} = 10^{20}\text{cm}^{-3}$, $N_A^{epi} = 5 \times 10^{15}\text{cm}^{-3}$, $n_i^{Si} = 1.2 \times 10^{10}\text{cm}^{-3}$, $n_i^{4H-SiC} = 1.88 \times 10^{-8}\text{cm}^{-3}$, $T = 300^\circ\text{K}$, $q = 1.6 \times 10^{-19}\text{C}$ and $k_B = 1.38 \times 10^{-23}\text{J}^\circ\text{K}^{-1}$

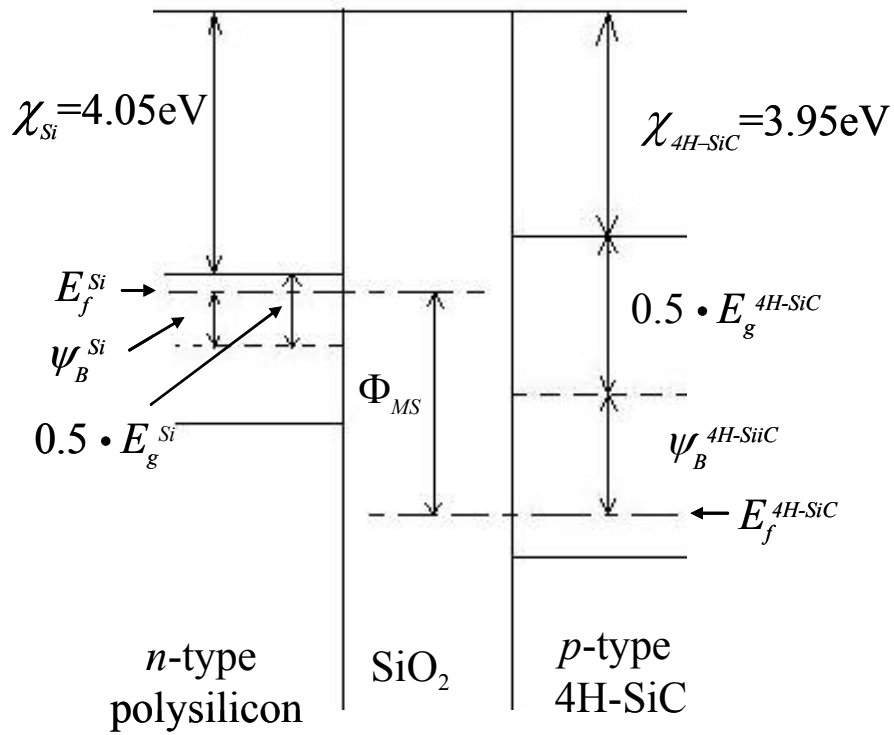


Figure 2.2. Work function difference between *n*-type polysilicon gate and *p*-type epi-layer 4H-SiC MOSFET .

Artificial Boundaries

Artificial boundaries consist of all boundaries in which the device structure ceases to exist for simulation purposes, but in reality, this boundary may not exist on the device physically. The artificial boundaries are placed far enough away from the carrier transport activity where the change in electrostatic potential, electron concentration and hole concentration, across the boundary, is negligible. Hence at the artificial boundaries, we have the conditions

$$\frac{\partial \phi}{\partial N} = \frac{\partial n}{\partial N} = \frac{\partial p}{\partial N} = 0 \quad (2.42)$$

where $\frac{\partial}{\partial N}$ is the derivative taken in the direction normal to the artificial boundary.

2.2.2. Finite Difference Discretization of the Semiconductor Equations

In order to solve the system of coupled differential equations comprising the drift diffusion model, each equation must be discretized in space. In this section I present the discretization scheme for the Poisson's equation and the current continuity equations. The Poisson's equation is solved inside the semiconductor and the oxide, whereas the current continuity equations are solved only inside the semiconductor. At the semiconductor-oxide interface, the Gauss's law is implemented in order to solve for the electrostatic potential.

Each equation is discretized in two dimensions using the finite difference method where each position, (x, y) , in the device is mapped to a mesh point, (i, j) . The position of x , at the i^{th} mesh line is designated by the notation x_i ; likewise, the position of y , at the j^{th} mesh line is designated by the notation y_j . If it is needed, additional points can be defined as lying between two consecutive mesh points. These points are designated by $\left(i \pm \frac{1}{2}, j\right)$ or $\left(i, j \pm \frac{1}{2}\right)$. The distance between two mesh points are designated by the variables h_i and k_j .

$$h_i = x_{i+1} - x_i \quad (2.43)$$

$$k_j = y_{j+1} - y_j \quad (2.44)$$

Other variables will be defined for the purposes of simplifying the writing of the discretized equations.

Poisson's Equation

Poisson's equation gives an analytical representation of the relationship between electrostatic potential (ϕ) and the net charge distribution.

Semiconductor-Insulator Interface

At the semiconductor-oxide interface, it is assumed that there are no free electrons and holes, and that the difference in the electric displacement vectors in the insulator and the semiconductor is equal to the effective surface charge.

$$\hat{a}_{surf} \cdot (\vec{D}_i - \vec{D}_s) = Q_{surf} \quad (2.45)$$

where, \vec{D} is the electric displacement vector and Q_{surf} is the effective surface charge density at the semiconductor-oxide interface, and \hat{a}_{surf} is a unit vector in the direction of the semiconductor-oxide interface.

This equation can be rewritten in form of Gauss's law by writing the electric fields at the semiconductor-oxide interface.

$$\epsilon_{ox} E_{ox} - \epsilon_s E_s = Q_{surf} \quad (2.46)$$

Here, the electric fields are the fields perpendicular to the interface. Writing them using the electrostatic potentials, we have

$$\epsilon_{ox} \left(-\frac{\partial \phi}{\partial y} \right)_{ox} - \epsilon_s \left(-\frac{\partial \phi}{\partial y} \right)_s = Q_{surf} \quad (2.47)$$

Writing the discretized forms of the first order derivatives we have the equation for the electrostatic potential at the interface.

$$F_{i,j_{ox}}^{\phi} = \phi_{i,j_{ox}+1} \left(\frac{\epsilon_s}{k_{j_{ox}}} \right) + \phi_{i,j_{ox}-1} \left(\frac{\epsilon_{ox}}{k_{j_{ox}-1}} \right) - \phi_{i,j_{ox}} \left(\frac{\epsilon_s}{k_{j_{ox}}} + \frac{\epsilon_{ox}}{k_{j_{ox}-1}} \right) + Q_{surf} = 0 \quad (2.48)$$

where, j_{ox} represents the mesh-line j which defines the interface. Q_{surf} is the net effective surface charge at the mesh-point (i, j_{ox}) . It is the sum of the fixed oxide charge and the interface trapped charge at that mesh-point.

Inside the Oxide

There is no charge present inside the oxide. Hence, the Poisson's equation will look like a simple Laplacian.

$$\nabla^2 \phi = 0 \quad (2.49)$$

Finite difference discretization of the above equation has the following form.

$$F_{i,j}^{\phi} = \frac{\phi_{i+1,j}}{h_1^2} + \frac{\phi_{i-1,j}}{h_2^2} + \frac{\phi_{i,j+1}}{k_1^2} + \frac{\phi_{i,j-1}}{k_2^2} - \phi_{i,j} \left(\frac{1}{h_1^2} + \frac{1}{h_2^2} + \frac{1}{k_1^2} + \frac{1}{k_2^2} \right) = 0 \quad (2.50)$$

where,

$$h_1^2 = \frac{h_i(h_i + h_{i-1})}{2}, h_2^2 = \frac{h_{i-1}(h_i + h_{i-1})}{2}, k_1^2 = \frac{k_j(k_j + k_{j-1})}{2}, k_2^2 = \frac{k_{j-1}(k_j + k_{j-1})}{2} \quad (2.51 - 54)$$

Inside the Semiconductor

Rewriting the Poisson's equation inside the semiconductor,

$$\nabla^2 \phi_{i,j} = -\frac{q}{\epsilon_s} \left(-n_{i,j} \exp\left(\frac{\phi_{i,j} - \phi_{n_{i,j}}}{V_{T_{i,j}}} \right) + n_{i,j} \exp\left(-\frac{\phi_{i,j} - \phi_{p_{i,j}}}{V_{T_{i,j}}} \right) + D_{i,j} \right) \quad (2.55)$$

Finite difference discretization of the above equation has the following form.

$$\begin{aligned}
F_{i,j}^\phi = & \frac{\phi_{i+1,j}}{h_1^2} + \frac{\phi_{i-1,j}}{h_2^2} + \frac{\phi_{i,j+1}}{k_1^2} + \frac{\phi_{i,j-1}}{k_2^2} - \phi_{i,j} \left(\frac{1}{h_1^2} + \frac{1}{h_2^2} + \frac{1}{k_1^2} + \frac{1}{k_2^2} \right) \\
& + \frac{q}{\varepsilon_s} \left(-n_{i,j} \exp\left(\frac{\phi_{i,j} - \phi_{n_{i,j}}}{V_{T_{i,j}}}\right) + n_{i,j} \exp\left(-\frac{\phi_{i,j} - \phi_{p_{i,j}}}{V_{T_{i,j}}}\right) + D_{i,j} \right) = 0
\end{aligned} \tag{2.56}$$

Steady State Electron Current Continuity Equations

The steady state electron and hole current continuity equations are solved at all mesh-points inside the semiconductor. They are discretized by the Scharfetter-Gummel scheme. The temperature term in the equation is modeled as a local temperature $T_{i,j}$. If the drift diffusion equations are coupled with the heat flow equation, then we would be able to extract the heat characteristics of the device. But I have not used the heat flow equation in my simulations, so the local temperature is in effect constant, and is equal to the operating temperature of the device.

The Scharfetter-Gummel discretization of the steady state electron current continuity equation is given as

$$\begin{aligned}
F_{i,j}^n = & \beta\left(\alpha_{i+\frac{1}{2}}\right) \frac{\mu_{n_{i+\frac{1}{2},j}} V_{T_{i+1,j}} n_{i+1,j}}{h_1^2} + \beta\left(-\alpha_{i-\frac{1}{2}}\right) \frac{\mu_{n_{i-\frac{1}{2},j}} V_{T_{i-1,j}} n_{i-1,j}}{h_2^2} \\
& + \beta\left(\alpha_{j+\frac{1}{2}}\right) \frac{\mu_{n_{i,j+\frac{1}{2}}} V_{T_{i,j+1}} n_{i,j+1}}{k_1^2} + \beta\left(-\alpha_{j-\frac{1}{2}}\right) \frac{\mu_{n_{i,j-\frac{1}{2}}} V_{T_{i,j-1}} n_{i,j-1}}{k_2^2} - (R_{i,j} - G_{i,j}) \\
& - n_{i,j} V_{T_{i,j}} \left[\beta\left(-\alpha_{i+\frac{1}{2}}\right) \frac{\mu_{n_{i+\frac{1}{2},j}}}{h_1^2} + \beta\left(\alpha_{i-\frac{1}{2}}\right) \frac{\mu_{n_{i-\frac{1}{2},j}}}{h_2^2} + \beta\left(-\alpha_{j+\frac{1}{2}}\right) \frac{\mu_{n_{i,j+\frac{1}{2}}}}{k_1^2} + \beta\left(\alpha_{j-\frac{1}{2}}\right) \frac{\mu_{n_{i,j-\frac{1}{2}}}}{k_2^2} \right] \\
= & 0
\end{aligned} \tag{2.57}$$

$n_{i,j}$ is the electron concentration at mesh-point (i, j) .

$\beta(\gamma)$ is the Bernoulli function defined as

$$\beta(\gamma) = \frac{\gamma}{\exp(\gamma) - 1} \quad (2.58)$$

and,

$$\alpha_{i+\frac{1}{2}} = \frac{\phi_{i+1,j} - \phi_{i,j}}{V_{T_{i,j}}}, \alpha_{i-\frac{1}{2}} = \frac{\phi_{i,j} - \phi_{i-1,j}}{V_{T_{i,j}}}, \alpha_{j+\frac{1}{2}} = \frac{\phi_{i,j+1} - \phi_{i,j}}{V_{T_{i,j}}}, \alpha_{j-\frac{1}{2}} = \frac{\phi_{i,j} - \phi_{i,j-1}}{V_{T_{i,j}}} \quad (2.59 - 52)$$

The mobility terms in the above equation are written as,

$$\mu_{n_{i\pm\frac{1}{2},j}} = \frac{\mu_{n_{xi\pm 1,j}} + \mu_{n_{xi,j}}}{2} \quad \text{and} \quad \mu_{n_{i,j\pm\frac{1}{2}}} = \frac{\mu_{n_{yi,j\pm 1}} + \mu_{n_{yi,j}}}{2} \quad (2.63, 64)$$

Here, $\mu_{n_{xi,j}}$ and $\mu_{n_{yi,j}}$ stand for the x-direction and the y-direction electron mobility respectively,

at mesh-point (i, j)

Steady State Hole Current Continuity Equations

The hole current continuity equation can be discretized the same way as the electron current continuity equation.

$$\begin{aligned} F_{i,j}^p &= \beta\left(-\alpha_{i+\frac{1}{2}}\right) \frac{\mu_{p_{i+\frac{1}{2},j}} V_{T_{i+1,j}} p_{i+1,j}}{h_1^2} + \beta\left(\alpha_{i-\frac{1}{2}}\right) \frac{\mu_{p_{i-\frac{1}{2},j}} V_{T_{i-1,j}} p_{i-1,j}}{h_2^2} \\ &+ \beta\left(-\alpha_{j+\frac{1}{2}}\right) \frac{\mu_{p_{i,j+\frac{1}{2}}} V_{T_{i,j+1}} p_{i,j+1}}{k_1^2} + \beta\left(\alpha_{j-\frac{1}{2}}\right) \frac{\mu_{p_{i,j-\frac{1}{2}}} V_{T_{i,j-1}} p_{i,j-1}}{k_2^2} + (R_{i,j}^p - G_{i,j}) \\ &- p_{i,j} V_{T_{i,j}} \left[\beta\left(\alpha_{i+\frac{1}{2}}\right) \frac{\mu_{p_{i+\frac{1}{2},j}}}{h_1^2} + \beta\left(-\alpha_{i-\frac{1}{2}}\right) \frac{\mu_{p_{i-\frac{1}{2},j}}}{h_2^2} + \beta\left(\alpha_{j+\frac{1}{2}}\right) \frac{\mu_{p_{i,j+\frac{1}{2}}}}{k_1^2} + \beta\left(-\alpha_{j-\frac{1}{2}}\right) \frac{\mu_{p_{i,j-\frac{1}{2}}}}{k_2^2} \right] \\ &= 0 \end{aligned} \quad (2.65)$$

The mobility terms in the above equation are written as,

$$\mu_{p_{i\pm\frac{1}{2},j}} = \frac{\mu_{p_{xi\pm 1,j}} + \mu_{p_{xi,j}}}{2} \quad \text{and} \quad \mu_{p_{i,j\pm\frac{1}{2}}} = \frac{\mu_{p_{yi,j\pm 1}} + \mu_{p_{yi,j}}}{2} \quad (2.66, 67)$$

Here, $\mu_{p_{x_{i,j}}}$ and $\mu_{p_{y_{i,j}}}$ stand for the x-direction and the y-direction hole mobility respectively, at mesh-point (i, j)

2.2.3. Numerical Methods

There are two numerical methods that are used to solve the set of discretized equations shown in the section above. The first method is an iterative Gummel Block method which starts with an initial guess for ϕ , ϕ_n and ϕ_p , at all mesh-points inside the device and solves the three equations consecutively, to get to a solution. This solution acts like the initial guess for the next solver, which is the Newton solver. The Newton solver solves for all three variables ϕ , ϕ_n and ϕ_p at all mesh-points simultaneously, using the Gauss-Newton Algorithm.

Gummel Block Method

The Poisson, electron current continuity, and the hole current continuity equations are solved for the electrostatic potential (ϕ), electron quasi-Fermi level (ϕ_n), and the hole quasi-Fermi level (ϕ_p), respectively, one after the other, using an iterative solver.

First, the discretized Poisson's equation is solved for ϕ at all points in the mesh using an iterative method. In this case, ϕ_n and ϕ_p are kept constant. Next, using the new ϕ calculated over the mesh, the discretized electron current continuity equation is solved for ϕ_n over the mesh. In this case, ϕ and ϕ_p are not allowed to change. Finally, using the new ϕ and ϕ_n values, the hole current continuity equation is solved at all mesh points and the new ϕ_p is obtained.

The discretized finite-difference equations are solved using the iterative Gauss-Seidel method. Here, as an example, I show how the solution for ϕ is obtained iteratively.

The discretized Poisson's equation is arranged in the form shown below

$$f_{\phi}(\phi^k, \phi_n, \phi_p) = 0 \quad (2.68)$$

where, k denotes the current iteration. The solver begins with an initial guess for ϕ at all mesh points in the device.

According to Newton's method for solving nonlinear equations, we can write

$$f_{\phi}(\phi^{k+1}, \phi_n, \phi_p) = f_{\phi}(\phi^k, \phi_n, \phi_p) + \Delta\phi^k \cdot \left(\frac{\partial f_{\phi}}{\partial \phi} \right)^k = 0 \quad (2.69)$$

Hence, we have,

$$\Delta\phi^k = \frac{-(f_{\phi})^k}{\left(\frac{\partial f_{\phi}}{\partial \phi} \right)^k} \quad (2.70)$$

and,

$$\phi^{k+1} = \phi^k + \Delta\phi^k \quad (2.71)$$

Here, $\phi = \phi_{i,j}$ = electrostatic potential at the mesh point (i, j) . The iterations continue till the error $\Delta\phi^k$ falls below a prescribed error criterion.

Once convergence is reached for the electrostatic potential, a similar method is used to solve for the electron quasi-Fermi level (ϕ_n) and then for the hole quasi-Fermi level (ϕ_p). Once we have convergence for all three, we switch to the faster Newton's method.

Newton Method

Unlike the Block Gummel Method, the drift-diffusion equations remain coupled in this method. So ϕ , ϕ_n and ϕ_p are computed simultaneously. This is accomplished by defining a Jacobian matrix and solving for the changes in the three variables between iterations. This process is represented as matrix equation as

$$\begin{bmatrix} \frac{\partial F_{\vec{\phi}}^k}{\partial \vec{\phi}} & \frac{\partial F_{\vec{\phi}}^k}{\partial \vec{\phi}_n} & \frac{\partial F_{\vec{\phi}}^k}{\partial \vec{\phi}_p} \\ \frac{\partial F_{\vec{\phi}_n}^k}{\partial \vec{\phi}} & \frac{\partial F_{\vec{\phi}_n}^k}{\partial \vec{\phi}_n} & \frac{\partial F_{\vec{\phi}_n}^k}{\partial \vec{\phi}_p} \\ \frac{\partial F_{\vec{\phi}_p}^k}{\partial \vec{\phi}} & \frac{\partial F_{\vec{\phi}_p}^k}{\partial \vec{\phi}_n} & \frac{\partial F_{\vec{\phi}_p}^k}{\partial \vec{\phi}_p} \end{bmatrix} \begin{bmatrix} \Delta \vec{\phi}^k \\ \Delta \vec{\phi}_n^k \\ \Delta \vec{\phi}_p^k \end{bmatrix} = - \begin{bmatrix} F_{\vec{\phi}}^k \\ F_{\vec{\phi}_n}^k \\ F_{\vec{\phi}_p}^k \end{bmatrix} \quad (2.72)$$

where, the vectors $\vec{\phi}, \vec{\phi}_n, \vec{\phi}_p$ signify that the matrix operation is performed for all non-boundary mesh points of the variables ϕ, ϕ_n and ϕ_p . Once the above matrix equation is solved, the new values for ϕ, ϕ_n and ϕ_p are obtained as

$$\phi^{k+1} = \phi^k + \Delta \phi^k, \phi_n^{k+1} = \phi_n^k + \Delta \phi_n^k \text{ and } \phi_p^{k+1} = \phi_p^k + \Delta \phi_p^k \quad (2.73, 74, 75)$$

$F_{\vec{\phi}}, F_{\vec{\phi}_n}$ and $F_{\vec{\phi}_p}$ are as shown in equations 2.48, 2.50, 2.56, 2.57, and 2.65. The Jacobian matrix is made up of the derivatives of these functions with respect to ϕ, ϕ_n and ϕ_p .

The Newton solver is allowed to iterate till it reaches the specified convergence condition for all three variables. Then the current is calculated inside the channel, at the drain contact, at the source contact and at the substrate contact. If the current is continuous across the device, then the simulation is proper and all relevant data is stored in various files. A simple flowchart for the simulator is shown in Figure 2.3.

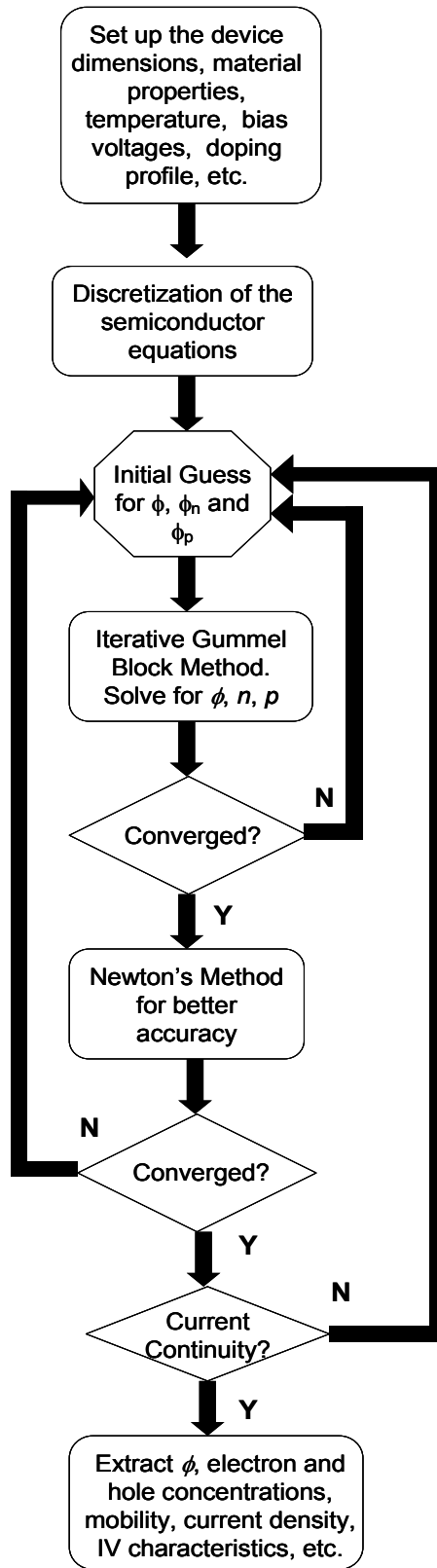


Figure 2.3. Flowchart for solving the drift-diffusion semiconductor equation system

2.2.4. 2D Mesh

A 2D non-uniform mesh has been created for discretizing the drift-diffusion equations for the MOSFET structure. The mesh is very fine near the drain and the source junctions where there is rapid change in potential and charge concentration. Whereas, near the center of the device, the mesh is coarse as there is not much variation in these physical quantities there. In order to capture the physics of the inversion layer, the mesh is kept very fine near the interface. The mesh spacing is kept as low as 2\AA near the interface. This has enabled me to extract detailed physics of the inversion layer. For example, mobility variations as a function of depth near the interface, or the current density variation as a function of depth in a 4H-SiC MOSFET. The mesh is carefully crafted so that the electrostatic potential does not vary by more than then thermal voltage within adjacent mesh points.

CHAPTER 3

3. Coulomb Scattering Mobility Model

In this chapter I describe in new Coulomb scattering mobility model in detail. I first talk about the need for a robust mobility model for Coulombic scattering of inversion layer electrons due to the trapped charges at the interface and the fixed charges in the oxide. Then, I describe the derivation of the Coulomb scattering rate and the Coulomb mobility from basic first principles physics. At the end I present my observations on this mobility model, and how well it reflects the various physical phenomena occurring in the inversion layer of a 4H-SiC MOSFET.

3.1. Need for a Robust Coulomb Scattering Mobility Model for 4H-SiC MOSFETs

Coulomb scattering of inversion layer mobile charges takes place due to the presence of occupied interface traps and fixed oxide charges at the SiC-SiO₂ interface. The Coulomb potential due to these trapped charges and oxide charges decreases with distance. Hence, mobile charges located close the interface experience more scattering as compared to the ones located away from the interface. Hence, a Coulomb scattering mobility model for the mobile charges needs to have a dependence on the distance between the mobile charge and the scattering charge center. Further,

the Coulomb potential is screened by the mobile charges. Hence the Coulomb mobility should also include the effect due to screening. As the density of trapped charge is very high for SiC MOSFETs, Coulomb scattering is an important phenomenon limiting the conductivity mobility in the inversion layer. All these factors prompted me to develop a quasi 2D Coulomb scattering mobility model which takes into account the effect of scattering due to interface trapped charges and fixed oxide charges, distribution of the fixed charges inside the oxide, distribution of mobile charges inside the inversion layer, and screening of the scattering charges by inversion layer mobile charges. The Coulomb mobility is also temperature dependent, because the density of occupied traps decreases with temperature and the effect of screening reduces with temperature.

Mobility models for Coulomb scattering of electrons by impurities in the semiconductor have been described in literature [16][18]. The impurities are distributed in the inversion layer and so the Coulomb scattering is three dimensional in nature. This model is not applicable to 4H SiC MOSFETs because all the scattering charges are located at the interface or some distance inside the oxide, while all mobile charges are located below the interface. Brooks-Herring model described Coulomb scattering for a 3D electron gas. 2D scattering by a Coulomb potential has been described by *Ando et al.* [19]. The authors have assumed the inversion layer to be a sheet of charge and an average mobility is calculated. *Sah et al.* [20] have described 2D Coulomb scattering of electrons by surface oxide charges. They have included the effect of electrons being distributed in the inversion layer and also of distribution of fixed charges inside the oxide [21]. But their mobility model does not have an explicit z -dependence that can be incorporated in a 2D device simulator. They assume various distribution functions for inversion layer electrons and scattering charges and calculate an average mobility based on that. *Gamiz et al.* [22] have described a very complex 2D Coulomb scattering model which is not suitable for inclusion in a drift diffusion device simulator. My mobility model does not require any specific distribution function for electrons in the inversion layer, or any distribution function for fixed charges inside

the oxide. It directly uses fixed charge densities at specific depths inside the oxide and the calculated electron concentration at various depths inside the semiconductor to calculate the scattering rate. Hence, it is easily incorporated in a 2D device simulator.

3.2. Deriving the quasi 2D Coulomb Scattering Rate Equation

The following assumptions are made about the distribution of the charged impurities causing Coulomb scattering of mobile carriers.

The charged impurities are of two types, fixed oxide charges and interface trapped charges. All these charges are located at the interface or inside the oxide. The positions of the scattering charge centers at the interface and inside the oxide are given by z_i , while the positions (depth) of the mobile carriers inside the semiconductor are given as z . $z = z_i = 0$ at the interface. I will be deriving the scattering model for electrons as the mobile carriers. Hence, from now on, electrons are taken as the mobile charges in the inversion layer.

We start with a 3D screened Coulomb potential [18]:

$$V(\vec{r}) = \frac{e^2}{4\pi\bar{\epsilon}} \cdot \frac{1}{r} \cdot e^{-q_{sc}r} \quad (3.1)$$

Here, $\bar{\epsilon}$ is the average permittivity given as [19]

$$\bar{\epsilon} = \frac{\epsilon_{ox} + \epsilon_{SiC}}{2} \quad (3.2)$$

And the screening wave vector q_{sc} is given as the inverse of the Debye length for semiconductors

$$q_{sc} = \sqrt{\frac{e^2 N_{inv}}{\epsilon_{SiC} Z_{av} k_B T_e}} \quad (3.3)$$

Here, N_{inv} is the average 2D inversion charge density at any point along the channel of the MOSFET. I calculate this 2D inversion charge density by integrating the 3D electron concentration over the depth inside the semiconductor. I obtain the electron concentration at each mesh point inside the device by solving the semiconductor equations described in Chapter 2.

Hence, the 2D inversion charge density is calculated by integrating these discrete electron concentration values numerically.

$$N_{inv} = \int_{z=0}^{z=\infty} n(z) dz \quad (3.4)$$

Also, Z_{avg} is the average depth of the inversion layer at any point along the channel of the MOSFET. It is evaluated by integrating the product of the depth and the 3D electron concentration and dividing it by the inversion charge density.

$$Z_{avg} = \frac{\int_{z=0}^{z=\infty} z \cdot n(z) \cdot dz}{\int_{z=0}^{z=\infty} n(z) \cdot dz} \quad (3.5)$$

In order to obtain the scattering rate, I need to formulate the perturbation factor (the screened Coulomb potential) into the Fermi Golden Rule. The Fermi Golden Rule gives the transition rate ($\Gamma_{\vec{k} \rightarrow \vec{k}'}$) for a scattering mechanism as

$$\Gamma_{\vec{k} \rightarrow \vec{k}'} = \frac{2\pi}{\hbar} |H|^2 \delta(E_{\vec{k}} - E_{\vec{k}'}) \quad (3.6)$$

Where, $E_{\vec{k}}$ and $E_{\vec{k}'}$ represent the energy of the mobile charge at the initial and final states \vec{k} and \vec{k}' .

The matrix element in Fermi's Golden rule can be written for the 3D Coulomb scattering case as

$$H_{3D} = \left\langle e^{-i\vec{k}_{3D} \cdot \vec{r}} \mid V(\vec{r}) \mid e^{i\vec{k}'_{3D} \cdot \vec{r}} \right\rangle = \int_{\vec{r}} V(\vec{r}) \cdot e^{i\vec{q}_{3D} \cdot \vec{r}} d\vec{r} \quad (3.7)$$

where $\vec{q}_{3D} = \vec{k}'_{3D} - \vec{k}_{3D}$. This looks like a 3D Fourier transform. Substituting for $V(\vec{r})$ from equation (3.1), we can write the integration using spherical co-ordinates as

$$H_{3D} = \frac{e^2}{4\pi\bar{\epsilon}} \int_{r=0}^{\infty} \frac{1}{r} e^{-q_{sc}r} r^2 dr \int_{\phi=0}^{2\pi} d\phi \int_{\theta=0}^{\pi} e^{iq_{3D}r\cos\theta} \sin\theta d\theta \quad (3.8)$$

Using change of variable $t = \cos\theta$

$$H_{3D} = \frac{e^2}{2\bar{\epsilon}} \int_{r=0}^{\infty} r e^{-q_{sc}r} dr \int_{t=-1}^1 e^{iq_{3D}rt} dt \quad (3.9)$$

$$H_{3D} = \frac{e^2}{2\bar{\epsilon}} \int_{r=0}^{\infty} r e^{-q_{sc}r} dr \left(\frac{e^{iq_{3D}r} - e^{-iq_{3D}r}}{iq_{3D}r} \right) \quad (3.10)$$

$$H_{3D} = \frac{e^2}{\bar{\epsilon}} \int_{r=0}^{\infty} e^{-q_{sc}r} \sin(q_{3D}r) dr \quad (3.11)$$

$$H_{3D} = \frac{e^2}{\bar{\epsilon}} \left[\frac{e^{-q_{sc}r}}{q_{sc}^2 + q_{3D}^2} [-q_{sc} \sin(q_{3D}r) - q_{3D} \cos(q_{3D}r)] \right]_0^{\infty} \quad (3.12)$$

On applying the limits we get,

$$H_{3D} = \frac{e^2}{\bar{\epsilon}} \frac{1}{q_{sc}^2 + q_{3D}^2} \quad (3.13)$$

This is the matrix element for the case of 3D Coulombic scattering. I am going to treat the Coulomb Scattering of inversion layer charges as a quasi 2D scattering phenomenon. As all the scattering charges are located at the interface or inside the oxide, and the mobile carriers being scattered are located at different depths in the inversion layer, the Coulomb scattering potential seen by the mobile charges depends upon the distance between them and the scattering charges. Hence the inversion charges located at different distances from the interface are scattered at different rates. For writing the scattering equations for a quasi 2D scattering phenomenon, I need to find the quasi 2D scattering matrix element H_{2D} . I assume that the scattering takes place in the X-Y plane, and is different for charges located at different positions in the z direction.

Hence, by taking the Inverse Fourier Transform of the 3D matrix element along the q_z direction, I will get the matrix element for a quasi 2D scattering phenomenon.

I first split the 3D scattering wave vector in to a 2D component and a z -component. The 3D scattering wave vector is written as

$$q_{3D} = \sqrt{q_{2D}^2 + q_z^2} \quad (3.14)$$

Taking \vec{q}_z in the direction of z , I can write the 2D matrix element by taking the Inverse Fourier Transform as

$$H_{2D} = \frac{1}{2\pi} \int_{-\infty}^{\infty} H_{3D} \cdot e^{iq_z z} dq_z \quad (3.15)$$

$$H_{2D} = \frac{1}{2\pi} \int_{-\infty}^{\infty} \frac{e^2}{\bar{\epsilon}} \cdot \frac{1}{q_{2D}^2 + q_z^2 + q_{sc}^2} \cdot e^{iq_z z} dq_z \quad (3.16)$$

$$H_{2D} = \frac{e^2}{2\pi\bar{\epsilon}} \int_{-\infty}^{\infty} \frac{e^{iq_z z}}{\left(q_z + i\sqrt{q_{2D}^2 + q_{sc}^2} \right) \left(q_z - i\sqrt{q_{2D}^2 + q_{sc}^2} \right)} dq_z \quad (3.17)$$

I solve this complex integral using the Residue method by considering the complex contours c_1 and c_2 shown in Figure 3.1. The complex integral can be solved as

$$H_{2D} = \frac{e^2}{2\pi\bar{\epsilon}} \cdot 2\pi i \operatorname{Res} \left\{ \frac{e^{iq_z z}}{q_z + i\sqrt{q_{2D}^2 + q_{sc}^2}} \right\} \Big|_{q_z = i\sqrt{q_{2D}^2 + q_{sc}^2}} \quad (3.18)$$

$$H_{2D} = \frac{e^2}{2\pi\bar{\epsilon}} \cdot 2\pi i \cdot \frac{\exp\left(-\sqrt{q_{2D}^2 + q_{sc}^2} \cdot z\right)}{2i\sqrt{q_{2D}^2 + q_{sc}^2}} \quad (3.19)$$

$$H_{2D} = \frac{e^2}{2\bar{\epsilon}} \frac{e^{-\sqrt{q_{2D}^2 + q_{sc}^2} \cdot z}}{\sqrt{q_{2D}^2 + q_{sc}^2}} \quad (3.20)$$

This is the z -dependent quasi-2D scattering matrix element that will be used to calculate the Coulomb scattering rate.

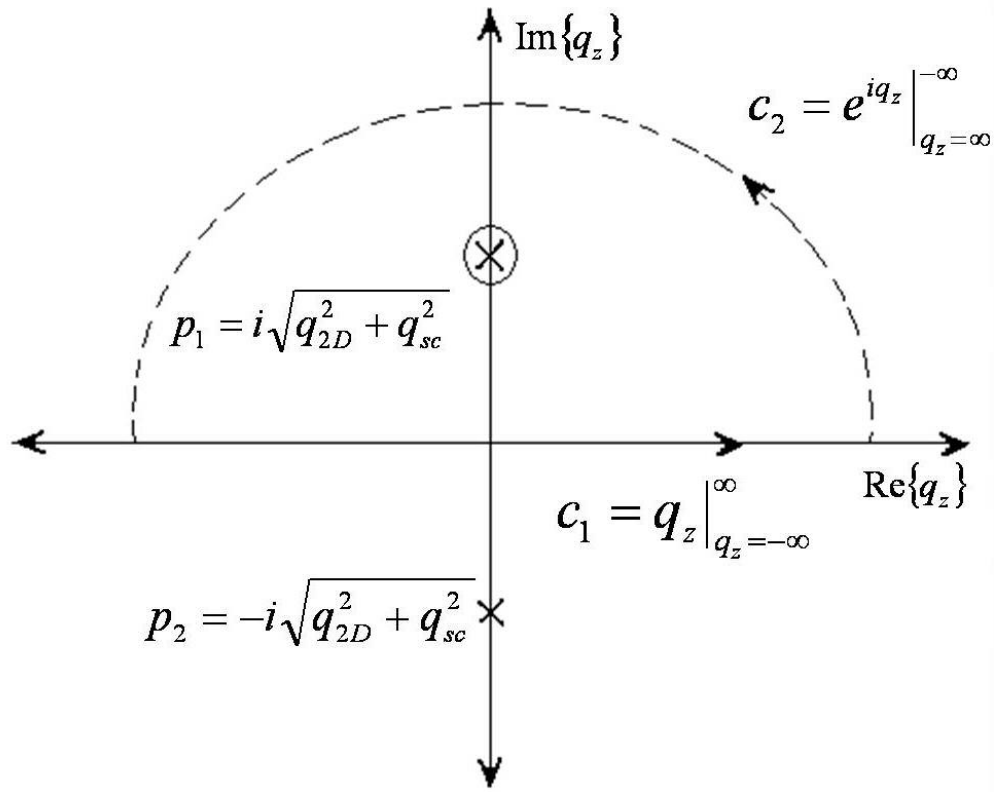


Figure 3.1 Complex poles (p_1 and p_2) of the term inside the integral which gives the quasi-2D matrix element H_{2D} (Equation 3.11). c_1 and c_2 are the complex contours that are used to evaluate the complex integral by the residue method.

Using the matrix element of equation (3.20) and the Fermi Golden Rule given in equation (3.7), the quasi 2D transition rate is given by

$$\Gamma_{\vec{k} \rightarrow \vec{k}'} = \frac{2\pi}{\hbar} |H_{2D}|^2 \delta(E_{\vec{k}} - E_{\vec{k}'}) = \frac{2\pi}{\hbar} \frac{e^4}{4\bar{\epsilon}^2} \frac{e^{-2\sqrt{q_{2D}^2 + q_{sc}^2} \cdot z}}{q_{2D}^2 + q_{sc}^2} \delta(E_{\vec{k}} - E_{\vec{k}'}) \quad (3.21)$$

Here \vec{k} and \vec{k}' are 2D wave-vectors representing the momentum of the mobile carrier before and after the scattering event. $E_{\vec{k}}$ and $E_{\vec{k}'}$ represent the energies of the mobile carrier before and after the scattering event.

The scattering charges are assumed to be distributed at the interface and inside the oxide with a 2D density given by $N_{2D}(z_i)$ at depth z_i inside the oxide.

$$N_{2D}(z_i) = \begin{cases} N_{it} + N_f(0) & z_i = 0 \\ N_f(z_i) & z_i < 0 \end{cases} \quad (3.22)$$

where, N_{it} is the interface trap density at the interface and $N_f(z_i)$ is the fixed oxide density at a distance z_i inside the oxide. Hence, the above transition rate equation can be rewritten as

$$\Gamma_{\vec{k} \rightarrow \vec{k}'} = \frac{\pi e^4}{2\hbar \bar{\epsilon}^2} \cdot N_{2D}(z_i) \cdot \frac{e^{-2\sqrt{q_{2D}^2 + q_{sc}^2} (z - z_i)}}{q_{2D}^2 + q_{sc}^2} \cdot \delta(E_{\vec{k}} - E_{\vec{k}'}) \quad (3.23)$$

The next step is to evaluate the relaxation time from the transition rate equation. Coulomb scattering is elastic in nature, and using the Born approximation, the 2D transport relaxation time is given as [19]

$$\frac{1}{\tau(z, z_i, E)} = \frac{1}{4\pi^2} \int_{k'=0}^{\infty} k' dk' \int_{\theta=0}^{\pi} (1 - \cos \theta) d\theta \cdot \Gamma_{\vec{k} \rightarrow \vec{k}'} \quad (3.24)$$

where, τ is the relaxation time for the scattering of a mobile charge located at a depth z inside the semiconductor having the final energy E , caused by Coulombic interaction with a scattering charge located at a depth z_i inside the oxide. θ is the scattering angle and \vec{k}' is the final state of the mobile charge after the scattering event.

Substituting the transition rate from the Fermi Golden rule, I get the Coulomb scattering rate equation as

$$\frac{1}{\tau(z, z_i, E)} = \frac{e^4 N_{2D}(z_i)}{4\pi\hbar\epsilon^2} \cdot \int_{k'} k' dk' \int_{\theta=0}^{\pi} \frac{e^{-2\sqrt{q_{2D}^2 + q_{sc}^2}(z-z_i)}}{q_{2D}^2 + q_{sc}^2} \sin^2\left(\frac{\theta}{2}\right) \delta(E_{\vec{k}} - E_{\vec{k}'}) d\theta \quad (3.25)$$

To get an expression for the Coulomb mobility from the above scattering rate, some algebra is involved. As a first step, the integral over the final wave vector \vec{k}' is reformulated in terms of the 2D scattering wave vector \vec{q}_{2D} .

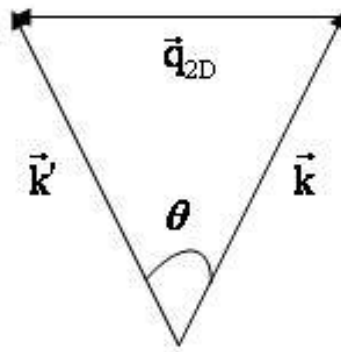


Figure 3.2. The quasi-2D scattering wavevector shown as difference between the final and the initial wavevectors. Coulomb scattering is elastic. Hence, the magnitudes of the final and initial wavevectors remain the same (electron/hole energy does not change). θ is the scattering angle.

As shown in Figure 3.2, the 2D scattering wave vector can be written as

$$\bar{q}_{2D} = \bar{k}' - \bar{k} \Rightarrow q_{2D} = 2k' \sin \frac{\theta}{2} \quad (3.26)$$

Here, q_{2D} represents the magnitude of the vector \bar{q}_{2D} while θ is the scattering angle.

Writing $\alpha = \theta/2$, I can rewrite equation (3.25) as

$$\frac{1}{\tau(z, z_i, E)} = \frac{e^4 N_{2D}(z_i)}{2\pi\hbar\bar{\epsilon}^2} \cdot \int_{k'} k' dk' \int_{\alpha=0}^{\pi/2} \frac{\exp\left(-2\sqrt{4k'^2 \sin^2 \alpha + q_{sc}^2}(z - z_i)\right)}{4k'^2 \sin^2 \alpha + q_{sc}^2} \cdot \sin^2 \alpha \cdot \delta(E_{\bar{k}} - E_{\bar{k}'}) d\alpha \quad (3.27)$$

I then substitute the final wave vector k' by the energy $(E_{\bar{k}'})$, by writing

$$E_{\bar{k}'} = \frac{\hbar^2 k'^2}{2m^*} \quad (3.28)$$

Hence, I can write,

$$dk' = \frac{1}{2} \sqrt{\frac{2m^*}{\hbar^2}} \frac{1}{\sqrt{E_{\bar{k}'}}} dE_{\bar{k}'} \quad (3.29)$$

The scattering rate equation then becomes

$$\frac{1}{\tau} = \frac{e^4 N_{2D}(z_i)}{2\pi\hbar\bar{\epsilon}^2} \cdot \int_{E_{\bar{k}}=0}^{\infty} \frac{m^*}{\hbar^2} \delta(E_{\bar{k}} - E_{\bar{k}'}) dE_{\bar{k}'} \int_{\alpha=0}^{\pi/2} \frac{\exp\left(-2\sqrt{\frac{8m^* E_{\bar{k}'}}{\hbar^2} \sin^2 \alpha + q_{sc}^2}(z - z_i)\right)}{\frac{8m^* E_{\bar{k}'}}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \cdot \sin^2 \alpha d\alpha \quad (3.30)$$

Replacing $E_{\bar{k}'}$ by E , and solving the above integral for dE gives the following energy dependent scattering rate equation.

$$\frac{1}{\tau(z, z_i, E)} = \frac{e^4 N_{2D}(z_i) m^*}{2\pi\bar{\epsilon}^2 \hbar^3} \cdot \int_{\alpha=0}^{\pi/2} \frac{\exp\left[-2\sqrt{\frac{8m^* E}{\hbar^2} \sin^2 \alpha + q_{sc}^2} (z - z_i)\right]}{\frac{8m^* E}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \cdot \sin^2 \alpha \cdot d\alpha \quad (3.31)$$

By a simple algebraic manipulation, the above integral can be rewritten as

$$\frac{1}{\tau(z, z_i, E)} = \frac{e^4 N_{2D}(z_i) m^*}{2\pi\bar{\epsilon}^2 \hbar^3} \cdot \frac{\hbar^2}{8m^* E} \int_{\alpha=0}^{\pi/2} \exp\left(-2\sqrt{\frac{8m^* E}{\hbar^2} \sin^2 \alpha + q_{sc}^2} (z - z_i)\right) \left(1 - \frac{q_{sc}^2}{q_{sc}^2 + \frac{8m^* E}{\hbar^2} \sin^2 \alpha}\right) d\alpha \quad (3.32)$$

The integration in the above term is not solvable analytically. I rewrite the above equation as

$$\frac{1}{\tau(z, z_i, E)} = \frac{e^4 N_{2D}(z_i)}{16\pi\bar{\epsilon}^2 \hbar} \cdot \frac{1}{E} \cdot F(z, z_i, E) \quad (3.33)$$

where, $F(z, z_i, E)$ is the energy dependent form factor given by

$$F(z, z_i, E) = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* E}{\hbar^2} \sin^2 \alpha + q_{sc}^2}\right) \exp\left(-2\sqrt{\frac{8m^* E}{\hbar^2} \sin^2 \alpha + q_{sc}^2} (z - z_i)\right) d\alpha \quad (3.34)$$

3.3. Depth Dependent Coulomb Scattering Mobility Equation

The scattering rate equation given in (3.33) is energy dependent. The average scattering rate $\left\langle\left\langle\frac{1}{\tau}\right\rangle\right\rangle$ is calculated using by approximating the average energy as $E = k_B T_e$ because I have a quasi 2D scattering mechanism. Using this approximation, I can write the average scattering rate as

$$\left\langle\left\langle\frac{1}{\tau}\right\rangle\right\rangle = \frac{e^4 N_{2D}(z_i)}{16\pi\epsilon^2 \hbar} \cdot \frac{1}{k_B T_e} \cdot F(z, z_i, T_e) \quad (3.35)$$

where, T_e is the electron (or hole) temperature, and F is the form factor is given as

$$F(z, z_i, T_e) = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* k_B T_e}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \right) \exp \left[-2 \sqrt{\frac{8m^* k_B T_e}{\hbar^2} \sin^2 \alpha + q_{sc}^2} (z - z_i) \right] d\alpha \quad (3.36)$$

The Coulomb mobility for a carrier at position z inside the semiconductor due to scattering by Coulombic interaction with scattering charges located at z_i inside the oxide is then given by

$$\frac{1}{\mu_C(z, z_i, T_e)} = \frac{m^*}{e} \left\langle\left\langle\frac{1}{\tau}\right\rangle\right\rangle = \frac{m^* e^3 N_{2D}(z_i)}{16\pi\epsilon^2 \hbar k_B T_e} \cdot F(z, z_i, T_e) \quad (3.37)$$

The total Coulomb mobility for a mobile carrier at a depth z can be obtained by adding up the scattering rates due to scattering charges located at different depths inside the oxide using Matheissen's rule as

$$\frac{1}{\mu_C(z, T_e)} = \sum_{z_i} \frac{1}{\mu_C(z, z_i, T_e)} \quad (3.38)$$

3.4. Physics of the Coulomb Scattering Mobility Model

The Coulomb scattering mobility model developed above incorporates some interesting physics of the inversion layer. The notable points of this model are summarized below.

1. The Coulomb scattering rate is directly proportional to the density of interface trapped charge and fixed oxide charge.
2. Fixed oxide charges located away from the interface into the oxide have less effect on the scattering of inversion layer electrons. This is due to the fact that the Coulombic potential decreases sharply with distance. It has been effectively represented as a component of the form factor (F) in the model presented above.
3. Mobile charges (electrons) located away from the interface and inside the semiconductor are scattered less as compared to those located near the interface. This is also incorporated in the form factor (F) of the model above. Thus, the distribution of electrons inside the inversion layer plays an important role in determining the total mobility, and hence the total current in the device. This distribution is obtained directly from the numerical solution of the semiconductor equations. Hence, I do not need to assume any particular distribution for the mobile charges inside the device. Thus this model is incorporated seamlessly into the drift diffusion device simulation methodology.
4. Physics of screening of the scattering charges by the inversion layer electrons has been included in the mobility model. The model clearly shows that with increase in inversion layer charge, the screening increases, causing the total Coulomb mobility to increase. An interesting thing that I have seen is that screening affects the electrons lying away from the interface more than those lying close to the interface. That is, the Coulomb mobility rises much more sharply away from the interface than close to it when the inversion

charge density is increased. This can be seen in the simulation results shown in Chapter 5. An explanation for this can be obtained by looking at the form factor (F) of the mobility model. The exponential term in the form factor is dependent on the product of the screening wave vector (q_{sc}) and the distance ($z-z_i$). Hence, for very small distances, the product is quite small, making the effective screening less. Whereas at larger distances, the effective screening is much higher.

5. Temperature dependence of Coulomb mobility is obtained implicitly from the model. For SiC MOSFETs, the effect of temperature on mobility is rather complicated. Three different phenomena are temperature dependent, and that too in different ways. The interface trap density (N_{it}) which is a part of the 2D scattering charge density (Equation 3.22) decreases with increase in temperature, thus causing an increase in Coulomb mobility. The screening wave vector (q_{sc}) decreases with increase in temperature (Equation 3.3), thus causing a decrease in Coulomb mobility. Also, the mobility term itself is directly proportional to temperature, causing the mobility to increase with temperature. Thus, a combined effect of these three terms gives the temperature dependence of Coulomb Mobility.
6. In the specific case when it is assumed that the interface trapped charge and the fixed oxide charge is located only at the 4H-SiC/SiO₂ interface, the depth dependent Coulomb mobility may be given as

$$\frac{1}{\mu_c(z, T_e)} = \frac{m^* e^3 (N_f + N_{it})}{16\pi\epsilon^2 \hbar k_B T_e} \cdot F(z, 0, T_e) \quad (3.39)$$

Where,

$$F(z, 0, T_e) = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* k_B T_e}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \right) \exp \left[-2 \left(\sqrt{\frac{8m^* k_B T_e}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \right) z \right] d\alpha \quad (3.40)$$

7. In the classic sheet approximation for the inversion layer, it is assumed that the inversion layer is an infinitesimally thin sheet of charge located at the interface. For this approximation, the Coulomb mobility at the interface can be written as

$$\frac{1}{\mu_C(T_e)} = \frac{m^* e^3 (N_f + N_{it})}{16\pi\epsilon^2 \hbar k_B T_e} \cdot F^{2D} \quad (3.41)$$

8. Where,

$$F^{2D} = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* k_B T_e}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \right) d\alpha \quad (3.42)$$

9. For the unscreened Coulomb scattering case, the depth dependent Coulomb mobility is reduced to

$$\frac{1}{\mu_C(z, z_i, T_e)} = \frac{m^* e^3 N_{2D}(z_i)}{16\pi\epsilon^2 \hbar k_B T_e} \cdot F^{unscreened} \quad (3.43)$$

where,

$$F^{unscreened} = \int_{\alpha=0}^{\pi/2} \exp \left[-2\sqrt{\frac{8m^* k_B T_e}{\hbar^2}} \sin \alpha (z - z_i) \right] d\alpha \quad (3.44)$$

CHAPTER 4

4. Complete Mobility Model and Simulation Technique for 4H-SiC MOSFET

In this chapter I describe the complete mobility model used for simulation of a 4H-SiC MOSFET. In addition to the Coulomb Scattering Mobility model described in the previous chapter, the complete mobility model for 4H-SiC MOSFET includes the bulk mobility model, surface phonon mobility model, surface roughness mobility model and high field mobility model. I will describe each model and then link them together to form the complete model that is implemented in the drift diffusion simulator. In the second part of the chapter I will describe the simulation methodology specific for 4H-SiC MOSFETs. I will talk about the interface trap density model that has been implemented in the simulator and compare it to experimentally observed interface trap density profiles. I will then describe the methodology I have used to extract the fixed oxide charge density from experimental data. I have included a summary at the end of the chapter to summarize all the information provided so far, and to lead on to the results detailed in the next chapter.

4.1. Complete Mobility Model

Mobility of mobile charges in the 4H-SiC MOSFET is limited by several scattering mechanisms. In order to incorporate the physics of these different scattering mechanisms, each scattering mechanism is modeled as a mobility term. All these mobility terms are added using Matheissen's rule to get the total mobility, which is then included in the drift diffusion equations. The mobility behaves differently along different crystal axes. Hence the each mobility term is defined as a vector with x -mobility and y -mobility components. The x -component is the mobility component parallel to the interface direction, whereas the y -component is perpendicular to the interface. The total mobility can be divided in two main groups dependent on the parallel field – the low field mobility (μ_{LF}) and the high field mobility (μ_{HF}). The total low field mobility is made up of bulk mobility (μ_B), surface phonon mobility (μ_{SP}), surface roughness mobility (μ_{SR}) and Coulomb mobility (μ_C) of mobile carriers. The high field mobility is limited by the electron and hole saturation velocity in 4H-SiC inversion layer. By Matheissen's rule, the total mobility can be written as

$$\frac{1}{\mu_T} = \frac{1}{\mu_{LF}} + \frac{1}{\mu_{HF}} = \frac{1}{\mu_B} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} + \frac{1}{\mu_{HF}} \quad (4.1)$$

All the mobilities are derived for electrons. Similar relations can be used for hole mobilities too.

4.1.1. Bulk Mobility

Acoustic phonon scattering and ionized impurity scattering in the bulk are the mechanism limiting bulk mobility of charge carriers [28]. I have used the Caughey - Thomas method for

modeling bulk mobility [29]. The bulk mobility can be represented as being dependent on the doping density and temperature according to the following relation.

$$\mu_B = \frac{\mu_{\max} \left(\frac{300}{T} \right)^{\eta_B} - \mu_{\min}}{1 + \left(\frac{D}{N_{ref}} \right)^{\gamma_B}} + \mu_{\min} \quad (4.2)$$

The following table gives the values for the temperature dependence parameter (η_B), and doping dependence parameters (N_{ref} and γ_B) [11][23].

Table 4.1. Parameter values used for calculating the bulk mobility in a 4H-SiC MOSFET.

	4H-SiC
μ_{\max} (cm ² /Vs)	1071.0
μ_{\min} (cm ² /Vs)	5.0
η_b	2.4
N_{ref} (cm ⁻³)	1.9×10^{17}
γ_b	0.40

4.1.2. Surface Phonon Mobility

Using Fermi's Golden Rule, the surface acoustic phonon scattering rate can be written as [20]

$$\frac{1}{\tau_{ac}} = \frac{m^* D_{ac}^2 k_B T}{\hbar^3 \rho_s v_s^2} \quad (4.3)$$

where, ρ_s is the areal mass density of 4H-SiC, v_s is the velocity of sound, m^* is the density of states effective mass and D_{ac} is the acoustic phonon deformation potential for 4H-SiC. Values of D_{ac} reported in literature range from 11 eV to 23.8 eV [10][11][27].

The surface acoustic phonon mobility can hence be written as

$$\mu_{ac} = \frac{q\tau_{ac}}{m_c} = \frac{q\hbar^3 \rho_s v_s^2}{m^* m_c D_{ac}^2 k_B T} \quad (4.4)$$

where, m_c is the conductivity effective mass of electrons in 4H-SiC.

The areal mass density ρ_s is approximately equal to the product of the bulk mass density and the average channel thickness. Hence, we obtain the following relation for ρ_s .

$$\rho_s = \rho_{bulk} Z_{avg} = \rho_{bulk} (Z_{CL} + Z_{QM}) \quad (4.5)$$

Z_{avg} is the average channel thickness. It can be written as the sum of the classical channel thickness (Z_{CL}) and a small quantum correction (Z_{QM}). The classical channel thickness and the quantum correction are given by

$$Z_{CL} = \frac{3 k_B T}{2 q E_{\perp}} \quad (4.6)$$

and,

$$Z_{QM} = \left(\frac{9\hbar^2}{4q m_{\perp} E_{\perp}} \right)^{1/3} \quad (4.7)$$

Here, E_{\perp} represents the component of the electric field perpendicular to the mobility component.

Hence for x -mobility, E_{\perp} is the field perpendicular to the interface, while for y -mobility, it is the field parallel to the interface. m_{\perp} is the perpendicular effective mass for electrons in 4H-SiC.

Writing the complete form of the surface phonon mobility, we have

$$\mu_{ac} = \frac{q\hbar^3 \rho_{bulk} v_s^2}{m^* m_c D_{ac}^2 k_B T} \left(\frac{3 k_B T}{2 q E_{\perp}} + \left(\frac{9\hbar^2}{4q m_{\perp} E_{\perp}} \right)^{1/3} \right) \quad (4.8)$$

The above equation can be reformulated as

$$\mu_{ac} = \frac{A}{E_{\perp}} + \frac{B}{TE_{\perp}^{1/3}} \quad (4.9)$$

A and B are parameters having the following forms.

$$A = \frac{3 \hbar^3 \rho_{bulk} v_s^2}{2 m^* m_c D_{ac}^2} \quad (4.10)$$

$$B = \frac{q \hbar^3 \rho_{bulk} v_s^2}{m^* m_c D_{ac}^2 k_B} * \left(\frac{9 \hbar^2}{4 q m_{\perp}} \right)^{1/3} \quad (4.11)$$

m^* is the 2D density of states effective mass, m_c is the conductivity effective mass and m_{\perp} is the perpendicular effective mass. They can be derived from the longitudinal (m_1 , m_2) and transverse (m_3) effective masses for the lower band of 4H SiC [25].

$$m^* = \sqrt{m_1 m_2} = m_{\perp} \quad (4.12)$$

$$\frac{1}{m_c} = \frac{1}{2} \left(\frac{1}{m_1} + \frac{1}{m_2} \right) \quad (4.13)$$

The measured and calculated values of the parameters defining the surface acoustic phonon mobility in 4H-SiC MOSFETs are given in Table 4.2. The surface acoustic phonon mobility reduces with increase in perpendicular field. Hence, it has more effect at higher gate voltages. Also, with increase in temperature, phonon vibrations increase, causing increased phonon scattering of mobile charges. Hence, the surface acoustic phonon mobility decreases with increase in temperature.

Table 4.2. Parameter values for calculating surface phonon mobility in 4H-SiC MOSFETs.

	4H-SiC
ρ_{bulk} (g/cm ³)	3.2
vs (cm/s)	1.37×10^6
D_{ac} (eV)	20
m_1, m_2, m_3 (for electrons)	0.29, 0.58, 0.33
m^*, m_c, m_{\perp} (for electrons)	0.41, 0.39, 0.41
A (cm/s)	7.8243×10^7
B ((V/cm) ^{-2/3} •°K•cm/s)	9.9240×10^6

4.1.3. Surface Roughness Mobility

Surface roughness scattering is dependent on the quality of the semiconductor-insulator interface. At low temperature and high perpendicular electric field, surface roughness scattering is known to strongly degrade surface mobility [28]. It is described as varying inversely with the square of the surface charge density [30][31]. The surface roughness scattering rate can be written as –

$$\frac{1}{\mu_{SR}} = \frac{m_{\parallel}}{q} \frac{\Delta^2 L^2}{h^3} \left(\frac{q^2}{\epsilon_s} \right)^2 (n_s + N_{dr})^2 f_{SR} \quad (4.14)$$

where, m_{\parallel} is the effective mass parallel to the surface, Δ is the root mean square deviation of the roughness, L is the correlation length of the roughness, n_s is the surface carrier concentration, N_{dr} is the depletion region areal charge, and f_{SR} is given by

$$f_{SR} = \int d\theta (1 - \cos \theta) \exp\left[-(1 - \cos \theta) k_F^2 L^2 / 2\right] \quad (4.15)$$

Using Gauss's law to relate the surface charge ($n_s + N_{dr}$) to the normal electric field,

$$n_s + N_{dr} = \frac{E_{\perp} \epsilon_s}{q} \quad (4.16)$$

the surface roughness mobility can be written as -

$$\mu_{SR} = \frac{\Gamma_{SR}}{E_{\perp}^2} \quad (4.17)$$

Simulations show that surface roughness scattering becomes important at high gate voltages. I have used a value of around 3.7×10^{12} V/s for Γ_{SR} . This is much lower than the values used for Si MOSFETs ($> 10^{14}$ V/s). It suggests that 4H-SiC MOSFETs have a much rougher surface than Si MOSFETs. Better fabrication technique would make the surface much smoother giving reduction in surface roughness scattering.

4.1.4. Coulomb Scattering Mobility

The development of the Coulomb Scattering Mobility model for 4H-SiC MOSFETs has been described in Chapter 3. I would just like to note here that the Coulomb Scattering mobility is inversely proportional to the density of occupied traps and the fixed oxide charge at the interface. I would also like to note that the Coulomb scattering mobility rises sharply with increasing distance from the interface, and that up till a certain high temperature, it rises with rise in temperature.

4.1.5. High Field Mobility

The effect of high lateral field on the scattering of charged carriers in the inversion layer is modeled by considering a high field mobility component. At high lateral fields, the velocity of the charged carriers in the inversion layer approaches the saturation velocity (v_{sat}). Hence, it

becomes independent of the lateral field. Considering this, the high field mobility can be expressed as [15]

$$\mu_{HF} = \frac{v_{sat}}{E_{\parallel}} \quad (4.18)$$

The saturation velocity depends on various parameters. Essentially, it can be thought as the maximum velocity a mobile carrier can reach in the inversion layer. As the carriers are accelerated by the lateral field, they gain energy. But due to scattering in the inversion layer near the interface, their energy cannot exceed beyond a certain limit. Hence, their maximum velocities are limited by the amount of scattering they experience. So, the saturation velocity of carriers near the interface will be different from those away from the interface, as the amount of scattering is different in both cases. The variation of saturation velocity with depth can be extracted by Monte Carlo simulations of a mobile charge traveling inside the semiconductor at different depths from the interface. I have not yet done this. I use an average saturation velocity for all carriers. This saturation velocity though is allowed to change with change in gate voltage, because scattering rates change with change in gate voltage. But this method is not without its own drawbacks. With increase in gate voltage, up to a certain point, the total scattering increases. Hence, the average saturation velocity should decrease. But after a certain gate voltage, screening of the occupied interface traps causes a drop in the amount of Coulomb scattering taking place. Hence, the saturation velocity at the interface should increase. But at the same time, with increase in gate voltage, perpendicular electric field increases, leading to increase in surface acoustic phonon scattering and surface roughness scattering. These mechanisms will try to reduce the saturation velocity. I have not yet come up with a model that takes into effect all these mechanisms and calculate the proper average saturation velocity as a function of gate voltage. I have used different values of the average saturation velocity which would give me proper IV characteristics at high fields (high drain voltages), that fit the experimentally measured values.

4.1.6. Total Mobility

The complete mobility of charged carriers inside the semiconductor is given by adding up the effects of low field and high field scattering mechanisms by Matheissen's rule. This total mobility is directly incorporated in the device simulator as part of the electron and hole current continuity equations. The mobility model is temperature dependent. Temperature dependence is evident in the models for bulk mobility, surface acoustic phonon mobility and the Coulomb scattering mobility. It is seen that for 4H-SiC MOSFETs, at low gate fields, the total surface mobility increases with increase in temperature. This is due to the fact that the dominant mobility at low gate fields, which is the Coulomb Scattering mobility, shows an increase with increase in temperature.

4.2. Simulation Technique and Application to 4H-SiC MOSFETs

In this section, I will discuss two aspects related to simulation of 4H-SiC MOSFET devices. First, I will present a strategy to evaluate the occupied interface trapped charge at the SiC-SiO₂ interface from an energy dependent model for the density of states of interface traps. I will then talk about how I identify and include another very important parameter for 4H-SiC MOSFETs – the fixed oxide charge density.

4.2.1. Interface Trap Model

Experimental measurements of interface trap density of states for 4H SiC have shown a flat distribution of traps in the middle of the bandgap and an exponential increase near the band edges [5][6][32][33][34]. I use a similar distribution function for the interface trap density of

states for 4H-SiC MOSFETs. I extract the values for midgap and band-edge values of the density of states by comparing simulated IV curves to experimental data.

For the traps lying in the upper half of the bandgap, the density of states can be described as –

$$D_{it}^A(E) = D_{it_{mid}} + D_{it_{edge}} \exp\left(-\frac{E_C - E}{\sigma_{it}}\right) \quad (4.19)$$

where, E_C is the energy at the conduction band edge. Similarly, for the traps lying in the bottom half of the bandgap, the energy dependent density of states can be written as –

$$D_{it}^D(E) = D_{it_{mid}} + D_{it_{edge}} \exp\left(\frac{E_V - E}{\sigma_{it}}\right) \quad (4.20)$$

where, E_V represents the energy at the valence band edge.

$D_{it_{mid}}$ and $D_{it_{edge}}$ are empirical quantities that are determined by comparing the simulated IV curves to experimental data. Some restrictions have been imposed on the values for these quantities. The value for $D_{it_{mid}}$ is not allowed to be less than the minimum mid-gap density of states values reported in literature, and $D_{it_{edge}}$ is not allowed to exceed the maximum reported band-edge density of states values.

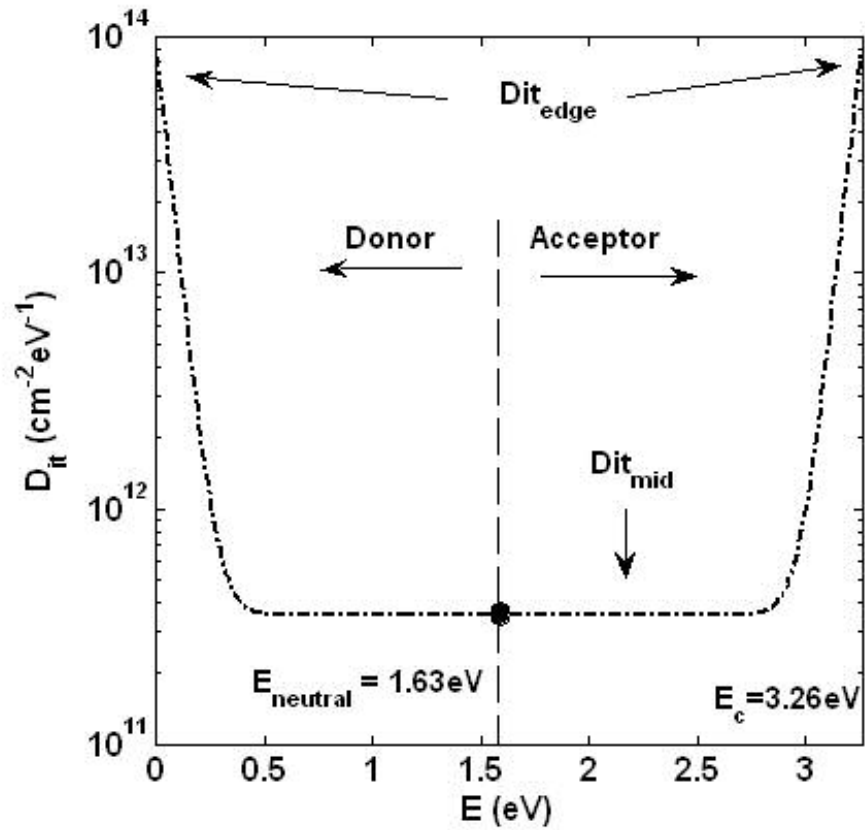


Figure 4.1. Interface trap density of states for 4H-SiC MOSFET. $D_{it_{\text{edge}}} = 9.5 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$
 $D_{it_{\text{mid}}} = 4.0 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ and $\sigma_{it} = 0.0515$

The occupancy of the traps depends on the energy distribution of inversion layer mobile charges. I use Fermi statistics to calculate the density of occupied interface traps. My model uses the mid-gap energy as the neutrality point $\left(E_{neutral} = \frac{(E_C + E_V)}{2}\right)$. Traps above the neutrality point are acceptor-type, while those below the neutrality point are donor-type. Electrons can fill the traps which have energies between the neutrality point (mid-gap) level and the electron Fermi energy level; whereas, holes can fill the traps which have energies between the hole Fermi level and the neutrality point (mid-gap) level. Hence, according to Fermi statistics, I can write the probability function for the occupancy of the traps lying above the mid-gap as –

$$f_n(E) = \frac{1}{1 + \frac{1}{2} \exp\left(\frac{E - E_F^n}{k_B T}\right)} \quad (4.21)$$

Instead of using the Fermi energy (E_F^n), I use the electron concentration at points closest to the interface to write the probability function. Writing the electron concentration (n) in terms of the Fermi energy, I have –

$$n = N_C \exp\left(\frac{E_F^n - E_C}{k_B T}\right) \quad (4.22)$$

Substituting for the electron Fermi energy in (4.21), the probability density function for occupancy of the acceptor-type traps can be written as -

$$f_n(E) = \frac{1}{1 + \frac{1}{2} \frac{N_C}{n} \exp\left(-\frac{E_C - E}{k_B T}\right)} \quad (4.23)$$

where, N_C is the effective conduction band density of states for 4H-SiC, n is the density of electrons close to the interface, and E_C is the conduction band minimum at the temperature T .

Similarly, the probability distribution function for occupancy of donor-type traps can be written as

$$f_n(E) = \frac{1}{1 + \frac{1}{2} \frac{N_V}{p} \exp\left(\frac{E_V - E}{k_B T}\right)} \quad (4.24)$$

where, N_V is the effective valence band density of states for 4H-SiC, p is the density of electrons close to the interface, and E_V is the conduction band minimum at the temperature T .

The density of occupied acceptor-type interface traps is given by

$$N_{it}^A = \int_{E_{neutral}}^{E_c} D_{it}^A(E) f_n(E) dE \quad (4.25)$$

Similarly, the density of occupied donor-type interface traps is calculated as -

$$N_{it}^D = \int_{E_V}^{E_{neutral}} D_{it}^D(E) f_p(E) dE \quad (4.26)$$

The reason for using the electron and hole concentrations to calculate the occupied trap density is that the drift diffusion simulator directly calculates these values. Hence, the dependence of the occupancy of interface traps on the electron and hole concentration in the device is achieved implicitly. With increase in gate voltage, the surface electron concentration increases for n-channel a 4H-SiC MOSFET. Hence, more of the interface traps near the conduction band edge are occupied. Figures 4.2 and 4.3 show the occupancy of the interface traps at two different gate voltages. It can be clearly seen that at higher gate voltage, the probability function describing the occupancy is shifted more towards the conduction band edge.

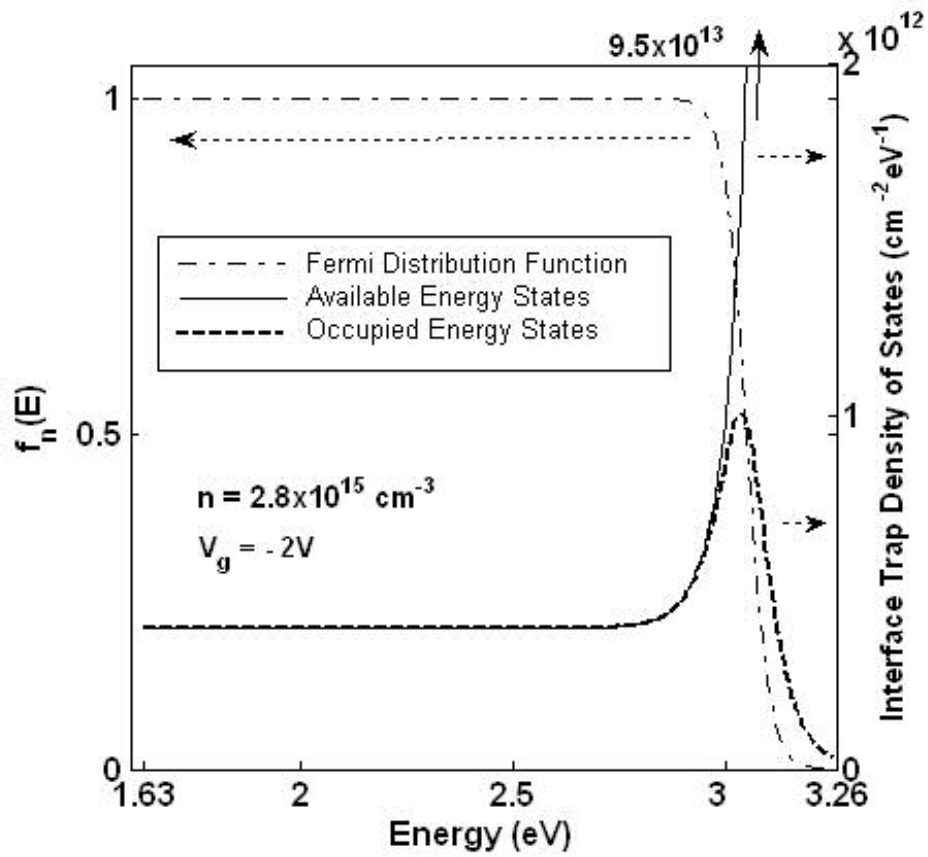


Figure 4.2. Fermi distribution function and the density of occupied acceptor-type interface traps at a low gate voltage of $-2V$. The electron concentration at the surface is quite high, indicating that the electron Fermi level is closer to the conduction band edge. The complete curve for the available energy states is not shown. It actually stretches up till $9.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ as shown in Figure 4.1. $D_{it_{edge}} = 9.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ $D_{it_{mid}} = 4.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ and $\sigma_{it} = 0.0515$

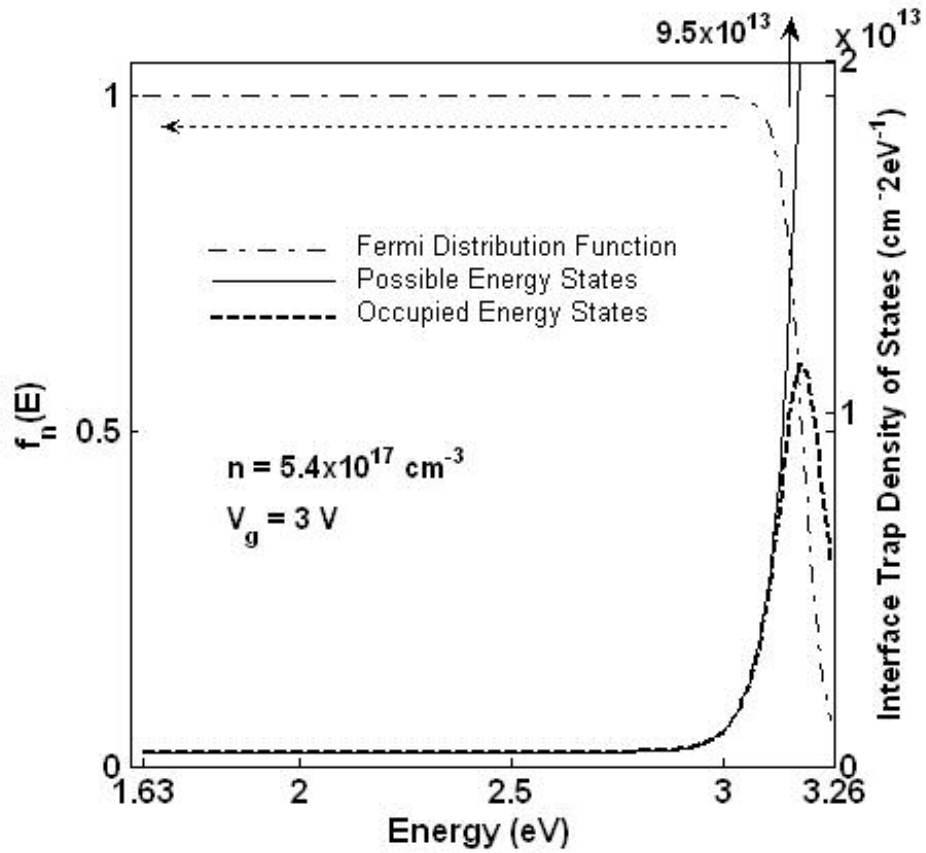


Figure 4.3. Fermi distribution function and the density of occupied acceptor-type interface traps at a gate voltage of 2V. The electron concentration at the surface very high, indicating that the electron Fermi level is closer to the conduction band edge. Compare the Fermi distribution function curve to the one in Figure 4.2. It is clear that the curve has shifted towards the conduction band edge, indicating that the electron Fermi energy level has shifted towards the conduction band edge. The complete curve for the available energy states is not shown. It actually stretches up till $9.5 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ as shown in Figure 4.1. $D_{it_{edge}} = 9.5 \times 10^{13} \text{ cm}^{-2}\text{eV}^{-1}$

$$D_{it_{mid}} = 4.0 \times 10^{11} \text{ cm}^{-2}\text{eV}^{-1} \text{ and } \sigma_{it} = 0.0515$$

Temperature dependence of the occupied interface trap density is also obtained from the probability functions. With increase in temperature, the Fermi distribution function curves shift away from the band edges. So, the traps lying closer to the band edges remain less filled. Hence, the total number of occupied traps decreases. Thus, with increase in temperature, the occupied trap density decreases. Figure 4.4 shows the comparison between the occupied interface trap densities at two different temperatures, and at a particular gate voltage. At lower temperatures, the occupation of traps, which is shown by the dotted line, is more towards the conduction band edge, as compared to the high temperature case.

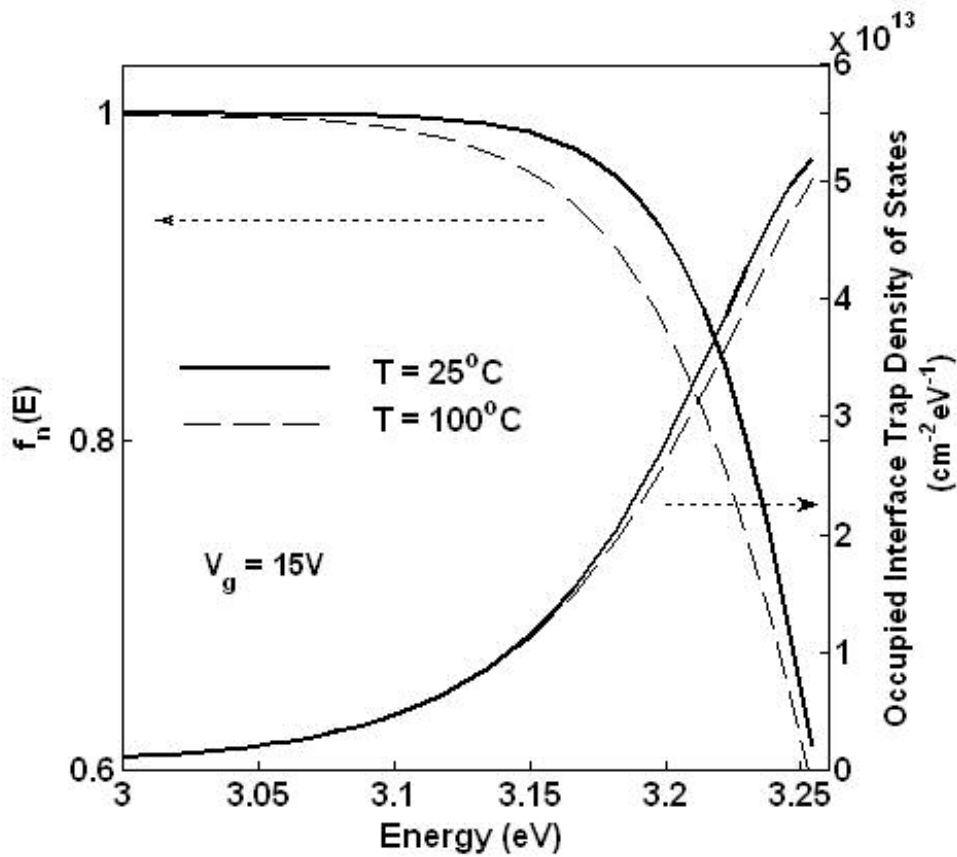


Figure 4.4. Occupation of acceptor-type interface traps by electrons at two different temperatures. As compared to room temperature, at 100°C , the Fermi distribution function curve is shifted away from the conduction band edge. Hence, fewer electrons fill up the interface states, causing the occupied interface trap density to decrease. The available interface traps density of states is not shown in the figure. It is the same as shown in Figure 4.1.

4.2.2. Fixed Oxide Charge Density

Fixed oxide charge density in a MOSFET can be estimated from threshold voltage variation with temperature. Threshold voltage in a MOSFET is dependent on the gate-semiconductor work function difference, the bulk built in potential, the depletion charge density, the interface trapped charge density, the inversion layer charge density, and the fixed oxide charge density. All the above mentioned quantities, except for the fixed oxide charge density, change with change in temperature. Using experimentally measured threshold voltages at different temperatures, it is possible to extract the fixed charge for a given MOSFET. It is seen in simulations (Figure 5.5) and experiments [4] that the inversion charge is very small at threshold. Hence, assuming that there is no inversion charge at threshold and that the band bending at the surface is twice the bulk built-in potential, I can write the equation for temperature dependent threshold voltage as

$$V_t(T) = \Phi_{MS}(T) + 2\psi_B(T) + \frac{\sqrt{2qN_A^-(2\psi_B(T))}}{C_{ox}} + \frac{q}{C_{ox}}(N_{it}(T) - N_f) \quad (4.27)$$

Φ_{MS} is the work function difference between the polysilicon gate and 4H-SiC substrate, ψ_B is the bulk built in potential, N_A^- is the bulk doping density, C_{ox} is the oxide capacitance, N_{it} is the temperature dependent occupied interface trap density at threshold and N_f is the fixed oxide charge density.

I define a theoretical threshold voltage (V_{tTHEO}) as the threshold voltage calculated by excluding the effect of fixed charge and occupied interface trap charge.

$$V_{tTHEO}(T) = \Phi_{MS}(T) + 2\psi_B(T) + \frac{\sqrt{2qN_A^-(2\psi_B(T))}}{C_{ox}} \quad (4.28)$$

The values for the theoretical threshold voltage are calculated, whereas, the values for the actual threshold voltage are taken from experiments. I have used experimental data from measurements done at the Army Research Lab (ARL), on a $200\mu\text{m}\times 200\mu\text{m}$ 4H-SiC MOSFET manufactured by Cree. Inc. The oxide thickness and the doping density values have been provided by Cree and are as listed in Table 4.1. Based on these values, the bulk built-in potential, and the depletion charge densities calculated at threshold, are also listed in Table 4.1. Figure 4.3 shows the measured threshold voltage and the theoretical threshold voltage as function of temperature.

Comparing the two equations for temperature dependent threshold voltage, I can write the difference between the fixed charge and temperature dependent occupied trap density as

$$N_f - N_{it}(T) = \frac{C_{ox}}{q} (V_{t_{theo}}(T) - V_t(T)) \quad (4.29)$$

As discussed in the previous section, N_{it} decreases with increase in temperature while N_f remains constant. Plotting $N_f - N_{it}(T)$ as a function of temperature (Fig. 4.4), we can estimate the value of N_f as the maximum of the curve (where N_{it} is the minimum). The estimated value of N_f was $1.54 \times 10^{12} \text{ cm}^{-2}$. Actually, at threshold, there is going to be some inversion layer charge also. Hence N_f will be a little larger than the calculated value.

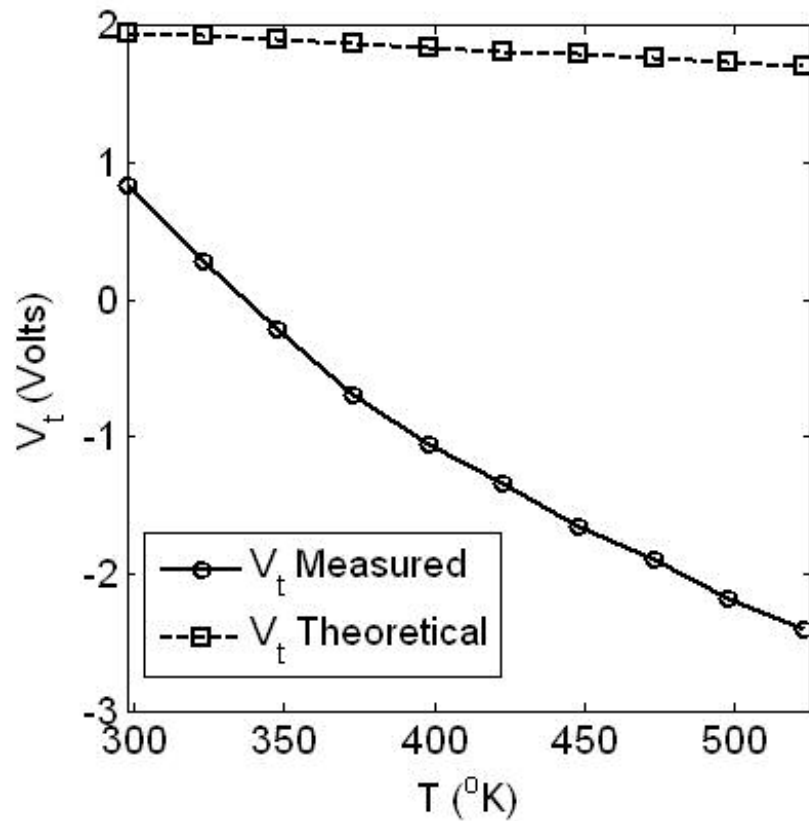


Figure 4.5. Measured threshold voltage and threshold voltage calculated by excluding the effect of fixed charge density and occupied interface trap density, at different temperatures. The threshold voltages have been measured (or calculated) for a $200\mu\text{m}\times 200\mu\text{m}$ 4H-SiC MOSFET with a polysilicon gate, oxide thickness of 600\AA , and a p-type epi-layer doping of $5\times 10^{15}\text{ cm}^{-3}$.

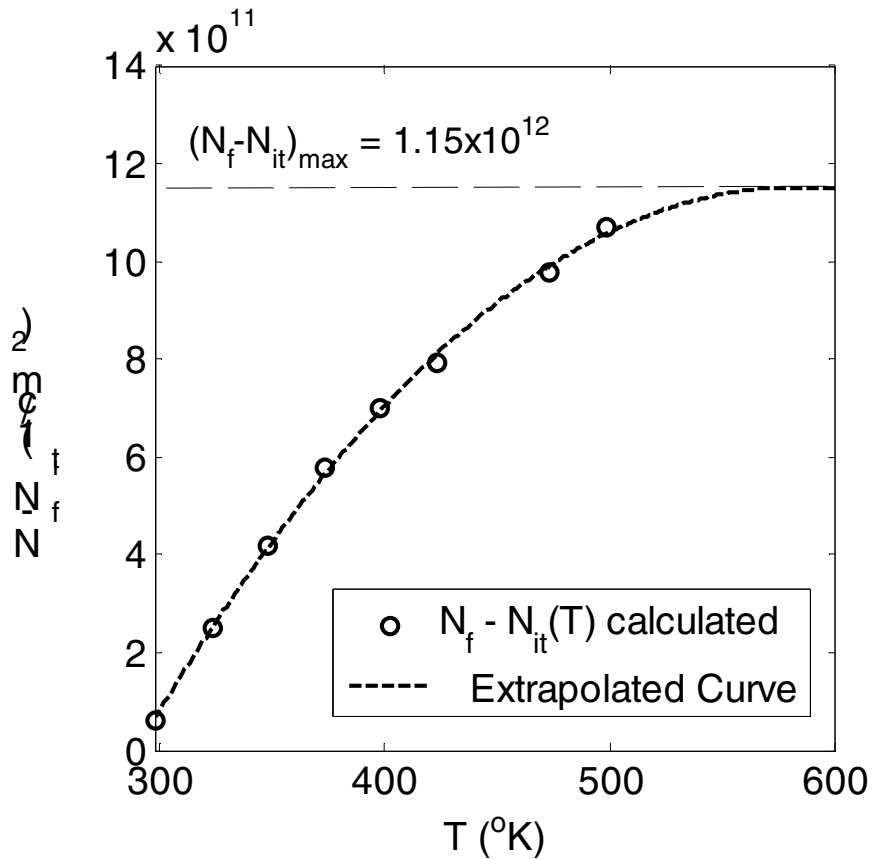


Figure 4.6. Plot of the difference between fixed oxide charge density and the occupied interface trap density as a function of temperature, obtained from threshold voltage measurements. By extrapolating the curve joining the data points, it is seen that the difference reaches a maximum value of $1.15 \times 10^{12} \text{ cm}^{-2}$. This can be interpreted as the point at which the occupied interface trap density reaches its minimum value. I take this value to be the value for the fixed oxide charge density.

4.2.3. 4H-SiC MOSFET Parameter Extraction Scheme

The mobility models described in Chapters 3 and 4, the formulation for the occupied interface trap density evaluation along with the fixed oxide charge values found analytically are input to the drift diffusion simulator described in Chapter 2. I am able to extract the electrostatic potential, electron concentration, hole concentration, details of current flow, electric fields, and mobility, inside the 4H-SiC MOSFET from the simulator. I also get terminal IV characteristics, which are then compared to experimental data.

In order to extract material properties from the simulator, I fit the low field and high field IV curves to experimental data. I have used experimental measurements made on 4H-SiC devices at ARL. I first try to fit the low field IV curves. I keep my drain voltage as 0.25 V and vary the gate voltage from around -4V to 15V. Various scattering mechanisms play the dominant roles at various gate voltages. At low gate voltages, in the subthreshold region, the total mobility is limited by Coulomb scattering. The midgap value of the interface trap density of states is obtained by fitting low field I_d - V_g curves in subthreshold to the experimental data. The interface traps lying close to the midgap are filled when the device is operating in the subthreshold region. Ideally, the occupancy of traps should be much less when the device is operating in the subthreshold region. But, owing to the very high density of states of interface traps in 4H-SiC, I see significant occupation of traps even when the device is operating in the subthreshold region. So, it is not easy to separate out the fixed charge and the occupied interface trapped charge even in subthreshold. I use the fixed charge density value calculated in the above section with a small correction for the inversion charge density. As gate voltage increases, the traps lying near the conduction band edge begin to fill up. Hence, the near threshold regions of the I_d - V_g curves give me the estimate for the conduction band edge density of states for interface traps.

With further increase in gate voltage, the inversion layer charge density begins to increase. This causes screening of the occupied interface traps. Hence, the Coulomb mobility begins to rise, and other scattering mechanisms begin to dominate. At higher gate voltages, the surface roughness mobility becomes the dominant scattering mechanism, and hence this region of the I_d - V_g curves gives me an estimate for the surface roughness parameter (Γ_{SR}).

Simulations and fitting of high lateral field IV curves (I_d - V_d characteristics) gives me the estimate for the electron saturation velocity (v_{sat}). It was required to change the saturation velocity for fitting I_d - V_d curves at different gate voltages. This suggests that the saturation velocity for electrons in the inversion layer is not constant, but changes with change in gate voltage.

All the simulations have been done for a $200\mu\text{m}\times 200\mu\text{m}$ 4H-SiC MOSFET. The device was fabricated at CREE Inc. and all the measurements were done at ARL. The MOSFET has a $3\mu\text{m}$ thick epi-layer which is doped at around $5\times 10^{15}\text{ cm}^{-3}$. It has polysilicon material as the gate contact. The oxide is thermally grown and has a thickness of around 600\AA .

CHAPTER 5

5. Simulation Results and Interpretations

In this chapter, I have described in detail the various simulations I have carried out and my interpretations of the results obtained. I start with describing the room temperature low field I_d - V_g and high field I_d - V_d simulations that fit the experimentally measured values. I then discuss details of the physics of the interface and the inversion layer that I can extract from my simulations. I describe the role played by interface traps at the SiC – SiO₂ interface in 4H-SiC in degrading mobility and lowering the mobile charge density in the inversion layer. I show detailed comparisons of various mobilities in the inversion layer and isolate the prominent mobility degrading mechanisms at room temperature. The simulations show that Coulomb scattering by occupied interface traps and fixed oxide charges is the dominant mobility degrading mechanism for 4H-SiC MOSFETs. The simulations also show that at higher gate voltages, surface mobility is degraded more due to surface roughness scattering than Coulomb scattering. I also discuss the effect of screening of the trapped charges and the fixed oxide charges, on Coulomb mobility near the surface. At the end, I describe my simulations predicting the performance enhancement of the 4H-SiC MOSFET that can be achieved by reduction in the interface trap densities at the band edges, and/or the reduction in surface roughness of the SiC – SiO₂ interface.

5.1. Room Temperature Fits to Experimental Data

Figures 5.1 to 5.3 show low field (subthreshold and linear region), and high field IV curves obtained by simulation of a $200\mu\text{m}\times 200\mu\text{m}$ 4H-SiC MOSFET at room temperature. The physical description of the MOSFET is given in Chapter 4. Very good agreement of the simulated curves with the experimental data has been achieved. Various material parameters have been used to get the simulations to fit to experimental data. These parameters and their effect on various physical processes have been detailed in Chapters 3 and 4. By comparing the low field I_d - V_g simulations to experimental data, I can get estimates for the interface trap density of states profile for the MOSFET. The estimated interface trap density of states profile is shown in Figure 5.4. This result is consistent with a few experimentally measured values given in literature [5][6][32][33][34]. I am also able to get the value of the surface roughness parameter by fitting the high gate voltage part of the I_d - V_g curve to experimental data. The surface roughness parameter value that I obtain is 3.7×10^{12} V/s. I believe that I might be overestimating the surface roughness scattering in my simulations. The reason for this is that I have implemented screening for Coulomb scattering, but not for surface roughness scattering. Screening reduces the effect of scattering at voltages where the inversion charge density is high. I intend to develop a more detailed model for surface roughness in the future. I have described a method for extracting the fixed oxide charge density in Chapter 4. For these simulations, I have used a fixed oxide charge density of 1.3×10^{12} cm^{-2} , which is slightly more than expected from the calculations shown in Chapter 4. This is in perfect accordance with the calculations, wherein I had mentioned that, as the inversion charge density is not going to be zero at threshold, the fixed oxide charge density will be slightly higher than calculated. At room temperature, the threshold voltage of this MOSFET is about 0.83V.

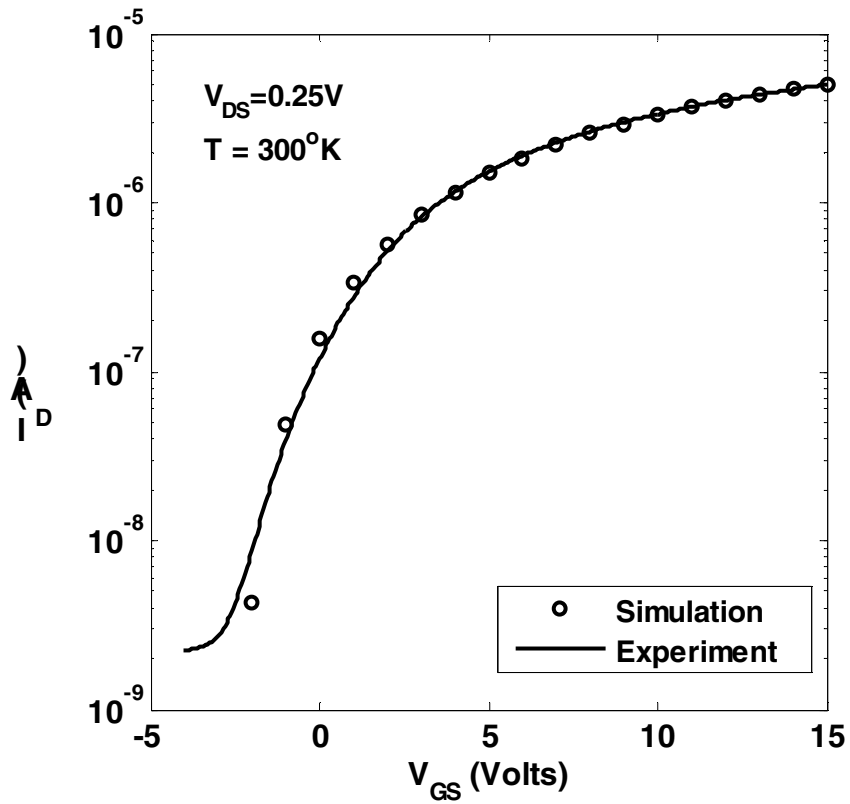


Figure 5.1. Drain current versus gate-source voltage on a logarithmic scale, for the $200\mu\text{m} \times 200\mu\text{m}$ 4H-SiC MOSFET at room temperature, and a drain-source voltage of 0.25V. Agreement between simulation and experiment is shown in the subthreshold region over several orders of magnitude.

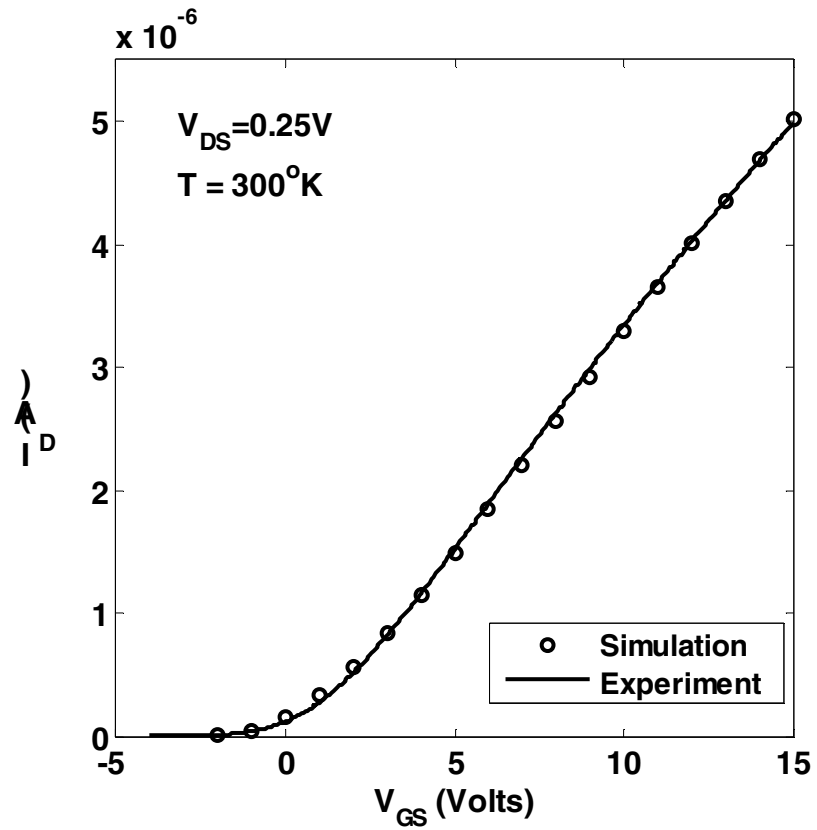


Figure 5.2. Drain current versus gate-source voltage on a linear scale, for a $200\mu\text{m} \times 200\mu\text{m}$ 4H-SiC MOSFET at room temperature, and a drain-source voltage of 0.25V. Agreement is achieved between simulation and experiment in linear region of operation.

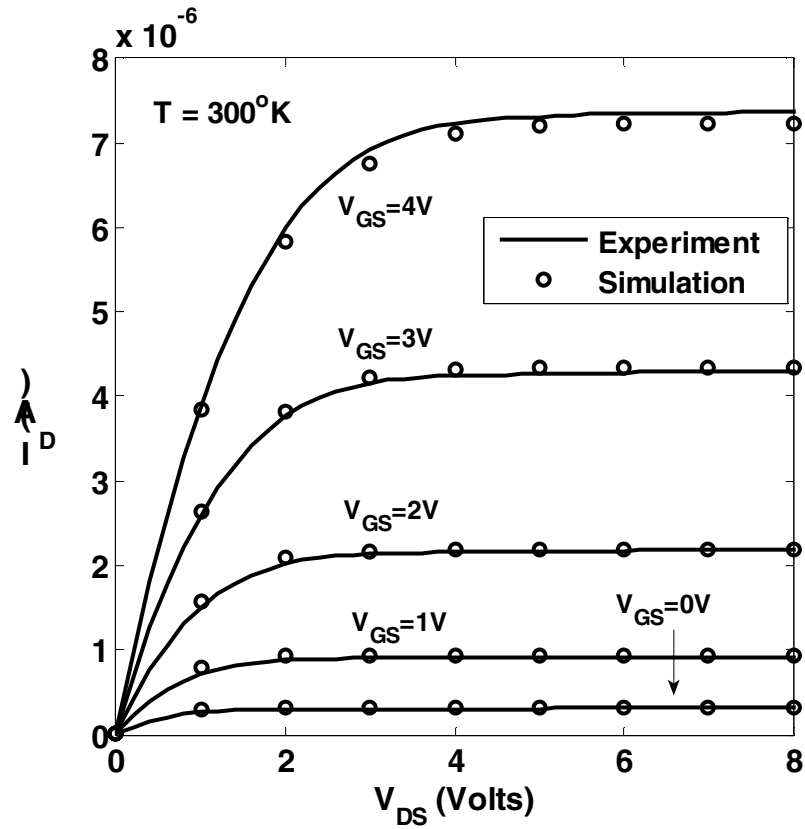


Figure 5.3. Drain current versus drain-source voltage for a $200\mu\text{m} \times 200\mu\text{m}$ 4H-SiC MOSFET at room temperature. Agreement is shown between simulation and experiment in the high field region, for several different gate voltages.

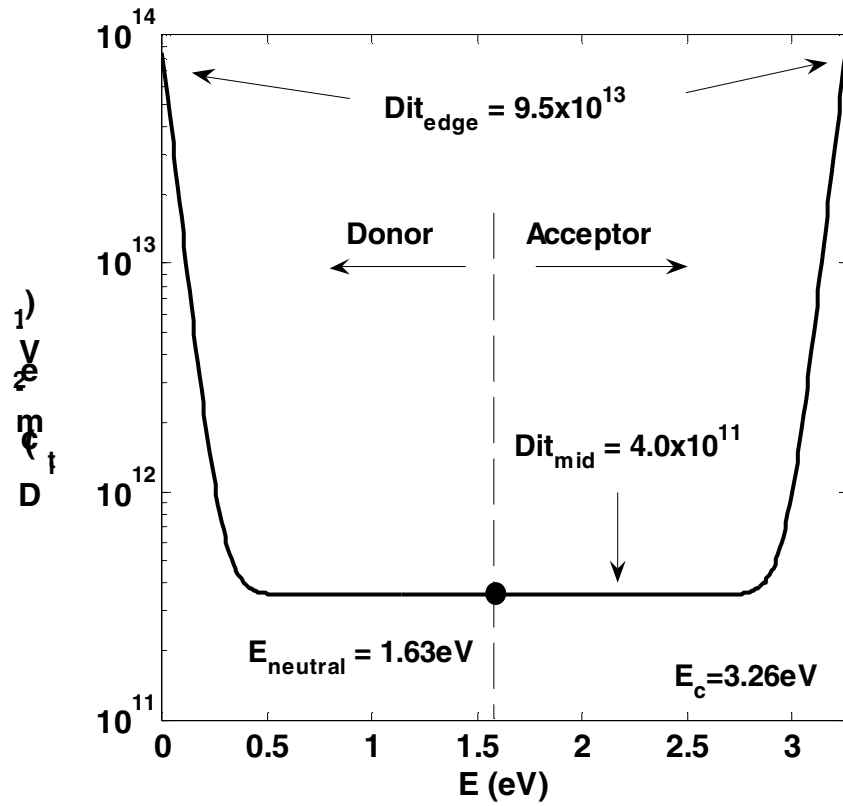


Figure 5.4. Interface trap density of states profile for a 4H-SiC MOSFET. The various parameters have been determined by comparing and fitting simulated room temperature I_d - V_g curve to experimental data. The best fit was obtained for $D_{it_{mid}} = 4.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, $D_{it_{edge}} = 9.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, and $\sigma_{it} = 0.0515 \text{ eV}$. The fixed oxide charge density was determined to be $1.30 \times 10^{12} \text{ cm}^{-2}$.

5.2. Room Temperature Physics of 4H-SiC MOSFETs

In this section, I will describe the physics inside a 4H-SiC MOSFET that can be inferred from my simulations. In all the plots, the various physical quantities are described at the center of the channel.

5.2.1. Interface Traps in 4H-SiC MOSFETs

The interface traps in 4H-SiC MOSFETs affect the device performance in two ways. Firstly, because of the excessive high density of traps, the density of occupied traps is much higher than the density of the mobile inversion charge at room temperature. Figure 5.5 shows the comparison of the occupied interface trap density and the mobile inversion charge density at observed at the center of the channel of the simulated MOSFET at room temperature. The drain – source voltage is kept at 0.25V. As can be clearly seen, the very high density of states of the interface traps has resulted in a much higher occupied interface trap density as compared to the inversion layer mobile charge density. Thus, the presence of interface traps significantly lowers the mobile charge density available for conduction, and thereby reducing the total current. It also gives a positive shift in the threshold voltage.

The other significant effect of the extremely large number of occupied interface traps, and the fixed oxide charge, is the severe degradation of the surface mobility in 4H-SiC MOSFETs due to Coulomb Scattering. The fixed oxide charge is assumed to be located at the interface. Usually it is located inside the oxide up to a depth of around 30Å. Figure 5.6 shows the Coulomb mobility as a function of depth inside the semiconductor at different gate voltages. It can be clearly seen that Coulomb scattering mobility is very low at the surface, but rises as we go deeper

inside the device. Due to the screening of the scattering charges by the mobile charges, the Coulomb scattering reduces sharply with depth away from the interface. Hence, the Coulomb mobility curves for higher gate voltages show a much steeper rise. Thus it can be inferred that Coulomb scattering of mobile charges by occupied interface traps and fixed oxide charge is significant only very close to the interface. It is the dominant mobility degradation mechanism close to the interface.

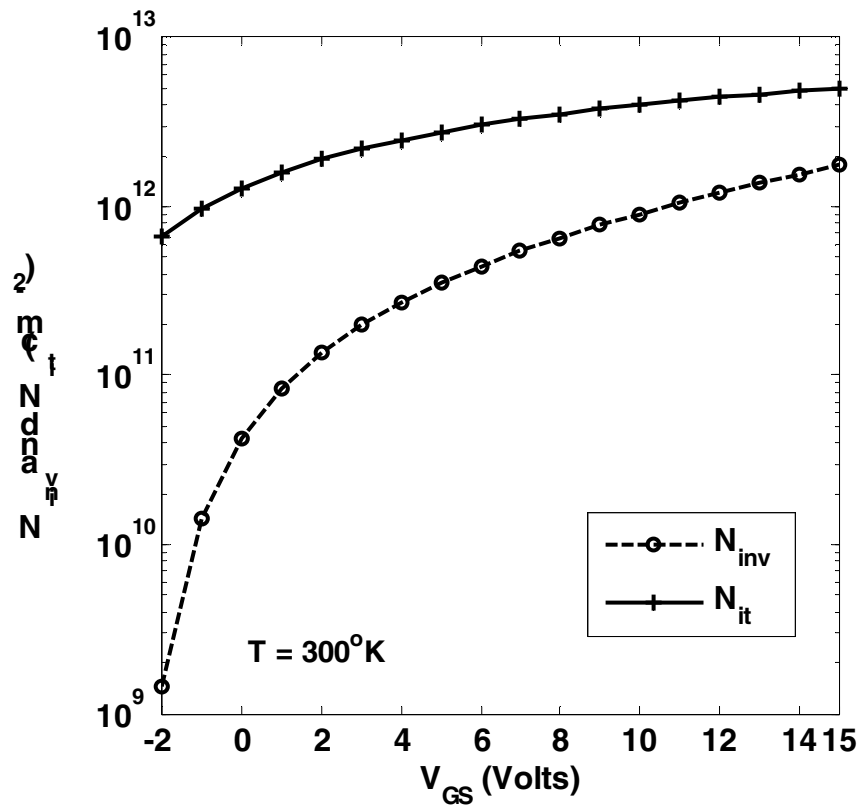


Figure 5.5. Comparison of the inversion charge density (N_{inv}) and the occupied interface trap density (N_{it}) at different gate voltages, at room temperature. The very high density of occupied traps reduces the number of free inversion layer carriers, and hence causes current degradation.

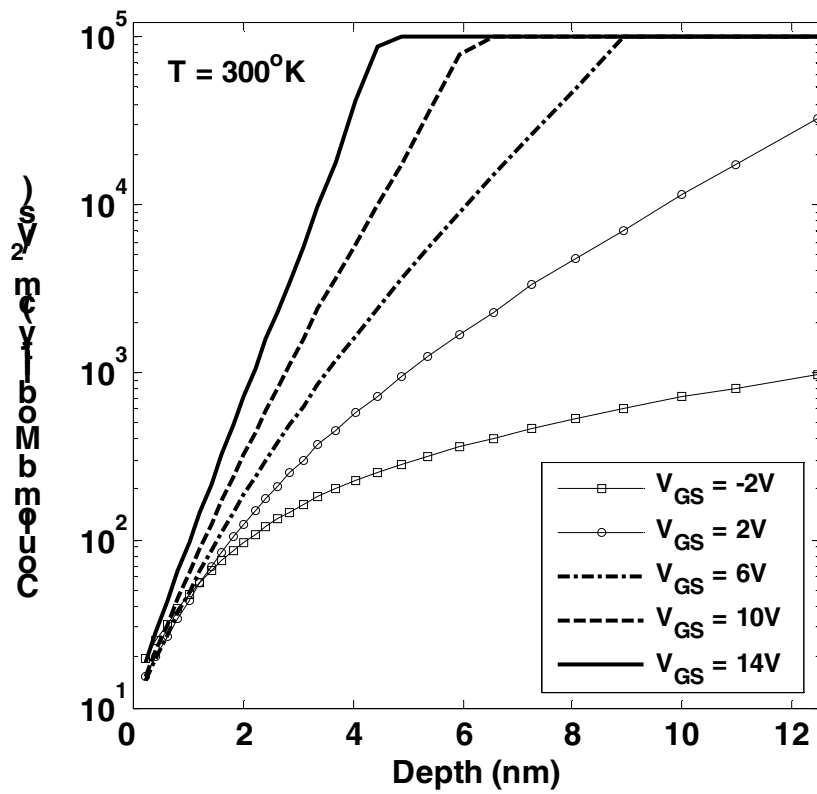


Figure 5.6. Coulomb scattering mobility (μ_C) plotted as a function of depth inside the semiconductor, at different gate voltages. Notice that the mobility is extremely low ($\sim 20 \text{ cm}^2/\text{Vs}$) at the surface, but rises quickly with depth. At higher gate voltages, due to the large number of inversion layer charges, screening of the scattering charges becomes strong, causing the Coulomb mobility to rise more sharply.

5.2.2. Surface Roughness

The other significant mobility degradation mechanism that is seen for 4H-SiC MOSFETs, is surface roughness. Figure 5.7 shows the surface roughness mobility curves as a function of depth inside the device, at different gate voltages. According to the surface roughness mobility model, the surface roughness scattering depends on the strength of the perpendicular electric field. As can be seen from the figure, at low gate voltages, the surface roughness mobility is quite high, and does not cause any degradation in the low field mobility. But at higher gate voltages, the perpendicular electric field becomes strong, leading to an increase in surface roughness scattering. In fact, at large gate voltages, the surface roughness scattering becomes more dominant than the Coulomb scattering, and it controls the total low field mobility.

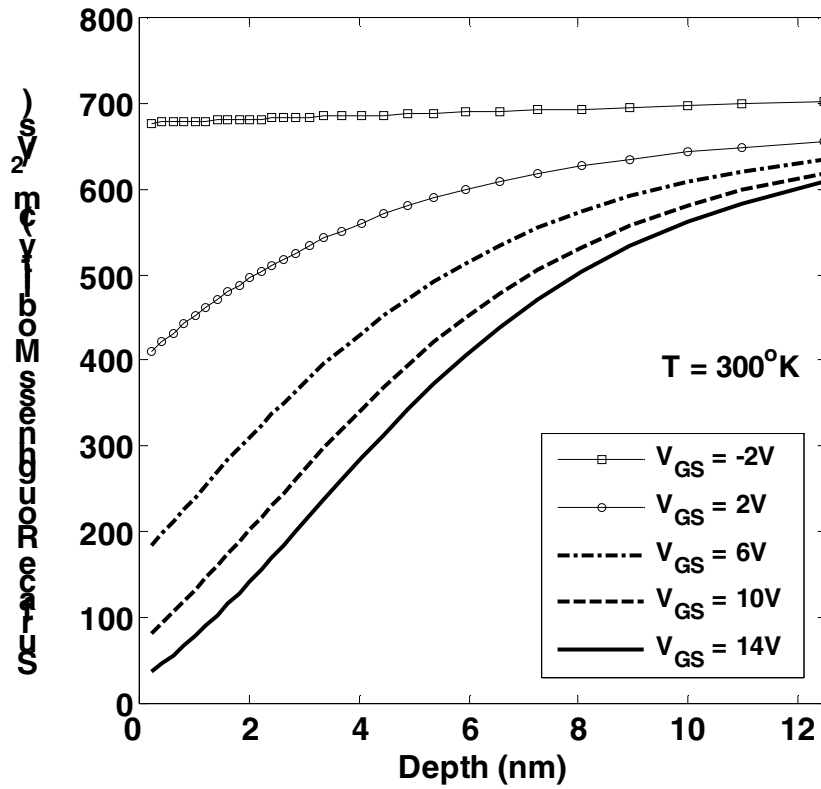


Figure 5.7. Surface roughness mobility (μ_{SR}) plotted as a function of depth inside the semiconductor. (μ_{SR}) is lowest at the interface, where the perpendicular field is the strongest. With increase in gate voltage, the perpendicular field increases, causing a decrease in the surface roughness mobility. The surface roughness factor was obtained as $\Gamma_{SR} = 3.7 \times 10^{12}$ V/s from I_d - V_g simulation fits to experimental data.

5.2.3. Total Low Field Mobility

Figure 5.8 shows the comparison between different low field mobility mechanisms at a gate voltage of 6V. The Coulomb mobility and the Surface Roughness mobility are the two main mobility limiting mechanisms at this gate voltage. The bulk mobility does not play much of a role in limiting the total mobility near the surface. The total mobility approaches the bulk mobility value much away from the surface. The surface phonon mobility also does not play a role in limiting low field mobility.

In Figure 5.9, I show the total low field mobility varying with depth at different gate voltages. Owing to the very low Coulomb mobility at the surface, the total low field mobility at the surface is very less. At 2\AA away from the interface, the total low field mobility is around $20\text{ cm}^2/\text{Vs}$ for gate voltages ranging from -2V to 14V . It rises quickly some distance away from the interface because screening starts playing a big role, causing the Coulomb scattering to reduce drastically. At $V_g = -2\text{V}$, there are very few inversion layer electrons, and hence, the screening is the least. Hence, the total mobility does not rise very quickly as we move away from the interface.

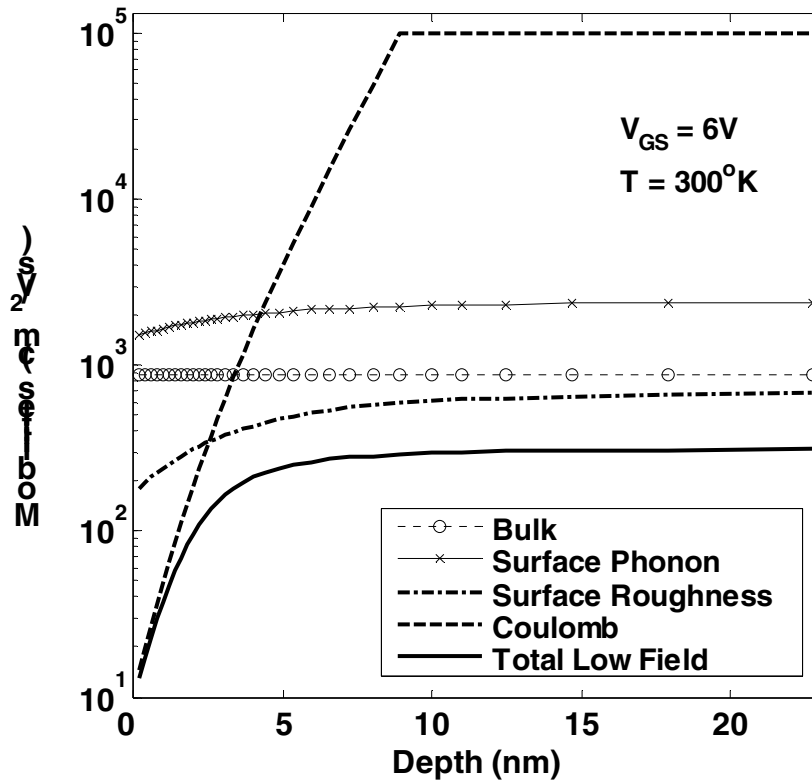


Figure 5.8. Figure showing the comparison between the various low field mobility components at a gate-source voltage of 6V, and at room temperature. The total low field mobility near the surface is limited by the Coulomb mobility, whereas the surface roughness mobility becomes dominant at a depth of around 3 nm. The total mobility reaches the bulk mobility value much deeper inside the semiconductor (> 20 nm)

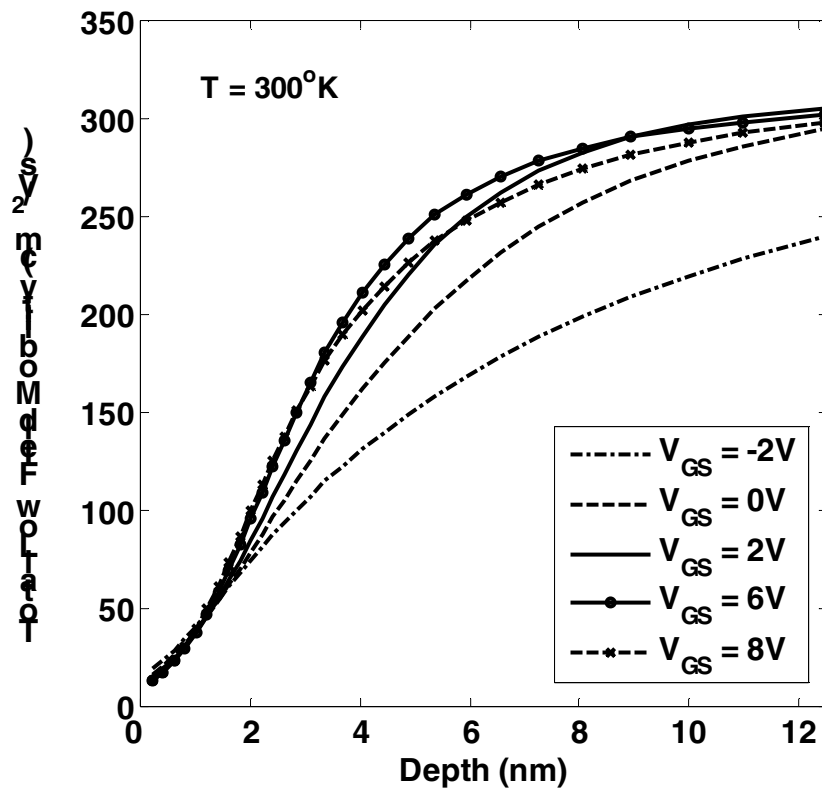


Figure 5.9. Total low field mobility (μ_{LF}) as a function of depth, at the center of the channel. Gate-source voltages range from -2V to 8V. The drain-source voltage is 0.25V, and the simulation is done for room temperature. The low values of the total mobility near the surface are due to large amount of Coulomb scattering close to the interface.

5.2.4. Electron Concentration and Current Density

The current flowing at any depth inside the semiconductor depends on the product of the total mobility, and the concentration of mobile charges at that depth. I have shown that the mobility at the surface is very low, but it rises sharply some distance away from the interface. In Figure 5.10, I show the variation of electron concentration with depth at different gate voltages. With increase in gate voltage, the electron concentration of the 4H-SiC N-MOSFET increases. The electrons are pulled near to the interface by the gate field. Hence, at any gate voltage, the electron concentration is the maximum nearest to the interface, and decreases exponentially with depth inside the semiconductor. This is the proper classical electron concentration variation with depth curve. Electron concentration reaches a value of $1 \times 10^{19} \text{ cm}^{-3}$ at the interface, at a gate voltage of 14 V.

We might be persuaded to think that, as the electron concentration is the highest at the interface, the maximum current will be flowing at the interface. But as shown in Figure 5.11 this is actually not the case. Because of the excessively high scattering and very low mobility at the interface, the peak of the current density curve is seen some distance away from the interface. Hence, in 4H-SiC MOSFETs, the maximum current does not flow at the interface, but some distance away from it, inside the semiconductor. This understanding of the current flow in a 4H-SiC MOSFET has been achieved by the implementation of the depth dependent Coulomb Scattering mobility model, and the extremely fine mesh spacing inside the device structure. Also, from the same current density curve, we can see that the peak of the curve shifts towards the surface with increase in gate voltage. This is seen because with increase in gate voltage, the electrons are pulled closer to the interface.

Figure 5.12 shows an average depth of the inversion layer as a function of gate voltage. The average depth of the inversion layer is calculated using Equation 3.5. This curve shows that the average depth of the inversion layer decreases with increase in gate voltage; which is another way of saying that the electrons are pulled closer to the interface with increasing gate voltage. The amount of screening is inversely proportional to the average depth of the inversion layer and directly proportional to the average density of the inversion layer. With increase in gate voltage, as the density of the inversion layer increases (Figure 5.5), and its average depth decreases (Figure 5.12), the amount of screening will rise rather quickly.

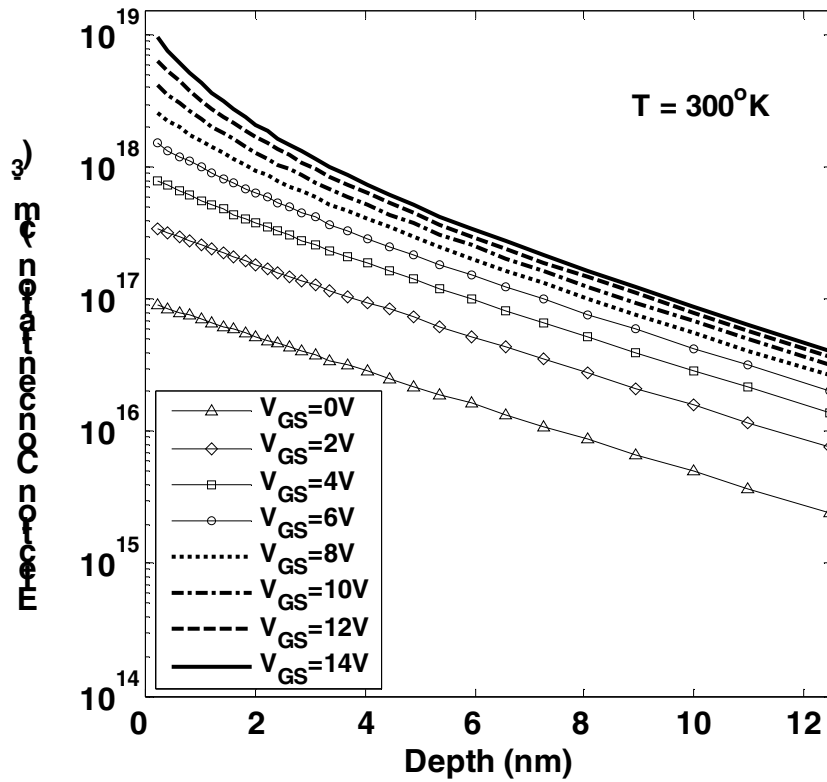


Figure 5.10. Variation of electron concentration with depth, at the center of the channel, shown for different gate-source voltages and at room temperature. The curves follow the classical electron distribution curve, showing the maximum concentration at the interface and an exponential decrease with depth inside the semiconductor.

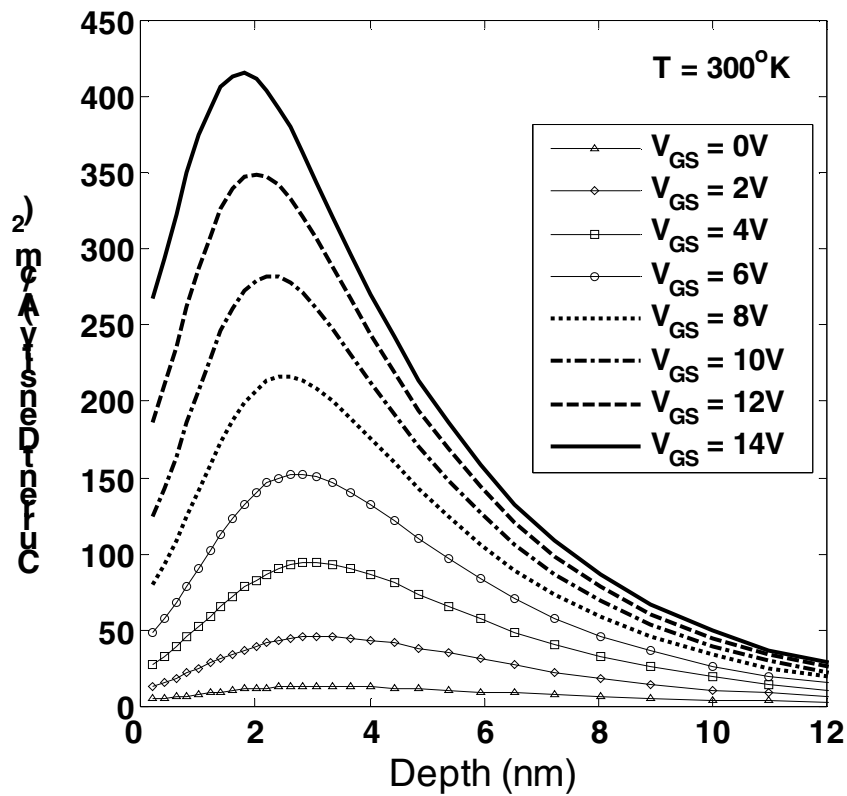


Figure 5.11. Current density variation with depth for a 4H-SiC MOSFET at room temperature. Because of the extremely low mobility near the surface, the maximum current does not flow at the surface, but some distance below it. For a gate-source voltage of 14V, when the MOSFET is in deep inversion, the peak of the current density is approximately 2nm below the interface. The current is spread out over a larger depth at low gate-source voltages. The peak shifts towards the interface with increase in gate-source voltage.

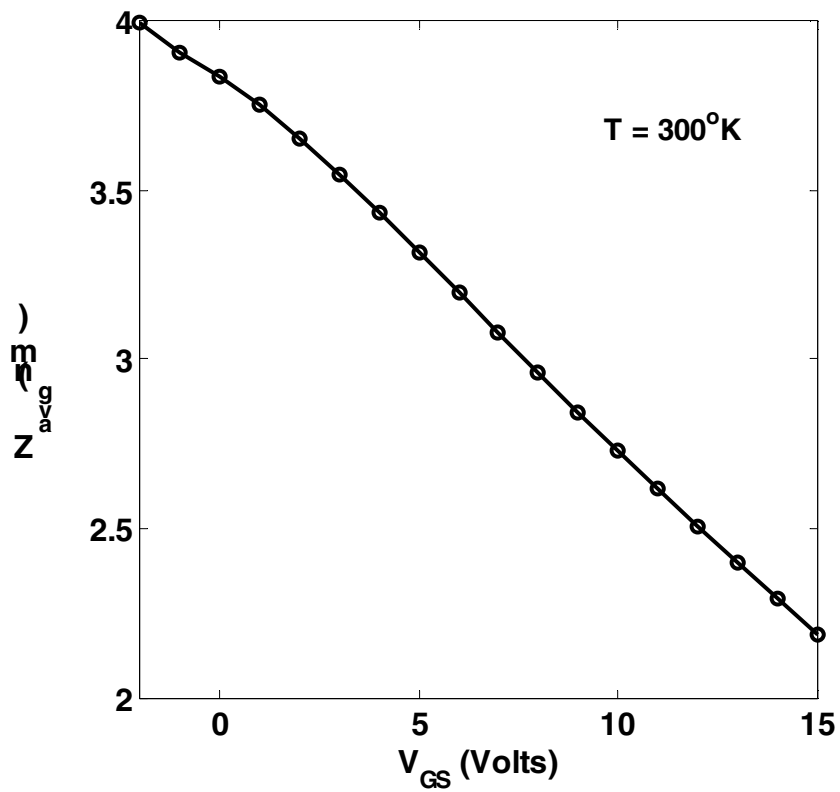


Figure 5.12. Average depth of the inversion layer (Z_{avg}) plotted as a function of gate-source voltage, at room temperature. With increase in gate-source voltage, the electrons are pulled closer to the interface, and hence the average depth of the inversion layer decreases.

5.2.5. Comparing Coulomb Mobility and Surface Roughness Mobility

Figures 5.13 and 5.14 show comparisons between the two dominant mobility degradation mechanisms – Coulomb Scattering, and Surface Roughness Scattering. The mobility at the center of the channel is plotted as a function of depth away from the interface towards the bulk. As shown in Figure 5.13, at a low gate voltage of 2V, the surface roughness mobility is very high and does not play a role in limiting the total mobility. The Coulomb mobility is low and is responsible for the low total mobility at the interface. Also, because of the low inversion charge density, the screening is also less here. Hence, the Coulomb mobility remains low for a much larger depth inside the semiconductor. In fact, as seen in the figure, for the entire depth over which the current is spread, the Coulomb mobility is the dominant mobility limiting mechanism. The total mobility curve follows the Coulomb mobility curve.

Now consider the comparison of Figure 5.14. The figure shows mobility curves at a gate voltage of 12 V. Here too, at the surface, the Coulomb mobility is the lowest. But now, there is a huge amount of screening due to the large inversion layer density. Hence, the Coulomb mobility shoots up very quickly, over a very small distance away from the interface. As the surface field is very high, the surface roughness mobility now dominates over much of the depth in which the current is spread. The total mobility curve now follows the surface roughness mobility curve. Hence, we can say that, even though the surface mobility is still controlled by Coulombic scattering due to the occupied interface traps, the actual current limiting mobility is controlled by the amount of surface roughness. This conclusion might not be entirely valid because surface roughness scattering is also screened; but I have not implemented a screened surface roughness scattering mobility model in my simulator.

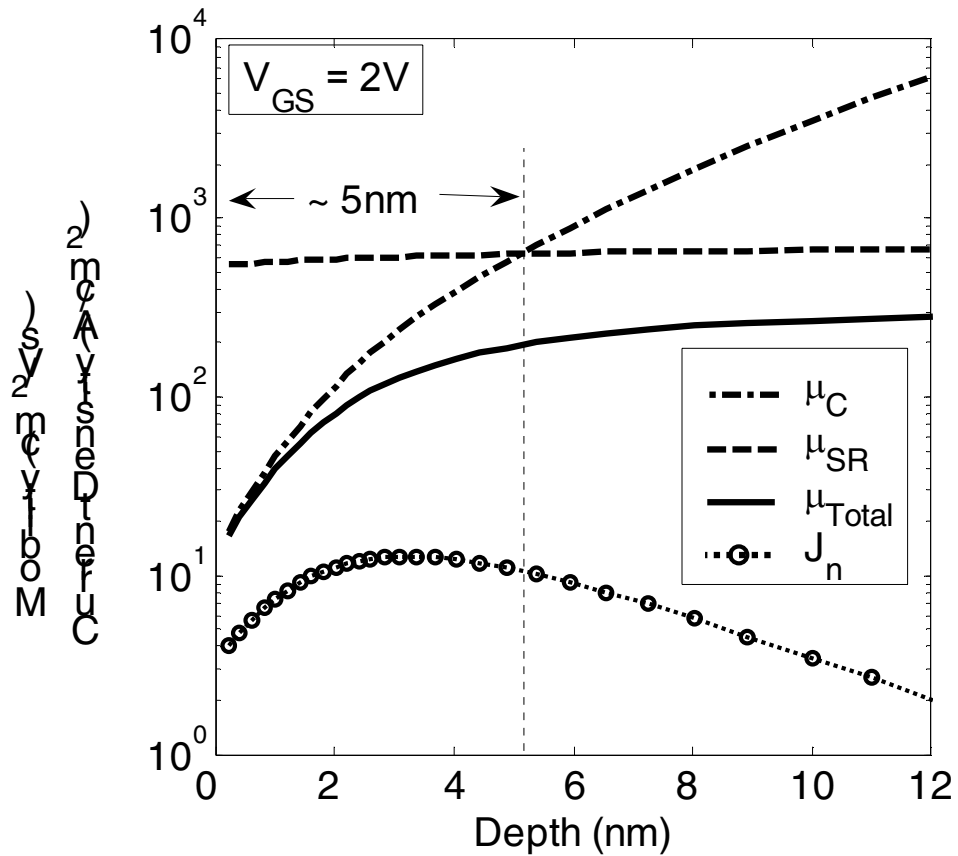


Figure 5.13. Comparison between Coulomb scattering mobility (μ_C) and surface roughness mobility (μ_{SR}) at a gate-source voltage of 2V. Coulomb mobility dominates the total low field mobility for most of the depth over which the current is spread. Coulomb scattering mobility curve crosses the surface roughness mobility curve at a depth of around 5nm. (Note: The scales for mobilities and the current density are the same, but their units differ.)

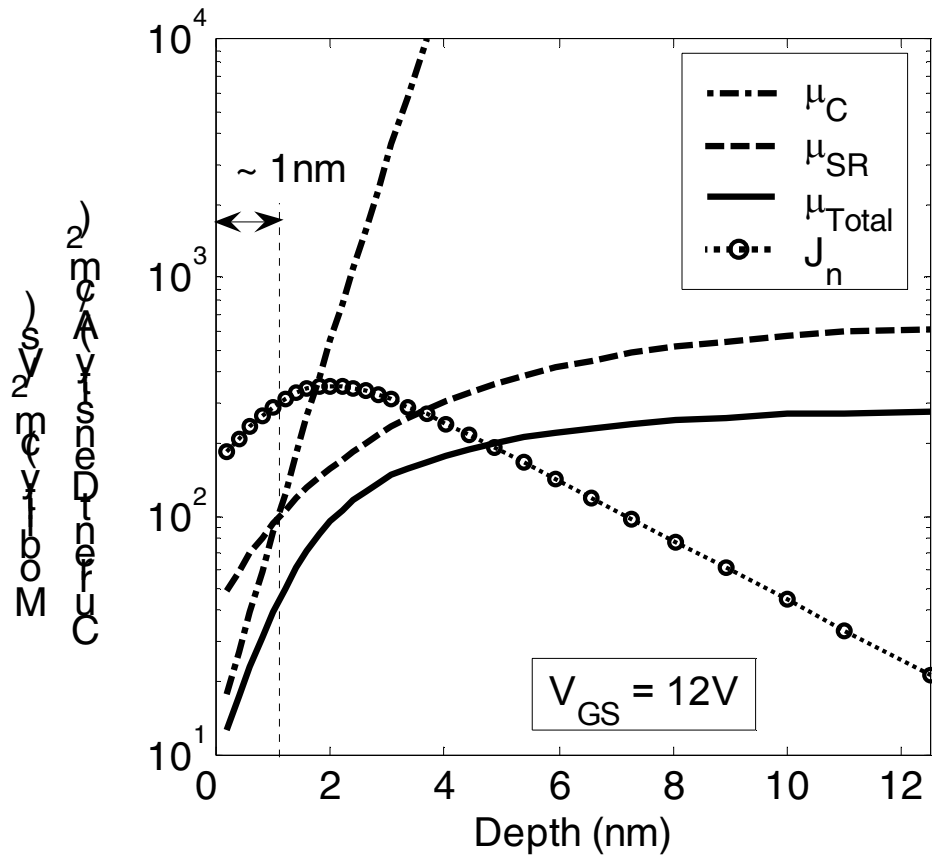


Figure 5.14. Comparison between Coulomb scattering mobility (μ_C) and surface roughness mobility (μ_{SR}) at a gate-source voltage of 12V. Coulomb mobility dominates the total low field mobility only near the surface. Beyond a depth of around 1nm, the surface roughness mobility dominates the total low field mobility for most of the distance over which the current is spread. (Note: The scales for mobilities and the current density are the same, but their units differ.)

5.2.6. Effect of Screening

Screening of the occupied interface traps and the fixed oxide charge by inversion layer mobile charges reduces the effect of Coulomb Scattering. The screened Coulomb potential falls off as an exponential, and hence its effect is limited to very small distances. In all the results shown above, the simulations include this effect of screening. Figure 5.15 shows the low field I_d - V_g characteristics of the same device, with the same interface trap density profile and with all the other parameters, but without the screening effect. It is very clearly seen that the current at higher gate voltages is much lower than the experimental value (and the previously shown simulated values). Thus screening plays an important role in reducing the Coulomb scattering, and thereby improving the device performance.

As shown in Figure 5.6, because of screening, the Coulomb mobility tends to increase with increase in gate voltage, even though the number of occupied traps also increases. This effect is especially noticeable some distance away from the interface. But, if the screening phenomenon is not considered, then we actually see the Coulomb mobility decreasing with increasing gate voltage. This is shown in Figure 5.16. Also notice how the Coulomb mobility does not rise as rapidly as in the case where screening was considered.

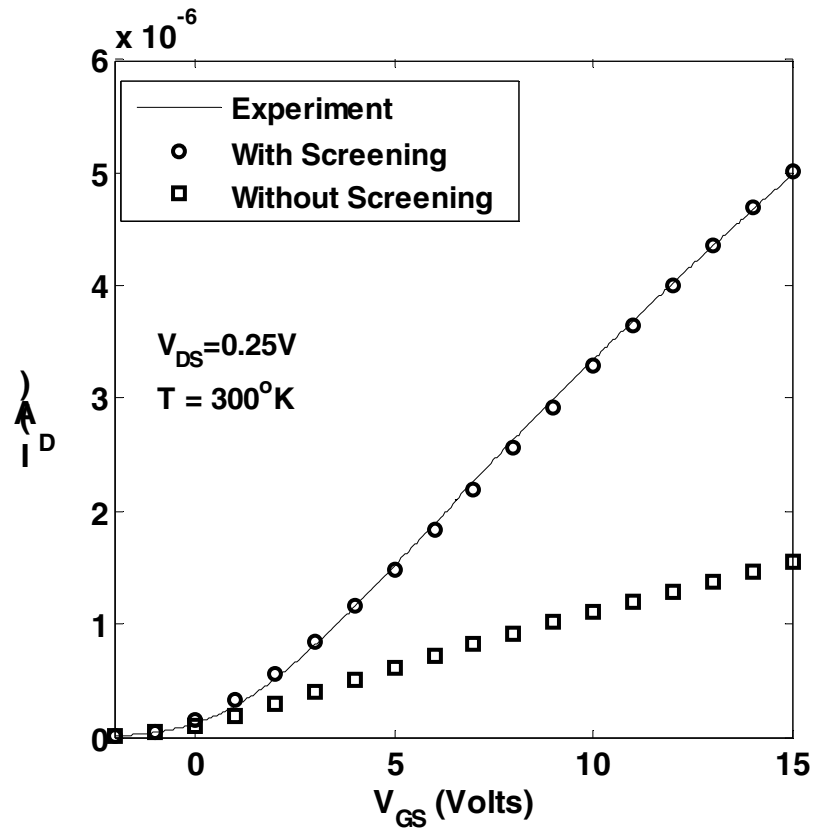


Figure 5.15. Low field drain current versus gate-source voltage characteristics for the two cases of screened and unscreened Coulomb scattering mobility models. Screening of the charged scattering centers by inversion layer electrons causes a reduction in Coulomb scattering at higher gate-source voltages, causing the current to rise.

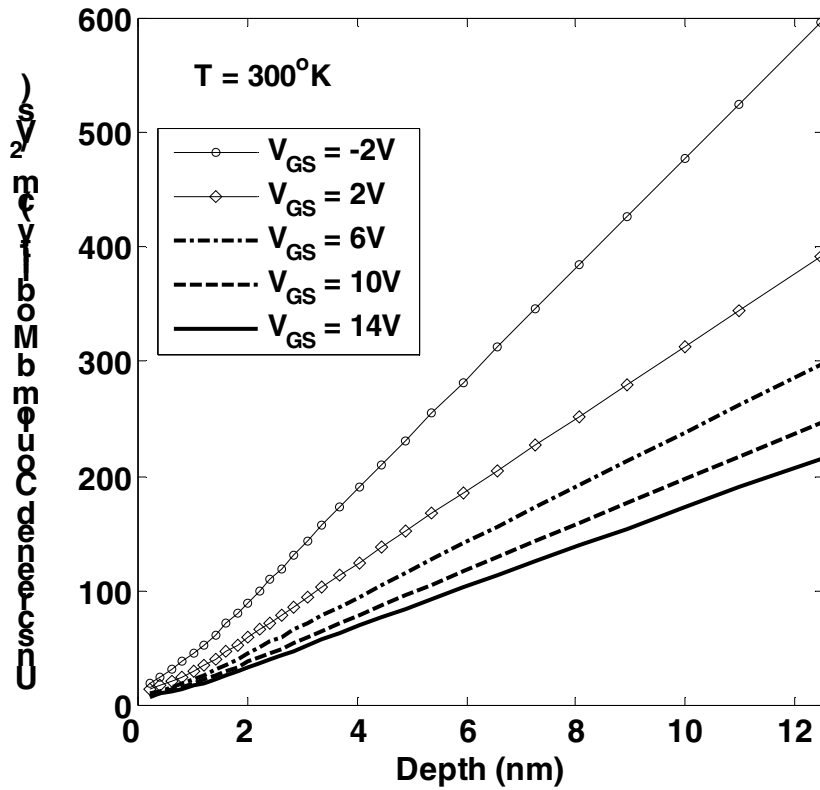


Figure 5.16. Coulomb scattering mobility plotted as a function of depth inside the semiconductor for the case of unscreened Coulomb scattering. With increase in gate-source voltage, the density of occupied traps increases, causing reduction in Coulomb mobility. This is contrary to the result (Figure 5.6) when screening of these traps by the inversion layer electrons is taken into account.

5.3. Device Performance Predictions based on Simulations

In this section, I describe the predictions of device performance that I can make on the basis of my drift diffusion simulations and mobility models. I will focus on the two main performance degrading mechanisms that I have talked about, viz. Coulomb Scattering due to occupied interface traps, and Surface Roughness Scattering.

5.3.1. Reduction of the Occupied Interface Trap Density

As I have described earlier, the extremely high density of occupied interface traps in 4H-SiC is due to the sharp exponential rise in the interface state density of states near the conduction band and valence band edges. So, if the density of states of the traps near the band edges is reduced, then device performance should improve. There have been various discussions about fabrication methods which give a reduction in the band edge density of states of interface traps in SiC. Annealing in Nitrous Oxide (NO) is one way in which the density of interface traps near the band edges has been reduced. I now show simulations which predict how a 4H-SiC MOSFET device will perform if the interface trap density of states is reduced by factors of 10 and 100.

As has been discussed above, the interface traps lower the amount of inversion charge present in the device at any given gate voltage, and also cause mobility degradation at the surface due to Coulomb scattering of mobile charges. Figure 5.17 shows a comparison of the inversion layer charge densities when the interface trap density of states at the band edge is reduced by a factor of 10. Note that in the real case where my simulations have matched the experimental data, the inversion layer charge density is always less than the occupied interface trap density at all gate voltages. But when I reduce the density of states at the band edge by a factor of 10, the

inversion layer charge density rises sharply and becomes more than the occupied interface trap density at a gate voltage of around 2V. Hence, there are a lot more mobile charges available for conduction.

Figure 5.18 shows the Coulomb mobility as a function of depth, at different gate voltages, after a 10 fold reduction in trap density at the band edge. Notice how the mobility at the surface has increased as compared to Figure 5.6.

Figure 5.19 shows the current density variation with depth, at different gate voltages. Owing to the increased surface mobility as a result of the reduction in occupied states, the current density at each gate voltage has increased. Also, the peak of the current density is now shifted closer to the interface.

A combination the increased inversion charge density and increased surface mobility will give an increase in the current flowing through the device. Figure 5.20 shows the I_d - V_g curves of the 4H-SiC MOSFET, for the cases of unchanged, factor 10 reduced, and factor 100 reduced, interface trap density of states. The increase in current is significant when the interface trap density is reduced by a factor of 10. But, the increase in current is not significant when they are reduced further. The reason for this is that there is not much change in the surface mobility now, as the dominant mobility degradation mechanism is the surface roughness scattering. Also notice that the improvement in current is more marked in the low gate voltage region of the curve. This is because at higher gate voltages, surface roughness mobility is comparable to Coulomb mobility. Hence, at higher gate voltages, the total mobility is not changed much, when the interface trap density of states is reduced.

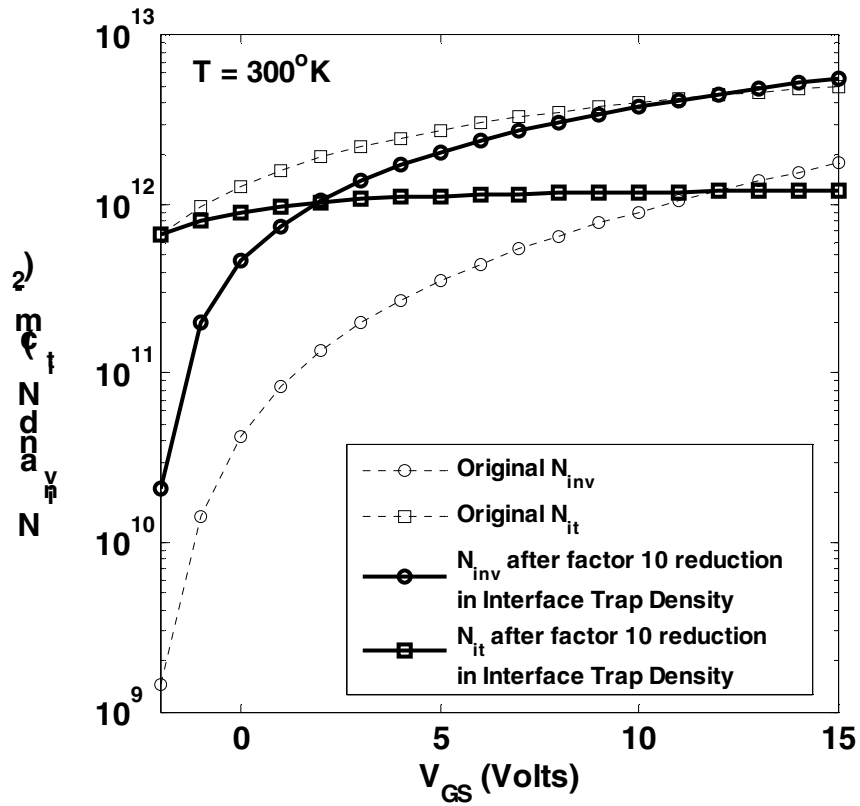


Figure 5.17. Comparison of the inversion charge density (N_{inv}) and the occupied interface trap density (N_{it}) at different gate voltages, for two different interface trap density of states profiles. The original interface trap density of states profile is as shown in Figure 5.4. The other curves are for the case when Dit_{edge} is reduced by a factor of 10 to $9.5 \times 10^{12} \text{ cm}^{-2}\text{eV}^{-1}$. Inversion charge density actually becomes more than the occupied trap density in the new reduced density of states case. Compare with Figure 5.5.

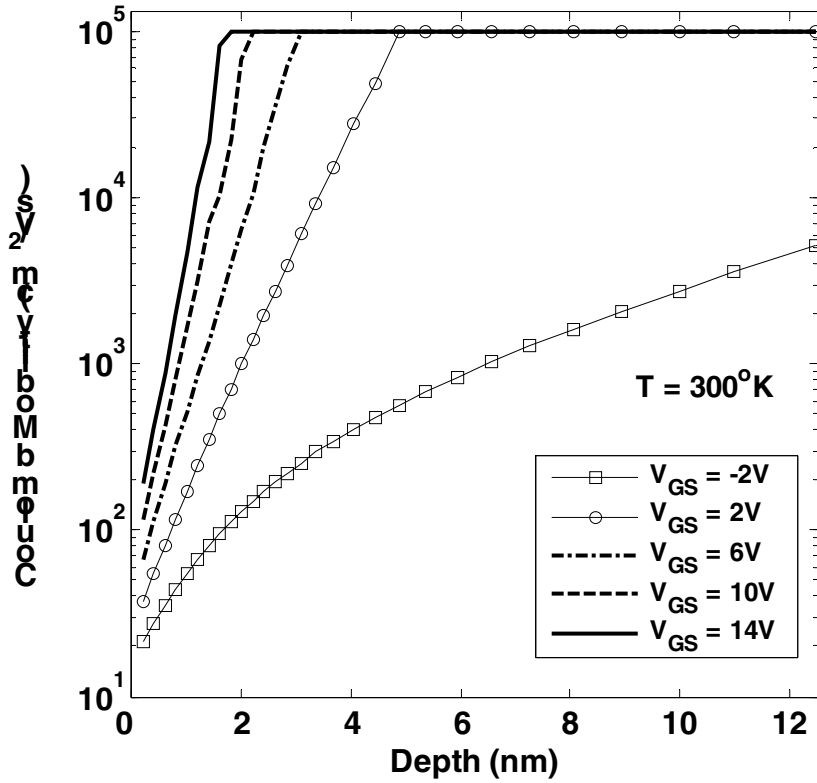


Figure 5.18. Coulomb scattering mobility (μ_C) plotted as a function of depth inside the semiconductor, at different gate voltages, for the case of reduced interface trap densities. Density of interface traps at the band edge has been reduced by a factor of 10 to $Dit_{edge} = 9.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Compare the minimum value of the Coulomb mobility at the surface ($\sim 200 \text{ cm}^2/\text{Vs}$) at a gate-source voltage of 14V, to the value of around $20 \text{ cm}^2/\text{Vs}$ shown in Figure 5.6.

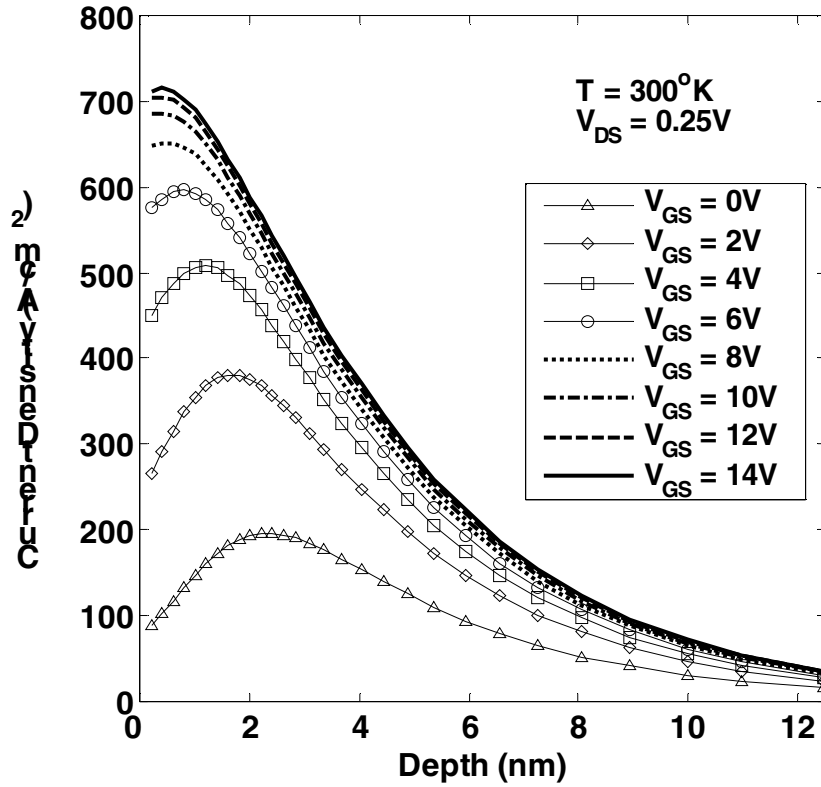


Figure 5.19. Current density variation with depth at room temperature for a 4H-SiC MOSFET with reduced density of states of the interface traps. Density of interface traps at the band edge has been reduced by a factor of 10 to $Dit_{edge}=9.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$. Compare the curves to the ones shown in Figure 5.11. Owing to the reduction in occupied traps at higher gate-source voltages, the peak current density has increased at higher gate voltages, and has also shifted closer to the interface.

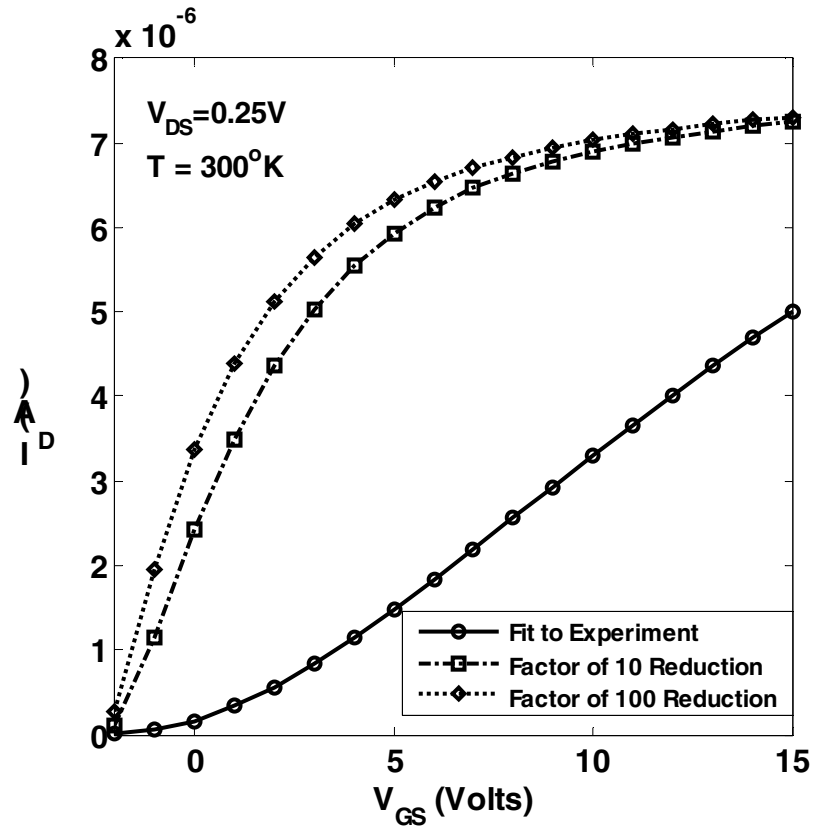


Figure 5.20. Drain current versus gate-source voltage for a 4H-SiC MOSFET at room temperature, and drain-source voltage of 0.25V. The three curves correspond to different density of states of the interface traps. The curve fitting the experimental data has a band edge density of states value of $9.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, while the other two curves have the Ditedge values as $9.5 \times 10^{12} \text{ cm}^{-2} \text{ eV}^{-1}$ and $9.5 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$. Notice how the current increases a lot for the first 10-fold reduction in interface trap density of states, while it does not increase significantly for the second reduction.

5.3.2. Reduction in Surface Roughness

The perpendicular component of the electric field is very small at low gate voltages, resulting in very less surface roughness scattering; whereas, at high gate voltages, due to a large perpendicular field, surface roughness scattering is large. Thus, surface roughness scattering plays an important role in limiting the low field mobility at large gate voltages. Hence, a reduction in surface roughness will improve the surface mobility at large gate voltages, but will not have much of an effect in subthreshold and near threshold regions. Figure 5.21 shows the I_d - V_g curves obtained when the surface roughness is reduced by factors of 10 and 100.

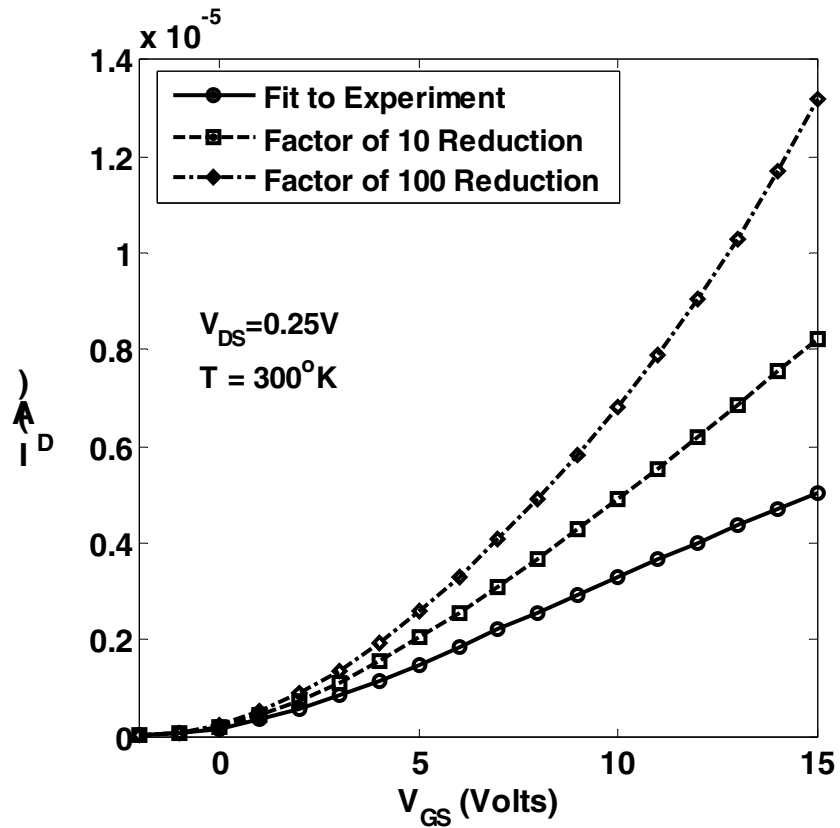


Figure 5.21. Drain current versus gate-source voltage curve for a 4H-SiC MOSET at room temperature and a drain-source voltage of 0.25V. Improvement in current at higher gate voltages is obtained on reduction of the surface roughness. There is not much improvement in current at lower gate voltages, because surface roughness scattering is not significant at low gate voltages.

5.3.3. Combined Reduction of Interface Trap Density and Surface Roughness

My simulations show that for device operation near threshold, reduction in interface trap density of states near the band edges gives a more pronounced performance enhancement than reduction in surface roughness. Figure 5.22 shows the comparison of the device IV characteristics for the cases of reduction in surface roughness, and the reduction in interface trap density of states, at a gate voltage of 4V. As can be clearly seen, reduction of surface roughness gives only about a 60% improvement in current, whereas, reduction of the interface states density gives a whopping 500% improvement in current.

At higher gate voltages though, improvement in surface roughness gives about the same performance enhancement, as the improvement in interface trap density of states would give. Figure 5.23 shows the current densities obtained when both, the interface trap density of states and the surface roughness are reduced by a factor of 10 each. Compare these current densities to the ones shown in Figures 5.11 and 5.19. A combined reduction in both interface trap density and surface roughness gives a much more significant performance enhancement, than each individual reduction. This is very evident in Figure 5.24, which shows the currents obtained when the interface trap density and the surface roughness are reduced by a factor of 10, individually, and in combination.

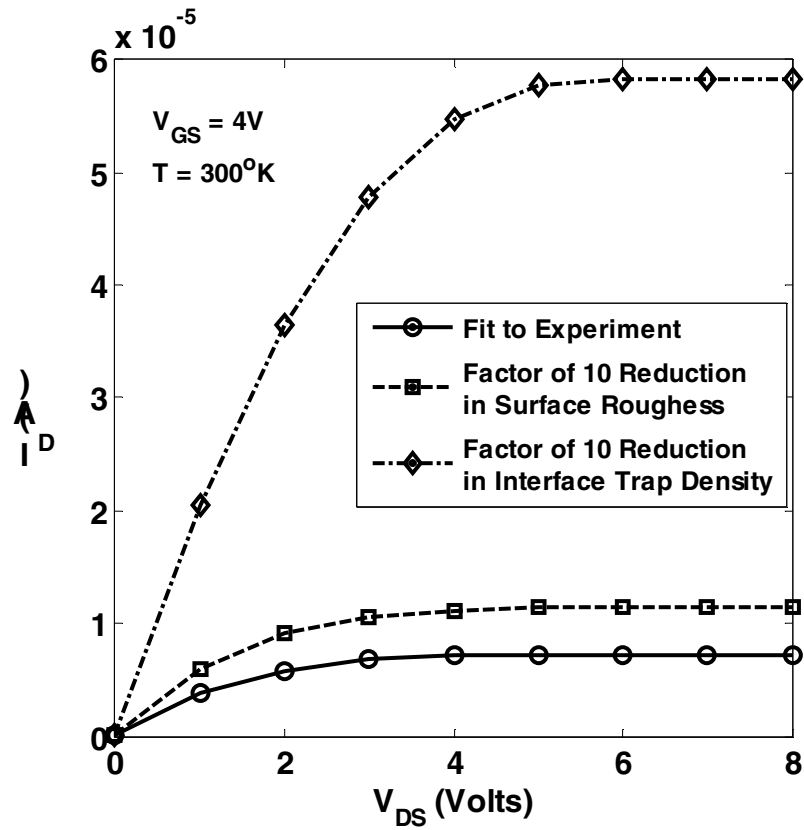


Figure 5.22. Comparison of the improvement in currents due to reduction in surface roughness, and the reduction in interface trap density of states, at a gate-source voltage of 4V. As Coulomb scattering dominates the total mobility at low gate voltages, reduction of interface trap density of states has a much higher effect on the current than the reduction in surface roughness, at $V_g = 4V$.

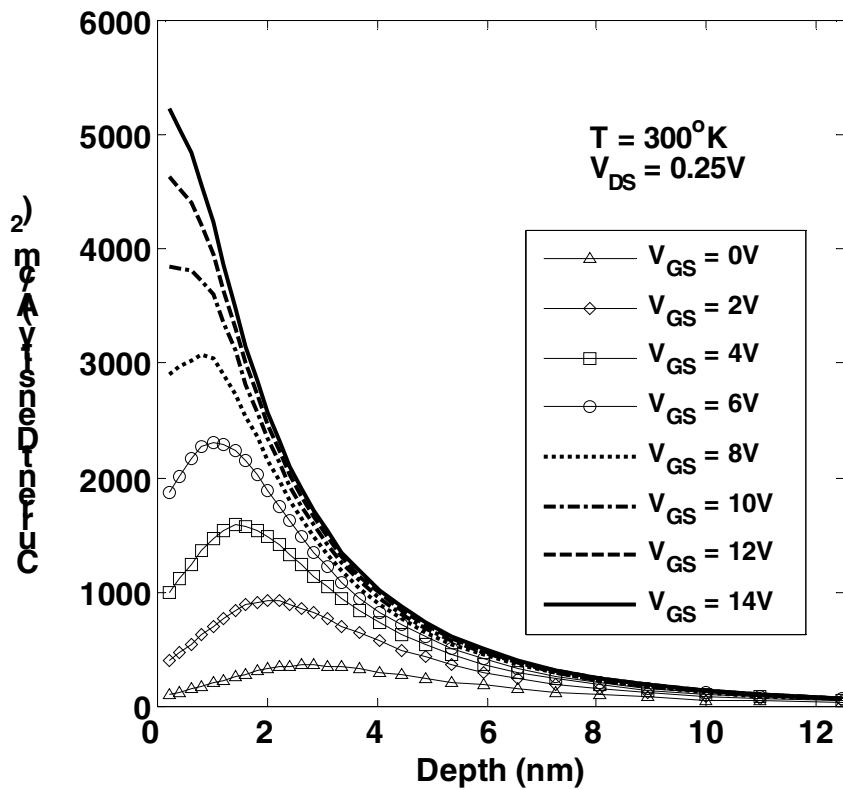


Figure 5.23. Current density variation with depth at the center of the channel in a 4H-SiC MOSFET, after reduction in the density of interface states at the band edge, and a reduction in the surface roughness, by a factor of 10 each. Compare the current densities obtained at higher gate voltages to the ones shown in Figures 5.19 and 5.11. The current densities near the surface rise up sharply at higher gate voltages because surface roughness scattering, and Coulomb scattering due to interface traps, are both high at large gate voltages. The rise is as much at lower gate voltages, because surface roughness does not play much role at low gate voltages.

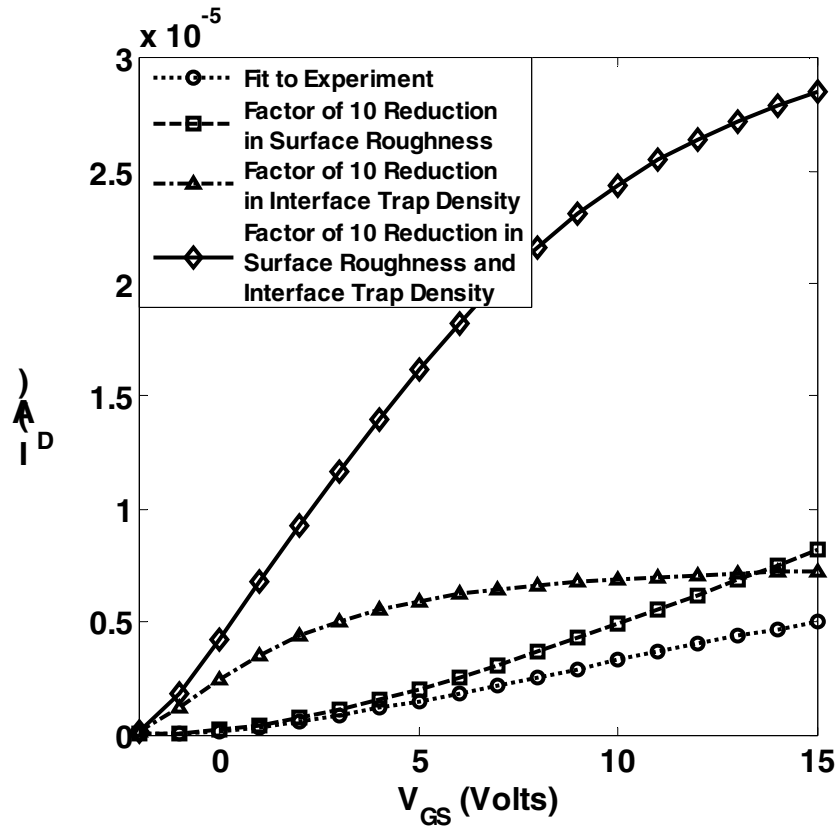


Figure 5.24. Drain current versus gate-source voltage at room temperature, with the surface roughness and the interface trap density of states reduced by a factor of 10 each. Notice how significant is the rise in current at higher gate voltages as compared to the cases when either one of two degrading mechanisms is improved.

5.4. Future Work

In this work I have developed a robust Coulomb scattering mobility model that describes the physics of the inversion layer in 4H SiC MOSFETs in great detail. So far, I have used this model to extract parameters for room temperature simulation. The next step will be to evaluate the performance of the model at higher temperatures by carrying out high temperature simulations and comparing the results to experiments. Also, the simulations have been carried out for steady state. Now, transient simulations with proper models should be designed and implemented. SiC MOSFETs are to be used as high power devices. High power devices have different structures so that they can be operated at very high voltages without causing breakdown of the materials. Hence, rather than just simple MOSFET structures, simulation of DMOSFET, UMOSFET and VMOSFET structures should be carried out.

I would like to thank all of you who have taken the time to read my thesis. I hope this work was somewhat informative and interesting to you.

REFERENCES

- [1] Yu (Anne) Zeng, Amela Softic, and Marvin H. White, "Characterization of Interface Traps in Subthreshold Regions of Implanted 6H- and 4H-SiC MOSFETs", International Semiconductor Device Research Symposium 2001, p. 213-215 (2001)
- [2] Charles J. Scozzie, and James M. McGarrity, "Effects of Interface-Trapped Charge on the SiC MOSFET Characteristics", Proceedings: 4th International High Temperature Electrons Conference, p. 23 (1998)
- [3] Emil Arnold, and Dev Alok, "Effect of Interface States on Electron Transport in 4H-SiC Inversion Layers", IEEE Trans. on Electron Devices, **48**, p. 1870 (2001)
- [4] N. S. Saks, and A. K. Agarwal, "Hall mobility and free electron density at the SiC/SiO₂ interface in 4H-SiC", Appl. Phys. Letters, **77**, p. 3281 (2000)
- [5] S. Harada, R. Kosugi, J. Senzaki, W. Cho, K. Fukuda, K. Arai, and S. Suzuki, "Relationship between channel mobility and interface state density in SiC metal-oxide-semiconductor field-effect transistor", J. Appl. Phys., **91**, p. 1568 (2002)
- [6] S. Suzuki, S. Harada, R. Kosugi, J. Senzaki, W. Cho, and K. Fukuda, "Correlation between channel mobility and shallow interface traps in SiC metal-oxide-semiconductor field-effect transistors", J. Appl. Phys., **92**, p. 6230 (2002)
- [7] E. Dubaric, M. Hjelm, H-E. Nilsson, C. S. Petersson, and P. Käckell, "The Effect of Different Transport Models in Simulations of a 4H-SiC Ultra Short Channel MOSFET", ICM '99: The Eleventh International Conference on Microelectronics, (1999)
- [8] Matthias Roschke, and Frank Schwierz, "Electron Mobility Models for 4H, 6H, and 3C SiC", IEEE Trans. on Electron Devices, **48**, p. 1442 (2001)
- [9] H-E. Nilsson, K. Bertilsson, M. Hjelm, and E. Dubaric, "Numerical Simulation of Field Effect Transistors in 4H- and 6H-SiC", J. of Wide Bandgap Materials, **9**, p. 293 (2002)

- [10] H-E. Nilsson, U. Sannemo, and C. S. Petersson, “Monte Carlo simulation of electron transport in 4H-SiC using a two-band model with multiple minima”, *J. Appl. Phys.*, **80**, p. 3365 (1996)
- [11] R. Mickevicius, and J. H. Zhao, “Monte Carlo study of electron transport in SiC”, *J. Appl. Phys.*, **83**, p. 3161 (1998)
- [12] J. B. Roldán, F. Gámiz, and J. A. López-Villanueva, “A Detailed Simulation Study of the Performance of β -Silicon Carbide MOSFETs and a Comparison with their Silicon Counterparts”, *Semiconductor Science and Technology*, **12**, p. 655 (1997)
- [13] V. R. Vathulya, and M. H. White, “Characterization of Inversion and Accumulation Layer Electron Transport in 4H and 6H-SiC MOSFETs on Implanted *p*-type Regions”, *IEEE Trans. on Electron Devices*, **47**, p. 2018 (2000)
- [14] S. K. Powell, N. Goldsman, C. J. Scozzie, A. Lelis, and J. M. McGarrity, “Self-Consistent Surface Mobility and Interface Charge Modeling in Conjunction with Experiment of 6H-SiC MOSFETs”, *International Semiconductor Device Research Symposium 2001*, p. 572-574A (2001)
- [15] S. K. Powell, N. Goldsman, J. M. McGarrity, J. Bernstein, C. J. Scozzie, and A. Lelis, “Physics-based numerical modeling and characterization of 6H-silicon-carbide metal-oxide-semiconductor field-effect-transistors”, *J. Appl. Phys.*, **92**, p. 4053 (2002)
- [16] R. Raghunathan, and B. J. Baliga, “Temperature Dependence of Hole Impact Ionization Coefficients in 4H and 6H-SiC”, *Solid-State Electronics*, **43**, p. 199 (1999)
- [17] N. A. Poklonski, S. A. Vyrko, V. I. Yatskevich, and A. A. Kocherzhenko, “A semiclassical approach to Coulomb scattering of conduction electrons on ionized impurities in nondegenerate semiconductors”, *J. Appl. Phys.*, **93**, p. 9749 (2003)
- [18] D. Chattopadhyay, and H. J. Queisser, “Electron scattering by ionized impurities in semiconductors”, *Rev. of Modern Physics*, **53**, p. 745 (1981)

- [19] T. Ando, A. B. Fowler, and F. Stern, “Electronic Properties of 2D systems”, Rev. of Modern Physics, **54**, p. 437 (1982)
- [20] C. T. Sah, T. H. Ning, and L. L. Tschopp, “The Scattering of Electrons by Surface Oxide Charges and By Lattice Vibrations at the Silicon-Silicon Dioxide Interface”, Surface Science, **32**, p. 561 (1972)
- [21] T. H. Ning, and C. T. Sah, “Theory of Scattering of Electrons in a Nondegenerate-Semiconductor-Surface Inversion Layer by Surface-Oxide Charges”, Physical Review B, **6**, p. 4605 (1972)
- [22] F. Gámiz, A. López-Villanueva, J. A. Jiménez-Tejada, I. Melchor, and A. Palma, “A comprehensive model for Coulomb scattering in inversion layers”, J. Appl. Phys., **75**, p. 924 (1994)
- [23] C. J. Scozzie, F. B. McLean, and J. M. McGarrity, “Modeling the temperature response of 4H silicon carbide junction field-effect transistors”, J. Appl. Phys., **81**, p. 7687 (1997)
- [24] M. N. Darwish, J. L. Lentz, M. R. Pinto, P. M. Zeitzoff, T. J. Krutsick, and H. A. Vuong, “An Improved Electron and Hole Mobility Model for General Purpose Device Simulation”, IEEE Trans. on Electron Devices, **44**, p. 1529 (1997)
- [25] G. Pennington, and N. Goldsman, “Self-consistent calculations for *n*-type hexagonal SiC inversion layers”, J. Appl. Phys., **95**, p. 4223 (2004)
- [26] H. Linewih, and S. Dimitrijević, “Channel-carrier Mobility Parameters for 4H SiC MOSFETs”, Proc. 23rd International Conference on Microelectronics (MIEL 2002), **2**, p. 425 (2002)
- [27] H. Iwata, K. M. Itoh, and G. Pensl, “Theory of the anisotropy of the electron Hall mobility in *n*-type 4H- and 6H-SiC”, J. Appl. Phys., **88**, p. 1956 (2000)
- [28] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, “A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices”, IEEE Trans. on Computer-Aided Design, **7**, p. 1164 (1988)

- [29] D. Caughey, and R. Thomas, "Carrier Mobilities in Silicon Empirically Related to Doping and Field", Proceedings of IEEE, **52** (1967)
- [30] W. Liang, N. Goldsman, I. Mayergoyz, P. J. Oldiges, "2-D MOSFET Modeling Including Surface Effects and Impact Ionization by Self-Consistent Solution of the Boltzmann, Poisson, and Hole-Continuity Equations", IEEE Trans. on Electron Devices, **44**, p. 257 (1997)
- [31] A. Hartstein, T. H. Ning, and A. B. Fowler, "Electron Scattering in Silicon Inversion Layers by Oxide and Surface Roughness", Surface Science, **58**, p. 178 (1976)
- [32] N. S. Saks, S. S. Mani, and A. K. Agarwal, "Interface trap profile near the band edges at the 4H-SiC/SiO₂ interface", Appl. Physics Letters, **76**, p. 2250 (2000)
- [33] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, and H. Shiomi, "Interface properties in metal-oxide-semiconductor structures on n-type 4H-SiC (0338)", Applied Physics Letters, **81**, p. 4772 (2002)
- [34] G. Pensl, M. Bassler, F. Ciobanu, V. Afanasev, H. Yano, T. Kimoto, and H. Matsunami, "Traps at the SiC/SiO₂ Interface", Mat. Res. Soc. Symp. Proc., **640**, H3.2.1 (2001)