ABSTRACT

Title of dissertation: MULTI-TERMINAL JOSEPHSON EFFECT

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Conventionally, a Josephson junction is an ubiquitous quantum device formed by a weak link between a pair of superconductors. In this work, we demonstrate the dc Josephson effect in mesoscopic junctions of more than two superconducting terminals. We report fabrication and characterization of the 3- and 4-terminal Josephson junctions built in a top-down fashion from hybrid semiconductor-superconductor InAs/Al epitaxial heterostructures. In general, the critical current of an N-terminal junction is an $(N-1)$-dimensional hypersurface in the space of bias currents, which can be reduced to a set of critical current contours (CCCs). The CCC is a key ground state characteristic of a multi-terminal Josephson junction, which is readily available from regular electron transport measurements. We investigate nontrivial modifications of the CCC's geometry in response to electrical gating, magnetic field, and phase bias. All observed effects are described by the scattering formulation of the Josephson effect generalized to the case of $N > 2$. Our observations indicate superconducting phase coherence between all the terminals which establishes the Josephson effect in mesoscopic junctions of more than two superconductors. Such multi-terminal junctions could find their applications in a broad range of fields from topologically protected quantum computation to quantum metrology.

MULTI-TERMINAL JOSEPHSON EFFECT

by

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Chapter 1

Introduction

This dissertation experimentally investigates hybrid InAs/epi-Al multi-terminal Josephson junctions. A multi-terminal Josephson junction (JJ) [1] consists of $N > 2$ independent superconductors (terminals) coupled to each other through a normal scattering region (Fig. 1.1). In this case, the supercurrent I_j in terminal j becomes a multi-variable function of all the $N-1$ independent phase-differences $\phi_j - \phi_N$ (the N-th terminal can be assumed grounded). In theory, such a non-local coupling of supercurrents originates from the formation of Andreev bound states [2] (ABS), the wave-functions of which are nearly equally present in all of the terminals. The concept of multi-terminal Josephson junctions first appeared decades ago in the context of supercurrent transistors [3], direct-current flux transformers [4, 5], and superconducting qubits [6].

An increased interest in hybrid InAs/epi-Al multi-terminal junctions arose recently in the context of topological superconductivity. It was realized that braiding of Majorana fermions in topological superconductors [7–9] requires T-junctions of at least three or more terminals [10–12]. More recently, striking effects were predicted even for junctions of conventional superconductors. They include the strong breaking of Kramers degeneracy without a Zeeman field for $N = 3$ [13] and the emergence of Weyl node physics for $N = 4$ [14], among other ideas. However, there is still a lack of experimental studies of the multi-terminal junctions.

In this thesis work, we fabricate and experimentally study transport properties of the 3- and 4-terminal Josephson junctions of different geometries. To characterize a 3-terminal JJ, we introduce

a new concept of the Critical Current Contour (CCC). Similar to the 2-terminal junctions where the value of critical current separates superconducting and finite voltage states, the CCC defines all values of simultaneously allowed supercurrents between all terminals. Chapter 3 provides a detailed description of transport features of a 3-terminal JJ, which is necessary to build our intuition before moving to a more complicated case of a 4-terminal junction, described in chapter 4. In case of a 4-terminal junction, its superconducting state characteristics becomes a 3D object, which we name Critical Current Surface (CCS). To simplify the characterization of junctions with $N > 3$, we introduce a biasing technique that reduces CCS to a set of CCC, which adequately describes the junction's state.

We continue the characterization of the multi-terminal junctions by exploring the effect of the perpendicular magnetic field on the CCC's geometry. We show that nontrivial modifications to the CCC's shape can be very well described in terms of the Random Scattering Matrix theory. Further, we explore the role of a junction's geometry and the effect of top-gating. Depending on the geometry of superconducting terminals, the coupling between opposite terminals (and hence multi-terminal effect) can be hidden or enhanced, which will result in different types of CCC's shape. Based on the coupling strength that relates to the junction's geometry, we divide junctions into three categories: wide, intermediate, and narrow. Intermediate type of junction can be driven to the narrow regime by top-gating, which reveals in changes of CCC's shape and its response to the magnetic field.

The ultimate manifestation of superconducting phase coherence in the conventional Josephson effect is the flux modulation of the supercurrent in a SQUID. We demonstrate the multiterminal superconducting phase coherence of our junctions by fabricating a multiterminal superconducting quantum interference device, nicknamed "multi-SQUID" (Chapter 5). In multi-SQUID, two terminals of a 4-terminal junction are connected with a loop and pierced with magnetic flux. By grounding the loop and applying biasing currents to the other two terminals, we observe the dramatic modification of CCCs in response to the phase bias. We conclude that piercing magnetic flux through the scattering region and flux-biasing the loop of a multi-SQUID leads to similar in nature multi-terminal superconducting interference effects.

The next logical step of this research would be to explore multi-terminal ABS by a direct tunneling spectroscopy. Such experiments require the fabrication of reliable gate dielectric and the

formation of very fine top gates, which adds extra complexity to already challenging fabrication process of a mesoscopic multi-terminal JJ. For that reason, an important part of this thesis work includes the development of fabrication recipes, as well as description of corresponding challenges and their possible solutions (Chapter 2). A preliminary result of a conductance measurement of a 3-terminal junction opens up a new chapter in the study of hybrid multi-terminal JJs.

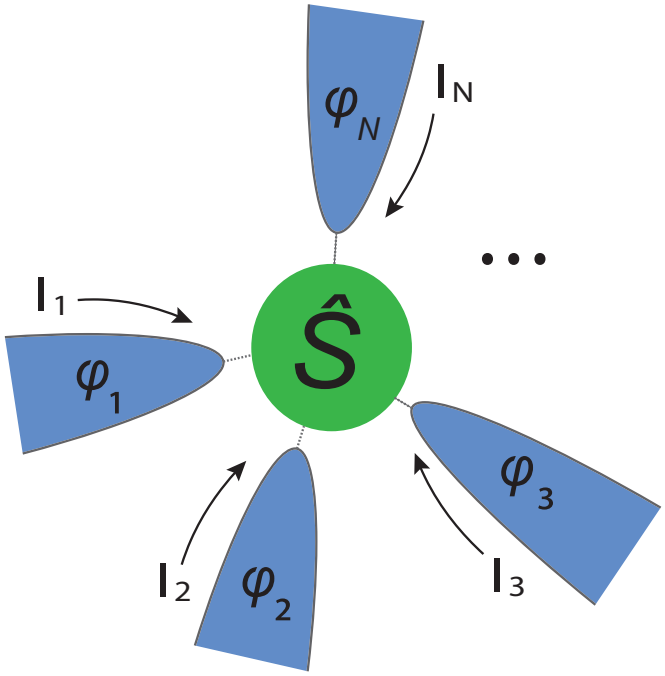

Figure 1.1: A junction of N superconducting terminals (blue) across a normal scattering region (green), which is characterized by the scattering matrix $\hat{S}$. Each terminal $j = 1, 2, ..., N$ has a superconducting phase ϕ_j and a supercurrent I_j.

1.1 Fundamental concepts

1.1.1 Josephson equations in the tunnel limit

Traditionally a Josephson junction is presented by a superconductor-insulator-superconductor system, where electrons tunnel from one superconducting terminal to another through a thin film of

oxide. Two basic equations originally derived for SIS junctions by Brian David Josephson are:

$$I_s = I_c \sin(\phi); \tag{1.1}$$

$$\dot{\phi} = 2eV/\hbar. \tag{1.2}$$

Where $\phi = \phi_1 - \phi_2$ is the phase difference between the two superconductors, e is an electron charge and $\hbar$ is the reduced Planck constant. I_c is the maximum supercurrent that junction can sustain while staying in the zero voltage regime [15].

When a supercurrent flows through a Josephson junction we can define energy stored in the junction. This energy associated with the phase difference ϕ across the Josephson junction:

$$E = E_J(1 - \cos\phi), \tag{1.3}$$

where $E_J = \Phi_o I_c/(2\pi)$ is the Josephson energy. This represents the energy stored in the junction in the superconducting state. This expression can be derived on the basis of simple thermodynamical arguments [16] or of microscopic theory [17]. In the thermodynamic derivation, the free energy change due to the work done by the current generator is: $dF_1 = IV_1dt$ and $dF_2 = IV_2dt$. As a consequence, the energy associated with the barrier itself is: $dF = dF_2 - dF_1 = I(V_2 - V_1)dt$. By using the general Josephson relations, we obtain the energy associated with the phase difference ϕ across the Josephson junction:

$$dF = \frac{\hbar}{2e} I_c \sin\phi d\phi. \tag{1.4}$$

By integration, free energy is:

$$F(\phi) = -\frac{\hbar}{2e} I_c \cos\phi + constant. \tag{1.5}$$

The constant is defined by imposing $F = 0$ for no current flow into the junction ($\phi = 2n\pi$ with $n = 0, 1, 2, ...$). In case of a N-terminal Josephson junction, the free energy becomes a function of $N - 1$ phase differences (one terminal assumed grounded).

1.1.2 Mesoscopic Josephson junctions

The universality of the Josephson equations makes them valid for all types of junctions although transport mechanism might be different. In case of hybrid InAs/Al junctions, where the role of the normal region performed by a semiconducting material, electrical transport can be described in terms of the scattering formalism, i.e. transport can be calculated under very general conditions, assuming that current is carried by the number of conducting channels, that could be defined by transmission probability [18]. But before discussing transport through hybrid SNS junction, let's first take a closer look at the building blocks separately.

We start by considering one of the main pillars of this work - InAs two-dimensional electron gas. The choice of material of the normal region plays a huge role in the properties of the Josephson junctions. The first advantage of the use of the semiconducting material is the potential ability to control the density of states in the junction. However, most of the intrinsic semiconductors behave like insulators at low temperatures that are required for superconductors [19]. Fortunately, some semiconductors exhibit significant surface conduction at low temperatures and InAs is one of them. Due to the Fermi level pinning into the conduction band InAs forms a natural layer of two-dimensional electron gas (2DEG) at the surface [20–22].

The proximity of conducting electrons to the surface on the other hand suffers from induced defects and hence lower mobility. To overcome the problem of defects, preserve high carrier concentration, and increase mobility the quantum well heterostructure could be engineered. By sandwiching a layer of InAs between two layers of InGaAs one can create a quantum well and confine electrons in a thin layer preserving high mobility. In this case 2DEG behavior can be modeled as a finite square quantum well [23] with the energy levels

$$E_n = \frac{\hbar^2}{2m^*}(\frac{n\pi}{w})^2 \tag{1.6}$$

where $\hbar$ is reduced Plank constant, m^* the effective mass, w the well width and n the band index. The Fermi wave vector and Fermi level could be defined by

$$k_F = \sqrt{2\pi n} \quad and \quad E_F = \frac{\hbar^2 k_F^2}{2m^*} \tag{1.7}$$

correspondingly, where n is a carrier concentration.

A few most important parameters used to quantitatively characterize 2DEG are Fermi velocity

$$v_F = \frac{\hbar k_F}{m^*} \tag{1.8}$$

and Fermi wavelength

$$\lambda_F = 2\pi/k_F \tag{1.9}$$

The average time that electron can travel between scattering events is denoted by τ. Typically it is given by the electron mobility $\mu = \frac{e\tau}{m^*}$ in 2DEG. This way, the average length that electron can travel without undergoing elastic scattering is given by mean free path

$$l_e = \tau v_F = \frac{\hbar\mu}{e}\sqrt{2\pi n}, \tag{1.10}$$

Design of the hybrid multi-terminal junctions must take into account electron coherence length to ensure the superconductivity will be induced over the whole length of the junction and between all terminals.

1.1.3 Andreev reflection

It is time to consider the underlying principle of electron transport in SNS junction. First, consider an interface between a normal conductor and a superconductor with a superconducting gap Δ. The gap is spatially dependent and vanishes in the normal regions faraway from the interface. An electron incident on the interface from the normal side with energy $E > \Delta$ can enter the superconductor, being converted into a quasiparticle with the same energy. If $E < \Delta$, the electron cannot be converted since quasiparticles are forbidden below the gap. A charge transfer may proceed instead: the electron can be retroreflected back as a hole and the $2e$ charge deficit in the metal implies that a Cooper pair with charge $2e$ is added to the superconductor. This process, illustrated in Fig.1.2, transfers the charge from the normal conductor side to the superconductor side called Andreev reflection. The momentum of the reflected hole is almost the same as that of the incident electron, since $k = k_F \pm E/\hbar v_F$ for electron and hole respectively, and $|E| \ll E_F$.

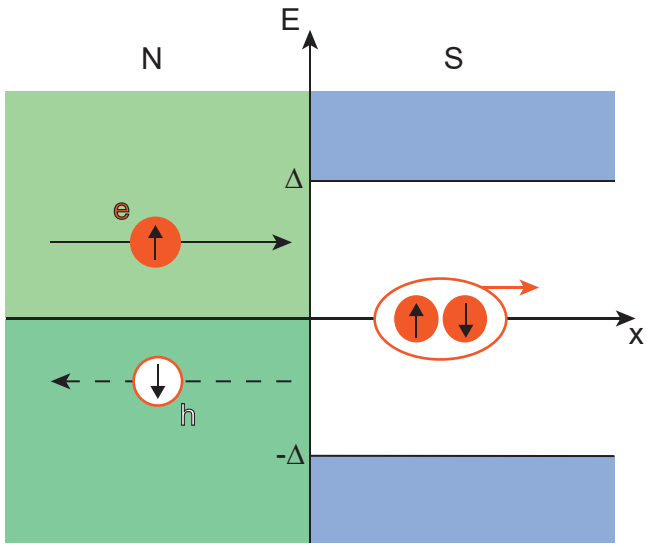

Figure 1.2: Energy space schematics of Andreev reflection process. An electron coming from the normal (N) conductor side to the superconducting (S) side is retro reflected as a hole with the same energy. A charge transfer occurs, which creates a Cooper pair in the superconductor.

Taking into account boundary conditions for the wave function at the interface, we can define Andreev reflection amplitude

$$r_A(E) = e^{-i\phi}\left(\frac{E}{\Delta} - i\frac{\sqrt{\Delta^2 - E^2}}{\Delta}\right). \tag{1.11}$$

Defining $\chi = -\arccos(E/\Delta) - \phi$, we can write $r_A = e^{i\chi}$. The electron is reflected as a hole with probability $|r_A|^2 = 1$. The outgoing hole has its phase shifted by χ with respect to the original electron. Similarly the other process where a hole is Andreev reflected as an electron results in a phase shift $\chi' = -\arccos(E/\Delta) + \phi$.

In a more general case, the interface has a non-unity transmission probability ($\tau < 1$). The process now includes a scattering matrix $s(E)$ defined for a single channel in the normal regime as

$$s = \begin{pmatrix} \sqrt{R}e^{i\theta} & \sqrt{T}e^{i\eta} \\ \sqrt{T}e^{i\eta} & -\sqrt{R}e^{i(2\eta-\theta)} \end{pmatrix}, \tag{1.12}$$

where R and T are reflection and transmission probability, and the phases θ and η are assigned as to satisfy the unitary condition $s^\dagger s = 1$. For electrons with energy $E > 0$, we can assign $s_e(E) = s(E)$. For holes obeying time-reverse Hamiltonian, and with opposite momentum, we can write $s_h(E) = s^\star(-E)$.

The transport through nanostructure may involve many processes with an electron making different trips to and from the interface. For example, the process with an electron transmitted through the nanostructure with probability amplitude t_e, Andreev-reflected as a hole from the superconductor with phase shift factor $e^{i\chi}$, then transmitted as a hole through the nanostructure again with probability amplitude t'_h results in the total Andreev reflection amplitude $r_{A0} = t_e t'_h e^{i\chi}$. More complicated process of order n can be generally written as $r_{An} = r_{A0}(r_h e^{i\chi'} r'_e e^{i\chi})^n$. Summing them up and using geometric series identity, we obtain the total probability amplitude of Andreev reflection:

$$r_{Atotal} = \sum_{n=0}^{\infty} r_{An} = \frac{t_e t'_h e^{i\chi}}{1 - r'_e r'_h e^{i\chi}} \tag{1.13}$$

In the limit $E \ll \Delta$, we can approximate $\chi + \chi' = -2\arccos(E/\Delta) \approx -\pi$. A typical nanostructure has equal probability amplitudes on both sides for both type or particles, so $t'_{e,h} = t_{e,h} = t$ and $r'_{e,h} = r_{e,h} = r$. The transmission and reflection coefficients are subsequently defined as $T = t^2$ and $R = r^2$, respectively. Using the condition $R^2 + T^2 = 1$, we can derive the Andreev reflection coefficient $R_A = |r_A|^2$:

$$R_A = \frac{T^2}{(2-T)^2}. \tag{1.14}$$

In the case of an interface with unity transmission probability, $T = 1$, we arrive at the result $R_A = 1$. In the tunneling limit where $T \ll 1$, we have $R_A \approx T^2/4$. This 2nd order dependence reflects the fact that Andreev reflection requires two transmission events: one of an electron and one of a hole.

1.1.4 Andreev bound states

Consider a Josephson junction which consists of a semiconductor placed between two superconductors. These superconductors have gaps with the same amplitude but different phases. The semiconducting region under consideration is short, such that the electrons and holes spend a short time

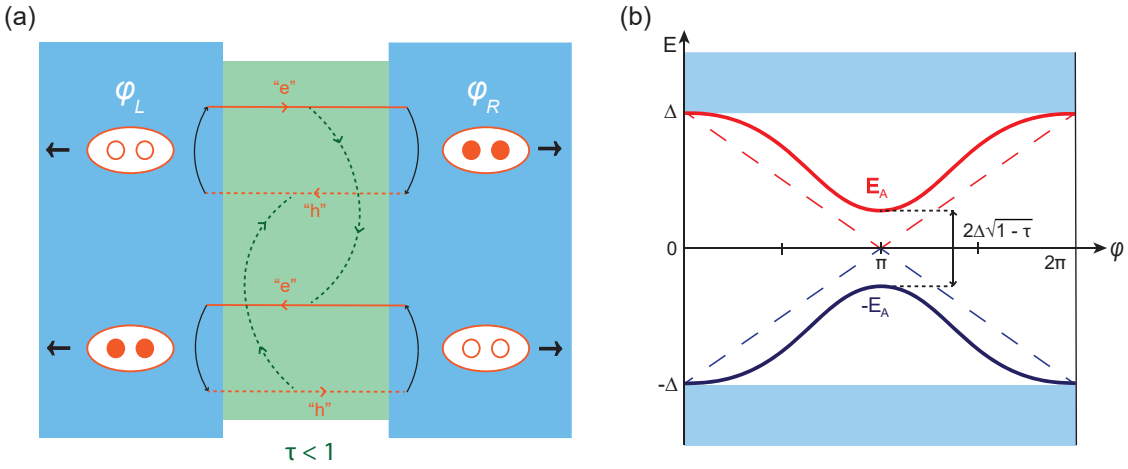

Figure 1.3: (a) A scheme presenting two one-particle ABS in the junction with imperfect transparency ($\tau < 0$). Solid lines correspond to the Andreev reflection process when right-moving electron (left-moving hole) is retroreflected as left-moving hole (right-moving electron). In case of imperfect transparency of the channel normal reflection might accrue, shown with green dotted lines. (b) ABS energy spectrum as a function of the phase difference between superconducting terminals. Transparency of the junction will affect the separation between levels, case of $\tau = 1$ shown by dashed lines. The normal reflections introduce coupling between Andreev levels. Note that energy levels are spin degenerate.

in it and superconductivity has no effect on them. An electron or hole with sufficiently low energy is reflected back and forth between the superconductors. This motion gives rise to discrete energy states: the Andreev bound states. This is in a way analogous to resonances occurring in Fabry-Perot optical cavities where laser lights also travel back and forth between the mirrors.

Such a process is described qualitatively in Fig.1.3. A semiconductor (green) is placed between two superconductors (blue) with different phases: left one has phase φ_L, right one has phase φ_R. An electron incident on the right superconductor is represented as a solid red line. It is Andreev-reflected (black line) as a hole (dotted red line). This hole is subsequently Andreev-reflected from the left superconductor as an electron moving right again. The same process also occurs for a hole incoming to the right (lower loop). Additionally, these electron and hole can be normally reflected (green dashed line), respectively, due to the finite reflection coefficient of the interfaces. These normal reflections couple the two processes (top and bottom loops).

The energy of the discrete bound state can be calculated using the scattering matrix approach as follows. Let the amplitudes of outgoing states in the nanostructure be b_{Le}, b_{Re}, b_{Lh}, b_{Le} and those

of incoming states be a_{Le}, a_{Re}, a_{Lh}, a_{Le}. Using scatter matrix s for a single channel, as defined in Eqn.1.12, and spinor notation, we can write

$$\begin{pmatrix} b_e \\ b_h \end{pmatrix} = \begin{pmatrix} s & 0 \\ 0 & s^\star \end{pmatrix} \begin{pmatrix} a_e \\ a_h \end{pmatrix}, \tag{1.15}$$

where

$$b_e = \begin{pmatrix} b_{Le} \\ b_{Re} \end{pmatrix}; \qquad b_h = \begin{pmatrix} b_{Lh} \\ b_{Rh} \end{pmatrix}; \qquad a_e = \begin{pmatrix} a_{Le} \\ a_{Re} \end{pmatrix}; \qquad a_h = \begin{pmatrix} a_{Lh} \\ a_{Rh} \end{pmatrix}$$

Andreev reflection from the superconductors converts electrons to holes and vice versa. Such a process can be described by defining the Andreev scattering matrices s_{eh} which converts holes to electrons, and s_{he} which converts electrons to holes.

$$s_{eh} = \begin{pmatrix} e^{i\chi'_L} & 0 \\ 0 & e^{i\chi'_R} \end{pmatrix}; \qquad s_{he} = \begin{pmatrix} e^{i\chi_L} & 0 \\ 0 & e^{i\chi_R} \end{pmatrix}, \tag{1.16}$$

and write the Andreev reflection equation for electrons and holes:

$$\begin{pmatrix} a_e \\ a_h \end{pmatrix} = \begin{pmatrix} 0 & s_{eh} \\ s_{he} & 0^\star \end{pmatrix} \begin{pmatrix} b_e \\ b_h \end{pmatrix}. \tag{1.17}$$

The Andreev reflection phase shifts are again given as $\chi_{L,R} = -\phi_{L,R} - \arccos(E/\Delta)$, $\chi'_{L,R} = \phi_{L,R} - \arccos(E/\Delta)$ for the left and right superconductors.

Eqn.1.15 and Eqn.1.17 can be combined to give an eigenvalue equation containing a 4x4 matrix Π:

$$\begin{pmatrix} b_e \\ b_h \end{pmatrix} = \begin{pmatrix} s & 0 \\ 0 & s^\star \end{pmatrix} \begin{pmatrix} 0 & s_{eh} \\ s_{he} & 0 \end{pmatrix} \begin{pmatrix} b_e \\ b_h \end{pmatrix} = \Pi \begin{pmatrix} b_e \\ b_h \end{pmatrix} \tag{1.18}$$

The solution exist only if $\det(\Pi - 1) = 0$. This can be solved to give the energy of the bound

state:

$$E_A = \sqrt{1 - \tau \sin^2(\varphi/2)} \tag{1.19}$$

where τ is the transmission probability of the semiconducting region, and $\varphi = \phi_L - \phi_R$ is the phase difference across the junction [24] [25] [26]. This way, the energy of ABS depends on phase difference and transmission coefficient. At $\varphi = 0$ and 2π the ABS merge to continuum states. Other than at these points ABS are localized at the weak link in contrast with continuum states that are delocalized and propagating. In fact, ABS originates from the twist of phase around the weak link region and at perfect transmission $\tau = 1$ will form a "ballistic ABS". A finite transmission is a result of normal reflection process that is inelastic scattering of impurities inside normal region, which happens in addition to Andreev reflection. Normal reflection couples two reflectionless states (shown in green arrows in Fig. 1.3 (a)), which opens a gap $2\Delta\sqrt{1-\tau}$ at $\varphi = \pi$ (Fig. 1.3 (b)).

In case of a multi-terminal junction, the Andreev bound states are formed between all the terminals. The energy of such multi-terminal ABS becomes a function of multiple phase differences, and its wave function is nearly equally present in all superconducting leads. The latter fact results in simultaneous superconducting phase coherence between multiple terminals.

Recently, the physics of multi-terminal ABS became the subject of numerous theoretical proposals [10,11,13,14,27–52]. The first category of proposals explore the band topology of multiterminal Josephson junctions [13, 14, 27–39]. These papers explore the structure of the ABS energies in the $(N-1)$ dimensional Brillouin zone, where the phase differences $\phi_j - \phi_N$ play a role of quasi-momenta. Theoretical studies of such multi-terminal junctions predicted band structures with topologically protected states [14,28–31] and Weyl nodes [32–35]. In the second category of theoretical proposals, a junction of more than two topological superconductors is used to perform braiding operations on the zero-energy Majorana bound states [10, 11, 40–52] as these operations are essential for the realization of topologically protected quantum computation [53]. The demonstration of coherent transport in multi-terminal Josephson junctions is an important stepping stone for bringing these numerous theoretical proposals to fruition.

1.1.5 Multiple Andreev reflections

When traveling through the voltage-biased junction, electrons and holes gain or lose an energy eV. The current does not depend on the spatial distribution of the voltage [26] , so we can assume that the voltage drops over an arbitrary point of the channel (shown by magenta-colored dashed line on Fig.1.4). Let us consider a quasiparticle of energy E coming from the lower band of the left superconductor with the energy E slightly bellow $-\Delta$ (Fig.1.4 (a)). After crossing voltage drop line it arrives at the right electrode with energy $E + eV$. If $E + eV > \Delta$ the quasiparticle may leave the junction entering available states above Δ. Alternatively, the quasiparticle might be Andreev-reflected at the right terminal (Fig.1.4 (b)), then electron will be converted into hole and vise versa. The hole will start moving backwards and will also cross voltage drop line and increase its energy by $E+2eV$. It will escape to the left electrode and the total charge transfer will equals $2e$. Since the probabilities of Andreev reflections rapidly decrease with increasing energy (Eqn.1.11), the probabilities of charge transfer via Andreev reflection at higher energies are small.

Situation is different for the small voltages ($eV \ll \Delta$). Now, for the quasiparticle coming from the bottom left band, there are no available states within Δ and the quasiparticle must undergo Andreev reflection. More precisely, an electron (hole) will undergo n even (odd) Andreev reflections and reach the higher band of the right (left) superconductor where it recombines into a quasiparticle. This process is called the *multiple Andreev reflection* (MAR) of order n+1. The minimum number of Andreev reflections for a quasiparticle of energy E under the voltage bias V is given by

$$n(E, V) = \frac{\Delta - E}{eV} \tag{1.20}$$

If we neglect the continuum and assume the quasiparticles are extracted at the energy $E = -\Delta$ from the left electrode, the MAR process will take simpler form

$$n(V) = \frac{2\Delta}{eV} \tag{1.21}$$

where n is the order of MAR. Let us consider a MAR process of order 3 shown in Fig.1.4 (d). A quasiparticle of energy E from lower left band is ejected as an electron in the normal region. It reaches right terminal at energy bellow the gap and undergoes the Andreev reflection, so now the

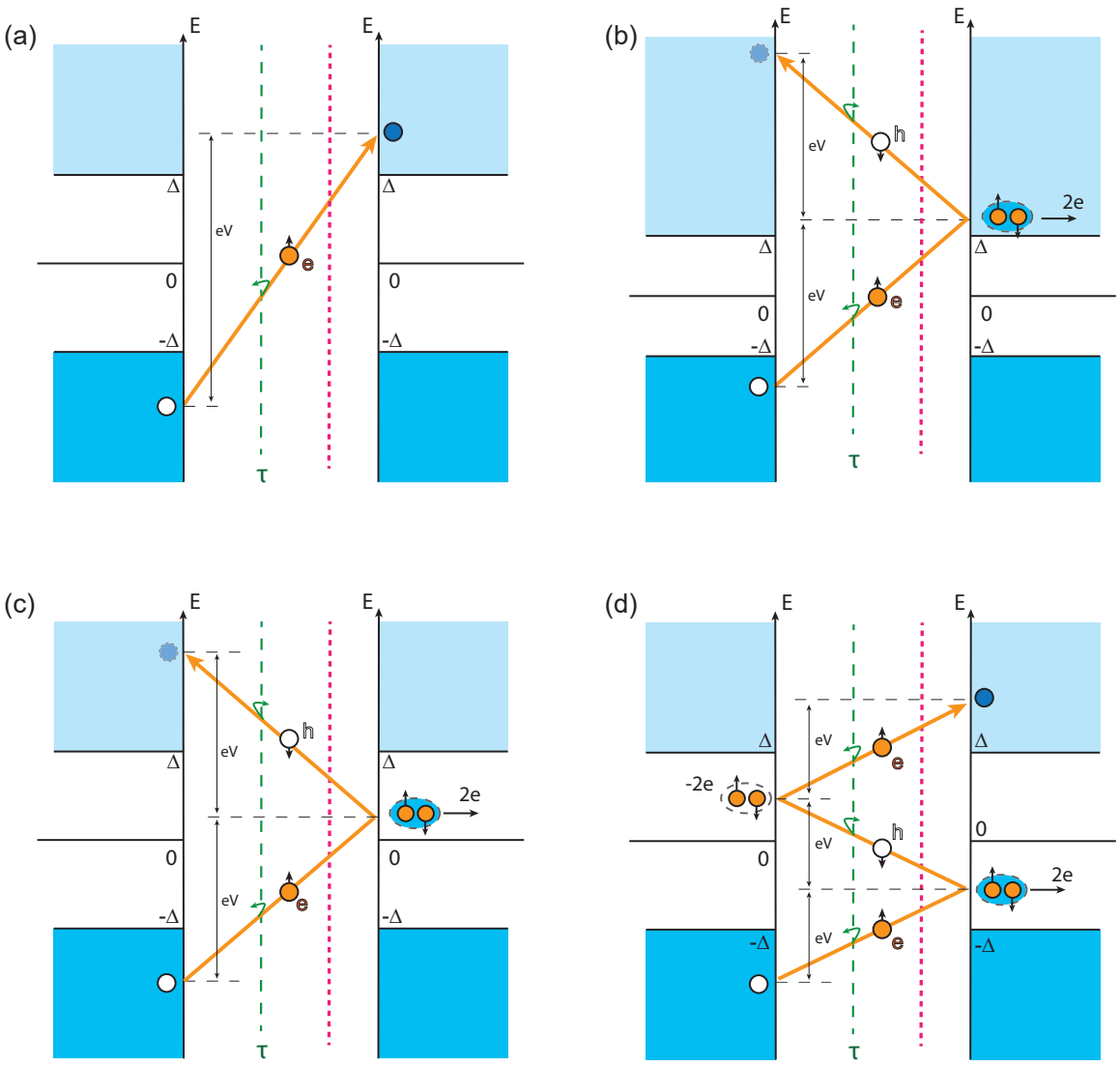

Figure 1.4: Mechanisms of charge transfer in a voltage-biased Josephson junction with finite transmission coefficient $\tau < 1$. Electrons (holes) acquire energy eV due to the voltage difference between superconducting terminals, schematically shown by magenta-colored dashed line (energy eV acquired when crossing dashed line from the left (right)). (a) When $eV > 2\Delta$ a quasiparticle can be transferred from left to right in one shot. (b) It may also be Andreev-reflected and get to the left at a higher energy. When $eV \ll \Delta$ multiple Andreev reflections (MARs) are required for charge transfer. (c) MAR process of order 2. (d) MAR process of order 3.

hole is traveling to the left. Upon arrival the energy of the hole is still lower than Δ, so it also being Andreev-reflected as backward moving electron. Once the energy of the electron (hole) above the gap, it can exit normal region at the right (left) upper band. Importantly after *each* Andreev reflection, a Copper pair is created on the right or annihilated on the left (shown by filled or empty ellipse in Fig.1.4 (d)). That will be reflected as resonances (peaks or deeps) in dV/dI characteristics of the Josephson junction. Processes shown in Fig.1.4 (a,b) will not create such resonances in dV/dI characteristics.

The MAR process of order n results in charge transfer of ne. Additionally, due to the finite probability of transmission electrons and holes might be normally reflected, which is shown by green curved arrows on Fig.1.4. In case when junction supports several transport channels, the MAR process happens in each channel independently.

For the case of multi-terminal junctions one can expect MAR process happen between several terminals [54] assuming approximately equal coupling between all superconducting terminals. On the other hand, for the junction of Y- or X-shape geometry the 2-terminal coupling between adjoint terminal is strong due to the large shared interface. This way, one can expect to see a set of MAR resonances for each pair of terminals, i.e. three sets for the 3-terminal junction and six sets for the 4-terminal junction.

1.1.6 Random scattering matrix theory for multi-terminal hybrid junctions

Treatment of mesoscopic systems poses a big challenge since on one hand electron transport obeys rules of quantum mechanics and must be described using tools of quantum mechanics, but on the other hand, mesoscopic systems are too large and models must take into account too many parameters to describe transport properties of the system properly. In many cases, the complexity of the system makes it impossible to accurately calculate properties, so a statistical approach is taken instead. This way one considers an average over an ensemble of macroscopically equivalent, but microscopically different samples. In other words, in cases when it's impossible to describe the system in detail, one can look at the corresponding system as "black boxes" and adopt methods of statistical description.

A powerful tool of Random Scattering Matrix (RSM) theory was developed to describe quantum

transport of mesoscopic systems. RSM is especially useful for the case of N-terminal semiconducting-superconducting junctions since an increasing number of terminals, large number of channels, random impurities and a few other variables make modeling of multi-terminal junctions extremely complicated. The use of RSM allows precise modeling of supercurrents in the absence of microscopic details.

The junction's CCC can be obtained numerically in the framework of RSM using the following procedure. Let's consider a model of a general N-terminal Josephson junction (Fig. 1.1) with the terminals characterized by the uniform gap Δ and phases ϕ_j, $j = 1, ..., N$ and with the exposed semiconductor junction region characterized by a multi-channel energy-independent scattering matrix $\hat{S}$. The scattering matrix is generated randomly, and it is assumed to belong to one of the ensembles of random unitary matrices, restricted only by the system's fundamental symmetries. Three ensembles with different scattering symmetry classes are known: circular orthogonal ensemble (COE), which respects both spin-rotation and time-reversal symmetry; circular unitary ensemble (CUE), describing broken time-reversal symmetry, and circular symplectic ensemble (CSE), respecting time-reversal symmetry but not spin-rotation symmetry [55].

The main characteristics of the junction can be derived from the spectrum of the supercurrent-carrying ABS, whose energy E_n^A, $n = 1, 2, ...$ is given by the Beenakker's determinant equation [13, 56, 57]:

$$\det[1 - \exp\left(-2i \arccos(E/\Delta)\right) \hat{r}\hat{S}^* \hat{r}^* \hat{S}] = 0. \tag{1.22}$$

Here $\hat{S}$ is the junction's normal scattering matrix, E is the ABS energy, Δ is the superconducting gap in the terminals, and the matrix $\hat{r} = \exp(i \times \mathrm{diag}[\phi_1, \phi_2, ..., \phi_N])$ incorporates the superconducting phases ϕ_j of all the terminals. In case of a time-reversal symmetry, $\hat{S}$ must be orthogonal. The ground state energy of the junction E_g and the supercurrents I_j ($j = 1, ..., N$) are given by

$$E_g = -(1/2) \sum_n E_n^A; \;\; I_j = \partial E_g / \partial \phi_j (2e/\hbar), \tag{1.23}$$

where the sum in the former equation runs overall positive ABS. The effect of extended phase-sensitive states can be neglected.

In case of a N-terminal Josephson junction, the ground state energy E_g is a function of $N-1$ phase differences. When the junction is driven with bias currents I_1, ... I_{N-1}, the free energy F is given by

$$F(\phi_1, ..., \phi_{N-1}) = E_g(\phi_1, ..., \phi_{N-1}) - \frac{\hbar}{2e} \sum_{i=1}^{N-1} I_i \phi_i, \tag{1.24}$$

For the junction to be in the zero-voltage state, there should exist a stable equilibrium position of the free energy. It requires both ∇F=0 and the positiveness of the Hessian eigenvalues. Then, the CCC is obtained from a boundary of allowed bias currents $I_1, \ldots, I_{N1}$.

This is the $(N-1)$-dimensional tilted washboard potential problem, which is used in general to describe the current-biased Josephson junctions. Unlike calculating the critical current of 2-terminal Josephson junctions, the second-derivatives of the free energy need to be investigated to construct the zero-voltage region in the multi-terminal Josephson junctions.

For $N = 3$ devices, the physically allowed non-dissipative currents can be obtained by sweeping the variables ϕ_1 and ϕ_2.The boundary of the resulting simply-connected shape defines a 2D contour of possible critical current pairs $\{I_1^c, I_2^c\}$ - the critical current contour. For $N = 4$ case, a pairwise balanced current bias can be used without an explicit grounding. In this case it is more convenient to formally keep a four-variable Josephson energy but impose a constraint $I_i = -I_j = I_{ij}$ on the currents. Under such symmetric bias conditions, the critical current of a 4-terminal junction is also a set of three 2D contours $\{I_{13}^c, I_{24}^c\}$, $\{I_{12}^c, I_{34}^c\}$, and $\{I_{23}^c, I_{41}^c\}$.

Modeling of multi-terminal junctions with RSM is independent of the detail and could be generalized to the majority of the systems sharing corresponding symmetries. We expect that our measurements (presented in Chapter 3 and Chapter 4) and analysis would guide the basic characterization of any other physical implementation of coherent multi-terminal Josephson junctions.

1.1.7 Multi-terminal JJs as a topological matter

The race of quantum technologies is getting more and more momenta over the past years since more and more people recognize the potential of this area. History knows quite a few examples of how

scientific discoveries could change the world. One of the most prominent examples is nuclear technologies: what started as a regular experiment in the lab ended up changing the power distribution of the whole world for many decades.

There are a few leading approaches to implement quantum computers: quantum dots, trapped ions, and superconducting qubits. However, most of them share the same weakness of decoherence, the inability to store quantum information for sufficiently long times poses a serious limitation for stable development. A possible solution to the decoherence problem came from the emerging field of topological physics. It's been proposed that topology can protect quantum information from decoherence under certain conditions. The foundational theory was proposed to detect topological states in exotic systems like p-wave superconductors, which are extremely hard to work with. Fortunately, the same theory provides us with the ingredients needed to engineer the topological state of matter: induced superconductivity (to ensure particle-hole symmetry and create symmetric spectrum), strong spin-orbit interaction and magnetic field (to break time-reversal symmetry (TRS) and lift Kramers degeneracy of the electron levels). Moreover, those ingredients could be brought together in a simple multi-component system consisting of s-wave superconductor, such as aluminum, semiconductor with strong spin-orbit interaction, such as InAs, and magnetic field is an old friend of experimental physicists, so it should not be a problem, right? Not quite. The main constraint posed on the magnetic field in terms of achieving a topological state is that it must be aligned perpendicular to the spin-orbit field, i.e. along the current direction. This could be done to initialize topological state in 1D systems like nanowires [58], but will pose a problem for performing unitary operations since they must take place in 2D space. There are a few proposals aiming to overcome this limitation, like the use of ferromagnetic materials [59], but one stands out.

The main motivation for our work was an elegant theoretical proposal suggesting that lifting of Kramers degeneracy and breaking of time-reversal symmetry can be done by means of the multiple superconducting phase differences instead of conventional magnetic field [13]. While the use of phase difference as a source of TRS breaking is ineffective in short 2-terminal Josephson junctions due to negligibly small splitting of the energy levels, this limitation can be resolved by the addition of an extra superconducting terminal. In case of multi-terminal junction, the effect of TRS breaking by superconducting phase differences alone leads to large splitting of the Kramers doublets comparable

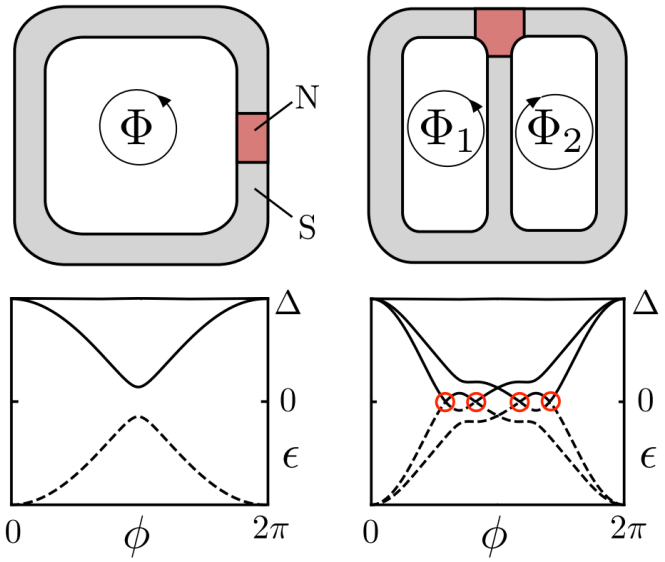

Figure 1.5: Figure adapted from Ref [13]. Comparison of a 2-terminal junction vs 3-terminal junction configuration and corresponding ABS spectra. A superconducting ring (grey) allows one to concentrate the effect of a magnetic flux Φ on the small area of a Josephson junction (red). Bottom left: The junction has subgap Andreev levels whose energy depends on the phase difference $2e\Phi/\hbar = \phi$. Each level is doubly degenerate since in a short junction a finite phase difference does not induce a splitting of the Kramers degeneracy. Top right: Kramers degeneracy can be efficiently removed in a three-terminal junction, even in the absence of an external magnetic field. Bottom right: Andreev spectrum for $2e\Phi_1/\hbar = 2e\Phi_2/\hbar = \phi$. Both the splitting of Kramers degeneracy and Andreev level crossings at zero energy (marked by red circles) appear in the spectrum.

to the superconducting gap Δ. This way, multi-terminal Josephson junctions were predicted to be topologically nontrivial even if the superconducting leads are topologically trivial and no exotic materials are used to make the junction, i.e. the junction itself may be considered as an artificial topological material [14]. This could be achieved by bringing together a few key ingredients: 1) superconductivity to ensure symmetric spectrum; 2) strong spin-orbit interaction and multiple phase difference to lift spin degeneracy; 3) 2D geometry to enable manipulation operations. Moreover, N-terminal Josephson junctions may provide realizations of topology in $N-1$ dimensions since $N-1$ independent superconducting phases will play the role of bandstructure quasimomenta.

On the other hand, multi-terminal Josephson junctions are desirable for electric sensing and logic applications, they have been also attracting attention in the context of supercurrent transistors [3], direct-current flux transformers [4, 5], and superconducting qubits [6].

Chapter 2

Design, fabrication, and measurement techniques

This chapter describes the foundation of the experiment. Three main pillars that made this work possible are material, fabrication, and measurement set up. If any of the pillars fail, further work would not be possible. In fact, it took a long time to stabilize and align all three components.

2.1 Material

The material for the experiment was provided by marvelous Javad Shabani and his fantastic group. Here we present the main overview of the material and its properties, but will not go into the details regarding growth challenges, MBE process, and parameters extraction. Interested readers are welcome to study the following references [60–62].

The challenge of material development for proximity experiments as well for Majorana experiments is to achieve a good coupling between 2DEG and superconductor as well as good control of two-dimensional electrons. This goal was hardly achievable in previous years since the superconducting contacts were deposited after etching of the top semiconducting layers. Such a fabrication process creates multiple imperfections in the interface and hence negatively affects the properties of the device. A breakthrough in the materials came with the development of quantum well structures

with epitaxial superconducting contact that was grown *in situ*. The contact transparency for the devices based on such an epitaxial structure is close to unity. There are a few main characteristics that should be considered when designing a material system. First of all, it is essential to ensure a good coupling of 2DEG with the surface meaning the quantum well layer should be placed sufficiently close to the surface. On the other hand, it is important to preserve carrier mobility of the deep quantum wells. The optimal thickness of the top barrier preserves reasonable mobility and wave function overlap at the surface ensuring both: good proximity effect and fine gate tuning.

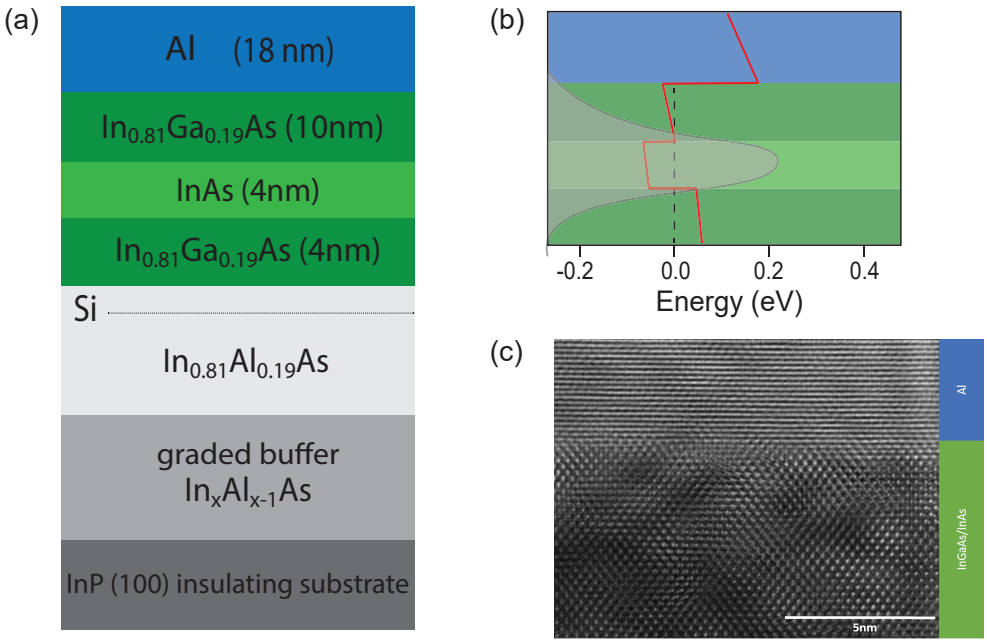

Figure 2.1: (a) Sketch of the material structure of 2DEG with epitaxial Al with exact parameters of JS127 wafer. (b) Conduction band level (red line) and 2DEG probability density (shaded gray) showing the wavefunction being focused in the InAs layer. (c) TEM image of an identical wafer.

The heterostructure wafer used for this thesis is presented in Fig. 2.1 (courtesy of J.Shabani). The sample was grown on semi-insulating InP (100) substrates. First, a step graded buffer layer of $In_xAl_{1-x}As$ is grown to compensate for lattice mismatch between the active region and InP substrate. The delta-doped Si layer is placed slightly below the surface of the buffer layer. Then the quantum well of 4 nm layer $In_{0.81}Ga_{0.19}As$, 4 nm layer InAs and 10 nm layer of $In_{0.81}Ga_{0.19}As$ is grown. After the quantum well is grown, the substrate is cooled to promote the growth of epitaxial Al [60]. At

the beginning of the project, we have tested several wafers with the quantum well of the same kind, but with a few growth differences. Among them, one, named JS127, was particularly good and all experimental data presented in this report was obtained using the JS127 wafer. The characterization of the 2DEG yielded an electron mobility of $\mu = 16000$ cm^2/Vs at a density of n $= 1.5e12$ cm^2 at zero gate.

2.2 Fabrication of devices

Nanofabrication must be ranked as an ultra-modern art. Gentle, but firm grip of the tweezers, creative design of devices, precise breath control during wire-bonding - these are just a few of the marvelous things the world of nanofabrication can offer you. The necessary ingredients for being successful with a fab are: the ability to strictly follow the recipe (if it already exists), the ability to pay attention to every detail to notice any deviations at early stages and fix them, and luck. Unfortunately (or fortunately?), we had a little luck during the last few years, so we had to compensate for it by numerous tries and errors, and eventually by experience. At the beginning of the chapter, we'll discuss the main techniques and tricks of nanofabrication in detail, and in the end, we provide a condensed recipe.

With the progress of the research, the fabrication recipe was also evolving from the 3-step process for the first devices (Fig. 2.2 (a)) to the 8-step process for conductance measurements at the final stages (Fig. 2.2 (b)). Here we present the final version of the recipe, it can be divided into steps:

0. Design and chip preparation.
1. Mesa etch.
2. Aluminum etch - open the gaps.
3. Aluminum contact pads deposition.
4. Gold probes deposition.
5. Oxide deposition.
6. Fine gates deposition.

7. Big gates deposition.
8. Wire-bonding and room-temperature testing.

A working horse of the nanofabrication process is of course an electron beam writer. All devices reported in this thesis were fabricated with the Elionix GLS-100 system, which is a 100 kV e-beam writer. Deposition of aluminum for the contact pads was done in the Plassys e-beam deposition system, while gold parts (both probes and gates) were deposited using several different e-beam deposition systems. Oxide deposition was a bottleneck of the research. In order to develop a stable recipe we experimented with several deposition methods and systems, this fascinating journey will be discussed in great detail later in the chapter.

2.2.1 Design

As mentioned before, it is very challenging to grow a material of desired properties and quality. Once we started to work with the JS127 wafer and confirmed its nice properties (i.e. superconductivity can be induced in the junctions with a channel length of $500 - 600$ nm), we tried our best to make our design as efficient as possible and were placing around 20 devices per chip. Later my colleague Hanho Lee modified the design of contact pads to further increase the packing density and we ended up putting 40-50 devices per chip. The before/after chip outline is shown in Fig. 2.3. The other side of the medal was that wire-bonding became proportionally more challenging, we compensated for it by hundreds of hours of practice and the ability to quickly achieve a trance state of mind.

One important thing to keep in mind is that for the first step of fabrication one will need to preserve a mask of resist on top of the future devices and open the area everywhere else. Typically when a bigger part of the chip needs to be opened while preserving the mask on the small areas, negative resist should be used. In case of negative resist one would only need to expose a small area of devices and keep the rest of the chip unexposed. At the very beginning we attempted to employ this approach experimenting with maN-2401 and maN-2405, however, encountered a range of problems. First of all, the shelf time of maN resists is only 6 months and when it's close to the expiration date it starts to behave unpredictably. Second, most of the commercially available maN

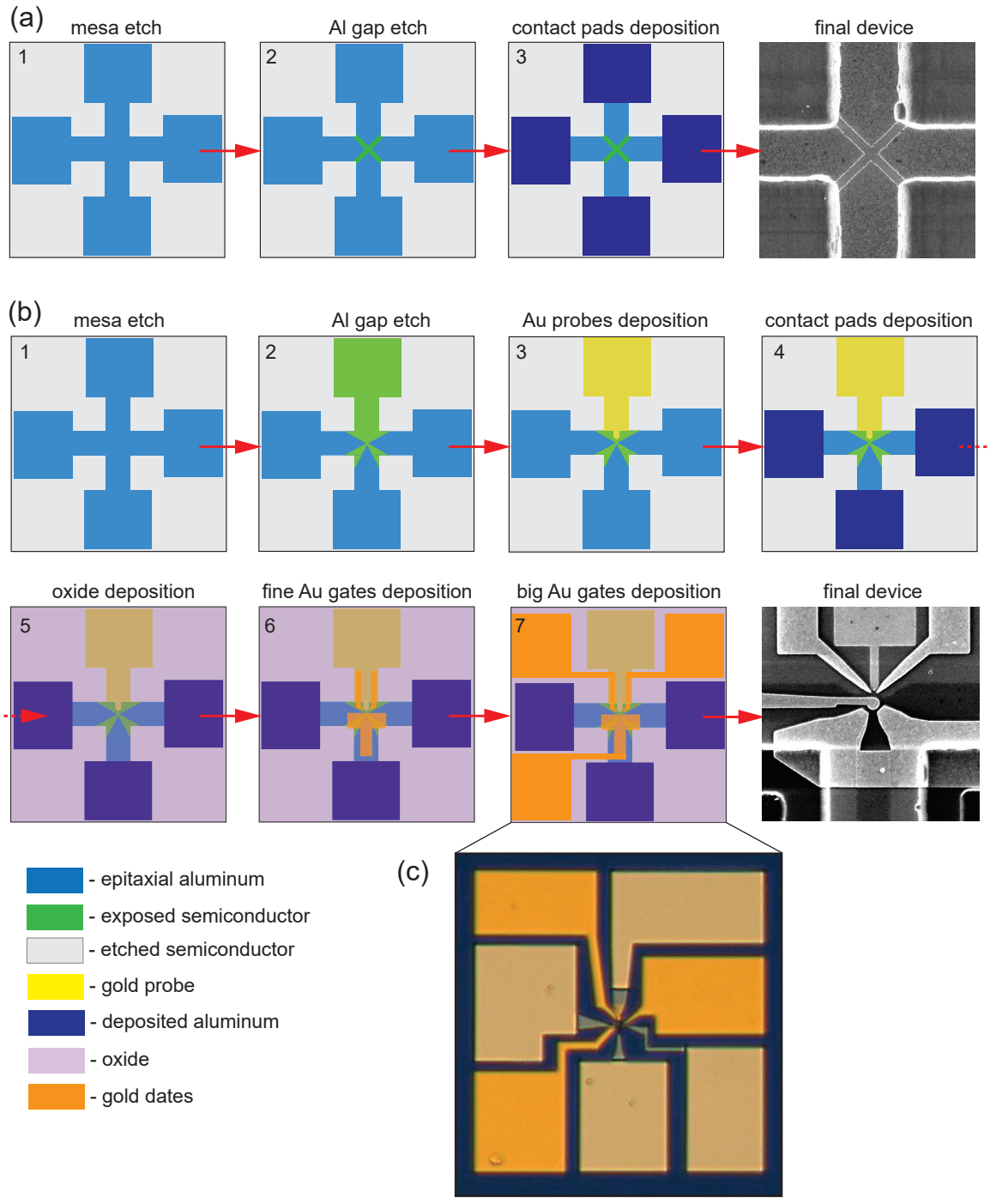

Figure 2.2: (a) Fabrication flow of the 3-step process used at the first stages of the project for CCC characterization measurements and an SEM image of a final device. (b) Fabrication flow of the 7-step process used at the later stages of the project for conductance measurements and an SEM image of a final device.

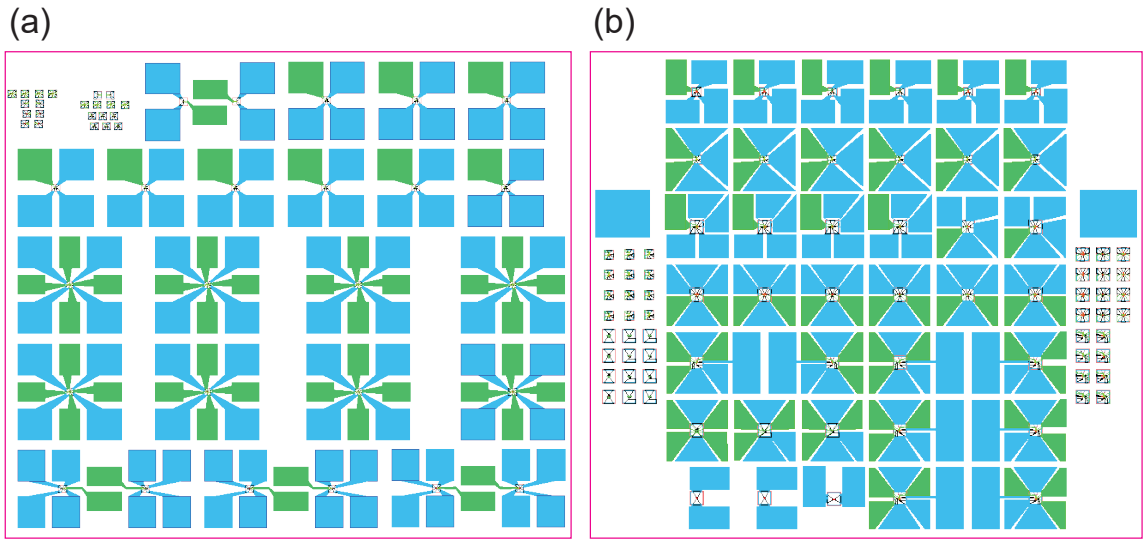

Figure 2.3: (a) Example of chip outline used at the first stages of research, blue areas correspond to Al pads and green to Au pads of gates (a set of squares in the top left corner is copies of devices without contact pads for SEM imaging). (b) Example of chip outline after modification (set of squares on the sides are also copies of devices for SEM imaging). Alignments marks would be located in corners and not shown here.

develops will etch aluminum. Even though it might seem like a bonus since the top aluminum layer has to be etched anyway, in fact, development/etching goes uneven and leaves random islands of aluminum. Moreover, during the following step of intentional aluminum etch the etchant would frequently penetrate underneath the maN mask causing severe overetch of devices. As a result of these obstacles, it was decided to use PMMA resists and do inverse design, i.e. to expose everywhere except small areas of the devices.

The inverse design was prepared in two steps. First, the direct design would be created in AutoCAD (Fig. 2.4 (a)). This design would include all steps and details of final devices (future gaps in aluminum, gates, probes, etc.) and saved in .dxf format. Then the file would be open in the Layout Editor for a subtraction (Fig. 2.4 (b)). Subtraction could also be done in Autocad using the SUBTRACT command, however, I find it more convenient to use Layout's Boolean functions since it allows an easy mix and match of elements as well as subtraction of all elements of one layer. The inverse file could also be saved in .dxf format, however, our e-beam system worked better with .gds format.

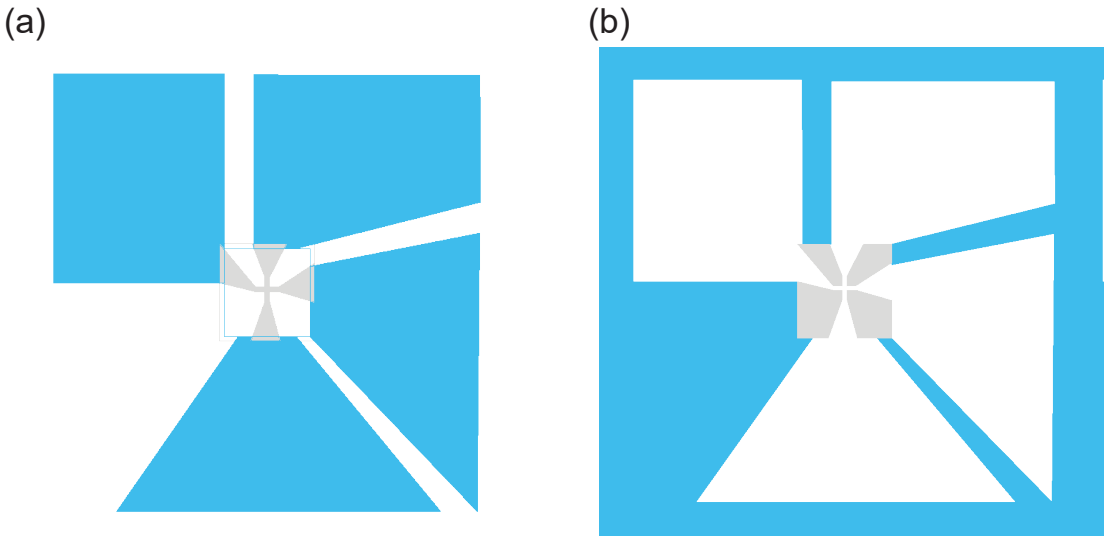

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Figure 2.4: (a) Direct design of the device prepared in AutoCAD and expected after lithography. (b) Inverse design after Boolean subtraction indicating the area that will be actually exposed. Grey region exposed with low 1 nA current for higher precision, a blue region exposed with 100 nA current.

Another important part of the design is the proper choice of the **alignment marks**. At the first stages of the project, when fabrication included only 3 steps, manual alignment was used. The alignment precision was up to $100 - 200$ nm and was easily compensated by an extra overlap of layers in the design. The design would include 4 sets of marks located at each corner of the chip approximately $3 - 4$ mm apart. Each set consisted of several squares of different orientations with respect to each other (Fig. 2.5 (a)). Having different patterns for each mark was helpful in case of errors during the alignment because looking at the orientation of the mark one could certainly identify which mark is used and which corner it is and hence define the location of the main pattern. In the beginning, we have been experimenting with the position of alignment marks by placing them close to devices, approximately 300 um apart, but did not notice any improvement in precision. For 5×5 mm chips using 4 alignment marks located in the corners and doing global alignment is enough.

Once the fab evolved to the 8-step process the need for more precise alignment arose. At this stage at least 3 layers must have been aligned very well to each other (aluminum gaps, gold probes, and gold gates), so the alignment precision must be within a few tens of nanometers. To achieve

such precision we switched to automatic alignment (Elionix team claims $20-30$ nm precision with automatic alignment, which seems to be quite accurate). The shape of the marks was changed to standard shape for Elionix: a cross with wings of 100 um lengths, 10 um width and 4 squares in the center (Fig. 2.5 (b) insert). However, we still kept some of the manual marks to help with navigation. As previously, having 4 sets of marks in the corners of the chip (approximately $3-4$ mm apart) and global auto-alignment was sufficient to achieve the required precision.

The marks would be created during the first step of fabrication and etched during the mesa etch. The problem was that after several steps of fabrication marks become quite used and appear blurred under the SEM, which makes precise alignment more complicated or even impossible. There are many solutions to this problem from etching marks much deeper to depositing some contrast material on them, however, all of these solutions assume an additional step of fabrication and we did not want to make the recipe more complicated than it has to be. A simpler solution to this was an addition of a second set of marks (inner crosses on Fig. 2.5 (b)). This way we would use the outer cross-like marks during steps 2-4 and the inner cross-like marks for steps 6-7.

Once you have thought your design through in every detail and made all necessary arrangements, you can finally get your hands "dirty" in the cleanroom.

2.2.2 Sample preparation

The fabrication starts with the selection of the right piece of material. We were receiving the material in quarters of 3 inch wafers and cleaved it manually into approximately 4×5 mm pieces. That size of the chip was selected based on our CAD design and an attempt to use the material as frugally as possible. The cleaving technique was the following: a glass slide was pressed to the front side of the quarter (touching it only with the edge), then we scratch a line along the glass edge with a diamond scribe. This way we "draw" a set of parallel lines with a spacing of approximately 4 mm and form several stripes. Then the quarter is transferred on top of the glass with one stripe hanging from the edge. We gently press in a corner of the stripe and it breaks off. After all, stripes are separated, we rotate them 90 degrees, scratch lines with a spacing of 5 mm and similarly separate them into small pieces. During this procedure, the corners and edges of the chips will get damaged, but this method

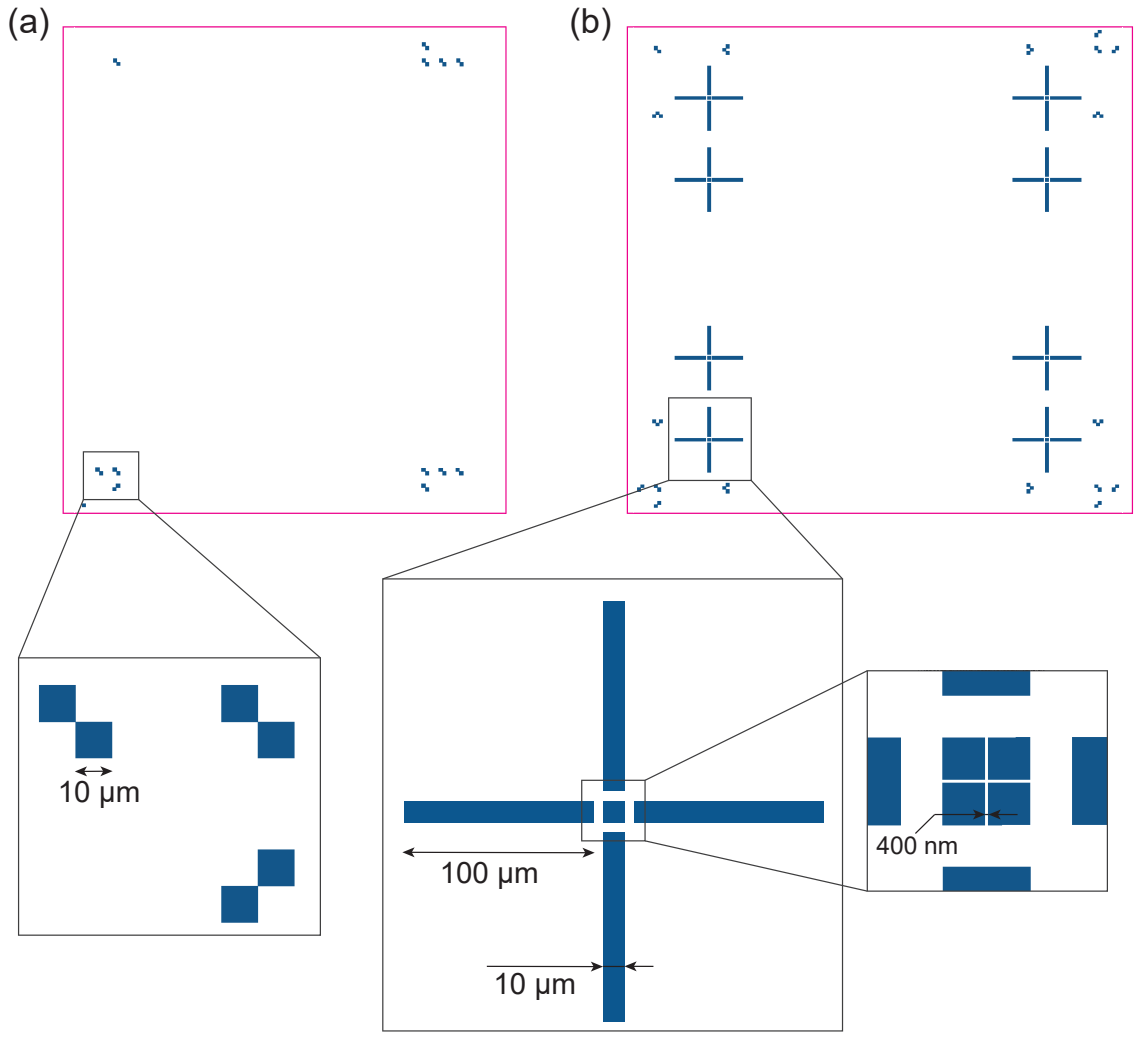

Figure 2.5: Example of (a) manual alignment marks used at the first stages of the project and (b) auto-alignment marks used in a more recent fabrication. Note two sets of auto marks, the outer marks were used in fabrication steps 2-4, then the inner marks were used at steps 6-8.

allows to reliably produce pieces of the desired size and hence, efficient usage of the material. To compensate for damaged edges we make sure our designs in CAD files do not exceed 3.5×4.5 mm dimensions.

Using this method we would usually get 22 squared pieces and a few edge pieces from the quarter, however, not all of them could be used for the device fabrication since material properties near the edge of the wafer are worse. At the end of the day, we had 9 pieces that were categorized as "good", 10 pieces categorized as "ok for a test" and around 5-6 "dose matrix" fellows.

After the proper piece was selected, it was cleaned with acetone and isopropanol (IPA). Typically during cleaning in acetone chips needed to be sonicated to remove dust from cleaving. The problem was that sonication (even for 10 sec) sometimes would cause the chip to break into halves. After going through denial, anger, bargaining, depression, and acceptance the problem was solved by switching the glass beaker with a plastic beaker. Once switched to the plastic beaker, we never had a breaking problem again even when sonicated for several minutes at different stages of fabrication.

We start cleaning in acetone only in the first round of sample cleaning, at the later steps when the resist has to be removed, it's better to start cleaning with PG remover first (NMP based solvent).

Cleaning procedure could be summarized as following:

- 15 min in PG remover at $60°$C (except the first step).
- 3 min in acetone.
- 3 min in IPA + rinsing with IPA.
- Blow-dry with N_2.

Important to note that after sonication at the preparation step it is generally a better practice to exclude sonication of the chip during the other steps since it might negatively affect the device.

After the chip is cleaned, it's inspected under the optical microscope and then the resist can be spun. For the first step of fabrication we use 950 PMMA A3, spun at 4000 rpm it forms a $\sim$$180$ nm thick film, then the chip is baked for 1 min at $180°$C on a hot plate.

2.2.3 Mesa etch

Once the chip is ready we can proceed to the e-beam lithography. The e-beam lithography is usually done in two steps: first with 1 nA current we define fine features of the future devices (i.e. crosses and Y-shapes showed in grey on Fig. 2.4 (b)) and alignment marks, then with 100 nA current everything else is exposed to define contact pads (the blue region on Fig. 2.4 (b)). There must be an overlap of $10 - 20$ um between these two layers since during the current change from 1 nA to 100 nA an offset will be introduced.

After e-beam writing the chip is developed for 2 min in the IPA:DI (3:1) mixture that was kept at $6°$C. Development in cold IPA:DI solution provides higher contrast and better-defined shapes compared to development in MIBK. For precise development and reproducible results it's important to keep IPA:DI at ($6°$C) during the development time by, for example, keeping it in the ice bath or in the water cooler. However, from multiple tests, we determined that our recipe is not very sensitive to the few degrees of temperature change during 2 min of development and used a simpler development protocol. The bottles with premix IPA:DI solution would be kept in the refrigerator at approximately $5°$C. Before development, we would make all necessary preparations (find a timer, set it to 2 min, grab the chip with reverse action tweezers, prepare a beaker, make sure nothing will stand between you and your nitrogen gun), then take a bottle from the refrigerator, fill a beaker and start development immediately. From time to time we would check the temperature in the refrigerator by sticking a thermometer in the test bottle of water that was kept near IPA:DI bottles.

Then the chip would be inspected under the optical microscope to ensure writing and development went as expected. When you do it for the hundredth time, you get very tempted to skip that part with an optical microscope. Never succumb to this temptation, it is a trap. Always check your sample with the microscope before proceeding to further steps!

Once chip perfection is verified, start preparing the etching solutions. The etching will go in two steps: etching of aluminum film and etching of semiconducting heterostructure. The aluminum film is etched in the commercially available Aluminum Etchant Type D from Transene. To heat up the etchant the beaker is placed in the hot ($50°$C) water bath for 10 min. Warming could also be done on a hot plate, but a water bath ensures more uniform temperature distribution in the volume as

well as good reproducibility each time. Etch rate will vary a lot depending on the temperature. Prior fabrication of working devices we verified that 10 min is more than sufficient to heat up the etchant to $50°$C. After 10 min, once the etchant is hot, a beaker with DI water is placed in the water bath right next to the etchant beaker and the chip is grabbed by the stainless steel tweezers. The chip would be immersed in the hot etchant for 10 sec and then moved to DI water beaker to stop etching. It takes $7 - 8$ sec to etch a layer of native AlOx and the etching of the aluminum film will be done in the next $2 - 3$ sec at a rate of 25 nm / sec. Note that the etch rate will double with every ($10°$C). So it's very important to control the temperature of the etchant precisely, have a beaker with water right next to the etchant and make sure that resist sticks to the surface very well. After stopping the etching process in the first beaker with DI water, move the chip to the second beaker with DI water, change your tweezers, then blow dry with a nitrogen gun.

The second step is the etching of semiconducting mesa. For this step the general solution for III-V is used, which is $H_3PO : H_2O_2 : HO_2$ with addition of citric acid. The etching will strongly depend on H_2O_2/citric acid ratio. We used an established ratio of $H_3PO : H_2O_2 : Ci : HO_2$ (3 : 3 : 55 : 220) citemortenthesis and obtained an etch rate of approximately 60 nm / min. The etching mixture could be prepared in advance but might change its properties if stored for a long time. We have noticed that after approximately two weeks of storage the etch rate would increase almost two times, so we would never use a mixture that is more than a few days old. For the important samples, we would prepare a mixture of exactly 24 hours before the etch to keep etching consistent from sample to sample.

To prepare the mixture start by making a 1M citric acid mixture. Since citric acid is usually available in the form of the powder to prepare 1M solution dissolve 192.12 grams in 1 liter of water (or 48.03 grams in 250 ml). Take a 500 ml beaker, filled it with 250 ml of DI water. Use a big measuring cylinder to take 55 ml of citric acid and add it to the water. Use a fine measuring cylinder to take 3 ml of hydrogen peroxide and then 3 ml of phosphoric acid, pour them into the water one by one. If the bottles with phosphoric acid or hydrogen peroxide are big, it might be very challenging to pour 3 ml. In this case, use a pipette, but make sure the material of the pipette is compatible with the acids. Due to the unstable nature of hydrogen peroxide (it decomposes into water and oxygen quite rapidly once the seal of the bottle is broken) we would always use a new 250 ml bottle of

H_2O_2 and open it right before mixing the etchant. The other 247 ml were donated to the cleanroom regularly.

Therefore, right after etching the top Al layer the chip would be etched in semiconductor etchant for 4 min (resulting in 250 nm depth), then rinsed with DI water, again inspected under the microscope and then the resist would be stripped. During the etch hold chip parallel to the main axe of the beaker's cylinder and swing back and force with 2 Hz rate. Mesa etch corresponds to step 1 on Fig. 2.2.

2.2.4 Aluminum gap etch

For the second step (Fig 2.2) we also use 950 PMMA A3, also spinning at 4000 rpm for 60 sec and baking at $180°$C for 60 sec as well. In principle, any PMMA from the A3-A6 family (both 495 and 950) can be used for the first two steps, we happened to have A3, it worked and we stuck to it. Two things to consider here is that now you have a high change of approximately 250 nm and it won't be a good idea to use a thin resist. On the other hand, you want to open fine features of an order of 100 nm and with too thick resist it might be very challenging.

The fabrication steps would be standard:

- Spin coat with a resist and bake
- Electron beam lithography to open small gaps
- Develop
- Etch in Aluminum Etchant Type D for 10 sec at $50°$C
- Strip the resist

We have fabricated several samples using this recipe, but at some point, things suddenly stop to work. With no obvious change in the recipe, we would get the gaps in aluminum to be severely overetched (Fig. 2.6 (b)). We spent a long time investigating the problem, but have not found a reasonable explanation for this change. Apparently, the problem was that the resist would not

stick to the surface well enough and during the etch process some of the etching mixtures would penetrate underneath the PMMA mask.

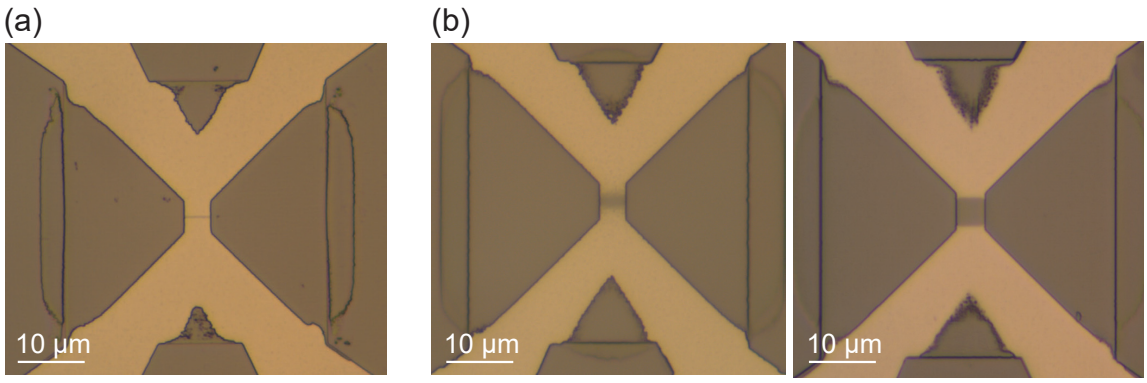

Figure 2.6: Demonstration of (a) a good etched gap in Al and (b) two examples of overetched gap.

A counterintuitive solution to this problem was suggested by a postdoc from Javad's lab Billy Mayer. It was suggested to cover the chip with silicon adhesive solution HMDS before spinning PMMA. HMDS datasheets state that it's very important to properly apply the solution by evaporating it in a water-free chamber. Under the "How NOT to apply HMDS" authors state that one should never use HMDS in a spinner and bake the photo-resist after applying HMDS since it might cross-link bottom layers of photo-resist [63]. The suggested solution to the overetch problem breaks all these rules, but for mysterious reasons actually do the job. Your sanity will tell you it shall never work, but don't judge until you try it yourself.

To apply HMDS, load the chip in the spin-coater and set a timer for a long time, say 10 min, at 3000 rpm. Prepare one pipette filled with HMDS and another with DI water. Start rotation, apply $2-3$ drops of HMDS to the sample, wait for a few seconds (you should see colors change in the beginning as film getting thinner), apply $4-5$ drops of water. Repeat these steps 2 more times, i.e. apply HMDS 3 times, then clean it with water also 3 times. The final step must be water. Stop rotation, but keep the vacuum on, and thoroughly blow-dry the chip with a nitrogen gun. Then switch spinner parameters and spin resist, as usual, following by usual baking. Voilà, no overetch anymore. This trick can also work when you have problems depositing some fine features, like QPC gold contacts.

2.2.5 Aluminum contact pads deposition

The thickness of epitaxial aluminum films is only $10 - 20$ nm and it might be very challenging to wire-bond to it. Since we have quite small contact pads there is no right for a mistake (or at least for too many mistakes) and to make wire-bonding simpler and more reproducible, we deposit an additional $100 - 150$ nm of aluminum on top of the contact pads (step 3 on Fig. 2.2(a)). This step also requires alignment, but obviously, it does not have to be very precise. To deposit a relatively thick film of aluminum you must have a thick resist mask. The golden rule of lift-off is that the thickness of depositing film must be 25 % or lower than the resist thickness. I.e. for 100 nm of the aluminum film, the resist must be at least 400 nm thick.

For the third step, we use a stack of two layers of 495 PMMA A4. Spin at traditional 4000 rpm, bake 1 min, then spin a second layer and bake 2 min at $180°$C. Proceed to e-beam writing, open the windows on top of the contact pads, deposit aluminum, lift-off in hot acetone. For the lift-off preheat some acetone to 60 C, leave the chip in for $30 - 60$ min, then spray with additional acetone. At the further steps of fabrication, we tried to exclude sonication due to the paranoia that almost ready chip might break into pieces, and usually spraying with acetone was enough to remove all extra metal. If a lot of metal is still left on the surface of the chip, a short sonication for $5 - 10$ sec in a plastic beaker might be used.

2.2.6 Normal probes

For the tunneling spectroscopy, we have chosen to use normal metal probes. At step 2 of aluminum etch, we remove epitaxial aluminum from the areas where gold probes are going to be deposited, then in separate e-beam writing, we create a mask in a double layer MMA-PMMA structure. To make sure the resist is cleaned well during the development we choosing higher than usual e-beam doses, i.e. the dose which causes the features to be $15 - 20$ % wider than in the original design. Then deposition of $5nm$ Ti and $30nm$ of Au follows. When this step is needed, we perform it as a third step, and contact pads deposition will follow after (Fig.2.2 (b)). This switch of order is done to preserve the freshness of alignment marks to ensure good alignment of the most sensitive features.

Gold deposited to the InGaAs forms a Schottky barrier with the resistance of a few $k\Omega$ (at 10 mK).

To perform tunneling spectroscopy it is essential that the resistance of the barrier would be higher than the resistance of the lines, which is in our case $8.4\ k\Omega$. Thus, to create a tunnel barrier split gates will be created later, on top of the oxide layer.

2.2.7 Oxide deposition

The creation of a reliable oxide layer was the biggest challenge of the project (step 5 in Fig. 2.2 (b)). We have tried multiple ways and machines available for us over the past few years, each method would have some disadvantages. Here we briefly summarize methods that were tried in a search of reliable oxide:

1. **ALD of Al2O3** using Beneq TFS 500 at UMD Fablab.

   We started by using a standard recipe for Al_2O_3 deposition, which was using short pulses (TriMethyl Aluminum (TMA) + H_2O_2, 1 sec purge time). The standard deposition temperature for this system $150°$C and the lowest pressure that could be achieved is only around 5e-3 Torr due to the large volume of the chamber. We experimented with different thickness of oxide (30 nm, 60 nm, 80 nm). From the chip with 30 nm of Al_2O_3 approximately 90 % of devices would demonstrate leakage current. On the chip with 60 nm of Al_2O_3 approximately 50 % of devices would leak, but another 50 % could be gated to complete depletion of 2DEG. From the chip with 80 nm of oxide, a bit more than 50 % of devices would not leak, however, it was taking very high voltage to deplete, approximately $20 - 30$ V compared to $3 - 4$ V for 60 nm oxide chip. An average critical current for the devices from these chips was around 1 uA. An additional problem was the parallel conductance. Before the deposition of oxide, the resistance between two isolated devices would be around $5\ k\Omega$ at room temperature, which would lead to $M\Omega$ resistance after cool-down. However, after the deposition of oxide resistance at room temperature would decrease to $1 - 2\ k\Omega$ and will stay of the same order after cool-down.

   We have also run a few tests modifying the deposition recipe: decreasing the temperature, increasing after pulse purge time to 30 sec and to 60 sec (that increased deposition time from 30 min to $6 - 8$ hours), but it did not result in noticeable change.

2. **ALD of Al2O3** using the Kurt J Lesker ALD-150LE system, deposited by Shabani's group at

NYU.

The deposition was performed at $120°$C and pressure of 1.18 Torr using standard precursors of TMA and water. Purging time was 16 sec after TMA and 1 sec for 3 pulses of water + additional 20 sec after the sequence of three. During 600 cycles a film of 60 nm was deposited. After the oxide deposition gold gates were created during the 2-step lithography process. Unfortunately, almost for all devices from these chips, the gates would leak. Moreover, the resistance between devices was also low: around 300 $k\Omega$ at room temperature and around 700 $k\Omega$ at 10 mK. Critical current was varying from 700 nA to 2 uA for different devices.

3. **Sputtering of HfOx.**

   Sputtering was performed on AJA International ATC 1800 V using 3" HfOx target. The pressure during deposition was varying between $4.6 - 4.8$ mT and the power was 60 W. At such parameters, we get a deposition rate of 2.5 nm / min and the temperature of the sample was close to the room temperature. We also deposited a film of 60 nm. For the sputtering films of HfOx we have got somewhat controversial results. On one hand, the resistance between devices stayed the same as for the bare chip at room temperature and would increase to $30 - 40$ $k\Omega$ after cool-down. Also, the average critical current value was $200 - 300$ nA. On the other hand, gates on many devices would leak. We have an inconsistency between several chips, for example on one chip 75 % of gates would work and only 25 % leak, but on two other chips only 10 % of gates would work. A possible explanation is that these chips were treated differently during the fabrication steps of gates deposition and wire bonding. We assume that the problem might come from baking steps when chips were heated to $180°$C.

4. **Electron beam deposition of HfOx** was performed on Denton Vacuum Explorer 14. A standard HfOx target was heated up with an electron beam, evaporated, and deposited on the chip. Denton has a pretty big chamber, the chip is mounted $40 - 50$ cm away from the crucible and, like in case with sputtering, was not heated much more than room temperature. The deposition rate was around 1 nm / sec and the thickness of the film was also 60 nm. After e-beam deposition we saw a big change in junctions' properties - there was no supercurrent

at zero gate voltage and it would appear at a positive gate. At a higher positive gate the critical current would increase like devices were fully depleted at zero gate and could be tuned to the supercurrent regime by applying positive voltage. This effect is associated with oxygen deficiency during the deposition process and was also expected to appear for sputtering, however, it did not. There is no profound explanation of how the deposition of the insulator and the conditions of its deposition affect the properties of the device, so here we just list our experimental findings.

2.2.8 Fine gates deposition

The sixth step of fabrication (Fig. 2.2 (b)) is the deposition of top gates. During the scope of work, we have been trying different geometries of the gates starting from the global gate, which was covering the whole junction, to fine gates to create tunneling barriers. The fabrication of the gates was performed in two steps: in the first step, we would define fine features of the gates as well as short connecting lines that later would be overlapped with a metal of the second step that forms contact pads. During the first step, we deposit a thin film of Ti/Au (5/30 nm) to ensure smooth liftoff of fine features. There are several approaches to form fine gates:

1. Use a thin single layer of resist, for example, 950 PMMA A2 or A3. The thickness of the mask then would be around 100 nm, so deposition of 35 nm of metal would slightly violate the golden rule of 25 %, which might result in bad lift-off. I.e. features would either be peeled off from the chip because of the vertical walls or extra metal would stay on the chip thus shorting different gates(Fig 2.7 (a)). On the other hand, a thin layer of resist might be beneficial if using a low voltage ($20-30$ keV) e-beam writer. In this case the rule "the smaller feature the thinner resist must be" will work, however, for high voltage e-beam writers ($100-125$ keV) one can define fine features even in a thick resist due to the small forward scattering of electrons in the MMA/PMMA layer [64]. Therefore, a second option is...

2. Use a thinker resist like 495 PMMA A4 or even a double stack of the same resist (A4+A4). That would increase the height of the mask and help decrease the probability of the vertical walls

to be formed during deposition, and hence decrease the probability that fine gates could be peeled off. When working with high voltage e-beam lithography systems we find it preferable to use thicker resist structures when lift-off is needed. Another reason for choosing thicker resist is that sonication is not recommended after the oxide is deposited and thicker resist film allows to perform lift-off simply by spraying with acetone on the chip without sonication (after preliminary 60 min in hot acetone). However, the vertical walls still can be formed, which can result in bad lift-off and extra metal flakes attached to the surface (Fig 2.7 (b)).

3. Use a double layer of resists, when the bottom layer is softer than the top one, for example, MMA EL9 (or 495 PMMA A4) and 950 PMMA A3. Due to the difference in structure, more of the bottom layer resist would be removed during the development, thus forming an undercut. An undercut structure allows to eliminate a formation of vertical walls and work great when very fine features need to be deposited on a non very sticky surface. It is also easy to perform lift-off without sonication (Fig 2.7 (c)). However, with such a double-layer structure one might encounter a problem if depositing a wetting layer of Ti since the undercut might be very big, i.e. the top layer might get completely suspended. If electrodes are located in close proximity it can lead to shortening.

From our experience, the third recipe worked the best, even when the spacing between electrodes is only 100 nm. The low forward scattering effect at our 100 kV lithographer together with development at cold IPA:DI preserves most of MMA between the electrodes. But we must pause here for a short, but very important discussion of resist baking. Keeping in mind that long baking at 180 C might cause oxide or device degradation, we tried to limit our baking time to 1 min for the first layer and 2 min for the second layer. We used the same resist bi-layer and same baking time to create normal probes and the recipe worked beautifully. However, after the deposition of gates, we encounter a problem: the Ti shadow was repeating the shape of the mask, however Au layer will be only partially deposited and partially shaded. The weird thing was that the shadow would form at different angles and in different directions for several devices from the same chip as shown in the (Fig. 2.8 (a)).

We spend a long time investigating the problem by performing deposition at the angle and with rotation, or fully flat, or in three different deposition systems, but still, see the same problem. It

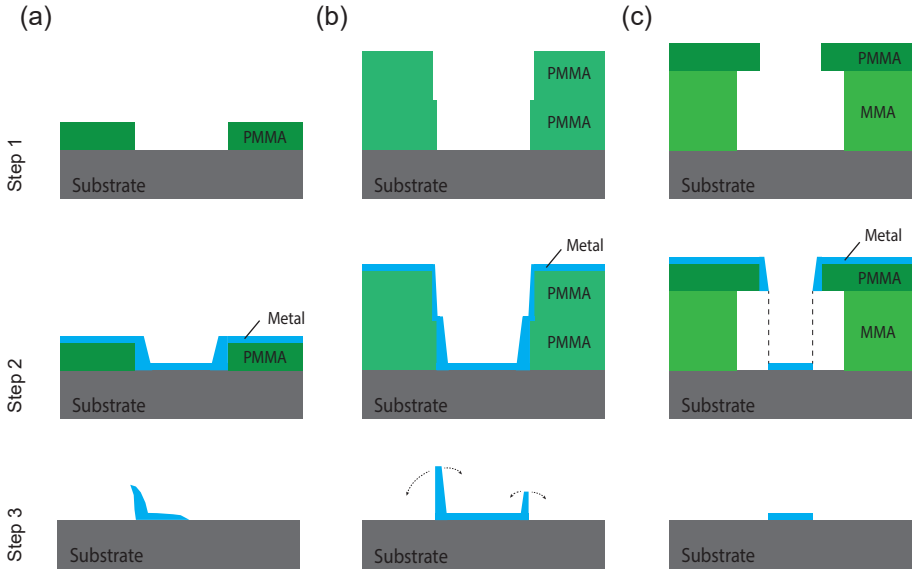

Figure 2.7: Comparison of different types of resist stacks for metal deposition.

became apparent that the problem is caused by resist, not by the deposition problem, so we did a test with baking the chip for 1 min $+ 20$ min and indeed the shading problem did not manifest itself. The reason was that after deposition of a quite thick layer of oxide the baking of resist would go slower. That is why this recipe worked for gold probes - they were formed on the 2DEG/Al layer, so the resist was baked properly. Once oxide is deposited it decreases the heating of MMA/PMMA, especially PMMA, so it does not harden sufficiently. Then, during the deposition process, the chamber will heat up during deposition of a first Ti layer and will make resist harden and shrink, but still, it's already developed it will shrink and bend randomly resulting in random shadow for the gold film. Therefore, the goal was to make sure we harden the top layer of PMMA without baking it for long. The way PMMA changes from liquid to hard solid is by evaporating the solvent - anisole. And if we cannot remove it by baking from the bottom, why do not we try to remove it from the top by loading the chip into a deposition chamber and pumping for a sufficiently long time? These tests were done during the pandemic and with limited access to the lab, so chips were first baked for $1 + 2$ min and then loaded into Plassys and pumped for 48 hours. Presumably, an overnight pumping would be also enough. Pumping did a great job and the fine gates mystery was resolved (Fig. 2.8 (b)).

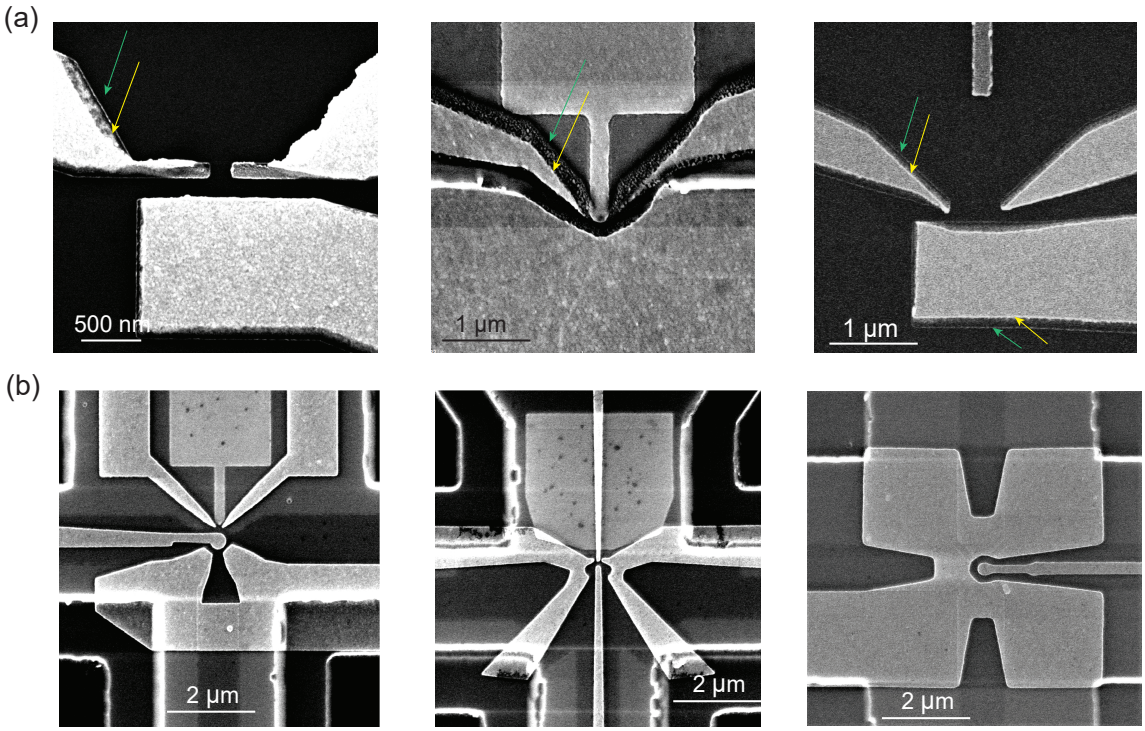

Figure 2.8: SEM images of (a) problems with fine gates deposition on top of oxide dielectric. Green arrows indicate the shade of Ti, yellow arrows shade of Au. (b) Examples of the good gates fabricated after high vacuum treatment of the PMMA were introduced prior to the e-beam writing. On the (b) two shades are matching.

2.2.9 Big gates deposition

Deposition of bigger parts of the gates like contact pads and connecting lines is easier, but still contain a few important points (step 7 in (Fig. 2.2 (b)). First of all, when designing gates make sure that the first and second layers will overlap on top of the mesa, such that the thin 30 nm layer of gold does not have to go through the height change (it will result in gates being disconnected). But this overlap must be sufficiently far from the junction area, at least $20 - 30$ um. Second, to deposit a thick layer of gold (and you want a very thick layer to make your wirebong time less miserable) it is important to use a thick PMMA mask, to deposit 100 nm of gold you need a 400 nm thick resist and to deposit 150 nm you will need 600 nm thick resist. Here using a double layer of the same resist is preferable, for example, two layers of 495 PMMA A6. Usually for the mesa of $200 - 250$ nm depositing $100 - 150$ nm of gold is sufficient to compensate for a height change and make sure the line won't have a break. However, if mesa etched for more than 250 nm a thicker gate metal shall be deposited.

2.2.10 Wire-bonding and room-temperature testing

To make electrical contact to the devices we mount it to the copper sample holder by applying a drop of PMMA and baking for 10 min at 60° C. Copper pads of the holder require special treatment prior wire-bonding due to the nasty copper oxide. Cleaning the pads is essential for successful wire-bonding, because when the tip makes the first bond on the dirty pad it may get contaminated with nasty stuff that going to be transferred to the chip causing difficulties at the second bond. If you have problems making a second bond (on the chip) make sure to clean the contact pads of the holder. To clean the pads we apply some soldering flux and keep it for 60 sec, then gently brush the pads with a wooden stick and rinse with IPA. We use manual wedge wire-bonder with Al wire from West-Bond Inc. Typical bonding parameters are 300 power and 30 sonication time for the first bonds and 180 power and 75 sonication time for the second bond.

Once devices are connected to the holder it's a good practice to measure the resistance through each bonded device as well as the resistance between devices. From our experience, if the resistance through the device was higher than $1\ k\Omega$, the device will not work after cool-down.

2.2.11 Recipes summary

A condensed overview of fabrication steps:

Mesa etch

1. Clean 3 min in acetone + 5 sec sonication, 3 min in IPA, N_2 blowdry.
2. Spin coat: 950 PMMA A3 at 5000 rpm for 60 sec. Bake 60 sec at $180°$C.
3. E-beam:
   (a) Fine features: I $= 1$ nA, writefield size $= 100$ um, 1000000 dots, skip 20x20 dots, dose time $= 0.018$, 450 uC/cm^2.
   (b) Alignment marks: I $= 1$ nA, writefield size $= 100$ um, 1000000 dots, skip 20x20 dots, dose time $= 0.018$, dose 450 uC/cm^2.
   (c) Big features: I $= 100$ nA, writefield size $= 500$ um, 1000000 dots, skip 40x40 dots, dose time $= 0.28$, dose 700 uC/cm^2.
4. Develop in IPA:DI (3:1) at $6°$C for 2 min, blowdry with N_2.
5. Al etch with Transene Type D for 10 sec at $50°$C, stop in DI water, double wash in a second beaker with DI water, N_2 blowdry.
6. Mesa etch: 4 min in $H_3PO : H_2O_2 : Ci : HO_2$ (3:3:55:220), stop in DI water, N_2 blowdry.
7. Strip resist: 15 min in PG remover at $60°$C, 3 min in acetone, 3 min in IPA, N_2 blowdry.

Aluminum gaps

1. Spin HMDS: start spinning at 3000 rpm, deposit 3 drops of HMDS, deposit $4-5$ drops of DI water. Repeat 3 times finishing with DI water. Stop spinning, N_2 blowdry.
2. Switch spinning program. Spin coat: 950 PMMA A3 at 5000 rpm for 60 sec. Bake 60 sec at $180°$C.
3. E-beam:

(a) Cross-shape gaps in aluminum: I $= 1$ nA, writefield size $= 100$ um, 1000000 dots, skip 10x10 dots, dose time 0.012, dose 1200 uC/cm^2.

(b) Pointy-shape gaps in aluminum: I=1 nA, writefield size=100 um, 1000000 dots, skip 12x12 dots, dose time 0.01152, dose 800 uC/cm^2.

(c) Contact pads clear-off: I=100 nA, writefield size=500 um, 1000000 dots, skip 20x20 dots, dose time 0.012, dose 1200 uC/cm^2.

4. Develop in IPA:DI (3:1) at $6°$C for 2 min, blowdry with N_2.

5. Al etch with Transene Type D for 10 sec at $50°$C, stop in DI water, double wash in a second beaker with DI water, N_2 blowdry.

6. Strip resist: 15 min in PG remover at $60°$C, 3 min in acetone, 3 min in IPA, N_2 blowdry.

Gold probes

1. Spin coat: MMA EL9 at 5000 rpm for 60 sec. Bake 1 min at $180°$C. Spin 950 PMMA A3, bake 2 min at $180°$C.

2. E-beam:

   (a) Small parts: I=1 nA, writefield size=100 um, 1000000 dots, skip 10x10 dots, dose time 0.01, dose 1000 uC/cm^2.

   (b) Big parts: I=100 nA, writefield size=500 um, 1000000 dots, skip 20x20 dots, dose time 0.01, dose 1000 uC/cm^2.

3. Develop in IPA:DI (3:1) at $6°$C for 2 min, blowdry with N_2.

4. Deposit 5 nm Ti + 100 nm Al.

5. Lift-off 1 hour in acetone at $60°$C, spray with acetone, spray with IPA, N_2 blow dry.

Al contact pads

1. Spin coat: 495 PMMA A4 at 5000 rpm for 60 sec. Bake 1 min at $180°$C. Spin the second layer of PMMA A4, bake 2 min at $180°$C.

2. E-beam:

   (a) I=100 nA, writefield size=500 um, 1000000 dots, skip 40x40 dots, dose time 0.06, dose 1500 uC/cm^2.

3. Develop in IPA:DI (3:1) at $6°$C for 2 min, blowdry with N_2.

4. Deposit 5 nm Ti + 100 nm Al.

5. Lift-off 1 hour in acetone at $60°$C, spray with acetone, spray with IPA, N_2 blow dry.

Oxide deposition (e-beam of HfOx)

1. Clean 3 min in acetone, 3 min in IPA, N_2 blowdry with N_2.

2. Load sample into the chamber, install sample shatter and system shatter, load a copper crucible with HfOx granules. Close chamber, pump overnight (pressure prior deposition must be $< 5e-7$ Torr).

3. In the morning turn on the e-beam current, verify the central position and slowly ramp up the current to achieve a deposition rate of 1-2 A/sec.

4. Deposit 60 nm, ramp down the current, let chamber to cooldown and unload.

Fine gold gates

1. Clean 3 min in acetone, 3 min in IPA, N_2 blowdry.

2. Spin coat: 495 PMMA A4 at 5000 rpm for 60 sec. Bake 1 min at $180°$C. Spin the second layer of PMMA A4, bake 2 min at $180°$C.

3. E-beam:

(a) QPC-like gates: I=1 nA, writefield size=100 um, 1000000 dots, skip 12x12 dots, dose time 0.01152, dose 800 uC/cm^2.

(b) Narrow gates: I=1 nA, writefield size=100 um, 1000000 dots, skip 10x10 dots, dose time 0.012, dose 1200 uC/cm^2.

4. Develop in IPA:DI (3:1) at 6°C for 2 min, blowdry with N_2.

5. Deposit 5 nm Ti + 30 nm Au.

6. Lift-off 1 hour in acetone at 60°C, spray with acetone, spray with IPA, N_2 blow dry.

Big gold gates

1. Spin coat: MMA EL9 at 5000 rpm for 60 sec. Bake 1 min at 180°C. Spin 950 PMMA A3, bake 2 min at 180°C.

2. Load into the deposition chamber and pump overnight, unload and proceed to e-beam writing.

3. E-beam:

(a) I=1 nA, writefield size=100 um, 1000000 dots, skip 12x12 dots, dose time 0.01008, dose 700 uC/cm^2.

(b) I=100 nA, writefield size=500 um, 1000000 dots, skip 25x25 dots, dose time 0.010940, dose 700 uC/cm^2.

4. Develop in IPA:DI (3:1) at 6°C for 2 min, blowdry with N_2.

5. Deposit 5 nm Ti + 100 nm Au.

6. Lift-off 1 hour in acetone at 60°C, spray with acetone, spray with IPA, N_2 blow dry.

2.3 Measurement techniques and electronics

2.3.1 Setup and filtering

For the measurement of the hybrid semiconducting/superconducting devices, good shielding and filtering are very important. Although the base temperature of the dilution refrigerators is 10 mK, the electrons that flow through the device might be hot and significantly increase the effective temperature of the device. That could cause several types of troubles, from the smearing of some features to a complete inability to measure a supercurrent. Therefore, additional attention should be paid to the thermalization of the electrical lines.

The measurements were performed in two bottom loading dilution refrigerators from BlueFors. In general, the two refrigerators are very similar, the main difference being that one of them was the first bottom loading system from the company, which contained a set of RF lines and a homemade coil to apply a magnetic field. The second refrigerator was a newer model configured purely for DC measurements (with twisted pairs) and has a vector magnet. The same base temperature setup was used in both refrigerators and it could be seen in Fig. 2.9 (c).

The chip sits in a copper box (Fig. 2.9 (a,b)), consisting of two parts: top part serves as a holder for the chip and has a soldered circular connector; the bottom bulky part with a cavity serves as shielding for the chip and helps to thermalize the chip holder. From the sample holder, the measurement lines go into the copper powder filter that blocks high-frequency radiation.The copper powder filter, made by Roman Kuzmin, is made with a rectangular copper box containing 6 trenches inside. To make a filter, the Stycast 2850 was used due to its non-zero thermal conductance at low temperatures. The epoxy was mixed with copper powder in a ratio of 50/50 at low speed to eliminate the formation of bubbles. Then 2 wires were places in each trench, filled with the mixture, and left to harden. Then, the copper box was sealed with indium wire (Fig. 2.10 (c)).

After the copper powder filter, the measurement lines go to the RC filter. At the beginning of this work, the role of an RC filter was performed by the line's capacitance and a single $5\ k\Omega$ resistor soldered to each line right in the sample holder PCB board. We pause here for a short discussion of filtering importance and a useful testing tip suggested by Vlad Manucharyan. First attempts to measure supercurrent in the hybrid devices were done with only room temperature

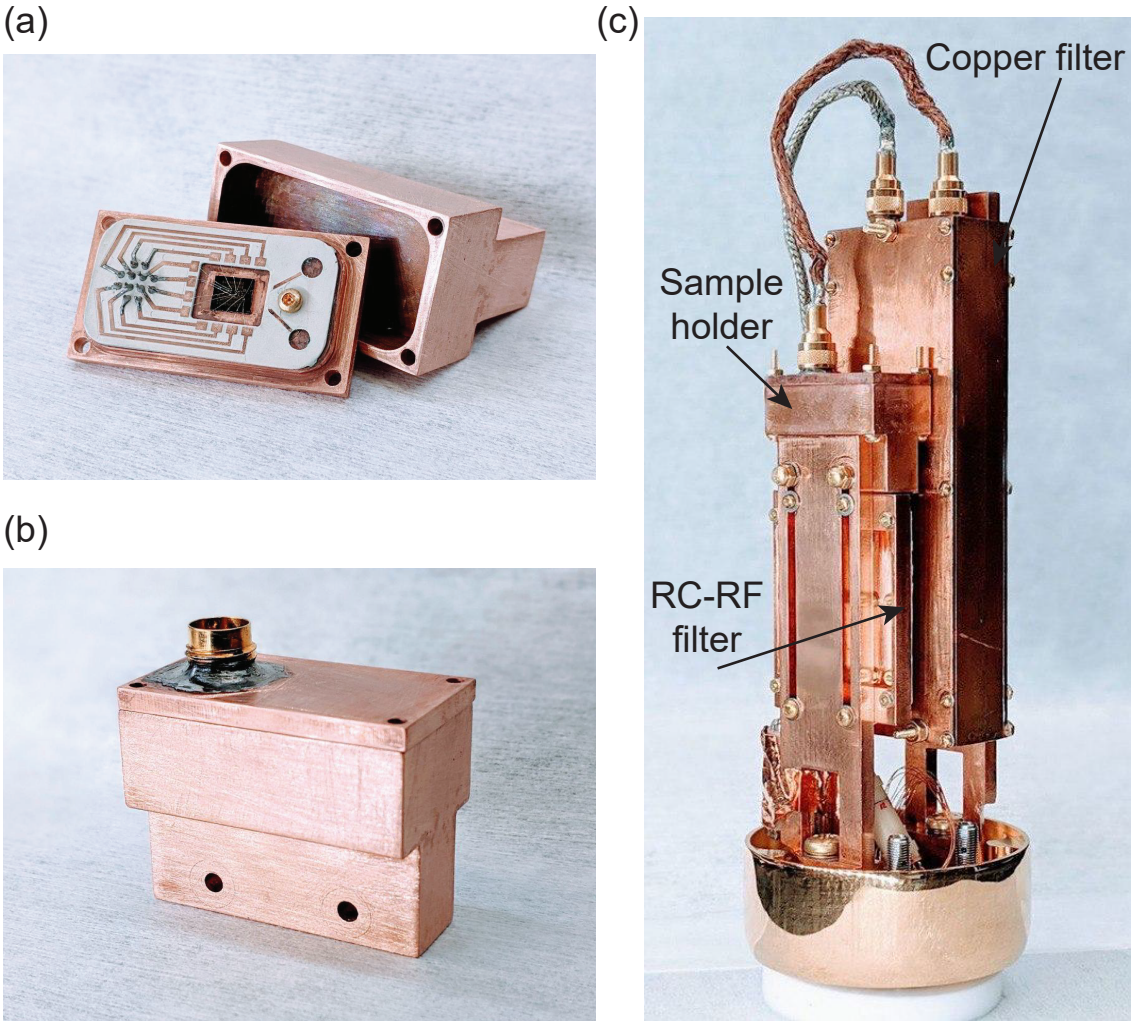

Figure 2.9: (a,b) A copper box sample holder, the chip is mounted to the top part of the box. (c) In an assembled probe, arrows indicate the position of the sample holder, RC-RF filter, and copper powder filter.

filters at the breakout box and the copper powder filter. We saw no supercurrent whatsoever and it was hard to tell if the problem was with filtering or with a device. Then Vlad suggested testing the setup by measuring Al/AlOx/Al tunnel junctions that are usually used for the qubits in our group. Tunnel junctions are very sensitive to noise and could be easily burned by high current or high noise, moreover, those junctions have been measured so intensively over past decades that you know what to expect pretty well. Their sensitivity and ability to visually define if the junction was burned (visually under the SEM of course) makes Al/AlOx/Al junctions perfect candidates for electrical setup testing. However, it is strongly recommended to use junctions of a big area, at least $1x2\ um$. The small tunnel junctions of the area, say $200x200\ nm$, are very fragile and can't be used for preliminary testing, only as a golden standard for fine-tuning.

The addition of RC filter was sufficient to measure wide tunnel junctions and we proceed to hybrid InAs/Al junctions. The data presented in chapters 3, 4 and 5 was obtained in that setup. Later in the work, we replaced the RC filter with a more sophisticated RC&RF one shown in Fig. 2.10 (a). The filter consists of 3 stage RC filter with the elements chosen to have low-pass cut-off frequency $f_c = 1/(2\pi RC) = 14.2kHz$ (Vishay Foil Resistors of $R = 2\ k\Omega$ and Kemet $C = 5.6nF$ capacitors), and 3 π-filers of 80 MHz, 900 MHz, and 3000 MHz cut-offs. As a result, the measurement lines are filtered in a range from approximately 15 kHz to almost 20 GHz and above. Voltage-biased measurements mentioned in chapter 6 was performed using this RC&RF filter. The picture of the filter is shown in Fig. 2.10 (b).

2.3.2 Measurement techniques

In this part, we briefly review the measurement details and techniques used for measurements reported in the chapters 3,4 and 5. The measurements of a critical current contour (which will be discussed in greater detail in Chapter 3) was done in a current biased measurement setup. Each device was typically connected for 4-point measurement, meaning 6 lines for a 3-terminal device and 8 lines for a 4-terminal device. We perform a standard lock-in transport measurements to obtain differential resistance dV/dI or conductance dI/dV. We start by testing every pair of terminals which are connected to one lock-in (Stanford Research SR865 or 865A) and measured in differential mode. Then measurement configuration was changed to accommodate a second lock-in and

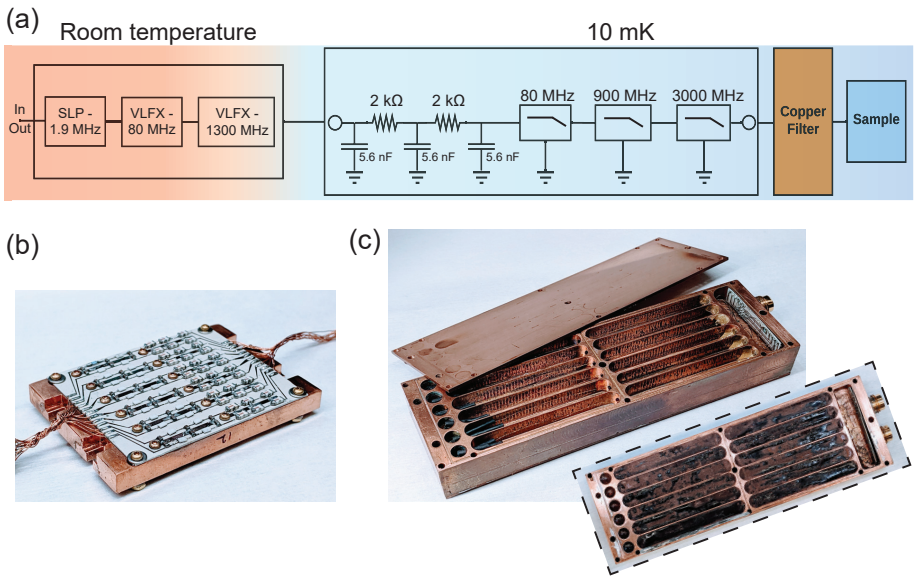

Figure 2.10: (a) Schematics of a line's filtering (only one line is shown). (b) A picture of RC-RF filter (12 lines). (c) Opened copper powder filter, the top picture shows six empty trenches with two wires each, insert shows backside of the filter with trenches filled with epoxy/copper powder.

perform 2 currents measurement. The setup configuration would be different for 3- and 4-terminal devices and it is shown in Fig.2.11 (a,b). We used $1\ M\Omega$ bias resistor on each driving line to fix AC current on values typically around $5\ nA$. Since the values of the critical current was in the range of $0.2 - 1\ uA$, the value of $I_{AC} = 5 - 10\ nA$ was sufficient for a good resolution. For the case of low critical currents ($< 30nA$), we used smaller values of I_{AC} down to $\sim 100\ pA$. The signal was amplified with voltage amplifiers SR560 by a factor of 100. Simultaneously, two dc voltages were measured with digital multimeters HP 34401A.

For the differential conductance measurements described in Chapter 6, we used a voltage bias setup that is shown in Fig.2.12. For that measurement the resistance of the tunneling contact shall be much higher than the resistance of the lines. With all filters, the resistance of our lines was $\sim 8.3\ k\Omega$ and the normal resistance of the junction was in the range of $0.2 - 2\ k\Omega$. Higher resistance of the contact was achieved by applying a gate voltage. Measurement configuration was as following: an AC+DC voltage was applied with a lock-in, and the resulting in the circuit current was found with the help of a current preamplifier SR570 and the lock-in.

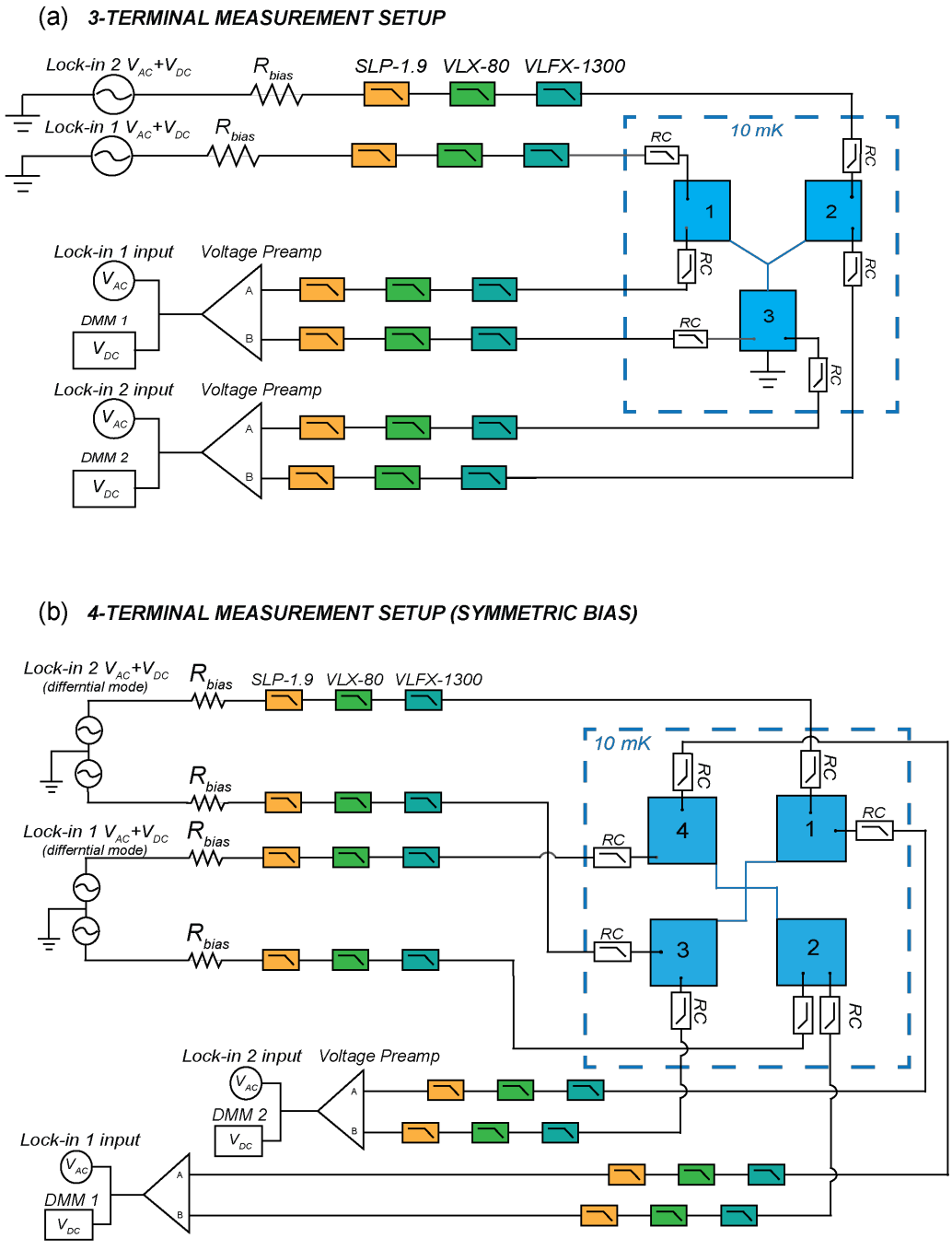

Figure 2.11: (a) Measurement setup of the 3-terminal junction. One terminal is grounded and two independent currents are sources in the other two terminals. The RC filters inside the refrigerator are the $5\ k\Omega$ resistors soldered into PCB board. Three colored filters at room temperature are commercially available filters from Mini-Circuits mounted in the breakout box. (b) Measurement setup of the 4-terminal junction in a symmetric bias scheme. Two lock-ins are connected to two pairs of terminals in deferential mode.

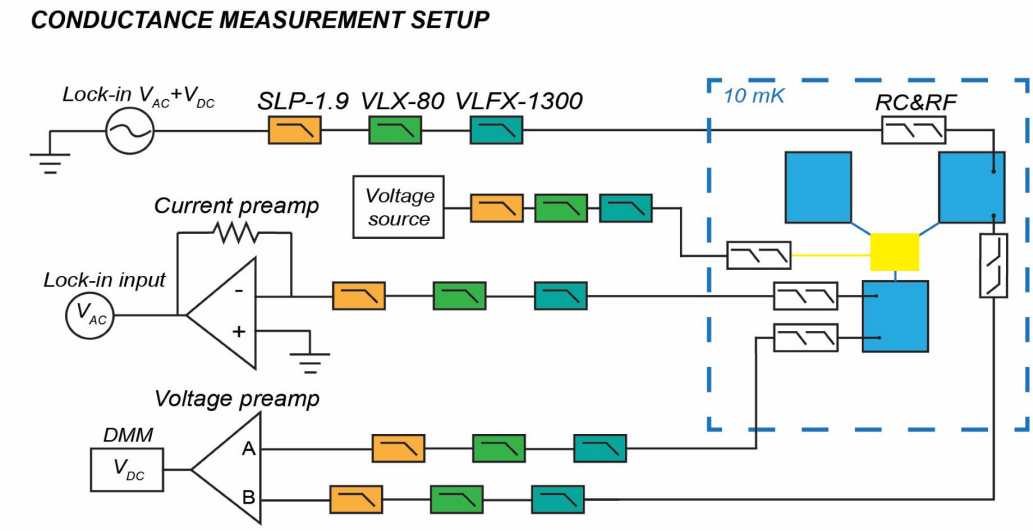

Figure 2.12: Schematics of the setup used for the conductance measurement. Room temperature filters are the same, the RC&RF filters are homemade and presented in Fig.2.10.

Chapter 3

The multi-terminal Josephson effect: 3-terminal case

In this chapter, we present a summary of the results of transport measurements of the 3- terminal Josephson junctions. We introduce the idea of a multi-current measurement and novel concept of the Critical Current Counter (CCC) arising from the measurement of the 3-terminal junctions. The two-current plots of differential resistance will be discussed in great detail in this chapter. It will allow us to build a solid understanding of the rich features of two-current plots of 3-terminal junctions before moving on to the more complex case of 4-terminal junctions. In particular, we introduce the concept of CCC, discuss lines of lower resistance as well as high order Multiple Andreev Reflections (MARs). Finally, we present the magnetic field data to demonstrate the non-trivial geometric responses of the CCCs to the perpendicular field.

3.1 3-terminal Josephson junction

As we discussed in the Introduction, "more is different" and the addition of an extra terminal to the traditional 2-terminal Josephson junction creates an additional degree of freedom for the system and gives rise to the set of peculiar effects. In conventional 2-terminal junctions, supercurrent is a

function of the superconducting phase difference. Meanwhile, in the 3-terminal junctions supercurrent becomes a multivariable function of the 2 independent phase differences. Due to the addition of the extra terminal, we can perform 2-current measurement by grounding one terminal and sourcing two currents into the junction through the other two terminals. In our hybrid super-semi junctions, the supercurrent is governed by the formation of the Andreev Bound States, which energy E_{ABS} will depend on all 3 superconducting phases since the wave function is nearly equally present in all of the terminals.

To start characterization of the device, we first measure individual dV/dI characteristics between each pair of terminals in a differential mode of lock-in, thus extracting values of normal resistance and critical current, aka quasi 2-terminal measurement. During this measurement, the third terminal is floating. Once supercurrent through individual pairs is confirmed, we perform a new measurement by sourcing two currents into the junction simultaneously and measuring differential resistances for each current. Voltages between each sourcing terminal and the ground are also measured simultaneously. The interaction of two currents in one junction creates several physical effects that we are going to discuss in detail further.

The first peculiar feature of the N-terminal junctions arises from the opportunity to apply N currents to the junction. The important parameter of the critical current value I_c in the 2-terminal junctions (Fig 3.1 (a)) transforms into a 2D object of Critical Current Contour (CCC) for the 3-terminal junctions (Fig 3.1 (b)) and a 3D Critical Current Surface for the 4-terminal junctions (Fig 3.1 (c)). I.e. in the $N = 2$ case, the critical current is simply the maximal current that the junction can withstand while maintaining zero voltage. However, for $N = 3$, there are two independent currents I_1 and I_2, and the current combinations for which both terminals are at zero voltage define a simply connected 2D region in the (I_1, I_2)-space. Thus, the scalar two-terminal critical current is replaced by a geometric object - the critical current contour surrounding the zero-voltage region. For $N > 3$, the zero-voltage region is surrounded by an $(N - 1)$-dimensional hypersurface, i.e. only values within the surface satisfy the case of multi-terminal junction being in the superconducting regime.

During the scope of this work, we have measured several of alike 3-terminal devices that had minor modifications. In this thesis, we present the result for the two most representative examples

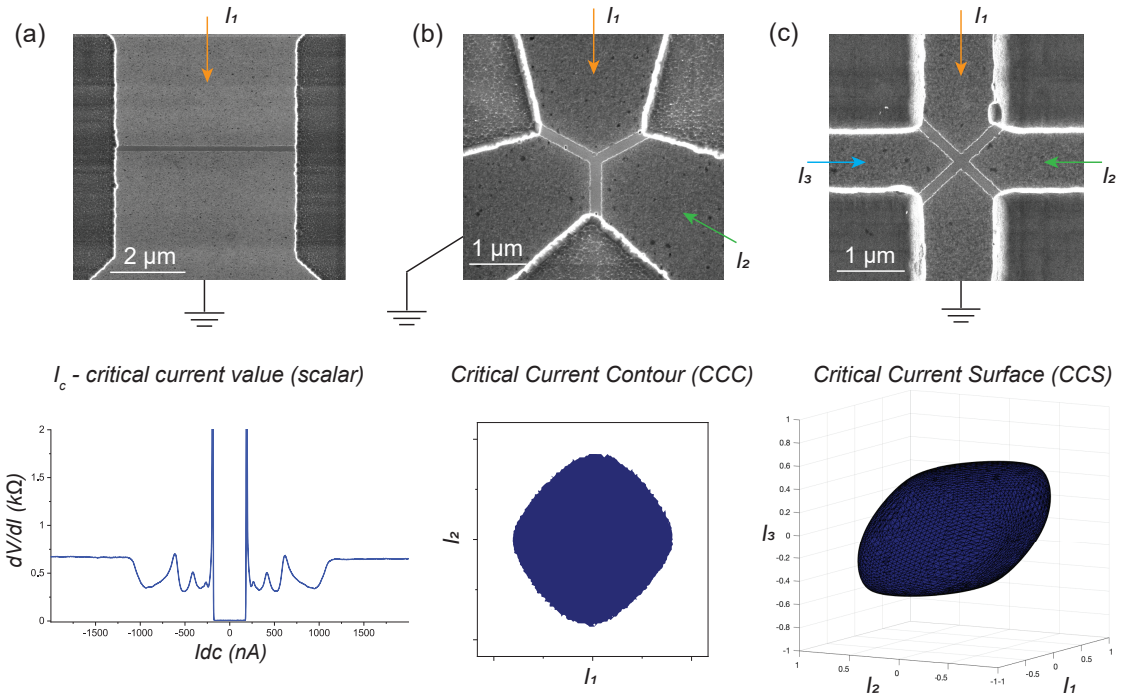

Figure 3.1: (a) SEM image of a 2-terminal JJ and a corresponding typical differential resistance as a function of a driving current. (b) SEM image of a 3-terminal JJ and typical differential resistance maps of two-current measurement. The dark blue area corresponds to the superconducting state, the white-colored area to the finite voltage state. The boundary of the dark blue region is the Critical Current Contour (CCC). (c) SEM image of a 4-terminal JJ and a simulation of the three-current measurement. The space confined inside the blue object corresponds to the supercurrent between all pairs of terminals, the surface of the object is the Critical Current Surface.

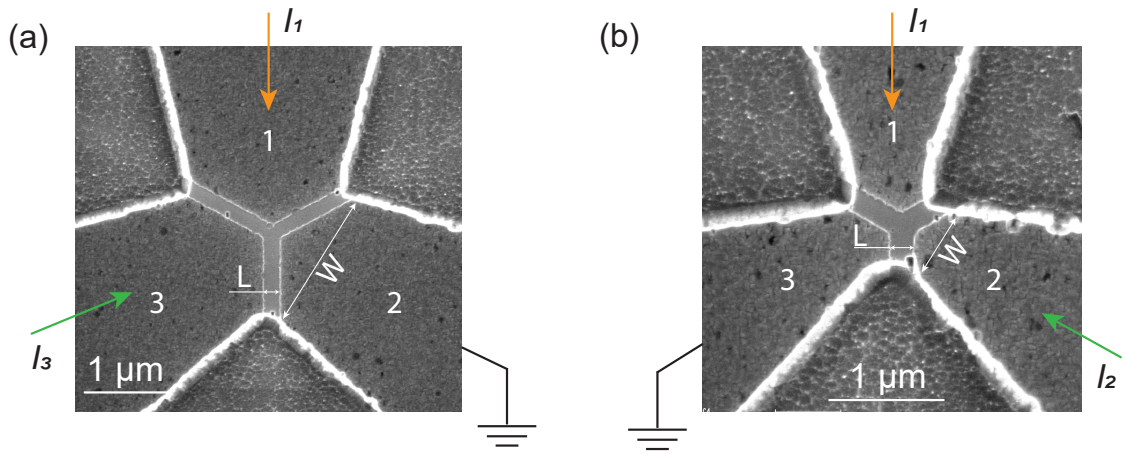

Figure 3.2: SEM images of the 3-terminal junctions and schematic set up of (a) larger junction C5, (b) smaller junction C4.

shown in Fig. 3.2. The bigger junction (3.2 (a)) labeled C5 has a terminal width of $W \approx 1.5$ um and the spacing between Al terminals of $L = 150$nm; the smaller junction in Fig. 3.2 (b) labeled C4 has a terminals width of $W \approx 0.7$ um and the spacing between Al terminals of $L = 150$nm. The aspect ratio (W/L) of the junctions is 10 and 4.6 correspondingly and quite high, which leads to a large number of channels per each arm (≈ 160 for C5 and ≈ 70 for C4, using the material's Fermi wavelength $\lambda_F \approx 25$ nm). The estimated mean free path in our material 2DEG is $l_e \approx 450$ nm and phase coherence length $l_\phi \approx 700$ nm. That corresponds to the junction being in a nearly ballistic regime. However, due to the natural imperfections of material acting as scattering centers and transverse modes of electrons in such wide junctions, our junctions are partially in intermediate regime.

Although the Y-shaped geometry of the gap is not optimal to study the multi-terminal effect (since coupling between neighboring terminals is much stronger than between opposite), it was originally chosen from consideration of induced proximity limits. There was a concern about how far the superconductivity could be induced for the Josephson junction based on this specific material. The results of the tests on two-terminal devices were varying several times for different material stacks. Hence, for the first multi-terminal devices the geometry of short and narrow junctions was selected ($W = 200$nm and $L = 600$nm). Later, when the material proved to be able to support induced

superconductivity on the length of a few hundreds of nanometers, the geometry was modified to decrease the coupling between adjoint terminals by making superconducting leads pointy-like.

3.2 Introduction to two-current measurements

As discussed above, the 3-terminal junction can be measured by grounding one terminal and sourcing 2 currents to the other two terminals (Fig. 3.2). Hence, to fully characterize the 3-terminal Josephson junction we perform three measurements by grounding each terminal and sourcing two current to the other terminals. As a result, we get 6 plots of differential resistance: two plots taken simultaneously for each current during three measurements (Fig 3.3). On each plot we can distinguish two main regimes: 1) the central dark-blue area corresponds to the superconducting state between all 3 terminals, while 2) everything outside of the dark-blue region corresponds to the finite voltage state. In general, the shape of the superconducting region is oval-like for each measurement, however, the details of the oval, like aspect ratio or tilt, may vary. It could be easily understood considering the nature of the device - since junctions could be asymmetric due to random imperfections in the scattering region or nanofabrication process, the measurement plots and shapes of superconducting regions will differ depending on which terminal was grounded for the particular measurement.

The 2-current plots are rich with features and hard for immediate understanding, so, first, we are going to discuss them one by one for a simpler understanding of each phenomenon and at the end, we will merge all of them into one plot.

We start our discussion by considering the rays of lower resistance coming from the central blue region and extending behind the boundaries of the plot (Fig. 3.4 (b)). The nature of these lines can be better understood from differential resistances plotted versus voltage that was measured simultaneously. From the Fig. 3.4 (c) we can see that 3 lines of lower resistance correspond to the cases of $V_1 = 0$ (horizontal line), $V_2 = 0$ (vertical line) and $V_1 - V_2 = 0$ (45° tilted line). Hence, this is the case when the whole multi-terminal junction has already switched to the finite voltage state, but there is still a supercurrent between one pair of terminals. This is a generic feature for the 3-terminal junctions that we measured and we have not seen any additional lines at different angles

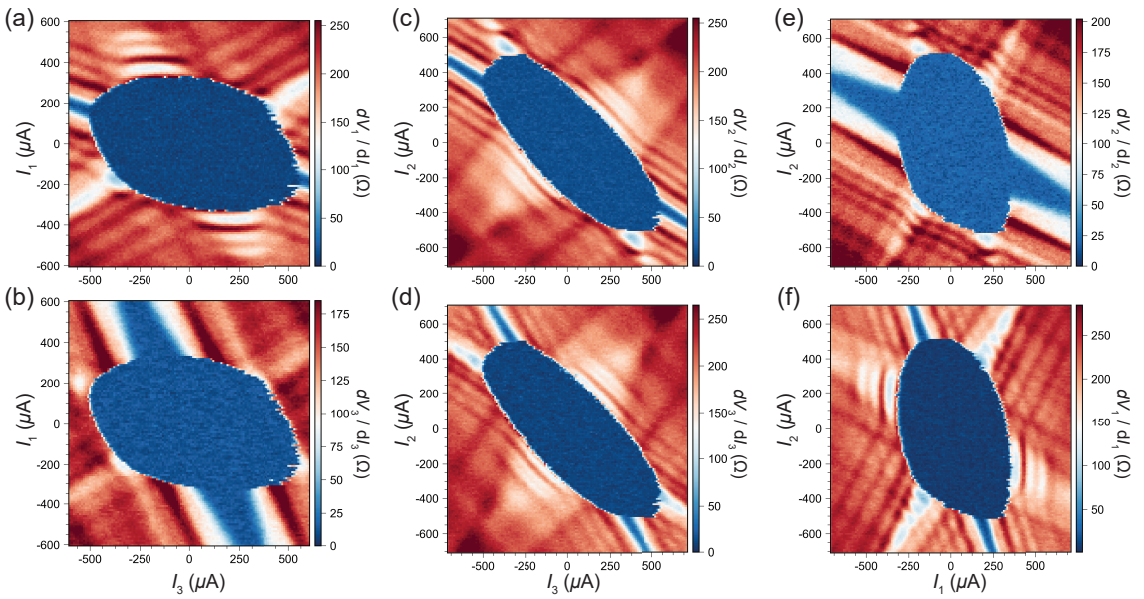

Figure 3.3: Plots of differential resistance for each pair of terminals: (a,b) terminal 2 is grounded; (c,d) terminal 1 is grounded; (e,f) terminal 3 is grounded.

that could correspond to the quartet modes or higher-order transport.

The Fig 3.5 shows the two-current measurement of a smaller junction C4 from Fig. 3.2 (b) (width of terminals ≈ 700 nm). The smaller device demonstrates similar properties, that are modified due to the junction's size. We can still see the circular superconducting region, however, of a much smaller area, which corresponds to the lower values of the critical current typical for smaller junctions. Normal resistance has also increased and now of the order of a kΩ, so $I_c R_n$ value is approximately the same as for the wide junction. There are also 3 rays corresponding to the case of supercurrent flow between only one pair of terminals when the whole junction has switched to a finite voltage state.

3.3 Critical Current Contour concept

We pause here to discuss one of the most important features of the two-current measurements - the Critical Current Contour. During the two-current measurement we simultaneously measure the voltage V_1 and V_2 of terminal 1 and 2, as well as the differential resistance dV_1/dI_1 and dV_2/dI_2,

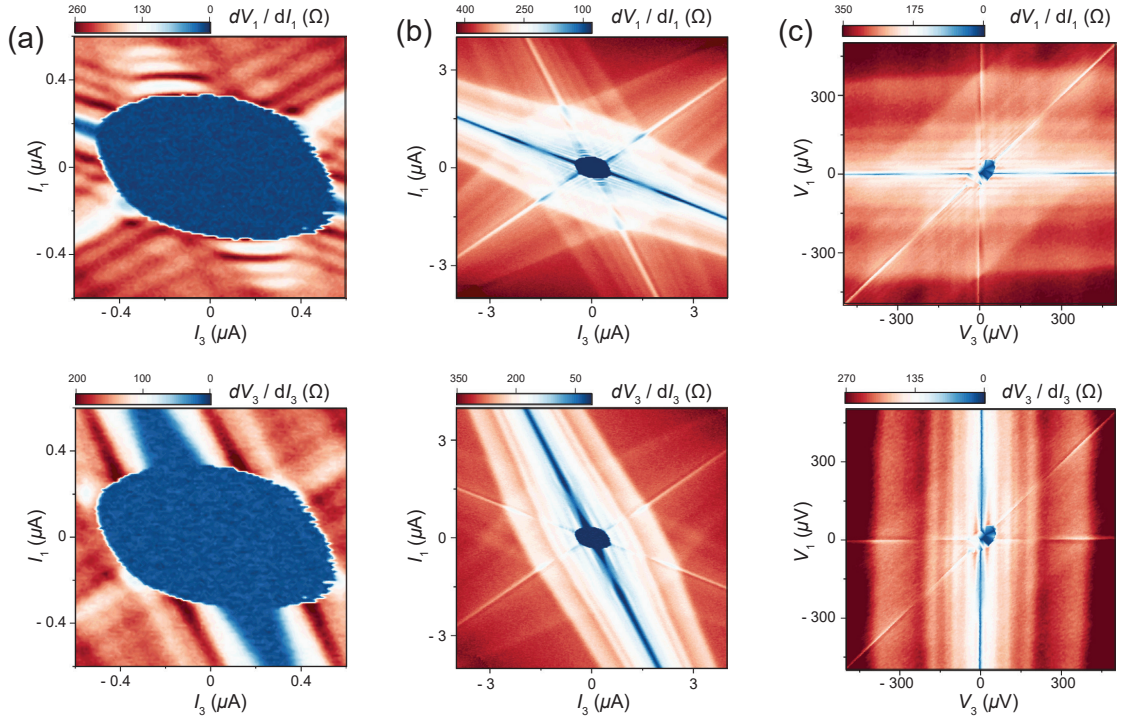

Figure 3.4: (a) Two currents plots of differential resistance dV_3/dI_3 and dV_1/dI_1 for device C5, terminal 2 is grounded. (b) Zoom out of plots from (a). (c) Differential resistance is shown on (b) as a function of voltage (voltage was measured simultaneously).

as a function of the bias current I_1 and I_2. Hence, we obtain two plots of differential resistance simultaneously. The area of the superconducting region is going to be very similar for these two plots, however, it might have some deviations. For example, in Fig. 3.4 (a,low) it seems like the superconducting state is extended outside of the circle. However, the multi-terminal junction is only in the zero-voltage regime when all voltages are zero, i.e. when supercurrent can flow between all pairs of terminals. Thus, to obtain the CCC we overlap two plots of differential resistance namely dV_1/dI_1 and dV_2/dI_2 as shown in Fig. 3.6 (a). As a result, we draw a white dashed line around zero voltage state indicating the CCC on top of the dV/dI plots as a guide for an eye as in Fig 3.6 (b). We underline the importance of both dV/dI plots to reconstruct the CCC.

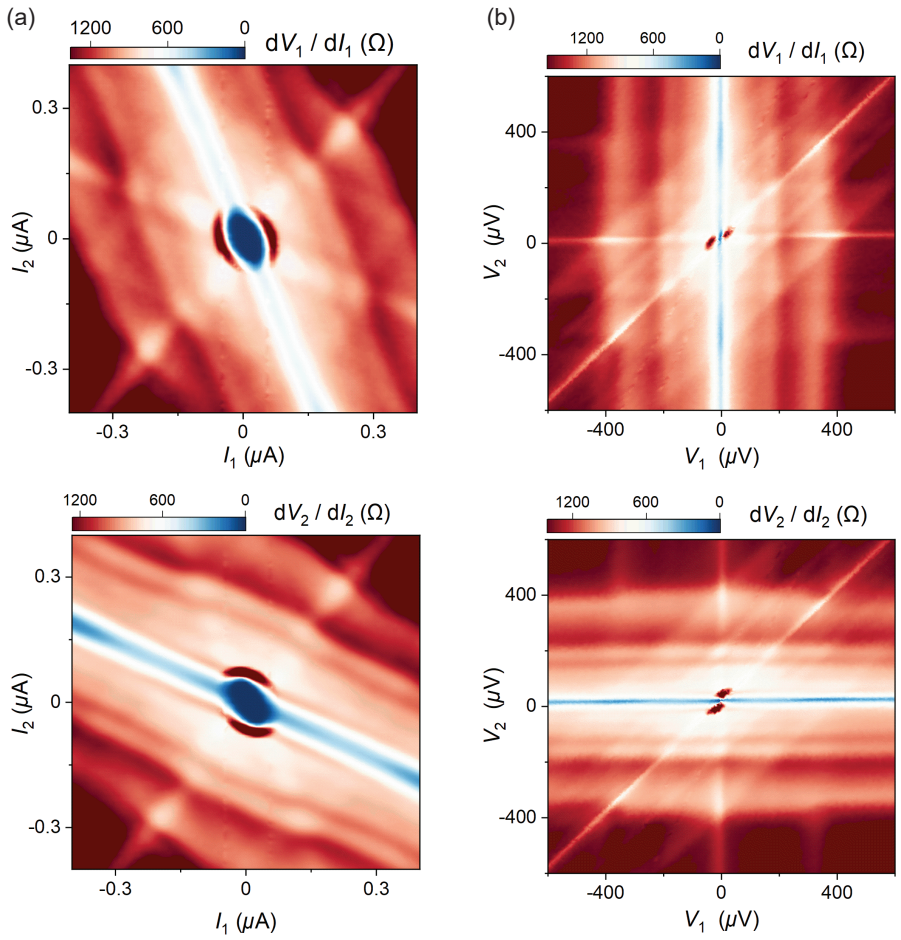

Figure 3.5: (a) Two currents plots of differential resistance dV_2/dI_2 and dV_1/dI_1 for smaller device C4, terminal 3 is grounded. (b) Differential resistance shown on (a) plotted as a function of voltage (voltage was measured simultaneously).

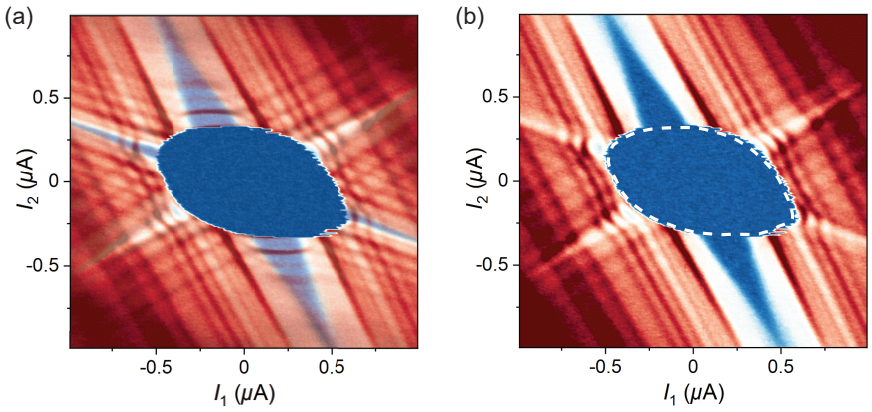

Figure 3.6: (a) Intersection of two differential resistance maps dV_1/dI_1 and dV_2/dI_2, to identify the boundary of the true superconducting region of the multi-terminal junction. (b) Resulting Critical Current Contour is shown by white dashed line plotted on top of one differential plot.

3.4 Multiple Andreev reflections in a 3-terminal junction

Another peculiar effect that could be seen from the 2 current measurements is a set of parallel lines that goes along the lines of lower resistance, which we identify as Multiple Andreev reflections (MAR). Two sets are presented in Fig 3.7 (a,b) as black dotted lines on top of the dV/dI plots in (I_1, I_2)-plane. The black dotted lines were extracted from voltage data that is presented in Fig 3.7 (c,d) and given by the conditions $e|V_1| = 2\Delta/n$, $e|V_2| = 2\Delta/n$, respectively, where n is an integer and $\Delta \approx 180$ μeV. For details see section 1.1.5. Furthermore, to verify that MAR lines for $n = (2-8)$ indeed correspond to the conditions $2\Delta/n$, we plot the resistance data as a function of $2\Delta/eV_1$ and $2\Delta/eV_3$ (Fig. 3.7(e,f)). The resonance lines match $2\Delta/n$ conditions.

The presence of high-order MAR resonances along with the induced gap Δ being close to the gap of the aluminum film indicates a nearly ballistic transport in the exposed semiconductor region and a high-transparency superconductor/semiconductor interface. Thus, the finite-voltage data confirms the high-quality of both the heterostructure and the fabricated devices. Transport in the narrower leads junction (Fig. 3.5) has all the same features described above. The MAR features are notably smeared, which may be the effect of scattering at the imperfect fabrication-defined edges. Nevertheless, a few lowest-order resonances are resolved and they give a similar value of the induced gap $\Delta \approx 180$ μeV.

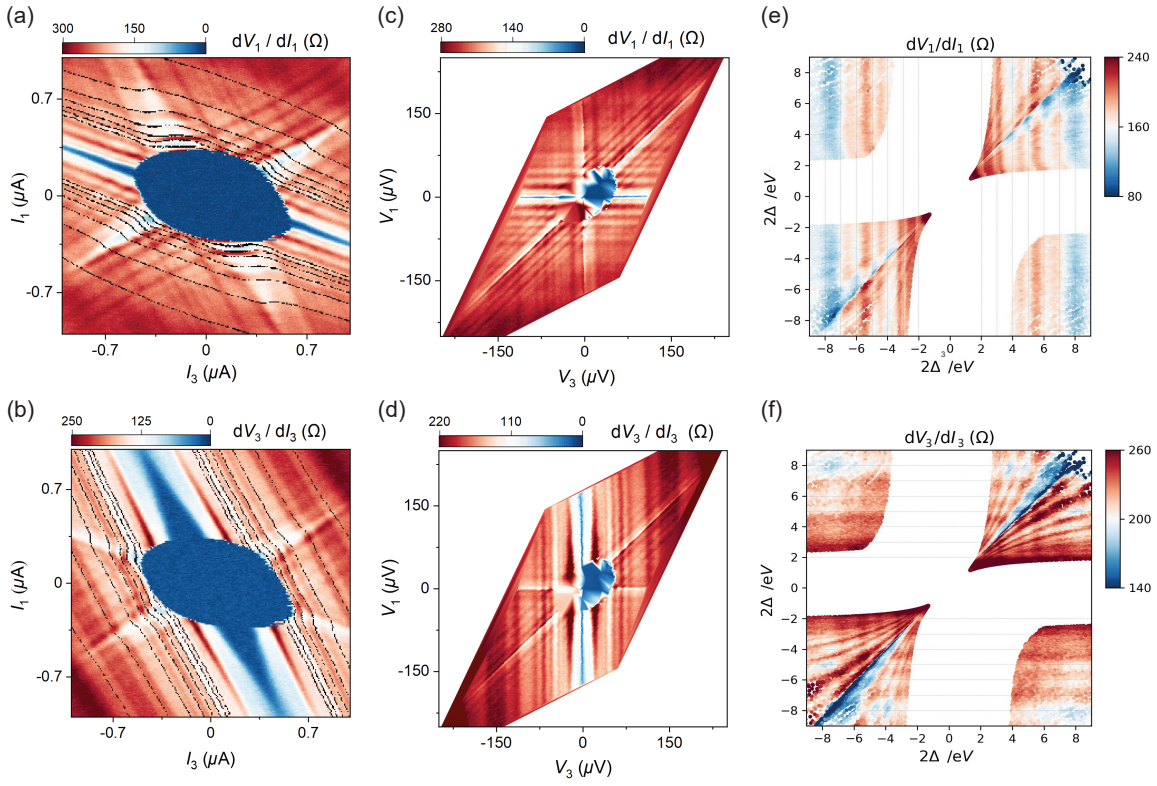

Figure 3.7: Differential resistance maps of the 3-terminal Josephson junction as a function of (a,b) current I_1 and I_3 (black dotted lines extracted from measured voltage and and given by the conditions $e|V_1| = 2\Delta/n$, $e|V_2| = 2\Delta/n$), where n is an integer; (c,d) voltage V_1 and V_3; and (e,f) as a function of $2\Delta/eV_1$ and $2\Delta/eV_3$.

3.5 Effect of magnetic field

Next, we apply a perpendicular magnetic field to the wider junction. For the data presented in this section, we used an externally-mounted homemade superconducting coil connected to Yokogawa current source. At zero magnetic field, the CCC is smooth oval-like. With the increase of the field, we see that the size of CCC is decreasing. But more importantly, the CCC is qualitatively changing the shape to triangle-like, developing sharp corners, and becoming not inversion symmetric anymore. The importance of this effect will be revealed further when we discuss the effect of the magnetic field on the 4-terminal junctions.

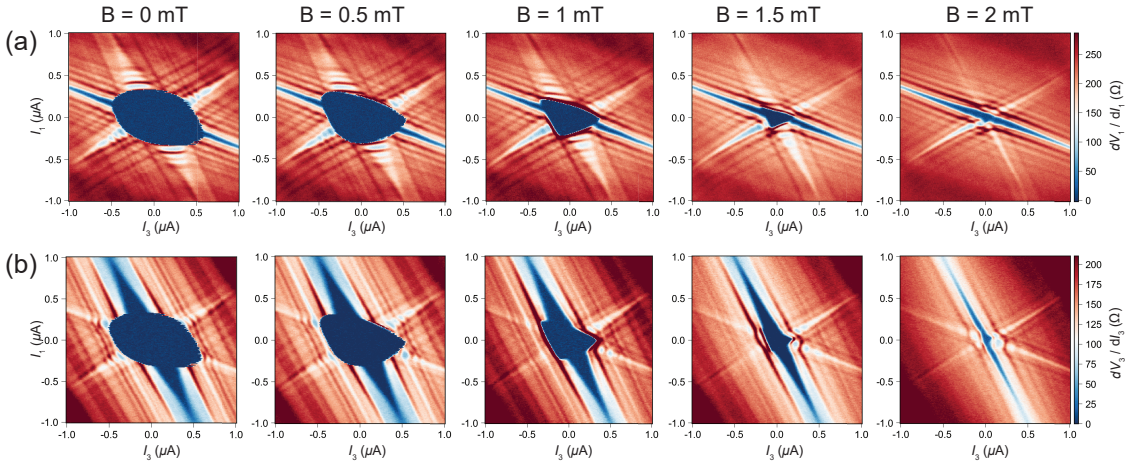

Figure 3.8: Effect of the magnetic field on a 3-terminal junction. (a,b) Differential resistance maps of the 3-terminal Josephson junction at B=0 mT (most left) and B=2 mT (most right). Note transition of CCC shape from oval to a triangle.

In Fig. 3.8 we show the CCC response to the applied perpendicular magnetic field. Top and bottom rows of plots in Fig 3.8 (a,b) correspond to differential resistance maps dV_1/dI_1 and dV_2/dI_2. For both pairs of terminals, we see a similar transition of CCC from rounded to triangular, however, the dominating vertex of the triangle is different for each pair and defined by the total phase accumulated by the electrons moving between certain superconducting terminals. The base of the triangle is stretched along the line of lower resistance corresponding to the active pair of terminals (1-2 or 3-2).

3.6 Conclusion

Now, it is time to combine all discussed features together. In the Fig. 3.9 we indicate all key findings of the 3-terminal junctions: the lines of lower resistance are labeled with corresponding voltages; the round CCC is shown by white dashed line surrounding the zero-voltage state between all 3 terminals; MAR lines, extracted from voltage measurement, are plotted as black dashed lines on $I - I$ plots. Comparison of wide and narrow junctions demonstrates that these three key features are general for hybrid semiconducting/superconducting junctions.

In this chapter, we studied the simplest case of the multi-terminal junctions - a 3-terminal junction and we used it to build our intuition for understanding the main features of the two-current measurements. The key experimental findings can be summarized as follows:

- Characterization of multi-terminal junctions can be done with two-current differential resistance maps. The main three features of such maps are critical current contour, lines of lower resistance, and high order MARs.

- CCC is necessarily oval and inversion-symmetric at zero magnetic field. A perpendicular magnetic field eliminates the contour's inversion-symmetry and CCC deforms to a triangle shape.

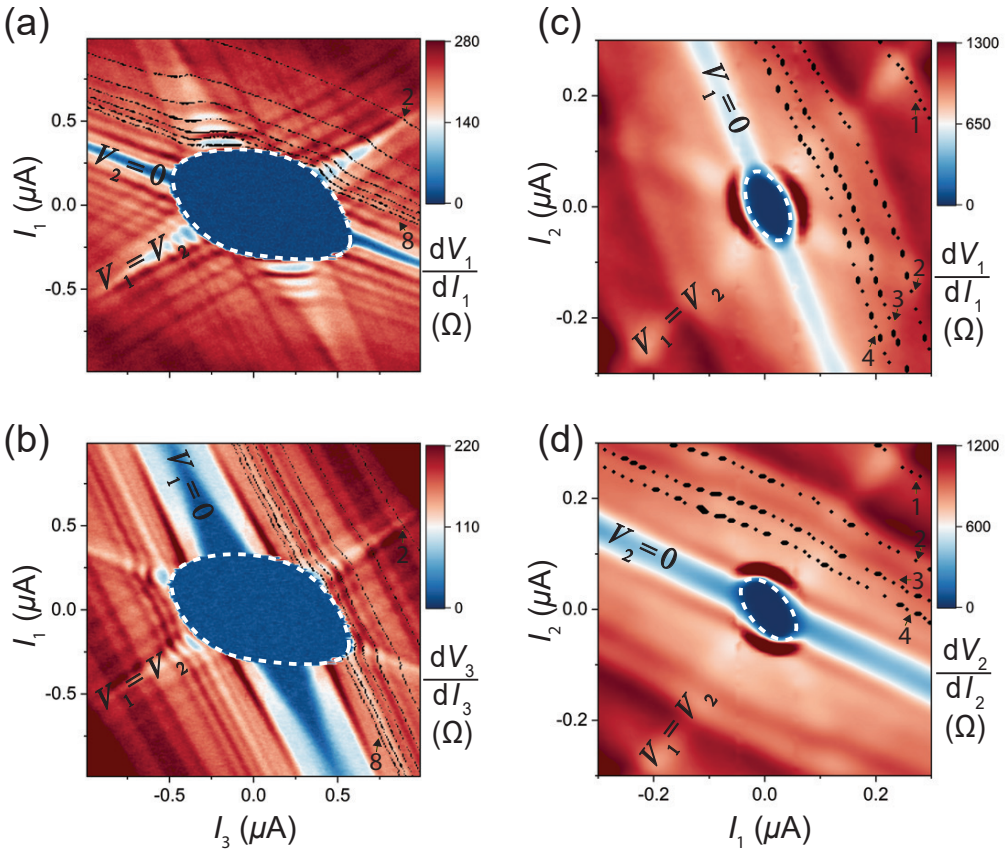

Figure 3.9: Transport properties of 3-terminal Josephson junctions. (a,b) Differential resistance maps of the device shown in Fig. 3.2 (a); terminal 2 is grounded. (c,d) Same measurement for the device shown in Fig. 3.2 (b). The CCC of both junctions are indicated by a dashed white line as a guide for the eye. The radial features in the resistance corresponding to the three conditions $V_1 = 0$, $V_2 = 0$, and $V_1 - V_2 = 0$. Some of the MAR conditions $eV_1 = 2\Delta/n$ (a,c) and $eV_2 = 2\Delta/n$ (b,d) are shown as the black lines obtained using independently measured voltages V_1 and V_2 ($n = 1 - 8$). The third set of MAR corresponding to $e(V_1 - V_2) = 2\Delta/n$ is not marked. The induced gap Δ is about 180 μeV for both devices.

Chapter 4

The multi-terminal Josephson effect: 4-terminal case

Having understood the main transport features of the three-terminal junctions, we move on to interpreting the more complex resistance maps of the four-terminal junctions. The general picture of the 3-terminal features stays unchanged, but its complexity evolves significantly. In this chapter, we present a summary of the results of transport measurements of the 4- terminal Josephson junctions. We will briefly introduce the idea of a multi-current measurement and a concept of the Critical Current Surface (CCS) for the 4-terminal junctions. Further, we will discuss how the characterization of a 4-terminal junction can be simplified by the 2-current measurement in the symmetric bias setup. The effect of the perpendicular magnetic field applied to the 4-terminal junctions manifests itself as non-trivial geometric responses of the CCCs and is an inherent transport manifestation of multi-terminal superconducting phase coherence. Finally, we will discuss the effect of gating on a 4-terminal junction. We find that a multi-terminal junction supports two transport regimes, that depend on the junction's geometry or, in some cases, the junction can be tuned between these regimes by a gate.

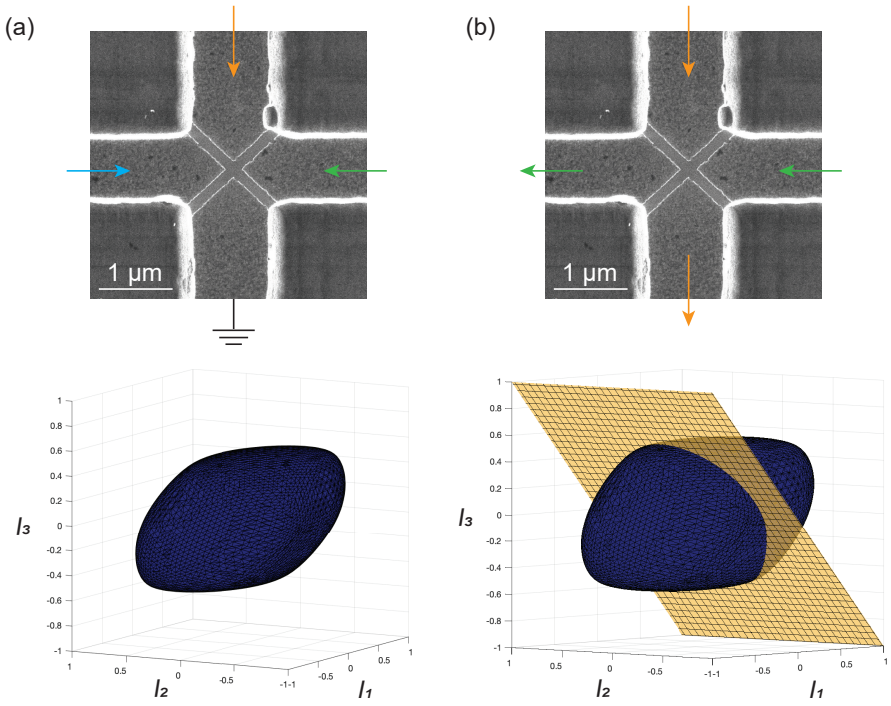

Figure 4.1: Two ways to measure 4-terminal Josephson junction. (a) Grounding one terminal and sourcing three currents will produce a 3D object of Critical Current Surface. (b) Measurement in a symmetric bias setup by pairing terminals in differential mode is equivalent to taking a slice of CCS.

4.1 Specificity of $N > 3$ junctions

One famous joke that quantum mechanics does not obey the rules of arithmetic because in quantum mechanics counting goes like "one, two, too many", is nicely demonstrated by the 4-terminal Josephson junctions.

A 4-terminal junction can be measured by grounding one terminal and sourcing currents to the other 3 terminals. The zero-voltage state of such a device could be represented by a three-dimensional manifold in the space of the three independent bias currents - Critical Current Surface (Fig. 4.1 (a)). However, it is very impractical to perform that type of measurement due to its complexity. For example, to measure one plot of such type would take a few days.

Instead, we can perform symmetric bias measurement (Fig. 4.1 (b)) by pairing the four terminals into three possible combinations $((1,2),(3,4))$, $((2,3),(4,1))$, and $((1,3),(2,4))$, i.e. apply symmetric currents to each pair such that $I_1 = -I_3 = I_{13}$ and $I_2 = -I_4 = I_{24}$, etc., which is equivalent to

taking the slices of the Critical Current Surface. Consequently, the zero-voltage state can be characterized by three two-dimensional CCC defined in the planes of the currents $(I_{12}; I_{34})$, $(I_{23}; I_{41})$, and $(I_{13}; I_{24})$, respectively (Fig. 4.2. The latter biasing configuration is particularly interesting because the two currents I_{13} and I_{24} are forced to flow across each other in the central junction region. We use the differential resistance data taken in the $(I_{13};\ I_{24})$-plane in order to review the generic transport features encountered in our four-terminal junctions.

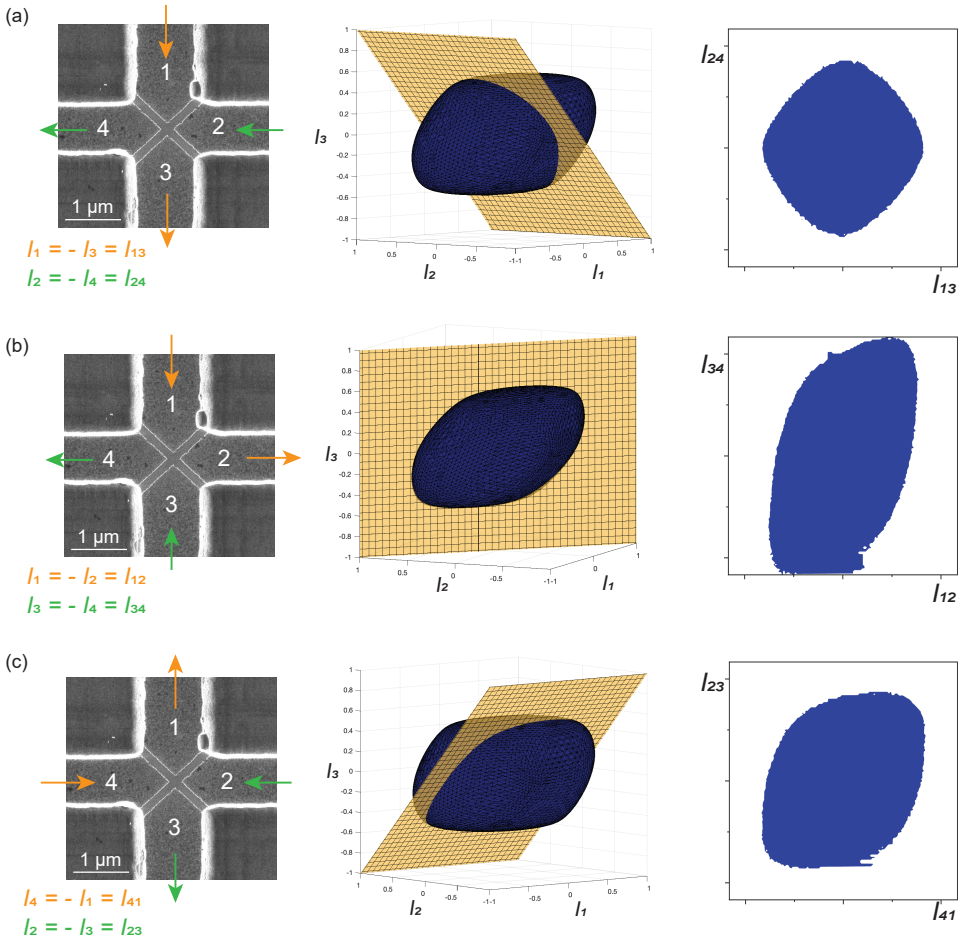

Figure 4.2: Differential symmetric biasing combinations for a 4-terminal junction and corresponding planes in 3D space. The 3D CCS was generated using the random scattering matrix method. The right column presents the data that matches CCC of the slices.

4.2 Four-terminal Josephson junction characterization

To characterize the 4-terminal junction we perform a similar analysis as for the 3-terminal junctions. In symmetric bias measurement setup, measuring only the two differential resistances dV_{13}/dI_{13}, dV_{24}/dI_{24} gives sufficient information for identifying the zero-voltage state and constructing the critical current contour. The CCC is generated by overlapping zero-voltage regions of two plots of differential resistance (Fig. 4.3 (a,b))) that are taken simultaneously. Here, similarly to the 3-terminal junctions, the zero-voltage region in the $(I_{13}; I_{24})$-plane satisfies $dV_{13}/dI_{13} = dV_{24}/dI_{24} = 0$.

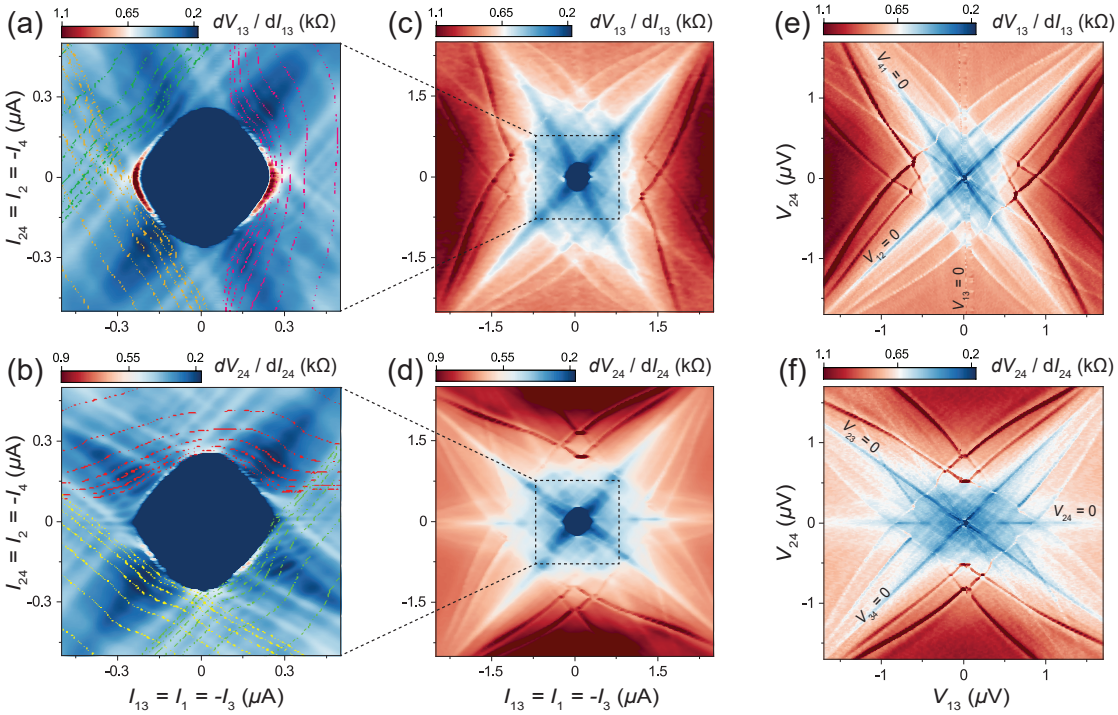

Figure 4.3: Transport in a four-terminal junction. (a,b) Zoom-in onto the zero-voltage region of differential resistance across the terminal pair (2,4) and (1,3) in the device shown in Fig. 4.1. The colored lines represent the MAR conditions: (red) $eV_{24} = 2\Delta/n$; (yellow) $eV_{23} = 2\Delta/n$; (lite green) $eV_{34} = 2\Delta/n$; (magenta) $eV_{13} = 2\Delta/n$; (orange) $eV_{41} = 2\Delta/n$; (dark green) $eV_{12} = 2\Delta/n$. Here $\Delta \approx 160$ μeV and $n = 5$. (c,d) Zoom out of differential resistance plots. (e,f) Differential resistance plots versus voltage. The six radial features represent the conditions $V_{12} = 0$, $V_{23} = 0$, etc., as marked directly on the plots.

Outside the zero-voltage region, there are six radial directions of reduced differential resistance,

corresponding to zero voltage across only *one* of the six terminal pairs. It could be seen from the $V-V$ plots in Fig. 4.3 (e,f), where we label each line for better understanding. Also, in Fig 4.4 (a,b) the lines of lower resistance (marked with blue and red arrows) match the colored lines of zero-voltage in Fig. 4.4 (c,d), which correspond to the voltage being zero between only one pair of terminals.

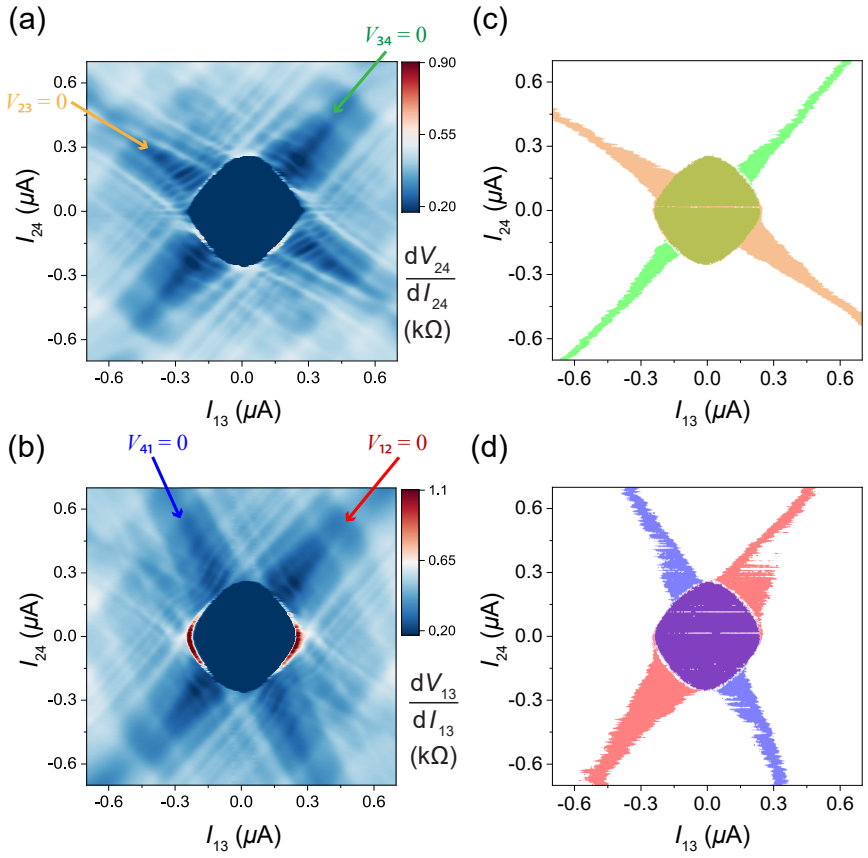

Figure 4.4: Differential resistance maps of the 4-terminal junction (a,b) and zero voltage regions across 4 pairs of terminals (c,d), measured simultaneously. The colored regions in (c,d) correspond to $V_{12}=0$ (red), $V_{23}=0$ (yellow), $V_{34}=0$ (green), $V_{41}=0$ (blue).

In Fig. 4.3 (c,d) immediately outside the CCC, there is an intricate structure in the differential resistance map. We believe most of this structure can be also explained by MAR involving the voltage drops across the six possible terminal-pairs. For example, using independently-measured voltages, we indicate the equipotential lines in the $(I_{13};\, I_{24})$-plane corresponding to the $n=2-8$

MAR conditions directly on top of the data in Fig. 4.3 (a,b) (colored dashed lines). Each color corresponds to the specific pair of terminals. Notably, we found evidence for the 8th-order MAR involving the more separated terminal pairs $(1;3)$ and $(2;4)$. Such an observation confirms that every pair of terminals in our four-terminal junction is connected by transparent channels across the semiconductor.

Additionally, to check that measuring two plots of differential resistance is indeed sufficient to ensure that the voltage between all the six terminal pairs is zero we measured voltages across 4 pairs of terminals simultaneously. In Fig. 4.4 the colored regions correspond to zero voltage across certain pair of terminals. An overlap of four colored central regions Fig. 4.4 (c,d) matches the shape of CCC obtained from the overlap of $I - I$ maps.

4.3 Effect of magnetic field

To further study the properties of the 4-terminal junction we apply a perpendicular magnetic field. Fig 4.5 shows the differential resistance across the different terminal pairs that were measured for $B = 0$ mT and $B = 2$ mT as a function of the three possible symmetric current pairs $(I_{13}; I_{24})$, $(I_{12}; I_{34})$, and $(I_{41}; I_{23})$. For each combination and terminal pairs, we can see an oval or round shape of CCC at $B = 0$ mT that gradually changes with the applied field as the field adds an extra phase to the ABSs. Although for each combination of biasing current the modification goes differently, we can note similarities in the pattern of the change: the CCC shrinks and develops vertices, i.e. the shape transforms from smooth oval to asymmetric and irregular.

When we consider the case of biasing adjoint terminals $(I_{12}; I_{34})$, and $(I_{41}; I_{23})$ in Fig. 4.5 (b,c), we can see one line of lower resistance becomes more prominent than the others and CCC takes triangle-like shape with the base of the triangle stretched along this line. However, in the case of $(I_{13}; I_{24})$ pairing when two currents are forced to flow perpendicular to each other, the CCC develops a more complicated shape with extra vertex. Note that flipping the sign of magnetic field is equivalent to inverting the contours around the origin (lowest part in Fig. 4.5).

The field $B = 2$ mT dramatically modifies the zero-voltage region in each of the three maps (Fig. 4.5). Such a field corresponds to approximately 1/5 of flux quantum piercing the exposed

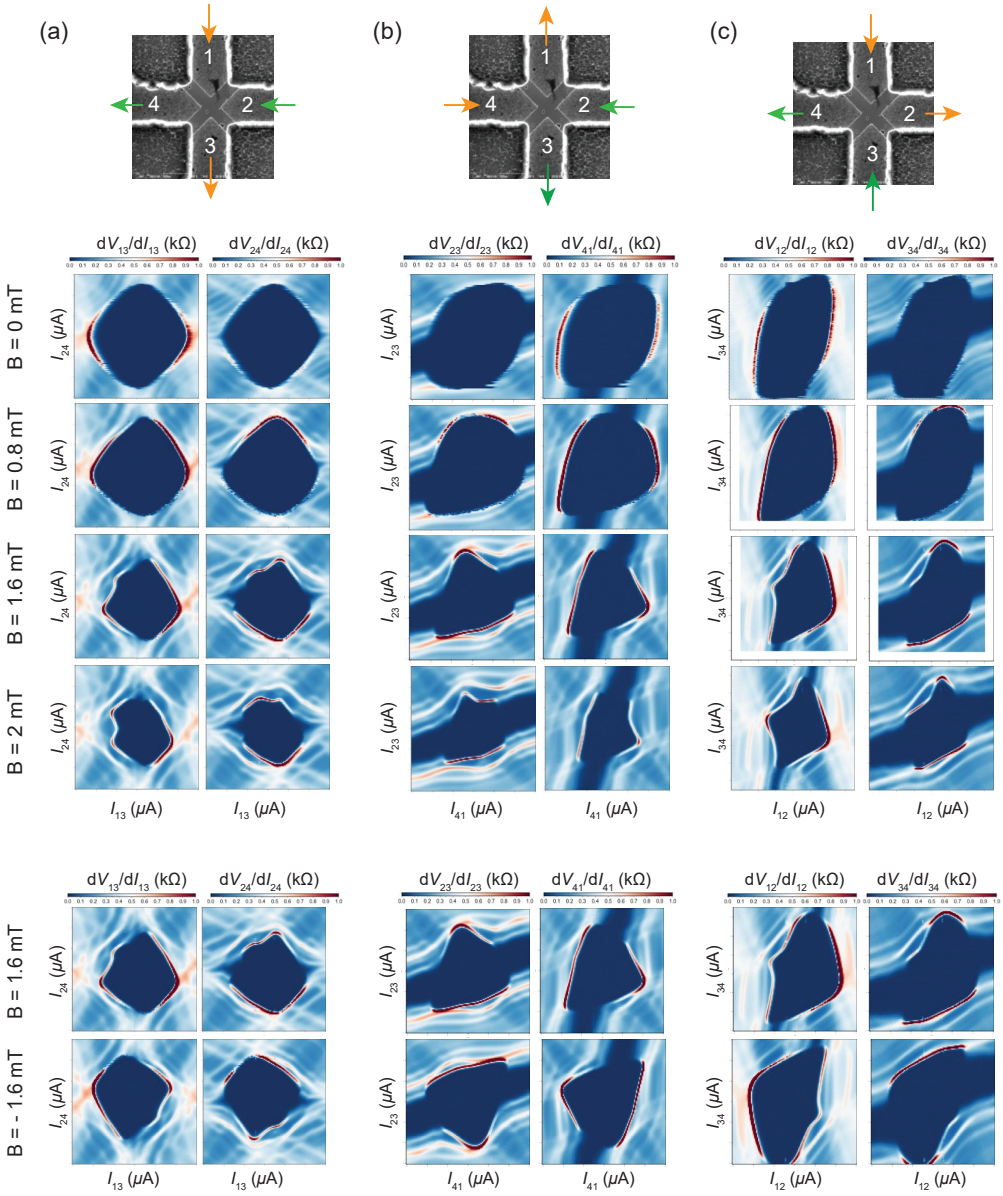

Figure 4.5: Effect of magnetic field on a 4-terminal junction for three possible current combinations. (a) Differential resistance maps of $(I_{13}; I_{24})$ pairs, (b) of $(I_{41}; I_{23})$ pairs and (c) of $(I_{12}; I_{34})$ pairs. The six columns show the evolution of CCC with increasing magnetic field for all pairs of terminals. The bottom part of two rows compares the data at $B = 1.6$ mT vs. $B = -1.6$ mT, which is equivalent to inversion of the CCC around the origin.

semiconductor in the junction, although in reality, the flux is probably larger due to the flux focusing effect. We avoided measuring at a higher field as it starts to gradually suppress superconductivity in aluminum.

To better understand CCC transformation in the magnetic field we visualize each of the three extracted CCC by painting in blue the zero-voltage region and setting everything else to white (Fig. 4.6). The first column of Fig. 4.6 (a) shows the CCC at $B = 0$ (dark blue), the second column compares the CCC at $B = 0$ mT (light blue) and $B = 1.2$ mT (solid blue). Each following column follows this logic: compares CCC corresponding to the magnetic field value labeled on top of the column with CCC of the previous column.

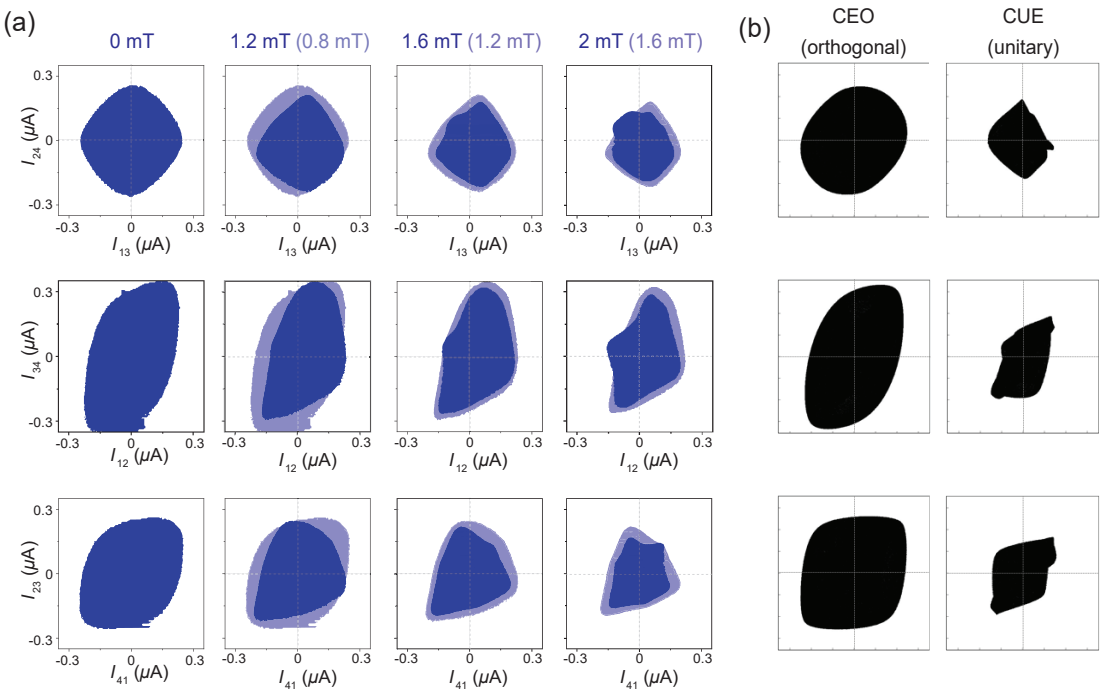

Figure 4.6: Magnetic field modulation of three critical current contours of a symmetrically-biased 4-terminal junction. (a) The solid blue color indicates the zero-voltage condition on the two bias currents. The copy of the measured shape at a previous field is added in a semi-transparent color for ease of comparison. The range is 100 nA/div along both axis. (b) Scattering matrix theory prediction using a random matrix $\hat{S}$ chosen from the circular orthogonal ensemble and circular unitary ensemble.

At zero field, all the three contours are convex and symmetric with respect to inversion around the origin. The field $B = 1.2$ mT distorts the CCC such that they are still convex but no longer

inversion-symmetric. A qualitatively new feature arises on increasing the field to $B \approx 1.6$ mT: the local curvature changes its sign around several points of the contour. For even stronger field $B = 2$ mT such features become more pronounced. Note that although the contour's geometry in the presence of the B-field is qualitatively different, their total area is reduced only by about a factor of two. Such dramatic sensitivity of the CCC geometry to magnetic flux piercing the semiconductor is indicative of the phase-coherent supercurrent flow across the multiple terminals of the junction.

In the last two columns of Fig. 4.6 (b) we compare measured critical current contours to a theory. As discussed in Chapter 1, the supercurrents are determined by the phase-derivatives of the junction's ground state energy, while the ground state energy itself is related to the junction scattering matrix $\hat{S}$ [56]. In the absence of microscopic details, it is common to model $\hat{S}$ as a random matrix. The scattering matrix $\hat{S}$ is assumed to belong to one of the ensembles of random unitary matrices restricted only by the system fundamental symmetries. Three ensembles with different scattering symmetry classes are known: circular orthogonal ensemble (COE), which respects both spin-rotation and time-reversal symmetry; circular unitary ensemble (CUE), describing broken time-reversal symmetry, and circular symplectic ensemble (CSE), respecting time-reversal symmetry but not spin-rotation symmetry [55]. A generic property of a COE contour is a strictly positive curvature. To find a matrix $\hat{S}$ from this ensemble which reproduced all three measured critical current contours at $B = 0$ (compare Fig. 4.6 (a - first column) and Fig. 4.6 (b - first column) the number of scattering matrices were generated, then those matrices that match data the best were selected. More details on the procedure can be found in section 1.1.6. The CUE contours are drastically different. The curvature is now changing sign at random. This behavior mimics remarkably well the data at $B = 2$ mT.

To summarize, the change of CCC shape under the magnetic field from rounded to irregular indicates the transition between CEO to CUE symmetry ensemble. I.e. rounded CCC corresponds to the case of time-reversal symmetry being preserved and the irregular shape of CCC indicates broken time-reversal symmetry as expected in the magnetic field.

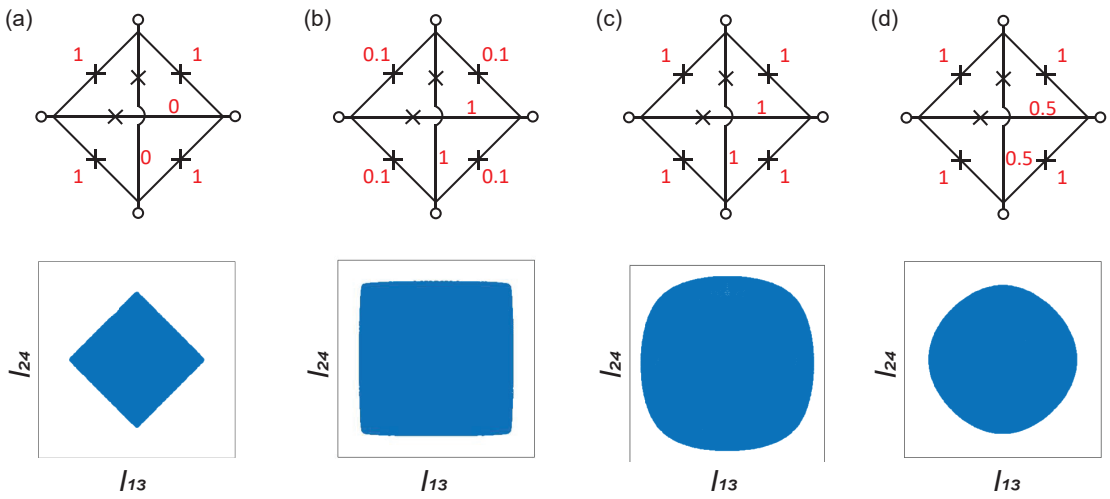

Figure 4.7: Representation of the 4-terminal junction in terms of six junction model. Red numbers represent the coupling strength between different superconducting terminals and the bottom raw shows simulations of corresponding CCC shape.

4.4 Junction's geometry and multi-terminal regime

An important question to ask in case of the X-shaped junction is if this is indeed one multi-terminal junction or rather a combination of the four 2-terminal junctions? To answer this question we first study the behavior of the CCC using the six junctions network model.

As can be seen from Fig. 4.7 we investigate the shape of CCC depending on coupling strength between superconducting terminals using a 6 junction model. When the coupling between adjoint terminals is strong (unity) and the coupling between opposite terminals is negligibly small, the CCC has a rhombus shape (Fig. 4.7 (a)). In contrast, when the coupling between opposite terminals is strong, but between adjoint is weak, the CCC takes an almost square shape (Fig. 4.7 (b)). Although this scenario is very unlikely to take place in reality (adjoint terminals coupling will always be stronger or comparable to opposite terminals coupling), it is useful for building our intuition. Equal coupling strength of all six links will produce a rounded square (Fig. 4.7 (c)) and the last case of strong adjoint terminal coupling and intermediate opposite terminal coupling (Fig 4.7 (d)) produces a round shape of CCC. Hence, the coupling strength between terminals will directly affect the shape of CCC. Now the question is how this coupling could be controlled? The favorite activity of experimental physicists is to turn everything into a control knob.

A simpler way to control the strength of the couplings is by choosing different geometries of the junctions. Based on the 6-junction model analysis we identify three types of junctions based on their geometry: wide junctions, intermediate junctions, and narrow (or pointy) junctions (Fig. 4.8). We introduce such categories based on the length of the interface between adjoint terminals. This way, we can roughly say that the junctions with $L \geq 1.5$ um is categorized as wide, $L \leq 1.5$ um is intermediate and the junctions with needle-like terminals as narrow (or pointy).

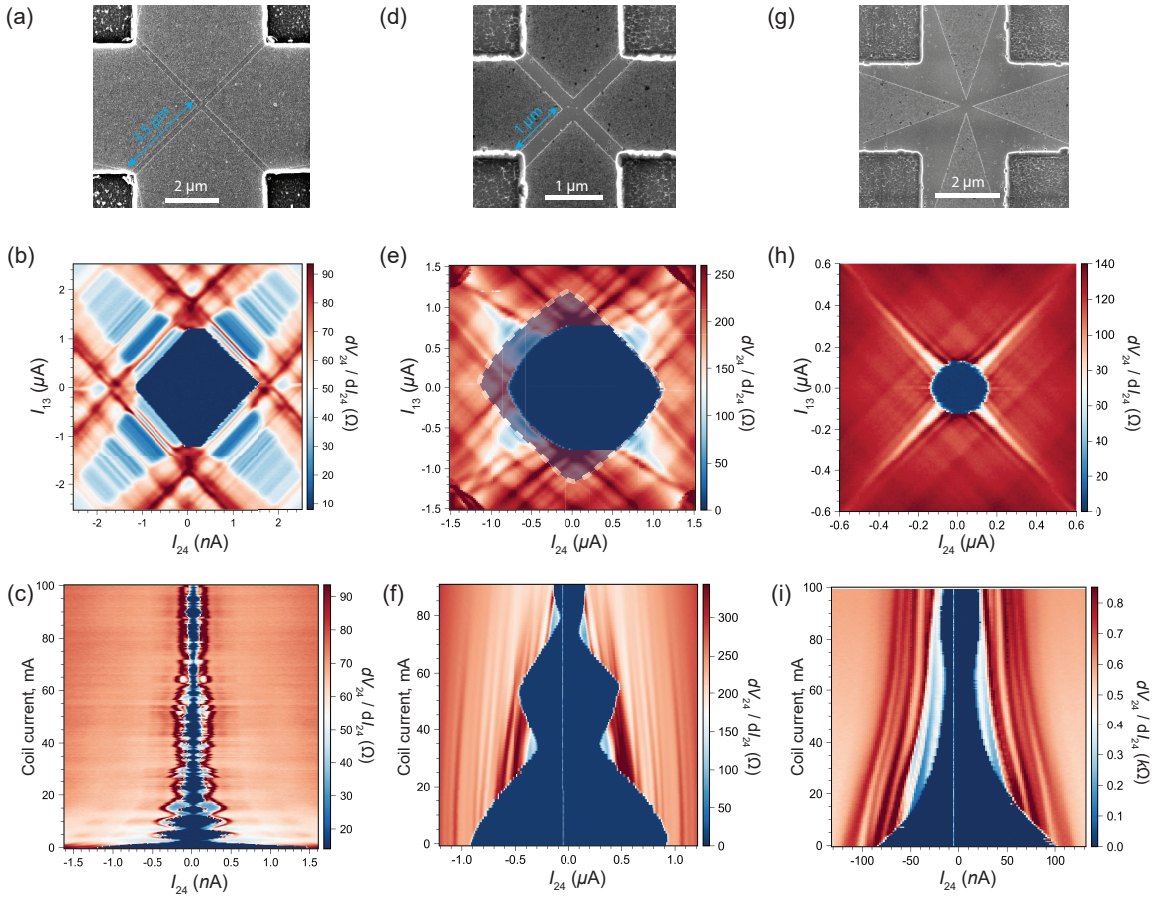

Figure 4.8: Comparison of the geometry of the 4-terminal Josephson junctions (a, d, g) and corresponding data presenting CCC for each geometry (b,e,h). (c,f,i) Fraunhofer pattern measured for one pair of terminals for each geometry.

The reason for such categorization could be understood once one start to think about the very first definition of the multi-terminal junction: the ABS's wave function is nearly equally present in

all of the terminals. I.e. the multi-terminal effect is present in junctions of all geometries, however, it might be hidden by the competing effect coming from the ring of 2-terminal junctions.

Speaking in terms of the 6 junctions model, in wide junctions the coupling of the adjoint terminal will strongly dominate the value of coupling between opposite terminals, up to the degree that opposite terminal coupling can be neglected. By decreasing L the adjoint coupling will also be decreased making the multi-terminal effect more prominent. Hence, we can reformulate the categorization rule in terms of multi-terminal effect: in wide junctions multi-terminal effect so small that it could be neglected and CCC is rhombus-like (Fig. 4.8 (a,b)); in intermediate junctions, the effect is weakly noticeable and manifests as slight rounding of the rhombus (Fig 4.8 (d,e)); in narrow junctions, the strength of the multi-terminal effect is comparable with 2-junctions contribution and CCC takes perfectly rounded shape (Fig 4.8 (g,h)).

Change of junction's geometry obviously leads to change of the size of the junction, which could be seen from magnetic field data (Fig 4.8 (c,f,i)). For the wide 4-terminal device the I_c modulates very quickly with the applied perpendicular magnetic field, the first node appears at a few mA of coil current. However, for the intermediate junction, the first node appears only at 37 mA and for the narrow junction node is less prominent and appears only at $60mA$. Although the exposed 2DEG area is much larger for the narrow device, the effective area of the junction is much smaller and focused at the very center where all 4 terminals meet. For the narrow junctions we estimate the number of transport channels to be lower than 10.

4.5 Effect of top-gating on CCC

One advantage of our specific hybrid semiconductor/superconductor materials platform is that the carrier density in the junction's scattering region can be tuned using a top-gate. This was achieved by depositing a thin dielectric layer on top of the pre-fabricated four-terminal junction device shown in Fig. 4.9 (a) and then covering the junction completely by a metal film electrode which is the top-gate. The gate electrode consists of a 5 nm Ti adhesion layer and a 100 nm Au electrode layer. A 50 nm-thick aluminum oxide film was deposited using atomic layer deposition at CUNY cleanroom.As a result, the application of a sufficiently large negative voltage (around -5 V for this

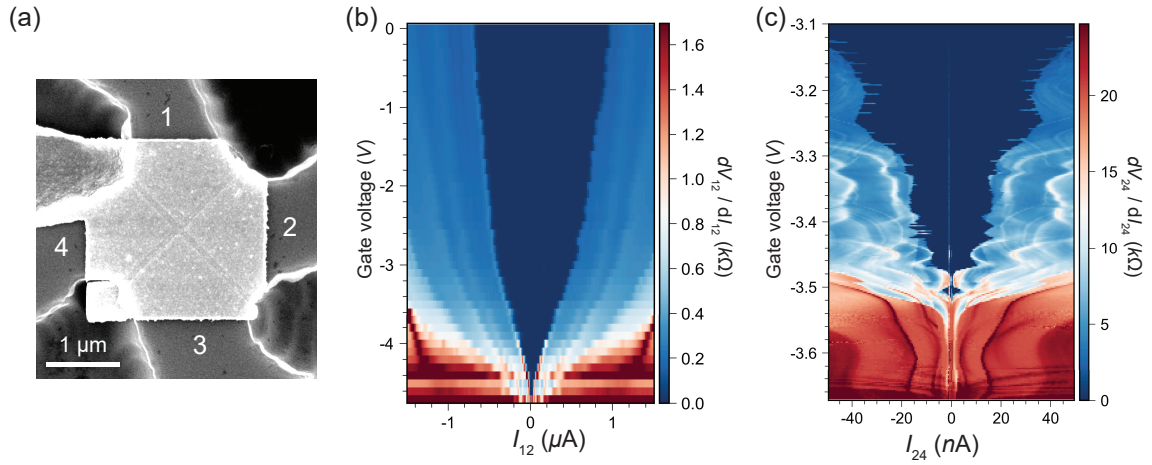

Figure 4.9: (a) SEM image of the 4-terminal junction with a top gate. (b) Gate dependence of the critical current for one pair of terminals, at approximately $V_G = -5$ V the junction is fully depleted. (c) Zoom-in on gate dependence of the identical device.

device) to the top-gate completely suppresses the conductance across every terminal's pair (Fig. 4.9 (b)). To ensure the supercurrent was not suppressed by the heating caused by the large gate voltage, we simultaneously measured the leakage current between gate and the substrate. The rule of thumb for our measurements was that leakage current should not exceed $50pA$ value.

Another peculiar effect of I_c modulation was observed at sufficiently high gate voltages, near full depletion. Such oscillations were present in both 3- and 4-terminal devices, however, their intensity or pattern was changing from device to device. Similar to the nanowire experiments such oscillations can be associated with energy levels broadening [65].

In Fig. 4.10, we show the evolution of CCC in a top-gated four-terminal junction at five different gate voltages V_g. We focus on the differential resistance data in the $(I_{13}; I_{24})$-plane as we did for the non-gated device. At $V_g = 0V$, the junction has strong hysteresis which prevents us from measuring a true shape of CCC. In order to reconstruct the real shape of the zero-voltage region we performed four scans in four directions going from negative to positive values of rapidly changing current (either I_{13} or I_{24}) and then changing the direction by going from positive to negative. Then we exchange pairs and repeat these two measurements. In the end, we get four plots and overlap them to produce the true shape of a zero-voltage state. We show it by drawing a semi-transparent blue rhombus and show true CCC by the white dashed line in Fig. 4.10. This way, we can see that the

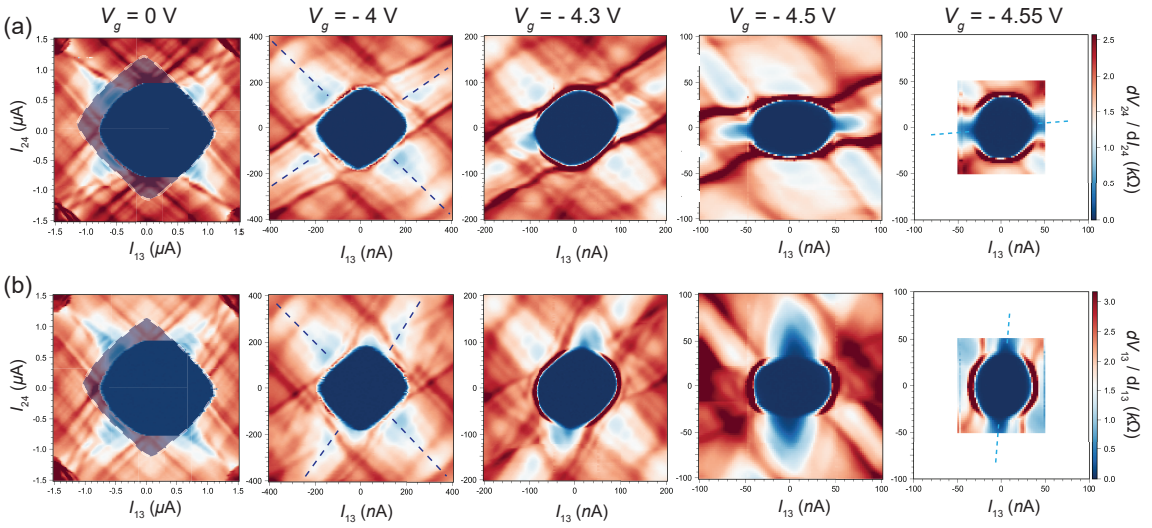

Figure 4.10: Effect of top-gating on a four-terminal junction. CCC of the 4-terminal intermediate junction response to top-gating for both pairs of terminals. At zero voltage strong hysteresis prevents from measuring the true shape of CCC, so we show the result of one measurement withdrawn on top blue rhombus that was reconstructed from four measurements with a sweep in four directions. At higher gate voltage CCC transforms from rhombus to circle indicating the junction's transition from "2-terminal network" to a multi-terminal regime. The change of prominence of rays of lower resistance confirms such transition (shown by blue dashed lines).

shape of CCC at $V_g = 0V$ is a rhombus, which corresponds to the case of large coupling between the adjoint terminal and wide junction scenario.

At $V_g = -4V$ the hysteresis is decreased, so taking only one scan is sufficient. The shape of CCC is still rhombus, but the corners start to round indicating a small contribution from opposite terminals coupling. The CCC evolving into a circle at $V_g = -4.3V$, now the shape is very similar to the one presented in Fig. 4.3: it obeys the inversion symmetry but it is notably asymmetric with respect to flipping one of the two axis. Moving to $V_g = -4.5V$ deforms the CC into a nearly an oval stretched along the I_{13}-axis. Moving a bit further down in gate voltage to $V_g = -4.55V$, the CCC becomes nearly a circle with a radius of about 30 nA. Such a current scale corresponds to the critical current of a single transparent channel. On the other hand, the product of such a current scale with the normal resistance scale (a few $kOhm$) is about 100 uV and this is close to the value of the induced gap $\delta = 180$ uV. Thus, we conclude that top-gating can readily bring our junctions into the regime of one or a few scattering channels per terminal. Moreover, the junctions of intermediate

type are originally closer to the wide junction regime (ring of four 2-terminal junctions) but can be driven to the multi-terminal regime with the top-gating.

Also, note the position of the lines of lower resistance. At $V_g = 0$ and even at $V_g = -4\ V$ we can see prominent lines of lower resistance at $30° - 45°$ tilt, we indicate them with dashed blue lines at Fig. 4.10 ($V_g = -4\ V$). These lines correspond to supercurrent flow between one pair of adjoint terminals, i.e. $V_{12} = 0$, $V_{41} = 0$, $V_{23} = 0$ or $V_{34} = 0$ as shown in Fig. 4.3 (e,f). At gate voltage up to $-4V$ the lines of $V_{13} = 0$ or $V_{24} = 0$ are not visible. Their traces start to form at $V_g = -4.3\ V$ and become more prominent at $V_g = -4.5\ V$ (Fig. 4.10 (right column)). That also indicates that top-gating suppresses the coupling between adjoint terminals, so the coupling between opposite terminals becomes more prominent and manifests itself in visible rays of lower resistance as well as circular CCC.

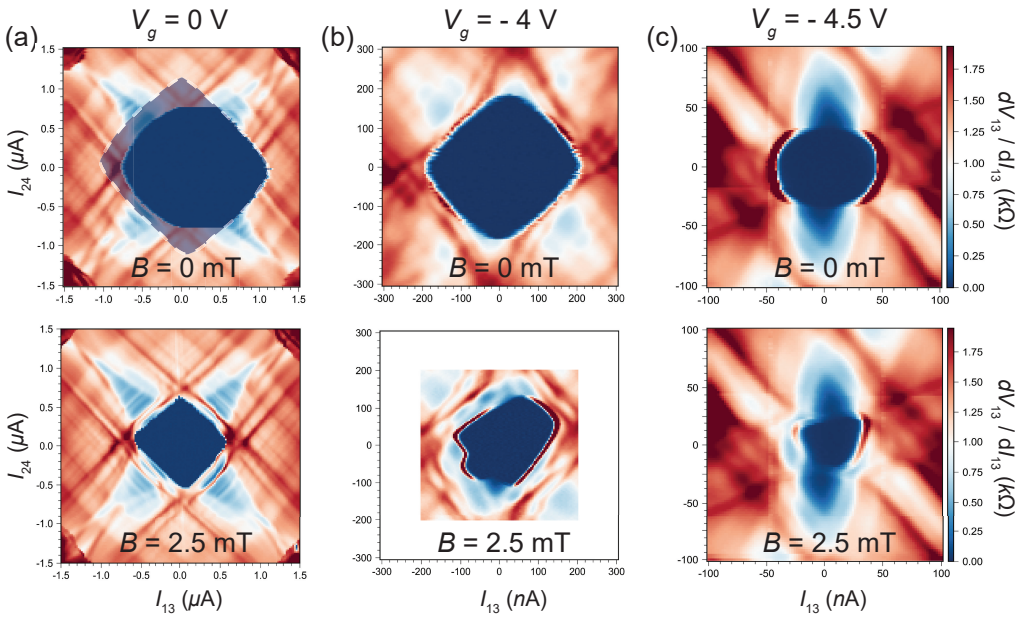

Figure 4.11: Effect of top gating and magnetic field on the 4-terminal junction. (a) At zero gate junction is in the "wide" regime and under applied magnetic field CCC shrinks, but stays rhombus. (b) At $V_G = -4$ V CCC is still rhombus in the absence of magnetic field, but develops prominent irregularities and becomes asymmetric at $B = 2.5$ mT. (c) At $V_G = -4.5$ V CCC takes a circular shape and modifies into the triangle in the presence of the magnetic field.

One more way to probe the transition between a 2-terminal network to the multi-terminal regime is to analyze the effect of the magnetic field. Fig 4.11 shows the effect of the gate and the magnetic

field. Measuring CCC at different gate values can be compared to taking the photo of the junction's state while measuring CCC in the presence of a magnetic field is similar to taking the x-ray. Application of the B-field at $V_g = 0V$ shrinks the CCC, but the shape still stays rhombus. However, B-field drastically modifies CCC at $V_g = -4V$ producing an irregular shape that is very similar to the one presented in Fig. 4.6. Although CCC still seems rhombus at $V_g = -4V$, the magnetic field reveals high contribution from multi-terminal effect. When applying B-field at $V_g = -4.5V$ the CCC takes triangle-like form, but can't develop prominent irregularities due to the low value of I_c.

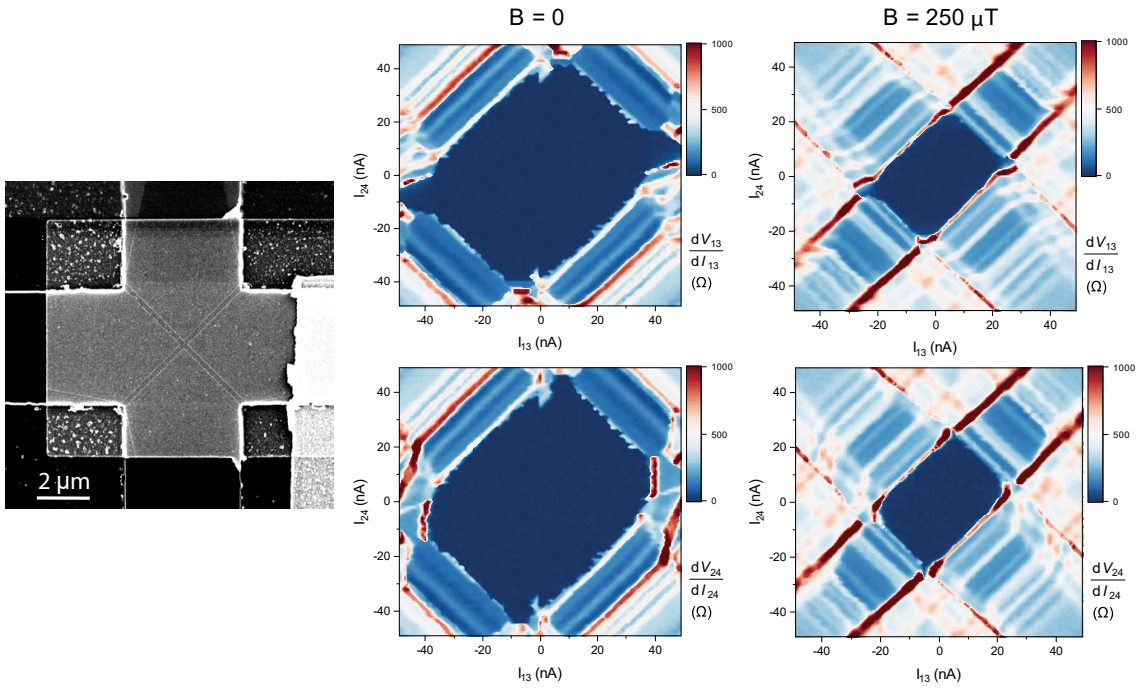

Figure 4.12: Differential resistance maps of a 4-terminal wide junction at (a) zero field and (b) field of $0.25\ \mu$T.

Finally, let us stress that one does not expect coherent multi-terminal scattering to occur in junctions with too wide leads. In that case, the scattering matrix in Eq.1.22 looses its multi-terminal structure and breaks into blocks representing two-terminal scattering. As a consequence, the CCC would loose the geometric properties discussed previously. Recall that by definition the multi-terminal Josephson effect takes place when wave functions of ABS are present in all superconducting

terminals. In the junctions with too wide leads (width of 3.5 μm) the coherent multi-terminal transport will take place only in the very center of the junction, but 2-terminal transport will drastically dominate. This way, the contribution from multi-terminal transport will be negligibly small.

As a sanity check, we have fabricated intentionally wide four-terminal junctions and applied the gate voltage to reduce the normal conductance scale to that of our small coherent junction devices. Indeed, the CCC of such wide junctions are dramatically different from those narrow type (Fig. 4.12), but they bear similarities to those reported in two recent experiments [66, 67]. The contours are no longer convex in zero field and they shrink on increasing the field while keeping their inversion-symmetry. Although increasing magnetic field results in slight rounding of the vertices or asymmetry of the rhombus, CCC do not go into a circle or demonstrate irregular deformations. In this case, supercurrent transport must be modeled using a network of 2-terminal Josephson junctions, which is equivalent to Beenakker's scattering matrix approach with block-diagonal scattering matrices coupling different pairs of terminals.

4.6 Conclusion

In this chapter, we explored 4-terminal hybrid semiconductor/superconductor devices.The key experimental findings can be summarized as follows:

1. Characterization of any multi-terminal junction can be done by performing two-current measurements in a symmetric biasing setup. Two-current plots have the same set of features as plots of 3-terminal junctions: CCC, six rays of lower resistance, MARs between all six pairs of terminals.

2. Four-terminal junctions can be either in the multi-terminal regime or in the "2-terminal network" regime. We introduce the categories of wide, intermediate, and narrow junctions based on the coupling between six terminals and the corresponding shape of CCC. Intermediate junctions can be tuned between the last two regimes by a top-gating.

3. CCC responses to the magnetic field and top gating. For the junctions in multi-terminal regime, a perpendicular magnetic field eliminates the contour's inversion-symmetry and a sufficiently

large field can introduce nodes: the curvature becomes discontinuous at seemingly random locations along the contour.

4. The observed CCC geometries of our multi-terminal junctions can be remarkably well reproduced using the scattering theory of the Josephson effect generalized to the case of $N > 2$. A randomly generated scattering matrix constrained by fundamental symmetry can reproduce the behavior of CCC under different circumstances. The effect of magnetic fields can be captured by switching to the circular unitary ensemble (CUE), which is appropriate in the absence of time-reversal symmetry.

We expect that our measurement and analysis would guide the basic characterization of any other physical implementation of coherent multi-terminal Josephson junction.

Chapter 5

Multi-terminal superconducting quantum interference device (multi-SQUID)

The ultimate manifestation of superconducting phase-coherence in the conventional Josephson effect is the flux-modulation of the supercurrent in a SQUID. A conventional SQUID consists of two Josephson junctions in a superconducting loop pierced by magnetic flux. The supercurrents flowing in each arm can interfere constructively or destructively depending on the magnetic flux. The supercurrent interference in the multi-SQUIDs is more complex. This chapter presents the detailed study of the phase-bias effect in the multi-terminal junctions. Here, the external magnetic flux Φ piercing the loop establishes the phase-difference $\phi_4 - \phi_3 = \Phi \times 2e/\hbar$ while the current is applied to the other two terminals 1 and 2. In case the loop is floating, the current I_1 flowing into the terminal 1 equals the current $-I_2$ flowing into the terminal 2 due to the current conservation, so we can define $I_{12} = I_1 = -I_2$. In such a biasing configuration the multi-SQUID resembles a conventional SQUID in the sense that it is a flux-controlled two-terminal superconducting device. However, in case the loop is grounded, the current I_1 and I_2 can be set independently, and the multi-SQUID becomes a flux-controlled three-terminal junction.

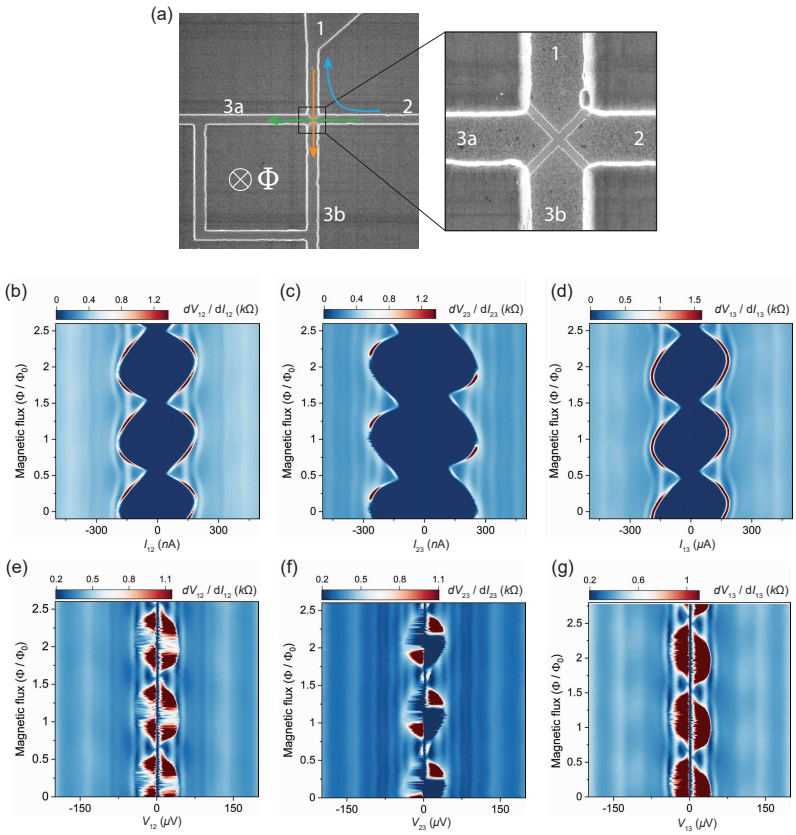

Figure 5.1: (a) SEM image of the 4-terminal JJ with a loop. Colored arrows schematically indicates biasing currents for each 3 measurements: blue - between terminals 1 and 2 (3/loop is floating), green - between 2 and 3/loop (1 floating), orange - 1 and 3/loop (2 floating). (b,c,d) Differential resistance between terminal 1 and 2, 2 and 3, 1 and 3 correspondingly as a function of the flux Φ through the loop. $\Phi_0 = h/(2e)$ is the superconducting flux quantum. (e,f,g) Differential resistances plotted versus measured voltage.

5.1 Effect of phase-bias in a 4-terminal JJ

In the first test, we float the loop and measure the differential resistance dV_{12}/dI_{12} as a function of the bias current I_{12} and the flux Φ through the loop (Fig.5.1). Flux-periodic oscillations of dV_{12}/dI_{12} are clearly visible while the critical current is notably asymmetric with respect to positive and negative values, with the exception of the integer and the half-integer flux (Fig.5.1 (b)). At these points $I_+c = I_-c$. It is still symmetric under the current and flux inversion ($I \to -I$, $\Phi \to -\Phi$). Our observation can be understood as a result of the superconducting phase-drag effect [68]: the

externally-set phase difference $\phi_4 - \phi_3$ induces a phase-difference between the terminal 1 and 2, which periodically offsets the maximally allowed value of supercurrent I_{12}. The critical current oscillations for the other two pairs are nearly identical (Fig.5.1 (c,d)). However, in this case, oscillations appear due to the constructive or destructive interference between bias current and current created in the loop by the flux. The values of flux and half-flux are identical for all pairs of terminals. During each test, the voltage was measured simultaneously.

In Fig. 5.1 (e,f,g) we present differential resistance maps plotted versus voltage. The MAR lines are straight in $I - \Phi$ plane and go parallel to $V = 0$ line, but their intensity oscillates (can be better seen on Fig. 5.1 (g) at $V = -120\ \mu V$). That corresponds to MAR oscillation in the z-direction with being maximum at integer flux quantum and minimum at half flux, which makes MAR lines appear dashed.

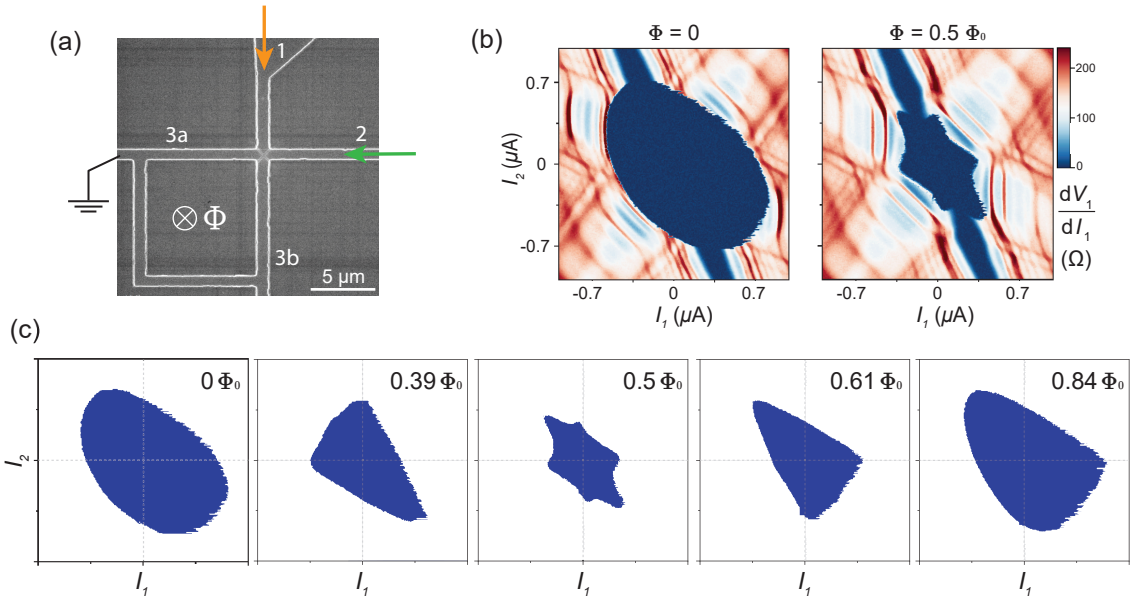

Figure 5.2: (a) SEM image of the 4-terminal JJ with a loop and schematic measurement setup. (b) Differential resistance of the terminal 1 as a function of the two currents I_1, I_2, for an integer flux (left) and a half-integer flux (right) through the loop; the loop is grounded. (c) Evolution of the CCC as a function of flux through the loop. Note the formation of an unusual inversion-symmetric star-shape at the half-integer flux bias.

In a more elaborate multi-SQUID experiment, we ground the loop (terminals 3a and 3b), and treat the device as a three-terminal junction. Repeating the procedures of two-current measurement

described in Chapter 3, we measure the resistance maps of dV_1/dI_1 and dV_2/dI_2 as a function of (I_1, I_2) and Φ. While the familiar shape of the CCC at a zero flux is similar to that of a regular three-terminal junction, the half-integer flux introduces a dramatic modification: the CCC acquires the shape of a skewed six-pointed star, which respects inversion-symmetry. Note that the flux bias expectedly does not affect the transport at non-zero voltage. The clearly visible MAR resonance has a similar pattern to those shown in Fig. 3.7 (c,d), and they merely shift in the (I_1, I_2)-plane in order to adjust to the modified geometry of the CCC (Fig. 5.3). We have tracked the evolution of CCC as a function of flux which results in a similar deformation to that induced by the magnetic field described in Chapter 4 and Fig. 4.6.

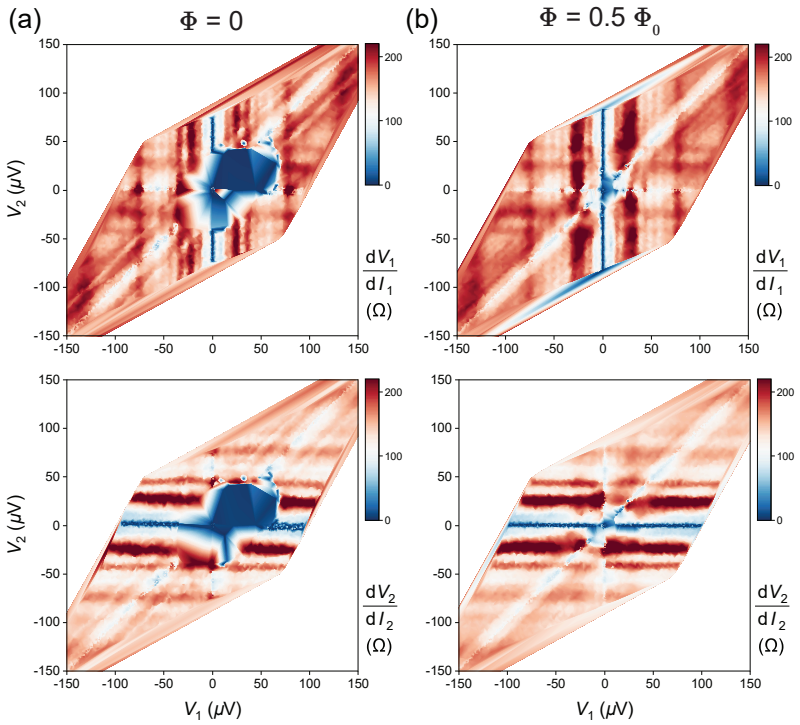

Figure 5.3: Differential resistances of the 4-terminal Josephson junction with a superconducting loop pierced by different magnetic flux (a) $\Phi = 0$, (b) $\Phi = 0.5\Phi_0$. The position of the MAR lines does not depend on flux.

The evolution of the CCC can be described as follows. At zero flux, the shape of CCC is an almost perfect oval, very similar to the 3-terminal junction. When the flux value is between zero and $\Phi_0/2$, the shape of CCC changes to an isosceles triangle with the base facing the top-left corner (Fig 5.2

(c)). The closer the flux value to the $\Phi_0/2$ the smaller triangle gets. Simultaneously the second triangle with the base facing the lower-right corner starts increasing. At the $\Phi_0/2$ the triangles have approximately the same area and form a star. Further increase of the flux value leads to the inverse process: decrease of the first triangle and increase of the second until eventually CCC turns into the oval at $\Phi = \Phi_0$. Such transition suggests that for flux values between 0 and $\Phi_0/2$ one path around the loop is more preferable than the other, at $\Phi_0/2$ both paths are equivalent, and at values between $\Phi_0/2$ and Φ_0 the second path prevails.

Note the low value of applied magnetic field - maximum $4\mu T$ compared to the $2mT$ in Chapters 3 and 4. Yet, in a multi-SQUID, CCC undergoes more prominent transformation than in previous experiments. Magnetic field in the junction region is essentially zero in case of a multi-SQUID, but the flux Φ through the loop sets a phase-difference $\phi_3 - \phi_4 = \Phi \times 2e/\hbar$. It could be taken into account as a constraint that can be directly incorporated into the $\hat{r}$-matrix of Eq. 1.22, which makes the ABS spectrum and hence the CCC flux-dependent.

5.2 Conclusion

We present the very first experimental demonstration of the multi-SQUID. Piercing magnetic flux through the scattering region and flux-biasing the loop of a multi-SQUID leads to similar in nature multi-terminal superconducting interference effects. The multi-terminal ABS are flux dependent, which results in rapid modulation of CCC shape.

Chapter 6

Summary and outlook

6.1 Summary of results

In the scope of this thesis work we have studied 3- and 4-terminal InAs/epi-Al hybrid Josephson junctions in different configurations and geometries. We have introduced a new concept of the *critical current contour* (CCC) — the key ground state characteristic of a multi-terminal Josephson junction. Such a geometric object is readily available from an elementary transport measurement, yet it remained overlooked in previous theoretical and experimental studies. To test the new concept, we created a variety of novel junction devices, including the very first demonstration of the multi-SQUID. The CCC undergoes non-trivial deformations in response to electrostatic gating, magnetic field, and a phase-bias, which are the three external stimuli usually used to probe the Josephson effect in two-terminal junctions. Yet, all our observations are reproduced remarkably well by the scattering theory of multi-terminal Andreev bound states, which makes no assumptions about the junction's microscopic details. It is thus probable that our data represents a generic manifestation of the Josephson effect in mesoscopic junctions of more than two superconductors.

Additionally, we demonstrated gate controlled multi-terminal junctions, which can act as superconducting digital devices [69], tunable superconducting transformers, and non-linear elements, which can be useful for controlling superconducting quantum bits [70] and creating quantum-limited sensors and amplifiers [71]. In particular, replacing certain multi-junction elements, such as

Josephson ring modulators [72] and Josephson rhombus chains [73] with multi-terminal Josephson junctions introduces a potentially useful resource to the quantum circuits toolbox.

Finally, we have also developed a set of stable fabrication techniques that could be adopted by various projects based on hybrid material structures and beyond.

6.2 Future perspectives

Our experiments were made possible by the favorable properties of the epitaxial InAs/Al heterostructure: transparent semiconductor/superconductor interface, high-mobility of the exposed surface 2DEG, and overall robustness with respect to the device fabrication procedures. Even more intriguing developments are expected with such a materials platform in the context of recently proposed experiments on multi-terminal Josephson junctions. As already noted, gating the carrier density in the semiconductor allows depleting the transport into the single-channel regime. In this case, the junction's ABS energies as a function of multiple phase-differences can be individually resolved in a tunneling experiment [74]. Such a measurement would test e.g. predictions of the Weyl nodes physics in four-terminal junctions [14].

Thus, the next logical step of the project would be to perform tunneling spectroscopy of the junctions. To perform such measurement we had to solve several technical problems in nanofabrication and measurement setup to enable voltage-biased measurement. A preliminary test was performed in a 3-terminal JJ with a partial gate (Fig. 6.1 (a)). The gap in Al was etched in the shape of a triangle, unlike the usual Y-shape. The top-gate was deposited with offset, such that it fully covered one superconducting terminal and part of the exposed semiconducting region. The junction then was gated until resistance between terminals 3 and 2 was of the order of $20\ k\Omega$ and conductance measurement was performed (terminal 1 floating) Fig 6.1 (a). Such measurement can not be called a true tunneling conductance measurement due to the possibly large number of tunneling channels defined by the width of superconducting lead. However, resulting plots of differential conductance contain a rich pattern of lines possibly related to ABS. Also, the lines corresponding to Δ can be seen up to the $V_g = -1.2V$ and 2Δ lines up to $V_g = -1.26V$.

For a thorough study of ABS spectra, devices of improved architecture are needed. So, the 8-step

fabrication procedure described in Chapter 2 was developed. We are now at the point of full preparedness to implement a conductance study of the multi-terminal Josephson junctions and results will be reported in near future. We hope, that a deep understating of the nature of multi-terminal junctions will make them more attractive to suggested applications and enable new unimaginable applications like it was with classical 2-terminal junctions.

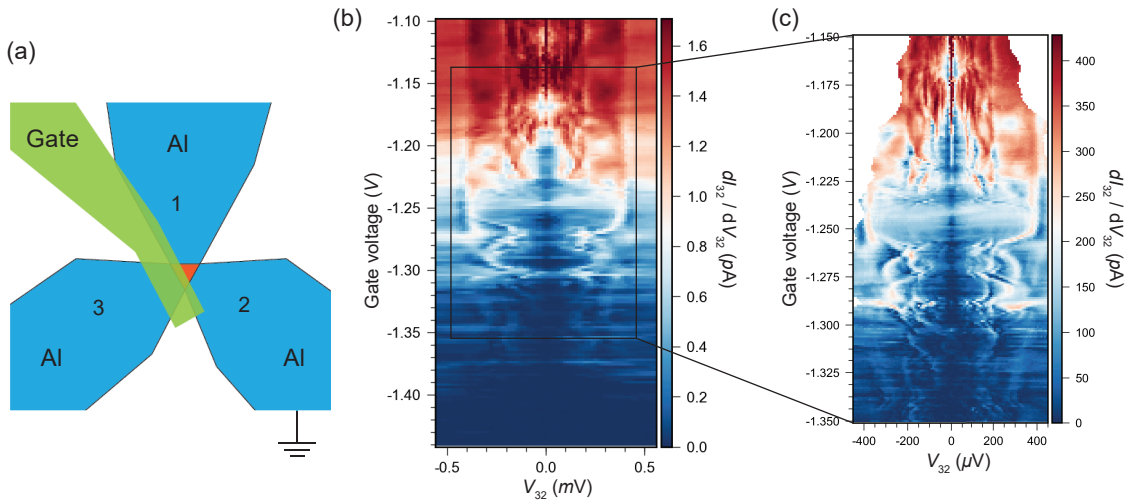

Figure 6.1: (a) Schematic representation of a 3-terminal junction with partial top gate. Orange region correspond to exposed 2DEG region, blue - superconducting leads. (b) Differential conductance of the 3-terminal Josephson junction (terminal 2 grounded, terminal 1 floating).

Our 2D device architecture with tunneling probes can be readily extended to enable multiple experimental studies of the Andreev spectra and topological state of matter. For instance, the non local conductance measurement is predicted to overcome difficulties of the local tunneling conductance in distinguishing between topological and trivial states [75]. To perform non local conductance measurement a system of at least three terminals is required, which makes it difficult to implement in a nanowire system. With the 2D platform one can engineer such system of multiple superconducting terminals as well as two tunneling contacts to study global ABS dependence on the multi-terminal phase difference. The results of recent study [76] demonstrates that the value of magnetic field required to achieve topological state can be lowered by the phase difference in a 2-terminal junction equals π. This gives hope to achieve topological states only by means of multiple phase differences.

Moreover, our material was also shown to have a strong spin-orbit coupling, resulting in recently reported evidence of the induced p-wave order in the presence of an in-plane magnetic field [77]. With our work, all components are now in place to explore tri-junctions of topological superconductors, required for braiding of Majorana fermions [10–12].

Appendices

Appendix A

Art gallery

The pictures in this appendix did not make it into the scientific part of the dissertation for various reasons, but too beautiful to never be seen. They shall be considered as art objects only.

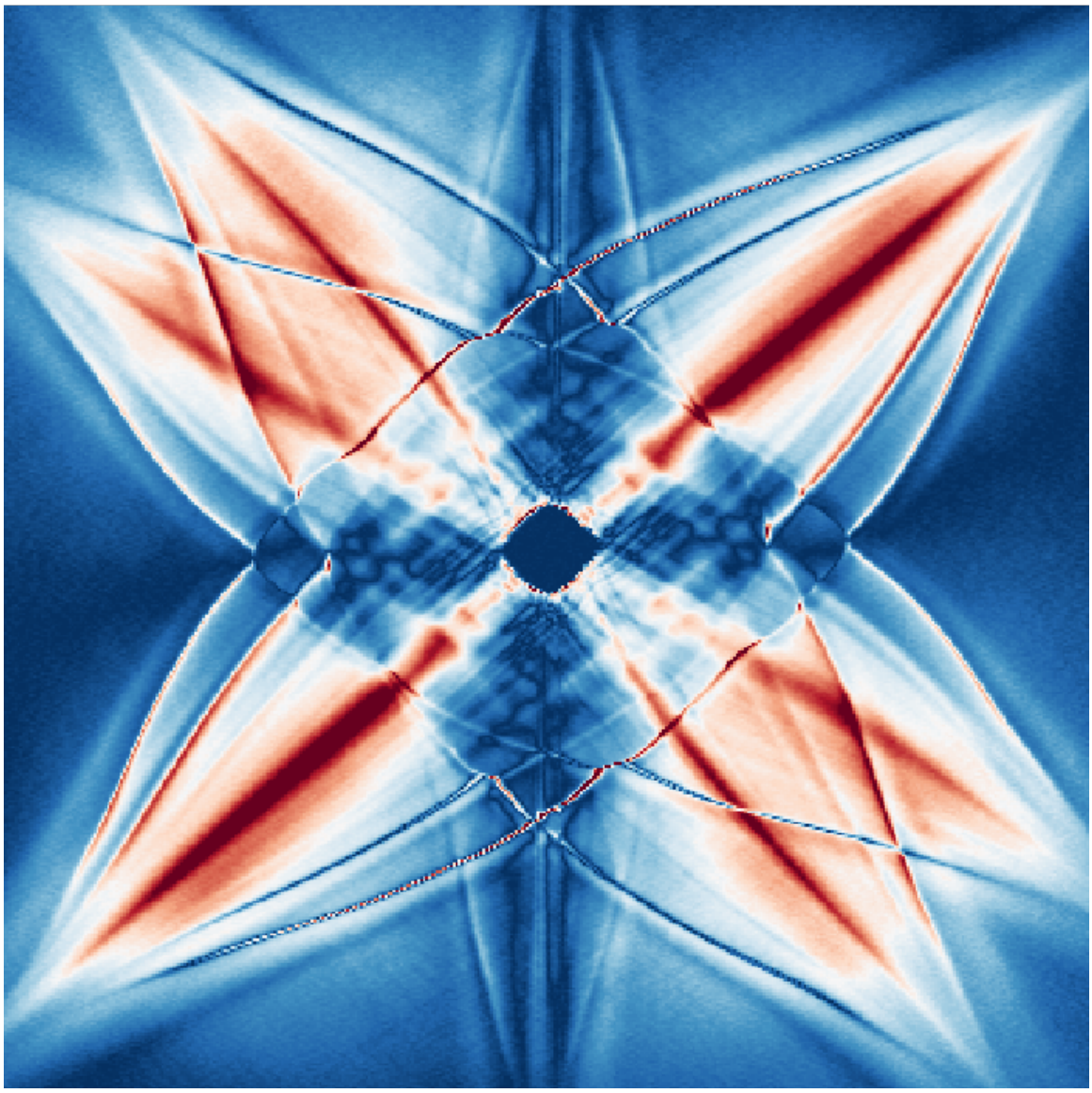

Figure A.1: Improvisation 42

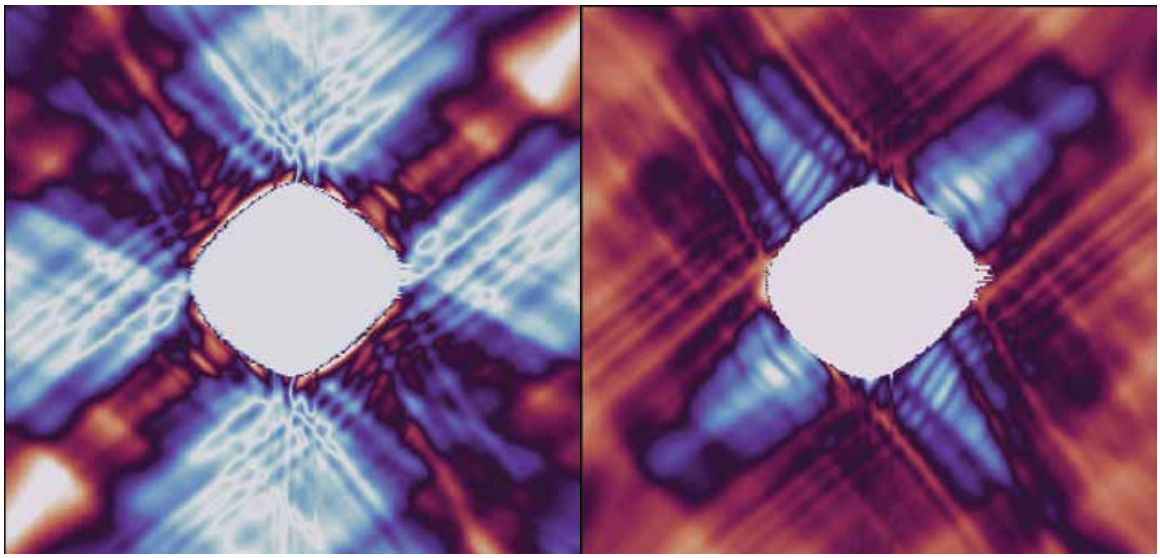

Figure A.2: Delicate transition

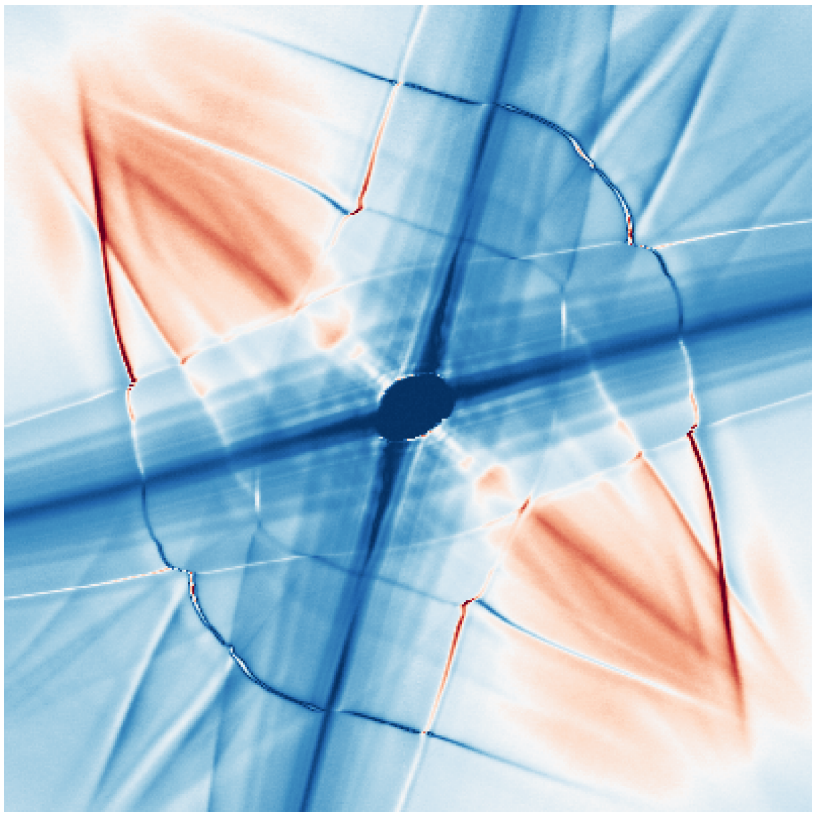

Figure A.3: Dominant diagonal

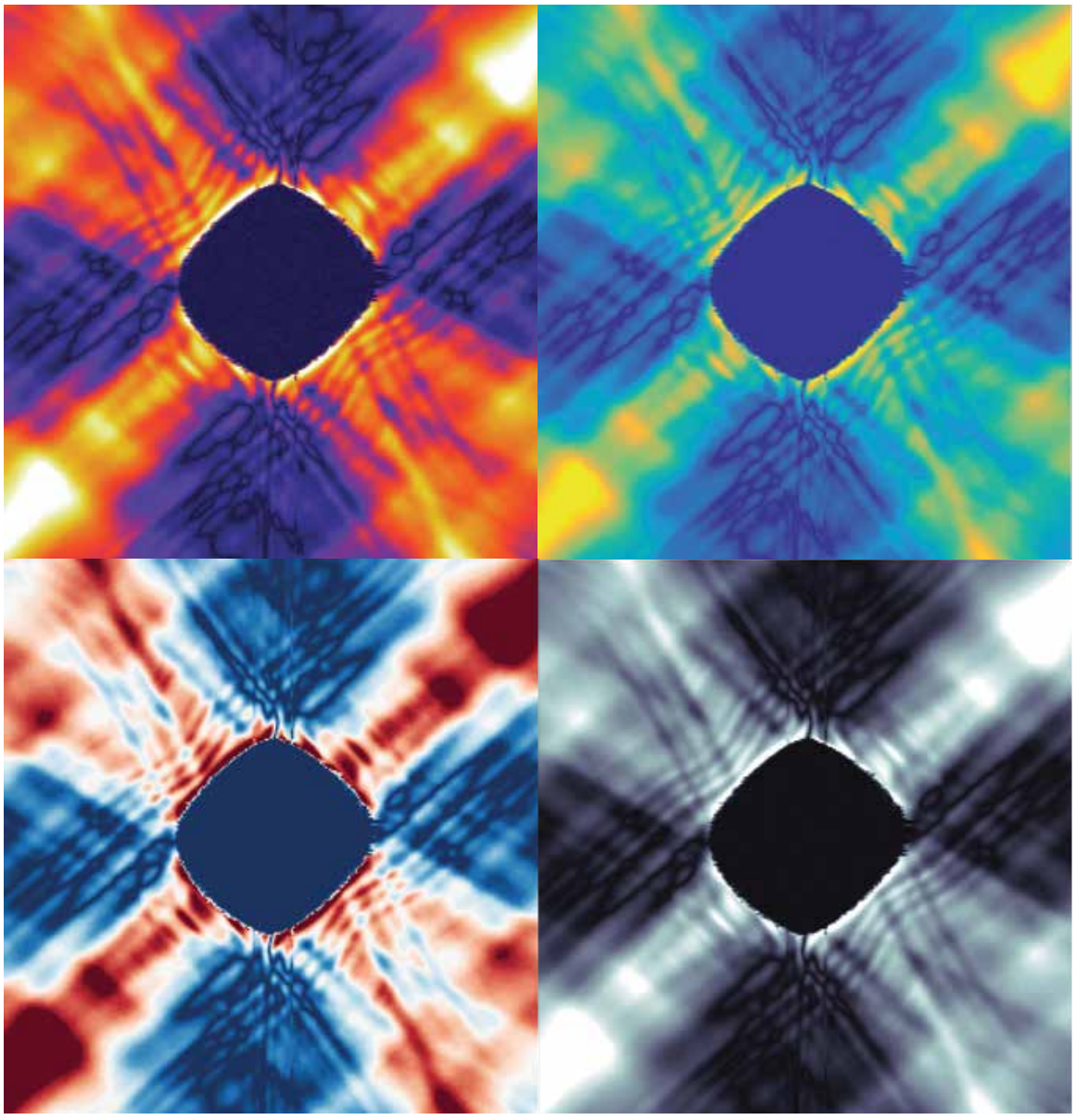

Figure A.4: 4 plots

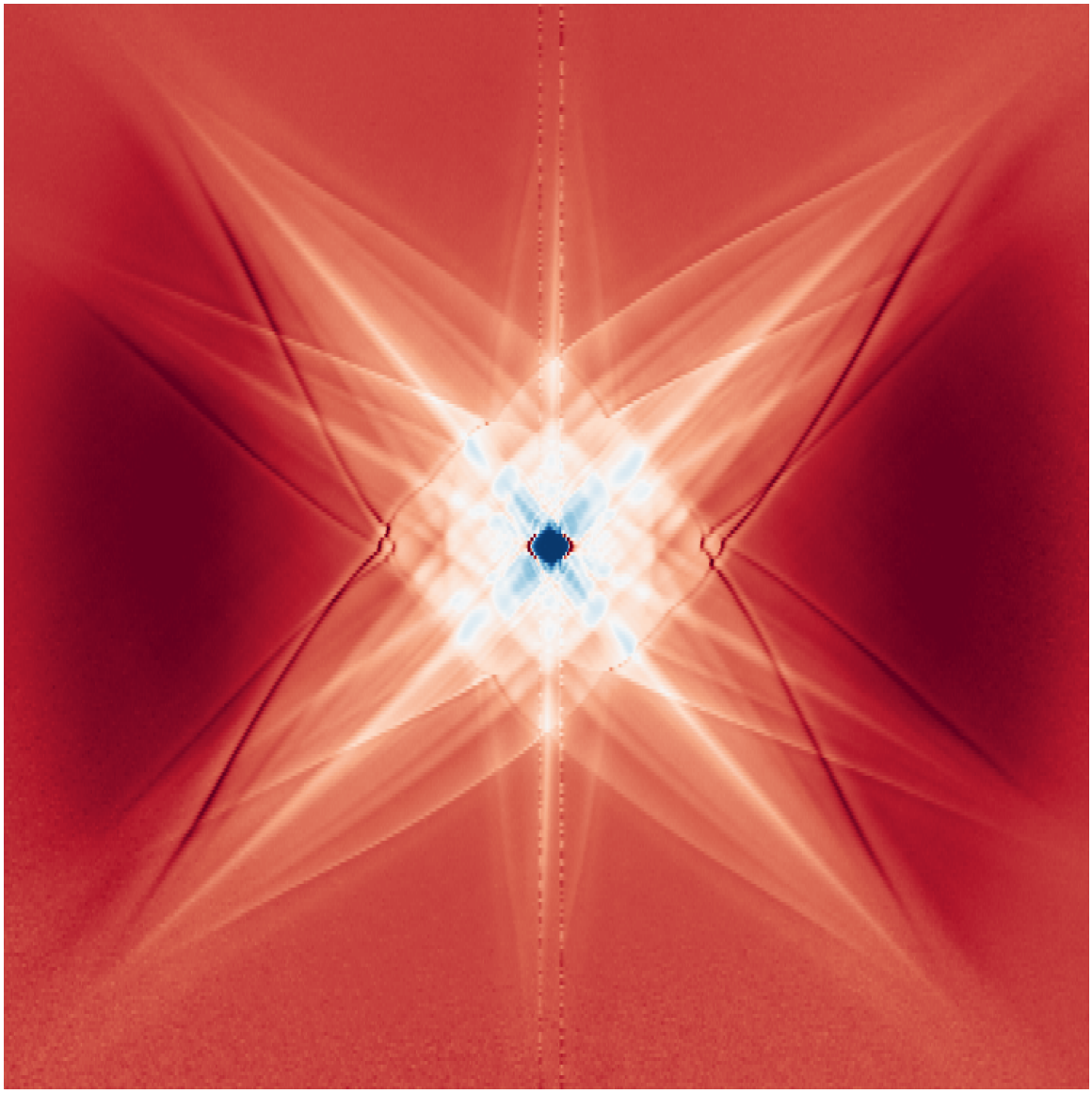

Figure A.5: Composition X

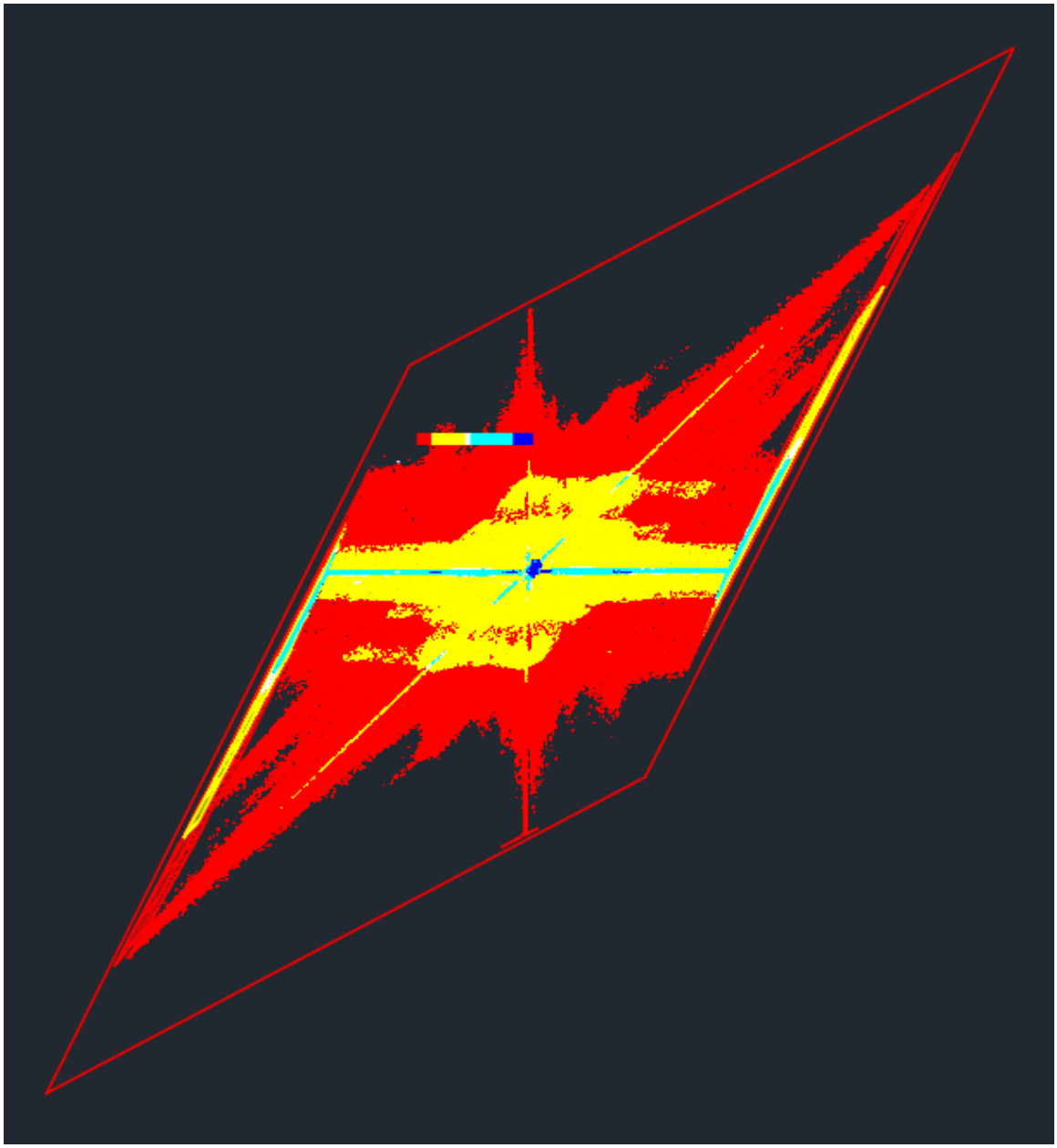

Figure A.6: Current-biased frustration

Bibliography

[1] Brian David Josephson. Possible new effects in superconductive tunnelling. *Phys. Lett.*, 1(7):251–253, 1962.

[2] I. O. Kulik and A. N. Omel'yanchuk. Josephson effect in superconductive bridges: microscopic theory. *Sov. J. Low Temp. Phys.*, 4(3), 1978.

[3] Yu. G. Bevza, V. I. Karamushko, E. A. Kel'man, G. G. Tsach, and I. M. Dmitrenko. Electrically controlled josephson elements. *Sov. J. Low Temp. Phys.*, 5(7), 1979.

[4] R. de Bruyn Ouboter, A. N. Omelyanchouk, and E. D. Vol. Multi-terminal squid controlled by the transport current. *Physica B: Condensed Matter*, 205(2):153–162, 1995.

[5] M. Amin, A. N. Omelyanchouk, and A. M. Zagoskin. Dc squid based on the mesoscopic multi-terminal josephson junction. *Physica C: Superconductivity*, 372:178–180, 2002.

[6] M. Amin, A. N. Omelyanchouk, A. Blais, Alec Maassen van den Brink, G. Rose, T. Duty, and A. M. Zagoskin. Multi-terminal superconducting phase qubit. *Physica C: Superconductivity*, 368(1-4):310–314, 2002.

[7] Roman M Lutchyn, Jay D Sau, and S Das Sarma. Majorana fermions and a topological phase transition in semiconductor-superconductor heterostructures. *Phys. Rev. Lett.*, 105(7):077001, 2010.

[8] Yuval Oreg, Gil Refael, and Felix von Oppen. Helical liquids and majorana bound states in quantum wires. *Phys. Rev. Lett.*, 105(17):177002, 2010.

[9] Vincent Mourik, Kun Zuo, Sergey M Frolov, SR Plissard, Erik PAM Bakkers, and Leo P Kouwenhoven. Signatures of majorana fermions in hybrid superconductor-semiconductor nanowire devices. *Science*, 336(6084):1003–1007, 2012.

[10] Liang Fu and Charles L Kane. Superconducting proximity effect and majorana fermions at the surface of a topological insulator. *Physical Review Letters*, 100(9):096407, 2008.

[11] Jason Alicea, Yuval Oreg, Gil Refael, Felix Von Oppen, and Matthew P. A. Fisher. Non-abelian statistics and topological quantum information processing in 1d wire networks. *Nature Physics*, 7(5):412, 2011.

[12] Tong Zhou, Matthieu C Dartiailh, William Mayer, Jong E Han, Alex Matos-Abiague, Javad Shabani, and Igor Žutić. Phase control of majorana bound states in a topological x junction. *Physical Review Letters*, 124(13):137001, 2020.

[13] B Van Heck, S Mi, and A. R. Akhmerov. Single fermion manipulation via superconducting phase differences in multiterminal josephson junctions. *Physical Review B*, 90(15):155450, 2014.

[14] Roman-Pascal Riwar, Manuel Houzet, Julia S Meyer, and Yuli V Nazarov. Multi-terminal josephson junctions as topological matter. *Nature communications*, 7:11167, 2016.

[15] Francesco Tafuri. *Fundamentals and Frontiers of the Josephson Effect*. Springer, 2019.

[16] B.D. Josephson. Supercurrents through barriers. *Adv. Phys.*, 14:419–451, 1965.

[17] P.W.Anderson. Special effects in superconductivity. *Lectures on the Manybody Problem, Ravello*, 2:113–135, 1963.

[18] Thomas Schapers. *Superconductor/Semiconductor Junctions*. Springer, 2001.

[19] N. Mermin N. Ashcroft. *Solid State Physics*. Philadelphia: Saunders College Publishing, 1976.

[20] M. Scheffler K. Horn. *Handbook of Surface Science, Chapter 7 - Electronic Structure of Semiconductor Surfaces*. North-Holland, 2000.

[21] K. Hirakawa M. Noguchi and T. Ikoma. Adhesion promotion - hmds. *Phys. Rev. Lett.*, 66(17):2243–2246, 1991.

[22] Gino V Graziano, Joon Sue Lee, Mihir Pendharkar, Chris J Palmstrøm, and Vlad S Pribiag. Transport studies in a gate-tunable three-terminal josephson junction. *Physical Review B*, 101(5):054510, 2020.

[23] David J. Griffiths. *Introduction to quantum mechanics*. Pearson, 1995.

[24] C. W. J. Beenakker and H. van Houten. Josephson current through a superconducting quantum point contact shorter than the coherence length. *Phys. Rev. Lett.*, 66:3056–3059, Jun 1991.

[25] Akira Furusaki and Masaru Tsukada. Dc josephson effect and andreev reflection. *Solid States Communications*, 78:299–302, 1991.

[26] Yuli V. Nazarov and Yuli M. Blanter. *Quantum Transport: Introduction to Nanoscience*. Cambridge, 2009.

[27] Tomohiro Yokoyama and Yuli V. Nazarov. Singularities in the Andreev spectrum of a multiterminal Josephson junction. *Phys. Rev. B*, 92(15):155437, oct 2015.

[28] Erik Eriksson, Roman-Pascal Riwar, Manuel Houzet, Julia S. Meyer, and Yuli V. Nazarov. Topological transconductance quantization in a four-terminal Josephson junction. *Phys. Rev. B*, 95(7):075417, feb 2017.

[29] Hong-yi Xie, Maxim G Vavilov, and Alex Levchenko. Topological Andreev bands in three-terminal Josephson junctions. *Phys. Rev. B*, 96(16):161406, oct 2017.

[30] Xiao Li Huang and Yuli V. Nazarov. Topology protection-unprotection transition: Example from multiterminal superconducting nanostructures. *Phys. Rev. B*, 100(8), 2019.

[31] E. V. Repin, Y. Chen, and Y. V. Nazarov. Topological properties of multiterminal superconducting nanostructures: Effect of a continuous spectrum. *Phys. Rev. B*, 99(16):165414, apr 2019.

[32] Hong-Yi Xie, Maxim G. Vavilov, and Alex Levchenko. Weyl nodes in Andreev spectra of multiterminal Josephson junctions: Chern numbers, conductances, and supercurrents. *Phys. Rev. B*, 97(3):035443, jan 2018.

[33] Janis Erdmanis, Árpád Lukács, and Yuli V. Nazarov. Weyl disks: Theoretical prediction. *Phys. Rev. B*, 98(24):241105, dec 2018.

[34] Hong-Yi Xie and Alex Levchenko. Topological supercurrents interaction and fluctuations in the multiterminal Josephson effect. *Phys. Rev. B*, 99(9):094519, mar 2019.

[35] Panagiotis Kotetes, Maria Teresa Mercaldo, and Mario Cuoco. Synthetic Weyl Points and Chiral Anomaly in Majorana Devices with Nonstandard Andreev-Bound-State Spectra. *Phys. Rev. Lett.*, 123(12):126802, 2019.

[36] M. P. Nowak, M. Wimmer, and A. R. Akhmerov. Supercurrent carried by nonequilibrium quasiparticles in a multiterminal Josephson junction. *Phys. Rev. B*, 99(7), 2019.

[37] Lucila Peralta Gavensky, Gonzalo Usaj, and C. A. Balseiro. Topological phase diagram of a three-terminal Josephson junction: From the conventional to the Majorana regime. *Phys. Rev. B*, 100(1):014514, jul 2019.

[38] Viktoriia Kornich, Hristo S. Barakov, and Yuli V. Nazarov. Fine energy splitting of overlapping Andreev bound states in multiterminal superconducting nanostructures. *Phys. Rev. Res.*, 1(3):1–5, 2019.

[39] Manuel Houzet and Julia S. Meyer. Majorana-Weyl crossings in topological multiterminal junctions. *Phys. Rev. B*, 100(1):14521, 2019.

[40] A. Zazunov, R. Egger, M. Alvarado, and A. Levy Yeyati. Josephson effect in multiterminal topological junctions. *Phys. Rev. B*, 96(2):1–10, 2017.

[41] Daniel Litinski, Markus S. Kesselring, Jens Eisert, and Felix von Oppen. Combining Topological Hardware and Topological Software: Color-Code Quantum Computing with Topological Superconductor Networks. *Phys. Rev. X*, 7(3):031048, sep 2017.

[42] R. M. Lutchyn, E. P.A.M. Bakkers, L. P. Kouwenhoven, P. Krogstrup, C. M. Marcus, and Y. Oreg. Majorana zero modes in superconductor-semiconductor heterostructures. *Nat. Rev. Mater.*, 3(5):52–68, 2018.

[43] Mircea Trif and Pascal Simon. Braiding of Majorana Fermions in a Cavity. *Phys. Rev. Lett.*, 122(23):236803, jun 2019.

[44] Alessio Calzona and Björn Trauzettel. Moving Majorana bound states between distinct helical edges across a quantum point contact. *Phys. Rev. Res.*, 1(3), 2019.

[45] Oscar Viyuela, Sagar Vijay, and Liang Fu. Scalable fermionic error correction in Majorana surface codes. *Phys. Rev. B*, 99(20):205114, 2019.

[46] Michael Hell, Karsten Flensberg, and Martin Leijnse. Coupling and braiding majorana bound states in networks defined in two-dimensional electron gases with proximity-induced superconductivity. *Physical Review B*, 96(3):035444, 2017.

[47] Corneliu Malciu, Leonardo Mazza, and Christophe Mora. Braiding majorana zero modes using quantum dots. *Physical Review B*, 98(16):165426, 2018.

[48] IC Fulga, B van Heck, M Burrello, and T Hyart. Effects of disorder on coulomb-assisted braiding of majorana zero modes. *Physical Review B*, 88(15):155435, 2013.

[49] Torsten Karzig, Falko Pientka, Gil Refael, and Felix von Oppen. Shortcuts to non-abelian braiding. *Physical Review B*, 91(20):201102, 2015.

[50] B Van Heck, AR Akhmerov, F Hassler, M Burrello, and CWJ Beenakker. Coulomb-assisted braiding of majorana fermions in a josephson junction array. *New Journal of Physics*, 14(3):035019, 2012.

[51] Torsten Karzig, Yuval Oreg, Gil Refael, and Michael H Freedman. Universal geometric path to a robust majorana magic gate. *Physical Review X*, 6(3):031019, 2016.

[52] Luzie Weithofer, Patrik Recher, and Thomas L Schmidt. Electron transport in multiterminal networks of majorana bound states. *Physical Review B*, 90(20):205416, 2014.

[53] David Aasen, Michael Hell, Ryan V. Mishmash, Andrew Higginbotham, Jeroen Danon, Martin Leijnse, Thomas S. Jespersen, Joshua A. Folk, Charles M. Marcus, Karsten Flensberg, and Jason Alicea. Milestones toward Majorana-based quantum computing. *Physical Review X*, 6(3):1–28, 2016.

[54] M Houzet and Peter Samuelsson. Multiple andreev reflections in hybrid multiterminal junctions. *Physical Review B*, 82(6):060517, 2018.

[55] C. W. J. Beenakker. Random-matrix theory of quantum transport. *Reviews of Modern Physics*, 69(3):731, 1997.

[56] C. W. J. Beenakker. Universal limit of critical-current fluctuations in mesoscopic josephson junctions. *Physical Review Letters*, 67(27):3836, 1991.

[57] Hong-Yi Xie, Maxim G Vavilov, and Alex Levchenko. Topological andreev bands in three-terminal josephson junctions. *Physical Review B*, 96(16):161406, 2017.

[58] Michiel W. A. de Moor Attila Geresdi Eduardo J. H. Lee Jelena Klinovaja Daniel Loss Jesper Nygård Ramón Aguado Leo P. Kouwenhoven Elsa Prada, Pablo San-Jose. From andreev to majorana bound states in hybrid superconductor-semiconductor nanowires. *Nature Reviews Physics*, 2:575–594, 2020.

[59] Y.; Krogstrup P.; Marcus C. M. Vaitiekėnas, S.; Liu. Zero-bias peaks at zero magnetic field in ferromagnetic hybrid nanowires. *Nature Physics*, 2020.

[60] J Shabani, M Kjaergaard, HJ Suominen, Younghyun Kim, F Nichele, K Pakrouski, T Stankevic, Roman M Lutchyn, P Krogstrup, R Feidenhans, et al. Two-dimensional epitaxial superconductor-semiconductor heterostructures: A platform for topological superconducting networks. *Physical Review B*, 93(15):155402, 2016.

[61] William Mayer, Joseph Yuan, Kaushini S Wickramasinghe, Tri Nguyen, Matthieu C Dartiailh, and Javad Shabani. Superconducting proximity effect in epitaxial al-inas heterostructures. *Applied Physics Letters*, 114(10):103104, 2019.

[62] Kaushini S Wickramasinghe, William Mayer, Joseph Yuan, Tri Nguyen, Lucy Jiao, Vladimir Manucharyan, and Javad Shabani. Transport properties of near surface inas two-dimensional heterostructures. *Applied Physics Letters*, 113(26):262104, 2018.

[63] Merck Performance Materials GmbH. Intrinsic electron accumulation layers on reconstructed clean inas(100) surfaces. 2020.

[64] ChiiDong Chen Cen Shawn Wu, Yoshiyuki Makiuchi. High-energy electron beam lithography for nanoscale fabrication. *InTech*, 2010.

[65] R.R. LaPierre J. Baugh K. Gharavi, G.W. Holloway. Nb/inas nanowire proximity junctions from josephson to quantum dot regimes. *Nanotechnology*, 28, 2017.

[66] Anne W. Draelos, Ming Tso Wei, Andrew Seredinski, Hengming Li, Yash Mehta, Kenji Watanabe, Takashi Taniguchi, Ivan V. Borzenets, François Amet, and Gleb Finkelstein. Supercurrent Flow in Multiterminal Graphene Josephson Junctions. *Nano Lett.*, 19(2):1039–1043, 2019.

[67] D.C. Tsui. Observation of surface bound state and two-dimensional energy band by electron tunneling. *Phys. Rev. Lett.*, 24(7):303–306, 1970.

[68] MHS Amin, AN Omelyanchouk, and AM Zagoskin. Mesoscopic multiterminal josephson structures. i. effects of nonlocal weak coupling. *Low Temperature Physics*, 27(8):616–623, 2001.

[69] Susumu Takada, Shin Kosaka, and Hisao Hayakawa. Current injection logic gate with four josephson junctions. *Japanese Journal of Applied Physics*, 19(S1):607, 1980.

[70] Zhenyi Qi, Hong-Yi Xie, Javad Shabani, Vladimir E. Manucharyan, Alex Levchenko, and Maxim G. Vavilov. Controlled-z gate for transmon qubits coupled by semiconductor junctions. *Physical Review B*, 97(13):134518, 2018.

[71] N. Bergeal, R. Vijay, V. E. Manucharyan, I. Siddiqi, R. J. Schoelkopf, S. M. Girvin, and M. H. Devoret. Analog information processing at the quantum limit with a josephson ring modulator. *Nature Physics*, 6(4):296–302, 2010.

[72] N Bergeal, F Schackert, M Metcalfe, R Vijay, VE Manucharyan, L Frunzio, DE Prober, RJ Schoelkopf, SM Girvin, and MH Devoret. Phase-preserving amplification near the quantum limit with a josephson ring modulator. *Nature*, 465(7294):64–68, 2010.

[73] L. B. Ioffe and M. V. Feigel'man. Possible realization of an ideal quantum computer in josephson junction array. *Phys. Rev. B*, 66(22):224503, 2002.

[74] J-D Pillet, C. H. L. Quay, P. Morfin, C. Bena, A. Levy Yeyati, and P. Joyez. Andreev bound states in supercurrent-carrying carbon nanotubes revealed. *Nature Physics*, 6(12):965–969, 2010.

[75] M. Kjaergaard A. R. Akhmerov T. O. Rosdahl, A. Vuik. Andreev rectifier: A nonlocal conductance signature of topological phase transitions. *Physical Review B*, 97, 2018.

[76] Antonio Fornieri, Alexander M Whiticar, F Setiawan, Elías Portolés Marín, Asbjørn CC Drachmann, Anna Keselman, Sergei Gronin, Candice Thomas, Tian Wang, Ray Kallaher, et al. Evidence of topological superconductivity in planar josephson junctions. *arXiv preprint arXiv:1809.03037*, 2018.

[77] William Mayer, Matthieu C. Dartiailh, Joseph Yuan, Kaushini S. Wickramasinghe, Alex Matos-Abiague, Igor Žutić, and Javad Shabani. Phase signature of topological transition in josephson junctions. *arXiv preprint arXiv:1906.01179*, 2019.