ABSTRACT

Title of Dissertation: MASKLESS FABRICATION OF JUNCTION FIELD EFFECT TRANSISTORS VIA FOCUSED ION BEAMS

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Focused ion beam (FIB) techniques were used to construct junction field effect transistors (JFETs) on a mesa of n-type silicon on an SOI chip. The implantation and metal contacts were made by FIB, which suggests that this technique can be used to make transistors in a non-standard geometry, such as the tip of a scanning probe or on a MEMS structure. FIB dopant implantation was used to direct-write the source, gate, and drain regions of each device. The contact resistance of platinum grown on silicon byFIB - induced deposition was investigated, and found to be suitable for producing ohmic contacts to heavily doped silicon. Several proof-of-concept devices were made with FIB deposited platinum as contacts to demonstrate the technique's potential. Other devices were created with conventional aluminum contacts instead of FIB-platinum as a control set, to isolate and investigate the effect of variable gate doping on device characteristics. All devices were 90 μm by 90 μm with a gate length of 1 μm. A graded doping profile was found to be an effective means of decreasing the short-channel effects that result in increasing source-drain current past saturation.

MASKLESS FABRICATION OF JUNCTION FIELD EFFECT TRANSISTORS VIA FOCUSED ION BEAMS

by

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Chapter I: INTRODUCTION

The current generation of microprocessor, with lithography dimensions of 0.10 μm or less, incorporates millions of transistors on each chip. Regardless of the ultimate limits of lithography, this number will only increase in the near future. As microchips become denser and more complex, more work is needed to design, and to verify the design of the circuitry. To keep the time and expense of fabricating new microprocessors from being prohibitive, novel techniques must be developed to speed the design process. Any procedure so developed must integrate with and be applicable to current silicon microchip production technology in order to gain any acceptance in industry.

Focused ion beam (FIB) systems can be used to repair and modify optical lithography masks and metal interconnect lines on chip through ion milling and ion-induced metal deposition. These procedures are most valuable in the design and testing stages of microcircuit manufacture, when the layout may need to be changed often to meet desired performance goals. FIB repair allows minor modifications to the mask or circuit to take place without making a completely new set of masks, or restarting the lithographic process. This can lead to greater efficiency and lower total cost for the design of a product.

This work investigates the next level of FIB circuit modification: the creation of active devices utilizing solely FIB fabrication, instead of the traditional masked lithographic process that defines the modern silicon industry. Though a maskless process cannot provide the throughput required for mass production, it could be valuable in development, offering nearly unlimited flexibility in creating and testing new layouts.

There are two major avenues of research within this thesis. First, the suitability of FIB processes to accomplish the tasks required of maskless device production has been investigated, with an emphasis on the novel areas of direct-write nonlinear active area doping, and FIB-induced metallization to provide device contacts. Second, junction field effect transistors (JFETs) were created utilizing maskless FIB fabrication techniques as proof-of-principle devices to show the potential of the technique. These transistors have been compared to theoretical device models to gain insight into the fabrication process.

Chapter II: BACKGROUND

II.1 MOTIVATION FOR WORK

Transistor production without masked lithographic processes has implications in a number of areas, most notably research and development. Focused ion beams can effect many of the processes needed in silicon manufacturing. Ion milling is the most basic FIB application, with ion beams used to selectively sputter material from a substrate. Direct-write FIB lithography is possible using ion-sensitive resists. Metal can be selectively deposited by ion-induced deposition, and, metal alloy ion sources allow doping profiles to be directly written onto a substrate. These four processes can be combined to direct write junction field effect transistors onto a silicon wafer. By contrast, metal-oxide-semiconductor field effect transistors (MOSFETs)require a high -quality insulator for the gate which cannot be deposited through FIB techniques.

One potential application for FIB technology is microcircuit design. A circuit layout could be directly fabricated on a wafer for testing. The modified design could then be fabricated with the desired changes as easily as the first circuit was fabricated. The process of generating the mask patterns for the desired circuit, and fabricating the mask set can be completely bypassed, saving time and money. In this way, multiple generations of a circuit design may be more quickly fabricated and tested.

A second application for a maskless FIB fabrication process is designing a unique transistor. The direct-write ability allows device dimensions and doping profiles to be tailored to meet a specific need. Novel transistor devices could be fabricated via FIB

techniques, and then tested for their electrical characteristics. The physical properties of the next device built can then be changed according to data gathered from preceding devices. Again, in this type of application, the FIB process allows for a more efficient research and development process. Additionally, there are some novel device structures that can be most easily made via FIB techniques; these will be further discussed in the literature search section of this proposal.

Finally, there is a small class of applications where FIB fabrication would not necessarily be limited to the design phase of a device. Although the low throughput of any FIB process ill suits such techniques for mass production, specialty devices not intended for mass production are not outside the realm of possibility. These would be small-scale circuits created as part of a larger design, for a very specific function. One possible area where this might be useful is cryptography. An encryption algorithm circuit could be designed and fabricated with no physical evidence of its creation - the mask - left behind, reducing the chance that the encryption circuit might be compromised at some point. Finally, FIB fabricated circuits would not be limited by the normal planar processing steps needed by conventional fabrication. Therefore, FIB microcircuits for specialty devices could be formed on nearly any semiconductor surface, rather than being confined to fabrication on a standard wafer.

II.2 PREVIOUS WORK AND LITERATURE SURVEY

Ion beams have been used in the semiconductor industry since the 1960s, in the form of broad-beam, unfocused ion implanters that provide controlled, reproducible doping of silicon substrates with a variety of ion species produced by gas excited into a

plasma state. Early work on producing a focused ion beam suitable for microfabrication was done at Hughes Laboratories in 1973, where a conventional ion implanter was modified with an electrostatic lens to focus the beam produced to a spot size of 3.5 μm.[1] The system was used to demonstrate direct-write boron implantation into silicon, as well as exposure of an ion-sensitive resist for lithography. Since then, smaller, high brightness ion sources have been developed and used to obtain a sub-micrometerspot size with a high current density. Currently most FIB systems use a liquid metal ion source (LMIS), developed in the mid-1970s that provide good source characteristics together with the ability to produce a beam with a wide variety of ion species.[2,3] The production of high quality, long-life liquid metal ion sources allowed FIB systems to more readily accomplish all of the tasks required for microcircuit fabrication and repair: lithography, milling, implantation, and deposition.

The feasibility of focused ion beam lithography relies on the existence of positive and negative ion-sensitive resists, which have been extensively studied for use in ion projection lithography.[4] These resists are composed of long polymer chains that may be broken by the energy of the incident ions in a process known as scission, or that may be bonded to one another in a process known as cross-linking. In positive resist, the scission process dominates, leaving the ion-exposed areas vulnerable to dissolution in a chemical developer, whereas the unexposed areas will remain after development. Ion-exposure in a negative resist results in predominantly cross-linking, hardening the exposed area against the developer, so that only the exposed areas will remain. One of the better-known positive ion resists is poly-methyl methacrylate (PMMA), which is also used as a resist for electron-beam and deep UV lithography. It allows for excellent feature

definition but demonstrates poor etch resistance, so other resists have been investigated for industrial use.[5]

A variety of ion species can be used to expose ion-sensitive resists. The range of implanted ions into materials used in the semiconductor industry has been extensively modeled as a function of species and energy.[6] The dose required to expose resist with an ion beam varies inversely with the atomic weight of the ion species used.[7] To expose PMMA with arsenic ions, for example, requires a dose of approximately 10^{12} ions/cm^2. With helium ions, by contrast, a dose of over 10^{13} ions/cm^2 is needed. A more recent study found light ion sensitivities to be between 10^{12} and 10^{13} ions/cm^2, with a contrast of 2.7.[8] Light ions such as hydrogen and helium penetrate much deeper into the resist than heavier ions do at the same energies, however, and do not significantly damage or dope any underlying semiconductor substrates. Unfortunately, liquid metal ion sources cannot produce H or He ions, so light ions are not currently compatible with most FIB systems. Light metallic ions such as boron have a reduced range, allowing them to expose less than a micrometer of resist even at implantation energies on the order of 200 keV, but are LMIS compatible. The underlying substrate is often protected against implantation and damage by a multi-layer resist structure, or a sacrificial layer of metal underneath the resist.

In addition to maskless exposure of resist, focused ion beams have the capability to alter the surface of materials directly. The most basic of these processes is ion milling, which was demonstrated for silicon and gallium arsenide substrates as early as 1979.[9,10] Ion milling selectively removes material from the surface of the target through sputtering of the substrate atoms. When accelerated ions strike the substrate, they impart energy in

a series of primary collisions, which then causes further collisions within the substrate atoms.[11] When these secondary collisions occur within roughly 5 Å of the material surface, they can impart enough energy to the atoms there to overcome their binding energies and escape the surface. The sputter yield, defined as the number of substrate atoms removed per incident ion, is a complex function that must generally be determined experimentally.[12] When the sputter yield is greater than unity, more material leaves the substrate than is incident upon it, and effective ion milling can occur.

Ion milling is effective on most surfaces, but has several drawbacks. Ion-sputtered atoms can often redeposit on the surface, especially when deep structures such as vias are being milled. This leads to v-shaped cavities as sputtered material redeposits on the structure's sidewalls. Another drawback to ion milling is that the high doses and heavy ions required both implant and damage the surface, saturating it with the incident ion species and amorphizing the surface area around the beam. Using a gas that reacts with the substrate in conjunction with an ion beam can provide better etch characteristics at a lower ion dose.[13] Instead of sputtering, the ion beam induces a chemical reaction between the substrate and gas adsorbed on the surface, producing ion-induced etching. This technique shows enhanced etch characteristics for both silicon and gallium arsenide.[14]

Ion implantation has been well understood for decades, with tables of ion penetration range and lateral straggle readily available for many ion species and materials of interest, at varying ranges.[6] The incident ions penetrate the crystal structure of the substrate, causing damage within a certain distance of the surface. This damage can be repaired through a thermal annealing process that provides enough energy to allow the

crystal lattice to reform, at the same time also activating the dopant atoms as they become incorporated into the semiconductor lattice.

Most broad beam ion implantation takes place at an angle of seven degrees between the beam and the normal crystal symmetry axis of the substrate to minimize the effects of beam channeling. Channeling occurs when the incident ions strike the substrate parallel to a crystal plane and penetrate deeper than they otherwise would since they can travel farther without collision. Research into channeling implantation into silicon finds that channeling is maximized for low doses, while at doses higher than a certain threshold dose, ion damage renders the surface of the substrate amorphous and reduces any further channeling. For arsenic implantation into (100)Si, the threshold dose is 3×10^{13} ions/cm^2.[15,16] The threshold dose for lighter boron ions into (100)Si is 10^{15} ions/cm^2, since below this dose the implantation profile is little influenced by surface damage.[17] The channeling implantation range boron is much larger than that of arsenic, reaching 0.4 μm at an implantation energy of only 20 KeV. For FIB implantation, the high beam current density results in greater surface damage, and therefore lower threshold doses which serve to reduce channeling.

Focused ion beam deposition relies on an adsorbed organo-metallic precursor gas on the silicon surface. When the ion beam scans over an area with adsorbed gas, the gas dissociates and metal is deposited on the surface of the substrate. Ideally, the organic components of the precursor gas will become volatile and leave pure metal behind as the deposited material, but in practice this does not occur. The deposited materials tend to be amorphous, composed of the desired metal along with carbon, oxygen, and occasionally

substrate material.[18] The materials available for ion-induced deposition are limited by the need for an appropriate precursor gas, but include gold,[19] platinum,[18,20] tungsten,[21] and silicon dioxide.[22]

The rate of accretion for FIB-deposited material depends not only on the characteristics of the ion beam, but also on the pressure and flow rate of the precursor gas. Focused ion beam deposition is further complicated by the fact that both the substrate and the deposited material are subject to milling during deposition. If the gas flow rate is too low to refresh the adsorbed precursor layer on the surface as it reacts, there will be more undesirable milling, adversely impacting the deposition rate. A detailed calculation of the atoms deposited per indicant ion, known as net yield, must consider all these factors.[19,23,24]

The semiconductor industry primarily uses focused ion beam systems to repair and modify lithography masks, though FIBs find some use in microcircuit repair during the research and design phase of a device. There is not much in the available literature concerning mask repair using focused ion beams. It is generally a simple process: excess material defects are milled away, and insufficient material defects are filled through ion-assisted metal deposition. Ion milling may be used to repair phase shift masks as well, though the ion radiation has the drawback of causing transmittance reduction in the quartz material that compose the masks.[25] This can be resolved by using ion-assisted etching using a much lower doses than ion milling, and hence far less transmittance reduction to the quartz. Focused ion beam repair of stencil masks has also been investigated.[26] Since clear areas for a stencil mask are gaps in the mask, the challenge is repairing insufficient material defects without a substrate on which to deposit material.

The repair is possible by building up a bridge of the deposited material across the gap, though more work needs to be done to determine the feasibility of this process in industry use.

The first attempts at circuit repair involving the joining of conductors occurred before the advent of ion-induced metal deposition using organo-metallic gasses. The method developed by Musil and Melngailis[27,28] relies on ion milling a via through a metal-dielectric-metal layer system. The ion beam mills through the first metal layer and the dielectric, stopping at the underlying layer. In one variant of the technique, the sidewalls of the via are slanted, and evaporated metal is used to make a contact between the two metal layers. In the second variant, the via is milled with vertical sidewalls and a relatively high aspect ratio, then an area of the lower metal layer is sputtered away with the ion beam. Due to the high aspect ratio, the sputtered metal redeposits on the sidewalls of the via, connecting the two metal layers. Obviously, the major drawback to this technique is that it can only connect two vertically separated layers of metal, whereas many circuit-rewiring tasks require horizontal connection.

The main drawback to FIB modification and repair of IC devices is the low writing speed of the beam, which results in a very low throughput. This low throughput makes focused ion repair processes unsuitable for large-scale modification and repair of microchips. The procedure has found most use in the field of microchip testing and prototyping, where the long process time is not as much of a hindrance. Motorola has used FIB repair to speed the design debug phase of its MC68040 microprocessor.[29] The lifetime of FIB repairs to integrated circuits has been investigated to determine the confidence with which FIB repairs may be used during the prototyping phase of a

circuit.[30] The study, performed by Alcatel Telecom, focused on electromigration failure in FIB-deposited metal. The authors found an average lifetime for FIB repairs of several months to several years, which is satisfactory for prototyping needs.

There is little in the literature directly concerning the creation of field effect transistors using FIB processes. However, several devices have been made using a mixed processing approach that combines standard masked lithography with FIB technology to dope the active area, or define the channel. One of the earliest examples of this was a project at Hughes Research Laboratories using a focused ion beam to implant the source, drain, and channel of a MOSFET with a 90 kV B-Pt ion beam.[31] A layer of aluminum was used to block out the heavier platinum ions, while allowing lighter boron ions to pass through and dope the silicon substrate. The gate and contact pads were defined by conventional optical lithography. The electrical characteristics of the FIB-doped device in this case were similar to a comparable device made using a masked broad beam implanter to dope the active area.

A second class of FIB-MOS experiments have used focused ion beams to modify standard MOSFET designs to achieve enhanced performance. Researchers at Hitachi's Central Research Laboratory have fabricated enhancement MOSFETs using a focused ion beam to implant an ultra-short gate.[32,33] Planar lithography was used to fabricate a depletion mode MOSFET, with a thin implanted n-type region as the conducting channel, on a p-type substrate. Boron was then FIB-implanted through the channel, forming a shortp- type region and converting the device into an enhancement mode MOSFET with an effective channel length defined by the width of the implanted region. This FIB-MOS device has slightly higher gain, and significantly improved source-drain breakdown

voltage and short-channel threshold effect when compared to a similar conventional enhancement mode MOSFET.

II.3 BASIC JUNCTION FIELD EFFECT TRANSISTOR THEORY

Field effect transistors are three terminal devices, where a voltage applied to the third terminal, known as the gate, controls the current through the first two, known as the source and drain. In junction field effect transistors (JFETs), the control voltage modulates the depletion regions formed from the interface between p-type and n-type semiconductor regions. The extent of these depletion regions controls the effective size of a conducting channel between the source and drain, and thus changes the resistance of the device. A detailed explanation of basic JFET characteristics follows.

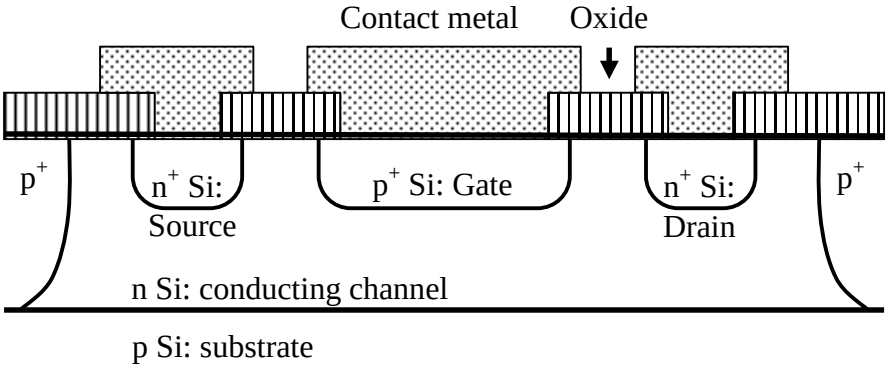

Figure 1: Cross-sectional view of a planar n-JFET.

The simplest planar JFET is shown pictorially in Figure 1, and is denoted an n-JFET due to the n-type conducting channel. The basic structure is formed from an epitaxially grown n-type silicon layer deposited on a p-type silicon substrate. In standard JFET operation, the source is grounded and voltage is applied to the drain, causing electron flow from the source to the drain, as current flows in the opposite direction. The

source and drain regions are heavily doped n^+Si to ensure good electrical contact between the metal and the channel, while the gate is heavily doped to create a larger depletion region to control the channel. The doping may be accomplished through chemical vapor deposition (CVD) or ion implantation, but in both cases thermal diffusion is used to drive the dopant atoms deeper into the device. The oxide and metal regions are defined by photolithography and grown through (CVD) and electron-beam evaporation, respectively. Finally, device isolation is achieved through deep p-type implants.

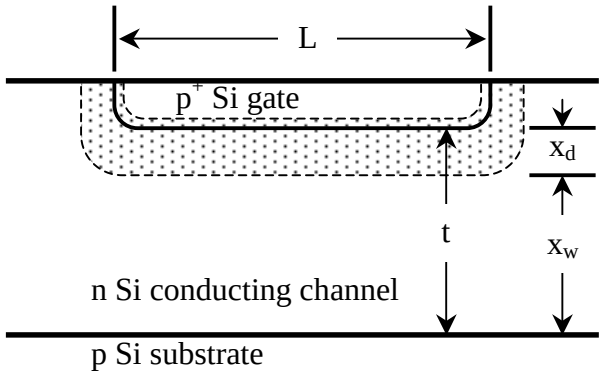

Figure 2: Cross sectional view of JFET channel.

The region of interest for JFET analysis is the area just underneath the gate implant. Figure 2 shows a simple model of the channel, with dimensions of interest labeled, and depletion regions denoted by the shaded area. The length of the p^+ doped gate along the source-drain axis is denoted by L, and the distance between the gate and the substrate is the thickness t. The extent of the depletion region into the channel is x_d, and the undepleted channel width is x_w. The gate width, not shown, generally refers to the dimension of the device perpendicular to the source-drain axis.

Three major approximations must be made for the initial analysis of the device. The first of these is the depletion region approximation. This assumes that the depletion

regions around the *pn*-junction are completely devoid of carriers, and have with sharp boundaries beyond which the density of carriers is equal to the density of donor or acceptor atoms in the material. The second approximation is the quasi-neutrality approximation, which means that number of carriers in any region of a semiconductor is approximately equal to the dopant atom concentration at that point. Therefore, the semiconductor region may be assumed to be neutral with respect to charge. Finally there is the gradual channel approximation, in which it is assumed that only electric fields parallel to the vertical axis within the channel effect the depletion regions. In other words, the assumption is that the field along the length of the channel from source to drain is much less than the field perpendicular to the *pn*-junction.

The gradual channel approximation allows the extent of the depletion region at any point along the channel length to be treated as a one-dimensional problem. Therefore, an analysis of the junction can be made and extrapolated to find the characteristics of the device. When two differently doped semiconductor regions come into contact to form a *pn*-junction, the electrons from the n-type region will diffuse into the p-type region. Likewise, holes will diffuse into the n-type region. The diffused carriers will combine with and neutralize the majority carriers in the region, thus creating a space-charge region depleted of carriers with uncompensated donor or acceptor ions in the semiconductor lattice. These uncompensated ions will create an electric field across the depletion region, which balances the diffusion across the junction. The extent of the depletion regions at equilibrium is determined by the requirement that the electric force balance diffusion, and by conservation of charge. Since depletion regions are almost entirely devoid of carriers, almost no current flows through them.

Analysis of the *pn*-junction begins with the one-dimensional Poisson equation,

$$-\varepsilon_s \frac{d^2\phi}{dx^2} = \varepsilon_s \frac{dE}{dx} = \rho = q(p - n + N_d - N_a)$$

Here, $\phi(x)$ is the electric potential as a function of position x, $E(x)$ is the electric field, ε_s is the dielectric permittivity within the semiconductor, and q is the charge of an electron. The space-charge density ρ is the sum of the hole density p, the electron density n, the atomic donor density N_d, and the atomic acceptor density N_a, where n and N_d are negative due to the charge of the electron. Within the depletion regions, the hole and electron densities may be assumed to be zero by the depletion approximation, leaving $\rho=N_d$ in the channel, and $\rho=N_a$ in the gate. This simplification allows integration of the Poisson equation over the depletion regions to determine an electric field of

$$E(x) = -\frac{qN_d}{\varepsilon_s}(x_n - x), \text{ for } 0 < x < x_n$$

$$\text{and } E(x) = -\frac{qN_a}{\varepsilon_s}(x_p + x), \text{ for } -x_p < x < 0,$$

where x_p and x_n are the boundaries of the depletion region in the gate and channel, respectively. At $x = 0$, the requirement that the electric field be continuous leads to the statement of charge conservation $N_a x_p = N_d x_n$. This derivation also yields a potential drop across the depletion region, called the built-in potential ϕ_i:

$$\phi_i = \frac{kT}{q} \ln \frac{N_d N_a}{n_i^2}$$

where k is Boltzmann's constant, T is the temperature, and n_i is the intrinsic carrier concentration of the semiconductor. Finally, the total width of the depletion region is:

$$x_n + x_p = \left[2\frac{\varepsilon_s}{q}\phi_i\left(\frac{1}{N_a}+\frac{1}{N_d}\right)\right]^{\frac{1}{2}}$$

For the case of the simple JFET, the heavily doped gate region implies that $N_a >> N_d$, so $x_n >> x_p$ and the extent of the depletion region into the channel can be approximated as:

$$x_d = x_n = \left[2\frac{\varepsilon_s}{q}\phi_i \frac{1}{N_d}\right]^{\frac{1}{2}}$$

A voltage applied to the gate disrupts this equilibrium. Positive voltage on the gate can forward bias the junction, causing ohmic current flow if it is greater than the junction's built in voltage; JFETs are not usually operated with forward bias on the gate. Negative voltage on the p^+ gate acts to reverse bias the junction. This and drives carriers further away from the junction and increases the depletion region, so that with an applied gate voltage V_G:

$$x_d = \left[2\frac{\varepsilon_s}{q}\left(\phi_i - V_G\right) \frac{1}{N_d}\right]^{\frac{1}{2}}$$

This equation can be applied to the simple JFET model, so that for an applied gate voltage V_a the thickness of the conducting channel under the gate is $x_w = t\text{-}x_d(V_G)$.

For very low drain-source voltages, the conducting channel has an effective linear resistance R_{lin} given by:

$$R_{lin} = \rho\frac{L}{x_w W}$$

where the channel resistivity $\rho = (q\mu N_d)^{-1}$, with μ denoting the electron mobility within

the semiconductor. Therefore, if a small voltage V_{DS} is applied from the drain to source (which is generally assumed grounded) of a JFET, the current through the channel is given by:

$$I_{DS} = \frac{q\mu_n N_d x_w}{L} V_{DS}$$

In terms of the built in and applied voltages on the gate junction, this becomes:

$$I_{DS} = q\mu_n N_d t \frac{W}{L}\left(1 - \left[\frac{2\varepsilon_s}{qN_d t^2}(\phi_i - V_G)\right]^{\frac{1}{2}}\right) V_{DS}$$

When a significant voltage is applied at the drain terminal, the resultant voltage drop across the length of the channel can cause the depletion region to vary along with the voltage, as shown in Figure 3.

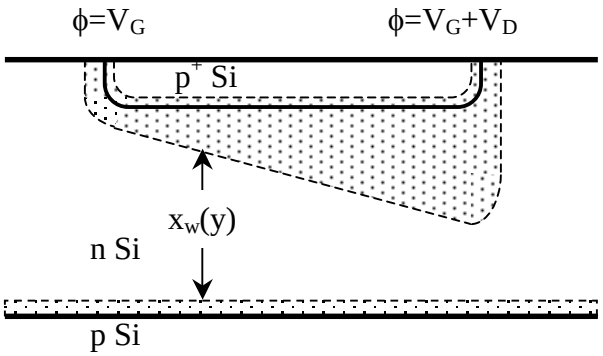

Figure 3: Cross sectional view of JFET channel with applied gate and drain voltage.

Using the gradual channel approximation, the extent of the depletion region at any point along the channel can be calculated as a function of the voltages on the gate and drain with respect to the source. Since there are no sources or sinks of current along the channel, the current I_{DS} must remain constant. Therefore, the differential voltage drop $d\phi$ will be equal to $I_{DS}\, dR$. If the length dimension of the JFET is denoted by y, then dy is

the differential length element and $d\phi$ is given by:

$$d\phi = \frac{I_{DS}\,dy}{Wq\mu_n N_d x_w(y)}$$

The term $x_w(y)$ in this expression is the width of the conducting region as a function of distance along the channel. It is a function of the gate voltage as described above, with an additional voltage term $\phi(y)$ that arises from the voltage applied to the drain:

$$x_w = t - \left[\frac{2\varepsilon_s}{qN_d}\left(\phi_i - V_G + \phi(y)\right)\right]^{\frac{1}{2}}$$

The entire expression can be integrated over 0 to L in y, and 0 to V_{DS} in to ϕ obtain:

$$I_{DS} = G_0\left(V_{DS} - \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d t^2}\right)^{\frac{1}{2}}\left[\left(\phi_i - V_G + V_{DS}\right)^{\frac{3}{2}} - \left(\phi_i - V_G\right)^{\frac{3}{2}}\right]\right)$$

In this equation, the term G_0 corresponds to the conductance of the channel when completely undepleted:

$$G_0 = q\mu_n N_d t\frac{W}{L}$$

For low V_{DS}, the I_{DS} equation reduces to the expression previously derived by assuming only negligible voltages on the drain, and is linear: for any given gate voltage, the JFET behaves like an ohmic resistor for very small voltages on the drain. At larger voltages, decreasing channel dimensions causes the current to increase less than linearly with voltage. Finally, the channel will become depleted at one end as $x_w \to 0$ close to the drain, a condition known as pinch-off. At this point, electrons will continue to flow from source down the mostly undepleted channel, and sweep through the pinched-off depletion

region to the drain due to the high electric fields across it. Further increasing the drain voltage after pinch-off causes only a greater voltage drop across the pinched-off depletion region, so the current saturates at a constant value. The saturation current I_{DSat} is:

$$I_{DSat} = G_0\left[\frac{qN_d t^2}{6\varepsilon_s} - (\phi_i - V_G)\left(1 - \frac{2}{3}\left[\frac{2\varepsilon_s(\phi_i - V_G)}{qN_d t^2}\right]^{\frac{1}{2}}\right)\right]$$

Saturation occurs at the pinch-off voltage, V_{DSat}:

$$V_{DSat} = \frac{qN_d t^2}{2\varepsilon_s} - (\phi_i - V_G).$$

Finally, the entire channel will be depleted for a sufficiently negative gate, and no current will flow. This is the turn-off voltage, V_T:

$$V_T = \phi_i - \frac{qN_d t^2}{2\varepsilon_s}.$$

Chapter III: DEVICE FABRICATION

III.1 DESIGN

The JFET design that was used in this project was chosen for simplicity and potential for creation using the tools at hand; this transistor design is unique because it can be fabricated using only FIB techniques. The final design is shown in Figure 4. The device is formed on a mesa of epitaxially deposited n-type (100) silicon on top of silicon dioxide, with an isolated p-type base layer separating the two. The source and drain regions are defined by arsenic (As) implantation, and the gates by boron (B) implantation. Finally, FIB-deposited platinum lines and contact pads allow connection to the device's terminals.

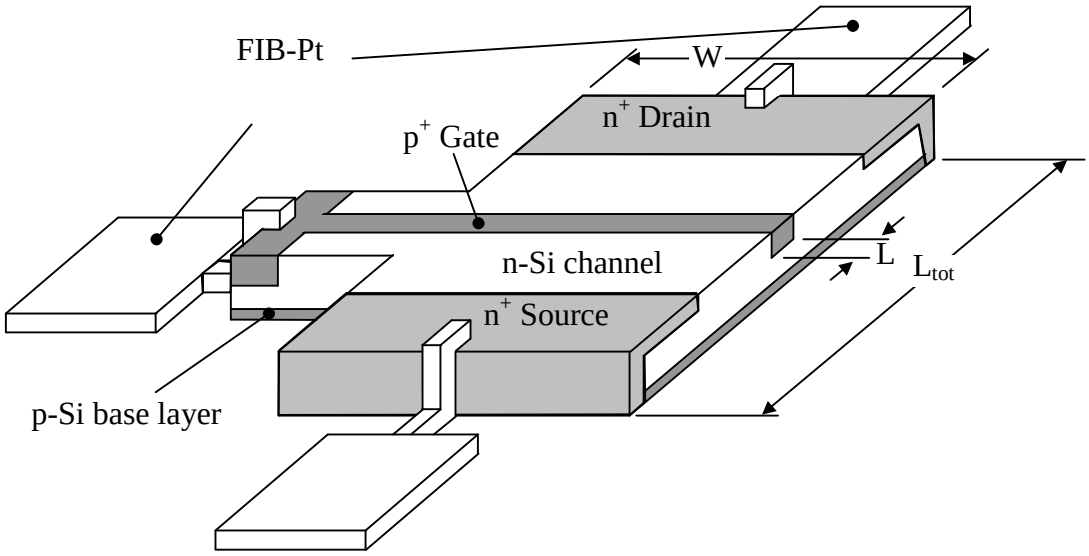

Figure 4: Diagram of maskless planar FIB-JFET.

The FIB-implantation of the gate determines the channel length *L*, allowing precise control over this dimension. For the device diagrammed above, *L* is one

micrometer. This gate dimension allows for a device that exhibits short-channel effects without being dominated by them. The range of the p-type dopant into the silicon determines the effective channel thickness *t*, and is a function of the beam energy and the ion species used. The physical length and width of the active area, L_{tot} and W respectively, are roughly ninety micrometers. The source and drain areas are ninety micrometers wide by thirty micrometers long, though in some devices they are longer to cut down on channel resistance. The gate spar, fifty micrometers long and roughly twenty micrometers wide, serves to isolate the gate contact implant from the source and drain implants. A two hundred angstrom layer of thermal silicon dioxide covers the active area, save for three wide vias to allow contact with the metallization. Finally, each platinum contact pad is approximately a square fifty micrometers on each side. The contact pads are connected to the device terminal by a slightly thinner platinum area, shown smaller than actual size in Figure 4 for clarity.

The physical dimensions of the mesa used in this design are large, especially when compared to the submicrometer dimensions that are currently standard in industry. Ideally, the total device length would be small in comparison to the device width, in order to minimize the extra resistance found in series with the channel. FIB-deposited platinum, however, requires a large contact area to obtain reasonable contact resistances to the heavily doped silicon at the source and drain terminals. Using a larger mesa size also eliminates much of the potential error associated with aligning the sample in the FIB systems so that only the desired area is exposed during each step. This equates to a higher yield in a process that is intrinsically slow. Therefore, a larger mesa size is a worthwhile trade-off, especially since the gate is directly written by the FIB. Therefore,

the active area of the device is controllable, and can be made as small as desired despire the large mesa size.

An alternate JFET configuration is worth mentioning – the lateral FIB-JFET, shown in Figure 5. This device is similar to the JFET in Figure 4, except that there are two gate terminals, and the depletion regions pinch-off the channel parallel to the length of the channel. In this configuration, the focused ion beam directly controls the extent of the gates into the channel. This is the main advantage of the lateral FIB-JFET: that theoretically it can be directly tailored for any gate configuration.

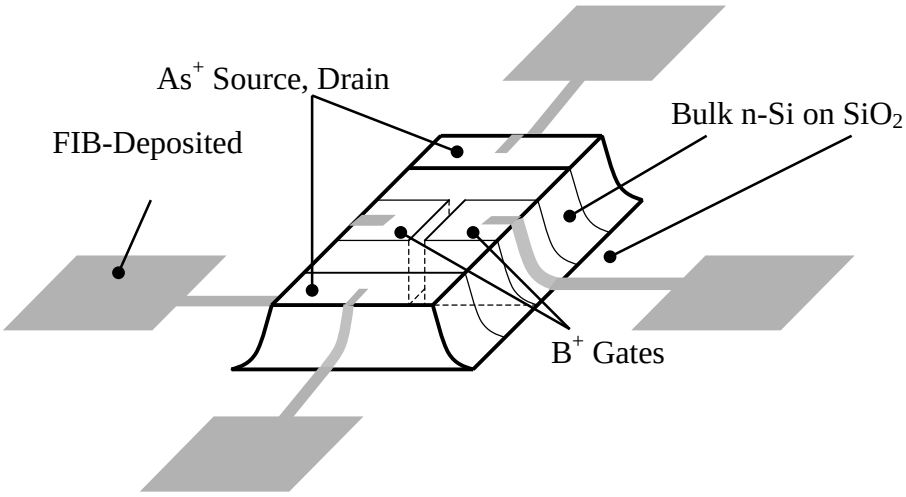

Figure 5: Diagram of maskless lateral FIB-JFET.

Achieving this precise gate tailoring is difficult in practice, however, due to the nonuniform implantation profile of accelerated ions into materials. Thermal diffusion can even out the depth profile, but would also diffuse out the precisely implanted lateral profile as well. Using multiple exposures at varying ion energies to achieve a more uniform range profile is not practical, as changing the energy of a FIB column necessitates refocusing and sample realignment. Placing two ion implants at differing

energies to within the submicrometer tolerances required by the gate is not possible with the equipment available. Finally, a channel thin enough to see a roughly uniform ion dose from a single implant would be subject to modulation by the interfaces with the oxide at the top of the channel, and the p-type layer at the bottom. For these reasons, the several lateral JFETs fabricated for this project did not work, and the design was abandoned in favor of the planar JFET structure.

III.2 FABRICATION PROCESS

The JFET devices were built on silicon on insulator (SOI) chips, which incorporate a layer of silicon dioxide buried under the surface of the silicon wafer to enhance device isolation. This buried oxide layer is created by implantation to drive in the oxygen and damage the silicon crystalline lattice. Subsequent heating to anneal out the damage incorporates the oxygen into the lattice and forms silicon dioxide beneath the surface. The reformed silicon surface layer is crystalline, but of relatively poor quality due to the previous damage and heating. Therefore, a new silicon layer is epitaxially grown on the surface with the desired resistivity for device fabrication. The SOI wafer for this project was purchased pre-fabricated. The base wafer was lightly-doped p-type silicon with <100> orientation and a resistivity of 10-20 Ω·cm, with a four inch diameter. The buried oxide was 3750 Å thick underneath 1900 Å of reformed p-Si. Finally, 4000 Å of epitaxially-grown n-type Si <100> were grown on the surface, with a resistivity of 0.08 Ω·cm. Once the wafers were obtained, they were broken into smaller chips to allow for multiple experimental runs and process tests with a limited number of purchased SOI wafers.

The chips were cleaned prior to processing by immersion in piranha etch, a 5:1 mixture of sulfuric acid (H_2SO_4) and hydrogen peroxide (70% H_2O_2 in water). After ten minutes in the piranha to clean trace metals and organic residue, the chips were rinsed in deionized (DI) water, dipped in hydrofluoric acid (HF) for five seconds to remove any native oxide, then rinsed in DI water again. This piranha etch is the standard cleaning procedure used throughout the fabrication process until the metallization was complete.

The first step in the fabrication process was definition of the silicon mesa for the active area of the device. This was accomplished through conventional photolithography rather than FIB lithography, to simplify the process. Focused ion lithography is a well-studied process, but generally requires a complex multi-level resist structure or a source of light ions such as hydrogen or helium, neither of which were available for this work. An available mask set with an appropriate pattern was used to define the active area. Etching was performed by immersion in poly-Si etchant, a mixture of nitric acid (HNO_3), deionized water (H_2O), and hydrofluoric acid (HF) in a 64:33:3 ratio. Poly-Si etchant was preferred over a more directional reactive ion etch (RIE), as wet etching results in sloping sidewalls for the features formed. This in turn allows for directional focused ion implantation of the entire sidewall which is crucial for later making contact to the area, as the metallization must make contact to only the implanted region. This is illustrated in Figure 6.

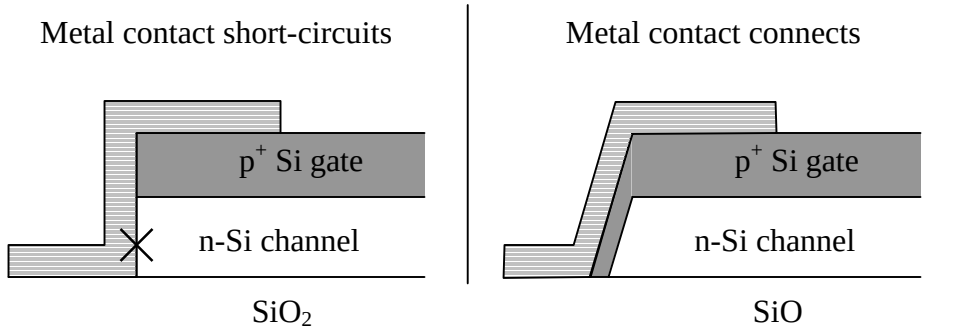

Figure 6: Straight vs. sloping sidewalls for contacts.

After mesa definition, rapid thermal oxidation (RTO) was used to thermally deposit 200 Å of SiO_2 on the surface of the mesa. The samples were quickly brought to 775 ˚C in an oxygen environment using a quartz lamp oven, and held at that temperature for 30 seconds to allow the oven to stabilize. The temperature was then raised to 1125 ˚C at a rate of 60 ˚C per second, and kept in a constant flow of oxygen at atmospheric pressure for 15 minutes, followed by a slight cool-down and fifty seconds of annealing in a nitrogen environment at 1050 ˚C. The samples were then allowed to cool normally to room temperature in a flow of nitrogen at atmospheric pressure, a process which took fifty minutes. This process forms the oxide layer and consumes approximately 88 Å of silicon from the surface of the mesa. The thermal oxide growth is omnidirectional, so the oxide covers the mesa sidewalls as well. The oxide serves to eliminate conduction paths along the surface of the device, and keep the gate isolated from the source and drain. Additionally, the process also causes diffusion in the active area, where donor atoms from the more heavily doped n-Si epitaxial layer spread into the lightly doped p-Si layer and overcompensate the acceptors there, turning the entire active area n-type.

After oxidation, the mesa was ready for ion implantation in a 150 kV FIB

implanter built by Nanofab. This system is compatible with a variety of liquid metal ion sources, allowing for operation with a variety of ion species. The LMIS used for this project contained an alloy of arsenic, palladium, and boron (As/Pd/B). It was run with a heater current of 3 A, and an extraction voltage of 10 kV to achieve optimal emission. The As/Pd/B LMIS emits boron (B^+) and arsenic (As^+), which can act as electron acceptors and donors, respectively, when placed into a silicon crystal lattice. As^{++} is emitted, but not with enough beam current to dope the source and drain areas in a reasonable time. Other emitted ion species contain palladium, and so are not suitable for silicon doping. The FIB column contains an E×B mass filter that allows implantation of the substrate by a single ion species, as undesirable species are filtered out.

The chip to be processed was mounted on a six-inch silicon dummy wafer, which fits into a removable aluminum pallet designed for the Nanofab FIB. This pallet locks onto a stage within the implanter, which is driven by piezoelectric motors. The stage position, measured by laser interferometry, is controllable to within fifty nanometers under optimum conditions. Since the Nanofab does not have the ability to rotate either the stage or the focused ion beam, axial alignment to the stage must be performed manually during the mounting process, to a high a degree of precision as possible. An optical microscope was used to align the sample to two cross marks on opposite sides of the stage, FIB-milled at the same y-position as measured by the laser interferometers. The sample rotation with respect to the stage after this alignment procedure was less than 0.04 degrees. Once the sample was aligned and inserted into the FIB system, a few of the patterned areas were designated as test areas, and FIB imaged for measurement purposes. The imaging dose is greater than the dose usually used for implantation, so simply using

the FIB to look at a semiconductor device ruins it. For this reason, a few test areas were sacrificed for in-situ measurement of the precise distance between the area to be patterned and identifiable alignment markers some nearby on each area.

For device implantation, the local alignment marks were found via imaging, then the stage was blindly moved to the active area. The dopant ions were implanted through the oxide grown previously, which served to scatter the incident ions somewhat and reduce channeling. The source and drain regions were implanted with As^+ accelerated through 120 kV, at a dose of 2×10^{15} ions per cm^2. The high accelerating voltage served to drive the ions deeply into the channel, and the high dose served to ensure that the source and drain regions would be strongly n^+ after thermal annealing. The gate was implanted with 10 kV B^+ ions, with dose from 10^{14} to 10^{15} ions per cm^2. Since boron ions have a much lower atomic weight than arsenic ions do, this lower acceleration energy was sufficient to drive the boron ions deep enough to form a conducting channel an appropriate distance into the silicon for transistor operation. The dose was varied for different devices to achieve different junction depths; higher doses result in higher concentrations of boron deep within the channel, and therefore a deeper metallurgical junction. Varying the implantation energy is a more direct way of controlling the implantation ion range and therefore the junction depth. The FIB implanter cannot vary ion energy while the ion beam is in use however, and this technique is thus unsuitable for devices where the doping depth profile varies along the length of the channel.

After implantation, the chips were cleaned again and the dopant atoms activated by rapid thermal annealing (RTA), in the same oven used to grow the oxide. This was done by heating to 1100 ˚C for ten seconds, in a nitrogen environment. This is sufficient

to reform the crystal lattice and incorporate the implanted donor and acceptor ions, but not long enough to cause much significant diffusion. Limited diffusion is necessary to keep the implanted gate region from spreading too much and destroying the conducting channel below the gate. The ten second annealing causes the implanted boron gate profile to spread approximately one tenth of a micrometer, which is acceptable. Arsenic has a much lower diffusivity, and therefore the source and drain profiles change very little during annealing.

The final major step in the fabrication process was metallization, to provide contacts from the device to a needle probe station for testing. This was accomplished using FIB-induced platinum deposition, to make the contact pads and connect them to the active area of the device. Due to the size of the needle probes, the contact pads needed to be at least fifty micrometers on a side, which requires a substantial amount of FIB-deposited material to produce. The FIB metal deposition process results in exposure of the surrounding areas to the beam, causing damage and implantation of gallium ions. Therefore, the active device areas must be protected during metallization.

Protection of the active areas was accomplished by spinning Shipley 1813 photoresist over the chip, at a speed of 3000 rpm to produce a layer 1.85 μm thick. The resist was pre-baked at 100 ˚C for one minute, then exposed in octagonal patterns 100 μm wide using a Leitz optical microscope focused at high magnification to illuminate and expose the contract area for three minutes. Ultraviolet filters were removed from the microscope during this procedure to allow full spectrum illumination of the resist. The resist was developed by immersion in Shipley 352 developer for one minute, then hard baked for ten minutes at 120 ˚C, which reduced the photoresist thickness to 1.7 μm.

With the photoresist layer in place, the chip was given a ten second O_2 plasma cleaning to remove organic residue on the exposed surfaces, then dipped in HF for 25 seconds to strip the 200 Å of thermal oxide on the surface. Metallization was done in a Dual Beam 620 FIB/SEM (scanning electron microscopy) system, made for microcircuit imaging and repair through milling and metal deposition. A 30 kV Ga^+ ion beam was used to induce platinum deposition, with a beam current of 1000 pA, a dwell time of 0.2 μs and a -50% overlap between dwell points. The approximate pattern size for each contact pad was 60 μm by 60 μm, and the FIB took 40 minutes to deposit to a nominal thickness of 0.25 μm. The precursor compound used was (trimethyl)-methlcyclopenta-dienylplatinum ($(CH_3)_3(CH_3C_5H_4)Pt$), heated to 39 ˚C to vaporize it into a gaseous state. After deposition of all contacts was complete, the resist was stripped in acetone, and the chip heated to 400 ˚C for 20 minutes in H_2N_2 forming gas. This forming gas step served to both sinter the platinum contacts and passivate the silicon-oxide interface. A SEM image of the finished device is shown in

Figure 7, with a reference bar at the bottom to indicate scale. The imaging beam was accelerated to 20 kV, and had a current of 84 pA. The overall image is dark due to the thermal oxide covering the surface of the device, which contrasts poorly with the buried oxide layer the device is fabricated on. Silicon dioxide, as an insulator, has a low secondary electron emission rate which makes it appear dark to SEM imaging. The three bright rectangular areas are the FIB-deposited platinum contact pads. The lighter octagonal areas around them are where the oxide was etched away to allow the platinum to contact to the source, gate, and drain terminals. The silicon mesa upon that serves as the active area of the device is visible due to the relatively high voltage used: 20 kV

electrons are energetic enough to penetrate the surface oxide and generate secondary electrons from the silicon underneath. The mesa's outline has been highlighted in the SEM image by a dashed line, for clarity.

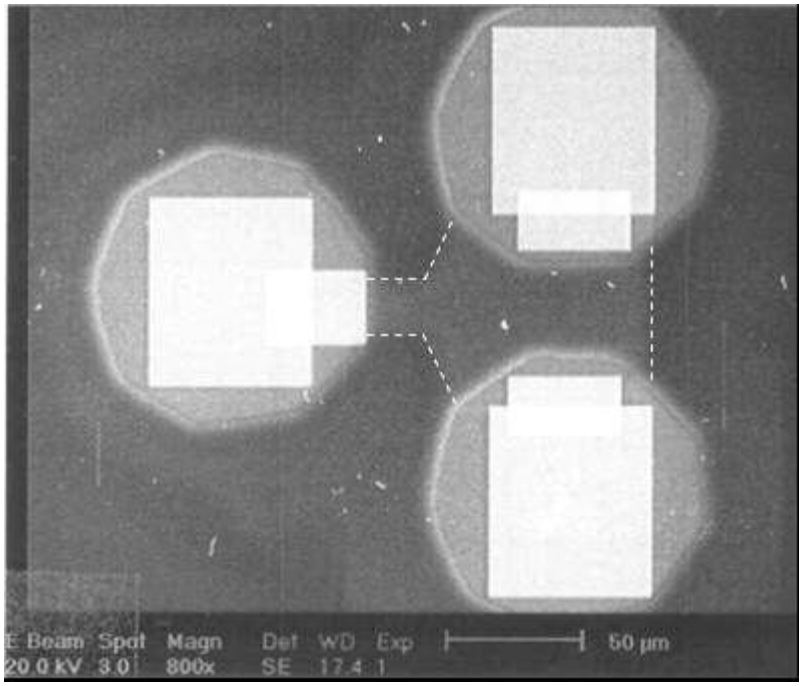

Figure 7: Top-down SEM image of planar FIB-JFET denoting mesa dimensions.

III.3 FABRICATION PROCESS ILLUSTRATED

This section presents the previously described fabrication process in a visual format for purposes of illustration. The dimensions in Figure 8 to Figure 14 are not to scale.

SOI wafer as purchased on standard 4" p-Si wafer

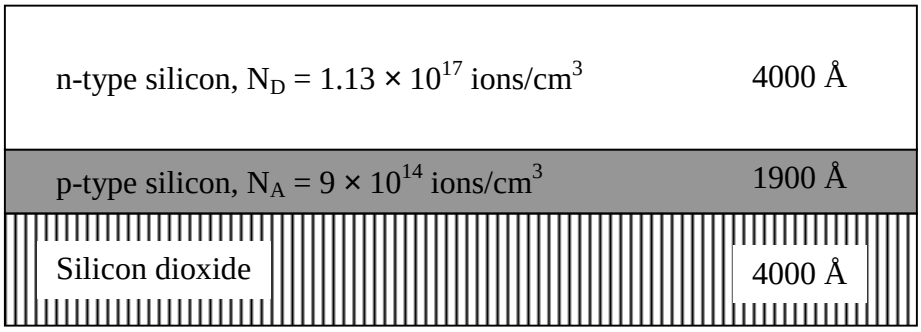

Figure 8: Cross sectional view of SOI wafer as purchased.

Mesa definition by conventional lithography and poly-Si wet etch

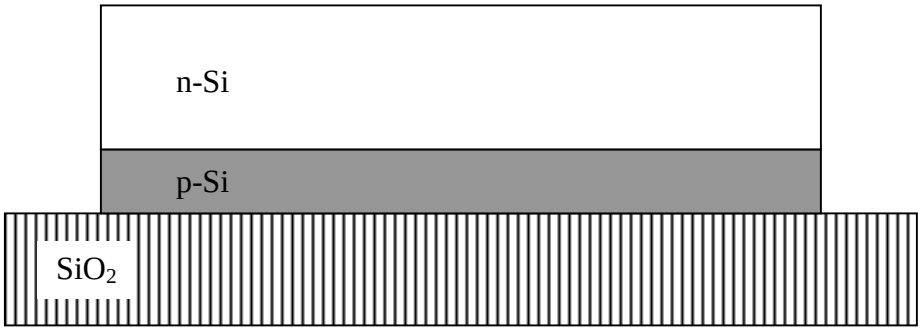

Figure 9: Cross-section of wafer after mesa definition

Rapid thermal oxidation to grow surface oxide, and dopant diffusion
15 minutes at 1125 ºC; 200 Å SiO_2 grown on exposed Si surfaces

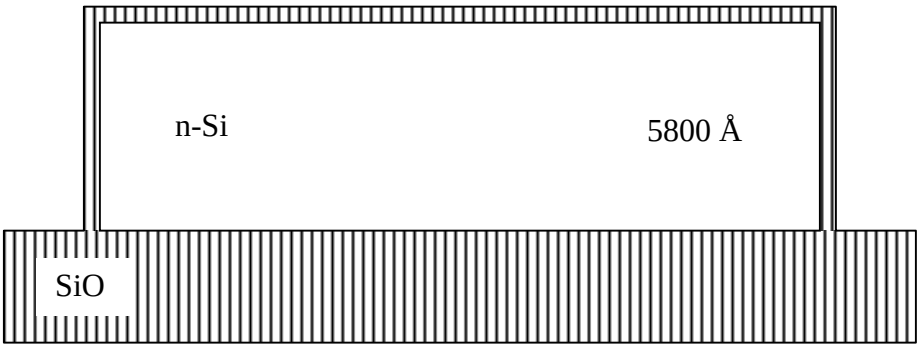

Figure 10: Cross-section of wafer after rapid thermal oxidation

Source, gate, and drain regions doped via patterned FIB implantation,

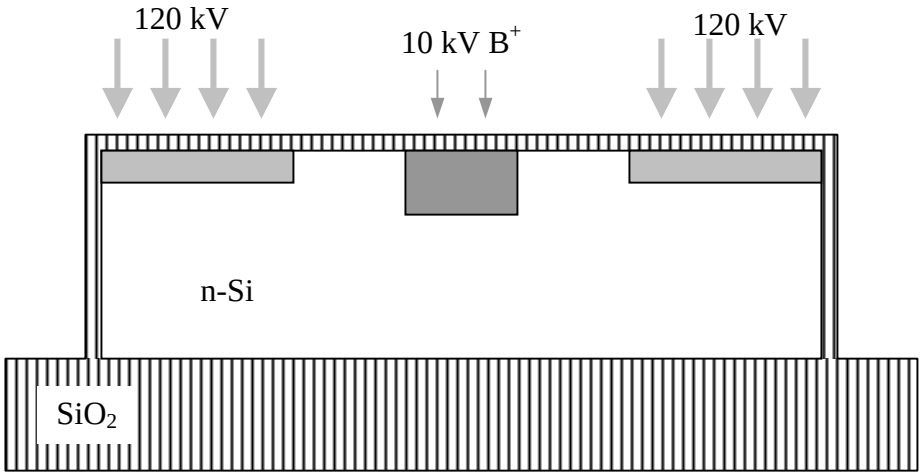

Figure 11: Cross section of wafer during focused ion beam implantation

Rapid thermal annealing to activate and diffuse dopant atoms

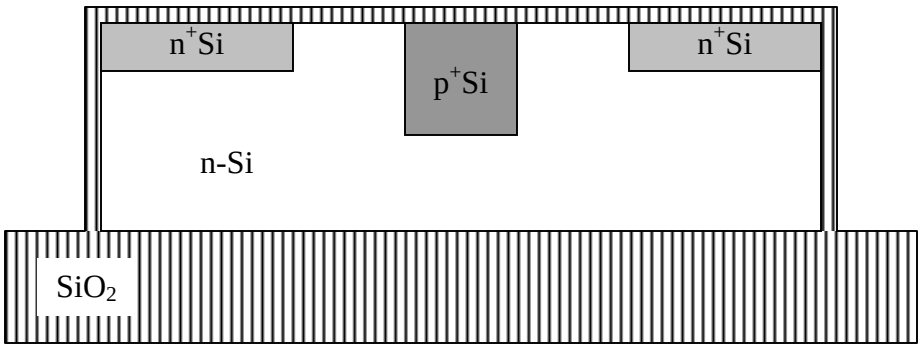

Figure 12: Cross sectional view of wafer after rapid thermal annealing

Optical microscope lithography to define contact areas for metallization

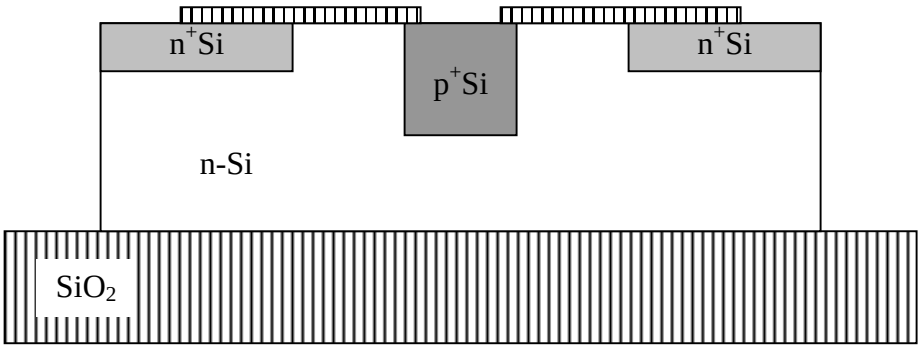

Figure 13: Cross section of wafer with contact areas exposed for metallization

FIB-induced Pt deposition with 30 kV Ga^+ beam to create

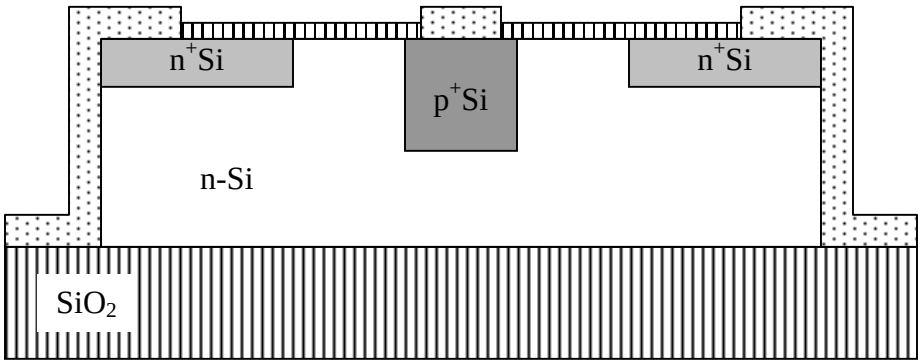

Figure 14: Cross section of finished JFET after FIB-induced Pt deposition

Chapter IV: PROCESS CHARACTERIZATION

IV.1 FOCUSED ION IMPLANTATION

It is important to know the concentration profile of implanted ion species as a function of depth for a given implantation energy, and a variety of models have been constructed to enable the semiconductor industry to do just this. The critical dimension in FIB implantation of a planar n-JFET is the p^+ gate. The extent of the doped region must be such that a conducting channel of undepleted n-type silicon exists under the gate for zero gate bias. At the same time, the *pn* junction created needs to be deep enough that the conducting channel can be cut off by the depletion regions for a reasonable voltage applied to the gate. This creates a need for very precise control of the range and dose of the implanted gate ions. In contrast, the depth of the source and drain implantation does not need to be as carefully controlled as that of the gate, though the dopants must be concentrated enough to ensure that the metallization contact region is strongly n-type. Increasing implant depth and dopant concentration does reduce the device resistance in series with the channel, however, which improves JFET performance.

The path of an ion through solid matter is determined by its collisions with the electrons and nuclei in the medium, referred to as electronic and nuclear stopping respectively. Inelastic electron collisions serve to slow the incident ions without changing their direction of motion. Collisions with the atomic nuclei occur at low energies and tend to be elastic, scattering the ions in different directions. The stopping interactions are stochastic in nature, which makes the path and endpoint of any single ion impossible to determine. Due to the extremely large number of ions involved in FIB

processes, however, statistical methods can be used to model the most probable implantation profile over a large number of incident ions.

One of the first comprehensive attempts to model implantation using the above concepts is known as LSS theory, after its creators Lindhard, Scharff, and Schiott.[6] LSS theory assumes that the target material is amorphous and that the depth profile of implanted ions into a material can be described as a Gaussian function with a mean range and a standard deviation about that range. For the projected range R_p and the standard deviation about the range σ_p, the Gaussian function with peak concentration f_0 is:

$$f(x) = f_0 \exp\left[-\frac{(x - R_p)^2}{2\sigma_p^2} \right]$$

Tables of these variables have been calculated using LSS theory, and are published as a function of ion species, ion energy, and substrate material. For boron at 10 kV into silicon, the R_p is 340 Å and the σ_p is 210 Å. For 120 kV arsenic into silicon, range R_p is 680 Å and σ_p is 280 Å. Gaussian functions with these parameters are shown in Figure 15.

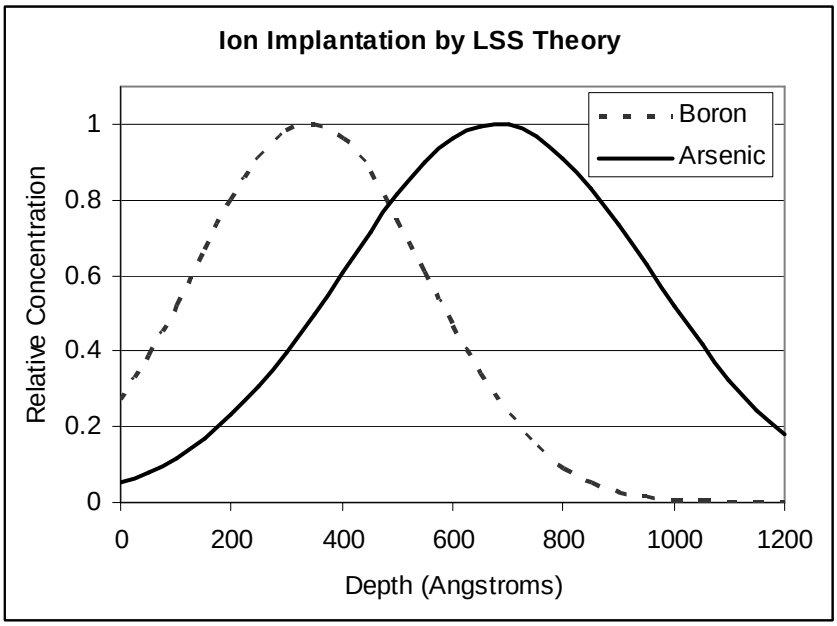

Figure 15: LSS-derived Gaussian functions of boron and arsenic implantation.

Numerical methods are used to obtain higher accuracy in ion implantation simulations. The Monte Carlo method simulates ion trajectories through the target material, with calculated changes in energy and direction brought about by collisions. Large numbers of Monte Carlo generated trajectories are then totaled to model a complete implantation profile for ions of a given energy and species into a target. These profiles can be fairly accurately described by Pearson IV distributions, which are like Gaussians but asymmetric, especially at high energies. In addition to range and deviation, the Pearson IV distribution is also described by parameters for skewness γ and kurtosis β, which is a measure of the distribution's flatness. The equation for a Pearson IV distribution is[34]

$$f(s) = f_0 \exp\left[\frac{1}{2b_2}\ln\left(b_0 + b_1 s + b_2 s^2\right) - \frac{b_1/b_2 + 2b_1}{\sqrt{4b_0 b_2 - b_1^2}}\tan^{-1}\left(\frac{2b_2 s + b_1}{\sqrt{4b_0 b_2 - b_1^2}}\right)\right]$$

where

$$s = x - R_p,$$

$$b_0 = -\sigma_p^2\left(4\beta - 3\gamma^2\right)/A,$$

$$b_1 = -\gamma\sigma_p\left(\beta + 3\right)/A,$$

$$b_2 = -\left(2\beta - 3\gamma^2 - 6\right)/A, \text{ and}$$

$$A = 10\beta - 12\gamma^2 - 18.$$

These parameters were calculated for boron and arsenic implantation into silicon for the energies used in the fabrication process. Fifty thousand ion trajectories were simulated and analyzed using a program called SRIM (Stopping and Range of Ions in Matter).[35] The SRIM calculated Pearson IV parameters for 10 keV boron and 120 keV arsenic implantation into silicon are summarized below in Table 1. Similar calculations were performed for silicon capped with a 200 Å layer of silicon dioxide, and those results are included. The calculated implantation profiles are shown in Figure 16 and Figure 17.

Ion Species	Oxide (Å)	Range (Å)	Deviation (Å)	Skewness	Kurtosis
10 kV B^+	0	422	191	0.121	2.56
10 kV B^+	200	420	192	0.128	2.50
120 kV As^+	0	832	274	0.0998	2.46
120 kV As^+	200	823	266	0.181	2.49

Table 1: SRIM calculated ion range data for implantation

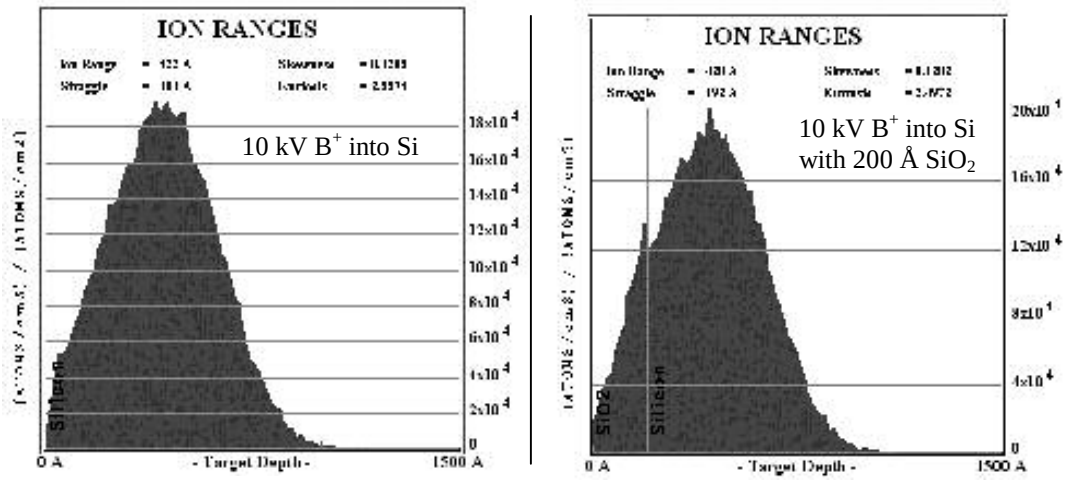

Figure 16: Boron implantaion profiles at 10 kV into silicon calculated by SRIM.

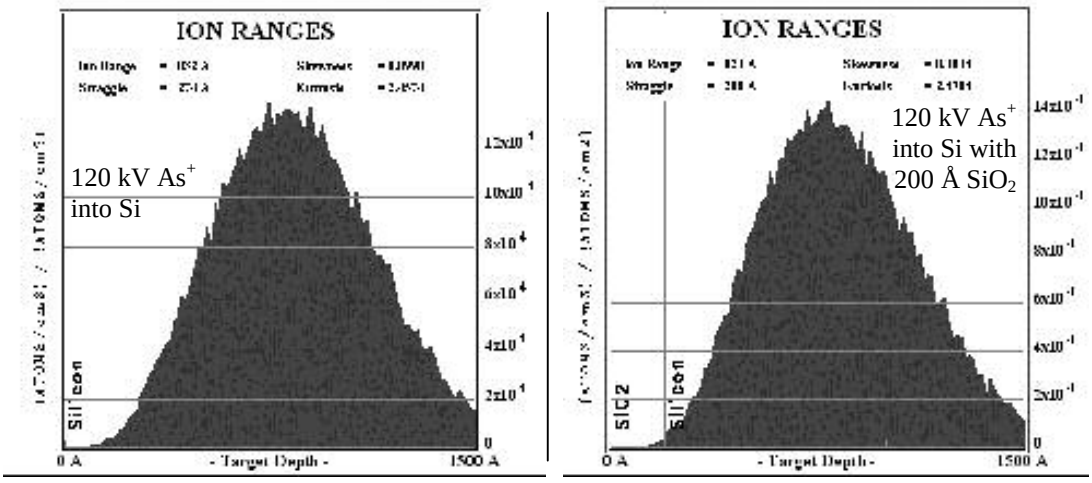

Figure 17: Arsenic implantaion profiles at 10 kV into silicon calculated by SRIM.

Both LSS theory and the above SRIM Monte Carlo calculations assume that the target material is amorphous. Semiconductor grade silicon is crystalline, however, and ion implantation that is parallel to certain crystal orientations will experience far less scattering than it otherwise might in an amorphous target. This will result in deeper penetration of the implanted ions into the substrate when channeling is a factor.

High ion doses (approximately 10^{15} ions/cm^2 for silicon) can damage the

crystalline structure of the substrate surface enough to turn it amorphous, which affect further implantation by reducing channeling. To avoid these complications, most ion implantation is performed with an angle of seven degrees between the beam and the vector normal to the surface of the substrate. This angle is sufficient to ensure minimal channeling and therefore implantation very similar to the case of an amorphous substrate.

The ion implanter used in this project does not have inherent sample-tilt capability, however, so ion channeling must be taken into account when modeling the range of the dopant ions used. Channeling can be beneficial, in that it allows ions to be placed deeper into the substrate and with a greater range deviation than would otherwise be possible at a given energy, without requiring a long thermal diffusion. The channeling-enhanced profile is preferable to one obtained by simply using higher acceleration energies because more of the dopants remain near the surface, which must be strongly doped to provide a good contact.

To accurately model the profile of the channeled ion implantation, a Monte Carlo program called Crystal-TRIM was used.[36] Crystal-TRIM calculations include effects due to the crystal structure, such as channeling and surface damage. Several calculations using this program were run to simulate implantation profiles for various ion acceleration energies, which were then compared. This is how 10 kV was chosen for the gate boron implantation energy. The results of these calculations are given in Table 2, and Figures Figure 18, Figure 19, and Figure 20. The input parameters to Crystal-TRIM are given in Appendix A.I. The silicon/oxide interface is shown as a black line at 200 Å on those charts where implantation was done through SiO_2. Simulations for boron were done with

and without the 200 Å oxide layer, and at doses of 10^{14} and 10^{15} ions per cm^2. The arsenic implantation was simulated with and without the oxide layer, at a constant dose of 2×10^{15} ions per cm^2. Channeling effects, seen in the long tail to the distribution, are clearly visible for low-dose boron implantation without oxide. As expected, channeling is not as much of an issue with implantation through oxide, or with high doses where the ions damage the surface of the silicon.

Ion Species	Dose (ions/cm^2)	Oxide (Å)	Range (Å)	Deviation (Å)	Skewness	Kurtosis
10 kV B^+	10^{14}	0	1067	528	0.164	2.16
10 kV B^+	10^{14}	200	430	233	1.24	6.60
10 kV B^+	10^{15}	0	837	440	0.690	3.10
10 kV B^+	10^{15}	200	422	213	1.04	6.05
120 kV As^+	2×10^{15}	0	865	358	1.68	11.9
120 kV As^+	2×10^{15}	200	815	289	0.765	5.61

Table 2: Crystal-TRIM calculated ion range data for implantation

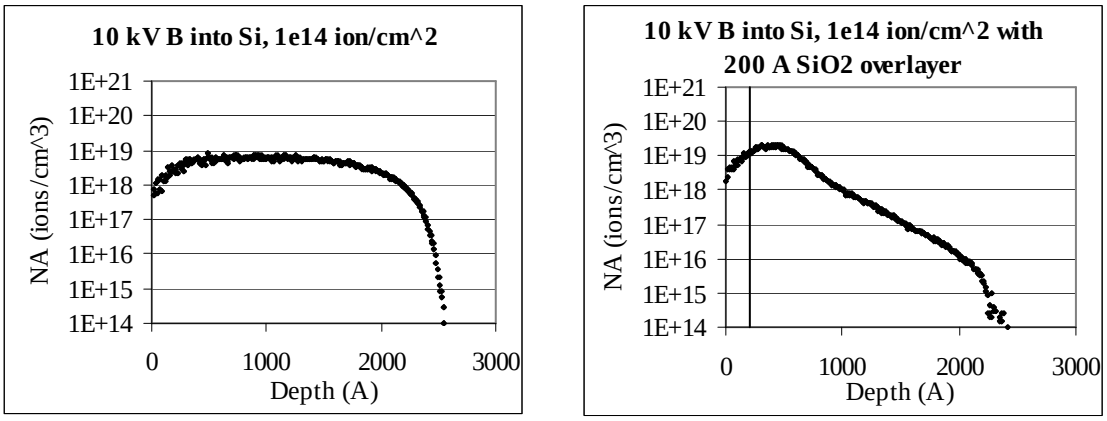

Figure 18: Boron implantation into Si, at 10 keV and 10^{14} ion/cm^2, calculated by Crystal-TRIM

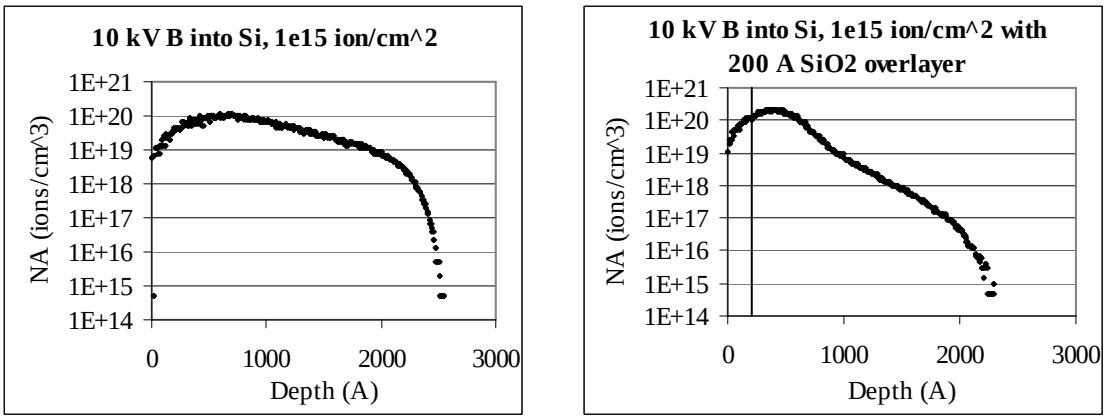

Figure 19: Boron implantation into Si, at 10 keV and 10^{15} ion/cm^2, calculated by Crystal-TRIM

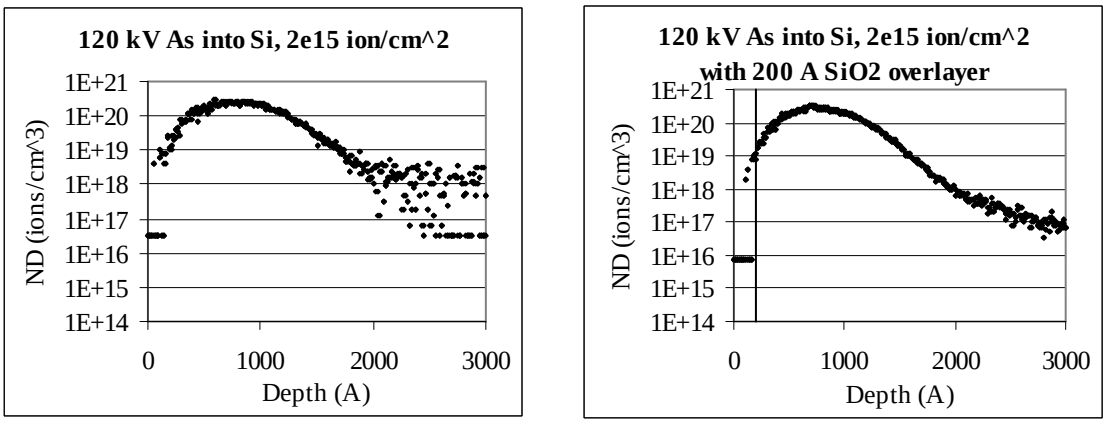

Figure 20: Arsenic implantation into Si, at 120 keV and 2 x 10^{15} ion/cm^2, calculated by Crystal-TRIM

IV.2 THERMAL ANNEALING

Thermal annealing to activate the implanted ions will cause the dopant distribution to smooth out and spread slightly. Due to the extremely short heating period used in RTA, the dopant spread will be on the submicrometer scale for boron, which is a relatively fast diffuser in silicon. This is sufficient to impact the gate dopant depth profile considerably and must be taken into account during device simulation to correctly calculate the extent of the depletion region under the gate. Additionally, the RTO process

used to form the surface oxide on the device will cause diffusion between the phosphorous doped epitaxial layer and the underlying p-Si layer, and this must be accounted for as well.

Three equations are used to describe the annealing and diffusion process in silicon.[37] The first is the Poisson equation in three dimensions,

$$\nabla \cdot \left(\varepsilon \ \vec{E} \right) = q\left(p - n + N_D^+ - N_A^- \right)$$

where $\boldsymbol{E}$ is the vector electric field as a function of position in three dimensions, and ε is the dielectric permittivity, which is not necessarily a constant. Second, a flux equation can be written for each diffusing species in the material, including not only donor and acceptor atoms but also interstitial and vacancy defects created by ion damage during implantation. For each species denoted by a subscript i, the vector particle flux $\boldsymbol{J}_i$ is given by:

$$\vec{J}_i = -D_i \nabla S_i + Z_i \mu_i S_i \vec{E}$$

In this equation, D_i and S_i are the concentration and diffusivity of each species, respectively, while Z_i is the charge state and μ_i is again the field-dependent mobility. Finally, conservation of mass requires a continuity equation for all species, with the generation-recombination rate given by G_i:

$$\frac{\partial S_i}{\partial t} + \nabla \cdot \vec{J}_i = G_i$$

Simulation of dopant diffusion for the maskless JFET was done using TSuprem4, an update of the Stanford SUPREM program.[38] The wafer as purchased had a 4000 Å epitaxial n-type layer on the surface, with a concentration of 1.13×10^{17} cm^{-3}

phosphorous ions. The layer underneath is boron doped with a concentration of 9×10^{14} cm^{-3}, separated from the bulk of the wafer by 3750 Å of silicon dioxide. The rapid thermal oxidation step – fifteen minutes at 1125 ˚C to grow silicon dioxide – also causes the phosphorous dopants in the epitaxially deposited n-Si layer to diffuse into the lightly doped underlying p-Si region. This has the effect of obliterating the p-type region and making the entire surface layer above the oxide n-type. TSuprem4 was used to simulate the diffusion of phosphorous throughout these three regions, and the results are shown in Figure 21, with the original distribution given by the dotted line, and the diffused profile in a solid line. The dotted vertical line at 0.59 μm is the silicon / oxide interface. The input file used in TSuprem4 is given in Appendix A.I.

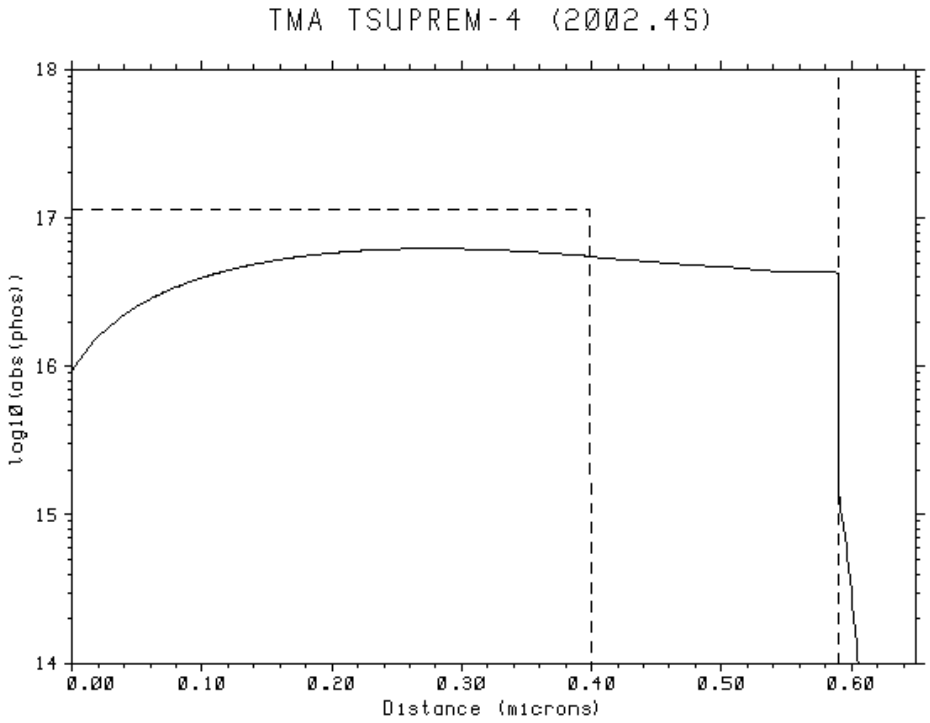

Figure 21: Phosphorous dopant profile before and after oxidation diffusion.

The phosphorous diffusion will overcompensate for the acceptors in the lightly doped

boron region just above the oxide, resulting in a completely n-type active area prior to ion implantation.

Diffusion modeling was used to simulate the dopant profiles of the gate and source/drain regions after the activation annealing, which was 10 seconds at 1100 ˚C. The final dopant profiles in the active area determine the series resistance of the device, as well as the extent of the depletion region under the gate. The calculated dopant profiles before and after rapid thermal annealing are shown in Figures Figure **22** and Figure 23. In each graph the original profile denoted by a dashed line, and the final profile is denoted by a solid line. For the gate implantation, the absolute value of the difference between the boron and background phosphorous concentration is plotted, showing the concentration of fixed donor and acceptor ions as a function of distance under the gate. The dip in the profile is the metallurgical junction, where the donor and acceptor concentrations are equal to one another. Boron diffuses rapidly in silicon, causing the junction to shift farther from the surface. This effect is seen for the profiles implanted at a dose of 10^{14} ions/cm^2 and 10^{15} ions/cm^2. The junction for the 10^{14} ions/cm^2 profile is 0.156 µm below the surface, while the junction for the more heavily doped 10^{15} ions/cm^2 profile is at 0.185 µm.

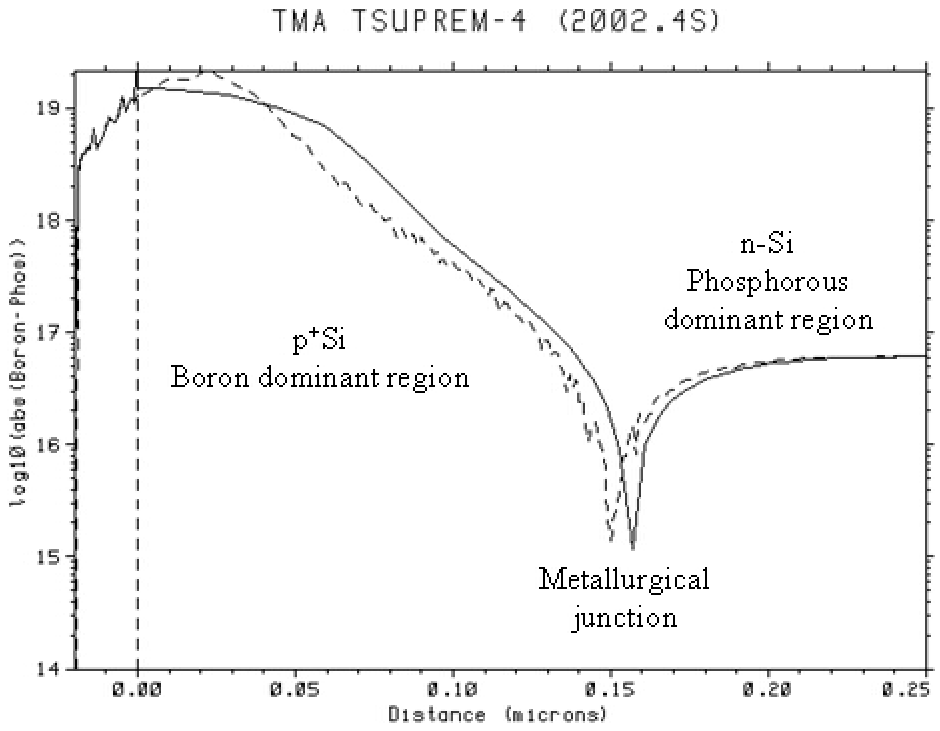

Figure 22: Boron profile for 10^{14} ion/cm^2 implantation before and after RTA.

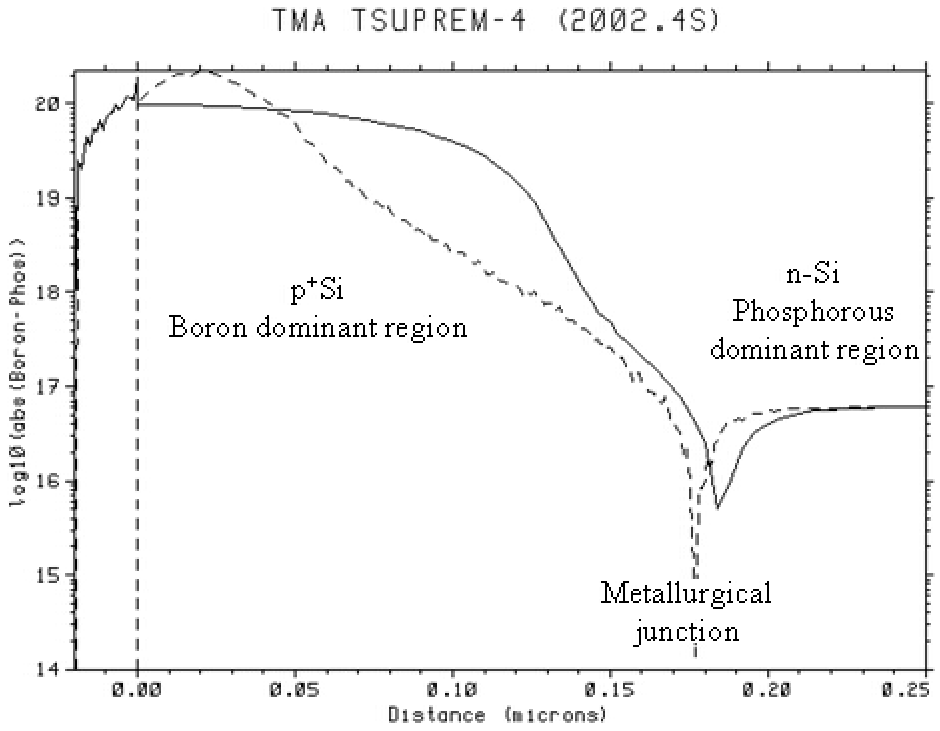

Figure 23: Boron profile for 10^{15} ion/cm^2 implantation before and after RTA.

The arsenic implantation profiles are shown in Figure 24, with the arsenic concentration added to the background phosphorous concentration to give the total donor ion concentration. Arsenic is a slow diffuser in silicon compared to born, so there is less change in the dopant profile after annealing. The most important aspect of the simulation results is the high concentration of donors near the surface of the silicon layer, which insures that the surface is strongly n^+ silicon. This is critical for assuring good ohmic contact between the active area and the metallization.

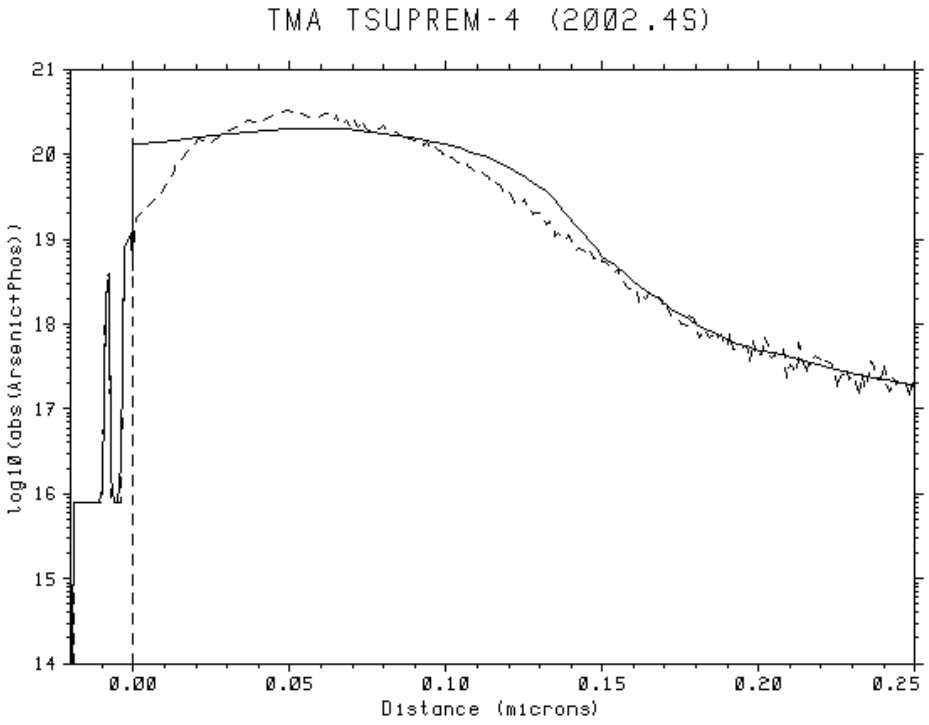

Figure 24: Arsenic profile for 1015 ion/cm2 implantation before and after RTA.

IV.3 METALLIZATION

The properties of the FIB-deposited platinum must be known to accurately predict the properties of the final device. The thin-film resistivity and contact resistance of the material determine the series resistance added to the device due to the contacts.

Characterization of the platinum / silicon interface at the surface of the material is especially important, as the device will not function if the metal-silicon junction forms a rectifying contact instead of an ohmic one.

Published values for the resistivity of FIB-deposited platinum vary over an order of magnitude from 70 to 700 μΩ·cm, highly dependent on beam current and deposition parameters such as background pressure and gas flow rate.[18,20] Therefore, the resistances have been measured empirically for the FIB-deposited platinum produced by the equipment used to make the contact pads. The resistivity of the deposited platinum was determined by a standard four-point probe measurement, which allows resistivity measurements without the resistance of the probe wires or contacts affecting the result. A four inch p-type silicon wafer with (100) orientation and 6000 Å of thermally grown SiO_2 on the surface was chosen for the substrate. Nominally 5000 Å of aluminum was electron-beam evaporated onto the surface, and patterned with optical lithography and wet aluminum etchant. The four-point measurement pattern consists of four contact pads and connecting spars arranged as shown in Figure 25.

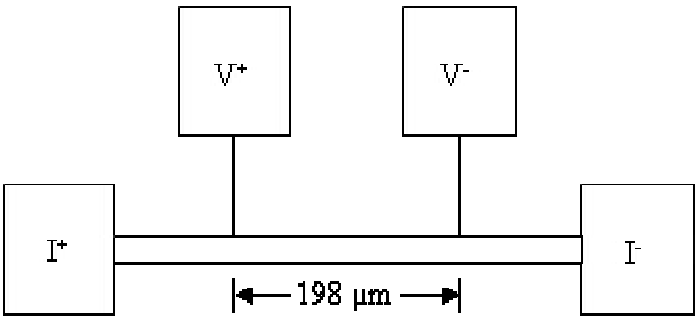

Figure 25: Four point resistance measurement pattern

In a four-point measurement, a set current is driven across the two end contacts. The two

top contacts are used to measure the voltage drop along a specific length of the main spar. With the voltage, current, and dimensions of the spar known, the metal resistivity can be calculated.

The aluminum line was L = 198 μm long, w = 7 μm wide and t = 0.57 μm thick, with a four point.resistance of R = 2.47 Ω. The thin-film resistivity of the evaporated aluminum is then $\rho = Rwt/L$, or 3.57 μΩ·cm. The platinum's resistivity was determined by milling away 30 μm of aluminum, replacing it with a strip of FIB-deposited platinum and then re-measuring the four-point resistance of the entire spar. The deposited platinum strip was 30 μm long and 5 μm wide, with a bit extra on each end to overlap the aluminum and ensure good electrical contact between the two materials. The height of the deposited platinum was 0.66 μm as measured by surface profilometer. The total modified spar resistance was 18.9 Ω, of which 2.1 Ω was due to the remaining 168 μm of aluminum. Assuming negligible contact resistance between the platinum and aluminum lengths, the resistance of the deposited platinum line is 16.8 Ω and the resistivity is therefore 185 μΩ·cm.

The contact resistance of the FIB deposited platinum to silicon was determined experimentally as well; these results have been presented at the 2001 EIPBN conference and published.[39] For most metals deposited onto silicon, the type of contact depends more on the semiconductor doping than the metal used, due to Fermi level pinning at the silicon surface. Conventionally deposited metal contacts to p, p^+, and n^+ doped silicon are generally ohmic, and contacts to n-type silicon tend to be rectifying.

The first step in this experiment was determining the nature of the contact

between the FIB deposited material and the silicon substrate. This was a fairly straightforward test, done by depositing metal contacts with known properties onto variously doped silicon wafers with <100> orientation, direct-writing FIB-metal contacts 150 μm away onto areas of bare silicon, and measuring the voltage drop as a function of current. The control metal was aluminum alloyed with 1% silicon by weight, which is known to provide a rectifying contact to n-type silicon, and a low-resistivity ohmic contact to silicon otherwise. The wafers used had the doping of 1.5×10^{15} cm^{-3} for the n-Si, 3.2×10^{16} cm^{-3} for the p-Si, and 1.7×10^{19} cm^{-3} for the p^+-Si. The n^+ wafer was made by using phosphorous-infused spin-on glass to dope a p-type wafer, and had a surface dopant concentration of roughly 10^{20} cm^{-3} after drive-in diffusion. The current-voltage (IV) curves between the aluminum and FIB contacts were measured before and after sintering, which was performed at 400 °C for 20 minutes, in an N_2 environment. The contacts to p-Si were conducting but not ohmic before and after sintering, while the contacts to n-Si were either rectifying or did not conduct at all. The p^+-Si contacts were found to be ohmic before and after sintering, while the n^+-Si contacts were nonconducting prior to sintering, but ohmic afterwards.

A more thorough investigation of contact resistance was performed for the n^+ and p^+ doped Si wafers, which are the only two cases directly applicable to the JFET design in this project. Such heavily doped regions make for very low resistance tunneling contacts, and as such are expected to be ohmic. The silicon wafers for this experiment were manually cleaved into chips 1 cm wide and 5 cm long. The chips were cleaned with piranha etchant for ten minutes, then given a 30 second dip in HF to remove all traces of

organic residue and oxide from the surface. A series of FIB-metal contact pads in either platinum or tungsten was then deposited on the chips in two lines parallel to their long dimension. Each pad was 75 μm long by 75 μm wide, nominally 0.5 μm thick, and 5 mm apart from the others of its type. After metal deposition, each chip was sintered for 20 minutes in an environment of H_2N_2 forming gas, at 400 °C. The slope of the IV curve between each platinum contact was measured, and plotted as a function of the distance between the contacts tested. These plots are shown in Figure 26.

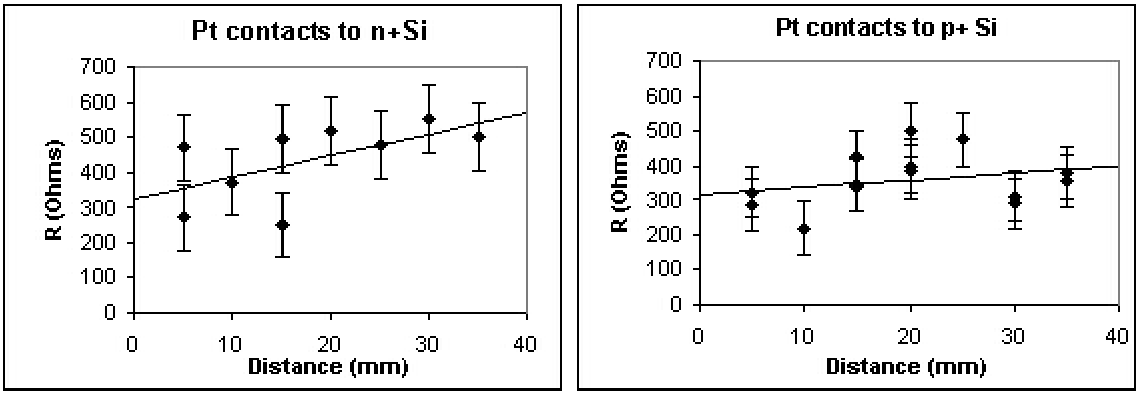

Figure 26: Total resistance of Pt contacts and Si along a silicon strip for n^+ and p^+ Si.

The total resistance between two FIB deposited contact pads R_T is the sum of the silicon resistance R_S and the resistance from the contacts to the silicon, R_C / A, the contact resistance divided by the area of the contacts. Since all the contact pads are deposited with the same area and under similar conditions, R_C and A can be assumed to be constant. R_S, by contrast, should to first order vary linearly with the distance between the contact pads, for distances that are large compared to the dimensions of the pads and comparable to the width of the chip. Therefore, a linear regression analysis was performed on the data, and the best-fit line determined. If it is assumed that R_S goes to zero as the distance

between the contact pads goes to zero, then the y-intercept of the best-fit line will correspond to R_C / A, which can be multiplied by A to yield simply R_C. The slope corresponds to R_S, which should only depend on the substrate and not the contacts used. The data is presented in Table 3.

Contacts	Error in y (Ω)	Slope (Ω / mm)	Y-intercept (Ω)	R_C ($x10^{-3}$ Ω cm^2)
Pt to n^+ Si	95.1	6.14 ± 3.16	326.1 ± 64.5	9.17 ± 1.82
Pt to p^+ Si	46.9	1.98 ± 1.30	320.8 ± 28.9	9.02 ± 1.32

Table 3: Measured contact resistance data for FIB-deposited Pt

There is a large variation in the resistance from point to point for all the data sets, suggesting that the contact resistance of any one deposited pad can vary substantially; the calculated error for each data point was as large as 95.1 Ω. Though the variation is large, there is an overall linear trend in the data for both data sets. This allows determination of R_C to within a calculated error. The calculated contact resistance in both cases is high, roughly 10^{-2} Ω·cm^2. This is two orders of magnitude higher than the contact resistance of for Al-Si alloy contacts to similarly doped silicon.[40] One possible explanation for the relatively high resistance of the platinum contacts is silicide formation: PtSi and Pt_2Si can form at 350 °C at a platinum-silicon junction.[41] Silicide formation could potentially impede the ohmic tunneling contact between the heavily doped silicon and the metal, and thus increase the contact resistance. Another factor is surface damage due to the gallium ion beam. The total dose required to deposit the Pt pads was $5.4 \cdot 10^{17}$ cm^{-2}, which is greater than the critical dose needed to amorphize the surface of the silicon. Even though the deposited material will act as a stop for the ion beam once it is formed, a significant

fraction of the total dose will impinge upon the surface silicon before contact formation. Therefore, the Pt contact deposition is quite likely to amorphize the silicon to a depth of several hundred angstroms, which corresponds to the projected range of the Ga^{+} beam.

Chapter V: DEVICE SIMULATION

V.1: ABRUPT-JUNCTION ANALYSIS

The general equations describing long-channel, abrupt-junction JFET operation have been presented in section II.3. The equations for drain-source current, conductance of the undepleted channel, the saturation current, and saturation voltage are repeated below.

$$I_{DS} = G_0\left(V_{DS} - \frac{2}{3}\left(\frac{2\varepsilon_s}{qN_d t^2}\right)^{\frac{1}{2}}\left[\left(\phi_i - V_G + V_{DS}\right)^{\frac{3}{2}} - \left(\phi_i - V_G\right)^{\frac{3}{2}}\right]\right)$$

$$G_0 = q\mu_n N_d t\frac{W}{L}$$

$$I_{DSat} = G_0\left[\frac{qN_d t^2}{6\varepsilon_s} - \left(\phi_i - V_G\right)\left(1 - \frac{2}{3}\left[\frac{2\varepsilon_s\left(\phi_i - V_G\right)}{qN_d t^2}\right]^{\frac{1}{2}}\right)\right]$$

$$V_{DSat} = \frac{qN_d t^2}{2\varepsilon_s} - \left(\phi_i - V_G\right).$$

These equations may be applied to FIB-fabricated JFETs by approximating the implanted *pn* interface under the gate as an abrupt junction with a heavily doped gate. This is reasonably valid when the applied voltage is large enough so that the depletion region extends well into the n-type channel. The approximation does not consider short-channel effects, nor is there a way to account for the variations in gate doping that are possible with FIB-JFETs. The abrupt junction approximation is therefore far from ideal for simulating all FIB-JFET effects, but can be used to gain a rough understanding of

expected transistor characteristics. Transistor IV curves are shown in Figures Figure 27 and Figure 28 for an abrupt-junction JFET with the channel dimensions of the fabricated devices. Gate acceptor concentrations of 10^{19} and 10^{20} ions/cm^3 respectively, to correspond to the 10^{14} and 10^{15} ion/cm^2 doping profiles previously modeled.

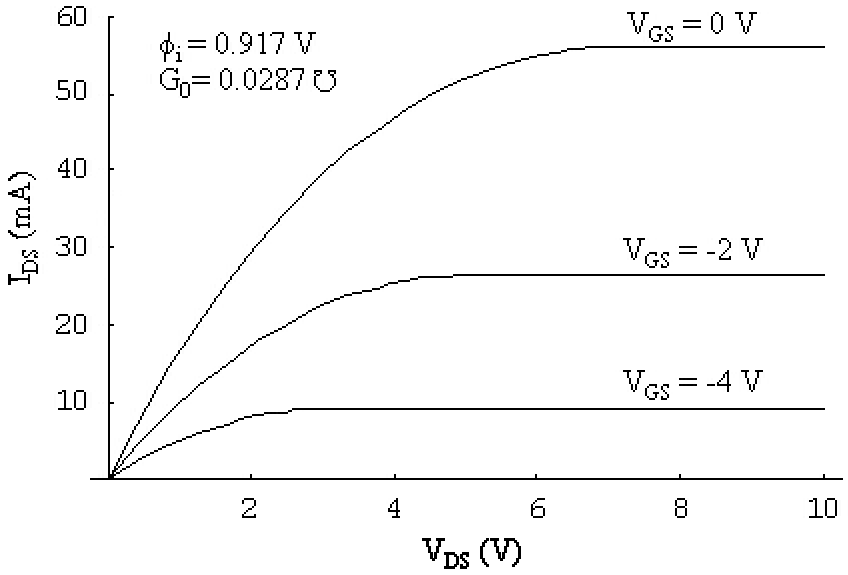

Figure 27: IV curves for an abrupt junction JFET with a gate doping of 10^{14} B^+ ions/cm^2.

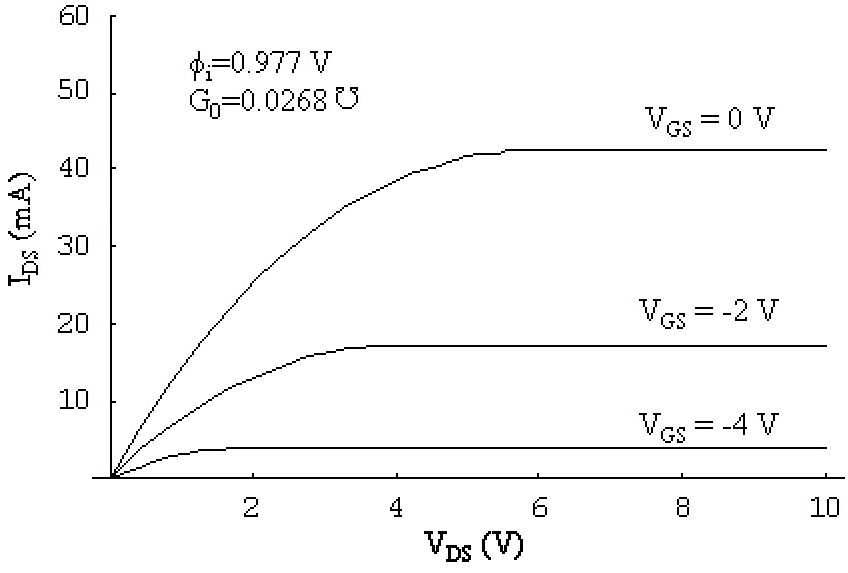

Figure 28: IV curves for an abrupt junction JFET with a gate doping of 10^{15} B^+ ions/cm^2.

V.2: NON-ABRUPT JUNCTION ANALYSIS

The abrupt approximation is a large departure from the actual doping profile in the depleted region. More complicated doping profile approximations are generally not completely solvable by analytic techniques, but can yield greater insight into device characteristics and performance. One such approximation is the linear junction, which may be appropriate for a investigating low-voltage performance assuming that the depletion region lies within the linear regime in the unbiased case.

The linear junction analysis uses the approximation $N_D - N_A = ax$, where the concentration gradient a is given in units of cm^{-4}. The total width of the depletion region is w. Due to the symmetry of the doping profile around the metallurgical junction, the depletion region will extend from $-w/2$ to $+w/2$. Within the depletion regions, then, the charge concentration is $\rho = qax$, and Poisson's equation in one dimension becomes

$$\frac{d^2\phi}{dx^2} = -\frac{qax}{\varepsilon_s}$$

This can be integrated to give the electric field $E(x)$, using the boundary condition that the field must go to zero at the edges of the depletion region.

$$E(x) = \frac{qa}{2\varepsilon_s}\left(x^2 - \frac{w^2}{4}\right)$$

A second integration yields the potential, where C is the constant of integration:

$$\phi(x) = -\frac{qa}{2\varepsilon_s}\left(\frac{x^3}{3} - \frac{w^2 x}{4}\right) + C$$

The built-in voltage across the depletion region is $\phi_i = \phi(w/2) - \phi(-w/2)$, or

$$\phi_i = \frac{qaw^3}{12\varepsilon_s}$$

This expression can be compared to the built in voltage derived from carrier concentration equations

$$n = n_i \exp\left(\frac{q\phi}{kT}\right), \text{ and } p = n_i \exp\left(-\frac{q\phi}{kT}\right)$$

These can be solved for the potentials at each end of the depletion region with the carrier concentration given by $p = -aw/2$ and $n = aw/2$ to yield:

$$\phi_i = \frac{2kT}{q}\ln\left(\frac{aw}{2n_i}\right)$$

These two expressions for the built in voltage can be equated to give an expression for the unbiased depletion region width w in terms of only known factors:

$$\frac{2kT}{q}\ln\left(\frac{aw}{2n_i}\right) = \frac{qaw^3}{12\varepsilon_s}$$

This must be solved numerically or graphically rather than analytically.

The values of a for the 10^{14} and 10^{15} ion/cm^2 dose B^+ gate implantations into the silicon active area are 2.59×10^{22} and 4.31×10^{22} cm^{-4}, respectively. This results in a depletion-region width of w equal to 0.136 μm for the 10^{14} ion/cm^2 implantation and 0.116 μm for the 10^{15} ion/cm^2 implantation. For both cases, the depletion region around the metallurgical junction is clearly nonlinear over the calculated extent of the depletion region, so the linear approximation is not valid for this analysis, even in the case of low applied voltage.

A more complicated approach, and the best fit to the implanted doping profile is

the exponential approximation, where $N_D - N_A = N_D - N_0 e^{-x/\lambda}$. This analysis is conducted in a similar fashion to the previous two, by integrating Poisson's equation to obtain the electric field and potential within the depletion region. Due to lack of symmetry around the metallurgical junction, a simple relationship between the boundaries of the depletion region in the p-type gate and n-type channel, x_p and x_n respectively, does not exist. Using the depletion and quasi-neutrality approximations, the electric field can be calculated as:

$$E(x) = \frac{q}{\varepsilon_s}\left[N_0 \lambda \left(e^{-\frac{x}{\lambda}} - e^{-\frac{x_n}{\lambda}} \right) + N_D \left(x - x_n \right) \right]$$

This expression can be integrated over the depletion region to give an expression for the built in voltage drop in terms of x_p and x_n:

$$\phi_i = -\frac{q e^{-\frac{x_n + x_p}{\lambda}}}{2\varepsilon_s}\left[-2e^{\frac{x_n}{\lambda}} \lambda^2 N_0 + e^{\frac{x_n + x_p}{\lambda}} N_D \left(x_n - x_p \right)^2 + 2e^{\frac{x_p}{\lambda}} \lambda N_0 \left(\lambda + x_n - x_p \right) \right]$$

A second expression for the voltage drop may be found from the carrier concentrations just outside the depletion region, which yields:

$$\phi_i = \frac{kT}{q}\left[Ln\left(\frac{N_D}{n_i} \right) + Ln\left(\frac{N_D}{n_i} e^{-\frac{x_p}{\lambda}} \right) \right]$$

These two equations may be solved for the built in voltage of the junction, given a third equation that relates x_p and x_n by charge conservation:

$$\int_{x_p}^{x_j} \left(N_D - N_0 e^{-\frac{x}{\lambda}} \right) dx + \int_{x_j}^{x_n} \left(N_D - N_0 e^{-\frac{x}{\lambda}} \right) dx = 0$$

The solution to these three equations must be found numerically. Once the unbiased junction parameters are known, a relationship can be calculated for the extent of the

depletion region as a function of the total voltage drop. The total voltage drop across the depletion region at any given point is a combination of the built in voltage, the voltage applied to the gate, and the voltage due to the drain-source current through the channel. By integrating the potential along the length of the channel, the drain-source current I_{DS} can be found as a function of the voltage applied to the gate, and the voltage applies to the drain.

Applying the exponential approximation to the implantation profiles previously calculated using Crystal-TRIM requires fitting the approximation parameters to the calculated data as closely as possible. For the 10^{14} ion/cm^2 case, $N_0 = 1.12 \times 10^{20}$ cm^{-3} and $\lambda = 2.06 \times 10^{-6}$ cm. For the 10^{15} ion/cm^2 case, $N_0 = 7.46 \times 10^{22}$ cm^{-3} and $\lambda = 1.32 \times 10^{-6}$ cm. The IV curves calculated using these values are shown in Figures Figure 29 and Figure 30.

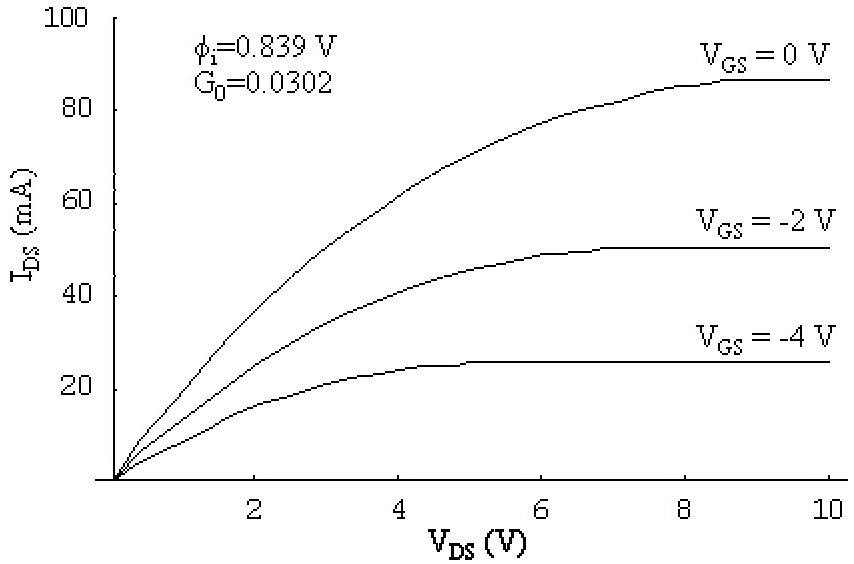

Figure 29: IV curves for an exponential JFET with a gate doping of 10^{14} B^+ ions/cm^2.

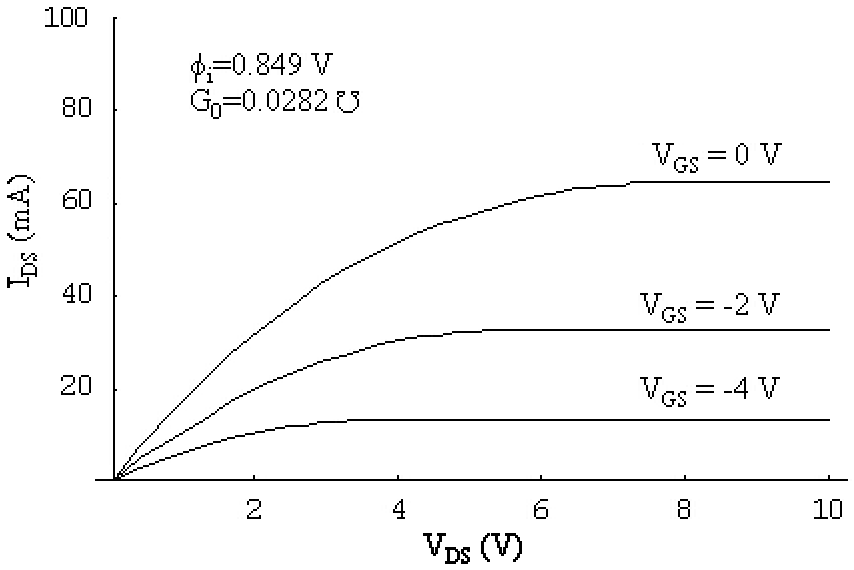

Figure 30: IV curves for an exponential JFET with a gate doping of 10^{15} B^+ ions/cm^2.

These IV characteristics are from the active area underneath the gate only, and may be compared to the similar IV curves previously calculated for the abrupt junction case. The exponentially-doped JFET has a higher saturation current and higher saturation voltage for similar bias conditions, as is shown in Figure X for 10^{14} B^+ ions/cm^2 and V_{GS} = 0 V.

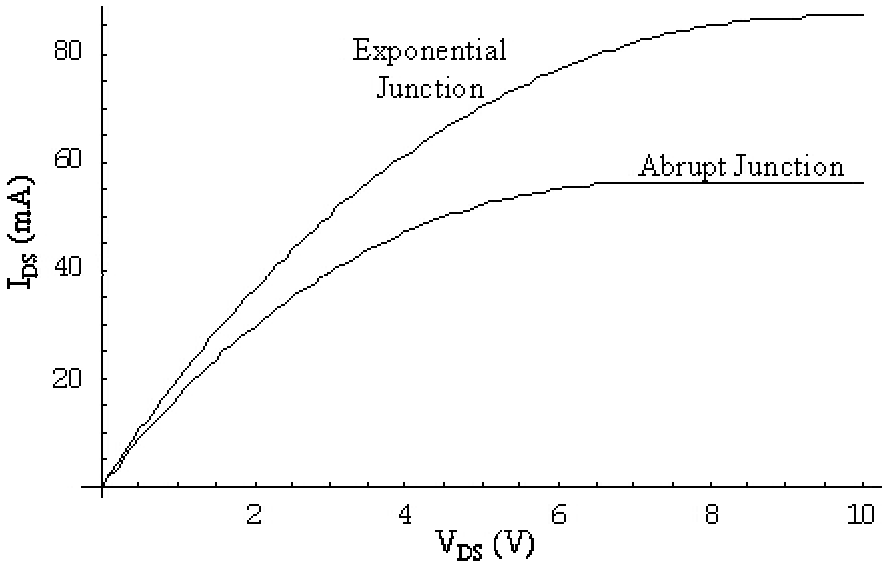

Figure 31: IV curve comparison for abrupt vs. exponential JFET approximations.

To fully model the FIB fabricated JFET, the effects of the source and drain regions as well as the contacts must be taken into account. The result of this will be a resistance in series with the channel, R_S, which lowers the effective voltage drop seen across the channel. If V_{DS} is the voltage applied between the source and drain, and V_A the voltage drop across the active area under the gate, then the current through the device I_{DS} will be given by the relationship:

$$V_{DS} = I_{DS}(V_A)R_S + V_A$$

Since the calculation I_{DS} given a value for V_A of requires a numerical solution, this more complex case does as well. Values of R_S that are large compared to the unbiased channel resistance will tend to dominate the characteristics of the device, causing most of the voltage drop to occur across the series resistance. This results in the device acting like a resistor, with very high voltages required before saturation is reached. Actual calculation of R_S is difficult, due to graded doping profiles near the source and drain, and the placement of the contact pads on the surface of the device. Assuming that the bulk of the non-channel device resistance comes from the undoped area around the gate spar where the resistivity is 0.125 Ω·cm, the device series resistance is approximately 1000 Ω. With a total contact area of 1000 μm^2, the contribution to the series resistance from the contacts will be another 1000 Ω, assuming an average contact resistance of 10^{-2} Ω·cm^2. Using these numbers, an approximate value for R_S is 2 kΩ. This is far larger than the unbiased linear-region channel resistance $R_{lin} = 1/G_0$ calculated for both gate doping doses considered above, which is roughly 40 Ω in both cases. To represent a working FIB-JFET, therefore, either a smaller channel must be assumed, or higher-order effects

must be taken into account when constructing the model.

V.3: PISCES DEVICE SIMULATION

The device calculations above rely on several approximations that are not generally valid: carrier concentrations decrease gradually within the depleted area around the junction instead of abruptly going to zero and Poisson's equation must be solved in two dimensions rather than simply one. Additionally, the electron mobility in the channel will vary as a function of both dopant concentration and electric field. The electric field dependence of electron mobility is critical, as drift velocity begins to saturate within an electric field of 10^4 V/cm for electrons in silicon at 300 K. This is known as the hot carrier effect, and is due to high energy phonon collisions with the silicon lattice as the electron drift velocity approaches the thermal velocity. It becomes important for short-channel junctions where the electric field along the channel can become very high in saturation, and so must be taken into account for FIB-JFETs.

To consider these higher order effects, a program called PISCES was used.[42] Given a specified semiconductor structure and applied bias condition, PISCES solves for the carrier concentrations, electric field, currents, and potential within the device. The simulator only works in two dimensions, but the FIB-JFET's large width and relative uniformity along the width makes this a valid approximation.

PISCES assumes that the distribution function is equal to some original distribution plus a perturbing factor, and solves six equations simultaneously to generate its results.[43] The first of these is the Poisson equation in two dimensions in terms of the electric potential Φ:

$$\nabla \cdot \left(-\varepsilon \nabla \Phi \right) = q\left(p - n + N_D^+ - N_A^- \right)$$

As with thermal modeling, carrier continuity must be taken into account. Where u is the net electron-hole recombination rate, this is described by:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \overrightarrow{J_n} - u \text{ and } \frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \overrightarrow{J_p} - u$$

Energy must be conserved as well. If w_n is the kinetic energy density of electrons, s_n is the electron energy flux, $\boldsymbol{E}_n$ the field acting on the electrons (which may be different for from the field acting upon holes), and u_{wn} is the net loss rate term for both recombination and phonon scattering, then the electron energy conservation equation is:

$$\frac{\partial w_n}{\partial t} = -\nabla \cdot \overrightarrow{s_n} + \overrightarrow{j_n} \cdot \overrightarrow{E_n} - u_{wn}$$

Similarly, for holes this becomes:

$$\frac{\partial w_p}{\partial t} = -\nabla \cdot \overrightarrow{s_p} + \overrightarrow{j_p} \cdot \overrightarrow{E_p} - u_{wp}$$

Finally, the thermal diffusion equation for the semiconductor lattice is used. In this expression, the subscripts L, n, and p refer to the lattice, electrons and holes respectively, and apply to the temperature T, the specific heat c, and the thermal conductivity κ. The energy relaxation times for electrons and holes are τ_{wn} and τ_{wn}, respectively, u_{SRH} is the rate of Shockly-Read-Hall recombination, and E_g is the band-gap energy of the semiconductor. Given these terms, the equation for thermal diffusion is:

$$c_L \frac{\partial T_L}{\partial t} = \nabla \cdot \left(\kappa_L \nabla T_L \right) + u_{SRH} \left[\frac{3}{2} kT_n + E_g\left(T_L\right) + \frac{3}{2} kT_p \right] + \frac{w_n\left(T_n\right) - w_n\left(T_L\right)}{\tau_{wn}} + \frac{w_p\left(T_p\right) - w_p\left(T_L\right)}{\tau_{wp}}$$

The simplest use of PISCES in the context of this work is to simulate the active area under the gate of JFETs made with both doping profiles discussed previously: the

cases of uniform 10^{14} ion/cm^2 and 10^{15} ion/cm^2 boron doping. This allows comparison with the previously considered abrupt and exponential junction calculations. The results are shown in Figures Figure 32 and Figure 33; the input file used to generate the results is given in Appendix A.I.

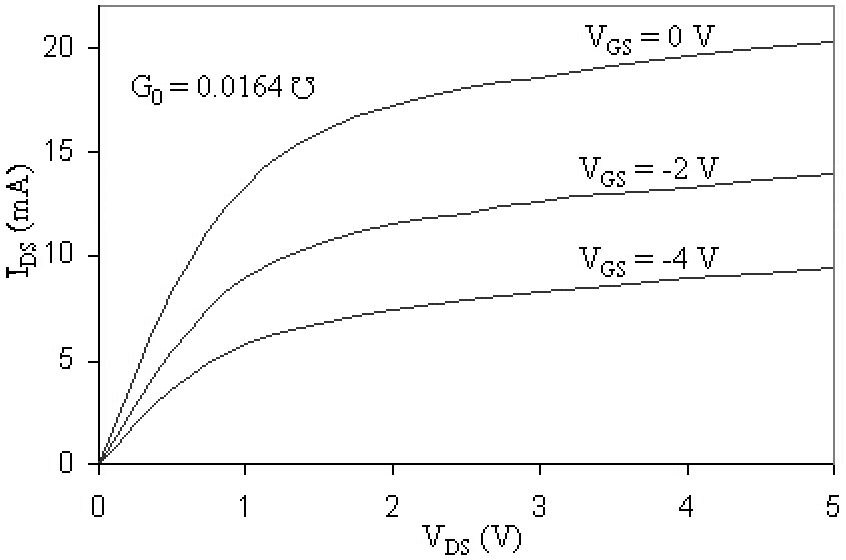

Figure 32: Simulated IV curves, JFET channel with a gate doping of 10^{14} B^+ ions/cm^2.

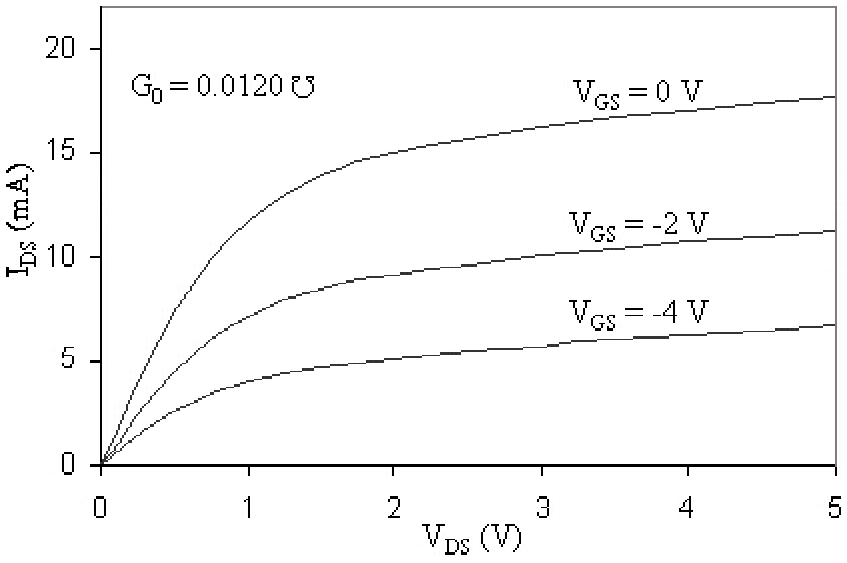

Figure 33: Simulated IV curves, JFET channel with a gate doping of 10^{15} B^+ ions/cm^2.

The most important aspect of the PISCES simulation is that it predicts increasing I_{DS} after saturation is reached, due to short-channel effects. Additionally, the series resistance of the contacts and the device beyond the channel region can be accounted for. PISCES simulations of a device with the dimensions and source/drain doping of the FIB-JFET, but without gate doping or contact resistance, calculated a total resistance of 980 Ω between source and drain. This is close to the previous estimate of 1000 Ω for the device series resistance. This figure can be added to the estimated contact resistance of the FIB-deposited platinum to the source and drain, then halved to yield an estimated 990 Ω of total series resistance per side of the device. The results of including this resistance are shown in Figure 34 for the case of a JFET with average FIB-platinum contacts and uniform gate doped implanted with a dose of 10^{14} B^+ ions/cm^2.

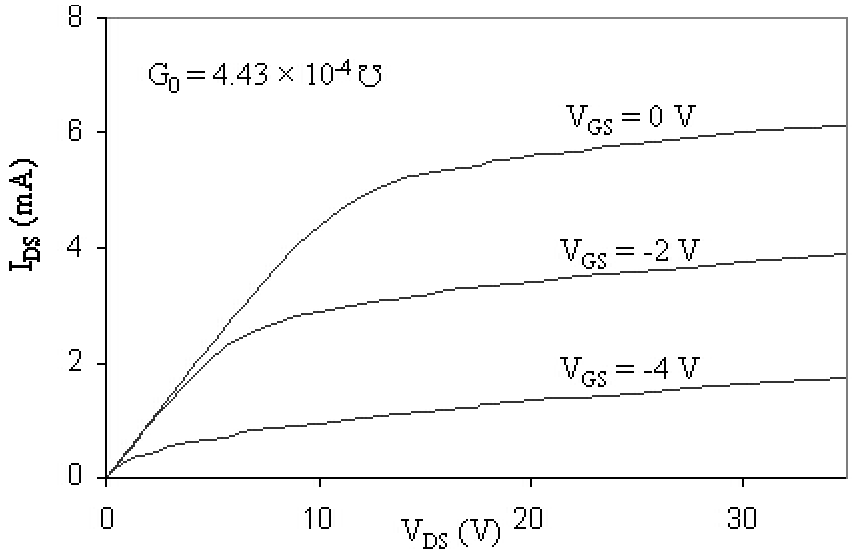

Figure 34: Simulated IV curves, JFET with 10^{14} cm^{-2} gate doping and Pt contacts.

The unbiased channel conductance G_0 corresponds to a linear region resistance R_{lin} of 2.26 kΩ. This is only slightly larger than the total series resistance, and so dominates the low-voltage characteristics of the device. The series resistance also causes a smaller voltage drop across the channel for a given V_{DS}, reducing the effective saturation current and increasing the pinch-off voltage of the device. All of these effects can be expected in the actual FIB-JFET. The above simulation represents the best device modeling that was possible given the information and tools at hand, and serves as a useful reference point for the expected characteristics of the device.

Chapter VI: RESULTS AND DISCUSSION

VI.1: FIB-JFET DEVICE CHARACTERISTICS

Seventeen JFETs were created according to the procedure given in Chapter III and their characteristics analyzed; due to time and equipment constraints only a limited number of devices could be made. All devices were constructed concurrently on the same SOI chip, and therefore subjected to identical process conditions. Similarly, the ion implantation for all devices was done in the same processing run. This served to minimize dissimilarity due to process variation, and allow device comparison based on differences in gate doping profiles. The final step in the fabrication process, contacting the active areas to large metal pads for testing, was done separately.

JFETs with four gate doping profiles were investigated in this work. Six of the seventeen were constructed with a uniform gate doping to act as control devices. Half of these uniformly-doped JFETs were implanted with 10^{14} ions/cm^2 over the gate region and half with 10^{15} ions/cm^2, both cases at the standard implantation energy of 10 keV and a gate length of 1 µm. The other devices were made with one of two gate dopings that varied along the length of the channel, to investigate the potential of non-uniform devices for enhanced transistor properties. The first of these was a step gate, where half of the one-micrometer gate was implanted with 10^{14} ions/cm^2 of boron, while the other hand was implanted to 10^{15} ions/cm^2. The second was a more linearly-graded gate, varying from with 10^{14} to 10^{15} ions/cm^2 along the length. The implantation was done in steps of 0.1 micrometers, but SUPREM thermal simulations indicate that the doping profile is

relatively linear after the annealing process. For devices with non-uniform gates, the more heavily doped regions were implanted closer to the designated drain, and the more lightly doped regions closer to the source. For uniform gate devices, the distinction between source and drain is a matter of convention only.

The first four devices were fabricated according to the procedure given in Chapter III, one with each of the four doping profiles described above. Device metallization was done using FIB-induced deposited of platinum as previously discussed, and as shown in **Figure 7**. The remaining thirteen JFETs were fabricated with evaporated or sputtered aluminum contacts instead of platinum in order to speed the fabrication process and provide more reliable contact to the active areas. The JFETs with platinum contacts were made as proof-of-principle devices to show the potential of fully FIB-fabricated devices. The aluminum contact devices were made to assist in studying the effects of nonuniform gate doping by reducing the variability of the device's contacts.

The measured current-voltage (IV) characteristics of all seventeen devices are summarized in Table 4 and shown in Appendix A.2. All devices save for the first two were measured with channel voltage applied to the drain and the source grounded, then again with voltage applied to the source and the drain grounded. Negative gate voltage was applied between the gate and source when channel voltage was applied to the drain, and vice versa. Table 5 summarizes the differences in the devices in each devices under different the two voltage configurations. Source-drain configuration data was not measured for the first two devices due to an oversight at the time.

Device	Doping (ion/cm^2)	Contact	R_{sat} (kΩ)	$R_{Lin\ 0\ DS}$ (Ω)	I_{Dsat} (μA)	V_T (V)
1	10^{14}	FIB Pt	1480	8725	140	-1.3
2	10^{15}	FIB Pt	780	2439	1140	-4.4
3	$10^{14}/10^{15}$ (Step)	FIB Pt	5730	5654	120	-1.3
4	10^{14} to 10^{15} (Linear)	FIB Pt	62	17462	-	-6.2
5	10^{14}	Al/Si	2250	3500	170	-1.1
6	10^{15}	Al/Si	469800	44800	3.1	-0.66
7	$10^{14}/10^{15}$ (Step)	Al/Si	120000	11100	15	-0.65
8	10^{14} to 10^{15} (Linear)	Al/Si	21870	5720	38	-0.7
9	10^{14}	Al/Si	68	2116	2300	-8.4
10	10^{15}	Al/Si	145	3278	1250	-4.8
11	10^{14} to 10^{15} (Linear)	Al/Si	130	2808	1500	-6.3
12	10^{14}	Al/Si	69	2908	1900	-6.9
13	10^{15}	Al/Si	84.0	4317	1200	-4.9
14	$10^{14}/10^{15}$ (Step)	Al/Si	84.3	2609	1550	-4.7
15	10^{14} to 10^{15} (Linear)	Al/Si	126.3	3434	1350	-5.4
16	$10^{14}/10^{15}$ (Step)	Al/Si	138.5	2446	1850	-5.2
17	10^{14} to 10^{15} (Linear)	Al/Si	132.0	2685	1480	-4.8

Table 4: Current-voltage characteristics for FIB-JFETs.

Device	R_{sat} DS (kΩ)	R_{sat} SD (kΩ)	R_{Lin} DS (Ω)	R_{Lin} SD (Ω)	I_{Dsat} (μA)	I_{Ssat} (μA)
1	1480		8725		140	
2	780		2439		1140	
3	5730	12280	5654	5589	120	130
4	62	23.0	17462	16798	-	-
5	2250	2600	3500	3500	170	230
6	469800	1000000	44800	43100	3.1	3.3
7	120000	1190000	11100	10600	15	20
8	21870	310.0	5720	5600	38	45
9	68	104.7	2116	2735	2300	1900
10	145	73.9	3278	3673	1250	1250
11	130	118.6	2808	3350	1500	1400
12	69	74.3	2908	2324	1900	2200
13	84.0	121.0	4317	5745	1200	700
14	84.3	236.0	2609	4163	1550	960
15	126.3	122.2	3434	3514	1350	1400
16	138.5	125.9	2446	2011	1850	2100
17	132.0	141.7	2685	2823	1480	1400

Table 5: FIB-JFET current-voltage characteristic comparison.

Two of the FIB-JFETs were adversely affected by short-circuiting between terminals, either within the device or due to conduction along the surface. JFET 4, shown in Figure 40 and Figure 41, had a conducting path between the drain and source terminals apart from the normal conducting channel. This accounts for the large increase in drain-source current after pinch-off and under high negative gate-source voltages, and is why no saturation current could be measured. JFET 8, shown in Figure 48 and Figure 49,

similarly had a conducting path between the gate and source terminals. Measurements between the gate and the source in reverse-bias yielded a resistance of 1.36 MΩ.

Device 3, with a gate uniformly doped with 10^{15} ion/cm^2 boron, had the best IV characteristics of all the devices with FIB-Pt contacts. It had close to the expected characteristics of a FIB-JFET as modeled by PISCES, though the saturation current is lower than expected and short-channel effects not as pronounced, suggesting that the channel is thinner than process modeling suggests. The other Pt-contacted FIB-JFETs exhibited R_{lin} values up to 20 kΩ higher, and lower V_T values of approximately -1 V. These two terms were expected to be much the same for all devices with similar contacts given the relatively small variation in junction depth. This suggests either that there was significant variation in the resistivity of the FIB-Pt contacts, or that the FIB ion implantation was deeper than expected.

The JFETs with FIB implantation and Al/Si contacts deposited by sputtering show much greater linear region uniformity, with an average value of 2950 ± 650 V for R_{lin} and -6 ± 1 V for V_T. This implies that the variation in previous devices was primarily due to inconsistencies in metallization resistivity rather than FIB implantation. A minor trend towards improved saturation region characteristics due to nonlinear gate doping can be seen in this device set as well, by looking at the effective resistance of the channel after pinchoff. In an ideal long-channel device, this value R_{sat} should be zero. In practice, electron velocity saturation due to high electric fields causes a steady increase in I_{Dsat}, resulting in an effective saturation resistance $R_{sat.}$ The average R_{sat} for uniformly gate doped JFETs with sputter-deposited Al/Si contacts was 92.3 ± 28.1 kΩ. This figure

was higher for variably gate doped devices when channel voltage was applied to the source, closer to the more lightly doped region of the gate, and the drain was grounded. The average R_{sat} for variably doped JFETs under these conditions was 181 ± 78 kΩ for devices with step gates, and 149 ± 50 kΩ for devices with linearly doped gates.

VI.2 PISCES DEVICE ANALYSIS

The data from lightly and heavily doped uniform-gate Al/Si contact FIB-JFETs was used in an attempt to construct a less complex, but more accurate model. These devices were examined in particular because they offer the simplest case of JFETs with uniform gate implantation and consistent contact resistance. This was attempted by varying the JFET models described in Chapter V to fit the measured data. The primary device characteristics examined for this were the average values for R_{sat}, R_{lin}, I_{Dsat}, and V_T. The average values for these are given below in Table 6.

Device characteristics	R_{sat} (kΩ)	R_{Lin} (Ω)	I_{Dsat} (μA)	V_T (V)
Lightly-doped (10^{14} ion/cm^2)	78.9	2520	2100	-7.65
Heavily-doped (10^{15} ion/cm^2)	105.7	4250	1225	-4.85

Table 6: Average FIB-JFET characteristics for uniform gate Al/Si contact devices.

Abrupt junction JFET theory proved unable to provide a reasonable fit to these data points for the lightly and heavily doped case together. The junction depths, channel resistivity, and the total series resistance due to contacts and geometry were varied within reasonable limits to fit the data in Table 6. This did not produce satisfactory results, as

any combination of parameters that produced the proper values for linear-region resistance resulted in saturation currents and pinch-off voltages that were far too low. A similar attempt with PISCES using the implantation profiles generated by Crystal-TRIM produced better results, with reasonably accurate modeling of R_{lin} and I_{Dsat}. This model assumed the previously calculated implantation and channel doping profiles to be accurate, but that the thickness of the silicon mesa was effectively 0.4 μm rather than its measured dimension of 0.59 μm. Additionally, the fitted series resistance due to device geometry and contact resistance was higher than expected, 2260 Ω rather than 1000 Ω. While PISCES did not produce a perfect model of the FIB-JFET, it does offer some potential insight into how the final device differs from the initial theory. The reduced effective channel thickness is a logical result, given that only the top 4000 Å of the original SOI chip was high-quality, epitaxially deposited silicon. It is reasonable to assume that the 1900 Å bottom layer, formed by re-annealing after high-energy oxygen implantation to form the buried oxide, has greatly reduced electron mobility compared to the epitaxial layer.

The PISCES device model offers a possible explanation for the improved saturation region characteristics of graded-gate devices. Simulation of the electric field along the conducting channel of a step-graded device shows that the field is spread more evenly along the channel when compared to a device with uniform gate doping, rather than having as sharp a peak near the drain. This results in a 40% reduction in the maximum electric field along the channel, and therefore less electron velocity saturation. This is shown in Figure 35.

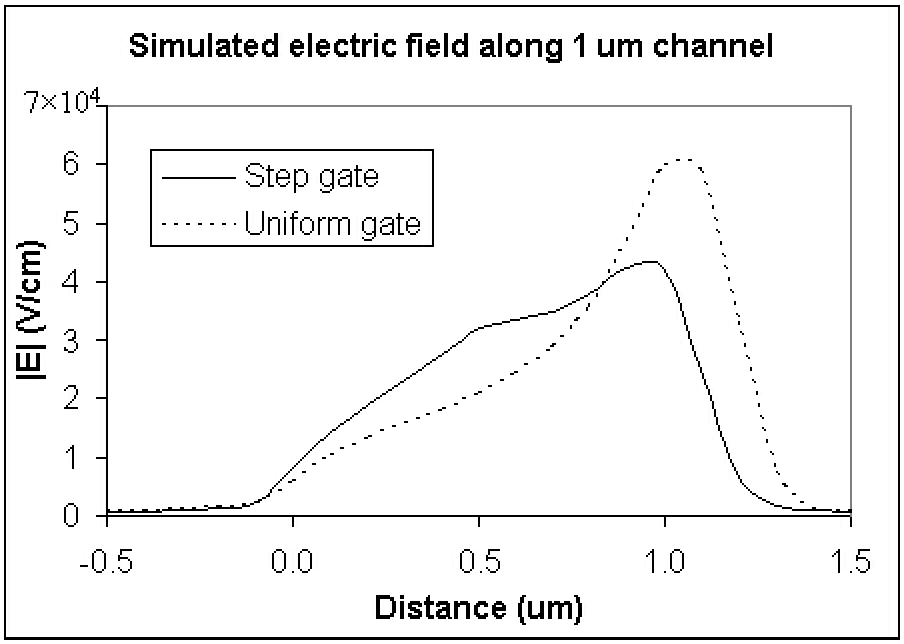

Figure 35: Simulated channel electric field for graded vs. uniform gate FIB-JFET.

Chapter VII: CONCLUSIONS

VII.1 SUMMARY OF WORK

This work investigated the feasibility of creating junction field effect transistors using focused ion beams. The usefulness of such devices and the history of microcircuit modification via focused ion beams was discussed in brief. The theory of basic abrupt-junction JFETs was reviewed, as were the calculations needed to adjust the basic theory to better describe an ion-implanted junction. A detailed fabrication process was presented, and the intricacies of focused ion beam gate implantation and contact metallization were examined in detail. Finally, a number of viable FIB-JFETs were created, analyzed, and compared to device simulations produced by PISCES.

In conclusion, focused ion beam techniques can be used to produce field effect transistors without traditional lithographic processing. This has great potential for device creation on non-planar surfaces, the creation of novel devices requiring graded doping profiles, and rapid prototyping. FIB-created junction field effect transistors were designed, modeled, and fabricated on an SOI chip as proof-of-concept devices. Platinum deposited through ion-induced deposition was found to be a viable material for device contacts, though the resistivity and contact resistance are significantly higher than conventional aluminum contacts. FIB-JFETs with graded gate doping profiles were shown to have improved characteristics in the saturation region due to short-channel effects, possibly due to a lowering of the peak electric field in the device channel. A step graded gate, with the half of the gate nearer the device source doped more heavily than

the half nearer to the drain, proved effective at reducing the increase of drain-source current past device pinch-off.

VII.2 FUTURE WORK

FIB techniques show great potential for nonplanar, maskless device fabrication. To develop these techniques fully, more work needs to be done. The ion-induced platinum deposition process is highly dependent on the parameters of both the ion beam and the precursor gas. The deposition system used in this project offered little precursor gas control; future work will ideally use a system with the ability to measure and control both gas flow parameters and substrate temperature. This will allow precise control over the composition, and therefore the electrical characteristics, of the deposited platinum compound. Another possible method to improve the metallization is to investigate the potential of other materials. Ion-induced tungsten deposition is a viable alternative FIB metallization, with lower, more stable contact resistance to heavily doped silicon.[39]

Another area for future work is experimental determination of the gate implantation profile before and after annealing, which was not possible within the scope of this project. In the present work, this was accomplished by simulating ion transport and diffusion during the implantation and diffusion processes, respectively. Ideally, the implantation profile could be measured directly as a function of dopant concentration versus depth through a technique such as secondary-ion mass spectroscopy (SIMS). Exact information on the doping profile would enable a much better understanding of the gate junction characteristics, and therefore the characteristics of the FIB-JFET as a whole.

APPENDICES

A.I: Input files for Crystal-TRIM, SUPREM, and PISCES

Crystal-TRIM sample input parameters for boron into silicon

Profile: 1D
Energy: 10 keV
Orientation: 1 0 0
Tilt Theta0: 0
Rotation Phi0: 0
Beam divergence: 0.2865º
ZBL stopping file: scoef2.dat
Atomic ion: yes
Atomic number: 5
Most abundant isotope: yes
C_λ: standard
Cel_{100}: 1
Cel: 1.32
Projectile histories: 5000
Bruno-Schmidt splitting: yes
Default splitting: yes
ISIGDEPTH: 10
Overlayers: yes
    Thickness: 200 Å
    Density: 2.19 g/cm^2
    SiO_2: yes
Si at room temperature: yes
Damage accumulation: yes
    Model: 6
    c_{acc}: 0.1
    c_{crit}: 0.5
Dose: 10^{14} ions/cm^2
Predamage: no
Depth interval width: 10 Å
Final energy: 0.01 keV

Crystal-TRIM sample input parameters for arsenic into silicon

Profile: 1D
Energy: 120 keV
Orientation: 1 0 0
Tilt Theta0: 0
Rotation Phi0: 0
Beam divergence: 0.2865º
ZBL stopping file: scoef2.dat
Atomic ion: yes
Atomic number: 33
Most abundant isotope: yes
C_λ: standard
Cel_{100}: 1
Cel: 1.39
Projectile histories: 5000
Bruno-Schmidt splitting: yes
Default splitting: yes
ISIGDEPTH: 10
Overlayers: yes
    Thickness: 200 Å
    Density: 2.19 g/cm^2
    SiO_2: yes
Si at room temperature: yes
Damage accumulation: yes
    Model: 6
    c_{acc}: 0.3
    c_{crit}: 0.5
Dose: 2×10^{15} ions/cm^2
Predamage: no
Depth interval width: 10 Å
Final energy: 0.121 keV

SUPREM input file for thermal diffusion calculation of annealing process

```
$ Definition of the vertical mesh, ie, depth into the substrate
line y loc = 0.40 spacing=0.001 tag=surf
line y loc = 0.59     spacing = 0.001 tag=interface
line y loc = 0.96   spacing = 0.001 tag=back

$ Definition of the horizontal mesh – only one dimension considered
line x loc=-0.2 spacing=0.1 tag=right
line x loc=0.2 spacing=0.1 tag=left

$ Set up SOI wafer – silicon over silicon dioxide
region silicon xlo=right xhi=left ylo=surf yhi=interface
region oxide xlo=right xhi=left ylo=interface yhi=back


$ Set up the exposed surface – top of substrate only
bound exposed  xlo=right  xhi=left ylo=surf yhi=surf

$ Calculate the initial mesh with 9e14 ion/cm^2 boron concentration
init <100> boron=9e14

$ Deposit the epitaxial silicon layer with higher phosphorous doping
deposit silicon thickness=0.4 spaces=400 phosphorous=1.13e17

$ Plot the original phosphorous profile
select z=log10(abs(phos))
plot.1d x.val=0 bottom=14 top=18 right=0.65 line.typ=3

$ Oxidation process: 15 minutes at 1125 C
diffuse time=15 temp=1125

select z=log10(abs(phos))
plot.1d x.val=0 cle=f axi=f line.typ=1

select z=phos
print.1d x.val=0

$ Deposit 200A silicon dioxide
deposit oxide thickness=0.02 spaces=20

$ Define boron profile in y, from Crystal-TRIM data
profile boron in.file=B_10kV_1e15_SiOx2.txt
```

```
$ Rapid Thermal Annealing diffusion: 10 seconds at 1100 C
diffuse time=.1666667 temp=1100

$ Plot the final profile
select z=log10(abs(ars+phos))
plot.1d  cle=f axi=f line.typ=1

$ Print final boron profile for use in PISCES
select z=bor
print.1d
```

PISCES input file for simulation of device characteristics

mesh rectangular nx=21 ny=20

$ JFET7b, only active area under gate considered. 83.0 um by 87.2 um.
$ X direction here is parallel to length of transistor.
$ Implant line centered at 0.5 um in x.

$ Set up the x-direction mesh, out to 83 um.
x.m node=1 loc=0
x.m node=21 loc=83

$ Set up the y-direction mesh.
y.m node=1 loc=0 ratio=1
y.m node=16 loc=0.59 ratio=1
y.m node=20 loc=0.80

$ Define regions; from 0 to 0.59 um deep is silicon; below that is the buried oxide.
region number=1 ix.low=1 ix.high=21 iy.low=1 iy.high=16 silicon
region number=2 ix.low=1 ix.high=21 iy.low=16 iy.high=20 sio2

$ Electrodes: Source=1, Drain=2, Gate=3
electrode n=1 ix.low=1   ix.high=7   iy.low=1 iy.high=1
electrode n=2 ix.low=15 ix.high=21 iy.low=1 iy.high=1
$electrode n=3 ix.low=32 ix.high=40 iy.low=1 iy.high=1

$ Background phosphorous doping from Crystal-TRIM and SUPREM
doping ascii x.left=0 x.right=83.0 inf=Prof_P.txt

$ Source and drain doping, arsenic input file from Crystal-TRIM and SUPREM
doping ascii x.left=0 x.right=27 inf=Prof_As2.txt
doping ascii x.left=56 x.right=83 inf=Prof_As2.txt

$ Uniform 1e14 doping, boron input file from Crystal-TRIM and SUPREM
doping ascii x.left=1 x.right=2 inf=Prof_B14.txt

$ Uniform 1e15 doping, boron input file from Crystal-TRIM and SUPREM
$doping ascii x.left=1 x.right=2 inf=Prof_B15.txt

contact all alum

$ Initial solution with no carriers present
symbolic newton carrier=0
method itlim=50 trap
model srh fldmob conmob

```
solve init

$ Set up full Newton solutions with both electrons and holes, set tolerances.
symbolic newton carrier=2
method p.tol=1e-10 c.tol=1e-10 itlim=10000 trap

$ Use Shockley-Reed-Hall recombination, include field-dependence of mobility,
$  include dopant concentration dependence of mobility.
model srh fldmob conmob

solve prev v1=0 v2=1 v3=0 elec=3 vstep=1 nsteps=9

print points ix.low=1 ix.high=71 iy.low=25 iy.high=25
print solution ix.low=1 ix.high=100 iy.low=1 iy.high=30
```

A.II: FIB-JFET current-voltage characteristics

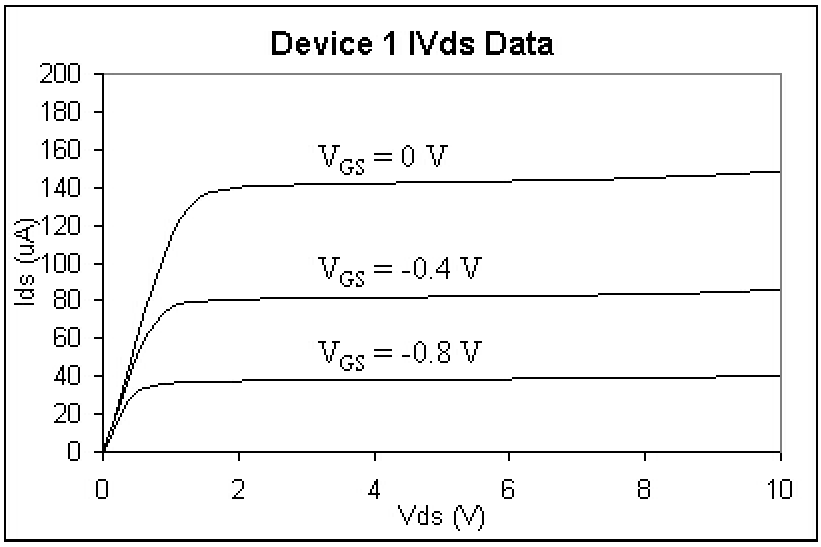

Figure 36: Drain-source IV curves for JFET 1, uniform lightly doped gate with Pt contacts.

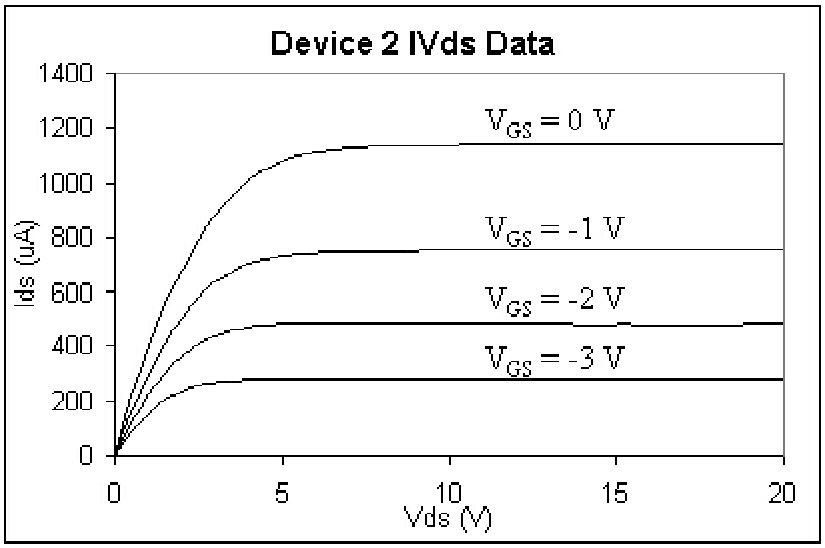

Figure 37: Drain-source IV curves for JFET2, uniform heavily doped gate with Pt contacts.

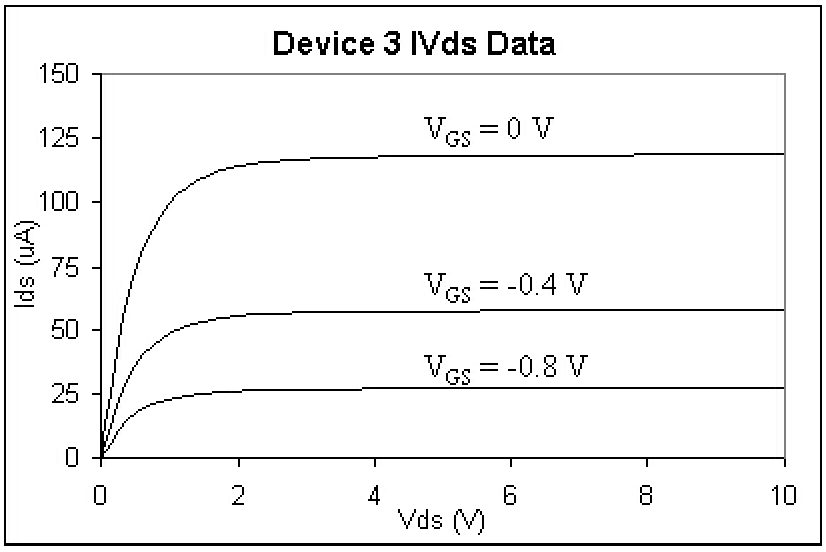

Figure 38: Drain-source IV curves for JFET 3, step doped gate with Pt contacts.

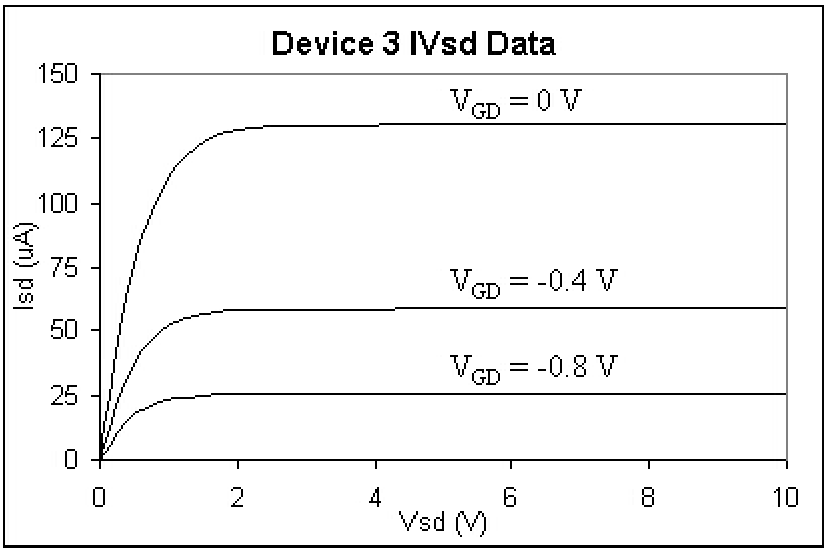

Figure 39: Source-drain IV curves for JFET 3, step doped gate with Pt contacts.

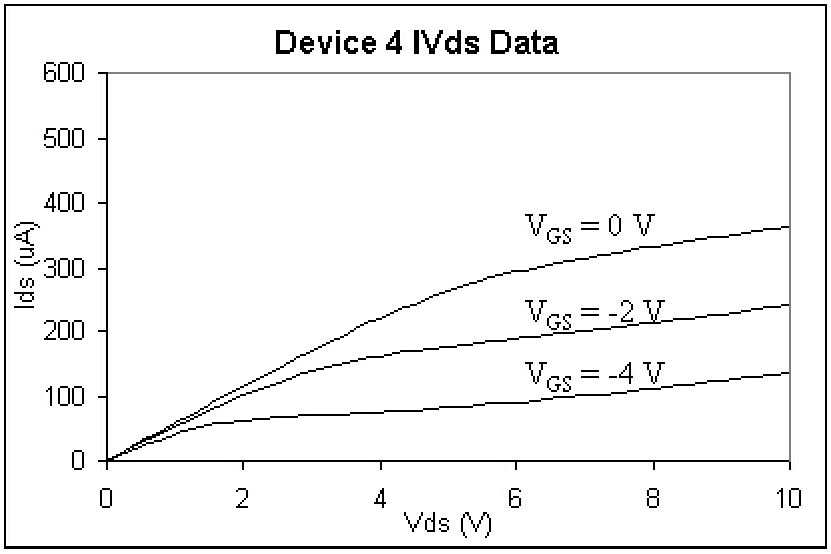

Figure 40: Drain-source IV curves for JFET 4, linearly doped gate with Pt contacts.

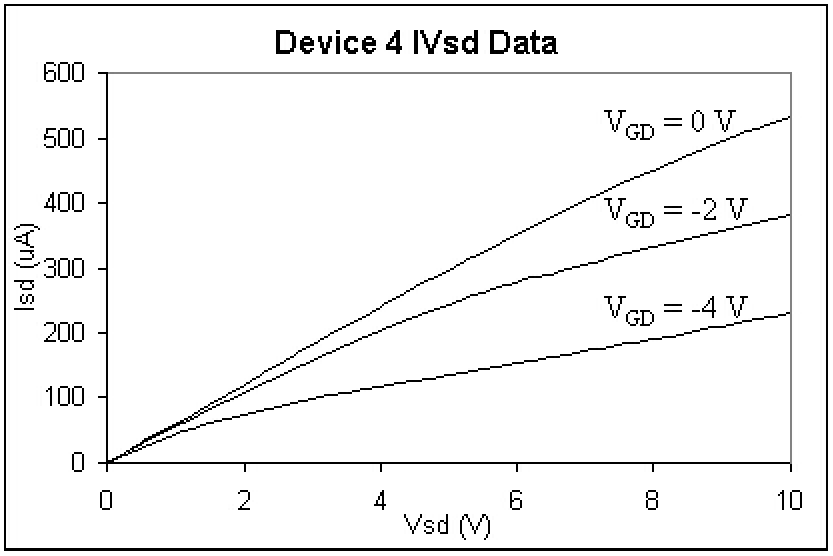

Figure 41: Source-drain IV curves for JFET 4, linearly doped gate with Pt contacts.

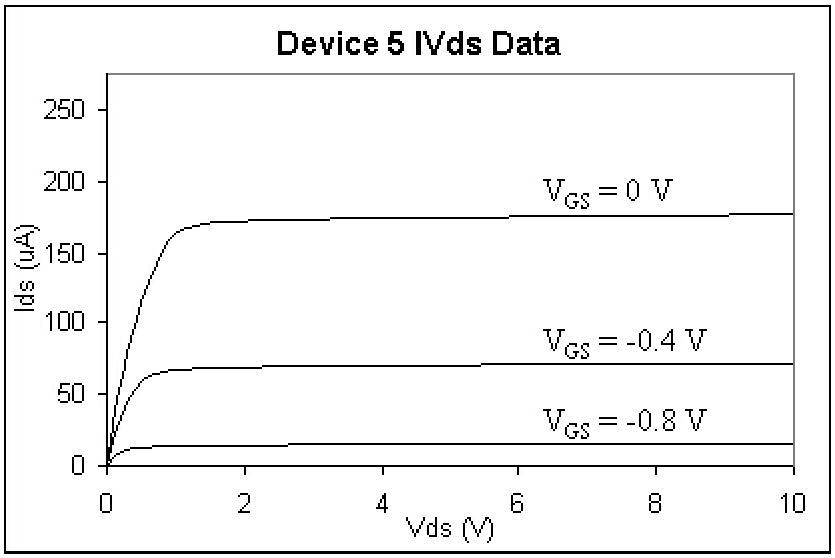

Figure 42: Drain-source IV curves for JFET 5, uniform lightly doped gate with Al contacts.

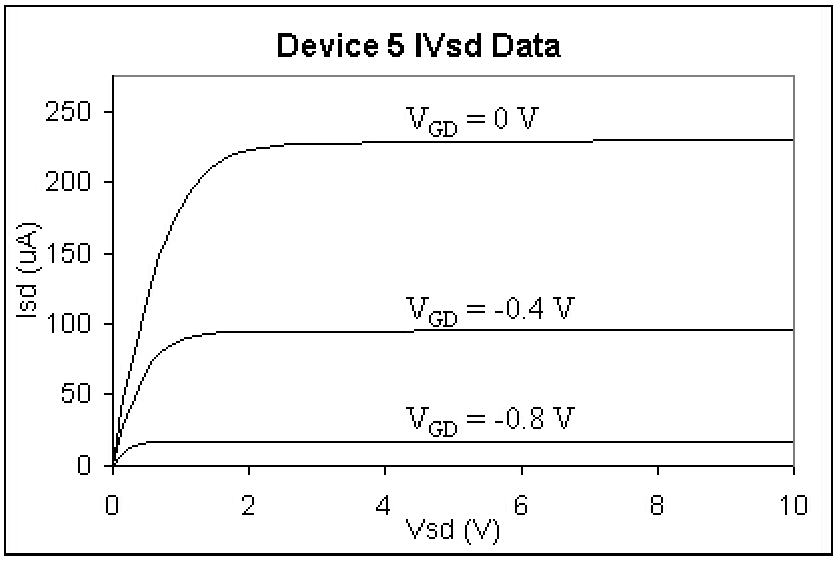

Figure 43: Source-drain IV curves for JFET 5, uniform lightly doped gate with Al contacts.

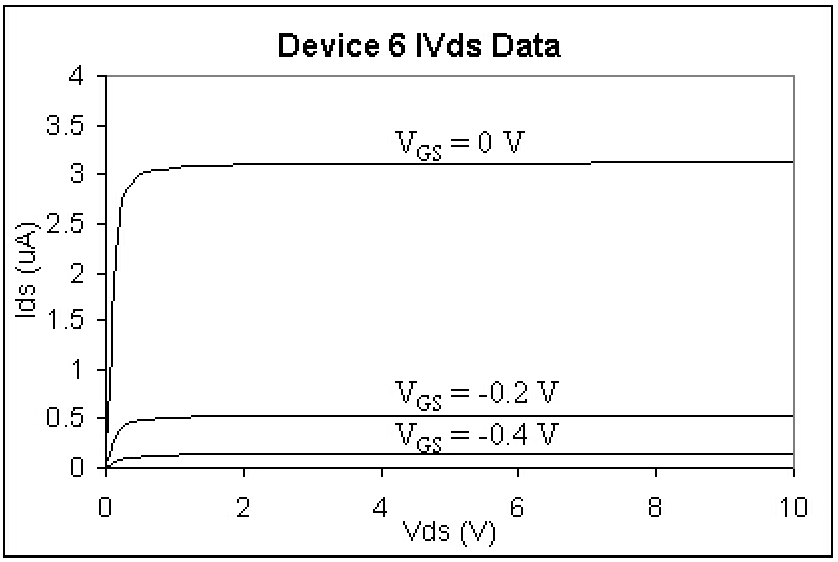

Figure 44: Drain-source IV curves for JFET 6, uniform heavily doped gate with Al contacts.

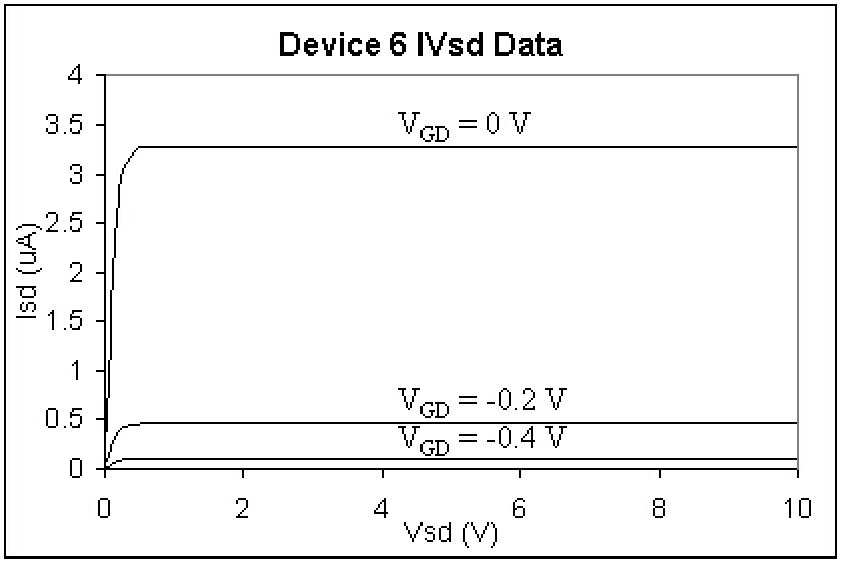

Figure 45: Source-drain IV curves for JFET 6, uniform heavily doped gate with Al contacts.

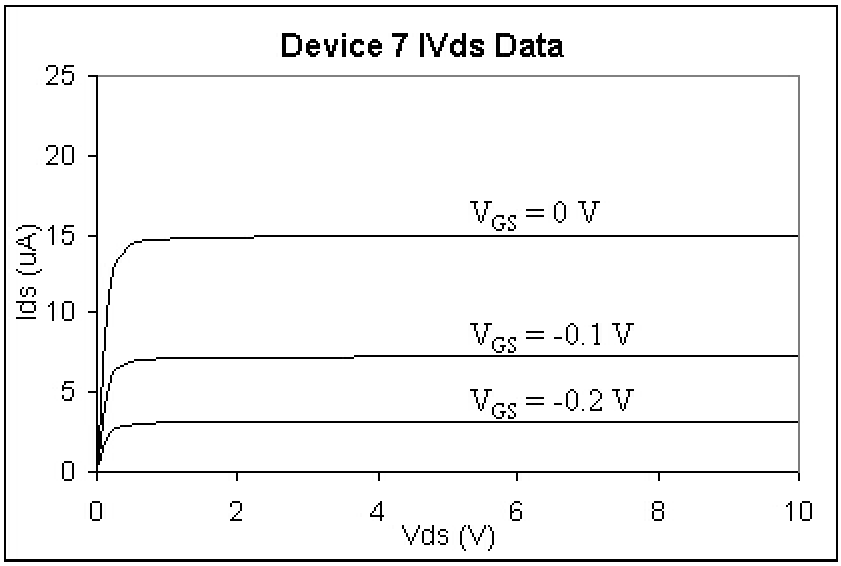

Figure 46: Drain-source IV curves for JFET 7, step doped gate with Al contacts.

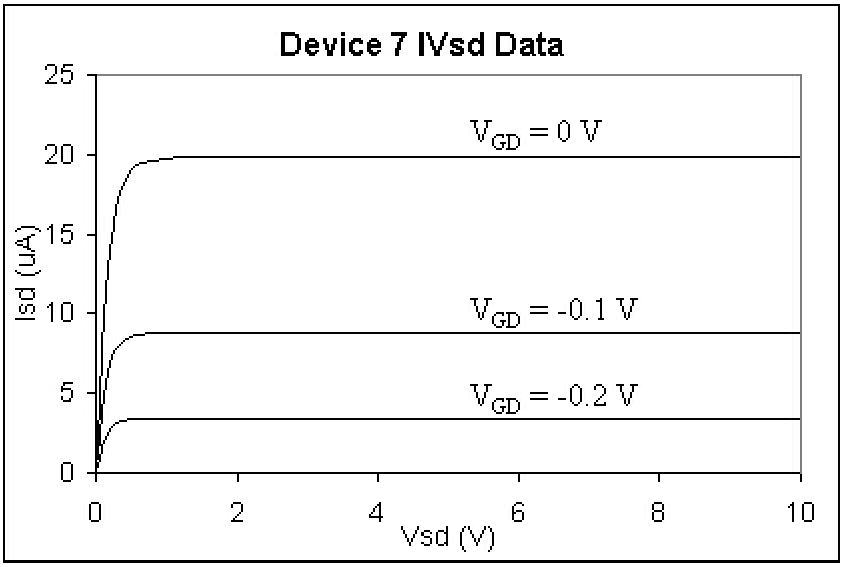

Figure 47: Source-drain IV curves for JFET 7, step doped gate with Al contacts.

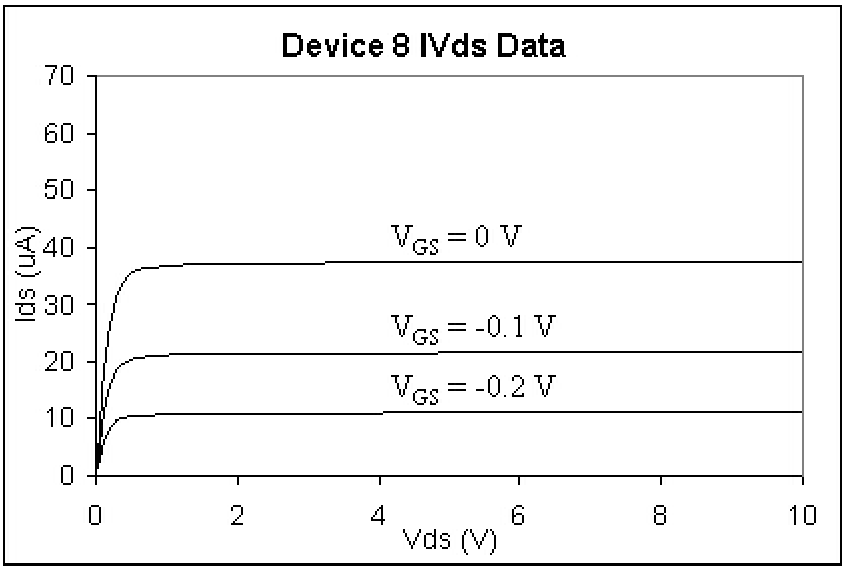

Figure 48: Drain-source IV curves for JFET 8, linearly doped gate with Al contacts.

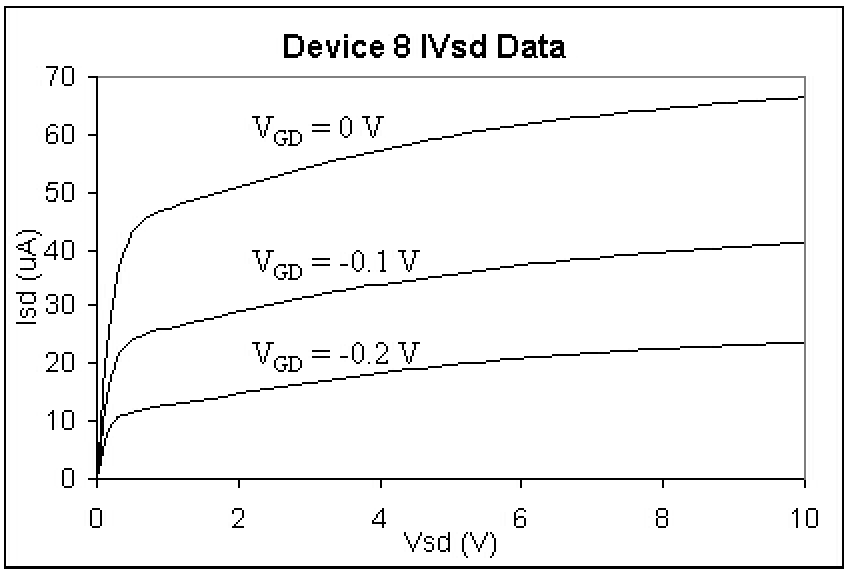

Figure 49: Source-drain IV curves for JFET 8, linearly doped gate with Al contacts.

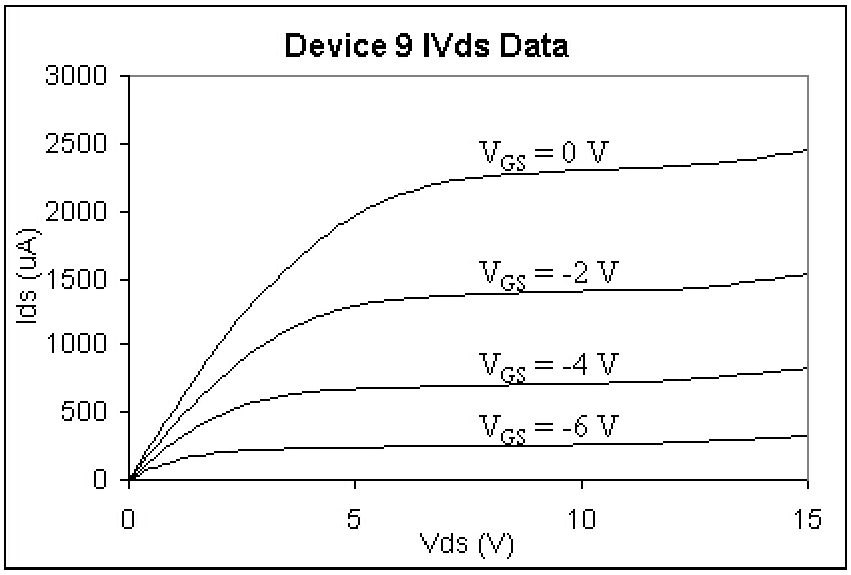

Figure 50: Drain-Source IV curves for JFET 9, uniform lightly doped gate with Al contacts.

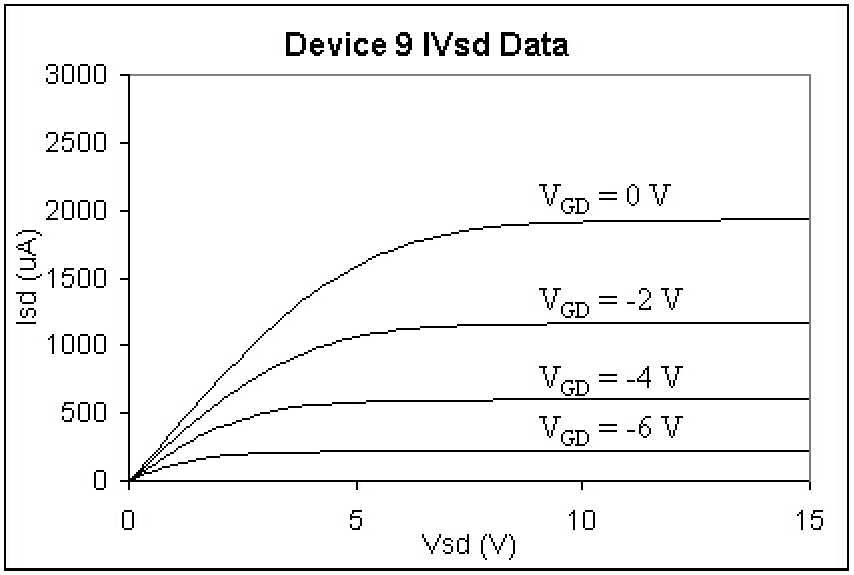

Figure 51: Source-drain IV curves for JFET 9, uniform lightly doped gate with Al contacts.

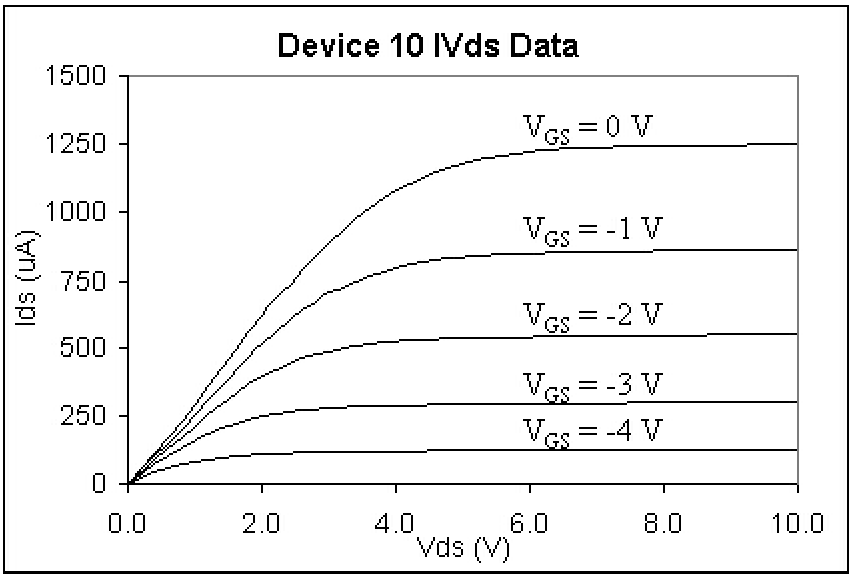

Figure 52: Drain-source IV curves for JFET 10, uniform heavily doped gate with Al contacts.

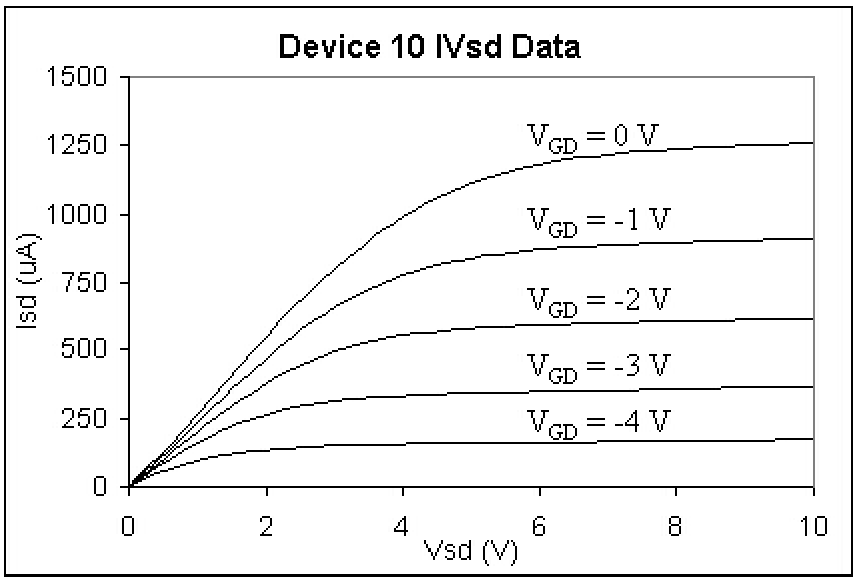

Figure 53: Source-drain IV curves for JFET 10, uniform heavily doped gate with Al contacts.

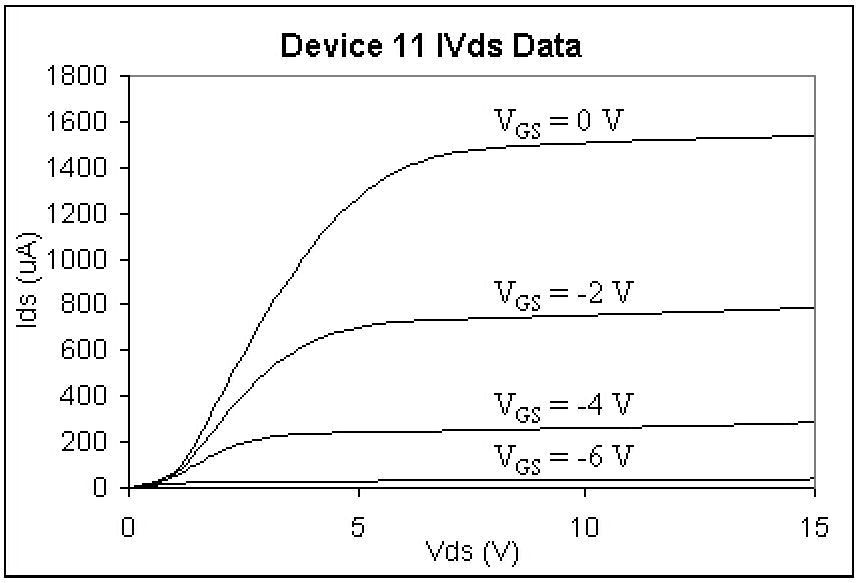

Figure 54: Drain-source IV curves for JFET 11, linearly doped gate with Al contacts.

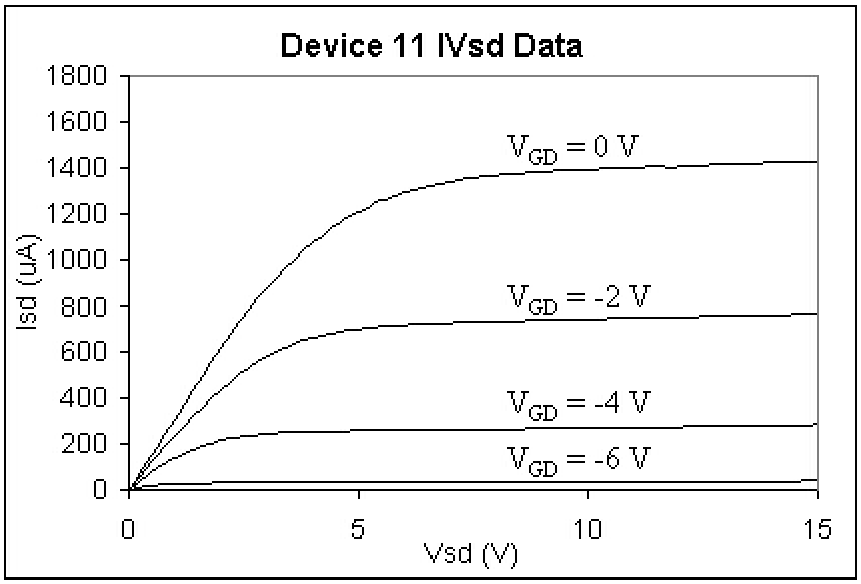

Figure 55: Source-drain IV curves for JFET 11, linearly doped gate with Al contacts.

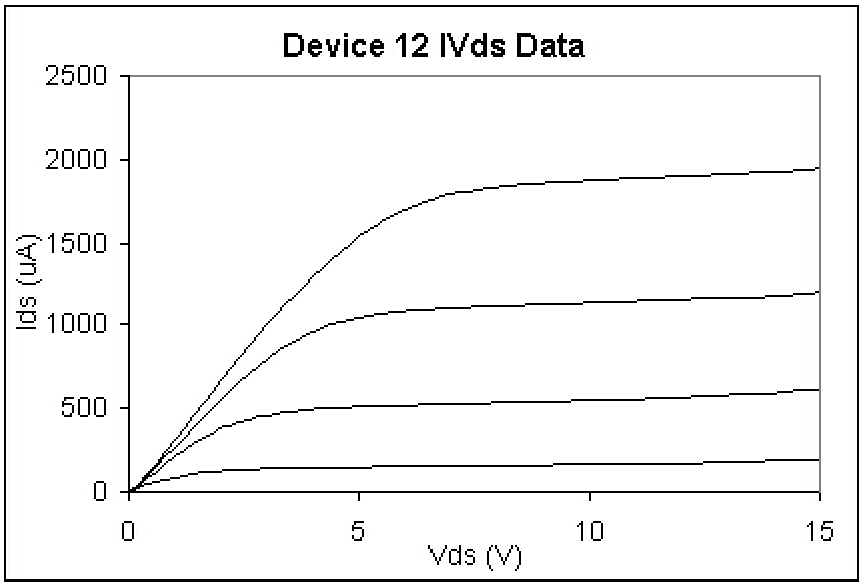

Figure 56: Drain-source IV curves for JFET 12, uniform lightly doped gate with Al contacts.

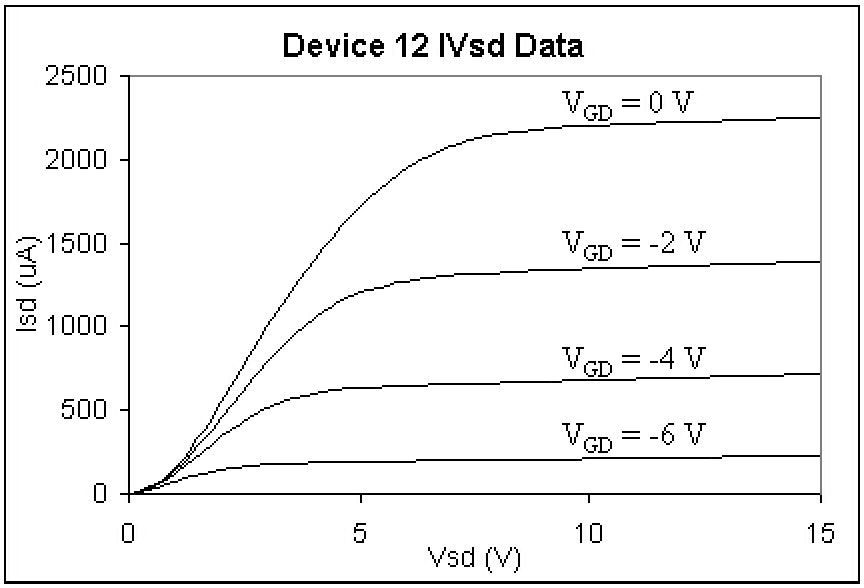

Figure 57: Source-drain IV curves for JFET 12, uniform lightly doped gate with Al contacts.

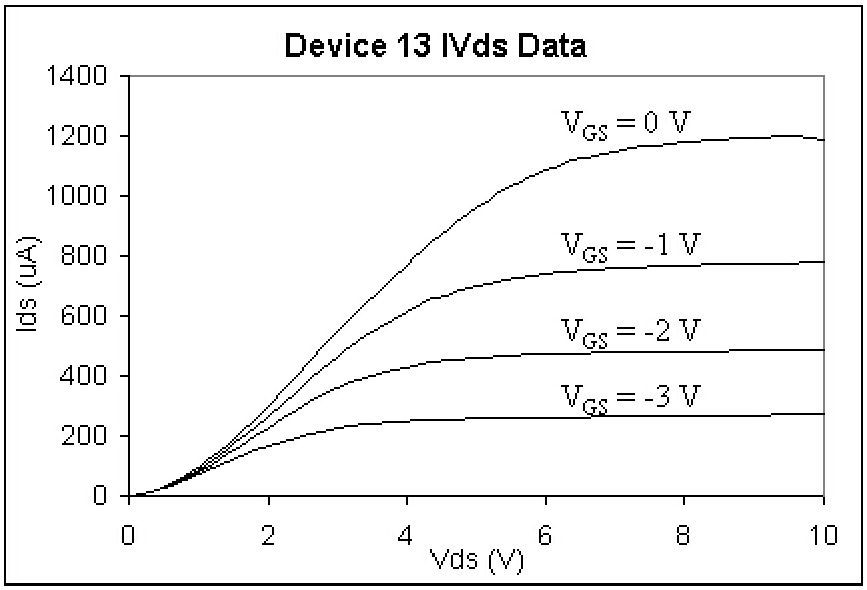

Figure 58: Drain-source IV curves for JFET 13, uniform heavily doped gate with Al contacts.

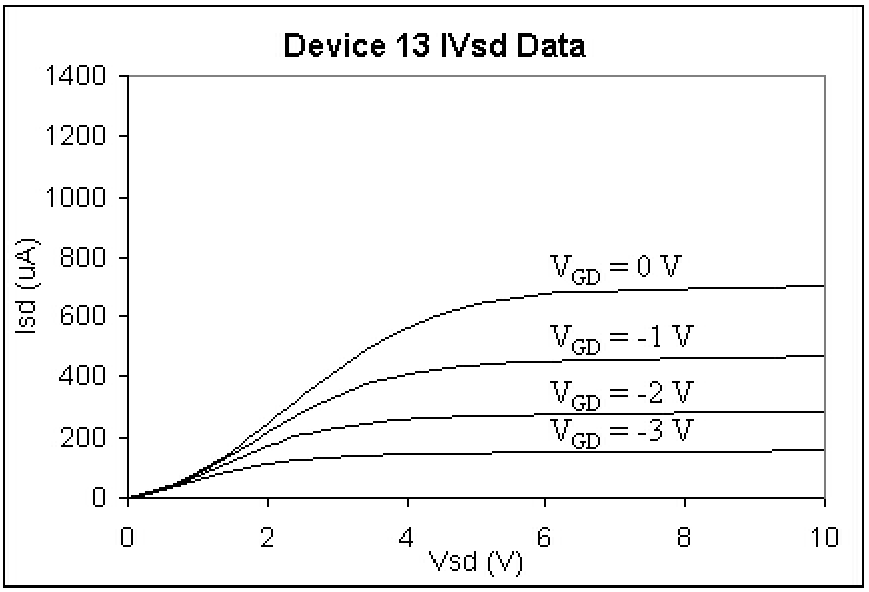

Figure 59: Source-drain IV curves for JFET 13, uniform heavily doped gate with Al contacts.

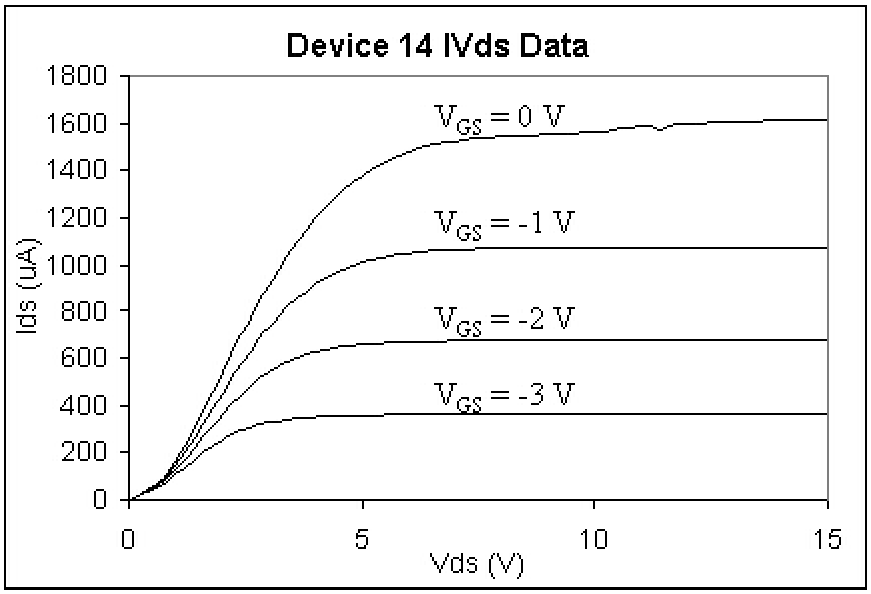

Figure 60: Drain-source IV curves for JFET 14, step doped gate with Al contacts.

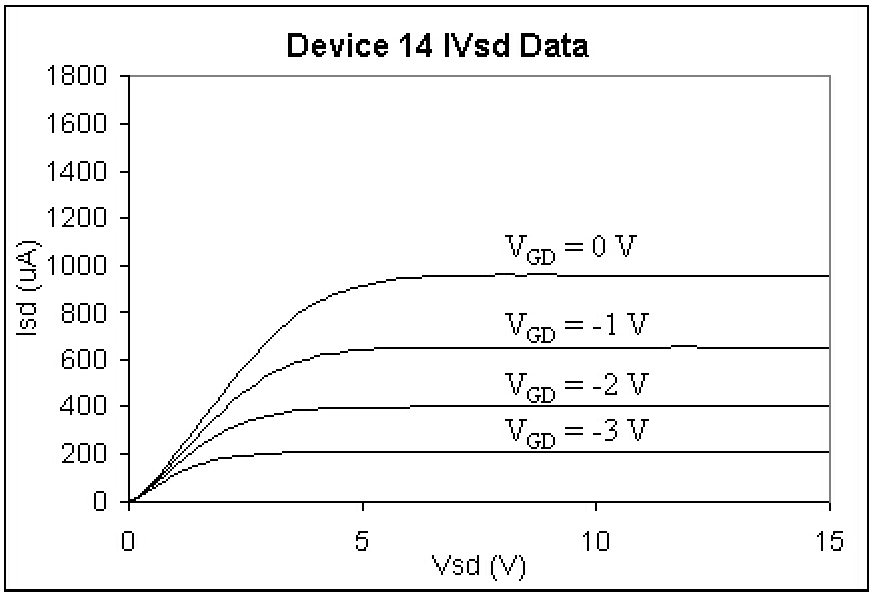

Figure 61: Source-drain IV curves for JFET 14, step doped gate with Al contacts.

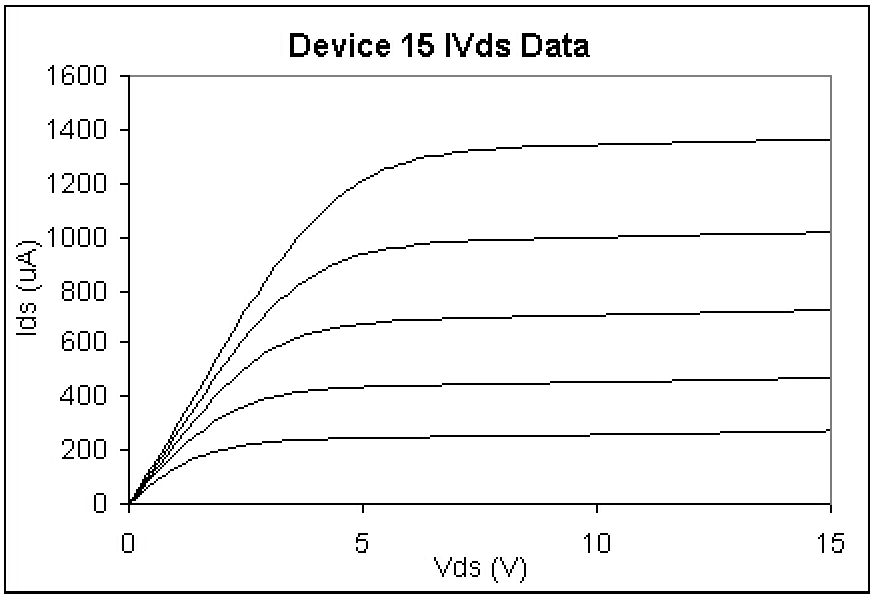

Figure 62: Drain-source curves for JFET 15, linearly doped gate with Al contacts.

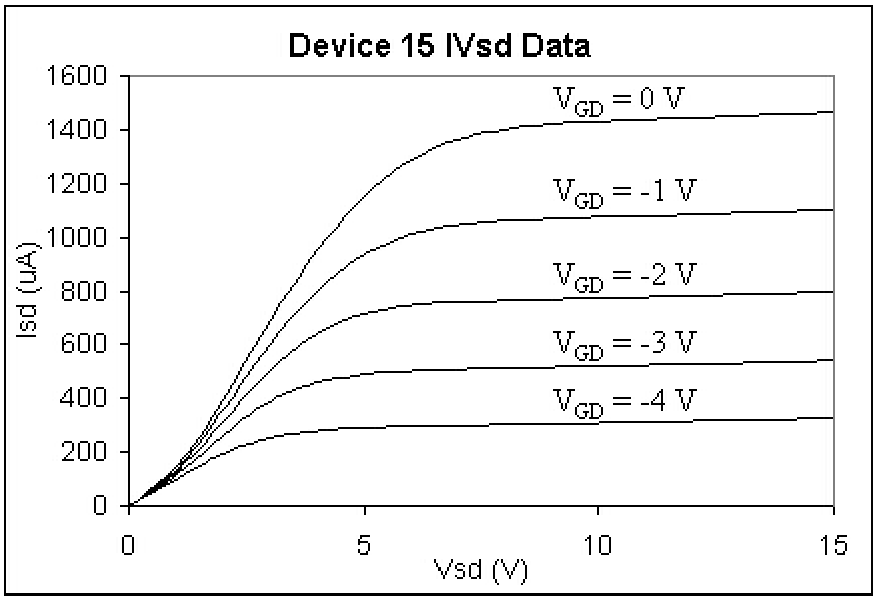

Figure 63: Source-drain curves for JFET 15, linearly doped gate with Al contacts.

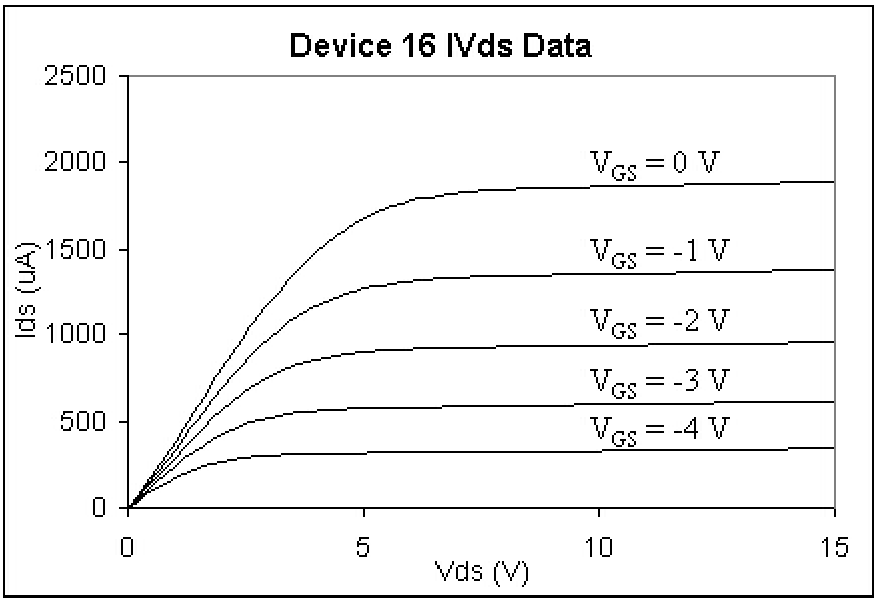

Figure 64: Drain-source IV curves for JFET 16, step doped gate with Al contacts.

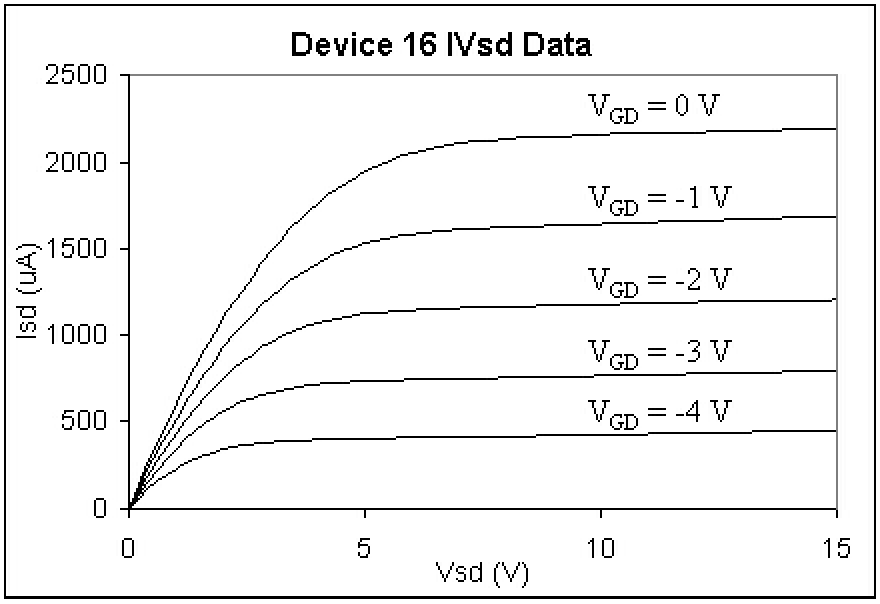

Figure 65: Source-drain IV curves for JFET 16, step doped gate with Al contacts.

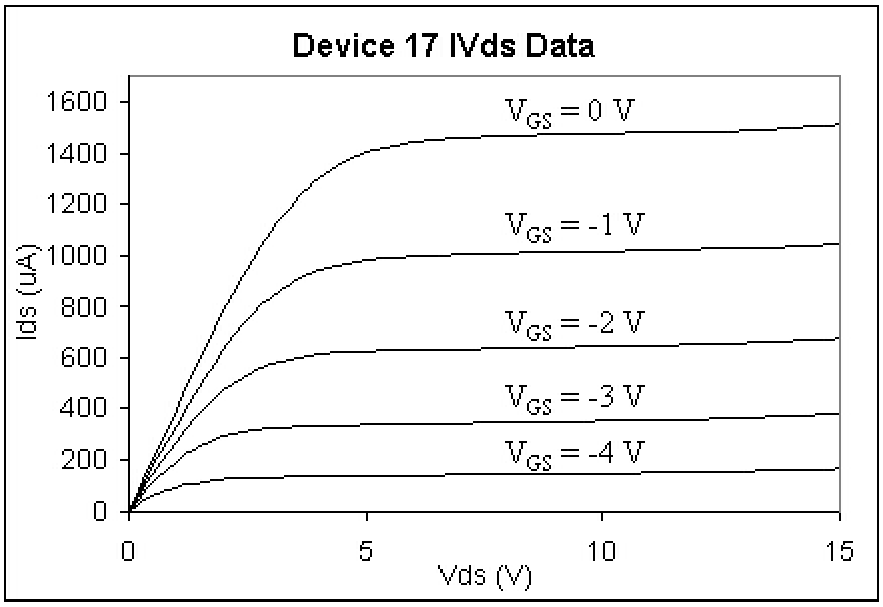

Figure 66: Drain-source IV curves for JFET 17, linearly doped gate with Al contacts.

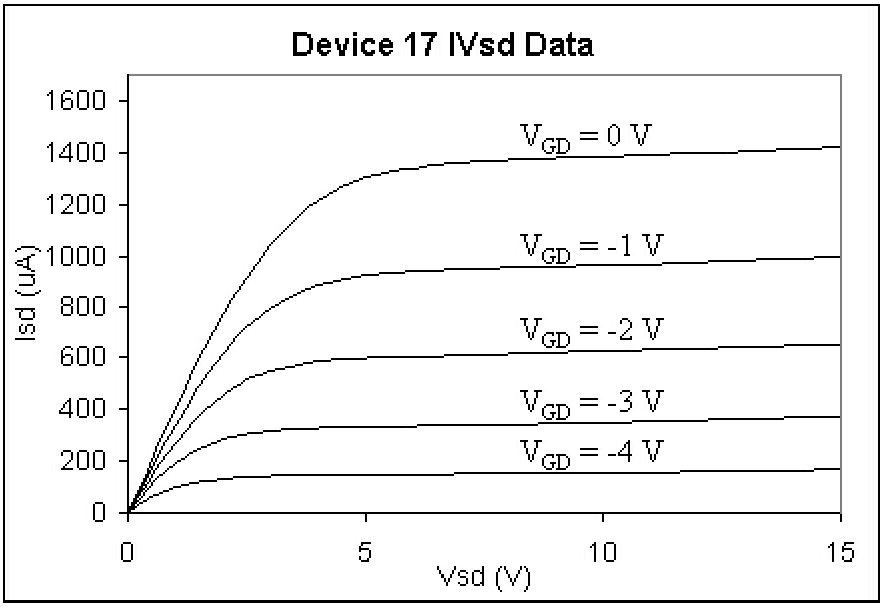

Figure 67: Source-drain IV curves for JFET 17, linearly doped gate with Al contacts.

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