ABSTRACT

Title of Dissertation: REGULATED TRANSFORMER RECTIFIER UNIT FOR MORE ELECTRIC AIRCRAFTS

Ayan Mallik, Doctor of Philosophy, 2018

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The impending trends in the global demand of more-electric-aircrafts with higher efficiency, high power density, and high degree of compactness has opened up numerous opportunities in front of avionic industries to develop innovative power electronic interfaces. Traditionally, passive diode-bridge based transformer rectifier units (TRU) have been used to generate a DC voltage supply from variable frequency and variable voltage AC power out of the turbo generators. These topologies suffer from bulky and heavy low-frequency transformer size, lack of DC-link voltage regulation flexibility, high degree of harmonic contents in the input currents, and additional cooling arrangement requirements. This PhD research proposes an alternative approach to replace TRUs by actively controlled Regulated Transformer Rectifier Units (RTRUs) employing the advantages of emerging wide band gap (WBG) semiconductor technology. The proposed RTRU utilizing Silicon Carbide (SiC) power devices is composed of a three-phase active boost power factor correction (PFC) rectifier followed by an isolated phase-shifted full bridge (PSFB) DC-DC converter. Various innovative control algorithms for wide-range input frequency operation, ultra-compact EMI filter design methodology, DC link capacitor reduction approach and

novel start-up schemes are proposed in order to improve power quality and transient dynamics and to enhance power density of the integrated converter system. Furthermore, a variable switching frequency control algorithm of PSFB DC-DC converter has been proposed for tracking maximum conversion efficiency at all feasible operating conditions. In addition, an innovative methodology engaging multi-objective optimization for designing electromagnetic interference (EMI) filter stage with minimized volume subjected to the reactive power constraints is analyzed and validated experimentally.

For proof-of-concept verifications, three different conversion stages i.e. EMI filter, three-phase boost PFC and PSFB converter are individually developed and tested with upto 6kW (continuous) / 10kW (peak) power rating, which can interface a variable input voltage (190V-240V AC RMS) variable frequency (360Hz – 800Hz) three-phase AC excitation source, emulating the airplane turbo generator and provide an AC RMS voltage of 190V to 260V. According to the experimental measurements, total harmonic distortion (THD) as low as 4.3% and an output voltage ripple of ±1% are achieved at rated output power. The proposed SiC based RTRU prototype is ~8% more efficient and ~50% lighter than state-of-the art TRU technologies.

REGULATED TRANSFORMER RECTIFIER UNIT FOR MORE ELECTRIC AIRCRAFTS

by

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Dissertation submitted to the Faculty of the Graduate School of the
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V…….. Input AC amplitude

V_{DC}……... Intermediate DC link voltage

V_{kn}……... 'k'th phase-neutral voltage

V_{nN}……... Neutral to DC link negative voltage

V_O……. Output voltage

i_K…….. 'k'th phase current

d_{kH} ……... High side duty ratio for 'k'th phase (k=A, B or C)

f_{sw}……..... Switching frequency

C_{DC}……... Intermediate DC link capacitor

C_O……. Output capacitor

P……... Output power

P_{switch}……..Total switching losses in PFC MOSFETs

P_{ind}……...Total conduction losses in PFC boost inductors

$P_{ESR,PFC}$ ……...Equivalent series resistance (ESR) losses in PFC DC link capacitors

$P_{cond,PFC}$……..Net conduction losses in PFC stage

P_{body}……Total power loss in body capacitors of PFC MOSFETs

$P_{sw,PFC}$…….Total switching losses in PFC MOSFETs

$P_{snubber}$……Total power losses in PSFB secondary side snubber circuit

$P_{sw,pri}$……...Total switching losses in PSFB primary side

P_{SR}……Total conduction losses in SR MOSFETs

$P_{trans,sec}$……Total conduction losses in transformer secondary side

$P_{cond,Ls}$……..Total conduction losses in PSFB secondary inductor

$P_{ESR,PSFB}$……..ESR losses in PSFB output capacitors

$P_{sw,sec}$……...Total switching losses in PSFB secondary side

$P_{cond,pri}$……..Total conduction losses in PSFB primary side including transformer winding

P_{Gate}……..Total gate power losses

P_{Core}……..Transformer core loss

P_{PFC}……....Total losses in PFC stage

P_{PSFB}……Total losses in PSFB stages

P_{tot}……Total power losses in RTRU

$r_L{}'$……..DC resistance of output inductor

r_T'……DC resistance of transformer secondary winding

R_{DS}'……Drain-source on-sate resistance of PSFB secondary MOSFETs

r_T……DC resistance of transformer primary winding

R_{DS}……Drain-source on-sate resistance of PSFB primary MOSFETs

$R_{DS,PFC}$……Drain-source on-sate resistance of PFC MOSFETs

I_{RMS}……RMS of PFC MOSFET current

$I_{in,RMS}$……RMS of PFC input phase current

$i_{s,RMS}$……RMS of PSFB secondary current

$i_{sec,RMS}$……RMS of PSFB secondary MOSFET current

$i_{pri,RMS}$……RMS of PSFB primary MOSFET current

i_p……PSFB primary side winding current

Chapter 1: Introduction

1.1 More Electric Aircrafts

Relentless increase in air traffic poses the question of how to achieve better fuel efficiency while minimizing environmental damage, and especially in a fuel-efficient manner. Advances in Power Electronics are enabling companies, like Boeing for example, to replace pneumatic systems, vital for flights, with electrical systems. As has been the case with the 787 models, Boeing is hoping to achieve fuel savings of about 3%, and extract as much as 35% less power from the aircraft's engines [1]. The various types of power utilized in an aircraft can be categorized into electrical, mechanical, pneumatic and hydraulic power. The distribution and utilization of electrical power is highly dependent on the power generation and distribution architecture inside the airplane. The Boeing 777 electrical system, shown in Fig.1.1, is "comprised of two independent electrical systems" the main and the backup [1].

The main system involves "two engine-driven integrated drive generators/ turbo generators, a generator driven by the auxiliary power unit (APU), three generator control units, and a bus power control unit." The specifications of the power generation of the 777 are 3-phase 115V RMS AC output from a constant speed turbo generator.

Two of the engines running at regular speed combine to form an engine-drive, which is also called "Integrated drive generator (IDG)". As a back-up alternative, there is an auxiliary generator, which also works at constant speed. Every generator located in the main system can be used by one or both main buses and the load circulated from left to right.

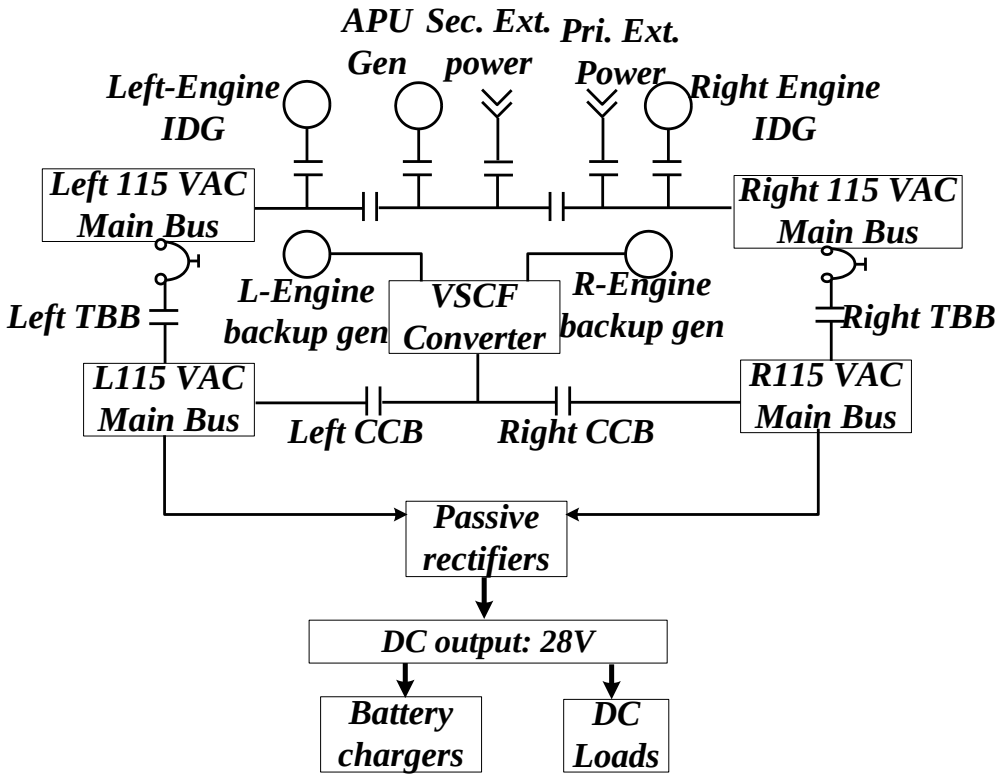


Fig.1.1. Electrical power generation and distribution architecture inside Boeing 777

(APU: Auxiliary power unit, TBB: Terminal bus bar, VSCF: variable speed constant frequency, IDG: Integrated drive generator, CCB: Centralized circuit breaker)

On the other hand, the Boeing 787 electrical system shown in Fig. 1.2 has a hybrid voltage design. The system is comprised of "six generators, two per engine and two per APU-operating at 235 VAC" [2]. The voltage outputs from all the turbo generators vary in a wide range of frequencies depending on the generator speed at different flight conditions. This enables elimination of requirement of gearbox-based heavy VSCF generator unlike Boeing-777 utilizing fixed frequency generators. Additionally, ground power receptacles are included in the system design "for airplane servicing on the ground without the use of the APU" [2-3].

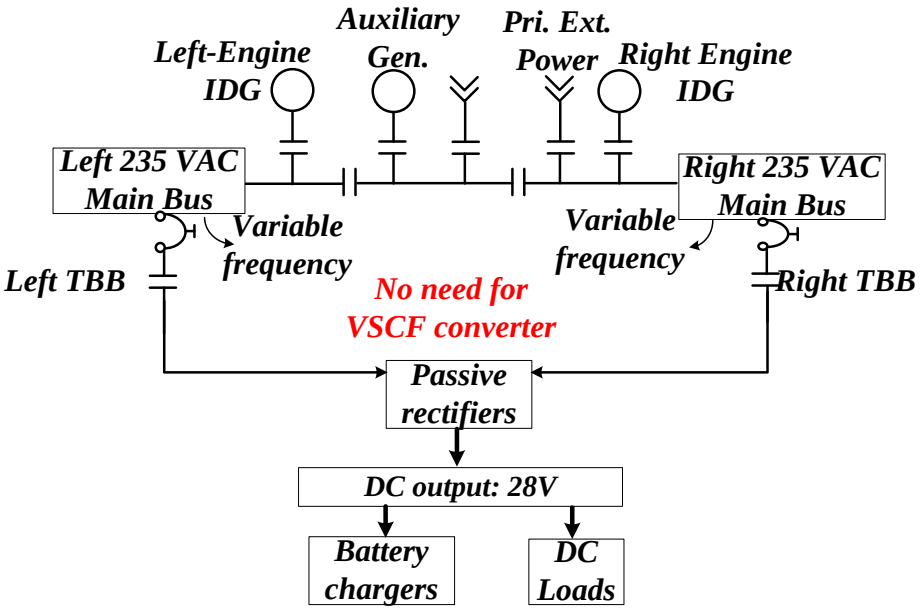


Fig. 1.2. Electrical power generation and distribution architecture inside Boeing 787

All the systems' generators are directly connected to the engine gearboxes and can be operated at a variable frequency (360 to 800 Hz) proportional to the engine speed [4]. With the new 787 no-bleed architectures, which moves away from the previous pneumatic school of thought, to the electrical, Boeing is aiming to achieve the following:

- All the APU components that were typically associated with the pneumatic power delivery in Boeing 777 are eliminated i.e. now rely on electrical components
- Highly efficient engine cycles
- Higher efficiency in secondary power extraction, power transfer and energy usage
- Also, as a note of interest, the remote power distribution units (RPDUs) are designed based on solid state power controllers (SSPC) in B-787 instead of the traditional thermal circuit breakers and relays, prevalent in the architecture of the B-777.

Finally, as a summary, the Boeing 787 Dreamliner relies much more heavily on electricity, than any other Boeing airplane. In order to use more electricity than any other airplane, the 787 must also produce "more electricity – 1.5 megawatts, or four times as much as other Boeing airplanes [4]. The more electric aircraft (MEA) concept in general calls for a reduction in size and weight in order to reduce the take-off weight of the aircraft which finally results in cost reduction due to reduced fuel consumption.

1.1.1 Transformer Rectifier Unit

Traditionally, passive diode-bridge based transformer rectifier units (TRU) have been used to generate a DC voltage supply from variable frequency and variable voltage AC power out of the generators. A conventional TRU consists of a three-winding transformer with its primary winding connected to the input AC voltage of the onboard generator of the plane and its secondary and tertiary windings connected to the output DC-link [5-6]. The topology presented in [5], shown in Fig. 1.3(a) contains a transformer, in which all the windings are wye-connected. In this approach, the secondary and tertiary windings are connected to two three-phase diode-bridges, which are connected in parallel through a switch. The rectified DC output corresponding to the secondary winding has higher amplitude than the rectified DC voltage level from tertiary winding. Once the control switch is ON, the TRU output comes from secondary side winding V_{R1}, and tertiary bridge rectifier diodes remain reverse biased and turned off. TRU output comes from tertiary bridge rectifier V_{R2}, once the control switch is OFF. Therefore, the average output voltage from TRU becomes $dV_{R1}+(1-d)V_{R2}$, where 'd' is the duty ratio of S_1. This topology intends to provide an average output voltage of 28V through averaging the two DC outputs [5].

Another TRU configuration includes a three-winding transformer with its primary wye-wound winding connected to the AC input power, and both delta-wound secondary/tertiary windings connected to two three-phase diode-bridge rectifiers, which are connected to an output filter through a synchronous rectification switching circuit [6], shown in Fig. 1.3(b). The topology proposed in [7] acts as a 12-pulse rectifier using phase-shifted transformers. Both of the above mentioned topologies [5–6] use low frequency transformers with multiple windings, which make the system bulky, heavy and degrade the efficiency. Another issue with these topologies is the presence of the 5th and higher order harmonics in the input current waveform, which increases the total harmonic distortion (THD), and in turn causes harmonic losses. High switching frequency operation will cause significant core losses in the transformer and degrade the efficiency. In addition, it is very difficult to tightly regulate the output DC link voltage using diode bridges and without oversizing the DC-link filter capacitor. Another TRU configuration, shown in Fig. 1.3(c) [7] consists of three single-phase diode-bridge converters, each followed by an individual single-phase boost DC-DC converter, with their outputs connected in parallel. An additional stepdown DC-DC converter is required for output voltage regulation at the desired voltage [7]. Using more devices and capacitors in this topology increases the weight and size of the converter and utilization of front-end diode bridge rectifiers decreases the total conversion efficiency.

In order to improve the output voltage ripple and smoothen the input AC current, 12 or 18-pulse rectifier systems (shown in Fig. 1.3(d)) are used in most of the traditional airplane power systems, listed in Table 1.1.

Table 1. 1. Commercially available TRUs – state-of-the-art technologies

Manufacturer (Part number)	Power (kW)	Volume ($inch^3$)	Weight (lbs.)	Efficiency	Power factor	Input frequency	Input voltage
Avionic Instruments TRU4200-1B-1883	4.2kW	222	11	85%	0.95	340-600Hz	108-118 VAC, 3-phase
Avionic Instruments RTR5600-1A-2014	5.6kW	621	22	85%	0.97	380-420Hz	108-118 VAC, 3-phase
Avionic Instruments TRU8400-1A-1009	8.4 kW	494	24.25	86%	0.95	380-420Hz	190-210 VAC, 3-phase
Crane (81-107)	5.6kW	455	15.6	86%	0.96	324-600Hz	115VAC, 3-phase
Crane (81-083)	7kW	723	18.5	85%	0.95	400Hz	115VAC, 3-phase

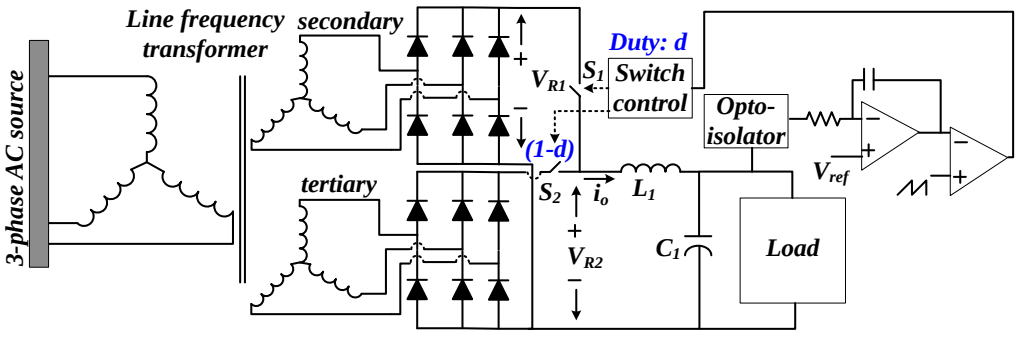


Fig. 1.3 (a) Transformer rectifier unit structure proposed in [5]

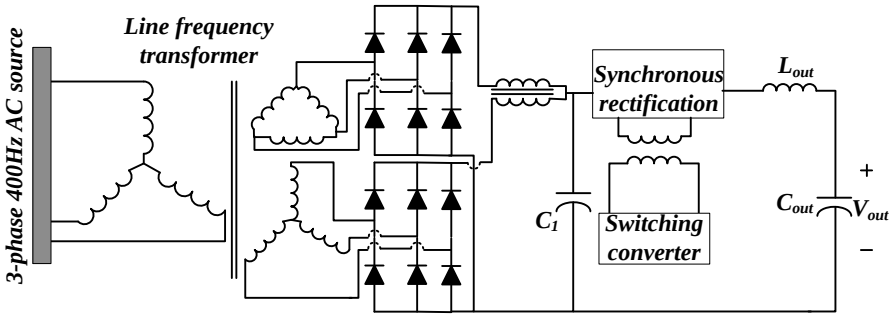


Fig. 1.3(b) Transformer rectifier unit structure proposed in [6]

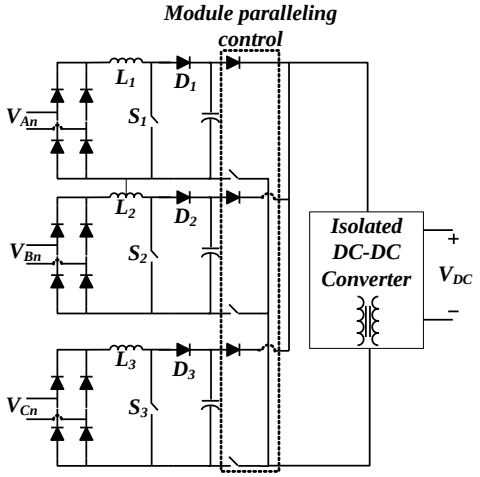


Fig. 1.3(c) Transformer rectifier unit structure proposed in [7]

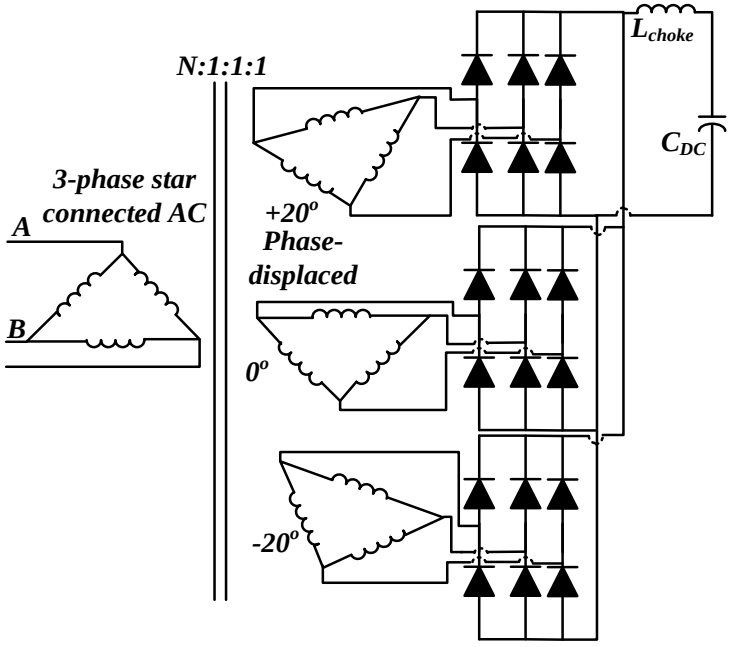


Fig. 1.3(d) Transformer rectifier unit using 18-pulse rectifier structure [8]

One of the conventional approaches to operate a '6k' pulse rectifier system is to provide a suitable spatial phase displacement between the primary side and secondary side transformer windings. Fig. 1.3(d) shows an eighteen-pulse rectifier using a transformer with a delta primary and three phase 20^{o} displaced wye secondary windings. Any 'k' pulse rectifier system will have harmonics at frequencies $(kn\pm1)f_g$, where 'f_g' is turbo generator output frequency and 'n' is any integer. Avionic systems have very stringent limits for 11^{th} and 13^{th} grid harmonics amplitude according to DO-160F avionics standard, which cannot be fulfilled with 12-pulse front-end rectifier systems. In the eighteen-pulse system shown in Fig. 1.3(d), the input current will have theoretical harmonic components at the following multiples of the fundamental frequency: 17, 19, 35, 37, 53, 55, etc. Since the magnitude of each harmonic is proportional to the reciprocal of the harmonic number, the eighteen-pulse system has a lower theoretical harmonic current distortion than twelve-pulse rectifier system. Also, it is important to mention that any '6k' pulse rectifier system utilizes 'k' number of line frequency transformers. Therefore, although 18 or higher pulse rectifier systems are the feasible choices for TRUs, there is great potential in replacing them by active rectifier systems, due to the higher volumes and weights coming from line-frequency transformers in passive TRUs.

Furthermore, relatively larger differential mode capacitors (~3-5μF) are required in order to comply with EMI standards, which in turn draw high amounts of reactive power [11]. To compensate for this reactive power, huge inductances (~10-15mH) need to be placed in parallel to the filter capacitors, which again make the system heavier. Therefore, keeping weight minimization as a major target for airplane power supplies

sets a restriction / limitation on using TRUs as auxiliary power supplies. Some of the state-of-the-art TRUs [9-10], designed based on 12 or 18-pulsed rectifiers are listed in table 1.1. Moreover, most of the state-of-the-art TRUs operate at 115VAC within a narrow range of input AC excitation frequency (around 400Hz). The Crane 81-107 can operate with the input voltage frequency range from 324Hz to 600Hz.

1.1.2 Regulated Transformer Rectifier Unit

The replacement of the non-electric systems by electrical units results in a considerably higher electrical power demand. Whereas in a conventional aircraft Boeing 777, the installed capacity is about 400 kVA, the installed capacity of the recently released MEA aircraft Boeing 787 Dreamliner will have an installed capacity of 1 MVA [4]. In order to avoid the aforementioned issues of the conventional TRUs, an alternative approach is to design a RTRU using an actively controlled three-phase AC-DC converter. The input to RTRU will be the 3-phase variable-frequency variable-voltage AC output of the turbo generator and the RTRU output will be regulated at around 28V DC. Fig. 1.4 and Fig. 1.5 represent the existing and the proposed electrical system diagrams of Boeing 787, respectively. As a major difference, unlike 115VAC 400Hz (fixed frequency) operation in Boeing 777, the variable-frequency starter generators (VFSGs) in Boeing 787 supply 235 VAC at a variable frequency ranging between 360 and 800 Hz. The outputs of four VFSGs are fed together to the 235 VAC distribution buses. The 235 VAC is then transformed and rectified by an Auto Transformer Rectifier Unit (ATRU) to supply large 270 VDC loads such as Cabin Air Compressors, fuel pumps, and hydraulic pumps. The distribution buses also supply two 115 VAC bus bars via Auto Transformer Units (ATUs), and four 28 VDC buses via

Transformer Rectifier Units (TRUs). As better alternatives to the TRUs, the main focus of this work i.e. RTRU is shown as a part of the proposed electric power system architecture of Boeing 787 in Fig. 1.5. In the proposed architecture, the RTRU consists of a three-phase active boost-type power factor correction (PFC) converter followed by a phase-shifted full-bridge (PSFB) isolated DC-DC converter. The power factor correction converter is tied to the airplane grid through a front-end EMI filter stage. The active power conversion enhances power density, lowers weight, improves efficiency, and enables better voltage regulation and improved EMI performance in comparison to the conventional TRUs. Furthermore, due to tight output voltage regulation, it would reduce the weight of low voltage distribution cables and wiring onboard the airplane. The proposed regulated rectifier unit is capable of operating in a wide range of input frequencies between 360Hz and 800Hz and input voltage RMS between 190V and 260V, depending on the alternator speed of a turbo generator. One of the main challenges lies in designing a unique controller maintaining all specified avionic requirements over the entire range of source frequencies. Furthermore, as far as the power flow is concerned, it is important to mention that any active power converter system is prohibited from regenerating energy back to the mains grid in airplanes [11]; therefore, RTRUs with bidirectional rectifier systems must have a control signal to disable the reverse power flow. However, in the case of a failure, where for instance the rectifier system is disabled, an energy feed-back could occur.

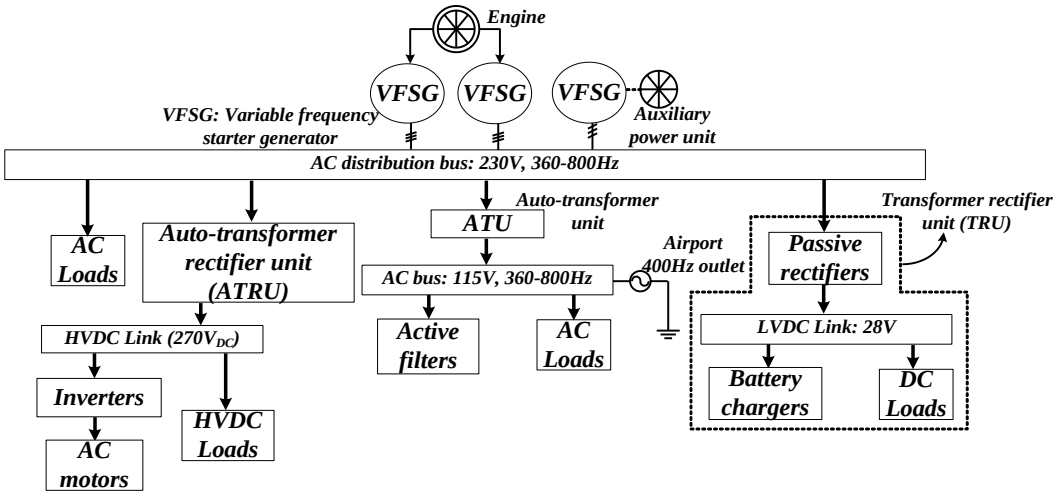


Fig. 1.4. Electrical power system architecture inside Boeing 787 Dreamliner [12]

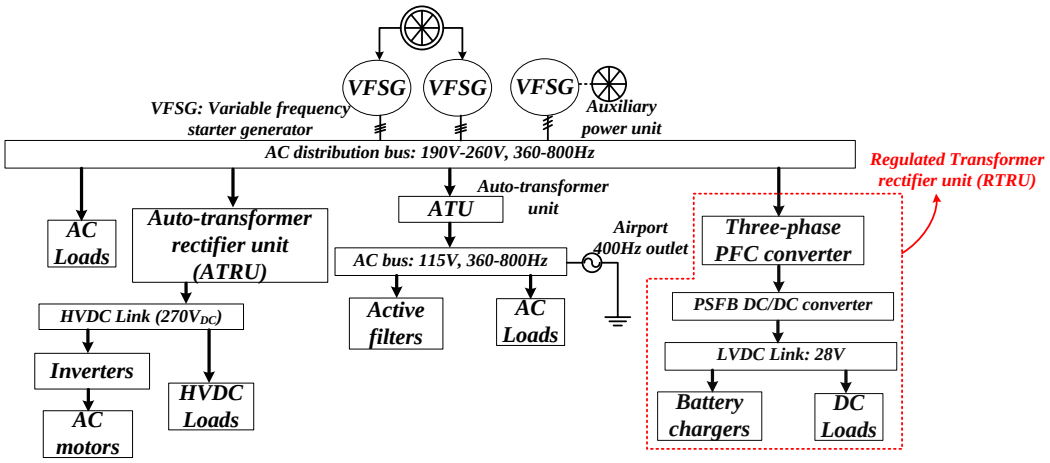


Fig. 1.5. Electrical power system architecture with the proposed RTRU inside Boeing 787 Dreamliner

In this work, the RTRU is designed with an objective of strictly satisfying all the following requirements, which are specifically applied to the next generation MEAs.

1.1. The RTRU shall provide regulated nominal 28V$_{DC}$ power.

1.2. The RTRU shall have a continuous rating of 6kW on its output under normal operating conditions and a transient (overload) rating upto 10kW.

1.3. With an average 3-phase input voltage steady-state conditions the RTRU steady state output voltage shall be 28V DC nominal with maximum peak-peak ripple of ±1%.

1.4. Startup process needs to be completed within five line cycles with an inrush current below four times of rated current [13].

1.5. The RTRU efficiency shall be greater than 92% under normal operating conditions at rated load.

1.6. Targets for the power factor and THD are set as >0.99 and <5%, respectively at full load, based on the future trend of power quality regulations [11].

1.7. RTRU shall meet Conducted EMI requirement defined by DO-160F EMI/EMC standard [14], shown in Fig. 1.6.

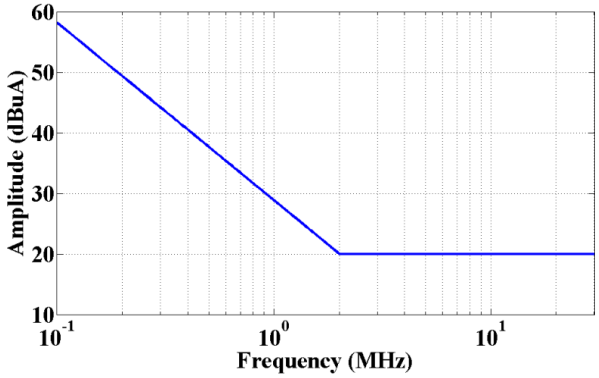


Fig. 1.6. DO-160F EMI Standard

As for mains interfaces in industrial environment, AC-DC converter systems used in aircraft applications must comply with (avionics) standards. Primarily the airborne standard DO160F [14] and the military standard MILSTD704F [15] have to be satisfied. Some major power quality requirements including individual upper bounds on current harmonics are listed as follows.

1.8. Current harmonics limits (I_h) are summarized in Table 1.2 [I_1: fundamental amplitude].

Table 1.2. Current harmonics limits

Harmonic Order	Limits
3^{rd}, 5^{th}, 7^{th}	$I_h = 0.02\ I_1$
Odd Triplen Harmonics (h = 9, 15, 21, ..., 57)	$I_h = 0.1\ I_1 / h$
Odd Non Triplen Harmonics 11,13	$0.03\ I_1$
Odd Non Triplen Harmonics 17, 19	$0.04\ I_1$
Odd Non Triplen Harmonics 23, 25	$0.03\ I_1$
Odd Non Triplen Harmonics	$I_h = 0.3\ I_1 / h$
(h = 29, 31, 35, …, 61)	
Even Harmonics 2 and 4	$I_h = 0.01\ I_1 / h$
Even Harmonics > 4 (h = 6, 8, 10, ..., 62)	$I_h = 0.0025\ I_1$

1.9. The input phase-to-neutral AC RMS voltage may vary between 190V and 260V

1.2 Objectives and Research Problems

The fundamental objective of this work is to replace the passive TRU solutions by wide band gap Silicon Carbide (SiC) based actively controlled RTRUs with fulfilling all the electrical requirements of more-electric-aircrafts, listed in section 1.1.2. Moreover, the research concentrates on enhancing the specific and gravimetric power density of AC-DC conversion unit and also, on improving all the performance parameters such as efficiency, dynamic performance, start-up, input power quality, and EMI across all load power levels.

Subsequently, the major research problems on which research effort has been focused in this work are briefly as follows:

- Duty compensated feedback control of three-phase boost PFC for THD improvement -- Improved power quality
- Control of three-phase PFC without using any input voltage sensors -- Economic and reliability benefits
- Fast start-up PFC control with minimum inrush current -- Less stress on power devices
- Design of adaptively tuned compensator for maintaining unity power factor with THD<5% at any grid frequency from 360Hz to 800Hz -- Improved power quality
- A novel soft switching methodology in three-phase boost PFC -- Higher efficiency
- Variable switching frequency control of phase-shifted full-bridge (PSFB) DC-DC converter for maximum efficiency point tracking -- Higher efficiency, economic benefits
- Derivation of EMI noise model in RTRU and an innovative approach to design common mode (CM) filter stage -- Better understanding on EMI noise
- Ultra-compact and optimized design of EMI filter for RTRU -- Improved power density
- Reduced state observer-based state-feedback control of two-stage integrated AC-DC converter – power quality enhancement and faster dynamics
- Maximum efficiency tracking of RTRU using variable intermediate DC link voltage at a wide range of operating conditions – higher efficiency

- Intermediate DC link capacitance reduction in a three-phase RTRU – Improved power density

1.3 Synopsis of the Dissertation

In Chapter 2, design and control of three-phase boost PFC converter including different design considerations and hardware implementation are carefully discussed. Innovative control methodologies for improving the input power quality in wide input frequency range are introduced and analyzed in detail. A novel concept of soft-switching strategy in a three-phase boost PFC converter using an auxiliary switching circuit is proposed and experimentally validated for the first time; zero voltage switching (ZVS) is performed at all six switches of the PFC stage.

In Chapter-3, three following major control objectives have been individually analyzed and achieved through a unique integrated controller: (i) to minimize the start-up time with minimum inrush current (ii) to achieve perfect unity PF at the entire range of source frequencies (360 Hz to 800 Hz for avionic applications) and (iii) to achieve fast tracking of reference phase currents i.e. faster settling under any load or line transients.

In Chapter-4, hardware design considerations of phase-shifted full-bridge (PSFB) converter with low voltage, high-current output in RTRU application are analyzed. Furthermore, the total losses are formulated as a function of switching frequency and conditions for zero-voltage-switching in frequency domain. Parametric minimization of loss model is performed to determine the optimum value of switching frequency for achieving maximum conversion efficiency in PSFB stage. Thereby, a comparison

between fixed and variable switching frequency control methods is presented with experimental validations.

In Chapter-5, a comprehensive procedure and a set of guidelines for designing compact EMI filter for RTRU application are presented. Different design constraints based on maintaining the unity power factor operation and hence, limiting reactive power transfer below a certain limit are also discussed analytically. Furthermore, a genetic algorithm based constrained optimization process for minimizing filter volume is performed to obtain optimum LC parameters for practical realization. Finally, experimental results of EMI spectrum of the converter with implemented EMI filter are captured by spectrum analyzer and proven to be complying with DO-160F conducted EMI standard.

In Chapter-6, the overall stability, dynamic performance, and power efficiency maximization for further improvement of the RTRU have been investigated, analyzed and discussed. Different innovative methodologies are proposed, experimentally verified and compared with state-of-the-art for the following problem statements: (i) state-feedback control loop design of the integrated two-stage AC-DC converter for power factor maximization and dynamics improvement; (ii) efficiency maximization of the integrated RTRU by optimum variable intermediate DC link voltage.

In Chapter-7, passive component's volume minimization and thus, RTRU power density enhancement is implemented by reducing the intermediate DC link capacitance, its size and its weight. The capacitance reduction technique is realized by minimizing the amplitude of the switching frequency component of the ripple current

through the DC link capacitor, which is in turn achieved by PFC phase-duty ratio modulations without affecting the PFC action.

In Chapter-8, relevant conclusions from the research works performed during the PhD research phase along with several prospective future researches on alternative RTRU topologies for performance enhancement and power electronics optimization are presented and discussed in brief.

Chapter 2: Three-Phase Six-Switch Boost-type Power Factor Correction (PFC) Converter for RTRU Applications: Control and Soft-switching

Typically, a RTRU is composed of a front-end AC-DC PFC stage followed by an isolated DC-DC stage [16]. Active PFC rectifier circuits are well suited for implementing a rectifier system with high power density, low weight and high input current quality. The active AC-DC rectifier topologies can be divided into phase-modular systems and direct three-phase rectifier systems. Phase modular systems consist of three single-phase rectifiers, each of which could be connected in Y (phase-neutral) or Δ (phase-phase) configuration. Compared to a direct three-phase rectifier system, due to power pulsation, large capacitors must be applied in the individual DC links of the modular systems for single-phase systems. Also, equal active power sharing between three different phase units must be ensured for suitable operation, which additionally requires a supervisory controller and identical hardware design for all three modules.

Direct three-phase rectifier circuits perform direct energy conversion from the three-phase AC-mains to a single DC-bus, where the DC link requirement goes down significantly under a symmetric balanced three-phase AC source. Three-phase active rectifier systems can be typically divided into three major categories- (i) boost-type PFC (ii) buck-type PFC and (iii) buck-boost-type PFC [16]. Buck-type PFC shows discontinuous input phase currents and therefore, requires an extremely challenging EMI filter to shape the grid current to meet all the individual harmonics limitations.

Furthermore, a considerable high differential mode (DM) capacitor is required to sink the discontinuous ripple current, which can potentially degrade the power factor in the wide-range of grid frequency (360Hz to 800Hz) operation. Therefore, buck-type PFCs do not seems suitable for airplane power supply applications with strict requirements on power quality. Similarly, buck-boost-type PFC faces the same issues of discontinuous input current and hence, requires higher DM capacitor degrading the power quality. Therefore, an AC-DC topology with continuous input current reduces the burden on EMI filter design and improves the input power factor due to less reactive power requirement by DM capacitors. This makes three-phase boost-derived power factor correction rectifier a suitable choice for active three-phase AC-DC conversion. The front-end PFC stage can be implemented by different boost-type topologies with different number of active devices; four-switch, three-switch and even single-switch converters. In four-switch topology, the two switches in one phase leg are replaced by two capacitors [17, 18]. In three-switch converter, also referred as 'Vienna Rectifier', each phase leg has bidirectional current flow by combination of a single switch and multiple diodes [19]. The main concern in these two topologies is the complicated controller design and the increased number of diodes in 'Vienna Rectifier', which could also result in more conduction loss especially at higher power. In single-switch topology, three-phase single-switch AC-DC boost converter is widely used for its simple control and no need for input current sensors [20]. But the phase currents typically contain low-frequency harmonic distortion, which applies additional burdens on EMI filter design. Therefore, three-phase six-switch boost-type PFC is selected in our design due to its simplified structure, less current stress, less number of

semiconductor devices and high conversion efficiency [21-22]. In the majority of applications, the input current of the active three-phase PFC rectifiers are required to have a total harmonic distortion (THD) less than 5% and an input power factor (PF) greater than 0.99 [22-23]. With the motivation of achieving fast dynamics, enhanced power quality, improved conversion efficiency for the front-end PFC stage, the following research areas are deeply investigated and analyzed in the following sections: (a) duty compensated feedback control for THD improvement (b) PFC control by using only one voltage sensor (c) fast start-up control with minimum inrush current (d) soft-switching implementation in a three-phase boost PFC.

2.1 Basic operation and design details

2.1.1 Operation Details

Prior to moving into the research contributions, the operation and design details are discussed in this section. The overall structure of a three-phase active boost-type rectifier is shown in Fig. 2.1. In this topology, there are three inductances in series with the AC source.

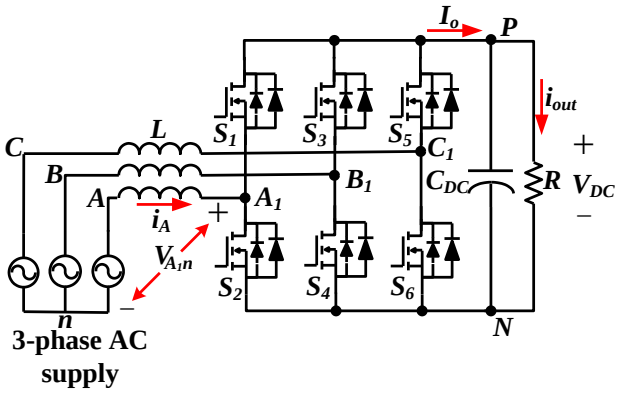


Fig. 2.1 Three-phase boost PFC rectifier

These inductances help to boost the input AC voltage and filter the input current, thus reducing the harmonic contents. The top and bottom set of MOSFETs are switched in a complementary fashion with a fixed deadband. The instantaneous DC link current can be formulated as the relationship, presented in Eq. (2.1).

$$S_A i_A + S_B i_B + S_C i_C = C_{DC} \frac{dV_{DC}}{dt} + \frac{V_{DC}}{R} \tag{2.1}$$

where S_A, S_B, S_C denote the PWM states (0 if OFF, 1 if ON) of high-side switches of phase *A*, *B*, *C*, respectively. Taking a switching average of the above relationship, Eq. (2.2)-(2.4) could be established for a better and clear understanding of the relationship between duty ratios and currents in a balanced 3-phase, active boost rectifier with open-neutral point i.e. $i_A+i_B+i_C=0$.

$$\frac{1}{T}\int_0^T (S_A i_A + S_B i_B + S_C i_C)dt = \frac{1}{T}\int_0^T \left(C_{DC} \frac{dV_{DC}}{dt} + \frac{V_{DC}}{R}\right) dt \tag{2.2}$$

Assuming V_{DC}, i_A, i_B, i_C to be constant over a switching cycle in Eq. (2.2), the following equations could be formulated.

$$d_{AH} i_A + d_{BH} i_B + d_{CH} i_C = \left(C_{DC} \frac{dV_{DC}}{dt} + \frac{V_{DC}}{R}\right) \tag{2.3}$$

$$(d_{AH} - d_{CH}) i_A + (d_{BH} - d_{CH}) i_B = C_{DC} \frac{V_{DC}(n) - V_{DC}(n-1)}{T_s} + \frac{V_{DC}(n)}{R} \tag{2.4}$$

where, d_{kH} and d_{kL} represent the duty ratios of high side and low side MOSFETs, respectively of '*k*'th phase ('*k*' is *A* or *B* or *C*). i_k denotes the instantaneous current through '*k*'th phase inductor ('*k*' is *A* or *B* or *C*). C_{DC}, V_{DC} and I_o denotes the output capacitor, DC link voltage and average DC link current, respectively. Eq. (2.3) is obtained by discretizing Eq. (2.2) in sample domain.

2.1.2 Design details

Three phase active boost PFC requires various components starting from power stage passive components like inductor, capacitor, and power diodes to the active devices like MOSFETs, drivers, and their power supply, among others. Front end power stage of boost PFC requires three inductors, one DC link capacitor, six power diodes, six power MOSFETs. Apart from the power stage components, a set of five sensors (two line voltages, two line currents, one output voltage) along with sensing circuits is required.

The converter is designed for nominal input voltage of 230V (phase-neutral RMS), 400 Hz and rated power of 6 kW. The minimum DC link voltage must be greater than line-line peak voltage corresponding to maximum AC input voltage i.e. $V_{DC} > V_{LL,max}\sqrt{2} = 260\sqrt{6} = 640V$. In this design, DC link voltage is kept at 650V. Since maximum voltage stress across each PFC MOSFET is DC link voltage i.e. 650V, three-pairs of 1200V SiC MOSFETs are selected in this design. The effective RMS current stress of each switch can be determined as:

$$I_{RMS} = I_a \sqrt{\frac{4\pi + \sqrt{3}(3 + 4M)}{24\pi}} \tag{2.5}$$

where, I_a is the 'A' phase RMS current and 'M' is the modulation index, given by $M = V_{LL}\sqrt{3}/V_{DC}$. Fast Schottky SiC diodes are placed antiparallel to the six PFC MOSFETs, in order to minimize the reverse recovery, to offer less forward voltage drop and hence, result in less conduction loss. The diodes will conduct only during the deadband interval, which is ~5% of a switching cycle in our design. Therefore, a conservative current rating of each diode could be considered as 5% of phase current RMS, which is ~1A at 100% overload condition. Each MOSFET needs to be driven through a gate

driver, whose output side must be electrically isolated from the DSP ground. Considering the propagation delay, driving voltage, isolation level and maximum current delivering capability, Si82391AD is found as a good choice of gate driver, being able to isolate the gate pulse inductively (through transformer) from DSP and to drive a pair of complementary MOSFETs.

The DC link capacitor needs to be large enough to suppress the voltage ripple (as low as 2% (Δ_v) of minimum DC link voltage ($V_{o,min}$)), caused by switching frequency component and this is formulated in Eq. (2.6). Also, assuming no requirement for hold-up time, the DC link capacitance value can be set at 100 µF according to the following equation.

$$C_{DC} = \frac{P_{o,max}}{\Delta_v 2\pi f_{sw} V_{o,min}^2} \tag{2.6}$$

Contextually, it is noteworthy to mention that there persists no line frequency multiple component on the DC link voltage in case of a balanced three-phase boost PFC unlike single phase PFC converter. This can be simply proved by formulating the total power delivered from source to load as follows, which does not include any multiple of ω_g.

$$P_{delivered} = V_{An}i_A + V_{Bn}i_B + V_{Cn}i_C = VI\left[\sin^2(\omega_g t) + \sin^2\left(\omega_g t - {}^{2\pi}/_{3}\right) + \sin^2\left(\omega_g t + {}^{2\pi}/_{3}\right)\right] = \frac{3}{2}VI \tag{2.7}$$

The value of selected boost inductance is of 400µH, which is required per phase to limit the maximum possible ripple amount within 5% of RMS magnitude of inductor current [23]. C058110A2 core (from Magnetics) with high-flux material is selected for building the boost inductors, considering the balance between permeability degradation with higher power and core loss. A list of components with brief specifications used in the PFC stage is summarized in Table 2.1.

Table 2. 1. Component counts and specifications

Components	Part number	Quantity	Purpose
Gate driver	SI82391AD	3	Driving MOSFETs
DC-DC converters	NMG1515SC (Murata)	8	Isolated power supply to gate drivers
MOSFETs	CMF10120D (Cree)	10	Active semiconductors
Diodes	C2D05120A (Cree)	10	Passive semiconductors
DC link capacitors	B32776G0206K (20µF)	6	PFC output capacitor
Current sensors	LA55 (LEM Inc.)	3	Sensing input line currents
15-5 V	TPS71550DCKR	5	Gate driver primary side supply
Zener diode	1SMA12AT3G	20	Protection from voltage surge
Chip Inductor	820nH (MLP2012SR82T)	50	Filtering action
Common mode choke	ACM90V-701-2PL-TL00	10	Filtering of SMPC converters

2.2 Duty compensated feedback control of three-phase boost PFC

In three-phase AC-DC boost PFC structure, there exists a floating potential (V_{nN}) between source neutral and DC link negative terminal, which sets a challenge in maintaining a higher power quality in a three-phase boost PFC without sensing the voltage V_{nN}. This becomes even more challenging if there is no available access to the source neutral of three-phase generator, which is the case in the auxiliary power units of more electric airplanes. Traditionally, the average current control of the three-phase six-switch boost PFC rectifier has been digitally implemented using three independent current controllers with a common triangular carrier [24-25]. However, the dynamics of the reference duty ratios in a three-phase boost PFC are not actually independent. In fact, there are cross-coupled terms in their relationships due to the common-mode potential between source neutral and DC link negative terminal, as established in this research document. Therefore, the input current waveforms obtained from the control method, presented in [24-25], have high THDs, degrading the power quality.

As an alternative option, vector control method using space vector PWM (SVPWM) technique is often used in a six-switch boost PFC rectifier for reducing the total number of switching transitions in a switching cycle to improve the THD and enhance the conversion efficiency [26]. However, higher execution time, due to computationally complex procedure of sector determination and duty calculation in vector control, limits the maximum switching frequency. Similar complexity also arises for sliding mode control using a single core DSP-based implementation [27]. Furthermore, a zero-sequence-signal (ZSS) injection method with three-step and six-step PWM has been proposed in [29], which adds up an additional feedforward term,

derived from input voltage to the current loop compensators' outputs. However, the three-step PWM is adversely affected by duty-cycle limitations and has unbalanced conduction losses between the upper and lower switches of the three-phase rectifier bridge. Moreover, an input phase voltage duty-feed-forward control strategy is proposed in [30], for improving the zero crossing issues and power quality in a single-phase boost PFC.

Therefore, by addressing the aforementioned issues, this section presents a duty compensated feedforward control strategy capable of ensuring a lower THD and a power quality comparable to SVPWM based vector control or the methods proposed in [29-30], which is done by injection of a common-mode duty ratio term to each current compensator's output with an additional advantage of eliminating two input voltage sensors. Unlike [29-30], this duty compensation term is not a function of input voltages, rather a function of duty ratios at the preceding switching cycle. The proof, detailed derivation, and its influence in terms of harmonics reduction are analytically presented and justified in subsection 2.2.1.

2.2.1 Plant characteristics and small signal analyses

For PFC operation, the reference reactive power in a three-phase active boost rectifier should be set to zero and active power should be set to the total nominal power of the converter. In a Sine-PWM method, inner current loop consists of three lines current references, which are functions of voltage-loop PI controller output and line voltages. Hence, power factor correction requires feedback and regulation of the three phase input currents and is achieved through inner loop current mode control. Current control is achieved using an inner control loop that measures the input phase currents

and controls the inductor-neutral voltages (V_{A1n}, V_{B1n}, V_{C1n}), to force the phase current to track its reference value. In our work, a linear control strategy, combining feedback and feedforward controllers with injection of a compensation duty factor and without using any input voltage sensors, has been proposed and implemented. The proposed control structure is shown in Fig. 2.2.

A three-phase boost PFC consists of three coupled AC-DC boost converters, one of which is shown in Fig. 2.3 [30]. According to Fig. 2.3, the output and input voltages of the converter are V_{DC} and V_{AN}, respectively. From the volt-second balance of the boost inductor L for 'k'th phase, Eq. (2.8) could be formulated.

$$V_{kN} = (1-d_{kL})V_{DC} = d_{kH}V_{DC} \tag{2.8}$$

V_{A1N} could be 0 or V_{DC}, depending upon whether lower leg switch S_2 is ON or OFF, respectively. Therefore, the switching average of the voltage across the leg-midpoint if 'k'th phase to the negative terminal of DC link i.e. V_{i1N} would be $d_{kH}V_{DC}$. Hence, Eq. (2.9) could be formulated for any decoupled AC-DC converter. Let's assume the estimated input phase voltages are ($\tilde{V}_{An}, \tilde{V}_{Bn}\ \tilde{V}_{Cn}$) for phase A, B and C, respectively.

$$\tilde{V}_{An} + V_{nN} = L\frac{di_k}{dt} + d_{kH}V_{DC} \tag{2.9}$$

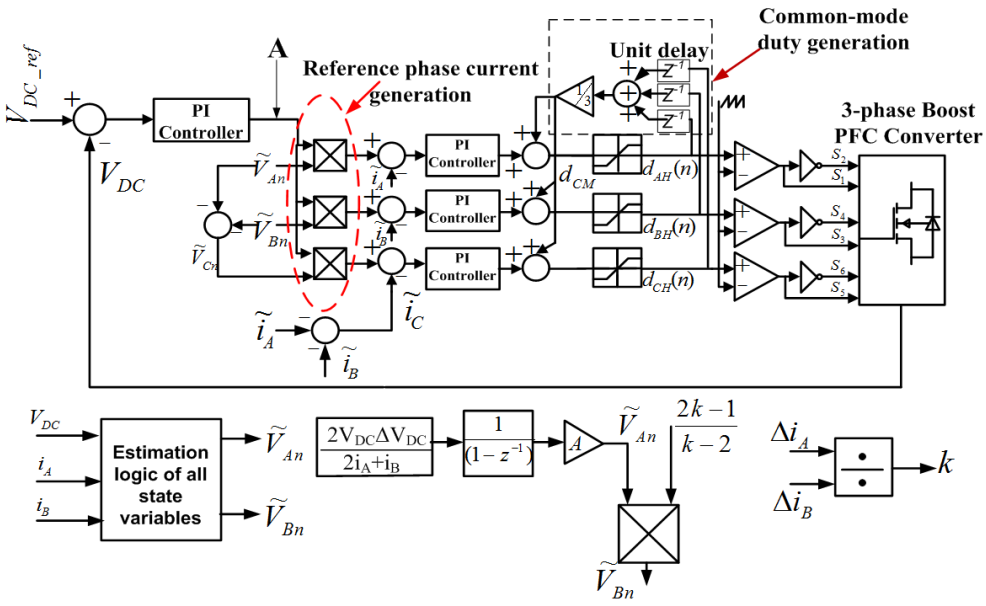


Fig. 2.2. Block diagram of the proposed control system for a three-phase active boost rectifier

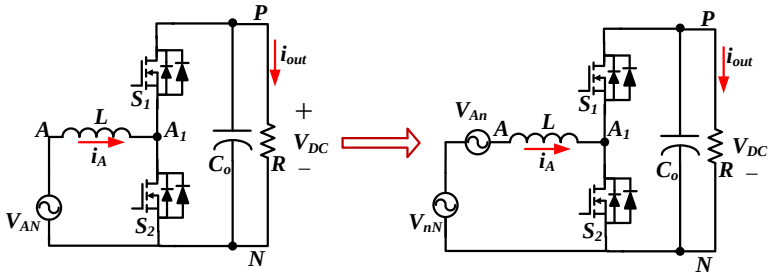


Fig. 2.3. One independent leg of a three-phase active boost-type rectifier.

Applying summation operator to both sides of Eq. (2.8) and by varying phase '*k*' from *A* to *C*, the subsequent relationships are formed for a balanced three-phase system i.e. $V_{An}+V_{Bn}+V_{Cn}=0$.

$$(\tilde{V}_{An}+\tilde{V}_{Bn}+\tilde{V}_{Cn})+3V_{nN}=L\frac{d}{dt}(\sum_{k=A}^{C}i_k)+V_{DC}\sum_{i=A}^{C}d_{iH} \tag{2.10}$$

$$V_{nN}=\frac{L\frac{d}{dt}(\sum_{k=A}^{C}i_k)+V_{DC}\sum_{i=A}^{C}d_{iH}}{3}=\frac{\sum_{k=A}^{C}V_{L,k}+V_{DC}\sum_{i=A}^{C}d_{iH}}{3} \tag{2.11}$$

The inductor voltages can be written as the sum of its different frequency components, as presented in Eq. (2.12).

$$\sum_{k=A}^{C} V_{L,k} = \sum_{\substack{n=2m+1 \\ m\geq 1}} V_{L,n}[\cos(n\omega t) + \cos(n(\omega t - 2\pi/3)) + \cos(n(\omega t + 2\pi/3))] = 3V_{L,3}\cos(3\omega t) + \sum_{h=5,7,..} V_{L,h} \tag{2.12}$$

where, $V_{L,h}$ denotes the 'h'th order harmonics of any phase inductor voltage. In a conventional linear feedback-only control with Sine-PWM technique, the instantaneous sum of all the duty modulation signals, generated from three outputs of inner loop current compensators have 120^o phase difference and hence, add up to zero. Therefore, as can be seen from Eq. (2.11), the sum of three inductor phase voltages will depend only on V_{nN}, the voltage between input AC neutral and DC negative terminal, which is non-zero for a three-phase boost PFC converter, shown in Eq. (2.13). This implies that although the sum of all the inductor voltage fundamentals will be 0, there will be non-zero third and higher order harmonics present in the inductor voltage, which will definitely be present in the input currents as well.

$$3V_{nN} = V_{L,3}\cos(3\omega t) + \sum_{h=5,7,..} V_{L,h} \tag{2.13}$$

Therefore, in order to eliminate the undesired third and higher-order odd harmonics from the inductor current and inductor voltage waveforms, an additional duty ratio of 'x' needs to be added to each of the current loop compensators' outputs, which can potentially cancel the effect of V_{nN} on the input line currents and inductor voltages. As can be seen from Eq. (2.11), for a balanced 3-phase system with input currents without any harmonics, V_{nN} can be presented as,

$$V_{nN} = V_{DC}(d_{AH}+d_{BH}+d_{CH})/3 \tag{2.14}$$

Therefore, since the sum of the three current compensators' outputs is zero due to 120° mutual phase shift, as a result of the common-mode duty ratio injection, the following relationship holds.

$$3xV_{DC} + \sum_{k=A}^{C} V_{L,k} = 3V_{nN} \tag{2.15}$$

Hence, in order to make the individual inductor voltage harmonics and input current harmonics equal to zero, the value of 'x' should be V_{nN}/V_{DC}, i.e. $x=(d_{AH}+d_{BH}+d_{CH})/3$. Thus, the modified reference duty ratio of any switch by proposed control could be derived in discrete time domain according to Eq. (2.16):

$$d_{kH}[n] = \frac{\tilde{V}_{kn} + V_{nN}[n]}{V_{DC\_ref}} = K\sin(\omega t) + \frac{\sum_{k=A,B,C} d_{kH}[n-1]}{3}\frac{V_{DC}}{V_{DC\_ref}} \tag{2.16}$$

Thus, the reference duty ratios for each phase are obtained by the following relationships in discrete time domain with sampling time T_s and presented in Eq. (2.17) to Eq. (2.19).

$$d_{AH}[n] = K_1\sin(\omega n T_s) + \frac{d_{AH}[n-1]+d_{BH}[n-1]+d_{CH}[n-1]}{3}\frac{V_{DC}}{V_{DC\_ref}} \tag{2.17}$$

$$d_{BH}[n] = K_2\sin(\omega n T_s - \frac{2\pi}{3}) + \frac{d_{AH}[n-1]+d_{BH}[n-1]+d_{CH}[n-1]}{3}\frac{V_{DC}}{V_{DC\_ref}} \tag{2.18}$$

$$d_{CH}[n] = K_3\sin(\omega n T_s + \frac{2\pi}{3}) + \frac{d_{AH}[n-1]+d_{BH}[n-1]+d_{CH}[n-1]}{3}\frac{V_{DC}}{V_{DC\_ref}} \tag{2.19}$$

Second term in Eq. (2.17) to Eq. (2.19) represents the additional term, derived as zero sequence or common mode duty injection to each individual phase-current controller output. Since, V_{nN} is the common additional term to be added to all three phase voltages to form V_{AN}, V_{BN}, V_{CN}; ignoring the effect of this common-mode potential on the duty

reference generation would keep high amount of harmonics uncompensated in the switching PWM pattern in duty waveform. Hence, the input phase current would have contained all the harmonics present in the V_{Nn} waveform, presented in Eq. (2.12). Therefore, using Eq. (2.15), the additional duty feedforward term (x) is derived and used in Eq. (2.17)-Eq. (2.19) in order to nullify the effect of common-mode potential V_{Nn}. In order to get a better insight, the effects of considering or ignoring this additional term in the control loop on the input current harmonics are presented in Section 2.2.2 on Simulation and Experimental results.

Applying perturbations on duty ratios on both sides of Eq. (2.17), discarding other variables' small signal variations and taking 'z'-transform, the following small signal relationship is obtained between cross-duty-ratio terms.

$$\frac{\Delta d_{AH}(z)}{\Delta d_{BH}(z)} = \frac{rz^{-1}/3}{1 - rz^{-1}/3} = \frac{rz^{-1}}{3 - rz^{-1}} \tag{2.20}$$

where, 'r' represents the ratio between measured DC link voltage and its reference value, which could vary between 0 and $1+h$, where 'h' will determine the amount of DC voltage overshoot. Also, taking 'z' transform on the perturbed duty ratios in Eq. (2.16) and discarding the small-signal variation of phase voltage and DC output voltage, the following is obtained.

$$\Delta d_{AH}(z)[1 - \frac{rz^{-1}}{3}] = \frac{rz^{-1}}{3}[\Delta d_{BH}(z) + \Delta d_{CH}(z)] \tag{2.21}$$

Converting the relationship in Eq. (2.20) to Laplace domain through bilinear transformation, Eq. (2.22) is formulated, which provides the relative variation of duty ratios of different phases.

$$\frac{\Delta d_{AH}(s)}{\Delta d_{BH}(s)} = \frac{r\dfrac{1-sT/2}{1+sT/2}}{3-r\dfrac{1-sT/2}{1+sT/2}} = \frac{(r+1)+(r-1)sT/2}{(3-r)+(3+r)sT/2} \tag{2.22}$$

The pole being located at *p=-2(3-r)/(3+r)* i.e. left half plane ensures the cross-duty variation to be stable at a perturbation in any phase duty ratio. This inter-phase cross-coupling makes the input phase-neutral voltage not only a function of its corresponding duty ratio, but also cross-coupled with other phase-duty ratios, demonstrated by Eq. (2.23).

$$\tilde{V}_{An}(n) = L\frac{i_A[n]-i_A[n-1]}{T_s} + V_{DC}\left(d_{AH}[n] - \frac{\sum_{i=A}^{C} d_{iH}[n-1]}{3}\right) \tag{2.23}$$

Applying perturbations on the phase current and the duty ratios in Eq. (2.23), and taking the '*z*' transform, Eq. (2.24) is obtained.

$$-\frac{L}{T_s}(1-z^{-1})\Delta i_A(z) = V_{DC}\left[\left(1-\frac{z^{-1}}{3}\right)\Delta d_{AH}(z) - z^{-1}(\Delta d_{BH}(z)+\Delta d_{CH}(z))\right] \tag{2.24}$$

Now, using Eq. (2.21) and Eq. (2.24), and applying bilinear transformation, the self-transfer function ($T_{self}(s)$) of the phase current-to-duty ratio, shown in Eq. (2.25) is determined.

$$T_{self}(s) = \frac{\Delta i_A(s)}{\Delta d_{AH}(s)} = \frac{4V_{DC}[(1-r)+sT]}{3Ls[(r+1)+(r-1)sT/2]} \tag{2.25}$$

Using a similar method, the cross transfer function ($T_{cross}(s)$) of phase current-to-duty ratio, in Eq. (2.26) is derived.

$$T_{cross}(s) = \frac{\Delta i_A(s)}{\Delta d_{BH}(s)} = \frac{4V_{DC}[(1-r)+sT]}{3Ls[(3-r)+(3+r)sT/2]} \tag{2.26}$$

The self and cross transfer functions characterize the plant and thus, will be used in closed loop stability analyses. The cross-coupling effect, presented by the transfer function at Eq. (2.26) is stabilized by the addition of the common-mode or zero-sequence duty ratio term to each of the individual phase duty ratios, shown in Eq. (2.17) - Eq. (2.19). Furthermore, it is important to ensure stability of the overall loop by choosing proper controller parameters. For example, in order to design '*A*' phase current compensator ($C_A(s)$), the unity loop gain needs to be ensured. For a plant transfer function of $G_A(s)$, shown in Eq. (2.27), $1+C_A(s)G_A(s)<0$ should necessarily hold.

$$G_A(s) = \frac{\Delta i_A(s)}{\Delta d_{AH}(s)} = \frac{4V_{DC}[(1-r)+sT]}{3Ls[(r+1)+(r-1)sT/2]} = \frac{H(s+z)}{s(s+p)} \tag{2.27}$$

In the above equation, $H=8V_{DC}/(3L(r-1))$, $z=(1-r)/T$, $p=2(r+1)/(T(r-1))$. 'r' can vary from 0 to $1+h$, depending on the DC link voltage value and 'h' will determine the maximum ripple on the DC link nominal value. The characteristic equation of the overall loop gain is presented in Eq. (2.28).

$$s^3 + (k_p H + p)s^2 + (k_i + k_p z)Hs + k_i Hz = 0 \tag{2.28}$$

From Routh-Hurwitz stability criterion [24], the following conditions on the controller parameters are obtained for the stability of the overall closed loop system and the closed current loop bode plot is presented in Fig. 2.4, which exhibits a phase margin of 120^o and unity power factor.

$$k_p > \frac{-P}{H} = -\frac{3L(r+1)}{4TV_{DC}} \tag{2.29}$$

$$k_i > \frac{k_p z}{k_p Hz + pz - 1} \tag{2.30}$$

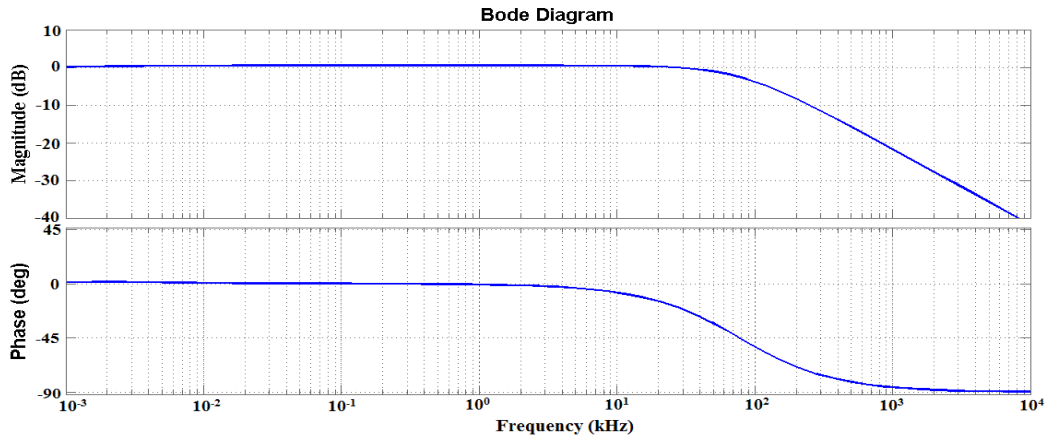


Fig. 2.4. Bode plot of closed loop system response

PI compensators for all the phase currents are designed by obeying the above inequalities. Final duty ratios are obtained by adding inner loop current controller outputs to the additional common mode duty ratio. Duty ratios obtained from the inner current controller loops are compared with a high frequency carrier wave to generate a switching PWM pattern to be fed to the top side MOSFETs.

2.2.2 Simulation and Experimental Results

Simulation results:

The converter is simulated with an input AC voltage of 230V (phase-neutral RMS) at 400 Hz. The simulations are carried out in MATLAB-Simulink at the rated nominal specifications, prior to the real-time implementation. Fig. 2.5 shows the simulation results of a 10-kW PFC converter with conventional averaged current mode control without any feed-forward duty term in the control loop.

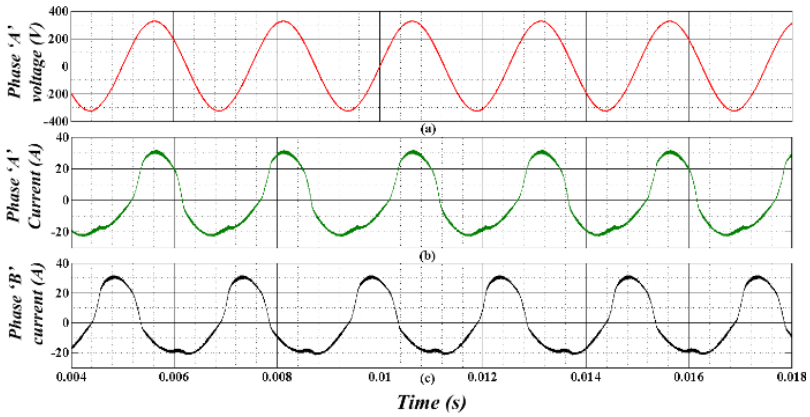


Fig. 2.5. Simulation results of three-phase boost PFC at 10kW power with averaged-current mode control (without any additional duty compensation).

Fig. 2.6 demonstrates the simulation results of the 10-kW PFC converter with the injection of common mode duty ratio compensation term, derived from the proposed control in this research document. The input current waveforms according to conventional averaged current mode control have high amount of harmonics content (THD of 30%), as opposed to the proposed feed-forward based control, offering THD of 3.4%.

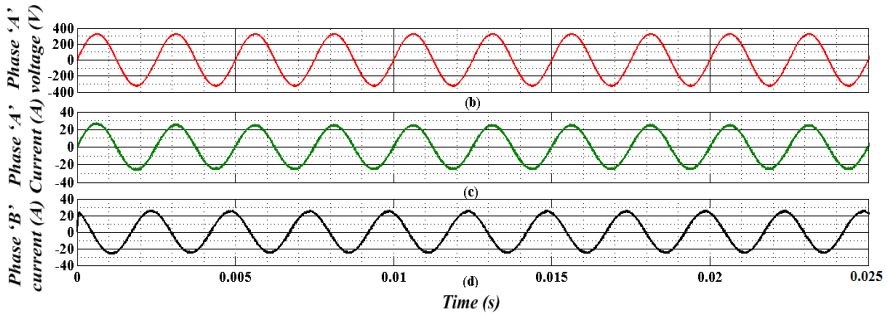


Fig. 2.6. Simulation results of three-phase boost PFC at 10kW power with the proposed control (with injection of common-mode duty ratio).

For a better understanding of the harmonics effect on the phase current in two different control methods, a FFT plot is presented in Fig. 2.7, which clearly implies that the

power spectral density (|FFT(i_A)|2/N, where N is the transform length), at lower order harmonics is far less in the proposed control.

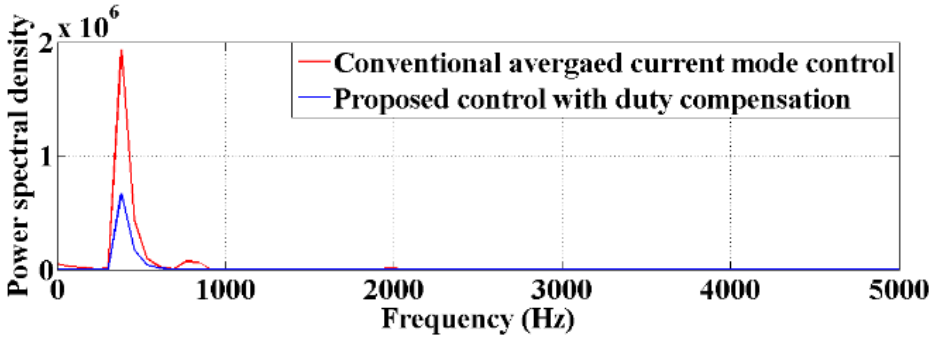


Fig. 2.7. FFT plot of the phase 'A' current at two different control methods

Experimental results:

As a proof-of-concept verification of the operation of three-phase active boost rectifier with the proposed control logic, a 6 kW (continuous) / 10kW (peak power) laboratory prototype is built according to the key nominal specifications, presented in Table 2.2. The designed prototype is shown in Fig. 2.8.

Table 2.2. Key design specifications of the PFC converter

Parameters	Specifications
Input voltage (V_{in})	230V, 400Hz (nominal)
Output voltage reference (V_{DC_ref})	650V (nominal)
Output continuous/peak power (P_{out})	6kW/10kW (max.)
Switching frequency (f_s)	100 kHz
Boost inductor (L)	400µH
DC link capacitor	100µF
MOSFETs	CMF10120D (SiC, 1.2kV)

The converter is capable of converting 190V-260V three-phase AC-line voltages into a regulated DC-link voltage in the range of 300V to 650V. In order to have advantages

in complying with the conducted EMI standard (DO160F), the switching frequency is selected at 100 kHz. The control logic is implemented in a DSP TMS320F28335 with the PI parameters (K_p=1.5, K_i = 100), derived by satisfying the inequalities in Eq. (49-50). Fig. 2.9 shows the steady state operation of the PFC converter at 6kW and represents the stable and settled down output DC link voltage of the PFC.

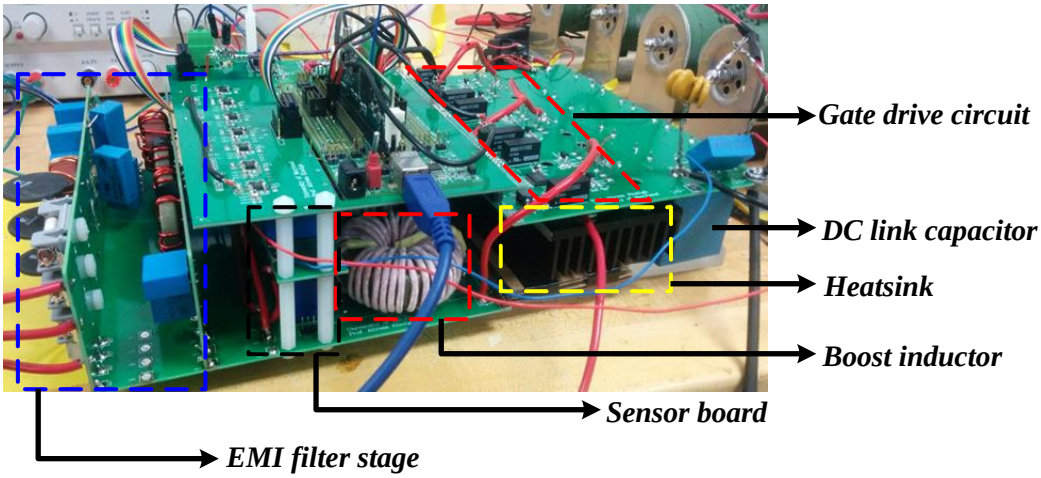
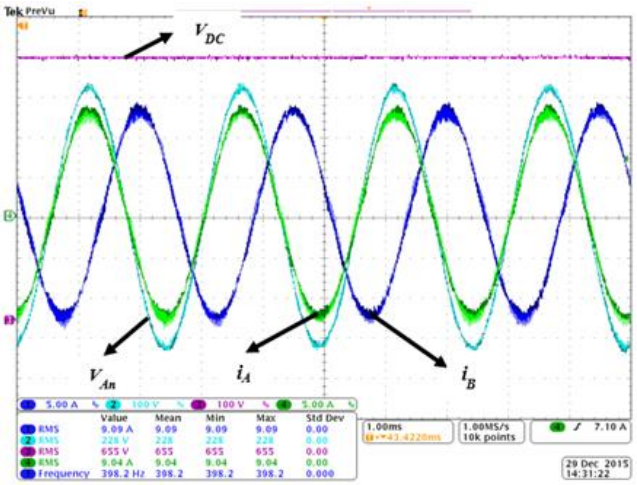
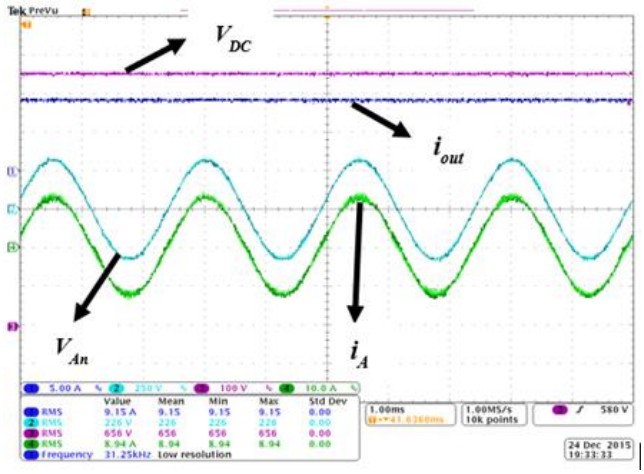


Fig. 2.8. Photo of the three-phase boost PFC prototype.



(a)V_{DC}=650V, i_A (RMS) =i_B (RMS) =9.06A, V_{An} (RMS) =230V, P_{out}=6kW



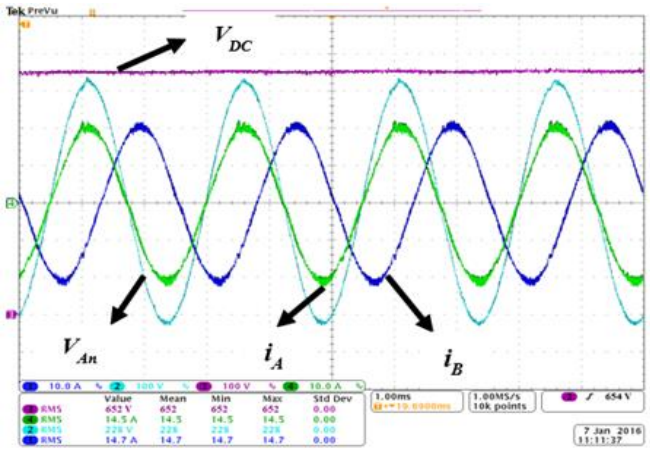
(b) V_{DC}=650V, i_{out}=9.15A, i_A (RMS) =9A, V_{An} (RMS) =230V, P_{out}=6kW

Fig. 2.9. Experimental waveforms (at 400Hz. source frequency) of the converter at 6kW (a) Phase 'A' voltage and current, Phase 'B' current, DC link voltage; (b) Phase 'A' voltage & current, DC link voltage & load current

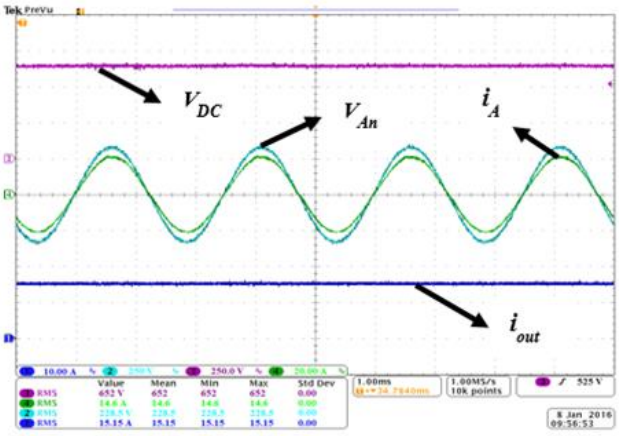
The DC link voltage is regulated at 650V with a ripple of ±1% (7V), as implied by Fig. 2.9(a). Fig. 2.9(b) shows the load voltage along with load current for a more accurate calculation of output power, as the load resistance value may not be accurate because of temperature rise in continuous run of the circuit. Fig. 2.9(b) clearly demonstrates the unity power factor operation of the converter, as the input phase 'A' current and voltage are exactly in phase. The experimental result at 6kW exhibits a conversion efficiency of 98.4% and a THD of 4.1%, which proves the operation of power converter with a very good power quality.

Fig. 2.10(a) and Fig. 2.10(b) show measurement results at a line frequency of 400 Hz and an output power of Pout = 9.8 kW (V_{in}=230V RMS, V_{DCref}=650V), where a conversion efficiency of 98.2% and THD of 4.1% are measured. In addition to the operation of the converter at 400 Hz, experiments are also conducted at intermediate frequencies as the rectifier stage of RTRU should maintain PFC operation in a wide

variable range of source frequencies (360-800 Hz). Fig. 2.11 represents the experimental waveforms of the converter at 120V RMS input voltage and 400V output voltage reference at source frequency of 800Hz with 2.1 kW load power.



(a) V_{DC}=652V, i_A (RMS) =i_B (RMS)=14.6A, V_{An} (RMS) =230V, P_{out}=9.8kW



(b) V_{DC}=650V, i_{out}=15.15A, i_A(RMS)=14.6A, V_{An}(RMS)=230V, P_{out}=9.8kW

Fig. 2.10. Experimental waveforms of the converter at 10kW (a) Phase 'A' voltage and current, Phase 'B' current, DC link voltage; (b) Phase 'A' voltage & current, DC link voltage & load current.

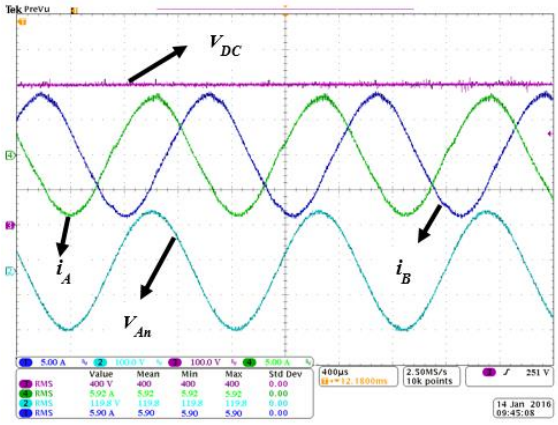


Fig. 2.11. Experimental waveforms of the converter at 800Hz source frequency & 2.1kW load power V_{DC}=400V, i_A (RMS) =i_B (RMS) =5.92A, V_{An} (RMS) =120V, P_{out}=2.1kW.

The measurements at 800Hz source frequency convey a power factor of 0.999, efficiency of 98.5%, THD of 4.2% and also, exhibits a tight regulation of the DC link voltage (ripple < ±1%) with the proposed control. As can be seen from the input current waveforms in the above experimental results, the zero-crossing portion is totally distortion free and overall THD is below 4.5% at all power levels, which demonstrates a good agreement between the experimental results and the theoretical claims. THD obtained from our proposed control is slightly better than three-step PWM duty feedforward (derived from input voltages) approach in [29] with an additional benefit of having no effect on power quality with changing the duty ratio limit or facing source disturbance, unlike the method in [29].

In addition, the converter is also tested in different line conditions to check the accuracy of the proposed control logic at variable operating conditions. During a 25% overvoltage line transient (from 210V to 265V phase-neutral RMS) applied at the input phase voltage, shown in Fig. 2.12, the proposed controller maintains the stability of the closed-loop system with input power factor of 0.997 and a settling time of 0.18ms for

DC link voltage. The phase current amplitude reduces by 20% after the input line overvoltage, as the load power is kept unchanged.

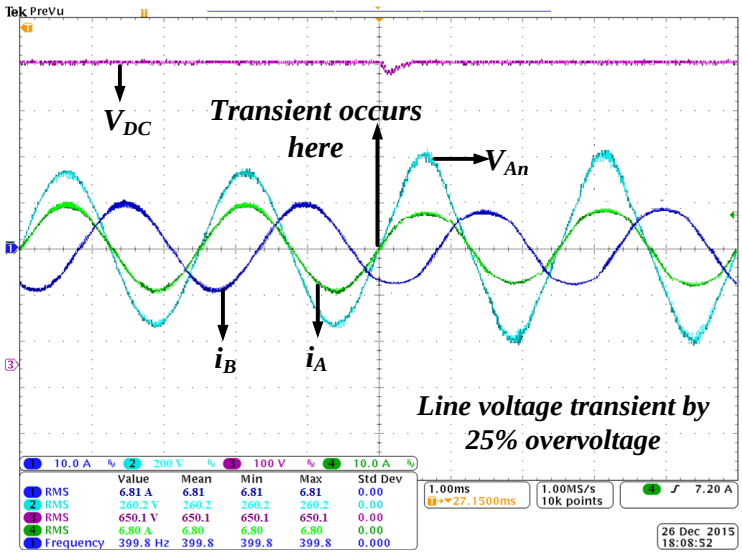


Fig. 2.12. Experimental waveforms of the converter under input line transient from 230V to 285V phase-neutral RMS at 400Hz source frequency and V_{DC}=650V.

Furthermore, the converter is tested with the variation in source frequency from 400Hz to 800Hz at the rated input voltage, and as can be seen from the experimental results in Fig. 2.13, the controller maintains the stable and regulated converter operation with the PF of 0.999 and THD of 4.2% both before and after the frequency transient with a fixed DC link of 650V.

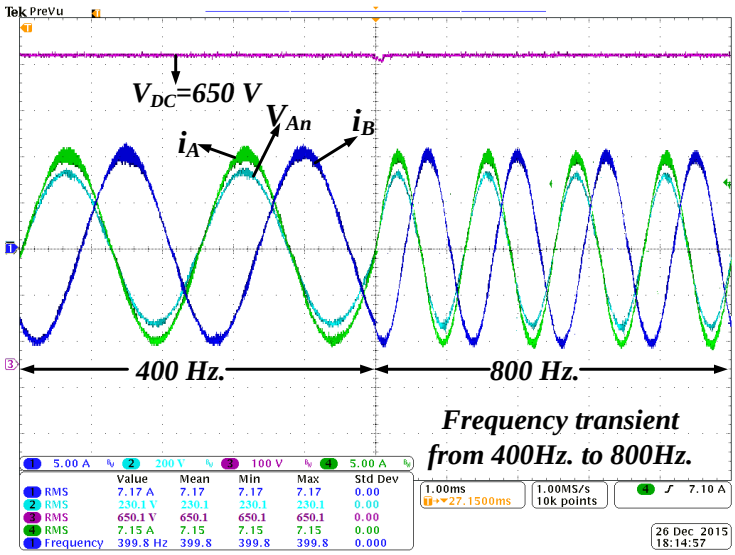


Fig. 2.13. Experimental waveforms of the converter under input frequency transient from 400Hz to 800 Hz at 230V phase-neutral RMS and V_{DC}=650V.

2.2.3 Loss Evaluation of the PFC Converter

Power losses in power stage components arise from boost inductors (magnetic core loss and DC conduction loss) and ESR loss in DC link capacitors. Switching and conduction loss in MOSFETs, forward conduction losses in diodes add up to calculate the total semiconductor losses, incurred in the PFC converter. According to the calculations of loss data using the governing relationships mentioned in [16], the switching, conduction and diode losses are 53.3W, 41W, and 40W, respectively at 10kW PFC operation. The total incurred DC conduction loss in all the power inductors is 18.3W. In our design, the total calculated magnetic core loss in three power inductors is 15W, obtained from Eq. (2.31) at a PFC operation with 10kW load power. Core loss density (P_{core}) is a function of AC flux swing (B_{pk}) and frequency (f), shown in Eq. (2.31). The parameters (k, a, b) and flux density (B), core volume (V_{core}) can be determined from core loss charts, datasheets and the curve fit loss equation [32].

$$P_{core} = kf^{a} B_{pk}{}^{b} V_{core} \tag{2.31}$$

The RMS value of ripple current through DC link capacitor and ESR loss (P_{ESR}) are calculated from Eq. (2.32) and Eq. (2.33).

$$i_{Co} = d_A i_A + d_B i_B + d_C i_C - \frac{V_{DC}}{R} \tag{2.32}$$

$$P_{ESR} = i_{Co}{}^{2} \times ESR \tag{2.33}$$

According to Eq. (2.32), RMS ripple current through DC link capacitor is 16A, which will lead to 2W of ESR loss per each of the five parallel 20µF capacitors. Thus, total theoretically calculated power loss in the combined EMI & PFC circuit is 182.6W at 10kW load power and hence, it would lead to a theoretical efficiency of 98.2%. A linearly extrapolated graph demonstrating the conversion efficiency variation of PFC over a wide range of load power (from 200W to 10kW) is shown in Fig. 2.14 (a), which confirms that the efficiency is always above 98% at a load power between 1kW and 10kW. The fall of efficiency beyond a certain power level is due to the significant conduction loss in three inductors, varying proportional to the square of load power. Furthermore, the loss split at the peak power of 10kW is represented using a pie chart in Fig. 2.14 (b).

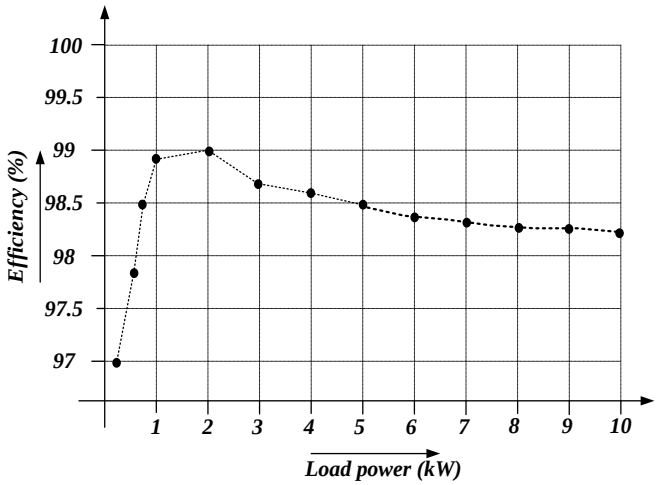


Fig. 2.14. (a) Efficiency of the three-phase boost PFC versus output power (kW).

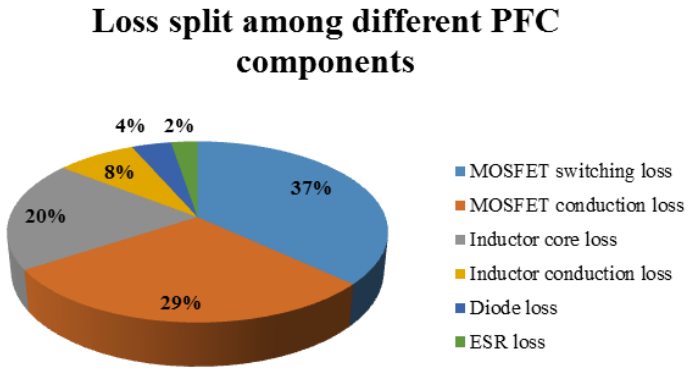


Fig. 2.14. (b) Power loss split in different components.

According to the obtained measurements over a wide range of load power (1-10kW), the high-end efficiencies and low THD enable the converter to achieve high power density and high gravimetric power density of 1.1 kW/liter with a total volume of 274 $inch^3$. As another evaluation parameter, harmonics of the input current are calculated by Fourier analysis of the measured current waveform till 30^{th} order and shown in Fig. 2.15.

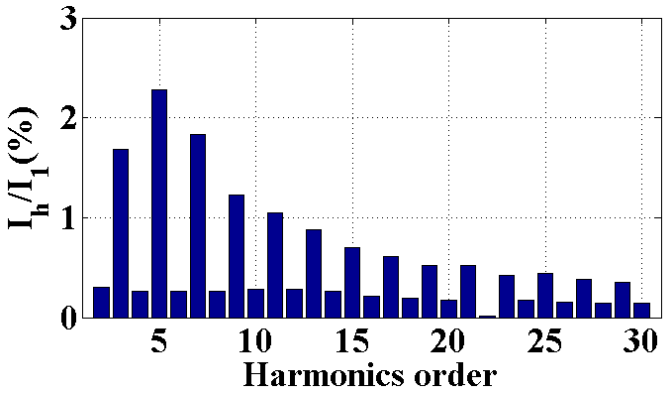


Fig. 2.15. Harmonic spectrum of phase current at rated input and 10kW load power

The harmonics content is quantified by the ratio between RMS current value at a specific harmonic frequency (I_h) and its fundamental root-mean-square (RMS) value (I_1). To keep the carrier frequency outside the dominant harmonic frequency band for improving THD, a switching frequency of 100 kHz is used such that the carrier harmonics are above the 125^{th} harmonic under 800 Hz line.

In addition to the improvement of power quality for three-phase PFC, it is also very important to maintain a consistently high efficiency throughout the load power range. Since three-phase boost PFC is inherently a hard-switched converter, there is a scope for bringing in soft-switching technique and thereby, being able to switch at a higher frequency without increase switching loss. The next subsection analyzes and explains about the methods of soft-switching implementation with minimum number of extra add-on components.

2.3 A Soft-Switching Strategy for Three-Phase Boost PFC

Keeping the objective of improving the conversion efficiency, it is very important to analyze the loss breakdown of the entire system into component level. It is noticed from the experimental measurements that a significant portion of the total losses in a hard-

switched converter such as a PFC arises from the switching loss. Additionally, the anti-parallel diodes of the six switches face reverse recovery problems, which cause high di/dt, common-mode (CM) conducted EMI noise and also, reduction in conversion efficiency. In order to alleviate the aforementioned problems with hard-switched PFC converter, several soft-switching techniques have been proposed either by modifying the control and PWM logic or by adding an additional auxiliary circuit. The auxiliary commutated resonant pole converter [78] can operate with ZVS using an additional auxiliary circuit. However, the auxiliary circuit uses six additional switches and their corresponding gate drivers, which would increase the overhead cost of the system. The concept of resonant DC link (RDCL) [79-80] makes the auxiliary resonant circuit relatively simpler, but the design requires an auxiliary switch with high voltage rating. In addition, ZVS operation of switches with the RDCL concept requires a discrete pulse width modulation (DPWM) strategy [81], which can potentially cause low frequency sub-harmonic oscillations, degrading the overall EMI response. Another soft-switching approach is presented in [82], which makes use of the transformer leakage inductance and a separate resonant capacitor to achieve ZVS. However, one major disadvantage of this topology is the higher current stress on each switch in the matrix converter, as the current flowing through each switch in the switching instant could be as high as double of the rated current.

An effective soft-switching implementation is performed in [83-84], which utilizes transformer leakage inductance, parasitic capacitances of the MOSFETs, and also enables utilization of MOSFET body diodes instead of additional fast recovery diodes. However, due to the topological constraints, this is not applicable to the three-phase

boost PFC. Another effective soft-switching strategy was proposed for three-phase six-switch boost PFC [85-86] with a compact auxiliary circuit, which consists of one bidirectional switch and one LC branch. Although the used number of components is less, the voltage ratings of both switch and capacitor have to be at least equal to the DC link voltage and the current ratings of the switch and inductor have to be at least equal to the load current magnitude. Therefore, these constraints would potentially increase the size and total cost of the components. Another robust soft-switching implementation was performed in [87] with instantaneous power feedback scheme. This method incorporates three auxiliary resonant commutation circuits, each for one phase. However, overall six switches along with their individual gate drivers, six diodes and three resonant inductors are used specially for the soft-switching circuit, which increases the total additional component counts and losses. By addressing these issues, a passive non-dissipative snubber-based soft-switching technique [88] was proposed in a single-phase boost-type three-level converter. However, it is very challenging to extend this approach to a three-phase six-switch PFC due to the fact that this soft-switching based auxiliary circuit was specifically developed for three-level converters.

In our work published in [89], an innovative soft-switching approach is proposed to alleviate the aforementioned issues of existing methods. The proposed ZVS strategy uses three additional bidirectional switches and one resonant inductor, as a part of the auxiliary circuit. Requirement of an additional resonant capacitor is avoided by accessing the midpoint of the output DC link. This could be easily implemented by putting a series combination of two equal capacitors across the DC link. In order to achieve ZVS while switching transient, the parasitic capacitance of the corresponding

main-switch is discharged by the resonating current, caused by the resonant inductor and one of the two series DC link capacitors. A major advantage of the proposed soft switching circuit is that ZVS can be achieved in the auxiliary switches, which significantly reduces the extra losses from the add-on system. However, since there could be a potential issue of mismatch in equal voltage sharing across two series capacitors, a voltage balancing method is incorporated by some additional modifications in feedback control loop, which requires voltage sensing of any of the two series capacitors by a simple resistive divider network. This dissertation elaborately describes the active clamping ZVS concept in three-phase six-switch structure, followed by gradual reduction in redundancy in the initial soft-switching structure, in order to reach to the modified proposed structure with three switches and one inductor.

2.3.1 Proposed Soft-switching Circuit for a Three-Phase Boost PFC

The proposed soft-switching methodology is fundamentally based on ZVS active clamping in a boost-derived topology and Fig. 2.16 represents ZVS configuration for a regular DC-DC boost converter.

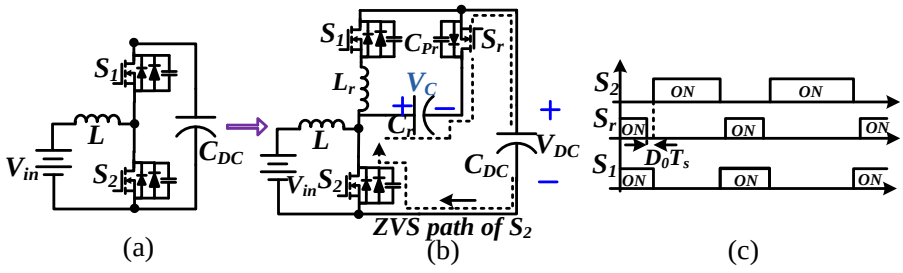


Fig. 2.16. ZVS active clamping in a regular DC-DC boost converter

Fig. 2.16 shows an active clamping in a regular DC-DC boost converter, which uses one resonant inductor, one resonant active-clamping capacitor with clamped voltage V_C and one MOSFET, as a part of the auxiliary ZVS circuit. In the above circuit, in order to achieve a ZVS turn-ON of S_2, the gate pulses at S_2 and S_r must be complementary to each other with a fixed dead-time. The auxiliary switch S_r is turned off before turning off S_1 or turning on S_2, which is demonstrated in Fig. 2.42(c). Once S_r is turned off, there is a resonance between L_r, C_r and C_{Pr} (i.e. the parasitic capacitance of S_r). Due to the charging resonating current through C_{Pr}, the blocking voltage across C_{Pr} will reach V_C+V_{DC} within a certain interval. Eventually, the voltage across the parasitic capacitor of S_2 will fall down to 0, which will result in ZVS if the pulse is applied to S_2 after the complete discharge of parasitic capacitance of S_2. On the other hand, once S_2 turns off and S_1 turns on, there is a parasitic resonance, happening between L_r and C_{Pr} with the active clamped capacitance (C_r) in series path. Within a resonant cycle, C_{pr} gets discharged fully and ensures the ZVS for S_r before the next turn-on pulse. Thus, ZVS of both main and auxiliary switches can be achieved through this method. Similarly, another auxiliary circuit could be added to the main circuit in order to achieve ZVS for S_1. Thus, a complete ZVS structure for a DC-DC boost leg, consisting of two active switches, can be achieved.

Thereby, the active clamping ZVS concept could be extended to a three-phase boost PFC, as it consists of three coupled AC-DC boost converters with the same output V_{DC}. Fig. 2.17(a) represents one phase leg consisting of two switches, connected across the DC link and Fig. 2.17(b) and Fig. 2.17(c) demonstrate the combination of main and auxiliary circuits for achieving ZVS for both S_1 and S_2. Fig. 2.17(b) represents the ZVS

active clamped phase-leg, directly obtained from the extension of a regular DC-DC boost leg. Since, L_{r1}, C_{r1}, S_{r1} and S_2 form a loop and L_{r2}, C_{r2}, S_{r2} and S_1 form another loop structure, Fig. 2.17(b) could be restructured to Fig. 2.17(c) without any loss of generality and symmetry.

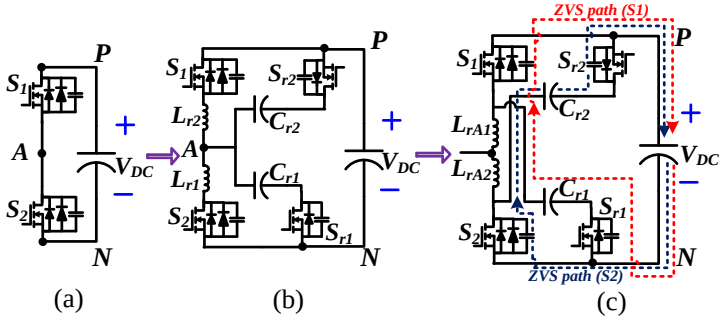


Fig. 2.17. (a) One phase-leg (b) one phase-leg with ZVS circuit (c) one phase-leg with modified soft-switching circuit

Prior to turning ON S_2, the discharge of the S_2 parasitic capacitor happens through the parasitic resonance, caused by L_{rA2}, C_{r2} and the parasitic capacitance of S_{r2}, shown in blue dotted line in Fig. 2.17(c). The pulse could be applied to turn on S_2 with ZVS, after the voltage across S_{r2} becomes $V_{DC}+V_{C2}$, where V_{C2} is the clamping voltage of C_{r2}. Similar operation is followed for turn-on process of S_1, which is shown in red dotted line in Fig. 2.17(c). Same replica of the ZVS phase-leg, shown in Fig. 2.17(c) could be used in the ZVS structure of all three legs in a three-phase boost PFC, which is demonstrated in Fig. 2.18(b). The whole structure consists of additional 6 resonant inductors, 6 resonant capacitors and 6 switches, as a part of the auxiliary circuit. However, in order to reduce the total component counts in the auxiliary circuit, it is very crucial to find out the redundancies in the overall structure. As can be seen from the structure in Fig. 2.18(b), there is star (Y) connection of two pairs of three arms,

where each arm consists of a series combination of a resonant capacitor and an auxiliary switch. Z_{1*} denotes one of the 6 arms, which is a combination of C_{r1} and S_{r1}. The two common points of the star connections are positive and negative terminals of the DC link. By some algebraic modifications, the star-connected impedances can be converted into a delta structure, where the arms will be connected between line-to-line (*A*-*B* or *B*-*C* or *C*-*A*). However, the values of the equivalent delta-connected impedances will be different from star-connected ones, which will give us a different combination of L_r and C_r for each switch. The transformed circuit is shown in Fig. 2.19(a).

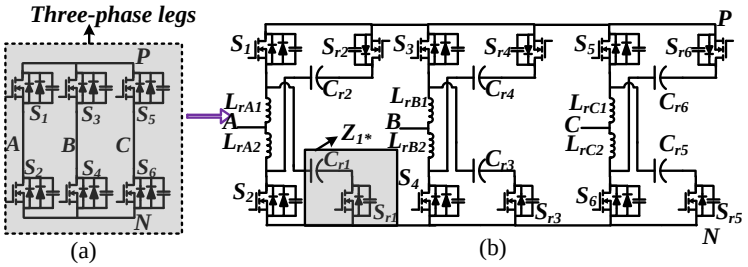


Fig. 2.18. (a)Three-phase legs (b) Three-phase legs with first modified soft-switching auxiliary circuit

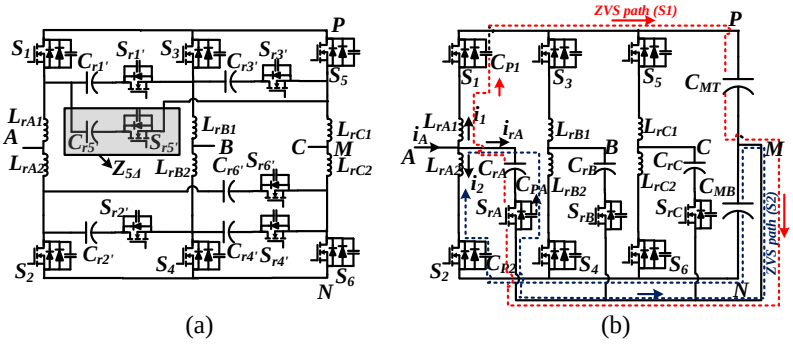


Fig. 2.19. (a) Second modified soft-switched three-phase PFC legs (b) Third modified soft-switched three-phase legs with reduced number of capacitors

As can be seen from Fig. 2.19(a), the terminals of delta-connected switch-capacitor combinations are connected to either positive (*P*) or negative (*N*) side of the DC link output. As an example, if either of S_1 or S_5 is ON, the corresponding terminal of $Z_{5\Delta}$

will be connected to P. If either of S_2 or S_4 is ON, the corresponding terminal of S_{r2} & C_{r2}, combination will be tied to *N*. It physically means that the resonating current during the switching instant will either take the path from *P* to *N* or from *N* to *P*. Therefore, instead of using six switch-capacitor combinations, only three switch-capacitor combinations will suffice the required purpose, if one end of each switch-capacitor combination is connected to a midpoint (*M*) of two equal series-connected active-clamped capacitors (C_{MT} and C_{MB}) across the DC link. In that case, the resonating current will take the path from *P* to *M* or *M* to *N*. Another terminal of each of the switch-capacitor combination will be connected to the midpoint of each phase leg, where the resonating inductors L_{ri1}, L_{ri2} (where, '*i*' is *A* or *B* or *C*) are placed symmetrically around the midpoints *A*, *B*, *C*. Thus, the restructured auxiliary circuit with ZVS active clamping, shown in Fig. 2.19(b) contains 3 less capacitors than the initially proposed circuit in Fig. 2.18(b). One of the most important design parameters is the discharge time of a parasitic capacitor of a main switch, which will help in determining the required deadband between any two complementary switches. The soft-switching dynamics of the circuit in Fig. 2.19(b) is demonstrated by Eq. (2.34) - Eq. (2.39), in case of achieving ZVS for S_2. In the following equations, i_2 denotes the current through L_{rA} and V_{CrA} denotes the voltage across auxiliary switch S_{rA}.

$$L_{rA2}\frac{di_2}{dt}+\frac{\int i_2 dt}{C}-\frac{V_{DC}}{2}+\frac{\int i_2 dt}{C_{PA}}-V_{CrA}=0 \tag{2.34}$$

$$L_{rA2}\frac{di_2}{dt}+\frac{\int i_2 dt}{C_{eq}}=\frac{V_{DC}}{2}+V_{CrA} \tag{2.35}$$

$$L_{rA2}\frac{d^2 i_2}{dt^2}+\frac{i_2}{C_{eq}}=0 \tag{2.36}$$

$$i_2(t) = \frac{V_{CrA}}{\sqrt{L_{rA2}/C_{eq}}} \sin(\omega_o t) \tag{2.37}$$

$$V_{Cp2}(t) = \frac{V_{DC}}{2} - V_{CrA}(1 - \cos(\omega_o t)) \tag{2.38}$$

$$t_{ZVS} = \frac{1}{\omega_o}(\cos^{-1}(1 - \frac{V_{DC}}{2V_{CrA}}) \tag{2.39}$$

where, $\omega_0 = 1/\sqrt{(L_{rA2}C_{eq})}$; $C_{eq} = CC_{PA}/(C+C_{PA})$, and t_{ZVS} is the full discharge time of C_{PA}. Furthermore, during the switching interval, the resonating current either flows through L_{ri1} or L_{ri2}, depending on the switch under ZVS and the same current flows through the switch-capacitor branch of '*i*'th phase. Therefore, it is straightforward to include the resonating inductor in series with the switch-capacitor branch and thus, the modified structure in Fig. 2.20(a) is obtained. Moreover, since no two switches change their states simultaneously in a symmetric SVPWM strategy, any one of the three switch-capacitor resonant branches will be active at a particular switching transient. Therefore, the three resonant inductors could be potentially replaced by a common branch of resonant inductor between the DC link midpoint (*M*) and the intersection point of three active clamping branches.

Similar analogy can be applied on the resonant capacitors (C_{rA}, C_{rB}, C_{rC}) and thus, these capacitors could be integrated with the C_{MT} and C_{MB}, as the resonating current through any of three active clamped branches flows through either C_{MT} or C_{MB}. After all these modifications, the finally obtained soft-switched three-phase leg, shown in Fig. 2.20(b) contains three additional switches and one resonant inductor (L_{res}). The extra component counts do not include the capacitors (C_{MT}, C_{MB}), as they can be potentially integrated as DC link capacitors. Since the resonating current through the

additional auxiliary branch could be bipolar, a MOSFET is the preferred switch. Thus, the ZVS of a complementary pair of main switches happens through the same auxiliary switch. Fig. 2.21(a) and 2.21(b), showing the complete structure of the soft-switched three-phase boost PFC topology, demonstrate the ZVS occurrence of S_1 and S_2, respectively. As can be seen from the ZVS current path in both the cases, the direction of resonating current flow through the auxiliary switch gets reversed in the case, when the complementary main switch turns on. As soon as the main switch turns off, ZVS of the auxiliary switch is achieved through the resonance within a time of $2\pi/\omega_{aux}$, where, ω_{aux} is the auxiliary resonant frequency caused by L_{res}, C_{MB} or C_{MT} and the parasitic capacitance of the main switch, which just turned off. In order to have a better mathematical understanding on the dynamics of the resonant elements while ZVS, some relevant time-domain relationships are demonstrated by Eq. (2.40)-Eq. (2.47) in the following subsection.

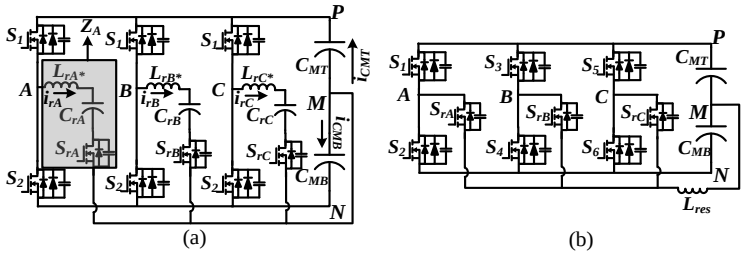


Fig. 2.20. (a) Fourth modified soft-switched three-phase legs (b) Final proposed soft-switched structure of three-phase legs

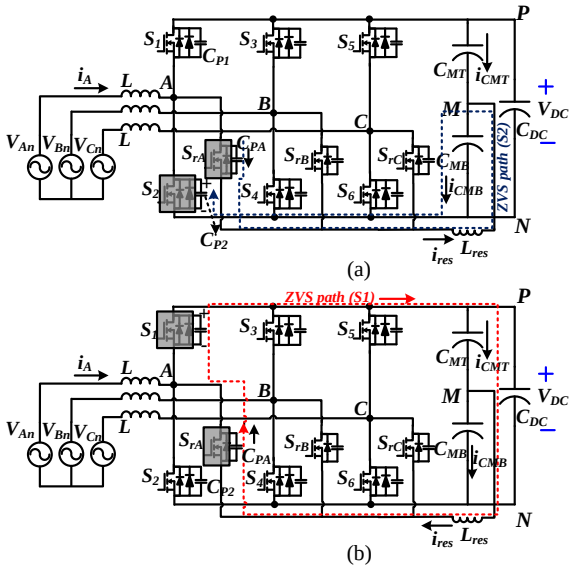


Fig. 2.21. Final proposed soft-switched 3-phase boost PFC structure (a) ZVS path of S_2 in the finally proposed soft-switched structure of three-phase PFC (b) ZVS path of S_1 in the proposed soft-switched PFC structure

2.3.2. Design Considerations

I. Selection of Parameters:

$$\frac{\int i_{rA}dt}{C_{PA}} + L_{res}\frac{di_{res}}{dt} + \frac{\int i_{CMB}dt}{C_{MB}} + \frac{\int i_{rA}dt}{C_{P2}} = 0 \tag{2.40}$$

Since, S_1 is ON during the discharging time of C_{P2} before the full-discharge time expires, the node 'A' is tied to V_{DC}, ad hence, the following relationships could be formulated.

$$\frac{\int i_{rA}dt}{C_{PA}} + L_{res}\frac{di_{res}}{dt} - \frac{\int (i_{res} - i_{CMB})dt}{C_{MT}} = 0 \tag{2.41}$$

Combining Eq. (2.40) and Eq. (2.41), a relationship between i_{res} and i_{CMB} can be established according to Eq. (2.42)-Eq. (2.43).

$$\frac{\int i_{res}dt}{C_{MT}} = \frac{\int i_{rA}dt}{C_{P2}} \tag{2.42}$$

$$i_{res} = \frac{C_{MT}}{C_{P2}} i_{rA} \tag{2.43}$$

From the two possible parallel paths between *M* and *A* along the flow of i_{res}, the following equation can be written.

$$i_{CMB} = i_{res} \frac{1/\omega C_{MT}}{1/\omega C_{MT} + 1/\omega C_{MB} + 1/\omega C_{PA}} \tag{2.44}$$

If the design is carried out with the constraint that the active clamped capacitances i.e. C_{MT} and C_{MB} are significantly larger than any parasitic capacitance i.e. $C_{MT}>>C_{PA}$ and $C_{MB}>>C_{PA}$, Eq. (2.44) implies that i_{CMB} can be neglected with respect to i_{res}. Thus, Eq. (2.131) can be restructured as the following.

$$\frac{\int i_{res} dt}{C_{eq1}} + L_{res} \frac{di_{res}}{dt} = 0 \tag{2.45}$$

where, $C_{eq1}= (C_{MT}*C_{P1})/(C_{P1}+C_{P2})$. Applying the initial conditions i.e. $i_{res}(0)=0$ and $V_{CP2}(0)=V_{DC}$; the following expressions for resonating current and drain-source voltage of S_2 are obtained.

$$i_2(t) = \frac{V_{CrA}}{\sqrt{L_{res}/C_{eq1}}} \sin(\omega_r t) \tag{2.46}$$

$$V_{Cp2}(t) = \frac{V_{DC}}{2} \cos(\omega_r t) \tag{2.47}$$

Therefore, the time for complete discharge of parasitic capacitance of S_2 is $t_{ZVS}=\pi/(2\omega_r)$, where $\omega_r=1/\sqrt{(L_{res}C_{eq})}$. The design of the resonant elements should ensure that the maximum total discharge time (t_{ZVS}) is more than switch turn-on time, to avoid short across DC link. However, t_{ZVS} should not be kept very high, so that the diode loss can be minimized. In our design, t_{ZVS} is kept as 100ns, which is just more than the turn-ON

time of the selected main switch (part number: CMF10120D, SiC MOSFET) and hence, the resonant time cycle is set 400ns. By combining this condition with the assumption that $\omega_r >> \omega_s$ (ω_s: switching frequency $=2\pi f_s$, where f_s=100 kHz in our design) in order not to pass the switching frequency component through the auxiliary resonant circuit, the selected combination of resonant elements are as follows: L_{res}=0.8µH; $C_{MB}=C_{MT}=C_M$=200nF, which satisfy all the requirements. This combination of LC parameters will produce a t_{ZVS} of 100ns and $\omega_{aux} = 1/\sqrt{(L_{res}(C_M \| C_{P2}))}$=50MHz, which ensures the ZVS of auxiliary switch within 20ns from the turn-off of main switch.

Furthermore, in order to find out the current rating of the used auxiliary switch, i_{res} needs to be expressed in terms of i_A and other system parameters. Assuming the switching transient when S_1 is ON (about to be OFF), S_2 is OFF (about to be ON) and S_{rA} is OFF, there are two parallel paths (from *A* to *M*) for i_A to flow. Let's say, the impedances are Z_1 and Z_2, which are given by $Z_1=1/(\omega C_{MT})$ and $Z_2=(\omega L_{res}+1/\omega C_{PrA})$. Therefore, the resonating current (i_{res}) flowing through the auxiliary switch and resonant inductor is given by the following relationship.

$$i_{res} = \frac{Z_1}{Z_1 + Z_2} i_A = \frac{C_{\mathrm{Pr}A}}{C_{MT}} \frac{i_A}{\omega^2 L_{res} C_{\mathrm{Pr}A} + 1} \tag{2.48}$$

Since, L_{res} and C_{PrA} take part in a resonance with a fixed frequency ω_r, the resonant current expression can be reframed as Eq. (2.49), under the assumption that $\omega_r >> \omega_s$.

$$i_{res} = = \frac{C_{\mathrm{Pr}A}}{C_{MT}} \frac{i_A}{1 + \omega^2 / \omega_r^2} \approx \frac{C_{\mathrm{Pr}A}}{C_{MT}} i_A \tag{2.49}$$

Since, the parasitic body capacitance of the main switch is significantly less than C_{MT} (design assumption), the resonant current magnitude is much lower than the line

current, i_A. The fact that $i_{res} << i_A$, could be also used in justification of not distorting the input phase current. Therefore, $\omega_r >> \omega_s$ condition does not allow the switching frequency component of input phase current to flow through the resonant circuit, and hence, maintains the input current waveform at the desired shape i.e. in phase with input voltage. According to the calculated value of C_{MT}, the magnitude of i_{res} would be less than 3A, at 2.2kW load power and 400V DC link voltage (design condition). As can be seen from the proposed soft-switched structure of three-phase PFC, the maximum voltage stress across the auxiliary switch can go as high as half of the DC link voltage, if there is equal voltage sharing between C_{MT} and C_{MB}. Considering all these rating requirements, 600V Si MOSFETs (IXTP10N60P) are selected as the auxiliary switches and SiC MOSFETs (CMF10120D) are selected for the main switches.

II. Voltage balancing at DC link midpoint:

One of the most crucial design issues is to ensure the equal voltage sharing between C_{MT} and C_{MB}, in order to use the half of DC link voltage as rating for the auxiliary switches. This could be achieved by sensing the voltage across either C_{MB} or C_{MT}, and regulating their voltages at $V_{DC\_ref}/2$. Therefore, a PI controller is added in the voltage loop for regulating V_{MN} and the controller output is added to the output of DC link voltage PI controller, shown in Fig. 2.48. Thus, the resulted sum acts as a trans-conductance for the current loop control.

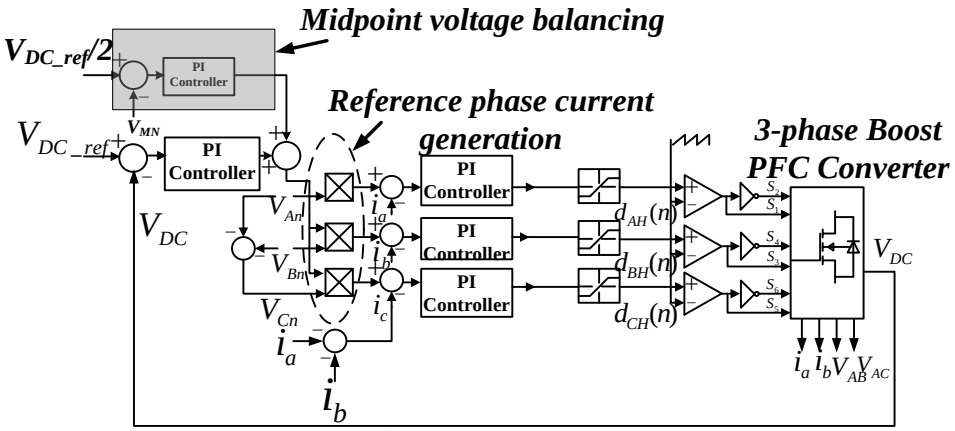


Fig. 2.22. DC link midpoint voltage balancing logic of a three-phase PFC

2.3.3. Experimental Results

As a verification to the proposed soft-switching methodology, an experimental prototype of a three-phase active boost rectifier is designed and developed. With the consideration of power density and efficiency, the switching frequency is selected as 100 kHz. The soft-switching control algorithm is implemented in TMS320F28335. Fig. 2.49 shows the steady state operation of the PFC converter at 120V, 60Hz AC input at a DC link voltage reference of 400V with 6.18A phase current RMS. Also, the experimental results exhibit an input current THD of 5.2%. Fig. 2.50 shows a deadtime more than 100ns between the fall of drain-source voltage of a main switch (from 400V to 0V) and the rising edge of its corresponding gate pulse logic, which confirms the ZVS operation of the switch.

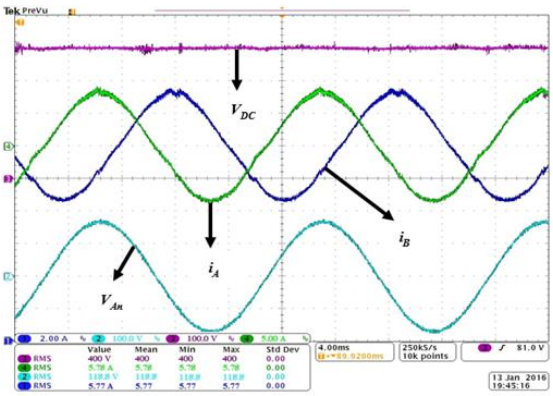


Fig. 2.23. Experimental waveforms of the converter; phase currents: i_A (RMS) =i_B (RMS) =6.18A

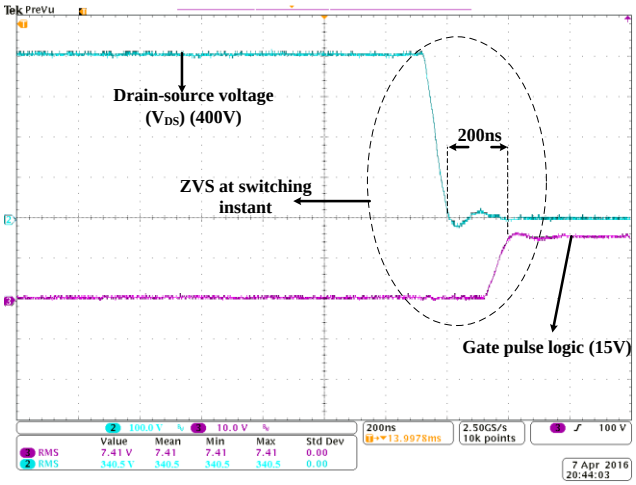


Fig. 2.24. ZVS of a main switch: drain-source voltage of S_1, gate pulse of S_1

With the ZVS implementation, total power loss reduces by 40%, giving rise to the efficiency value by 0.7%. Moreover, if Si MOSFETs are used for the main switches, the increase in efficiency will be more significant with the soft switching implementation. For example, if 1.2kV Si MOSFETs (part no. IXTH12N120) are used for the main switches, the total turn-on loss at 6kW load power is 90W (55% of total power loss), with a net efficiency of 97.2%. With the soft-switching, this efficiency could be potentially increased to 98.5%, which is greater than hard switched PFC with SiC MOSFETs. Also, as opposed to [5] and [6], this proposed auxiliary resonant circuit

with reduced number of active semiconductors enhances the converter performance further with 2% more efficiency improvement.

2.4 Summary

In this chapter, a novel control methodology, which derives and sets forth the injection of a common-mode or zero sequence duty ratio term to each linearized current controller output of a three-phase active boost rectifier, is proposed, analyzed and developed. This additional term seen at Eq. (2.16) has the advantages of enhancing power quality and reducing harmonics content without requiring any access to the source neutral. In addition, an innovative methodology to control the three-phase PFC with eliminating two input voltage sensors is proposed and analyzed. A 6kW (continuous)/10kW (peak) laboratory prototype of a three-phase active boost rectifier is designed with the specifications of some of the RTRUs in future MEAs.

The three-phase active boost rectifier was tested in a wide range of load powers up to 10kW and a 400Hz, 230V RMS phase-neutral AC input voltage at a switching frequency of 100 kHz. A maximum efficiency of 98.2%, a THD as low as 4%, DC link voltage ripple of 1% and an input power factor above 0.999 are achieved in the experiment at the rated input voltage and 10kW load power. Furthermore, the effectiveness of the proposed control is illustrated and supported by experimental results at different source frequencies of 400Hz and 800 Hz, which could be a usual situation in airplane generators. Thus, the proposed control with precise modeling along with utilization of SiC-based switching devices enable the PFC prototype to satisfy high-end conversion efficiency, good power quality, low THD, and enhanced power density.

Also, in this chapter, a novel soft-switching methodology is introduced and applied to a three-phase six-switch boost PFC topology. The auxiliary resonant circuit to carry out ZVS in the main-switches consists of three bidirectional active switches (preferably MOSFETs) and one resonant inductor. The major advantage with the proposed circuit is the soft-switching achievability in the auxiliary switches, which definitely reduces the additional losses in the add-on circuit.

An experimental prototype is developed to verify the proof-of-concept of the proposed circuit. Experimental results with the soft-switching implementation show an increase in conversion efficiency by 0.7% (from 98.2% to 98.9%) without compromising the input power quality. Furthermore, the soft-switched three-phase boost PFC converter with Si-MOSFETs (IXTH12N120) shows a conversion efficiency of 98.5%, which is even greater than the efficiency of a hard switched SiC-based converter with similar specifications.

Chapter 3: Fast start-up wide input frequency control of three-phase boost PFC

One of the major concerns in any converter as a part of auxiliary power supply unit is the start-up action. Fast startup is quite important in many applications in automotive and avionics industries. Achieving fast start-up becomes challenging especially when another simultaneous objective is to limit the inrush current below a certain level, due to the device rating limitation. A fast start-up operation in a switching DC-DC converter can be achieved using an additional circuit consisting of two extra switches and a capacitor as shown in [59], which introduces extra size and cost to the system. Until now, few research works have been carried out on startup control methods of the Y-connected three-phase PFC systems [60-62]. One possible reason for the lack of focus on start-up control in the research community could be the perception of straightforward application of the start-up control algorithm for single-phase PFCs [59] into three-phase systems. However, the three-phase implementation is far from being straightforward due to its complex structure, more number of switches, more voltage sources and bi-directional nature.

Furthermore, a two-step procedure comprising of (i) limiting the pre-charging current by utilizing SCR and (ii) modifying the conventional average current loop control is utilized in a three-phase AC system to achieve fast start-up with reduced inrush [60]. However, limiting the phase current requires extra hardware including resistors, power diodes and mechanical relays, which adds extra size and cost to the system. Furthermore, the method in [60] does not consider the constraint of faster settling of the converter. In addition, the current spike during start-up inrush-current

limiting method proposed in [60] can be reduced if duty-cycle feedforward is employed in the current control-loop design. Furthermore, a novel soft-start control in [62] outlines a closed-loop compensation method to increase the start-up input impedance of an isolated three-phase three-switch buck-type rectifier. However, the proposed method in [62] does not account for minimizing the start-up time i.e. faster settling, which may be an important requirement in many applications.

A few other key considerations for PFC-based systems in avionics applications are to maintain the regulation and stability in a wide source frequency range (typically 360Hz to 800Hz for avionics applications) and also, to keep a fast reference (phase current) tracking under any disturbances/transients in load power and line voltage. In most of the conventional PFC controller designs, the input phase angle displacement deviates from zero i.e. unity PF does not prevail with wide change in AC frequency as the corresponding closed loop Bode plot does not maintain a flat mid-band characteristic. However, there has been hardly any research work looking into the problem of designing a PFC controller working at a wide source frequency range. One possible reason for neglecting this problem is the perception of achieving unity power factor at any source frequency as the magnitude of the input frequency is very small as compared to the current loop bandwidth, which makes the phase response a constant zero at low frequency zone. However, the research in this document proves mathematically and validates experimentally that a conventional Proportional-Integral (PI) compensation cannot maintain the zero-phase response at wide input frequency variation.

Several research works focusing on the current loop compensator design have been carried out to resolve such PFC regulation issues and power quality improvement. In [63], it is shown that output voltage settling rate as well as input current quality can be improved by appending Proportional (P) compensation with input voltage feedforward rather than using a duty-cycle feedforward only. The research in [64] shows that zero-sequence-signal (ZSS) injection enables the output voltage regulation in a wider input voltage range and helps enrich the input power quality by reducing the total harmonic distortion (THD), which have equivalent performances as different continuous and discontinuous space vector modulation methods [65]–[68]. Moreover, duty-feed-forward (DFF) is mostly employed when current controllers with PI compensation are used to reduce the phase shift between a phase voltage and phase current, and consequently, improve the PF [69]. However, the controllers in the aforementioned methods [63-68] are designed to ensure unity PF only at a fixed source frequency. Also, the stability of the inner current loop in [69] is not guaranteed under wide change in line/load conditions and the method in [69] does not aim for optimizing the settling time for reference tracking under a load transient.

The control strategy, proposed in [70] establishes an output voltage loop for regulating the output voltage irrespective of the variations in load current and utility voltage and also, offers a fast dynamic response and unity PF at all operating conditions. The work in [70] proposes a non-linear sliding mode controller (SMC) to achieve faster settling transient. In addition, the average current mode control with or without zero-sequence-signal injection is proposed in many research works [71], which mainly emphasize on reducing the input current THD by compensating the lower order

odd harmonics. However, the current loop compensators in most of these average current controllers exhibit Bode plots with phase angle displacement, not held at zero degree throughout the operating range of source frequencies (360Hz to 800Hz in case of avionics applications). More research works, proposed in [72-75] discuss different PFC control methods in establishing a wider-bandwidth current loop and reducing the overall harmonics. As these methods are highly specific to the circuit topologies, none of these methods is applicable to a six-switch PFC.

In order to take care of the two aforementioned issues, two major aspects in terms of control of the converter i.e. (i) fast start-up operation with a new voltage loop compensation and (ii) good power quality and improved dynamics through the proposed current control loop have been individually achieved, which makes it an integrated control strategy in terms of implementation due to satisfying both the objectives simultaneously. The fast start-up, proposed in our work [14] is achieved by establishing a non-linear voltage loop controller, objectifying to minimize the cost function considering the area under voltage error versus time curve. This is proved to be the equivalent as minimizing the overshoot (or inrush phase current) as well as setting time. One major advantage associated with this approach is that no additional hardware or auxiliary circuit is engaged unlike many other existing technologies. It is proved that minimizing the cost function helps in reducing the reference phase current, which in turn reduces the current stress through semiconductors. Furthermore, it is proved that zero phase angle cannot be achieved throughout a wide frequency range using a conventional PI-based compensator in a six-switch PFC plant. Therefore, a new structure of current loop compensator is deduced by keeping a second order equivalent

closed loop system with flat mid-band frequency response. In addition, in order to achieve a faster tracking of input phase current reference, a modified state feedback controller is designed and its output is added to the linear compensator's output to generate the final duty reference. Thus, the integrated control strategy combining both the voltage and current compensators is digitally implemented and verified with a proof-of-concept of a 6-kW laboratory prototype.

The major control objectives are (i) to minimize the start-up time with minimum inrush current (ii) to achieve perfect unity PF at the entire range of source frequencies (360 Hz to 800 Hz for avionic applications) and (iii) to achieve fast tracking of reference phase currents i.e. faster settling under any load or line transients.

3.1 Fast start-up PFC control with minimum inrush current

First objective i.e. fast start-up performance with minimum inrush current is realized by introducing and implementing a non-linear voltage loop controller. It is analytically shown that the inrush current increases as the start-up time goes down. Therefore, an additional constraint of limiting the magnitude of inrush current below a certain safety limit (depending on the applications and device ratings) is applied besides the start-up time.

The expressions for the start-up time and the corresponding phase current are obtained from the outer DC link voltage controller loop analysis. The reference output current is generated by multiplying the DC link voltage PI controller output with a constant gain (g) and the DC link is charged by the current i_o, which makes the plant as $1/sC$. Laplace domain analysis gives us the closed loop voltage transfer function,

shown below. K_{pv} and K_{iv} denote the PI controller parameters for the conventional DC link voltage control loop.

$$\frac{V_{DC}(s)}{V_{DC}^{*}(s)} = \frac{K_{pv}s + K_{iv}}{(s^2C + sK_{pv} + K_{iv})} \quad (3.1)$$

Given that the DC link voltage reference V_{DC}* is a constant value (set at 650V in our design), inverse Laplace transformation would provide us a time domain expression for the actual DC link voltage.

$$V_{DC}(t) = V_{DC}^{*}[1 - \exp(-\sigma t)\sin(\omega t + \varphi)] \quad (3.2)$$

Where, $\sigma = K_{pv}/2C$ and $\omega = \sqrt{\frac{K_{iv}}{C} - \frac{K_{pv}^2}{4C^2}}$. (3.3)

A straightforward way to reduce the settling time (t_s) could be to increase the value of K_{pv} so that $exp(-\sigma ts) < 0.05$ (for 5% settling band), which implies $\sigma t_s > 3$. However, at the cost of reduced start-up time, the equivalent phase current reference gets substantially scaled up. The DC voltage controller output (i.e. trans-conductance) is directly proportional to the phase current reference, established from the power balancing relationship. Also, upon setting a higher K_p, the value of 'g' increases proportionally.

$$V_{DC}^{2}g = 3V_{An}i_A \Rightarrow i_A = \frac{V_{DC}^{2}g}{3V_{An}} = \frac{V_{DC}^{2}(K_p(V_{DC} - V_{DC}^{*}) + K_i \int_{<Ts>}(V_{DC} - V_{DC}^{*})dt}{3V_{An}} \quad (3.4)$$

Therefore, with a requirement of fast settling of DC voltage, both the current reference and actual current go higher. One of the major objectives is to keep the start-up time below 5ms and start-up transient phase current below four times the steady state RMS value in a three-phase six-switch PFC converter, operating nominally at 400Hz in an

auxiliary power supply unit for avionics applications. During the start-up operation, no steady state analyses are valid and PFC operation does not hold, which requires us to consider the instantaneous converter dynamics for detailed analyses. Moreover, since the objective is to minimize the overall start-up time, the minimization cost function is defined as a linear combination of the sum of error in output voltage and the cumulative sum of error square of output voltage, which is expressed in Eq. (3.5). In the expression of *J*, the error is squared so that absolute values of the deviations from the reference value can be accumulated as the error can be bipolar in nature. *J* denotes the voltage controller output i.e. an equivalent trans-conductance to the all three phases, shown in the voltage controller block diagram in Fig. 3.1.

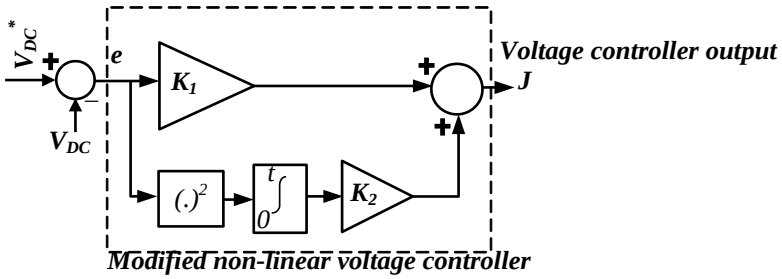


Fig. 3. 1. The proposed voltage controller

Faster settling indicates lower area under voltage-error vs time curve i.e. lesser value of *J*, as demonstrated clearly in Fig. 3.2. Lower the settling time and lower the deviations from the reference voltage value would imply less shaded area under the error voltage (V_{DC}^*- V_{DC}) curve. Also, less start-up current requires a lower phase current reference, assuming a constant current loop gain, which implies lower *J*.

$$J = K_1 e_v + K_2 \int_{-\infty}^{t} e_v^2 \, dt \tag{3.5}$$

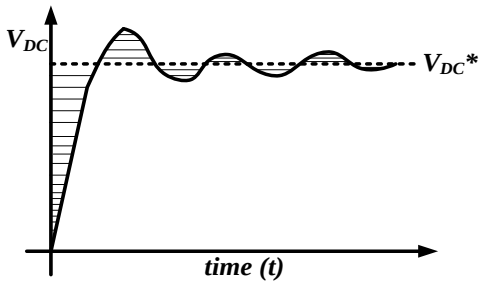


Fig. 3.2. A typical waveform for the DC link voltage settling

where, $e_v = V_{DC}^* - V_{DC}$. Thus, the overall voltage controller behaves as a non-linear function of the error in the output voltage. The above expression can be intuitively judged from the fact that minimizing the start-up time is equivalent to minimizing the area under the second norm of error in output voltage plotted against time. The first term in the expression of J denotes the weightage to reduce the steady state error to zero. The individual weightages K_1 and K_2 are determined from the following two conditions.

(i) $dJ/dt = 0$ at $V_{DC} = V_{DC}^*$, which produces the following expression.

$$K_1 \dot{e_v} + K_2 e_v^2 + K_2 \int_{-\infty}^{t} \frac{d}{dt}(e_v^2)\, dt = 0;\ K_1 = -\frac{2K_2 e_v^2}{\dot{e_v}} \tag{3.6}$$

Thus, the interdependence between K_1 and K_2 is formulated by the above relation, using the DC voltage sensor data and calculating $e_v = V_{DC}^* - V_{DC}$.

(ii) It is our target to maintain the J at its optimum value J*. Therefore, $\dot{J}(J - J^*) < 0$ holds at all values of V_{DC}. If $V_{DC} > V_{DC}^*$ i.e. $J > J^*$, the aim should be to make $J' < 0$ so that both the voltage error and the cumulative square error values decrease over time and vice-versa holds. Multiplication of $(J-J^*)$ and J' is computed online with the updated values of the output voltage at each switching cycle and refreshing the cumulative square-error value.

$$(J - J^*)\dot{J} = \left[K_1 e_v + K_2 \int_{-\infty}^{t} e_v^2 dt - J^*\right] \times [K_1 e_v + 2k_2 e_v^2] = (K_1^2 e_v - K_1 J)\dot{e_v} +$$

$$K_1 K_2 \left(2e_v^3 + \dot{e_v} \int_{-\infty}^{t} e_v^2 dt\right) - 2K_2 J^* e_v^2 + 2K_2^2 e_v^2 \int_{-\infty}^{t} e_v^2 dt < 0 \qquad (3.7)$$

The optimum J^* is calculated imposing the constraints that $V_{DC} = V_{DC}^*$ (at steady state) and $e_v = V_{DC}^* exp(-t/\tau)$, where τ is $T_s/3$, assuming T_s as the 5% settling time. The set requirements in the variation of the error voltage are that (i) there is no DC link voltage overshoot to minimize the start-up current. Therefore, the reference shape of the DC link voltage is assumed to be first-order exponential RC rise. (ii) At $t=T_s$, the error voltage reaches within 5% settling band. Therefore, the net expression of J^* (at the steady state) stands out as follows:

$$J^* = K_2 \int_{-\infty}^{T} V_{DC}^{*2} \exp(-2t/\tau) dt = \frac{K_2 V_{DC}^{*2} T_s}{6} (1 - \exp(-2T/\tau)) \approx \frac{K_2 V_{DC}^{*2} T_s}{6} \qquad (3.8)$$

The DC voltage controller's instantaneous output becomes as follows, where K_1 and K_2 effectively behave as the controller parameters.

$$J = K_1 (V_{DC}^* - V_{DC}) + K_2 \int_{-\infty}^{t} (V_{DC}^* - V_{DC})^2 dt \qquad (3.9)$$

Thereby, the coefficients K_1 and K_2 are selected by following the relationships in Eq. (3.7) – Eq. (3.8) after replacing J^* from Eq. (3.8) with a pre-selected start-up time T_s, which is targeted at 2.5 ms (one line cycle) in this design. Therefore, in order to establish a time-optimal control for the DC link voltage start-up, the conventional PI compensator is replaced by the new controller block, which generates the active power reference equivalent (J) as presented in Eq. (3.9). At steady state, output voltage error becomes zero, and value of the expression J remains constant i.e. $J'=0$.

3.2 Wide input frequency current loop controller design for three-phase boost PFC

The current loop compensator consists of two major parts with two different objectives i.e. state feedback controller for fast reference tracking and a second order linear compensator for ensuring unity PF over a wide input frequency range. A state-feedback based controller in cascode conjunction with a type-2 linear compensator is proposed for fast tracking of phase current reference under load transient, input line disturbance rejection and enhancement of the current loop bandwidth. A major element in order to establish the control strategy is to formulate the small signal plant characteristic of a three-phase six-switch PFC, which is performed in details in Section 3.2.1. The self and cross transfer function obtained from preceding analyses are presented as follows.

$$T_{self}(s) = \frac{\Delta i_A(s)}{\Delta d_{AH}(s)} = \frac{4V_{DC}[(1-r)+sT]}{3Ls[(r+1)+(r-1)sT/2]} \tag{3.10}$$

$$T_{cross}(s) = \frac{\Delta i_A(s)}{\Delta d_{BH}(s)} = \frac{4V_{DC}[(1-r)+sT]}{3Ls[(3-r)+(3+r)sT/2]} \tag{3.11}$$

where, '*r'* can vary from 0 to *1+h*, where '*h*' denotes the maximum ripple overriding on the nominal DC link voltage.

3.2.1 State feedback control for fast reference tracking:

In order to design the state-feedback controller, it is important to establish the state space representation of the three-phase six-switch PFC converter. The set of governing current-voltage relationships averaged over a switching cycle is represented in Eq. (3.12) – Eq. (3.13), which utilize the relation $V_{nN}= (d_{AH}+d_{BH}+d_{CH})*V_{DC}/3$.

$$V_{AN} = L\frac{di_A}{dt} + d_{AH}V_{DC} \Rightarrow L\frac{di_A}{dt} = V_{An} + \frac{d_{BH} + d_{CH} - 2d_{AH}}{3}V_{DC} \quad (3.12)$$

$$L\frac{di_B}{dt} = V_{Bn} + \frac{d_{AH} + d_{CH} - 2d_{BH}}{3}V_{DC} \quad (3.13)$$

The capacitor current expression is obtained by subtracting the load current from the sum of top three switch currents, presented in Eq. (3.14).

$$C\frac{dV_{DC}}{dt} = d_{AH}i_A + d_{BH}i_B + d_{CH}i_C - \frac{V_{DC}}{R} = (d_{AH} - d_{CH})i_A + (d_{BH} - d_{CH})i_B - \frac{V_{DC}}{R} \quad (3.14)$$

Noting the above state equations, two phase currents (i_A, i_B) and the output DC link voltage are considered to be the state variables of the system i.e. $X=[i_A\ i_B\ V_{DC}]$. Therefore, the state space representation of the system $X'=AX+BU$, is given by the following expression, where the input voltages are considered to be inputs to the system.

$$A = \begin{pmatrix} 0 & 0 & \frac{d_{BH} + d_{CH} - 2d_{AH}}{3L} \\ 0 & 0 & \frac{d_{AH} + d_{CH} - 2d_{BH}}{3L} \\ \frac{d_{AH} - d_{CH}}{C} & \frac{d_{BH} - d_{CH}}{C} & \frac{-1}{RC} \end{pmatrix} \quad (3.15)$$

Duty ratios act as the control variables, which are the elements of '*A*' matrix and thus, make the system as linear time varying (LTV) in nature. Consequently, the overall small signal stability of the system needs to be judged locally around each operating point in order to check the system response against any line disturbance or load transient.

In the proposed control structure, in order to enable faster tracking of current reference and to perform line disturbance rejection, a small signal duty component is added to the linear compensator's output. This small signal component is derived as a linear

combination of the small signal changes in state variable feedback i.e. $\Delta d_{AH}=K_{a1}\Delta i_A+K_{a2}\Delta i_B+K_{a3}\Delta V_{DC}$. Assuming zero perturbation in the input voltages, the frequency domain Laplace transformation gives us the following: $(sI-A)\Delta X(s) = 0$. In order to ensure the asymptotic small signal stability of the closed loop system, the eigenvalues of ($sI-A$) must lie on the left half plane and accordingly, the state feedback parameters are selected. The characteristic equation for the closed loop system is given by the following.

$$s^3 + as^2 + bs + c = 0 \tag{3.16}$$

where, $a=1/RC$;

$$b = \frac{d_{BH} + d_{CH} - 2d_{AH}}{3L} \times \frac{d_{AH} - d_{CH}}{C} - \frac{d_{AH} + d_{CH} - 2d_{BH}}{3L} \times \frac{d_{BH} - d_{CH}}{C}. \\ = \frac{4d_{AH}d_{CH} - 4d_{BH}d_{CH} - 2d_A^{\,2} + 2d_B^{\,2}}{3LC} \tag{3.17}$$

Where, the top side MOSFET duty ratios are derived through addition of linear compensators' outputs and small signal components from state-feedback controller outputs i.e.

$d_{AH} = d'_{AH} + \Delta d_{AH} = d'_{AH} + K_{a1}\Delta i_A + K_{a2}\Delta i_B + K_{a3}\Delta V_{DC}$ and $d_{BH} = d'_{BH} + \Delta d_{BH} = d'_{BH} + K_{b1}\Delta i_A + K_{b2}\Delta i_B + K_{b3}\Delta V_{DC}$

In order to ensure all the solutions to be negative, the following relationships must hold by Routh-Hurwitz criterion: $a>0$ and $ab-c>0$ i.e. $b>0$. Applying the detailed expressions for the duty ratios, the stability conditions are restructured as follows:

$1/RC>0$, which always holds true and $2d_{CH} > d_{AH} + d_{BH}$, which implies the following:

$$2(d'_{CH} + K_{c1}\Delta i_A + K_{c2}\Delta i_B + K_{c3}\Delta V_{DC}) > [(d'_{AH} + d'_{BH})\{(K_{a1} + K_{b1})\Delta i_A + (K_{a2} + K_{b2})\Delta i_B + (K_{a3} + K_{b3})\Delta V_{DC}\}] \quad (3.18)$$

The second condition implies that if $d_{AH}>d_{BH}$ in a switching cycle, $2d_{CH}>d_{AH}+d_{BH}$ has to hold true i.e. d_{CH} must be greater than the arithmetic mean of d_{AH} & d_{BH}. Alternatively, in a switching cycle if $d_{AH}<d_{BH}$ holds, $d_{AH}+d_{BH}>2d_{CH}$ must hold true. After confirming the closed-loop state feedback stability, the pole placement method can be applied to obtain the characteristic polynomial. At any load or line disturbance, the settling time varies inversely with the pole magnitudes. Comparing different coefficients of the polynomial with Eq. (3.16), the controller parameters can be obtained.

Furthermore, one of the important concerns is to check the small signal stability of the converter against the system disturbances. Hence, a vital step is to determine the equivalent closed current-loop transfer function considering both the linear compensator and state-feedback controller. From the feedback control structure of phase 'A', shown in Fig. 3.3, the following expression can be written.

$$[C(i_A^* - i_A) + \Delta d_{A,sfb}]G = i_A \quad (3.19)$$

where, $\Delta d_{A,sfb}$ is the additional duty added from the state feedback compensator, which is given by: $\Delta d_{A,sfb} = K_1\Delta i_a$, considering zero variation in other two state variables. In 'z' domain, $\Delta d_{A,sfb}(z)=K_{a1}(1-z^{-1})i_A(z)$ follows that the bilinear transformation would give us the following.

$$\Delta d_{A,sfb}(s) = K_{a1}\frac{sT}{1+sT/2}i_A(s) \quad (3.20)$$

Assuming $T_1(s)=K_{a1}sT/(1+sT/2)$, the following is obtained.

$$\frac{i_A(s)}{i_A^*(s)} = \frac{G(s)C(s)}{1+G(s)C(s)-G(s)T_1(s)} \tag{3.21}$$

Also, if an undesired PWM disturbance arises due to sensor noises or digital glitches, it is shown that the noise amplitude asymptotically dies down to a very low value at steady state with a proper selection of controller parameters. In order to determine output (i.e. phase current) to disturbance (η) transfer function, the reference current amplitude is assumed zero. Equivalent transfer function turns out as follows.

$$\frac{i_A(s)}{\eta(s)} = \frac{G}{1+CG} = \frac{H(s+2\xi a)(s+z)}{s(s+p)(s+2\xi a)+K_{a1}H(s+z)(s+2\xi a)+Hs(s+p)} \tag{3.22}$$

With a unit step disturbance noise, the translated impact on the measured phase current amplitude in steady state can be obtained using final value theorem in Laplace domain.

$$\lim_{t\to\infty}(i_A(t)) = \lim_{s\to 0}(sI_A(s)) = \lim_{s\to 0}\frac{s\eta(s)G(s)}{1+C(s)G(s)} = \lim_{s\to 0}\frac{G(s)}{1+C(s)G(s)} = \frac{1}{K_{a1}} \tag{3.23}$$

Therefore, by pre-fixing a large value of K_{a1} in the pole-placement process, the impact of noise disturbance on the phase current can be made negligible. Thus, it clearly shows that the proposed control scheme enables disturbance rejection from PWM input as well as fast tracking of reference, which is clearly validated by the experimental results with transients, presented in Section 3.4.3.

3.2.2 The proposed linear compensator:

With respect to the derived plant characteristics, there are two following typical regulation issues associated with a PI compensator: (a) the phase displacement angle between input voltage and current is not maintained at zero over a wide range of source frequencies (360Hz to 800Hz), and (b) the gain of the transfer function $i_a/i_a^*(s)$ (input

current to its reference) is not maintained at unity i.e. the transfer function characteristic is not perfectly flat over the input AC frequency range of 360Hz to 800Hz. These two issues would cause undesired reactive power flow towards the load and lose the phase current regulation. Therefore, the proposed strategy brings in a modification in terms of bandwidth enhancement and shaping a flat-top gain characteristic. The overall structure of the control block diagram is shown in Fig. 3.3.

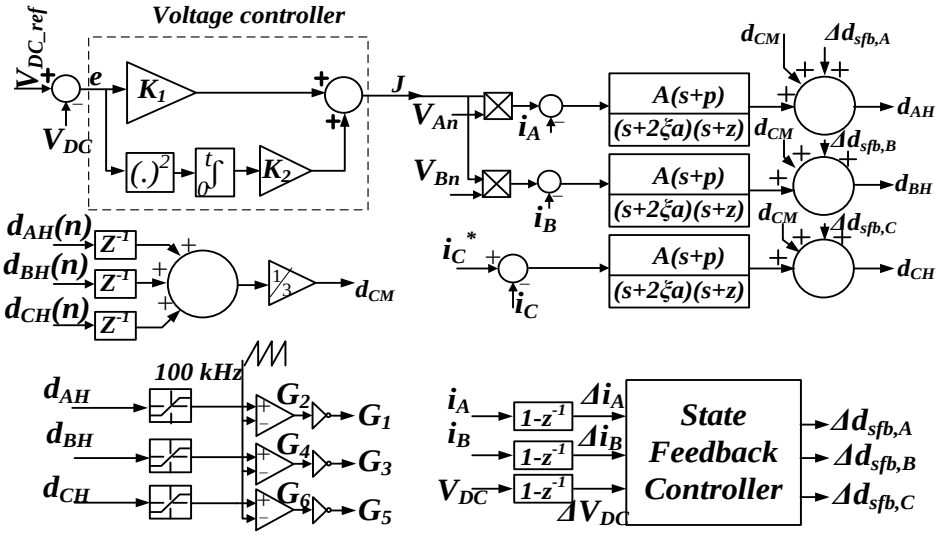


Fig. 3.3. The proposed control block diagram

The current references for the three phases in the proposed control loop are derived by multiplying the non-linear voltage controller's output (*J*) with the input phase voltages. The closed loop transfer function of the current loop with the conventional PI compensator is given as follows and its corresponding frequency domain Bode plot is presented in Fig. 3.4. The compensator parameters are selected in such a way that the unity gain of the transfer function $i_a(s)/i_a^*(s)$ is maintained. Therefore, the loop gain must be much greater than unity in the entire wide frequency range, which is demonstrated in Eq. (3.25).

Transfer function:

$$T_{CL}(s) = \frac{C_{PI}(s)G(s)}{1 + C_{PI}(s)G(s)} = \frac{H[k_p s^2 + s(k_p z + k_i) + k_i z]}{s^3 + (p + Hk_p)s^2 + H(k_p z + k_i)s + Hzk_i} \tag{3.24}$$

Loop gain >>1 implies

$$H\sqrt{[(k_p{}^2\omega^2 + k_i{}^2)(\omega^2 + z^2)]} >> \omega^2\sqrt{\omega^2 + p^2} \tag{3.25}$$

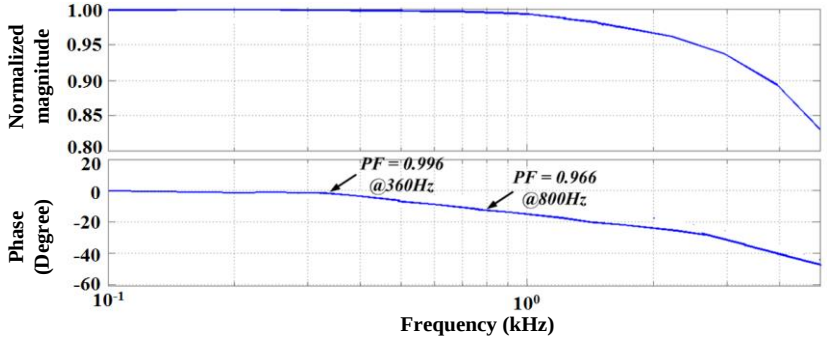


Fig. 3.4. Bode plot of the closed loop transfer function with PI compensator

PI controller is designed by satisfying the above constraint. From the transfer function, the relationship between the phase angle displacement and frequency could be obtained as Eq. (3.26) and is plotted in Fig. 3.5. As can be seen from Fig. 3.5, the phase angle increases monotonically in the range of 360-800Hz, which results in degrading the input power factor in case of PI compensation. The variation of power factor with input AC frequency is shown in Fig. 3.6.

$$arc(T(j\omega)) = \tan^{-1}\frac{(k_p z + k_i)\omega}{k_i z - k_p\omega^2} - \tan^{-1}\frac{H(k_i + k_p z)\omega - \omega^3}{Hzk_i - (p + Hk_p)\omega^2} \tag{3.26}$$

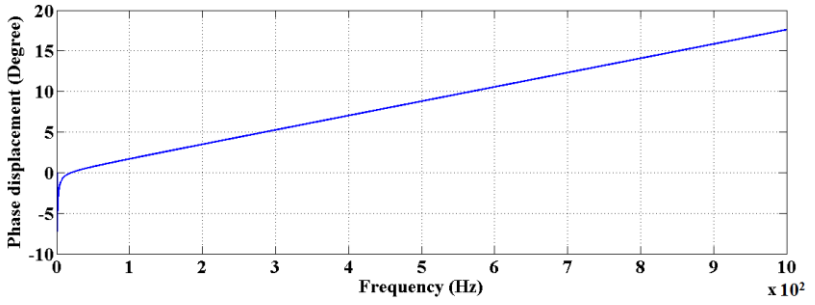


Fig. 3.5. Variation of phase displacement with source frequency

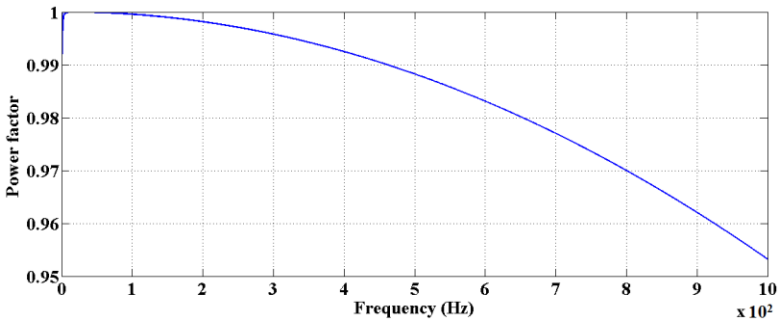


Fig. 3.6. Variation of power factor with source frequency

As can be seen from the above plot, the gain and phase-angle displacement touch nearly 5-10 dB and 5-10^{o}, respectively in the low-mid frequency band (100Hz to 1 kHz). From the variation of phase angle displacement with source frequency using the PI parameters satisfying Eq. (3.25), it is inferred that the power factor can be as low as 0.96 at 800Hz source operation, which drastically reduces the efficiency. On the other hand, the proposed strategy solves this issue by presuming the closed loop system as an equivalent first or second order transfer function. For a pre-defined closed loop structure *(T(s))*, the compensator can be determined from the following relationship.

$$T(s) = \frac{CG}{1+CG} \Rightarrow C(s) = \frac{T(s)}{(1-T(s))G(s)} \tag{3.27}$$

Typically, the bandwidth of a current loop compensator in a PFC system is kept as 1/10th of switching frequency and at-least 10 times of the AC source frequency. In case of a 100 kHz switching PFC converter working with a maximum input frequency of 800Hz, the bandwidth is typically maintained at 10 kHz. Therefore, an equivalent closed loop structure with first or second order (damping factor 0.5) characteristics is represented in Eq. (3.28) and Eq. (3.29), respectively and Fig. 3.7 presents their frequency responses.

$$T_1(s) = \frac{2\pi \times 10^4}{s + 2\pi \times 10^4} \tag{3.28}$$

$$T_2(s) = \frac{(2\pi \times 10^4)^2}{s^2 + 2\pi \times 10^4 s + (2\pi \times 10^4)^2} \tag{3.29}$$

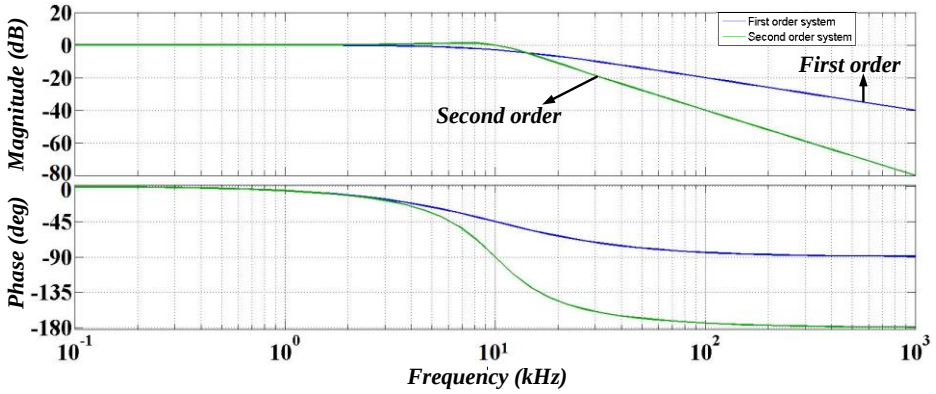


Fig. 3.7. First and second order systems with corner frequency of 10 kHz.

As can be seen from the above plot, both the gain and phase angle responses perfectly coincide each other at the extremum of source frequency range (i.e. 360Hz and 800Hz). The attenuations offered to the switching frequency and its multiples are more in case of a second order than a first order system, which would effectively improve the input current THD and differential mode (DM) EMI spectrum. Due to these advantages, the proposed method establishes a controller to form a second order equivalent system. By substituting the small signal plant characteristics from Eq. (3.4), the controller transfer function is obtained as follows with a Band-pass filter (BPF) characteristics

$$\frac{CG}{1+CG} = \frac{a^2}{s^2 + 2\xi as + a^2} \Rightarrow GC = \frac{a^2}{s^2 + 2\xi as} \Rightarrow C(s) = \frac{A(s+p)}{(s+2\xi a)(s+z)} \tag{3.30}$$

Where, $A=a^2/H$ and $H=8V_{DC}/(3L(r-1))$. There are three effective parameters i.e. a, p, z to be selected while designing the proposed controller. The controller structure has one

zero and two poles, where the zero (z) and one of the poles (p) are same as the pole and zero of the small signal PFC plant, respectively. The followings are the values of z and p obtained from Eq. (3.4), $z= (1-r)/T$, $p= 2(r+1)/(T(r-1))$ and 'r' can vary from 0 to $1+h$, where 'h' denotes the maximum ripple overriding on the nominal DC link voltage. Since the pole and zero locations of the plant vary upon different operating conditions unlike conventional PI compensation, the proposed controller shows variable characteristics to maintain the overall closed loop as second order system with desired corner frequency. In our design process, the damping factor is selected as 0.5 and cut-off frequency i.e. 'a' is chosen as $2\pi x10^4$ rad/s. Substituting $s=2(1-z^{-1})/T(1+z^{-1})$ using bilinear transformation, the discrete time-domain controller is implemented as follows (where, T is the sampling time).

$$D(z)[2(1+\xi aT)(2+qT)+4(\xi aqT^2-2)z^{-1}+2(\xi aT-1)(qT-2)z^{-2}] = E(z)[AT\{(2+pT)+2pTz^{-1}+(pT-2)z^{-2}\}] \quad (3.31)$$

which follows:

$$2(1+\xi aT)(2+qT)d[n] = AT\{(2+pT)e[n]+2pTe[n-1]+(pT-2)e[n-2]\} - 4(\xi aqT^2-2)d[n-1]-2(\xi aT-1)(qT-2)d[n-2] \quad (3.32)$$

The Bode plot of the closed loop PFC system considering the state-feedback compensator's effect (discussed in Section 3.4.3) is shown in Fig. 3.8. Both the gain & phase responses are maintained flat-top with a fixed gain of 3 dB and phase displacement of 3^o (i.e. PF of 0.995), as opposed to the non-uniform varying magnitude & phase response, shown by the conventional PI compensator. One important point to note is that the zero and pole of the controller depend on the operating conditions i.e. phase current, output voltage (or load power). Therefore, the digital implementation highly favors the adaptive tuning of the controller parameters, depending on the sensed

state variables. In our design process, the damping factor is selected as 0.5 and cut-off frequency i.e. '*a*' is chosen as $2\pi x10^4$ rad/s. The proposed control algorithm is implemented digitally in DSP TMS320F28335, which computes the controller pole (*z*) and zero (*p*) from the digitized sensor data through ADC channels. Finally, the phase duty ratios are generated by adding the outputs from the second order linear compensator and state-feedback controller, followed by duty saturation logic (minimum: 5%, maximum: 95%).

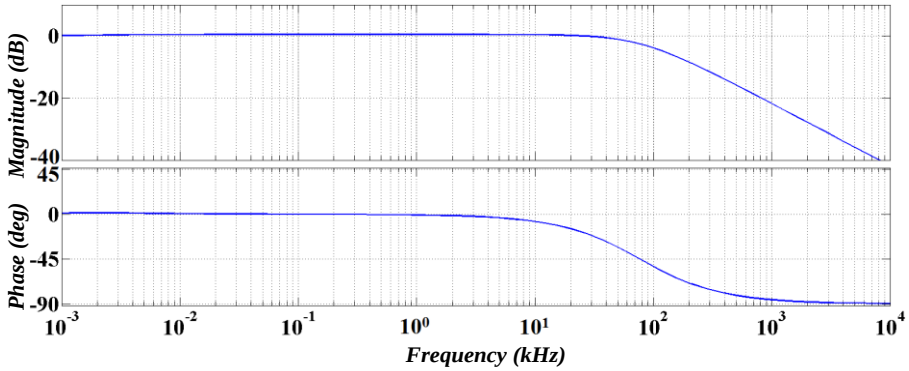


Fig. 3.8. Bode plot of the closed loop system with the proposed controller

As the controller parameters dynamically depend on the value of load power, the value of load resistance needs to be estimated at each sampling cycle. As the voltage control loop output (*J*) corresponds to the active power of the converter [76], it could be assumed to be proportional to V_{DC}^2/R, which is directly proportional to *1/R* for a constant output voltage assumption. From the control loop we have the followings.

$$i_A(n) = J\tilde{V}_{An}(n) \tag{3.33}$$

$$i_B(n) = J\tilde{V}_{Bn}(n) \tag{3.34}$$

Plugging the phase currents from Eq. (3.33) - (3.34) into the power balancing relation, '*R*' can be replaced in terms of '*J*' and hence estimated without using any load current sensor.

$$R = \frac{V_{DC}^{\ 2}}{2J(\tilde{V}_{An}(n)^2 + \tilde{V}_{\mathbf{B}n}(n)^2 + \tilde{V}_{An}(n)\tilde{V}_{Bn}(n))} \tag{3.35}$$

Therefore, the special achievements of the proposed control unlike PI compensation are (i) to maintain a unity power factor over a wide range of input frequency, (ii) to track the magnitude level of input current reference over the wide input frequency range, and (iii) improvement of current loop bandwidth to make the converter dynamics faster under any load/line disturbance.

3.3 Experimental Results

Proof-of-concept of the integrated fast-startup and enhanced bandwidth PFC controller is verified using the developed hardware of three-phase six-switch PFC converter with the specifications listed in Table 2.2. The PFC converter is tested in a wide range of operating conditions (variable AC source frequency) at 230V AC RMS input and nominal load power of 6kW. The whole set of experiments are classified into two major categories, associated with (a) faster output voltage loop (b) modified current loop with enhanced bandwidth and faster reference tracking.

The start-up experiments are conducted in the PFC stage, separately using PI compensator and the proposed integrated control strategy. Fig. 3.9 and Fig. 3.10 represent start-up waveforms (DC voltage, phase current & voltage) of PFC converter in case of PI compensation and integrated controller, respectively. From the experimental data, it is noted that the start-up times required in a 230V, 400Hz 6kW

PFC converter with a DC link reference voltage of 650V are 10 ms and 3 ms in cases of PI compensation and the proposed control, respectively.

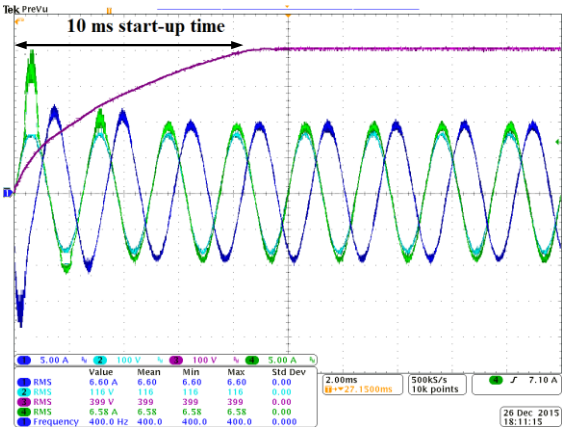


Fig. 3.9. PFC converter waveforms during start-up action with PI compensation

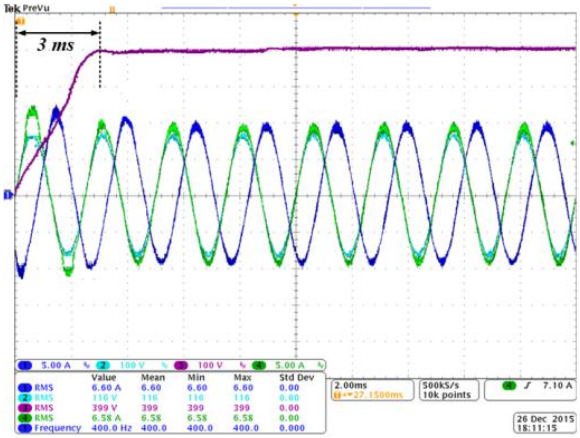


Fig. 3.10. PFC converter waveforms during start-up action with the proposed integrated control

Moreover, since the proposed integrated control takes care of minimizing the start-up time as well as transient current simultaneously, the start-up current with this control reduces to 10A from 23A. Additionally, in order to settle the DC link faster at 3ms using PI compensation, the start-up phase current goes up to 115A, which is even higher than the impulse current rating of the used semiconductor devices. Therefore, using linear PI compensation at the voltage loop with fast settling requirement may potentially bring into catastrophic device breakdown in the system. Furthermore, the

proposed control exhibits a superior performance in comparison to some of previous research works in terms of both start-up time and inrush current, which are 4 line cycles and 4 times rated RMS current in [70], 6 line cycles and 4 times rated RMS current in [59], respectively.

Furthermore, a set of experiments is carried out to test the regulation ability of the current loop in a PFC converter, operating at different AC source frequencies. Fig. 3.11 and Fig. 3.12 represent the PFC waveforms at the source frequencies of 400Hz and 800Hz, respectively with the PFC controller being designed for 400Hz source frequency. It is noted that although power factor is maintained at unity at 400Hz, in case of PI compensation it degrades to 0.951 at 800Hz AC frequency due to 18 degrees phase angle displacement, which matches with the theoretical calculation using Bode phase plot. To maintain the same active power flow, the phase current RMS magnitude goes higher than the rated reference value i.e. gain remains in the range of 0 to 10dB.

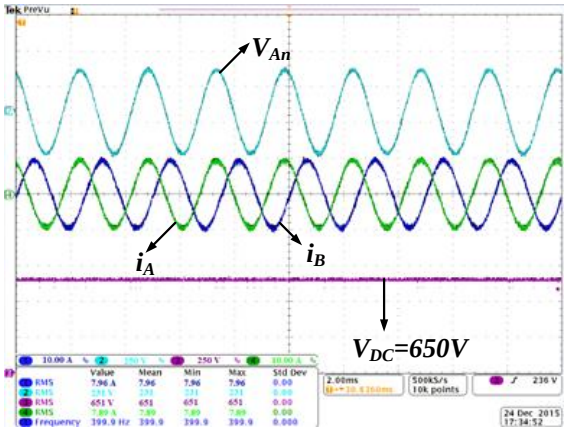


Fig. 3.11. 6kW PFC waveforms at 400Hz with the proposed control

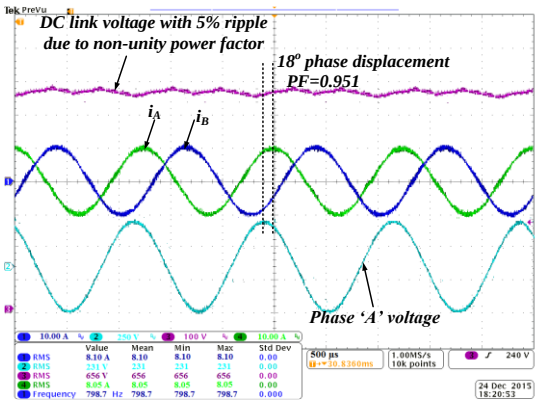


Fig. 3.12. 6kW PFC waveforms at 800Hz with the conventional control

Moreover, the implementation of the proposed control enables the PFC converter to maintain an input power factor more than 0.995 at the entire AC frequency range (400 Hz to 800 Hz), which in turn helps maintain a 0dB mid-band flat-top gain characteristics. This is demonstrated by capturing the PFC waveforms during a frequency transient between two extremums i.e. 400Hz to 800Hz, shown in Fig. 3.13.

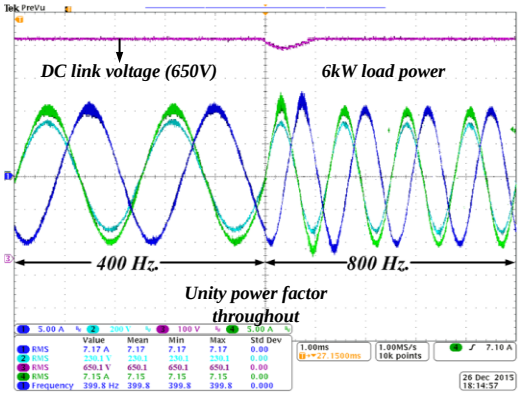


Fig. 3.13. Unity power factor at two extremum frequencies in the six-switch PFC at 6kW

Furthermore, in order to illustrate the effectiveness of the state-feedback control in conjunction with the proposed linear compensator, settling times of the DC link voltage to the reference value are noted under load transient from 6kW to 8kW. Fig. 3.14 and

Fig. 3.15 demonstrate the PFC waveforms under load transient with the conventional PI and the proposed integrated control respectively.

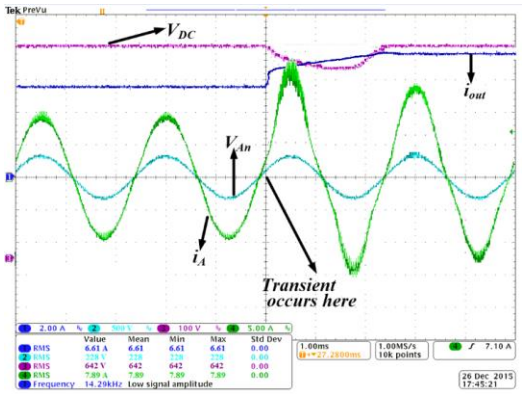


Fig. 3.14. PFC waveforms under load transient (6 kW to 8kW) with PI control

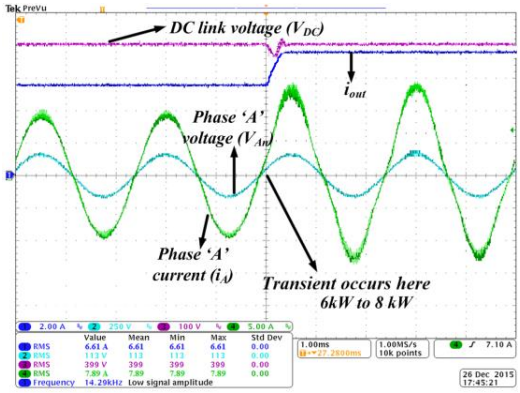


Fig. 3.15. PFC waveforms under load transient (6 kW to 8kW) with the proposed integrated control

The proposed control achieves 5% settling band within 0.2 ms, which is significantly faster than the conventional PI control, which takes 4ms (more than a line cycle) to settle. Placing the poles on the far left (with maintaining the current & voltage overshoot limits) provides freedom to maintain a fast tracking of the perturbed current reference in case of load transient. In order to illustrate the effectiveness of the proposed control structure, the start-up and steady state dynamics should be evaluated at extreme load conditions. Therefore, a set of experiments is conducted in order to demonstrate a

light load transient (from 1kW to 1.25kW and 1.25kW to 1kW) and a large step transient (from 1kW to 5kW using both proposed and PI compensations) separately, which are shown in Fig. 3.16 - Fig. 3.18.

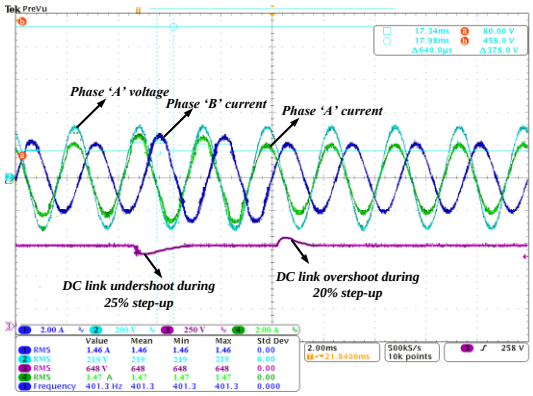


Fig. 3.16. Load transient of PFC converter from 1kW to 1.25kW and from 1.25kW to 1kW

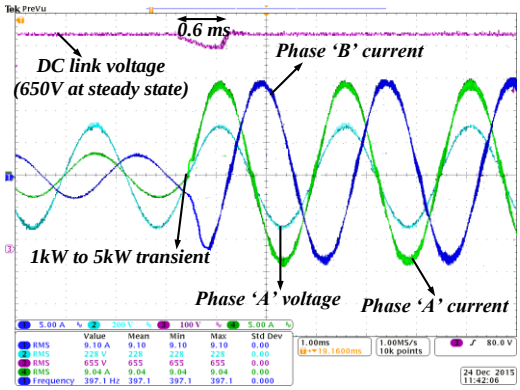


Fig. 3.17. Load transient of PFC converter from 1kW to 5kW using the proposed control

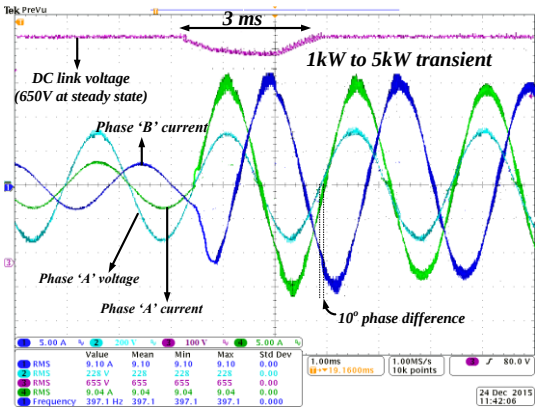


Fig. 3.18. Load transient of PFC converter from 1kW to 5kW using PI compensation

3.4 Summary

In this chapter, an integrated control strategy combining a fast start-up control and a well-regulated current loop with enhanced flat mid-band characteristics is introduced and analyzed. The proposed control strategy comprises of a non-linear compensator implemented in voltage loop and an adaptively tuned parameter-based current loop. The proof-of-concept is verified by experimenting a 6kW hardware PFC prototype at different AC source frequencies (from 400Hz to 800Hz) at 230V AC RMS input voltage. The start-up time and inrush current in case of the proposed control are reduced to 3ms & 10A from 10ms & 23A, obtained with the PI compensation. By proper pole placement method, the additional state-feedback compensation to the current loop enables 3.8 ms faster tracking of phase current reference under 30% load transient than a conventional linear PI control. Furthermore, the second order BPF-based current loop compensator as a part of the proposed control helps achieve a perfect unity (>0.995) PFC and accurate tracking of current reference.

Chapter 4: Phase-shifted full-bridge (PSFB) DC-DC converter for RTRU Applications

The third power conversion stage of RTRU is an isolated DC/DC converter according to our proposed architecture. Among the traditional DC-DC converter topologies, phase-shifted full bridge (PSFB) converters have drawn significant attention in medium-high power applications due to their simple structure and ZVS feature [90-92]. Unlike the resonant DC-DC topologies, the voltage gain of a PSFB converter does not depend on the switching frequency, rather only varies with the phase-shift angle between the duty cycles of any two diagonally located primary side switches. One of the most important considerations to achieve high-end conversion efficiency is to ensure ZVS at a wide range of load power. One of the biggest challenges designing a PSFB converter is maintaining ZVS at light load conditions, since it highly depends on the value of inductance and the switching frequency at low power. Increasing resonant inductance can help achieving ZVS in light load condition. However, increasing resonant inductance results in the duty cycle loss at the secondary side, additional dead-time conduction loss, and ringing across the secondary side rectifier [93-94]. An innovative maximum conversion efficiency tracking algorithm is proposed in this chapter, which is derived in Subsection 4.2.

In order to enhance the conversion efficiency without increasing the resonant inductance, several different methods have been proposed in the literature [94-103]. All of these methods require an add-on auxiliary circuit to ensure ZVS in a wide load range. An additional auxiliary transformer in series between the resonant inductor and

the PSFB transformer, and a capacitor connected on its secondary side is proposed in [94]. In this way, enough magnetizing energy can be supplied to the resonant inductor even at lighter load conditions. However, this additional energy will result in circulating current and conduction loss in the primary side, which may not improve the overall efficiency, even with ZVS. The circuit topology proposed in [95] utilizes an additional sub-circuit consisting of two inductors and two snubber capacitors, which result in circulating current due to resonance on the primary side. For a large output current application, this circulating current might be very high, which would introduce more conduction loss and potentially degrade the overall efficiency. In order to avoid these concerns, a voltage-doubler type rectifier is proposed in [96], which has lower circulating current and can achieve ZVS in both legs. However, it uses a very high value of leakage inductor, increasing the overall weight and also, experiences high current stresses on the secondary switches due to a larger deadtime.

Furthermore, a few methods [104-105] are proposed in order to improve the light load efficiency without using any auxiliary circuit components. Method presented in [104] discusses synchronous rectification (SR) turn-off schemes to create discontinuous conduction mode (DCM) of operation. The method proposed in [105] minimizes the secondary side conduction loss but does not address any approach for the overall loss minimization. Also, most of these methods need complex control and higher conduction losses in body diode of synchronous rectifiers.

A number of studies [106-114] have been done in improving the light load efficiency by achieving ZVS through modifying the circuit topology [106-107, 109] or improving the control technique [115]. Although the methods in [106-107, 109]

enhance the overall conversion efficiency at light loads (<1kW), the efficiency starts to fall down beyond a certain load range because of higher conduction loss in the auxiliary circuit components. This is especially true for the large output current applications. The method in [109] improves the efficiency by changing the dead-time over different loads but overlooks the effect of switching frequency on the overall efficiency, which does not ensure maximum efficiency. In addition, a variable switching frequency control of a PSFB DC-DC converter is proposed in order to enhance the conversion efficiency over a wide load range [114-115]. Although the proposed method in [115] shows improved efficiency in comparison to the fixed frequency control, the switching frequency calculation algorithm does not minimize the total power loss, and consequently it does not ensure maximum efficiency at all operating load powers.

In order to address and alleviate all the aforementioned issues related to the ZVS and efficiency improvement, a variable switching frequency control algorithm for efficiency maximization of the PSFB DC-DC converter is proposed in this chapter and this work is published in [152]. The total power loss is estimated considering switching frequency, device parameters, and component details, where the only variable parameter is the switching frequency except the phase-angle shift, which is reserved for voltage gain regulation. Thereby, a parametric minimization on the total power loss model is performed and it is found that the switching frequency corresponding to the minimum power loss does not depend on the component details. Rather, it depends only on the operating load power level. In addition, the proposed algorithm ensures validity of ZVS condition in the determined switching frequency. Otherwise, the model

derives another switching frequency at which the ZVS occurs at both the legs and ensures minimum power loss.

Furthermore, a state-feedback based control design approach is implemented to achieve a tight dynamic regulation on the PSFB converter output at any variable load and input voltage conditions. For regulating the output voltage at a reference level during a load transient, two sensors i.e. output voltage and load current sensors, are typically required to provide the required feedback information. One noteworthy point is that the weight of the current transformer for sensing the load current is quite high and takes a significant portion of the total weight of the converter, in the low-voltage high-current (>100A) secondary side. As an improvement, the proposed state-feedback based control strategy uses only one output voltage sensor and estimates the load current from the converter dynamics and switching information at the previous cycle. The detailed derivation regarding the estimation of the load resistance and load current is carried out in this chapter and a more comprehensive version is published in [117].

4.1 Basic Operation and design considerations

4.1.1 Modes of operation

A simplified circuit of the phase-shifted full bridge (PSFB) topology in a center-tapped configuration is shown in Fig. 4.1. MOSFETs S_1, S_2, S_3 and S_4 form the full bridge on the primary side of the transformer, T_1. S_1 and S_2 are switched with 50% duty ratio and 180^o out of phase from each other. Similarly, S_3 and S_4 are switched at 50% duty and 180^o out of phase with each other. The justification of selecting a center tapped configuration is to reduce the number of active semiconductors utilized on the high current side, i.e. to minimize the conduction loss in the switches.

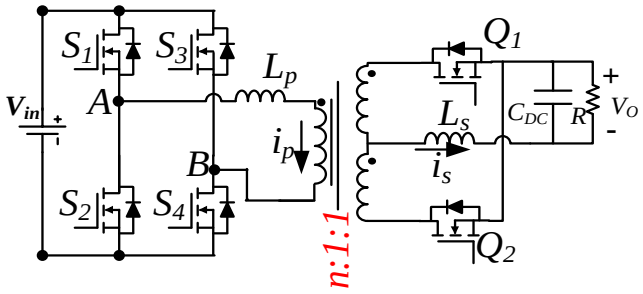


Fig. 4. 1. Basic structure of a center-tapped PSFB DC-DC converter.

The PWM switching signals for leg S_3 – S_4 of the full bridge are phase shifted with respect to those for leg S_1 – S_2. Amount of this phase shift decides the amount of overlap between diagonal switches, which in turn decides the amount of energy transferred. Q_1 and Q_2 provide rectification on the secondary side, while L_s and C_{DC} form the output filter. Inductor L_p provides assistance to the transformer leakage inductance for resonance operation with MOSFET capacitance and facilitates ZVS. Fig. 4.2 provides the switching waveforms for the system in Fig. 4.1.

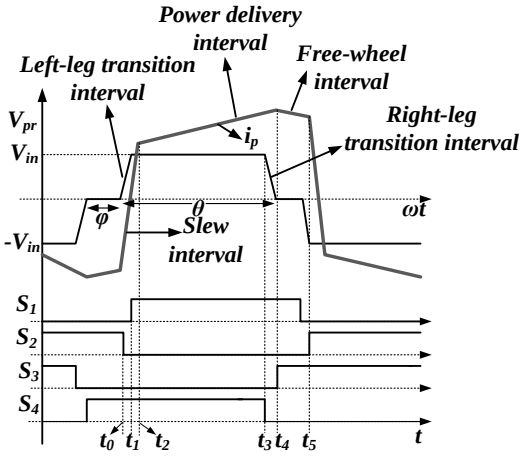


Fig. 4.2. Typical waveforms of primary voltage, primary current and gate pulses in a PSFB converter.

During ZVS phase-shift operation of the converter, there are five states in a half-cycle of operation. These states are briefly discussed due to the symmetric operation of the circuit.

A. Slew interval (t_0 to t_2):

This is the time interval when the primary current changes its flow direction. This time is established by primary input voltage level, load current and the total primary side resonant inductance, including the leakage inductance of the transformer and any additional inductance in the primary current path. Additional inductance may be required to store enough energy to displace the capacitive charge on the MOSFET output capacitance (C_{OSS}) and to offer realistic transition delay times.

B. Power delivery interval (t_2 to t_4):

This mode of operation is very similar to the conventional full bridge converter operation, when either of the two diagonally opposite switches (S_1 & S_4 or S_2 & S_3) are ON. Therefore, the applied voltage across the primary side of the transformer (including the additional leakage inductance) becomes V_{in} or $-V_{in}$, which results in power transfer to the load. The phase shift between diagonal switches determines the output voltage and total power transfer to the load side.

C. Free-wheeling interval (t_4-t_5):

During the freewheel time, reflected load current is circulated through the FET switches S_1 & S_3 or S_2 & S_4 and the voltage across the primary is zero. The freewheeling time increases with light loads for less power transfer and decreases with heavy loads for higher power transfer. In other words, the freewheeling time is a way for the controller to idle until the next appropriate state comes along. Fig. 4.2 shows the droop in primary current during this time, caused by conduction losses in the circulation path and output inductor ripple current.

D. Left-leg transition interval (t_0 - t_1):

The process of ZVS involves the charge displacement in the drain-source parasitic capacitances of the MOSFETs and occurs differently for the two legs of the primary side. During the left leg (S_1 & S_2) transition interval, the charge on the output capacitances of the A&B leg is displaced. For the left leg, the source of energy that displaces this charge is stored in the total primary resonant inductance. The displacement of this charge forces the voltage across MOSFET S_1 to zero (MOSFET S_2 ZVS occurs during the cycles second half), enabling zero voltage switching to take place. The charge is displaced in a time equal to one-fourth the resonant period, given by:

$$t_{LL} = \frac{\pi}{2} \times \sqrt{L_p' C_R} \tag{4.1}$$

Where, t_{LL} = Transition time for the left leg interval; L_p' = transformer leakage inductance + additional primary inductance and C_R = resonant capacitance, which is given by: $C_R = 4xC_{OSS}/3$, where The MOSFET output capacitance C_{OSS} is multiplied by 4/3 to approximate the average capacitance value during a varying drain-to-source voltage.

E. Right leg transition interval (t_3-t_4):

During this time interval, the full displacement of charge on the output capacitors of S_3 and S_4 happens and thus, terminates the power transfer interval. The reflected portion of the secondary current on the primary side supplies the energy for the full charge displacement, which ensures ZVS. Unlike the left-leg ZVS, the dynamics of capacitor discharge in this mode does not follow any resonating behavior, as the reflected output current behaves like a constant current source and discharges the output capacitances

of primary MOSFETs linearly. The ZVS transition time is given by the following relationship.

$$t_{RL} = \frac{C_R V_{in}}{I_p} \tag{4.2}$$

Since the source of energy for the discharging of output capacitors are directly load dependent, it is challenging to achieve ZVS at lighter loads. However, this does not pose a serious problem, as a variable switching frequency-based control method can potentially ensure the ZVS occurrence even at lighter loads without adding any hardware components, as proved in the next section of this research document.

4.1.2 Design considerations

The converter turns ratio is selected on the basis of the fact that the phase-shift duty (θ) should be limited in the range of 20% to 80% in order to reduce the peak primary current stress on the switches. The turns ratio (n) is selected to be 12:1:1 in the center-tapped configuration in our design based on the tradeoff between conduction loss (less at a lower '*n*') and core loss (higher flux density at a lower '*n*' for a fixed core cross-section). At 6kW rated load power, the secondary current is 214A, which would make secondary conduction loss one of the most dominant loss candidates and therefore, high-current side turn count is fixed at 1. A phase-shift duty ratio of 56% is required to enable the conversion from 650V to 31V DC. This is obtained from the simple voltage conversion relationship in a PSFB converter, as shown below.

$$V_{DC} = \frac{V_{in}(1-2\theta)}{n} \tag{4.3}$$

In order to ensure the core operation below magnetic saturation, the following inequality needs to be maintained and thus, minimum core window area can be

determined. This leads us to the requirement of E65/32/27 core, which can fit the required number of windings inside.

$$B_{\max} = \frac{V_{p-p} D_{\max} T_s}{N A_e} < B_{sat} \tag{4.4}$$

The similar constraints on field saturation are taken for selection the secondary inductor core and design of its number of turns. The selected core and material are E55/27/21 and 3C94, respectively.

Dimensioning of the resonant inductance with reference to the minimum load at which ZVS is required and the output capacitance of the used MOSFETs. In order to achieve soft switching (ZVS) at primary side, the primary current should lag the primary side voltage (V_{AB}). Therefore, in order to make the circuit inductive, a particular inductance is required to be in primary current path. Its value can be derived as:

$$L_{pri} \geq \frac{2C_{OSS} V_{in,\max}^{\ 2}}{\frac{I_{PP}}{2} - \frac{\Delta I_{L,out}}{2n}} - L_{lk} \tag{4.5}$$

Where, I_{PP} is the peak-primary current, L_{lk} is the leakage inductance value of transformer, C_{OSS} is the output capacitance of the MOSFET and $\Delta I_{L,out}$ is the peak-peak ripple of the secondary side rectified current.

Total calculated inductance value is 14µH, whereas the leakage inductance of the transformer is 6.5 µH. Therefore, an additional 7.5µH inductance is added. Considering a primary RMS current of ~10A, C058090A2 core is chosen for building the primary external inductor.

Since the secondary side current is 160A in nominal load conditions and can reach upto 320A in overload conditions, the conduction loss in the secondary side would be

the most significant loss in the whole system. Therefore, in order to improve the conversion efficiency significantly, minimizing the ON-state resistance of the secondary side rectifier should be as low as possible. Therefore, multiple MOSFETs (three in our design) are placed in parallel for realizing one switch and synchronous rectification (SR) is used for detecting the drain-source voltage of the MOSFET and the gate pulses are driven accordingly. Whenever the $V_{DS}<0$, SR drives high-logic gate pulse for that particular switch and the turning-off is controlled by the device current.

Primary switches are realized by the same MOSFETs (CMF10120D from Cree Inc.) as the PFC stage, as the voltage stress requirement is the DC link voltage, which is the same for the PFC stage. The specifications of the major components for the PSFB stage are listed in the following table.

Table 4.1. Key design parameters and their specifications

Parameters	Values	Quantity
Input voltage (V_{in})	650V	-
Output voltage reference (V_{o_ref})	31V	-
Output power (P_{out})	6kW	-
Transformer turns ratio (n)	12:1:1	-
Transformer core	E65/32/27, 3C94	1
Primary leakage inductance (L_p')	7.5 µH	
Secondary inductor (L_s)	30 µH	1
Secondary inductor core	E55/27/21, 3C94	1
DC link capacitor (C_{DC})	3.4 mF	1
Primary MOSFETs	SiC (1.2kV/24A)	4
Secondary MOSFETs	FDH055N15A (145A, 160V)	6

As a noteworthy design consideration, synchronous rectification is used to drive the secondary side MOSFETs to reduce the conduction loss and each secondary switch is realized by three MOSFETs in parallel for reducing the effective conduction resistance to 1.6 mΩ. This results in a total conduction loss of $2x80^2x0.0016 = 21W$ in the two sets of secondary MOSFETs at the rated power. The drain-source voltages of the secondary side rectification devices are sensed and accordingly, the synchronous rectification MOSFETs are driven by gate signals. UCC24610 is used as the SR controller IC and MIC4452 is used as a current buffer to drive multiple MOSFETs simultaneously.

4.2 Variable switching frequency maximum efficiency tracking control

4.2.1 Derivation of small signal plant characteristics

In order to control a phase-shifted full bridge converter at any switching frequency, it is important to design a control system, which will generate the reference value of the phase shift for achieving the reference output voltage at a particular load power. Therefore, the first requirement is to determine the frequency domain small signal transfer function $\Delta V_o/\Delta\varphi$, which can be split as the following.

$$\frac{\Delta V_o}{\Delta\varphi} = \frac{\Delta V_o}{\Delta V_{p1}} \times \frac{\Delta V_{p1}}{\Delta\varphi} \tag{4.6}$$

where, φ represents the phase-angle shift between two diagonally opposite switches and V_{p1} denotes the fundamental components of the primary voltage and V_o is the output voltage. In order to determine the AC voltage gain of the converter i.e. $\Delta V_o/\Delta V_{p1}$, the first harmonic approximation (FHA) equivalent circuit of PSFB shown in Fig. 4.3, is analyzed.

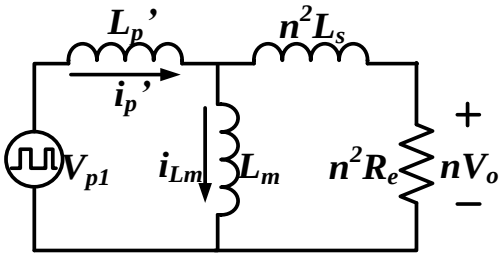


Fig. 4.3. Reduced equivalent circuit from FHA of PSFB converter.

Here, L_m is the magnetizing inductance of the transformer and R_e is the equivalent reflected AC resistance on the primary side, obtained from first harmonic approximation [105] i.e. $R_e = 8R/\pi^2$, where R is the original load resistance. Thereby, the overall voltage gain can be calculated as the following relationship, which shows a first order variation between the fundamentals of output voltage and primary side voltage.

$$\frac{V_o}{V_{p1}} = \frac{nR_eL_m}{(L_m + L_p')[s(n^2L_s + L_m \parallel L_p') + n^2R_e]} \tag{4.7}$$

$\Delta V_{p1}/\Delta\varphi$ i.e. the primary voltage variation with the phase-shift angle can be quantified by taking the ratio of the change in first harmonic amplitude of the primary voltage and the perturbation amount of the phase angle. For any phase shift angle φ, 'm'$^{\text{th}}$ harmonic amplitude of the primary voltage i.e. a_m can be determined as follows.

$$a_m = \frac{1}{\pi}\int_{<2\pi>} V_{pri}(t)\sin(nt)dt = \frac{V_{in}}{\pi}\left[\int_0^{\pi-\varphi}\sin(mt)dt - \int_{\pi}^{2\pi-\varphi}\sin(mt)dt\right] = \frac{V_{in}}{m\pi}[1+\cos(m\varphi)]\times[1-(-1)^m]$$

(4.8)

Accordingly, the first harmonic amplitude of the primary input voltage is formulated by the following relationships.

$$|V_{p1}| = \frac{2V_{in}}{\pi}(1+\cos(\varphi)) \tag{4.9}$$

Hence, $\frac{\Delta V_{p1}}{\Delta \varphi} = -\frac{2V_{in}}{\pi}\sin(\varphi)$ (4.10)

Therefore, the small signal transfer function between the output voltage and phase shift angle can be determined by multiplying Eq. (4.7) and Eq. (4.10), shown in Eq. (4.11), which is a first order system with a pole located at $p = n^2R_e/(n^2L_s+L_m||L_p')$.

$$\frac{\Delta V_o}{\Delta \varphi} = -\frac{2V_{in}}{\pi}\sin(\varphi)\frac{nR_eL_m}{(L_m + L_p')[s(n^2L_s + L_m \parallel L_p') + n^2R_e]} \quad (4.11)$$

Hence, this relationship could be framed as a typical first order system, as follows.

$$\frac{\Delta V_o}{\Delta \varphi} = \frac{A}{1+s\tau} \quad (4.12)$$

where, $A = -\frac{2V_{in}}{\pi}\sin(\varphi)\frac{L_m}{n(L_m + L_p')}$ (4.13)

$$\tau = \frac{n^2L_s + L_m \parallel L_p'}{n^2R_e} \quad (4.14)$$

4.2.2 Variable switching frequency state-feedback control

A state-feedback control algorithm is proposed for maintaining the output voltage at a fixed regulated value with a fast closed loop system dynamics, at any transient in load power or input voltage. The control system block diagram is shown in Fig. 4.4, where G_i corresponds to the gate pulse to the switch S_i ('i' = 1 to 4). The selected state variables ($\boldsymbol{x}$) of the converter are the primary current (i_p) and the instantaneous output voltage (v_o). The control variable (u) is the phase-shift between any two diagonal switches i.e. φ. One state space relation in Eq. (4.15) can be established by using the output voltage to phase shift transfer function in Eq. (4.12).

$$v_o + \tau\dot{v}_o = A\varphi \quad (4.15)$$

$$\dot{v_O} = -\frac{v_o}{\tau} + \frac{A}{\tau}\varphi \tag{4.16}$$

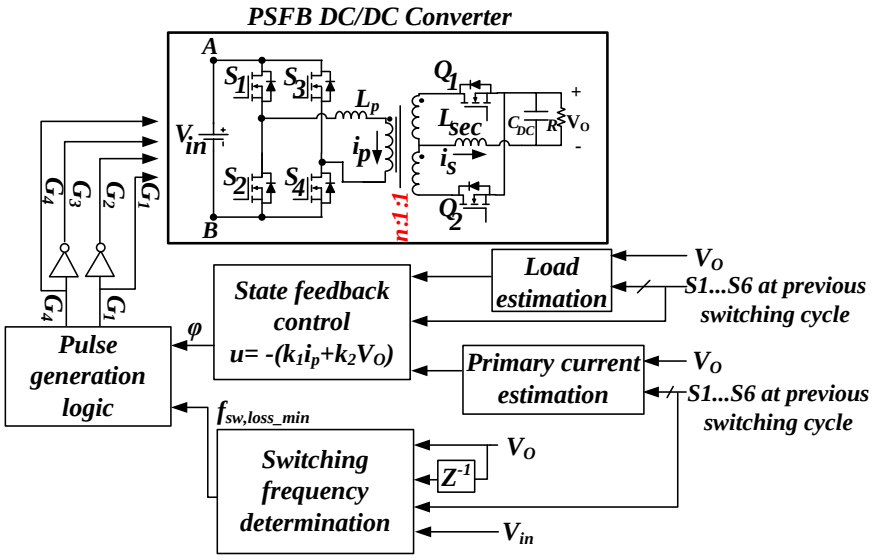


Fig. 4.4. Variable switching frequency state-feedback controller of PSFB converter.

Furthermore, from the voltage balancing at primary side i.e. Eq. (4.17) and applying $v_p = V_o\varphi$, the second state space relationship, shown in Eq. (4.18) can be formulated assuming $L_{eq} = n^2L_s + L_p$.

$$v_p = L_p\frac{di_p}{dt} + nL_s\frac{di_s}{dt} + nv_o \tag{4.17}$$

$$\frac{di_p}{dt} = -\frac{n}{L_{eq}}v_o + \frac{V_{in}}{L_{eq}}\varphi \tag{4.18}$$

Thereby, combining Eq. (4.16) and Eq. (4.18) and comparing with the state space equation for LTI systems i.e. $x' = Ax + Bu$, the matrices A and B are determined as follows.

$$A = \begin{pmatrix} 0 & -n/L_{eq} \\ 0 & -1/\tau \end{pmatrix} \tag{4.19}$$

$$B = \begin{pmatrix} A/\tau \\ V_{in}/L_{eq} \end{pmatrix} \tag{4.20}$$

Substituting $\boldsymbol{u = -kx}$ (where $\boldsymbol{k}=(k_1\ k_2)^T$ is a gain matrix), in the state space equation and taking its Laplace transformation, it is found that eigenvalues of the matrix ($\boldsymbol{sI-A+Bk}$) have to lie on the left-half plane in order to ensure stability of the system. Since the eigenvalues of ($\boldsymbol{sI-A+Bk}$) are same as the solutions of det ($\boldsymbol{sI-A+Bk}$) = 0, Routh-Hurwitz criterion could be applied to find the conditions for obtaining negative eigenvalues [99].

$$(sI - A + Bk) = \begin{pmatrix} s + \frac{Ak_1}{\tau} & \frac{n}{L_{eq}} + \frac{Ak_2}{\tau} \\ \frac{V_{in}k_1}{L_{eq}} & s + \frac{1}{\tau} + \frac{V_{in}k_2}{L_{eq}} \end{pmatrix} \tag{4.21}$$

$$\det(sI - A + Bk) = s^2 + s(\frac{1 + Ak_1}{\tau} + \frac{V_{in}k_2}{L_{eq}}) + (\frac{Ak_1}{\tau^2} - \frac{V_{in}k_1 n}{L_{eq}^2}) \tag{4.22}$$

After applying the Routh-Hurwitz criterion on ***det (sI-A+Bk)=0***, the following constraints on the gain matrix parameters are obtained; $k_1>0$; $k_2<(L_{eq}(1+Ak_1)/\tau V_{in})$. Moreover, since A and τ depend on the system variables V_{in} and R, the inequalities on k_1 and k_2 should take care of any variations in the load power and input voltage. In this case, R can be estimated from the detailed modeling of the converter dynamics and switching pulse information, as explained and derived in Section IV. A and τ would be calculated at each interrupt cycle from the measured state variables and phase-shift amount at the previous switching cycle and accordingly, k_1, k_2 could be updated.

4.2.3 Frequency dependent power loss model

For achieving ZVS at the lower load power, higher value of inductance is required in order to sink the enough energy from the parasitic drain-source capacitances to discharge them fully. Besides increasing the inductance value for ensuring ZVS, alternatively the switching frequency can be tuned to ensure ZVS at all switches. The

main objective of tuning switching frequency at different load powers is to manipulate the phase lag of the net input impedance and ensure that it is inductive in nature. Therefore, it is necessary to investigate the equivalent input impedance of the PSFB converter. Let, V_1 be the instantaneous primary side voltage, created due to linked flux and V_p is the instantaneous voltage across the primary side of the transformer including the leakage inductance. Therefore, the following relationships can be established from the analyses on the primary and secondary sides of the transformer.

$$V_p = L_p' \frac{di_p}{dt} + V_1 \tag{4.23}$$

$$\frac{V_1}{n} = L_s \frac{di_s}{dt} + V_o \tag{4.24}$$

$$i_s = C \frac{dV_o}{dt} + \frac{V_o}{R} \tag{4.25}$$

Taking the Laplace transformation on Eq. (4.23)-Eq. (4.25) and using $i_s(s) = ni_p(s)$, the following relationship is obtained.

$$Z_{in}(s) = \frac{s^2 RCL_{eq} + sL_{eq} + nR}{sCR + 1} \tag{4.26}$$

where, $L_{eq} = L_p' + n^2 L_s$. Therefore, the net phase lag of the input impedance can be formulated as Eq. (4.27).

$$\varphi_{lag} = \tan^{-1}\left(\frac{\omega L_{eq}}{nR - \omega^2 RCL_{eq}}\right) - \tan^{-1}(\omega CR) = \tan^{-1}\left[\frac{\omega(L_{eq} - nR^2C + \omega^2 R^2 C^2 L_{eq})}{nR}\right] \tag{4.27}$$

The frequency response of $Z_{in}(s)$ is shown by a Bode plot in Fig. 4.5, which represents that both the impedance magnitude and phase lag increase as the frequency increases. In terms of fulfillment of ZVS, minimum time lag (t_L) between the fundamental primary current and primary voltage must be 1/4th of a resonant cycle i.e. $\pi\sqrt{(L_p' C_R)}/2$, where,

$C_R = 4C_{OSS}/3$ and C_{OSS} is the output capacitance of each primary side MOSFET. Hence, the condition of the inductive phase lag of the input impedance being more than ωt_L i.e. Eq. (4.28) and Eq. (4.29) must be valid in order to ensure the ZVS operation.

$$\tan^{-1}\left[\frac{\omega(L_{eq} - nR^2C + \omega^2R^2C^2L_{eq})}{nR}\right] > \frac{\omega\pi}{2}\sqrt{L_p'C_R} \tag{4.28}$$

$$F(\omega) = \frac{\omega\pi}{2}\sqrt{L_p'C_R} - \tan^{-1}\left[\frac{\omega(L_{eq} - nR^2C + \omega^2R^2C^2L_{eq})}{nR}\right] < 0 \tag{4.29}$$

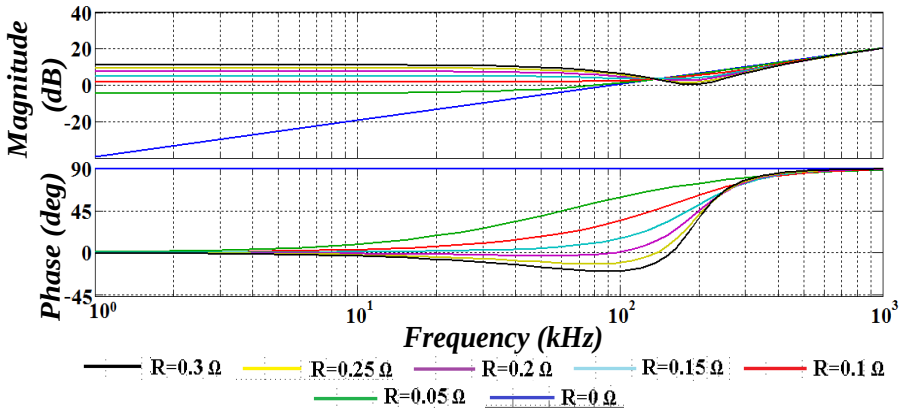


Fig. 4.5. Bode plot of the input impedance of PSFB converter.

The cut-in frequency above which the ZVS is confirmed, varies with output load power. The cut-in frequency (ω_c) can be determined from the equality condition of the inequality and is represented by the frequency axis intercept of $F(\omega)$ vs f(i.e. $\omega/2\pi$) curve, shown in Fig. 4.6, for different load conditions.

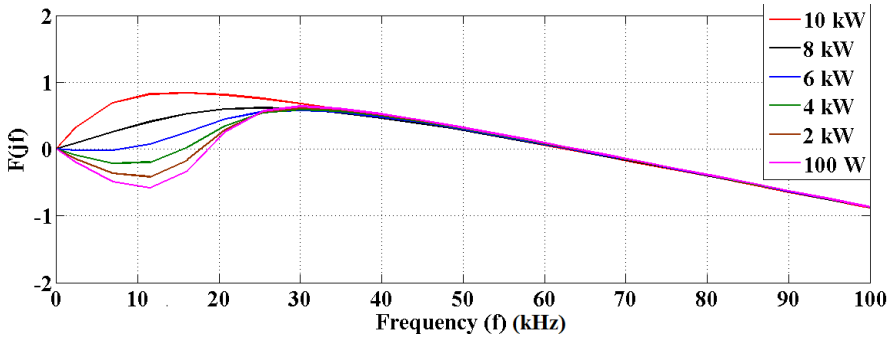


Fig. 4.6. Variation of cut-in frequency of ZVS occurrence in PSFB converter.

As can be seen from Fig. 4.6, the frequency intercept for all the load powers ranging from 100W to 10kW is around 60 kHz. According to Eq. (4.29), $F(\omega)$ has to be negative as a compulsory ZVS condition. Therefore, the ZVS is confirmed at the frequencies above 60 kHz for all the load powers from 0.1kW to 10kW.

4.2.4 Maximum efficiency tracking algorithm

As a broad objective of this work is to maximize the conversion efficiency at all operating points, it is required to perform loss modeling and minimize the total power loss by tuning the switching frequency. The main task is to determine the switching frequency, at which the total power loss would be minimum and to make the converter operate at that switching frequency if ZVS condition also satisfies simultaneously. The loss model assumes the primary side turn-on loss to be zero assuming ZVS operation of all the switches. First priority in the process of selection of switching frequency would be to minimize the total loss and also, to simultaneously ensure ZVS operation. If ZVS does not occur at the switching frequency with minimized loss, then a switching frequency satisfying Eq. (4.29) would be chosen. The reason is that as the frequency decreases, input impedance reduces according to Eq. (4.26), the current stress increases on both the primary and secondary sides, and the conduction loss increases and dominates the other losses in large output current applications. Therefore, a higher switching frequency, satisfying the ZVS condition in Eq. (4.29) should be selected for overall loss minimization. A flowchart depicting the switching frequency selection is shown in Fig. 4.7. Although the loss model is quite dependent on the design parameters of the system, the calculated switching frequency

for the minimized loss is proven to be independent of the device specifications and component details, and rather just a function of load power.

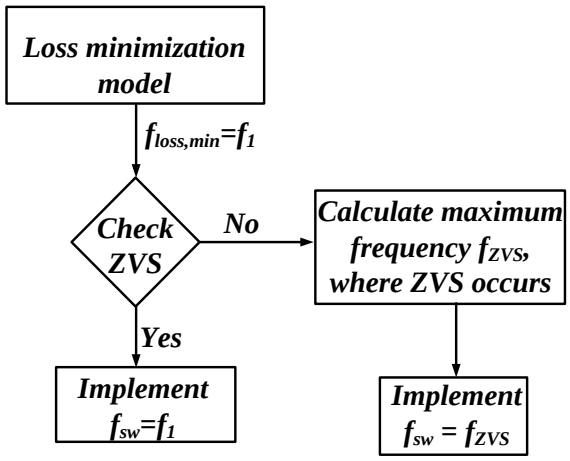


Fig. 4.7. Flowchart for the switching frequency selection procedure.

The total power loss, shown in Eq. (4.30) in the PSFB converter could be split into four major categories i.e. primary conduction loss ($P_{pri,cond}$), secondary conduction loss ($P_{sec,cond}$), transformer core loss (P_{core}) and primary side turn-off loss (P_{off}).

$$P_{tot} = P_{off} + P_{pri,cond} + P_{\sec,cond} + P_{core} = \frac{V_{pri,rms} I_{pri,rms} t_{off} f_{sw}}{2} + I^2_{pri,rms} R_{pri,cond} + I^2_{\sec,rms} R_{pri,cond} + k f_{sw}^2$$
$$= \frac{V^2_{pri,rms} t_{off} f_{sw}}{2|Z_{in}(s)|} + \frac{V^2_{pri,rms} R_{pri,cond}}{|Z^2_{in}(s)|} + \frac{n^2 V^2_{pri,rms} R_{pri,cond}}{Z^2_{in}(s)} + k f_{sw}^2 \quad (4.30)$$

Here, $V_{pri,rms}$, $R_{pri,cond}$ and $R_{sec,cond}$ are the primary side RMS voltage and conduction resistance of the primary & secondary MOSFETs. For a switching frequency of f_{sw}, the total power loss can be formulated as follows.

$$P_{tot}(f_{sw}) = \frac{k_1 f_{sw}}{Z_{in}(f_{sw})} + \frac{k_2}{Z^2_{in}(f_{sw})} + k_3 f_{sw}^2 = \frac{k_1 f_{sw} Z_{in}(f_{sw}) + k_2 + k_3 f_{sw}^2 Z^2_{in}(f_{sw})}{Z^2_{in}(f_{sw})} \quad (4.31)$$

where, $k_1 = V^2_{pri,rms} t_{off}/2$; $k_2 = V^2_{pri,rms} R_{pri,cond}$, $k_3 = k$. The optimum switching frequency at which the total power loss would be minimum can be determined by solving

$dP_{tot}(f_{sw})/df_{sw}$ = 0. Substituting the $|Z_{in}(s)|$ at $f=f_{sw}$ in the power loss expression and equating its derivative to zero, the following relationship is obtained.

$$k_1 Z_{in}(f_{sw}) Z_{in}'(f_{sw}) - k_1 f_{sw} Z_{in}(f_{sw}) Z_{in}'(f_{sw}) - 2k_2 Z_{in}'(f_{sw}) + k_3 Z_{in}^{\ 2}(f_{sw}) Z_{in}'(f_{sw}) = 0 \quad (4.32)$$

From the above equation, one straightforward solution could be obtained as $Z_{in}'(f_{sw})=0$, which leads to the following relationships by differentiating Eq. (4.26) with respect to $s=f_{sw}$.

$$\frac{f_{sw}^{\ 2} R^2 C^2 L_{eq} + 2RCL_{eq} f_{sw} + L_{eq} - nR^2 C}{(RCf_{sw} + 1)^2} = 0 \quad (4.33)$$

Hence, $$f_{sw} = \frac{\sqrt{4R^2C^2L_{eq}^{\ 2} + 4R^2C^2L_{eq}(nR^2C - L_{eq})} - 2RCL_{eq}}{2R^2C^2L_{eq}} = \left(\sqrt{\frac{n}{CL_{eq}}} - \frac{1}{RC}\right) \quad (4.34)$$

As can be seen from Eq. (4.34), the commanded switching frequency from the loss minimized model is independent of the design dependent parameters, such as k_1, k_2, and k_3. Although there are other multiple solutions to Eq. (4.32), all of them are dependent on k_1, k_2, and k_3, and thus, generate a switching frequency being dependent on the design specifications and component details. Those solutions may potentially generate misleading values of switching frequencies, upon the slight variation of component parameters with other physical parameters. Therefore, the solution from $Z_{in}'(f_{sw})=0$ is considered as the optimum switching frequency, which is only dependent on the output load power. From the established relationship in Eq. (4.34), it is understood that the switching frequency should be increased as the load resistance increases and vice-versa. Therefore, a higher switching frequency is desired in order to reduce the total loss at a lighter load condition. Again, in order to maintain the ZVS, the switching frequency should maintain the condition mentioned in Eq. (4.29), (i.e. f_{sw}> 60 kHz for our design considerations).

Since there will be no load resistance sensing in the real time implementation, *R* should be determined or estimated from the known measured system variables, in order to generate a frequency command according to Eq. (4.34). Differentiating Eq. (4.25) and substituting di_s/dt in Eq. (4.24), the relationship at Eq. (4.35) can be formulated and discretized at k^{th} sample in Eq. (4.36).

$$\frac{V_1}{n} = L_s\left(C\frac{d^2V_o}{dt^2} + \frac{1}{R}\frac{dV_o}{dt}\right) + V_o \tag{4.35}$$

$$\frac{V_1(k)-V_1(k-1)}{n} = L_s\left(\frac{V_o(k)-2\times V_o(k-1)+V_o(k-2)}{{T_s}^2}\right) + \frac{L_s}{R}\times\frac{V_o(k)-V_o(k-1)}{T_s} + V_o(k) \tag{4.36}$$

where, T_s is the sampling time of the closed loop implementation. From the sensor measurements, output voltages at k^{th} and $(k\text{-}1)^{th}$ samples are known to us. Furthermore, $V_1(k)$ and $V_1(k\text{-}1)$ will be either V_{in} or $-V_{in}$ or 0, which will be known to us from the input voltage and the primary switching pulse information. Thus, the unknown value of load resistance i.e. *R* could be estimated using the relationship, established in Eq. (4.36). Consequently, the primary current (i_p) at 'k'$^{\text{th}}$ sample can also be estimated according to Eq. (4.37), using the fundamental relationships, Eq. (4.23)-Eq. (4.25).

$$i_p(k) = \frac{i_s(k)}{n} = \frac{1}{n}\left(C\frac{V_o(k)-V_o(k-1)}{T_s} + \frac{V_o(k)}{R}\right) \tag{4.37}$$

4.2.5 Simulation and Experimental Results

In order to verify the proposed control methodology, the converter is simulated with a DC voltage of 650V at a rated nominal power of 6kW with 28V output DC voltage reference for the application of auxiliary power supply in a more-electric-aircraft. The simulation is performed in PSIM and the obtained results are shown in Fig. 4.8. The

PSFB converter is designed based on the well-established design considerations, presented in the literature [117-118]. The key design parameters and specifications are previously summarized in Table 4.1. As a noteworthy design consideration, synchronous rectification is used to drive the secondary side MOSFETs to reduce the conduction loss and each secondary switch is realized by three MOSFETs in parallel for reducing the effective conduction resistance.

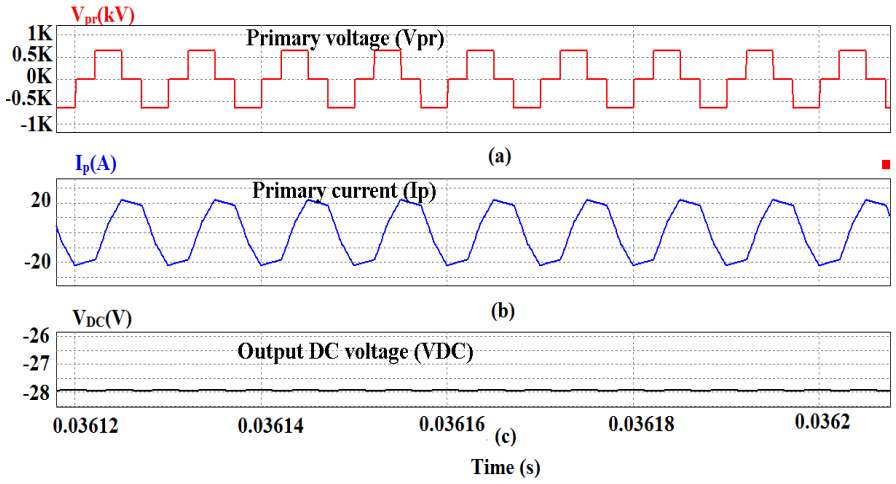


Fig. 4.8. Simulation results of PSFB converter (a) Primary voltage (V_{pr}) (b) Primary current (i_{pr}) (c) Output DC voltage (V_{DC})

As a proof-of-concept verification to the proposed control methodology, a laboratory prototype of 6kW (continuous)/8kW (peak) PSFB converter, shown in Fig. 4.9 is designed and developed. The control algorithm is implemented in a floating point DSP platform TMS320F28335.

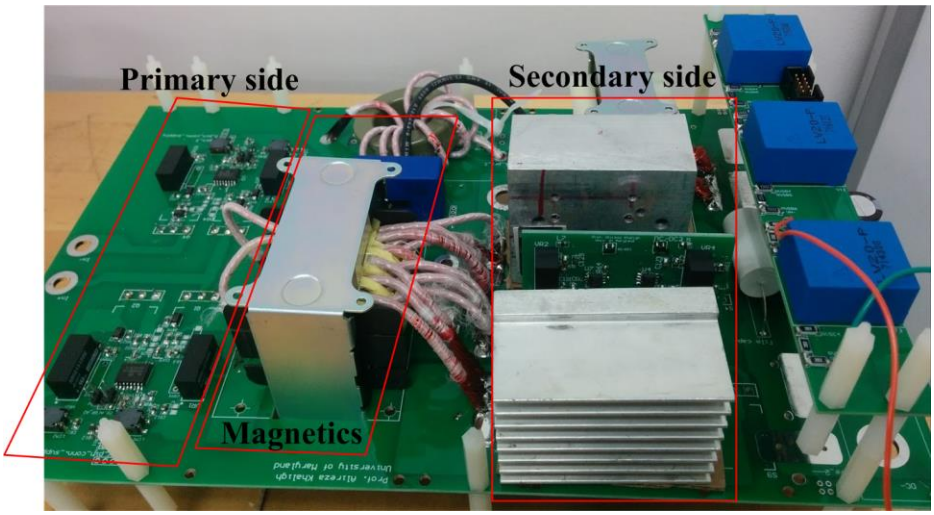


Fig. 4.9. Photo of the PSFB DC-DC experimental setup

Fig. 4.10 shows the steady state operation of the converter at 650V DC input and 6kW. The output DC voltage is settled at 28V DC with a ripple within ±1%. The secondary inductor current is averaged around 214 A with a ripple of ±10% and it is of twice the switching frequency, as the voltage across the inductor is rectified form of the linked secondary voltage. The ZVS occurrence of the primary side MOSFETs is demonstrated by the Fig. 4.11, which shows a 200ns deadtime between complete fall of drain-source voltage and the turn-on of gate pulse.

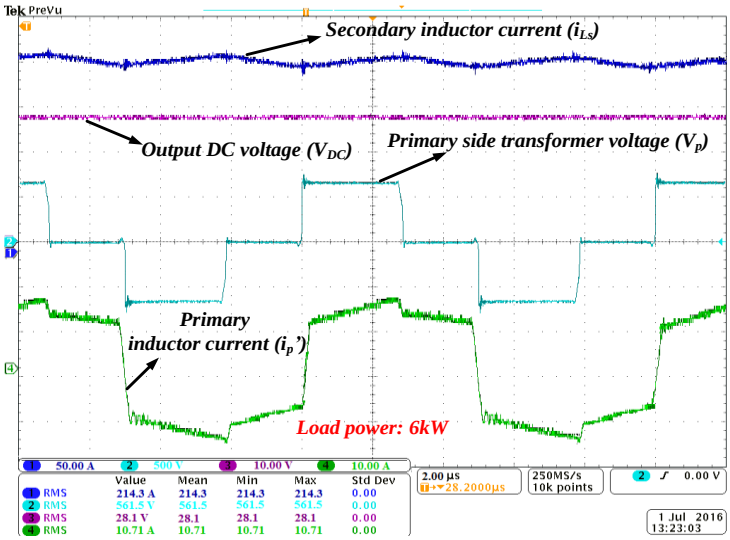


Fig. 4.10. PSFB waveforms at 6kW load power; V_{in} = 650V, V_O = 28V, Output current: 214.3A.

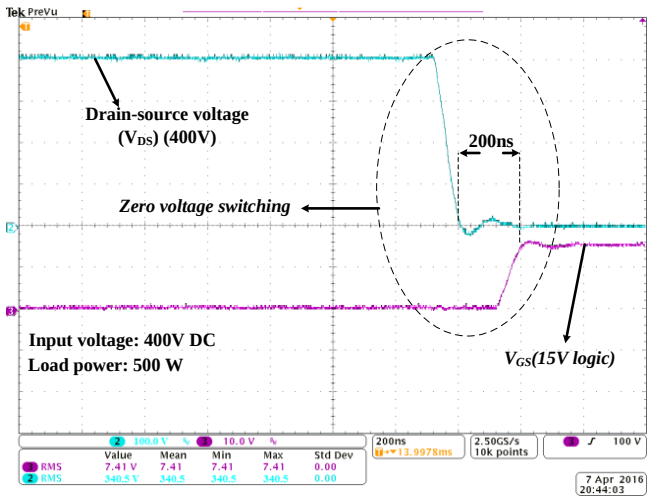


Fig. 4.11. ZVS in PSFB converter at 500W load power V_{in} = 400V, V_O = 20V, Output current: 25A.

Furthermore, the converter is also tested in different load and line conditions to check the accuracy of the proposed control logic at variable operating conditions. A 33% step-increment in load from 6kW to 8kW is applied during a running condition with nominal load, and the output voltage is settled at its reference value within 5µs with the state-feedback control approach, as shown in Fig. 4.12. It takes 12.5 µs to settle to the steady state under the same load transient with a PI controller, shown in Fig. 4.13. In addition, the undershoot in the output DC voltage under this load transient with the state-feedback and PI controller are 30% and 12% of the reference value, respectively, which prove the state-feedback control to be superior than PI in terms of dynamics and regulation of this converter. The output voltage ripple is maintained below ±1% at the steady state of the overload condition. It is also observed that there is a dynamic change in switching frequency from 100 kHz to 83 kHz as soon as the load is changed from 6kW to 8kW. The fact that these frequencies match well with the optimum switching frequencies in Table 4.2, proves high accuracy of the proposed control.

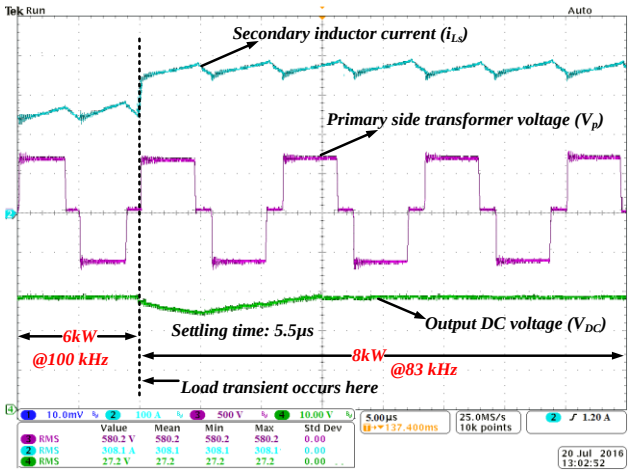


Fig. 4.12. PSFB waveforms at load transient from 6kW to 8kW in variable switching frequency, state-feedback control; V_{in} =650V, V_O = 28V, f_{sw} = 100 kHz @6kW and f_{sw} = 83kHz @8kW.

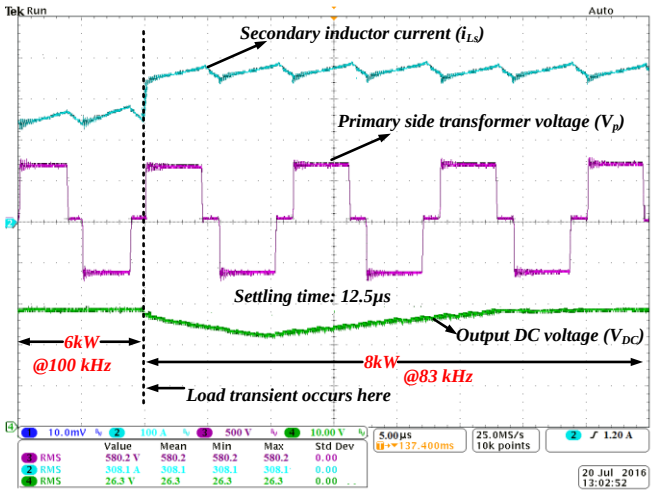


Fig. 4.13. PSFB waveforms at load transient from 6kW to 8kW in variable switching frequency, PI control; V_{in} =650V, V_O = 28V, f_{sw} = 100kHz @6kW and f_{sw} = 83kHz @8kW.

The converter is tested at different operating points in a wide range of load power (from 100W to 9kW) and variable switching frequencies in the range of 50 kHz to 220 kHz, listed in Table 4.2, as reported by the switching frequency calculating model for maximum efficiency operation of the converter at different load conditions. The measured efficiencies at the whole load power range with the proposed control are more than the reported peak efficiency values in the previous related works i.e. 95.6% in

[115], 91% in [107] and 92.8% in [109]. This proves the justification of the effect of variable switching frequency to track the maximum attainable efficiency at a particular load. In order to validate the improved performance by the variable switching frequency control, a graph demonstrating a comparison of conversion efficiencies at different load powers between the proposed control and a fixed frequency control method at 50 kHz is shown in Fig. 4.14, which clearly indicates an improved efficiency value at all the operating points. If the PSFB converter is operated at a switching frequency of 100kHz (same as PFC stage), the measured efficiency is reported as 97.2% at 6kW rated load.

Table 4. 2. Optimum switching frequencies at different load powers and efficiency comparison with fixed-frequency control at 50 kHz

Load power (kW)	$f_{sw,loss\_min}$(kHz)	Efficiency at $f_{sw,loss\_min}$	Efficiency at 50kHz
0.1	180	95	93
1	170	97	96.2
2	158	98.1	97.1
3	145	98.2	96.9
4	130	98.15	96.8
5	114	98.1	96.8
6	100	98.1	96.65
7	92	98.1	96.6
8	83	98.05	96.6

9	75	98	96.5
10	65	97.9	96.5

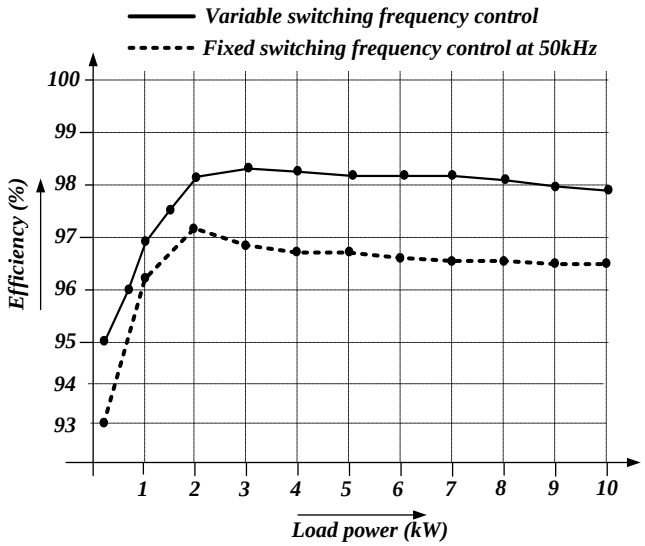


Fig. 4.14. Efficiency comparison between fixed and variable frequency control at different load power levels

4.3 Summary

In this chapter, a new control methodology, incorporating variable switching frequency operation at different load power levels in a PSFB DC-DC converter, is proposed to maximize the conversion efficiency. In addition, a state-feedback based control method is designed to regulate the PSFB converter at variable load and input voltage condition, with the elimination of a load current sensor. With implementation of this control, ZVS can be achieved at all power levels with just using transformer leakage inductance and removing any additional primary inductor.

As a proof-of-concept verification, a 6kW laboratory prototype of a PSFB DC-DC converter is designed and tested with 650V to 28V conversion specification for the

application of auxiliary power supply in a more-electric-aircraft. According to the experimental results, a maximum conversion efficiency of 98.1% with an output voltage ripple below ±1% is achieved and the converter dynamics becomes 7μs faster in 33% load transient through a state-feedback control in comparison to a PI controller. Furthermore, the experimental results exhibit higher conversion efficiencies at a wide load power range (100W-10kW) with variable switching frequency in comparison with a fixed switching frequency method.

Chapter 5: Electromagnetic Interference (EMI) Filter for RTRU Applications

Avionic systems must strictly comply with EMI standards while ensuring high reliability, and satisfying very high efficiencies, less weight, and high level of compactness [120]. Evolutions and rapid advancements in the high-power and high-speed semiconductor devices have enabled wide band gap-based converters with eliminated lower order harmonics in the input current waveforms; however, they exhibit a large high-frequency noise in the input line currents. A conventional approach to attenuate the higher-order harmonics has been to use passive components such as inductors and capacitors in combination with damping resistors. Utilization of the passive components makes the system bulky and less efficient, and thus reduces the volumetric and gravimetric power density. The only way to reduce the weight and size of the system is increasing the switching frequency, which currently might not be possible at higher power levels and would need computationally complex control logic [121].

EMI is transmitted in two forms, radiated noise and conducted noise. Radiated noise occurs in the range of 30MHz-1GHz, whose filtering requires the measurement of magnetic or electric fields in free space, causing the testing to become much more complex, and is out of the scope of this research. Conducted EMI as a major part of the noise contents consists of two categories commonly known as differential mode (DM) noise and common mode (CM) noise. The CM noise originates due to charging and discharging of parasitic capacitances, such as the capacitances between heat sink and

ground, the transformer inter-winding capacitances, measurement probe setup. On the other hand, magnetic coupling, and ringing in switching signals cause DM noise.

As the behavior of DM noise can be well predicted, multistage LC filters can be placed in the front end of PFC stage to achieve the required attenuation. As an improvement to the conventional multistage filtering action, a "zero-ripple" DM filter concept can be implemented [122-125]. On a different note, it is very difficult to identify and model CM noise and thus, challenging to design a filter, which can offer sufficient attenuation to meet standard requirements. In [126, 127], a CM-noise modeling approach was proposed for a single-phase PFC system, which considers the parasitic capacitances of power semiconductor devices to the heatsink. A few work on CM noise sources and propagation methods are also introduced for three-phase rectifier systems [128-135]. These work only include limited information on noise modeling of the converter and mainly contain the guidelines for the optimized design of EMI filter components. However, in order to design compact EMI filters, the most important information required are the values of the design corner frequencies of the converter. Since, the parasitic components in a converter majorly determine the CM corner frequencies, it is quite important to model the possible sources of noise in the converter for accurately locating the possible corner frequencies. Otherwise, an intuitive approach would require more number of filter stages to be put in cascade, in order to achieve the required noise attenuation and meet the standard requirements. In this research, the CM noise modeling technique for single-phase PFC [126, 130] will be extended to three-phase systems with detail mathematical validations. In addition, an EMI filter design and implementation for an ultra-compact three-phase active boost

rectifier will be presented. The research also discusses several important techniques to improve CM spectrum performance and also improve the baseline spectrum of the testing environment.

Another important stage for a complete design of EMI filter is to sufficiently attenuate the DM noise, which consists of a lower range of frequencies (<1MHz) than CM noise. Although DM noise attenuation to a certain extent is achievable by applying multi-stage filters [135, 136], DM stage filter adds the highest weight and size among the filter components to the integrated EMI & PFC stages, and adds an input displacement phase to the input currents, degrading the input power quality [137]. EMI filter design in [137] consists of conventionally existing three cascaded LC stages, where the corner frequency of each of these stages is determined from the converter performance without any filtering action and the target EMI requirements. Each EMI filter stage consists of three X-capacitors (DM), three Y-capacitors (CM), one common mode choke (L_C) and three differential mode inductors L_D (one in each input phase). However, as opposed to the conventional design method, it is theoretically possible and implementable to design the filter stage with three X capacitors and only one Y capacitor per stage in a new configuration, reducing the total weight and size of the system, which is proposed in this research. The performed study also shows that the proposed filter topology can offer same amount of attenuation as the conventional cascaded LC topology, with additional benefits of reduced number of LC components, less number of cascaded stages, much more compact size and a higher power density and minimum input phase displacement.

5.1 RTRU noise model

In order to design EMI filter stage to meet the standard requirements, an effective action would be to model the parasitic noise effects in a three-phase boost PFC circuit. Some of the strong sources of EMI generation are semiconductors and heatsinks attached to them. In many of the designs, the semiconductors are mounted on a common heatsink, which is connected to the protective earth. The parasitic capacitances between heatsink and ground should be considered in the noise modeling of the converter. In this section, a detailed review of noise components in a three-phase active boost rectifier is provided.

5.1.1 Three-phase PFC Noise Components

It is not easily possible to separate common mode (CM) and differential mode (DM) noises in a three-phase system. An orthogonal decomposition of three-phase variables is required to split them into CM and DM. Assuming i_1, i_2, i_3 to be the CM noise components of the phase currents i_a, i_b and i_c respectively, the CM (i_{CM}) and DM mode current components (i_{DM1}, i_{DM2}, i_{DM3}) can be determined using the following orthogonal relationship, presented in Eq. (5.1) with an additional relation $i_{DM1}+i_{DM2}+i_{DM3}=0$ and this orthogonal split model is framed in Fig. 5.1.

$$\begin{pmatrix} i_{DM1} \\ i_{DM2} \\ i_{CM} \end{pmatrix} = \frac{1}{3}\begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & 1 \\ 1 & 1 & 1 \end{pmatrix}\begin{pmatrix} i_1 \\ i_2 \\ i_3 \end{pmatrix} \tag{5.1}$$

The above transformation is valid if the three-phase system is symmetrical, linear and time invariant. Regardless of the type of three phase source and its noise sources, CM component of the phase current flows through a phase and takes the return path through

ground. From the above transformation equations, common mode noise component (i_{CM}) is given by the following.

$$i_{CM} = \frac{i_1 + i_2 + i_3}{3} \tag{5.2}$$

For a more comprehensive analysis, a generalized high-frequency noise model in a three-phase PFC circuit is shown in Fig. 5.1, which represents the CM components as series combinations of CM voltage sources and equivalent CM impedances. On the other hand, each DM noise component flows through a phase and returns through other two phases, which implies that $v_{DM1}+v_{DM2}+v_{DM3}=0$. DM noise components are modeled by three independent voltage sources in series with three differential mode impedances.

Since, the EMI spectrum is measured by line impedance stabilization network (LISN), the LISN impedances should also be considered in the path of each phase current flowing towards the protective earth. The CM voltage magnitude at the LISN is formulated by the following relation, where v_1, v_2 and v_3 represent the voltage drops due to CM noises across the LISN impedances of three phases A, B and C, respectively.

$$v_{CM} = R_{LISN} \frac{i_1 + i_2 + i_3}{3} = \frac{v_1 + v_2 + v_3}{3} \tag{5.3}$$

where, R_{LISN} is impedance between output of LISN and ground. Since, the noise source at each phase is modeled by a sum of corresponding CM and DM components, the DM equivalent voltage at '*i*'th phase is calculated by the following relationship.

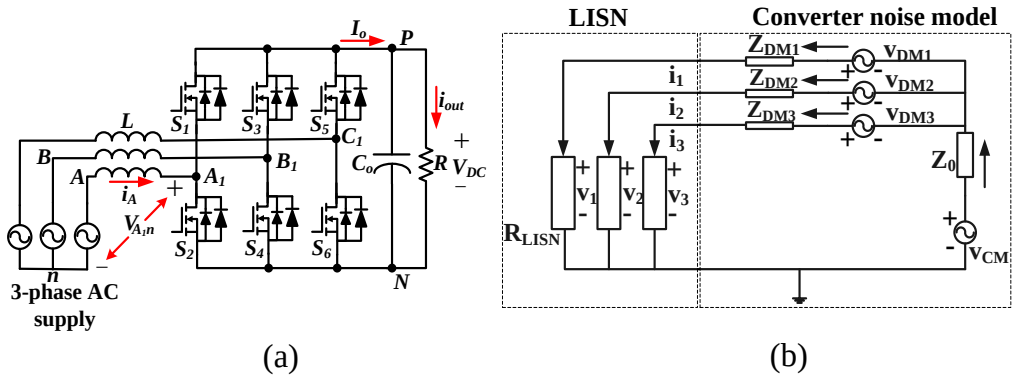


Fig. 5.1. (a) Three-phase boost PFC (b) High-frequency noise model of a three-phase PWM rectifier with LISN.

$$v_{DM,i} = v_i - v_{CM} = \frac{3v_i - v_1 - v_2 - v_3}{3} \tag{5.4}$$

Assuming a symmetrical distribution of common mode current components over all three phases, the following relation could be written.

$$i_i = i_{DM,i} + \frac{i_{CM}}{3} \tag{5.5}$$

However, in practical implementation, the content of CM component in all three phases may not be equal, which will result in non-intrinsic DM noise or mixed-mode (MM) noise [130]. Assuming the common mode currents of first two phases is i_o, and of the third phase is $i_o+\Delta i$, the following relationships representing three phase currents in terms of their respective CM and DM components could be formulated from the transformation matrices, shown in Eq. (5.6)-(5.9).

$$i_{CM} = \frac{3i_o + \Delta i}{3} \tag{5.6}$$

$$i_1 = i_{DM,1} + i_{CM} - \frac{\Delta i}{3} \tag{5.7}$$

$$i_2 = i_{DM,2} + i_{CM} - \frac{\Delta i}{3} \tag{5.8}$$

$$i_3 = i_{DM,3} + i_{CM} - \frac{\Delta i}{3} \tag{5.9}$$

The differential mode phase voltages can be obtained using the following relationships.

$$v_{DM,MM,1} = R_{LISN}(i_{DM,1} - \frac{\Delta i}{3}) \tag{5.10}$$

$$v_{DM,MM,2} = R_{LISN}(i_{DM,2} - \frac{\Delta i}{3}) \tag{5.11}$$

$$v_{DM,MM,3} = R_{LISN}(i_{DM,3} + \frac{2\Delta i}{3}) \tag{5.12}$$

Therefore, there are additional DM voltage drops of $2\Delta i/3$, $-\Delta i/3$ and $-\Delta i/3$ across three phases, due to unbalanced common mode current. This could practically happen if there is any minor mismatch in PCB layout between any two phases, which could be a very common situation in practical implementations.

5.1.2 Parasitic modeling of PFC stage

EMI noise sources in a three-phase PFC converter are mainly originated from several stray capacitances, such as semiconductor-heatsink capacitance, heatsink-ground capacitance, parasitic capacitances between DC link terminals to the ground, stray inductances due to PCB traces and physical connecting cables. In order to fully understand the propagation of these noise factors and their effects in the circuit operation, a detailed CM noise model needs to be derived. Fig. 5.2 shows the different possible sources of parasitic noises in a three-phase active boost rectifier, in which the parasitic components are shown in red-color to distinguish from power stage components. C_M and C_D denote the stray capacitances between a MOSFET's drain or

an external anti-parallel diode's cathode and the heatsink, respectively. These capacitances produce a very high-frequency overriding signal on the switching pulses and shift the CM noise level up in the EMI spectrum. C_{PG} and C_{NG} are respectively the parasitic capacitances from the DC link positive and negative terminals to the ground. Since, these capacitances exist in the path of the DC link current flow; and the DC link is a combination of switching averaged phase currents, hence, there would be a definite effect on the noise spectrums of individual phase currents. Furthermore, there is an additional capacitance between heatsink and ground, denoted by C_{HG} in Fig. 5.2. This capacitance is generated by the combined effect of inter-fin and fin-ground capacitances.

In order to establish a CM noise model of the converter, each MOSFET should be replaced by series combination of a bipolar square pulse of same frequency as switching frequency and a stray capacitance, between its drain and source. The DC link capacitance should be modeled as a short circuit as it would offer very small impedance at 100 kHz switching frequency and its multiple frequencies. Thus, the resulting noise model of a three-phase PFC converter is shown in Fig. 5.2.

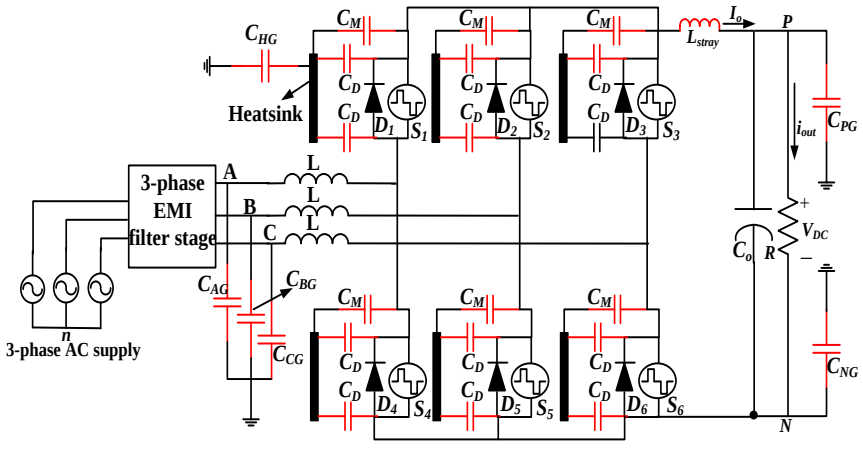


Fig. 5. 2. Noise modeling in a three-phase boost PFC converter.

According to Fig. 5.2, irrespective of the polarity of the phase current, the parasitic capacitance between semiconductor and heatsink is (C_M+$2C_D$). Furthermore, the output parasitic capacitance models the parasitics between the two DC link terminals and the protective earth, as the effective impedance of DC link capacitor itself becomes negligible at higher frequencies. In addition, because of long PCB trace from the input side to the output DC link side, the stray inductance (L_{stray}) should be considered in parasitic modeling, which could be lumped and placed between switching bridge and DC link. Besides, a significant amount of EMI noise is generated from the heatsink, connected to the semiconductors. Instead of a single heatsink, if multiple heatsinks with more number of fins are connected to the semiconductor devices in a single PFC converter, the effective parasitic effect increases, as the stray capacitances are in-fact connected in parallel. If the heatsink is connected to the earth for safety reasons in some applications, the most prominent effect is observed in terms of the EMI noise spectrum because of creating a resonating CM path. Besides, there are parasitic capacitances from phase to ground, which are not same for all three phases; rather the parasitic values depend on the instantaneous switching combination. In order to design the EMI filter stage, it is important to determine the values of frequencies of the resonant oscillations, caused by the parasitic parameters and thus, the related equations governing those oscillation frequencies are presented in Eq. (5.13)-Eq. (5.15). The corner frequency of DM filter stages could be determined from the intersection point of the frequency axis and the tangent, drawn to the first spectrum peak in the conducted EMI frequency range without any filtering action. In our design with 100 kHz switching frequency, the first spectrum peak will occur at 200 kHz, as based on DO-160F, the EMI requirement starts

from 150 kHz. Therefore, the DM corner frequency is set between 150 kHz to 200 kHz. On the contrary, the corner frequencies of CM stage are determined from the parasitic resonance frequencies, which are difficult to be determined in exact numerical values, but their approximate values could be calculated from Eq. (5.13)-(5.15), assuming the heatsink is grounded. Assumption of heatsink being grounded is based on the worse case situation, as the resonating frequency will increase because of less parasitic capacitance, as opposed to the case of floating heatsink. If heatsink is kept floating, C_{HG} will be in series with switch parasitics and cause a relatively lower resonating frequency, which could be partly attenuated by DM filter stage in addition to the CM stage and thus, makes the filtering effect better.

$$f_{noise,1} = \frac{1}{2\pi\sqrt{L_{stray}(C_{PG} + C_{NG} + k(C_M + 2C_D))}} \tag{5.13}$$

$$f_{noise,2} = \frac{1}{2\pi\sqrt{L(C_{AG} + C_{BG} + C_{CG} + k(C_M + 2C_D))}} \tag{5.14}$$

$$f_{noise,3} = \frac{1}{2\pi\sqrt{L(C_M + 2C_D)}} \tag{5.15}$$

In the above equations, 'k' could be 0, 1 or 2, depending on whether the heatsink is grounded to the protective earth. If the heatsink is grounded, the parasitic capacitances from semiconductor devices to heatsink will also participate in resonance with the stray capacitances between DC link terminal and the ground and then, 'k' is 0. 'k' could be 1 or 2, depending on the number of conducting high-side switches in the PFC converter. Similarly, the input boost inductances take part in resonance with line-ground parasitic capacitances and semiconductor parasitics, generating $f_{noise,2}$ and $f_{noise,3}$. These high-

frequency resonant oscillations should be significantly attenuated in the CM filter implementation, which is discussed in the following section.

5.1.3 PSFB noise model

Similar to the PFC stage, MOSFET parasitic capacitances and the stray path inductance will exist in the PSFB DC-DC converter stage too. In addition, due to the fact that there will be potential difference across any two turns of the high frequency transformer, they will act as parallel plate capacitor and form multiple inter-turn stray capacitances in series. The combination of these capacitances with the leakage and magnetizing inductances will give rise to another set of resonant frequencies, which fall in the common mode (CM) spectrum range i.e. >5MHz. This can be justified using the following equivalent noise modeling circuit in Fig. 5.3 with the estimated values of parasitic capacitances.

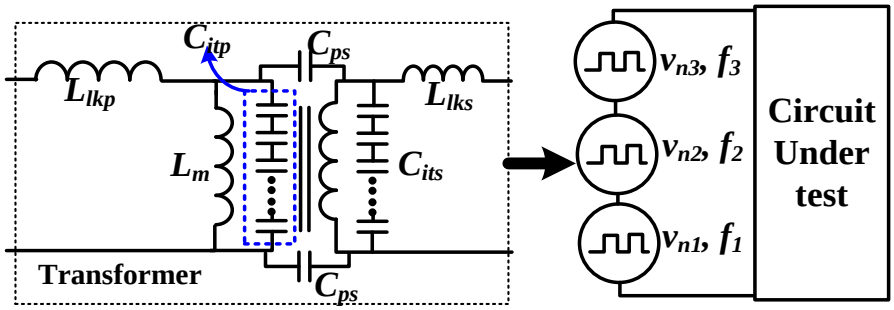


Fig. 5. 3. Equivalent noise model of PSFB converter

The general expression for all possible cut-off frequencies can be written as follows: $f_k = \frac{1}{\sqrt{(\alpha L_m + \beta L_{lkp} + \gamma N^2 L_{lks})(aC_{itp} + bC_{ps} + cC_{its})}}$, where $\alpha, \beta, \gamma, \delta, a, b, c$ can be 0 or 1. It can be analytically stated that there could be noise source of 21 possible corner frequencies and they can be placed in series in the noise equivalent circuit. The interturn

capacitance highly depends on the winding pattern and geometric orientation of different turns, which leads to a complex model of electric field distribution. However, a reasonable estimate for the parasitic capacitance could be the series equivalence of 'N-1' interwinding capacitances originating from 'N' turns in series; analytically it can be expressed as $C_{it} = \frac{\epsilon_o A_c}{(N-1)d}$, where ϵ_0 is the air permittivity, A_c is the core area, d is the gap between the neighboring turns. Doing so, we get the primary and secondary interwinding capacitances to be of 0.24 pF and 2.9 pF, respectively. Also, the capacitance between the primary and secondary conductors need to be considered; however, this capacitance will be much lower due to non-interleaved winding structure in our design. As a reasonable estimate, C_{ps} can be approximated as $C_{ps} = \frac{\epsilon_o A_c}{g}$, where g is the gap between primary and secondary layers and C_{ps} is determined as ~2pF. Having $12\mu H$ leakage inductance and $1mH$ magnetizing inductance in our design, the minimum and maximum possible corner frequencies would be $2.9MHz$ (DM zone) and $26MHz$ (CM zone), implying that all the noise frequencies fall in the conducted EMI range. The noise amplitudes at these frequency contents without any filter stage will be used as reference for designing the EMI filter parameters.

5.1.4 EMI spectrum without filter

Before designing the filter stage, it is required to determine the EMI amplitude spectrum of the PFC converter without any filtering action, which would assist in determining the required attenuation in DM and CM regions of spectrum. In this research, filter design is based on the specifications of a three-phase boost PFC, which is typically used inside an aircraft with a three-phase alternator with variable frequency

(360Hz – 800Hz), and variable AC output voltage (190V – 260V RMS). The target is to achieve the conducted EMI requirements according to DO-160F. The key design specifications are provided in Table 2.2.

Although most of the onboard airborne equipment handle DC voltage between +/-270V to avoid potential partial discharge, RTRU with PFC DC link voltage of 650V (in our design) is located in a highly pressurized chamber with a higher breakdown voltage according to Paschen's curve [137] and hence, the concern for partial discharge is minimized even with the high voltage across DC link.

The EMI amplitude spectrum without any filtering action is shown in Fig. 5.4, which implies that the highest peak of 91dBμA occurs at 200 kHz in the conducted EMI band. Other peaks are located in the higher multiples of switching frequency, which is set at 100 kHz in this design. However, there are specified maximum limits for the spectrum peak amplitudes in the whole conducted EMI range according to DO-160F standard requirements. Hence, in order to reduce the spectrum peak amplitudes to the specified limits, different attenuations are required at different frequencies by the implemented EMI filter. Therefore, the attenuation requirements of DM current waveforms by the EMI stage, shown in Eq. (5.16) are obtained by subtracting the conducted EMI standard, mentioned in DO-160F from the spectrum without any filter in Fig. 3 with a design margin of 6dB (according to DO160F requirements).On the contrary, required attenuation by the CM stage as shown in Eq. (5.17) is set with the worst case scenario, as identifying the effective range of frequency band in CM region is difficult and varies for different PCB layouts.

$$Att_{DM}[dB] = v_{DM}(f_d)[dB\mu A] - Limit[dB\mu A] + margin[dB] = 60dB \qquad (5.16)$$

$$Att_{CM}[dB] = v_{DM}(f_C)[dB\mu A] - Limit[dB\mu A] + margin[dB] > 50dB \qquad (5.17)$$

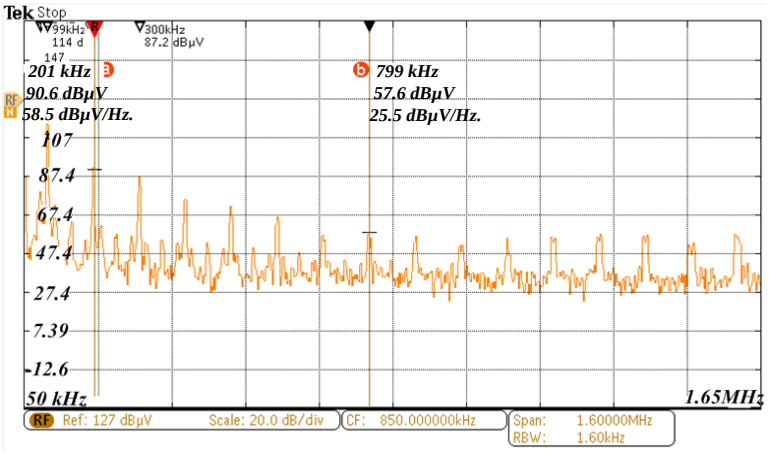


Fig. 5. 4. DM zone EMI results of PFC stage without any filter

In the above equations, f_C and f_D represent the corner frequencies to be designed for CM and DM stages, respectively.

5.2 Filter design

5.2.1 Design Considerations

While designing the EMI filter for RTRU, the following considerations must be kept in the design process flow.

i. The attenuation offered by the filter stage at the design frequency must be greater than its required value to comply with the standard. Typically, the design frequency is a multiple of switching frequency, where the first spectrum peak arises in the conducted EMI frequency range.

ii. In order to maintain the strict power factor requirement at a specified power level, there is a maximum limit for reactive power transfer, which sets an upper bound for net DM capacitance. Assume the specified requirement is to achieve $PF = PF_{min}$ at a load power of P_L.

Say the phase displacement angle is θ, the reactive power can be expressed as $Q = P_L \tan(\theta)$. The upper bound of net DM capacitance is formulated as follows.

$$C_{DM,max} = \frac{Q_L}{2\pi f_g V_{in}^2} = \frac{P_L \tan(\theta)}{2\pi f_g V_{in}^2} = \frac{P_L}{2\pi f_g V_{in}^2} \sqrt{\frac{1-PF_{min}^2}{PF_{min}^2}} \quad (5.18)$$

Assuming the EMI filter topology to be consisting of 'n' cascaded stages with symmetric LC parameters, each DM stage capacitor has an individual upper bound of $C_{DM,max}/n$.

iii. Magnetic saturation must be considered while selecting the filter inductor cores, especially for differential mode design. Selection of magnetic material for DM cores is very crucial for minimizing the core loss and hence, thermal burden.

iv. The common mode inductor cores must be selected in a way that it can avoid magnetic saturation due to using less number of turns for achieving a higher inductance value.

v. The upper bound of common mode capacitance must be selected in a way that the common mode leakage current flowing through the potential earth (PE) does not cross its safety limit mentioned in equipment standard.

5.2.2 Differential mode (DM) and common mode (CM) filter design

An important design parameter for the EMI filter design is switching frequency. Since, each unit of RTRU is designed for 6kW rated load power, in order to achieve high power density, SiC based MOSFETs supporting high-end switching frequencies are used in the design. A higher switching frequency will increase the DM corner

frequency, which will reduce the total weight of EMI filter. Furthermore, since the conducted EMI requirement starts from 150kHz according to DO-160F standard, an appropriate choice of switching frequency could be such a value, that the first valid peak amplitude becomes as low as possible. Accordingly, 100 kHz is set as a good selection of switching frequency of the converter. A further increase in switching frequency is limited by the execution time complexity of the control logic.

Although it is straightforward to determine the corner frequency of DM filter by checking the amplitude of first peak above the switching frequency i.e. at 200 kHz; however, determining the corner frequency for CM stage is quite difficult because of the challenges in identifying its variation range and high sensitivity to testing environment. Furthermore, for DM filter design, in addition to the required filter attenuation, the phase displacement (θ) of the input currents due to the currents drawn by the filter capacitors has to be considered. In this regard, Fig. 5.5 shows a configuration and phasor diagram of a PFC circuit with front-end filter stage, which produces a current i_a in phase with the voltage v_a. Since the voltage drop across L is very small at the line frequency, hence one can assume that $v_a=v_{in}$. The voltage v_a imposes a 90^o-leading current through C, as shown in the phasor diagram. The phasor diagram can also be used to derive the relationship in Eq. (5.19), to determine phase displacement (θ).

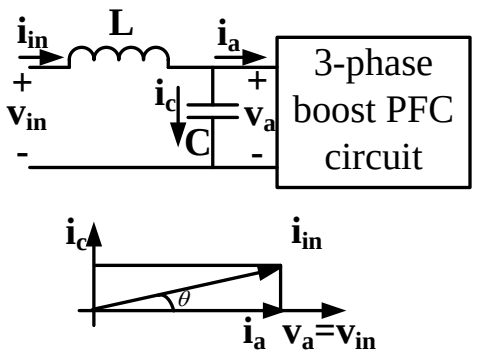


Fig. 5. 5. Phasor diagram of a single-stage LC filter before PFC circuit.

$$\theta = \tan^{-1}\left(\frac{V_{peak}}{I_{peak}}\sqrt{\frac{C}{L}}\right) \tag{5.19}$$

where, I_{peak} is the peak value of phase current i_a and V_{peak} is peak value of input phase voltage. From Eq. (5.20), the maximum value of input capacitor could be calculated.

$$C_{\max} = \frac{\pi\sqrt{LC}I_{peak,\min}}{V_{peak,high}}\tan(\cos^{-1}(IDF)) \tag{5.20}$$

where, *IDF* denotes the input displacement factor, which is the cosine of angle between fundamental phase voltage and fundamental phase current. $V_{peak,high}$ is the peak value of maximum possible input phase voltage and $I_{peak,min}$ is the minimum possible peak value of phase current at partial load demand. If the maximum phase displacement should be limited to 5^o (i.e. input displacement factor (IDF) = 0.996) at the rated output power, the DM filter capacitors are limited to a total capacitance of C_{DM} = 3.5 μF per phase, as obtained from Eq. (5.20) considering the values of $I_{peak,min}$ and $V_{peak,high}$ from specifications of the converter, listed in Table 2.2. At rated power of 6kW, $I_{peak,min}$ and $V_{peak,high}$ values are 11.2A and 358 V, respectively, obtained by assuming a variation on the input AC voltage to be limited to ±10% of its nominal value i.e. 230V RMS. For a

multi-stage cascaded configuration of filter, the parallel combination of all the capacitances, required per each stage, should not exceed 3.5 μF.

Another EMI filter topology, which is a modified two-staged cascaded EMI filter, shown in Fig. 5.6 is proposed in our design. In a conventional two-staged EMI filter, CM stage is a set of two CM chokes and six capacitors (line-ground) and the DM stage consists of three decoupled line inductors and three line-line capacitors (forming a CLC pi network). Unlike the conventional two-staged cascaded structure of EMI filter, this proposed structure uses reduced number of X-capacitors by three and reduced number of DM inductors, which potentially helps reducing the size and weight of the filter. For further analyses, CM and DM circuit equivalents of this filter topology are shown in Fig. 5.7 and Fig. 5.8, which require several assumptions to be taken to derive the filter parameters.

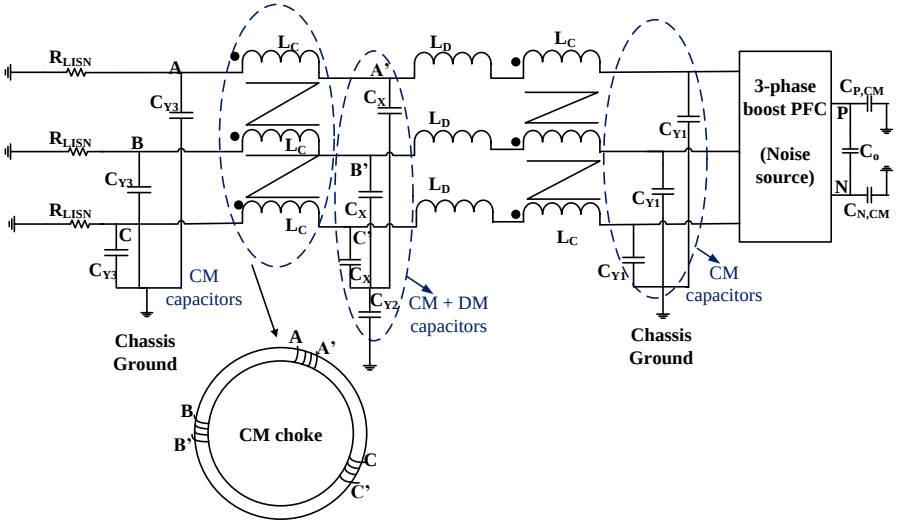


Fig. 5. 6. Cascaded two-staged EMI filter for three-phase boost PFC

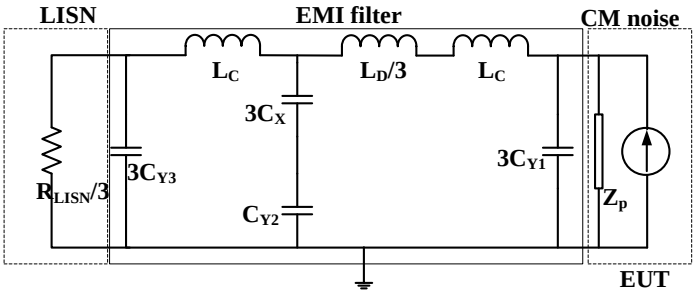


Fig. 5. 7. CM equivalent of the proposed EMI filter for three-phase boost PFC

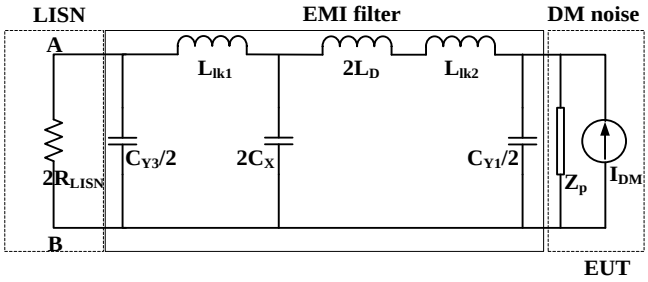


Fig. 5. 8. DM equivalent of the proposed EMI filter for three-phase boost PFC

One of the critical assumptions is that the impedance offered by Y-capacitors, connected to the equipment under test (EUT) should be negligible in comparison to EUT impedance (Z_p). In addition, the equivalent CM impedance should be very large in comparison to the LISN impedance, when all the phases contain common mode noise i.e.$1/(3\omega C_{Y1})<<Z_p$; $1/(3\omega C_{Y3})>>R_{LISN}/3$; $\omega(2L_C+ L_D)>>R_{LISN}/3$. Thus, with these assumptions, the two equivalent CM inductors are obtained as $L_{CM1}=L_C$ and $L_{CM2}=2L_C+ L_D$. Thereby, the CM noise takes the return path to the ground through two equivalent CM inductances (L_{CM1} and L_{CM2}) and two equivalent CM capacitances (C_{CM1} and C_{CM2}). The values of these equivalent capacitances and inductances can be determined using Eq. (5.24)-(5.25). This filter structure generates two resonant frequencies with two different corner frequencies ($f_{R,CM1}$ and $f_{R,CM2}$), where $f_{R,CM1}=1/(2\pi\sqrt{(L_{CM1}C_{CM1})})$ and $f_{R,CM2}=1/(2\pi\sqrt{(L_{CM2}C_{CM2})})$.

$$C_{CM1} = \frac{3C_{Y3}\dfrac{3C_X C_{Y2}}{3C_X + C_{Y2}}}{3C_{Y3} + \dfrac{3C_X C_{Y2}}{3C_X + C_{Y2}}} \tag{5.24}$$

$$C_{CM2} = \frac{3C_{Y1}\dfrac{3C_X C_{Y2}}{3C_X + C_{Y2}}}{3C_{Y1} + \dfrac{3C_X C_{Y2}}{3C_X + C_{Y2}}} \tag{5.25}$$

CM corner frequency is chosen as the minimum of all possible resonance frequencies, i.e. f_{noise1}, f_{noise2} and f_{noise3} caused by the parasitic LC values in the PCB layout and also, from some measurement probes. Although it is very tricky to determine the exact value of corner frequency unlike DM equivalent, but a good approximate to start the design could be obtained by plugging in the parasitic parameters with correct exponents in Eq. (5.13)- Eq. (5.15).

While analyzing the DM equivalent, the input side impedance offered by both Y-capacitance and effective series inductive path should be very large as compared to the total LISN impedance in order to complete a DM noise path i.e. $1/(0.5\omega C_{Y3})>>2R_{LISN}$; $\omega(2L_D+L_{lk1}+L_{lk2})>>2R_{LISN}$. In addition, impedance of Y-capacitor at the EUT side should be negligibly small as compared to the EUT impedance (Z_p) i.e. $1/(0.5\omega C_{Y1})<<Z_p$. With these assumptions, the two equivalent DM inductors are obtained as $L_{DM1}=L_{lk1}$ and $L_{DM2}=2L_D+L_{lk2}$, where L_{lk1} and L_{lk2} represent the leakage inductances of two CM chokes. Besides, two equivalent CM capacitors in noise path are obtained as $C_{DM1}=2C_XC_{Y3}/(C_{Y3}+4C_X)$; $C_{DM2}= 2C_XC_{Y1}/ (C_{Y1}+4C_X)$. Therefore, based on the mentioned assumptions, and parameter values in CM and DM equivalents, the corner frequencies of the filter stage are determined as $f_{R,DM1}=1/(2\pi\sqrt{(L_{DM1}C_{DM1})})$ and $f_{R,DM2}=1/(2\pi\sqrt{(L_{DM2}C_{DM2})})$.

All the filter parameters i.e. L_D, L_C, C_X, C_{Y1}, C_{Y2}, C_{Y3} can be calculated by considering $f_{R,DM1}$=100kHz, $f_{R,DM2}$=150kHz, and $f_{R,CM1}$, $f_{R,CM2} < min\{f_{noise,1}, f_{noise,2}, f_{noise,3}\}$, in our design. In order to reduce cost and size of the filter, the leakage inductance L_{lk} of the CM choke is often controlled to form a DM inductor. However, lack of regulation over the leakage inductance value can potentially change the resonant frequency and thus deteriorates the filtering action. Therefore, a separate set of inductor cores is used to realize the DM inductances in our design.

For the improvement in common mode EMI spectrum, 2.2 nF ceramic capacitors (of 2kV rating) are added from both positive and negative terminals of both PFC and RTRU DC links to the chassis ground, as shown in Fig. 5.6. The high frequency (in the order of MHz) harmonic components arising due to the switching, ringing, stray inductances and other PCB parasitics receive low impedance paths to the chassis ground through the common mode capacitors and thus, the common mode voltage stress can be significantly reduced.

5.2.3 Damping in EMI filter

It is important to look into the damping performance of the designed EMI filter stage, as any high-Q peak in frequency response may amplify particular frequency components coming from control loop or AC source frequency harmonics. A frequency response of two stage cascaded LC filter without any damping resistor is shown below, which indicates high-Q peak at third and fifth source frequency harmonics for a 400Hz supply. This can be explained by the fact that all the poles of filter transfer function are located on the imaginary axis.

$$T_{EMI}(s) = \frac{1}{1+s^2(L_1C_1+L_2C_2+L_1C_2)+s^4L_1L_2C_1C_2} \quad (5.26)$$

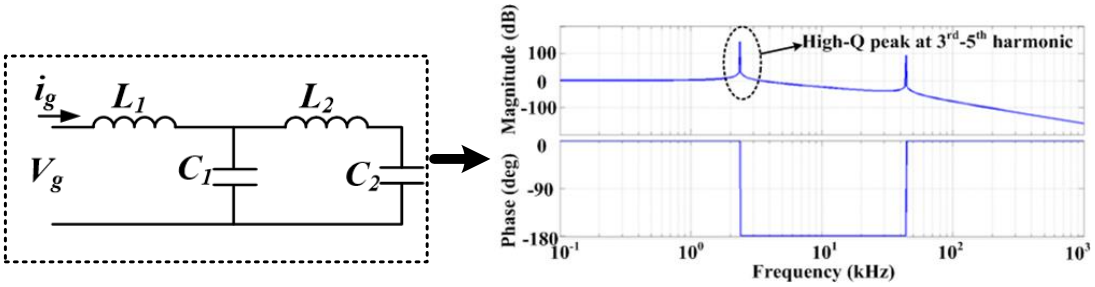


Fig. 5. 9. Frequency response of a two-stage LC filter without damping

In order to provide enough damping to the filter stage, a set of damping resistors are put in parallel to the DM inductors in our design, which flattens out the response at the cost of conduction losses. However, upon selection of 20Ω resistors, the additional conduction losses come out to be 4.8W, which is insignificant to the net output power of 6kW. The revised DM filter stage along with its frequency response are presented below. The transfer function of the revised filter, shown in Eq. (5.27) has all its poles with negative real parts, which indicate damping of the high-Q peaks from the previous undamped design.

$$T_{EMI}(s) = \frac{(R_1+sL_1)(R_2+sL_2)}{s^4R_1R_2L_1L_2C_1C_2+s^3L_1L_2(R_1C_1+R_1C_2+R_2C_2)+s^2(L_1L_2+R_1R_2C_2L_2+R_1R_2C_1L_1+R_1R_2C_2L_1)+s(L_1R_2+R_1L_2)+R_1R_2} \quad (5.27)$$

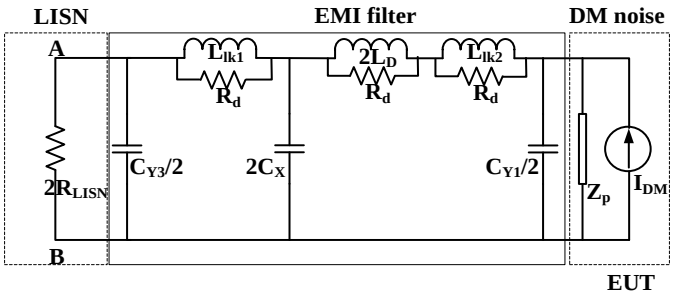


Fig. 5. 10. A two-stage LC filter with damping

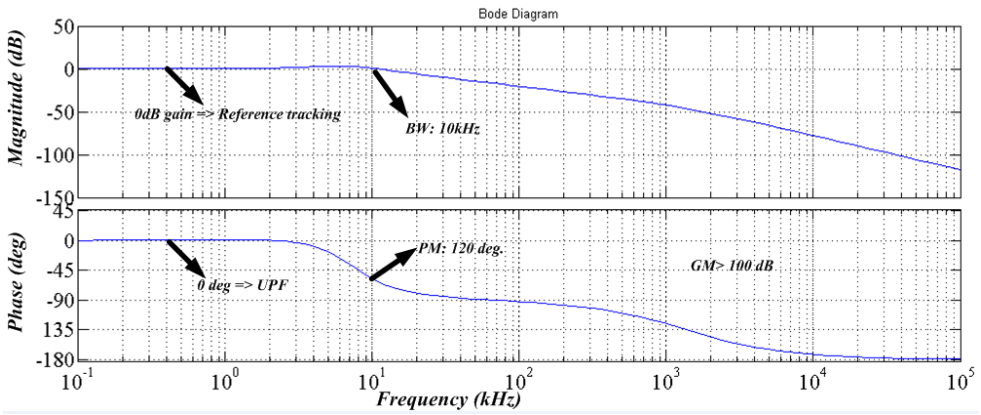


Fig. 5. 11. Frequency response of a two-stage LC filter with damping

5.3 Filter Volume Optimization

Some of the previous studies had shown that filter volume varies in an approximately linear fashion with the stored energy [11]. Therefore, in order to perform the volumetric optimization, the volume of capacitors and inductors are mapped to the domain of stored energy in the filter elements, by an approximated linear curve generated from minimum square fitting method. Thus, total filter volume is formulated as:

$$Vol_{filt}(L, C, n) = n(k_C C V_{in}^2 + k_L L I_{in}^2) \tag{5.28}$$

where, C and L are DM filter capacitors and inductors of each stage. The coefficients k_L and k_C can be estimated from a large database of datasheet specifications of the used filter components. The relation between filter volume and energy can be formulated more accurately if another linear term of inductance / capacitance value is added to the energy term; however, this would lead to high complexity in performing optimization method and hence, will be looked into in future studies. From the collected database of suitable film capacitors from TDK [139] and high-flux based DM inductors from Magnetics [120], the estimated linear fit between volume and stored energy in inductors

and capacitors yields to the parameter values as follows: $k_L = 0.1103\, mm^3/\mu J$ and $k_C = 0.1011 mm^3/\mu J$. In the process, the tuning variables are LC parameters and number of cascaded stages.

At a frequency of interest f_{int}, the required attenuation is given by the difference between spectrum amplitude without any filter and the maximum limit according to conducted EMI standard, shown in Eq. (5.29).

$$Att_{req,CM}(f_{int}) = 20\log\left(\frac{U_{CM}(f_{int})}{1\mu V}\right) - Limit\ (f_{int}). \tag{5.29}$$

Typically, f_{int} is the same as design frequency f_d, where the first spectrum peak appears in conducted EMI range; in our case, f_{int} is 200kHz i.e. twice of switching frequency. With 'n'-stage cascade LC filter, the attenuation offered at the frequency f_{int} would be as follows: $Att_{offered}(f_d) = 40\log(2\pi f_d (LC)^{n/2})$. For complying with the DM requirement, the following relation must hold true: $Att_{offered}(f_d) \geq Att_{req,DM}(f_d)$. Substituting L in terms of required attenuation and C in the volume expression, the filter volume can be restructured as follows, which formulates the minimization problem.

$$Vol_{filt} = 0.5n(k_C C V_{in}^2 + k_L I_{in}^2 \frac{1}{C}\left(\frac{10^{\frac{Att_{req}}{40}}}{2\pi f_{int}}\right)^{2/n}) \tag{5.30}$$

The solution for a minimal volume is given by:

$\frac{\partial Vol_{filt}}{\partial C} = 0$, which yields to $C = \frac{I_{in}}{V_{in}}\sqrt{\frac{K_L\left(\frac{10^{\frac{Att}{40}}}{2\pi f_{int}}\right)^{2/n}}{K_C}}$ (5.31)

For a given number (n) of filter stages, C can be determined to minimize the filter volume; however, the obtained C value may not satisfy its upper bound requirement,

shown previously in Eq. (5.18). In that case, C is fixed at its maximum allowable value and L is determined using the attenuation requirement relation. Typically, number of filter stages could vary from 1 to 3; therefore, such process for calculating L and C is iterated for $n = 1, 2, 3$ and the (n, L, C) combination corresponding to minimum total volume is selected for the final design. This method yields to the following parameters: $n = 2; L = 95\mu H, C = 315nF$ for the PFC stage to be complying with DO-160F standard.

Moreover, a relatively more formal method using suitable optimization algorithm can be applied to determine the LC combinations. The constrained optimization problem stands out as to minimize the cost function Vol_{filt} subject to the condition $nC < C_{DM,max}$, obtained from the power factor requirement condition formulated in Eq. (5.18). Genetic algorithm based approach is utilized to solve this problem and the optimized solution is as follows: $n = 2; L = 100\mu H; C = 310nF$. It is important to notice that the filter parameters obtained from both the above methods match very closely to each other. The corresponding theoretical minimum filter volume turns out as 21 inch^3., which, however will deviate to some extent in practical implementation due to standard available (off-the-shelf) filters and approximation of linear relation between volume and energy. The actual realization of filter is discussed in the next subsection.

5.4 Filter construction

Finally, the designed values of optimized LC parameters satisfying our requirements are listed in Table 5.2. Total weight of the designed EMI stage with the proposed topology is 1-lbs, which is just 1/5th of the weight of PFC stage and its dimension is 2.5

x 7 x 2 inch^3. The proposed design is compared with an existing appropriate design approach [118] in terms of the LC parameter values and their corresponding quantities. The EMI filter design method, discussed in [138], proposes a three-staged cascaded EMI filter and its specifications are listed in Table 5.3. As a major difference in terms of weight and compactness, the important factors are the quantities and equivalent values of CM and DM inductor chokes due to their dominant sizes and weights, which are less in our design than the approach in [138].

Table 5. 1. EMI filter component values in our proposed topology

Component	Value	Quantities	Specs
X-capacitor	310nF (each)	3	Film capacitor, 530V AC
Y-capacitor	4.7nF(each)	7	Film capacitor, 330V AC
CM choke	1.4mH	2	W409 core, Iron based material; B_{max}=1.2T
DM choke	100µH	6	T90 core (90% Tungsten)
$C_{P,CM}$ and $C_{N,CM}$	11nF each	2	3kV DC voltage stress capacity

Table 5. 2. EMI filter component values in the topology proposed in [135]

Component	Value	Quantities	Specs
X-capacitor	680nF (each)	3	Film capacitor
Y-capacitor	220nF(each)	9	Film capacitor
CM choke	2.1mH	3	T60006-L2040-W453 (toroid)

DM choke	166µH	3	00K4017E090 (Kool Mu, E core)

As an important design requirement, the CM and DM inductor cores should operate in linear region of B-H curve at the rated power, with minimum losses due to DC resistance and magnetic core. The CM inductors have to withstand the high frequency CM voltage. In addition, the core-saturation is avoided if Eq. (5.32) is satisfied.

$$B_{sat} > B_{CM,\max} = \frac{\int_0^{T_p} v_{CM}\,dt}{NA_{fe}} = \frac{(V_O/3)T_s}{NA_{fe}} \tag{5.32}$$

where, $T_s=1/f_s$. T_p denotes the maximum length of a common mode pulse. In our design $T_p=T_s$. V_o, N and A_{fe} denote the instantaneous output voltage, number of turns on CM choke and effective flux area of the core, respectively. Accordingly, very high permeability (µ=40,000) toroid cores (part numbers W409 and W380) with high saturation flux density (B_{sat}), are used in the design of common mode chokes. The high-frequency DM current ripple does not cause magnetic core losses due to the mutual compensation of the magnetomotive forces (MMF) but DC conduction losses caused by skin and proximity effect have to be considered in selecting the core. Accordingly, the toroidal cores (T90) with relatively less permeability than CM core are selected for the design of DM chokes.

Furthermore, the capacitors are selected based on the voltage ratings, which are at least the peak value of line-line input voltages for X capacitors and line-ground isolation voltages for Y capacitors. To maintain these requirements in our design, film capacitors with lower ESR (part number: B32912A3224K) are used in DM stage and film capacitors (part number: B81123C1472M) with higher isolation voltage (3kV) are

used in CM stage of EMI filter. Furthermore, an upper limit of the number of filter stages (N_{max}) could be determined using Eq. (5.30)- Eq. (5.31) for overall volume minimization. Att_{req} is the attenuation requirement by DM filter stage at the design frequency f_D and Att_{LC} is the attenuation of an LC filter with N filter stages.

$$Att_{LC}(f_D) = (2\pi f_D)^{2N}(2LC)^N \geq Att_{req}(f_D) \tag{5.33}$$

$$N_{\max} = \frac{1}{(2\pi f_D)^2(2LC)} \ln(Att_{req}(f_D)) \tag{5.34}$$

Accordingly, an optimal number of filter stages is obtained as 2 and thus, implemented experimentally to meet the conducted EMI requirements, evaluated in Section 5.2.

5.5 Experimental results

With the design considerations proposed in Section 5.2, as a proof-of-concept verification to the operation of EMI filter for a three-phase boost PFC converter, a set of experiments is conducted with a 6kW hardware prototype for integrated EMI&PFC stage, shown in Fig. 5.12. Since the applications of the developed prototype mainly focus on the avionics domain, the selected EMI standard is DO-160F, which has a conducted EMI range from 150 kHz to 30MHz.

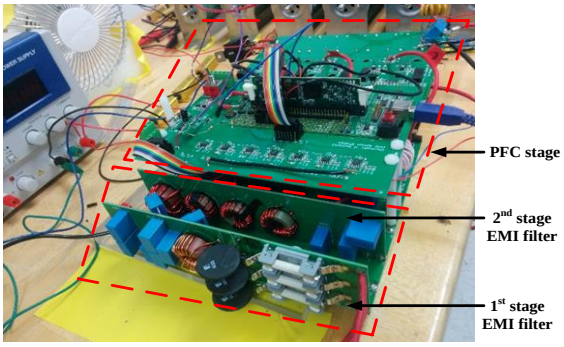


Fig. 5. 12. Photo of the integrated EMI and three-phase boost PFC prototype.

The complete range of conducted EMI spectrum, combining DM and CM range (150 kHz to 30 MHz) after the filtering action by our proposed topology, is demonstrated in Fig. 5.13, which ensures complying with DO-160F conducted EMI requirement standard at all frequencies. The plot below is obtained by plotting the extracted data from spectrum-analyzer into MATLAB.

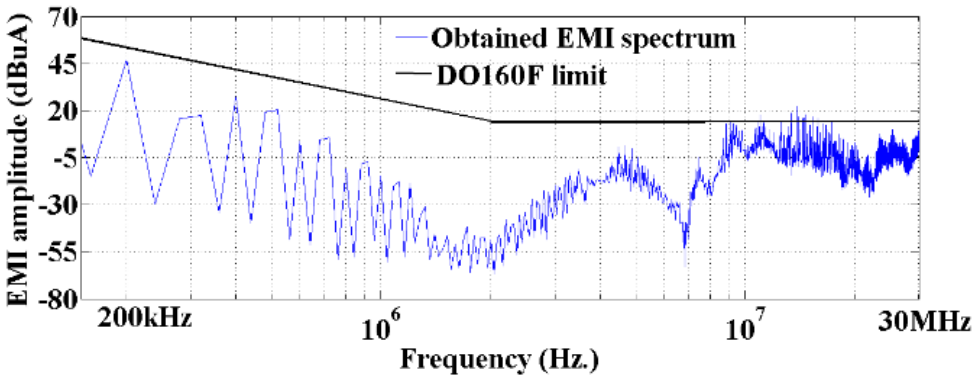


Fig. 5. 13. EMI spectrums over entire conducted EMI range after applying the proposed EMI filter.

Fig. 5.14 represents the input phase displacement in the current waveforms, power factor and THD after the filter stage implementation, at 6kW output power. An input phase displacement of 1.8 degrees, power factor of 0.999 and 4.3% THD are measured from the reported results of the integrated stage of PFC and EMI. The conversion efficiencies of PFC alone and integrated PFC & EMI stages are 98.4% and 98.2%, respectively, which are greater than the reported value of 96.7% efficiency, in an existing EMI & PFC integrated stage, proposed in [120]. From the efficiency values of PFC-alone and integrated EMI & PFC stage, the efficiency of EMI stage-alone would be 99.6%.

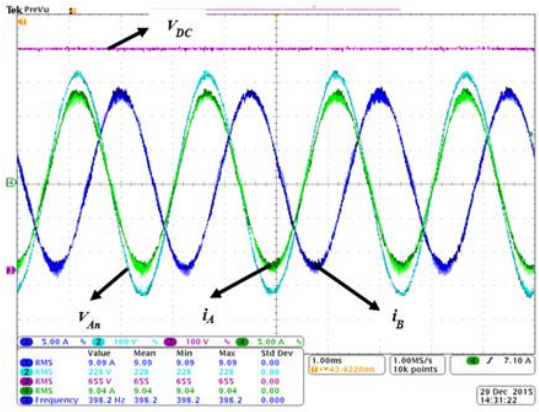


Fig. 5. 14. Experimental waveforms of the converter at 6kW (a) Phase 'A' voltage and current, Phase 'B' current, DC link voltage. V_{DC}=650V, i_A (RMS) =i_B (RMS) =9.06A, V_{An} (RMS) =230V, P_{out}=6kW.

As another evaluation parameter, harmonics of the input current are calculated by Fourier analysis of the measured current waveform till 30th order and shown in Fig. 5.15.

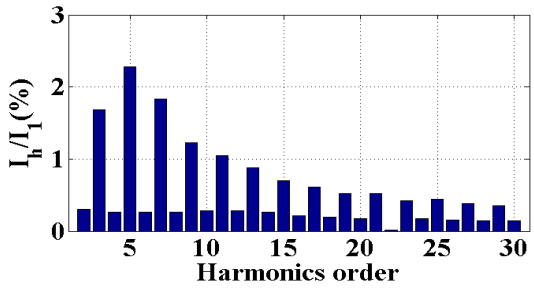


Fig. 5. 15. Harmonic spectrum of phase current at rated input and 10kW load.

The harmonics content is quantified by the ratio between RMS current value at a harmonic frequency (I_h) to the fundamental RMS (I_1). A switching frequency of 100 kHz is used such that the carrier harmonics are above the 125th harmonic under 800 Hz line. Thus, considerably less harmonics content at multiples of the fundamental-frequency enables the converter to achieve a THD as low as 4.3% at 230V phase-neutral 400Hz AC input and 10kW load power.

5.6 Summary

In this chapter, design of a three-phase EMI filter topology to meet the conducted EMI requirements of a three-phase boost PFC converter for avionics applications is proposed and discussed in detail, along with identification and modeling of CM noises, originated from different sources. The integrated combination of a 6 kW front-end EMI and boost PFC stage is designed within a dimension of 12x7.8x4 $inch^3$ with a volumetric power density of 1.1kW/liter. Furthermore, a comparative study between the proposed two-staged EMI filter topology and existing CC topology with same weight and dimension, shows that the proposed topology meets the conducted EMI requirements at all frequencies between 150 kHz and 30 MHz, as opposed to the CC topology, which fails to satisfy the requirements at some frequencies in DM and CM range. The EMI spectrum amplitude is reduced below 60dBµA at 150 kHz and below 20 dBµA at frequencies above 2MHz with the proposed topology.

The integrated stage of EMI and PFC is tested up to 10kW at 230V RMS phase-neutral, 400Hz AC input and 100 kHz switching frequency. The EMI stage maintains a conversion efficiency of 99.6%, THD of 4.3% and adds a maximum phase-shift of only 1.8^o to the input line current, which enables the converter to maintain a good power quality.

Chapter 6: Cascaded Two-stage Isolated AC-DC Converter for RTRU Applications: Control and Efficiency Maximization

The proposed power electronic architecture in RTRU design is a cascaded AC-DC converter, which consists of a three-phase boost-type power factor correction (PFC) rectifier followed by a phase shifted full-bridge (PSFB) DC-DC converter. Although the design, analyses and innovative methods to improve individual converters' performance have been discussed in the previous chapters, it is still important to research, investigate and discuss the overall stability, dynamics performance, and efficiency maximization strategy for the entire RTRU. Since RTRU operates at variable loading conditions inside the aircraft, a unique set of design space variables, such as: control parameters, and switching frequency will not lead to the globally optimized performance; rather, there needs to be a supervisory controller that will set the command for these changeable parameters to ensure the optimized power quality, efficiency at all operating conditions. Keeping these objectives, the following research ideas are introduced, developed and verified in three sections of this chapter: (i) stability analysis and thereby, control loop design for power factor maximization, dynamics improvement of the integrated converter at a wide range of load and AC line conditions (ii) maximizing the net RTRU conversion efficiency by varying the intermediate DC link voltage at different loading conditions (derived from loss modelling) (iii) minimizing the intermediate DC link capacitance through ripple current

harmonics minimization using duty modulation and an innovative control loop design. All these sections are elaborately and comprehensively discussed as follows.

6.1 Reduced observer state-feedback control

The control methods play crucial roles in determining the overall stability, dynamic performance, and perfect regulation of the converter. The stability and regulation issues become more critical in case of a cascaded converter topology, which is studied in this chapter. Even though both stages might individually be stable through their independent control systems, the cascade combination may lose its stability and regulation at some operating conditions. Several research works [141-142] have concentrated on resolving such instability issues in a cascade converter. The work in [141] focuses on the improvement of phase & gain margins through manipulating the input impedance of the second stage in a two-staged AC-DC converter by a digital filter implementation in the feedback loop. Although there is a certain improvement in the gain and phase crossover frequencies, the method overlooks the effects of the output load power variations. Furthermore, a stability investigation on cascade two-staged PFC converter is done in [142-143], which experimentally detects and proves the occurrence of period doubling bifurcation phenomena but does not discuss any control approach to prevent this instability issue.

A research on control strategy for high power AC-DC-AC cascaded power converter is carried out in [144], which proposes cascaded voltage control, power factor control and voltage balancing control. However, the work does not address the potential issue of instability, which may arise due to the change in power flow direction i.e. rectifier to inverter mode. In addition, a control method on cascaded buck-boost PFC

converter is proposed in [145], which achieves a non-distorted sinusoidal current for wide range of output voltage levels. However, similar control approach is not applicable for an integrated three-phase PFC and PSFB converter due to different plant characteristics. Furthermore, [146] presents an analysis of the instability of PFC power supplies with various AC sources, considering the input impedance of the PFC supply at different load conditions. Several qualitative solutions for damping the voltage control loop or adding power dissipating elements to the resonant circuit to reduce quality factor are proposed to improve the stability; however, it is not verified experimentally. Furthermore, stability analyses of cascaded converters for bidirectional power flow applications are discussed in [147]. This work mainly focuses on the effect of gain-margins of both stages on the cascade stability; however, the study does not include the methods to improve the overall stability. In addition, more related studies [148-151] are performed with the focus of stability investigation of cascade converters and a majority of those manipulate the conventional averaged current control loop to increase the stability margins. However, the effects of other control strategies on improving the stability are not considered in these studies.

In order to address and alleviate the issues related to the instability of a cascaded two stage AC-DC converter, a reduced state observer-based state-feedback control approach is proposed in this chapter. The integrated PFC and PSFB topology can be structured as a three-phase PFC converter with a switching load, which represents the DC-DC stage. The input impedance of the DC-DC stage acts as the output load of the first stage. It is shown that the cascaded converter may lose its stability at some output load conditions with the conventional PI controller. The main reason for such instability

is that the overall closed loop transfer function of three-phase PFC stage will inherently encounter right-half poles at particular load conditions. The proposed approach eliminates the occurrence of right half poles, as all the eigenvalues of the closed loop transfer function are inherently negative, irrespective of the feedback gain parameters. Furthermore, even though the converter is stable with the conventional PI control at some load conditions, the input power factor deviates from unity due to the imposed constraints on the PI parameters to ensure stability. Therefore, there will be reactive power transfer to the load side, resulting the efficiency degradation. The proposed control helps the converter achieve a unity power factor at all load powers, as the gain parameters are independent of load resistance. Another major contribution of this control is that it reduces three sensor counts (i.e. one input phase current, DC-DC primary current and final output voltage), whereas these measurements are definite requirements for the conventional PI control.

6.1.1. PSFB converter modelling:

In order to control the cascaded AC-DC converter shown in Fig. 6.1, it is required to model the DC-DC stage as an equivalent load to the first converter stage i.e. three-phase PFC rectifier. The input impedance of the PSFB converter is the same as the output impedance of the PFC stage, which helps to reduce the overall topology to a three-phase PFC with a switching load. Therefore, it is necessary to investigate the equivalent input impedance of the PSFB converter. Let, V_1 be the instantaneous primary side voltage, created due to the linked flux and V_p is the instantaneous voltage across the primary side of the transformer including the leakage inductance and L_p' is the net primary inductance. Also, let's assume the ESRs of the DC bus capacitor, output

capacitor and output inductor are $r_{C'}$, r_L, and r_C, respectively. Therefore, the following relationships can be established from the analyses on the primary and secondary sides of the transformer.

$$V_p = L_p' \frac{di_p}{dt} + V_1 \tag{6.1}$$

$$\frac{V_1}{n} = L_s \frac{di_s}{dt} + r_L i_s + V_o \tag{6.2}$$

Taking the Laplace transformation of Eq. (6.2), the following relationship is obtained.

$$\frac{V_1(s)}{n} = (sL_s + r_L) i_s(s) + V_o(s) \tag{6.3}$$

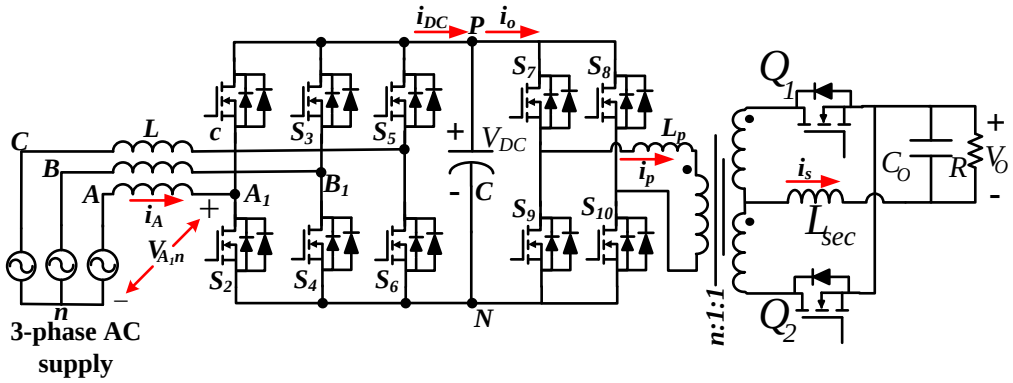


Fig. 6. 1. Integrated two stage AC-DC converter for RTRU

The secondary side current can be formulated as follows in Laplace domain.

$$i_s(s) = \frac{V_o}{1/sC_o + r_C} + \frac{V_o}{R} \tag{6.4}$$

Taking the Laplace transformation on Eq. (6.1)-Eq. (6.4) and using $i_s(s) = ni_p(s)$, the following relationship is obtained.

$$\frac{V_p}{i_p}(s) = \frac{s^2(R+r_C)C_oL_{eq} + s(L_{eq} + n^2C_or_L(R+r_C)) + n^2R(1+sC_or_C)}{sC_o(R+r_C)+1} \tag{6.5}$$

where, $L_{eq} = L_p' + n^2 L_s$. The net input impedance $Z_{in}(s)$ can be formulated as follows.

$$Z_{in}(s) = \frac{v_{DC}}{i_o} = \frac{v_{DC}}{V_p} \times \frac{V_p}{i_p} \times \frac{i_p}{i_o} \tag{6.6}$$

where, v_{DC} is the instantaneous output DC voltage. From the first-harmonic approximation (FHA), the above relationship can be restructured as Eq. (6.7).

$$Z_{in}(s) = \frac{v_{DC}}{< i_o >_1} = \frac{v_{DC}}{< V_p >_1} \times \frac{< V_p >_1}{< i_p >_1} \times \frac{< i_p >_1}{< i_o >_1} \tag{6.7}$$

where, $<V_p>_1$, $<i_p>_1$, and $<i_o>_1$ represent the first harmonic components of the primary voltage, primary current and input current of the PSFB stage, respectively. For any phase shift angle φ, 'm'th harmonic amplitude of the primary voltage i.e. a_m can be determined as follows.

$$a_m = \frac{1}{\pi} \int_{<2\pi>} V_p(t)\sin(nt)dt = \frac{V_{DC}}{m\pi}[1+\cos(m\phi)]' \ [1- (-1)^m] \tag{6.8}$$

Accordingly, the first harmonic amplitude of the primary input voltage is formulated by the following relationships.

$$|V_{p1}| = \frac{2V_{in}}{\pi}(1+\cos(\phi)) \tag{6.9}$$

$$\frac{v_{DC}}{< V_p >_1} = \frac{\pi}{2(1+\cos\varphi)} \tag{6.10}$$

Furthermore, i_o can be expressed in terms of i_p, as follows; $i_o = i_p$ if $0<\theta<\pi-\varphi$; $i_o = 0$ if $\pi-\varphi<\theta<\pi$; $i_o = -i_p$ if $\pi<\theta<2\pi-\varphi$; $i_o = 0$ if $2\pi-\varphi<\theta<2\pi$. Therefore, the fundamental components of i_o and i_p can be related by determining Fourier coefficient as follows.

$$\frac{< i_p >_1}{< i_o >_1} = \frac{\pi}{2(1+\cos\varphi)} \tag{6.11}$$

Therefore, the net input impedance can be determined using Eq. (7) and is formulated as follows.

$$Z_{in}(s) = \frac{\pi^2}{4(1+\cos\varphi)^2} \times \frac{s^2(R+r_C)C_oL_{eq} + s(L_{eq} + n^2C_or_L(R+r_C)) + n^2R(1+sC_or_C)}{sC_o(R+r_C)+1} \quad (6.12)$$

The form of $Z_{in}(s)$ helps us to represent the whole DC-DC stage in an equivalent impedance form as shown in Fig. 6.2(a), assuming the ESRs to be zero and k = $\pi^2/4(1+\cos\varphi)^2$.

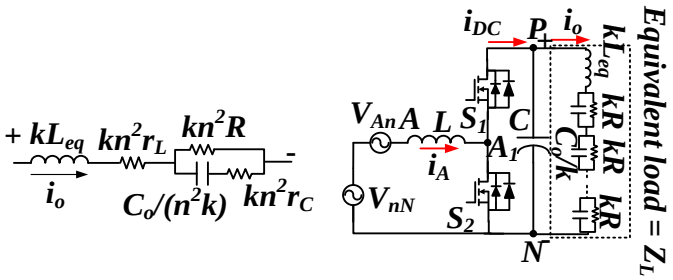


Fig. 6. 2. (a)The DC-DC converter model as an equivalent load to the PFC (b) One phase of the integrated converter

Therefore, the net phase lag of the input impedance can be formulated as Eq. (6.13) and will be used in calculation of the phase difference in overall control loop for stability condition.

$$\varphi_{lag} = \tan^{-1}\left(\frac{\omega L_{eq}}{nR - \omega^2 RC_oL_{eq}}\right) - \tan^{-1}(\omega C_oR) = \tan^{-1}\left[\frac{\omega(L_{eq} - nR^2C_o + \omega^2R^2C_o{}^2L_{eq})}{nR}\right] \quad (6.13)$$

6.1.2 Three-phase boost PFC converter modeling

For analyzing the overall transfer function of the three-phase PFC converter with load impedance $Z_L(s) = Z_{in}(s)$, the three-phase six-switch PFC is split into three cross-coupled single phase AC-DC PFCs, whose inputs have a common coupling term of V_{nN} i.e. potential between AC neutral and DC link negative terminal. This could be

justified from the fact that the input of the 'i'th-phase single phase PFC is the potential difference between i'th phase and the DC link negative terminal i.e. V_{iN}, which can be expressed as $V_{iN}=V_{in}+V_{nN}$, i.e. the sum of phase-neutral voltage (V_{in}) and neutral-DC link negative potential difference (V_{nN}). One of such single-phase converters (of phase 'A') is shown in Fig. 6.2(b).

V_{A1N} could be 0 or V_{DC}, depending upon whether lower leg switch S_2 is ON or OFF, respectively. Therefore, the switching average of the voltage across the leg-midpoint of 'k'th phase to the negative terminal of DC link i.e. V_{i1N} would be $d_{kH}V_{DC}$, where d_{kH} represents the high side duty ratio of 'k'th phase. Hence, Eq. (6.14) could be formulated for any AC-DC converter.

$$\tilde{V}_{kn}+V_{nN}=L\frac{di_k}{dt}+d_{kH}V_{DC} \tag{6.14}$$

Applying summation operator to both sides of Eq. (6.14) and by varying phase 'k' from A to C, the subsequent relationships are formed for a balanced three-phase system i.e.

$$\tilde{V}_{An}+\tilde{V}_{Bn}+\tilde{V}_{Cn}=0 \tag{6.15}$$

$$(\tilde{V}_{An}+\tilde{V}_{Bn}+\tilde{V}_{Cn})+3V_{nN}=L\frac{d}{dt}(\sum_{k=A}^{C}i_k)+V_{DC}\sum_{i=A}^{C}d_{iH} \tag{6.16}$$

$$V_{nN}=\frac{V_{DC}\sum_{i=A}^{C}d_{iH}}{3} \tag{6.17}$$

Thus, the reference duty ratio for phase 'A' is obtained by the following relationship in discrete time domain with sampling time T_s and output DC reference of V_{DC}*, and similarly other phase duty ratios can be formulated.

$$d_{AH}[n]=\frac{V_{An}[n]+V_{nN}[n]}{V_{DC}^{*}}=K_1\sin(\omega nT_s)+\frac{d_{AH}[n-1]+d_{BH}[n-1]+d_{CH}[n-1]}{3}\frac{V_{DC}}{V_{DC}^{*}} \quad (6.18)$$

The circuit structure in Fig. 2(b) leads to the following relationship.

$$V_{AN}=sLi_A(s)+d_{AH}v_{DC}(s) \quad (6.19)$$

Taking perturbation on both sides of Eq. (6.19) at the operating duty ratios of D_{AH}, D_{BH}, D_{CH} for A, B, C phases, respectively and using Eq. (6.18), the following small-signal transfer function between phase current and intermediate DC link voltage is obtained.

$$\frac{\Delta i_a(s)}{\Delta v_{DC}(s)}=\frac{4D_{AH}+D_{BH}+D_{CH}}{3sL} \quad (6.20)$$

The output DC link current (i_{DC}) can be formulated as the sum of switching averaged currents of three top side PFC switches, formulated as follows.

$$i_{DC}=\sum_{k=A}^{C}d_{kH}i_k=(d_{AH}-d_{CH})i_a+(d_{BH}-d_{CH})i_b=i_{Cmid}+i_o \quad (6.21)$$

where i_{Cmid} denotes the current through the DC bus capacitor C. Considering an ESR $r_{C'}$ in the DC bus capacitor, i_{Cmid} and V_{DC} can be related as follows in Laplace domain.

$$i_{Cmid}(s)=\frac{v_{DC}(s)}{r_{C'}+1/sC} \quad (6.22)$$

The DC link voltage can be written as: $v_{DC}=i_oZ_L$, which leads to the relationship: $\Delta v_{DC}=i_o\Delta Z_L+Z_L\Delta i_o$. Substituting v_{DC} with $v_{DC}=V_{DC}+\Delta V_{DC}$ and duty ratios as $d_{kH}=D_{kH}+\Delta d_{kH}$ in Eq. (6.23) the following relation is obtained.

$$\frac{sC}{sCr_{C'}+1}\Delta V_{DC}+\frac{\Delta V_{DC}}{Z_L(s)}=(D_{AH}-D_{CH})\Delta i_a+(D_{BH}-D_{CH})\Delta i_b+(\Delta d_{AH}-\Delta d_{CH})I_A+(\Delta d_{BH}-\Delta d_{CH})I_B \quad (6.23)$$

where, the instantaneous DC link voltage i.e. v_{DC} is represented as the sum of two components i.e. a small signal voltage ΔV_{DC} and the average DC voltage i.e. V_{DC}, and

similarly, $d_{AH} = D_{AH}+\Delta d_{AH}$. Applying Laplace transformation on the both sides of Eq. (6.20) and with zero perturbation on the phase currents, the following relationship is obtained.

$$\frac{\Delta d_{AH}(s)}{\Delta v_{DC}(s)} = \frac{sC(r_{C'} + Z_L(s)) + 1}{Z_L(s) I_A (1 + sCr_{C'})} \tag{6.24}$$

Dividing Eq. (6.20) by Eq. (6.24), the phase-current to the duty ratio transfer function can be established.

$$G_p(s) = \frac{\Delta i_a(s)}{\Delta d_{AH}(s)} = \frac{(r_{C'} + Z_L(s)) I_A (1 - {4D_{AH} + D_{BH} + D_{CH}}/{3})}{sL(sCZ_L(s) + sCr_{C'} + 1)} \tag{6.25}$$

Similar plant characteristics will be obtained by analyzing the other two phases of AC-DC converters (phase 'B' and 'C').

6.1.3. Regulation issues with the PI control

The control objectives are to: (i) regulate the output voltage V_O at its reference value V_O^*, (ii) maintain the unity input power factor operation for all three-phases. In a conventional control system, the output of the DC link voltage compensator (PI) acts like an active power reference and is multiplied to three input phase voltages to generate the current references for the inner loop current controllers (PI). Therefore, the loop gain transfer function for the phase current control can be represented by: $L(s)=G_p(s)G_c(s)$, which is given by the following relationship.

$$L(s) = \frac{(k_p s + k_i) Y (r_{C'} + Z_L(s))}{s^2 L(1 + sCZ_L(s) + sCr_{C'})} \tag{6.26}$$

where, $G_c(s)=k_p+k_i/s$ and $Y=I_A(4D_{AH}-D_{BH}-D_{CH})/3$. Substituting $Z_L(s)$ from Eq. (6.12) into the above relation, and applying Routh-Hurwitz stability criterion, it is obtained that both the following conditions must hold simultaneously.

$$nL < RL_{eq}CY \tag{6.27}$$

$$(nRLC - R^2L_{eq}C^2Y)(L + Ak_pYL_{eq} + ARCYL_{eq}) > ALCk_iYL_{eq}{}^2 \tag{6.28}$$

Although the second condition can be satisfied by tuning k_p and k_i adaptively, the first requirement is totally dependent on the system parameters, load resistance and the operating duty ratios, which we have no control on. Therefore, the overall plant may lose its stability at some operating points of output load powers. Above all, even though the plant is stable at an operating point, the input power factor is not unity due to the narrow allowable range of PI parameters, according to the imposed condition at Eq. (6.29). To justify it mathematically, the overall phase of $i_a(s)/i_a{}^*(s)$, should be calculated and checked whether it can be set to zero, with allowable controller parameters.

$$arc\left(\frac{i_a(s)}{i_a{}^*(s)}\right) = arc\left(\frac{G_p(s)G_c(s)}{1+G_p(s)G_c(s)}\right) = arc\left(\frac{(k_ps+k_i)Y(r_{C'}+Z_L(s))}{s^2L+s^3LC(r_{C'}+Z_L(s))+(k_ps+k_i)Y(r_{C'}+Z_L(s))}\right) \tag{6.29}$$

The converter is operating as a PFC converter if the overall phase of the control loop, obtained from Eq. (6.27) can be made zero by tuning the PI parameters in their allowable ranges according to Eq. (6.28). In order to verify this, the plot of maximum attainable power factor i.e. $\cos(arc(i_a(s)/i_a{}^*(s)))$ against the load power is shown in Fig. 6.3, obtained from MATLAB using the design specifications provided in Table 6.1.

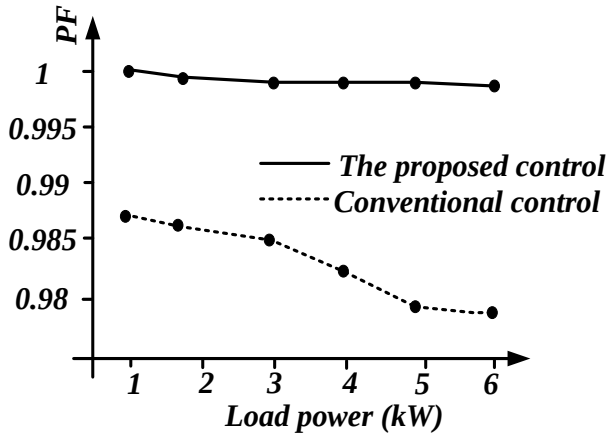


Fig. 6. 3. Power factor variation over load power at two different control strategies

As it can be seen from the Fig. 3, the power factor is reasonably less than unity at heavier loads, reducing the overall conversion efficiency. In addition, it increases the reactive power transfer to the intermediate DC capacitor (C), with twice of grid frequency ripple components. Furthermore, there is an inherent issue of instability, irrespective of PI parameters, according to Eq. (6.25), which makes the conventional control inappropriate in terms of regulation and stability of this cascaded AC-DC converter. In order to resolve these control issues, the state-feedback based control with reduced state observer design is proposed and explained in the Section 6.1.4.

Furthermore, as a part of special cases, the system stability at no load and short-circuit conditions is discussed. At no load ($R \rightarrow \infty$), the equivalent input impedance becomes as follows, which acts as a series RLC combination with equivalent resistance as $n^2(r_L+r_C)$.

$$Z_{in,NL} = \frac{s^2 L_{eq} C + sn^2 (r_L + r_C) C + n^2}{sC} = sL_{eq} + n^2 (\frac{1}{sC} + r_L + r_C) \tag{6.30}$$

From the small signal plant between DC voltage and phase ‘A’ duty, it can be inferred that the poles of the PFC plant i.e. the solutions of the characteristic equation i.e.

$1+sC(r_{C'}+Z_L(s))=0$ need to lie in the left-half plane, in order to ensure the stability of the converter at no-load.

The real parts of the solutions of $1+sC(r_{C'}+Z_L(s))=0$ are located at

$$\mathrm{Re}(p)=\frac{-n^2(r_L+r_C)+r_{C'}}{L_{eq}} \tag{6.31}$$

which is strictly negative, ensuring the stability of the equivalent converter plant at no-load condition. Similarly, the short-circuit condition i.e. $R\rightarrow 0$ yields to the equivalent PSFB input impedance form as follows:

$$Z_{in,SC}=\frac{s^2L_{eq}Cr_C+s(L_{eq}+n^2r_Lr_CC)}{sCr_C+1}=sL_{eq}+\frac{sn^2r_Lr_CC}{sCr_C+1} \tag{6.32}$$

The stability of the converter plant needs the real parts of the solutions of $1+sC(r_{C'}+Z_L(s))=0$ to be located at the left half plane. Substituting $Z_L(s)$ from the above expression, the characteristic equation stands out as follows.

$$s^3C^2L_{eq}r_C+s^2(CL_{eq}+C^2n^2r_Lr_C)+sCr_C+1=0 \tag{6.33}$$

Applying Routh-Hurwitz criterion in an equation $As^3+Bs^2+Cs+D=0$, BC-AD>0 must hold given all coefficients are individually positive, to prove strictly negative solutions. In the characteristic Eq. (6.33), BC-AD= $C^3r_Lr_C^2>0$ holds always true, which proves the strictly negative poles of the PFC plant at short-circuit conditions, implying its stability. Moreover, the stability and regulation of the system during no-load and short-circuit conditions are discussed more and supported by the experimental results in the Section V.

6.1.4. Observer Based State Feedback Control

The observer-based state-feedback control is designed for the PFC stage with a switching averaged load, representing the DC-DC converter stage. In this case, the second stage DC-DC converter is operated in open loop with a reference phase shift φ = nV_o^*/V_{DC}; where, V_o^* is the output voltage reference, 'n' is the transformer turns ratio and V_{DC} is the intermediate DC link voltage. A reference output DC link voltage will directly map to a particular V_{DC}, which acts as a controlled variable. Therefore, the DC-DC switching pulses will be generated in a conventional way with the calculated phase shift, as depicted in the well-established literature [22, 94] and shown in the control block diagram in Fig. 6.4.

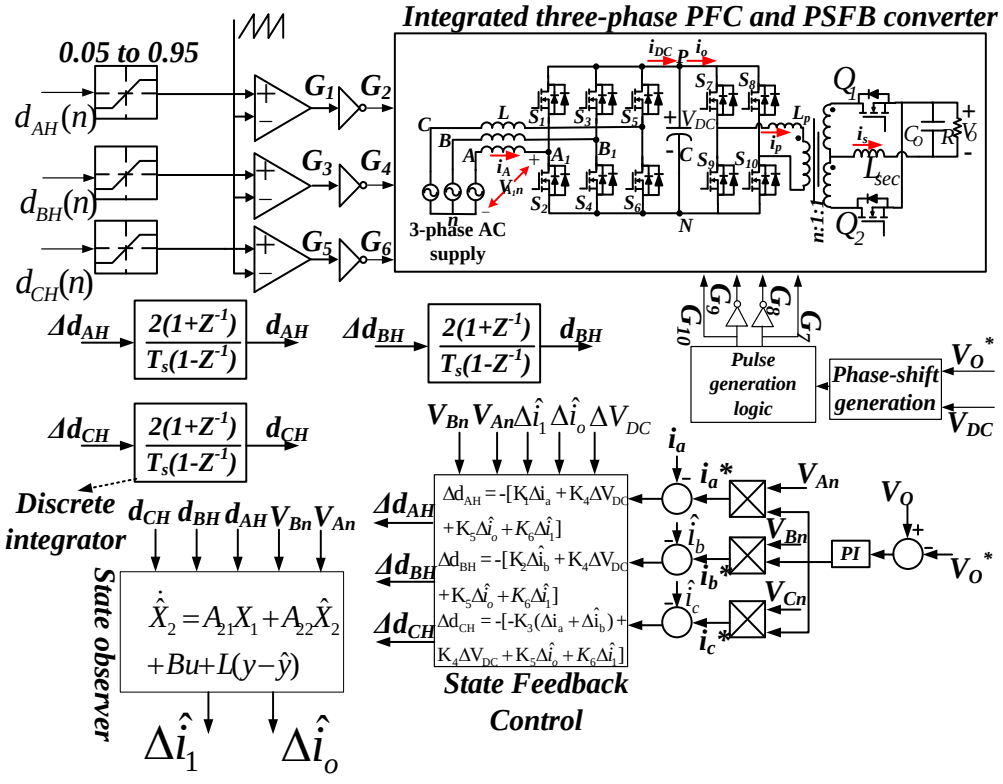


Fig. 6. 4. Control Strategy of the integrated PFC and PSFB converter

In order to establish the state feedback control of the cascaded AC-DC converter, it is important to determine the state variables in the system. By removing the redundancy in a three-phase balanced system, there are seven state variables i.e. two input phase voltages, two phase currents, the intermediate DC link voltage, primary current of the DC-DC stage and the output DC voltage. The state space equations for the overall converter stage are established as follows in Eq. (6.34) – Eq. (6.35) using Eq. (6.14) and applying $V_{nN}=(d_{AH}+d_{BH}+d_{CH}).V_{DC}/3$.

$$\frac{di_a}{dt} = -\frac{2d_{AH}-d_{BH}-d_{CH}}{3L}V_{DC} + \frac{V_{An}}{L} \tag{6.34}$$

$$\frac{di_b}{dt} = -\frac{2d_{BH}-d_{AH}-d_{CH}}{3L}V_{DC} + \frac{V_{Bn}}{L} \tag{6.35}$$

From the intermediate DC link capacitor current relation in Eq. (6.36), the following is obtained.

$$i_a(d_{AH} - d_{CH}) + i_b(d_{BH} - d_{CH}) = i_{Cmid} + i_o \tag{6.36}$$

where i_o is the PSFB input current, i_{Cmid} is the current flowing through the intermediate DC link and also, let's assume $i_1=i_o'$, i.e. first derivative of i_o, which would be used in later analyses. From the Eq. (12) and Fig. 6.4, the following relationship can be established.

$$k(s^2(R + r_C)CL_{eq} + s\left(L_{eq} + n^2C(r_LR + r_Lr_C + Rr_C)\right) + n^2R)i_o(s) = (sC(R + r_C) + 1)v_{DC}(s) \tag{6.37}$$

which implies

$$k\left(R'CL_{eq}\frac{d^2i_o}{dt^2} + L'_{eq}\frac{di_o}{dt} + n^2Ri_o\right) = (CR'\frac{dv_{DC}}{dt} + v_{DC}) \tag{6.38}$$

Where, $R'=(R+r_C)$, $L'_{eq}=L_{eq}+n^2C(r_LR+r_Lr_C+Rr_C)$.

Assuming $\frac{di_o}{dt} = i_1$, Eq. (39) can be restructured as follows:

$$k\left(R'CL_{eq}\frac{di_1}{dt}+L'_{eq}i_1+n^2Ri_o\right)=(CR'\frac{dv_{DC}}{dt}+v_{DC}) \quad (6.39)$$

Since the PSFB DC-DC stage is modeled as an equivalent load, its associated state variables are embedded in the above relation. Therefore, it is required to redefine the state variable vector to **X** = [i_a i_b V_{DC} i_o i_1] based on the Eq. (6.34)-Eq. (6.39), where, i_o and i_1 are two augmented state variables. The input variable vector is defined as: **U** = $[V_{An}\ V_{Bn}]^T$. This control will be carried out with utilizing four measurements i.e. i_a, V_{DC}, V_{An}, V_{Bn}. As a benefit of the proposed control, one phase current sensor can be eliminated by estimating its value accurately and using it as a feedback state variable. In our design, phase 'A' current information is fed back directly from sensor and phase 'B' current is estimated by the observer and used as another state variable.

Thereby, combining Eq. (6.34) - Eq. (6.39) and comparing with the state space equation for linear time invariant (LTI) systems i.e. **x'=Ax+Bu**, the matrices **A** and **B** are determined as follows.

$$A=\begin{pmatrix} 0 & \frac{d_{BH}+d_{CH}-2d_{AH}}{3L} & 0 & 0 & 0 \\ \frac{d_{AH}-d_{CH}}{C} & 0 & \frac{d_{BH}-d_{CH}}{C} & \frac{-1}{C} & 0 \\ 0 & \frac{d_{AH}+d_{CH}-2d_{BH}}{3L} & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 1 \\ \frac{d_{AH}-d_{CH}}{CL_{eq}} & \frac{1}{R'CL_{eq}} & \frac{d_{BH}-d_{CH}}{CL_{eq}} & \frac{-(n^2+1)R}{R'CL_{eq}} & \frac{-L'_{eq}}{L_{eq}R'C} \end{pmatrix} \quad (6.40)$$

$$B=\begin{pmatrix} 1 & 0 \\ 0 & 1 \\ 0 & 0 \\ 0 & 0 \\ 0 & 0 \end{pmatrix} \quad (6.41)$$

In this control, the output variable is the final DC output voltage i.e. $V_O = V_{DC}\varphi/n$. As seen from the Fig. 2(a) (ignoring the ESRs), the output current can be written as:

$$i_o = \frac{V_o}{kR} + \frac{C}{k}\frac{dV_o}{dt} \tag{6.42}$$

Replacing dV_o/dt from the above relation into Eq. (6.36), the output voltage V_o can be expressed in terms of the system state variables, as follows.

$$\frac{n}{\varphi}\left(\frac{ki_o}{C} - \frac{V_o}{RC}\right) + \frac{i_o}{C} = \frac{i_a(d_{AH} - d_{CH}) + i_b(d_{BH} - d_{CH})}{C} \tag{6.43}$$

$$V_o = \frac{R\varphi}{n}\left[\left(1 + \frac{nk}{\varphi}\right)i_o - (d_{AH} - d_{CH})i_a - (d_{BH} - d_{CH})i_b\right] \tag{6.44}$$

Comparing the above relation with the state space equation **Y = CX+DU** for a LTI system, **D** is obtained as null (**0**) matrix and **C** is as follows:

$$C = \frac{R\varphi}{n}\begin{pmatrix} -(d_{AH} - d_{CH}) & 0 & -(d_{BH} - d_{CH}) & 1 + \dfrac{nk}{\varphi} & 0 \end{pmatrix} \tag{6.45}$$

C can be split as $\mathbf{C = [C_1 \mid C_2]}$, where $\mathbf{C_1}$ and $\mathbf{C_2}$ are 1×2 and 1×3 matrices, respectively with the same sequence of elements in **C** matrix. Since i_b, i_o and i_1 will be obtained from the state-estimators by observer design, the state variable vector can be split as $\mathbf{X = [X_1 \mid X_2]^T}$, where $\mathbf{X_1} = [i_a\ V_{DC}]$ is measured vector and $\mathbf{X_2} = [i_b\ i_o\ i_1]$ is the observer based estimated vector. Therefore, the matrix **A** can be split as follows with retaining same sequence of elements.

$$A = \begin{pmatrix} A_{11} & A_{12} \\ A_{21} & A_{22} \end{pmatrix} \tag{6.46}$$

where, $\mathbf{A_{11}}$, $\mathbf{A_{12}}$, $\mathbf{A_{21}}$ and $\mathbf{A_{22}}$ are 2×2, 2×3, 3×2, 3×3 matrices, respectively obtained from matrix **A** in Eq. (6.34). Similarly, $\mathbf{B = [B_1|B_2]^T}$, where $\mathbf{B_1}$ and $\mathbf{B_2}$ are 2×2 and 2×3

matrices from **B** in Eq. (6.41), respectively. In a reduced state observer design approach, the estimated $\mathbf{X_2}$ can be expressed as follows.

$$\frac{d\widehat{X_2}}{dt} = A_{21}X_1 + A_{22}\widehat{X_2} + B_2u + L(y - \hat{y}) \tag{6.47}$$

$$y = C_1X_1 + C_2X_2 \tag{6.48}$$

$$\hat{y} = C_1X_1 + C_2\hat{X}_2 \tag{6.49}$$

where, **L** is an observer gain matrix, given by $\mathbf{L = (L_1\ L_2\ L_3)^T}$. Substituting Eq. (6.48)-(6.49) in Eq. (6.47), the following relationship of the estimation errors in state variables i.e. $e = X_2 - \hat{X}_2$ can be established.

$$\dot{e} = A_{22}e + LC_2e \tag{6.50}$$

Therefore, in order to minimize the estimation error asymptotically to zero, eigenvalues of the matrix ($\mathbf{sI\text{-}A_{22}+LC_2}$) have to lie on the left-half plane. Since the eigenvalues of ($\mathbf{sI\text{-}A_{22}+LC_2}$) are same as the solutions of det ($\mathbf{sI\text{-}A_{22}+LC_2}$) = 0, Routh-Hurwitz criterion could be applied to find the conditions for obtaining negative eigenvalues, which leads to the following relationships.

$$eig\begin{pmatrix} s + qL_1(d_{BH} - d_{CH}) & qL_1(1+\frac{nk}{\varphi}) & 0 \\ qL_2(1+\frac{nk}{\varphi}) & s + qL_2(1+\frac{nk}{\varphi}) & -1 \\ \frac{d_{CH} - d_{BH}}{CL_{eq}} + qL_3(d_{BH} - d_{CH}) & \frac{R(n^2+1)}{CL_{eq}R'} + qL_3(1+\frac{nk}{\varphi}) & s + \frac{L'_{eq}}{L_{eq}RC} \end{pmatrix} < 0 \tag{6.51}$$

$$L_1L_2L_3(1+\frac{nk}{\varphi})(d_{BH} - d_{CH}) < 0 \tag{6.52}$$

$$L_1(d_{BH} - d_{CH}) + L_2(1+\frac{nk}{\varphi}) > 0 \tag{6.53}$$

where, q=Rφ/n. One noteworthy point is that the observer gains are independent of the load resistance 'R' and hence, any load variation would not affect the stability and

observability conditions, as long as L_1, L_2, L_3 are chosen by satisfying the conditions Eq. (6.52)-Eq. (6.53). In our design, L_3 is always set positive, and $L_1(d_{BH}-d_{CH})$ and $L_2(1+nk/\varphi)$ are set positive to satisfy the requirements.

The reference duty ratios for three phases can be generated through state-feedback control as:

$$\Delta d_{AH} = -[K_1\Delta i_a + K_4\Delta V_{DC} + K_5\Delta\hat{i}_o + K_6\Delta\hat{i}_1] \quad (6.54)$$

$$\Delta d_{BH} = -[K_2\Delta\hat{i}_b + K_4\Delta V_{DC} + K_5\Delta\hat{i}_o + K_6\Delta\hat{i}_1] \quad (6.55)$$

$$\Delta d_{CH} = -[-K_3(\Delta i_a + \Delta\hat{i}_b) + K_4\Delta V_{DC} + K_5\Delta\hat{i}_o + K_6\Delta\hat{i}_1] \quad (6.56)$$

where K= [K_1 K_2 K_3 K_4 K_5 K_6] is the gain vector and Δi_a, Δi_b, Δi_o and Δi_1 are the variations in the respective currents with respect to the previous sampling. The state space equations for X_1 and X_2 is represented by the following relationships.

$$\frac{d\widehat{X_1}}{dt} = A_{11}X_1 + A_{12}\widehat{X_2} + B_1U \quad (6.57)$$

$$\frac{d\widehat{X_2}}{dt} = A_{21}X_1 + A_{22}\widehat{X_2} + B_2U \quad (6.58)$$

Taking Laplace transformation on both sides of Eq. (6.57) and Eq. (6.58) and making the variation in the input voltages to be zero, the following expressions can be obtained.

$$\frac{\Delta X_1(s)}{\Delta X_2(s)} = (sI - A_{11})^{-1}A_{12} \quad (6.59)$$

$$\frac{\Delta X_2(s)}{\Delta X_1(s)} = (sI - A_{22})^{-1}A_{21} \quad (6.60)$$

As both the matrices A_{11} and A_{22} are dependent on the control variables i.e. phase duty ratios, the ranges of the gain parameters need to be determined from the stability condition that the eigenvalues of the matrices ($sI-A_{11}$) and ($sI-A_{22}$) must lie on the left half plane.

$$(sI - A_{11}) = \begin{pmatrix} s & \frac{2d_{BH}^{*} - d_{AH}^{*} - d_{CH}^{*}}{3L} \\ \frac{d_{CH}^{*} - d_{AH}^{*}}{C} & s + \frac{L'_{eq}}{L_{eq}RC} \end{pmatrix} \tag{6.61}$$

$$(sI - A_{22}) = \begin{pmatrix} s & 0 & 0 \\ 0 & s & -1 \\ 0 & \frac{R(n^2+1)}{CL_{eq}R'} & s + \frac{L'_{eq}}{L_{eq}RC} \end{pmatrix} \tag{6.62}$$

From Routh-Hurwitz stability criterion, the following three conditions must hold to ensure the negative eigenvalues.

$$\frac{1}{R^2C^2} + \frac{4(n+1)}{CL_{eq}} > 0 \tag{6.63}$$

$$(2K_1\Delta i_a + K_2\Delta i_b)K_2 > 0 \tag{6.64}$$

$$K_4, K_5, K_6 > 0 \tag{6.65}$$

Eq. (6.63) always holds as it is a sum of two positive quantities. K_4, K_5 and K_6 can be set any positive quantities to ensure the stability. However, the values of K_1 and K_2 will be condition specific, depending on the variations in the phase currents. One easy way to set these parameters is to set K_2 a positive value and $K_1 > -K_2(\Delta i_b/2\Delta i_a)$, which will satisfy Eq. (6.64). Therefore, at each sample Δi_a and Δi_b are to be computed and accordingly, K_1, K_2 will have to be set. Thereby, the operating duty ratios are obtained by the discrete time domain integration of Δd_{AH}, Δd_{AH} and Δd_{AH}, generated by Eq. (6.54)-(6.56). The PFC gate pulses are generated by feeding the duty ratios to a saturation block (0.05-0.95), PWM generator and dead-band module, shown in Fig. 6.4.

I. Selection of controller and observer poles

The poles for the state-feedback controller are placed based on fixing a settling time of two line cycles i.e. 5ms for both phase 'A' current and intermediate DC link voltage at the start-up as well as under any load / line transient. Therefore, the farthest pole magnitude would be corresponding to inverse of 1/3rd settling time, as the 2% settling time is typically 3x time constant in an asymptotic tracking. Hence, in our design, all the state-feedback poles are set at or below -1/(5/3)ms = -600Hz. Therefore, the characteristics equation by pole placement method (three repeated poles at -600Hz) becomes: $T_{sfb}(s)=(s+2\pi x600)^3$. Comparing the polynomial coefficients of $T_{sfb}(s)$ with the determinant of $\mathbf{(sI-A_{11})}$, the controller parameters K_1 to K_6 are obtained. The overshoots in the controlled state variables with variation of controller pole locations are obtained from a simulation, plotted in Fig. 6.6.

The objective of the pole placement for the state-feedback control is to ensure settling of all state variables by 5ms i.e. two line cycles at the start-up as well as during load / line transient. Therefore, the mathematical closed-loop transfer function model of a state-variable to its reference is checked with a step response. Fig. 6.5 shows the step response of the transfer function of DC link voltage to its reference at 4 different pole locations. As can be seen from the above simulation result, five repeated poles at -800Hz results in minimum overshoot and a settling time below 3 ms, which satisfies our target. Five different poles each at 100Hz interval starting from -600Hz results in maximum overshoot, which is not desired in hardware implementation.

Therefore, selecting the controller poles at -800Hz (five repeated), the state estimators are designed. Under a closed loop step response conducted in phase 'B'

current (i_b), it takes less than 2 ms to reach steady state, as shown in Fig. 6.6. Also, there remains a constant estimation delay of 40µs between the response patterns with and without observer (three repeated observer poles at -50 kHz), which keeps a good agreement with the theoretical calculations. At different observer pole locations (two poles at -50 kHz, one at -30 kHz), Fig. 6.7 exhibits that the observer response is delayed by 80µs, which is expected due to decreasing the pole magnitudes.

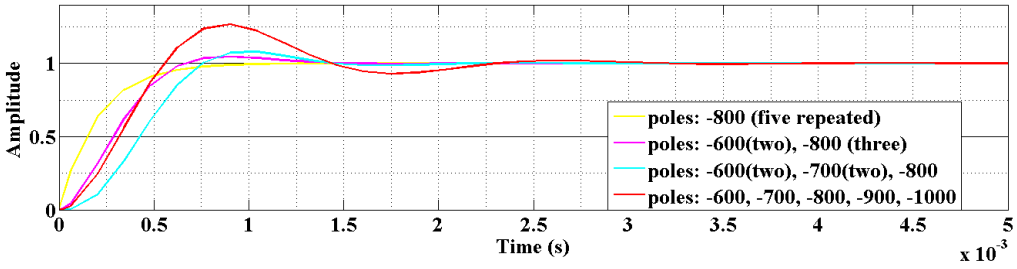


Fig. 6. 5. Step response of $V_{DC}(s)/V_{DC}^*(s)$ at different pole locations

In the process of state estimation, the estimation time is very crucial particularly for i_b, as any estimation time delay in i_b would lead to degradation of power factor and hence, reduction in efficiency. In the pole placement method, the observer poles (ω_p) are inversely related to the tracking time. With a requirement of keeping power factor above 0.995 needs to ensure the time delay is not more than 40µs, which is four switching cycles. Due to the asymptotic tracking, the net estimation time is typically 3 times of the time constant (τ), where $\tau=1/\omega_p$. Hence, the observer pole with maximum absolute value is -1/(40/3)µs = -75.1 kHz. In our design, all three poles are set at the same location i.e. -75.1kHz, which gives us the characteristic equation as $T_{ob}(s)=(s+2\pi x75100)^3$. By comparing the polynomial coefficients of $T_{ob}(s)$ with the determinant of $(\mathbf{sI-A_{22}+LC_2})$ in Eq. (6.51), the observer gains L_1, L_2, L_3 can be solved in terms of operating conditions and system parameters. It is to be noted that the

observer gains vary with the operating conditions (instantaneous duty ratios, phase current values) even under a fixed set of pole locations. The overshoots in the estimated state variables at different pole locations are obtained from a simulation, plotted in Fig. 6.6-6.7.

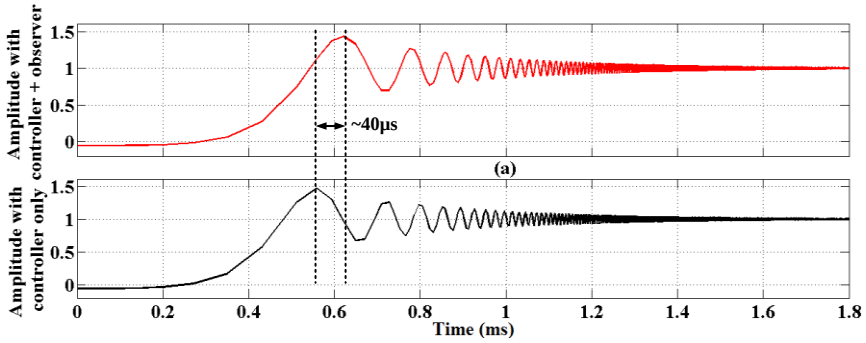


Fig. 6. 6. Closed loop step-response of phase 'B' current with and without observer at poles (repeated -50kHz)

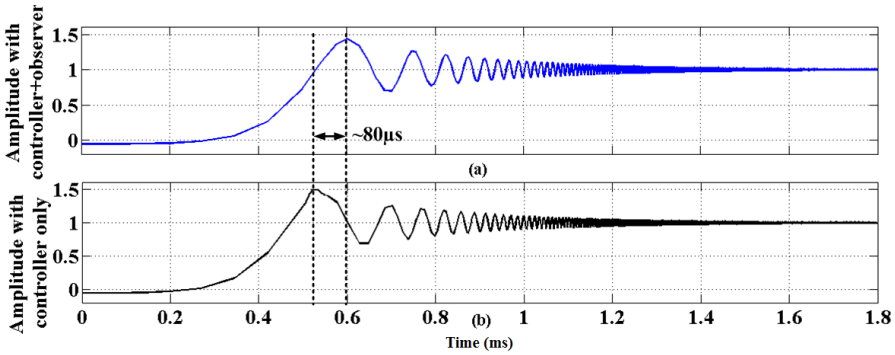


Fig. 6. 7. Closed loop step-response of phase 'B' current with and without observer at poles (two at -50kHz, one at -30kHz)

II. Disturbance immunity of the proposed control system

Besides confirming the stability and observability of the cascaded converter, it is also required to justify the disturbance immunity of the system. Therefore, zero mean high frequency Gaussian disturbances are added to the state-feedback controller outputs (system inputs) i.e. the manipulated phase duty ratios. In a simulation study,

the net duty ratio is generated by adding the state-feedback output with a 10MHz noise pattern n(t)=0.1 sin ($2\pi x10^7 t$), which is restricted within 10% band of the maximum variation of any duty ratio. For an illustration to the disturbance immunity, the transients of perturbation of five state variables are shown in Fig. 6.8. It is noted that the transient oscillations created due to disturbance injection dies down to zero within 40μs i.e. four switching cycles.

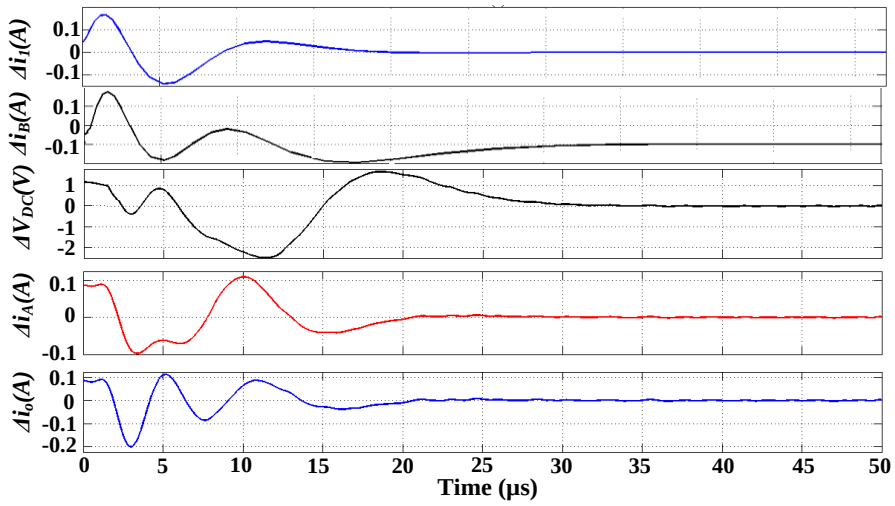


Fig. 6. 8. Changes in State variables under 10MHz Gaussian disturbance

One major advantage of this control is that none of the observer and state-feedback gain parameters depend on the load resistance variation and hence, ensures stability and high regulation, irrespective of any load variation. On the contrary, in case of conventional PI control, the cascaded converter has the instability issues, imposed by the load variation. In addition, as opposed to the fact that the input power factor reduces at some operating points in a conventional control, the power factor remains very close to unity (i.e. negligible reactive power transfer) with any variation in load power, shown in Fig. 6.3.

6.1.5. Experimental Results

In order to verify the proposed control methodology, the converter is simulated with an input AC voltage of 230V (phase-neutral RMS) at 400 Hz for avionics applications with the specifications of some of the RTRUs in future MEAs. Both the PFC and PSFB stage converters are designed based on the well-established design considerations, presented in the literature [22, 43, 91]. The key design parameters and specifications are summarized in Table 6.1. As a noteworthy design consideration, synchronous rectification is used to drive the secondary side MOSFETs of DC-DC stage to reduce the conduction loss and each secondary switch is realized by three MOSFETs in parallel for reducing the effective conduction resistance.

Table 6. 1. Key design parameters and their specifications

Parameters	Values	Quantity
Input AC voltage (V_{in})	230V, 400Hz, 3-phase	-
Output voltage reference (V_o^*)	28V	-
Output power (P_{out})	6kW	-
Boost inductance	0.4mH	3
Intermediate DC capacitance	0.1mF	1
PFC MOSFETs	CMF10120D (SiC, 1.2kV)	6
Transformer turns ratio (n)	12:1:1	-
Primary leakage inductance (L_p') of DC-DC stage	8 µH	1
Secondary inductor (L_s)	7.5 µH	1
DC link capacitor (C_{DC})	3 mF	1
Primary MOSFETs	SiC (1.2kV/24A)	4

Secondary MOSFETs	FDH055N15A (145A, 160V)	6
Switching frequency (f_{sw})	100 kHz	-

As a proof-of-concept verification to the proposed control methodology, a laboratory prototype of 6kW (continuous)/8kW (peak) cascaded PFC and PSFB converter is designed and developed. The control algorithm is implemented in a floating-point DSP TMS320F28335. In order to validate the power factor regulation issue with the conventional PI control, the PFC stage waveforms along with output DC voltage are shown in Fig. 6.9.

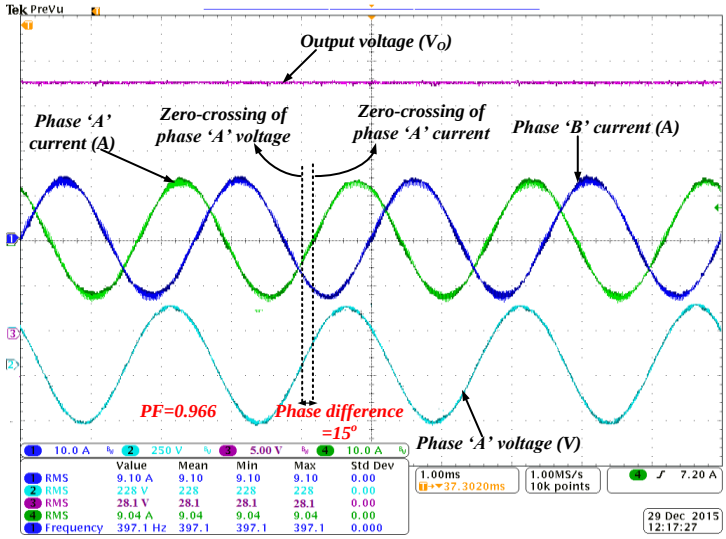


Fig. 6. 9. PFC stage waveforms @ 6kW, 230V AC input

This shows that although the overall system maintains stability, a 15° phase difference i.e. PF=0.966 exists between the phase voltage and current in the PI based control, which gives an overall efficiency to 91% according to the measurements. This is a major disadvantage / limitation of the conventional PI control, which is taken care of by the proposed control, as verified through the experiments.

Fig. 6.10 shows the steady state operation of the PFC stage with intermediate DC link voltage of 650V at 6kW with the proposed state-feedback-based control using observer and represents the stable and settled down output DC link voltage of the PFC. The experimental result at 6kW exhibits a conversion efficiency of 98.3%, a PF of 0.998 and a THD of 4.1% for the PFC stage, which proves the operation of power converter with significantly better power quality and higher conversion efficiency than the conventional control method. Fig. 6.11 shows that the output DC voltage of the PSFB converter is settled at 28V DC with a ripple within ±1% and with an efficiency of 97.1%. The secondary inductor current is averaged around 214 A with a ripple of ±10% and it is of twice the switching frequency, as the voltage across the inductor is rectified form of the linked secondary voltage. The overall efficiency of the integrated PFC and PSFB stage is measured to be 95.4%, which is 4.4% higher than the conventional control.

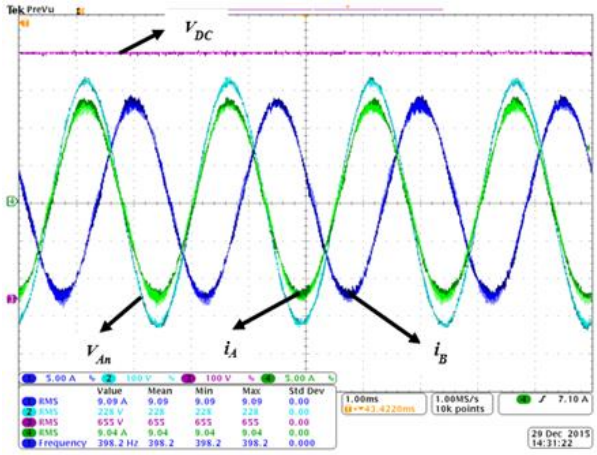


Fig. 6. 10. V_{DC}=650V, i_A (RMS) =i_B (RMS) =9.06A, V_{An} (RMS) =230V @ 6kW

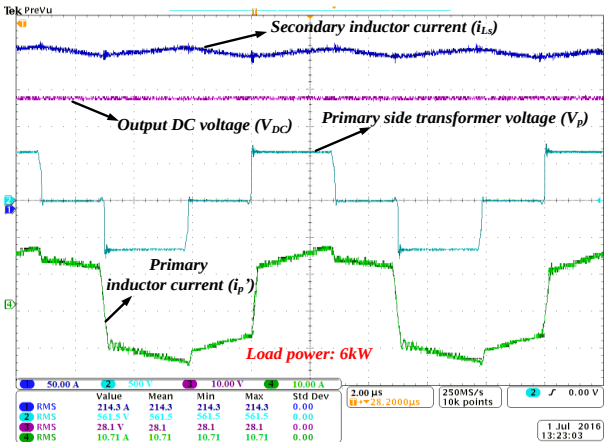
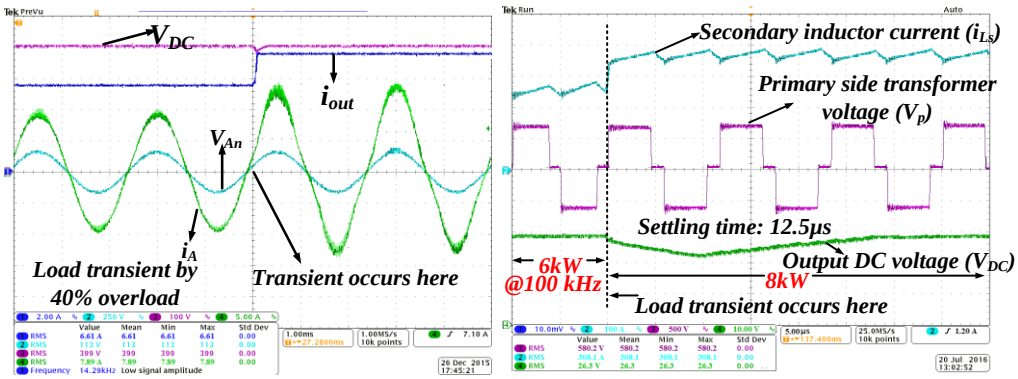


Fig. 6. 11. PSFB waveforms at 6kW load power; V_{DC} = 650V, V_O = 28V, Output current: 214.3A

As can be seen in the above waveform, there are periodic ringing oscillations during the rise and fall of the primary side transformer voltage as well as on the secondary inductor current waveform. This majorly happens due to the resonance caused by parasitic gate-source & drain-source capacitances of SiC MOSFETs and trace (& transformer leakage) inductance, which require developing a parasitic noise model for being included in the dynamic model of the converter plant, which is out of scope in this work.

In addition, the cascaded converter is tested at variable load conditions to illustrate the effectiveness of control methodology. Under 33% overload (6kW to 8kW), it takes 100µs (less than $1/20^{th}$ a power cycle) to settle down to the intermediate DC link reference voltage and phase currents, which indicates a reasonably fast transient dynamics of the proposed control. The time taken by the DC-DC stage to reach the reference output DC link voltage level i.e. 28V is 20µs. The waveforms under the load transient are shown in Fig. 6.12.



(a) (b)

Fig. 6. 12. (a) The converter waveforms under load transient from 6kW to 8kW (b) PSFB waveforms at load transient from 6kW to 8kW; V_{DC} =650V, V_O = 28V, f_{sw} = 100 kHz.

Furthermore, the undershoot in the output DC voltage under this load transient with the state-feedback controller is 10% of the reference value, which proves the state-feedback control to be robust in terms of voltage regulation. The output voltage ripple is maintained below ±1% at the steady state overload condition. Both the measured efficiencies and input power factor at the entire load power range with the proposed control are more than the reported peak efficiency and PF values in the previous related works i.e. 91.6% and 0.98 in [149], 92% and 0.99 in [150].

Zoomed-in phase current (i_b) waveforms near its peak with the observer implementation is shown in Fig. 6.13.

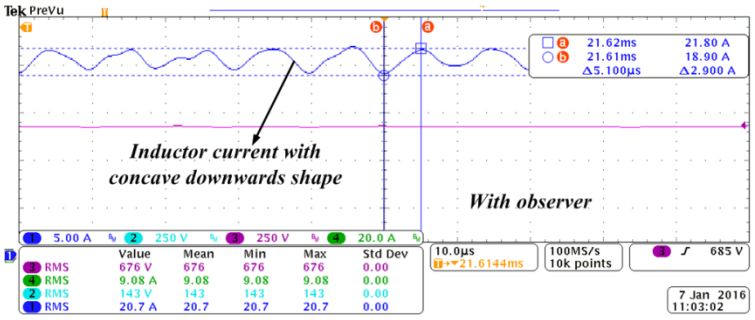


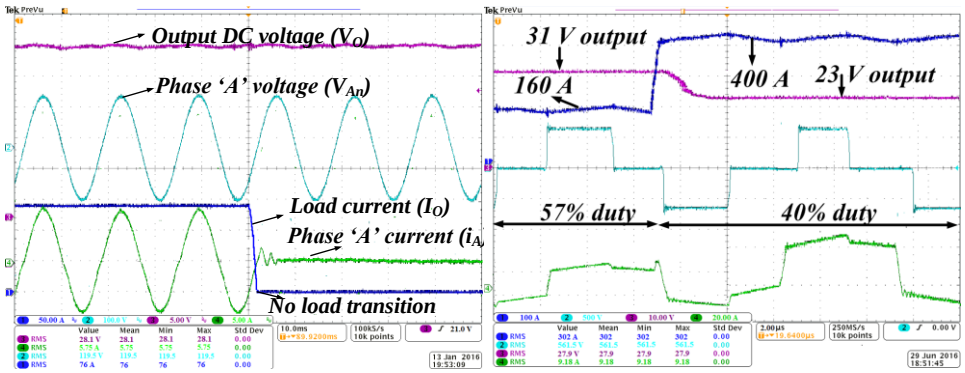
Fig. 6. 13. Zoomed-in phase 'B' current with the observer

As suggested by Fig. 6.13, the inductor current variation dynamics in a switching cycle becomes more parabolic or high order polynomial with using the observer due to its own effect of higher order filter dynamics. Moreover, the ripple content near the inductor current peak matches with the theoretically calculated ripple amplitude, which is expected because the duty command from the state-feedback controller at any phase instant does not depend on the observer model. This is justified from the theoretical fact that both the controller and observer are designed using separation principle (i.e. pole placement procedures for the controller and observer are independent).

The integrated PFC & PSFB stage is tested with a no-load condition with 230V 400Hz input AC voltage, as shown in Fig. 6.14(a). As soon as the no load is detected by load power estimation logic, the PFC side pulses are withdrawn and therefore, the intermediate DC link voltage is held almost constant due to having no discharging path, except high value of parallel bleeding resistor. Accordingly, the PSFB output voltage is maintained at its reference value (28V) by modulating the phase shift, even if there is any slight variation in the intermediate DC link voltage due to its slow decay through bleeding resistor. However, in this experiment, the intermediate DC voltage is held almost constant at 650V due to a very high (1MΩ) bleeding resistor. Thereby, the converter maintains regulated output voltage and DC bus voltage at such a condition, which justifies the theoretical analyses.

The short-circuit at the output terminal is also experimented with 230V 400Hz input AC voltage using a power supply equipped with delivering maximum 10kW. Since there is no output voltage regulation at short-circuit case, the objective is set at fixing the output at minimum 5V with delivering 400A load current. The load resistance is

reduced to 0.08Ω with a 400A output current at the short-circuit instant. After short-circuit detection, the phase-shift angle amount is reduced as much required to maintain the total power below 10kW and regulates the output voltage at 23V. Fig. 6.14(b) represents the DC-DC-stage waveforms during short-circuit.



(a) (b)

Fig. 6. 14. (a) Converter waveforms at no-load condition (b) PSFB stage waveforms during short circuit test

6.2 Variable DC Link Based Maximum Efficiency Tracking in RTRU

It is challenging to ensure efficient operation of a cascade two-staged AC-DC topology due to non-linear, non-monotonic variation of power efficiency characteristics of the two different converters. A number of research works has been individually carried out on three-phase six-switch PFC [5-7, 16] and PSFB DC-DC converter [91-97] by outlining their individual advantages. A number of research works [154-160] is carried out on a two-staged integrated AC-DC converter for different applications, aiming at enhancing the net efficiencies using different methods. The research work in [154] proposes a single-phase SEPIC PFC followed by a full-bridge LLC converter, connected to a high-voltage electric vehicle (EV) battery for charging

application. Instead of using conventional fixed DC link (PFC output) control with variable frequency (at the resonant stage) method, the research in [154] proposes a control approach with variable intermediate DC link voltage, depending on the battery voltage. The analysis shows an increase in efficiency by 3%, which is only applicable for a converter system with variable output voltage i.e. for battery load applications. Furthermore, an intelligent auto-tuned method of maximum efficiency tracking for a PFC and DC-DC integrated converter system is proposed in [155]. The key approach for optimum efficiency is dynamically optimized variation of the intermediate bus voltage as a function of the estimated load power. The model describing dynamic variation of intermediate bus voltage is developed by extrapolating several experimental efficiency data at different fixed DC bus voltage and different power levels. However, this is only an empirical method, which is not guaranteed to generate optimum DC bus voltage reference at variable operating conditions.

Furthermore, a variable switching frequency based control is implemented in a single-stage dual active bridge based AC-DC converter for light load performance improvement [156]. After estimating the load power, the switching frequency is tuned to ensure zero voltage switching (ZVS) and reduce the grid current distortion problem at lighter load to improve efficiency. However, a wide variation of switching frequency may affect the electromagnetic interference (EMI) spectrum, as the front-end EMI filter is typically designed with respect to a fixed switching frequency. In addition, a variable DC link approach is implemented in three-level single-stage PFC converter for achieving high power factor [157]. Since there is an inherent current distortion issue in a discontinuous conduction mode (DCM) operated multi-level PFC converter with a

lower DC link voltage, adjusting the DC link with respect to the line voltage improves the input power quality. However, in DCM, the efficiency drops with higher DC link voltage, enforcing a trade-off between the efficiency and power factor.

In addition, an on-line maximum duty point tracking technique has been proposed as an algorithm to improve two-stage server power efficiency for an integrated PFC circuit topology followed by a phase-shifted full bridge (PSFB) converter [158-159]. An optimized DC bus voltage is dynamically obtained to maximize PSFB duty ratio i.e. to minimize the primary side circulating loss, which helps in enhancing efficiency by 2.5% for a 2kW prototype. However, the approach holds true below a certain load power as the PFC conduction loss dominates at higher load power with a lower DC link voltage i.e. higher phase shift, which will degrade the overall efficiency. Furthermore, a control scheme is developed for improving efficiency in high step down dual-active bridge DC-DC converter [160]. Based on the output load power, the control angle (governing the duty ratio) and phase shift angle between two legs are derived from a state feedback control algorithm in order to track maximum efficiency trajectory.

In addition, a variable switching frequency-based efficiency maximization algorithm is proposed for a PSFB DC-DC converter over a wide load range [161]. Based on the output voltage and load power, an optimized combination of effective duty cycle and switching frequency is generated from the controller proposed in [161]. Although this method shows improved efficiency in comparison to the fixed frequency control, the switching frequency calculation algorithm is based only on ensuring ZVS, but neglects the effect of other losses in the system.

In the research work in [162], a variable dc link technique is proposed to track the maximum efficiency point of the LLC converter for plug-in electric vehicle battery-charging applications over a wide battery voltage range. Since the proposed charging system in [162] consists of a PFC followed by a LLC converter, the intermediate DC link voltage is varied proportionally to the battery voltage by operating the LLC converter at its resonant frequency. However, this method only minimizes the LLC converter loss, but does not consider the PFC loss in total loss minimization. Also, similar concept is not applicable for the proposed converter system in our work, which deals with a constant output voltage at the load.

Addressing the aforementioned challenges and concerns in efficiency improvement of a cascaded AC-DC isolated topology, our research in [163] proposes a variable intermediate DC link voltage-based control method. The intermediate DC bus voltage reference is obtained from the operating conditions (i.e. input AC conditions, load power, switching frequencies, component specifications) subject to minimizing the total power loss. From the detailed mathematical loss modeling, it is analytically shown that the total loss varies in a non-monotonic, non-linear fashion with the intermediate DC bus voltage at a fixed load power level. Therefore, the proposed method obtains the optimum DC bus voltage reference (within a certain upper and lower limit) using numerical solution of loss-minimization condition and is validated by experimental results.

6.2.1. Loss Modeling of the Integrated AC-DC Converter

The total power losses in the integrated two-stage AC-DC conversion stage are categorized into conduction, switching, core and other losses incurred in PFC and

PSFB converters separately. Each category of loss is mathematically analyzed in the later subsections.

I. Loss analyses in the PFC stage:

As a first step to determine the conversion efficiency, it is important to establish an accurate loss estimation model for the integrated three-phase boost PFC & DC-DC PSFB converter. The losses in the PFC stage can be majorly classified into several categories, such as (i) conduction & switching losses in the power semiconductor devices, (ii) conduction loss in the boost inductors and ESR of the DC link capacitor, and (iii) dead-time loss in the anti-parallel Schottky diodes. All these losses majorly depend on the intermediate DC link voltage, values of RMS currents through different phases, switches and the DC link capacitor. Therefore, the fundamental tasks are to determine the value of RMS current through the DC link capacitor and the MOSFETs. Determining the root-mean-square (RMS) switch current requires the information of the modulation index and the phase current RMS value. The typical waveform of a switch current (looking like a chopped version of phase current) is shown in Fig. 6.15, which is nothing but the product of the respective phase current and its switching function. At a time instant '*t*' and instantaneous duty ratio of δ, let's consider a small time segment '*dt*', where the ON time will be given by $\delta(dt)/T$ and the instantaneous current will be $Isin(\omega t)$, where ω denotes the line frequency in rad/s ; $T=1/f_s$ denotes the switching cycle and f_s denotes the switching frequency. Therefore, the switch current RMS expression is obtained as follows.

$$I_{rms} = \sqrt{\frac{1}{T}\int_0^T I^2 \sin^2(\omega t)\delta(t)dt} = \sqrt{\frac{I^2 V_{pk}}{TV_{DC}}\int_0^T \sin^3(\omega t)dt} = I\sqrt{\frac{4V_{pk}}{3\pi V_O}} \tag{6.66}$$

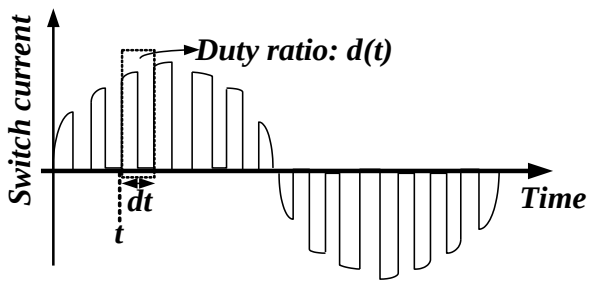


Fig. 6.15. Typical PFC switch current waveform

where, V_{pk} and I denote the phase-neutral peak voltage and phase RMS current, respectively. The next task is to determine the DC link capacitor current RMS value, which is required to calculate the equivalent series resistance (ESR) loss. The DC link capacitor current can be expressed as the sum of currents through all three top side MOSFETs, as presented in Eq. (6.67), where d_{AH}, d_{BH} and d_{CH} are the duty ratios of the three high-side MOSFETs for phases *A*, *B*, and *C*, respectively.

$$I_{DC} = d_{AH} i_A + d_{BH} i_B + d_{CH} i_C \tag{6.67}$$

where i_A, i_B and i_C are the currents through phase '*A*', '*B*' and '*C*', respectively; I_{DC} represents PFC output current i.e. sum of capacitor current and input current to the DC-DC stage. For a balanced three-phase AC system, the above relationship can be restructured as follows:

$$I_{DC} = (d_{AH} - d_{BH}) i_A + (d_{AH} - d_{CH}) i_C \tag{6.68}$$

The expression for the RMS value of I_{DC} can be calculated by taking the square of expression in Eq. (6.69), by applying $d_{iH}=V_{in}/V_{DC}$, $V_{in}= Vsin(\omega t)$, and substituting the RMS values of phase currents from Eq. (6.66).

$$I_{DC,RMS}{}^2 = \frac{21 I^2 V^2}{8 V_O{}^2} \tag{6.69}$$

Therefore, $I_{DC,RMS} = \frac{IV}{V_O}\sqrt{\frac{21}{8}}$ (6.70)

Therefore, the total conduction loss in the PFC stage is given by,

$$P_{Cond,PFC} = P_{Switch} + P_{ind} + P_{ESR,PFC}$$
$$= 6{I_{rms}}^2 R_{DS,PFC} + 3{I_{in,RMS}}^2 r_L + {I_{DC,RMS}}^2 r_C = \frac{16}{9\pi}\left(\frac{P^2 R_{DS,PFC}}{V_{DC}V_{pk}}\right) + \frac{2P^2 r_L}{3{V_{pk}}^2} + \frac{7P^2 r_C}{12{V_{pk}}^2} \quad (6.71)$$

where, the input phase current RMS is replaced by $P/3V_{in,RMS}$ and V_{pk} represents peak-to-peak input voltage. The equivalent DC resistances of each boost inductor and DC capacitor are denoted by r_L and r_C, respectively. Defining the modulation index as $M = 1.5V_{pk}/V_{DC}$, the overall conduction loss expression from Eq. (6.71) can be restructured as follows.

$$P_{Cond,PFC} = \frac{P^2}{{V_{pk}}^2}\left(\frac{32M}{27\pi}R_{DS,PFC} + \frac{2r_L}{3} + \frac{7r_C}{12}\right) \quad (6.72)$$

where, $R_{DS,PFC}$ denotes the on-state resistance of PFC MOSFETs. It is also important to include the losses incurred in the MOSFET body capacitances (C_{OSS}) arising due to hard switching. Since the blocking voltage of each PFC MOSFET is the DC link voltage V_{DC}, the body capacitance loss can be expressed as follows:

$$P_{body} = 6C_{OSS}V_{DC}^2 f_s \quad (6.73)$$

Thus, the expression for the PFC stage switching losses is given by,

$$P_{sw,PFC} = 6\frac{I_{RMS}V_{DC}f_s t_{tr}}{2} + 6C_{OSS}V_{DC}^2 f_s = Pf_s t_{tr}\sqrt{\frac{8V_{DC}}{3\pi V_{pk}}} + 6C_{OSS}V_{DC}^2 f_s \quad (6.74)$$

where, f_s denotes the switching frequency, t_{tr} represents the sum of turn-on and turn-off durations of the used device and P denotes the total output power.

II. Loss analyses in the DC-DC PSFB stage:

It is important to revisit the switching waveforms of the converter prior to the loss analysis. Fig. 6.16 provides the switching waveforms of the PSFB converter and the detailed modes of operation can be referred to the existing literature [75, 117, 119].

The losses in the PSFB DC-DC stage comprises of the turn-off and conduction losses in the primary side MOSFETs, conduction losses on the secondary MOSFETs and the secondary inductor, core loss and winding loss in the high-frequency transformer. Therefore, determining an accurate expression for the RMS currents through secondary inductor, secondary MOSFETs is fundamentally very important for loss modeling.

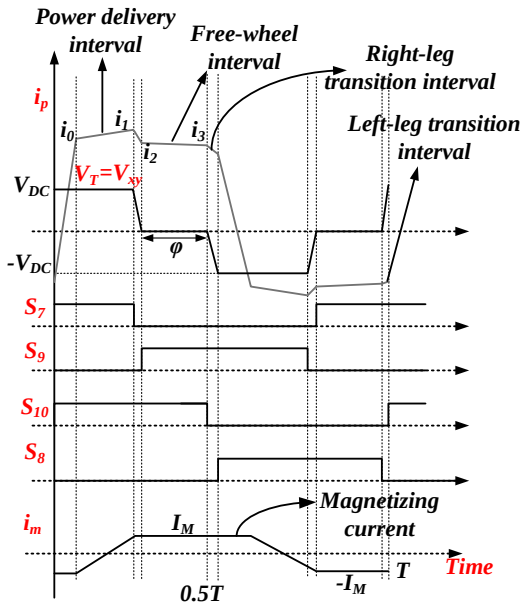


Fig. 6. 16. Typical waveforms of primary voltage, primary current and the gate pulses in a PSFB converter.

Secondary side losses:

(1) Conduction loss:

The typical waveform of the secondary inductor current is shown in Fig. 6.17, which is triangular with twice switching frequency as fundamental component. The secondary inductor varies with a slope of $(V_{DC}/n - V_O)/L_s$ and discharges with a falling slope of $-V_O/L_s$. Therefore, the following equations can be formed, assuming $x=\varphi T/2\pi$, where φ denotes the phase difference between the switching signals of S_5 and S_8. By calculating the voltage gain of the converter, φ turns out as follows: $\varphi=(1-nV_O/V_{DC})$

$$\alpha + \frac{V_{DC}/n - V_O}{L_s} x = \beta \tag{6.75}$$

The average inductor current can be calculated through the area under the inductor current curve over half switching cycle, which is calculated as $\langle i_s \rangle = (\alpha+\beta)/2$. Therefore, the following relationship can be established from power balance, considering zero average current though the output capacitor.

$$(\alpha + \beta) = \frac{2P}{V_O} \Rightarrow \alpha = \frac{P}{V_O} - \frac{V_{DC} - nV_O}{2nL_s} x \tag{6.76}$$

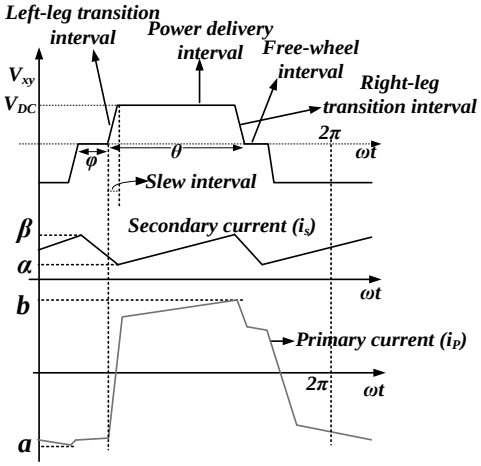


Fig. 6. 17. Typical waveforms of primary and secondary currents

The RMS current expression of the secondary inductor current is framed by adding the squares of two separate piecewise continuous linear segments, as shown in Eq. (6.77).

$$i_{s,RMS}{}^2 = \frac{1}{T}[\int_0^x (\alpha + \frac{\beta-\alpha}{x}t)^2 dt + \int_x^{T/2} (\beta - \frac{\beta-\alpha}{T/2 - x}t)^2 dt]$$
$$\Rightarrow i_{s,RMS} = \sqrt{[(\alpha^2 - \beta^2)\frac{\varphi}{\pi} + \beta^2 + \frac{V_{DC}}{nL_s}(1-\frac{\varphi}{\pi})(\frac{2\varphi}{\pi} - 1) + \frac{V_{DC}{}^2(1-\frac{\varphi}{\pi})^2}{3n^2 L_s{}^2}]} \quad (6.77)$$

As can be seen from the above relation, secondary RMS current is a function of the intermediate DC link voltage, the output load power and the phase shift amount. In order to calculate the conduction loss in the secondary side switches, it is required to establish the expression for switch RMS current. During the power transfer interval, the switch current is same as the inductor current and during the zero interval, the switch current is half of the inductor current after assuming the ON-resistances to be same for both the secondary side devices. Therefore, the RMS of secondary switch current ($i_{sec,RMS}$) is given as follows:

$$i_{\text{sec},RMS}{}^2 = \frac{1}{T}[i_{s,RMS}{}^2 x + \frac{i_{s\,RMS}{}^2}{2}(\frac{T}{2} - x)] = i_{sRMS}{}^2(\frac{1}{4} + \frac{x}{2T})$$
$$\Rightarrow i_{\text{sec},RMS} = i_{s,RMS}\sqrt{(\frac{1}{4} + \frac{\varphi}{4\pi})} \quad (6.78)$$

The above expression implies that the secondary current RMS increases with high phase shift angle i.e. more duration of power transfer interval in a switching cycle. In order to reduce the conduction losses in the switches in the high-current secondary side, multiple switches are placed in parallel to reduce the effective on-state resistance.

Therefore, the combined conduction losses incurred in the secondary transformer winding, the output inductor and synchronous rectification (SR) MOSFETs can be expressed as follows.

$$P_{SR} + P_{trans,sec} + P_{cond,Ls} = i_{s,RMS}^2(r_L' + r_T') + i_{sec,RMS}^2 R_{DS}' \quad (6.79)$$

where, r_L', r_T'represent the DC resistances of the output inductor and secondary winding; R_{DS}'represents secondary side SR on-state resistance. Based on the specifications of used Litz wire on the secondary windings of the transformer and inductor, DC resistances are calculated as 1.6 mΩ and 0.9 mΩ, respectively. Also, the calculated skin depth at 100 kHz switching frequency is more than the diameter of each strand (AWG-40) of the Litz wire. Therefore, the AC loss arising due to skin effect can be ignored for both transformer and inductor in this design.

For calculating the ESR loss in the output capacitor, the RMS current through output capacitor needs to be determined. The output capacitor current is the difference between the output inductor current (i_s) and load current (P/V_O), which is a zero-mean bipolar triangular current with peak values of $\pm\frac{V_{DC}-nV_O}{2nL_S}x$, obtained from Eq. (6.75) and Eq. (6.76). This yields to an RMS value of $\frac{V_{DC}-nV_O}{nL_S}x\sqrt{3}$. Therefore, the ESR loss is expressed as follows.

$$P_{ESR,PSFB} = \frac{3r_C'(V_{DC}-nV_O)^2x^2}{n^2L_S^2} \tag{6.80}$$

where, r_C' denotes the ESR of the output capacitor.

(2) Switching loss:

One important point to note is that the secondary SR MOSFETs achieve ZVS, as their anti-parallel body diodes conduct first and then, by sensing the small positive voltage drop across source-drain, the SR gate pulses are generated. However, the turn-offs of the SR MOSFETs are hard-switching, which results in a total turn-off loss $P_{sw,sec}$ for two switches, expressed as follows.

$$P_{sw,sec} = \left(V_O + {}^{V_{DC}}/_{n}\right) i_{sec,RMS} t_{s,off} f_s \tag{6.81}$$

(3) Snubber loss:

The designed PSFB stage does have snubber circuit on the secondary side to suppress the voltage spike across the MOSFET, caused by secondary side transformer leakage inductance. The snubber loss can be estimated as the leakage inductor energy loss per switching cycle. Maximum leakage energy stored can be $0.5L_{lks}I_{sp}^2$, where L_{lks} is the secondary leakage inductance and I_{sp} is the peak of the secondary current, which is β in the waveform shown in Fig. 6.17. From short circuit and open-circuit tests, the secondary side leakage is estimated as 100 nH.

$$P_{snubber} = 0.5L_{lks}\beta^2 f_s \tag{6.82}$$

Primary side losses:

(1) Conduction loss:

The conduction loss in the primary side switches depend on the RMS primary current, which can be determined from the cumulative sum of squares of piecewise continuous line-segment equations over a switching cycle. The typical primary current waveform is shown in Fig. 6.17, which consists of four line-segments i.e. two for power transfer interval and two for zero interval. Let's assume the valley and peak of the primary inductor current are given by 'a' and 'b', respectively.

$$a + \frac{V_{DC} - nV_O}{L_p} x = b \tag{6.83}$$

From the ideal power balancing condition, the input power from the input DC link of the PSFB stage is assumed equal to the load power, which leads to the following condition.

$$V_{DC} < i_{in} >= P \tag{6.84}$$

Where, $< i_{in} >= \frac{1}{T}[aT + \frac{(b-a)T}{2}] = \frac{a+b}{2}$ (6.85)

Substituting 'b' in terms of 'a', we get the followings.

$$a = \frac{P}{V_{DC}} - \frac{T}{4L_p}[nV_O(1-\frac{\varphi}{\pi})] \quad (6.86)$$

$$b = \frac{P}{V_{DC}} + \frac{T}{4L_p}[nV_O(1-\frac{\varphi}{\pi})] \quad (6.87)$$

Therefore, the primary switch current RMS is obtained as follows.

$$i_{pri,RMS}{}^2 = \frac{1}{T}[\int_0^x (a + \frac{b-a}{x}t)^2 dt + b^2(\frac{T}{2} - x)] = \frac{\varphi}{2\pi}[\frac{a^2 + ab - 2b^2}{3}] + \frac{b^2}{2} \quad (6.88)$$

In order to calculate the primary side conduction loss in transformer, the inductor current RMS value is required. It is important to mention that any switch current is same as inductor current during one power transfer interval and one zero interval. For the other half of switching cycle, the same switch current remains at zero. Hence, RMS of i_p is $\sqrt{2}$ times RMS of any switch current i.e. $i_{p,RMS}=\sqrt{2}\, i_{pri,RMS}$.

According to the nature of Eq. (6.88), PSFB primary current RMS increases monotonically with output power at a fixed DC link voltage and decreases monotonically with intermediate DC link voltage at a fixed load. The overall primary side conduction loss in the four switches and primary transformer winding is given as follows.

$$P_{cond,pri} = (4R_{DS} + 2r_T)\{\frac{\varphi}{2\pi}[\frac{a^2 + ab - 2b^2}{3}] + \frac{b^2}{2}\} \quad (6.89)$$

where, r_T and R_{DS} are the primary winding resistance and on-state resistance of primary MOSFETs, respectively.

(2) Switching loss:

PSFB primary side switching loss is the combined turn-off losses in the four MOSFETs, as all the MOSFETs achieve ZVS above ~30W load power, which is proved later in this section. The switching loss expression is formulated as follows.

$$P_{sw,pri} = 2V_{DC}\sqrt{\frac{\varphi}{2\pi}[\frac{a^2+ab-2b^2}{3}]+\frac{b^2}{2}t_{off}\ f_s} \tag{6.90}$$

where, t_{off} denote the turn-off time of the primary MOSFETs.

It is important to establish the conditions for ZVS in the primary side MOSFETs of the PSFB converter. Typically it is relatively more challenging to achieve ZVS in the lagging leg switches (S_8 and S_{10}), as the inductive energy is relative less for the right leg transition in comparison to left leg transition [116]. As can be seen from Fig. 6.17, the inductor current magnitude in right leg transition is less than that in left-leg transition. Therefore, in order to achieve ZVS for the lagging leg switches, the stored inductive energy must be greater than the stored capacitive energy in the MOSFET body capacitor, which is expressed as follows:

$$\frac{1}{2}L_p i_3^2 \geq C_{OSS}V_{DC}^2 \tag{6.91}$$

The load current can be calculated as the difference between reflected secondary peak current and half ripple current on the secondary side, which is formulated as follows.

$$i_{load} = (i_1 - i_m)n - 0.5i_{ripple} \tag{6.92}$$

Where $i_m = \frac{1}{2}\frac{V_{DC}(0.5T_s D_{eff})}{L_m}$ is the peak magnetizing current, D_{eff} is the effective duty cycle and I_{ripple} is the peak-to-peak ripple current of the output filter. From the Fig. 6.17, $D_{eff}=(0.5-\varphi/2\pi)$ holds. Furthermore, the following expression can be written using Fig. 6.17, where V_T denotes the primary side transformer voltage during the free-wheeling operation.

$$i_3 = i_2 - \frac{V_T}{L_p}\left(1 - D_{eff}\right)T_s = i_1 - \Delta I - \frac{V_T}{L_p}\left(1 - D_{eff}\right)T_s \quad (6.93)$$

where ΔI is the decay in primary current during the dead-time interval, which can be expressed as follows using the time-domain equations of primary current, given in [116].

$$\Delta I = \frac{V_{DC} - nV_O}{Z}\cos(\omega t_{dead}) \quad (6.94)$$

where $Z = \sqrt{\frac{L_p}{C_{OSS}}}$ is the equivalent characteristic impedance and t_{dead} is the set deadtime, which is 500 ns in this design.

V_T is the sum of voltage drops across the primary side conducting devices in the free-wheeling interval and V_T is assumed to be zero for the simplicity of analysis.

Therefore, combining Eq. (6.91)- Eq. (6.94), the ZVS condition is formulated as follows.

$$\frac{1}{2}L_p\left[\frac{i_{load} + 0.5(\beta - \alpha)}{n} + \frac{V_{DC}T_s D_{eff}}{L_m} - \Delta I\right]^2 \geq C_{OSS}V_{DC}^2 \quad (6.95)$$

which is further simplified to Eq. (31), by substituting (β-α) from Eq. (10) and $D_{eff} = 0.5 - \frac{\varphi}{2\pi}$; $\varphi = \pi(1 - \frac{nV_O}{V_{DC}})$.

$$i_{load} \geq nV_{DC}\left[\sqrt{\frac{2C_{OSS}}{L_p}} - \frac{T_s nV_O}{2V_{DC}L_m}\right] + n\frac{V_{DC} - nV_O}{Z}\cos(\omega t_{dead}) - \frac{T_s(V_{DC} - nV_O)^2}{4nL_s V_{DC}} \quad (6.96)$$

Using the converter specifications listed in Table 6.3, the required minimum load power (i.e. 28V ×i_{load}) for the fulfilment of ZVS is plotted against V_{DC} in Fig. 6.18.

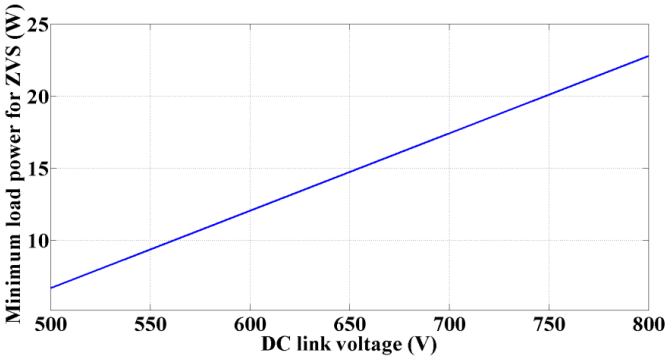


Fig. 6. 18. Minimum load power for ZVS with varying DC link voltage

Other losses include gating loss in the PFC and PSFB MOSFETs, expressed as $P_{Gate} = Q_g f_s V_{DD}$, where Q_g and V_{DD} are the gate charge of the MOSFET and gate driver supply voltage, respectively. Utilizing CMF10120D (with 47.1 nC gate charge) as the power MOSFETs for PFC and primary DC-DC side and using gate driver supply voltage of 15V, the net gating losses are calculated as 0.7W at 100kHz switching frequency. This loss remains unchanged regardless of any variations in intermediate DC link voltage. Therefore, optimum V_{DC} calculation process is independent of the gating losses.

(3) Core losses in transformer and output inductor:

Furthermore, one major part of the total losses comes from the core loss due to high frequency switching in the transformer as well as secondary filter inductor. Traditionally, the field intensity *H* of a magnetic core in a power converter is calculated using the inductance value at the RMS current level. The magnetic flux density *B* and the effective flux Φ can be obtained using the empirical relation between relative permeability (μ) and *H*. The magnetic core loss is a function of ΔB i.e. change in flux density over a switching cycle, which is again a function of ΔH that can be determined from two current values i.e. maximum and minimum current levels over a switching

cycle. An empirical formula of the core loss as a function of the switching frequency and magnetic flux density can be given as follows.

$$P_{core} = Kf_s^{\alpha} B_m^{\beta} \tag{6.97}$$

where K, α, β are called Steinmetz parameters, which are usually provided by the manufacturers or can be found by curve fitting. The change in magnetic flux density is an empirical function of change in magnetization intensity (H) i.e. ΔB=g(ΔH), which depends on the current ripple. At any instant, the magnetization intensity (H) is expressed as $H=NI/L_e$, where N, L_e and I denote the number of turns, mean flux length and current, respectively. Therefore, ΔH for the transformer in a switching cycle becomes as follows: $\Delta H=NV_{DC}x/L_mL_e$, where L_m denotes the magnetizing inductance of the core. ΔH for the secondary inductor in a switching cycle becomes as follows: $\Delta H=N(V_{DC}/n - V_O)x/L_SL_e$, where L_S denotes the secondary filter inductance. Using the B-H characteristics from the datasheet of 3C94 magnetic material (used for both transformer and secondary inductor), the sum of transformer and inductor core losses can be structured as the following.

$$P_{core} = Kf_s^{\alpha}[(\frac{NV_{DC}x}{L_mL_e})^{\beta} + (\frac{N(V_{DC}/n - V_O)x}{L_SL_e})^{\beta}] \tag{6.98}$$

For 3C94 material, the core loss in the transformer and inductor is proportional to the square of flux density change in a switching cycle and also proportional to the switching frequency. Therefore, the total magnetic core loss can be formulated as follows.

$$P_{core} = Kf_s[(\frac{NV_{DC}x}{L_mL_e})^2 + (\frac{N(V_{DC}/n - V_O)x}{L_SL_e})^2] \tag{6.99}$$

6.2.2. Net power losses in the integrated AC-DC stage:

Combining the losses in both the PFC and PSFB stages, the overall loss expression stands out as follows, which is a function of intermediate DC link voltage, the switching frequencies of AC-DC and DC-DC stages and the output load power. It is easier to analyze the loss dependence on V_{DC} if the loss terms are organized in different exponents of V_{DC}. Thus, the PFC losses can be formulated as follows.

$$P_{PFC} = K_0 + \frac{K_1}{V_{DC}} + K_2\sqrt{V_{DC}} + K_3 V_{DC}^2 \tag{6.100}$$

Where,

$$K_0 = \frac{P^2}{V_{pk}^2}\left(\frac{2r_L}{3} + \frac{7r_C}{12}\right) \tag{6.101}$$

$$K_1 = \frac{P^2}{V_{pk}V_{DC}}\frac{48}{27\pi}R_{DS,PFC} \tag{6.102}$$

$$K_2 = Pf_S t_{tr}\sqrt{\frac{8}{3\pi V_{pk}}} \tag{6.103}$$

$$K_3 = 6C_{OSS}f_s \tag{6.104}$$

Different categories of PSFB losses are summed up and thus, the following V_{DC}-dependent loss equation can be formulated.

$$P_{PSFB} = \frac{K_4}{V_{DC}^3} + \frac{K_5}{V_{DC}^2} + \frac{K_6}{V_{DC}} + K_7 + K_8 V_{DC} + K_9 V_{DC}^2 +$$

$$0.5t_{off}f_s\sqrt{\frac{1}{4R_{DS}+r_T+r_L}\left[\frac{K_{11}}{V_{DC}} + K_{12} + K_{13}V_{DC} + K_{14}V_{DC}^2\right]} \tag{6.105}$$

where, $K_{11} = (4R_{DS} + r_T + r_L)\left[\frac{n^3V_O^3T}{4L_p}\left(P - \frac{n^2V_O^2T}{12L_p}\right)\right]$ (6.106)

$$K_{12} = (4R_{DS} + r_T + r_L)\left[\frac{7n^4V_O^2T^2}{96L_p^2} - \frac{3n^2V_O^2T}{4L_p} + \frac{P^2}{2}\right] \tag{6.107}$$

$$K_{13} = (4R_{DS} + r_T + r_L)[\frac{nV_O PT}{L_p} - \frac{n^3 V_O^3 T^2}{12L_p^2}] \quad (6.108)$$

$$K_{14} = (4R_{DS} + r_T + r_L)\frac{n^2 V_O^2 T^2}{32L_p^2} \quad (6.109)$$

$$K_4 = K_{11} + \frac{n^3 V_O^3 T R_{DS}'}{2L_s}(P + \frac{V_O^2 T}{L_s}) \quad (6.110)$$

$$K_5 = K_{12} + \frac{n^3 V_O^3 T(0.5R_{DS}' + r_L' + r_T')}{2L_s}\left(P + \frac{V_O^2 T}{L_s}\right) + \frac{nV_O R_{DS}'}{2}(1.5\frac{nV_O TP}{L_s} - \frac{nV_O TP}{R_{DS}' L_s}) \quad (6.111)$$

$$K_6 = K_{13} + K_5 + \frac{nV_O R_{DS}'}{2}(\frac{P^2}{V_O^2} + \frac{V_O^2 T^2}{L_s^2}) \quad (6.112)$$

$$K_7 = K_{14} + (0.5R_{DS}' + r_L' + r_T')\left(\frac{P^2}{V_O^2} + \frac{V_O^2 T^2}{3L_s^2}\right) - \frac{V_O^2 R_{DS}' T^2}{3L_s^2} \quad (6.113)$$

$$K_8 = (0.5R_{DS}' + r_L' + r_T')\frac{-2V_O T^2}{3L_s^2} + \frac{V_O^2}{6nL_s^2} + \frac{6r_C' V_O f^2}{n^2 L_s^2} \quad (6.114)$$

$$K_9 = (0.5R_{DS}' + r_L' + r_T')\frac{-T^2}{3n^2 L_s^2} + \frac{Kf_s^2}{L_s L_e} + \frac{3r_C' f^2}{n^2 L_s^2} + \frac{n^2 K f_s^3}{L_m L_e} + \frac{L_{lks} f_s^3}{8n^2 L_s^2} \quad (6.115)$$

Therefore, the total loss in the integrated AC-DC stage as a function of V_{DC}, can be expressed as follows, where the coefficients K_1 to K_{14} are independent of V_{DC}, as established in Eq. (6.102-6.115).

$$P_{tot} = P_{PFC} + P_{PSFB} = \frac{a}{V_{DC}^3} + \frac{b}{V_{DC}^2} + \frac{c}{V_{DC}} + d + eV_{DC} + fV_{DC}^2 + g\sqrt{V_{DC}} + h\sqrt{\frac{K_{11}}{V_{DC}} + K_{12} + K_{13}V_{DC} + K_{14}V_{DC}^2} \quad (6.116)$$

In the above expression, $a=K_4$; $b=K_5$; $c=(K_6+K_1)$; $d=(K_0+K_7)$; $e=K_8$; $f=(K_3+K_9)$; $g=K_2$; $h=1/\sqrt{4(R_{DS,ON}+r_L+r_T)}$.

Therefore, total losses can be minimized with respect to either of the three variable parameters (DC link voltage and two stage switching frequencies) at each load power level, which is discussed in the Section III and Section IV. As can be seen in Eq.

(6.116), the overall loss expression contains several non-linear terms of V_{DC}, where the exponents can vary from -3 to +2, including fractional exponents. Therefore, to minimize the total loss with respect to varying DC link voltage is not a straightforward process, as at each instant the coefficients keep changing due to the variation of operating conditions. The detailed procedure of efficiency maximization with variable DC link voltage is explained in Section III. Furthermore, since the coefficients K_1 to K_{12} are function of DC-DC stage switching frequency, the loss minimization can be feasibly performed with the variation of V_{DC}, which is analyzed in Section IV.

6.2.3. Variable DC Link & Fixed Switching Frequency Control Methodology

Intermediate DC link voltage can be set as a variable parameter in order to minimize the total power loss at any load power demand, so that conversion efficiency can be maximized. Prior to introducing the proposed approach, it is to be mentioned that the variation of the intermediate DC link voltage is limited between a minimum (V_{min}) and maximum (V_{max}) limits, which are prefixed by the limitation of boost operation of the PFC stage and device ratings. The minimum DC link voltage has to be greater than the input line-line AC peak voltage and lesser than around 70% of the maximum switch stress rating. Therefore, V_{min} and V_{max} are set as 600V and 800V, respectively. It is important to note that the variation of total loss with change in DC link voltage at different load power levels will highly depend on the components & device specifications of the converter.

The state-of-the art and proposed algorithms to track the maximum efficiency using the loss minimization model are presented in the following subsections.

I. Intelligent numerical approaches and their trade-offs:

The key point to be considered is to finish the real time execution of algorithm to determine optimum DC link voltage within a sampling cycle, which is 10 μs in this design. Although different intelligent algorithms may be employed in determining the optimum V_{DC}, real-time implementation will definitely slow down the execution time and thus, will limit the upper bound of the switching frequency. The switching frequencies of both PFC and PSFB converter stages are fixed at 100 kHz based on the trade-offs between magnetics volume and efficiency. Therefore, the program loop execution of the complete control logic has to be finished by 10μs; otherwise, there will be under-sampling, potentially resulting in loop instability.

The major complicacy in the mathematical expression determining optimum DC link voltage is the existence of fractional order terms in the polynomial. Since it is not straightforward to determine the number of roots of a fractional order polynomial, research efforts [164] have concentrated more on the stability of a system with such characteristic polynomial, not on determining the solutions. One proposed approach in [164] is to convert the fractional order polynomial into an extended integer order polynomial by scaling up the exponents and then, different numerical optimization based solving algorithms can be applied to it. One of the intelligent algorithms for solving non-linear higher order equations is Levenberg-Marquardt Optimization [165-166], which is used by ‘fsolve’ command in MATLAB. This is termed as numerical approach. However, this algorithm involves gradient descent method requiring to perform inverse of a high rank matrix. Matrix inversion is a highly time expensive operation, which is not implementable to be executed real-time in a high sampling

frequency converter system. This method can be implemented offline to find out the optimum solutions at different loading conditions and may be realized in terms of a two-dimensional look-up table in DSP program. However, this method will significantly lose accuracy due to discretization in look-up table and also, will suffer from space / memory complexity in DSP implementation.

Due to the above listed reasons, one appropriate approach is to linearize the fractional order terms in polynomial and then, to apply method of bisection in searching for solutions, which is relatively simpler and real-time executable with an acceptable upper bound of efficiency errors.

II. Loss minimization model:

First, the intermediate DC link voltage level is to be located where the losses become minimum i.e. $\delta P_{tot}/\delta V_{DC}=0$. If the optimum DC link voltage remains in between V_{min} and V_{max}, it can be set as a reference to the voltage loop of three-phase boost PFC. Therefore, the immediate important task is to determine the expression for $\delta P_{tot}/\delta V_{DC}$. Since there are some terms with non-integral exponents present in the polynomial expression Eq. (51), the proposed method linearizes those fractional order terms around the operating point $V_{DC}=V_{DC}^*$, where V_{DC}^* is the sampled DC link voltage. This method is termed as "analytical" approach. However, the deviation of accuracy of V_{DC} solution due to the linearization approximation in analytical approach should be considered during the calculation process. For example, if '$\sqrt{x}$' is linearized with respect to $x=x_0$ using Taylor series expansion, the following is obtained.

$$\sqrt{x} \approx \sqrt{x_0} + \frac{(x-x_0)}{2\sqrt{x_0}} = \frac{(x+x_0)}{2\sqrt{x_0}} \tag{6.117}$$

Therefore,

$$\sqrt{\frac{K_{11}}{V_{DC}}+K_{12}+K_{13}V_{DC}+K_{14}V_{DC}^2}=\frac{K_{11}\left(\frac{1}{V_{DC}}+\frac{1}{V_{DC}^*}\right)+2K_{12}+K_{13}\left(V_{DC}+V_{DC}^*\right)+K_{14}\left(V_{DC}+V_{DC}^*\right)^2}{2\sqrt{\frac{K_{11}}{V_{DC}^*}+K_{12}+K_{13}V_{DC}^*+K_{14}{V_{DC}^*}^2}} \tag{6.118}$$

Hence, the linearized form of the overall loss expression in Eq. (6.116) can be expressed as follows.

$$P_{tot}=\frac{a}{V_{DC}^3}+\frac{b}{V_{DC}^2}+\frac{c'}{V_{DC}}+d'+e'V_{DC}+f'V_{DC} \tag{6.119}$$

where,

$$c'=c+\frac{K_{11}}{2\sqrt{\frac{K_{11}}{V_{DC}^*}+K_{12}+K_{13}V_{DC}^*+K_{14}{V_{DC}^*}^2}} \tag{6.120}$$

$$d'=d+\frac{\sqrt{V_{DC}^*}}{2}+K_{12}+\frac{\sqrt{\frac{K_{11}}{V_{DC}^*}+K_{12}+K_{13}V_{DC}^*+K_{14}{V_{DC}^*}^2}}{2} \tag{6.121}$$

$$e'=e+\frac{V_{DC}}{2\sqrt{V_{DC}^*}}+K_{12}+\frac{K_{13}+2K_{14}V_{DC}^*}{\sqrt{\frac{K_{11}}{V_{DC}^*}+K_{12}+K_{13}V_{DC}^*+K_{14}{V_{DC}^*}^2}} \tag{6.122}$$

$$f'=f+\frac{K_{14}}{2\sqrt{\frac{K_{11}}{V_{DC}^*}+K_{12}+K_{13}V_{DC}^*+K_{14}{V_{DC}^*}^2}} \tag{6.123}$$

After linearizing the fractional order terms in power loss expression, it is required to determine the infimum solutions of $\delta P_{tot}/\delta V_{DC}=0$, which leads to the following equation.

$$\frac{\partial P_{tot}}{\partial V_{DC}}=\frac{-3a}{{V_{DC}}^4}-\frac{2b}{{V_{DC}}^3}-\frac{c'}{{V_{DC}}^2}+e'+2f'V_{DC}=0 \tag{6.124}$$

Which implies the following polynomial of V_{DC}:

$$\psi(V_{DC})=2f'{V_{DC}}^5+e'{V_{DC}}^4-c'{V_{DC}}^2-2bV_{DC}-3a=0 \tag{6.125}$$

III. The proposed analytical approach to determine optimum solution:

The flowchart for determining the optimum V_{DC} solution in analytical approach is presented in Fig. 6.19. It becomes mathematically intensive to determine how many valid DC link voltage level exists between the allowable range of DC link voltage. If $\delta P_{tot}/\delta V_{DC}=0$ holds at multiple V_{DC} levels, the V_{DC} where P_{tot} is minimum is chosen. Let's assume there exists 'm' number of solutions of $V_{DC} > V_{min}$ satisfying $\delta P_{tot}/\delta V_{DC}=0$ and 'n' number of solutions of $V_{DC}>V_{max}$, satisfying $\delta P_{tot}/\delta V_{DC}=0$. This implies that there would be (m-n) number of V_{DC} solutions in the range of $[V_{min}, V_{max}]$, satisfying $\delta P_{tot}/\delta V_{DC}=0$. In order to find out the number of roots above V_{min}, a new variable '$q'=V_{DC}-V_{min}$ is introduced and V_{DC} in Eq. (6.125) is replaced by $q+V_{min}$ to obtain the modified relationship, Eq. (6.126). Similarly, another variable '$r' = V_{DC}-V_{max}$ is introduced and V_{DC} in Eq. (6.125) is replaced by $r+V_{max}$ to obtain the modified relationship, in Eq. (6.127). In the modified set of relationships, 'm' and 'n' are the number of positive roots of 'q' and 'r', respectively.

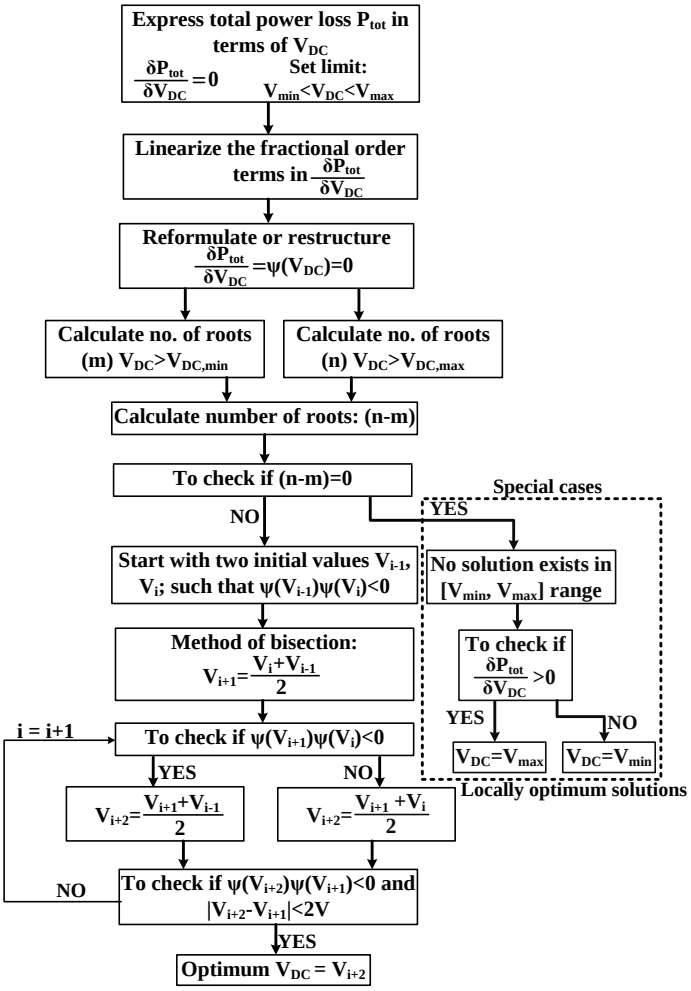


Fig. 6. 19. Flowchart of determining optimum V_{DC} by the proposed analytical method

$$\alpha_5 q^5 + \alpha_4 q^4 + \alpha_2 q^2 + \alpha_1 q + \alpha_0 = 0 \tag{6.126}$$

$$\beta_5 r^5 + \beta_4 r^4 + \beta_2 r^2 + \beta_1 r + \beta_0 = 0 \tag{6.127}$$

Where, α_0 to α_5 can be mathematically calculated in terms of a, b, c', e', f', V_{min} and β_0 to β_5 can be mathematically calculated in terms of a, b, c', e', f', V_{max}. Number of solutions of $V_{DC}>V_{min}$ i.e. q>0, can be determined from the number of sign changes on the coefficients in the first column of Routh-Hurwitz array. The array coefficients for the descending order of V_{DC} exponents are as follows:

$$coeff_1 = \alpha_5; coeff_2 = \alpha_4; coeff_3 = \frac{-\alpha_5\alpha_2}{\alpha_4}; \tag{6.128}$$

$$coeff_4 = \frac{-\alpha_5\alpha_2^{\,2} + \alpha_4(\alpha_5\alpha_0 - \alpha_4\alpha_1)}{\alpha_5\alpha_2} \tag{6.129}$$

It is important to note that all of these coefficients fundamentally depend on the operating conditions of the converter i.e. load power level, output voltage and input AC voltage levels. Under any variation of these parameters, the values of the coefficients may change, which may also alter the number of sign changes among these coefficients i.e. number of V_{DC} solutions less than V_{min}. Furthermore, after replacing all the 'α_i's by 'β_i's, the Routh-Hurwitz coefficients of Eq. (6.127) could be obtained and the number of sign changes among this set of coefficients will determine the number of V_{DC} solutions greater than V_{max} i.e. r>0. In addition, several conclusions can be drawn about the solutions of Eq. (6.126) and Eq. (6.127).

- The number of sign changes in the RH coefficients cannot be more than 3, which implies that the maximum number of roots satisfying $V_{DC}>V_{min}$ or $V_{DC}>V_{max}$ is 3.
- Therefore, the maximum number of roots lying between [V_{min}, V_{max}] satisfying $\delta P_{tot}/\delta V_{DC}=0$ is three.
- If the number of roots between [V_{min}, V_{max}] is even i.e. 2, $\psi(V_{max})$ and $\psi(V_{min})$ will be of same sign. Alternatively, if number of roots between [V_{min}, V_{max}] is odd i.e. 1 or 3, $\psi(V_{max})$ and $\psi(V_{min})$ will be of opposite signs.

In order to find the solutions (if exists) in [V_{min}, V_{max}], bisection method is applied. If $\psi(V_{max})$ and $\psi(V_{min})$ are of opposite signs, V_{min} and V_{max} are assigned as the initial iterations. Otherwise, a step of 10V is kept on reducing from V_{max} in each iteration until

any sign change is observed. After that, the new obtained V_{DC} point and V_{max} are assigned as two initial values to start with the algorithm.

At each step the method divides the interval in two by computing the midpoint $V_{i+1}= (V_{i-1}+V_i)/2$ of the interval and the value of the function ψ (V_{i+1}) at that point. Unless V_{i+1} is itself a root (which is very unlikely, but possible) there are now only two possibilities: either $\psi(V_{i-1})$ and $\psi(V_{i+1})$ have opposite signs and bracket a root, or $\psi(V_{i+1})$ and $\psi(V_i)$ have opposite signs and bracket a root. The method selects the subinterval that is guaranteed to be a bracket as the new interval to be used in the next step. In this way an interval that contains a zero of $\psi(V_{DC})$ is reduced in width by 50% at each step. The process is continued until the interval is sufficiently small (selected as 2V in our method).

The method is guaranteed to converge to a root of $\psi(V_{DC})$, if ψ is a continuous function on the interval $[V_{min}, V_{max}]$ and $\psi(V_{i-1})$ and $\psi(V_i)$ have opposite signs. The number of iterations needed, n, to achieve a given error (or tolerance), ε, is given by: $n=\log_2\{(V_{max}-V_{min})/\varepsilon\}$. Under a selection of 2V tolerance band, the maximum number of iteration to find a solution is $\log_2(800-600) \sim 8$.

Consequently, the values of the power losses at all the V_{DC} solutions in $[V_{min}, V_{max}]$ are computed using Eq. (60) and the V_{DC} corresponding to the minimum power loss is set as a reference voltage level for the PFC DC link voltage controller.

IV. Special cases:

As a special case, if at any instant, no solutions of V_{DC} exists between $[V_{min}, V_{max}]$ and $\delta P_{tot}/\delta V_{DC}<0$, the DC link voltage reference of the PFC stage is set at $V_{DC}^*=V_{max}$. This is because $\delta P_{tot}/\delta V_{DC}<0$ implies that increasing the V_{DC} level will help reduce the total

power losses. On the other hand, under the case of no V_{DC} solution in [V_{min}, V_{max}], if $\delta P_{tot}/\delta V_{DC}>0$ holds, PFC DC link voltage reference is set as V_{min}, as lowering the DC voltage level will reduce the power loss. Special cases arise when the PFC DC link voltage is held at either V_{max} or V_{min}.

Case-1: If at any instant $V_{DC}=V_{max}$ & $\delta P_{tot}/\delta V_{DC}<0$ & no solution exists in the interval [V_{min}, V_{max}], the PFC DC link reference is maintained to be held at V_{max}.

Case-2: Similarly, if at any instant $V_{DC}=V_{min}$ & $\delta P_{tot}/\delta V_{DC}>0$ & no solution exists in the interval [V_{min}, V_{max}], the PFC DC link reference is maintained to be held at V_{min}.

Case-3: If at any instant $V_{DC}=V_{max}$ & $\delta P_{tot}/\delta V_{DC}>0$ & no solution exists in the interval [V_{min}, V_{max}], the PFC DC link reference is maintained to be held at V_{min}.

Case-4: If at any instant $V_{DC}=V_{min}$ & $\delta P_{tot}/\delta V_{DC}<0$ & no solution exists in the interval [V_{min}, V_{max}], the PFC DC link reference is maintained to be held at V_{max}.

If V_{DC} is held at V_{min} or V_{max}, and solution(s) belonging to [V_{min}, V_{max}] exist for $\delta P_{tot}/\delta V_{DC}=0$, the solutions corresponding to the minimum power loss is set as a reference level for the PFC DC link voltage for the next sampling cycle.

V. Normalized loss variation versus intermediate DC link voltage:

Table 6.2 shows the optimum DC link voltages at different load power levels at 230V phase-neutral RMS AC voltage. The V_{DC} solutions in both the analytical methods (by linearizing the fractional order terms) and numerical approaches (with the original equations) are tabulated below, which shows an error within ±2%. Therefore, the analytical method of solving V_{DC} is digitally implemented due to its less computational complexity and faster execution. The loss of accuracy in optimum V_{DC} prediction

would lead to a change in efficiency less than 0.3%, which is sacrificed as a trade-off to the faster execution.

Table 6. 2. Optimum V_{DC} levels with varying load power levels

Load power (kW)	V_{DC}(analytical)	V_{DC} (numerical)	% change in efficiency
0.2	600V	600V	0
2	600V	600V	0
4	630V	612V	0.24
6	672V	665V	0.19
8	682V	673V	0.21
10	705V	689V	0.12

The variation of total power loss with change in intermediate DC bus voltage (V_{DC}) is plotted in MATLAB for different load power levels, as shown in Fig. 6.21. As can be seen, there is an increasing pattern of optimum V_{DC} with increasing load power. However, this does not imply that the V_{DC} can be fixed to its optimum value for maximum load, as the optimum V_{DC} for other load powers are different, as can be seen from Fig. 6.20. The optimum V_{DC} corresponds to the voltage level where the minimum valley of the normalized loss exists.

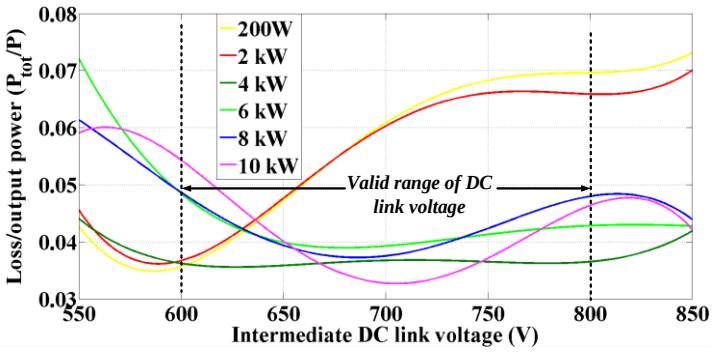


Fig. 6. 20. Total power loss variation with intermediate DC voltage levels a different load power

It is noted that the V_{DC} level (within he allowed range) at which the power loss is minimum keeps a good agreement with the analytically determined optimum solutions. It is worth mentioning that the variation of total power loss with change in intermediate DC bus voltage for 200W and 2kW loads show a different trend compared to other loads. This is because of the following reasons:

(i) at a relatively lighter load, the switching loss typically dominates conduction loss, as the input current and other branch currents are relatively small. Again, with a lower DC link voltage at lighter load, the switching loss will be less and hence, efficiency will be relatively better in comparison to a higher V_{DC}.

(ii) The conduction loss starts to dominate switching loss at higher range of load power, as the conduction loss varies with input current in quadratic fashion. At heavier load, efficiency would be more in case of a higher DC link voltage, as this will result in reduced conduction loss.

Therefore, in case of two low-end power levels i.e. 200W and 2 kW, normalized loss is less at 600V DC link voltage in comparison to 800V. However, in case of other higher power levels, conduction loss dominates at 600V in comparison to 800V DC link and hence, the normalized loss (shown in Fig. 6.21) is more in case of 600V, which follows the opposite trend compared to the lighter loads.

It is important to mention that the optimum V_{DC} is a function of the load power. As can be seen in the expression of total power loss in Eq. (51), the coefficients *a, b, c* and *d* are dependent variables of load power. Therefore, the load power must be estimated in each sampling / execution loop and will be accordingly updated in the proposed algorithm of determining optimum V_{DC}. The load power estimation method is

discussed in Section IV. Thus, the proposed algorithm works well even if the load power shuttles from its rated value i.e. 6kW to peak power i.e. 10kW.

VI. Response to any fault conditions:

It is important to mention that efficiency maximization algorithm is involved during the steady state operation of RTRU. In the program loop, a supervisory control is involved to monitor the values of all the sensed variables (three-phase voltages, phase currents, DC link voltage, output voltage, and load current) at each sampling instant and to check if they are in the allowable range for normal operation. Once any faults (short-circuit at the output, input phase failures, power interrupt, overcurrent, overvoltage) happen, it is the primary aim of the supervisory controller to detect the fault and thereby, clear all the MOSFET PWM signals to cut the power flow and hence, shut down the RTRU safely. During the fault duration, the intermediate DC link voltage falls down to 0 by first order RC discharge through bleeding resistor (~470kΩ in this design) across the PFC DC link capacitor. After the faults get cleared or RTRU resumes its safe steady operation, variable DC link based efficiency maximization algorithm is brought back into the control loop.

6.2.4. Control Algorithm Implementation

The major control objectives are to (i) maintain the final output voltage at a stable regulated value (ii) keep the input power factor above 0.995 and total harmonic distortion (THD) of the input current below 5% [74]. In the proposed control loop, shown in Fig. 6.21, for the integrated AC-DC converter, the sum of the outputs from the voltage controllers (PFC DC link and final DC voltage) imply the active power

reference. This is multiplied with three individual phase voltages to obtain the phase current references. Also, in variable DC link voltage control method, the intermediate DC link reference is calculated from the optimum V_{DC} generation logic. Under any variation of the intermediate DC link voltage due to any load change, the PSFB voltage controller manipulates the phase angle shift to maintain the final output voltage at a constant level.

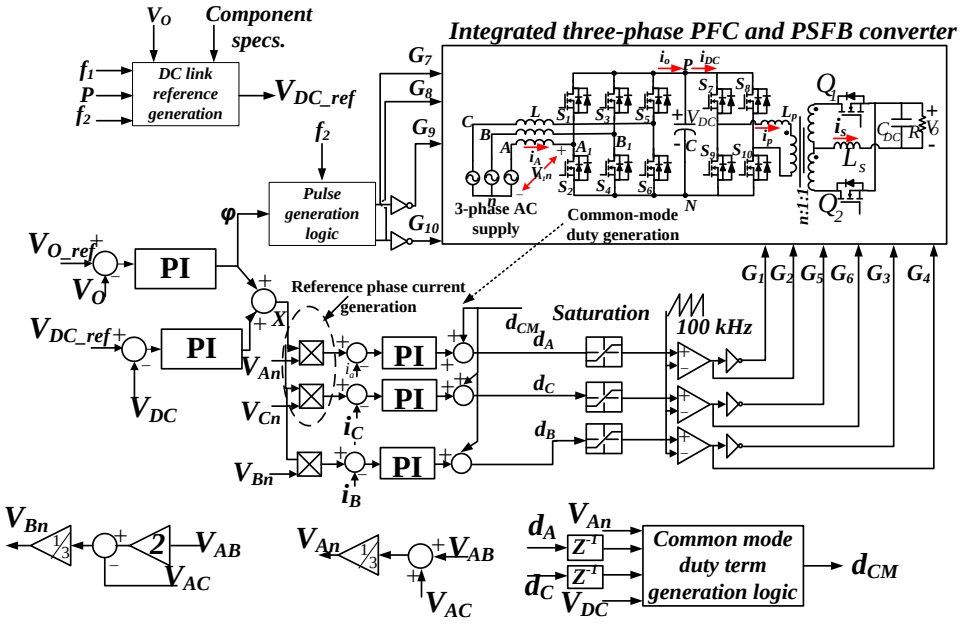


Fig. 6. 21. Variable DC link control method of an integrated two-staged AC-DC converter.

The proposed variable DC link voltage control is implemented in digital signal processor (DSP) TMS320F28335. The control algorithm includes two voltage mode PI controllers in discrete domain and three simultaneous current controllers. There prevails certain logic complexity in determining the optimal V solution (if exists) in the range [V_{min}, V_{max}]. Using the inherent processor configuration, conventional averaged current mode control with fixed V_{DC} takes 4μs for computing the program execution loop, where discrete domain implementation of three current loop PI

controllers consumes 60% of total execution time. On the other hand, variable DC link control logic execution takes 10 µs, where the computation of optimal V_{DC} solution consumes 70% of total execution time. Therefore, there should be a minimum time interval of 10 µs between two consecutive sets of samples of DC link voltage, assuming 100% CPU utilization in a single-core DSP. As a result, the effective switching frequency should be kept below the maximum sampling frequency, which is 100 kHz in this implementation technique.

Furthermore, since the optimum V_{DC} level is a function of the input AC conditions as well as load power level, it is a necessary requirement to estimate the output load at each sampling instant. For a balanced three phase system with open neutral point i.e. $V_{An}+V_{Bn}+V_{Cn}=0$ and $i_A+i_B+i_C=0$; the following relationship can be formulated.

$$V_{DC}{}^2 = R[i_A(V_{Bn} + 2V_{An}) + i_B(V_{An} + 2V_{Bn})] \tag{6.130}$$

As the sum of voltage loop PI outputs (X) corresponds to a proportional quantity to the active power of the converter [74], it could be assumed to be proportional to $V_{DC}{}^2/R$, which is directly proportional to $1/R$ for a constant output voltage assumption. From the control loop we have the followings.

$$i_A(n) = XV_{An}(n) \tag{6.131}$$

$$i_B(n) = XV_{Bn}(n) \tag{6.132}$$

where, $V_{An}(n)$ and $V_{Bn}(n)$ denote the phase-neutral voltages for phase 'A' and 'B', respectively at 'n'th sampling cycle. Plugging the phase currents from Eq. (6.131-6.132) into the power balancing relation Eq. (6.130), the estimated load resistance 'R_{est}' can be determined in terms of 'X'.

$$R_{est} = \frac{V_{DC}{}^2}{2X(V_{An}(n)^2+V_{Bn}(n)^2+V_{An}(n)V_{Bn}(n))} \tag{6.133}$$

6.2.5. Experimental Results

A set of experiments is conducted to (i) verify the closed loop stability of the integrated system (ii) check the efficiency variation with load power level with two different methods i.e. fixed DC link & fixed switching frequency, variable DC link & fixed switching frequency control. Therefore, a 6kW hardware prototype of integrated two-staged AC-DC converter is developed using the specifications of an auxiliary power unit in more-electric-aircraft (MEA) applications.

A list of key parameters of converter specification is provided in Table 6.3. As can be seen from the 6kW steady state PFC waveforms in Fig. 6.22, the power factor is maintained at unity and the intermediate DC link voltage is settled at 650V in the fixed DC link voltage control method. Both the PFC and DC-DC stages are switched at 100 kHz. As suggested by Fig. 6.23, the PSFB output voltage is well-regulated at 28V, with an average output current of ~214A. The input current waveform of the PFC stage (shown in Fig. 6.23) exhibits a power factor of 0.996 and THD of 4.3%.

Table 6. 3. Key design parameters and their specifications

Parameters	Values	Quantity
Input AC voltage (V_{in})	230V, 400Hz, 3-phase	-
Output voltage reference (V_o^*)	28V	-
Output power (P_{out})	6kW	-
Boost inductance	0.4mH	3
Intermediate DC capacitance	0.1mF	1
PFC MOSFETs	CMF10120D (SiC, 1.2kV)	6
Transformer turns ratio (n)	12:1:1	-
Primary leakage inductance (L_p') of DC-DC stage	8 µH	1

Magnetizing inductance (L_m)	800 µH	
Secondary inductor (L_s)	7.5 µH	1
DC link capacitor (C_{DC})	3 mF	1
Primary MOSFETs	SiC (1.2kV/24A)	4
Secondary MOSFETs	FDH055N15A (145A, 160V)	6
Switching frequency (f_s)	100 kHz	-

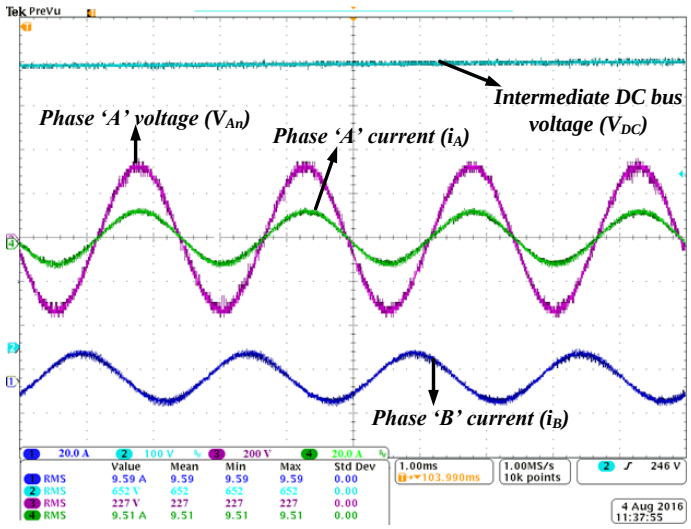


Fig. 6. 22. 6kW PFC stage waveforms (at 230V 400Hz AC input)

In order to illustrate the effectiveness of the variable DC link method, a step-change in load from 6kW to 4kW is performed and as shown in the experimental result in Fig. 6.24, the DC link voltage settles down near the numerically calculated optimum level (~612V) after the transient. The PSFB output voltage settles to 28V at the steady state. The calculated input current THD before and after the transient are 4.3% and 4.8%, respectively. Furthermore, to maintain the same output voltage with a different DC link voltage, the phase-shift angle is manipulated by the PSFB controller, as can be understood from the output voltage dynamics. The measured efficiency of the integrated stage is 97.2%. It is noteworthy that the experimentally obtained DC link

voltages of 665V and 673V at 6kW and 8kW power levels, respectively match well with the theoretically predicted optimum voltage levels (672V and 682V, respectively), shown in Table 6.2.

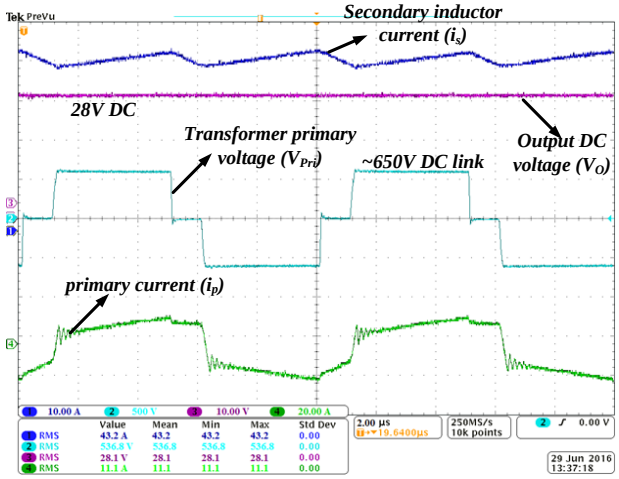


Fig. 6. 23. 6kW PSFB stage waveforms

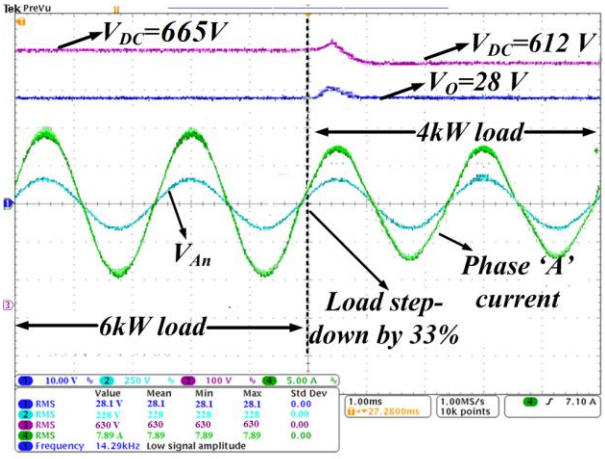


Fig. 6. 24. A load transient from 6kW to 4kW in the integrated RTRU, demonstrating the change in intermediate DC link voltage from 665V to 612V

Furthermore, a set of values of the conversion efficiencies is obtained from experimenting the integrated AC-DC converter at different load power levels using both fixed & variable DC link control methods and is shown in Fig. 6.25. The variable DC link control exhibits a steady state efficiency of 97% at the rated load with a light

load efficiency of 93.5%, whereas the rated and light load efficiencies are 95.1% and 91.8%, respectively in fixed DC link control.

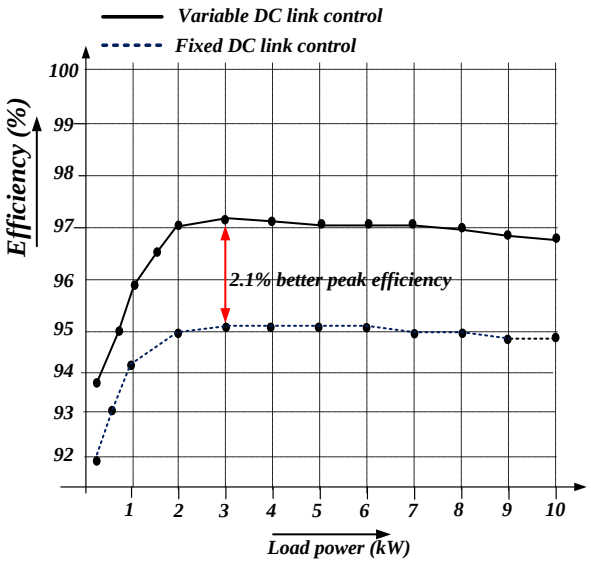


Fig. 6.25. Efficiency comparison between fixed DC link and variable DC link control

6.3 Summary

In this chapter, a new control methodology, incorporating reduced-state observer-based state-feedback control for a cascaded three-phase PFC and PSFB DC-DC converter is proposed and implemented. Its main objective is to ensure stability and achieve unity power factor at wide range of power levels upto 8kW. The reduced state observer design reduces the total sensor counts by three, as opposed to the seven required measurements in the conventional control with PI compensator. As a proof-of-concept verification, a 6kW laboratory prototype is designed and tested with 230V, three-phase, 400Hz AC to 28V DC conversion specification at 6kW for the application of auxiliary power supply in a more-electric-aircraft. According to the experimental results, a maximum conversion efficiency of 95.4%, THD of 4.1%, a PF of 0.998 and an output voltage ripple below ±1% are achieved at the steady state. In addition, during

33% overload condition, the converter demonstrates fast dynamics with only 100μs settling time and maintaining unity PF. Furthermore, the experimental results exhibit an improvement in power factor from 0.966 (PI control) to 0.998 in state-feedback control.

Also, in this chapter, a variable DC link voltage control method is introduced and analyzed in order to maximize the conversion efficiency of an integrated two-staged AC-DC converter. According to the experimental results, the steady state efficiency of the integrated stage becomes 95.2% with the conventional fixed DC link control, whereas it is improved to 97.2% by the implementation of variable DC link control method. Furthermore, during 50% step-up in load power, the converter exhibits a change in DC link voltage from 650V to 680V for loss minimization, which closely matches with the theoretical calculation.

Chapter 7: Intermediate DC Link Capacitor Reduction in RTRU

Avionic vehicular systems should be strictly of less weight and high level of compactness. Conventionally, in order to smoothen the DC link voltage, bulky electrolytic capacitors or even bulkier film capacitors (for improved reliability) have been utilized in the three-phase rectifiers or any cascaded power unit or inverter-based systems (e.g. aerospace, traction drive applications). In the case of a single-phase AC system, the DC link capacitance value mainly depends on the amount of second harmonic reactive power, delivered by the source. This is because the input power is $P_{in}= VIsin^2\theta=0.5VI\ (1-cos2\theta)$, which has an alternating amplitude of $0.5VI$. Therefore, there will be a high spectrum peak at the twice harmonic of source frequency in the Fast Fourier transform (FFT) of DC link current / voltage, which will require a bulky DC capacitor to limit the voltage ripple. On the other hand, in case of a three-phase system, the amount of second or lower order harmonics transferred to the load is almost zero under unity PFC operation. However, volume and weight of the intermediate DC link capacitors due to attenuating switching frequency ripple become a serious concern for the power-density-critical applications [167]. Furthermore, since the capacitor is one of the most vulnerable components in a power circuit, it is undoubtedly desirable to reduce the DC link capacitance value for enhancing the reliability and improving the overall power density of the converter.

Various research works [168-179] has been carried out on the DC link capacitor reduction in a three-phase rectifier / inverter-based system. A common approach is to

inject harmonic currents to nullify the alternating portion of the input power. In [168], the researchers have proposed a method of injecting an additional term to the duty ratio expression, which in turn injects third order harmonic current and reduces the DC link stress. However, this method degrades the input power quality by increasing THD. Since the DC link capacitor current of a three-phase PFC consists of switching frequency and its multiple orders, whereas the single-phase PFC DC link capacitor contains a significant amount of twice grid frequency component. In this regard, several methods [169-171] are proposed in order to achieve a DC link ripple current reduction. The work in [169] proposes a DC link ripple reduction method for paralleled three-phase voltage source converters (VSC) with interleaving. With a proper optimization of interleaving phase angle between switching states of the two parallel VSCs, the current ripple RMS can be minimized to 35%. Furthermore, a control method is proposed in [170] to reduce the DC link capacitor ripple current in a back-to-back three-phase converter. The objective of this method is to create 180^{o} phase difference between the switching frequency components of output current of rectifier and input current of inverter stage, which is achieved by a phase-modulated PWM method, introduced in [170]. However, this method is applicable only in multiple three-phase units connected in series or parallel combination. A method describing switching frequency component reduction of DC link capacitor in a single-phase AC-DC two-stage topology is introduced in [171]. The study shows that implementation of different PWM methods (triangular, sawtooth, reverse-sawtooth) in AC-DC and DC-DC stages have effects on the capacitor ripple current amount, which is reduced upto 38% by using the proposed approach in [171].

Furthermore, the method discussed in [172] proposes including a filter in the output voltage sensing path and compensating the second and other lower order harmonics. Although the output capacitor ripple amount can be minimized in this method, the input currents get distorted and displacement power factor deviates from unity. In addition, researchers [172-174] proposed an active method for reducing DC link current ripple by introducing an additional switching leg with one pair of switches, connected to a LC combination. The reactive energy is partially circulated in this LC combination instead of its full transfer to the output DC capacitor. Although the DC link capacitor is reduced, the implementation would be expensive and less reliable due to introducing active semiconductor-based solution. In addition, a method of carrier modulation with duty shaping algorithm is proposed in [174], which achieves a DC link current reduction of 50%. However, the algorithm is particularly structured for a cascaded system of boost converter and three-phase inverter, typically used for grid-tied PV applications. Moreover, another method for reduction of DC link capacitor stress for a double three-phase drive unit through phase-shifted control and phase displacement is proposed in [175] that reduces the DC link capacitor by upto 30%. However, the switching logic compromises with the overall power quality of the input currents.

Furthermore, it is analyzed and shown in [176] that PAM/PWM mode of operation in a three-phase induction motor drive application can lead to a significant reduction in capacitor ESR loss by reducing the DC-bus capacitor ripple current, leading to increased capacitor lifetime or decreased capacitor size. The method is based on on-line adjustment of the DC link voltage as a function of the variable speed of the motor drive. However, the same technique cannot be applied to a battery connected traction

inverter system, whose DC link is regulated by the battery. In addition, a few research works [178-179] is done on estimating the DC link ripple current stress for parallel three-phase inverters; however, none of these discusses about the ripple current reduction techniques.

Majority of research work in the literature has been focused on minimizing DC link capacitance in single phase AC-DC converters. There is not much research effort on the DC link capacitance reduction in three-phase active rectifier/inverter-based systems. Perhaps, this is due to the fact that there should inherently be no lower order grid frequency harmonic components in DC link current/voltage. However, as shown in our research in [180] the switching frequency harmonic amplitude of the DC link current could be as high as $1/3^{rd}$ of the root mean square (RMS) value of the phase current. It is shown that the intermediate DC link current stress is not minimum in a conventional duty generation logic using average current control, and it can be further optimized by modifying the duty generation logic. Therefore, the DC link capacitor can be further reduced by minimizing the switching fundamental component of the intermediate DC link ripple current without any extra hardware, which is the major focus of this work. The switching fundamental components of both these currents are calculated using generalized state space averaging (GSSA) technique and first harmonic approximation modeling of the DC-DC stage.

The proposed method derives a combination of three phase duty ratios for the PFC converter stage in order to reduce the fundamental switching harmonic component of the intermediate DC link capacitor current, without affecting the input power factor of any phases. In the proposed method, detailed analyses on plant characteristics of both

PFC and DC-DC stages are performed for synthesizing the controller parameters and also, minimizing the intermediate DC link voltage ripple at a wide range of operating conditions. The analyses in this chapter regarding the harmonic reduction of the intermediate DC link current are based on the assumption of both AC-DC and DC-DC stages operating at same switching frequency.

7.1 DC Link Current Stress at Conventional Control

A simplified circuit of the cascaded three-phase boost PFC and PSFB DC-DC converter with a center tapped configuration is shown in Fig. 7.1. The detailed modes of operation of six-switch PFC and PSFB converters can be referred to the well-established literatures in [94, 181].

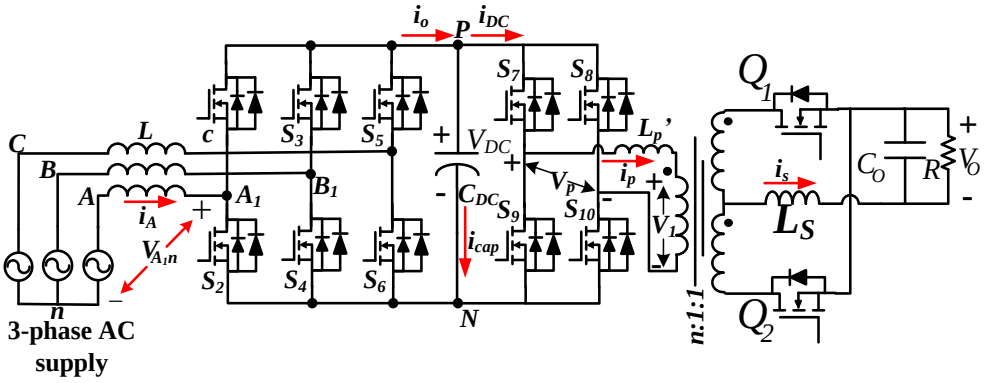


Fig. 7.1. Structure of the integrated three-phase boost PFC and PSFB converter.

It is interesting to determine the maximum DC link ripple in the PFC output capacitor, if no ripple compensation technique is adopted in a conventional control, shown in Fig. 7.2. Therefore, our aim is to determine amplitudes of different frequency components in the current through C_{DC} i.e. $i_{cap}=i_o-i_{DC}$, as the current stress through C_{DC} will directly affect the voltage stress across it. The AC ripple current flowing through

the secondary side of the DC-DC stage is a combination of the reflected amount of the ripple current flowing through C_{DC} and the AC ripple current arising due to the switching action in the PSFB stage.

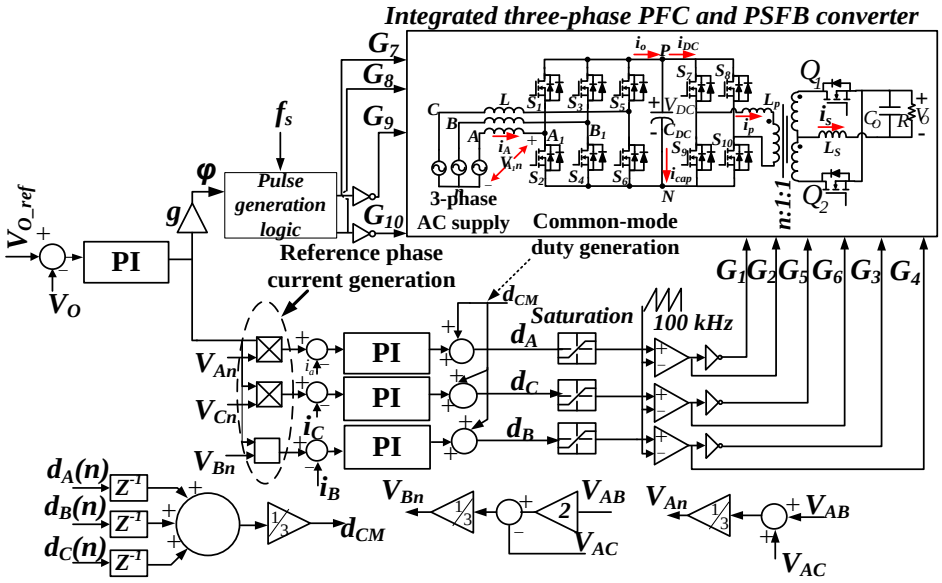


Fig. 7.2. The control block diagram without DC link current minimization logic

The intermediate DC link capacitor ripple current will largely depend on the first switching harmonic amplitude in the sum of the top three switch currents. The switching average of the output current is expressed as follows.

$$i_o = d_A i_A + d_B i_B + d_C i_C \tag{7.1}$$

where, d_A, d_B, and d_C represent the duty ratios of the high-side switches in phase *A*, *B*, and *C*, respectively. From the modeling of the three-phase PFC, it is known that each of the duty ratios is a sum of PI controller output and the common mode duty-ratio term. Using the duty ratio expressions for three phases A, B, C derived in Section 2.2.1 , the net PFC output current is derived in Eq. (7.2), assuming $i_A=Isin(\omega t)$, $i_B=Isin(\omega t-2\pi/3)$,$i_C=I\ sin(\omega t+2\pi/3)$.

$$i_o = MI\left[\sin^2(\omega t) + \sin^2\left(\omega t - \frac{2\pi}{3}\right) + \sin^2\left(\omega t + \frac{2\pi}{3}\right)\right] + MId_{CM}\left[\sin(\omega t) + \sin\left(\omega t - \frac{2\pi}{3}\right) + \sin\left(\omega t + \frac{2\pi}{3}\right)\right] = \frac{3MI}{2} \quad (7.2)$$

where, '*M'* denotes the modulation index of the generated phase duty ratios. Therefore, the output current of PFC stage does not contain any twice-grid frequency or low-order harmonic unlike single phase PFC. However, due to charging and discharging of the PFC output capacitor, the output current contains switching frequency components. Since the minimum frequency component is the switching frequency (100 kHz in our case), it is important to determine the fundamental amplitude of i_o, in order to quantify the intermediate DC link voltage ripple. The PFC bridge output current is the sum of three top-phase leg switch currents and hence, formulated in Eq. (7.3).

$$i_o = S_A i_A + S_B i_B + S_C i_C = (S_A - S_C) i_A + (S_B - S_C) i_B \quad (7.3)$$

where, S_A, S_B and S_C are the switching functions of the top-leg switches of phase *A*, *B* and *C*, respectively. They take the value '1' and '0', when the corresponding switches are ON and OFF, respectively. In order to determine the switching frequency ripple on the DC link voltage, it is required to individually determine the first harmonic amplitude of both the PFC output current and input current to the DC-DC stage. Therefore, applying the convolution relationship of the generalized state space averaging (GSSA) on Eq. (7.3), the 1st harmonic component of the bridge output current can be formulated in Eq. (7.4), where $<x>_k$ represents amplitude of the 'k'th harmonic component of a signal x(t).

$$< i_o >_1 = < (S_A - S_C) >_1 < i_A >_0 + < (S_A - S_C) >_0 < i_A >_1 + < (S_B - S_C) >_1 < i_B >_0 + < (S_B - S_C) >_0 < i_B >_1 \quad (7.4)$$

The first harmonic of phase currents can be assumed zero, i.e. $<i_A>_1=<i_B>_1=0$, as the line currents can be assumed constant over a switching period. To simplify Eq. (5.137) further, it is required to determine 1st and 0th order Fourier coefficients of switching functions. For example, $<S_A>_1$ and $<S_A>_0$ are the 1st and 0th Fourier coefficients of phase 'A' switching function and are calculated using Eq. (7.5) and Eq. (7.6).

$$< S_A >_k = \int_{<T>} S_A \exp(j\omega t) dt \tag{7.5}$$

Therefore, the 1st harmonic of PFC output current essentially depends only on the switching harmonics, present in the PWM duty ratios. The switching function S_A with an instantaneous duty ratio d_A can be graphically represented by comparing a constant value with a triangular carrier signal and thus, demonstrated in Fig. 7.3. Thereby, the 0th and 1st Fourier coefficients are calculated as follows, assuming $\theta=\omega t$.

$$< S_A >_1 = \int_0^{\pi-d_A\pi} 0 d\theta + \int_{\pi-d_A\pi}^{\pi+d_A\pi} 1\times\exp(j\theta) d\theta + \int_{\pi+d_A\pi}^{2\pi} 0 d\theta = \frac{-1}{\pi}\sin(d_A\pi) \tag{7.6}$$

Similarly, the switching fundamentals of the switching functions of *B* and *C* phase i.e. S_B & S_C are represented by $<S_B>_1=-\sin(d_B\pi)/\pi$ and $<S_C>_1=-\sin(d_C\pi)/\pi$, which are real and hence, same as their conjugates. From the law of generalized state space averaging, it is known that the negative order Fourier coefficients are conjugates of the same positive order Fourier coefficients, which leads to: $<S_k>_1=<S_k>_{-1}$, where *k* is *A*, *B* or *C*. In addition, it is a known fact that the averages of the switching functions are the corresponding phase duty ratios of the top switches i.e. $<S_A>_0=d_A$, $<S_B>_0=d_B$, $<S_C>_0=d_C$.

Substituting the fundamental of switching functions from Eq. (7.5)-Eq. (7.6), Eq. (7.4) can be restructured as follows.

$$< i_o >_1 = \frac{i_A}{\pi}(\sin(d_C\pi) - \sin(d_A\pi)) + \frac{i_B}{\pi}(\sin(d_C\pi) - \sin(d_B\pi)) \quad (7.7)$$

The next task is to determine the $<i_{DC}>_1$ in Eq. (7.8), which is the ratio between first harmonic component of intermediate DC voltage and FHA-derived input impedance of DC-DC stage. Thus, $<i_{DC}>_1$ can be obtained using first harmonic approximation (FHA) analysis of the DC-DC stage, as follows.

$$< i_{DC} >_1 = \frac{< V_{DC} >_1}{Z_{in}} \quad (7.8)$$

where, Z_{in} is the input impedance of the PSFB DC-DC stage, formulated in Section 3.2.3. Now, the task is to determine the switching fundamental component of the DC link voltage. In a three-phase PFC connected to a DC link capacitor, the following relationship can be established using the loop formed by phases *A*, *B* and the DC link.

$$V_{A1B1} = -V_{S1} + V_{DC} + V_{S4} \quad (7.9)$$

where, V_{S1} and V_{S4} are the voltages across the switches S_1 and S_4 and can be written in terms of their corresponding phase switching functions: $V_{S1} = -(1-S_A)V_{DC}$ and $V_{S4} = S_B V_{DC}$. From KVL, $V_{A1B1}=V_{A1}-V_{B1}=(V_{An}-V_{LA})-(V_{Bn}-V_{LB})$ holds, where V_{LA} and V_{LB} represent the inductor voltages of phase 'A' and 'B', respectively. Since both the phase voltages and inductor voltages are varying with line frequency, the first switching harmonic of V_{A1B1} is considered to be zero in the analyses. Now, taking the first Fourier coefficients of the relationship in Eq. (7.9), the followings are obtained.

$$< V_{A1B1} >_1 = -< (1 - S_A)V_{DC} >_1 + < V_{DC} >_1 + < S_B V_{DC} >_1 = < (S_A + S_B)V_{DC} >_1 \quad (7.10)$$

This implies

$$< S_A + S_B >_0 < V_{DC} >_1 + < S_A + S_B >_1 < V_{DC} >_0 = 0 \quad (7.11)$$

Using the previously established switching function fundamentals, the final expression of $<V_{DC}>_1$ is obtained as the following.

$$<V_{DC}>_1 = \frac{V_{DC}}{\pi(d_A + d_B)}[\sin d_A\pi + \sin d_B\pi] \tag{7.12}$$

Putting $<V_{DC}>_1$ back into Eq. (7.8) and using the expression of Z_{in}, the switching fundamental of i_{DC} can be calculated, as shown below.

$$<i_{DC}>_1 = \frac{\frac{V_{DC}}{\pi(d_A + d_B)}[\sin d_A\pi + \sin d_B\pi]}{\frac{\pi^2}{4(1+\cos\varphi)^2} \times \frac{s^2RC_oL_{eq} + sL_{eq} + nR}{sC_oR + 1}} \tag{7.13}$$

The intermediate DC link capacitor current is the difference between the PFC bridge output current and the input current to the DC-DC stage i.e. $i_{cap} = i_o - i_{DC}$. Hence, the first harmonic component would be $<i_{cap}>_1 = <i_o>_1 - <i_{DC}>_1$, which is expressed as follows.

$$<i_{cap}>_1 = \frac{i_A}{\pi}(\sin(d_C\pi) - \sin(d_A\pi)) + \frac{i_B}{\pi}(\sin(d_C\pi) - \sin(d_B\pi))\frac{\frac{V_{DC}}{\pi(d_A+d_B)}[\sin(d_A\pi)+\sin(d_B\pi)]}{\frac{\pi^2}{4(1+\cos\varphi)^2} \times \frac{s^2RC_OL_{eq}+sL_{eq}+nR}{sC_OR+1}} \tag{7.14}$$

As can be seen from the above expressions in Eq. (7.12)-Eq. (7.14), both the current and voltage ripples on the intermediate capacitor are factors of duty ratios of two phases. This implies that the third phase can be independently controlled for maintaining the PFC action only. Using the above expressions of $<i_o>_1$ and $<i_{DC}>_1$, $<i_{cap}>_1$ are plotted in MATLAB as a function of i_A and i_B (following 120^o phase difference) at a range of duty ratios from 0 to 1 with the converter specifications listed

in Table 6.3. The values of the first harmonics flowing through C_{DC} at a wide range of load power are extracted from MATLAB results and presented in Fig. 7.4.

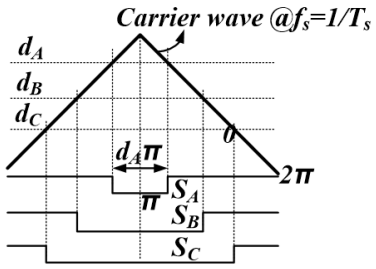


Fig. 7.3. Switching function generation

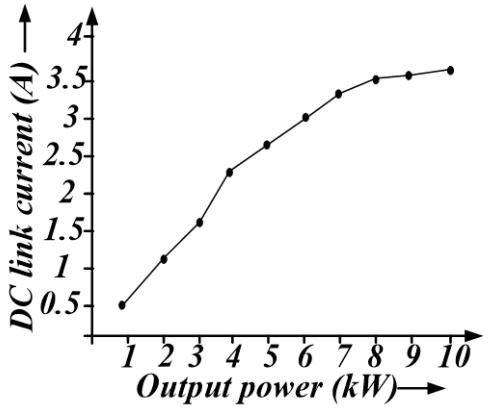


Fig. 7.4. DC link current vs output power level

Also, $<i_{cap}>_1$ takes the maximum value when $d_C \rightarrow 1$, $d_B = d_A \rightarrow 0$, which can be proved by solving $\delta i_{cap}/\delta d_A = \delta i_{cap}/\delta d_B = \delta i_{cap}/\delta d_C = 0$. The maximum value taken by i_{cap} is given by: $\max(i_{cap}) = \max(|(i_A + i_B)/\pi|) = \max(|i_C/\pi|)$, which is approximately 30% of phase current amplitude. It is important to note that the harmonic current through capacitor will be less than 30% of phase current amplitude at different operating conditions of duty ratios. Therefore, a better estimate to quantify the capacitor ripple current would be its RMS value over a switching cycle, which can be determined from the time-domain plot of Eq. (7.14). From Fig. 7.5, the RMS value of switching

harmonic of capacitor current ripple is determined as 2.1A, which is 21.7% of the phase current amplitude.

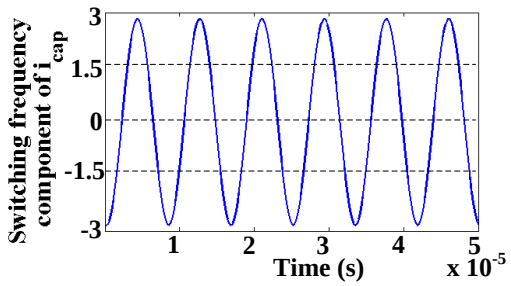


Fig. 7.5. Switching harmonic of capacitor ripple current

Also, for a better understanding, FFT of the DC link capacitor current (i_{cap}) is plotted over a wide frequency range (upto 500kHz) after simulating a 100kHz switching integrated AC-DC converter at 6kW load, which corresponds to ~8A phase RMS current.

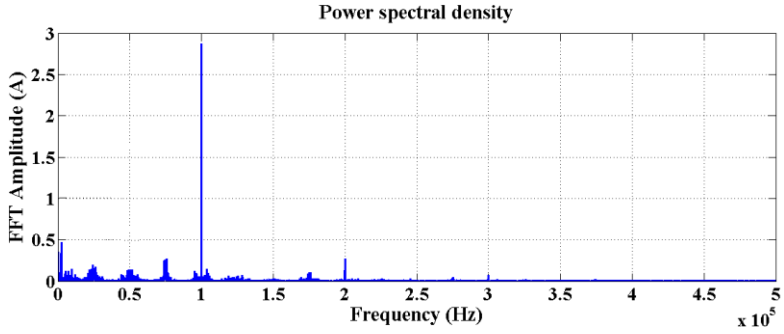


Fig. 7.6. FFT of the DC link capacitor current (i_{cap})

As concluded from the results, the RMS value of the first switching harmonic of DC link current could be 2.1A i.e. as high as ~28% of the phase current RMS in the conventional averaged current control method, which matches close to our theoretical estimation. Moreover, amplitude of the second harmonic of switching frequency is less than 2% and other higher order harmonic amplitudes stay even below 0.5% of phase current amplitude, as seen from the FFT of capacitor current. Therefore, it is inferred

that the first harmonic highly dominates other higher order harmonics in terms of spectrum strength. The worst-case voltage ripple of C_{DC} would be decided by the amount of its RMS current and the switching frequency and would be governed by the following, assuming that the maximum duty ratio of any phase could be 1. The worst-case ripple could arise when dC→1, dB=dA→0 and its expression is presented below.

$$\max(\Delta V_{DC}) = \frac{1}{C_{DC}} \max\left\{\int_0^{T_s} i_{cap}\, dt\right\} = \max\left\{\frac{<i_O>_1 T_s}{C_{DC}}\right\} - \min\left\{\frac{<i_{DC}>_1 T_s}{C_{DC}}\right\} =$$

$$\max\left\{\left|\frac{(i_A+i_B)T_s}{\pi C_{DC}}\right|\right\} = \max\{|\frac{i_C T_s}{\pi C_{DC}}|\} \qquad (7.15)$$

Therefore, at 6kW load power, the minimum C_{DC} required to maintain 2% voltage ripple (of 650V DC link reference) is 200μF at 100 kHz switching frequency, which is obtained from the following formula, derived from Eq. (7.15).

$$C_{DC} = \max\{|\frac{i_C T_s}{\pi \Delta V_{DC}}|\} \qquad (7.16)$$

If a higher voltage ripple is allowed by keeping a lower C_{DC}, the ripple amount would be propagated to the PSFB output and hence, a bulky capacitor needs to be implemented at the final output for its tight regulation. Therefore, it will be of significant advantage if the PFC switching scheme can take care of lowering the ripple current through C_{DC}, and hence, reduce the C_{DC} requirement without compromising any PFC action in phase currents, described in Section IV.

Furthermore, another objective of the control approach is to regulate the output DC voltage at a reference value and maintain the unity power factor operation of the input phase currents. Therefore, the typical choice of the state variables in such cascaded converter system would be the PSFB output voltage, any two input phase voltages and any two input phase currents. However, with such selection of state variables, the

intermediate DC link voltage will not be regulated, which potentially leaves a challenge in the selection of voltage stress rating of the switch. In a conventional average current mode controlled loop, shown in Fig. 7.2, the PFC stage phase current references would be generated by multiplying the DC voltage controller output with the respective phase voltages. Typically, the voltage control loop is developed for maintaining only the final DC output (PSFB output in our case) at its reference level. As a result, no constraint is imposed on the reference level of the intermediate DC link voltage.

7.2 Intermediate DC Link Capacitor Reduction Method

In order to take care of the concern of DC voltage regulation, the feedback control is applied for both the intermediate and final DC voltages, shown in Fig. 7.7. The sum of the both voltage controller outputs acts as a trans-conductance, which is multiplied to the PLL synchronized phase voltages and generates the phase current references. The output of the PSFB voltage controller also acts a reference to the phase angle difference between the diagonally opposite switches, which refers to a higher active power at a higher phase difference. The pulse width modulation (PWM) signals of the DC-DC stage are generated using the phase angle reference and switching frequency information.

The control objective is to develop a stable, well-regulated control system for the integrated AC-DC converter with simultaneously minimizing the intermediate DC link ripple current. In order to prove the stability of the proposed closed loop system, it is required to derive the plant characteristics of the integrated stage.

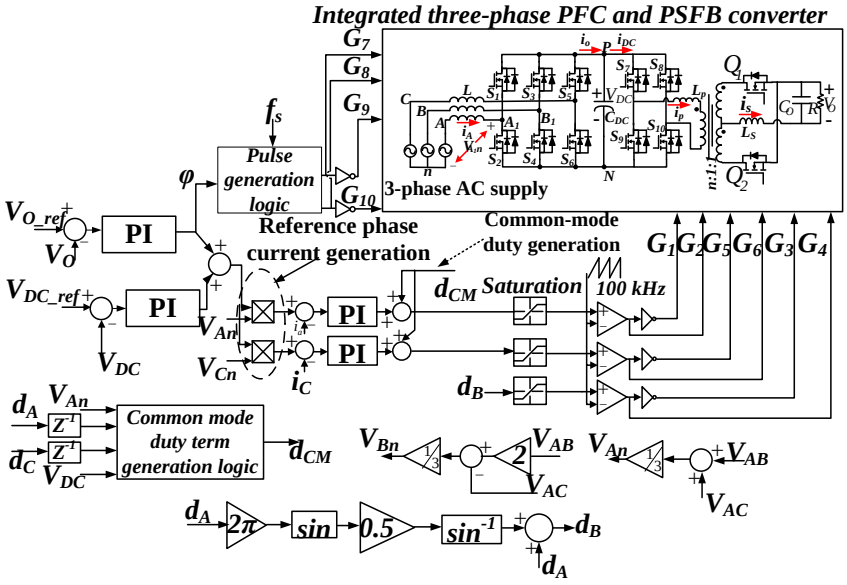


Fig. 7.7. The proposed control strategy for DC-link capacitor reduction

In PFC stage analyses, taking perturbation on the operating duty ratios of D_{AH}, D_{BH}, D_{CH} for *A*, *B*, *C* phases, respectively, the following small-signal transfer function between phase current and intermediate DC link voltage is obtained.

$$\frac{\Delta i_a(s)}{\Delta v_{DC}(s)} = \frac{4D_{AH} + D_{BH} + D_{CH}}{3sL} \tag{7.17}$$

The PFC output current i_o can be formulated as $i_o = i_{cap} + i_{DC} = (d_A - d_C)i_A + (d_B - d_C)i_B + V_{DC}/Z_{in}$. Taking Laplace transformation on the both sides of the previous expression and applying perturbation in phase 'A' duty and current, the following relationship is obtained.

$$\frac{\Delta d_A(s)}{\Delta v_{DC}(s)} = \frac{sCZ_{in}(s)+1}{Z_{in}(s)I_A} \tag{7.18}$$

Combining Eq. (7.17) and Eq. (7.18), the plant transfer function between phase duty and current is obtained and shown in Eq. (7.19). Considering a PI compensator on this plant and applying the Routh-Hurwitz stability criterion on its characteristics

equation, shown in Eq. (7.20), the stability conditions are obtained as $K_p>0$, $K_i>K_pL_{eq}C$, which gives us flexibility to choose any positive K_p and consequently, select K_i to ensure stability.

$$G_p(s)=\frac{\Delta i_a(s)}{\Delta d_{AH}(s)}=\frac{Z_{in}(s)I_A(1-\frac{4D_{AH}+D_{BH}+D_{CH}}{3})}{sL(sCZ_{in}(s)+1)} \tag{7.19}$$

$$s^2L(1+sCZ_{in}(s))+(k_ps+k_i)YZ_{in}(s)=0 \tag{7.20}$$

In terms of minimizing C_{DC}, it is our aim to minimize the net cost function expression $<i_{cap}>_1=<i_o>_1-<i_{DC}>_1$, presented in Eq. (7.21), obtained from previous GSSA analysis. Each of these two currents i.e. i_o and i_{DC}, consist of a DC content and different components of switching frequency and its multiples. However, only the average component will be responsible for active power transfer to the load and the switching frequency component is obvious to be present due to the duty modulation in the control loop. As described in the previous section, switching frequency component has the major contribution in determining the overall value of the capacitor to maintain a particular ripple limit. Here, the main objective is to minimize the switching frequency harmonics with respect to the phase duty ratios of the three phases in the PFC stage, without violating the PFC action.

$$< i_{cap} >_1=\{\frac{i_A}{\pi}(sin(d_C\pi)-sin(d_A\pi))+\frac{i_B}{\pi}(sin(d_C\pi)-sin(d_B\pi))-\frac{\frac{V_{DC}}{\pi(d_A+d_B)}[sind_A\pi+sind_B\pi]}{\frac{\pi^2}{4(1+cos\,\phi)^2}\times\frac{s^2RC_oL_{eq}+sL_{eq}+nR}{sC_oR+1}}\} \tag{7.21}$$

For the sake of simplicity of the calculation, the above expression is reduced as the following.

$$< i_{cap} >_1=(k_A(sin(d_A\pi)+k_B(sin(d_B\pi)+k_C(sin(d_C\pi)) \tag{7.22}$$

where,
$$k_A = \frac{i_A}{\pi} - \frac{V_{DC}}{\pi(d_A + d_B)Z_{in}} \tag{7.23}$$

$$k_B = -\frac{i_B}{\pi} - \frac{V_{DC}}{\pi(d_A + d_B)Z_{in}} \tag{7.24}$$

$$k_C = \frac{i_B - i_A}{\pi} \tag{7.25}$$

Therefore, minimizing the first harmonic current imposes an extra constraint on the phase duty ratios. However, since it is of the primary concern that the PFC action must be maintained, any two phases (say *A* and *C*) should be controlled exactly same as the proposed loop in Fig. 7.6. If the currents of these two phases maintain their individual reference waveforms with UPF, the third current would certainly maintain the PFC action, as the sum of the three currents has to be zero in an open neutral three-phase AC system. This flexibility on the third phase duty ratio implies that it can be derived subject to the constraint of minimizing the overall DC link ripple without affecting PFC action. In order to minimize the duty-dependent capacitor current (i_{cap}) expressed in Eq. (7.21), it turns out that the partial derivatives of the cost function (i_{cap}) with respect to d_A and d_B should be individually zero, i.e. $\delta i_{cap}/\delta d_A = \delta i_{cap}/\delta d_B = 0$, which finally leads to the following expressions. The ultimate objective is to obtain an inter-relation between the phase duty ratios using Eq. (7.26 -7.27).

$$i_A \cos(d_A \pi) = \frac{V_{DC}[(d_A + d_B)\pi \cos(d_A \pi) - \sin(d_A \pi) - \sin(d_B \pi)]}{Z_{in}\pi(d_A + d_B)^2} \tag{7.26}$$

$$i_B \cos(d_B \pi) = \frac{V_{DC}[(d_A + d_B)\pi \cos(d_B \pi) - \sin(d_A \pi) - \sin(d_B \pi)]}{Z_{in}\pi(d_A + d_B)^2} \tag{7.27}$$

Taking the ratio of Eq. (7.26) and Eq. (7.27), the following relationship between d_A and d_B is obtained.

$$cos(d_A\pi)\,sin(d_B\pi) + cos(d_A\pi)\,sin(d_A\pi) - sin(d_A\pi)\,cos(d_B\pi) - sin(d_B\pi)\,cos(d_B\pi) = 0 \quad (7.28)$$

Hence, the phase 'B' duty can be finally formulated as the following.

$$d_B = d_A + \sin^{-1}\left(\frac{\sin 2d_A\pi}{2}\right) \quad (7.29)$$

This implies that the phase 'B' duty will be directly governed by phase 'A' duty, which is synthesized from the condition of power factor correction. The inter-dependence of phase duty ratios, as expressed in Eq. (7.29) is never imposed in a conventional PFC control and modulation technique. Therefore, the proposed approach ensures to impose such interdependence among the phase duty ratios by using only two phase-current feedback controllers. As opposed to the conventional control strategy, where three cross-coupled phase current controllers are developed, the third phase PI compensator is removed in our proposed approach and the third phase duty is being derived using its interdependence with the instantaneous duty ratios of other two phases.

In this approach, one of the major challenges will be to find out the floating-point potential V_{nN}, which plays an important role in the overall duty ratio function. The method used in Section II for determining V_{nN} cannot be used here, as the third phase is not controlled the same way as other two phases are done. From the structure of phase duty ratios for the PFC stage, it is clear that: $d_C[n] = M\sin\left(\omega nT_s - {}^{2\pi}/_{3}\right) + \frac{V_{nN}}{V_{DC}}$; $d_A[n] = M\sin(\omega nT_s) + \frac{V_{nN}}{V_{DC}}$. Adding these together, Eq. (7.30) is obtained.

$$\frac{2V_{nN}}{V_{DC}} = (d_A + d_C) + M\sin(\theta + \frac{\pi}{3}) \quad (7.30)$$

In the above relation, '*M*' is modulation index i.e. the ratio of phase-neutral peak voltage to the reference DC link voltage. Performing the subtraction operation between the same two duty ratios, the following is obtained.

$$(d_A - d_C) = \sqrt{3}M\,cos(\theta + \frac{\pi}{3}) \tag{7.31}$$

Using the above two relationships, Eq. (7.32) derives an expression of the common mode duty ratio independent of grid phase angle computed by PLL.

$$\frac{V_{nN}}{V_{DC}} = \frac{1}{2}[(d_A + d_C) + \sqrt{M^2 - \frac{(d_A - d_C)^2}{3}}] \tag{7.32}$$

It is to be remembered that the above ratio would be calculated based on the duty ratios in the previous cycle (*(n-1)*th) and thus, would be used in the duty ratio derivation in 'n'th cycle. Therefore, the final expressions of the duty ratios of phase '*A*' and '*C*' can be recomputed using the following relationships.

$$d_A[n] = \frac{V_{An} + V_{nN}}{V_{DC}} = PI_A + \frac{1}{2}[(d_A[n-1] + d_C[n-1]) + \sqrt{M^2 - \frac{(d_A[n-1] - d_B[n-1])^2}{3}} \tag{7.33}$$

$$d_C[n] = \frac{V_{Cn} + V_{nN}}{V_{DC}} = PI_C + \frac{1}{2}[(d_A[n-1] + d_C[n-1]) + \sqrt{M^2 - \frac{(d_A[n-1] - d_B[n-1])^2}{3}} \tag{7.34}$$

where, PI_A and PI_C denote the outputs of the PI compensators of phase '*A*' and '*C*', respectively.

By implementing this control strategy, it is expected that the harmonics amplitudes of the switching frequency multiples will be reduced significantly. In order to validate this concept, the FFT spectrum of the capacitor current at 6kW output power is plotted and it is observed that the spectrum amplitudes of second & higher order harmonic components are reduced to 10% and even lesser. This confirms the reduction in RMS current stress on the intermediate DC link capacitor. The maximum amplitude

($<i_{cap}>_{1,max}$) of the fundamental switching frequency component can be quantified by replacing the optimum condition of d_B from Eq. (7.29) in the net cost function expression in Eq. (7.21), which leads to Eq. (7.35). The maximum capacitance to maintain ΔV_{DC} ripple is formulated in Eq. (7.36).

$$< i_{cap} >_{1,\max} = \sqrt{(k_A^{\,2} + \frac{k_B^{\,2}}{4} + \frac{3k_C^{\,2}}{4})} \tag{7.35}$$

$$C_{DC} < \frac{< i_{cap} >_{1,\max} T_s}{\Delta V_{DC}} \tag{7.36}$$

The numerical value of the maximum ripple current through the DC link capacitor can be determined by calculating k_A, k_B and k_C from the converter specifications. Thus, it is proven that the DC link current ripple, obtained by conventional averaged current-based control is not minimum, rather utilizing the flexibility on the third phase duty, imposing an optimal constraint on it gives minimum DC link current stress and hence, requires a lower DC link capacitance.

In order to establish the stability of the overall system, the open loop Bode plot corresponding to the loop gain of the system is shown in Fig. 7.8, which denotes the gain crossover frequency (f_{BWC}) and phase margin of 5 kHz and 85°, respectively.

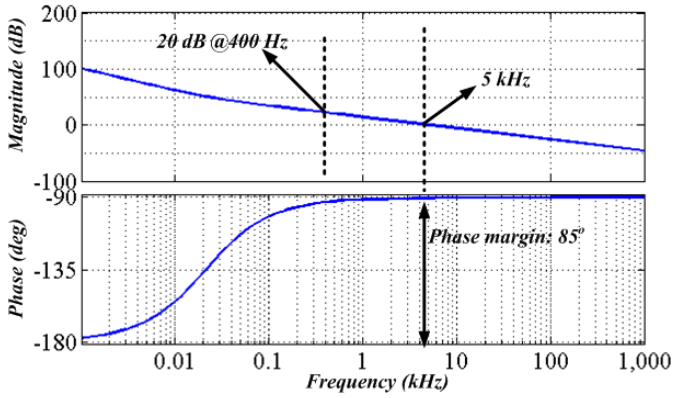


Fig. 7.8. Open loop Bode plot of the proposed control loop

The loop gain at 400Hz is 20dB, which implies that the closed loop gain at the grid frequency is near unity. From 3^o phase displacement at the grid frequency, the input power factor stands out as 0.995. Furthermore, during the load transient, the amount of overshoot and settling time depend on the closed loop quality factor, which is related to the phase margin in the following way, established in [31].

$$Q = \frac{\sqrt{\cos(\phi_M)}}{\sin(\phi_M)} \tag{7.37}$$

From the calculated phase margin with the designed controller, the closed loop quality factor is 0.3, which denotes a damping coefficient of 1.67. The relationship between settling time and the damping coefficient [31], shown in Eq. (7.38), gives a 5% settling time of 100 µs, which maintains a good agreement with the experimental results of load transient.

$$t_{st} = \frac{4}{\xi\omega_n} = \frac{4}{2\pi f_{BWC}\xi} \tag{7.38}$$

where, ζ is the damping coefficient and ω_n is the current loop crossover frequency.

Furthermore, in order to theoretically validate the effectiveness of the DC link current stress minimization approach, a FFT of the intermediate DC link capacitor current i.e. i_{cap} is plotted in Fig. 7.9.

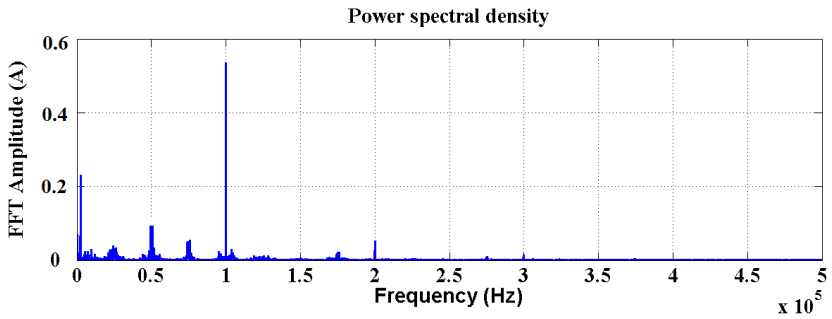


Fig. 7.9. FFT of the DC link capacitor current under the proposed control strategy

With the proposed control, the switching harmonic peak current reduces to 0.55A as seen from the FFT in Fig. 7.9, which implies the RMS current to be 0.4A due to the sinusoidal variation of switching harmonic component. This 80% reduction (from 2.1A to 0.4A) in capacitor current ripple RMS demonstrates a significantly reduced current stress on C_{DC}. The DC link voltage ripple will also be scaled down to 20% of its uncompensated value, as the voltage ripple is proportional to its current stress, as seen from Eq. (7.14).

One of the important aspects to analyze is the regulation of the PFC output voltage during any load transient. This requires an accurate dynamics of intermediate DC voltage during the load transient; therefore, a frequency domain voltage loop study followed by time domain analyses is performed. Fig. 7.10 shows the equivalent voltage control loop of three-phase boost PFC with an equivalent load Z_L, i.e. the input impedance of switching DC-DC converter. The DC voltage controller output (Y) denotes the equivalent phase trans-conductance, which being multiplied with phase voltages generates the phase currents. The intermediate DC link voltage can be expressed as the multiplication of output current and equivalent PFC output impedance i.e. $Z_L||1/sC_{DC}$. For simplicity at the steady state, Z_L can be approximated by an equivalent resistive load R_{eq} from the perspective of power balancing, where $R_{eq}=V_{DC}^2/P$. The relationship between the PFC output voltage and DC voltage controller output can be derived using Eq. (7.39).

$$V_{DC} = i_o(Z_L \parallel \frac{1}{sC_{DC}}) = \frac{3}{2}KVY(Z_L \parallel \frac{1}{sC_{DC}}) = \beta Y(Z_L \parallel \frac{1}{sC_{DC}}) \tag{7.39}$$

Where V is the peak phase-neutral voltage and $\beta=3KV/2$.

Thus, the transfer function between PFC DC link voltage and its reference can be determined, as shown in Eq. (7.40).

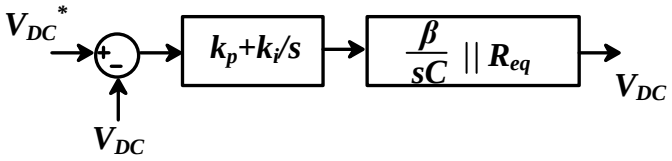


Fig. 7.10. Voltage control loop for three-phase PFC

$$V_{DC} = V_{DC}^* \frac{\beta / C_{DC} (k_p s + k_i)}{s^2 + s\frac{\beta}{R_{eq} C_{DC}}(1 + k_p R_{eq}) + \frac{\beta k_i}{C_{DC}}} \tag{7.40}$$

Therefore, the instantaneous DC link voltage can be expressed in terms of its reference value, equivalent load resistance and controller parameters in the following way.

$$V_{DC} = V_{DC}^* [\exp(-\frac{\gamma_2 t}{2})\{\cos(\sqrt{\gamma_3^2 - \frac{\gamma_2^2}{4}})t + \frac{\gamma_1(z-\gamma_2)}{\sqrt{\gamma_3^2 - \frac{\gamma_2^2}{4}}} \sin(\sqrt{\gamma_3^2 - \frac{\gamma_2^2}{4}})t\}] \tag{7.41}$$

where $\gamma_1=\beta k_p/C_{DC}$, $\gamma_2=\beta(1+R_{eq}k_p)/R_{eq}C_{DC}$. $\gamma_3=\beta k_i/C_{DC}$.

During the load step-down, the increase in equivalent load resistance would result in reduction in γ_2. At the instant of load rejection (i.e. $t \rightarrow 0$), the maximum value of V_{DC} during the overshoot at load reduction could be expressed as follows.

$$V_{DC,max} = V_{DC}^* \max\left[\cos\left(\sqrt{\gamma_3^2 - \frac{\gamma_2^2}{4}}\right)t + \frac{\gamma_1(z-\gamma_2)}{\sqrt{\gamma_3^2 - \frac{\gamma_2^2}{4}}} \sin\left(\sqrt{\gamma_3^2 - \frac{\gamma_2^2}{4}}\right)t\right] = V_{DC}^*(1 + \frac{\gamma_1^2(z-\gamma_2)^2}{\gamma_3^2 - \frac{\gamma_2^2}{4}}) \tag{7.42}$$

Therefore, the maximum overshoot of V_{DC} during load step-down can be limited by the selection of a lower γ_1 and higher γ_3, which require a low k_p and high k_i, respectively.

In this design, the maximum overshoot of PFC DC voltage is restricted below 6% of the reference DC link voltage.

In order to validate the proposed analyses of DC bus voltage overshoot, an experiment on 33% load reduction (from 6kW to 4kW) is conducted and the corresponding waveform in Fig. 7.11 (in Section V) represents an overshoot of 15V in PFC DC link, which is less than 6% of its reference level.

Furthermore, it is important to mention that the bandwidth and the stability margins of the PFC current loop do not depend on the output capacitance, rather depends only on the boost inductance [182], as the output voltage is assumed constant in the current loop analyses. However, the stability margins and bandwidth of the PFC output voltage loop highly depends on the output capacitance. From the voltage loop transfer function, shown in Eq. (7.40), the bandwidth and phase margin can be expressed as follows.

$$f_{BWV} = \sqrt{\frac{\beta k_i}{C_{DC}}} \tag{7.43}$$

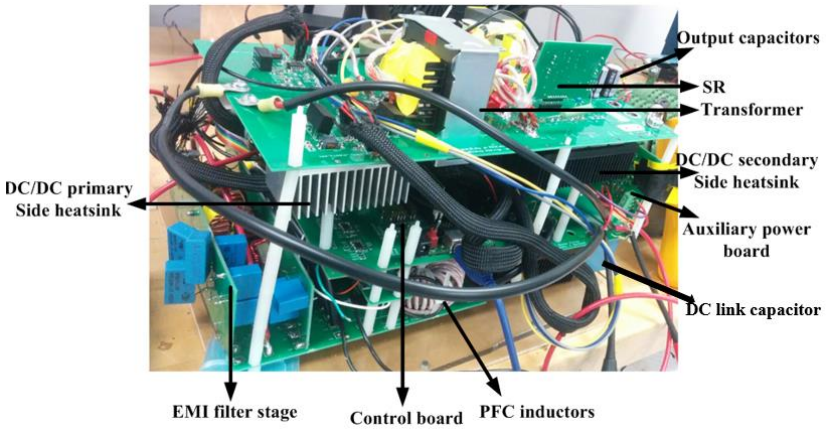
$$\phi_{PM} = 90^{o} + \tan^{-1}\frac{2\pi f_{BWV} k_p}{k_i} \tag{7.44}$$

In this design with 45µF intermediate capacitance and used controller parameters, the bandwidth and phase margin of the voltage loop are 40 Hz and 125^{o}, respectively.

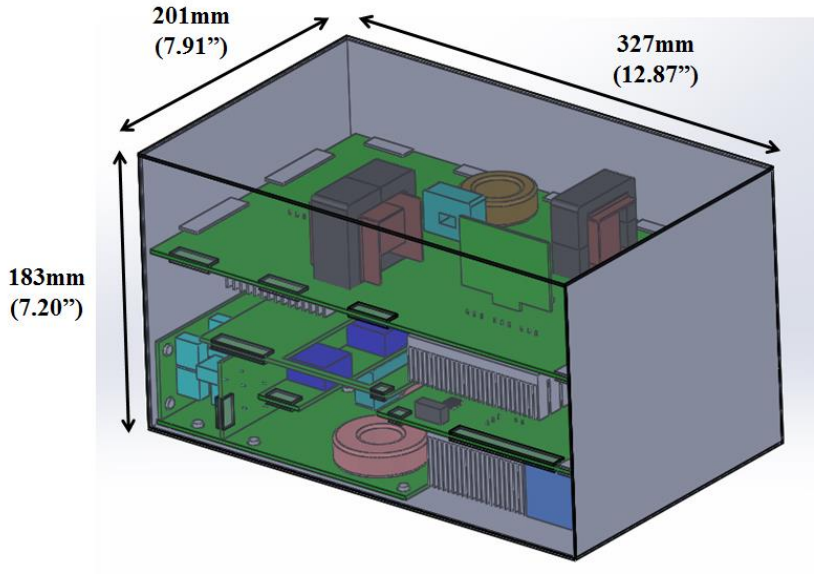
7.3 Experimental Results

As a proof-of-concept verification to the proposed control and DC link current reduction methodologies, a hardware prototype of a three-phase boost PFC and PSFB DC-DC converter with 6kW (continuous)/ 10kW(peak) rating, shown in Fig. 7.11 (a),

is designed and tested. For distinct visualization, the model developed in Solidworks is shown in Fig. 7.11 (b).



(a)



(b)

Fig. 7.11. (a) Prototype of integrated three-phase PFC and PSFB DC-DC stage (b) Solidworks model of RTRU

The control algorithm is implemented in a floating-point DSP TMS320F28335. The nominal test condition is kept at 230V phase-neutral RMS 400Hz AC input and 28V DC output, which is typical for avionics applications with the specifications of

some of the regulated transformer rectifier units (RTRUs) in more-electric-airplanes (MEA). The intermediate DC link voltage is regulated at 650V, which follows a modulation index of 0.75. The cascaded converter is experimented under a wide range of input voltages and load powers to validate the effectiveness of the proposed control and DC link current reduction method. Both the PFC and PSFB converters are designed with a list of converter specifications according to Table 6.3, by following the important guidelines and considerations, mentioned in the well-established literature [77, 181]. Synchronous rectifications (SR) are used in the secondary side switching of the PSFB converter to minimize the conduction loss and therefore, three MOSFETs are used in parallel to realize one secondary switch for minimizing the overall ON resistance.

Fig. 7.12 shows the steady state experimental waveforms of the PFC stage with the proposed control at 6kW load. The final output DC voltage and the intermediate DC link reference are set at 28V and 650V, respectively. A set of experimental results is collected with the conventional control using intermediate DC link capacitor of 200 μF, which gives 1% voltage ripple around the reference value i.e. 650V DC. The steady state voltage and current waveforms of the PFC and PSFB stages are shown in Fig. 7.12 and Fig. 7.13, respectively.

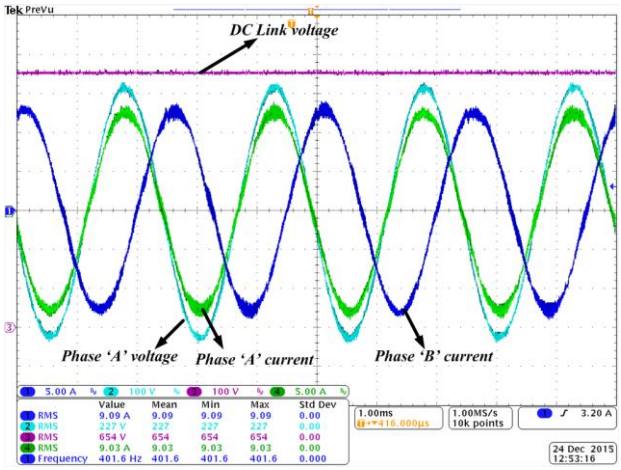


Fig. 7.12. V_{DC}=650V, i_A =i_B =9.06A (RMS), V_{An} (RMS) =230V, P_{out}=6kW.

As seen in Fig. 7.13, the input currents maintain power factor (PF) of 0.998 and a THD of 4.2% at 6kW. On the other hand, the PSFB output voltage is regulated at 28V DC a steady state phase angle shift of 57°, shown in Fig. 7.13.

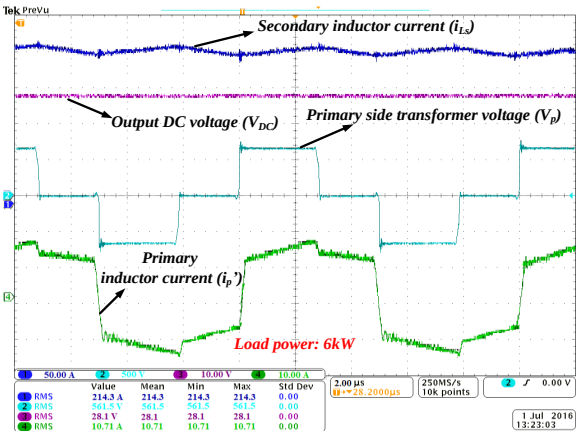


Fig. 7.13. PSFB waveforms at 6kW load power; V_{DC} = 650V, V_O = 28V.

With the proposed DC link capacitor reduction algorithm using the list of design specifications and applying the maximum ripple current expression from Eq. (168), <1% voltage ripple can be obtained using a 45 µF PFC output capacitor, which is less than 1/4th of the PFC DC link capacitor without any compensation for maintaining the same ripple. For a better illustration, the PFC stage waveforms using 45 µF DC-link

capacitor with and without the compensation strategy are shown in Fig. 7.14 and Fig. 7.15, respectively.

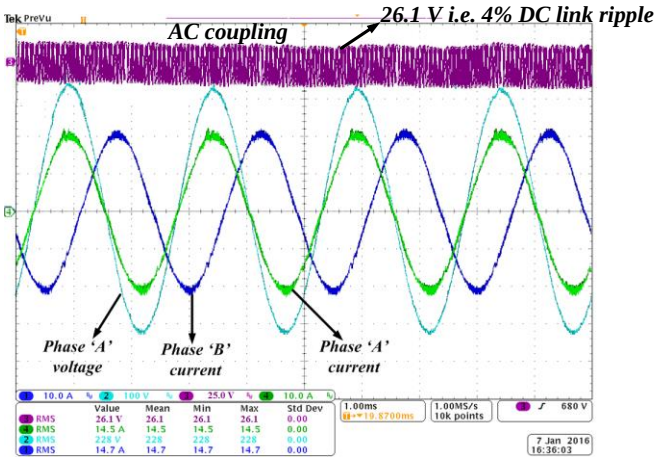


Fig. 7.14. Voltage and current waveforms of the 6kW three-phase inverter experiment with conventional control: 4% DC voltage ripple with 45µF capacitance (as seen from the AC coupling measurement of DC link voltage)

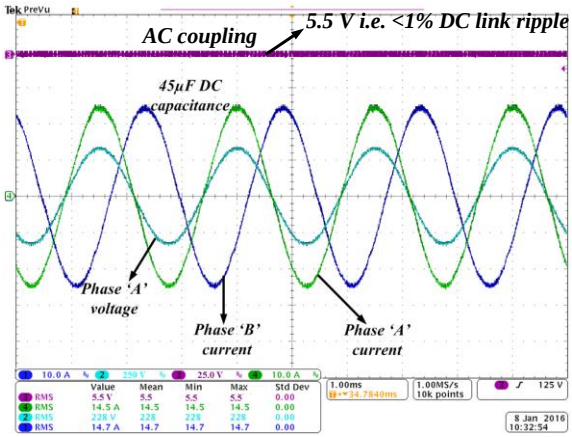


Fig. 7.15. Voltage and current waveforms of the 6kW three-phase inverter experiment with the proposed control: 1% DC voltage ripple with 45µF capacitance (as seen from the AC coupling measurement of DC link voltage).

For a clear understanding of the high frequency ripple magnitude, the DC link voltage measurements are taken in AC coupling mode, which shows 100 kHz AC ripple variation around the mean DC link voltage (i.e. 650V). It shows that the proposed DC

link current minimization strategy can reduce the DC link voltage ripple from 4% i.e. 26.1V to <1% i.e. 5.5Vat 45 µF PFC capacitance with maintaining input current THD of 4% and PF of 0.995 for all three input phases. The experimental results with this approach at 6kW exhibit a conversion efficiency of 98.3% for the PFC stage and 97.1% for the PSFB stage.

In addition, the cascaded converter is tested at variable load conditions to illustrate the effectiveness of control methodology. Under 33% overload (6kW to 8kW), it takes 100µs (less than 1/20th a line cycle) to settle down to the intermediate DC link reference voltage and phase currents, which indicates a reasonably fast transient dynamic of the proposed control, as shown in Fig. 7.16. The time taken by the DC-DC stage to reach the reference output DC link voltage level i.e. 28V is 100µs. The waveforms under the load transient are shown in Fig. 7.16, which demonstrate both the settled down voltages V_{DC} and V_O. The converter waveforms during 33% step-down in load power are shown in Fig. 7.17, which demonstrates a <6% overshoot in the output DC voltage.

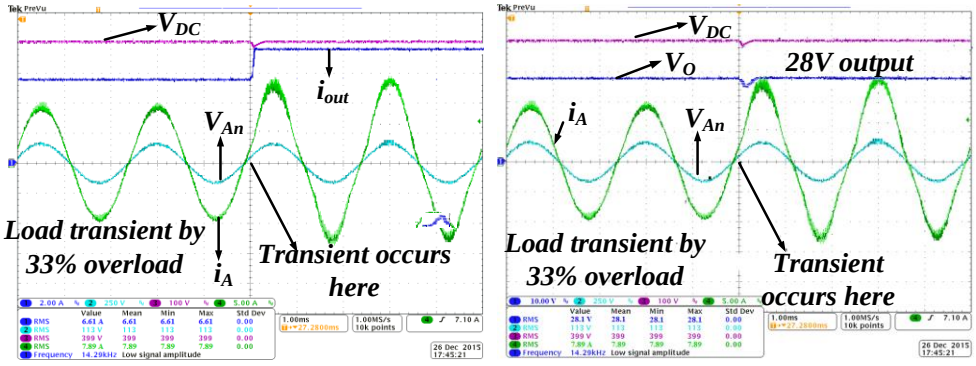


Fig. 7.16. The converter waveforms under load transient from 6kW to 8kW.

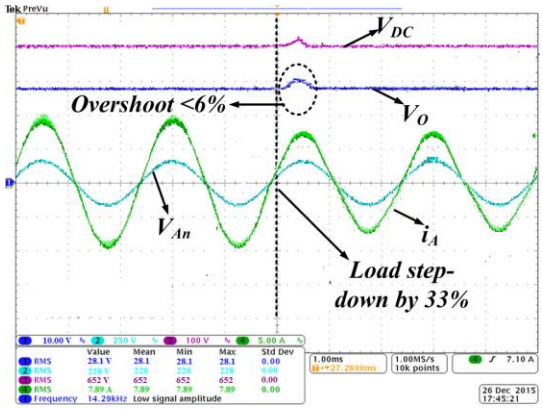


Fig. 7.17. The converter waveforms under load step-down from 6kW to 4kW

It is important to note that although the existence of even order pulsations in load power under the presence of odd-order current harmonics holds true for a single-phase AC system, but the AC components of load power delivered by three phases sum up to zero due to 120^o mutual phase difference in a balanced three-phase AC system.

For better understanding, based on the fast Fourier transformation (FFT), the amplitudes of different harmonic components of input phase current after load transient are plotted in a bar-chart form in Fig. 7.18 and compared with their individual limits specified by DO-160F EMI standard for avionics applications.

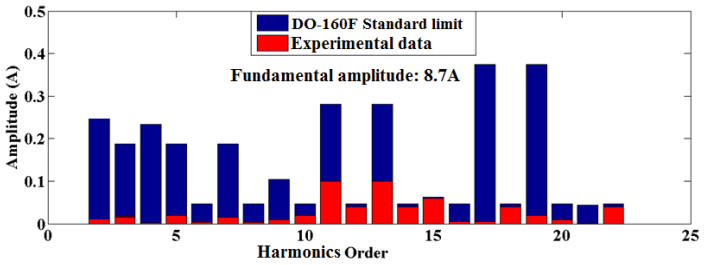


Fig. 7.18. FFT amplitudes of lower order grid frequency harmonics (800 Hz (2nd harmonic) to ~9kHz (22nd harmonic))

Please note that the amplitude of the fundamental component is 8.7A at 6kW load and rated input voltage. Thus, the maximum THD of input currents of all three phases

after the load transient is calculated from experimental data and obtained as 4.8%, which is reasonably good. In order to achieve a good input power quality, the current loop bandwidth is kept at 5 kHz (PI coefficients: k_p=0.008, k_i=1000), which offers a reasonable attenuation to the grid frequency harmonics components of the input current and also, maintains reasonably good transient performance.

The DC link capacitor (film type) takes a significant portion of both weight and volume of the entire system. A pie-chart, shown in Fig. 7.19, is plotted for a clear understanding about the weight contribution of different components at the cascaded combination structure, discussed in this work.

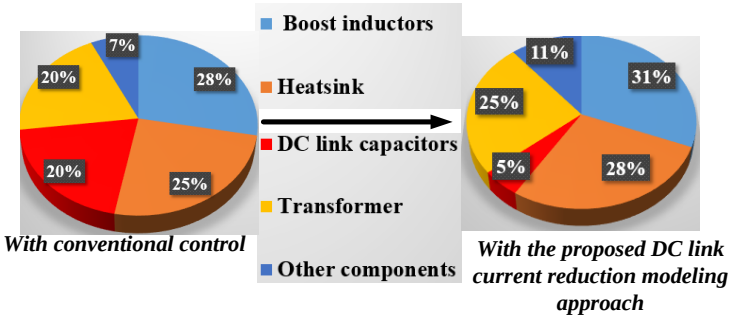


Fig. 7.19. The weight split of components in the cascaded AC-DC stage.

The reduction of the capacitor value from 200 µF to 45 µF helps lower down the weight of the capacitor bank from 1.5 lbs. to 0.4 lbs., which reduces the overall weight by 1.1 lbs. and improves the overall specific power density by 12% approximately. Furthermore, this capacitor reduction benefits in overall volume reduction by 50 $inch^3$, which is about 8% of the overall system volume. The amount of DC link capacitance reduction through the proposed methodology is more than some of the earlier proposed methods i.e. 50% reduction through delayed output voltage control [168], 20-30% reduction in [169-170]. Although ~25% reduction in DC capacitor current can be achieved in [171] by variable DC link voltage implementation, it uses speed of the

motor as a governing variable, which cannot be used for a three-phase based rectifier-based converter system. Furthermore, the input current THD is slightly improved (~by 0.5%) due to less switching component in the proposed approach unlike the proposed method in [168], which reduces the voltage ripple by distorting the input current.

7.4 Summary

In this chapter, a method to reduce the intermediate DC link capacitance for a cascaded combination of a three-phase boost PFC and a PSFB DC-DC converter is proposed and validated through a proof-of-concept verification by experimenting a laboratory prototype at 6kW load power. Since the DC link current stress is highly dependent on the phase duty ratios, the prospective control approach imposes an additional constraint on the duty ratios, subject to minimizing the DC link current without affecting unity PFC operation. The proposed control method enables over 70% reduction of DC capacitance, which leads to reducing the overall system weight by 10% and improving the overall specific power density by 16%. In addition, the control method ensures a THD of 4% and a PF of 0.998. The proposed approach is general, and a similar duty constrained modeling approach can be applied for power density improvement of a single-phase rectifier or inverter-based system through DC link capacitor reduction.

Chapter 8: Conclusions and Future Work

8.1 Conclusions

This dissertation work proposes an innovative approach to replace TRUs by actively controlled RTRUs employing the advantages of emerging wide band gap (WBG) semiconductor technology. The work comprehensively investigates and discusses fundamental theoretical design and control strategy along with implementation of different performance enhancement schemes for a three-phase active boost rectifier and a PSFB DC-DC converter along with front-end EMI filter stage, as major parts of a RTRU, which is used as an auxiliary power supply unit in more electric airplanes (MEAs). The duty compensated feedback control system is proposed to improve the input power quality of RTRU, which improved the THD from 9.1% to 4.3%. In addition, switching loss improvement in PFC stage has been carried out by implementing zero-voltage switching using minimum add-on auxiliary components, which helps improve the conversion efficiency by 0.6%. Furthermore, implementation of a fast start-up control without increasing the inrush current level is proposed in this work, which makes the RTRU start-up action four times faster than using a conventional control loop.

Moreover, the maximum efficiency tracking at different loading conditions for the PSFB converter is performed by variable switching frequency control, which shows an increase of near 1.5% in comparison to the conventional fixed frequency control. Such concept can be applied to many other DC/DC converters to minimize the power loss with keeping a potential challenge of EMI filter design in mind. The RTRU efficiency

maximum is tracked by varying the intermediate DC link voltage for different loading conditions, which results in 1% efficiency improvement in comparison to fixed DC link approach. Besides, the power density improvement through intermediate DC link reduction is achieved by minimizing the ripple current with switching frequency component flowing through the intermediate capacitance. The ripple current is minimized with respect to the phase duty ratios without affecting the unity power factor operation, which enables over 70% reduction of DC capacitance leading to 10% weight reduction and 16% power density improvement.

The validations of various implemented control methodologies, start-up schemes, and dynamics improvement of the integrated converter are performed through conducting experiments on the developed prototypes of individual converters with upto 6kW (continuous)/ 10kW (peak) load power. The RTRU output DC voltage ripple is kept within a band of ±1% (peak-peak), which satisfies the tight voltage regulation requirement. The input current THD is measured as 4.3% obtained after analyzing the real-time experimental data in MATLAB. The conversion efficiencies of PFC and PSFB converters are reported as 98.4% and 97.2%, respectively at 6kW continuous load with 100 kHz fixed switching frequency, from the experimental measurements. In addition, the frequency spectrum of input AC current of the RTRU complies with RTCA DO-160F conducted EMI requirement (from 150 kHz to 30 MHz) with the designed two-staged EMI filter of only 1.1 lbs.

8.2 Future work

The future work as an extension to this dissertation work could be majorly classified into two parts: (i) evaluation of other alternative topologies (ii) RTRU system level optimization, which are explained as follows.

8.2.1. Alternative prospective RTRU topologies

The existing Silicon Carbide (SiC) based RTRU design uses a two-stage structure – a three-phase boost PFC cascaded with a PSFB DC-DC converter. While the existing design meets the specifications, it does not ensure modularity – failure of a single component in any part of the circuit renders the complete inoperable. There could be multiple alternative solutions by which modularity can be brought into the system.

The first solution could be using three 3-phase RTRUs of 2 kW power rating (each) in parallel as shown in Fig. 8.1. Under component failures in any of the units, rest other units will operate and can deliver power to the RTRU loads. However, under any phase failure in the input side, all three units will suffer equally, and the power flow amount will be restricted. One major advantage of this solution is that it does not require any access to the source neutral point.

As can be seen from the volume and weight split of different major power components of RTRU, the DC link capacitor takes a significant fraction. Therefore, DC link less AC-DC converters have potential to become popular in MEA applications requiring high-density power conversion. Three-phase isolated matrix converter [183] shown in Fig. 8.2 can potentially be one of the promising solutions. This solution will

have less number of active power semiconductors than a two-stage topology, implying less failure probability and higher reliability.

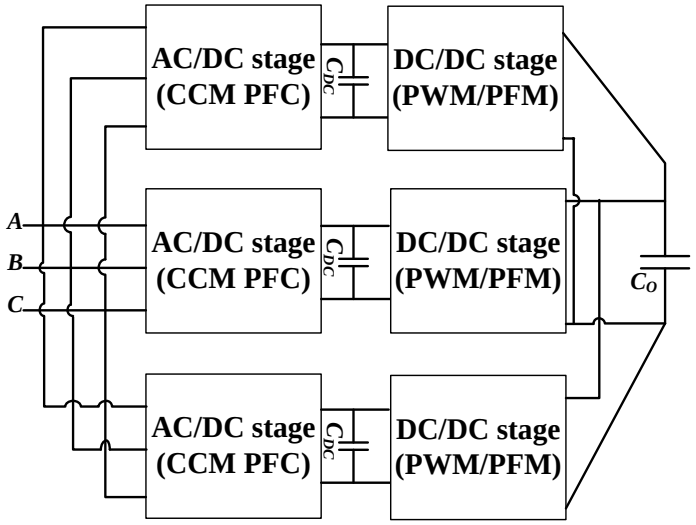


Fig. 8. 1. 3-phase modular RTRU (alternative-1)

Since the currents entering into the three half-bridges contain both line frequency and switching frequency components, the attenuation requirement imposed on the DM EMI filter is higher than a conventional two-stage RTRU with front end CCM PFC. However, matrix converter does not require any boost inductor; so, a comprehensive comparison of magnetics volume and weight between matrix and other two-stage converters could be of great research interest. In order to maintain both unity input power factor and the required voltage gain throughout the AC input swing, the control complexity is expected to be higher than a conventional two-stage topology. The control variables are the duty ratios of the primary and secondary half-bridges and the phase-shift angle between primary and secondary PWMs. One major potential advantage of this topology is feasibility of achieving ZVS in the primary side MOSFETs due to inductive nature of the switching frequency component of current

[185]. However, it is challenging to ensure ZVS in the secondary side MOSFETs throughout the entire AC line cycle and hence, is of important research interest to make this topology suitable for high-frequency RTRU application by incorporating soft-switching.

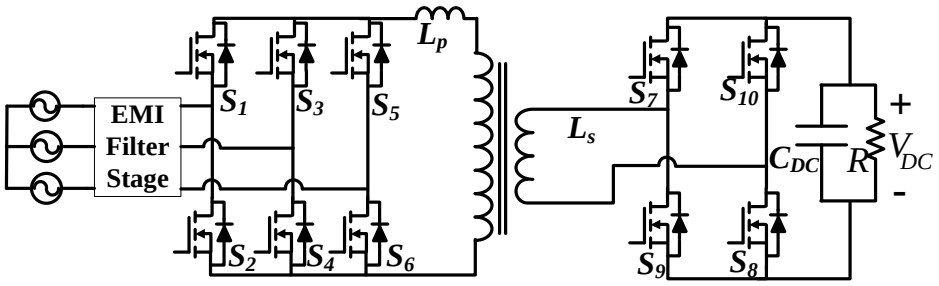


Fig. 8. 2. Three-phase matrix-converter based RTRU (alternative-2)

In order to further improve the modularity even in the case of phase failures, an alternative circuit consisting of three single-phase single-stage AC-DC converter units in parallel at the output can be constructed as shown in Fig. 8.3. One important requirement in the construction is that the AC-DC converter unit has to be galvanically isolated to separate the electrical faults between the input and output sides of RTRU. Also, the isolation must be realized by high-frequency DC-DC transformer in order to reduce the size and weight of magnetic components. One additional requirement is that this topology will require access to the source neutral point of the turbo generator. One prospective circuit topology for single stage AC-DC converter is shown in Fig. 8.4, which is a type of direct-matrix converter [184].

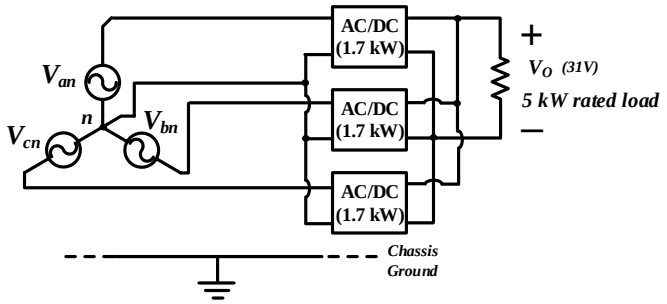


Fig. 8. 3. The proposed converter topology in a 3-phase 5-wire system

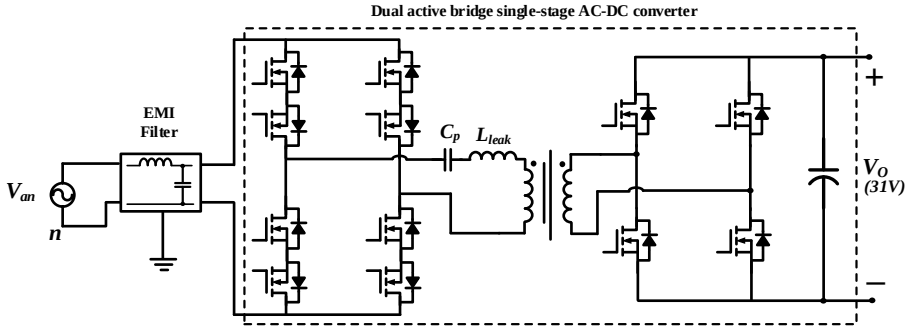


Fig. 8. 4. Schematic showing the converter topology along with the EMI filter (alternative-3)

In this architecture, three line-neutral voltages (i.e. V_{An}, V_{Bn}, V_{Cn}) would be fed as inputs to the three single-phase converters. With a nominal input voltage of 235V phase-neutral RMS, the maximum voltage stress across a device would be the peak input voltage i.e. $235\sqrt{2} = 332$V, which would allow us to utilize GaN MOSFETs of 650V voltage-stress rating. The use of GaN switches allows for higher-frequency operation – shrinking the size of magnetic components in the circuit, while improving efficiency due to improved ZVS performance.

Each of the converters could be designed for a nominal continuous power of 2 kW, which would add up to 6 kW continuous power for the overall three-phase RTRU. However, if a failure occurs in any one phase, the corresponding unit will be taken offline, and the remaining two units will supply 4 kW for a short duration. Thermal

management system for each of these units has to be designed with respect to the power losses at 2 kW load condition.

The proposed converter topology eliminates the high-voltage DC link and achieves PFC action as well as isolation in a single converter stage. The elimination of the DC-link capacitor and the output inductor provide the volume savings required to balance out the extra weight added due to the modular design approach. The low component count and elimination of the DC-link capacitors increases the overall reliability of the system.

Another variant of the topology presented in Fig. 8.5 could be an indirect-matrix conversion, where the primary side of the transformer is realized by a series combination of diode-bridge rectifier and an actively controlled full-bridge structure. There is an AC link of small capacitance at the output of the rectification unit for sinking the switching ripple current. Also, in order to reduce the conduction losses, the rectification can be realized by a synchronous rectification based active full-bridge structure. Although the component count in the direct and indirect matrix converter structures are the same, the gate driver design considerations and switching logic are different in both the topologies.

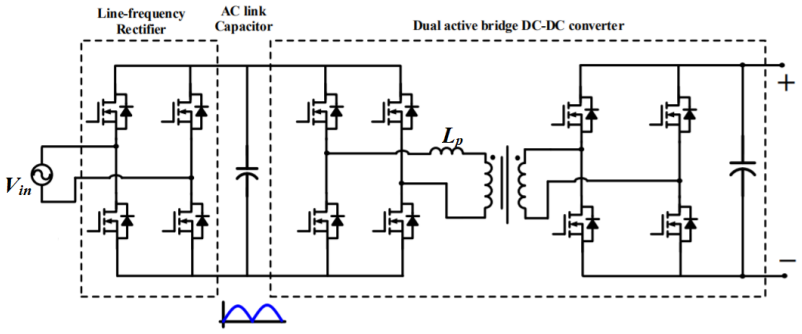


Fig. 8.5. Indirect matrix-based single-stage AC-DC converter topology(alternative-4)

Another alternative of single-stage AC-DC conversion for RTRU applications can be realized using push-pull configuration [185], shown in Fig. 8.6. The RTRU will be designed using the power architecture shown in Fig. 8.3, where the inputs of three such converter units are connected across three phase-neutral terminals and outputs are connected in parallel to provide 28V DC. This converter has the following features: a) galvanic isolation b) bi-directional power flow, c) ZCS turn-off for the primary side switches and ZVS turn-on for the secondary side, d) linear power relationship for easy control implementation, e) unity power factor with open-loop control. Zero Current Switching (ZCS) on the high voltage (low-current) side will lead to reduction in switching losses and improved efficiency. The switching frequency can also be increased, thus reducing the size of the magnetic components considerably. It should be noted that the AC-DC converter with push-pull configuration utilizes two primary windings by saving half of the number of switches in comparison to the full-bridge-based topology in Fig. 8.4, which however uses only a single primary winding.

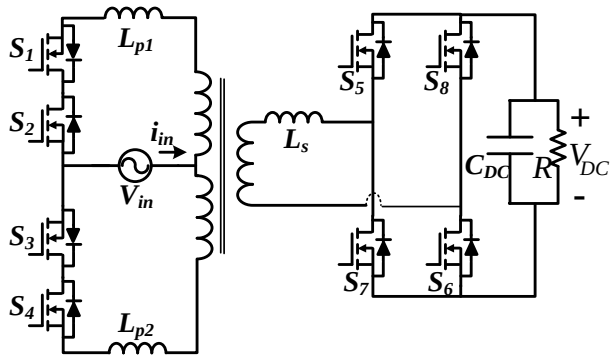


Fig. 8.6. Single-stage AC-DC converter in push-pull configuration (alternative-5)

The alternative modular RTRU solutions can also be realized by two-stage single-phase AC-DC conversion solutions, where the first stage could be continuous conduction mode (CCM)/ critical conduction mode (CRM) PFC and the second stage

could be high-frequency isolated DC-DC converter [186-187], as shown in Fig. 8.7. In order to improve the boost inductor volume, one of the most advanced topology is variable frequency CRM PFC, which also has an additional advantage of achieving ZVS and hence, facilitates to go higher operating frequency. One of the important design challenges is to design the EMI filter stage for a spectrum with multiple fundamental components. The DC/DC stage could be any PWM controlled or pulse frequency modulation (PFM)-based half/full-bridge converter, which could be different variants of CLLC, LLC, dual active bridge (DAB) converters.

In order to maintain the modularity under phase-failure, the first AC-DC stage needs to have access to the neutral point so that three single-phase modules can be constructed, where two units will be operable under the failure of one phase. If the neutral point access is not provided as shown in Fig. 8.8, line-line voltages can be fed as inputs to the single-phase units, where failure of one single phase will make two units inoperable. Also, with an input of 235V AC RMS, the minimum DC link voltage in phase-neutral type input is $235\sqrt{2} = 332$V, which can take the advantages of using GaN MOSFETs. On the other hand, the DC link voltage has to be greater than $235\sqrt{6} = 580$V in case of phase-phase input, which has the only WBG option of using SiC MOSFETs. Furthermore, higher DC link voltage will increase the switching losses but would reduce the conduction losses due to less average current. Therefore, there remains an ample scope for an interesting study of selecting the circuit configuration and DC link voltage level.

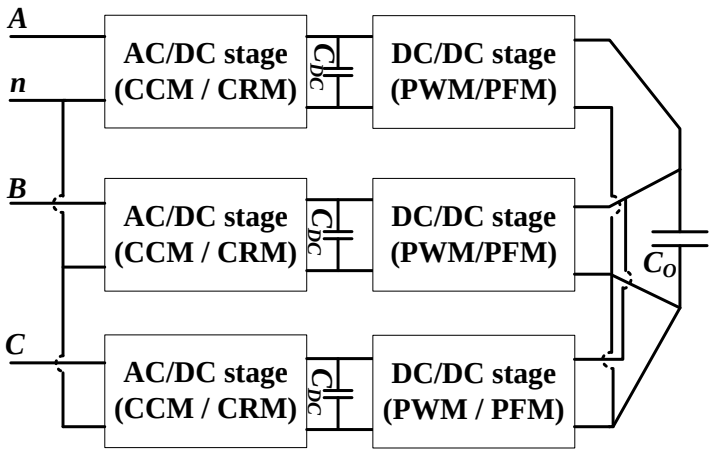


Fig. 8. 7. Two-stage modular RTRU with neutral access requirement (alternative-6)

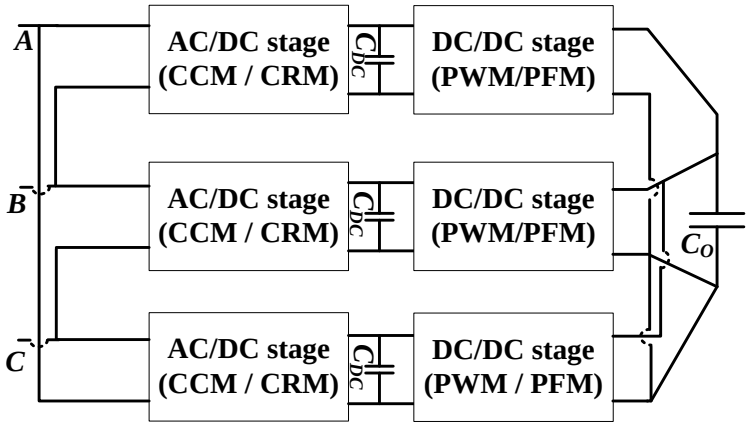


Fig. 8. 8. Two-stage modular RTRU with no neutral access requirement (alternative-7)

Therefore, in a nutshell, future research can be carried out on selection of suitable converter topologies facilitating the emergence of WBG semiconductor power devices and also being able to push the switching frequency higher to further reduce the size of passive components. More extensive investigations need to be performed on modes of circuit operation, implementing soft-switching so that operating frequency can be made higher without affecting the power loss. While improving the circuit structure, the research will need to focus on implementing advanced control techniques to improve the system dynamics during load/line transients, enrich the power quality and improve the disturbance immunity.

8.2.2. Power electronic optimization of RTRU

As a part of the systematic and comprehensive design procedure, it is crucial to develop a multi-objective optimization routine for different performance metrics such as efficiency, volume, reliability and cost using accurate component models and data. The optimization routines consider different converter topologies and component choices, and the reliability aspects in both the component level and system level, which represent important decision variables. Moreover, such multi-objective optimizations can lead to a complex problem formulation and thus require considerable solving effort, which may be further looked into by applying different machine learning-based approaches.

Prior to starting the optimization process, all the variables/parameters should be categorized into two parts: (i) design space, and (ii) performance space. The interests of consumers or customers will be concentrated majorly on the performance space; on the other hand, the system designers can only alter the design space parameters in order to satisfy the performance demand. Performance space variables include power factor (PF), efficiency (η), power density (ρ), weight, reliability (σ); whereas, the design space consists of values of passive (L, C, transformer) components, device specifications, thermal management specifications (i.e. number of heatsink fins, fluid flowrate, heatsink volume), DC link voltage, etc.

Based on the selected RTRU topology and design space parameters, the resulting current and voltage waveform expressions are developed for each component, which should then be used to optimize the EMI filter, DC link capacitor, output inductor, and the high-frequency transformer. In the Pareto optimization, all available degrees of

freedom, i.e. all design space variables (passive component values, DC link voltage, turns ratio) are considered. Then each component needs to be optimized independently with an iterative temperature/loss calculation, in order to take the temperature dependent losses into account.

The performance gain achieved by using the optimization procedure would vary with design specifics, but nonetheless is a significant step towards a more systematic design approach for power electronic converters and hence, is of immense research interest for future designs demanding for strict performance requirements of RTRU.

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