ABSTRACT

Title of Thesis: REMAINING LIFE ASSESSMENT
PROCESS OF ELECTRONIC SYSTEMS

Vidyasagar Shetty, Master of Science, 2003

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The remaining life assessment (RLA) process is a reliability prediction process, which predicts amount of life left in a system. Remaining life assessment is performed on hardware, which has already seen operational life. This thesis details the remaining life assessment process in detail and also provides a case study of remaining life assessment performed on the Shuttle Remote Manipulator System (SRMS). The electronics of Shuttle Remote Manipulator System was designed in the 1970s with a target application life of ten years. They have performed without any failures for over 20 years. The remaining life assessment process was done to investigate if the life of the SRMS could be extended until the year 2020. The remaining life assessment concluded that the electronics could

be extended until 2020 due to the robust design and lack of damage caused to the assemblies.

REMAINING LIFE ASSESSMENT PROCESS OF ELECTRONIC SYSTEMS

by

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1 Background and Motivation

Maintaining the reliability of electronic products is a major concern for companies because the failure to do so can lead to huge financial losses. For e.g., Toshiba corp. agreed to a $1.1 billion settlement for allegedly selling defective laptop computers in the U.S., the first fallout from a wave of lawsuits and government inquiries over a flaw that may be common to the products of many major computer makers1. This thesis is an attempt at improving the reliability process by developing a reliability prediction process called Remaining Life Assessment (RLA). The Remaining Life Assessment (RLA) process is a reliability prediction process, which predicts amount of life left in a system. Remaining life assessment can be done on systems, which have seen a considerable amount of life. This thesis presents the RLA approach through the case study of the RLA of Space Shuttle Remote Manipulator System (SRMS). The RLA process can help in the improving the reliability of electronics systems by being able to detect failures and causes of failure that would occur in the systems exposed under certain life cycle conditions. The remaining life assessment process is to certain extent a derivation of PoF process developed and used by CALCE. The Computer Aided Life Cycle Engineering (CALCE) Center at the University of Maryland developed a PoF approach for electronic product qualification and accelerated testing in the early 1990s. The PoF approach utilizes knowledge of the life-cycle load profile, package architecture, and material properties in identifying potential failure mechanisms and provides a rational method of analysis and testing to predict expected life cycles in the field application (1-5). Physics of failure (PoF) supplies the link between failures under normal use conditions and the failures taking place during the accelerated tests. PoF establishes a qualitative and quantitative

relationship between the particular failure mechanisms, the product properties, and environmental conditions.

All the research for the project (RLA of SRMS) has been performed in CALCE-UMCP (University of Maryland College park). The sponsor of the project was MD Robotics (MDR), Canada. All the information about SRMS has been provided by MDR.

1.1 Space Shuttle Remote Manipulator System

This section introduces the case study material i.e. Space Shuttle Remote Manipulator System (SRMS, Figure 1-1). Since its maiden voyage aboard U.S. Space Shuttle Columbia in 1981, the Shuttle Remote Manipulator System (SRMS), known as Canadarm, has demonstrated its reliability, usefulness, and versatility and has provided strong, yet precise and delicate handling of its payloads. Canadarm was designed, developed and built by Spar Space Systems Robotics operation, now MD Robotics under contract to the National Research Council of Canada. The first arm was Canada's contribution to NASA's Space Shuttle Program. Subsequently, NASA ordered four additional units. Canadarm has performed flawlessly for 20 years; placing satellites into their proper orbit and retrieving malfunctioning ones for repair. Perhaps its most notable mission was the repair of the Hubble Space Telescope. Canadarm was used as a mobile work platform for astronauts during numerous space walks required to repair the faulty telescope. Canadarm played a critical role retrieving the satellite, placing it in the cargo bay for repairs, and then re-deploying it. Unplanned exercises for Canadarm have included knocking a block of ice from a clogged waste-water vent that might have endangered the shuttle upon re-entry, pushing a faulty antenna into place, and successfully activating a satellite that failed to go into proper orbit. In December 1998 Canadarm played a critical role in the first assembly mission of the International Space

Station, mating the U. S. Unity node to the Russian-built Zarya. Canadarm will continue to play a vital role in the assembly of the space station. The Shuttle Remote Manipulator System consists of a shoulder, elbow and wrist joint separated by an upper and lower arm boom. The shoulder joint has two degrees of freedom, the elbow joint has one degree of freedom, and the wrist joint has up to three degrees of freedom. At a total weight of approximately 905 lbs., the Canadarm has recently been upgraded to maneuver payloads of up to 266,000 kgs. (in the weightlessness of space). Canadarm uses an end effector with a specially designed grapple fixture to place payloads in orbit.

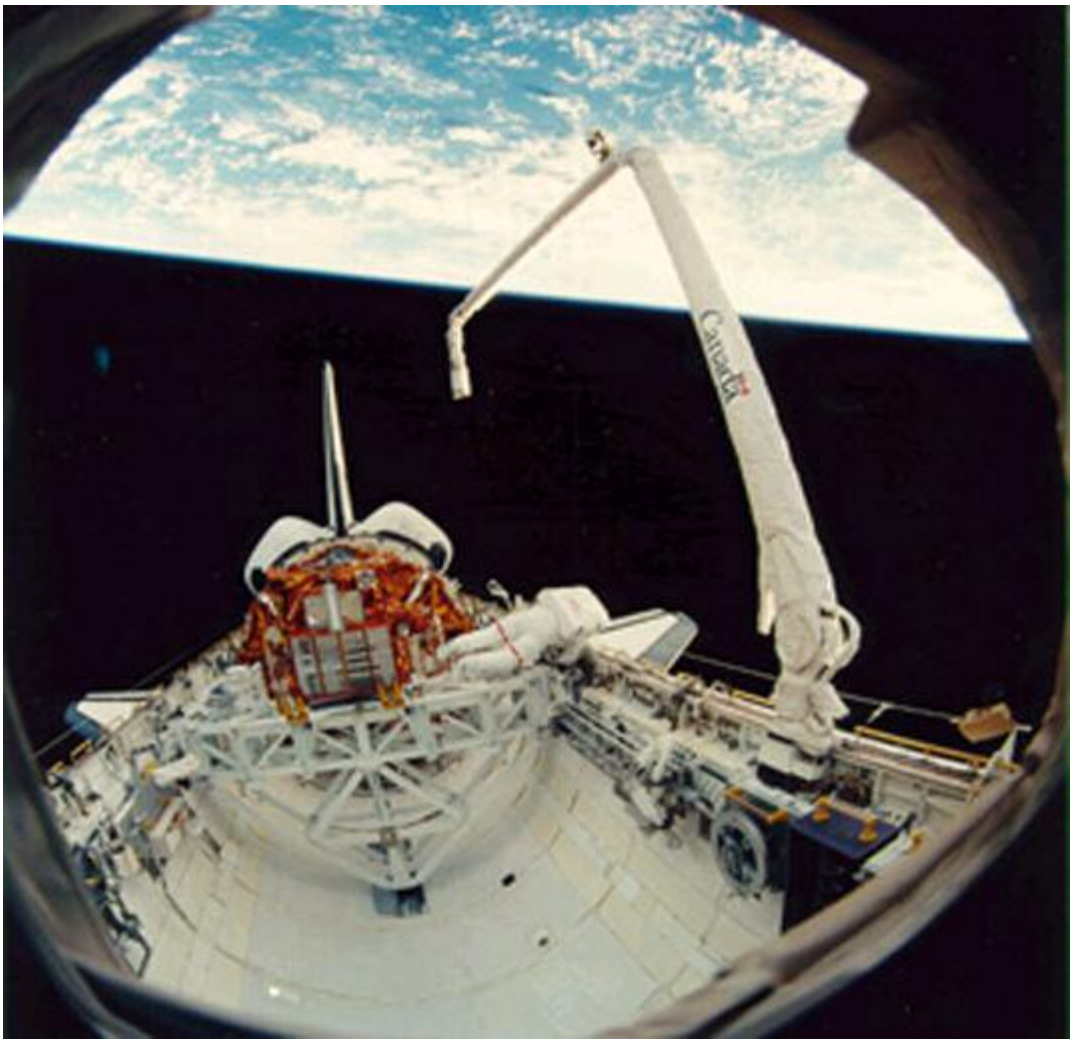


Figure 1-1: SRMS

1.2 Why RLA of SRMS and hardware chosen for RLA

The successor to the Space Shuttle, the second-generation Reusable Launch Vehicle (RLV), is not expected to be ready before 2020 and hence NASA hopes to extend the usage of the Space Shuttles into the year 2020. NASA has asked its major contractors to conduct remaining life assessment of the key components of the Space Shuttle, since MDR manufactures SRMS it was asked to do the RLA of SRMS.

Figure 1-2 shows the physical hierarchy of the SRMS. There are many systems and sub systems in the SRMS as observed from the physical hierarchy diagram. Since it is not possible that all the systems be analyzed for RLA. The EEEU was chosen as a

representative of the remaining life of the SRMS. The EEEU was chosen because boards in the EEEU experience the most harsh of all environmental conditions and they had the highest number of components per boards. However the EEEU units are still being used in the SRMS and hence physical analysis step of the RLA couldn't be performed. Hence as a physical representative of EEEU, SPA unit was chosen.

Similarities between the SPA and EEEU are:

- ③ SPA boards are similar to EEEU in terms of board layers (same number of layers and board materials), components, size, and exposure to similar testing (thermal, vibration) conditions.
- ③ The EEEU and some of the SPA units are in close proximity to each other in the SRMS, therefore the life cycle loads that contribute to damage to the boards affect both similarly.
- ③ The two units were designed and manufactured at the same time using same design rules and following the same standards.
- ③ The test schedules for the two units are similar.

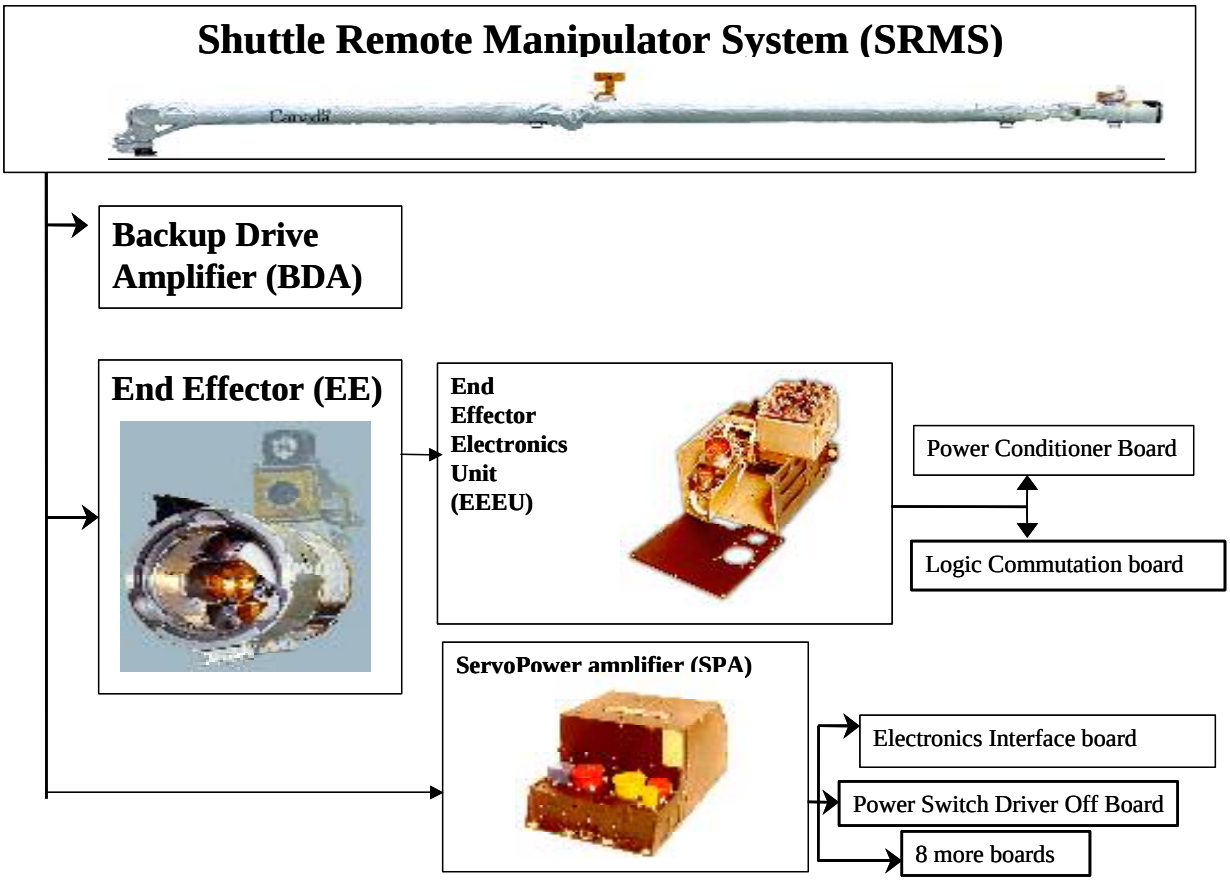


Figure 1-2: Physical hierarchy of the SRMS

2 Steps In Remaining Life Assessment Process

2.1 Physical analysis of assemblies

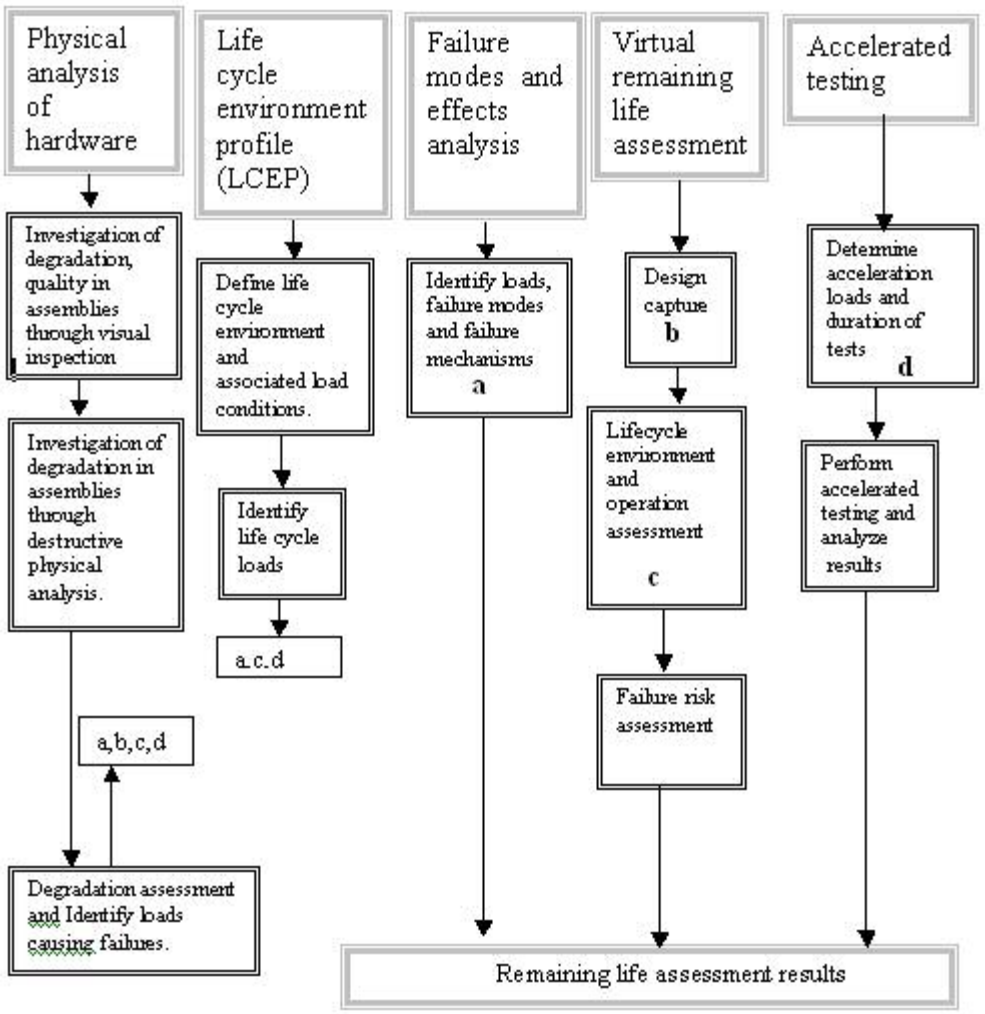
Physical analysis is the first step of the remaining life assessment process, as required by the RLA process the hardware available for physical analysis, needs to have been in operation for a certain period of time. The hardware may be present either in the form of a complete assembly or just the boards may be available for analysis. In the event of the presence of a assembly, first a tear down has to be performed and the boards have to be separated out. The tear down process has its importance in the fact that it is possible to analyze the working dimensions and tolerance and based on teardown experience it is possible to make improvements for future designs. Physical analysis gives an opportunity to evaluate other damages and deteriorations that may be caused by the environmental effects not accounted for in simulation processes. Tear down, visual inspection and destructive physical analysis formed the part of physical analysis process step of RLA.

2.1.1 Investigation of degradation, quality in assemblies through non destructive means

After the tear down is performed on the assembly visual inspection is performed on the boards. The visual inspection process helps to identify externally observable anomalies. Visual inspection may be performed by the naked eye or with the help of an optical microscope or sometimes an X-ray microscope. Visual inspection helps in identifying failures like large cracks ,voids or wiredebonding which are evident. E.g., the lead frame stamping process leaves residual stresses and sharp blurs that act as stress concentrators.

2.1.2 Investigation of degradation in assemblies through destructive physical analysis

Destructive physical analysis is done on boards to detect internal anomalies. Destructive physical analysis can only be performed after it is made sure that the visual inspection process is complete and all the external anomalies are detected.



2.1.3 Degradation assessment and identify loads causing failures

Based on the external and internal anomalies observed, it is possible to characterize if the anomalies occurred during manufacturing or during operation. A reverse engineering type of approach can be done to investigate anomalies and find out the loads that are responsible for the anomalies.

2.2 Life cycle environment profile (LCEP)

To investigate the cause of failures that occur during the life cycle of the electronics it is imperative to accurately characterize that the stress loads experienced during its life. Through the development of accurate Life Cycle Environment Profile (LCEP) based on

the events that take place in the life of electronics it is possible to identify loads, which act on the electronics. A life cycle environment profile (LCEP) is a forecast of events and associated environmental conditions that equipment will experience from manufacture to end of life. A life cycle environment profile helps to identify all possible load combinations so that the stresses acting on the product can be identified and can be incorporated in the product's design, test and qualification process to ensure the reliability of the electronic equipment for its entire life. Past research describes the need for life cycle analysis of electronic products in order to ensure product reliability[3]-[6]. The failure modes and mechanisms can be identified for each load which helps in improving the design by providing safeguards against failures for present systems and designing for better reliability in future systems. Environmental loads corresponding to manufacture and assembly, testing, handling, shipping, storage before and/or between usage, operation and rework are accounted for in the LCEP.

Importance of creating a LCEP is:

- Design engineers faced with the task of effective design need to provide safeguards against failure causing loads. LCEP can help identify the failure causing loads.
- Reliability Engineers encountering failures would like to get to the root cause of problems to weed them out. LCEP can identify life-threatening loads and from the loads it is possible to identify the failure modes and mechanisms. A comparison can be made of the failures observed with anticipated failures and hence root cause of failures can be identified.

- Not all environments merit consideration in determining the reliability of each product many are below the practical threshold for each part because the environment are sufficiently benign or because the inherent characteristics of the product are not susceptible to the stresses associated with the environment. Through LCEP it is possible to estimate the potential damage which can be caused by each load. E.g., Space electronics may be stored for long periods under benign temperatures which may have no effect on the electronics.
- If a LCEP is prepared for a particular system, then the same LCEP can be used for qualifying other systems manufactured in the future. E.g., A LCEP created for space electronics may show high operational temperatures. Using this temperature profile it is possible to qualify future space electronics by making them undergo testing at the temperatures and also providing safeguards. Hence the electronics used in the future are more reliable than previous ones.

The steps in developing an LCEP are as follows:

2.2.1 Define life cycle environment and associated load conditions

Describe the expected events occurring from manufacture to end of life. This step called as the LCEP step. For example, in the case of a space shuttle , these events or phases include assembly, qualification, , transportation to launch site, storage at the launch pad, launch, operation and rework. The entire life cycle of the electronic product should be separated into the key phases or events. The events are generally decided based on the commonality of loads acting on the system for a particular duration.

2.2.2 Identify life cycle loads

Identify the significant loads (temperature, vibration) from LCEP. Identify failure modes and mechanisms for each load. Use the listing of the failure modes and mechanisms as

a means for improving reliability. For e.g., during qualification testing the space assemblies are subjected to temperature cycling. During temperature cycle testing, products are held at cold temperature long enough to establish temperature stabilization and appropriate creep and stress relaxation of materials. Following this cold dwell materials are heated to the hot dwell where they remain for another minimum time period. The dwell at each extreme and two transition times constitute one cycle. Common failure modes include parametric shifts and catastrophic failures; common failure mechanisms include wirebonds fatigue, cracked or lifted dies, and package failure.

2.3 FMEA

A FMEA is a qualitative technique for determining and listing the possible failure modes, by which the product may fail. FMEA involves an analysis of the system to determine the effect of component or subsystem failure on the overall performance of the system and on the ability to meet performance requirements or objectives [42]. Based on the captured design and loading conditions, the possible failure modes and mechanisms are identified. A literature search or knowledge from similar existing products can aid in identification of possible mechanisms and modes. A FMEA is generally constructed in a table format. The major components or subsystems of the product are listed in the first column. The physical failure modes for each component are listed in the second column. In the third column the possible failure mechanisms are identified for each respective entry in columns one and two. The effects of the failure on the product are listed in the fourth column. Additional columns containing failure probability, criticality, or alternative failure ranking, determined from previous product knowledge, may be included for a more quantitative analysis. Likewise, columns listing symptoms or

methods of failure detection may be listed to help identify specific failure modes and mechanisms. For example, an FMEA of surface mount components assembled to a PWB under temperature cycling, may identify an electrical open as a failure mode due to thermomechanical fatigue mechanism.

2.4 Virtual remaining life assessment

Virtual remaining life assessment is performed to determine the remaining life at the circuit card assembly level. Virtual remaining life assessment is basically a simulation process where electronics are simulated under various life threatening loads . Software that can be used for VRLA are ansys, abacus, calcePWA etc.

2.4.1 Design Capture

Design capture is the process of identifying and documenting geometrical, material, and mounting information to generate a model of the physical hardware. Design capture involves evaluating the electronic system at all hierarchies (e.g., enclosure, circuit cards, parts, physical interfaces) based on the objectives of the assessment. Each individual component of the CCA is characterized by a set of geometrical and material parameters by the hardware capture and material identification and properties. Geometric data for a product is generally defined by the product's manufacturer by means of design drawings or electronic design files. Information may be obtained from the manufacturer, conducting reverse engineering, or by making reasonable assumptions based on literature and prior experience. Information such as component and interconnect geometry, circuit card geometry, and mounting conditions are needed for a model of the hardware. The identification of materials used in the construction of the electronic product is needed to understand the behavior of the materials and their failure response when subjected to loads in PoF. The material properties define how a material will react and degrade due to

loads applied during manufacture, assembly, storage, transportation, installation, rework, and operation.

2.4.2 Life cycle environment and operation assessment

Environmental and operational loads are applied to models of the product, created from the hardware capture, to determine the maximum stress areas in the product. During the stress assessment, the global loads experienced at the system level, are transformed to local loads throughout the product. The local loads are used to determine the potential failure sites. Te damage assessment utilizes the local loads (e.g., temperature at a component, curvature of the PWB below a component) found in the stress assessment and determines the time-to-failure of each failure site based on the failure mechanisms of interest. Since the same load can excite more than one failure mechanism, damage models representing the various mechanisms are used to estimate the time-to-failure for each failure mechanism. Likewise, multiple loads may excite the same failure mechanisms; therefore load interaction toward a failure mechanism must be considered when conducting the damage assessment. Models representing multiple load interactions should be used when available, even when a model is not available, the product's response to the multiple loads must be identified.

2.4.3 Failure Risk assessment:

Each failure site is ranked in terms of time-to-failure based on the results of the damage assessment for each failure mechanism in the life assessment. An initial reliability assessment is made based on the shortest time-to-failure.

2.5 Accelerated testing

Accelerated testing is conducting to cause the life aging process of products to occur at a rate faster than would be obtained under normal operating conditions. The steps involved in accelerated testing include the following:

1. Determine acceleration loads and duration of tests
2. Perform accelerated testing and analyze results

Care must be taken in specifying the accelerated conditions so that the failure modes and failure mechanisms are neither introduced nor removed. Excessive acceleration of a failure mechanism may trigger a failure mechanism that that may be dominant at service loads. This failure mechanism shifting may provide misleading service life predictions. Each stress may also cause multiple failure mechanisms to be accelerated with different sensitivities. For e.g., Temperature accelerates electromigration, ionic contamination and surface charge spreading but at different rates. Conversely a particular failure mechanism may be activated by multiple stresses. For e.g., corrosion is accelerated by temperature and humidity. In light of these complexities accelerated testing should not be employed without a thorough understanding of how the test correlates with service conditions. Table 2-1 gives examples of failure mechanisms and acceleration parameters.

Table 2-1: Failure mechanisms and acceleration parameters

Failure mechanisms	Acceleration parameters
Failure crack initiation	• Step load or displacement • Thermal shock
Fatigue crack propagation	• Cyclic load displacement and temperature
Diffusion	• Absolute temperature • Concentration gradient
Interdiffusion	• Absolute and cyclic temperature
Deadhesion and delamination	• Absolute temperature • Relative humidity

	• Contaminants
Corrosion	• Absolute temperature • Relative humidity • Contaminants
Electromigration	• Current density • Absolute temperature and temperature gradients
Electron-hole pair generation	• Radiation and dose rate
Popcorning	• Relative humidity followed by thermal shock

2.5.1 Determine acceleration loads and duration of tests:

Based on the dominant failure mechanisms and the critical failure sites found in the physical analysis and virtual remaining life assessment, environmental loads are selected that will precipitate the mechanisms. The environmental loads needed for accelerated testing will dictate the type of environmental testing equipment needed. For the accelerated test, failure needs to be defined based on the objectives of the test. Failure can be defined when an electrical parameter (i.e. voltage, resistance, current) is beyond specification or when the product ceases to operate (i.e. electrical open). A parameter that is beyond specification may be caused by an intermittent failure, where the product continues to operate but cumulative effects will grow to until the product ceases to operate. A failure that causes the product not to operate occurs when the stress level exceeds the threshold product strength. Examples of the threshold strengths are the tensile strength of a brittle material or the temperature level at which a component begins to malfunction. The failure detection scheme chosen for the testing need to be able to detect the defined failure. Failure detection and monitoring schemes need to be developed for the notification of a failure. The failure detection scheme should be able to monitor the critical failure sites and their likely failure modes. Characterizing the product response over the accelerated test loads enables insight into the interaction effects

between the applied environmental loads. The specimen characterization enables a prediction of the response of the specimen under accelerated test loads. If the loading profiles of the overstress test are similar to the selected test loads then the data for the specimen response characterization can be collected over the entire accelerated load range of the overstress test.

2.5.2 Perform accelerated testing and analyze results:

The test specimens are exposed to the accelerated tests. Monitoring of the test specimens during accelerated testing provides a time-to-failure. The test failures should be documented by recording when, where, what, the load level, and pictures of the failure. Each test failure should be analyzed to determine the root cause failure mechanism. The precipitated failure modes and mechanisms of the accelerated tests should correspond to the failure modes and mechanisms predicted to occur..A reliability assessment is made based on the test results and the objectives of the product assessment. A failure free operating period, failure rate, or mean time to failure may be found by statistical analysis given enough samples and the test objectives. The acceleration factor calculated in section can be used to quantitatively extrapolate a time-to-failure from the accelerated test environment to the field application environment. The assessment can serve the purposes of customer confidence, product development decisions, risk identification, warranties, and certification and regulatory concerns.

3 Physical Analysis of Assemblies

3.1 Investigation of degradation, quality in assemblies through nondestructive and destructive means

3.1.1 Disassembly and boards for inspection

Disassembly was performed on one of the Analog Servo Power Amplifiers. Physical analysis was performed on two of the circuit card assemblies (CCAs), identification numbers 2559013 and 2559022, which were removed from the module (see Figure-Figure 3-1-Figure 3-3), during the complete teardown of the unit.

Table 3-1: Board Identification

Board	Identification Number	Name of CCA	Analysis
1	2559013	Power Switch Driver "OFF" Board Subassembly	Visual inspection
2	2559022	Electronics Interface Board	Visual inspection

During the teardown, the following observations were made:

- Irreversible fasteners were used to secure assembly
- Conformal coating covering the boards and components
- Wires were bundled together and attached to the board with adhesive; no damage was observed
- Adhesive was also used to secure the parts to the boards
- There was limited physical working dimensions

Inspections were performed in accordance with:

- MSFC-STD-136 (June 11, 1971) Parts Mounting Design Requirements for Soldered Printed wiring Board Assemblies 11, and

- NASA-STD-8739.2 (August 31, 1999) Workmanship Standard for Surface Mount Technology, Chapter 12 12.
- IPC-A-610 (Revision C, January 2000), Acceptability of Electronic Assemblies [4]; Class 31
- ANSI/IPC-A-600 (Revision E August 1995), Acceptability of Printed Boards, Chapter 2 8

The inspections investigated the boards, components, and interconnections. These included:

- Board edges
- Base material
- Solder joints, connector pins
- Plated through holes
- Solder resist
- Dimensional characteristics
- Coatings
- Component damage
- Bow and twist
- Component mounting/securing

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[1] It was assumed that this product is Class 3 (IPC-A-610 Revision C, January 2000) therefore; acceptance and conformance were based on this classification.

Class 3 – High Reliability Electronics Products; Includes the equipment and products where continued performance or performance-on-demand is critical. Equipment downtime cannot be tolerated, and the equipment must function when required, as in the case of life support items or flight control systems. Assemblies in this class are suitable for applications where high levels of assurance are required, service is essential, or the end-use environment may be uncommonly harsh.

3.1.2 Low Magnification Visual Inspection

Based on Table 3-2 10, (Table 1-2 Inspection Magnification in section 1.8 Magnification Aids and Lighting, of IPC-A-610 Revision C, January 2000) along with the statement from MDR that the land widths are 0.030 inches, a magnification of 4X should be used (see highlighted section in table below). Each of the two boards was inspected using hand held illuminated magnifiers of 5X magnification. A low magnification stereoscope (15 – 60X) was used for areas of interest where it was determined that higher magnification was needed.

Table 3-2: Inspection Magnification

Land Widths or Land Diameters	Inspection Magnification Power	Referee Magnification Power
>1.0 mm [0.039 in]	1.75X	4X
0.5 to 1.0 mm [0.020 to 0.039 in]	4X	10X
0.25 to 0.5 mm [0.00984 to 0.020 in]	10X	20X
<0.25 mm [0.00984 in]	20X	40X

3.1.3 Board Inspection

(note that the boards are covered with conformal coating, hence observations are made through this covering)

At 5X magnification, the assemblies were checked for:

- Surface imperfections such as burrs, nicks, cut fibers, weave exposure or voids in the boards
- Conformal coating coverage
- Solder mask quality

- Subsurface imperfections such as foreign inclusions, measling/crazing, delamination between layers of the base material and/or between the base material and metal cladding, or laminate voids
- Imperfections in the conductive circuitry such as reduction of conductor width or thickness due to nicks, pinholes, or scratches
- Visible discoloration due to corrosion, contamination, overheating or electrical overstress (EOS) damage
- Isolated metal particles
- Board warpage (IPC-TM-650, number 2.4.22, procedure #1) using a flat glass plate and ceramic plated to elevate the sample so that it is supported only by the edges (see Figure 3-4 and Figure 3-5). % bow = (0.085 -0.07)/5.1 = 0.3% for board identification number 2559022. The specification specifies a maximum of 1.5%. For the other board, identification number 2559013, the % bow was 0.4%.

The results of the board visual inspection yielded no criteria for rejection in the above areas examined.

3.1.4 Dimensional Characteristic Compliance

After 20 years of storage/use, based on the assembly drawings supplied by MDR (2559013.pdf 6and 2559022.pdf 7) for the two boards on which visual inspection was done, physical dimensions (as given in the layout and board drawings) that could be measured, were within the specified tolerances. Measurements for the conductor spacing (minimum: 0.027 inches), conductor width (minimum: 0.022 inches), plated-through-hole (PTH) diameter (inner diameter: 0.032 inches) and lead diameter (0.02 inches) were all in compliance with the guidelines in MSFC-STD-136 11.The specification states that

component hole diameter shall be a maximum of 0.015 inches larger than the nominal component lead diameter. Using the measurements for the conductor spacings and metallization width (not thickness), and PTH and pad external dimensions. Plated-through-hole diameter (0.032 inches) minus the lead diameter (0.02 inches) is equal to 0.012 inches. This complies with the specification of < 0.015 inches. Minimum spacing between adjacent conductors for conformally coated boards shall be 0.0003 inches/peak volt. Based on our measurements, conductor spacing (minimum – 0.027 inches), these boards can withstand a peak of 0.027/0.0003 = 90 volts. The solder pads for the surface mount components all appear to be longer than twice their width (see Figure 3-6). Some of the PTHs in board 2559013 did not have annular rings on the component side. The fillets of the solder joints on the component side of the board would be smaller compared to the joints on the other side where there are annular rings (cross-sectioning needed to clearly view this). A picture is included in the board DPA report subsection.

3.1.5 Component Inspections[1]

From an external view, no anomalies were noted on any of the components inspected on the four boards. It was noted that some of the components were bent at the leads to accommodate limited space in the vertical direction (see Figure 3-7). In accordance with NASA-STD-8739.2, Chapter 12 – Quality Assurance Provisions, and MSFC-STD-136, inspections were conducted in the following applicable areas:

Solder Paste Application (visual observation of location, amount, and alignment of solder with respect to pad, reject criteria given in paragraph A below)

- Part Alignment

[1] note that the components are completely covered with conformal coating, hence observations made are through this covering

- Part Appearance
- Soldered Interconnections

The results of the visual inspection yielded no criteria for rejection in the above areas examined.

The reject criteria are as follows:

- Solder paste application
- Solder paste bridging between lands
- Isolated solder paste
- Void in the solder paste (only external)
- Solder paste misalignment that covers more than 25% of the open area between lands
- Smeared solder paste bridging conductors

Part Alignment

- Piggy-backed or stacked parts
- Chip parts have lateral overhang more than 25 percent the width of the part or inside overhang more than 50 percent of the end termination width
- Chip part tilting exceeds 25 percent of part thickness

Part Appearance

- Improper tinning of part leads.
- Part improperly supported or positioned (polarity, centering, planarity).
- Part damaged (especially cracks in ceramic parts).
- Cut, nicked, stretched, or scraped leads exposing base metal (except smooth impression marks resulting from bending tool holding forces).

- Flux residue.
- Improper positioning of leads to solder pad for lap terminations.
- Improper lead bending and cutting.
- Spliced part leads.

Soldered Interconnections

- Cold solder connection.
- Overheated solder connection.
- Fractured solder connection (externally visible)
- Poor wetting.
- Blowholes, and pinholes
- Insufficient solder
- Splattering of flux or solder on adjacent areas
- Contamination (e.g., lint, flux, dirt).
- Dewetting.
- Non-wetting.
- Dull or frosty appearance.
- Solder scratches.

For impact of these defects, refer to Solders and Soldering, Fourth Edition, written by Howard H. Manko 15.

3.1.6 Non operating Failure Mechanisms

These failure mechanisms are to be considered during storage and non-powered Ferry Flight and ground transportation. See “Long-Term Non-Operating Reliability of Electronic Products” 14 for more details. It has been noted by MD Robotics that the

assemblies are stored in climate controlled atmosphere where they are free from contamination, corrosive gases, radiation, shock and vibration. The temperature and humidity is kept under strict control. There are no specific recommendations regarding how long a printed board can be stored, or specific recommendations on temperature and humidity requirements for optimum storage conditions 13. The non-operating failure mechanisms examined are described.

3.1.6.1 Corrosion

Corrosion is defined as the chemical or electrochemical reaction of a metal with the surrounding environment. The continuation and rate of the corrosion process depend on the nature of the corrosion product. Conditions that accelerate corrosion include relative humidity, high temperatures, high contaminant concentrations, and the presence of dirt or dust, which can hold more moisture on the surface of the metal. Of these factors, relative humidity is the most important. Rapid acceleration of corrosion occurs beyond a critical value of relative humidity Corrosion also becomes more acute as product metallization tracks become narrower, and the separation between metallization tracks becomes closer. Since the boards and components are conformally coated, and no pits or nicks were observed during the visual inspection, it would be difficult for moisture to get to the metallic areas. Also, the metallization tracks on the boards are relatively large (0.03" compared to 0.003"[9]) and also widely spaced. These make failure due to corrosion unlikely.

3.1.6.2 Shock and Vibration (also addressed by VQ)

Shock and vibration are common accelerators of failure. The most frequent vibration-induced failures include flexing of leads and interconnects and the dislodging or damaging of parts and structures, or foreign particles in electronics. The degree of failure

generally depends on the natural frequencies, deflections, and mechanical stresses within components and materials produced by the shock and vibration environment. If the mechanical stresses so produced are below the acceptable long-term safe working stress of the materials involved, failures should not occur acceptable safe levels. Non-operating vibration levels during storage, Ferry Flights, and ground transportation are not significantly large or long-lasting when compared with launches or vibration tests. Since all of the components, wires and the majority of the fasteners are secured by solithane adhesive, damage from shock or vibration in the storage environment is unlikely. The effects of the solithane are not addressed in the virtual qualification, but would make things better (more secure parts).

3.1.6.3 Thermal

According to MDR, in a year's period approximately 356 days are spent in storage, which amounts to a period of 7120 cycles for 20 years and the temperature ranges from 27 to 17 °C. Approximately once every 3 missions, a Ferry Flight occurs over a 7 hour period with a temperature ranges from –40 to +35oC. The main failure mechanisms due to temperature excursions include fatigue and fracture of various package components, which occur primarily as a result of mismatches in the coefficients of thermal expansion (CTE) of the various materials that make up the assembly. This is covered in the virtual qualification section.

3.1.6.4 Electrical

Although perhaps not readily apparent, non-operating electronics can be subject to significant electrical failure mechanisms. While electrostatic discharge (ESD) is the most common in storage/dormancy environments, electrical failure can also be caused from

static charging of dust particles and organic vapors. Since the metal traces on the boards are relatively large, 0.03 inches compared to 0.003 inches (the state of practice in 2000) the possibility of damage due to ESD is negligible since the charge is distributed uniformly over the conductive trace – the larger the trace, the smaller the charge density. For the components, although the visual inspection did not reveal any anomalies, electrical testing is necessary to verify their integrity.

3.2 Key Findings and observations:

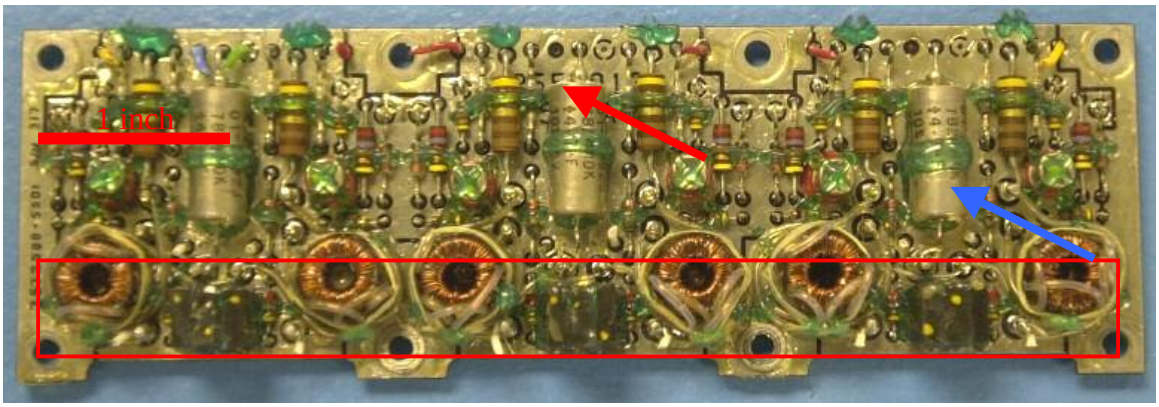
None of the two visually inspected boards had anomalies based on the acceptance criteria of standards: IPC-A-610 (2000), ANSI/IPC-A-600 (1995), MSFC-STD-136 (1971), and NASA-STD-8739.2 (1999). There is no observation, which would suggest a decrease in the expected life. Based on the observations during the teardown, in addition to the visual inspection observations, reworking the units is not recommend because:

- ③ The units are difficult to reassemble (screws, bolts and nuts hold the units together in such a way, that once taken apart, it is tough to reassemble them due to limited physical working dimensions). Since each unit may be assembled differently, "teardown procedure" as given by MD Robotics, may not be applicable to all units.
- ③ The wires and components, in particular transformers and transistors, on the boards are secured with an adhesive, which makes it difficult to remove them.
- ③ Based on the visual inspection, the PWB assemblies are robust and would probably not suffer from failure mechanisms normally incurred during storage such as electrostatic discharge (relatively large metallization lines and conductor spacing) corrosion due to moisture ingress (no defects in conformal coating which covers the board and components), fatigue or cracking due to thermal excursions

(no cracks, chips or nicks observed on board, parts or interconnections), and damage from shock and vibration (due to how the parts and boards are secured) .

3.3 Conclusion

From the visual inspection, no anomalies for the specified areas, were noted in any of the components or boards. These boards are of good quality, as seen by the external examination. The spacing and widths of the pads and traces are relatively large, making the PWB assemblies virtually immune to electro-chemical failure mechanisms. Also, the intact and complete coverage of the conformal coating will help to ensure that no moisture gets in to start contamination which could lead to corrosion. Note that this inspection is only external, and does not address parameters that may be examined during destructive physical analysis (DPA).



A

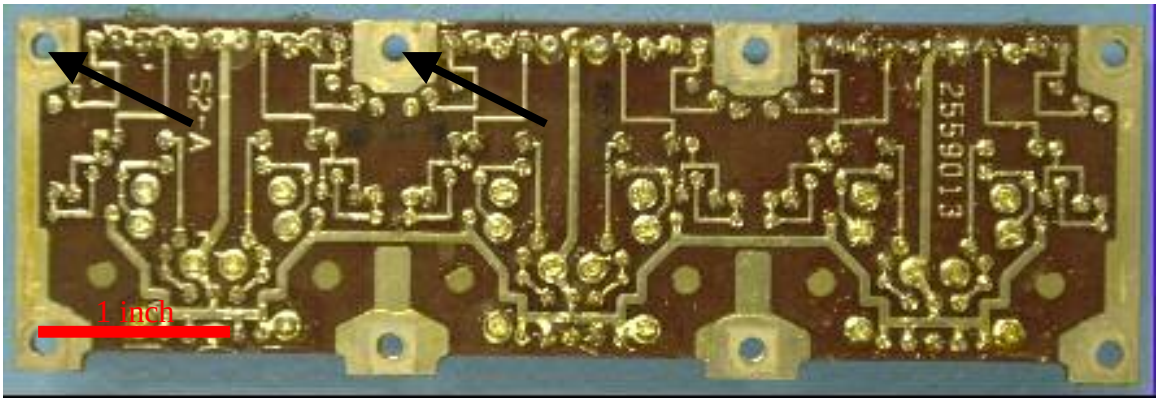


Figure 3-1 : These photos show the component side (A) and solder side (B) of board #1, identification number 2559013. A red rectangular box in A highlights some of the components (transformers) that would be difficult to remove. Also shown (see red arrow) is one of the PTHs that has not annular ring on this side. A blue arrow in A shows the adhesive used to secure the parts and wires. The 8 mounting holes (see black arrows in B) make the board more vibration resistant. Visual inspection was performed on this board

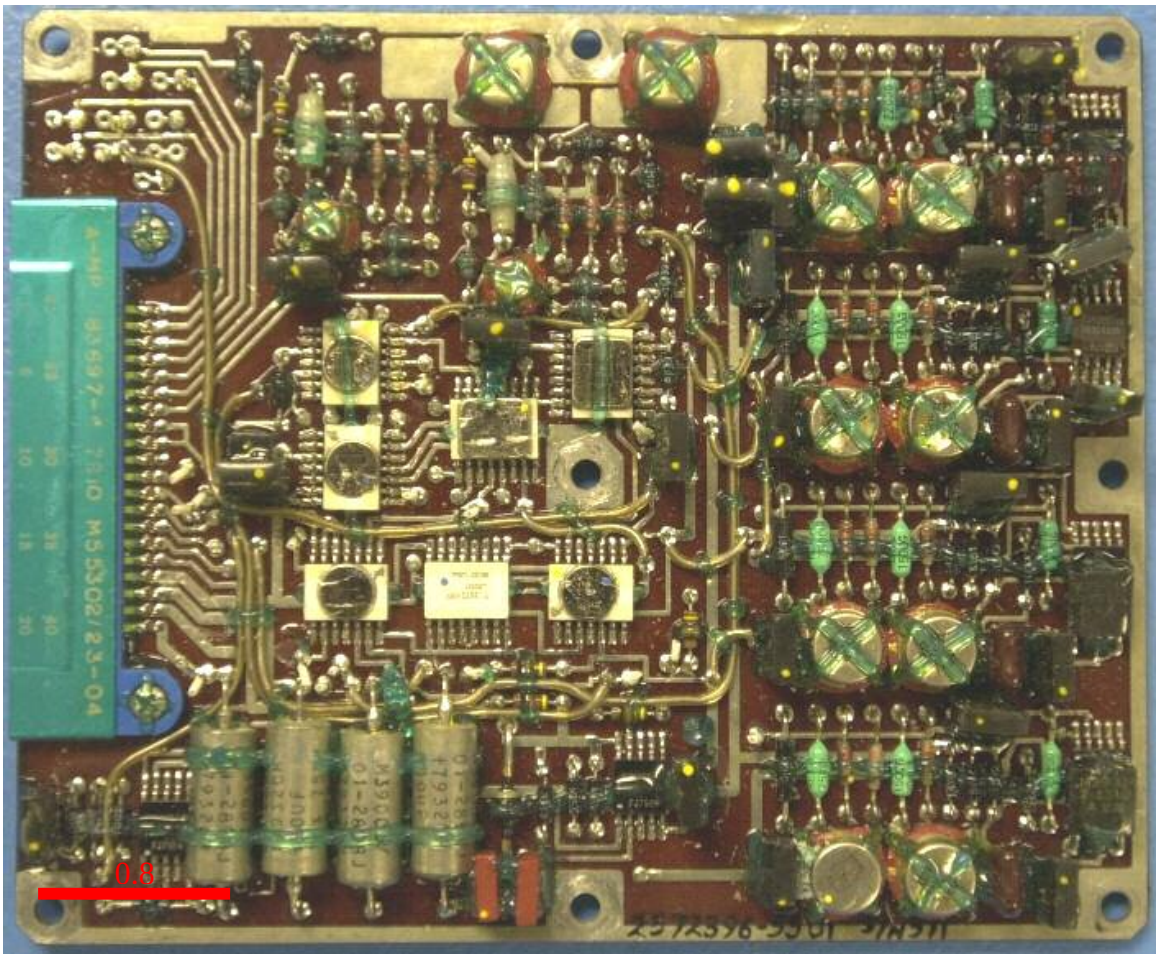


Figure 3-2: This photo shows the component side of board #2, identification number 2559022. Visual inspection was performed on this board.

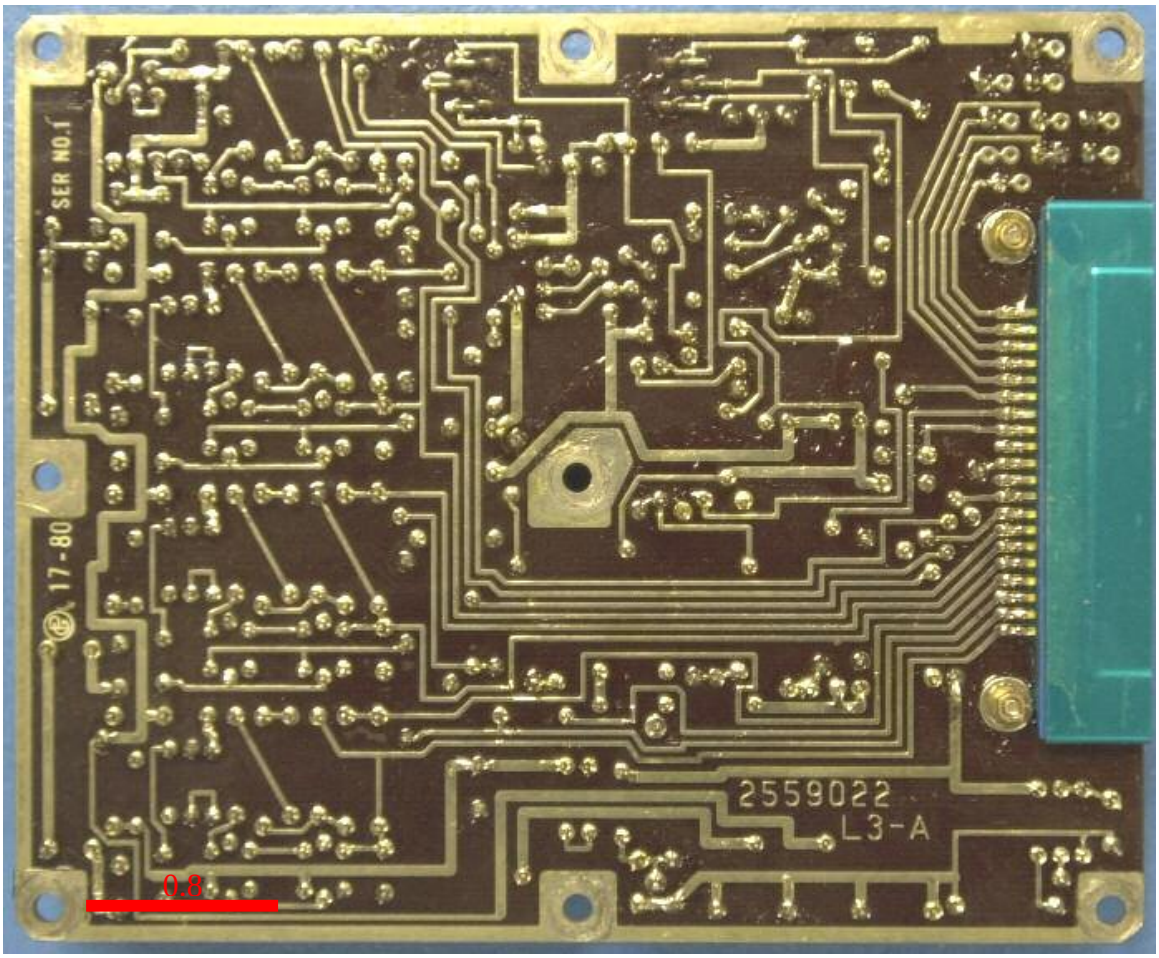


Figure 3-3: This photo shows the solder side of board #2, identification number 2559022. Visual inspection was performed on this board.

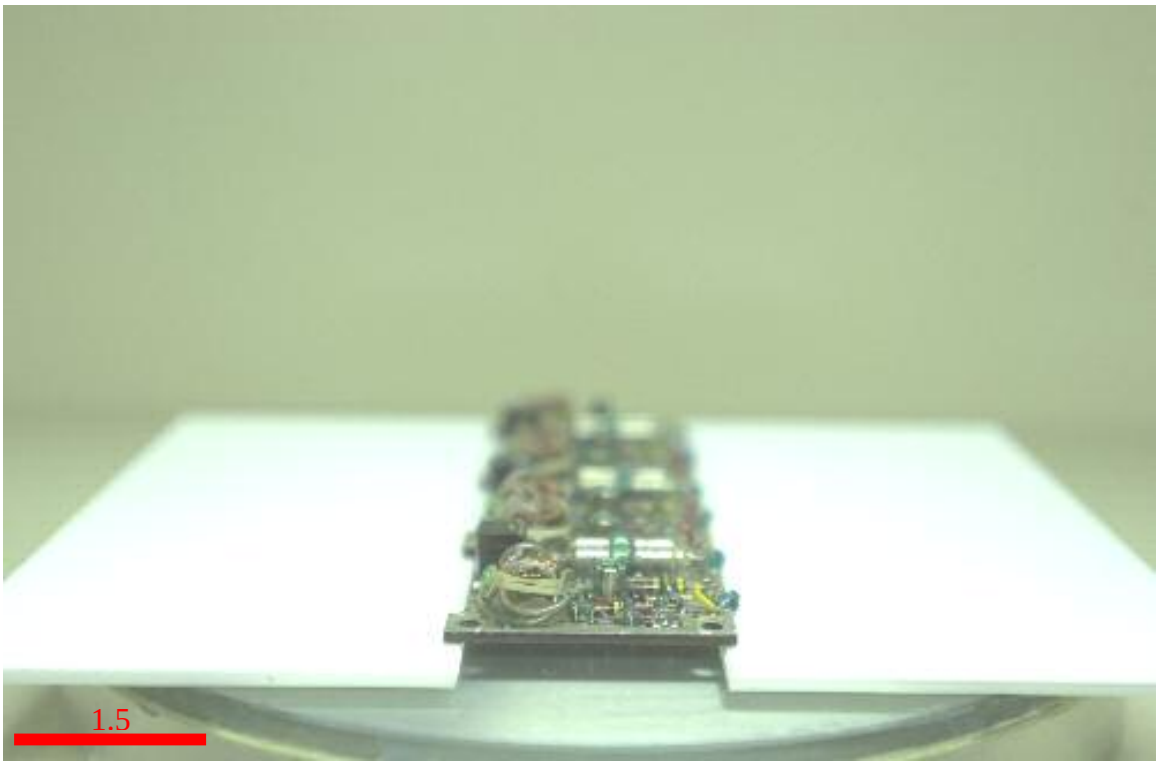


Figure 3-4: This photo shows the setup to measure board flatness. The board is suspended by its edges on ceramic plates on a flat glass plate.

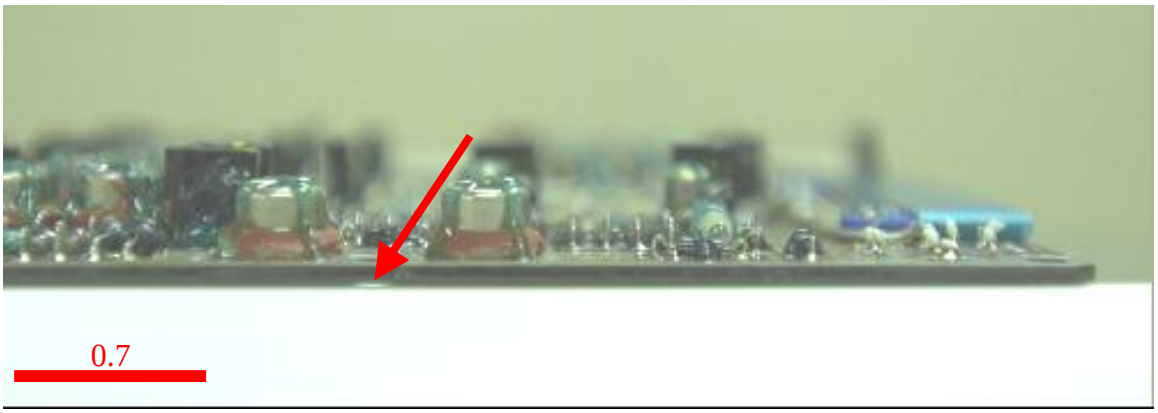


Figure 3-5: This photo shows the area where the measurement was taken for the board flatness assessment.

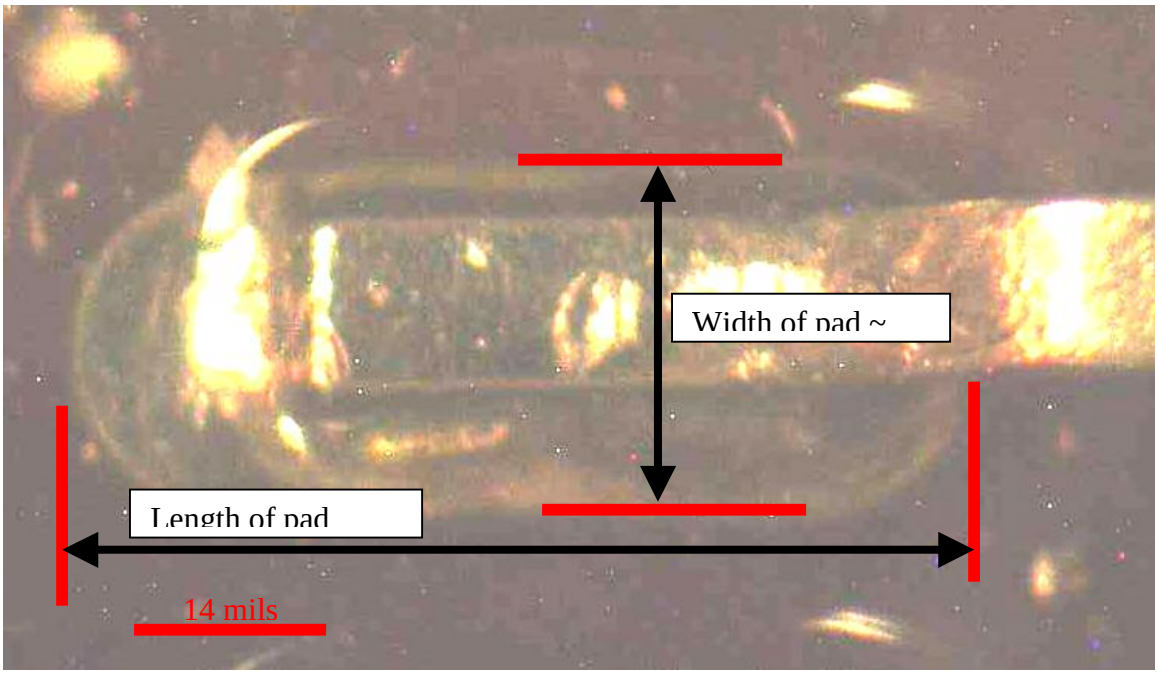


Figure 3-6: This photo shows the length of a pad compared to the width (0.08/0.03 ~ 2.7 > 2) which is greater than twice the width, in compliance to the specification.

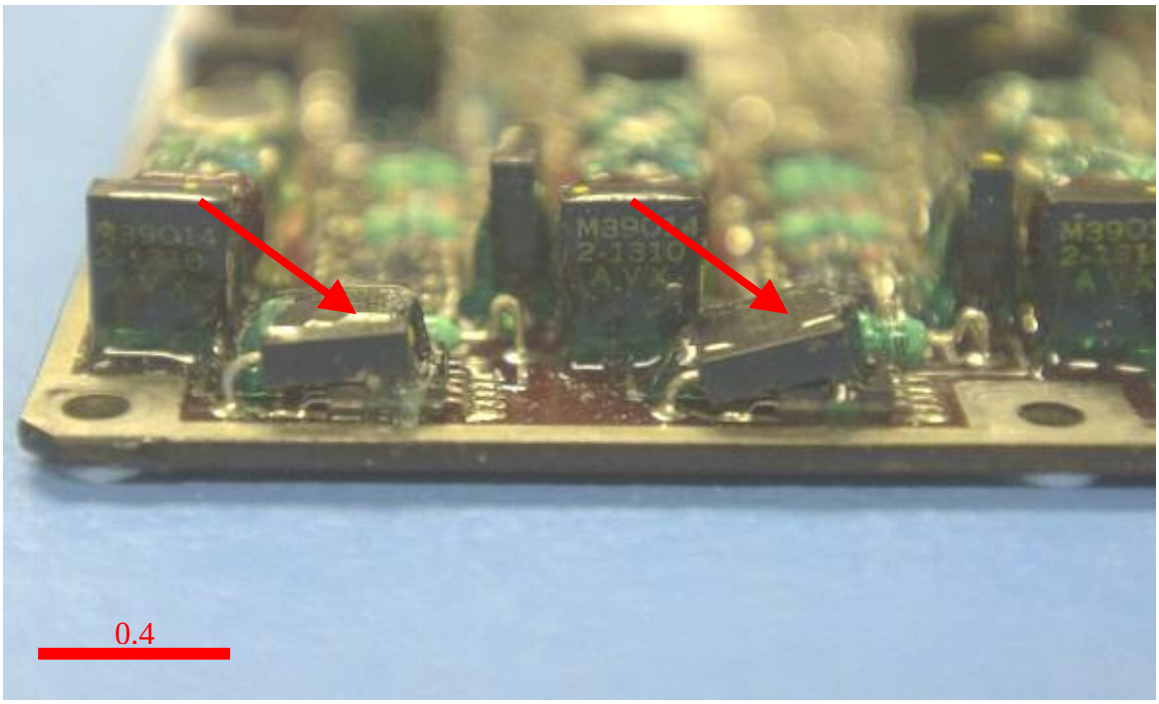


Figure 3-7: This photo shows bent components on board #2. This is done to facilitate small vertical clearances in these areas.

3.4 Investigation of degradation through destructive analysis

3.4.1 Destructive Physical Analysis of Selected Components

The cross-sectioned components were two tantalum capacitors (removed from board number 2559017) and two transformers (removed from board 2559023) (Table 3-3)

Table 3-3 Source of parts for DPA

Board Number	Action
2559017	DPA on two capacitors
2559023	DPA on two transformers

3.4.1.1 DPA procedure for the components

Each component was visually inspected using a low magnification microscope (10 - 50 X) and electrically tested. Since the transformers could not be removed from the board without risk of damage, the transformers were left on the board while the capacitors were removed. The components were then potted in a room-temperature cure epoxy resin (Allied High Tech Products). Potting ensures that there is no relative motion between the

board or part materials with respect to each other and also prevents chipping or edge rounding during cutting, grinding, and polishing. The cure is done under vacuum to remove any trapped air present in the sample. If air is trapped, it will cause bubbles to form in the epoxy resin and creating problems during the cross-sectional procedure and optical examinations. After the epoxy resin solidifies, sections of interest are cut out with a liquid cooled diamond edge-sectioning saw. An initial rough grind at 240 grit is used to remove material and get close to the area of interest. The sample undergoes successive grinding steps using SiC grinding paper (Allied High Tech Products). The grinding process moves on to a finer grit size only after all scratches from the previous grinding step have been removed. Typically, a sequence of 240-600-200 grit is used. The sample is then polished using 0.3 micron alumina (Allied High Tech Products). Samples are thoroughly cleaned between each stage of sample preparation. Micrographs of the polished cross sections are taken using optical (15 to 1000X) and/or environmental scanning electron (ESEM) microscopy (used when larger magnifications or higher resolutions are required)

3.4.1.2 Results of Preliminary Evaluation

The results of the destructive physical examination do not reveal any problems of degradation with the capacitors or transformers.

3.4.1.3 Electrical Testing

Electrical testing of the components revealed that each was functional. None of the coils for the transformers was open or shorted (resistance in each coil was less than 1 ohm). The capacitance values and leakage currents for the capacitors were within specification (see Table 3-4).

Table 3-4 Source of partss for DPA

Component	Capacitance (mF)			Specification (mF)
Capacitor	Capacitor	4.89	4.7 ± 10%	0.0
Capacitor	Capacitor	4.89	4.7 ± 10%	0.0

3.4.2 X-ray Analysis

No anomalies or defects were observed in the X-rays of the components (see Figure 44 and Figure 45).

3.4.3 Evaluation of Rejection Criteria – Capacitor (MIL-STD-1580A [1], see Figure 46 for layout)

A. Cracks extending through the glass header

B. Tubulet filled with solder less than 25% of its length when solder-plated leads are used and less that 50% of its length when gold-plated leads are used.

C. Voids in the tubulet solder or solder separation from the leads that reduces the solder fill requirements mentioned in “B.”

D. Anode (tantalum slug) not parallel to case within 15 degrees. Voids in tubulet solder or solder separation from lead or tubulet that reduces the fill to less than 25% of tubulet height for solder plated leads and less that 50% of its length when gold-plated leads are used.

E. Solder spikes inside unit or eyelet solder extending beyond bottom of tubulet.

F. Broken or cracked anode lead weld.

G. Anode immersed in solder that is less than 1/3 of its height.

H. Anchor solder cracked or pulled away from anode slug.

I. Solder buildup on inside of can with height greater than 0.50 mm (0.02 inches) resulting from solder rundown during sealing process.

J. Anode totally immersed in solder.

K. Anode cracked, broken or distorted.

L. Loose material 0.25 mm (0.01 inches) or large enough to bridge shortest distance between lead and can, or between tantalum pellet and can.

M. Any defect that reduces the part reliability (e.g., bulges or dents in the case).

N. Failure to meet external visual requirements.

1. Cracks on the cracks seal.

2. Cracked or cold solder joint around seal area.

3. Flux or foreign material on anode lead and around seal area.

None of the criteria that would cause the samples to be rejected were found in the capacitor cross-sections (see Figure 47 through Figure 51).

3.4.4 Evaluation of Rejection Criteria – Transformers (MIL-STD-1580A [1] 9)

a. Wire size not in accordance with MIL–STD-981 and applicable specification or drawing.

b. Interconnect ribbon not in accordance with applicable specification or drawing.

c. Internal wire leads attached only by soldering with no evidence of mechanical anchoring.

d. Wire windings that cross over other turns in going from one wound segment to adjacent segment.

e. Nicks, kinks, reduction in wire cross-section, or evidence of other wire damage.

f. Evidence of flux or other types of residues.

g. Teflon tape

h. Charred, crushed, discolored, or damaged wire insulation.

i. Repaired or spliced coil wire.

j. Wire-to-lead termination connections that do not show a sufficient stress relief loop.

k. Cold solder joints, or solder joints with no fillet around wire or termination.

l. No evidence of weld tip indentation in welded joints.

m. Cracks in welded joints.

n. Loose or splattered weld.

o. Lack of three (3) full nonoverlapping wraps of wire at each post termination.

p. Stranded conductor wire at terminations that does not show pretinning or that shows large globulesof solder that obscure the wire contour, or wire swelling due to excess wicking.

q. Solder that is not chemically Type Sn 60, Sn 62, or Sn 63 in accordance with QQ-S-571 or (for wire gauges smaller than size No. 38) Sn 10 for Class S devices.

r. Coils or other electronic components that show evidence of overheating.

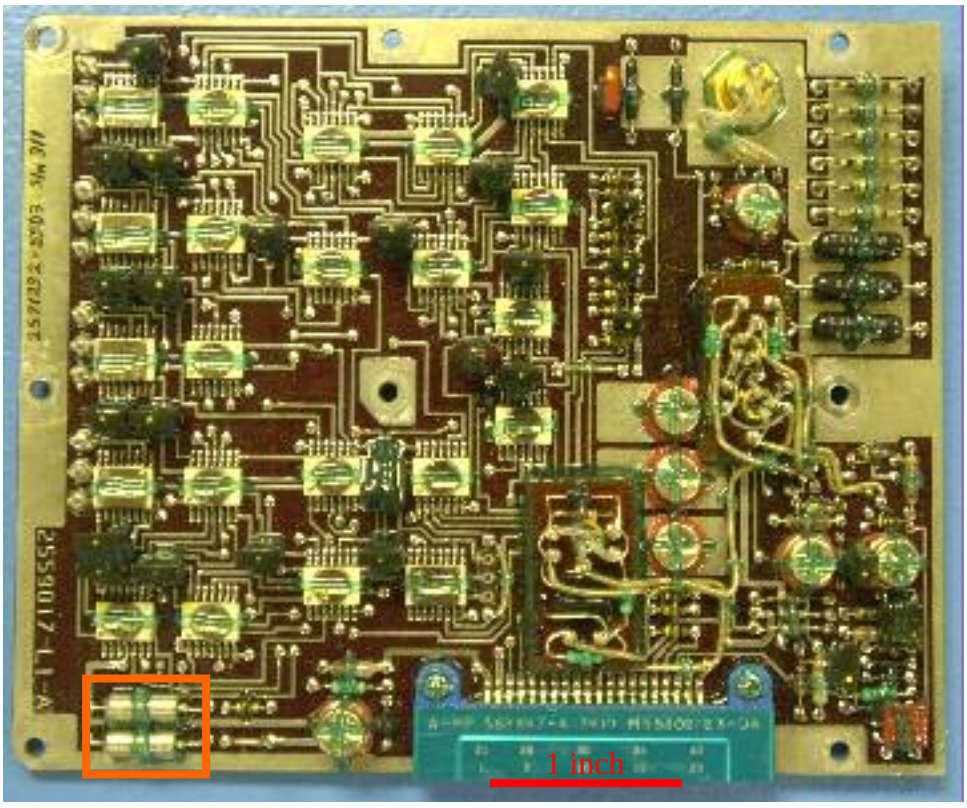
s. Fractures, cracks, or pinholes in solder joint.

t. Solder joints with sharp tips or peaks or with a protruding, bare wire-end or bare strands of a conductor.

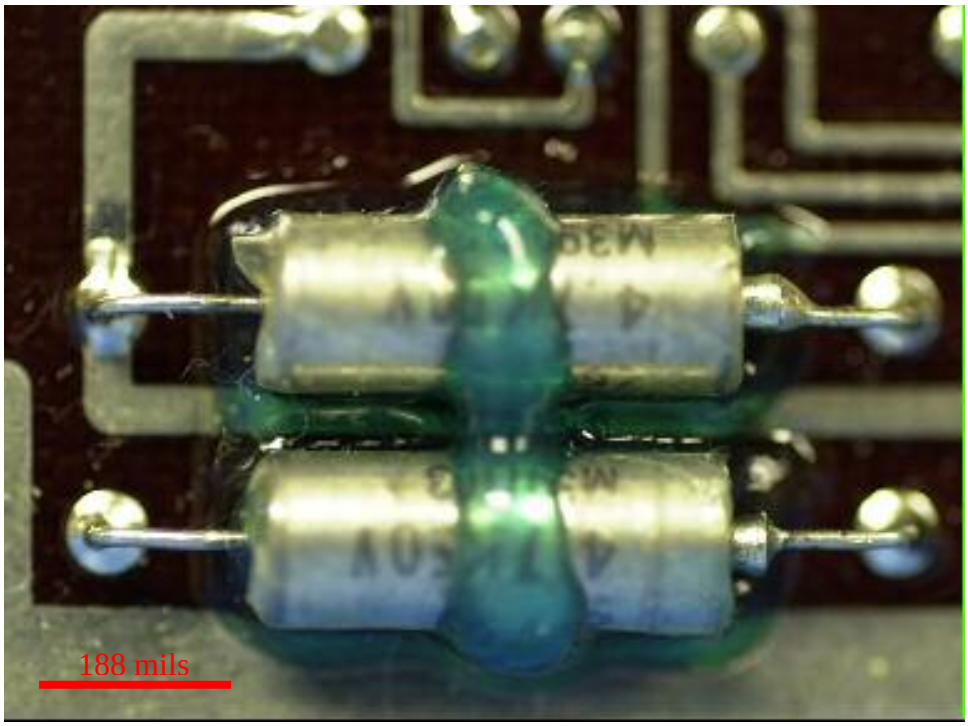
u. Foreign or extraneous matter embedded in or adherent to wire joints, between windings, or cores, or thin impregnation.

Conclusion

Although the samples contain voids in the solder, and slight pin misalignment, no reason for rejection was found, based on the criteria set by Mil-Std-1580 and what was observed in the cross-section.

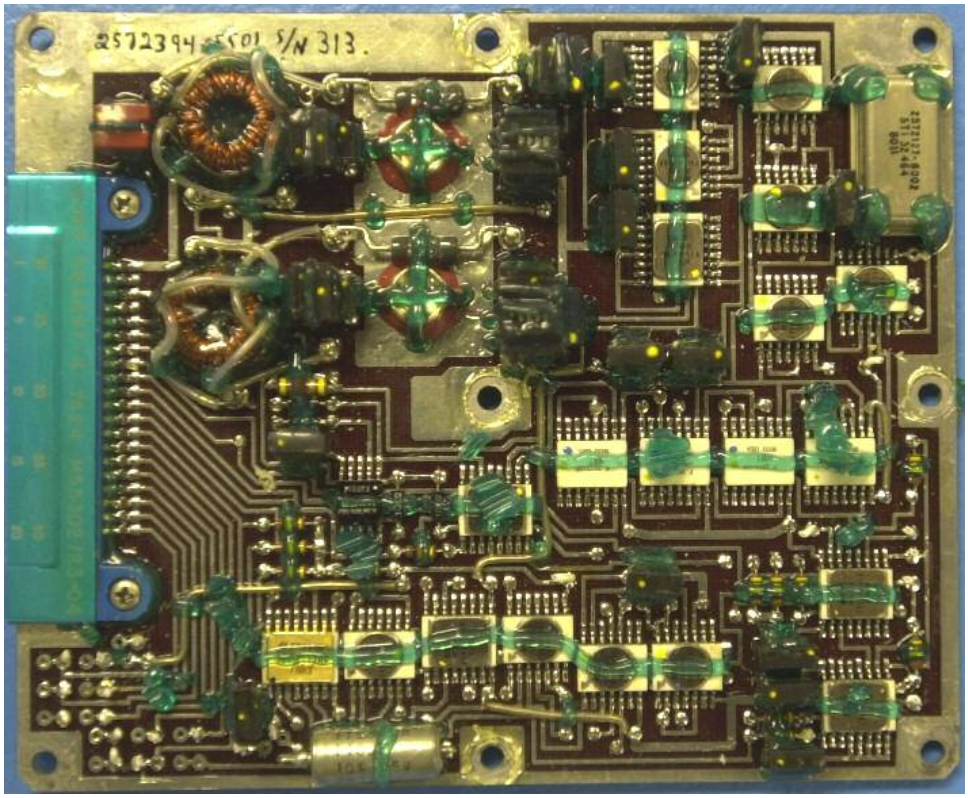


A

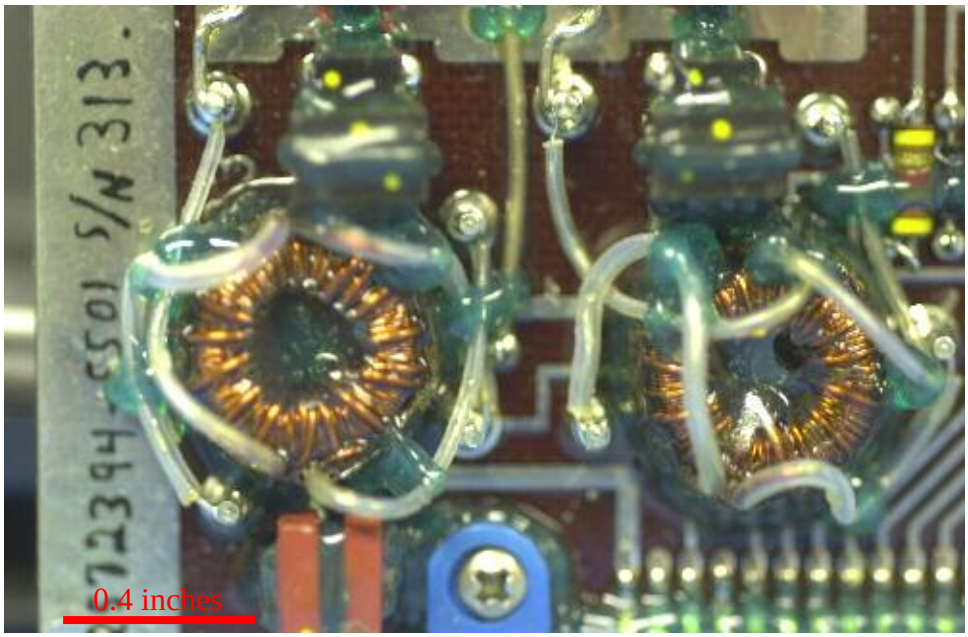


B

Figure 3-8These photos show the location on board number 2559017 from where the two capacitors for the DPA were removed (see red box in A). Figure B shows an enlargement section with the two capacitors.

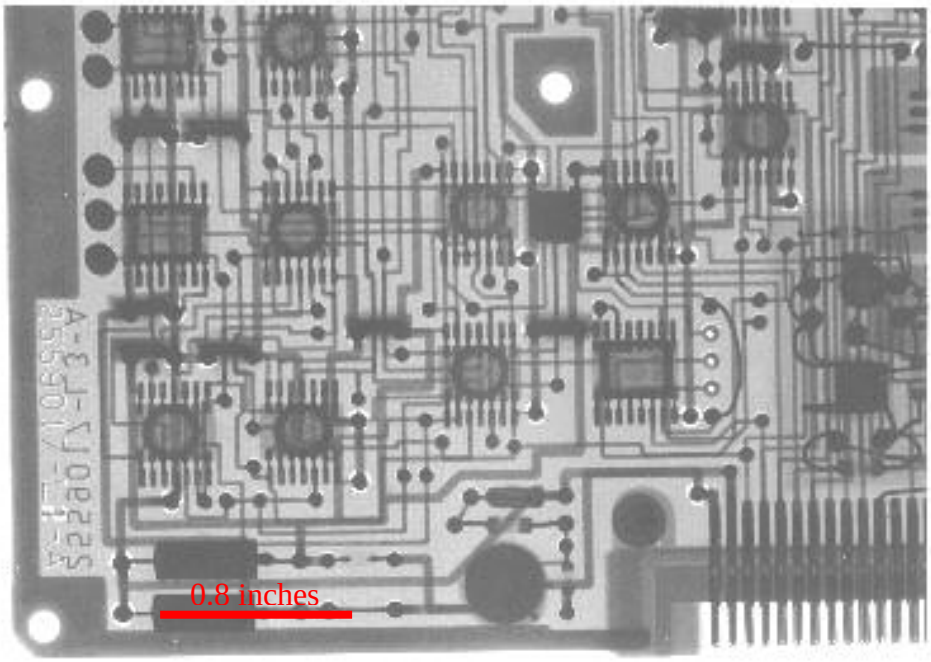


A

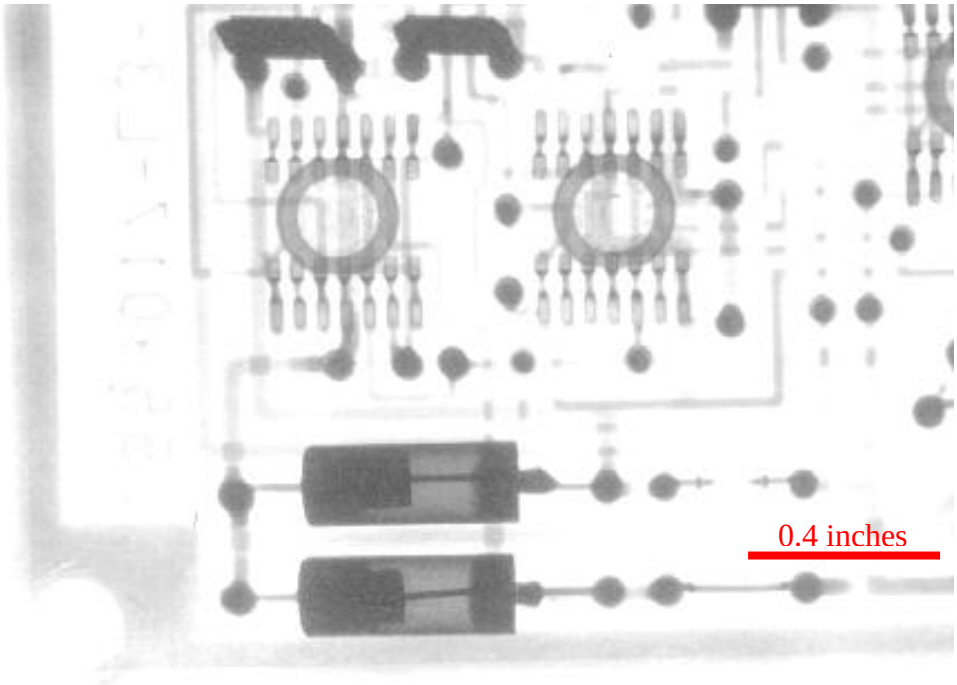


B

Figure 3-9: These photos show the location on board number 2559023 from where the two transformers for the DPA were removed (see red box in A). Figure B shows an enlarged section with the two transformers.



A



B

Figure 3-10: These X-ray images show the layout for board number 2559017 in the area containing the two capacitors that were removed for the DPA. Figure B shows an enlarged section with the two capacitors.

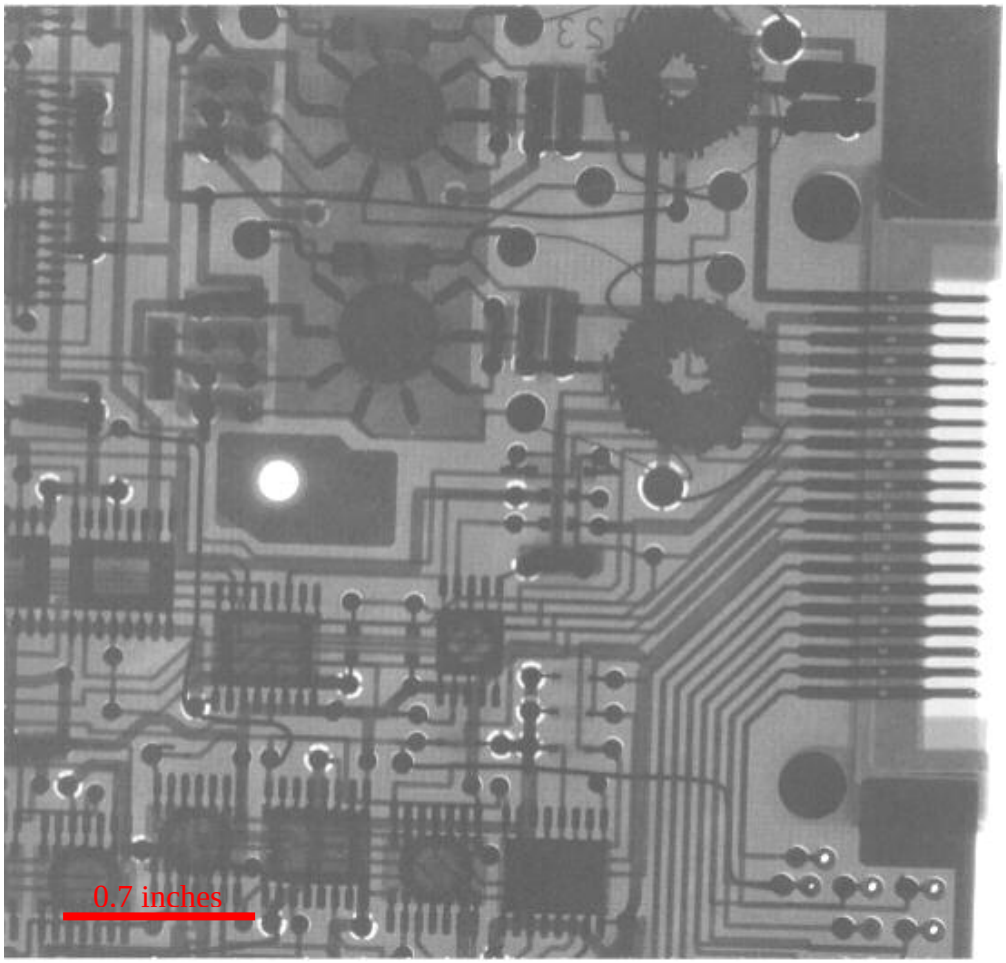


Figure 3-11: This X-ray image shows the layout for board number 2559023 in the area containing the two transformers that were removed for the DPA.

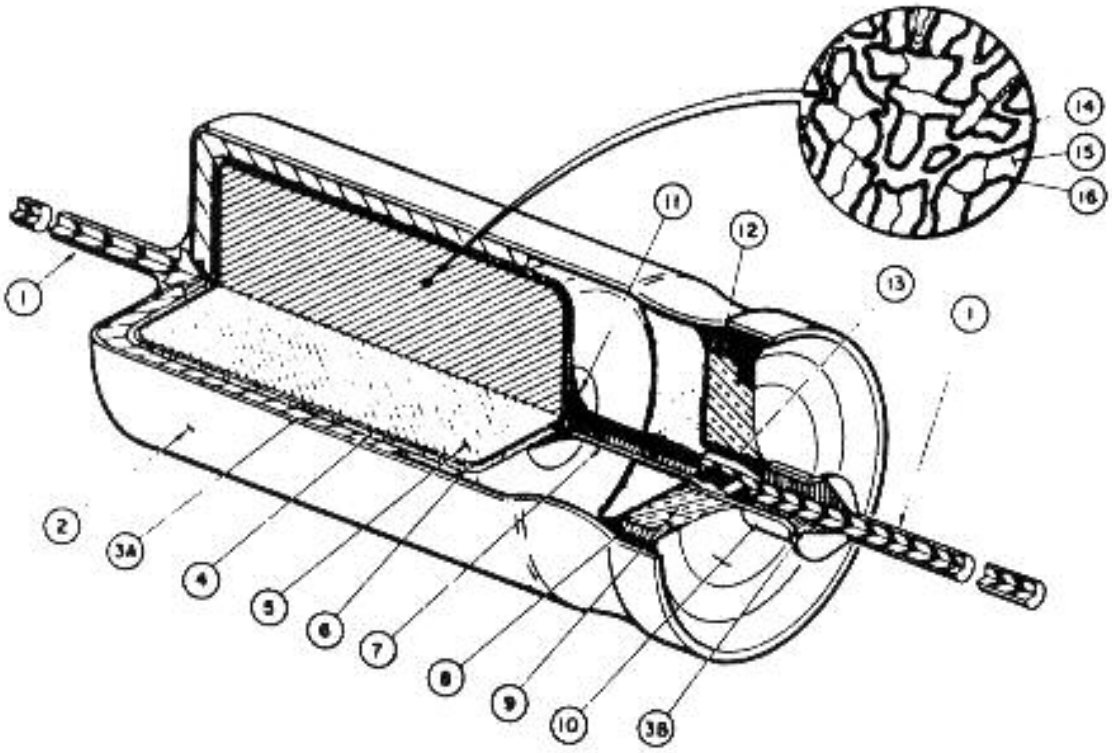
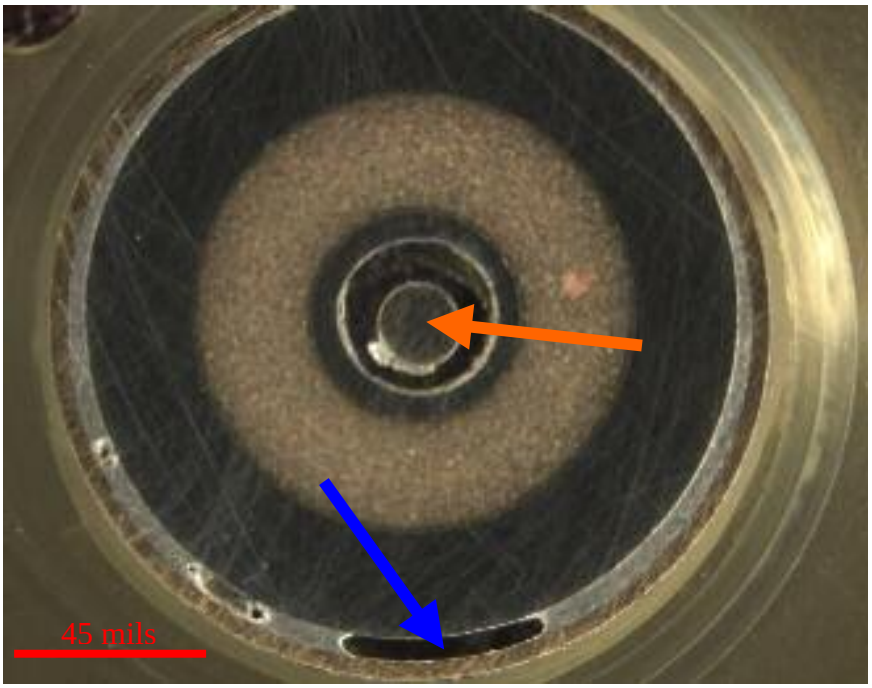
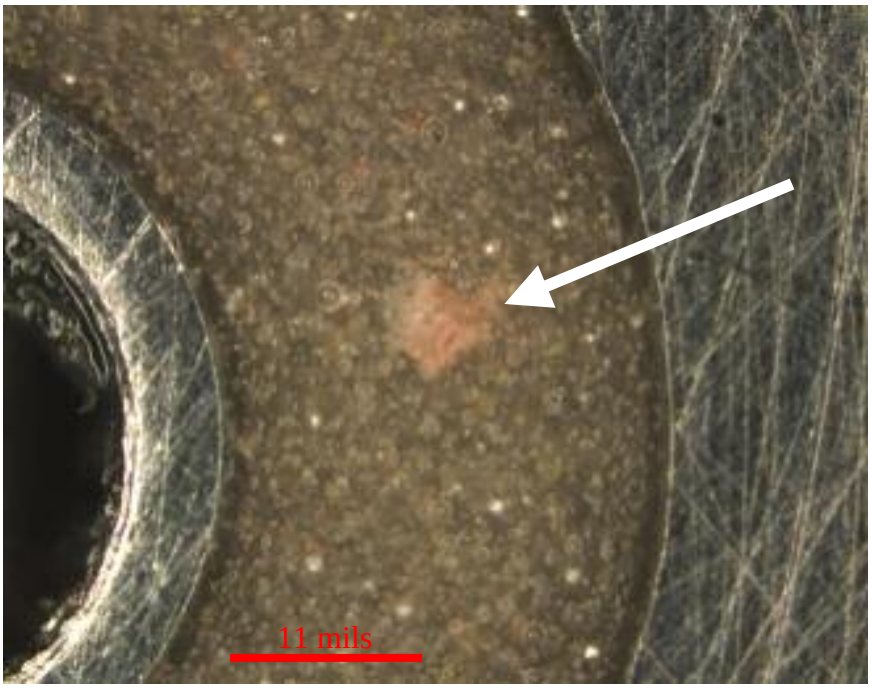


Figure 3-12: This schematic shows a typical solid tantalum capacitor (MIL-STD-1580A).

1. External leads
2. Case
3.
    A. Solder
    B. Solder
1. Conductive paint
2. Slug
3. Carbon film
4. Anode riser
5. Seal assembly
6. Seal assembly
7. Seal assembly
8. Permanganate
9. Case
10. Anode riser to lead lap weld
11. Oxide coating
12. Core
13. Dielectric film

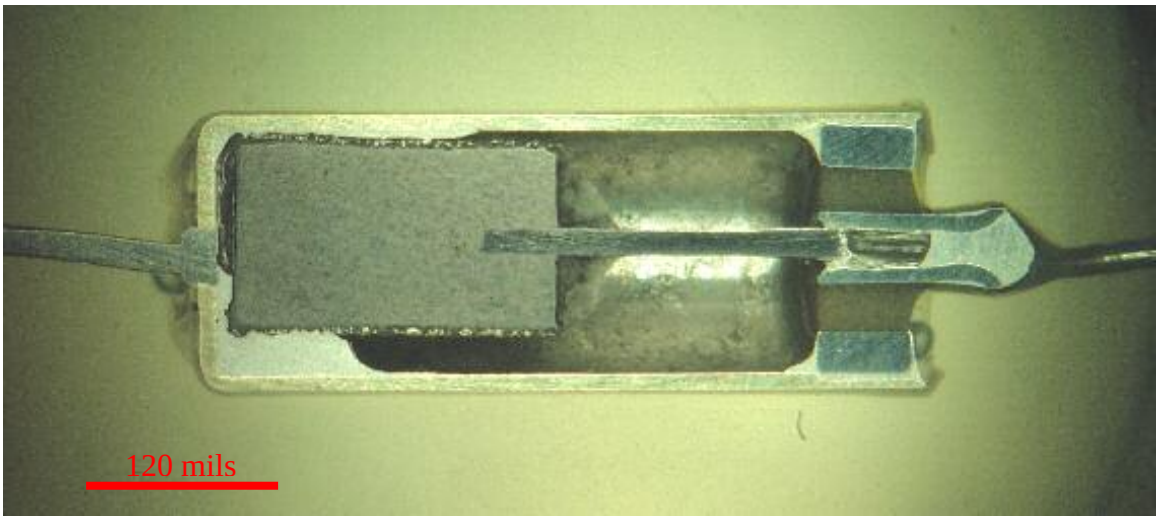


A

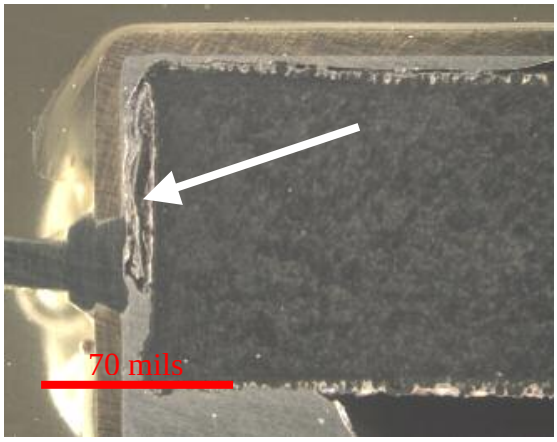


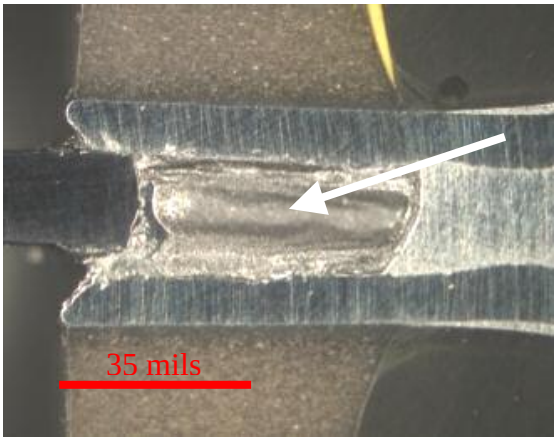
B

Figure 3-13: These photos show the cross-section top view of one of the tantalum capacitors. In A, it can be observed that the pin is not exactly centered, and that there are some voids in the solder. B is an enlargement of an area in A where a reddish discoloration was seen in the glass seal.



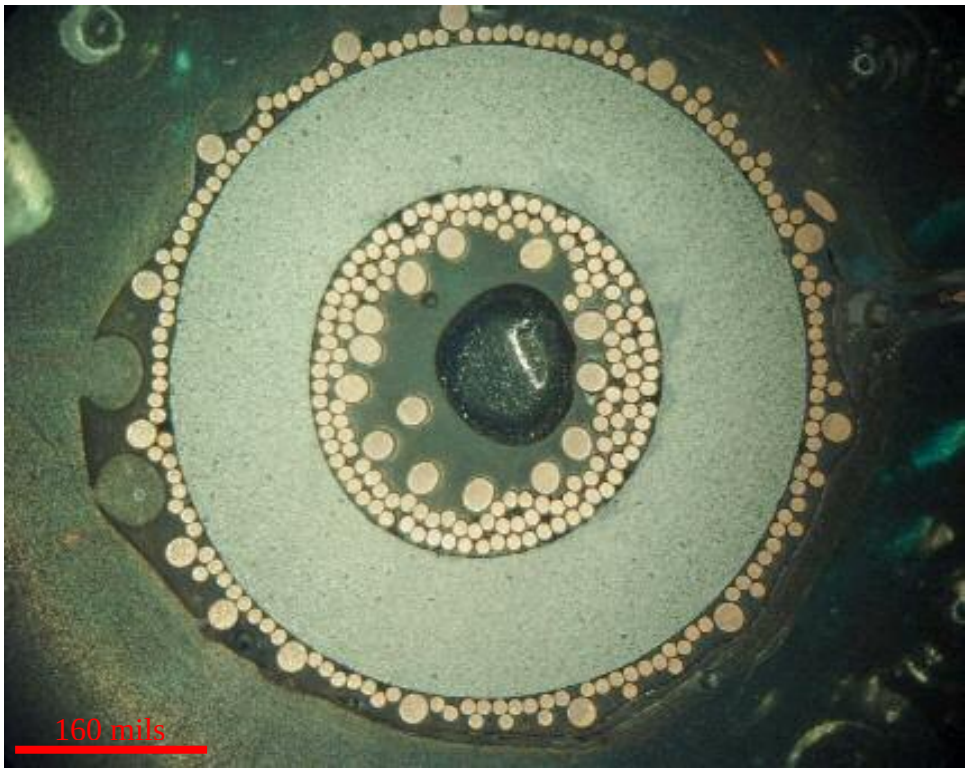
A



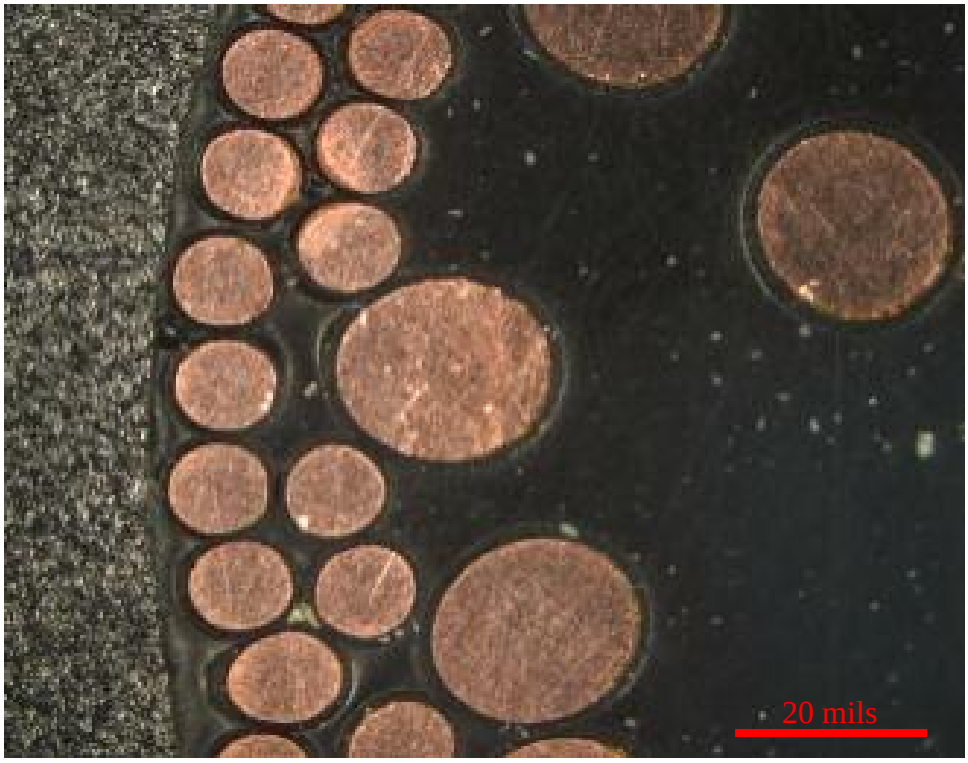


B **C**

Figure 3-14: These photos show the cross-sectional side overview of one of the tantalum capacitors (A). In B a void in the solder in the around the tantalum plug can be seen. In C a void in the solder in the tubulet is shown.

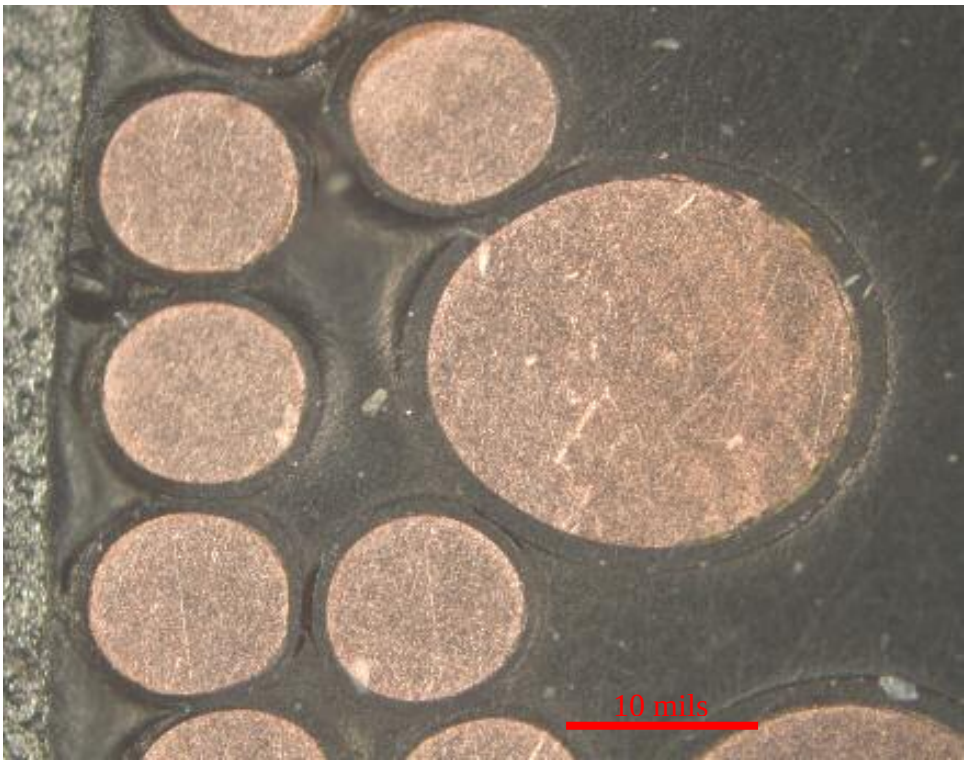


A



B

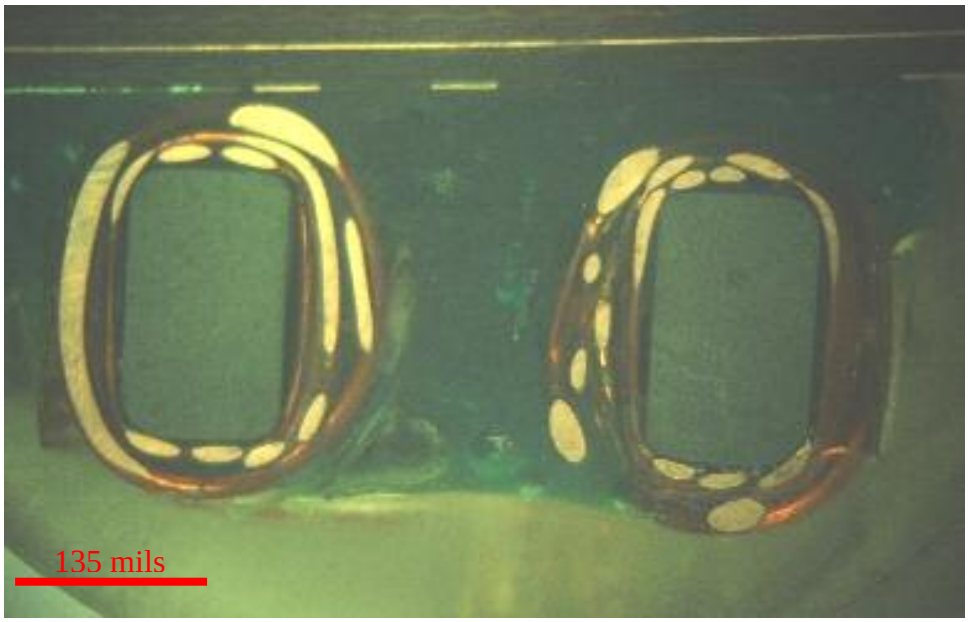
Figure 3-15: These photos show the cross-section top view of one of the transformers. B, an enlargement of an area in A, shows the separation between the coils.



A

B

Figure 3-16: These photos show the cross-section top view of one of the transformers. In B, it can be observed that there are voids between the coil wires.



A

B

Figure 3-17: These photos show the cross-sectional side overview of one of the transformers. B is an enlargement of an area in A.

4 LCEP

The life cycle loading for this project includes the environmental conditions that the boards are exposed during its complete life (e.g., testing, transportation, operation). The number of missions undertaken by an individual unit in the first 20 years is 15 for this project. Two profiles used for the simulation are:

- 20 years of life based on the environment seen by the boards in the last 20 years of operation
- 40 years of life, which includes the expected environment for the next 20 years of operation assuming an increased frequency of shuttle launch.

The life cycle loading characteristics included both operating and non-operating conditions. The testing for units may be done in two stages. One stage is during the manufacture of the electronic modules (e.g., SPA, EEEU) and the other is during the assembly of the complete SRMS. The complete SRMS consists of electronic modules and mechanical hardware. Where applicable, the environmental profiles are identified to be “module build” and “SRMS build.”

4.1 Thermal Life cycle

The thermal conditions are modeled for the SRMS unit, which had the worst environmental profile. The worst case refers to the Flight EEEU, which had to go undergo qualification (qualification is typically done only once after the initial manufacture for a unit not used in space missions) due to major design changes.

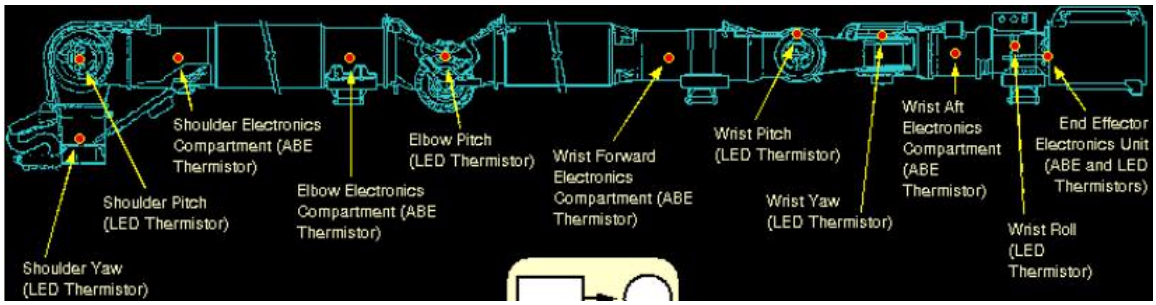


Figure 4-1: Location of thermistors on the SRMS

Figure 4-1 shows the location of the thermistors on the SRMS. The ABE thermistor at the EEEU unit end was used to obtain operation thermal cycle data.

Qualification (powered up): Qualification is used to see if the unit can withstand space conditions. It consists of 50.5 cycles. The temperature profile experienced is between –36 to 81°C. Out of the 50.5 cycles, 26 are during module build. The additional cycles were performed during SRMS build after the unit was redesigned. The profile of this cycle is shown in Figure 4-2.

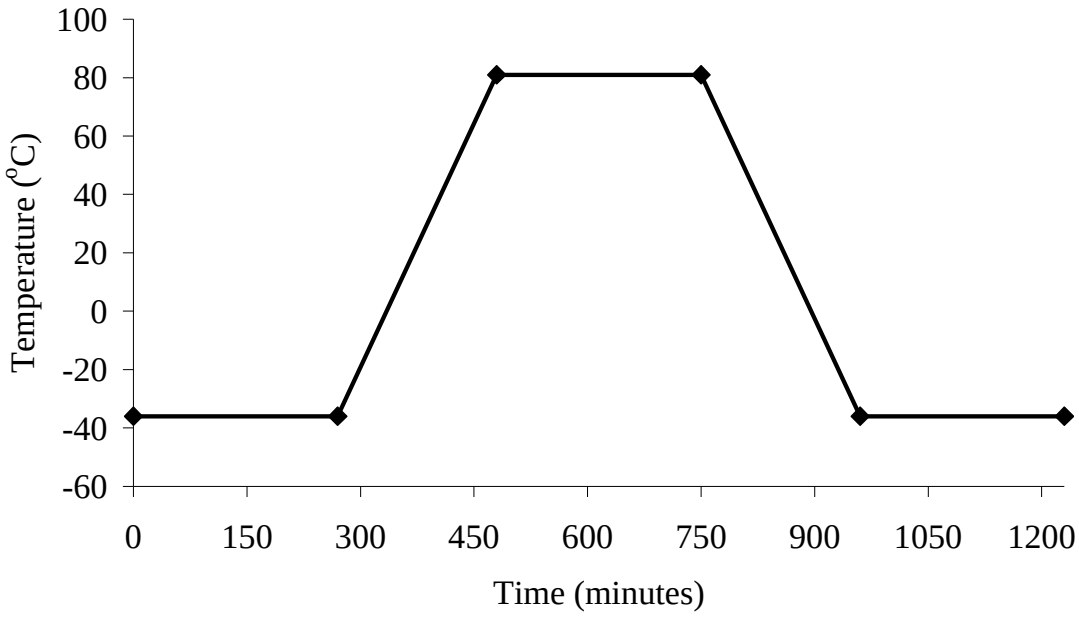


Figure 4-2 Qualification temperature cycle

Acceptance (powered up): After assembly or rework, the units have to be requalified through acceptance tests to see if they are capable of undertaking the next mission. 1.5 cycles of thermal cycling are undergone during the module build, 2 cycles are undergone during the SRMS build. From the testing after missions, and following rework of the units, there have been 16 more thermal cycles, so the total is 20 cycles with temperatures ranging from -25 to 70 °C. Figure 4-3 shows the profile of acceptance temperature cycle.

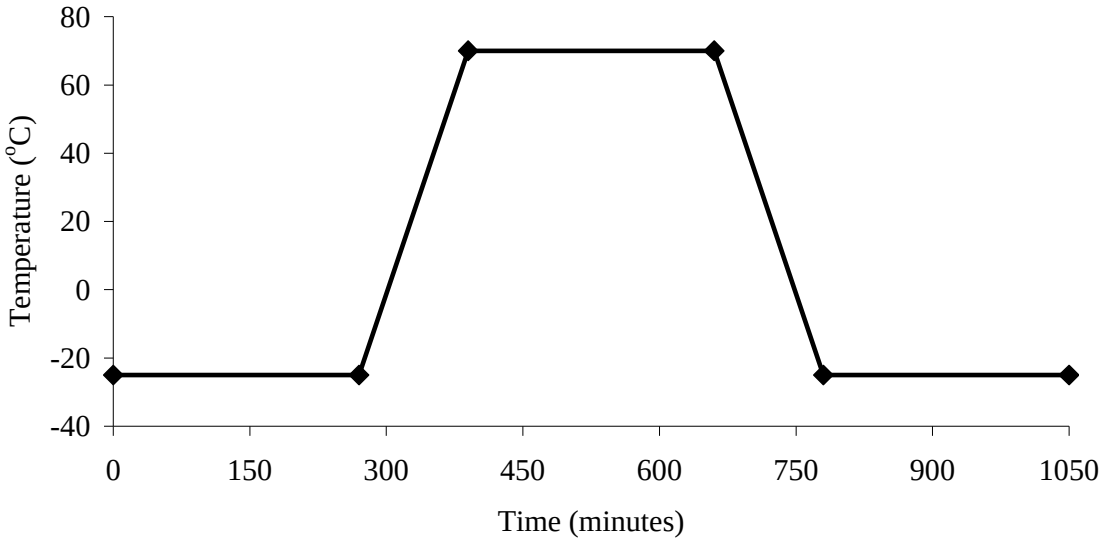


Figure 4-3 Acceptance temperature cycle

Ferry flight (non-operating): The Ferry Flights need to be undertaken when the shuttle cannot land in Florida and it uses the alternate landing site of Edwards Air force Base in California. This flight diversion takes place once in about every 3 missions so total number of ferry flights is 5 for 20-year operation. The temperature profile experienced is between -40and 35 °C. Figure 4-4 shows the profile of Ferry flight temperature cycle.

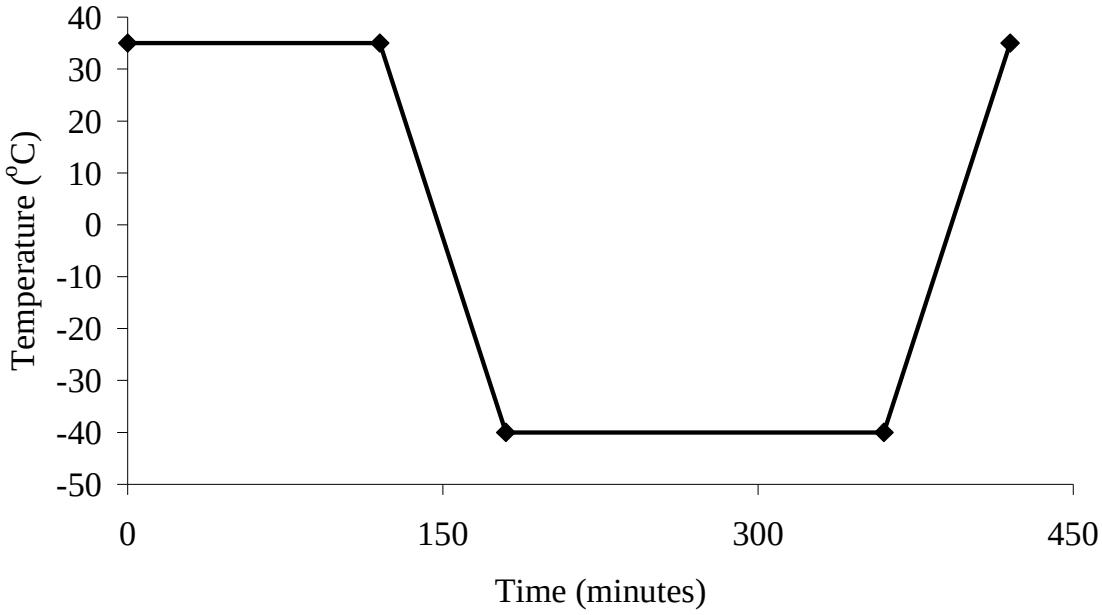


Figure 4-4 Ferry flight temperature cycle

Storage (non-operating): Each SRMS spends approximately 356 days a year in climate controlled storage. The temperature profile experienced is between 17 and 27ºC. It is assumed that one temperature cycle occurs each day so the total number of cycles is 7120 (20×356). Figure 4-5 shows the profile of storage temperature cycle.

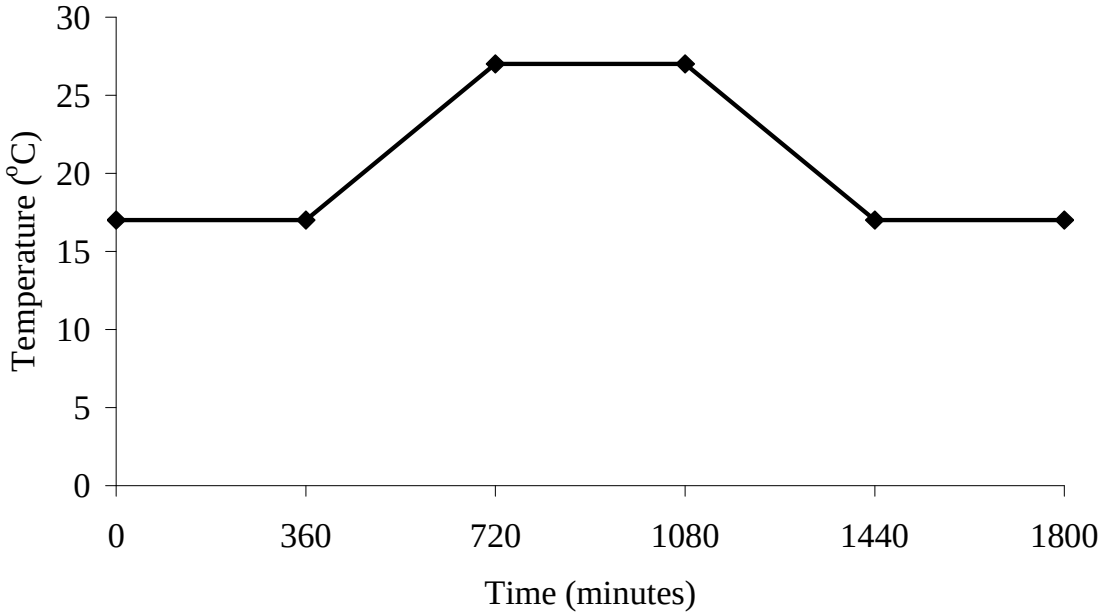


Figure 4-5 Storage temperature cycle

Operation (powered up): consists of 4 different operation cycles based on the environmental profile given by MD Robotics. Figure 4-6 shows the profile of operation temperature cycle. The four temperature cycles are as follows:

Operation cycle 1: This cycle approximates the zone 1 shown in Figure 4-6. The temperature range is from 2 to 10 °C. Each cycle has 185 minutes-dwell time at maximum temperature, 175 minutes dwell time at minimum temperature, 720 minutes ramp from minimum to maximum temperature, 270 minutes ramp from maximum to minimum temperature. There are 3 cycles in one mission. In 15 missions over 20 years, the total number of cycles is 45.

Operation cycle 2: This cycle approximates the zone 2 shown in Figure 4-6. The temperature range is from 2 to 6 ºC. Each cycle takes 1.5 hours broken up uniformly between dwell times at maximum and minimum temperature and the ramp up and the ramp down times. There are 16 cycles in one mission of 12 days, so there are a total number of 192 cycles. In 15 missions over 20 years, the total cycles are 2880.

Operation cycle 3: This cycle approximates the zone 3 shown in Figure 4-6. The temperature range is from 4 to 25 °C. Each cycle has 60 minutes-dwell time at maximum temperature, 720 minutes dwell time at minimum temperature, 720 minutes ramp from minimum to maximum temperature, 720 minutes ramp from maximum to minimum temperature. There are 2 cycles in one mission. In 15 missions over 20 years, the total cycles are 30.

Operation cycle 4: This cycle approximates the zone 4 shown in Figure 4-6. The temperature range is from –6 to 4°C. Each cycle takes 720 minutes-dwell time at maximum temperature, 360 minutes dwell time at minimum temperature, 360 minutes

ramp from minimum to maximum temperature, 360 minutes ramp from maximum to minimum temperature. There are 2 cycles in one mission in 15 missions over 20 years the total number of cycles are 30.

The temperature conditions given above are for the first 20 years. It is expected that each SRMS would undertake 25 more missions in the next 20 years. During the next 20 years, it will undergo 75 cycles more of operation temperature cycle 1, 4800 of operation temperature cycle 2, 50 of operation temperature cycle 3, 50 of operation temperature cycle 4, 7000 cycles more of storage, 16 cycles more of acceptance and 9 more ferry flight cycles.

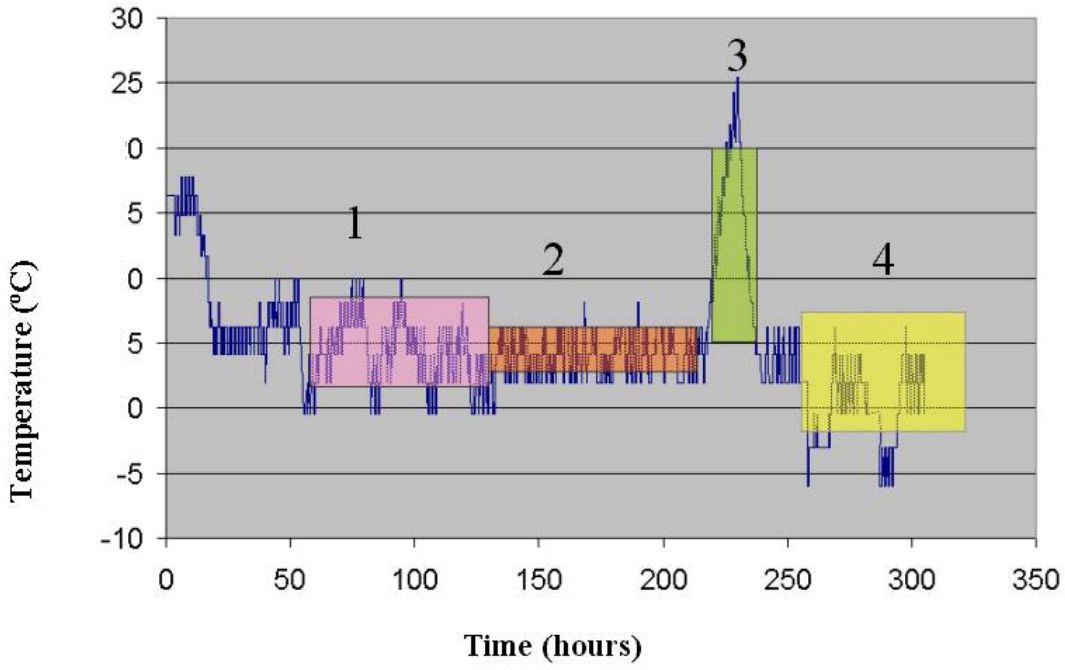


Figure 4-6 Operation temperature cycle example

4.2 Vibration

The vibration data given by MD Robotics follow the same build profile as that of thermal conditions. Figure 4-7 shows the graphical description of vibration profiles. From the

graphical description, it can be inferred that the Qualification for the End Effector is done only once and at the beginning. The 20-year profile sees 4 acceptance, and 3 qualification and acceptance vibration tests for the End Effector. The acceptance vibration is performed 5 times for the End Effector electronics unit. Each vibration profile is explained in detail below.

End Effector Electronics unit acceptance vibration test (EEEU AVT): The End Effector Electronics Unit undergoes acceptance tests after construction or rework. It is done for a period of 1 minute and since it is done 5 times a total time of 5 minutes is taken for 20 year profile. Table 4-1 EEEU AVT gives the power spectral density (PSD) values for the cycle at different frequencies.

Table 4-1 EEEU AVT

Frequency (Hz)	Power Spectral Density (g2/Hz)
20	**0.032**
80	**0.500**
200	**0.500**
2000	**0.005**

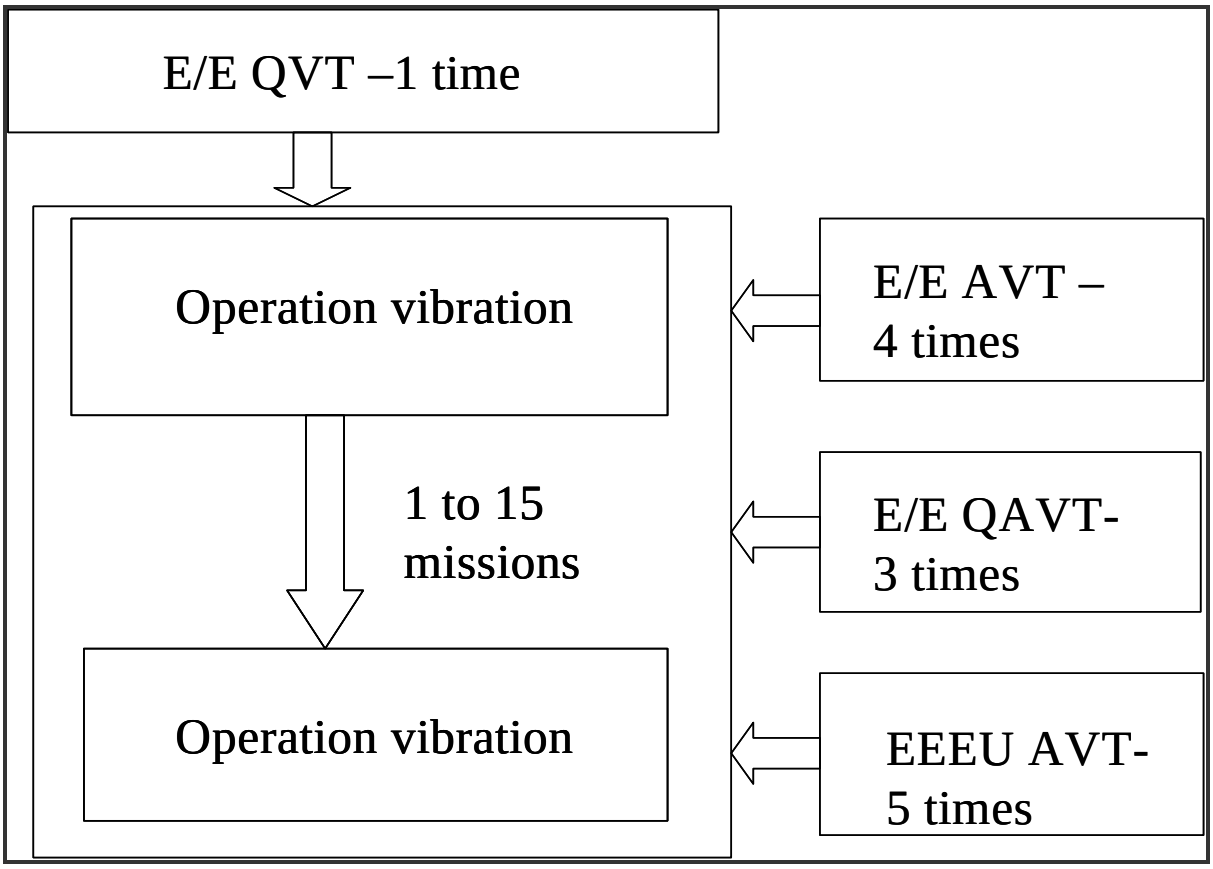


Figure 4-7: Graphical description of vibration profiles

End Effector acceptance vibration test (E/E AVT): This is acceptance vibration done for the whole End Effector assembly to confirm workmanship (quality of the work) of the unit after construction or rework. This test is done 4 times for 15 missions; and the takes one minute each time. Table 4-2gives the power spectral density (PSD) values for the cycle at different frequencies.

Table 4-2: E/E AVT

Frequency (Hz)	Power Spectral Density (g2/Hz)
20	**1**
80	**1**
275	**0.085**
470	**0.05**

2000	**0.05**

End Effector quality and acceptance vibration test (E/E QAVT): This vibration cycle is performed during Qualification of the unit. The purpose of QAVT is to prove that the Qualification unit is designed well enough to survive all AVT's, which a flight unit will see. It is done 3 times for 15 minutes each. Table 4-3 gives the power spectral density (PSD) values for the cycle at different frequencies.

Table 4-3: E/E QAVT

Frequency (Hz)	Power Spectral Density (g2/Hz)
20	**0.017**
80	**0.068**
350	**0.068**
2000	**0.012**

End Effector qualification vibration test (E/E QVT): This vibration cycle is performed during Qualification of the unit. The purpose of QVT is to prove that the Qualification unit is designed well enough to survive all life vibrations, which a flight unit will see. It is done once for 50 minutes. Table 4-4 gives the power spectral density (PSD) values for the cycle at different frequencies.

Table 4-4: E/E QVT

Frequency (Hz)	Power Spectral Density (g2/Hz)
20	**0.010**
80	**0.040**
350	**0.040**
2000	**0.007**

Operation vibration: This refers to the vibration that the boards are exposed to in a normal mission, it lasts for 5 seconds, and since there are total of 15 missions the total time taken is 75 seconds. The PSD profile of the End Effector Electronics unit qualification vibration test (EEEU QVT) is used for operation profile because it is considered as an indicator of operation vibration. Table 4-5 gives the power spectral density (PSD) values at different frequencies.

Table 4-5: Operation vibration

Frequency (Hz)	Power Spectral Density (g2/Hz)
20	**0.010**
80	**0.040**
350	**0.040**
2000	**0.007**

The data for 40 years includes 8 more EEEU AVT's and 125 (5 seconds per launch) seconds more for operation vibration.

5 Failure Modes and Effects analysis

Failure modes and effects analysis (FMEA) was done to identify the different failures and modes of failure that can occur at the component, subsystem, and system levels. The FMEA was initially done based on the failures that have occurred and were observed during the physical analysis. FMEA identified temperature and vibration as the two loads that would possible cause maximum damage on the electronics. Table 5-1 gives a FMEA done on the system and second half of the table gives a complete listing of failure effects for space electronics.

Table 5-1: FMEA table

FAILURE MODES	FAILURE LOADS AND EFFECTS
Open circuit,unmating of contact surfaces of connectors.	Vibration and g forces encountered during launch.
Possible instability of transformers, corrosion of metallization, electrical open, shift in parametrics.	High temperature(150 degree c) because of solar radiation. High temperature proximity of power sources where heavy electric currents have heating effects.
Wire breakage and broken leads.	
Effect of fretting or mechanical fatigue of interconnection materials.	Cracks of voids around weld circumference.
Weld at low heat produce too small spot weld size and inadequate weld strength under tension and shear.	Open circuits, component failures, electrical resistance of wirebonds increase significantly as a function of time and temperature.
Reduction in contact efficiency when dissimilar metals are in contact.	Thermal cycling causes the reduction in contact efficiency continued cycling expansion and contradiction may cause one part to slightly exceed its material elastic limit at one temperature extreme.
Thermal fatigue cracking.	Stresses imposed in solder joints during thermal cycling where free thermal expansion is partly or entirely restrained.
Cleavage fracture caused due to formation of intermetallics.	Under high temperatures.
Formation of cracks due to board distortion problems.	High temperature may cause the base laminate of PCBs to rise above the glass transition temperature in turn causing the epoxy or the laminate to become soft causing a relaxation of the support medium which is usually woven glass fibre thus causing board distortion.
Failures (open circuit – solder joint) due to difference on expansion and contraction of PCB's , component parts and conformal coating applied to assemblies.	Caused due to temperature cycling during qualification tests.
Degradation of internal copper tracks to plated	Caused by repeated thermal shocks by reworking of

through holes.	joints (each application of hot soldering iron).

Table 5-2: Listing of all possible failures and effects for space electronics

Events of LCEP during which the load occurs	Environment	Principal effects	Typical failures induced
Testing and operation	High temperature	Thermal aging Oxidation Structural change Chemical reaction Softening, melting and sublimation Viscosity reduction/ evaporation Physical expansion outgassing	Insulation failure due to melting Alteration of electrical properties due to changes in resistance On chip failures (metallization migration, Kirkendall voiding in wirebonds, slow trapping, time dependent dielectric breakdown) 1820 Melting of solder joints 1921 Unequal expansion of assemblies leading to fracture 19 Ionic contamination 19
Testing and operation	Low temperature	Increased viscosity and solidification Ice formation Embrittlement Physical contraction Glass transition temperature	Alteration of electrical properties due to changes in resistance Unequal expansion between components and board leading to fracture due to CTE (coefficient of thermal expansion) mismatch Increased brittleness of metals
Storage	High relative humidity	Moisture absorption Chemical reaction Corrosion Electrolysis Metal migration	Metallization corrosion (on-chip) 182223 Delamination 182425 Loss of electrical properties due to corrosion and chemical reactions Cracking in electronic parts due to moisture absorption 161823 Reduction in electrical resistance due to conduction through moisture
Storage	Low relative humidity	Desiccation Embrittlement Granulation	Loss of mechanical strength Structural collapse

			Alteration of electrical properties “dusting”
Operation	High pressure	Compression	Structural collapse Penetration of sealing Interference with function
Operation	Low pressure	Expansion Outgassing Venting Reduced dielectrical strength of air	Fracture of container Explosive expansion Alteration of electrical properties Loss of mechanical strength Insulation breakdown and arc-cover Corona and ozone formation
Operation	Solar radiation	Actinic and physiochemical reactions Embrittlement Thermal gradients	Surface deterioration Alteration of electrical properties Discoloration of materials Ozone formation
Transportation and operation	Sand and dust	Abrasion Clogging	Increased wear Interference with function Alteration of electrical properties
Transportation	Salt spray	Chemical reactions Corrosions Fungus Salt deposits Electrolysis	Increased wear of electronic parts and assemblies Alteration of electrical properties Surface deterioration Increased conductivity Metallization corrosion 16182223
Transportation and Operation	Wind	Force application Vibration Deposit of materials Heat loss (low velocity) Heat gain (low velocity)	Structural collapse Loss of mechanical strength Mechanical interference and clogging 16 Accelerated abrasion 16 Accelerated low temperature effects (low velocity) Accelerated high temperature effects (high velocity)
Operation	FreezingRain	Physical stress Water absorption and immersion Erosion Corrosion	Mechanical stress due to CTE mismatch between structural components Increase in weight Change in electrical properties due to change in resistance/conductivity Delamination 18232425

			Material deterioration On chip failures (metallization corrosion, delamination) 182223
Testing and Operation	Temperature shock	Mechanical stress	Structural collapse or weakening Seal damage
Operation	High speed particles (nuclear irradiation)	Heating Transmutation and ionization	Thermal aging, Oxidation Alteration of chemical, physical and electrical properties Production of gases and secondary particles
Operation	Zero gravity	Mechanical stress Absence of convection cooling	Interruption of gravity dependant functions Aggravation of high temperature effects
Operation	Ozone	Chemical reactions Crazing, cracking Embrittlement Granulation Reduced dielectric strength of air	Rapid oxidation Alteration of chemical, physical and mechanical properties Production of gases and secondary particles
Operation	Explosive decompression	Severe mechanical stress	Rupture and cracking Structural collapse
Operation	Dissociated gases	Chemical reactions Contamination Reduced dielectric strength	Alteration of physical, chemical and electrical properties
Operation	Acceleration	Mechanical stress	Structural collapse
Testing and Operation	Vibration	Mechanical stress fatigue	Loss of mechanical strength Interference with function Increased wear Structural collapse
Operation	Magnetic fields	Induced magnetization	Interference with function Alteration of electrical properties Induced heating

6 Virtual remaining life assessment

The virtual remaining life assessment was performed using calcePWA software (26-36). Virtual remaining life assessment using calcePWA was conducted on two SPA boards (Power Switch Driver Off and Electronics Interface) and on two EEEU boards (Logic & Commutation and Power Conditioner). The steps of the virtual remaining life assessment are as follows:

6.1 Design capture

There was a marked difference in the design capture for the SPA and EEEU boards. The availability of the SPA boards made it possible for dimensions to be measured physically from the boards, however for the EEEU boards this was not possible. For the EEEU parts, which were common with the SPA, the measured data from the SPA were used. For parts that were not common with the SPA, dimensions were taken from the MIL Spec or measured from the assembly drawings. Interconnect related dimensions such as solder joint area, and solder joint height were based on similar components in SPA. Geometric calculations were made to obtain solder dimensions. For example, the solder joint area was found out using assuming that the area difference between the drill hole and the pad was approximately equal to the solder joint area. The drill hole diameter and pad diameter was given in the assembly drawings.

Part Data: The part data entered in calcePWA consisted of information about the package type (e.g., gullwing, insertion mount), case material, placement orientation with regard to end of the board, part dimensions (e.g., length, width and thickness), weight, lead material and all the interconnect dimensions. Table 6-1 gives part data entered for four parts of the Electronics Interface board. The X and Y-axes were assigned by the user of

the software. Approximations were done for the part locations on the board based on the board assembly drawings, this was done to prevent part overlap in the board models.

Table 6-1: Example of part data entered for Electronic Interface board parts

MD Robotics part identification number / Attributes	Q2	U16	R66	D7
Description	Transistor	Comparator	Transistor	Diode
Interconnection type	Insertion mount	Gullwing	Axial	Axial
Center of component to edge of board along X axis	35	122.75	102.72	47.45
Center of component to edge of board along Y-axis	80.55	71.78	99.62	88.32
Solder bond area (mm2)	1.307	1.535	1.307	1.307
Underfill material	Silicon rubber	Kapton tape	Solithane	Solithane
Standoff height (mm)	2.08	0.06	0.177	0.18
Solder joint height (mm)	0.50	0.20	0.559	0.559
Power dissipated (Watts)	0.36	0.15	0	0
Length (mm)	4.5	4.5	3.9	4.5
Width (mm)	5.9	6.4	1.3	1.5
Thickness (mm)	6	6	1.3	1.5
Lead material	Alloy 42	Alloy 42	Alloy 42	Alloy 42

Interconnect data: The interconnect data entered in calcePWA is included in part data and has information about the components standoff height, solder joint height, solder joint bond area, interconnection type (e.g., Insertion mount, gullwing), interconnection format (e.g., single-inline, dual inline) and interconnect dimensions (the dimensions of the leads, radius of bends, the thickness variations). Table 6-2 and Figure 6-1explain the various

interconnect dimensions for Insertion mount and interconnects, Table 6-3 and Figure 6-2 provide the same for gullwing interconnects.

Board data: The board data entered in calcePWA include information about the board layers, thickness of layers, layer materials, metallization material, and percent metallization. The laminate material for all the four boards is polyamide. Copper is the metallization material and based on the surface area covered by copper on the board, the percentage of metallization is estimated. Table 6-4 through Table 6-7 give the board layers and the percentage of copper present among these layers based on the surface area occupied by it. There is less than 100% copper even on the copper layers. To ensure that the total volume percentage adds up to 100% for each layer, it is assumed that the rest of the material is polyamide and polyamide is taken as the board material. The copper and polyamide material combination is used to estimate aggregate thermo -physical properties of the layers.

Table 6-2: Interconnect dimensions for gullwing components

Lead dimensions	Explanations of the dimensions
L2	Length between package body and transition point
L1	Lead length after the transition point
W2	Lead width prior to transition point
W1	Lead width after to transition point
T2	Lead thickness of segment 2
T1	Lead thickness of segment 1

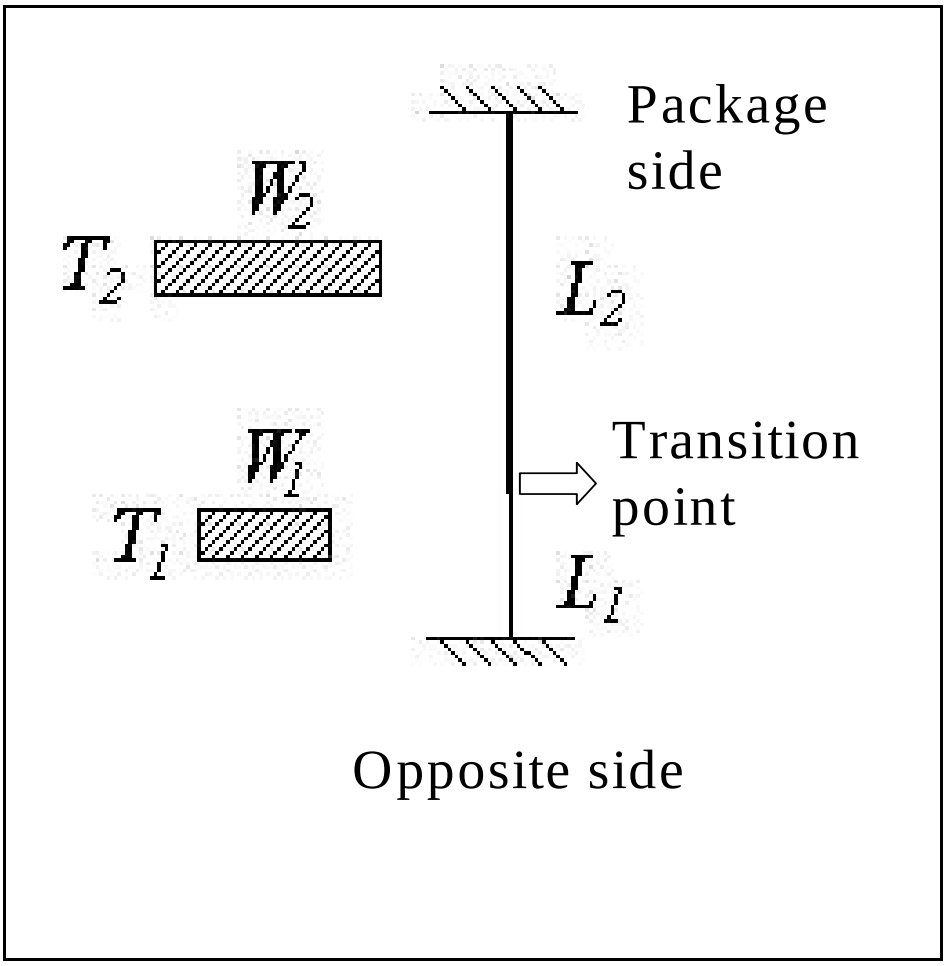


Figure 6-1: Interconnect dimensions for Insertion mount components

Table 6-3: Interconnect dimensions for gullwing components

Lead dimensions	Explanation of the dimensions
L3	Length between package body and 1st bend
R2	Radius of curvature of 1st bend in lead
L2	Lead length between 1st bend and transition point
L1	Lead length after transition point and before last bend
Gullwing foot length	Length on the pad after the bend
R1	Radius of curvature at the foot
W1	Lead width after to transition point
T1	Lead thickness
W2	Lead width prior to transition point
T2	Lead thickness

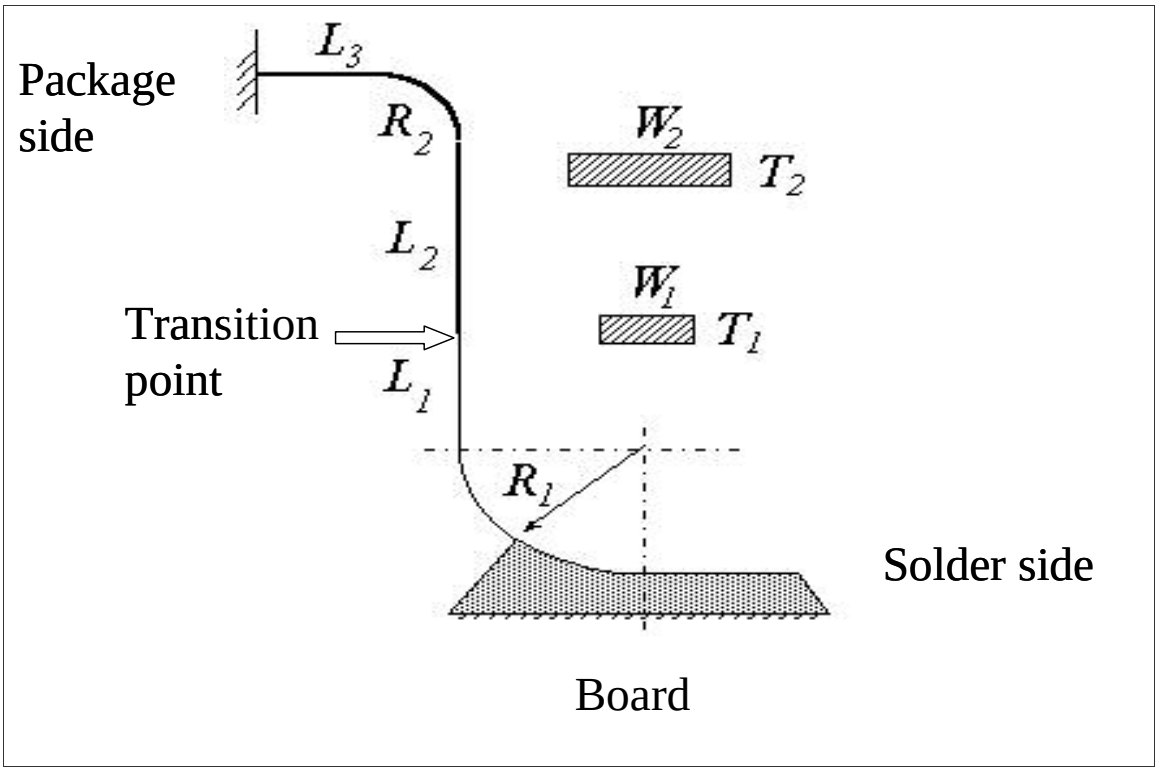


Figure 6-2:Interconnect dimensions for gullwing components

Table 6-4: Layers and materials of Power Switch Driver off board (SPA)

Layers	Layer material	Thickness (µm)	Metallization material	Percent metallization
1	Polyamide (between copper traces)	0.889	Copper	95
2	Polyamide (between copper layers)	38.481	Copper	0
3	Polyamide (between copper traces)	0.889	Copper	32

Table 6-5: Layers and materials of Electronic Interface board (SPA)

Layers	Layer material	Thickness (µm)	Metallization material	Percent metallization
1	Polyamide (between copper traces)	0.889	Copper	20
2	Polyamide (between copper	38.481	Copper	0

	layers)			
3	**Polyamide (between copper traces)**	**0.889**	**Copper**	**98**
4	**Polyamide (between copper layers)**	**76.962**	**Copper**	**0**
5	**Polyamide (between copper traces)**	**0.889**	**Copper**	**98**

Table 6-6: Layers and materials of Logic and Commutation board (EEEU)

Layers	Layer material	Thickness (µm)	Metallization material	Percent metallization
1	**Polyamide (between copper traces)**	**0.889**	**Copper**	**20**
2	**Polyamide (between copper layers)**	**38.481**	**Copper**	**0**
3	**Polyamide (between copper traces)**	**0.889**	**Copper**	**95**
4	**Polyamide (between copper layers)**	**76.962**	**Copper**	**0**
5	**Polyamide (between copper traces)**	**0.889**	**Copper**	**20**

Table 6-7: Layers and materials of Power Conditioner assembly board (EEEU)

Layers	Layer material	Thickness (µm)	Metallization material	Percent metallization
1	**Polyamide (between copper traces)**	**0.889**	**Copper**	**95**
2	**Polyamide (between copper layers)**	**38.481**	**Copper**	**0**
3	**Polyamide (between copper traces)**	**0.889**	**Copper**	**15**

6.2 Assumptions and difficulties in design capture for calcePWA

When complete engineering data was not available, assumptions were made by CALCE and MD Robotics regarding inputs to the calcePWA models. The assumptions were made in those places where it was difficult or impossible to obtain or measure the dimension due to various constraints (e.g., presence of solithane layers)

Assumptions made and changes made to be suited for modeling in calcePWA are:

Early in the process, it was found that the assembly-drawing dimension could not be treated as "to the scale." For the SPA boards, the part dimensions were measured wherever possible. The transformers present in the Power switch driver off board were cylindrical in shape but had to be modeled as square because of inability of calcePWA to model cylindrical shapes. Figure 6-3 and Figure 6-4 show how the transformer is modeled as a square shape. These types of modifications were introduced by CALCE in other product models. Based on the previous analysis it was found that this assumption does not introduce significant errors in life calculation. The part dimensions of the two EEEU boards (only those not common to the two SPA boards) were obtained through measurements from part drawings with the assumption that the dimensions in drawings were to scale. MD Robotics suggested that this level of error in dimensions will be acceptable. Power dissipation values were estimated by MD Robotics through voltage derating information, empirical circuit analysis, and other documents. Military specifications for parts were used for obtaining some dimensions. It was found that the military specifications did not have unique part dimensions and could only be used in conjunction with other documents.

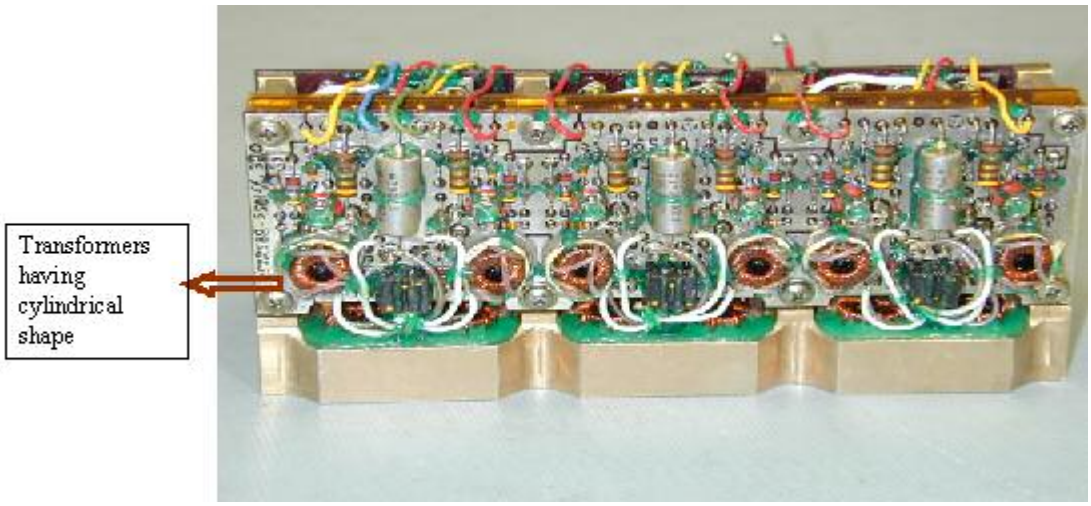


Figure 6-3: Power Switch Driver Off board

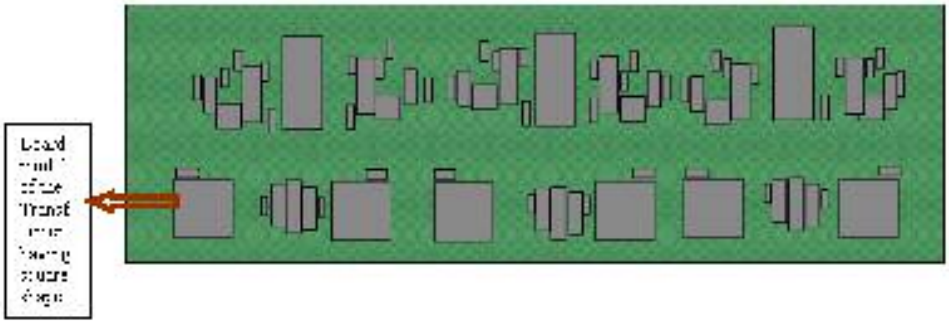


Figure 6-4: Board model of Power Switch driver off board

6.3 Life Cycle Environment and Operation Assessment

The life cycle profile of the EEEU and SPA boards go through various thermal and vibration analyses. Life cycle environment and operation assessment transformation process of virtual remaining life assessment results in temperature and displacement profiles under various load conditions that are used in damage simulation.

6.3.1 Thermal Loads

calcePWA thermal analysis is based on the control volume theory and uses a finite difference approach. The thermal analysis program automatically discretizes the board,

based on the number of layers through the thickness and grid size specified on the planar surface of the board. The discretization process creates a three dimensional matrix of the nodes representing the cubic sections of each layer. Thermal resistances for each node are based on the layer material and the material inserts within the cubic region defined by individual nodes. When the thermal analysis is performed, the program calculates the node temperatures for each layer. The thermal analysis assumed conduction as the primary cooling method. The powered on thermal profiles need the boards thermal analysis results at the temperature limits (e.g., qualification –36 and 81ºC).

The temperatures for which boards are modeled are specified as uniform boundary conditions along all the edges. As an example, Figure 6-5 shows the temperature distribution across the Electronics Interface board at 81ºC.

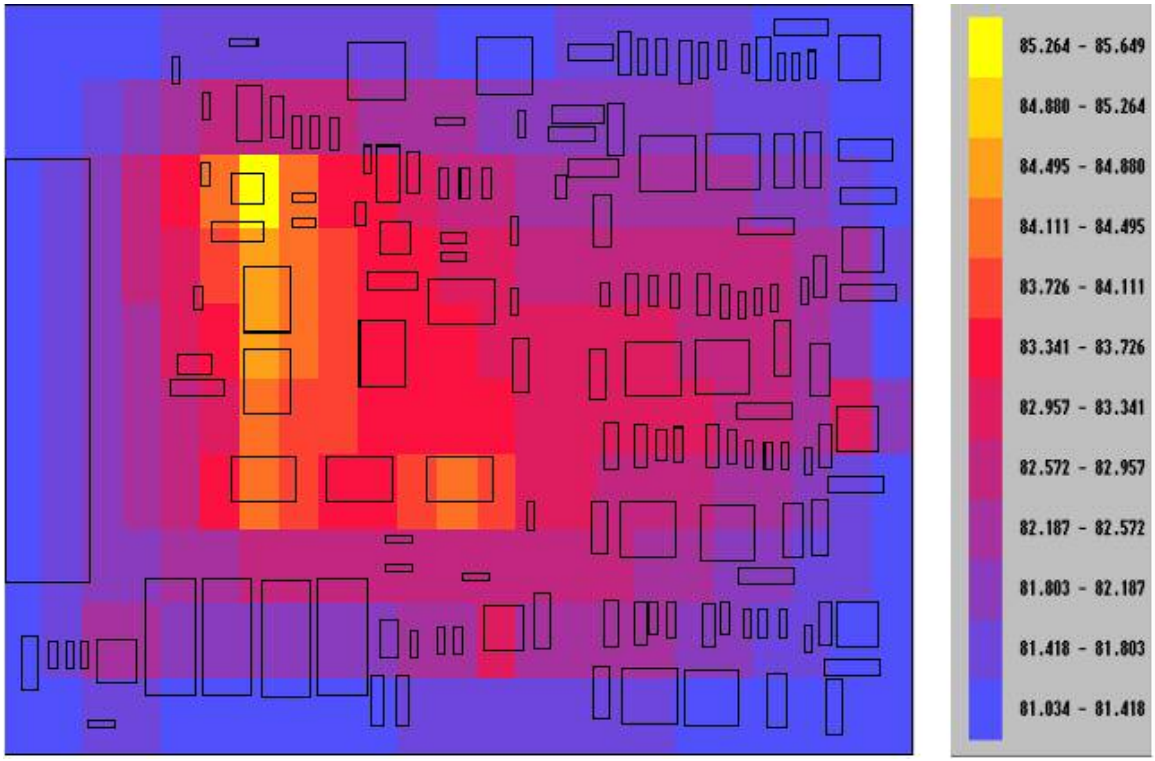


Figure 6-5: Temperature distribution across Electronics Interface (SPA) at 81º C.

6.3.2 Vibration Loads

In calcePWA vibration analysis tool, the PWB is divided into number of Kirchoff plate elements (elements with three degrees of freedom, out of plane displacement, and rotation about both in-plane axes). The stiffness matrix and the consistent mass matrix of each material are determined using material properties information and variational methods. The elemental matrices are assembled into respective global matrices for the whole structure using material properties information and variational methods. Once the global stiffness and the mass matrices are calculated, the natural frequencies and the mode shapes are determined using eigenvalue and eigenvector extraction techniques. The loading conditions are based on how the boards are fastened to the whole unit. The electronics interface board is fastened at 8 points by screws to the unit; these 8 points were taken in calcePWA as simply supported loading conditions. The conditioner is fixed rigidly over a continuous length so the simply supported section is modeled across the complete connector length. Figure 6-6 shows the loading conditions of the electronic interface boards. Figure 6-7 shows locations of maximum curvature of the same board at natural frequency of 807 Hz, the maximum curvature is observed at the support points, the components near these points have the maximum vibration induced stress. Figure 6-8 shows board displacement distribution across that board.

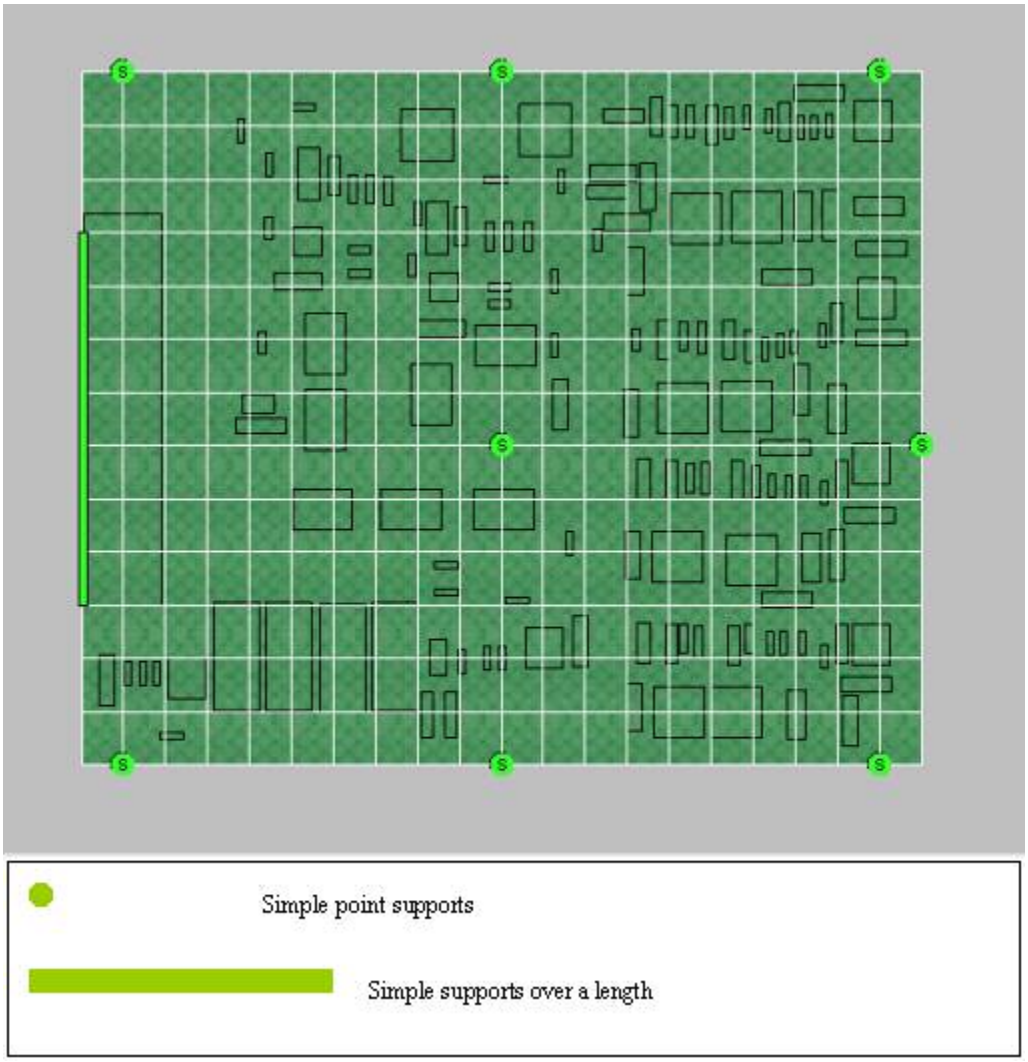


Figure 6-6: Position of supports for Electronics Interface

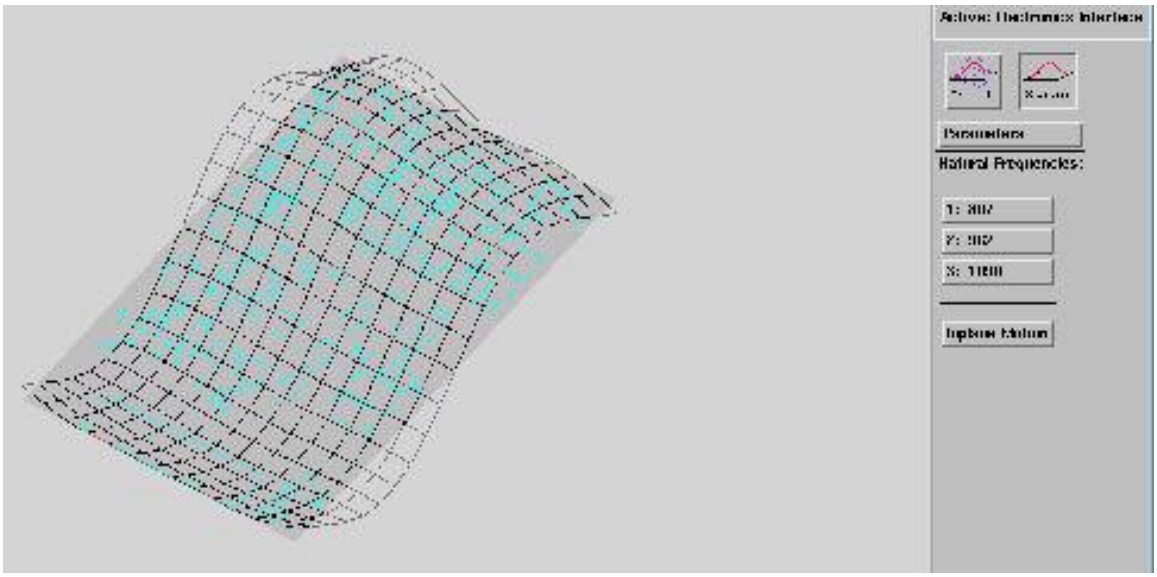


Figure 6-7: Vibration modes at natural board frequencies (807 Hz) of Electronics Interface (SPA) board

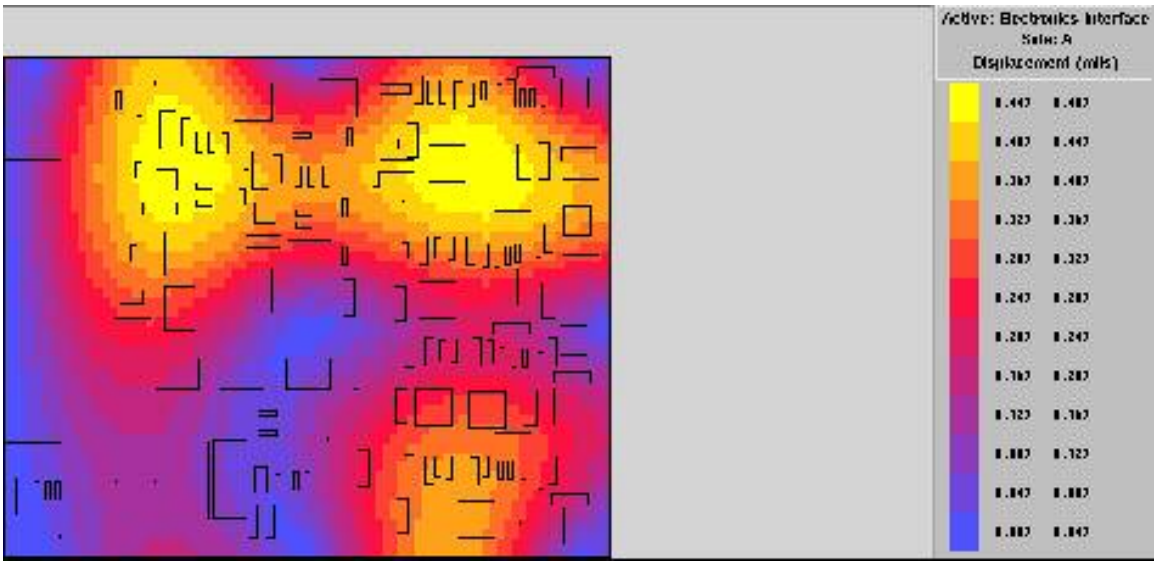


Figure 6-8: Board displacement due to vibration of Electronics Interface (SPA) board

6.4 Failure Risk Assessment

calcePWA simulation results list damage to individual parts in terms of damage ratio (DR). Damage ratio is defined as the ratio of the number of cycles experienced to estimated number of cycles to failure. When the DR value reaches one, the component is predicted to fail. Table 6-9 through Table 6-12 list summary of results for calcePWA simulation. The first column of each table provides the MD Robotics part identification number. The second and third column shows the damage ratio for the part with a precision to two decimal points for 20 and 40 years respectively. The fourth column shows the interconnection type. The last column shows the calcePWA failure model that is used to calculate the primary damage. In each table, the 10 parts with maximum damage ratios are listed for each board starting with the part with maximum damage ratio. Table 6-9 details the simulation results for the Power Switch Driver Off board (SPA) for the first 20 and 40 years respectively. For the first 20 years, the life cycle segment that causes cycle that causes the maximum damage is the qualification

temperature cycle. (The maximum accumulated damage is for capacitor N3C4, the other listed components have damage ratio in same order of magnitude). The cycles to failure estimate for the qualification temperature cycle is 4256.51 and its contribution to damage ratio is 0.01186 in the first 20 years (54.18% of total DR). Similarly, the total DR can be found out by adding the individual damage ratios caused by each life profile segment, the storage has a DR of 0.006721, acceptance has a DR of 0.002935, the ferry flight has a DR of 0.000226, all the four operation cycles have a DR of 1.4812E-05, 4.702-E-05, 6.9076E-05, 2.1291E-05 respectively. Summing all of them up, the total DR for 20 years is 0.02189. The vibration DR is not taken into account because the DR is zero for all vibration cycles. For the 40 years of operation, the storage temperature cycle becomes the dominant contributor to the total damage ratio. Table 6-10 details the simulation results for the Electronics Interface board (SPA) for the first 20 and 40 years respectively. The life cycle segment that causes cycle that causes the maximum damage in the first 20 years is the qualification temperature cycle. (The maximum accumulated damage is for connector P1, the other listed components have damage ratio in same order of magnitude). The cycles to failure estimate for the qualification temperature cycle is 786 and its contribution to damage ratio is 0.06424 in the first 20 years (95% of DR). The qualification temperature cycle remains the most dominant one after 40 years of operation too. Table 6-11 details the simulation results for the Logic and Commutation board (EEEU) for the first 20 and 40 years respectively. The life cycle segment that causes cycle that causes the maximum damage for the first 20 years is the qualification temperature cycle. (The maximum accumulated damage (0.15) is for the connector P1, the next 9 components have damage ratio significantly less than P1 and those are all in

same order of magnitude). The cycles to failure estimate for the qualification cycle is 405, its damage ratio is 0.1247 (85.62% of DR). The qualification cycle remains the most dominant one after 40 years of operation too. The failure model details are provided in appendix A. Table 6-12 details the simulation results for the Power Conditioner board for the first 20 and 40 years respectively. The life cycle segment that causes cycle that causes the maximum damage is the qualification temperature cycle. (The maximum accumulated damage is for capacitor C5, the next 9 components have damage ratio in same order of magnitude). The cycles to failure estimate, for the qualification cycle is 4.669E+03, and its contribution to damage ratio is 0.0108 (53% of DR). For the 40 years of operation, the storage temperature cycle becomes the dominant contributor to the total damage ratio. The parts P1 of the Electronics Interface board and P1 of the Logic and commutation board are similar, but they have differing damage ratios because of the differences in their physical attributes (e.g., size of the connectors, number of pins). The factors that made a difference in the damage ratio are the qualification cycle and acceptance cycle. The qualification cycle produces a damage ratio of 0.064 in the logic and commutation while it is 0.014 for the Electronics Interface board, the acceptance cycle has a damage ratio of 0.019 for the Logic and Commutation board while it is 0.002 for the Electronic Interface board the combination of these two factors make a difference in the DR. The comparisons between the two connectors are shown in Table 6-8.

Table 6-8: Comparison of the two P1 Connectors on SPA and EEEU Boards

Attributes	P1 of the SPA	P1 of EEEU
Length (mm)	60.5	70
Width (mm)	12.1	12.1
Number of pins	40	50
Joint height (mm)	0.559	0.559
Package CTE (°C)	2.34E-05	2.34E-05

Board CTE (ºC)	**1.566E-05**	**1.566E-05**

Table 6-9: Damage assessment for Power switch driver off (SPA) board for first 20 and 40 years

MD Robotics part identification number	Damage ratio for 20 years operation	Damage ratio for 40 years operation	Interconnection type
N3C4	0.02189	0.03133	Insertion mount
N5C4	0.02	0.03	Insertion mount
N1C4	0.02	0.03	Insertion mount
N6C2	0.02	0.03	Insertion mount
N1C2	0.02	0.03	Insertion mount
N4C2	0.02	0.03	Insertion mount
N3C2	0.02	0.03	Insertion mount
N5C2	0.02	0.03	Insertion mount
N2C2	0.02	0.03	Insertion mount
N5C3	0.01	0.01	Insertion mount

Table 6-10: Damage assessment for Electronics Interface board (SPA) for first 20 and 40 years

MD Robotics part identification Number	Damage ratio for 20 years operation	Damage ratio for 40 years operation	Interconnection type
P1	0.0678	0.07121	Gullwing
C9	0.02	0.03	Insertion mount
C2	0.02	0.03	Insertion mount
C7	0.02	0.03	Insertion mount
C4	0.02	0.03	Insertion mount

C6	**0.02**	**0.03**	**Insertion mount**
C11	**0.02**	**0.03**	**Insertion mount**
C33	**0.02**	**0.03**	**Insertion mount**
C37	**0.02**	**0.03**	**Insertion mount**
C31	**0.02**	**0.03**	**Insertion mount**

Table 6-11: Damage assessment for Logic and Commutation (EEEU) for first 20 and 40 years

MD Robotics part identification number	Damage ratio for 20 years operation	Damage ratio for 40 years operation	Interconnection type
P1	**0.14232**	**0.15967**	**Gullwing**
C11	**0.02**	**0.03**	**Insertion mount**
C18	**0.02**	**0.03**	**Insertion mount**
C22	**0.02**	**0.03**	**Insertion mount**
C16	**0.02**	**0.03**	**Insertion mount**
C19	**0.02**	**0.03**	**Insertion mount**
C4	**0.02**	**0.03**	**Insertion mount**
C15	**0.02**	**0.03**	**Insertion mount**
C14	**0.02**	**0.03**	**Insertion mount**
C34	**0.02**	**0.03**	**Insertion mount**

Table 6-12: Damage assessment for Power conditioner board (EEEU) for first 20 and 40 years

MD Robotics part identification Number	Damage ratio for 20 years operation	Damage ratio for 40 years operation	Interconnection type
C5	**0.02044**	**0.02958**	**Insertion**

			mount
C12	**0.02**	**0.03**	**Insertion mount**
C1	**0.02**	**0.03**	**Insertion mount**
C7	**0.02**	**0.03**	**Insertion mount**
C3	**0.02**	**0.03**	**Insertion mount**
C4	**0.02**	**0.03**	**Insertion mount**
C2	**0.02**	**0.03**	**Insertion mount**
C13	**0.02**	**0.03**	**Insertion mount**
C9	**0.02**	**0.03**	**Insertion mount**
C11	**0.02**	**0.03**	**Insertion mount**

7 Accelerated testing

Acceleration factor for estimating an enhanced rate of damage accumulation on the SPA board was calculated using the simulation results of the two SPA boards. The actual accelerated testing was done at MDR the reason being limitations like limited thermal chamber time, longer dwell times (more time for cables to be connected) to be used so that it is possible to perform a full functional test at maximum and minimum temperature. The other reason was that we wanted to do accelerated thermal cycling to the point of failure of the part so accuracy of calcePWA simulation results could be established but MDR didn't want to go the full length because they just wanted to simulated the life for next 20 years.

Vibration accelerated testing done at MDR

Vibration profiles from 2 sets of tests conducted were:

③ The first is the 1g (input) sine sweep. The highest peak for the 309 unit was a ~4G peak around 1400 Hz. The highest peaks for 305 were a ~14G peak around

700 Hz and a ~12G peak around 1100 Hz). The highest peaks for 212 were 2Gs peaks around 650 Hz and 1400 Hz.

- ③ The second test was a 12.8Grms input profile (using the E/E QVT profile). Note that the peaks roughly correspond to the locations seen in the sine sweep profiles. The vibration seen by the accelerometers mounted to the SPAs were 15.96G for SPA 309, 25.31G for SPA 305, and 14.74G for SPA 212.

Observations of the tests were :

- ③ The SPA on face B (y-axis) generated the most amplification in the input vibration. This would have been due to it being cantilevered slightly on the side and the narrow width of the SPA's base in the drive axis for this configuration.
- ③ The SPA on face C was also cantilevered, but was driven in the length of the base, and had more stability which prevented the vibrations from being amplified as much.

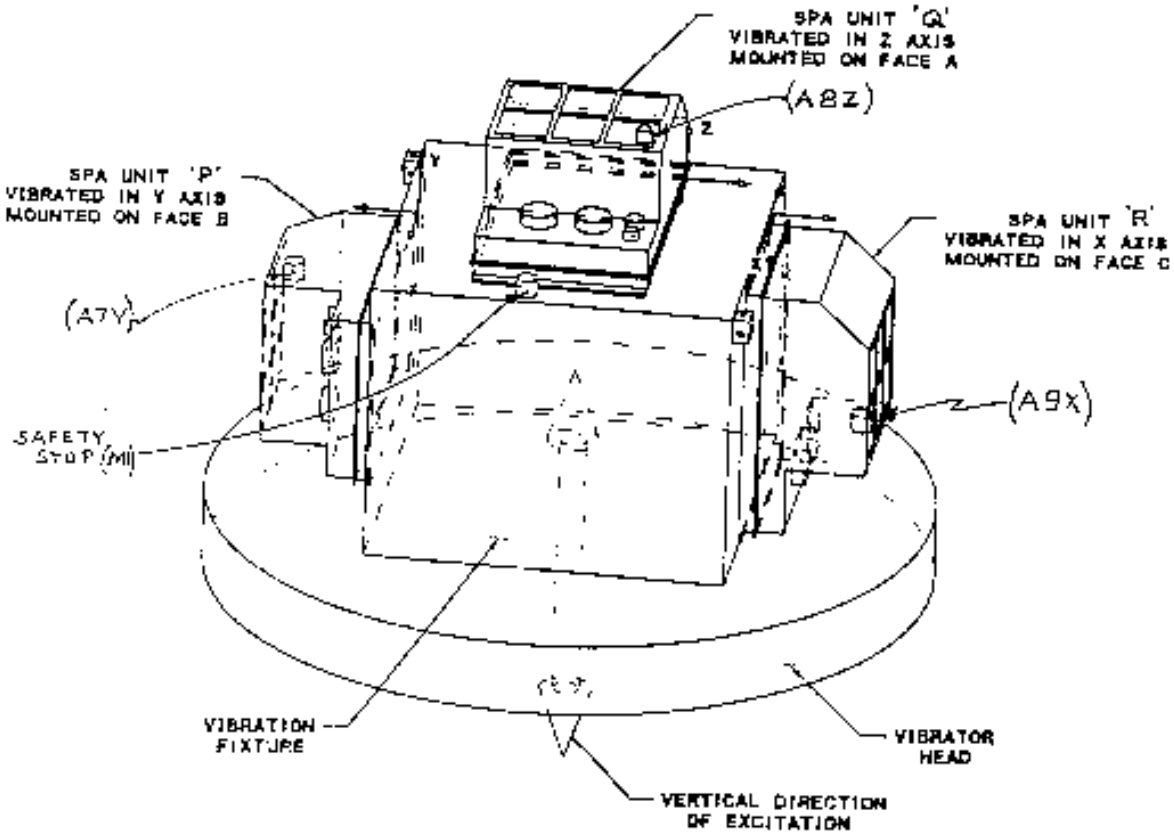


Figure 7-1 : In picture above, the vibration axes are shown for the three SPAs that were vibrated. For the vibration profiles sent, the SPA 212 is on the top of the cube (unit Q / z-axis / face A), SPA 305 is on the left-hand side (unit P / y-axis / face B), and SPA 309 is on the right-hand side (unit R / x-axis / face C).

③ The SPA on top (face A / z-axis) had no significant cantilevering and did not greatly amplify the vibration input.

Conclusions made from the testing were :

③ Amplifications were caused by the physical design of the units (materials and shape).

③ The amplification seen by the unit on top (z-axis) was not very significant, nor was there significant amplification for the x-axis unit. Using this frame of reference, 7/10 SPA boards are in the x-y plane and the remaining 3 are the (small, well-secured) Power Switch boards in the y-z plane. Although the y-axis

unit has significant amplification, this will not impact the boards since it is in-plane with the boards.

Table 7-1 Calculation of Remaining Life for boards

Unit - Board and Critical Part	DR for 1st 20 years (with qualification)	DR for each subsequent 20 years	Life Remaining for Board
SPA - Power Switch Driver Off board (N3C4)	0.017	0.009	2184 years
SPA - Electronics Interface board (P1)	0.038	0.003	6413 years
EEEU - Logic & Commutation board (P1)	0.089	0.014	1301 years
EEEU - Power Conditioner board (C5)	0.016	0.008	2460 years

THERMAL

The thermal accelerate life testing was composed of three cycles of Baseline tests (with 157-minute plateau durations) and 24 cycles of Functional tests (with 74-minute plateau durations). The time/cycle totals were 464 minutes for each Baseline cycle and 298 minutes for each Functional cycle. Note EEEU underwent qualification testing in the first 20 years of life. Three of the other EEEUs have not undergone qualification testing. Applying the Acceleration Factors (AFs) from the revised Tables 29 through 32 above, the total accelerated time accumulated would be equal to:

For EEEU:

Functional cycles to make up 1st 20-years = 20*365*24*60/2854.587722/298 = 12.35736 cycles

(12.35736 Functional cycles * 298 minutes * 2854.587722) + (11.64264 Functional cycles * 298 minutes * 39977.66579) + (3 Baseline cycles * 464 minutes * 29781.26944) = 362.77 years

For other EEEUs (without Qualification testing):

Functional cycles to make up 1st 20-years = 20*365*24*60/47555.62896/298 = 0.7417664 cycles

(0.74177 Functional cycles * 298 minutes * 47555.62896) + (23.25823 Functional cycles * 298 minutes * 39977.66579) + (3 Baseline cycles * 464 minutes * 29781.26944) = 626.05 years

SPA passed its first direct drive test at the hot temperature during the first (Baseline) cycle. Applying the Acceleration Factors and assuming that the damage accumulated was 0.75 of a Baseline cycle, the total accelerated time accumulated at that point would be equal to:

For EEEU:

(0.75 Baseline cycles * 464 minutes * 2126.518505) = 1.41 years

For other EEEUs (without Qualification testing):

Baseline cycles to make up 1st 20-years = 20*365*24*60/35426.45554/464 = 0.639499 cycles

(0.639499 Baseline cycles * 464 minutes * 35426.45554) + (0.110501 Baseline cycles * 464 minutes * 29781.26944) = 22.91 years

SPA failed its second direct drive test at the hot temperature during the third cycle. Applying the Acceleration Factors from the revised Tables 29 through 32 above, and assuming that the damage accumulated was 1 Baseline cycle and 1.75 Functional cycles, the total accelerated time accumulated at that point would be equal to:

For EEEU:

(1.75 Functional cycles * 298 minutes * 2854.587722) + (1 Baseline cycle * 464 minutes * 2126.518505) = 4.71 years

For other EEEUs (without Qualification testing):

Functional cycles to make up 1st 20-years = 20*365*24*60/47555.62896/298 = 0.7417664 cycles

(0.74177 Functional cycles * 298 minutes * 47555.62896) + (1.00823 Functional cycles * 298 minutes * 39977.66579) + (1 Baseline cycle * 464 minutes * 29781.26944) = 69.14 years

8 Conclusions

It is difficult to rework or reassemble the SPA assembly. Assuming that the EEEU assembly is built in similar manner, the EEEU will be difficult to rework or reassemble. The units are difficult to reassemble once taken apart due to limited physical working dimensions. The wires and components, in particular transformers and transistors, on the boards are secured with an adhesive that makes it difficult to remove them without damaging. There were no defects found in any of the boards or components during the external visual inspection when examined according to NASA and IPC standards. From the assessment of the environmental and operational profile, it is seen that large majority

(>90%) of the time is spent in non-operating, controlled storage condition. The damage accumulated at interconnects after 20 years and 40 years of use is low with damage ratio below 0.05 for all parts except two. After 20 years, the highest damage ratio of 0.15 was observed on a gullwing connector of the Logic and Commutation board of EEEU. This analysis assumed nominal quality of boards, parts, and interconnects. The virtual qualification results predict that the remaining life of the interconnects is greater than 20 years (low damage ratios are found for 20 and 40 years of operation). The results of the board cross-section may impact the life predictions from the virtual qualification but that cannot be quantified without test results. Qualification thermal cycling was the most damaging environment for all components in all the four boards for the first 20 years of operation, while the damage caused by vibration was negligible. In the 40 years life profile, the effects of storage environment and operation cycles (number 2) begins to be dominant for some of the parts. From the simulation results, it is decided by MD Robotics that temperature cycling -50ºC to 100ºC is the most suitable accelerated test condition for accelerating damage accumulation. From visual inspection results, it can be seen that PWB assemblies are robust and would probably not suffer from any failure mechanisms normally incurred during storage such as electrostatic discharge, corrosion due to moisture ingress and, fatigue or cracking due to thermal excursions. Cross section of the boards and interconnect revealed several quality problems such as voids in solder joints, pin misalignment, nodules in the plated insertion mount (PTH) walls, and copper foil thinning (Thinned area can cause a large increase in current density, and violate specifications. Further cross-sectional analysis is necessary to estimate the size of the affected area and if there area other existing similar defects, and then enable one to make

a prediction regarding the impact on reliability due to these defects).Results of the component DPA show they meet Mil-Std-1580 requirements.No non-operating reliability issues have been identified from the visual and destructive inspection. There is latent reliability issue with at least one of the tantalum capacitors. Results of accelerated life test on tantalum capacitors suggest that one of the parts evaluated was potentially improperly labeled with respect to voltage rating or exhibits premature failure against established reliability level.

9 Future Work

To obtain a better confidence on the remaining life of the system, the following work will be necessary:

- ③ More board cross sectioning for better understanding of the board quality and the interconnect characteristics.
- ③ The DPA of the components in significant numbers for better estimate of the component degradation/quality patterns.
- ③ Component level virtual remaining life assessment will be necessary.
- ③ Testing of boards and components to failure to validate virtual remaining life assessment.

10 Contributions

A remaining life assessment process has been developed which could be used for other systems and fields like avionics. The remaining life assessment used in this thesis uses the principle of stastical estimate, which is basically finding a small part of the system, that is the representative of the whole system. In our case we choose the EEEU unit as the representative of the SRMS. This concept can be used for RLA of other big systems and

lot of time and money can be saved. The RLA process once done on the system gives a clear perspective of the failures and the causes of the failures, hence the results of the RLA process can be used as a benchmark for better design and reliability. The life cycle phases most detrimental to the electronics of the shuttle was determined and this information is helpful in design improvements for future space operations.

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