# ABSTRACT


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| Title of Document: | HIGHLY EFFICIENT SIC BASED ONBOARD CHARGERS FOR PLUG-IN ELECTRIC VEHICLES |
| | Haoyu Wang, Doctor of Philosophy, 2014 |
| Directed By: | Professor Alireza Khaligh<br>Department of Electrical and Computer Engineering |

Grid-enabled plug-in electrified vehicles (PEVs) are deemed as one of the most sustainable solutions to profoundly reduce both oil consumption and greenhouse gas emissions. One of the most important realities, which will facilitate the adoption of PEVs is the method by which these vehicles will be charged. This dissertation focuses on the research of highly efficient onboard charging solutions for next generation PEVs.

This dissertation designs a two-stage onboard battery charger to charge a 360 V lithium-ion battery pack. An interleaved boost topology is employed in the first stage for power factor correction (PFC) and to reduce total harmonic distortion (THD). In the second stage, a full bridge inductor-inductor-capacitor (LLC) multi-resonant converter is adopted for galvanic isolation and dc/dc conversion. Design considerations focusing on reducing the charger volume, and optimizing the conversion efficiency over the wide battery pack voltage range are investigated. The

designed 1 kW Silicon based charger prototype is able to charge the battery with an output voltage range of 320 V to 420 V from 110 V, 60 Hz single-phase grid. Unity power factor, low THD, and high peak conversion efficiency have been demonstrated experimentally.

This dissertation proposes a new technique to track the maximum efficiency point of LLC converter over a wide battery state-of-charge range. With the proposed variable dc link control approach, dc link voltage follows the battery pack voltage. The operating point of the LLC converter is always constrained to the proximity of the primary resonant frequency, so that the circulating losses and the turning off losses are minimized. The proposed variable dc link voltage methodology, demonstrates efficiency improvement across the wide state-of-charge range. An efficiency improvement of 2.1% at the heaviest load condition and 9.1% at the lightest load condition for LLC conversion stage are demonstrated experimentally.

This dissertation proposes a novel PEV charger based on single-ended primary-inductor converter (SEPIC) and the maximum efficiency point tracking technique of an LLC converter. The proposed charger architecture demonstrates attracting features such as (1) compatible with universal grid inputs; (2) able to charge the fully depleted battery pack; (3) pulse width modulation and simplified control algorithm; and (4) the advantages of Silicon Carbide MOSFETs can be fully manifested. A 3.3 kW all Silicon Carbide based PEV charger prototype is designed to validate the proposed idea.

# HIGHLY EFFICIENT SIC BASED ONBOARD CHARGERS FOR PLUG-IN ELECTRIC VEHICLES

By

Haoyu Wang

Dissertation submitted to the Faculty of the Graduate School of the
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# Dedication

To my parents and my wife.

# Acknowledgements

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# Chapter 1 Introduction

## *1.1. Background*

The gasoline price has kept on increasing since early 1990s. According to the Energy Information Administration (EIA) survey studies from 1990 to 2013, Fig. 1.1, the gasoline price has tripled since 1990. The rise of gas price increases the cost of conventional transportation.

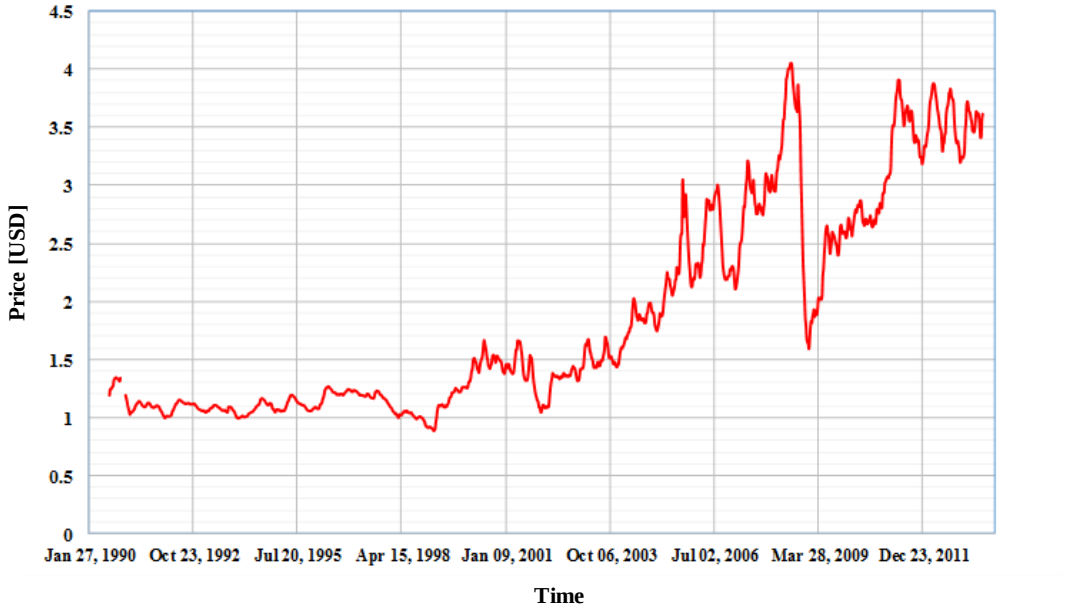



Fig. 1.1. Weekly U.S. regular conventional retail gasoline prices.

On the other hand, with the evolvement of material science and battery manufacturing technology, the price of a battery is decreasing gradually, and the corresponding energy density is increasing annually. This is demonstrated in Fig. 1.2 [1]. These trends are propelling the transition of transportation from conventional internal combustion engine (ICE) to the next generation electrified drive train

systems. Consequently, more and more efforts are being involved into developing advanced electric vehicle (EV) and plug-in hybrid electric vehicle (PHEV) technologies.

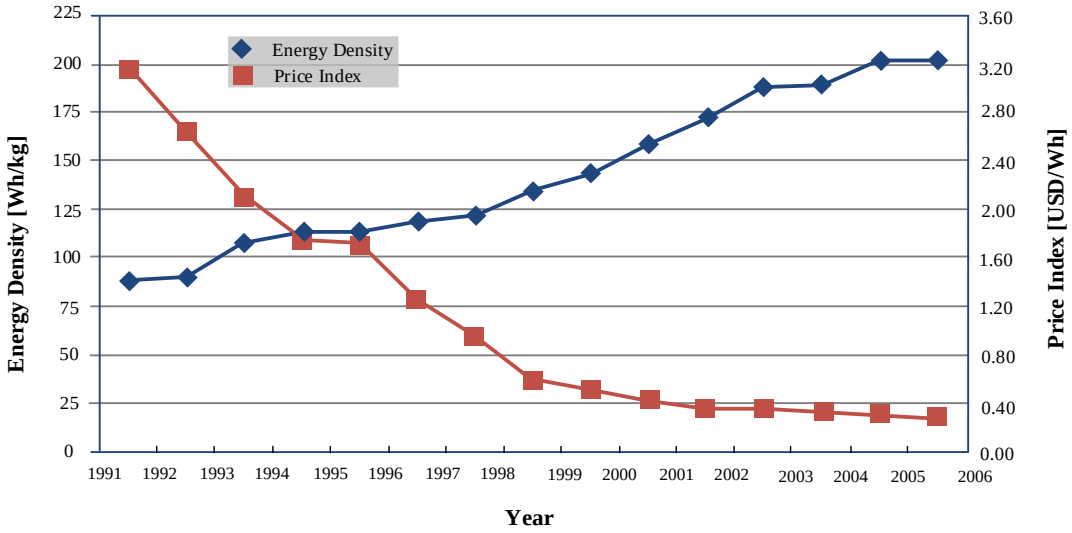



Fig. 1.2. Li-ion pricing and energy density (1991-2006)[1].

In the United States, an official domestic goal of putting one million electric vehicles on the road by 2015 has been established [2]. Different public policies have been implemented by governments to encourage the electrification of transportation system [3]. Fig. 1.3 demonstrates the projected annual light-duty electric vehicles sales worldwide. In this chart, In comparison with 2011, the sale of electric vehicles (EV) is predicted to increase by 46 times by 2017.

With the reduction of battery price, the price gap between conventional ICE vehicles and electric vehicles would become narrower. Electric vehicles are becoming more affordable. However, increasing the charging speed or reducing the charging time become one of the major concerns of ordinary consumers. Conventional ICE vehicles take 3 to 5 minutes to refuel the tank, while electric vehicles take a much

longer time to recharge the battery pack. Moreover, the lack of charging facilities also prevents the widespread adoption of electric vehicles [4].

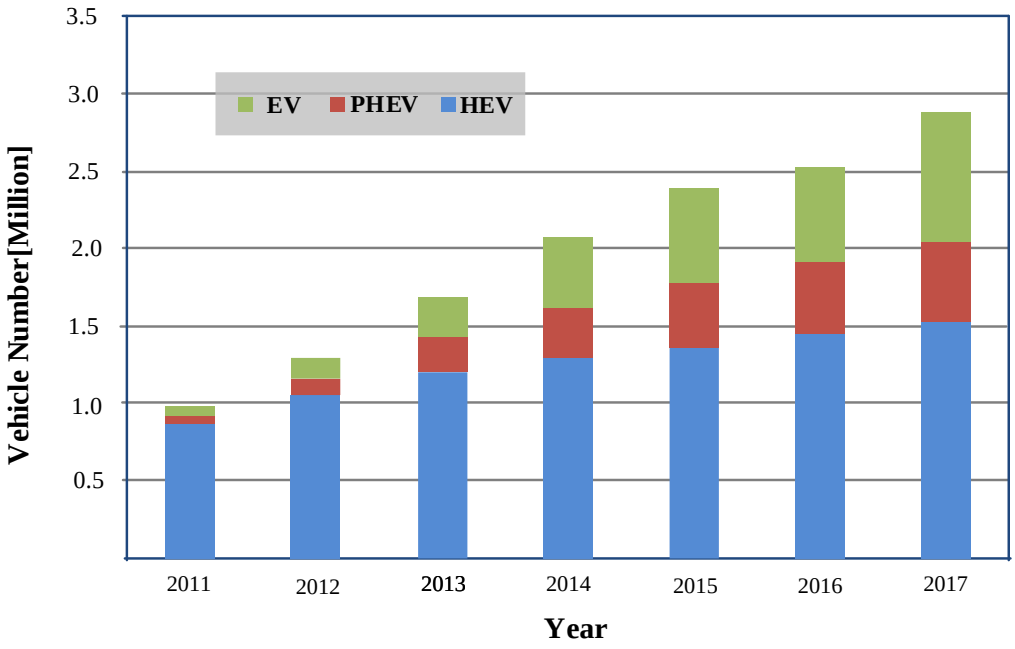



Fig. 1.3. Annual sales of light-duty electric vehicles worldwide (2011-2017) [5].

## *1.2. Charging Infrastructures and Charging Profile of Li-ion Battery*

Table 1-1 Charging power levels (Based in part on [6])

| Charging level | Power supply | Charging Power | Cost of charging infrastructure | Miles of Range for 1 hour of charge | Charging Time | |
|---|---|---|---|---|---|---|
| | | | | | EV | PHEV |
| Level 1 | 120 VAC Single Phase | 1.4 kW @ 12 amp | $500-$800 | 3~4 miles | ~17 hrs | ~7 hrs |
| Level 2 | 240 VAC Single Phase (Up to 80 amps) | 3.3 kW (onboard) 6.6 kW (onboard) | $3,150-$5,100 | 8~10 miles | ~7 hrs | ~3 hrs |
| | | | | 17~20 miles | ~3.5 hrs | ~1.4 hrs |
| Level 3 | 3 phase 208 VAC or 200 ~ 450 VDC | >50 kW (off board) | $30,000-$160,000 | 50~60 miles (80% per 0.5 hour charge) | 30~45 mins | ~10 mins |

| | | | | | | |
|---|---|---|---|---|---|---|
| | (~200 amps) | | | | | |

Depending on the power-level and the required charging facilities, charging of EVs and PHEVs can be classified into 3 different levels (as summarized in Table 1-1).

### 1.2.1 Charging Power Levels

In the United States, level 1 charging is adopted for single phase 120 V/12 A, 60 Hz grid outlet. Level 1 charger is easy to be integrated onboard. The installation cost of level 1 charging infrastructure is estimated to be $500 to $800 [7], [8]. The relative low price makes level 1 applicable to home charging. However, the low charging power increases the charging time of battery pack (up to 17 hours) to charge a typical 25 kWh battery pack from 20% state of charge (SOC) to full SOC.

Level 2 charging requires 240 V power outlet, which is available at the majority of house garages as well as public facilities. In comparison with level 1, without compromising the convenience of accessibility, the level 2 charging time is much less. The cost of installation including the residential electric vehicle supply equipment (EVSE) unit is expected to be $3,150 to $5,100 [9]. Consequently, level 2 charging is expected to be the dominant charging method available in majority of private and public facilities [3].

Level 3 or DC fast charging extends the charging power to a much higher level (excess of 50 kW). Consequently, the charging time is significantly reduced. The level 3 charging stations are expected to charge EV to 50% SOC in 20 minutes.

One of the frontier EV companies, Tesla, targets at 5 minutes fully charging its EVs in the foreseeable future using its supercharging stations [10], [11]. However, level 3 charging comes with its extremely high costs, which includes the installation cost, infrastructure cost, as well as the maintenance cost [12], [13]. Besides, delivering power to a battery pack very rapidly can cause overheat and potential damage to the battery cells. Moreover, drawing ultra-high power from the grid increases the demand from the grid and might incur overload problem of local distribution facilities [14]–[16]. Consequently, level 3 charging is mainly intended for commercial and public charging stations [17]–[19].

### 1.2.2 Battery Swapping

Instead of charging the battery pack overnight at home, the depleted battery pack could be replaced with a fully charged one in a short time, so that the driver is able to get back onto the road fast. This is where the concept of battery swapping comes from. 90 second battery swapping time, which is less time than it takes to fill up a traditional car at the gas station, has been reported by Tesla in 2013 [20]. Battery swapping is deemed as a proposing technique, which makes up the drawbacks of relative slow battery charging speed [21], [22]. However, current battery swapping technique is too specific to be applied to different models of electric vehicles and battery types. Universal battery swapping codes or standards must be composed and implemented before spreading this technique into the commercial market.

### 1.2.3 Battery Charging Profile

Table 1-2 lists the charging characteristics and infrastructures of the popular

EVs and PHEVs available in the market. All listed EVs and PHEVs are equipped with onboard chargers applicable to level 1 and level 2 charging. All EVs and PHEVs except Tesla Model S, utilize universal charge connector, which is defined by SAE J1772 standard.

Table 1-2 Charging characteristics and infrastructures of some manufactured PHEVs and EVs

| Vehicle | EV type | Price | Battery | Onboard Charger | E-Range | Connector Type | Charging Time | |
|---|---|---|---|---|---|---|---|---|
| | | | | | | | Level 1 | Level 2 |
| Nissan leaf | EV | $35,200 | 24 kWh Li-ion | 3.3 kW OBC | 100 mi | SAE J1772 JARI/TEPCO | 22 hrs | 8 hrs |
| BWM ActiveE | EV | Lease only | 32 kWh Li-ion | 7.2 kW OBC | 100 mi | SAE J1772 | 8-10 hrs | 4-5 hrs |
| Ford Focus | EV | $39,200 | 23 kWh Li-ion | 6.6 kW OBC | 76 mi | SAE J1772 | 20 hrs | 3-4 hrs |
| Mitsubishi I | EV | $29,125 | 16 kWh Li-ion | 3.3 kW OBC | 62 mi | SAE J1772 JARI/TEPCO | 13 hrs | 4~5 hrs |
| Honda Fit | EV | Lease only | 20 kWh Li-ion | 3.3 kW OBC | 76 mi | SAE J1772 | 6 hrs | 3 hrs |
| Toyota Prius | PHEV | $32,000 | 4.4 kWh Li-ion | 3.3 kW OBC | 15 mi | SAE J1772 | 3 hrs | 1.5 hrs |
| Chevy Volt | PHEV | $39,145 | 16 kWh Li-ion | 3.3 kW OBC | 35 mi | SAE J1772 | 10 hrs | 4 hrs |
| Cadillac ELR | PHEV | n/a | 16.5 kWh Li-ion | 3.3 kW OBC | 35mi | SAE J1772 | n/a | 4.5 hrs |
| Tesla Model S | EV | $95,400 | 85 kWh Li-ion | 10 kW OBC | 265 | Mobile Connector | 34 | 14 |

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | | | | | mi | | hrs | hrs |

*Specification data is based on public information and is subject to change.

Li-ion cell has much higher energy density than other battery chemistries, such as lead acid cell, nickel cadmium cell, as well as Ni-metal hydride cell [23]. In EVs and PHEVs, energy density and the weight of the battery are two of the most critical parameters that determine the electric range of vehicle. Consequently, Li-ion cell has dominated the market of EVs and PHEVs. This could be observed from Table 1-2, as all the listed EVs and PHEVs are equipped with a Li-ion battery pack. It should be noted that, although extended life cycles, increased energy density, and slight cost reduction have been achieved with the evolutions of battery technology [4], Li-ion battery pack is still the most expensive and heaviest component in EVs and PHEVs.

Various methods can be adopted to safely charge the Li-ion batteries. It is not only the battery chemistry which determines the power level at which a cell can accept a charge, but also the method used to charge the battery. The method shown in Fig. 1.4(a) is called constant current - constant voltage (CC-CV), which is a common charging technique. The basic idea behind this technique is that the battery is charged with a constant maximum current, typically defined by the cell manufacturer, up to the cut-off voltage. Then, it is voltage is kept fixed and it is charged at this constant voltage until the current draw decreases to around one tenth of the peak current or less, which represents a full charge [24]. To increase the charge acceptance rate of the battery, multi-stage constant current - constant voltage (MCC-CV) has been proposed [25]. The principle is nearly the same as CC-CV. However, instead of providing the

battery with one constant current level, several current steps are applied up to the cut-off voltage as shown in Fig. 1.4(b).

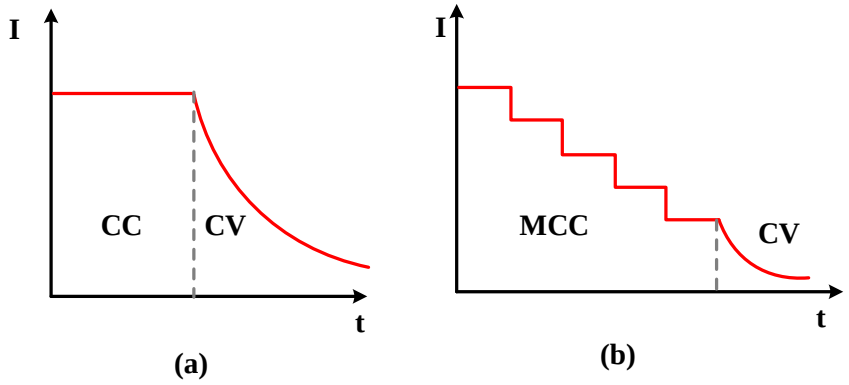



Fig. 1.4. The Li-ion battery charging techniques, (a) constant current-constant voltage, (b) multistage constant current-constant voltage.

The above-described charging methods have limited transfer power capability due to polarization, which include ohm polarization, consistency polarization, and electrochemical polarization. New charging methods, which reduce the influence of polarization, and therefore increase the charge acceptance rate, are still being actively investigated and pursued. One approach which discharges the battery at specific time intervals during charging to increase the charging acceptance is proposed in [22]. This approach can be applied to both CC-CV and MCC-CV techniques in order to yield a better performance. A simplified example of the CC-CV method with negative pulses is represented in Fig. 1.5(a). Another approach proposed in [26] utilizes a variable pulse charge strategy. In this approach, the optimal pulse charge frequency is continuously determined to distribute ions in the electrolyte evenly. Between pulses, a variable rest period is applied to neutralize and diffuse the ions. This rest period is defined by a maximum power point tracker to determine the maximum level of

current acceptance for a given SOC in real time. A typical waveform of the variable frequency associated with pulse charging is shown in Fig. 1.5(b). Using this method charge rate can be increased In comparison with conventional CC-CV and fixed frequency pulse charging methods.

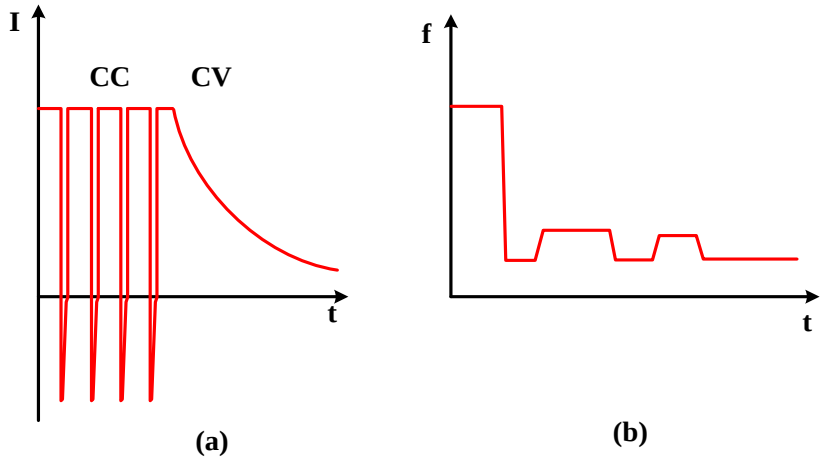



Fig. 1.5. Advanced fast charging techniques, (a) constant current –constant voltage with negative pulse, (b) variable frequency pulse charge [27].

## *1.3. Typical Energy Storage and Power Conversion Interfaces of EVs*

The typical power architecture of an EV is shown in Fig. 1.6. A high voltage (300 V~400 V) and high energy (tens of kWh) battery pack is installed onboard and functions as the energy storage unit. Besides, there are three main power electronic interfaces (PEIs), which are in charge of the power conversions. They are a) PEI for electric propelling, b) PEI for onboard appliances, and c) PEI for onboard charging.

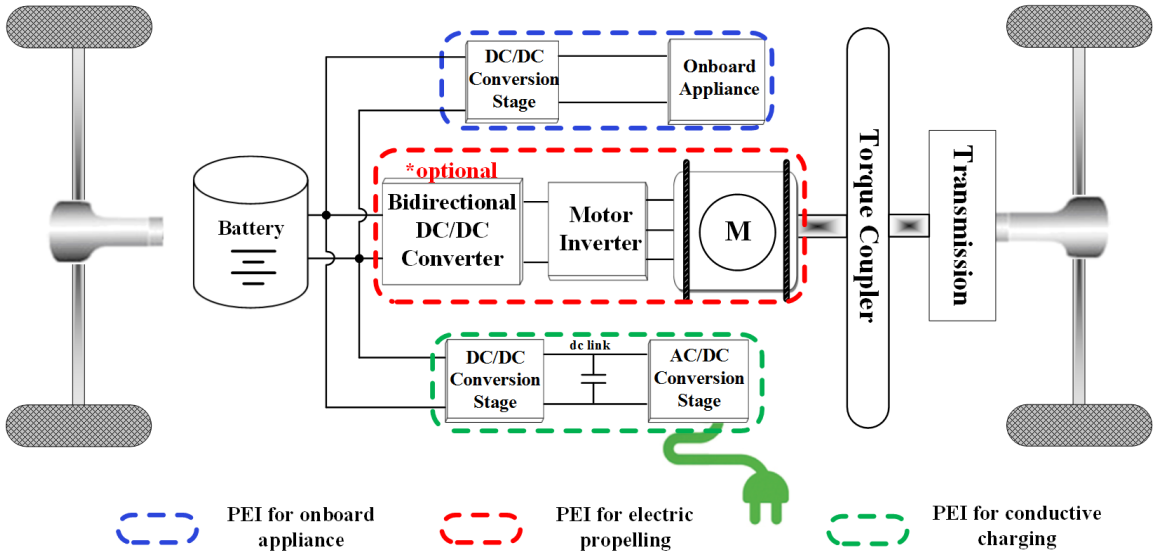



Fig. 1.6. General power architecture of an EV.

The PEI for electric propelling primarily consists of a motor inverter and a bidirectional dc/dc converter. Two operation modes, propelling mode and regenerative braking mode, are associated with this interface. In propelling mode, energy is transferred from the battery pack to the electric machine. In regenerative braking mode, the electric machine functions as a generator. The retrieved power from braking is transferred back to the battery pack. The motor inverter operates as a rectifier. The optional bidirectional dc/dc converter is used to obtain control over charging and discharging of the battery as port of the PEI for electric propulsion [28].

The PEI for onboard appliances is mainly a dc/dc converter. The dc/dc converter steps down the high voltage from battery pack (300 V~400 V) to 12 V to provide power to the onboard electric appliances, such as air conditioning, headlights, stereo systems, and etc. This converter must incorporate galvanic isolation to protect the low voltage electronic system from the potentially hazardous high voltage [29].

Energy flow in this PEI is unidirectional.

The PEI for onboard charger is used to transfer power from the grid to charge the battery pack. Typically, this onboard charger consist of two stages: 1) first stage for ac/dc conversion and power factor correction; 2) second stage for dc/dc conversion and galvanic isolation [3]. Currently, all commercialized onboard chargers have unidirectional power flow from grid to vehicle. However, since most vehicles are parked an average of 95 percent of the time, it is claimed that batteries could be used to let power flow from the vehicle to the power lines and back [30]. In this emerging vehicle-to-grid (V2G) technology, onboard chargers are required to have bidirectional power flows capability. When the vehicle is in idle mode, the battery can feed power back to the grid [31]–[34].

## *1.4. Typical Circuit Configurations of Onboard Charger*

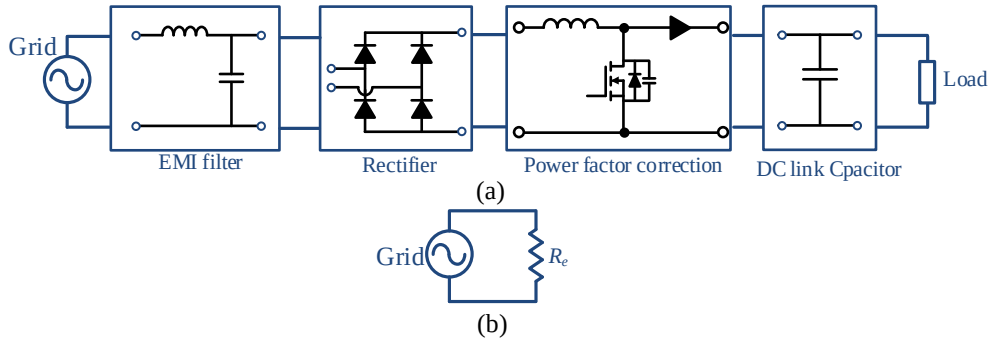



Fig. 1.7. (a) Typical block diagram of ac/dc PFC stage, (b) equivalent circuit model.

The first stage ac/dc PFC converter typically consists of an EMI filter, rectifier, PFC converter, as well as a DC link capacitor [see Fig. 1.7(a)]. The PFC converter is controlled by a high frequency signal to regulate the ac line current to follow the ac line voltage and frequency. Ideally, the ac/dc PFC stage could be

equivalent to a resistive load, as shown in Fig. 1.7(b), to eliminate the total harmonic distortion, and to maximize the power transfer.

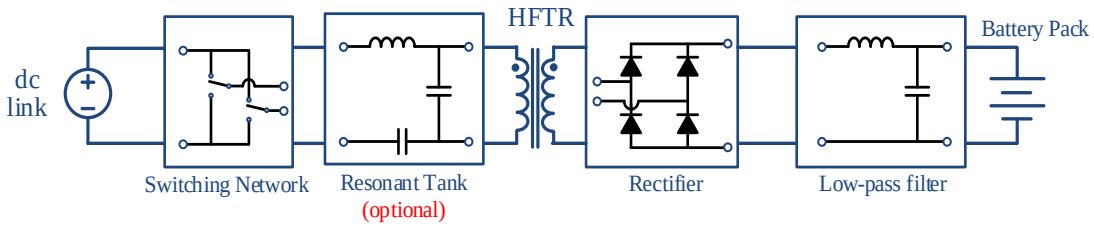



Fig. 1.8. Typical configuration of isolated dc/dc topology.

A typical second stage isolated dc/dc converter consists of a switching network, high frequency transformer, rectifier, and a low pass filter (see Fig. 1.8). For frequency modulated resonant converters, an additional resonant tank between switching network and high frequency is required.

Four different switching networks are shown in Fig. 1.9. With the same dc link voltage and switch ratings, root mean square (RMS) output voltage of full bridge is twice of that of half bridge configuration. Therefore, the full bridge topology with the same switch ratings can be designed and utilized with two times higher output power capability. In order to achieve shorter charging time, higher power level is always desirable for onboard battery chargers. Consequently, only full-bridge configurations are considered in this dissertation.

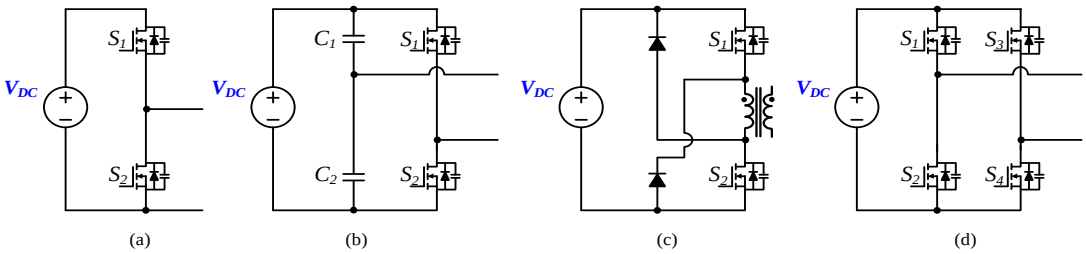



Fig. 1.9. Common switching networks, (a) half bridge, (b) half bridge with split

capacitor, (c) two switch forward, (d) full bridge.

Four different rectifier networks are shown in Fig. 1.10. Half wave rectifier only utilizes half of the input voltage cycle, and does not provide a high power density. Current doubler rectifier and center-tapped rectifier are more suitable for low voltage and high current applications, respectively. The voltage rating of rectifier diodes must be higher than twice of the output voltage. However, onboard battery charging is associated with high battery pack voltage and relatively low charging current, where full bridge rectifier is more suitable. Consequently, only full-bridge rectifier configurations are considered in this dissertation.

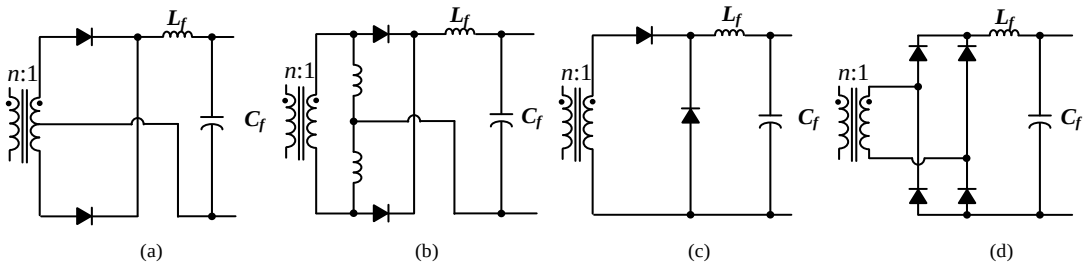



Fig. 1.10. Common rectifier networks, (a) center tapped rectifier, (b) current doubler rectifier, (c) half wave rectifier, (d) full bridge rectifier [35].

## *1.5. Challenges in Onboard Charger Design*

Typically, front-end ac/dc PFC stage is universal to different applications. While the second-stage isolated dc/dc converter is in charge of regulating the charger's output voltage and current to fit the different SOCs of battery. This dissertation focuses on the research of both the front-end ac/dc conversion and the second stage isolated dc/dc conversion.

The U.S. Department of Energy (DOE)'s technical targets on 3.3 kW level 2

onboard chargers is summarized in Table 1-3.

Table 1-3 DOE technical targets on onboard charger[36]

| 3.3 kW Charger | | | | |
|---|---|---|---|---|
| Year | Cost | Size | Weight | Efficiency |
| 2010 | $900-$1,000 | 6-9 liters | 9-12 kg | 90-92% |
| 2015 | $600 | 4 liters | 4 kg | 93% |
| 2022 | $330 | 3.5 liters | 3.5 kg | 94% |

In order to design an ultra-compact, and highly efficient onboard charging interface, following considerations must be taken into account:

1) High switching frequency is desired to reduce the volume and weight;

2) Both step-down and step-up operations should be realized to satisfy the wide output voltage range requirements;

3) Zero-voltage-switching (ZVS) feature is desired to reduce the switching losses as well as high frequency electro-magnetic interference (EMI);

4) A high-frequency transformer must be integrated to achieve galvanic isolation without compromising the size and weight;

5) Conversion efficiency must be optimized across the full battery voltage ranges as well as different load conditions.

However, it is a challenging task to satisfy all above-mentioned considerations simultaneously. As shown in Fig. 1.11, higher switching frequency is associated with smaller volt-second applied to the magnetic component. According to Eq. (1.1), the flux variation is also smaller. So the corresponding core losses are reduced. However,

core loss and the switching loss increases with the increase of frequency. With higher switching frequency, the conversion efficiency will degrade.

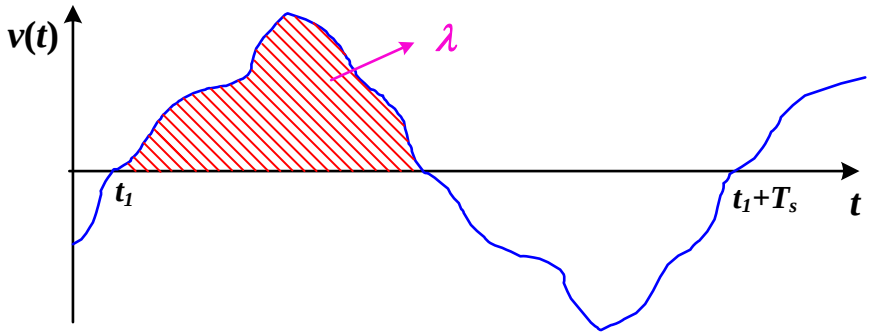



Fig. 1.11. An arbitrary transformer primary voltage waveforms, illustrating the volt-seconds applied during the positive portion of the cycle [37].

$$\Delta B = \frac{\lambda}{2nA_e} \tag{1.1}$$

where $\lambda$ is the voltage second applied to the primary side of transformer; $n$ is the number of primary turns; $A_e$ is the effective cross section area of the magnetic core.

In high switching frequency applications, MOSFET is preferred due to its fast switching speed and no tail current. In hard switching topologies, higher switching frequencies would lead to high stress and high EMI noise. Thus, soft switching techniques, which include zero voltage switching (ZVS) and zero current switching (ZCS), are desired. For MOSFETs, ZVS is more suitable due to the fact that operation with ZVS eliminates both body diode reverse recovery and semiconductor output capacitances from inducing switching loss in MOSFETs [37]. However, ZVS technique could lead to high circulating current and increased conduction losses. Moreover, in some specific topologies, such as phase shift full bridge converter, even

though ZVS operation is achievable in full loads; however, MOSFETs in the lagging leg might lose ZVS features in light load conditions.

Another challenge comes from the wide voltage variation of the high voltage battery pack in the EV. Corresponding to the depleted SOC and full SOC, the voltage of battery pack varies from the cut off voltage to the charge voltage (e.g. 320V to 420V). This means the dc/dc conversion stage must be able to be adapted to this wide voltage range. The pulse-width-modulation (PWM) topologies have the advantages of easy regulation of the output voltage in a wide range. However, they also have the disadvantages of incomplete ZVS range. Frequency modulated resonant topologies have a full ZVS range. However, the efficiency of resonant topologies can be only optimized in some specific output voltage.

To overcome those challenges and to develop an ultra-compact, highly efficient onboard charging system, following components and technologies need to be addressed:

1) Advanced magnetics material: The size of the magnetic component is constrained by the core loss associated with high switching frequency. In order to solve this problem, more advanced magnetics material with smaller core loss in higher switching frequencies must be adopted.

2) Advanced packaging technique: Packaging is directly relevant to the size of the onboard charging system. Packaging techniques help to improve the space utilization and heat dissipation.

3) Advanced cooling technique: Heat sinks take a large portion of the charging system volume. The size of the heat sink is directly determined by the cooling technique. Generally, active cooling is better than passive cooling. The liquid cooling is preferred in the case of conventional Silicon based power electronic interfaces.

4) Advanced switching power devices: Power losses from switching power devices such as MOSFETs and diodes take a large portion of the total system losses. Advanced power devices with low on resistances, high voltage ratings, faster switching speeds, and high operating temperature help reduce the power losses and the thermal stress.

5) Advanced converter topologies and control methods: The converter topology determines the circuit performances such as ZVS feature, EMI, circulating current, conduction losses, and switching losses. An optimized circuit topology and control method would help optimize the overall circuit performance over the wide battery SOC range.

This dissertation will mainly focus on the research of advanced converter topologies as well as control strategies using SiC power devices to optimize the overall power density and efficiency of the onboard charging system over the wide battery SOC range.

## *1.6. Silicon Carbide Power Devices*

As the power density, volume, and weight specifications of power electronic

systems become more stringent, topological configurations and control methods alone is not sufficient to fulfill the performance targets [27]. Wide bandgap power devices are expected to open up new markets for power conversion in high-power, high-temperature, and high-frequency applications where silicon (Si) technology is approaching its theoretical power limits [38]. Majority of industries including automotive and semiconductor device manufacturers are exploring the usage of wide band gap Silicon Carbide (SiC) and Gallium Nitride (GaN) power devices for power electronic based applications [39], [40].

The electric properties of various semiconductors power devices are summarized in Table 1-4. The bandgap of SiC is approximately three times higher than Si. This increases the energy needed for an electron jumping from valence band to conduction band. Thus, the number of electron-hole pairs created due to temperature rise is significantly reduced. This makes SiC devices much more stable in high temperature and more suitable for high-temperature applications. Moreover, the thermal conductivity of SiC devices is much better than Si devices, which facilities heat dissipation and the heat sink size can be significantly reduced.

Table 1-4 Electric properties of semiconductors

| Property | Si | GaAs | 3C-SiC | 6H-SiC | 4H-SiC | 2H-GaN | Diamond |
|---|---|---|---|---|---|---|---|
| Bandgap, $E_g$ (eV) | 1.12 | 1.43 | 2.4 | 3.0 | 3.2 | 3.4 | 5.5 |
| Electric Breakdown Field, $E_c$ (MV/cm) | 0.25 | 0.3 | 2.0 | 2.5 | 2.2 | 3.0 | 5.0 |
| Saturated Electron Drift Velocity, | 1.0 | 1.0 | 2.5 | 2.0 | 2.0 | 2.5 | 2.7 |

| | | | | | | | |
|---|---|---|---|---|---|---|---|
| $v_{sat}$ ($10^7$cm$^2$/s) | | | | | | | |
| Electron Mobility $\mu_n$ (cm$^2$/V·s) | 1350 | 8500 | 1000 | 500 | 950 | 440 | n/a |
| Hole Mobility, $\mu_p$ (cm$^2$/V·s) | 480 | 400 | 40 | 80 | 120 | 30 | 1600 |
| Relative dielectric constant, $\varepsilon_r$ | 11.9 | 13.0 | 9.7 | 10.0 | 10.0 | 9.5 | 5.0 |
| Thermal Conductivity (W/cm·K) | 1.5 | 0.5 | 5.0 | 5.0 | 5.0 | 1.3 | 20.0 |
| Direct/Indirect Bandgap | I | D | I | I | I | D | I |

Another advantage of SiC devices is their higher electric breakdown field. As shown in Table 1-4, 4H-SiC has an order of magnitude higher breakdown field and higher temperature capability than conventional Si. This means for the same blocking layer dopant density, SiC device has over an order of magnitude higher voltage blocking capability. High voltage blocking capability brings the benefit of reduced leakage current and associated leakage losses. On the other hand, for a desired breakdown voltage, SiC device has an order of magnitude lower blocking layer thickness [41]. Schottky didoes and MOSFETs are majority carries power devices. The on resistance of majority carrier power devices is inversely proportional to the blocking layer thickness, and proportional to the doping concentration. The reduced blocking layer thickness with increased doping concentration yield a SiC majority carrier devices much smaller on resistance compared to that of Si majority carrier devices[42]. Low on resistance brings the benefit of reduced conduction losses.

As shown in Table 1-4, GaN has higher bandgap and breakdown field than SiC. This brings GaN power devices the benefits of good high temperature

performance, high breakdown voltage, and low on resistance. However, GaN power devices are not commercially available at over 200V, 12A power ratings, which makes them not commercially ready to be used in designing onboard chargers for the automotive industry. This dissertation will mainly focuses on design and optimization of onboard charger based on Si and SiC power devices.

The parameters of three 600 V and 8 A power diodes are presented in Table 1-5. In comparison with Si Schottky diode, the forward voltage drop of SiC Schottky diode is improved by 31%. The leakage current of SiC Schottky diode (50 μA) is comparable with that of PiN Si diode (30 μA), while significantly improved in comparison with Si Schottky diode (250 μA). This improvement brings the benefit of reduced leakage losses. The most attracting feature of SiC Schottky diode is its zero reverse recovery. This eliminates the turning-off losses of the SiC Shottky diodes. The SiC diodes are the optimal options for ultra-high switching frequency applications. Specifically, applying SiC Schottky diodes in boost PFC stage results in zero reverse recovery losses and significantly reduced EMI.

Table 1-5 Comparison of diodes parameters

| Part Number | ETX0806 | QH08TZ600 | C3D08060A |
|---|---|---|---|
| Material | Si | Si | SiC |
| Technology | PiN | Schottky | Schottky |
| Breakdown voltage (V) | 600 | 600 | 600 |
| Average forward current $I_F$ (A) | 8 | 8 | 8 |
| Forward voltage at $I_F$, $V_F$ (V) | 3.4 | 2.6 | 1.8 |
| Maximum Reverse current, $I_R$ (μA) | 30 | 250 | 50 |
| Junction Capacitance, $C_T$ (pF) | 6 | 25 | 39 |
| Reverse Recovery time, $t_{rr}$ (ns) | 14 | 11.1 | 0 |
| Price, (USD) | 1.12 | 2.86 | 3.86 |

*Price data is based on digikey as of July 2013 and is subject to change.

The parameters of three 24 A power MOSFETs are summarized in Table 1-4. Super junction technology allows the thick drift region of a power MOSFET to be heavily doped. Therefore, the on resistance could be reduced without compromising the breakdown voltage [43]. As shown in the table, SiC power MOSFET has comparable on resistance with the Si super junction MOSFET. However, the voltage rating of SiC power MOSFET is twice of its Si counterpart.

In comparison with regular 1.2 kV Si power MOSFET, the on resistance, input capacitance, and output capacitance of SiC MOSFET are reduced by 68%, 88.9%, and 89.7%, respectively. Reduced on resistance, input capacitance and output capacitance bring the benefits of reduced conduction losses, gate driving losses and switching losses, respectively. The reverse recovery time and charge of body diode of SiC MOSFETs are reduced by 89.1%. Moreover, the fall time is reduced by 50%. This means faster switching speed can be achieved with SiC power MOSFET with the same voltage rating. The disadvantage of SiC power MOSFETs mainly comes from its high diode forward voltage drop. As shown in the table, the body diode of SiC MOSFET has three times higher forward voltage than Si MOSFET. This increases the conduction losses from the body diodes. Generally, the body diodes should be avoided to reduce the associated conduction losses.

Table 1-6 Comparison of MOSFETs parameters

| Part Number | IPB60R160C6 | APT24M120L | CMF10120D |
|---|---|---|---|
| Material | Si | Si | SiC |
| Technology | CoolMOS super junction | POWER MOS 8™ | Z-FET |
| Drain-source voltage, $V_{DS}$(V) | 650 | 1200 | 1200 |
| Drain current at 25°C $I_D$ (A) | 24 | 24 | 24 |
| Static drain-source on resistance | 0.16 | 0.50 | 0.16 |

| $R_{ON}$ (Ω) | | | |
|---|---|---|---|
| Input capacitance, $C_{iss}$ (pF) | 1660 | 8370 | 928 |
| Output capacitance, $C_{oss}$ (pF) | 314 | 615 | 63 |
| Fall time, $t_f$ (ns) | 8 | 42 | 21 |
| Rise time, $t_{rise}$(ns) | 13 | 27 | 34 |
| Body diode forward voltage, $V_F$ (V) | 0.9@11.3A | 1V@12A | 3.5V@5A |
| Body diode reverse recovery time, $t_{rr}$ (ns) | 460 | 1270 | 138 |
| Body diode reverse recovery charge, *Qrr* (nC) | 8200 | 30000 | 97 |
| Price, (USD) | 4.61 | 20.2 | 16.67 |

*Price data is based on digikey as of July 2013 and is subject to change.

### *1.7. Intellectual Merit and List of Contributions*

This dissertation focuses on how to achieve both the efficiency optimization over the wide voltage range and the capability to charge the deeply depleted battery packs simultaneously. We mainly concentrated on the perspectives of power electronics topologies, and control methodologies using SiC power semiconductors. The proposed efficiency enhancement technique can be extended to higher power level and will have a profound impact on the deployment of next generation PEVs.

The contributions of this work are listed as below.

1) We conducted a comprehensive literature review on the PEV onboard charging.

2) We proposed a new methodology to effectively evaluate the charging performances of resonant topologies.

3) We proposed and developed a Si based level 1 onboard charger based on

interleaved Boost PFC and full bridge LLC topologies.

4) We proposed a novel maximum efficiency point tracking technique for LLC based chargers. Using this proposed technique, we make the dc link voltage follow the battery voltage, so that the LLC converter is always operating in the vicinity of its resonant frequency, where the circuit losses are minimized. An efficiency improvement of 2.1% at the heaviest load condition and 9.1% at the lightest load condition for LLC conversion stage are demonstrated experimentally. This is the main engineering contribution of this work.

5) We proposed and developed a novel SiC based level 2 charger based on SEPIC PFC stage and maximum efficiency point tracking technique for LLC converter. For the first time, we achieved both the efficiency optimization over the wide voltage range and the capability to charge the deeply depleted battery pack simultaneously. The developed loss evaluation methodology, control technique, and design philosophy are modeled and validated mathematically. This is the main theoretical contribution of this work.

## *1.8. Outline of Dissertation*

This dissertation consists of eight chapters.

Chapter 1 is the introduction.

In chapter 2, states of the art of isolated charger topologies are reviewed and compared. Three different boost type converters (conventional boost, bridgeless

boost, and interleaved boost) are discussed and compared comprehensively for the front-end ac/dc PFC applications. For the second stage dc/dc conversion, different isolated dc/dc topologies are investigated for PEV battery charging applications. A comprehensive comparison is made between conventional full bridge isolated PWM buck converter, full bridge phase-shift PWM converter, full bridge series resonant pulse-frequency-modulation (PFM) converter, and full bridge LLC series parallel PFM converter.

In chapter 3, a methodology is proposed to effectively evaluate the circuit performance of resonant topologies in battery charging applications. This methodology includes evaluating the battery voltage, charging current, as well as the input root mean square (RMS) current characteristics to design the resonant chargers and to compare the chargers' performance. Using the proposed method, four full-bridge isolated resonant chargers, which are rated at 3.2 kW and used to charge a 360 V Li-ion battery pack, are designed and evaluated. Based on the analytical results, it is shown that the LLC charger takes the advantages of LCC and PRC chargers, while avoiding the drawbacks of SRC chargers. LLC can maintain better efficiency, voltage regulation, as well as short circuit protection performance over the full range of battery SOC. Thus, LLC could be chosen as a suitable candidate for PEV battery charging applications.

In chapter 4, a level 2 onboard PEV battery charger is proposed. Interleaved boost topology is used in the first stage for PFC and THD reduction while reducing volume of the magnetic components. In the second stage, a full bridge LLC resonant

converter is employed to achieve high conversion efficiency over the full voltage range of the battery pack. The suitability and advantages of the proposed converter are discussed and design guidelines are provided through theoretical analyses for both interleaved boost and full bridge LLC topologies. As a case study, design considerations for a 1 kW level 2 charger, which converts 110 V, 60 Hz ac to battery voltage range of 320 V to 420 V are provided.

The experimental results are presented for validation of simulations and analytical studies. The first stage interleaved boost converter demonstrates unity power factor operation at the rated power and achieves THD less than 4%. In the second stage LLC converter, the switching losses and conduction losses are optimized through operating the converter close to resonance frequency of the resonant tank.

In chapter 5, a novel maximum efficiency point tracking technique is proposed for LLC based plug-in electric vehicle battery chargers. With this proposed technique, dc link voltage always follows the change of battery pack voltage; which ensures that an LLC converter is always operating at the primary resonant frequency. Detail modeling and losses analysis are provided for an LLC converter operating at the resonant frequency. According to the theoretical analysis, a guideline is detailed to design LLC converters operating at maximum efficiency point. The designed LLC converter is simulated, and the simulation results show that an LLC converter is able to provide 2.5% efficiency improvement at the heaviest load condition and 8.9% efficiency improvement in the lightest load condition.

In chapter 6, an onboard PEV battery charger based on a SEPIC PFC stage

and an LLC topology is proposed. Proposed topology combination is able to charge the deeply depleted battery packs, whose voltage might goes down to 100 V. The maximum efficiency point tracking technique for the LLC topology is utilized to optimize the conversion efficiency of the charger. Since SEPIC topology owns the features of both boosting the input voltage and chopping the input voltage, it is utilized in the front-end power factor correction stage. A 3.3 kW charger prototype, which includes both the ac/dc and the isolated dc/dc stages, is designed to validate the proof of concept. Simulation results and experimental results demonstrate that the designed charger is able to maintain a wide dc link voltage range (100V-420V) while keeping the LLC converter operating at its maximum efficiency point.

Chapter 7 concludes this dissertation. Contributions of this work are summarized in this chapter. The future work is also discussed. The future efforts would focus on three aspects. 1) Implement the interleaved SEPIC PFC converter using coupled inductors, so that the power level of the PFC stage can be increased. 2) Boost the switching frequency from around one hundred kilo Hz to higher than Mega Hz. So that the size of the passive components is able to be further reduced. 3) Modify the circuit topology so that the power flow can be bidirectional.

# Chapter 2 State of The Art Isolated Battery Chargers

## *2.1 Introduction*

In plug-in electric vehicles (PEVs), an ultra-compact, highly efficient onboard charger is desired. In order to achieve those targets, the converter topologies must be optimized for high voltage PEV battery charging applications.

In PEV battery charging applications, the battery voltage and load condition vary in a wide range depending on the different state of charge (SOC) of the battery, as well as different battery types [44], [45]. Therefore, operating with maximum efficiency through reducing the conduction and switching losses over the full output voltage and load ranges is a challenging issue in PEV charger design.

In comparison with conventional pulse width modulation (PWM) converters, frequency modulated resonant converters exhibit advantages such as (a) reduced switching losses and thus higher conversion efficiency, (b) capability to operate at higher switching frequency, which helps to reduce the size of magnetic components and thus to improve the power density, and (c) zero voltage switching feature, which can eliminate some sources of electromagnetic interference [37], [46]. Consequently, resonant dc/dc converters are deemed as a good candidate for front-end dc/dc conversion applications, which requires a constant output voltage [35], [47], [48].

In this chapter, state of the art ac/dc PFC and isolated dc/dc topologies are reviewed for PEV battery charging applications. This chapter is organized as follows; Section 2.2 compares the performance of conventional boost, bridgeless boost, as

well as interleaved boost topologies in the power level of level 2 charging. In section 2.3, four different isolated full bridge dc/dc topologies are analyzed, discussed, and compared for PEV battery charging applications. Finally, Section 2.4 summarizes the study and features the benefits based on the achieved results.

## *2.2 Review of Front End ac/dc PFC Topologies*

Front end ac/dc converter is a critical component of PEV charger. Proper selection of the topology is essential to meet the regulatory requirements for input current harmonics, output voltage regulation and implementation of power factor correction [49]–[52].

Boost topology and its derivatives are widely used for ac/dc PFC purposes [53]. In comparison with operation in continuous conduction mode (CCM), boost converter operating in discontinuous mode (DCM) would have smaller switching losses. However, for high power level, operation in DCM means large current stress to circuit components. Therefore, only CCM is considered for high power PEV battery charging applications. Conventional boost topology, bridgeless boost topology, as well as interleaved boost topology are reviewed for application in ac/dc PFC stage for PEV battery charging applications.

### 2.2.1 Conventional Boost PFC Converter

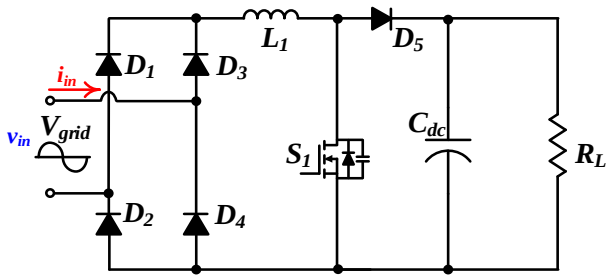



Fig. 2.1. Single phase boost PFC converter.

Fig. 2.1 shows the schematic of a single phase boost PFC converter. A diode bridge is utilized to rectify the ac voltage from the grid to dc; a boost converter is followed to correct the power factor. In comparison with interleaved topology, the ripple current of the filter capacitor is pretty high [54]. The main limitation of conventional boost PFC converter is the high conduction losses due to the current flow through the semiconductor devices [27]. The high frequency operation makes the reverse recovery losses from the boost diode a big concern. Utilizing SiC Schottky diodes could alleviate the reverse recovery problems to some extent. However, this also increase the total cost. Moreover, in high power level, the high peak current of the inductor in DCM is associated with bulky magnetic component.

### 2.2.2 Bridgeless Boost PFC Converter

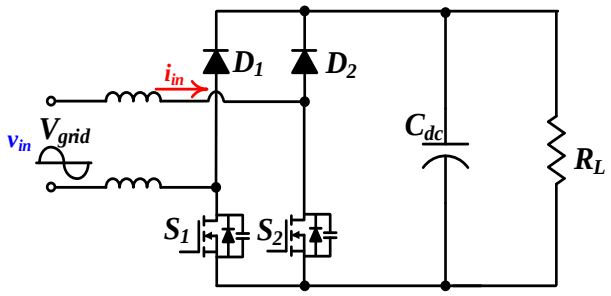


Fig. 2.2. Bridgeless PFC boost converter.

Fig. 2.2 shows the schematic of bridgeless PFC boost converter. In comparison with conventional boost PFC converter, bridgeless topology gets rid of the diode bridge while keep the boost feature. Consequently, the loss associated with diode rectifier bridge is reduced, which makes it suitable to be applied to higher power level. However, bridgeless configuration brings problems of high EMI [55], [56]. Besides, the floating input line makes it impossible to sense the input voltage without a low frequency transformer or an optical coupler. In order to sense the input current, complex circuit is necessary to sense the current in the MOSFET and diode separately [52], [57]. Moreover, in high power level, the high peak current of the inductor is also associated with bulky magnetic components.

### 2.2.3 Interleaved Boost PFC Converter

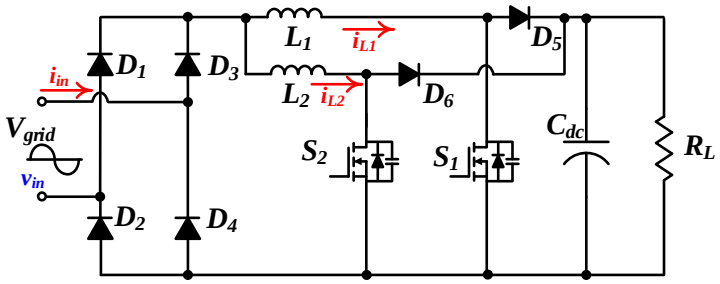



Fig. 2.3. Interleaved PFC boost converter.

Fig. 2.3 shows the schematic of interleaved PFC boost converter. In two phase interleaved topology, two boost converters are in parallel and operated with 180 degree phase difference. The input current equals to the summation of both inductor current. Since the inductor ripple currents are output of phase, they can cancel with

each other. Thus, the high frequency input current ripple could be significantly reduced, so that the size of input EMI filter could be reduced[58], [59]. Moreover, the power of the converter is evenly shared between those two boost legs, thus the current stress on the circuit components are reduced by half.

Performance comparison of three different PFC topologies are summarized in Table 2-1. As shown in Table 2-1, interleaved boost PFC topology has the best overall performance in high power applications.

Table 2-1 Comparison of ac/dc PFC topologies for PEV battery charging [52]

| Topology | Conventional boost | Bridgeless boost | Interleaved Boost |
|---|---|---|---|
| Power level | Low | Medium | High |
| EMI/Noise | Fair | Poor | Best |
| Capacitor ripple | High | High | Low |
| Input current ripple | High | High | Low |
| Magnetic Size | Large | Medium | Small |
| Efficiency | Poor | Good | Good |
| Cost | Low | Medium | Medium |

## *2.3 Review of Second Stage Isolated dc/dc Topologies*

### 2.3.1 Full Bridge Isolated PWM Buck Converter

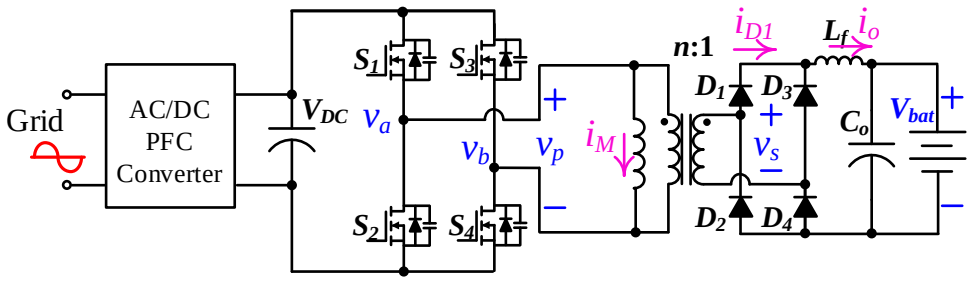



Fig. 2.4. Full bridge isolated PWM buck converter.

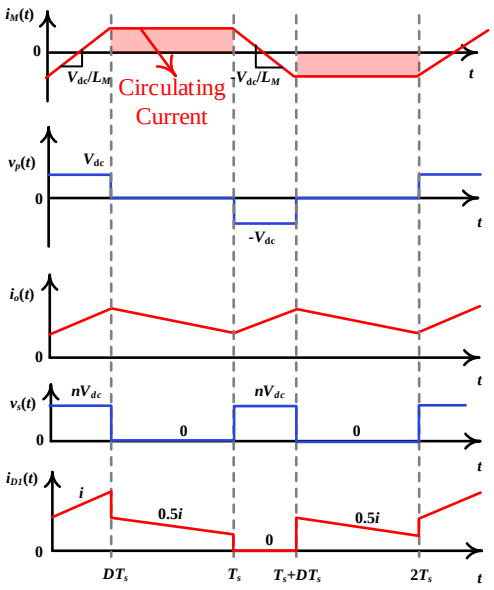



Fig. 2.5. Waveforms of full bridge isolated buck converter.

The schematic and the simulated waveforms of full bridge isolated buck converter in PEV battery charging application is shown in figures 2.4 and 2.5, respectively. In continuous conduction mode (CCM), the relationship between input and output voltages is specified in Eq. (2.1).

$$V_{bat} = nDV_{dc} \tag{2.1}$$

According to Eq. (2.1), it is easy to regulate the output voltage by controlling the duty cycle, *D*. The boost behavior required by battery charger could be achieved by appropriately designing the turns ratio of the transformer, *n*. In light load condition, which corresponds to the high SOC, the converter could switch to discontinuous conduction mode (DCM). In DCM mode, the MOSFETs are turned on at ZVS.

It should be noted that in CCM mode the MOSFETs of full bridge isolated buck converter are turned on and off with hard switching. This causes significantly

high switching losses and EMI problems, which greatly constrain the switching frequency. Moreover, in time interval ($DT_s$, $T_s$], current in magnetic inductor circulates in the primary side of the magnetic core. This causes high conduction losses.

### 2.3.2 Full Bridge Phase-shift PWM Converter

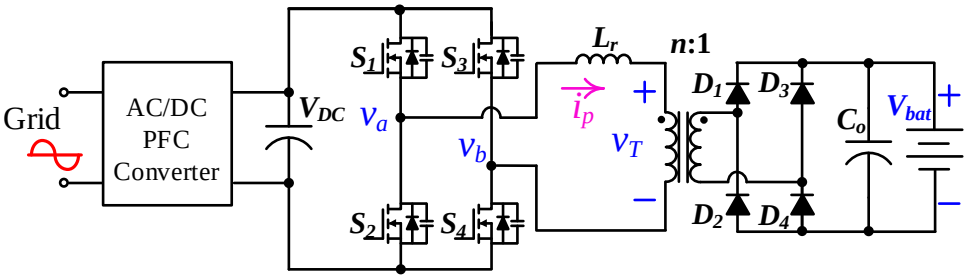



Fig. 2.6. Full bridge phase-shift PWM converter.

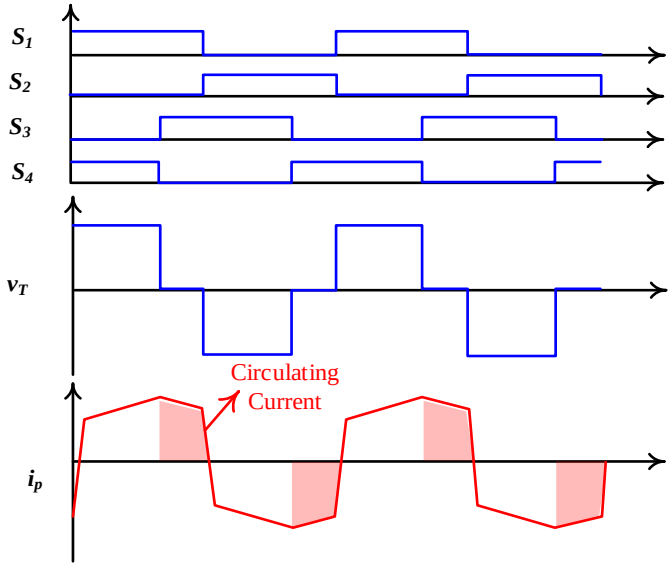



Fig. 2.7. Waveforms of full bridge phase-shift converter.

Full bridge phase-shift converter is one of the most popular topologies in the power range of a few kilowatts for isolated dc/dc conversion applications [60]–[64].

The schematic and simulated waveforms of full bridge phase-shift converter is shown in Fig. 2.6 and Fig. 2.7, respectively. In full bridge phase-shift converter, the primary side MOSFETs are turned on with ZVS; and the body diodes are turned off with ZCS. Output voltage is regulated by the duty cycle and is easy to control. Besides, control of full bridge phase-shift topology is easy to implement in comparison with its PFM resonant counterpart [65]. The relationship between input and output voltages is defined in Eq. (2.2).

$$V_{bat} = \frac{\sqrt{\alpha^2 + \frac{16\alpha}{D^2}} - \alpha}{8n} V_{dc} \tag{2.2}$$

where

$$\alpha = \frac{R_L T}{L_r} \tag{2.3}$$

where, $R_L$ is the equivalent load resistance, which is equal to battery voltage over charging current.

However, in PEV battery charging applications, the output power range is wide. In light load condition, limited energy is stored in $L_r$. This makes the MOSFETs in the lagging leg lose ZVS features [65]. Moreover, in the time intervals when either both upper switches are on or both lower switches are on, the circulating power is high and would cause higher conduction losses. Besides, the turning off of secondary diodes would cause high voltage overshoots and oscillations due to the high voltage of the battery pack.

### 2.3.3 Full Bridge Series Resonant Converter

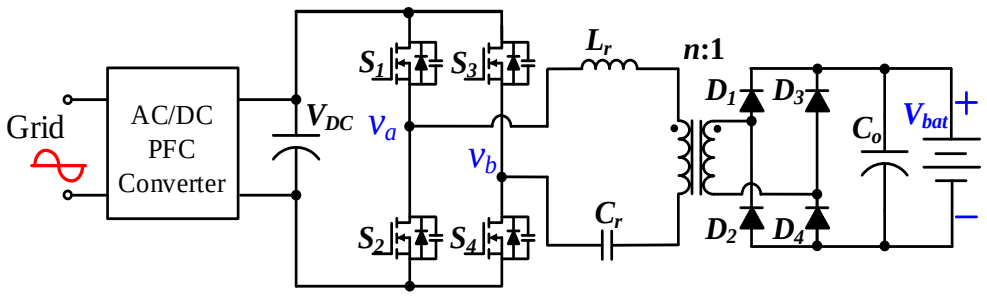



Fig. 2.8. Full bridge SRC PFM converter.

Full bridge series resonant converter (FB-SRC) is another candidate for isolated dc/dc conversion [44]. Schematic of full bridge series resonant converter is shown in Fig. 2.8. With the switching frequency higher than the resonant frequency of $L_r$ and $C_r$, the primary side power MOSFETs are turned on with ZVS, and freewheeling diodes are turned off with ZCS. This ZVS feature is irreverent to different load conditions. One of the most attractive features of FB-SRC is that its circulating losses are very low. Moreover, FB-SRC has good short circuit protection performances; short circuit current could be easily regulated by boost the switching frequency [66]. The relationship between output voltage and input voltage is demonstrated as,

$$V_{bat} = \left| \frac{R_L}{R_{ac} + j\omega L_r + 1/(j\omega C_r)} \right| \frac{8nV_{dc}}{\pi^2} \tag{2.4}$$

However, the critical defect of FB-SRC lies in its unacceptable poor voltage regulation performance in light load condition. Slight perturbation from input voltage causes large scale of frequency shift. This makes it hard to regulate the voltage and increases the switching losses and conduction losses. Moreover, secondary side

diodes are turned off with very high *di/dt*, which corresponds to big reverse recovery losses.

### 2.3.4 Full Bridge LLC Resonant Converter

Full bridge LLC resonant converter has been proved to be one of the most suitable candidates for dc/dc conversion in applications, which require constant output voltage [67]–[70]. When the input impedance is inductive, turning on of primary MOSFETs and turning off of freewheeling didoes are ZVS and ZCS, respectively. When the switching frequency is smaller than $f_p$, which is the resonant frequency of $L_r$ and $C_r$, secondary side diodes are turned off with ZVS.

$$V_{bat} = \left| \frac{j\omega L_r \,\|\, \frac{8n^2 R_L}{\pi^2}}{R_{ac} + j\omega L_r + 1/\left(j\omega C_r\right)} \right| \frac{V_{dc}}{n} \tag{2.5}$$

When switching frequency is smaller than $f_p$, and the input impedance is still inductive, circulating losses of FB-LLC are higher than FB-SRC, but much smaller than FB-FS. The short circuit performance of LLC is not as good as FB-SRC but still acceptable.

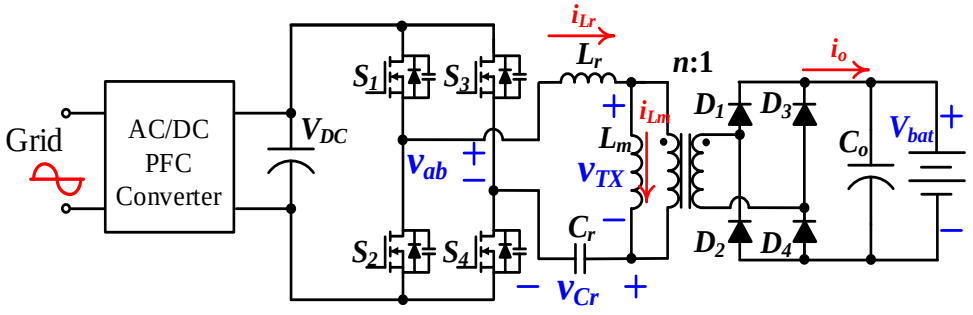



Fig. 2.9. Full bridge LLC PFM converter.

The performances of FB-Buck, FB-FS, FB-SRC, and FB-LLC topologies are summarized in Table 2-2.

Table 2-2 Comparison of isolated converters in PEV charging applications

| Performance | Full Bridge Isolated Buck | Full Bridge Phase Shift | Full Bridge Series Resonant | Full Bridge LLC Resonant |
|---|---|---|---|---|
| Modulation method | PWM | PWM | PFM | PFM |
| Additional filter inductor on secondary side | Yes | No | No | No |
| Short circuit protection performance | Bad | Bad | Good | Good |
| Primary MOSFETs switching losses in normal load | High, hard switching | Low, ZVS | Low, ZVS | Low, ZVS |
| Secondary diodes switching losses in normal load | High, hard switching | Low, ZCS | High, hard switching | Low, ZCS |
| Harmonics distortion in normal load | High | Low | Low | Low |
| Light load circulating losses | Low | High | Low | Moderate |
| Light load switching losses | Low | High, ZVS feature lost | Low | Low |
| Voltage regulation capability at light load | Good | Good | Poor | Good |

## *2.4 Summary*

In this chapter, three different boost type converters (conventional boost, bridgeless boost, and interleaved boost) are discussed and compared comprehensively for the front end ac/dc PFC applications. For the second stage dc/dc conversion, different isolated dc/dc topologies are investigated for PEV battery charging applications. A comprehensive comparison is made between conventional full bridge isolated PWM buck converter, full bridge phase-shift PWM converter, full bridge series resonant PFM converter, and full bridge LLC series parallel PFM converter.

# Chapter 3 Comprehensive Topological Analyses of Isolated Resonant Converters in PEV Battery Charging Applications

## *3.1 Introduction*

In onboard plug-in electric vehicle (PEV) battery chargers, an ultra-compact, highly efficient isolated dc/dc converter is desired for battery current regulation and galvanic isolation.

In comparison with conventional pulse width modulation (PWM) converters, frequency modulated resonant converters exhibit advantages such as (a) reduced switching losses and thus higher conversion efficiency, (b) capability to operate at higher switching frequency, which helps to reduce the size of magnetic components and thus to improve the power density, and (c) zero-voltage switching feature, which can eliminate some sources of electromagnetic interference [37], [46]. Consequently, resonant dc/dc converters are deemed as a good candidate for front-end dc/dc conversion applications, which requires a constant output voltage [35], [47], [48].

Based on the differences in the resonant tank and its relationship with the load, resonant dc/dc topologies are classified into four categories, (a) series resonant converter (SRC), (b) parallel resonant converter (PRC), (c) LCC series-parallel resonant converter (LCC), and (d) LLC series-parallel resonant converter (LLC). Fig. 3.1 illustrates these four types of isolated half-bridge resonant topologies, which may be used for onboard PEV charging applications.

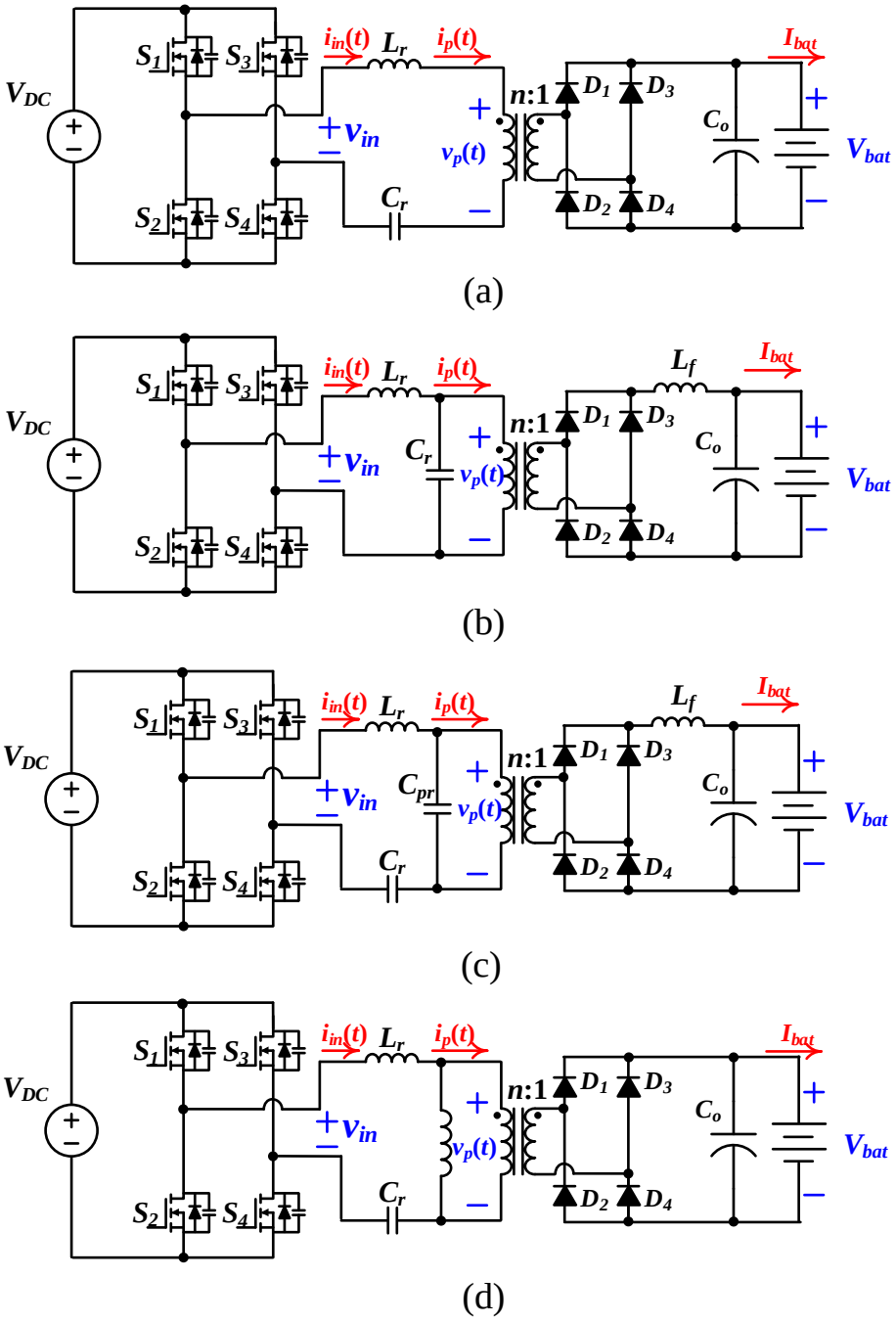



Fig. 3.1. Isolated resonant topologies in battery charging applications. (a) Series resonant converter (SRC). (b) Parallel resonant converter (PRC). (c) LCC series-parallel resonant converter (LCC). (d) LLC series-parallel resonant converter (LLC).

In this chapter, these four isolated half-bridge resonant converters (SRC, PRC,

LCC, and LLC) are investigated and evaluated for PEV battery charging applications. It is shown that that LLC could maintain good efficiency performance over a wide range of battery SOCs.

This chapter is organized as follows: Section 3.2 details the analysis methodology of resonant converters. Section 3.3 explains the charging profiles of a Li-ion battery pack. Section 3.4 illustrates the basic design and comparison considerations of resonant converters. In Section 3.5, the resonant converters in PEV battery charging applications are compared. Finally, Section 3.6 summarizes the study and features the benefits based on the achieved results.

## *3.2 Circuit Modeling and Analyses of Resonant Converters*

As demonstrated in Fig. 3.1, each topology consists of four parts: (a) a dc voltage source and switch network, which operate as a square wave generator, (b) a resonant tank, (c) a transformer and full bridge rectifier, and (d) a low-pass filter network and dc load, which is a battery pack.

### 3.2.1 Circuit Modeling

According to Fourier Series, the square wave, $v_{in}(t)$, contains dc component, first harmonic, and higher odd harmonics as shown in Eq. (3.1),

$$v_{in}(t) = 0 + \frac{4V_{DC}}{\pi}\sin(2\pi f_s t) + \sum_{n=3,5,7,\ldots} \frac{4V_{DC}}{n\pi}\sin(2\pi n f_s t) \tag{3.1}$$

where, $f_s$ is the switching frequency and also the frequency of first harmonic component. $v_{in}(t)$ is fed to the input terminals of the resonant tank. The primary

resonant frequency of the resonant tank, $f_p$, is the resonant frequency between $L_r$ and $C_r$,

$$f_p = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{3.2}$$

In order to optimize the conversion efficiency, $f_p$ is tuned to be close to desired switching frequency. Thus, the resonant tank works like a filter, which filters the higher odd harmonics of $v_{in}(t)$. To simplify the analysis, only the response of first harmonic is considered in the circuit analysis. This approach is named first harmonic approximation.

Using first harmonic approximation, the network consists of transformer, full bridge rectifier, low-pass filter, and dc load (battery) could be modeled as an ac resistor. By calculating the root mean square values of its input voltage and current, the equivalent ac resistance, $R_{ac}$, could be found as,

$$R_{ac} = \frac{8n^2}{\pi^2} \times R_L = \frac{8n^2}{\pi^2} \frac{V_{bat}}{I_{bat}} \tag{3.3}$$

where, $n$ is the turns ratio of the center-tapped transformer, $V_{bat}$ and $I_{bat}$ are the battery voltage and charging current, respectively. Detailed derivations will be provided in chapter 4.

By using the first harmonic approximation, and the equivalent load resistance $R_{ac}$, the circuit models of resonant converters are plotted in Fig. 3.2, where $v_{in,1}(t)$, $i_{in,1}(t)$, $v_{p,1}(t)$, and $i_{p,1}(t)$ denote the first harmonic components of input voltage $v_{in}(t)$, input current $i_{in}(t)$, voltage of the primary side of transformer $v_p(t)$ and the current of primary side of transformer $i_p(t)$, respectively.

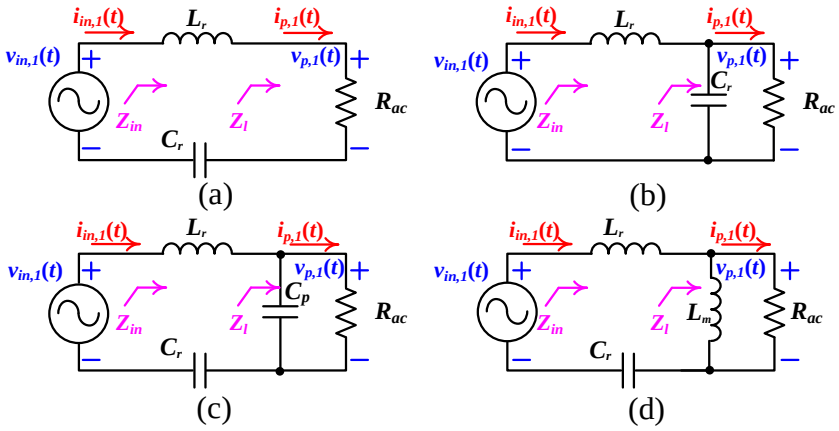



Fig. 3.2. Ac equivalent models of resonant converters. (a) SRC. (b) PRC. (c) LCC. (d) LLC.

### 3.2.2 Dc Voltage and Current Characteristics

According to the ac equivalent models shown in Fig. 3.2, the normalized voltage gain, transconductance, and the conductance of the circuit could be derived as,

$$G_n = \frac{v_{p,1,rms}}{v_{in,1,rms}} = \left| \frac{Z_l}{Z_{in}} \right| \tag{3.4}$$

$$g_n = \frac{i_{p,1,rms}}{v_{in,1,rms}} = \left| \frac{Z_l}{Z_{in}} \right| \frac{1}{R_{ac}} \tag{3.5}$$

$$C_n = \frac{i_{in,1,rms}}{v_{in,1,rms}} = \left| \frac{1}{Z_{in}} \right| \tag{3.6}$$

where, $Z_l$ and $Z_{in}$ are the input and load impedance of the ac equivalent model.

Accepting the accuracy of first harmonic approximation, the battery voltage, charging current and rms value of input current could be written as,

$$V_{bat} \approx \frac{v_{p,1,rms}}{v_{in,1,rms}} \frac{V_{DC}}{n} = \left| \frac{Z_l}{Z_{in}} \right| \frac{V_{DC}}{n} \tag{3.7}$$

$$I_{bat} = \frac{V_{bat}}{R_L} \approx \left|\frac{Z_l}{Z_{in}}\right| \frac{8n}{R_{ac}\pi^2} \tag{3.8}$$

$$i_{in,rms} \approx i_{in,1,rms} = \left|\frac{v_{in,1,rms}}{Z_{in}}\right| = \frac{2\sqrt{2}V_{DC}}{\pi}\left|\frac{1}{Z_{in}}\right| \tag{3.9}$$

The dc voltage and current characteristics are critical figure of merits in analyzing the circuit performance in battery charging applications.

### 3.2.3 Capacitive and Inductive Operations

The input impedance of the resonant circuit, $Z_{in}$, could be capacitive or inductive. Due to the filtering effect of the resonant tank, the input current, $i_{in}(t)$, is approximated as a sinusoidal function. The waveforms of input voltage $v_{in}(t)$, and its first harmonic component $v_{in1}(t)$, as well as $i_{in}(t)$ are plotted in Fig. 3.3.

Fig. 3.3(a) shows the circuit operation in capacitive region. $Z_{in}$ is capacitive, $i_{in}(t)$ leads $v_{in}(t)$ with certain phase difference $\phi_1$. As seen in the figure, the turn-off process of switches ($S_1$-$S_4$) is soft switching. However, the turn-on process of switches, and the turn-off process of freewheeling diodes ($D_{S1}$-$D_{S4}$) are both hard switching. The reverse recovery process of freewheeling diodes leads to significant switching losses. Consequently, the freewheeling diodes must have good reverse-recovery characteristics to avoid large reverse spikes flowing through the switches, and to minimize the diode turn-off losses. In capacitive operation, MOSFETs in high switching frequency applications are not suitable as the primary switches. It is possible to use thyrisors in low switching frequency applications [71].

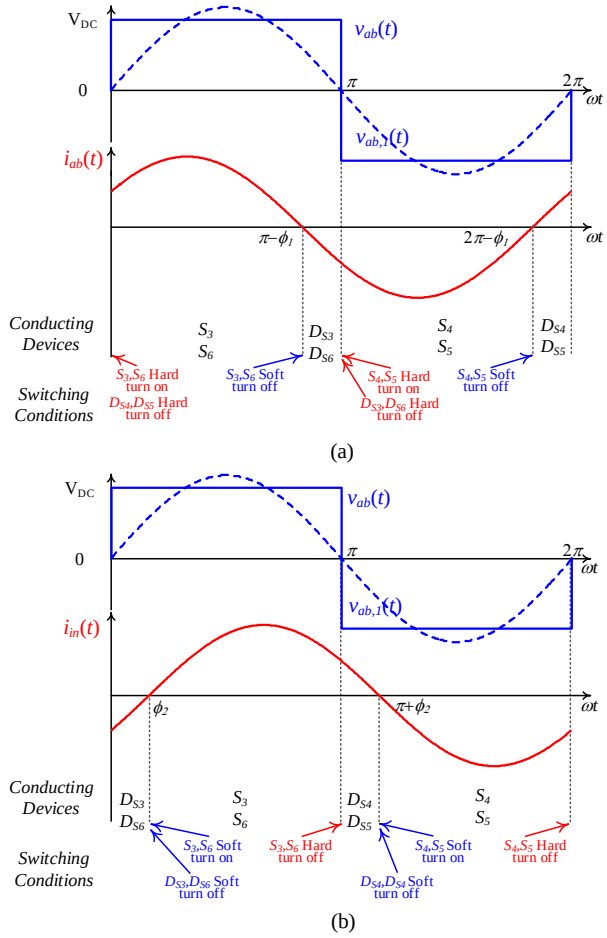



Fig. 3.3. Switching output waveforms in continuous conduction mode for resonant converters with (a) capacitive $Z_{in}$, and (b) inductive $Z_{in}$.

Fig. 3.3(b) illustrates the circuit operation in inductive region. $Z_{in}$ is inductive, $i_{in}(t)$ lags $v_{in}(t)$ with certain phase difference $\phi_2$. As seen in the figure, the turn-on process of switches, and the turn-off process of freewheeling diodes are both soft switching. However, the turn-off process of switches is hard switching. The reverse recovery losses from the freewheeling diodes are eliminated. The freewheeling diodes do not need to have very fast reverse-recovery characteristics. Thus, MOSFETs are suitable as primary switches in high switching frequency applications. Moreover, by paralleling small snubber capacitors directly with the switches, the turn-off losses of

the switches could be eliminated.

Operating the converter in high switching frequency would reduce the size of energy storage components and effectively improve the energy density of the converter. Therefore, only MOSFETs in high frequency application and inductive operations are considered in the following analyses.

SRC and PRC are single resonance converters. $f_p$ is the only resonance frequency of the resonant circuit. LCC has two resonance frequencies. $f_p$ is the frequency of the primary resonance. $f_{s,LCC}$ is the frequency of the secondary resonance between $L_r$, $C_r$, and $C_p$. $f_{s,LCC}$ could be calculated as,

$$i_{in,rms} \approx i_{in,1,rms} = \left| \frac{v_{in,1,rms}}{Z_{in}} \right| = \frac{2\sqrt{2}V_{DC}}{\pi} \left| \frac{1}{Z_{in}} \right| \tag{3.10}$$

$$f_{s,LCC} = \frac{1}{2\pi\sqrt{L_r C_r C_p / \left(C_r + C_p\right)}} \tag{3.11}$$

Similar to LCC, LLC also has two resonance frequencies. $f_p$ is the frequency of the primary resonance. $f_{s,LLC}$ is the frequency of the secondary resonance between $L_r$, $L_m$, and $C_r$. $f_{s,LCC}$ could be calculated as,

$$f_{s,LLC} = \frac{1}{2\pi\sqrt{C_r\left(L_r + L_m\right)}} \tag{3.12}$$

To illustrate different load conditions, quality factor $Q$ is introduced. $Q$ is defined to be the ratio between characteristic impedance ( $\sqrt{L_r / C_r}$ ) and $R_{ac}$.

$$Q = \frac{\sqrt{L_r C_r}}{R_{ac}} \tag{3.13}$$

Large $Q$ corresponds to small load resistance and heavy load condition. On the contrary, small $Q$ corresponds to large load resistance and light load condition.

## *3.3 Charging Profile of Li-ion Battery*

A battery cell is an electrochemical unit, which stores chemical energy and converts it to electrical energy. Among suitable batteries for PEVs [4], Li-ion batteries have the advantage of higher energy densities, no memory effect, and only a slow loss of charge when not in use [72].Thus, Li-ion batteries are growing in popularity for PEV applications. In this chapter, Li-ion battery is used as a case study to investigate the performance of resonance charger topologies.

Constant current (CC) and constant voltage (CC) charging is a commonly used charging strategy, which achieves fast charging while avoiding battery performance degradation [73]. Fig. 3.4 provides the charging characteristic of a single Li-ion battery cell. The battery cell has 3.6 V nominal voltage, and 2350 mAh capacity. A depleted battery is firstly charged with CC mode, and the voltage begins to increase. When the voltage reaches 4.2 V, the charging enters into CV mode, and the current begins to decrease. In the intersection between the CC mode and CV mode, the maximum charging power is achieved.

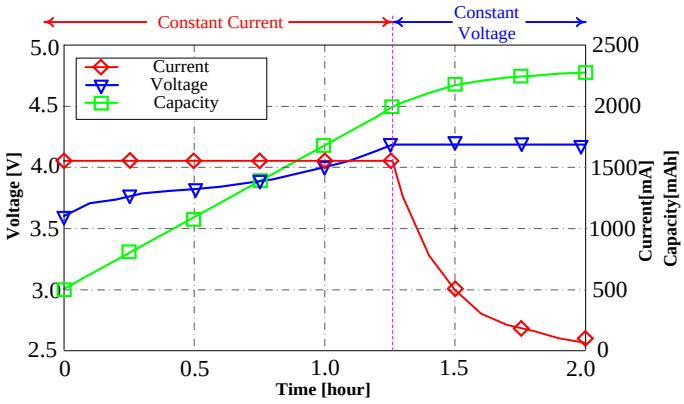



Fig. 3.4. Charging characteristics of a Li-ion battery cell.

Based on the charging data of single battery cell, the charging profile of a Li-ion battery pack could be obtained, as plotted in Fig. 3.5. The charging power of this battery pack is rated at 3.2 kW. In the charging process, battery on the load side could be equivalent to a resistor, whose resistance is equal to battery voltage over charging current.

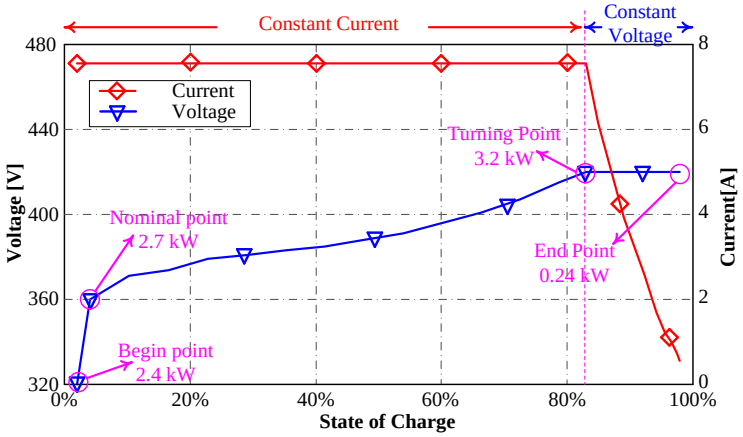



Fig. 3.5. Charging profile of a 360 V Li-ion battery pack rated at 3.2 kW.

According to Fig. 3.5, there are four key points in the charging process. Begin point and end point correspond to the beginning and end of the charging process, respectively. At nominal point, the battery voltage is equal to the nominal voltage of the battery pack. Turning point marks the transition from CC to CV charging mode.

Parameters of those four key points are summarized in Table 3-1. The quality factors could be easily calculated based on Eq. (3.10).

Table 3-1 Key points in the 3.2 kW charging profile of the PEV battery pack

| Parameter | Begin Point | Nominal point | Turning point | End point |
|---|---|---|---|---|
| $V_{bat}$ | 320V | 360V | 420V | 420V |
| $I_{bat}$ | 7.56A | 7.56A | 7.56A | 0.56A |
| $P$ | 2.4kW | 2.7kW | 3.2kW | 0.24kW |
| $R_L$ | 42.3 Ω | 47.6 Ω | 55.6 Ω | 750 Ω |

In the following sections, the analyses of resonant converter topologies are based on the charging profile of this 360 V Li-ion battery pack.

## *3.4 Basic Design and Comparison Considerations*

For the convenience of comparison, the dc link voltages and primary resonance frequencies are designed to be 300 V, and 200 kHz, respectively. MOSFTs are chosen as the primary switches. Thus, all the converters are designed to operate in inductive region.

According to previous analysis, in inductive operation, the turn-on of MOSFETs and the turn-off of freewheeling diodes are lossless. Besides, negligible losses are associated with the turn-on process of power diodes [37]. Hence, the dominant losses in inductive operation are conduction losses. Conduction losses are determined by the circulating energy in the resonant tank. High circulating energy in the resonant tank corresponds to high conduction loss. The circuit circulating power in the resonant tank could be calculated as,

$$P_c = \sum_{L=Lr,Lp} i_{L,rms}^2 j\omega L + \sum_{C=Cr,Cp} i_{C,rms}^2 \frac{1}{j\omega C} \tag{3.14}$$

By comparing the circulating power in the circuit, we are able to compare the related conduction losses in the converters.

At $f_p$, $L_r$ and $C_r$ resonate, and resonance impedance is zero. Thus, the circulating energy and consequently the conduction losses in $L_r$ and $C_r$ are minimized. However, with the increase of switching frequency (higher than $f_p$), the impedance of the resonant tank would increase. Thus, more energy would be circulated in the resonant tank instead of being transferred to the output [35]. The increased circulating energy increases the conduction losses and deteriorates the conversion efficiency. Usually, operating the converter in inductive region and closer to $f_p$ would have smaller conduction losses and thus higher conversion efficiency.

Since the turn-off of MOSFETs is hard switching, the related switching losses are the second important source of converter losses. The switching losses in the semiconductor devices are proportional to the switching frequency. High switching frequency corresponds to high turning-off losses from the MOSFETs.

In this specific battery charging applications, the switching frequency at "nominal point" is designed to be close to $f_p$. Thus, operating close to "nominal point" incurs both small conduction losses and small switching losses. The worst conversion efficiency corresponds to the "end point", which has lightest load condition and highest switching frequency. Therefore, in designing resonant converter, the target is

to optimize the circuit performance at the "end point", where the highest conduction losses and switching losses are expected.

Another important performance parameter of resonant converter is its short circuit protection capability. When short circuit happens, the power management module would boost the switching frequency to a higher value. Thus, the input impedance of the resonant tank would increase, which would limit the short circuit current.

Based on the aforementioned considerations, the aforementioned full bridge isolated resonant converters are designed and compared. Parameters of these circuits are provided in Table 3-2. Comparisons are made in Section 3.5.

Table 3-2 Parameters of designed resonant chargers

| Parameter | SRC | PRC | LCC | LLC |
|---|---|---|---|---|
| $n$:1 | 2/3 | 2 | 1.1 | 1 |
| $C_r$ | 10nF | 15nF | 15nF | 15nF |
| $L_r$ | 63.3μH | 42.2μH | 42.2μH | 42.2μH |
| $C_p$ | n/a | n/a | 14nF | n/a |
| $L_m$ | n/a | n/a | n/a | 42.2μH |
| $Q$ range | 0.29~ 5.22 | 0.022~ 0.39 | 0.072~ 1.28 | 0.087~ 1.55 |

## *3.5 Comparison of Resonant Converters in PEV Battery Charging Applications*

### 3.5.1 Series Resonant Charger

Based on equations (3.7-3.9), the dc voltage and current characteristics of the SRC PEV battery charger are plotted in Fig. 3.6. Five curves correspond to five load conditions, which include those four key points in the charging process, as well as the

short circuit condition. As seen in the figure, at $f_p$, SRC has the maximum voltage gain and operates as a constant voltage source. This is because the impedance of $L_r$ and $C_r$ is zero at $f_p$. The load voltage is equal to the input voltage. In order to provide some gain margin, this voltage is designed to be slightly higher than 420 V. With switching frequency higher than $f_p$, the impedance of the $L_r$ dominates the impedance of the resonant tank, which makes the circuit inductive.

In CC charging mode, the switching frequency shifts from 219.9 kHz to 212.2 kHz. This means low circulating energy in the resonant tank and small conduction losses. Generally, SRC charger has good performance in the CC charging mode.

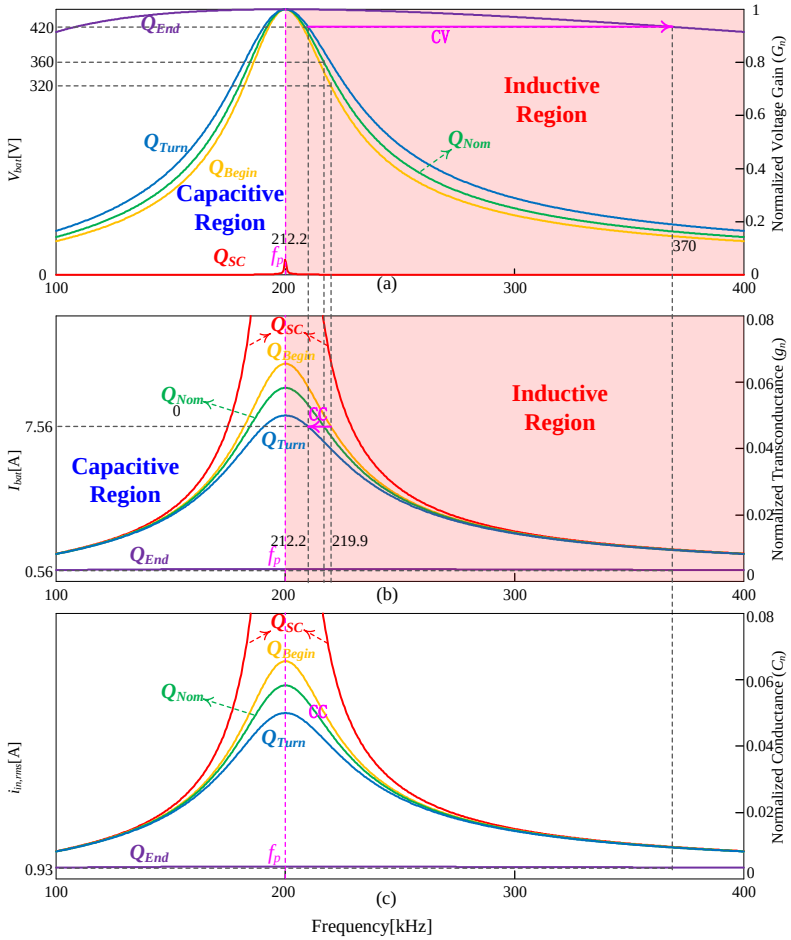



Fig. 3.6. Dc voltage and current characteristics of the SRC charger.

The second advantage of SRC battery charger is its good short circuit protection performance. As seen in Fig. 3.6, since the curve current at $Q_{SC}$ is steep, it is easy to boost the switching frequency to control the short circuit current.

Since the load is series with the resonant tank, the current flowing through the load is equal to the current circulating in the resonant tank. This makes the circuiting power in the resonant tank small in CV mode. Thus, the conduction losses are also small. Let's takes the "end point" as an example. At "end point", switching frequency goes to 370 kHz while input rms current is 0.93 A. Since the impedance of $L_r$ dominates the impedance of the resonant tank, circulating power could be approximated as,

$$P_c \approx i_{in,rms}^2 j\omega L_r = 84.9VA \tag{3.15}$$

This value is small In comparison with other topologies.

However, the critical defect of SRC lies in its unacceptable poor voltage regulation performance in light load condition. In light load condition, the slope of voltage curve is extremely small, which makes it hard to regulate the voltage.

Moreover, since the switching frequency is moved to a large value, this makes SRC suffer from high switching losses in CV charging mode. As a result, SRC is not a good candidate for PEV battery charger.

### 3.5.2 Parallel Resonant Charger

Similarly, the dc voltage and current characteristics of the PRC PEV battery

charger are plotted in Fig. 3.7. As seen in the figure, at $f_p$, PRC has the highest voltage gain in inductive region. The charging current is constant at $f_p$. In order to provide some margin, this current is designed to be slightly higher than 7.56 A. With switching frequency higher than $f_p$, the impedance of the $L_r$ dominates the impedance of the resonant tank, which makes the circuit inductive.

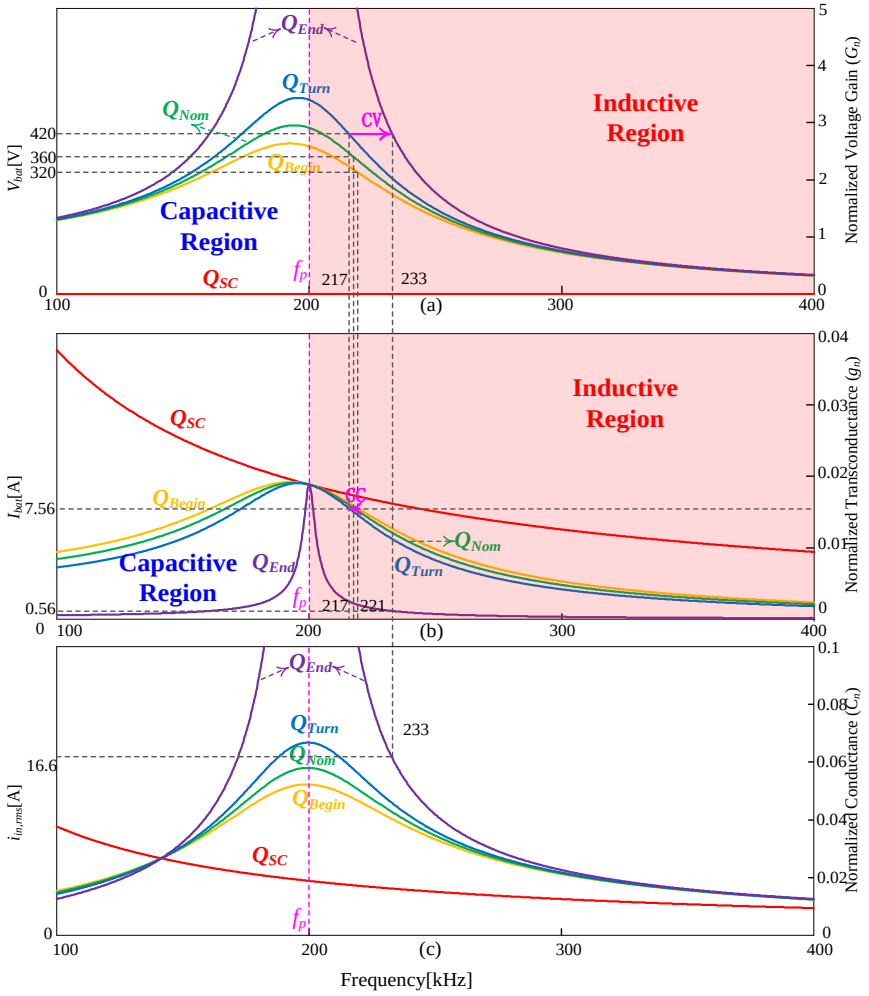



Fig. 3.7. Dc voltage and current characteristics of the PRC charger.

In CC charging mode, the operating frequency shifts from 221 kHz to 217 kHz. This means low circulating energy in the resonant tank and small conduction losses. Similar to SRC, PRC charger also has good performance in the CC charging

mode.

PRC battery charger also has good short circuit protection performance. When the short circuit happens, the input current would be limited by the impedance of $L_r$. As can be seen in Fig. 3.7, in inductive region, the short circuit current is always smaller than the constant current at $f_p$.

In constant voltage charging, the operating frequency shifts from 217 kHz to 233 kHz. As could be observed in Fig. 3.7, the input current is relatively independent on the load condition. This is the main disadvantage of PRC. This characteristic incurs its poor performance in light load or small quality factor condition. Let's take the "end point" as a simple example. At "end point", switching frequency is shifted to 233 kHz while input rms current is 16.6A. Since impedance of $L_r$ dominates impedance of the resonant tank, circulating power could be approximated as,

$$P_c \approx i_{in,rms}^2 j\omega L_r = 17.0kVA \tag{3.16}$$

This value is much larger than that of SRC. Thus, most of the current is circulating in the resonant tank and does not contribute to the power delivered to the load. This means high conduction losses and low conversion efficiency. Consequently, PRC is not a good candidate for PEV battery charger.

### 3.5.3 LCC Series-parallel Charger

The dc voltage and current characteristics of the LCC PEV battery charger are plotted in Fig. 3.8. As seen in the figure, in the boundary between inductive and

capacitive regions, LCC converter has the peak voltage gain. At $f_p$, LCC converter operates as a constant voltage source. While at $f_{s,LCC}$, LCC converter operates as a constant current source. In inductive region and within the same load line, both the voltage gain and transconductance decrease with the increase of switching frequency.

LCC is capacitive if the converter is operating below $f_p$, and is inductive if the converter is operating above $f_{s,LCC}$. In between $f_p$ and $f_{s,LCC}$, capacitive or inductive nature of input impedance is determined by the load condition. In inductive region, the impedance of the $L_r$ dominates the impedance of the resonant tank.

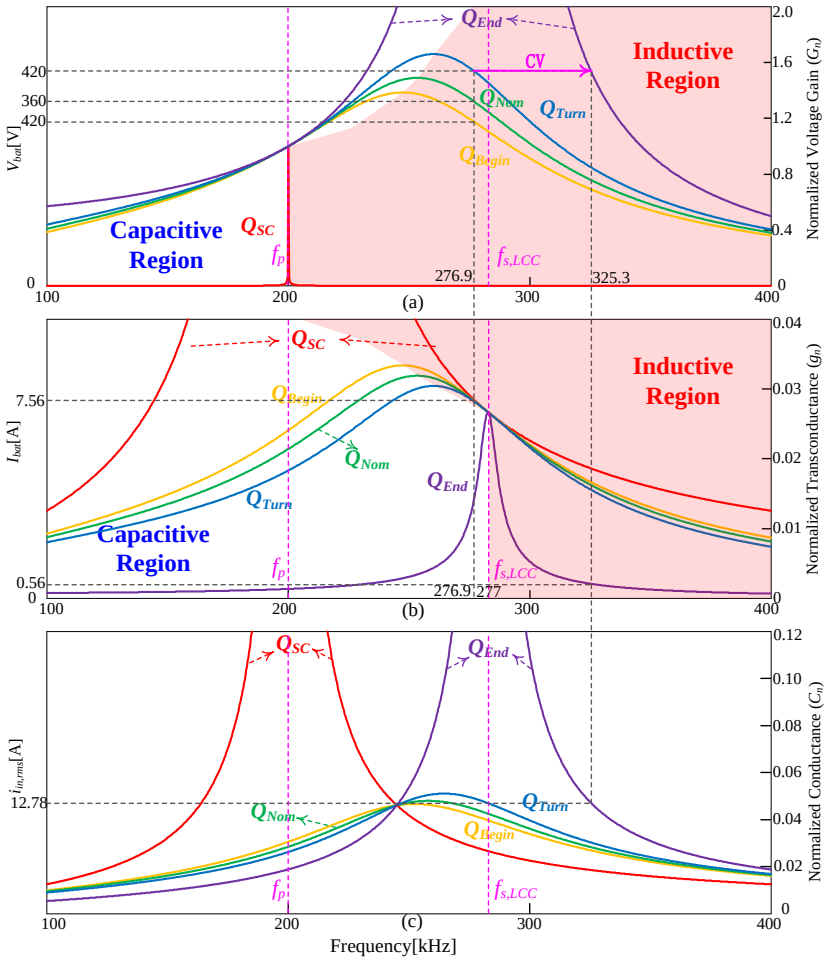



Fig. 3.8. Dc voltage and current characteristics of the LCC charger.

In CC charging mode, switching frequency shifts from 277 kHz to 276.9 kHz. This means the voltage is very sensitive to the load variation in CC charging mode. In comparison with PRC circuit, this frequency is further away from $f_p$. This means LCC converter has relatively high circulating energy in the resonant tank and large conduction losses in CC charging mode.

LCC battery charger also has good short circuit performance. When the short circuit happens, the input current is limited by the impedance of the inductance. As seen in Fig. 3.8(b), it is easy to limit the short circuit current by slightly boosting the switching frequency.

In CV charging mode, the operating frequency shifts from 276.9 kHz to 325.3 kHz. Similar to PRC, LLC also suffers from its poor performance in light load condition. This could be observed in Fig. 3.8. Let's take the "end point" as a simple example. At "end point", switching frequency goes to 325.3 kHz while input rms current is 12.78A. Since the impedance of $L_r$ dominates the impedance of the resonant tank, the circulating power could be approximated as,

$$P_c \approx i_{in,rms}^2 j\omega L_r = 14.1kVA \tag{3.17}$$

This value is much larger than that of SRC and around the same level as that of PRC. Most of the current is circulating in the resonant tank and does not contribute to the power delivered to the load. This means high conduction losses and low conversion efficiency.

Actually, beyond the secondary resonance frequency ($f_{s,LCC}$), the LCC circuit

behaves like a PRC converter. This is because at this condition, the impedance of $L_r$ is much larger than the impedance of $C_r$, which makes $L_r$ and $C_r$ behave like an inductor. This explains why LCC circuit has the same problem as PRC circuit in light load condition. Hence, LCC is not a good candidate for PEV battery charger.

### 3.5.4 LLC Series-parallel Charger

The dc voltage and current characteristics of the LLC PEV battery charger are plotted in Fig. 3.9. As seen from the figure, in the boundary between inductive and capacitive regions, LLC converter has the peak charging current. At $f_p$, LLC converter operates as a constant voltage source. While at $f_{s,LLC}$, LLC converter operates as a constant current source. In inductive region and within the same load line, both the voltage gain and transconductance decrease with the increase of switching frequency.

LLC is capacitive if the converter is operating below $f_{s,LLC}$, and is inductive if the converter is operating above $f_p$. In between $f_{s,LLC}$ and $f_p$, capacitive or inductive are determined by the load condition. In inductive region, the impedances of the $L_r$ and $L_m$ dominate the impedance of the resonant tank.

In CC charging mode, the switching frequency shifts from 193.3 kHz to 168 kHz. In comparison with LCC circuit, this frequency is smaller and closer to $f_p$. This means LLC has relatively smaller circulating energy in the resonant tank and smaller conduction losses in CC charging mode than LCC. In CV charging, the operating frequency shifts from 276.9 kHz to 325.3 kHz. At light load condition, the slope of voltage curve is still big, which makes it easy to regulate the output voltage. This makes LLC outperform SRC.

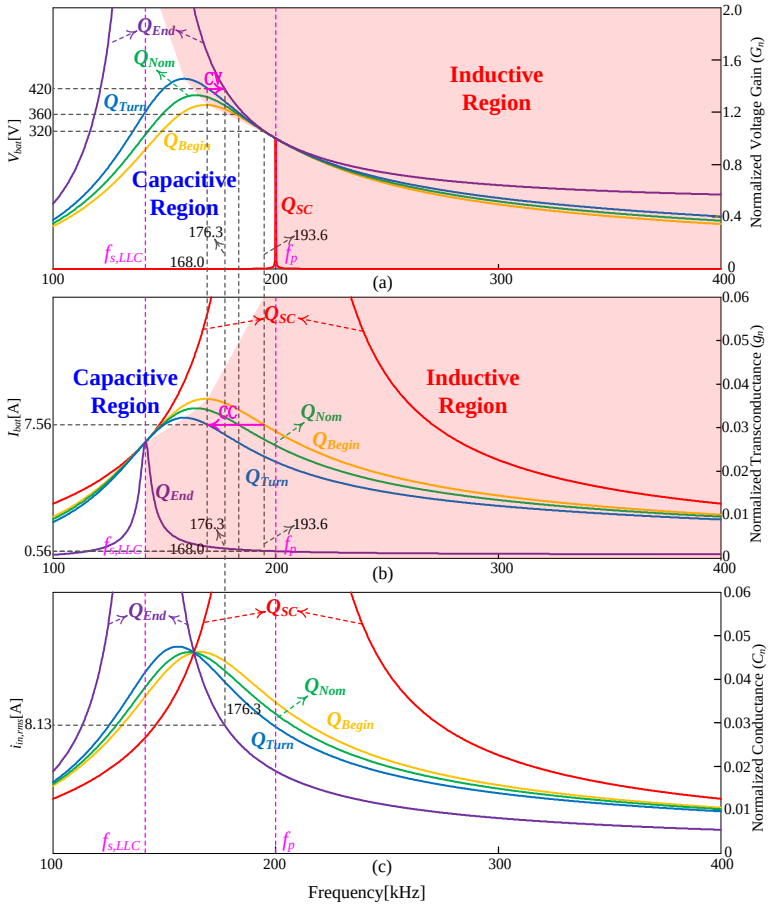



Fig. 3.9. Dc voltage and current characteristics of the LLC charger.

The short circuit performance of LLC is not as good as the other three resonant converters, but it is sufficient to control the short circuit current. This is because beyond $f_p$, the impedance of inductors is large enough to regulate the short circuit current. As seen in Fig. 3.9(b), by boosting the switching frequency, the short circuit current could be successfully reduced to normal level.

The performance in light load condition of LLC is much better than PRC and LCC. This could be observed in Fig. 3.9. Let's take the "end point" as a simple example. At "end point", switching frequency goes to 176.3 kHz while input current is 8.13A. The circulating power could be calculated as,

$$P_c = i_{in,rms}^2 j\omega L_r + i_{in,rms}^2 \frac{1}{j\omega C_r} + i_{Lm,rms}^2 j\omega L_m = 1.79kVA \tag{3.18}$$

This value is much smaller than that of PRC and LCC. This means much less conduction losses and higher conversion efficiency in CV charging mode.

Moreover, the switching frequency of LLC is much smaller than the other three topologies in the full load range. This means the LLC has the smallest switching losses among those four resonant converters.

The performances of SRC, PRC, LCC, and LLC chargers are summarized in Table 3-3. It is clear that LLC has good performance in the full range of battery SOC. Thus, LLC is a more suitable candidate for PEV battery chargers.

Table 3-3 Comparison of resonant converters in PEV charging applications

| Performance | SRC | PRC | LCC | LLC |
|---|---|---|---|---|
| Voltage regulation capability at high SOC | Bad | Good | Good | Good |
| Additional filter inductor on secondary side | No | Yes | Yes | No |
| Frequency range in CC charging mode | 219.9~212.2 kHz | 221~217 kHz | 277~276.9 kHz | 193.6~167.3 kHz |
| Efficiency in CC charging mode | High | High | Moderate | High |
| Short circuit protection performance | Very good | Very good | Very good | Good |
| Frequency range in CV charging mode | 212-370 kHz | 217-233 kHz | 276.9-325.3 kHz | 168.0-176.3 kHz |
| Circulating energy at highest SOC | 84.9 VA | 17.0 kVA | 14.1 kVA | 1.79 kVA |
| Conduction losses in CV charging mode | Very small | Very large | Very large | Small |
| Conduction losses in | Large | Small | Moderate | Small |

| | | | | |
|---|---|---|---|---|
| CV charging mode | | | | |
| Efficiency in CV charging mode | Moderate | Low | Low | Moderate |

### *3.6 Summary*

In this chapter, four resonant topologies (SRC, PRC, LCC, and LLC) are analyzed and compared in terms of their performance characteristics for PEV battery charging applications. A new methodology is proposed to effectively evaluate the circuit performance in battery charging applications. This methodology includes evaluating the battery voltage, charging current, as well as the input rms current characteristics to design the resonant chargers and to compare the chargers' performance.

Using the proposed method, four full bridge isolated resonant chargers, which are rated at 3.2 kW and used to charge a 360 V Li-ion battery pack, are designed and evaluated. Based on the analytical results, it is shown that LLC charger takes the advantages of LCC and PRC chargers, while avoiding the drawbacks of SRC chargers. LLC could maintain better efficiency, voltage regulation, as well as short circuit protection performance over the full range of battery SOC. Thus, LLC could be chosen as an excellent candidate for PEV battery charging applications.

# Chapter 4 Design and Analysis of a Full Bridge LLC Based PEV Charger Optimized for Wide Battery Voltage Range

## *4.1 Introduction*

High power density, high conversion efficiency, high power factor, and low THD are the desired features expected from onboard plug-in electric vehicle (PEV) battery chargers [74]–[76]. Fig. 4.1 shows the general power electronics architecture of a typical onboard PEV battery charger. The system consists of a front-end ac/dc converter used for rectification at unity power factor, and a second stage dc/dc converter responsible for battery current regulation and providing galvanic isolation [52], [77].

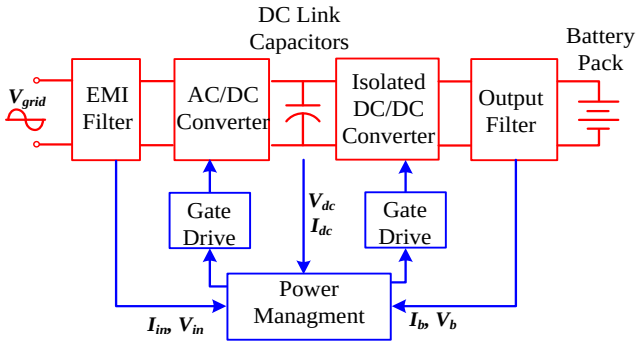



Fig. 4.1. General system architecture of a battery charger.

Boost converter is the common front-end PFC interface due to its simple structure, good THD reduction performance, and unity power factor operation capability [78]. However, the volume of the converter tends to increase with the increase of charging power. Moreover, high root mean square (rms) current in the dc link capacitors would generate high power loss and significantly reduce the capacitor's lifetime, leading to capacitor failures. In addition, the required inductance

value to reduce the ripples in the input current for better THD performance, would considerably increase as the charging power increases [79]. This results in a large-volume inductor core and wire size. In comparison with single phase boost PFC converter, the interleaved boost topology has the benefits of reduced overall volume and improved power density [80]–[82].

In the dc/dc isolation stage, resonant converters are preferable at high voltage and high power PEV battery charging applications. In particular, multi-resonance based LLC topology has several advantages over other resonant topologies, such as (a) good voltage regulation performance at light load condition, (b) the ability to operate with zero voltage switching (ZVS) over wide load ranges, (c) no diode reverse recovery losses through soft commutation, (d) low voltage stress on the output diodes, and (e) having only a capacitor as the output filter compared to the conventional LC filters [83], [84]. Despite these advantages, operating the circuit at the maximum efficiency considering the conduction and switching losses over the full output voltage ranges remains as a challenging issue, as the battery voltage varies in a wide range depending on the different state-of-charge (SOC) [45], [85], [86].

In this chapter, an onboard PEV charger topology consisting of an interleaved boost PFC rectifier followed by an LLC multi-resonant dc/dc converter is proposed. Both the interleaved boost PFC and the full-bridge LLC stages are extendable to much higher power levels with high power density and conversion efficiency. The proposed charger design is optimized for a wide voltage range (320V-420V) in a Lithium-ion battery pack. Moreover, the optimum design of LLC magnetic

components, to achieve the maximum overall efficiency, is addressed in detail. In addition, circumstantial loss analysis is addressed to evaluate the LLC converter's overall performance.

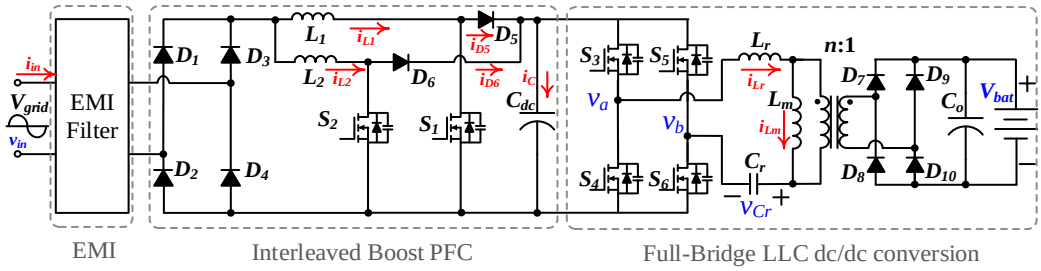



Fig. 4.2. Schematic of proposed interleaved level 2 isolated onboard charger.

## 4.2 *General Boost Converter*

As shown in Fig. 4.3, a general boost converter consist of an inductor *L*, a switch *S*, a diode *D*, and a filter capacitor *C*. The switch is turned on and off periodically with the period equals to *T*. The waveforms of the boost converter is plotted in Fig. 4.4.

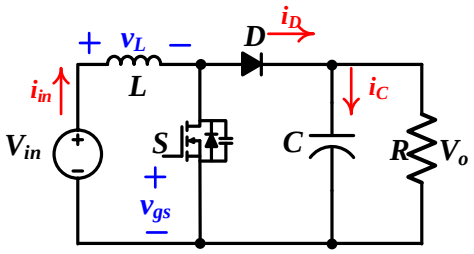



Fig. 4.3. Schematic of the general boost converter.

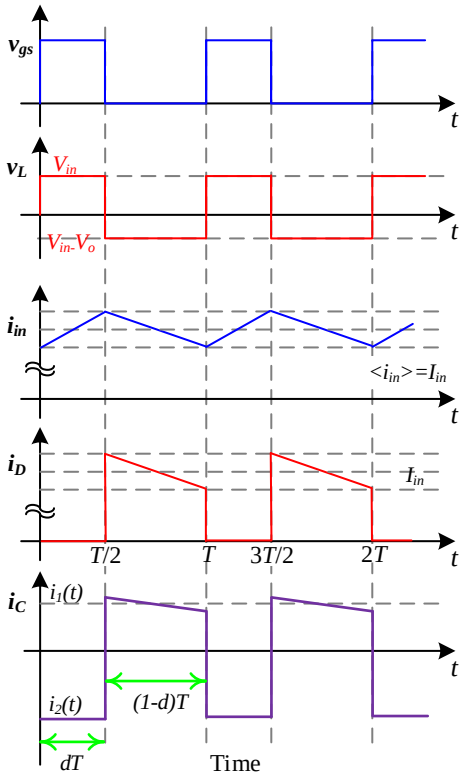



Fig. 4.4. Simulated waveforms of the general boost converter.

In (0, $dT$], the switch is on while the diode is off; the voltage across the inductor is the input voltage ($V_{in}$). In ($dT$, T], the switch is off while the diode is on; the voltage across the inductor is the input voltage subtract output voltage ($V_{in}$-$V_o$). According to the volt-second balance of inductor, the average voltage applied to the inductor during one switching period is zero as shown in Eq. (4.1).

$$dV_{in} + (1-d)(V_{in} - V_o) = 0 \tag{4.1}$$

According to Eq. (4.1), the relationship between input voltage and output voltage could be calculated as Eq. (4.2),

$$V_o = V_{in} / (1-d) \tag{4.2}$$

According to the principle of energy conservation, the power input equals to the power delivered to the load.

$$V_{in} I_{in} = V_o I_o \tag{4.3}$$

where $I_{in}$ and $I_o$ are the average values of input and output currents.

From equations (4.2) and (4.3), the relationship between input and output current is calculated as Eq. (4.4).

$$I_o = I_{in} / (1 - d) \tag{4.4}$$

In (0, $dT$], the input current increases at the speed of $V_{in}/L$. Thus, the input current ripple is calculated as Eq. (4.5),

$$\Delta i_{in} = i_{\max} - i_{\min} = dT \frac{V_{in}}{L} \tag{4.5}$$

For a single phase boost converter, the input current ($i_{in}$) equals the inductor current ($i_L$). Thus, the ripple current ratio [$K(d)$], which is defined to be the ratio between $i_{in}$ *and* $i_L$, is always equals to 1, as Eq. (4.6).

$$K(d) = \frac{i_{in}}{i_L} = 1 \tag{4.6}$$

Since the switching period is very small (usually smaller than 20 μs), the input current in each switching cycle could be approximated as a constant. Thus, the capacitor current ripple could be looked as a square wave. The envelope of the capacitor square wave is calculated as equations (4.7) and (4.8),

$$i_1(t) = i_{in}(t) - i_o(t) = i_{in}(t)d(t) \tag{4.7}$$

$$i_2(t) = -i_o(t) = -i_{in}(t)[1-d(t)] \tag{4.8}$$

For a single phase boost converter, the rms capacitor current can be calculated as Eq. (4.9),

$$i_{c,rms}(t) = \sqrt{i_2(t)^2 d(t) + i_1(t)^2[1-d(t)]} \tag{4.9}$$

Substituting equations (4.7) and (4.8) into Eq. (4.9), the normalized output capacitor rms current $i_{rms,1}/i_{in}$ can be obtained as,

$$i_{c,rms}(t)/i_{in}(t) = \sqrt{d(t) - d(t)^2} \tag{4.10}$$

## *4.3 Interleaved Boost Converter*

An interleaved converter is simply a multi-leg converter, each leg operating $360^o/n$ out of phase, where $n$ denotes the number of phases. A two-leg interleaved boost converter, whose interleaving legs are operated with $180^o$ phase difference, is shown in Fig. 4.5. The control of the interleaved converters is based on shifting the phase of $S_1$ with respect to $S_2$ such that the ripples cancel out the each other.

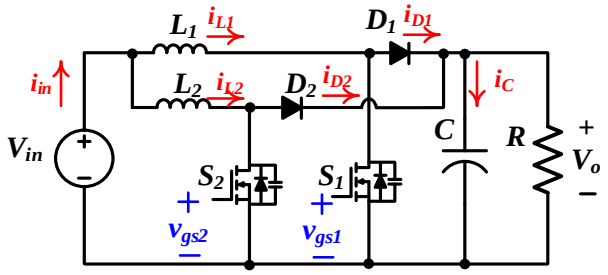



Fig. 4.5. Schematic of two phase interleaved boost converter.

### 4.3.1 Interleaving Effect on Input Ripple Current

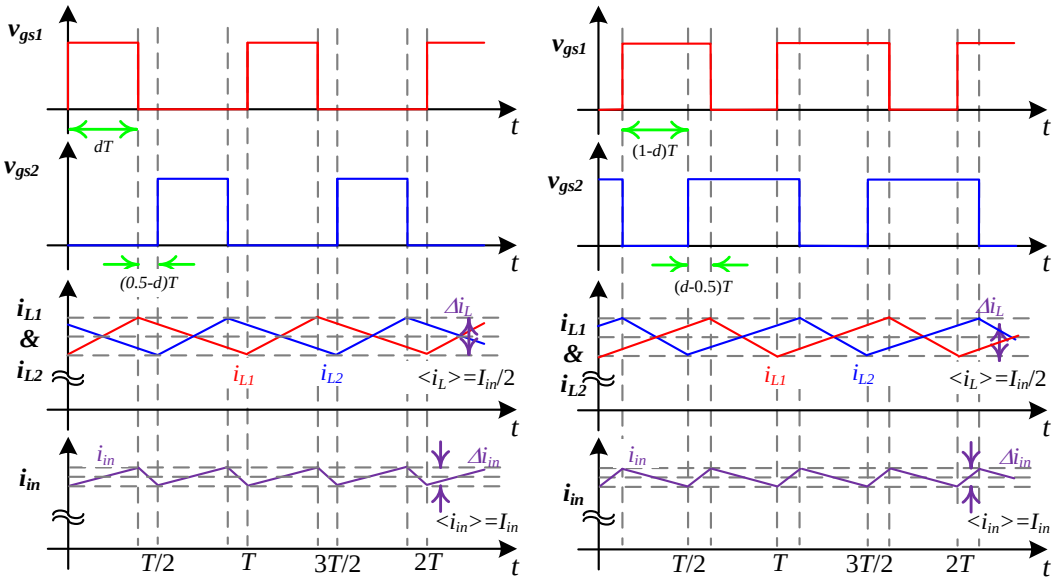



Fig. 4.6. Input current ripple of 2-phase interleaved boost converter. (a) $d <$ 0.5. (b) $d >$ 0.5.

The simulated current ripple waveforms of two phase interleaved boost converter are presented in Fig. 4.6. In one switching period (0, $T$], $S_1$ is on in [0, $dT$); $S_2$ is on in [$T$/2, $T$/2+$dT$). The input current ($i_{in}$) is the sum of the two inductor currents ($i_{L1}$+ $i_{L2}$). Since the regions [0, $T$/2) and [$T$/2, $T$) are symmetrical, the frequency of the input current ripple is doubled. Thus, a half period [0, $T$/2) is sufficient to calculate the input current ripple.

If $d \leq 0.5$, from 0 to $dT$, $S_1$ and $D_2$ are on, while $S_2$ and $D_1$ are off. The voltage across $L_1$ is $V_{in}$. Thus, $i_{L1}$ increases at the speed of $V_{in}/L$. The voltage across $L_2$ is ($V_{in}$-$V_o$). Thus, $i_{L2}$ changes at the speed of ($V_{in}$-$V_o$)/$L$. Since $I_{in}$ = $I_{L1}$ + $I_{L2}$, $I_{in}$ increases from the minimum value to the maximum value at the speed of (2$V_{in}$-$V_o$)/$L$. Thus, the input current ripple could be calculated as Eq. (4.11),

$$\Delta i_{in} = i_{\max} - i_{\min} = dT\frac{2V_{in} - V_o}{L} = dT\frac{(1-2d)V_o}{L} \tag{4.11}$$

If $d > 0.5$, from 0 to $(d\text{-}0.5)T$, $S_1$ and $S_2$ are on, while $D_1$ and $D_2$ are off. The voltages across $L_1$ and $L_2$ are both $V_{in}$. Thus, both $i_{L1}$ and $i_{L1}$ increase at the speed of $V_{in}/L$. Since $I_{in} = I_{L1} + I_{L2}$, $I_{in}$ increases from the minimum value to the maximum value at the speed of $2V_{in}/L$. Thus, the input current ripple could be calculated as Eq. (4.12),

$$\Delta i_{in} = i_{\max} - i_{\min} = (d-0.5)T\frac{2V_{in}}{L} = (1-d)T\frac{(2d-1)V_o}{L} \tag{4.12}$$

Either when $d < 0.5$, or $d > 0.5$, for each inductor, the current ripple could be calculated as Eq. (4.13),

$$\Delta i_L = dT\frac{V_{in}}{L} = dT\frac{(1-d)V_o}{L} \tag{4.13}$$

Thus, the ripple current ratio, *K(d)*, could be calculated as Eq. (4.14).

$$K(d) = \frac{\Delta i_{in}}{\Delta I_L} = \begin{cases} \dfrac{1-2d}{1-d}, d \le 0.5 \\ \dfrac{2d-1}{d}, d > 0.5 \end{cases} \tag{4.14}$$

According to equations (4.10) and (4.14), the curves of normalized current ripple as a function of duty cycle are plotted in Fig. 4.7. As seen in Fig. 4.7, In comparison with single phase boost topology, the two phase interleaved boost converter has smaller normalized ripple current over the full duty cycle range. The best input inductor ripple current cancellation occurs at 50 percent duty cycle.

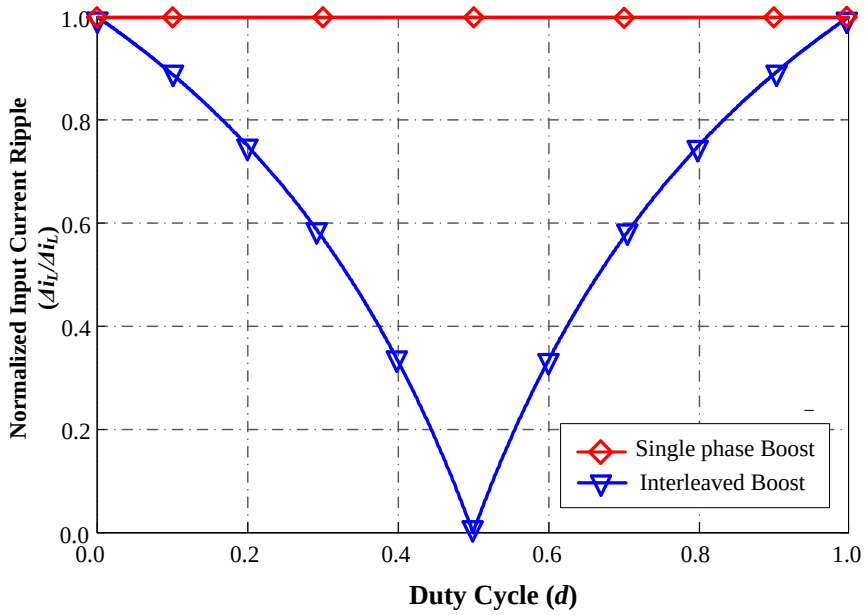



Fig. 4.7. Effectiveness of input ripple cancellation for interleaved converters.

### 4.3.2 Interleaving Effect on Magnetic Volume Reduction

The input current is evenly shared between two inductors. For the interleaved topology, the energy stored in the inductor is described as Eq. (4.15),

$$E = \frac{1}{2}L\left(\frac{I_{in}}{2}\right)^2 + \frac{1}{2}L\left(\frac{I_{in}}{2}\right)^2 = \frac{1}{4}LI_{in}^{\ 2} \tag{4.15}$$

According to Eq. (4.15), the energy stored in the inductor is reduced to half In comparison with single phase boost topology. This reduction could effectively reduce the total energy and inductor volume for the same criteria as of the conventional boost converter. A volume reduction of 32% is reported in case a two-leg interleaved structure is used [87].

### 4.3.3 Interleaving Effect on Output Capacitor

The root mean square (rms) current in the output capacitor generates power

losses due to the existence of equivalent series resistance (ESR). The temperature rise caused by the power loss may seriously reduce the capacitor life time [79].

For two phase interleaved boost converter, the output capacitor current is the sum of the two diode currents minus the dc output current ($i_{D1}$ + $i_{D2}$ - $i_o$). The output capacitor current waveform is plotted in Fig. 4.8.

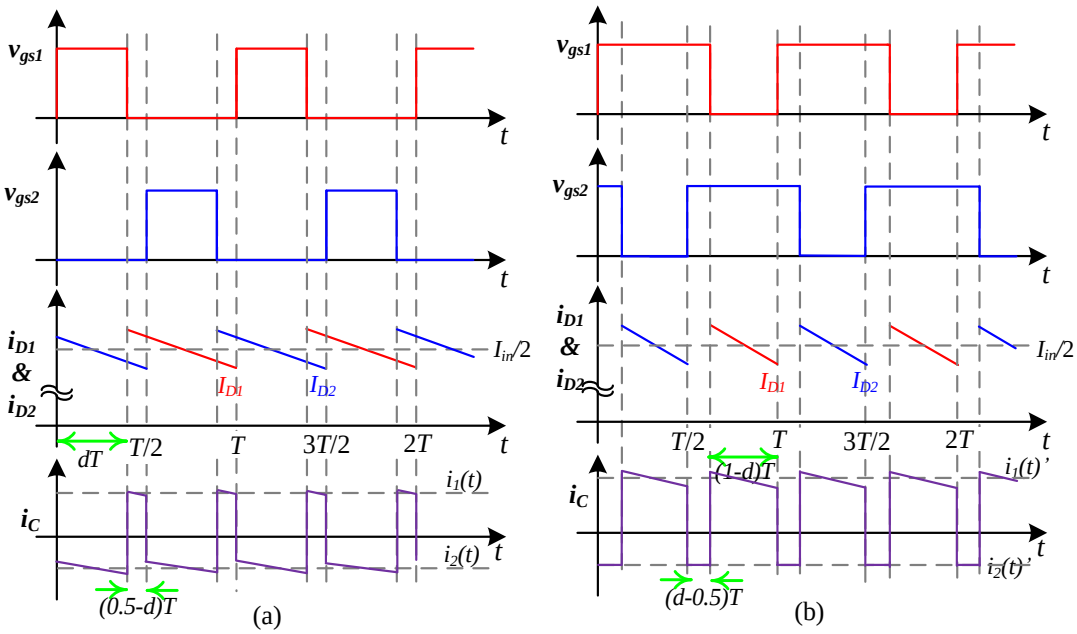



Fig. 4.8. Output capacitor current ripple of the 2 phase interleaved boost converter. (a) $d < 0.5$. (b) $d > 0.5$.

If $d \leq 0.5$ [see Fig. 4.8 (a)], the envelops of the capacitor current square wave of the double phase interleaved structure can be calculated as equations (4.16) and (4.17),

$$i_1(t) = i_{in}(t) - i_o(t) = d(t) i_{in}(t) \tag{4.16}$$

$$i_2(t) = \tfrac{1}{2} i_{in}(t) - i_o(t) = -[0.5 - d(t)] i_{in}(t) \tag{4.17}$$

If $d > 0.5$ [see Fig. 4.8 (b)], the envelops of the capacitor current square wave can be calculated as,

$$i_1'(t) = \tfrac{1}{2} i_{in}(t) - i_o(t) = i_{in}(t)[d(t) - 0.5] \tag{4.18}$$

$$i_2'(t) = -i_o(t) = -i_{in}(t)[1 - d(t)] \tag{4.19}$$

Hence, the rms value of capacitor current can be calculated as Eq. (4.20),

$$i_{c,rms}(t) = \begin{cases} \sqrt{2[0.5 - d(t)]i_1(t)^2 + 2d(t)i_2(t)^2} & d \le 0.5 \\ \sqrt{2[1 - d(t)]i_1'(t)^2 + 2[d(t) - 0.5]i_2'(t)^2} & d > 0.5 \end{cases} \tag{4.20}$$

Substituting equations (4.16-4.19) into Eq. (4.20), the normalized capacitor rms current $i_{c,rms}/i_{in}$ can be obtained as Eq. (4.21),

$$i_{c,rms}(t)/i_{in}(t) = \begin{cases} \sqrt{-d(t)^2 + 0.5d(t)} & d \le 0.5 \\ \sqrt{-d(t)^2 + 1.5d(t) - 0.5} & d > 0.5 \end{cases} \tag{4.21}$$

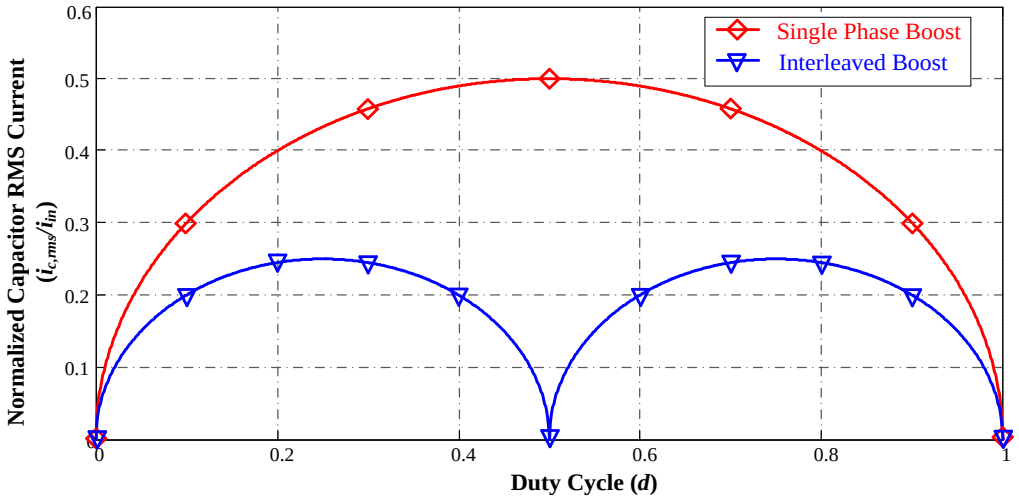



Fig. 4.9. Effectiveness capacitor rms current reduction for interleaved converters.

According to equations (4.14) and (4.21), the curves of normalized capacitor

rms current as a function of duty cycle are plotted in Fig. 4.9. In comparison with single phase boost structure, the peak capacitor rms current is reduced to half in the two phase interleaved structure. For the interleaved boost topology, as the duty cycle approaches 0, 0.5 and 1, the capacitor rms current would approach zero. The improvement in capacitor rms current reduces the power loss caused by ESR, reduces the electrical stress in the capacitor and improves the system reliability.

## 4.4 *Full Bridge LLC Converter*

A full-bridge LLC resonant converter is shown in Fig. 4.10. The series resonant network is formed by $L_r$, $C_r$, and $L_m$. $L_m$ is parallel with the load. There are two resonance in this resonant network. The primary resonance frequency ($f_p$) is determined by $L_r$ and $C_r$, while the secondary resonance frequency ($f_s$) is determined by $L_r + L_m$ and $C_r$. $f_p$ and $f_s$ are calculated in equations (4.22) and (4.23), respectively.

$$f_p = \frac{1}{2\pi\sqrt{L_r C_r}} \tag{4.22}$$

$$f_s = \frac{1}{2\pi\sqrt{(L_r + L_m)C_r}} \tag{4.23}$$

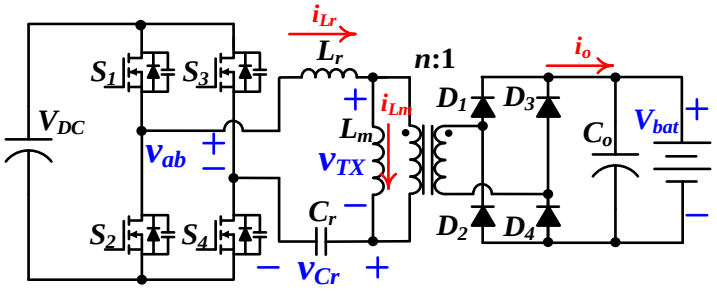



Fig. 4.10. Schematic of a full bridge LLC resonant converter.

Based on the relationship between the switching frequency ($f$), two resonant frequencies ($f_p$ and $f_s$), and the load condition, there are five possible modes of operation.

### 4.4.1 Operation Analysis with $f < f_s/2$

With the switching frequency smaller than $f_p/2$, the waveforms of the resonant tank input voltage ($v_{ab}$), resonant capacitor voltage ($v_{Cr}$), resonant inductor current ($i_{Lr}$), magnetizing inductor current ($i_{Lm}$), output current ($i_o$), and transformer primary voltage ($v_t$), are simulated. Fig. 4.10 denotes those parameters with the signs. When switches $S_1$ and $S_4$ is turned on, the initial value of $i_{Lr}$ could be either positive or negative, depending on the phase angle of the resonance. When $i_{Lr}(t_o)$ is positive, the simulated waveforms are shown in Fig. 4.11. The operation of half switching cycle can be divided into three modes, as shown in Fig. 4.12. The discussion below is based on the condition when $i_{Lr}(t_o)$ is positive.

Mode I ($t_o$, $t_1$)

According to Fig. 4.11, $i_{Lr}(t_o) > 0$. At $t_0$, body diodes $D_{S2}$ and $D_{S3}$ are turned off at a finite current and a finite voltage. Mode I begins at this moment. $i_{Lm}$ is equal to $i_L$; $i_{Lr}$ is positive and flows through $S_1$ and $S_4$. Switches $S_1$ and $S_4$ turns on at a finite current and at a finite voltage. Both the turn-off of $D_{S2}$ and $D_{S3}$ and the turn-on of $S_1$ and $S_4$ result in switching losses.

From $t_o$ to $t_1$, current flowing through $S_1$ and $S_4$ forces secondary diodes $D_1$ and $D_4$ to conduct. The voltage across the primary side of transformer and $L_m$ is $nV_o$.

Thus, $i_{Lm}$ increases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC} - nV_o$. $L_r$ resonates with $C_r$.

Mode II ($t_1$, $t_2$)

At $t_1$, $i_{Lm}$ reaches $i_{Lr}$ and mode II begins. Diodes $D_1$ and $D_4$ are turned off while diodes $D_2$ and $D_3$ is turned on.

From $t_1$ to $t_2$, the sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}+nV_o$. $L_r$ resonates with $C_r$.

During this mode, $i_{Lr}$ crosses zero twice somewhere in between $t_1$ and $t_2$. The auto switch of conductions happens between $S_1$ & $S_4$ and $D_{S1}$ & $D_{S4}$ at those time points.

Mode III ($t_2$, $t_3$)

At $t_2$, $i_{Lm}$ reaches $i_{Lr}$ again and mode III begins. Diodes $D_2$ and $D_3$ are turned off at zero current.

From $t_2$ to $t_3$, secondary diodes $D_{1\text{-}4}$ are all off. The sum of voltages applied across $L_m$, $L_r$ and $C_r$ equals to $V_{DC}$. $L_m$ *participates* in the resonance with $Lr$ and $C_r$. $i_{Lm}$ is equal to $i_{Lr}$.

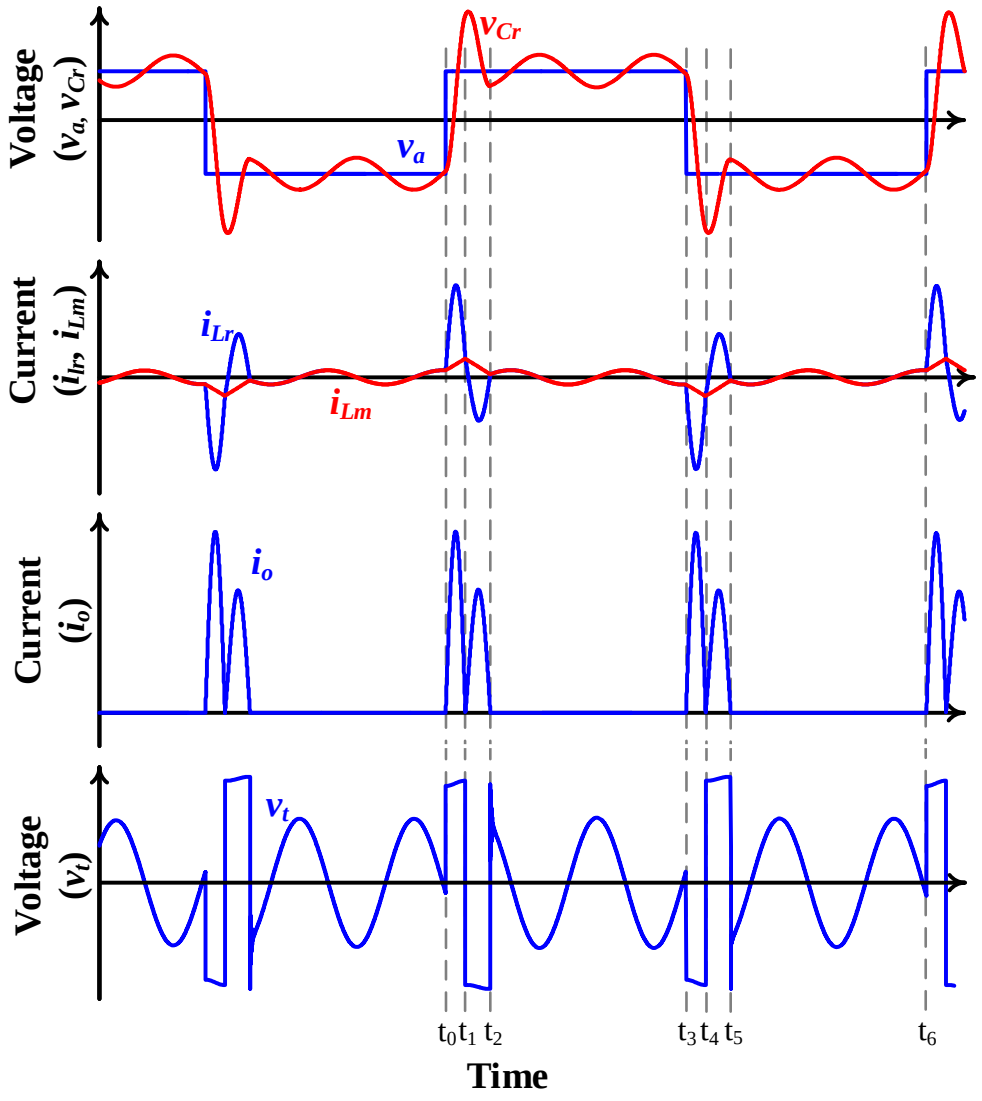



Fig. 4.11. Simulated waveforms of LLC resonant converter in ZCS operation with $f < f_s/2$ ($i_{Lr}(t_o) > 0$).

At this mode, depending on the switching period, $i_{Lr}$ crosses zero multiple times in between $t_2$ and $t_3$. Each time $i_{Lr}$ crosses zero, $S_1$ & $S_4$ and body diode $D_{S1}$ & $D_{S4}$ would swap conductions at zero voltage and zero current.

At $t_3$, switches $S_1$ & $S_4$ are turned off at a finite current and a finite voltage. Mode III ends at this moment. $i_{Lm}$ is equal to $i_{L;}$ $i_{Lr}$ is positive and flows through $S_2$ &

$S_3$. Body diode $D_{S2}$ & $D_{S3}$ is turned off at a finite current and at a finite voltage. Both the turn-on of $S_2$ & $S_3$ and the turn-off of $D_{S2}$ & $D_{S3}$ result in switching losses.

For the next half cycle, the operations are symmetrical to modes I-III.

According to the operation modes analysis, the switches are turned off at zero voltage and zero current. However, in the beginning of mode I and in the end of mode III, the turn-on of switches and the turn-off of body diodes are both hard switching.

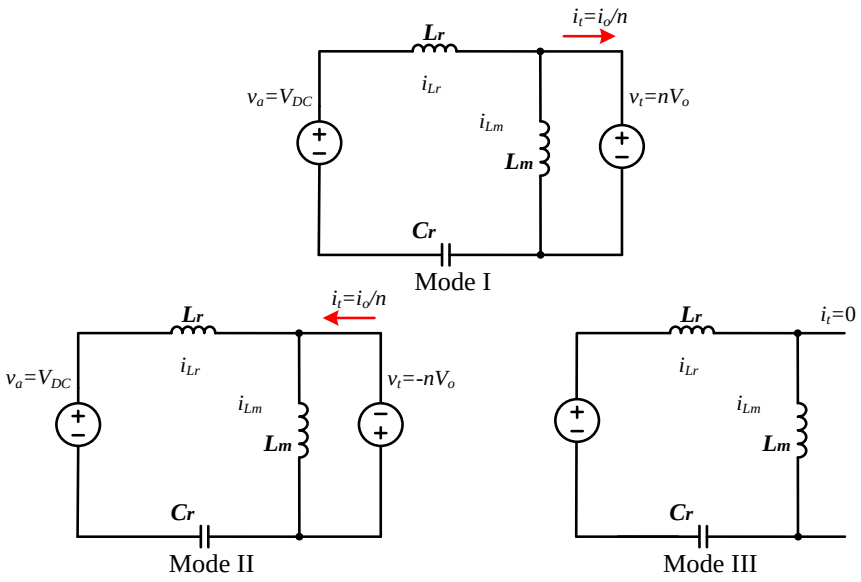



Fig. 4.12. Operating modes of LLC resonant converter in ZCS operation with $f < f_s/2$ ($i_{Lr}(t_o) > 0$).

### 4.4.2 Operation Analysis with $f_s/2 < f < f_s$

With the switching frequency between $f_s/2$ and $f_s$, the same group of waveforms is plotted in Fig. 4.13. The operation of half switching cycle can be divided into four modes. Fig. 4.14 shows those four operating modes.

Mode I ($t_o$, $t_1$)

At $t_0$, body diodes $D_{S2}$ & $D_{S3}$ are turned off at a finite current and a finite voltage. Mode I begins at this moment. $i_{Lm}$ is equal to $i_{L;}$ $i_{Lr}$ is positive and flows through $S_1$ & $S_4$. Switches $S_1$ & $S_4$ turns on at a finite current and at a finite voltage. Both the turn-off of $D_{S2}$ & $D_{S3}$ and the turn-on of $S_1$ & $S_4$ result in switching losses.

From $t_o$ to $t_1$, current flowing through $S_1$ & $S_4$ forces secondary diodes $D_1$ & $D_4$ to conduct. The voltage across the primary side of transformer and $L_m$ is $nV_o$. Thus, $I_{Lm}$ increases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}$ - $nV_o$. $L_r$ resonates with $C_r$.

Mode II ($t_1$, $t_2$)

At $t_1$, $i_{Lm}$ reaches $i_{Lr}$ and mode II begins. Diodes $D_1$ & $D_4$ are turned off at zero current without reverse recovery process.

From $t_1$ to $t_2$, the sum of voltages applied across $L_r$, $L_m$ and $C_r$ equals to $V_{DC}$. $L_m$ participates in the resonance with $L_r$ and $C_r$.

Mode III ($t_2$, $t_3$)

At $t_2$, the voltage across $L_m$ reaches $-nV_o$ and mode III begins. From $t_2$ to $t_3$, current flowing through $S_1$ & $S_4$ forces secondary diodes $D_2$ & $D_3$ to conduct. The voltage across the primary side of transformer and $L_m$ is $-nV_o$. Thus, $i_{Lm}$ decreases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}+nV_o$. $L_r$ resonates with $C_r$.

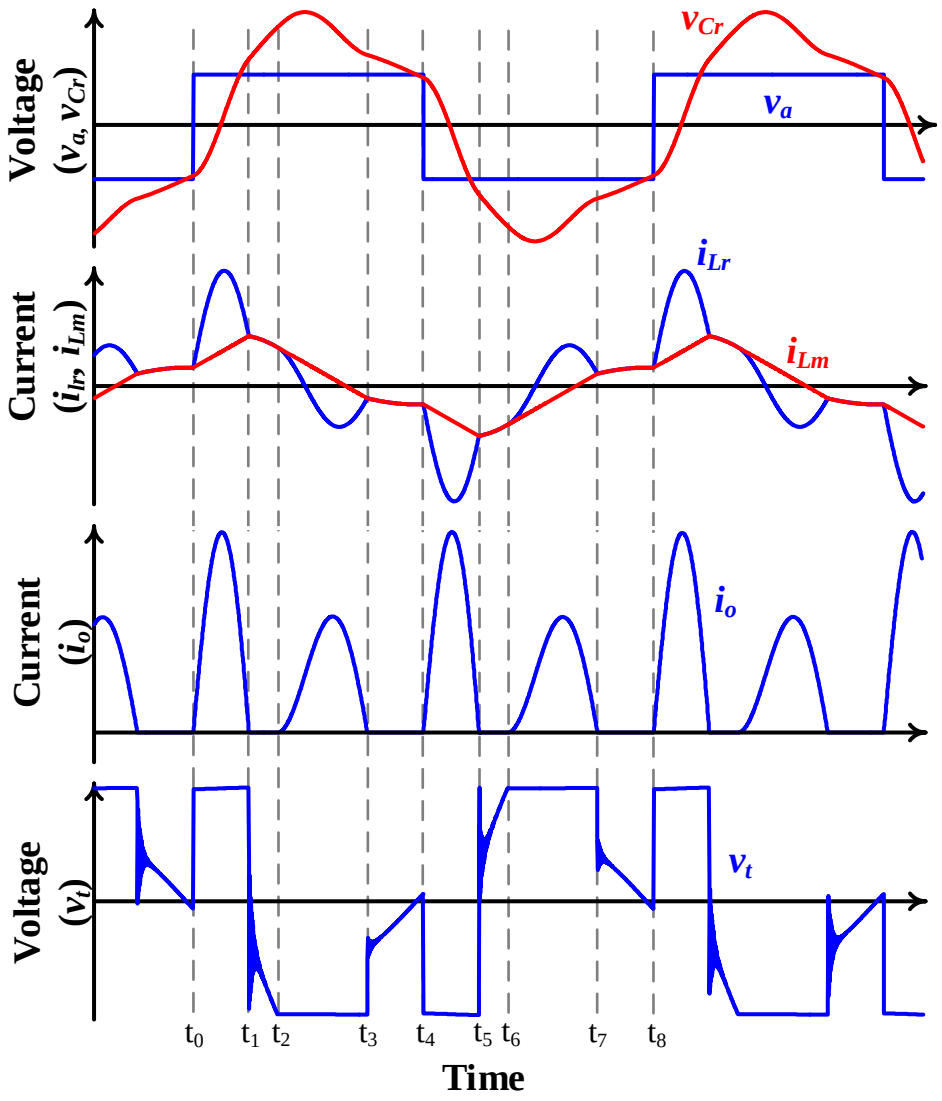



Fig. 4.13. Simulated waveforms of LLC resonant converter with $f_s/2 < f < f_s$.

At this mode, in the resonance, $i_{Lr}$ crosses zero somewhere in between $t_2$ and $t_3$. At this moment, $S_1$ & $S_4$ are turned off at zero current and the body diode $D_{S1}$ & $D_{S4}$ begins to conduct.

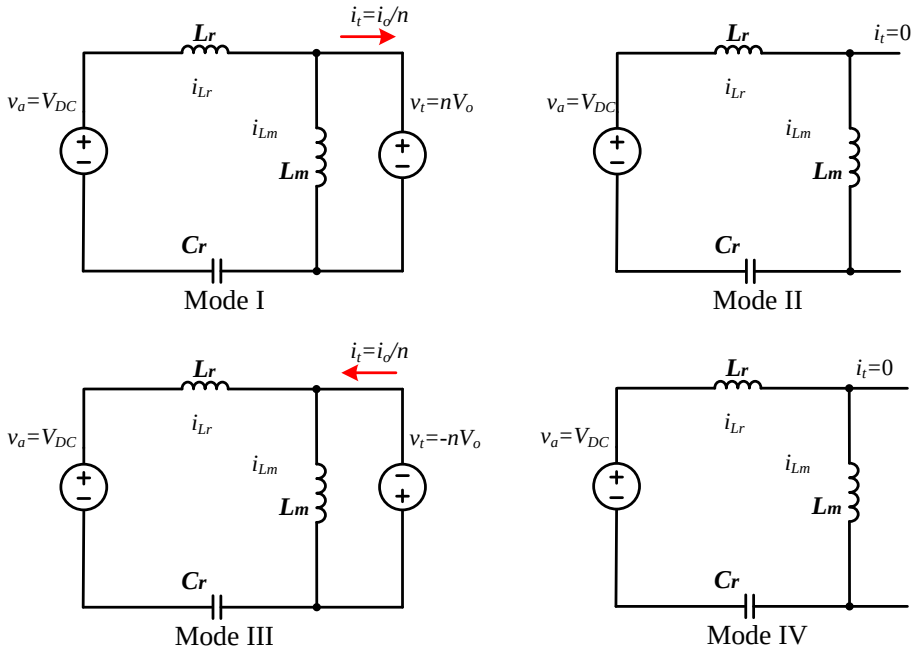



Fig. 4.14. Operating modes of LLC resonant converter with $f_s/2 < f < f_s$.

Mode IV ($t_3$, $t_4$)

At $t_3$, $i_{Lm}$ reaches $i_{Lr}$ again and mode IV begins. Diode $D_1$ & $D_4$ are turned off at zero current without small d$i$/d$t$.

From $t_3$ to $t_4$, the sum of voltages applied across $L_r$, $L_m$ and $C_r$ equals to $V_{DC}$. $L_m$ participates in the resonance with $L_r$ and $C_r$.

At $t_4$, body diodes $D_{S2}$ & $D_{S3}$ are turned off at a finite current and a finite voltage. Mode IV ends at this moment. $i_{Lm}$ is equal to $i_{L;}$ $i_{Lr}$ is negative and flows through $S_2$ & $S_3$. Switch $S_2$ & $S_3$ are turned on at a finite current and at a finite voltage. Both the turn-off of $D_{S2}$ & $D_{S3}$ and the turn-on of $S_2$ & $S_3$ result in turn-on switching losses.

For the next half cycle, the operations are symmetrical to modes I-IV.

According to the operation modes analysis, the body diodes are turned on and the switches are turned off with soft switching (both zero voltage and zero current). Secondary diodes are also turned on and off at zero current. However, the turn-off of body diodes and the turn-on of switches are both hard switching.

### 4.4.3 Operation Analysis with $f_s < f < f_p$ ($f$ close to $f_s$)

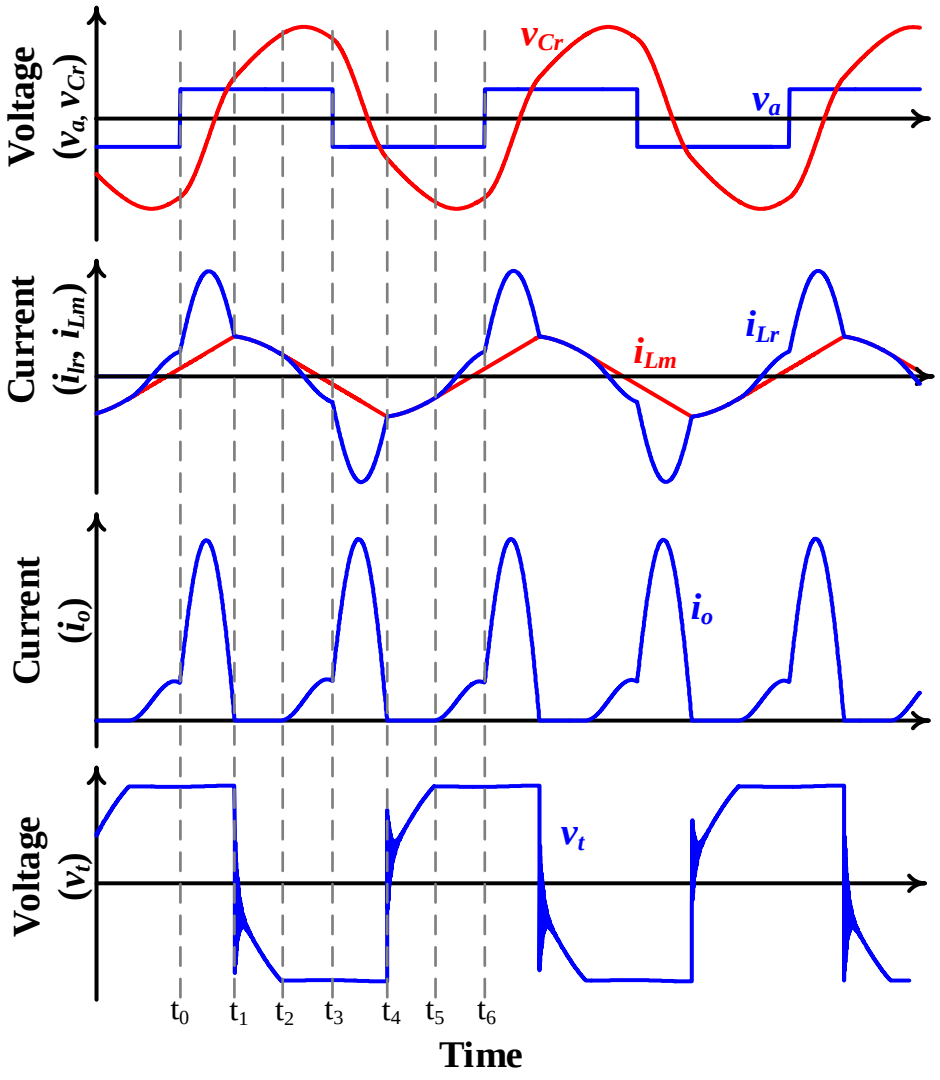



Fig. 4.15. Simulated waveforms of LLC resonant converter with $f_s < f < f_p$ ($f$ close to

$f_s$).

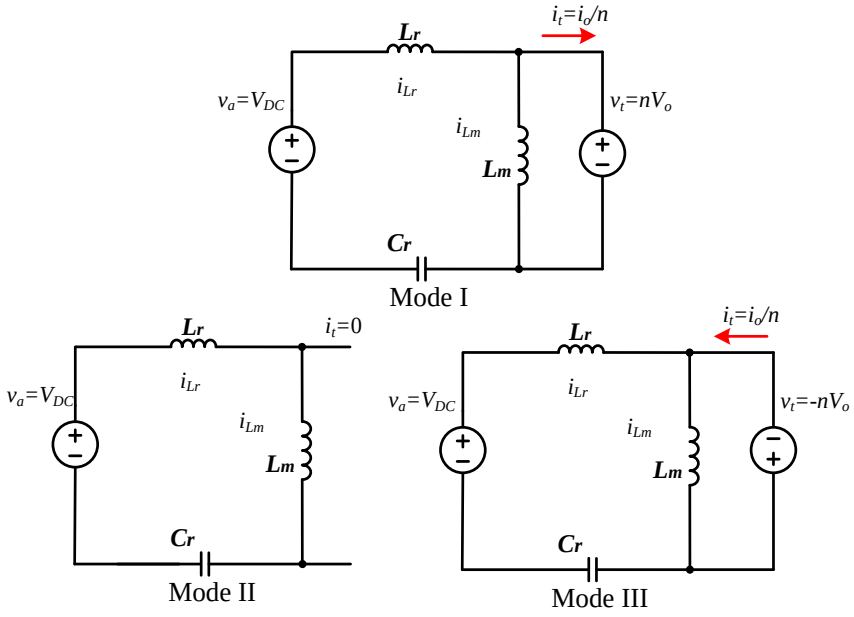



Fig. 4.16. Operating modes of LLC resonant converter with $f_s < f < f_p$ ($f$ close to $f_s$).

With the switching frequency between $f_s$ and $f_p$, if $f$ is sufficiently close to $f_s$, the same group of waveforms is plotted in Fig. 4.15. The operation of half switching cycle can be divided into three modes. Fig. 4.16 shows those three operating modes.

Mode I ($t_o$, $t_1$)

At $t_0$, body diodes $D_{S2}$ & $D_{S3}$ are turned off at a finite current and a finite voltage. Mode I begins at this moment. Switches $S_1$ & $S_4$ turn on at a finite current and at a finite voltage. Both the turn-off of $D_{S2}$ & $D_{S3}$ and the turn-on of $S_1$ & $S_4$ result in switching losses.

From $t_o$ to $t_1$, current flowing through $S_1$ & $S_4$ forces secondary diodes $D_1$ & $D_4$ to conduct. The voltage across the primary side of transformer and $L_m$ is $nV_o$.

Thus, $i_{Lm}$ increases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}$-$nV_o$. $L_r$ resonates with $C_r$.

Mode II ($t_1$, $t_2$)

At $t_1$, $i_{Lm}$ reaches $i_{Lr}$ and mode II begins. Diodes $D_1$ & $D_4$ are turned off at zero current without small d$i$/d$t$.

From $t_1$ to $t_2$, the sum of voltages applied across $L_r$, $L_m$ and $C_r$ equals to $V_{DC}$. $L_m$ participates in the resonance with $L_r$ and $C_r$.

Mode III ($t_2$, $t_3$)

At $t_2$, the voltage across $L_m$ reaches -$nV_o$ and mode III begins. From $t_2$ to $t_3$, current flowing through $S_1$ & $S_4$ forces secondary diode $D_2$ & $D_3$ to conduct. The voltage across the primary side of transformer and $L_m$ is -$nV_o$. Thus, $I_{Lm}$ decreases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}$+$nV_o$. $L_r$ resonates with $C_r$.

At this mode, in the resonance, $i_{Lr}$ crosses zero somewhere in between $t_2$ and $t_3$. At this moment, $S_1$ & $S_4$ are turned off at zero current and the body diode $D_{S1}$ & $D_{S4}$ begin to conduct.

At $t_3$, body diodes $D_{S1}$ & $D_{S4}$ are turned off at a finite current and a finite voltage. Mode III ends at this moment. $i_{Lr}$ is negative and flows through $S_2$ & $S_3$. Switches $S_2$ & $S_3$ turn on at a finite current and at a finite voltage. Both the turn-off of $D_{S1}$ & $D_{S4}$ and the turn-on of $S_2$ & $S_3$ result in turn-on switching losses.

For the next half cycle, the operations are symmetrical to modes I-III.

According to the operation modes analysis, the turn-off of switches are soft switching. Secondary diodes are turned off at zero current. However, the turn-off of body diodes and the turn-on of switches are both hard switching.

### 4.4.4 Operation Analysis with $f_s < f < f_p$ ($f$ close to $f_p$)

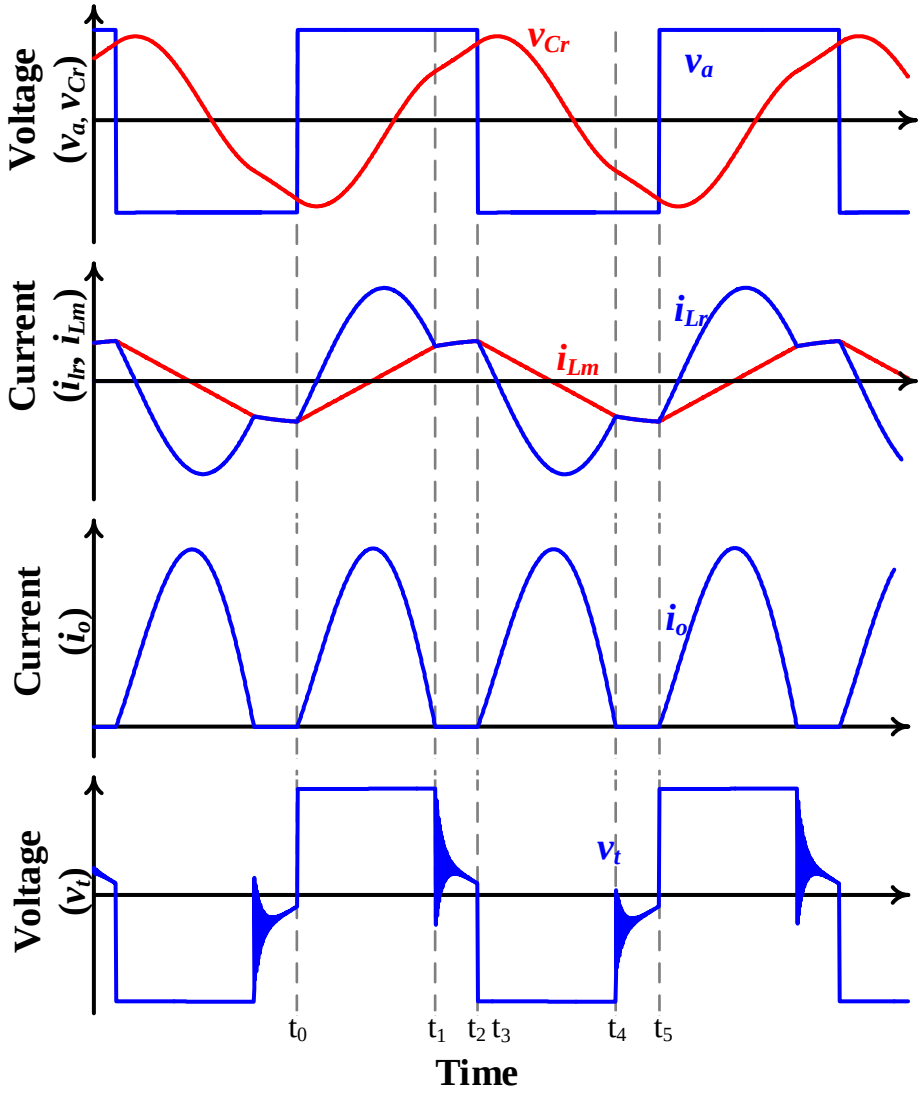



Fig. 4.17. Simulated waveforms of LLC resonant converter $f_s < f < f_p$ ($f$ close to $f_p$).

With the switching frequency between $f_s$ and $f_p$, if $f$ is sufficiently close to $f_p$, the same group of waveforms is plotted in Fig. 4.17. The operation of half switching cycle can be divided into two modes. Fig. 4.18 shows those two operating modes.

Mode I ($t_o$, $t_1$)

At $t_0$, switches $S_2$ & $S_3$ are turned off at a finite current and a finite voltage. Mode I begins at this moment. Body diodes $D_{S1}$ and $D_{S4}$ turn on. The turn-off of $S_2$ & $S_3$ results in switching losses.

From $t_o$ to $t_1$, current flowing through $S_1$ & $S_4$ forces secondary diode $D_1$ & $D_4$ to conduct. The voltage across the primary side of transformer and $L_m$ is $nV_o$. Thus, $i_{Lm}$ increases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}$-$nV_o$. $L_r$ resonates with $C_r$.

At this mode, in the resonance, $i_{Lr}$ crosses zero somewhere in between $t_0$ and $t_1$. At this moment, the body diodes $D_{S1}$ & $D_{S4}$ are turned off and the switches $S_1$ & $S_4$ begin to conduct at zero voltage.

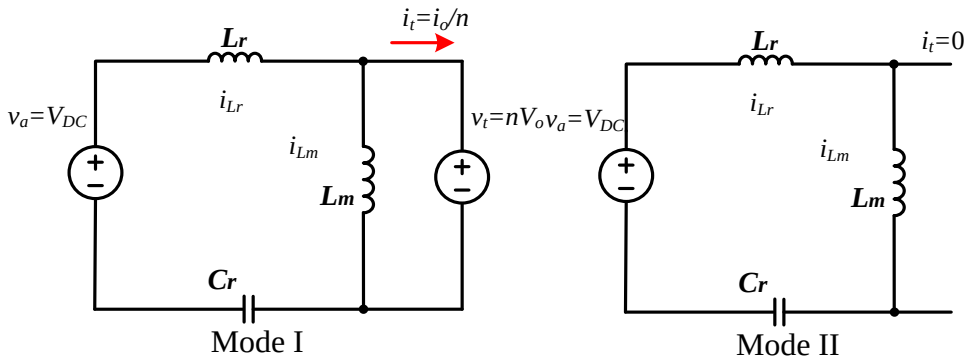



Fig. 4.18. Operating modes of LLC resonant converter $f_s < f < f_p$ ($f$ close to $f_p$).

Mode II ($t_1$, $t_2$)

At $t_1$, $i_{Lm}$ reaches $i_{Lr}$ and mode II begins. Diodes $D_1$ and $D_4$ are turned off at zero current with small d$i$/d$t$.

From $t_1$ to $t_2$, the sum of voltages applied across $L_r$, $L_m$ and $C_r$ equals to $V_{DC}$. $L_m$ participates in the resonance with $L_r$ and $C_r$.

At $t_2$, switches $S_1$ & $S_4$ are turned off at a finite current and a finite voltage. Mode II ends at this moment. $i_{Lr}$ is positive and flows through body diode $D_{S2}$ & $D_{S3}$. The turn-off of $S_1$ & $S_4$ result in switching losses.

For the next half cycle, the operations are symmetrical to modes I-II.

According to the operation modes analysis, the turn-on of switches and the turn-off of body diodes are both soft switching. Secondary diodes are turned off at zero current. However, the turn-off of switches is hard switching.

### 4.4.5 Operation Analysis with $f > f_p$

With the switching frequency larger than $f_p$, the group of waveforms are plotted in Fig. 4.19. The operation of half switching cycle can be divided into two modes. Fig. 4.20 shows those two operating modes.

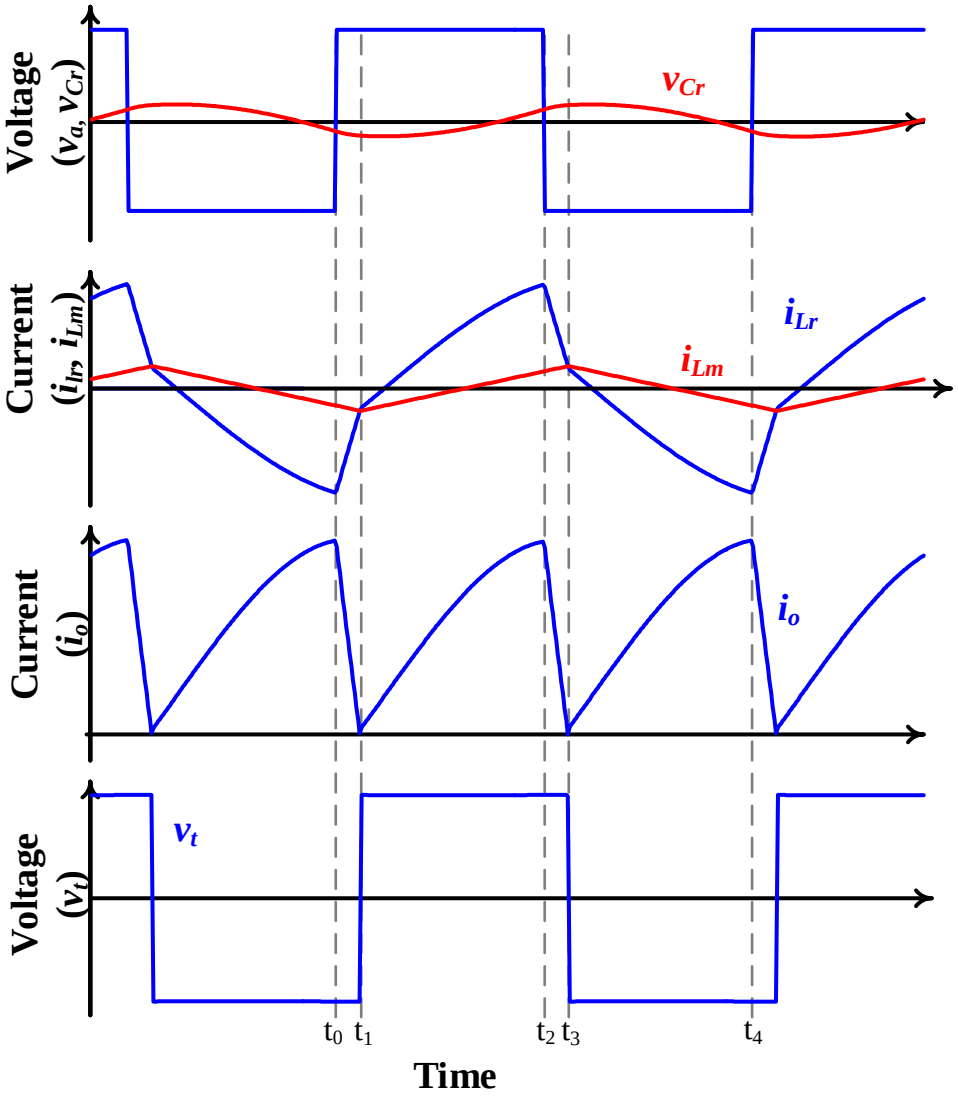



Fig. 4.19. Simulated waveforms of LLC resonant converter with $f > f_p$.

Mode I ($t_o$, $t_1$)

At $t_0$, switches $S_2$ and $S_3$ are turned off at a finite current and a finite voltage. Mode I begins at this moment. Body diodes $D_{S1}$ and $D_{S4}$ turn on. The turn-off of $S_2$ and $S_3$ result in switching losses.

From $t_o$ to $t_1$, current flowing through $S_1$ & $S_4$ forces secondary diode $D_2$ & $D_3$ to conduct. The voltage across the primary side of transformer and $L_m$ is $-nV_o$. Thus,

$i_{Lm}$ decreases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}+nV_o$. $L_r$ resonates with $C_r$. Secondary diodes $S_2$ & $S_3$ are turned off with large d$i$/d$t$. Turn off of $S_2$ & $S_3$ results in reverse recovery losses.

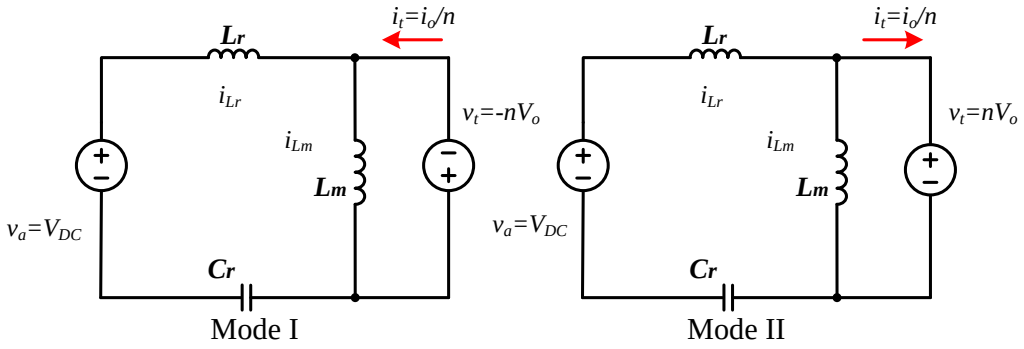



Fig. 4.20. Operating modes of LLC resonant converter with $f > f_p$.

Mode II ($t_1$, $t_2$)

At $t_1$, $i_{Lm}$ reaches $i_{Lr}$ and mode II begins. From $t_1$ to $t_2$, current flowing through $S_1$ & $S_4$ forces secondary diodes $D_1$ & $D_4$ to conduct. The voltage across the primary side of transformer and $L_m$ is $nV_o$. Thus, $I_{Lm}$ increases linearly. The sum of voltages applied across $L_r$ and $C_r$ equals to $V_{DC}$-$nV_o$. $L_r$ resonates with $C_r$.

$L_m$ does not participate in the resonance with $L_r$ and $C_r$.

At $t_2$, switches $S_1$ & $S_4$ are turned off at a finite current and a finite voltage. Mode II ends at this moment. $i_{Lr}$ is positive and flows through body diode $D_{S2}$ & $D_{S3}$. The turn-off of $S_1$ & $S_4$ results in switching losses.

For the next half cycle, the operations are symmetrical to modes I-II.

According to the operation modes analysis, the turn-on of switches and the

turn-off of body diodes are both soft switching (ZVS). Secondary diodes are also turned off at large d*i*/d*t*. The turn-off of switches and the turn-off of secondary diodes are both hard switching and result in switching losses.

### 4.4.6 Summary of Switching Conditions

Based on pervious analyses, the switching conditions of LLC converter are summarized in Table 4-1.

Table 4-1 Switching conditions of LLC converter

| Frequency Range | Additional Condition | Hard switching | | Soft switching (ZCS &ZVS) | |
|---|---|---|---|---|---|
| | | Turn on | Turn off | Turn on | Turn off |
| $f < f_s/2$ | $i_{Lr}(t_o) > 0$ | $S_1$-$S_4$ | $D_{S1}$-$D_{S4}$ | | $S_1$-$S_4$, $D_{S1}$-$D_{S4}$ |
| $f_s/2 < f < f_s$ | N/A | $S_1$-$S_4$ | $D_{S1}$-$D_{S4}$ | | $S_1$-$S_4$, $D_{S1}$-$D_{S4}$ |
| $f_s < f < f_p$ | $f$ near $f_s$ | $S_1$-$S_4$ | $D_{S1}$-$D_{S4}$ | | $S_1$-$S_4$, $D_1$-$D_4$ |
| | $f$ near $f_p$ | None | $S_1$-$S_4$ | $S_1$-$S_4$ | $D_{S1}$-$D_{S4}$, $D_1$-$D_4$ |
| $f > f_p$ | N/A | None | $S_{1\text{-}4}$, $D_1$-$D_4$ | $S_1$-$S_4$ | $D_{S1}$-$D_{S4}$ |

For the regions of (a) $f < f_s/2$, with $i_{Lr}(t_o) > 0$, (b) $f_s/2 < f < f_s$, and (c) $f_s < f < f_p$ with $f$ close to $f_s$, the freewheeling diodes (body diodes) are turned off at a finite current and finite voltage. In those cases, the freewheeling diodes must have good reverse-recovery characteristics to avoid large reverse spikes flowing through the switches, and to minimize the diode turn-off losses. It is possible to use thyrisors as switches in low-switching frequency applications.

For the regions of (d) $f_s < f < f_p$ with $f$ close to $f_p$, and (e) $f > f_p$, the freewheeling diodes (body diodes) are turned off at a zero current and at zero voltage. Thus, the freewheeling diodes do not need to have very fast reverse-recovery characteristics. In those cases, it is possible to use MOSFETs as switches in high-switching frequency applications.

In conclusion, if MOSFETs are used as the primary switches, it is preferable that LLC converter operates in the regions (d) $f_s < f < f_p$ with $f$ close to $f_p$, and (e) $f > f_p$.

### 4.4.7 Modeling with First Harmonic Approximation

In Fig. 4.21, the full bridge LLC multi-resonant converter is divided into three stages. In the first stage, the dc voltage source and four complimentary switches operate as a square wave generator. The second stage is a series LLC resonant network. The third stage consists of the $n$:1 transformer, rectifier and a resistive load. The load resistance is equal to the load voltage divided by load current.

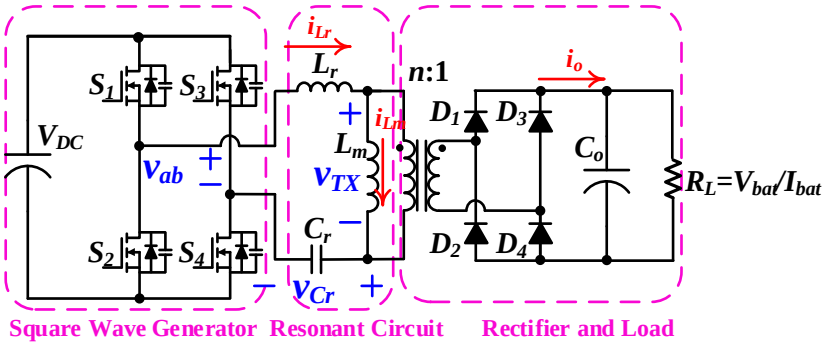



Fig. 4.21. Three stage configuration of full bridge LLC resonant converter.

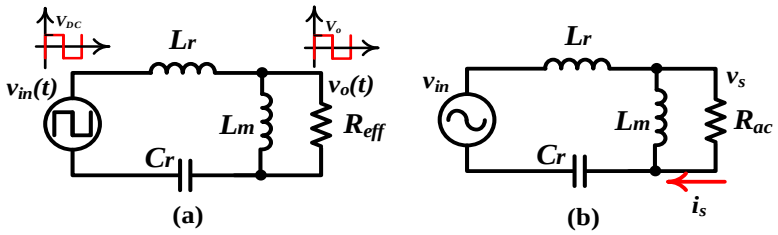



Fig. 4.22. (a) Simplified full bridge LLC converter circuit. (b) Circuit model under first harmonic approximation (FHA).

The resistive load in the secondary side of the transformer can be expressed as an effective resistor in the primary side [see Fig. 4.22 (a)]. To simplify the analysis, the leakage flux and parasitic effect in the secondary side of the transformer are ignored. For simplicity in the analysis, first harmonic approximation (FHA) method, in which only the first harmonic is allowed to pass the resonant network, is utilized [46].

On the input side, using Fourier series, the fundamental frequency component of the input square wave voltage is,

$$v_{in,1}(t) = \frac{4}{\pi} V_{DC} \sin(2\pi f_s t) \tag{4.25}$$

where $f_s$ is the switching frequency of the switches and also the frequency of the square wave. Its rms value is,

$$V_{in,1} = \frac{2\sqrt{2}}{\pi} V_{DC} \tag{4.26}$$

On the output side, $v_s$ is approximated as a square wave, the fundamental frequency component of the output square wave voltage is,

$$v_{s,1}(t) = \frac{4}{\pi} n V_o \sin(2\pi f_s - \varphi_v) \tag{4.27}$$

where, $\varphi_v$ is the phase angle of the fundamental frequency component of output voltage. Its rms value is,

$$V_{s,1} = \frac{2\sqrt{2}}{\pi} n V_o \tag{4.28}$$

Similarly, on the output side, $i_s$ is approximated as a square wave, the fundamental frequency component of output square wave current is,

$$i_{s,1} = \frac{2}{\pi}\frac{1}{n} I_o \sin(2\pi f_s t - \varphi_i) \tag{4.29}$$

where $\varphi_i$ is the phase angle of the fundamental frequency component of output current. Its rms value is,

$$I_{s,1} = \frac{\pi}{2\sqrt{2}}\frac{1}{n} I_o \tag{4.30}$$

Thus, using FHA, the ac equivalent load resistance, $R_{ac}$, is calculated as,

$$R_{ac} = \frac{V_{s,1}}{I_{s,1}} = \frac{8n^2}{\pi^2}\frac{V_o}{I_o} = \frac{8n^2}{\pi^2} R_L \tag{4.31}$$

Fig. 4.22(b) shows the model of the circuit under FHA.

### 4.4.8 Steady State Operating Characteristics

According to the circuit model in Fig. 3.9(b), the voltage gain *G*, transconductance *g*, and input impedance $Z_{in}$, could be calculated, as demonstrated in equations (4.32-4.34).

$$G = \left|\frac{v_s}{v_{in}}\right| = \left|\frac{j\omega L_m \| R_{ac}}{j\omega L_m \| R_{ac} + j\omega L_r + 1/j\omega C_r}\right| \tag{4.32}$$

$$g = \left|\frac{i_s}{v_{in}}\right| = \frac{1}{R_{ac}}\left|\frac{v_s}{v_{in}}\right| = \frac{1}{R_{ac}}\left|\frac{j\omega L_m \| R_{ac}}{j\omega L_m \| R_{ac} + j\omega L_r + 1/j\omega C_r}\right| \tag{4.33}$$

$$Z_{in} = j\omega L_m \| R_{ac} + j\omega L_r + 1/j\omega C_r \tag{4.34}$$

To illustrate differ load conditions, quality factor *Q* is introduced. *Q* is defined to be the ratio between characteristic impedance ($\sqrt{L_r/C_r}$) and the load resistance $R_{ac}$.

$$Q = \frac{\sqrt{L_r / C_r}}{R_{ac}} \tag{4.35}$$

Large *Q* corresponds to small load resistance and heavy load condition. On the contrary, small *Q* corresponds to large load resistance and light load condition.

Fig. 4.23 shows voltage gain *G*, transconductance g, and phase of input impedance versus $f_s$ for different values of quality factor *Q*. As seen from Fig. 4.23 (a), the peak voltage occurs somewhere between $f_s$ and $f_p$. From no load condition ($Q = 0$) to short circuit condition ($Q = \infty$), the peak voltage frequency shifts from $f_s$ to $f_p$. At $f_p$, the converter behaves like a constant voltage source.

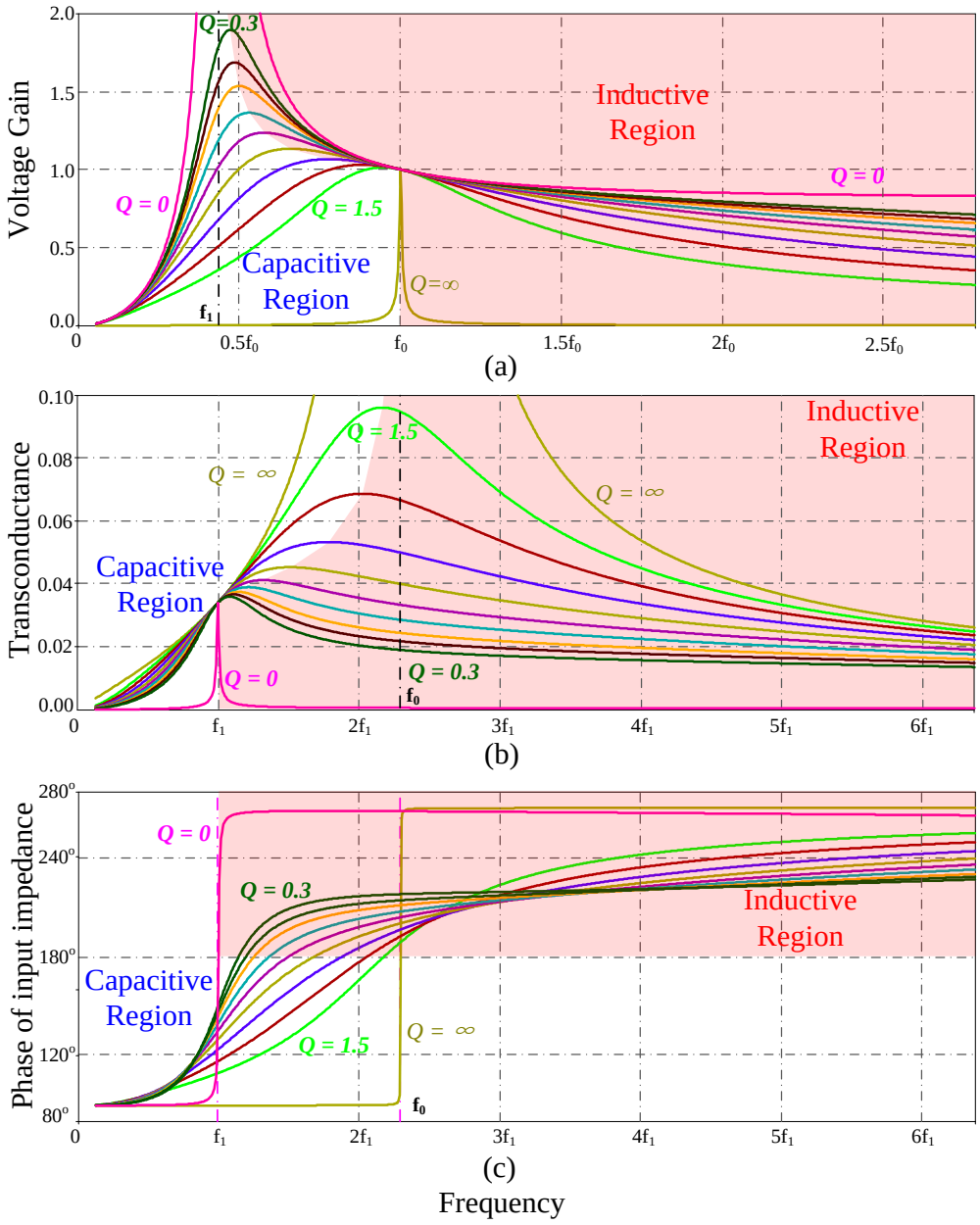



Fig. 4.23. Frequency characteristics of LLC resonant converter. (a) Voltage gain. (b) Transconductance. (c) Phase of input impedance.

From Fig. 4.23 (b), the peak current occurs somewhere between $f_s$ and $f_p$. From short circuit condition ($Q = \infty$) to no load condition ($Q = 0$), the peak current frequency shifts from $f_p$ to $f_s$. At $f_s$, the converter behaves like a constant current source.

The input impedance determines the nature (inductive or capacitive) of the resonant network. When the phase of input impedance is larger than $180^o$, the converter is inductive. When the phase of input impedance is smaller than $180^o$, the converter is capacitive. The boundary between capacitive and inductive regions is the $180^o$ phase line. From Fig. 4.23(c), the boundary operating frequencies occurs somewhere between $f_s$ and $f_p$. From short circuit condition ($Q = \infty$) to no load condition ($Q = 0$), the boundary operating frequency shifts from $f_p$ to $f_s$.

In an inductive load, the voltage lags the current, which creates a soft switch condition for the turn-off of freewheeling diodes ($D_{S1\text{-}S4}$). According to the discussion in Section 4.4.6, MOSFETs could be used as the primary switches in the inductive region.

In a capacitive load, the voltage leads the current, which creates a hard switch condition for the turn-off of freewheeling diodes ($D_{S3}$ and $D_{S4}$). According to the discussion in Section 4.4.6, MOSFETs is no longer suitable in this region. It is possible to use thyristors as switches in low switching frequency applications.

According to Fig. 4.23, when the switching frequency is higher than $f_p$, the resonant network is inductive. When the switching frequency is lower than $f_s$, the resonant network is capacitive. In between $f_s$ and $f_p$, inductive or capacitive is determined by the load condition. The analysis is consistent with the switching conditions summarized in Section 4.4.6.

## 4.5 *Designing a 1 kW PEV Charger Prototype*

In this section, the design considerations for an interleaved boost and LLC based PEV charger rated at 1 kW is presented. It is aimed to charge a Li-ion battery with 360 V nominal voltage from depleted (320 V) to fully charged (420 V) conditions. The charging process is divided into constant current (CC) and constant voltage charging (CV) stages [88].

### 4.5.1 Charging Profile of 1 kW Li-ion Battery

Fig. 4.24 provides the 1 kW charging characteristics of a 360 V battery pack. According to Fig. 4.24, there are four key points in the charging process. Begin point and end point correspond to the beginning and end of the charging process, respectively. Parameters of those four key points are summarized in Table 4-2.

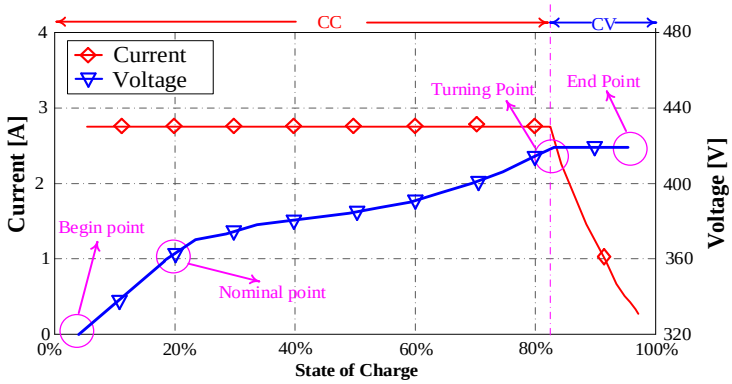



Fig. 4.24. Charging profile of a 360 V Li-ion battery pack rated at 1 kW.

Table 4-2 Key points in the charging profile of the PEV battery pack

| Parameter | Begin Point | Nominal point | Turning point | End point |
|---|---|---|---|---|
| $V_{bat}$ | 320V | 360V | 420V | 420V |
| $I_{bat}$ | 2.38A | 2.38A | 2.38A | 0.24A |
| $P$ | 762 W | 857 W | 1000 W | 100 W |
| $R_L$ | 134.5Ω | 151.3Ω | 176.5Ω | 1750 Ω |

The following section outlines charger design to ensure meeting battery charging requirements on these four critical operating points.

### 4.5.2 Interleaved Boost PFC Converter Design

In PFC boost converter, the instantaneous duty cycle $d$ varies with the input voltage as,

$$d(\theta) = 1 - \frac{|V_{in}|}{V_{DC}} = 1 - \frac{155.5|\sin\theta|}{V_{DC}} \tag{4.36}$$

where 155.5 V is the peak input voltage, and $\theta$ is the phase angle between the input voltage and current. The inductor current ripple can be expressed as,

$$\Delta I_L = \frac{|V_{in}|}{L} d(\theta) T_s = \frac{155.5 T_s}{L}\left(|\sin\theta| - \frac{155.5}{V_{DC}}(\sin\theta)^2\right) \tag{4.37}$$

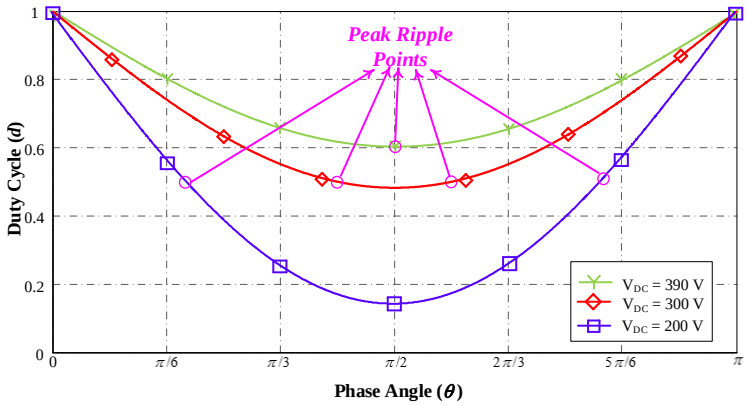



Fig. 4.25. Duty cycles corresponding to 390 V, 300 V, and 200 V dc link voltages.

Assume $x = |\sin\theta|$, then $0 \le x \le 1$. The derivative of $\Delta I_L$ is calculated as Eq. (4.38)

$$\frac{\delta \Delta I_L}{\delta x} = \frac{155.5 T_s}{L}\left(1 - \frac{311}{V_{DC}} x\right) \tag{4.38}$$

According to Eq. (4.38), if $V_{DC} \leq 311$ V, the peak ripple happens when $x = V_{DC}/311$. Substituting $x$ into Eq. (4.36), $d$ is calculated as 0.5. If $V_{DC} > 311$ V, the peak ripple happens when $x = 1$ and $\theta = \pi/2$. Based on the previous analysis, duty cycle close to 50% provides the best inductor current ripple cancellation, as well as rms capacitor current cancellation.

Conventionally, the dc link voltage of grid connected front end ac/dc converter, $V_{DC}$, has the typical value to be 390 V [89]. However, in this work, $V_{DC}$ is designed to be 300 V. This is because $V_{DC} = 300$ V has overall duty cycles closer to 0.5 and better ripple cancellation effect, which could be clearly observed in Fig. 4.25.

The circuit is designed to operate at 100 kHz switching frequency taking the tradeoff between the sizes of the inductors and dc link filter capacitor and switching losses into account. The inductor ripple current at the peak of line ($\theta = \pi/2$) is designed to be 30% of the inductor current.

$$\Delta I_{L\max} = \sqrt{2} I_{Lrms} \times 0.3 = \sqrt{2} \frac{P_{\max}}{2V_{in,rms}} \times 0.3 \tag{4.39}$$

According to equations (4.37) and (4.39), inductances could be calculated as:

$$L_1 = L_2 = \frac{T_s V_{in,rms} \times \sqrt{2}}{\Delta I_{L\max}} d(\theta = \frac{\pi}{2}) \tag{4.40}$$

The ripple voltage at the dc link capacitor is set to be 5% of the dc link voltage, which is 15 V. Based on this ripple voltage, the dc link capacitance could be calculated,

$$C_{DC} = \frac{2P_{\max}}{2\pi V_{DC} V_{ripple} 2 f_{line}} \tag{4.41}$$

## 4.6 *Full-Bridge Series LLC Converter Design*

$f_p$ and $f_s$ are the two resonance frequencies of the LLC resonant tank. When the switching frequency, $f$, is higher than $f_p$, the resonant tank becomes inductive. When the $f$ is lower than $f_s$, the resonant tank becomes capacitive. In between $f_s$ and $f_p$, inductive or capacitive operation region is determined by the load. On the other hand, as the switching frequency is varied closer to $f_p$, the impedance of the resonant tank becomes smaller. This can reduce the circulating energy in the resonant tank, which results in reduction in the conduction losses of the LLC converter. Therefore, the LLC converter is desired to operate in the inductive region and close to $f_p$ for minimizing switching and conduction losses and maximizing efficiency.

For design considerations, $f_p$ is preset by the optimum operating frequency of the MOSFETs, considering the tradeoff between high frequency operation and switching power loss. Thus, the product of $L_r$ and $C_r$ can be determined as the initial design step. Short circuit performance ($Q = \infty$) and peak voltage gain at maximum output power ($Q = Q_{turn}$) are two important considerations in designing $L_r$ and $C_r$. When the short circuit happens, the power management module shifts the switching frequency to a higher value ($2 \sim 3f_p$) to increase the impedance of the resonant tank, hence, the short circuit current could be effectively reduced and limited to a predetermined value. If $L_r$ is large, the resonant tank impedance becomes large as well, while the short circuit current becomes smaller. However, for a constant $f_p$, a larger $L_r$ would result in a smaller $C_r$, which increases the voltage stress of the

resonant capacitor as well as the quality factor. Increase of quality factor reduces the peak voltage gain. This might cause potential failure to fulfill the voltage gain specification at heavy load condition. The values of $L_r$ and $C_r$ are determined based on this tradeoff.

The design of $L_m$ is based on the tradeoff between conduction losses and switching losses. Smaller $L_m$ corresponds to smaller operation frequency range, which provides lower conduction losses. However, if $L_m$ decreases, the switch turning off current increases, which in turn would result in higher switching losses. The value of $L_m$ is determined from this tradeoff.

Based on those two design tradeoffs, the dc/dc stage parameters can be designed.

1) Selection of the turns ratio of transformer

The transformer turns ratio is determined by the ratio between dc link voltage and the nominal voltage of the battery pack,

$$n = \frac{V_{DC}}{V_{nom} + 2V_d} \tag{4.42}$$

where $V_d$ is the voltage drop across the secondary side diode.

2) Selection of $L_r$ and $C_r$

The primary resonance frequency was determined as $f_p$ = 200 kHz. According to Eq. (4.12), the product of $L_r$ and $C_r$ can be found as,

$$\sqrt{L_r C_r} = 1/(2\pi f_p) \tag{4.43}$$

As aforementioned, there is a tradeoff between the peak voltage gain at heavy load and the short circuit current. In this case, the peak voltage gain at the turning point is the heaviest load condition in CV charging mode. The voltage gain must be larger than 420/360 = 1.17. The short circuit current should be smaller than the maximum current of the charger (2.38 A). Based on this tradeoff, the optimal quality factor at the turning point $Q_{turn}$ is tuned to be 0.94, which satisfies the peak gain voltage and short circuit current requirements. Thus, the ratio between $L_r$ and $C_r$ can be determined by Eq. (4.44).

$$\sqrt{L_r / C_r} = Q_{turn} \times \frac{8n^2}{\pi^2} \times 151.3\Omega \tag{4.44}$$

From equations (4.42) and (4.44), $L_r$ and $C_r$ are calculated as 63.4 μH, and 10 nF, respectively.

3) Selection of the magnetizing inductance $L_m$

The design of $L_m$ is based on the tradeoff between conduction and switching losses. Decreasing $L_m$ would increase the resonant tank current at the instant of turn-off as well as the switching losses. While increase in $L_m$ would reduce the impedance of $L_m$ and increase the circulating energy in $L_m$. Different values of $L_m$ are investigated through evaluating circulating energies in the resonant tank and turning-off currents. The optimal magnetizing value is determined as 160 μH.

4) DC frequency characteristics evaluation

After determining the critical parameters, the dc frequency response of designed LLC converter must be evaluated to ensure that it fulfills the design specifications and exhibits overall good performance. If the design does not fulfill the requirement, we must go back to the initial step and adjust the design procedures until the optimal design is achieved.

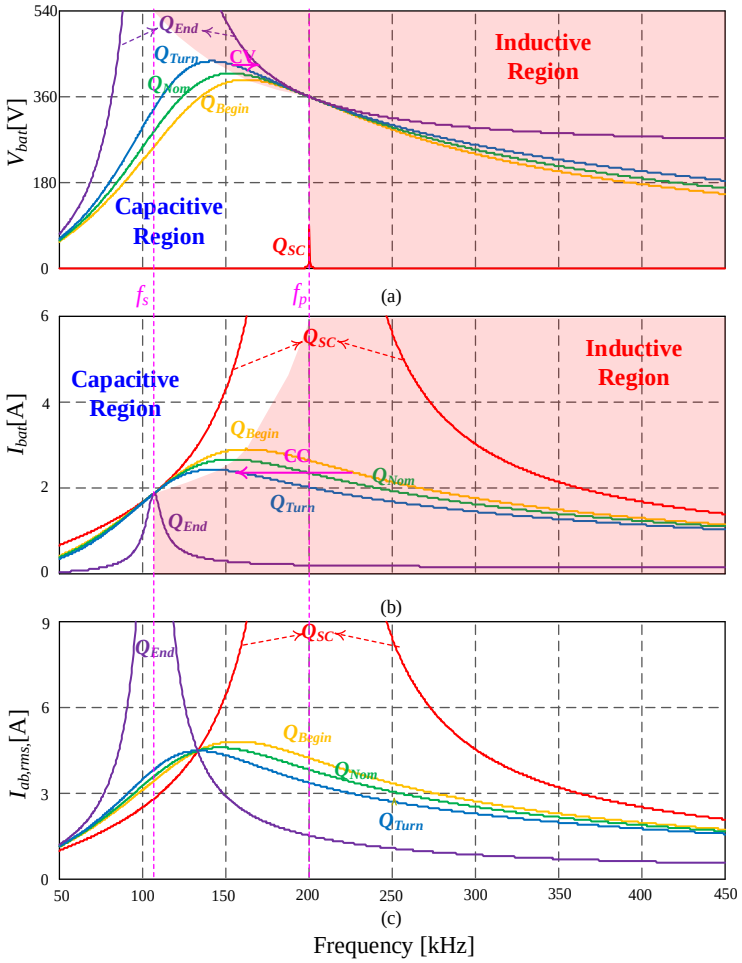



Fig. 4.26. Dc characteristics of the designed 1 kW LLC converter: a) output voltage, (b) charging current, (c) input current.

Based on equations (4.32-4.34), voltage and current curves versus wide frequency range for 1 kW charger are plotted in Fig.4.26. These parameters

correspond to begin point, nominal point, turning point, end point, and short circuit conditions.

According to Fig. 4.26 (a), in CV charging mode, the output voltage is constrained at 420 V, which is the fully charged battery pack voltage. From the turning point to the end point, the switching frequency increases from 159.1 kHz to 171.2 kHz. As seen from Fig. 4.26 (b), in CC charging mode, the charging current is limited to 2.38 A. From the begin point to the turning point, the switching frequency decreases from 225.3 kHz to 159.1 kHz. Under short circuit condition, the switching frequency needs to be boosted to higher than 330 kHz, so that the short circuit current could be constrained to be lower than the nominal current.

## *4.7 Optimization of the LLC Magnetic Components*

Due to the rigid requirements on the values of $L_m$ and $L_r$, both the transformer and the resonant inductor need to be customized.

In order to obtain the voltage and current ratings of the magnetic components, waveforms at peak power point (1 kW), which corresponds to the turning point of the charging process, are simulated, and resultant waveforms of resonant inductor current ($i_{Lr}$), resonant capacitor voltage ($v_{Cr}$), input voltage to the resonant tank ($v_{ab}$), voltage at the primary side of transformer ($v_p$), are plotted in Fig. 4.27.

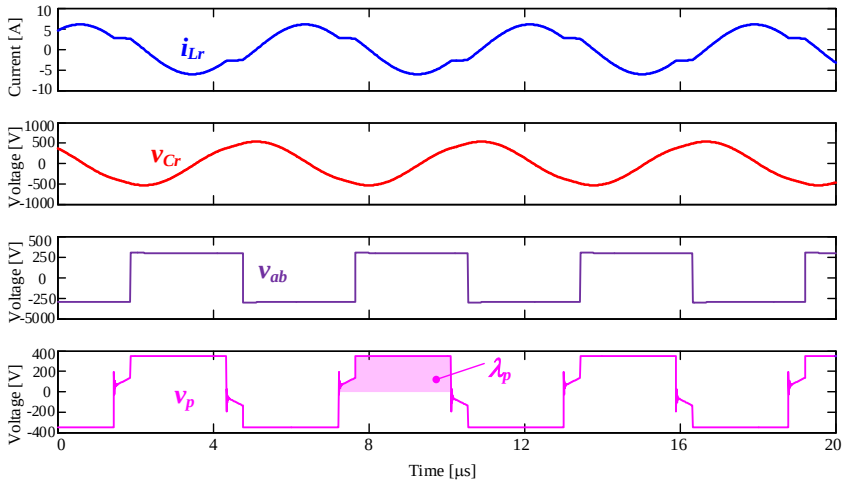



Fig. 4.27. Simulated LLC results at the turning point ($V_{bat}$=420 V, $I_{bat}$=2.38 A).

As shown in Fig. 4.27, due to the alternating current in the transformer primary side, flux in the magnetic core crosses both the first and third quadrants of the B-H loop. Peak ac flux density, $\Delta B$, is determined by the volt-second on the primary side of the transformer, $\lambda_p$, as,

$$\Delta B = \frac{\lambda_p}{2 n_p A_e} \tag{4.45}$$

where $A_e$ is the effective cross-section area of the core; $n_p$ is the number of primary turns.

Core loss, $P_{fe}$, is associated with $\Delta B$, as

$$P_{fe} = P_{cv} V_e = K_{fe} \left(\Delta B\right)^{\beta} V_e \tag{4.46}$$

where $P_{cv}$ is the core loss volume density; $K_{fe}$ is a constant of proportionality, which depends on the switching frequency; and $\beta$ is a constant depending on the material. For ferrite power material, the typical value of $\beta$ is 2.7.

The copper loss $P_{cu}$, can be calculated as,

$$P_{cu} = R_{cu} I_{tot}^2 = \frac{\rho n MLT}{A_w} I_{tot}^2 \tag{4.47}$$

where $\rho$ is the wire resistivity; $MLT$ is mean length per turn; $A_w$ is the cross-section area of the wire; and $I_{tot}$ is the total rms winding current, referred to the primary side,

$$I_{tot} = I_{p,rms} + nI_{s,rms} \tag{4.48}$$

According to equations (4.45)-(4.47), the total loss, $P_{tot}$, can be derived as a function of $\Delta B$,

$$P_{tot} = P_{fe} + P_{cu} = K_{fe} \left(\Delta B\right)^{\beta} V_e + \frac{\rho MLT}{A_w} \frac{\lambda_p}{2\Delta B A_e} I_{tot}^2 \tag{4.49}$$

According to Eq. (4.49), the derivative of $P_{tot}$ over $\Delta B_L$ could be calculated as,

$$\frac{dP_{tot}}{d\Delta B_L} = K_{fe} V_e \left(\Delta B\right)^{\beta-1} - \frac{\rho MLT}{A_w} \frac{\lambda_p}{2\left(\Delta B\right)^2 A_e} I_{rms}^2 \tag{4.50}$$

By equalizing the derivative to be zero, the optimal value of $\Delta B$, which corresponds to the minimum total loss, can be obtained. The design of the resonant inductor is based on this optimization. Design procedures are provided as below.

1) Select core material

In this application, ferrite cores, which have high saturation flux ($B_s$) and low losses at high frequencies, are preferable. PC40 ferrite core, with $B_s$ of 0.51 Tesla at room temperature, is chosen for both transformer and inductor.

2) Determine core size

According to Eq. (4.24), big core corresponds to big $A_e$ and provides sufficient margin to regulate both $\Delta B$ and core loss to a low value. Moreover, the core window must be large enough to fill the wire winding with specific gauge. However, big core causes the penalty of big core weight, and there will be little margin to tune the air gap length. Based on this consideration, ETD44 core is selected. Critical parameters of ETD44 core are detailed in Table II.

3) Select the number of turns

Based on Eq. (4.29) and Table 4-2, optimal $\Delta B$ is calculated to be 0.15 Tesla. The volt-second on the primary side of the transformer at 1 kW operation, which corresponds to the shaded area in Fig. 4.27, is calculated as,

$$\lambda_p = \int v_p dt = 1.03 \times 10^{-3} Vs \tag{4.51}$$

According to Eq. (4.45), the number of primary turns could be obtained,

$$n_p = \frac{\lambda_p}{2\Delta B A_e} = \frac{1.03 \times 10^{-3}}{2 \times 0.15 \times 1.75 \times 10^{-4}} = 19.62 \approx 20 \tag{4.52}$$

The secondary turns are found by,

$$n_s = \frac{n_p}{n} \approx 24 \tag{4.53}$$

4) Air gap length

The length of air gap $l_g$, can be calculated according to the desired inductance [37],

$$l_g = \frac{\mu_o n^2 A_e}{L} = \frac{4\pi \times 10^{-7} \times 20^2 \times 1.75 \times 10^{-4}}{160 \times 10^{-6}} = 0.55 mm \tag{4.54}$$

5) Check for saturation

$\Delta B$ equals to the maximum flux density. Since $\Delta B$ (0.14 Tesla) is designed to be much smaller than $B_{sat}$ (0.51 Tesla), saturation could be efficiently avoided in this design.

6) Evaluating the wire size

The upper limit cross section areas of primary and secondary wires, $A_{wp}$ and $A_{ws}$, can be evaluated based on Eq. (4.55),

$$A_{wp} n_p + A_{ws} n_s \le K_u A_W \tag{4.55}$$

where $A_w$ is the bobbin winding area. $K_u$ is the fill factor of the core window, and is assumed to be 0.5 in this design.

In high switching frequency operation, Litz wire must be used to reduce the skin effect and proximity effect losses. In this design, the wire gauge AWG 14 Litz cable, which is made of 250 strands AWG 38 wires, is used to wind both primary and secondary turns [90].

Practically, the leakage inductance on the primary side of the transformer must be excluded from the theoretical resonant inductance. In this design, the leakage inductance of the transformer is measured to be 0.89 μH. Thus, the inductance of the discrete inductor is calibrated as,

$$L = L_{Lr} - L_{Leak} \tag{4.56}$$

The design of inductor follows the same procedures as that of transformer.

Obtained design parameters of inductor and transformer are summarized in Table 4-3.

Table 4-3 Critical parameters of magnetic components

| Parameter | Symbol | Transformer | Resonant Inductor |
|---|---|---|---|
| Core type | N/A | ETD44 | ETD39 |
| Core material | N/A | PC47 | PC47 |
| Saturation flux (25°C) | $B_s$ | 0.51 Tesla | 0.51 Tesla |
| Vacuum permeability | $\mu_o$ | $4\pi\times10^{-7}$ | $4\pi\times10^{-7}$ |
| Inductance | $L$ | 160 μH | 62.51 μH |
| Magnetic path length | $l_m$ | 10.3 cm | 9.21 cm |
| Effective cross-section area | $A_e$ | 1.75 $cm^2$ | 1.25 $cm^2$ |
| Bobbin winding area | $A_W$ | 2.13 $cm^2$ | 1.74 $cm^2$ |
| Mean Length Path | $MLT$ | 7.62 cm | 6.86 cm |
| Effective Core Volume | $V_e$ | 18 $cm^3$ | 11.5 $cm^3$ |
| Primary turns | $n_p$ | 20 turns | 28 turns |
| Secondary turns | $n_s$ | 24 turns | N/A |
| Maximum flux | $\Delta B_{max}$ | 0.15 Tesla | 0.11 Tesla |
| Air gap length | $lg$ | 0.55 mm | 1.8 mm |
| Litz wire gauge | AWG | 14 | 14 |

## *4.8 Loss Analysis of the Full-Bridge LLC Converter*

### 4.8.1 Conduction Losses

The apparent power ($S$) from the dc link could be found from Eq. (4.57),

$$S = V_{DC} I_{in,rms} \tag{4.57}$$

The real power ($P$) delivered to the battery pack is,

$$P = V_{bat} I_{bat} \tag{4.58}$$

The reactive power ($Q_r$), which corresponds to the circulating power in the resonant tank, can be calculated as,

$$Q_r = \sqrt{S^2 - P^2} = \sqrt{(V_{DC} I_{in,rms})^2 - (V_{bat} I_{bat})^2} \tag{4.59}$$

According to Eq. (4.59) and the data extracted from Fig. 4.27, the reactive power corresponds to any specific point of the charging process can be calculated.

The reactive power is the figure of merit to evaluate the conduction losses in the circuit, since conduction losses are proportional to the reactive power as it circulates in the circuit.

For this specific design, the reactive powers at beginning point, nominal point, turning point, and end point are 726 VA, 693 VA, 602 VA, and 570 VA, respectively. The reactive power provides an intuitive insight to the level of conduction losses. Accurate conduction losses could be approximated based on rms current, equivalent series resistances (ESRs) of circuit components, as well as diode forward voltage drop.

### 4.8.2 Switching Losses

Since the converter operates in inductive region, both the turning-on of MOSFETs and turning-off of free-wheeling diodes are ZVS and lossless. Besides, losses associated with the turn-on process of power diodes are negligible. Moreover, diodes for rectification in the secondary side are turned on and off at zero current, hence, do not impose any additional switching losses. Consequently, turning-off losses of MOSFETs dominate the switching losses of LLC converter. The associated switching losses of each single MOSFET can be approximated based on Eq. (4.60).

$$P_{switch} \approx \frac{1}{4} I_{off} V_{DS} t_{overlap} f \tag{4.60}$$

where, $I_{off}$ is the turning-off current; $V_{DS}$ is the drain-source voltage when the switch is completely off; $t_{overlap}$ is the overlap time between $I_{DS}$ *and* $V_{DS}$ during the turning-off; and $f$ is the switching frequency.

### 4.8.3 Core Losses

Core loss volume density ($P_{CV}$) is the function of both the switching frequency and the peak ac flux density ($\Delta B$). The curves of $P_{CV}$ for PC47 ferrite are plotted in Fig. 3.28. Using Eq. (4.45), $\Delta B$ can be calculated. Likewise, the switching frequencies at different operation points can be obtained from the dc characteristics of the LLC converter. Consequently, core losses can be calculated as,

$$P_{switch} \approx \frac{1}{4} I_{off} V_{DS} t_{overlap} f \tag{4.61}$$

where, $V_e$ is the effective core volume.

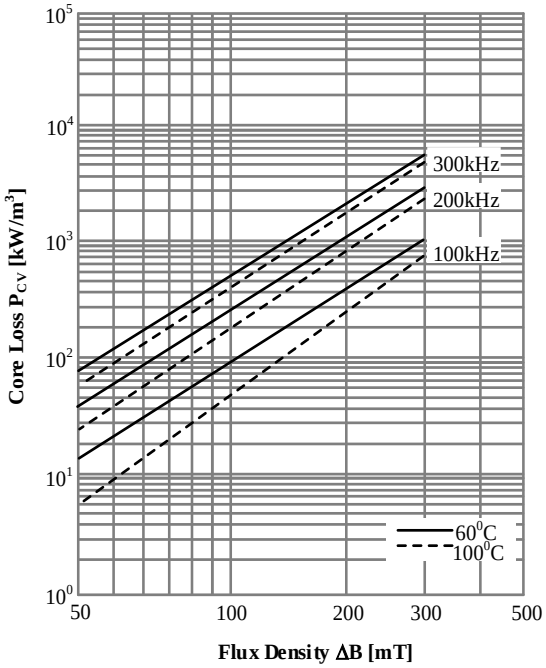



Fig. 4.28. Typical core loss chart for PC47 ferrite [91].

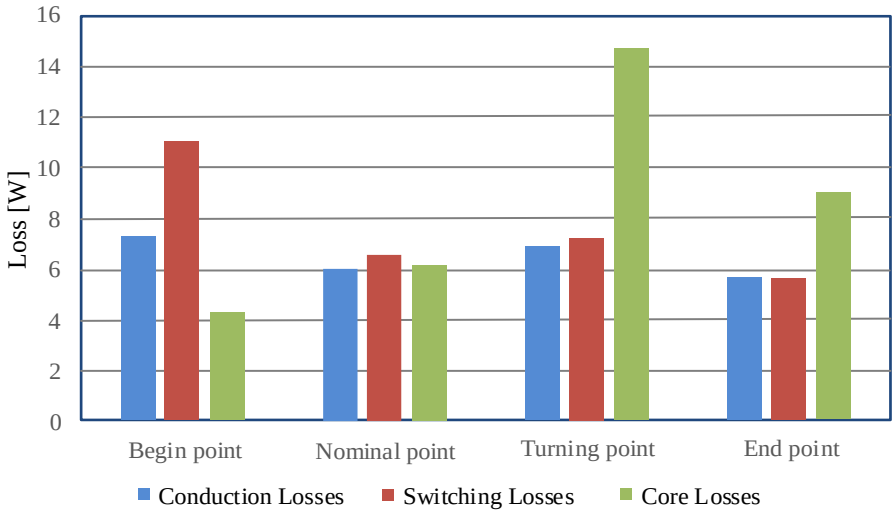


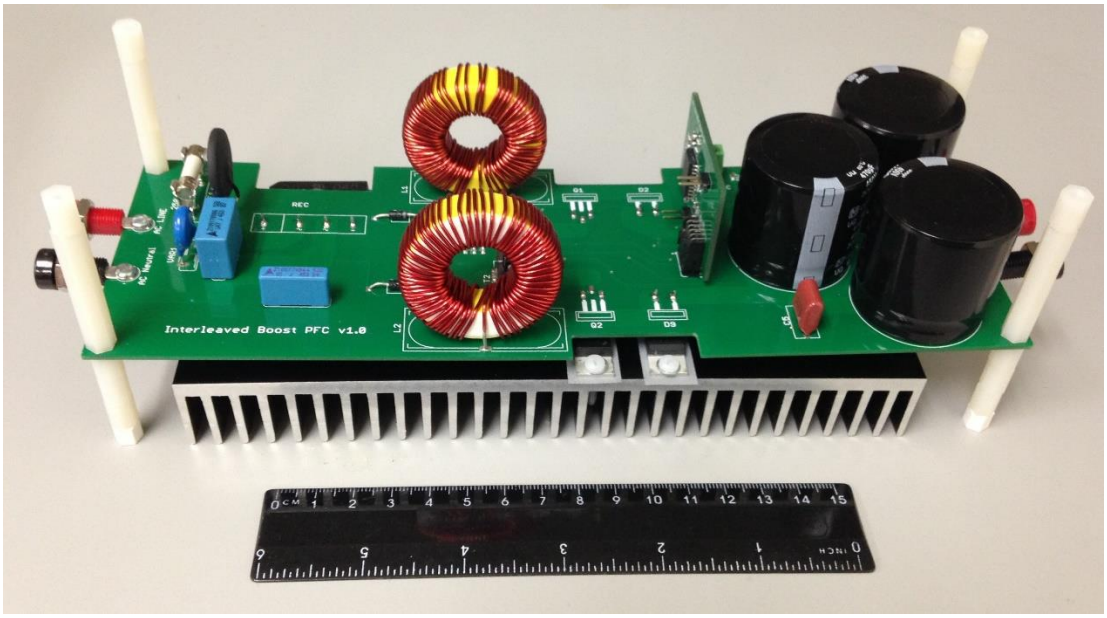

Fig. 4.29. Loss breakdown for critical operating points.

Fig. 4.29 provides the breakdown of the LLC full-bridge converter losses at the four critical operating points. According to Fig. 4.29, different losses dominate in different SOC of the charging process. In the beginning of the charging, switching loss dominates since the switching frequency is high. From begin point to turning point, there is an obvious increase particularly in the core losses. This is because both the volt-second of transformer and the peak current of inductor increase, resulting in increasing $\Delta B$, with the increase of power level. Conduction loss reaches its minimum value in the nominal point. This is because the resonant tank has minimum impedance in nominal point and thus minimum circulating power.

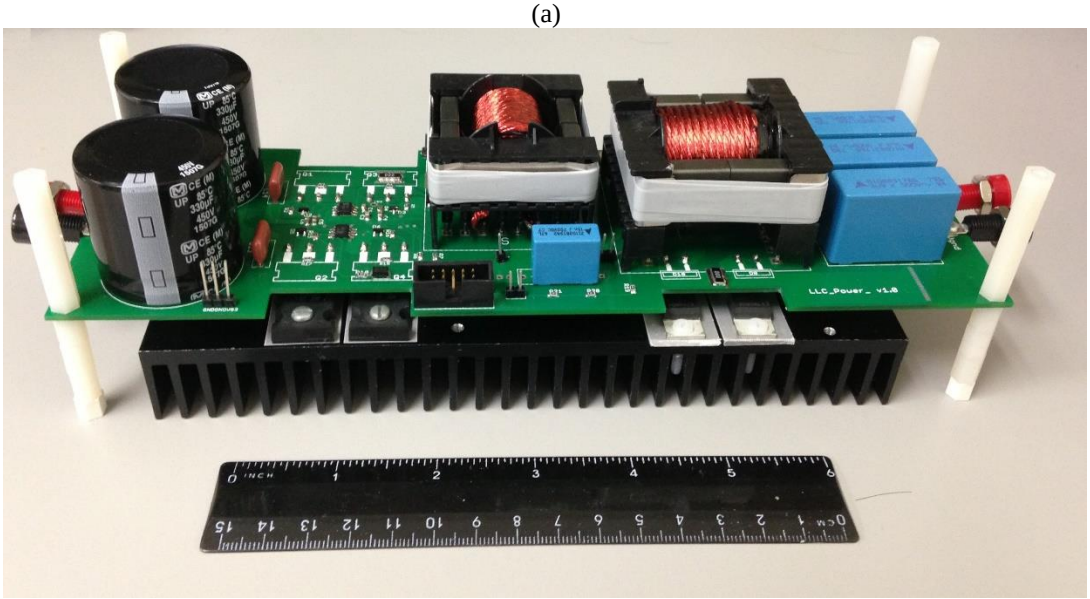
### *4.9* *Experiment* Results

A 1 kW prototype was built as a proof-of-concept to verify theoretical analyses. Key parameters and power devices of the prototype are listed in Table 4-4. A 1 kW prototype was built as a proof-of-concept to verify theoretical analyses. Key parameters and power devices of the prototype are listed in Table III. Photos of the

prototype is provided in Fig. 4.30. In Fig. 4.30 (b), the two magnetic components are resonant inductor and transformer, respectively.




(a)




(b)

Fig. 4.30. A 1 kW PEV charger prototype, (a) interleaved boost PFC converter, (b) full bridge LLC converter.

Table 4-4 Design of an interleaved full-bridge LLC onboard charger

| Symbol | Quantity or Device | Parameter |
|---|---|---|
| $C_{DC}$ | DC link capacitor | 3×330 μF |
| $V_{in}$ | Input voltage | 110 V/60 Hz |
| $V_{DC}$ | DC link voltage | 300 Vdc |
| $f_{pfc}$ | Switching frequency for PFC stage | 100 kHz |
| *IC1* | PFC controller | UCC28070 |
| $V_b$ | Battery voltage range | 320 V to 420 V |
| $P_{max}$ | Rated maximum power | 1 kW |
| $f_p$ | Primary resonant frequency | 200 kHz |
| $f_s$ | Secondary resonant frequency | 105.1 kHz |
| $N$ | Transformer turn ratio | 5:6 |
| $L_m$ | Magnetizing inductor | 160 μH |
| $L_r$ | Resonant inductor | 62.51 μH |
| $C_r$ | Resonant capacitor | 10 nF |
| $C_f$ | Output filter capacitor | 3×3.3 μF |
| *IC2* | Resonant controller | UCC25600 |
| $D_1$~$D_4$ | Diode Rectifier | NTE5322 |
| $S_1$~$S_2$ | Boost MOSFETs | FCA16N60N |
| $D_5$~$D_6$ | Boost Diodes | IDB06S60C |
| $S_3$~$S_6$ | LLC MOSFETs | STB23NM60ND |
| $D_7$~$D_{10}$ | Secondary Diode Rectifier | DSEP29-06A |

The waveforms achieved in the first stage interleaved boost converter are presented in Fig. 4.31 and Fig. 4.32. As seen from Fig. 4.31, the input current is in phase with the input voltage. The converter demonstrates power factor higher than 0.99. The dc link voltage is regulated at 300 V with a ripple voltage of 14.5 V. According to Fig. 4.32, In comparison with the inductor current ripple, the input current ripple is significantly reduced. At 1 kW operation, THD and conversion efficiency are measured as 3.61% and 96.3%, respectively.

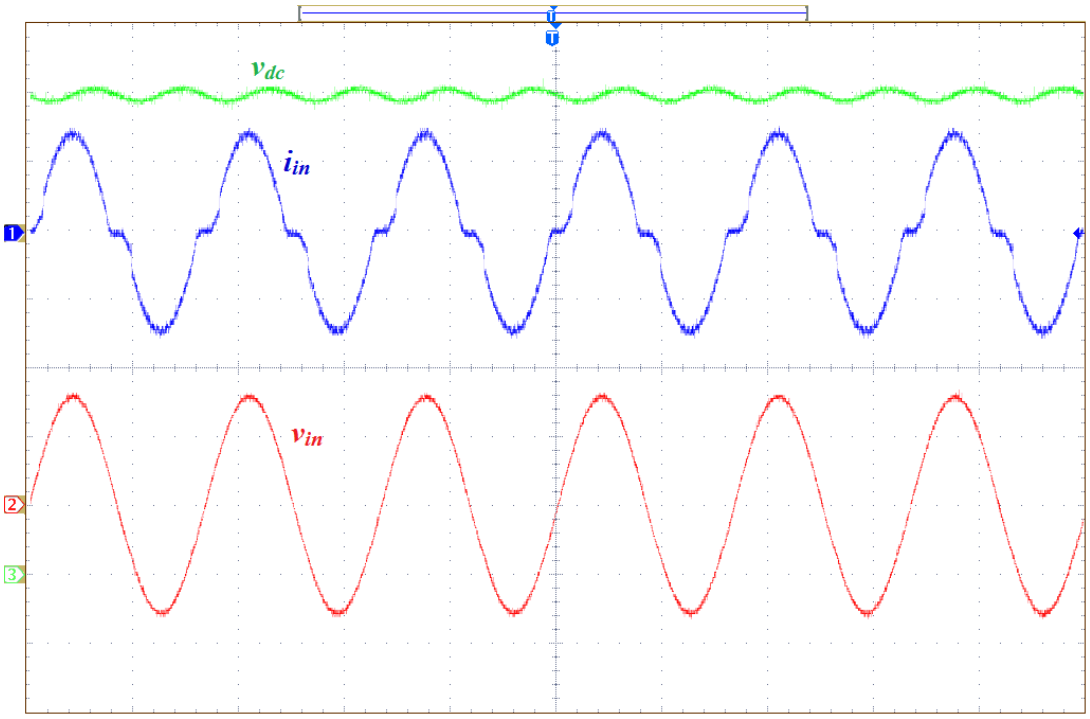



Fig. 4.31. Waveforms of interleaved boost PFC converter operating at 1 kW. From top to bottom: $v_{dc}$ (50V/div), $i_{in}$ (10A/div), $v_{in}$ (100V/div); time 10 ms/div.

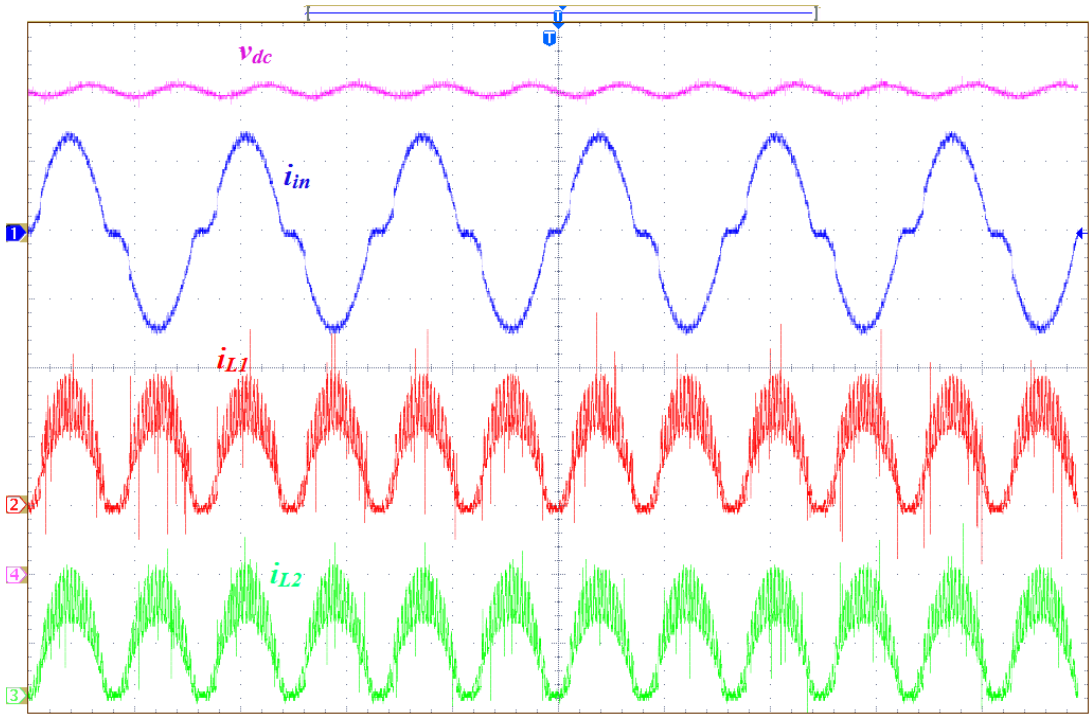



Fig. 4.32. Inductor waveforms of interleaved boost PFC converter operating at 1

kW. From top to bottom: $v_{dc}$ (50V/div), $i_{in}$ (10A/div), $i_{L1}$ (5A/div), $i_{L2}$ (5A/div); time 10 ms/div.

The experiment results of the second stage LLC converter are presented in figures 4.33-4.36. Waveforms of resonant inductor current $i_{Lr}$, resonant capacitor voltage $v_{Cr}$, output voltage of full bridge inverter $v_{ab}$, and gate drive signal of $S_4$ $v_{GS4}$, are recorded. High voltage differential probes are used to track and capture the waveforms of $v_{Cr}$ and $v_{ab}$. As it can be seen from these figures, the full-bridge LLC converter always operates in inductive region, where $i_{Lr}$ lags $v_{ab}$. Turning-on process of MOSFETs and turning-off process of free-wheeling diodes are both lossless.

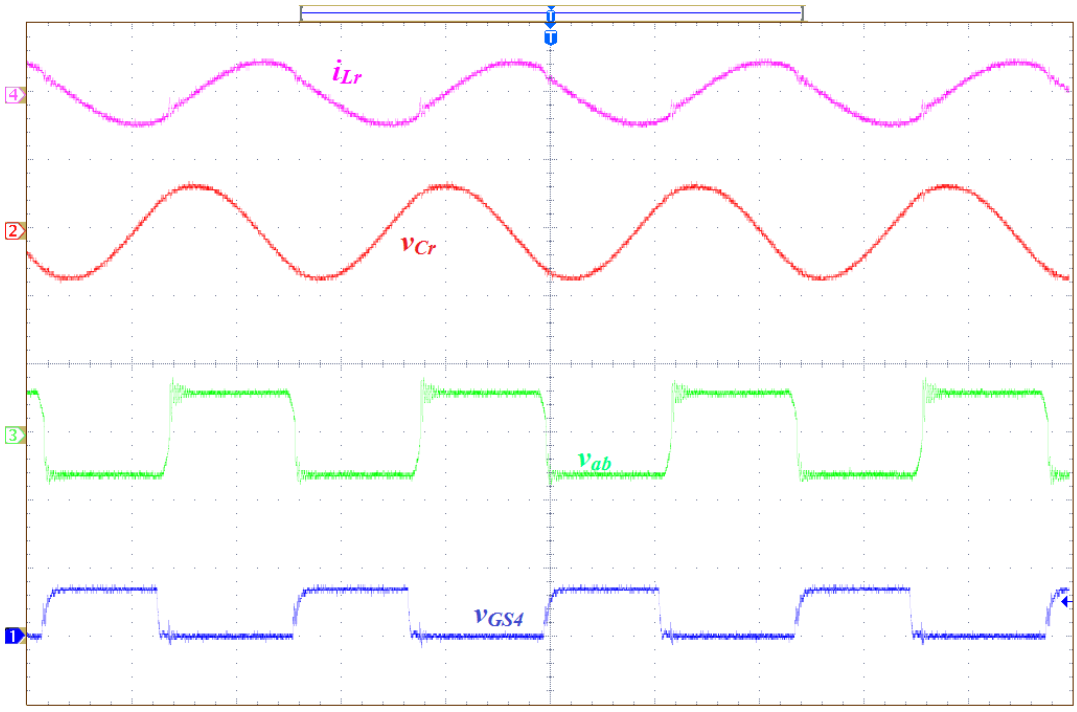



Fig. 4.33. LLC converter operating at begin point ($V_{bat}$ = 320 V, $I_{bat}$ = 2.38 A). From top to bottom: $i_{Lr}$ (10A/div), $v_{Cr}$ (500V/div), $v_{ab}$ (500V/div), $v_{GS4}$ (20V/div); time 2 μs/div.

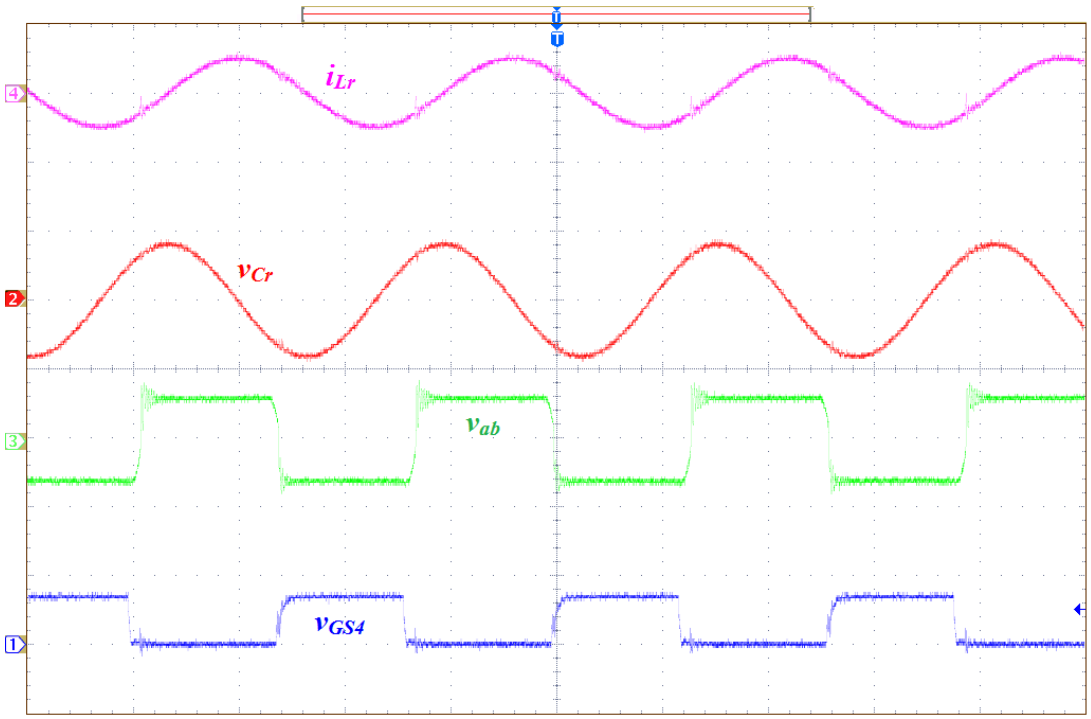



Fig. 4.34. LLC converter operating at nominal point ($V_{bat}$ = 360 V, $I_{bat}$ = 2.38 A). From top to bottom: $i_{Lr}$ (10A/div), $v_{Cr}$ (500V/div), $v_{ab}$ (500V/div), $v_{GS4}$ (20V/div); time 2 μs/div.

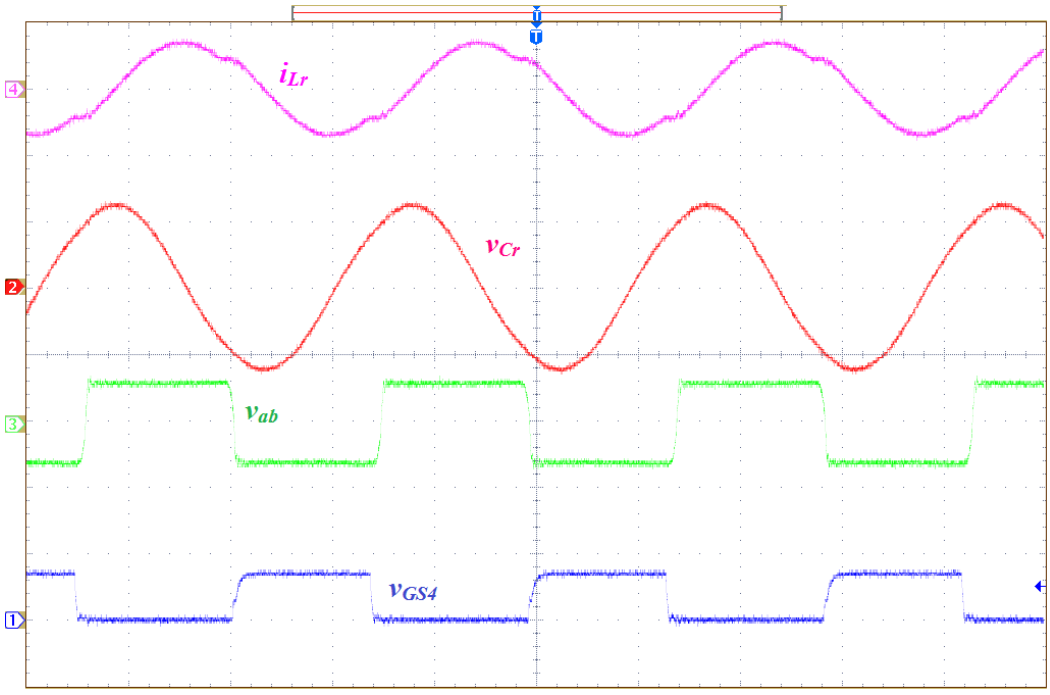



Fig. 4.35. LLC converter operating at turning point ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A).

From top to bottom: $i_{Lr}$ (10A/div), $v_{Cr}$ (500V/div), $v_{ab}$ (500V/div), $v_{GS4}$ (20V/div); time 2 μs/div.

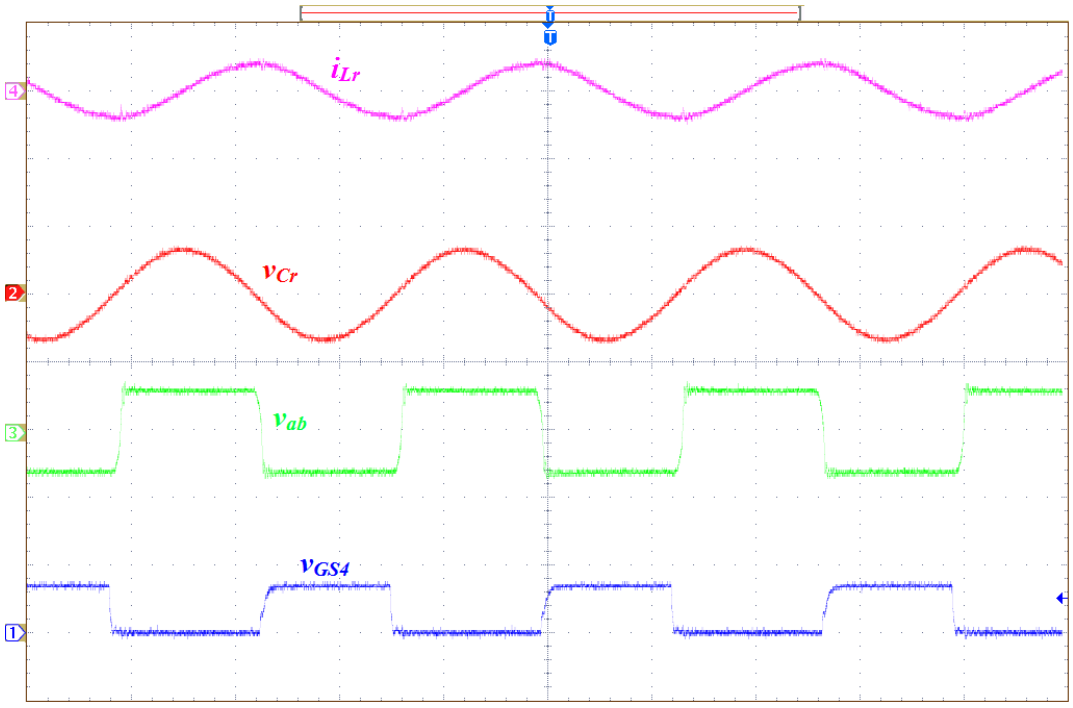



Fig. 4.36. LLC converter operating at end point ($V_{bat}$ = 420 V, $I_{bat}$ = 0.24 A). From top to bottom: $i_{Lr}$ (10A/div), $v_{Cr}$ (500V/div), $v_{ab}$ (500V/div), $v_{GS4}$ (20V/div); time 2 μs/div.

Fig. 4.33 demonstrates the operation at the begin point, where the switching frequency is regulated at 208.3 kHz. Fig. 4.34 shows the operation waveforms at the nominal point. At this point, switching frequency is regulated at 192.5 kHz. Likewise, Fig. 4.35 presents the operation at the turning point. The 1 kW peak power is achieved at this point, where the switching frequency is regulated at 172.3 kHz. The operation waveforms representing the end point are plotted in Fig. 4.36. The corresponding switching frequency is 185.1 kHz.

Multi-resonance phenomenon can be clearly seen in Fig. 4.35. At the moment $S_2$ and $S_4$ are turned off, $i_{Lr}$ starts to commutate from $S_2$ and $S_4$ to $D_{S1}$ and $D_{S3}$. This

forces $v_{ab}$ to abruptly change from –300V to 300V. From then on, $L_r$ resonates with $C_r$. Since secondary diodes $D_7$ and $D_{10}$ are on, $V_{bat}$ is applied to the secondary side of transformer. This makes the current in magnetizing inductor ($i_{Lm}$) increases linearly. When $i_{Lm}$ reaches $i_{Lr}$, $L_m$ begins to participate in the resonance with $L_r$ and $C_r$.

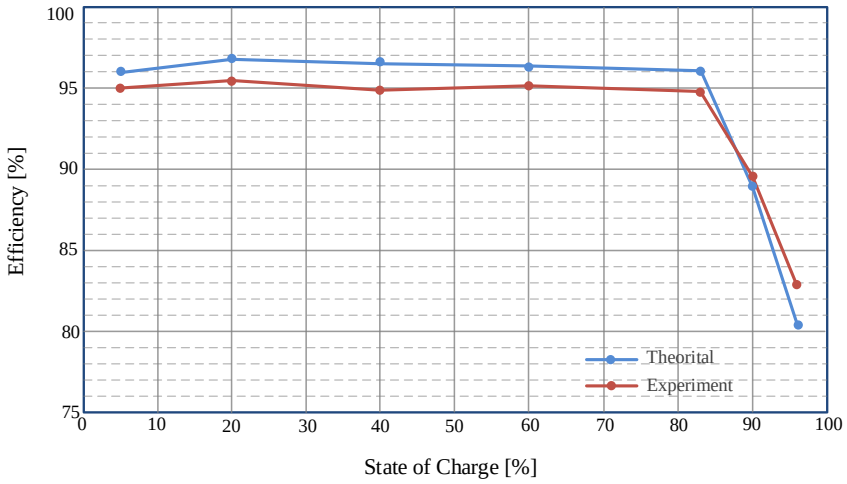



Fig. 4.37. Efficiency of the designed LLC converter versus state of charge of battery pack.

Efficiency of the LLC stage versus state of charge (SOC) of the battery pack is illustrated in Fig. 4.37. As it can be seen from Fig. 4.37, the LLC stage maintains good efficiency performance from the begin point to the turning point, where the output voltage varies from 320 V to 420 V. There is an obvious efficiency drop from turning point to end point. This is because in CV charging mode, $I_{bat}$ decreases fast. Hence, the charging power decreases quickly with the increase of SOC. However, the circulating power in the resonant tank remains high, which incurs high conduction loss. On the other hand, $\Delta B$ of magnetic core does not tend to decrease significantly, which poses relatively high core losses.

## *4.10 Summary*

In this chapter, an onboard PEV battery charger is proposed, analyzed, designed, and developed. Interleaved boost topology is used in the first stage for PFC and THD reduction as well as reducing volume of the magnetic components. In the second stage, a full bridge LLC resonant converter is employed to achieve high conversion efficiency over the full voltage range of the battery pack.

The suitability and advantages of the proposed converter are discussed and design guidelines are provided through theoretical analyses for both stages. As a case study, design considerations for a 1 kW charger prototype, which converts 110 V, 60 Hz AC to battery voltage range of 320 V to 420 V are provided, considering the characteristics of the converter.

Finally, the experiment results are presented for validation. The first stage interleaved boost converter demonstrates unity power factor operation at the rated power and achieves THD less than 4%. In the second stage LLC converter, the switching losses, conduction losses and core losses are optimized to achieve good overall efficiency performance over wide output voltage range. The future research will be focused on expanding power of the charger to a higher level and realizing bi-directional energy conversion.

# Chapter 5 Minimizing the Circulating Energy and Tracking the Maximum Efficiency Point of LLC Converter

## *5.1 Introduction*

The isolated battery charger typically consists of two power stages; front-end stage for rectification of ac input voltage and power factor correction, and second-stage dc/dc converter for voltage regulation and galvanic isolation [27], [92], [93]. Typically the rectifier is controlled through two cascaded control loops, where the inner control loop shapes the input current close to sinusoidal waveform in phase with the input voltage, and the outer control loop determines the amplitude of the input current according to the desired dc link voltage. In rectification stage, boost derived topologies [94]–[96] are preferred due to their simplicity in controlling the input current. In conventional approaches, the dc link voltage is regulated at a constant voltage, compatible with the universal ac input voltages from the grid (85~275V, 45~70Hz).

In dc/dc isolation stage, zero-voltage switching (ZVS) topologies are preferable to enhance efficiency of battery chargers [97]–[99]. In particular, LLC topology has several advantages over other ZVS topologies, such as (a) short circuit protection, (b) good voltage regulation in light load condition, (c) the ability to operate with ZVS over wide load ranges, (d) having only a capacitor as the output filter in comparison to the conventional LC filters [66], [100]. The design of the second stage LLC converter is highly related to the dc link voltage as battery voltage

greatly varies according to different SOC conditions. The constant-current constant-voltage (CC-CV) charging technique is the recommended charging profile for Lithium-ion batteries, which are the main energy storage units for world's top-selling highway-capable all-electric cars [24]. Fig. 3.4 in chapter 3 depicts the charging profile of a single Panasonic Li-ion battery cell. From depleted SOC to full SOC, voltage of the battery varies in a wide range.

The efficiency of the second stage dc/dc converter must be optimized over the wide battery voltage range to achieve the highest efficiency. Without any additional circuit or advanced control approach, the resonant tank parameters (the magnetizing inductance, resonant capacitor and inductor) of the LLC converter can be optimally designed to operate at high efficiency over a wide range in the curve given in Fig. 3.4 [99]–[103]. However, this approach provides high efficiency operation in a limited voltage range, and shows poor performance at light load condition, mainly due to the circulating current in the resonant tank. In [104], LLC converter is burst mode controlled where the basic idea is to operate the converter at its rated power by engaging the converter on and off repeatedly at light load condition, controlling the average power sent to the load. This approach is not suitable for battery charging applications as battery current becomes discontinuous, when LLC converter is turned off even if a bulky filter capacitor is utilized. Other techniques presented in literature modify the circuit components to enhance the light load efficiency of the LLC converter. In [105], two transformers are used to control the output voltage in a wide range, and in favor of increasing the efficiency at the light load. In [106], a modified LLC converter with interleaving feature is proposed to keep the switching frequency

constant and to improve the light load efficiency through phase shedding. However, these approaches increase the circuit components, particularly the magnetic component number [105]. A hybrid drive scheme is introduced for full-bridge synchronous rectifier in LLC, in favor of eliminating the secondary side diode conduction and reverse recovery losses [107]. In [108], a half bridge-LLC converter is operated at unity conversion ratio to increase the heavy load efficiency of a low voltage laptop adapter application. However, the output voltage variation window of laptop adapter is much smaller than that of PEV battery; a systematic approach for loss evaluation and efficiency improvement has not been provided; and the design considerations are not discussed.

This paper outlines a variable dc link approach to optimize the efficiency of the isolated dc/dc stage over the full battery voltage range and load conditions without adding any additional circuit or implementing on/off control. By actively controlling the dc link voltage with respect to the variation of battery voltage, the conversion efficiency of the dc/dc converter is always regulated to be the optimal value through keeping the switching frequency constant and thereby minimizing the circulating current in the resonant tank. With the proposed maximum efficiency point tracking technique, the efficiency performance of LLC converter is improved across the wide battery voltage range. Optimal design of the LLC converter together with the variable dc link approach has been provided. A comprehensive loss evaluation at key operating points has been presented, and compared with that of the conventional fixed dc link approach.

This chapter is organized as follow: In Section 5.2, a novel active controlled dc link voltage technique is proposed to optimize the efficiency of LLC converter over the wide output voltage range, which is based on the maximum efficiency point of LLC converter. In Section 5.3, circuit modeling and loss analyses at maximum efficiency point of LLC converter are provided. Design considerations are detailed in Section 5.4. Then, Section 5.5 provides the control strategy. Simulation results and efficiency comparison with conventional LLC charger are provided in Section 5.6 and Section 5.7, respectively. Finally, Section 5.8 outlines the summary.

## *5.2 Proposed Maximum Efficiency Point Tracking of LLC Converter*

### 5.2.1 DC Voltage Characteristics of LLC PEV Battery Charger with Fixed Dc Link Voltage

The block diagram of the conventional LLC based charger structure is depicted in Fig. 5.1. The dc link voltage is typically fixed at a constant value, within the range of 380V - 400V [52], [99], [109]. Based on the battery charging profile given in Fig. 3.4 in chapter 3, the dc voltage characteristics of LLC PEV battery charger is extracted as shown in Fig. 5.2.

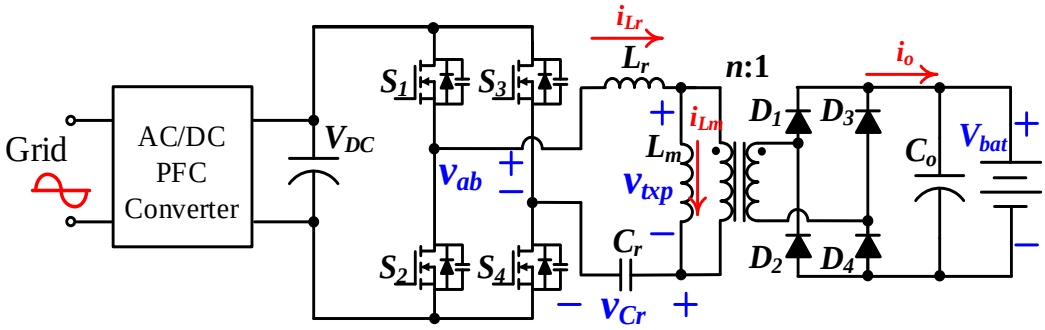


Fig. 5.1. The block diagram of the conventional LLC charger structure.

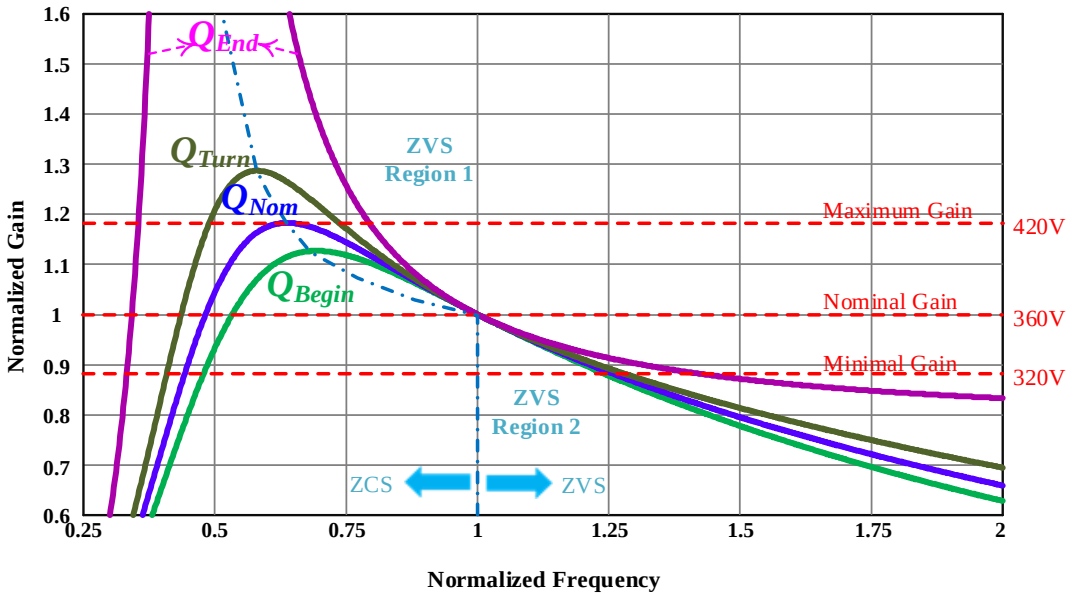



Fig. 5.2. Dc voltage characteristics of LLC charger.

In Fig. 5.2. Four different curves correspond to four critical operating points in the charging process of a Li-ion battery pack rated at 1 kW, which are marked literally in Fig. 5.2. Depending on the nature of the impedance of the resonant tank, the plane could be divided into two operation regions: inductive or ZVS, and capacitive or ZCS. MOSFETs need to be operated in ZVS region so that reverse recovery losses of freewheeling didoes could be eliminated. Boundary between ZCS and ZVS regions are marked in Fig. 5.2. ZVS region could be further divided into two regions. ZVS region 1 happens when switching frequency is below the resonant frequency between $L_r$ and $C_r$. ZVS region 2 happens when switching frequency is above the resonant frequency between $L_r$ and $C_r$. LLC converter in ZVS region 2 operates very similar to SRC converter.

Conventionally, $V_{DC}$, or the input voltage of LLC converter is fixed to be 390

V. In order to be adaptive to the wide voltage variation from the battery pack, LLC converter must be designed to have its operating region covering both the maximum gain and minimal gain. This means both ZVS region 1 and ZVS region 2 happen during the CC-CV charging process. Switching frequency varies in a wide range to regulate the output voltage to follow the battery pack voltage.

### 5.2.2 Operating Modes in ZVS Region 1

Fig. 5.3 shows the simulated waveform of LLC resonant converter working in ZVS region 1, in which the resonant tank input voltage $v_{ab}$, resonant inductor current $i_{Lr}$, magnetizing inductor current $i_{Lm}$, resonant capacitor voltage $v_{Cr}$, output current $i_o$, and transformer primary side voltage $v_{txp}$ waveforms are given. .

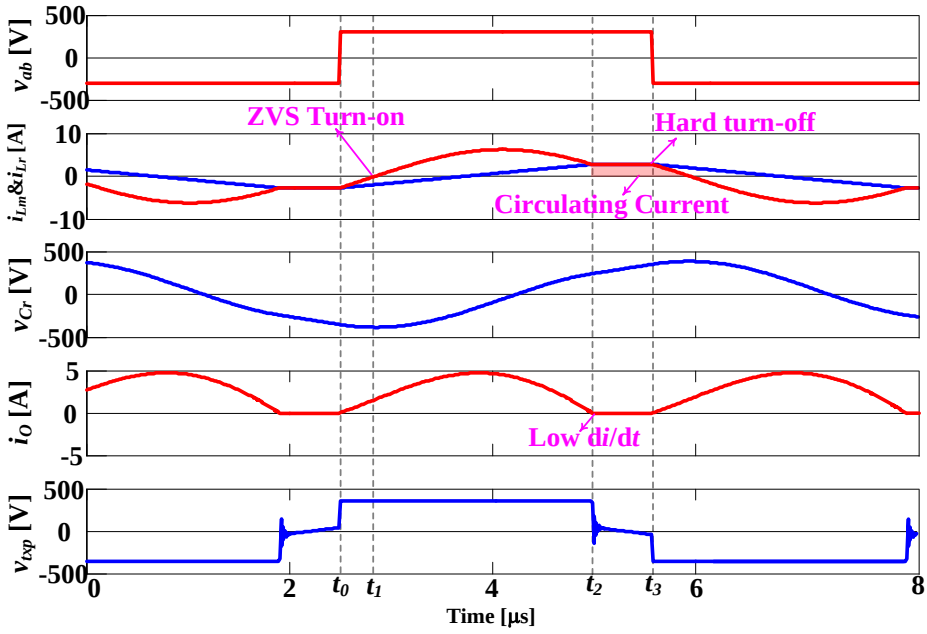



Fig. 5.3. Simulated waveforms of LLC converter operating in ZVS region 1.

In time interval [$t_0$, $t_2$), $i_{Lr}$ resonates up, and the difference between $i_{Lr}$ and $i_{Lm}$ is transferred to the load. Secondary diodes $D_1$ and $D_4$ are kept on, which regulates

$v_{txp}$ to be a constant voltage and equals to $nV_o$. Thus, $i_{Lm}$ increases linearly with the slope $nV_o/L_m$. At $t_1$, $i_{Lr}$ resonates from negative to positive; primary MOSFETs are turned on with ZVS and freewheeling didoes are turned off with ZCS. Consequently, reverse recovery losses from the freewheeling diodes are avoided.

At $t_2$, $i_{Lm}$ intersects with $i_{Lr}$; thus, secondary diodes $D_1$ and $D_4$ are turned off with ZCS. In time interval [$t_2$, $t_3$), $v_{txp}$ is no longer regulated by the output voltage, which makes $L_m$ participate into the resonance with $L_r$ and $C_r$. $i_{Lr}$ is circulating within the resonant network without delivering any power to the load. This circulating current causes conduction losses and core losses. The further switching frequency is away from the primary resonant frequency, the bigger circulating losses becomes.

### 5.2.3 Operating Modes in ZVS Region 2

Fig. 5.4 shows the simulated waveform of LLC resonant converter working in ZVS region 2. At $t_0$, primary MOSFETs $S_2$ and $S_3$ are turned off; freewheeling diodes $D_{S1}$ and $D_{S4}$ are turned on. This forces $v_{ab}$ to flip from $-V_{DC}$ to $V_{DC}$. In the time interval [$t_0$, $t_1$), a negative voltage, $V_{DC}/n$ - $V_o$, is applied across secondary didoes $D_3$ and $D_2$. This voltage forces $D_3$ and $D_2$ to turn off fast with a large $di/dt$, which causes reverse recovery losses of secondary didoes. $D_1$ and $D_4$ are turned on at $t_1$.

In time interval [$t_1$, $t_3$), $i_{Lr}$ resonates up, and the difference between $i_{Lr}$ and $i_{Lm}$ is transferred to the load. Secondary diodes $D_1$ and $D_4$ are kept on, which regulates $v_{txp}$ to be a constant voltage, equal to $nV_o$. Thus, $i_{Lm}$ increases linearly with the slope $nV_o/L_m$. At $t_2$, $i_{Lr}$ resonates from negative to positive; primary MOSFETs are turned on with ZVS and freewheeling didoes are turned off with ZCS. Consequently, reverse

recovery losses from the freewheeling diodes are avoided.

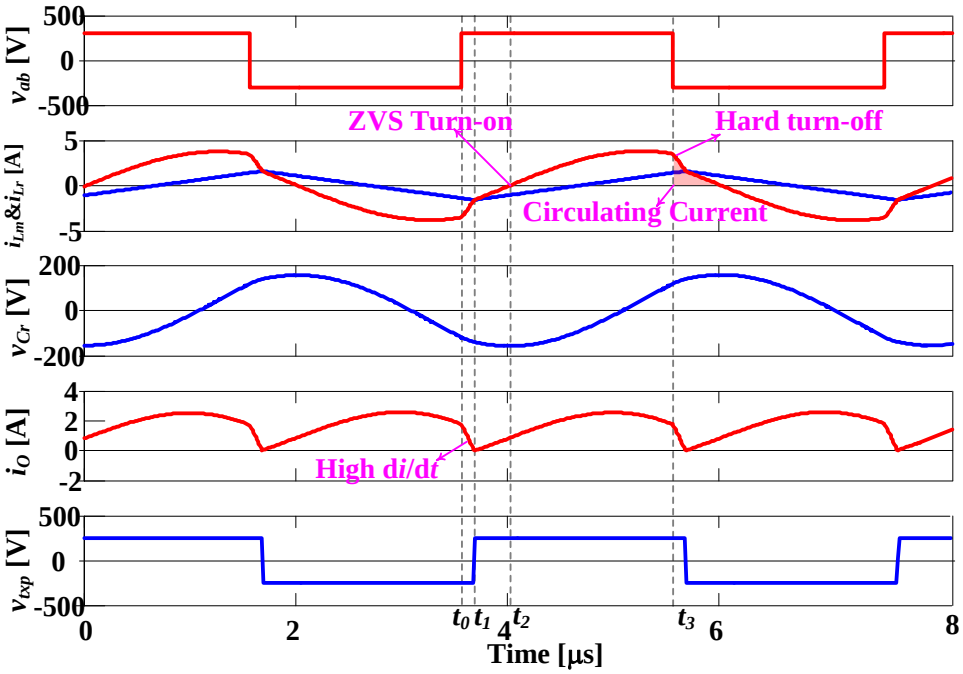



Fig. 5.4. Simulated waveforms of LLC converter operating in ZVS region 2.

Different from ZVS region1, $L_m$ never participates in the resonance with $L_r$ and $C_r$ in ZVS region 2. This means the circulating current as well as circulating losses are much smaller than operation in ZVS region 1.

### 5.2.4 Operating Modes in Primary Resonant Frequency

Fig. 5.5 shows the simulated waveform of LLC resonant converter working in primary resonant frequency. At $t_0$, primary MOSFETs $S_2$ and $S_3$ are turned off; freewheeling diodes $D_{S1}$ and $D_{S4}$ are turned on. This forces $v_{ab}$ to flip from $-V_{DC}$ to $V_{DC}$.

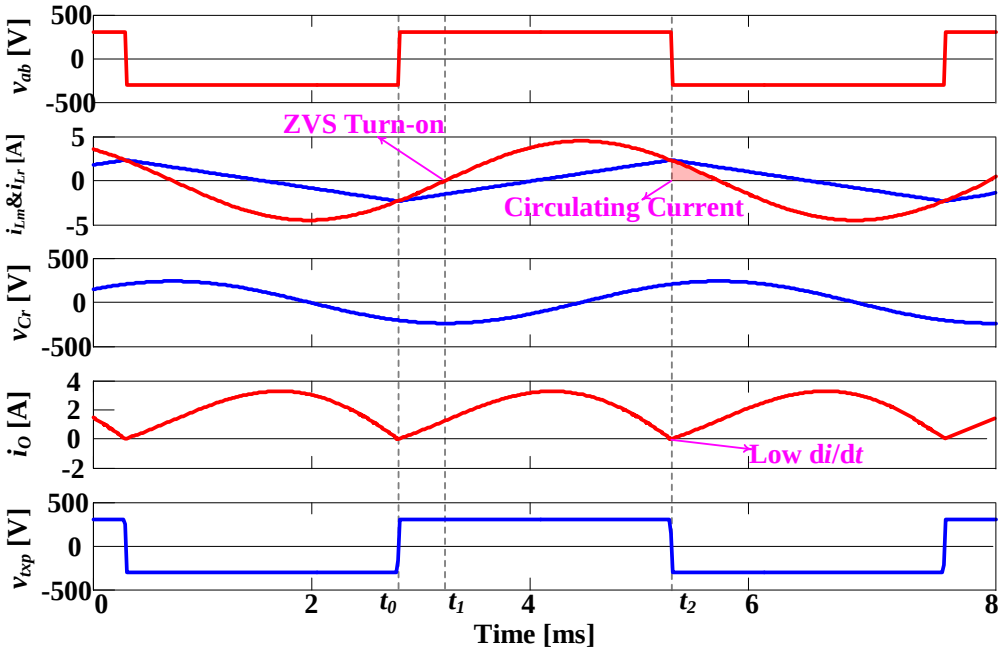



Fig. 5.5 Simulated waveforms of LLC converter operating in primary resonant frequency.

In time interval [$t_0$, $t_2$), $i_{Lr}$ resonates up, and the difference between $i_{Lr}$ and $i_{Lm}$ is transferred to the load. Secondary diodes $D_1$ and $D_4$ are kept on, which regulates $v_{txp}$ to be a constant voltage, equal to $nV_o$. Thus, $i_{Lm}$ increases linearly with the slope $nV_o/L_m$. At $t_1$, $i_{Lr}$ resonates from negative to positive; primary MOSFETs are turned on with ZVS and freewheeling didoes are turned off with ZCS. Consequently, reverse recovery losses from the freewheeling diodes are avoided.

At $t_2$, $i_{Lm}$ intersects with $i_{Lr}$. Primary MOSFETs $S_1$ and $S_4$ are turned off with hard switching; and the freewheeling diodes $D_{S2}$ and $D_{S3}$ begin to conduct. The output current goes to zero at $t_2$ with low $di/dt$. Thus, $D_1$ and $D_4$ are turned off with ZCS. Consequently, reverse recovery losses from the secondary diodes are avoided.

### 5.2.5 Proposed Maximum Efficiency Point Tracking Technique

Table 5-1 Comparison of LLC converter at different operating points

| Performance | ZVS Region 1 | ZVS Region 2 | Resonant Point |
|---|---|---|---|
| Primary MOSFETs turn-on | ZVS | ZVS | ZVS |
| Turning off loss of primary MOSFETs | Low | High | Low |
| *di/dt* of secondary diodes turn-off | Low | High | Low |
| Circulating energy | High | Low | Low |
| Conduction losses | High | Medium | Low |
| Switching losses | Low | High | Low |
| Harmonics | Low | High | Low |
| Overall performance | Moderate | Moderate | Best |

Performance of LLC converter at ZVS region 1, ZVS region 2, as well as at primary resonant frequency point are compared in Table 5-1. At primary resonant frequency, LLC converter has minimum circulating energy in the resonant tank, which corresponds to the lowest conduction losses. The conduction losses at resonant frequency are much smaller than conduction losses at ZVS region 1. Meanwhile, the switching losses at resonant frequency are much smaller than that of ZVS region 2. It can be concluded that operating LLC converter at primary resonant frequency corresponds to the minimum losses and the maximum conversion efficiency.

However, in PEV battery charging applications, the voltage of battery varies in a wide range. The converter must enter into ZVS region 2 if the battery voltage is smaller than nominal voltage, and must enter into ZVS region 1 if the battery voltage is higher than nominal voltage. The wide output voltage range brings significant challenges to the design of LLC converter.

The first challenge comes from the optimum design of LLC converter.

Typically, In comparison with LLC topology optimized for constant output voltage, optimizing LLC topology for wide output voltage range requires small inductor ratio ($L_m/L_r$) [110], [111]. With a small $L_m$, the turning off current of MOSFETs would be large. Consequently, the circulating current in $L_m$ would be high and the circulating loss from $L_m$ will become large. Consequently, the peak efficiency of LLC topology, which is optimized for wide output voltage range, will be reduced to a low level [101].

The second challenge comes from first harmonic approximation approach error. First harmonic approximation maintains good accuracy with switching frequency close to the primary resonant frequency [37]. For switching frequency far away from the primary resonant frequency, higher order harmonics must be accounted [100].

In this work, a novel maximum efficiency tracking technique is proposed, which constrains the switching frequency of the LLC converter to be equal to the primary resonant frequency, or the maximum efficiency point. The diagram of the proposed maximum efficiency tracking technique is shown in Fig. 5.6, where the dc link voltage varies with the variation of battery voltage. Voltage reference of the PFC controller comes from battery voltage sensor, and is proportional to battery voltage. Consequently, the dc link voltage increases gradually with the increase of state of charge and always follows:

$$V_{dc} = n(V_{bat} + 2V_D) \tag{5.1}$$

where, $n$ is the turn ratio of the transformer, $V_D$ is the voltage drop across each rectifier diode.

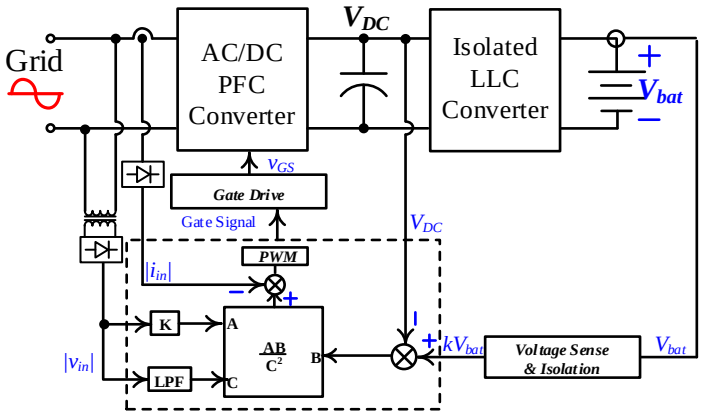



Fig. 5.6. Diagram of proposed maximum efficiency tracking technique.

With this control methodology, the LLC converter would automatically tune its switching frequency to be equal to the primary switching frequency. Thus, the maximum efficiency point could be always tracked, and the circuit performance across the wide output voltage range will be optimized.

## *5.3 Circuit Modeling and Loss Analysis at Maximum Efficiency Point*

### 5.3.1 Circuit Modeling at Maximum Efficiency Point

At resonant frequency, the resonant tank $L_r$ and $C_r$ in LLC topology operates as a band pass filter (BPF). The full bridge operates as a square wave generator. Since the diodes in the secondary rectification bridge also operate complimentarily the primary side of transformer is also modeled as a square wave signal. Equivalent circuit model of LLC converter at resonant frequency is plotted in Fig. 5.7.

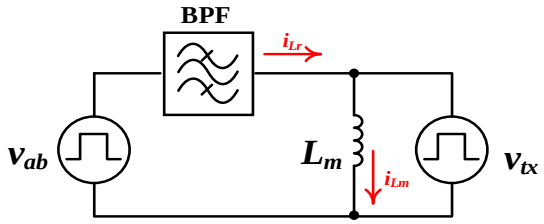



Fig. 5.7. Equivalent circuit model of LLC converter at resonant frequency.

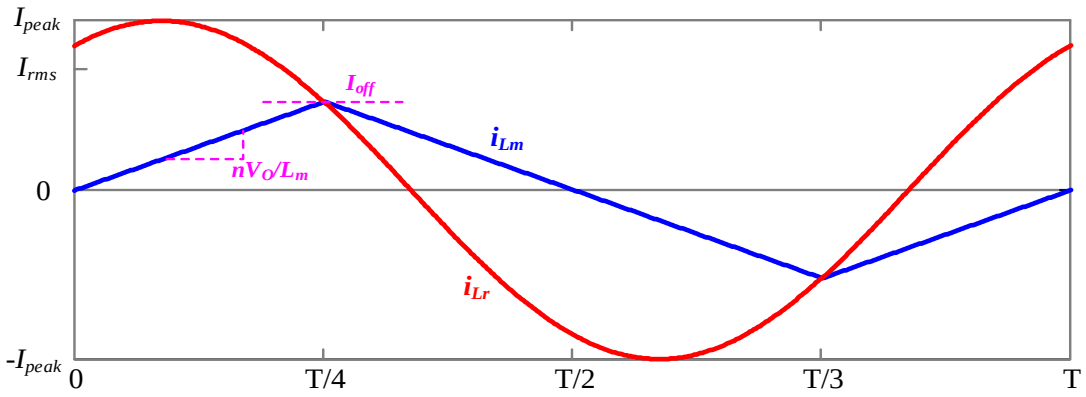



Fig. 5.8. Resonant tank current waveform at resonant frequency.

Due to the band pass filtering effect, only the fundamental frequency component of the square wave signal could pass. Fig. 5.8 provides the waveforms of $i_{Lm}$ and $i_{Lr}$ in a single switching period. From 0 to $T/4$, $i_{Lm}$ increases linearly with a rate of $nV_{bat}/L_m$. Thus, the turning off current of MOSFETs could be calculated as,

$$I_{off} = \frac{nV_{bat}T}{4L_m} \tag{5.2}$$

From $T/4$ to $3T/4$, according to the law of energy conservation, the energy from the dc link is equal to the energy consumed by the load. In other words, the energy of the dc link is transferred to the load. Thus,

$$\int_{T/4}^{3T/4} i_{Lr}\left(-V_{dc}\right)dt = \frac{V_{bat}^2}{R_L}\frac{T}{2} \tag{5.3}$$

$i_{Lr}$ is a sinusoidal function. Assuming the initial phase of $i_{Lr}$ is $\phi$, and the peak current is denoted by $I_{peak}$, $i_{Lr}$ can be represented as,

$$i_{Lr}(t) = I_{peak} \sin\left(\frac{2\pi}{T}t + \phi\right) \tag{5.4}$$

Since $i_{Lr}(T/4) = I_{off}$, $\phi$ can be obtained,

$$\phi = \arccos\frac{I_{off}}{I_{peak}} \tag{5.5}$$

Plugging Eq. (5.4) into Eq. (5.3), we can obtain,

$$I_{peak}V_{dc}\frac{\sin\phi T}{\pi} = \frac{V_{bat}^2}{R_L}\frac{T}{2} \tag{5.6}$$

Combining Eq. (5.5) with Eq. (5.6), $I_{peak}$ can be obtained as,

$$I_{peak} = \sqrt{\frac{n^2V_{bat}^2T^2}{16L_m^2} + \frac{\pi^2V_{bat}^4}{4R_L^2V_{dc}^2}} \tag{5.7}$$

The rms current can be derived as,

$$I_{rms} = \frac{I_{peak}}{\sqrt{2}} = \sqrt{\frac{n^2V_{bat}^2T^2}{32L_m^2} + \frac{\pi^2V_{bat}^4}{8R_L^2V_{dc}^2}} \tag{5.8}$$

Plugging Eq. (5.1) into Eq. (5.8),

$$I_{rms} = \frac{I_{peak}}{\sqrt{2}} = \sqrt{\frac{n^2V_o^2T^2}{32L_m^2} + \frac{\pi^2I_{bat}^2}{16n^2}} \tag{5.9}$$

### 5.3.2 Loss Analysis at Maximum Efficiency Point

Typically, four critical losses must be considered when analyzing the losses of LLC topology. They are a) conduction losses from the primary side, b) turning off losses from the primary side MOSFETs, c) core losses from the magnetic components, and d) conduction losses from the secondary rectification.

Conduction losses from the primary side are determined by the rms current of the resonant tank, $I_{rms}$. According to Eq. (5.9), $I_{rms}$ is a function of $L_m$. The larger $L_m$ is, the smaller $I_{rms}$ becomes; while smaller $I_{rms}$ corresponding to smaller conduction losses. Thus, conduction losses from the primary side could be reduced by increasing $L_m$.

Total turning off losses of the four primary MOSFETs can be calculated using Eq. (5.10).

$$P_{off} = \frac{n}{T} I_{off} V_{bat} t_{overlap} = \frac{n^2 V_{bat}^2 t_{overlap}}{4L_m} \tag{5.10}$$

where, $t_{overlap}$ is the overlap time between $I_{DS}$ *and* $V_{DS}$ during the turning-off process of MOSFET. According to Eq. (5.10), $P_{off}$ is a function of $L_m$. The larger $L_m$ is, the smaller $P_{off}$ becomes. Thus, turning off losses from the primary MOSFETs could also be decreased by increasing $L_m$.

Since there are two magnetic components, resonant inductor and transformer. Core loss need to be analyzed separately. Using Eq. (5.11), core losses can be calculated.

$$P_{fe} = k f_p^{\,x} \Delta B^y \tag{5.11}$$

where $k$, $x$, $y$ are coefficients determined by the core types and materials. $\Delta B$ is the flux density variation. According to Eq. (5.11), since $f_p$ is preset, core losses are mainly determined by $\Delta B$.

For resonant inductor $L_r$, $\Delta B$ is calculated using Eq. (5.12).

$$\Delta B_{Lr} = \frac{L\Delta i}{2n_{Lr}A_e} = \frac{LI_{peak}}{n_{Lr}A_e} = \frac{L}{n_{Lr}A_e}\sqrt{\frac{n^2V_{bat}^2T^2}{16L_m^2} + \frac{\pi^2V_{bat}^4}{4R_L^2V_{dc}^2}} \tag{5.12}$$

where, $A_e$ is the effective cross-section area of the ferrite core; $n_{Lr}$ is the number of turns winded on the core. According to equations (5.9) and (5.10), resonant inductor core losses are determined by $L_m$. The larger $L_m$ is, the smaller core losses become. Thus, core losses from the resonant inductor could be reduced by increasing $L_m$.

For transformer, $\Delta B$ is calculated using Eq. (5.13).

$$\Delta B_{TX} = \frac{\lambda_p}{2n_{TX,p}A_e} = \frac{nV_{bat}T}{4n_{TX,p}A_e} \tag{5.13}$$

where, $\lambda_p$ is the volt-second on the primary side of the transformer; and $n_{TX,p}$ is the number of turns on the primary side of the transformer. According to Eq. (5.13), core loss from the transformer is not a function of any of the resonant parameters ($L_m$, $L_r$, and $C_r$). It could be optimized by minimizing the total ferrite losses and copper losses of the transformer.

Conduction losses from the secondary rectification ($P_{rec}$) come from the forward voltage drop of the diodes ($V_{fwd}$) and are calculated using Eq. (5.14).

$$P_{rec} = \int_{T/4}^{3T/4} 2V_{fwd} i_o dt \approx 2V_{fwd} \overline{i_o} = 2V_{fwd} I_{bat} \tag{5.14}$$

Similar to the core losses of the transformer, $P_{rec}$ is not a function of the resonant parameters, and could be optimized by selecting the appropriate rectification diodes.

From the analysis, $L_m$ is the most critical parameter in designing the parameters of LLC resonant network. Typically, maximizing the value of $L_m$ while keeping the ZVS feature of primary MOSFETs could minimize the primary side conduction losses, reduce primary side MOSFETs turning off losses, and the transformer core losses.

## *5.4 Design Considerations*

According to the loss analysis in Section 5.3, it is always good to choose the maximum allowable value of $L_m$, so that the total losses could be minimized. Thus, it is necessary to find out the upper limit of $L_m$.

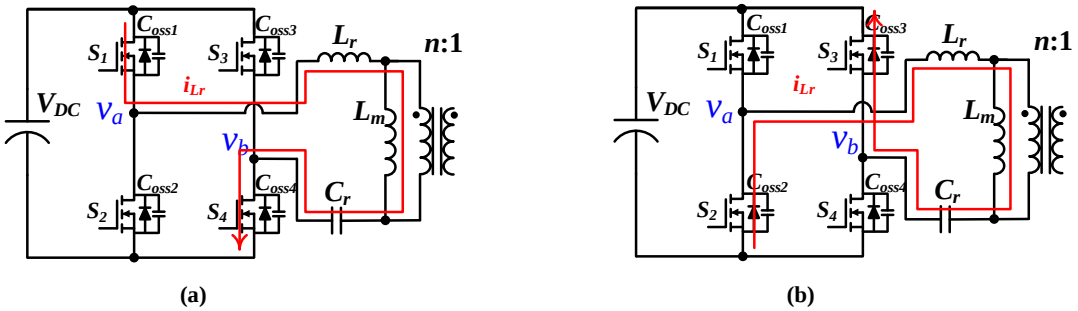



Fig. 5.8. Operation mode at (a) $t_3$ and (b) $t_4$.

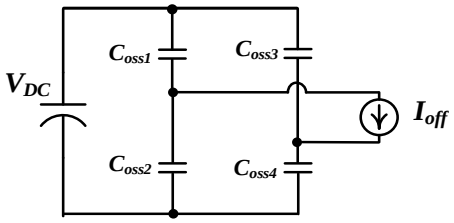



Fig. 5.9. Equivalent circuit of $v_{ab}$ transition.

The output voltage of full bridge, $v_{ab}$, is a square waveform, which switches between $V_{dc}$ to $-V_{dc}$. During each transition from $V_{dc}$ to $-V_{dc}$ or vice versa, internal output capacitance of power MOSFETs, shown by $C_{oss,i}$ ($i$ = 1:4), should be either charged or discharged. This could be observed from Fig. 5.8. Fig. 5.9 shows the equivalent circuit of the transition of $v_{ab}$ from $V_{dc}$ to -$V_{dc}$. During this process, $i_{Lr}$ could be seen as a constant current source with current equals to $I_{off}$. The charging of $C_{oss,1}$, $C_{oss,4}$ and discharging of $C_{oss,2}$, $C_{oss,3}$, are accomplished within a time period $t$, as calculated in Eq. (5.15).

$$t = \frac{4V_{dc}C_{oss}}{I_{off}} = \frac{16L_mC_{oss}}{T} \tag{5.15}$$

where, $C_{oss,1}$, $C_{oss,2}$, $C_{oss,3}$, and $C_{oss,4}$ are assumed to be equal and denoted by $C_{oss}$.

In order to ensure the ZVS turning on of MOSFETs, The length of this time period must be smaller than that of the deadband. The ZVS boundary waveforms are demonstrated in Fig. 5.10.

$$t_{dead} \geq t = \frac{16 L_m C_{oss}}{T} \tag{5.16}$$

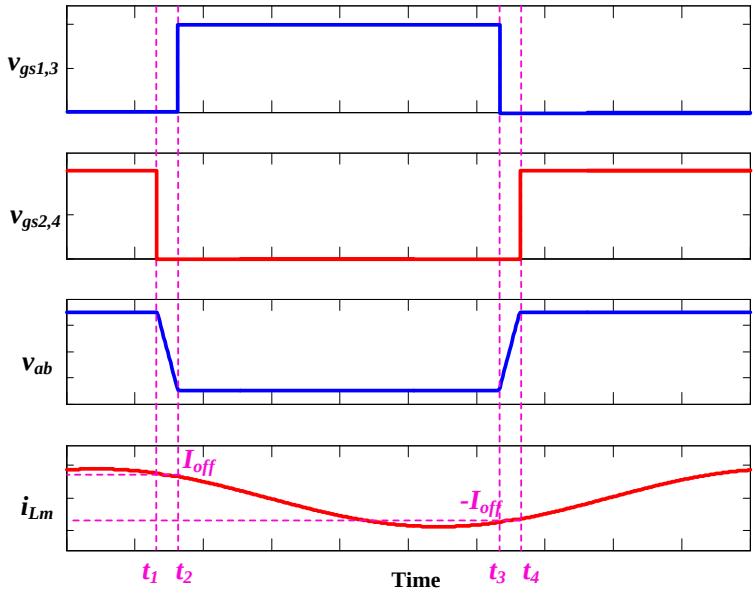



Fig. 5.10. ZVS boundary waveform: MOSFETs output capacitors are charged and discharged in the deadband.

According to Eq. (5.16), the upper limit of $L_m$ could be obtained,

$$L_m \leq \frac{T t_{dead}}{16 C_{oss}} \tag{5.17}$$

Thus, the maximum allowable value of $L_m$ could be determined as Eq. (5.18),

$$L_m = \frac{T t_{dead}}{16 C_{oss}} \tag{5.18}$$

After determining $L_m$, the next step is to determine $L_r$ and $C_r$. The product of $L_r$ and $C_r$ is calculated from the primary resonant frequency,

$$L_r C_r = \frac{1}{4\pi^2 f_p^2} \tag{5.19}$$

In order to evaluate the load condition, quality factor $Q$ is introduced as,

$$Q = \frac{\sqrt{L_r / C_r}}{n^2 R_L} \tag{5.20}$$

where, $\sqrt{L_r/C_r}$ is called the characteristic impedance. Generally, for specific load condition ($R_L$), smaller characteristic impedance or smaller $Q$, corresponds to higher peak voltage gain. On the other hand, smaller $Q$ corresponds to smaller $L_r$. This means bigger inductor ratio, $L_m/L_r$. Increasing the inductor ratio cause the peak gain to decrease [35], [110].

For maximum efficiency point tracking technique, it is always desired to operate the LLC circuit at $f_p$, where the normalized voltage gain is unity. However, due to the voltage ripple on the dc link capacitor from the PFC stage, it is necessary to have a secure gain margin (e.g. ±10%). This gain margin must correspond to a narrow frequency range, so that the circuiting power in the resonant tank could be kept small. According to Eq. (5.20), the heaviest load condition corresponds to the smaller $R_L$, or the begin point of the charging process. According to Fig. 5.2, as it can be seen from the curve associated with the begin point, the voltage gain in the desired frequency range (e.g. $0.9f_p$~$1.1f_p$) must cover the secure gain margin (e.g. 1.1~0.9), so that the

designed LLC converter is able to tolerant the voltage variation from the dc link capacitor with little efficiency degradation. Consequently, the value of characteristic impedance or *Q* at beginning point can be found based on this consideration.

According the aforementioned design considerations, a 1kW LLC prototype is designed. The parameters are summarized in Table 5-2.

Table 5-2 Design of a 1 kW LLC onboard charger

| Symbol | Quantity or Device | Parameter |
|---|---|---|
| $V_{dc}$ | DC link Voltage | 324V to 424V |
| $V_b$ | Battery voltage range | 320 V to 420 V |
| $P_{max}$ | Rated maximum power | 1 kW |
| $f_p$ | Primary resonant frequency | 200 kHz |
| $T$ | Resonant period | 5 μs |
| $M_{peak}$ | dc gain at 180 kHz at begin point | 1.1 |
| $C_{oss,eq}$ | Equivalent output capacitance of MOSFET | 435 pF |
| $t_{dead}$ | Deadband time | 150 ns |
| $n$ | Transformer turn ratio | 1:1 |
| $L_m$ | Magnetizing inductor | 107.6 μH |
| $L_r$ | Resonant inductor | 31.7 μH |
| $C_r$ | Resonant capacitor | 20 nF |
| $C_f$ | Output filter capacitor | 3×3.3 μF |

## *5.5 Control Strategy*

The control scheme of proposed maximum efficiency point tracking LLC charger is plotted in Fig. 5.11. Different from conventional two stage chargers with constant dc link voltage, proposed control strategy ensures that dc link voltage follows the change of battery pack voltage. Voltage reference of the PFC controller comes from the isolated voltage sensing block and is proportional to the battery pack voltage. With this control strategy, the secondary LLC converter could be regulated to be working at the primary resonant frequency.

For the battery charging LLC interface, parallel double control loops are adopted. An external digital control is utilized to detect the state of charge of the battery pack. In the constant current charging mode, the current control loop is activated. Output current is sensed to compare with the reference current through an error amplifier. The error is compensated through a PI compensator and fed to the voltage controlled oscillator. The voltage controlled oscillator translates the voltage signal into frequency signal and feed it to the logic module. Corresponding complimentary gate signals with deadband are generated by the logic module. In the constant voltage charging mode. The voltage control loop is activated. Control of constant voltage operation is similar to that of constant current operation.

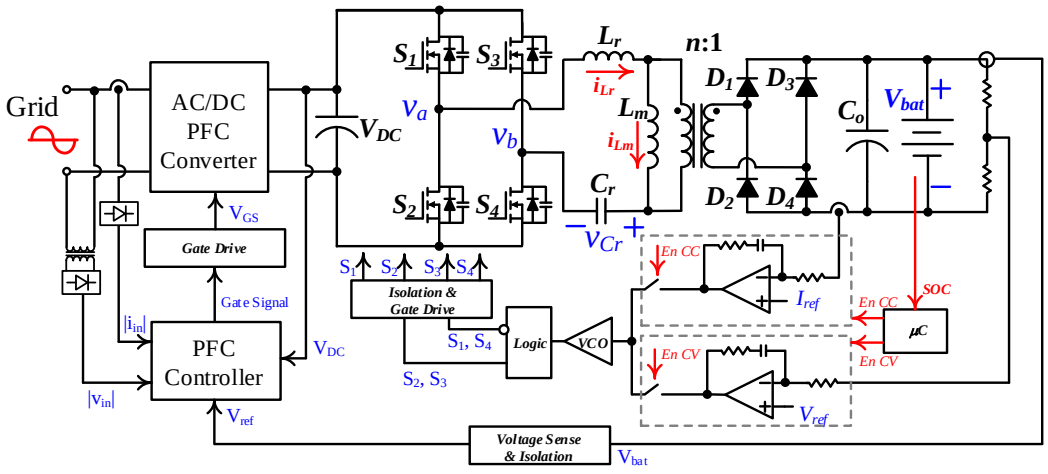



Fig. 5.11. Control schema of the proposed maximum efficiency point tracking of LLC charger.

## *5.6 Simulation Results*

Based on this design, the LLC converter is modeled and simulated. Figures 5.12-5.15 show the simulated waveform of designed LLC converter operating at

begin point, nominal point, turning point, and end point, respectively. According to the simulation results, the switching frequency is always regulated to be equal to the primary resonant frequency (200 kHz). This means the optimal operating point is successfully tracked. From the begin point to the turning point, with the increase of power level, the difference between $i_{Lr}$ and $i_{Lm}$ also increases gradually. This means the power delivered to the load is taking a bigger part in the total power issued from the supply. From the turning point to the end point, with the swift decrease of the power level, LLC converter operation mode moves from boundary conduction mode to discontinuous conduction mode.

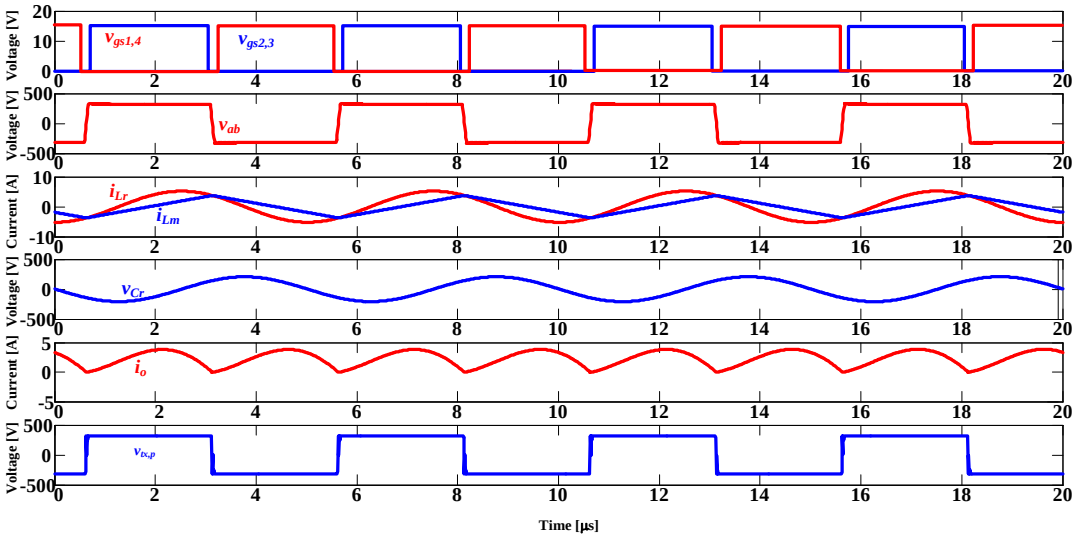



Fig. 5.12. Simulated result of LLC converter operating at begin point ($V_{bat}$ = 320 V, $I_{bat}$ = 2.38 A).

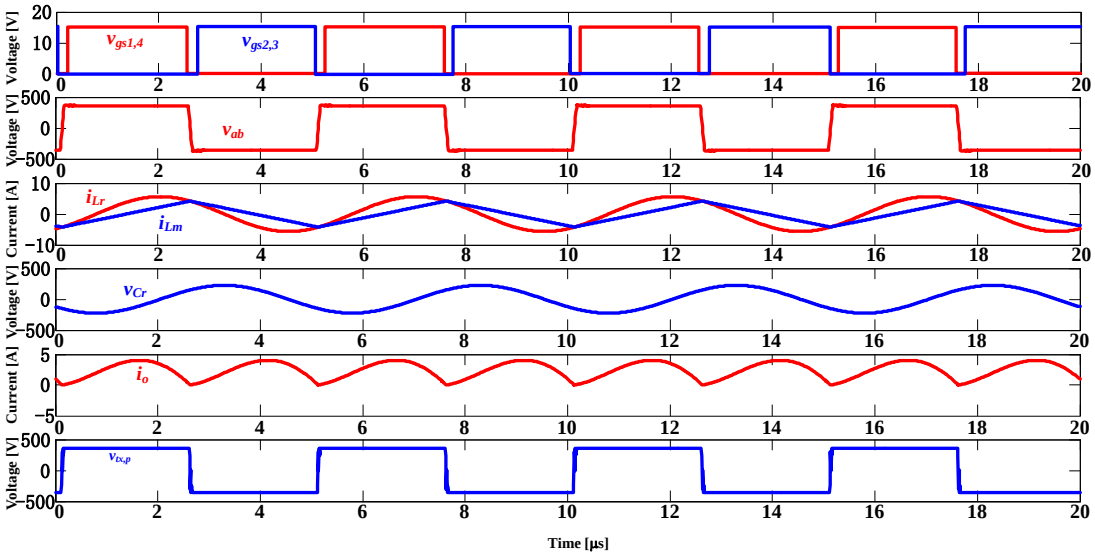



Fig. 5.13. Simulated result of LLC converter operating at nominal point ($V_{bat}$ = 360 V, $I_{bat}$ = 2.38 A).

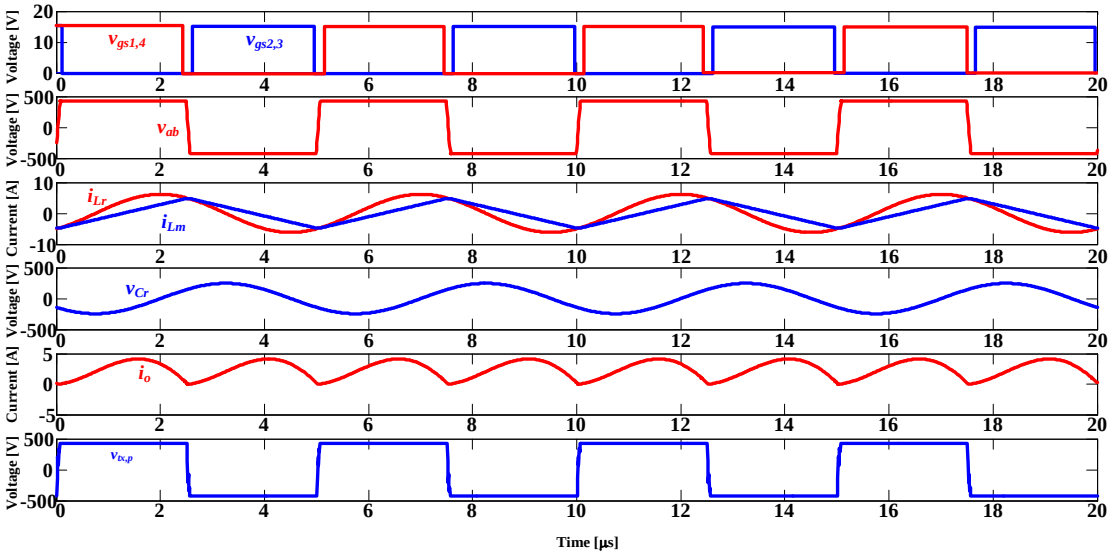



Fig. 5.14. Simulated result of LLC converter operating at turning point ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A).

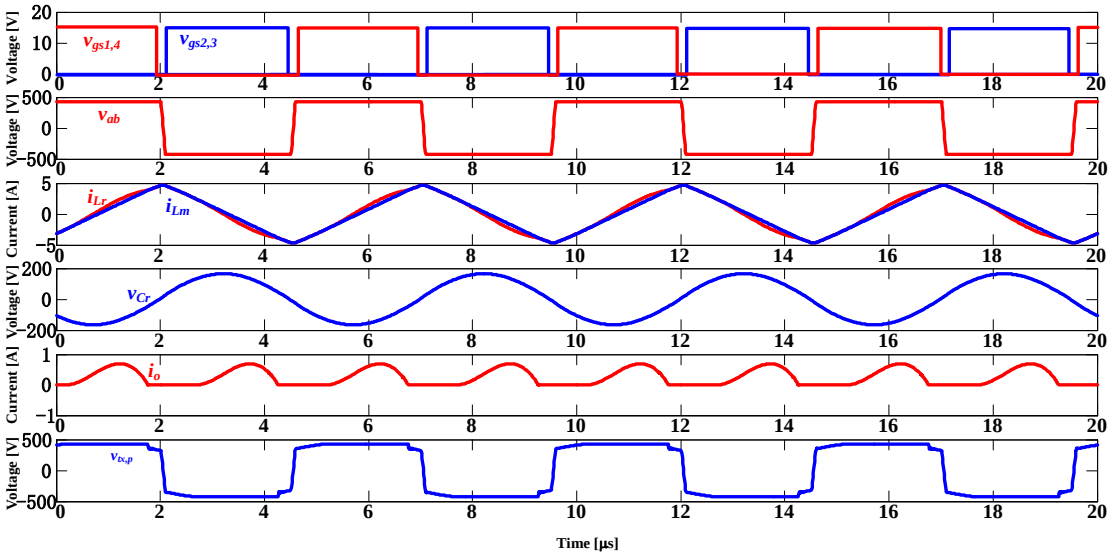



Fig. 5.15. Simulated result of LLC converter operating at end point ($V_{bat}$ = 420 V, $I_{bat}$ = 0.238 A).

## *5.7 Experiment Results*

Based on this design, the LLC converter is designed. Figures 5.16-5.20 show the experiment waveforms of designed LLC converter operating at rated power (1 kW). The switching frequency is always regulated to be equal to the primary resonant frequency (200.7 kHz).

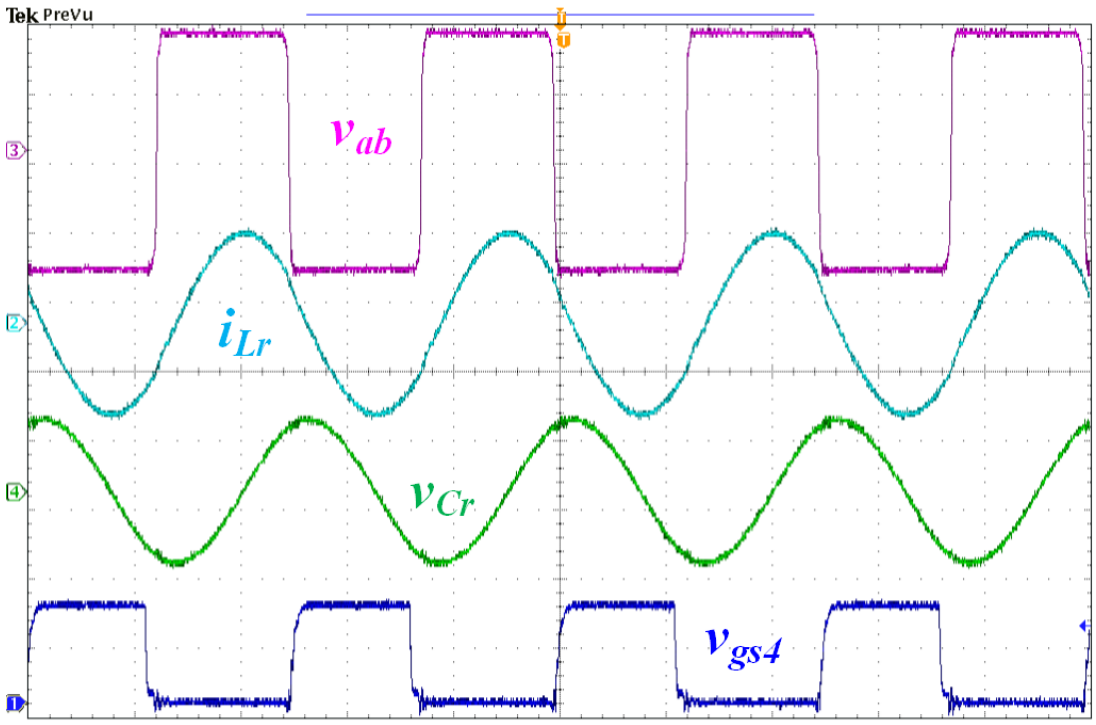



Fig. 5.16. Experiment result of LLC converter operating at rated power ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A). From top to bottom: $v_{ab}$ (200V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (200V/div), $v_{gs4}$ (10V/div), and time (2μs/div).

Fig. 5.16 shows the experimental waveforms of output voltage of full bridge inverter, $v_{ab}$, resonant inductor current $i_{Lr}$, resonant capacitor voltage $v_{Cr}$, and gate source voltage of $S_4$, $v_{gs4}$. Polarities and directions of voltage and current are denoted in Fig. 5.1. As shown in Fig. 5.16, both $i_{Lr}$ and $v_{Cr}$ are close to pure sinusoidal wave, which validates that the converter is operating at the primary resonant frequency. $i_{Lr}$ leads $v_{Cr}$, which validates that the converter is operating at inductive region.

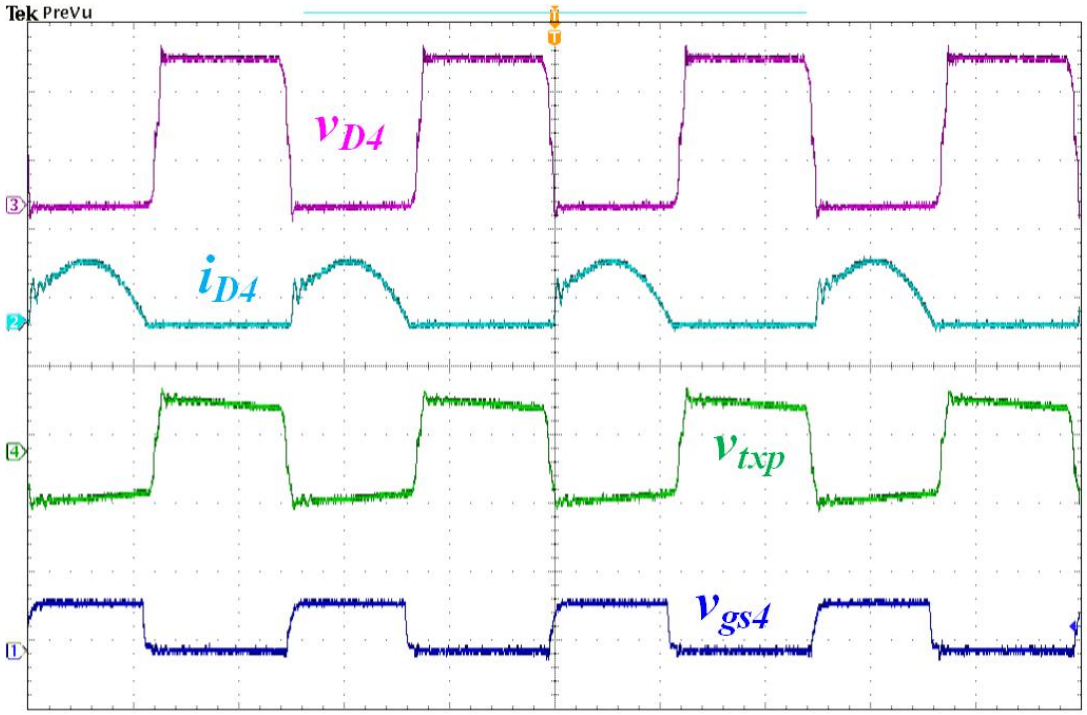



Fig. 5.17. ZCS operation of secondary diode at rated power ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A). From top to bottom: $v_{D4}$ (200V/div), $i_{D4}$ (4A/div), $v_{txp}$ (500V/div), $v_{gs4}$ (20V/div), and time (2μs/div).

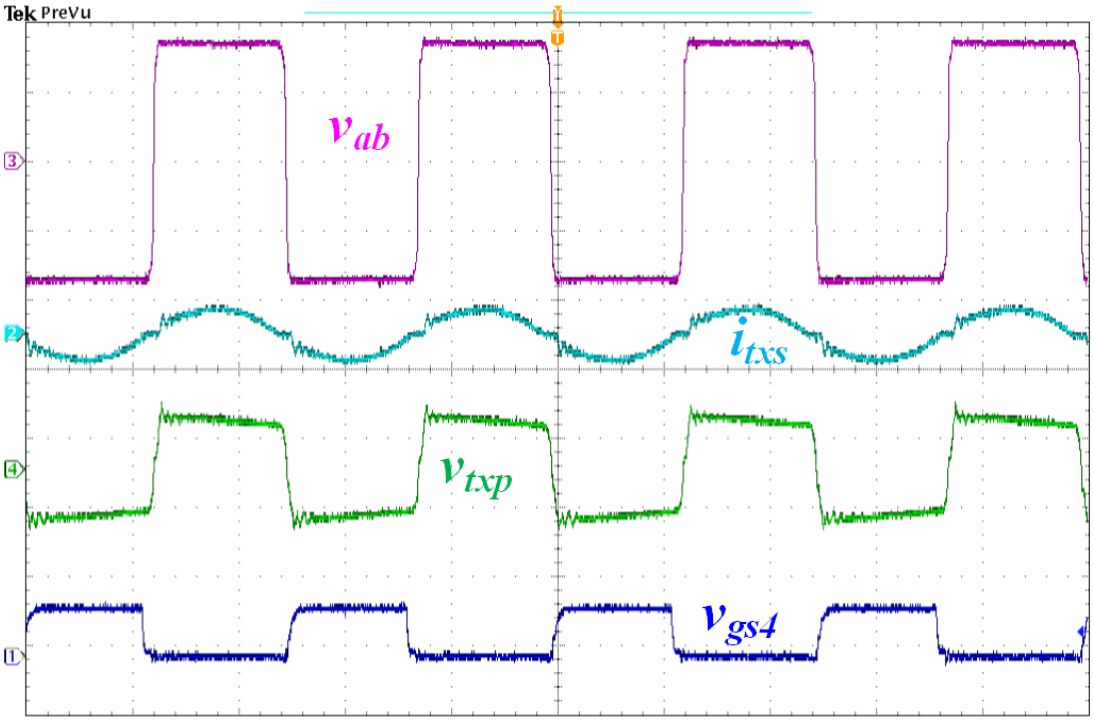



Fig. 5.18. Transformer secondary current at rated point ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A).

From top to bottom: $v_{ab}$ (200V/div), $i_{txs}$ (10A/div), $v_{txp}$ (500V/div), $v_{gs4}$ (20V/div), and time (2μs/div).

Fig. 5.17 demonstrates the ZCS turning-off of the secondary diodes. Waveforms of the cathode to anode voltage of $D_4$, $v_{D4}$, current of $D_4$, $i_{D4}$, primary side voltage of transformer $v_{txp}$, and gate source voltage of $S_4$, $v_{gs4}$, are recorded. As shown in Fig. 5.17, $D_4$ turns off when $i_{D4}$ reaches zero with low d$i$/d$t$. This shows that the reverse recovery of secondary diode is minimized.

Fig. 5.18 demonstrates the waveforms of $v_{ab}$, transformer *secondary* current, $i_{txs}$, $v_{txp}$, and $v_{gs4}$. As shown in Fig. 5.18, $i_{txs}$ is continuous; $v_{ab}$, and $v_{txp}$ are both square wave and in phase; which validate that: (a) the converter is operating at continuous conduction mode in the boundary condition between ZVS Region 1 and ZVS Region 2, and (b) the magnetizing inductor is not participating into the resonance, so that the circulating current is minimized.

Fig. 5.19 demonstrates the ZVS operations of primary MOSFETs $S_3$ and $S_4$. As shown in Fig. 5.19, both $S_3$ and $S_4$ are turned on at zero voltage. Waveforms of the input voltage $V_{dc}$, output voltage $V_{bat}$, $i_{Lr}$, and $v_{txp}$ are recorded in Fig. 5.20. Experimental results at the other critical operating points of the battery charging (with different battery voltage and current) are presented in Section 5.8.

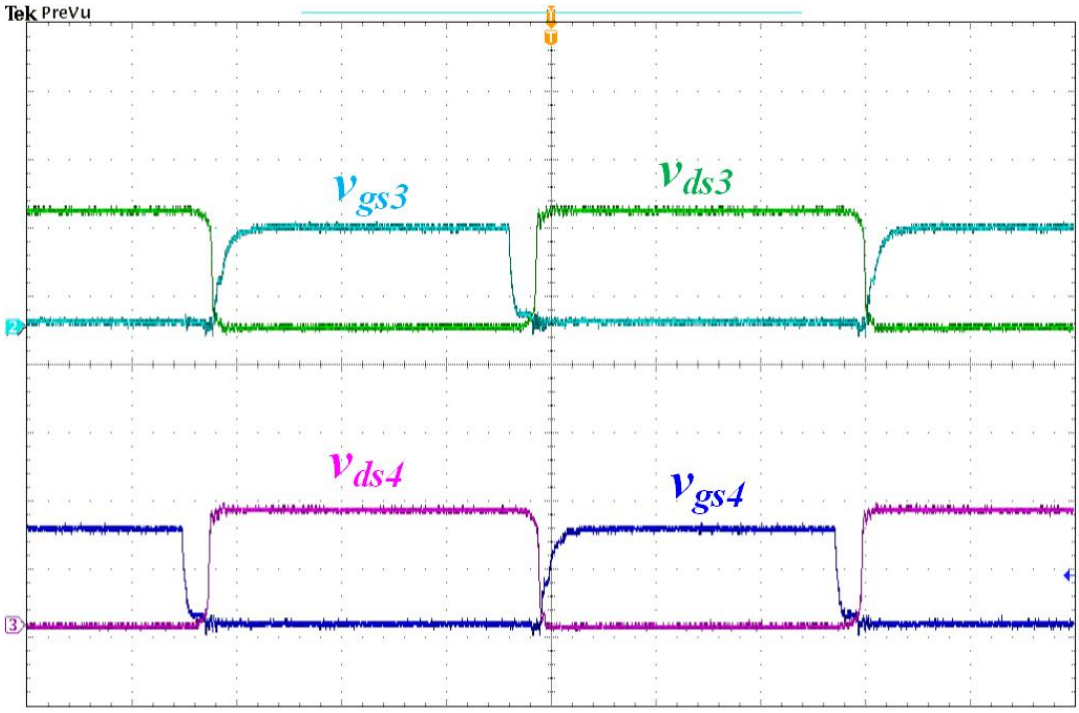



Fig. 5.19. ZVS operations of primary MOSFETs at rated power ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A). From top to bottom: $v_{ds3}$ (200V/div), $v_{gs3}$ (10V/div), $v_{ds4}$ (200V/div), $v_{gs4}$ (10V/div), and time (2μs/div)

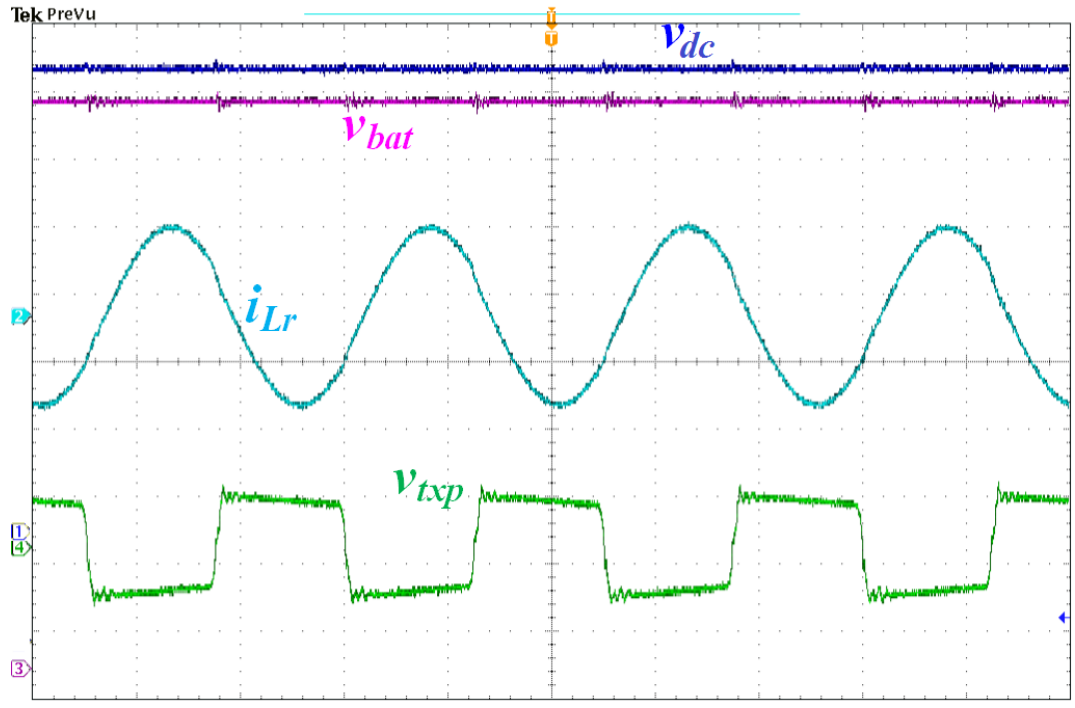



Fig. 5.20. Input voltage and output voltage waveforms at rated power ($V_{bat}$ = 420 V,

$I_{bat}$ = 2.38 A). From top to bottom: $V_{DC}$ (40V/div), $V_{bat}$ (50V/div), $i_{Lr}$ (4A/div), $v_{txp}$ (500V/div), and time (2μs/div)

## *5.8 Performance Comparison*

In order to make a comprehensive comparison, a 1 kW rated LLC charger with 390 V fixed dc link and compatible with 320 V to 420 V battery pack voltage is designed. The design parameters are summarized in Table 5-3.

Table 5-3 Design of a conventional 1 kW LLC onboard charger

| Symbol | Quantity or Device | Parameter |
|---|---|---|
| $V_{dc}$ | DC link Voltage | 390 V |
| $V_b$ | Battery voltage range | 320 V to 420 V |
| $P_{max}$ | Rated maximum power | 1 kW |
| $f_p$ | Primary resonant frequency | 200 kHz |
| $T$ | Resonant period | 5 μs |
| $C_{oss,eq}$ | Equivalent output capacitance of MOSFET | 435 pF |
| $t_{dead}$ | Deadband time | 150 ns |
| $n$ | Transformer turn ratio | 20:18 |
| $L_m$ | Magnetizing inductor | 80 μH |
| $L_r$ | Resonant inductor | 63.4 μH |
| $C_r$ | Resonant capacitor | 10 nF |
| $C_f$ | Output filter capacitor | 3×3.3 μF |

Circuit performance at the beginning point of the charging process ($V_{bat}$ = 320 V, $I_{bat}$ = 2.38 A) for both circuits is compared in Fig. 5.21. The turning off current of conventional LLC converter is 5.6 A, while the proposed LLC converter has turning off current equal to 1.9 A. This shows that switching losses are significantly reduced in the LLC converter with the proposed approach In comparison with that of the conventional fixed dc link voltage approach. Moreover, the circulating current in the proposed circuit is much smaller than that of the conventional one.

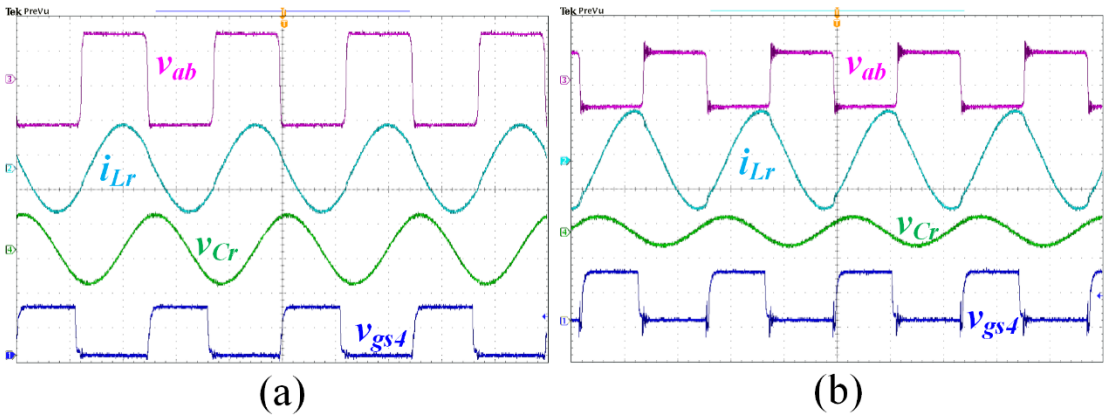



Fig. 5.21. LLC converter performance comparison at the begin point ($V_{bat}$ = 320 V, $I_{bat}$ = 2.38 A); a) proposed, from top to bottom: $v_{ab}$ (200V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (200V/div), $v_{gs4}$ (10V/div); b) conventional, from top to bottom: $v_{ab}$ (500V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (1kV/div), $v_{gs4}$ (10V/div); time (2µs/div).

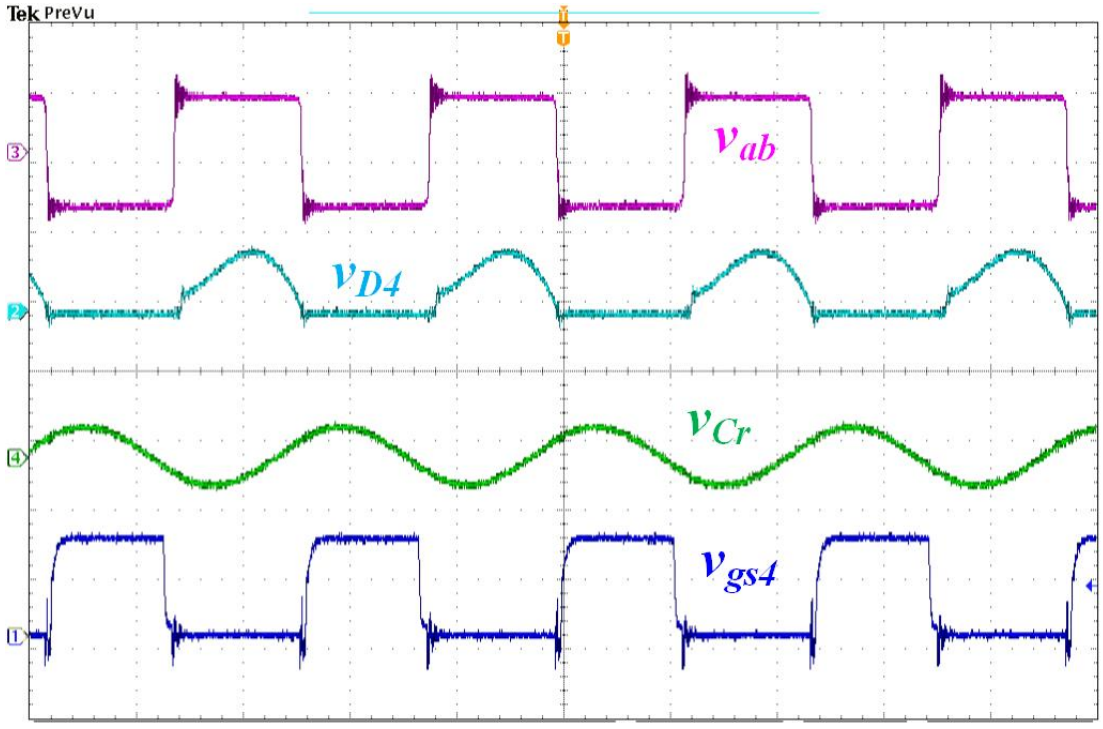



Fig. 5.22. Diode turning-off of designed converter using conventional fixed dc link voltage. ($V_{bat}$ = 320 V, $I_{bat}$ = 2.38 A); from top to bottom: $v_{ab}$ (500V/div), $i_{D4}$ (4A/div), $v_{Cr}$ (1kV/div), $v_{gs4}$ (10V/div); time (2µs/div).

The captured turning-off waveforms of $D_4$ for the conventional LLC charger with fixed dc link voltage, are given in Fig. 5.22. As seen from Fig. 5.22, $i_{D4}$ changes to zero with high d$i$/d$t$, which is an indicator of the reverse recovery losses from the secondary diodes.

Similarly, circuit performances at the nominal point ($V_{bat}$ = 360 V, $I_{bat}$ = 2.38 A), turning point ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A), and end point ($V_{bat}$ = 420 V, $I_{bat}$ = 0.238 A) are compared in figures 5.23-5.25, respectively. As shown in those figures, for each operating point, the turning off current of proposed LLC converter with dc link control is much small than that of conventional one. Similar to the previous conclusions, both the switching losses and the circulating current are greatly reduced at each operating point.

According to the loss analyses described in the previous subsection, the switching losses, conduction losses, as well as core losses are reduced over the wide SOC range of the battery pack. This conversion efficiency improvement is validated by the experiment data as plotted in Fig. 5.26.

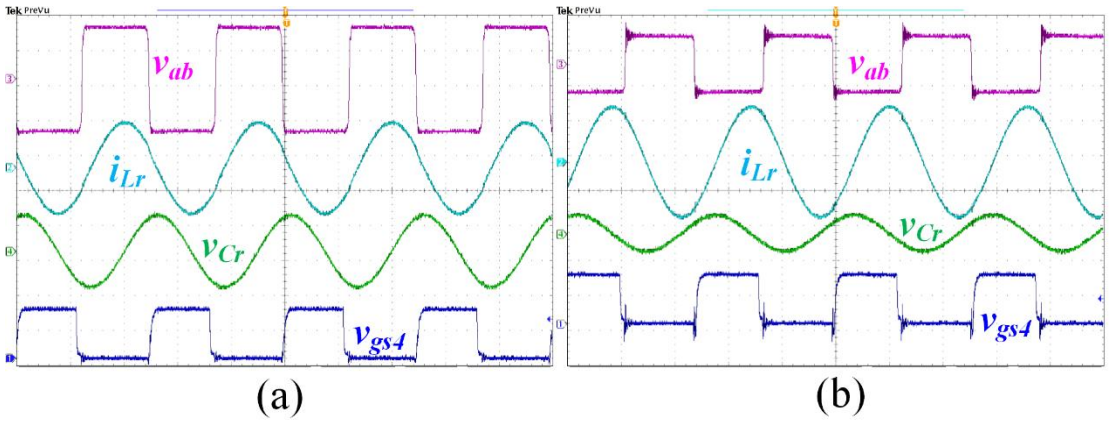



Fig. 5.23. LLC converter performance comparison at the nominal point; a) proposed;

b) conventional. ($V_{bat}$ = 360 V, $I_{bat}$ = 2.38 A); a) proposed, from top to bottom: $v_{ab}$ (200V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (200V/div), $v_{gs4}$ (10V/div); b) conventional, from top to bottom: $v_{ab}$ (500V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (1kV/div), $v_{gs4}$ (10V/div); time (2µs/div).

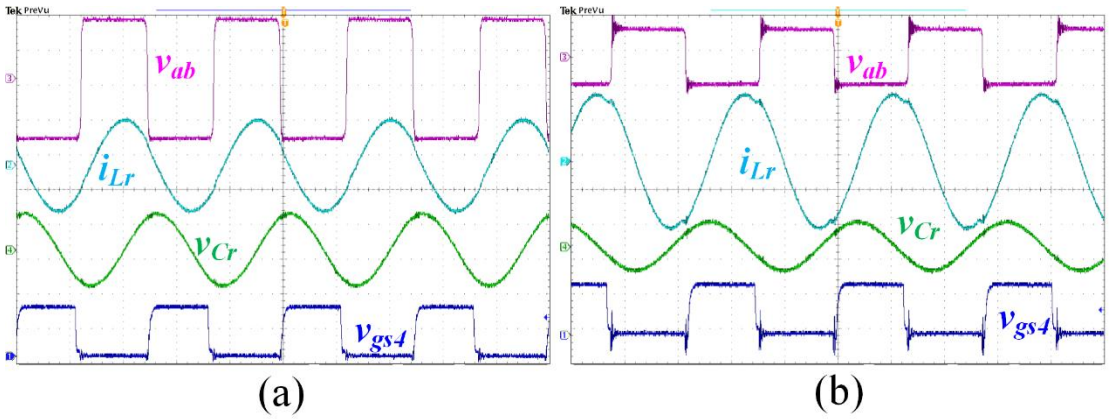



Fig. 5.24. LLC converter performance comparison at the turning point; a) proposed; b) conventional. ($V_{bat}$ = 420 V, $I_{bat}$ = 2.38 A); a) proposed, from top to bottom: $v_{ab}$ (200V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (200V/div), $v_{gs4}$ (10V/div); b) conventional, from top to bottom: $v_{ab}$ (500V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (1kV/div), $v_{gs4}$ (10V/div); time (2µs/div).

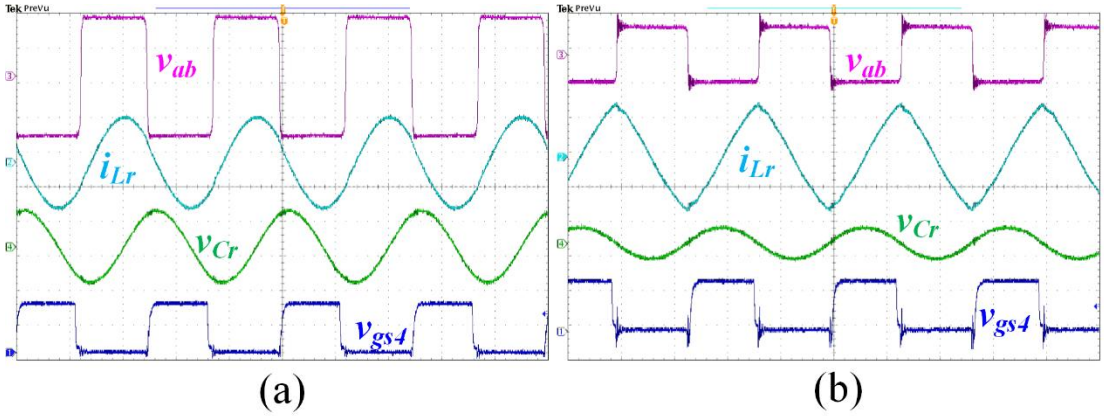



Fig. 5.25. LLC converter performance comparison at the end point; a) proposed; b) conventional. ($V_{bat}$ = 420 V, $I_{bat}$ = 0.238 A); a) proposed, from top to bottom: $v_{ab}$ (200V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (200V/div), $v_{gs4}$ (10V/div); b) conventional, from top to bottom: $v_{ab}$ (500V/div), $i_{Lr}$ (4A/div), $v_{Cr}$ (1kV/div), $v_{gs4}$ (10V/div); time (2µs/div).

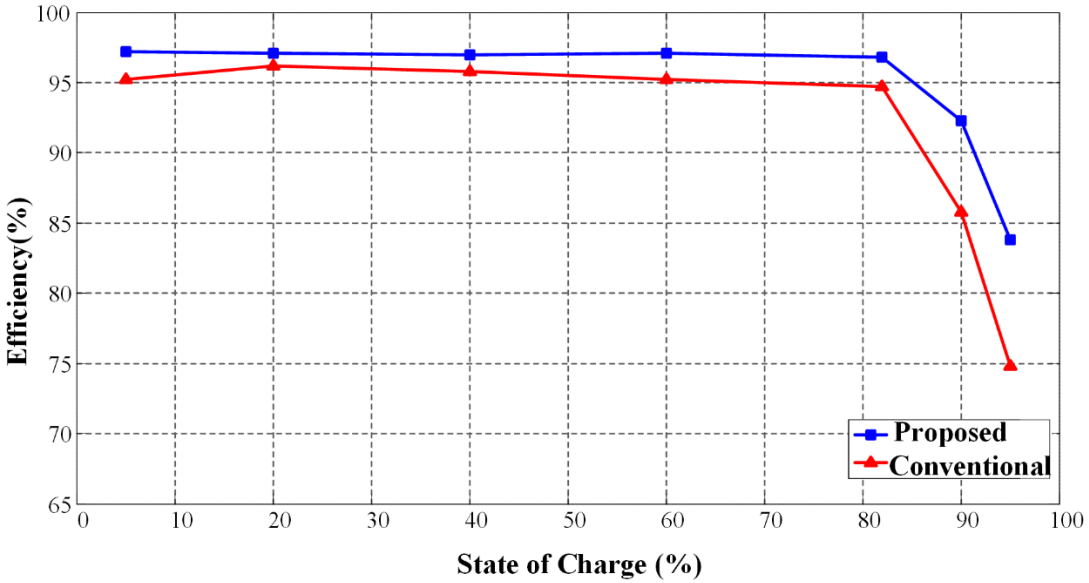



Fig. 5.26. Efficiencies of the designed LLC converters versus state of charge of battery pack.

## *5.9 Summary*

In this chapter, different isolated dc/dc topologies are investigated for PEV battery charging applications. A comprehensive comparison is made between conventional full bridge isolated PWM buck converter, full bridge phase-shift PWM converter, full bridge series resonant PFM converter, and full bridge LLC series parallel PFM converter. It is found full bridge LLC topology has the best overall performance in PEV battery charging applications.

The phenomenon of maximum efficiency point is introduced and analyzed in detail. A novel maximum efficiency point tracking technique is proposed for LLC based PEV battery chargers. With this proposed technique, dc link voltage always follows the change of battery pack voltage; which ensures that LLC converter is always operating at the primary resonant frequency.

Detail modeling and losses analysis are provided for LLC converter operating at the resonant frequency. According to the theoretical analysis, a guideline is detailed to design such an LLC converter operating at maximum efficiency point. The designed LLC converter is simulated, and the simulation results show that LLC converter is able to provide 2.5% efficiency improvement at the heaviest load condition and 8.9% efficiency improvement in the lightest load condition.

# Chapter 6 A Novel Approach to Design EV Battery Chargers Using SEPIC PFC Stage and Optimal Operating Point Tracking Technique for LLC Converter

## *6.1 Introduction*

The Li-ion batteries have dominated the battery market of electric vehicles (EVs) and plug-in electric vehicles (PHEVs). This is due to Li-ion chemistry's attractive features such as high energy density, no memory effect, and slow loss of charge. The charging profile of a typical Li-ion battery cell is plotted in Fig. 6.1. In most of the occasions, the voltage of Li-ion battery pack stays above 2.5 V/cell. Therefore, only the constant-current and constant-voltage charging strategies are discussed in most of the battery charger design literatures [112]–[115]. However, if the Li-ion battery is deeply depleted, the voltage of Li-ion battery might go down to 1 V/cell [116]. In this case, a pre-charge stage needs to be implemented to charge the battery to a pre-set voltage value. The wide voltage range of Li-ion cell is mapped to a wide voltage range (100 V – 420 V) of the onboard battery pack. Consequently, the onboard charger must be compatible with this wide voltage range [66]. However, this is not the case in majority of the chargers.

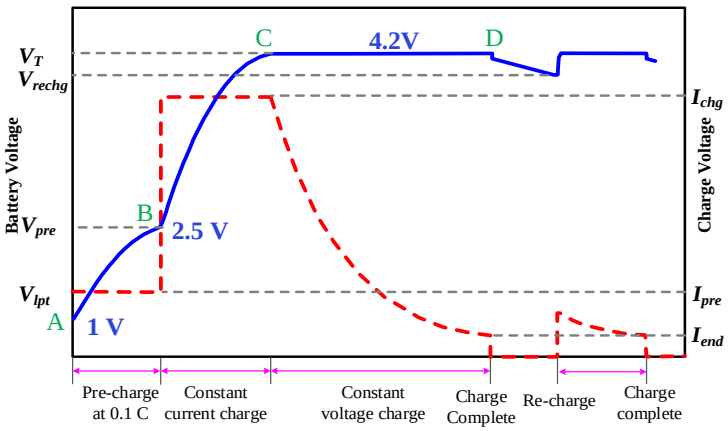



Fig. 6.1. Charging profile of Li-ion battery[116].

A typical isolated charger consists of two power converters, the front-end stage for rectification of ac input power and power factor correction (PFC), and the second-stage dc/dc converter for voltage/current regulation and galvanic isolation [3], [27], [85].

Boost and its derivative topologies are commonly utilized in the PFC stage. This is because of their simple circuit configurations, continuous input current, and low total harmonic distortion. In order to be compatible with the universal grid voltage (85 V-265 V, 47 Hz – 70 Hz), the output voltage of the boost converter (dc link voltage) is typically set to be 390 V [52], [99], [109].

In dc/dc isolation stage, zero-voltage switching (ZVS) topologies are preferable to enhance efficiency of battery chargers [65], [98], [117]. This is because the voltage stresses on the power MOSFETs are typically high. Therefore, hard-switching or zero-current switching topologies would have large switching losses and low conversion efficiency. In particular, LLC topology has several advantages over other ZVS topologies, such as (a) short circuit protection, (b) good voltage regulation

in light load condition, (c) the ability to operate with ZVS over wide load ranges , and (d) no diode reverse recovery losses through soft commutation [60]–[65].

The schematic of a conventional two stage isolated PEV battery charger based on boost PFC and full bridge LLC topologies is plotted in Fig. 6.2. In PEV battery charging applications, optimization of the LLC converter over the wide output voltage ranges becomes a challenging issue [99]–[101]. In[92][118], two recently reported LLC battery chargers have their output voltage ranges to be 320 V – 420 V and 250 V – 450 V, respectively. However, neither work is able to charge the deeply depleted battery packs (100 V - 250V).

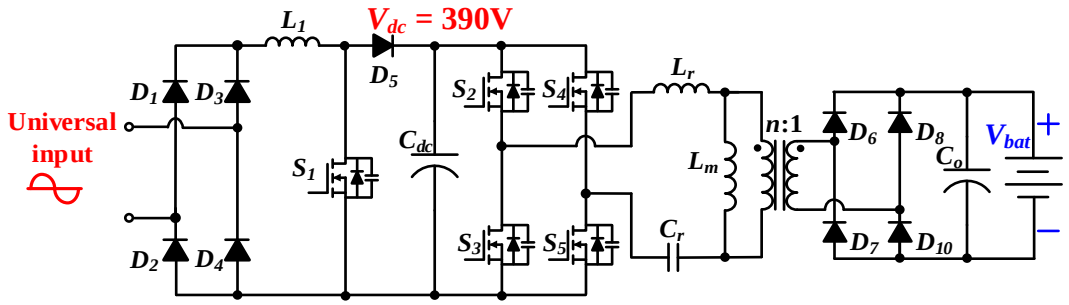



Fig. 6.2. Conventional two stage isolated charger based on boost PFC and full bridge LLC topologies.

This chapter proposes a new approach to design EV battery chargers using a single-ended primary-inductor converter (SEPIC) PFC stage and an optimal operating point tracking technique to optimize the efficiency of the LLC stage over the full battery voltage range (100 V – 420 V). The schematic of the proposed charger is plotted in Fig. 6.3. A SEPIC PFC stage is utilized. Thus, the dc link voltage can vary in a wide range without satisfying the compatibility to universal grid input. By actively controlling the dc link voltage with respect to the variation of battery voltage,

the conversion efficiency of the dc/dc converter is always regulated to be the optimal value through keeping the switching frequency close to its primary resonant frequency and thereby minimizing the circulating current in the resonant tank. With the proposed maximum efficiency point tracking technique, the efficiency performance of the dc/dc converter is improved across the wide battery voltage range. The analysis of LLC dc/dc stage has been published in [119].

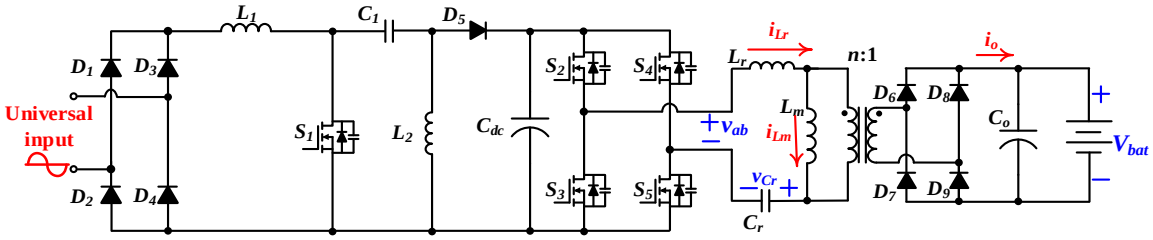



Fig. 6.3. Proposed two stage isolated charger based on SEPIC and full bridge LLC topologies.

## 6.2 *Review of SEPIC Converter*

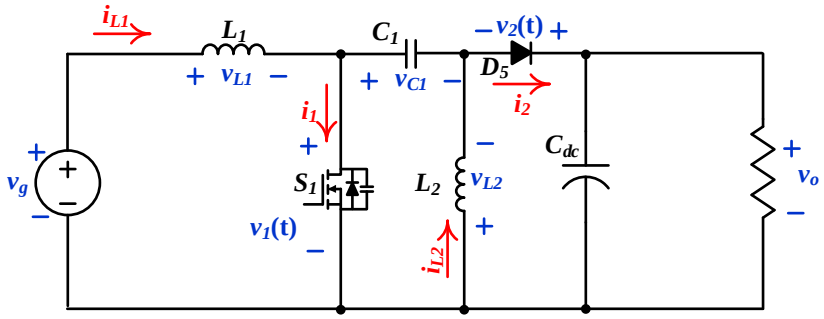



Fig. 6.4. Schematic of SEPIC converter.

Fig. 6.4 shows the schematic of a SEPIC converter. Notions of variables, symbols, and polarities are marked in Fig. 6.4. According to Kirchhoff's voltage law (KVL),

$$v_g - v_{L1} + v_{L2} = v_{C1} \tag{6.1}$$

In steady state, the voltage across the inductors ($\langle v_{L1} \rangle$ and $\langle v_{L2} \rangle$) are equal to zero. Thus, the steady state capacitor voltage is equal to the input voltage,

$$\langle v_{C1} \rangle = \langle v_g \rangle \tag{6.2}$$

If $C_1$ is large enough, accepting the accuracy of small ripple approximation, we have,

$$v_{C1} = v_g \tag{6.3}$$

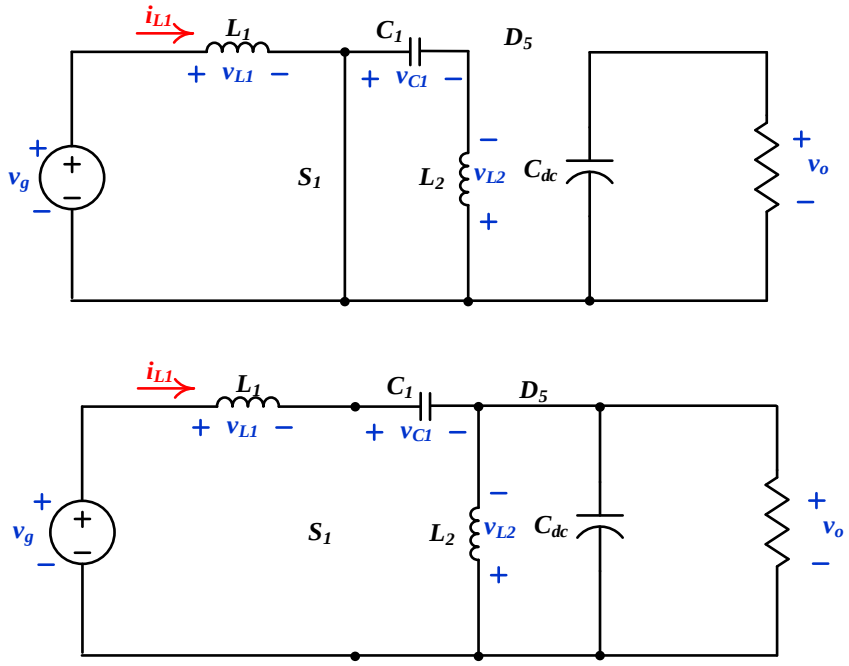



Fig. 6.5. Operation modes of SEPIC converter.

Fig. 6.5 shows the operation modes of SEPIC converter in continuous conduction mode. During (0, $dT_s$], MOSFET $S_1$ is on, and diode $D_5$ is off. Inductor $L_1$

is energized by the input source, and the capacitor $C_1$ charges the inductor $L_2$. The output capacitor $C_{dc}$ is discharged and provides power to the load. The inductor current $i_{L1}$ increases at the rate of $V_g/L_1$, as demonstrated in the equation below,

$$\frac{di_{L1}}{dt} = \frac{v_g}{L_1} \tag{6.4}$$

During ($dT_s$, $T_s$], MOSFET $S_1$ is off, and diode $D_5$ is on. Both $L_1$ and $L_2$ releases power to charge capacitors $C_1$, $C_{dc}$, and provide power to the load. According to Eq. (6.3) and KVL, the voltage across onto $L_1$ is equal to $-V_o$. Consequently, the inductor current $i_{L1}$ decreases at the rate of $-V_o/L_1$, as shown below,

$$\frac{di_{L1}}{dt} = -\frac{v_o}{L_1} \tag{6.5}$$

In steady state, the inductor current at $t = 0$ should be equal to the inductor current at $t = T$. Thus,

$$dv_g = (1-d)v_o \tag{6.6}$$

The relationship between input and output voltage for SEPIC converter can be derived as,

$$\frac{v_o}{v_g} = \frac{d}{1-d} \tag{6.7}$$

Since $d$ is within [0, 1], the voltage gain could be either larger than unity, or smaller than unity. This means, in rectifier application, the rectified output voltage

does not necessarily need to be greater than the amplitude of the grid voltage. Therefore, the SEPIC topology brings the benefit of wide dc link voltage range in the active rectifier applications.

Now, assuming $v_g$ is the rectified grid voltage, we would have

$$v_g = V_M \left|\sin(\omega t)\right| \tag{6.8}$$

where $V_M$ is the amplitude of grid voltage, $\omega$ is the angular frequency, which is typically 120π rad/s in the United States.

Neglecting the voltage ripple at the output capacitor, $v_o$ can be considered a constant equal to $V_o$. Thus, the corresponding duty cycle can be calculated as,

$$d(t) = \frac{V_o}{V_M \left|\sin \omega t\right| + V_o} \tag{6.9}$$

Eq. (6.9) describes how the duty cycle of SEPIC converter would vary in steady-state in the ac/dc power factor correction applications. The waveforms of $v_g$, $v_o$, and duty cycle $d$, versus phase angle are plotted in Fig. 6.6. According to Fig. 6.6, the varying range of duty cycle is,

$$\frac{V_o}{V_M + V_o} \le d(t) \le 1 \tag{6.10}$$

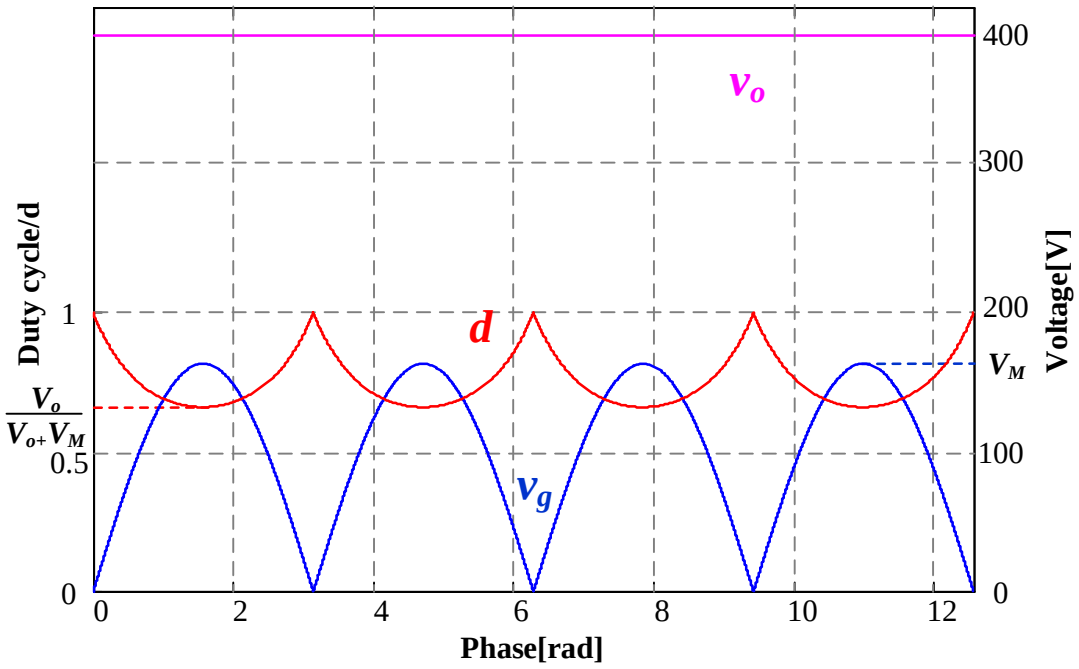



Fig. 6.6. Duty cycle of SEPIC converter in PFC application.

## *6.3 Circuit Modeling*

### 6.3.1 Small Signal Modeling

Derivation of the small signal model is based on the circuit averaging technique [37]. Based on the assumption that the frequency of the small signal perturbations are much smaller than the switching frequency of the converter, the currents and voltages are able to be averaged over one switching period.

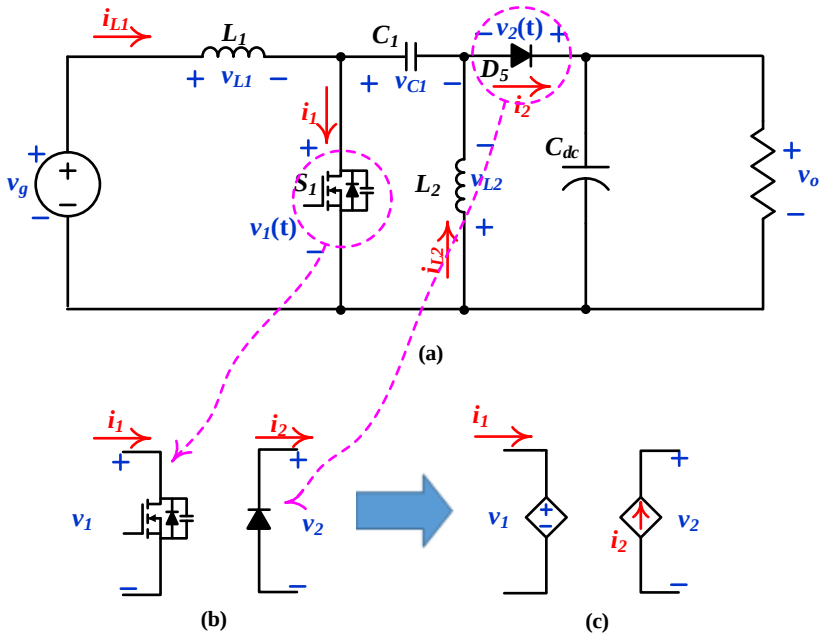



Fig. 6.7. Averaged switch model of SEPIC converter.

The switch network (MOSFT and diode) can be extracted from the circuit schematic as shown in Fig. 6.7. The MOSFT can be symbolized as a controlled voltage source, and the diode can be symbolized as a controlled current source. In order to analyze the steady-state operation of the circuit, internal series resistances of passive components and diode forward voltage drop are not taken into account for convenience in analysis. During (0, $dT_s$], $S_1$ is on while $D_5$ is off. Thus, MOSFET drain source voltage ($v_1$) is 0, while the diode reverse bias voltage ($v_2$) is $v_{C1}+V_o$. MOSFET drain source current ($i_1$) is $i_{L1} + i_{L2}$, while the diode forward current ($i_2$) is 0. During ($dT_s$, $T_s$], $S_1$ is off while $D_5$ is on. Thus, $v_1$ is $v_{C1}+V_o$, while the $v_2$ is 0. $i_1$ is 0, while $i_2$ is $i_{L1} + i_{L2}$. Thus, over one switching period, the averaged currents and voltages of the two terminal network could be derived as,

$$\langle v_1 \rangle_{Ts} = d' \left[ \langle v_{C1} \rangle_{Ts} + \langle v_o \rangle_{Ts} \right] \tag{6.11}$$

$$\langle i_1 \rangle_{Ts} = d\left[\langle i_{L1} \rangle_{Ts} + \langle i_{L2} \rangle_{Ts}\right] \tag{6.12}$$

$$\langle v_2 \rangle_{Ts} = d\left[\langle v_o \rangle_{Ts} + \langle v_{C1} \rangle_{Ts}\right] \tag{6.13}$$

$$\langle i_2 \rangle_{Ts} = d'\left[\langle i_{L1} \rangle_{Ts} + \langle i_{L2} \rangle_{Ts}\right] \tag{6.14}$$

where, $T_s$ is the switching period; $\langle x \rangle_{Ts}$ is the mean value of variable $x$ over one switching period $T_s$.

According to equations (6.11-6.14), it can be found that $\langle v_1 \rangle_{Ts} / \langle v_2 \rangle_{Ts} = d'/d$, $\langle i_1 \rangle_{Ts} / \langle i_2 \rangle_{Ts} = d/d'$. Thus, the two terminal network is able to be equivalent to be a dc transformer, as shown in Fig. 6.8. The turns ratio of the transformer is *d'*:*d*.

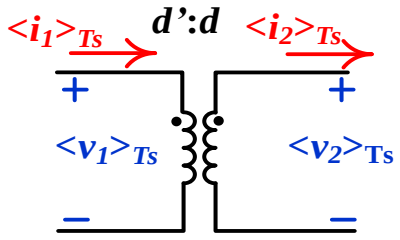



Fig. 6.8. Averaged dc model of the switch network.

In order to obtain the small signal ac model, the small signal perturbations must be applied. Each signal ($\langle v_1 \rangle_{Ts}$, $\langle v_2 \rangle_{Ts}$, $\langle i_1 \rangle_{Ts}$, $\langle i_2 \rangle_{Ts}$, $d$) can be expressed by its dc component, plus the ac small signal perturbation, as shown in the equation below.

$$\langle x \rangle_{Ts} = X + x \tag{6.15}$$

Inserting Eq. (6.15) into equations (6.11-6.14), and neglecting both the dc and second order components, the linearized ac signal is able to be extracted. The electric characteristics of the small signal model are demonstrated by the two equations below,

$$\hat{v}_1 = \frac{D'}{D}\hat{v}_2 - \left(\frac{V_1}{DD'}\right)d \tag{6.16}$$

$$\hat{i}_2 = \frac{D'}{D}\hat{i}_1 - \left(\frac{I_2}{DD'}\right)d \tag{6.17}$$

According to equations (6.16-6.17), the MOSFET can be equivalent to an independent voltage source in series with the primary side of an ideal transformer; while the diode can be equivalent to an independent current source in parallel with the secondary side of the transformer. Therefore, the small signal model of the switch network is demonstrated in Fig. 6.9.

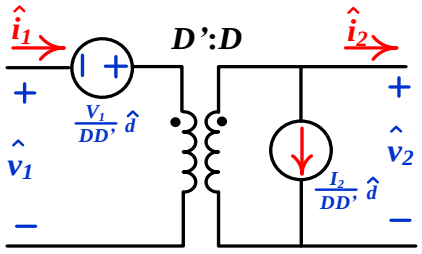



Fig. 6.9. Linearized small signal ac model of the switch network.

Inserting the small signal ac model into the SEPIC topology, the small signal model of the system can be obtained as shown in Fig. 6.10. Where $V_1$, $I_2$, and $D$, are the averaged dc values of MOSFET drain source voltage, diode current, and duty cycle, respectively. Those dc parameters vary with the operating point of the

converter. It should be noted that the derived small signal model is only applicable to the SEPIC topology operating in continuous conduction mode (CCM).

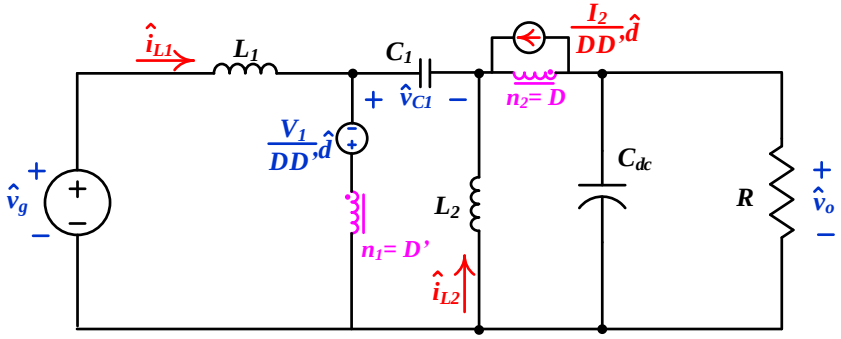



Fig. 6.10. Small signal model of SEPIC converter.

6.3.2 Current Loop Analysis

The small signal model has two independent ac sources: 1) $d$ as the control input; and 2) $\hat{v}_g$ as the line input voltage. In order to analyze the stability performance of the inner current regulation control loop, the control ($d$) to inductor current ($\hat{i}_{L1}$) transfer function ($G_{id}$) needs to be derived. In order to calculate $G_{id}$, the input voltage variations $\hat{v}_g$ should be set to zero. Thus, the modified small signal model is plotted in Fig. 6.11. The capacitance of the output filter capacitor ($C_{dc}$) is sufficiently large to be considered as short circuit in small signal analysis. The current source in Fig. 6.10 on the secondary side of transformer, $\frac{I_2}{DD'}d'$, is equivalent to the primary side, and becomes $\frac{I_2}{D'^2}d'$, as plotted in Fig. 6.11.

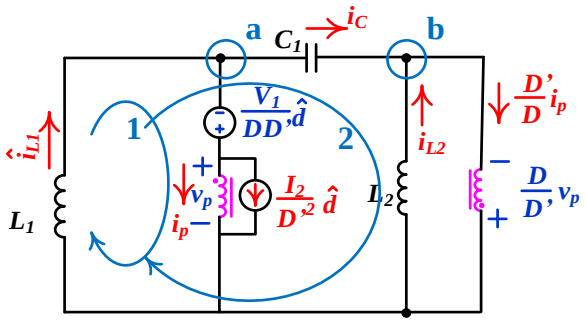



Fig. 6.11. Small signal model of SEPIC converter to calculate $G_{id}$ .

According to Fig. 6.11, applying KVL to loop 1 and loop 2, one can obtain,

$$\hat{i}_{L1}L_1 s - \frac{V_1}{DD'}d + v_p = 0 \tag{6.18}$$

$$\hat{i}_{L1}L_1 s + \frac{1}{C_1 s}i_C - \frac{D}{D'}v_p = 0 \tag{6.19}$$

where $v_p$ is the voltage applied to the primary side of the transformer.

Applying KCL to node a and node b, one can obtain that,

$$\hat{i}_{L1} - i_p - \frac{I_2}{D'^2}d - i_C = 0 \tag{6.20}$$

$$i_C + \frac{D}{D'}v_p \frac{1}{L_2 s} - \frac{D'}{D}i_p = 0 \tag{6.21}$$

where $i_p$ is the primary side current of the transformer.

Combining equations (6.18-6.21), unknowns such as $i_C$, $i_p$ and $v_p$ can be eliminated. Thus, the transfer function $G_{id}$ can be solved as,

$$G_{id} = \frac{\hat{i}_{L1}}{\hat{d}} = \frac{\frac{V_1}{D'} C_1 s^2 + I_2 s + \frac{1}{L_2} \frac{DV_1}{D'}}{C_1 L_1 s^3 + \left( D^2 \frac{L_1}{L_2} + D'^2 \right) s} \tag{6.22}$$

According to Eq. (6.22), the control to line current transfer function has three poles and two zeroes. Among those three poles, one exists in the origin point; the other two are a pair of undammed complex poles. The two zeroes are a pair of complex zeroes on the left half plane. With the change of the phase of the line, parameters in Eq. (6.22) would also change.

Based on Eq. (6.22) and the circuit parameters, which will be listed in the experimental section, the bode plot of the transfer function can be plotted. Fig. 6.12 shows the bode plot with the line phase angle equal to $\pi/2$. According to Fig. 6.12, the frequency of the pair of complex zeroes is below the frequency of the pair of complex poles. However, with the line phase angle small enough, the frequency of the pair of complex zeroes might be shifted above the frequency of the pair of complex poles. This might cause stability issues.

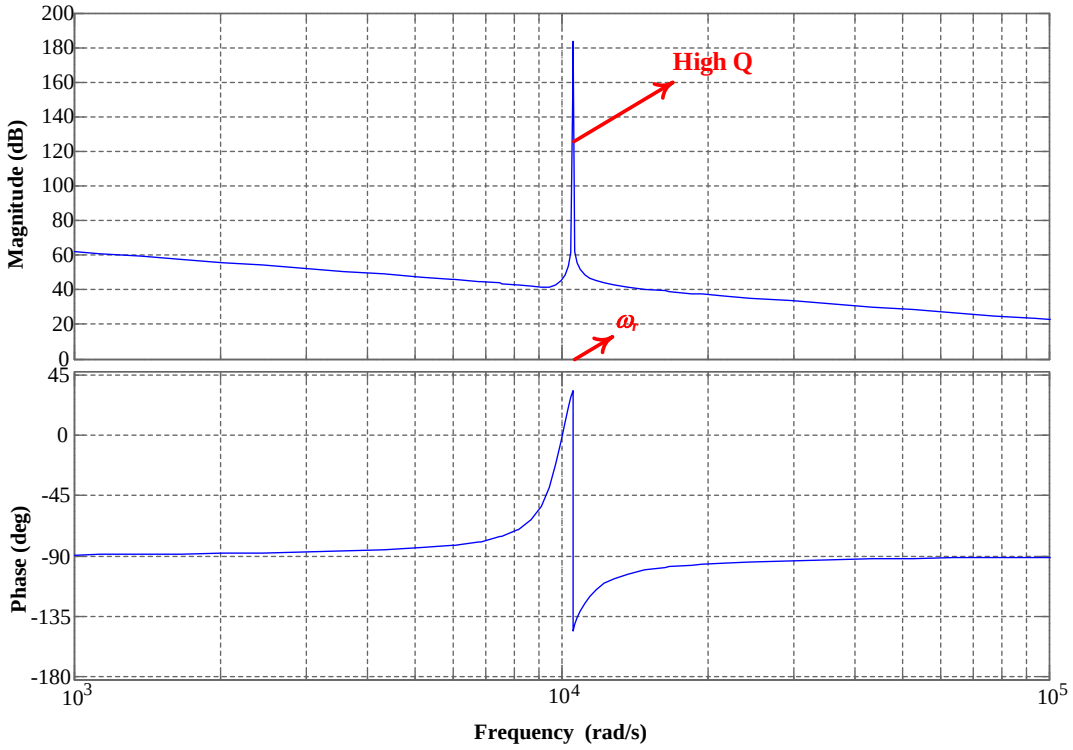



Fig. 6.12. Bode plot of $G_{id}$ with line phase angle = $\pi/2$.

$\omega_r$ is the angular corner frequency of the bode plot, and can be derived from the transfer function as,

$$\omega_r = \sqrt{\frac{D'}{L_1 C_1}} \tag{6.23}$$

At frequency $\omega_r$, there is a high magnitude spike. This means a high quality factor, $Q$, occurs at $\omega_r$, where $Q$ is a measure of the dissipation in the second order system.

It is difficult to obtain a stable system due to the high quality factor at $\omega_r$. Oscillations might occur in the input current [120]. In order to ensure the stability of

the converter, an R-C network need to be paralleled with the SEPIC capacitor, $C_1$, so that the complex poles can be damped. The modified schematic is demonstrated in Fig. 6.13.

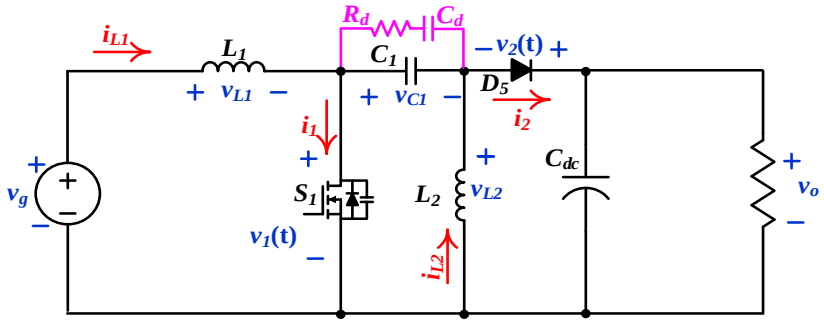



Fig. 6.13. Modified SEPIC converter with the damping R-C network.

Based on Fig. 6.13, the new control to inductor current transfer function can be derived as,

$$G_{id} = \frac{\hat{i}_{L1}}{d} = \frac{\frac{V_1}{D'}C_1C_dR_ds^3 + \left[\frac{V_1}{D'}(C_d + C_1) + I_2C_dR_d\right]s^2 + \left(I_2 + \frac{1}{L_2}\frac{DV_1}{D'}C_dR_d\right)s + \frac{1}{L_2}\frac{DV_1}{D'}}{C_1C_dR_dL_1s^4 + (C_d + C_1)L_1s^3 + \left(D^2\frac{L_1}{L_2} + D'^2\right)C_dR_ds^2 + \left(D^2\frac{L_1}{L_2} + D'^2\right)s} \tag{6.24}$$

The bode plot of the damped transfer function is plotted in Fig. 6.14. In comparison with the bode plot in Fig. 6.13, the magnitude spike at $\omega_r$ is significantly reduced. The values of $R_d$ and $C_d$ are determined by evaluating the crossover frequency and the $Q$. It should be noted that the power losses introduced by the damping network is negligible in comparison to the power level of the converter.

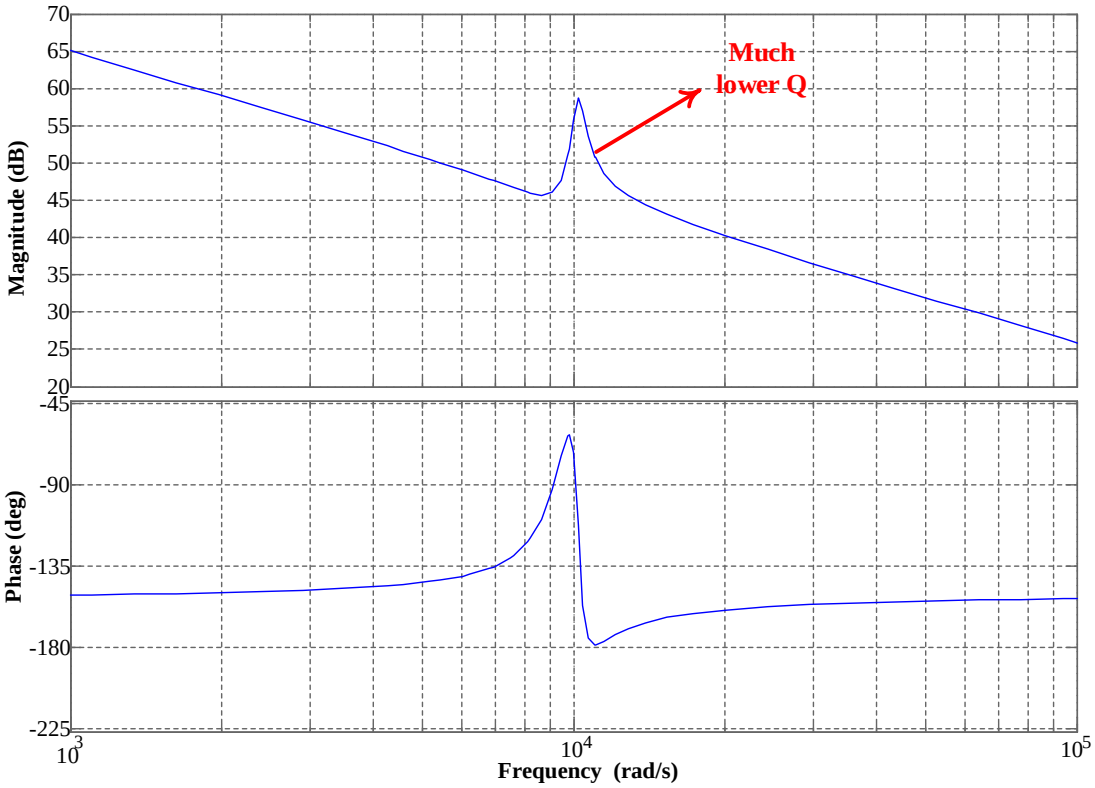



Fig. 6.14. Bode plot of $G_{id}$ with $R_d$-$C_d$ damping network (line phase angle = π/2).

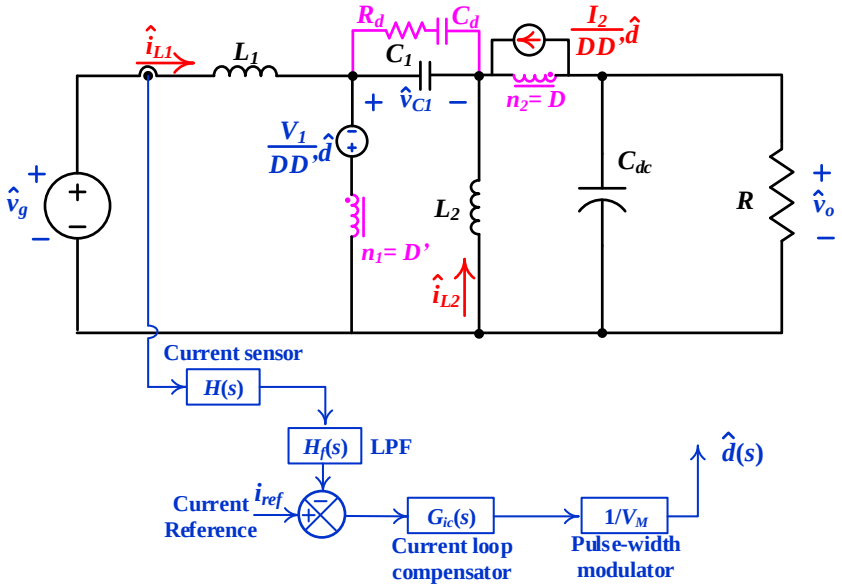



Fig. 6.15. Schematic of the current loop controller with the small-signal model.

Fig. 6.15 shows the schematic of the current control loop. In Fig. 6.15, a

current sensor is used to transduce the input inductor current signal into a voltage signal. The *s* domain transfer function of current sensor is $H_i(s)$. A low pass filter (LPF) is utilized to attenuate the high frequency switching harmonics. The *s* domain transfer function of low pass filter is $H_f(s)$. The sensed average inductor current is compared to the reference, $i_{ref}$, to generate an error signal. This error signal is compensated by the current loop compensator ($G_{ic}(s)$), and fed to the pulse-width modulator ($1/V_M$). Typically, a PI or lag compensator is utilized to ensure sufficient phase margin of the current control loop. The *s* domain loop gain can be obtained as,

$$T_i = H_i(\mathrm{s}) \times \mathrm{H}_f(\mathrm{s}) \times G_{ic}(\mathrm{s}) \times G_{id}(\mathrm{s}) / \mathrm{V}_M \tag{6.25}$$

### 6.3.3 Voltage Loop Analysis

Similarly, the control to output voltage gain can also derived. Only small signal perturbations on duty cycle and output voltage are considered. Fig. 6.16 shows the simplified ac small signal model. Since the voltage perturbation at the output node must be considered, the output capacitor can no longer be equivalent to be a short circuit.

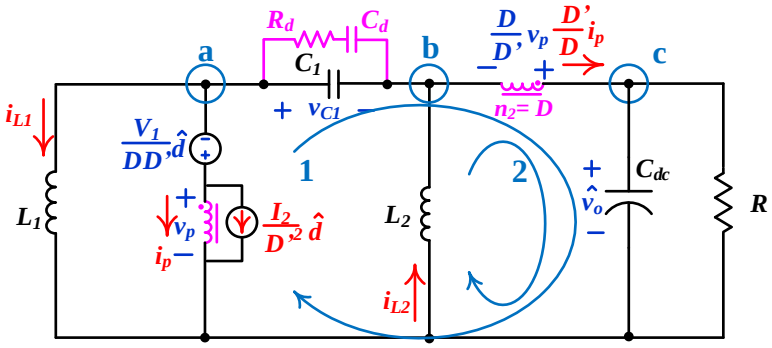


Fig. 6.16. Small signal model of SEPIC converter to calculate $G_{vd}$ .

According to Fig. 6.16, apply KVL to loop 1,

$$-v_p + \frac{V_1}{DD'}d + v_{C1} - \frac{D}{D'}v_p + \hat{v}_o = 0 \tag{6.26}$$

Apply KVL to loop 2,

$$sL_2 i_{L2} - \frac{D}{D'}v_p + \hat{v}_o = 0 \tag{6.27}$$

Apply KCL at node a,

$$i_p + \frac{I_2}{D'^2}d + \frac{v_{C1}}{Z_c} + \frac{v_p - \frac{V_1}{DD'}d}{sL_1} = 0 \tag{6.28}$$

where $Z_c$ is the impedance of the capacitor in parallel with the damping network.

Apply KCL at node b,

$$\frac{v_{C1}}{Z_c} + i_{L2} = \frac{D'}{D}i_p \tag{6.29}$$

Apply KCL at node c,

$$\frac{D'}{D}i_p - \frac{\hat{v}_o}{Z_o} = 0 \tag{6.30}$$

where $Z_o$ is the impedance of the output capacitor in parallel with the load resistor.

Combining equations (6.26-6.30), unknowns such as $v_{C1}$, $i_p$, $v_p$, and $i_{L2}$ can be eliminated. Thus, the transfer function $G_{vd}$ can be obtained as,

$$G_{vd} = \frac{\hat{v}_o}{d} = \frac{Z_o \frac{V_1}{D'} + Z_o Z_c \frac{V_1}{sL_1} + Z_o Z_c \frac{DV_1}{sL_1 D'} + Z_o \frac{V_1}{L_1 D'} L_2 - Z_o \frac{I_2}{D'^2} sL_2 - Z_o Z_c \frac{DI_2}{D'^2}}{\frac{D}{D'} sL_2 + Z_o \frac{L_2 D'}{L_1} + Z_c \frac{D^2}{D'} + Z_o D' + Z_o Z_c \frac{DD'}{sL_1} + sL_2 + Z_c \frac{L_2 D'}{L_1} + Z_o Z_c \frac{D'^2}{sL_1}} \tag{6.31}$$

where, $Z_c$ is the impedance of the SEPIC capacitor in parallel with the damping network ($R_d$ + $C_d$).

$$Z_c = \frac{C_d R_d s + 1}{C_1 C_d R_d s^2 + (C_d + C_1) s} \tag{6.32}$$

$Z_o$ is the impedance of the output capacitor parallel with the load.

$$Z_o = \frac{R}{sC_o R + 1} \tag{6.33}$$

Combining equations (31)-(33), one can obtain,

$$G_{vd} = \frac{\hat{v}_o}{d} = \frac{Num}{Den} \tag{6.34}$$

where $Num$ is the numerator of the equation,

$$
\begin{aligned}
Num = & -C_1 C_d R_d R \frac{I_2}{D'} L_1 L_2 s^4 \\
& + C_1 C_d L_1 R V_1 R_d s^3 + C_1 C_d R_d R V_1 L_2 s^3 - \left(C_d + C_1\right) R \frac{I_2}{D'} L_1 L_2 s^3 \\
& + \left(C_d + C_1\right) L_1 R V_1 s^2 - R C_d R_d L_1 \frac{D I_2}{D'} s^2 + R V_1 L_2 \left(C_d + C_1\right) s^2 \\
& + R C_d R_d V_1 s - R L_1 \frac{D I_2}{D'} s \\
& + R V_1
\end{aligned}
\tag{6.35}
$$

*Den* is the denominator of the equation,

$$
\begin{aligned}
Den = & R_d R L_1 L_2 C_o C_1 C_d D s^5 \\
& + R\left(C_d + C_1\right) C_o L_1 L_2 D s^4 + R_d C_1 C_d L_1 L_2 D s^4 \\
& + L_1 L_2 \left(C_d + C_1\right) D s^3 + R_d R L_2 C_1 C_d D'^2 s^3 + R R_d L_1 C_d C_o D^2 s^3 + R_d L_1 C_1 C_d D'^2 s^3 + R_d R L_2 C_d C_o D'^2 s^3 \\
& + R L_2 \left(C_d + C_1\right) D'^2 s^2 + R L_1 C_o D^2 s^2 + R_d L_1 C_d D^2 s^2 + L_1 \left(C_d + C_1\right) D'^2 s^2 \\
& + L_1 L_2 D' s^2 + R L_2 C_o D'^2 s^2 + R_d L_2 C_d D'^2 s^2 \\
& + L_1 D^2 s + R R_d C_d D D'^2 s + L_2 D'^2 s + R R_d C_d D'^3 s \\
& + R D'^3 + R D D'^2
\end{aligned}
\tag{6.36}
$$

The bode plot of the damped transfer function is plotted in Fig. 6.17.

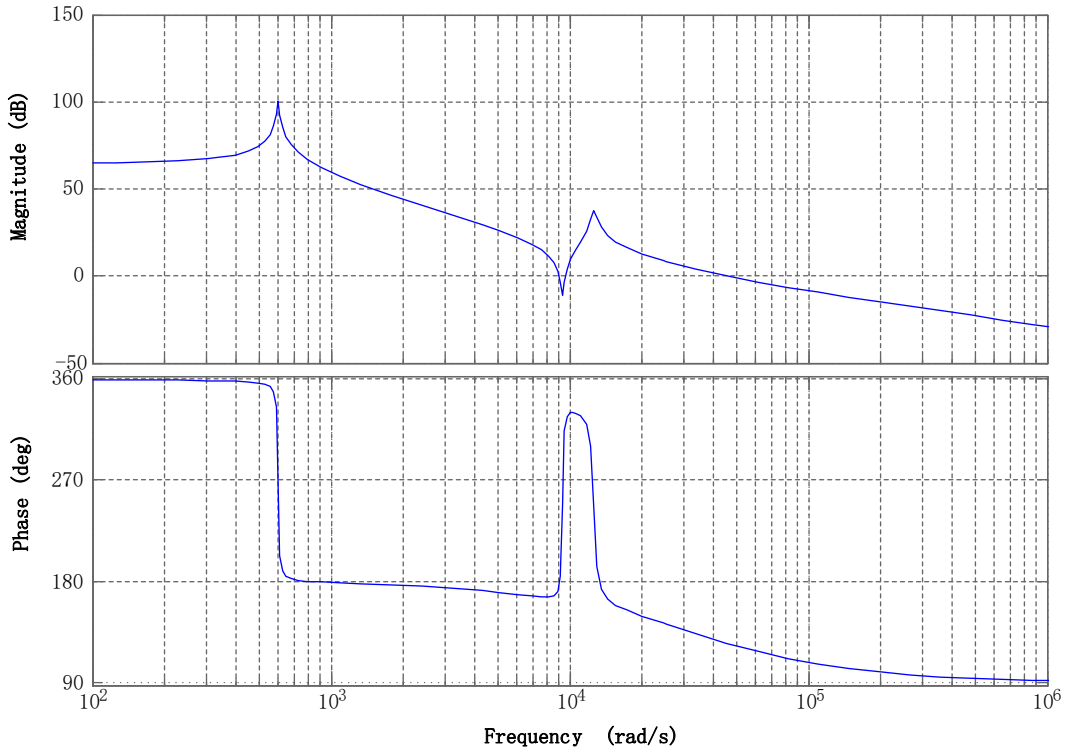



Fig. 6.17. Bode plot of $G_{vd}$ with $R_d$-$C_d$ damping network (line phase angle = π/2).

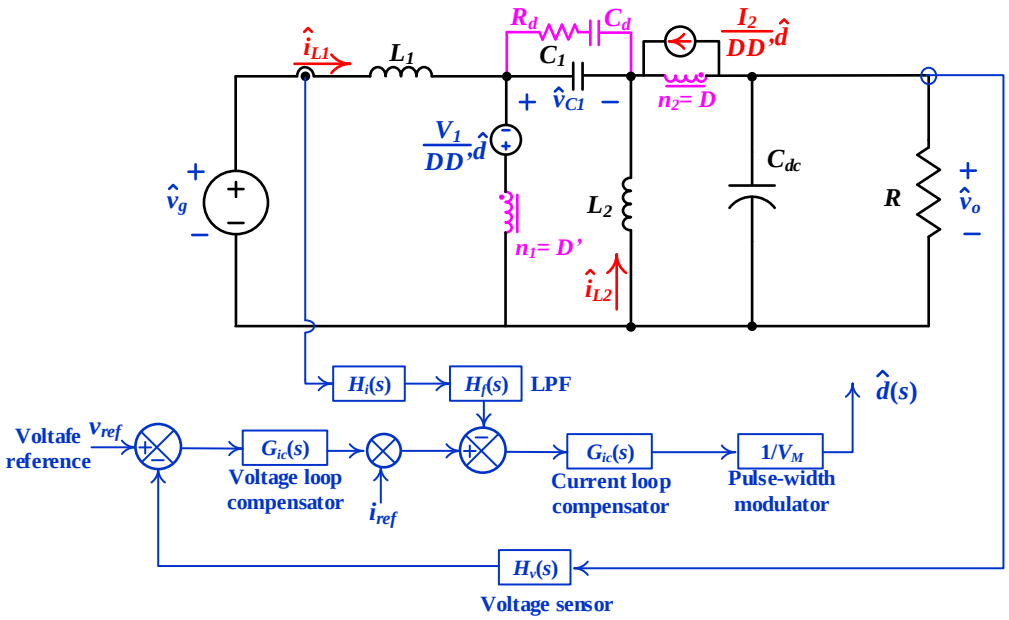



Fig. 6.18. Schematic of the voltage loop controller with the small-signal model.

Fig. 6.18 shows the schematic of the voltage control loop. In Fig. 6.18, a

voltage sensor is used to transduce the output voltage signal into an isolated scaled-down voltage signal. The *s* domain transfer function of current sensor is $H_v(s)$. The sensed voltage is compared to the reference, $v_{ref}$, to generate an error signal. This error signal is compensated by the voltage loop compensator ($G_{ic}(s)$). Output of the voltage loop compensator is multiplied by the current reference ($i_{ref}$) to generate the mixed reference signal. The sensed average inductor current signal is compared to the mixed reference to generate an error signal. This error signal is compensated by the current loop compensator, and fed to the pulse-width modulator. The *s* domain loop gain can be obtained as,

$$T_v = H_v(\mathrm{s}) \times G_{vc}(\mathrm{s}) \times G_{ic}(\mathrm{s}) \times G_{vd}(\mathrm{s}) / \mathrm{V}_M \tag{6.37}$$

## *6.4 Design Considerations*

### 6.4.1 Continuous Conduction Mode

In the PEV onboard battery charging applications, the power level of the front end ac/dc power factor correction stage is usually high. At the same power level, the current stresses of components in continuous conduction mode is much smaller than the discontinuous mode. Consequently, continuous conduction mode is preferred to discontinuous conduction mode.

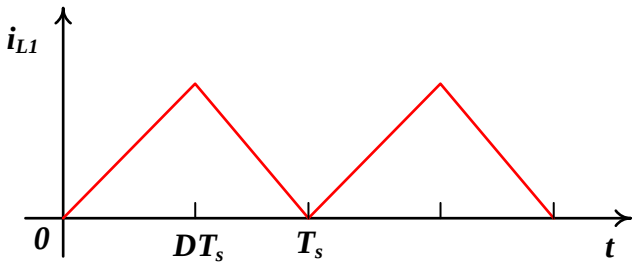



Fig. 6.19. Inductor current $i_{L1}$ at boundary conduction condition.

In the boundary conduction condition, the waveform of $i_{L1}$ is plotted in Fig. 6.19. During the time interval (0, $DT_s$], the inductor current increase at the rate of $v_g/L_{1,b}$, where $L_{1,b}$ is the boundary value of the input inductor $L_1$. The current ripple can be calculated as,

$$\Delta i_{L1} = \frac{v_g}{L_{1,b}} DT_s \tag{6.38}$$

The boundary condition happens when the current ripple is equal to twice the average input current. Thus,

$$\Delta i_{L1} = \frac{v_g}{L_{1,b}} DT_s = 2i_{in} \tag{6.39}$$

So that,

$$L_{1,b} = \frac{v_g}{2i_{in}} DT_s \tag{6.40}$$

Assuming unity power factor, the ratio of input voltage and input current would be an effective resistor. The value of the resistance is,

$$R_e = \frac{v_g}{i_{in}} = \frac{V_{rms}^{\ 2}}{P_{in}} \tag{6.41}$$

where, $V_{rms}$ is the root mean square value of the grid voltage, and $P_{in}$ is the input power.

Thus, the CCM condition for input current can be calculated as,

$$L_1 > \max\left\{\frac{R_e}{2} DT_s\right\} = \frac{V_{rms}^{\ 2}}{P_{in}} \frac{T_s}{2} \tag{6.42}$$

According to the Eq. (6.42), the smaller the switching period $T_s$ is, the more easily the converter can enter into CCM. The larger the minimum input power $P_{in,min}$ is, the more easily the converter can enter into CCM.

Similarly, the boundary conduction condition for inductor $L_2$ can be derived. The corresponding inductor current waveform is plotted in Fig. 6.20. During time interval ($DT_s$, $T_s$], the inductor current decreases at the rate of $V_o/L_2$. Thus, the current ripple can be calculated as,

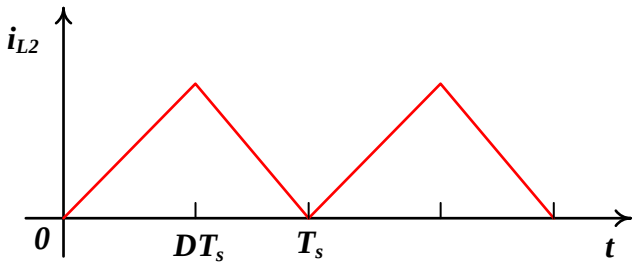



Fig. 6.20. Inductor current $i_{L2}$ at boundary conduction condition.

$$\Delta i_{L2} = \frac{V_o}{L_2} D' T_s \tag{6.43}$$

The boundary condition happens when the current ripple is equal to twice the average output current. Thus,

$$\Delta i_{L2} = \frac{V_o}{L_2} D' T_s = 2 i_o \tag{6.44}$$

So that,

$$L_{2,b} = \frac{R_L}{2} D' T_s \tag{6.45}$$

Thus, combing equations (6.9) and (6.45), the CCM condition for inductor current $i_{L2}$ can be calculated as,

$$L_2 > \max\left\{ \frac{R_L}{2} D' T_s \right\} = \frac{R_{L,\max}}{2} \frac{V_M}{V_M + V_o} T_s \tag{6.46}$$

According the Eq. (6.46), the smaller the switching period $T_s$ is, the more easily the converter can enter into CCM. The smaller the maximum value of load resistance, $R_{L,\max}$, is, the more easily the converter can enter into CCM.

### 6.4.2 Capacitor Voltage Ripple

For the SEPIC capacitor $C_1$, according to Eq. (6.2), the average voltage on $C_1$ is equal to the input voltage. This means that the line frequency voltage ripple is equal

to the amplitude of the grid voltage. Besides the line frequency voltage ripple, the switching frequency voltage ripple must be considered. The selection of $C_1$ is based on the trade-off between the requirement on low switch frequency voltage ripple and sinusoidal line frequency behavior.

The current waveform of $i_{C1}$ during two switching cycles is plotted in Fig. 6.21. During the time interval (0, $DT_s$], $C_1$ is discharged by the inductor current $i_{L2}$. The average value of $i_{L2}$ is equal to the output current $i_o$. Thus, the charge released from $C_1$ can be calculated as,

$$Q_{C1} \approx i_o DT_s \tag{6.47}$$

Consequently, the switching frequency voltage ripple on $C_1$ is,

$$\Delta v_{C1} = \frac{i_o DT_s}{C_1} \tag{6.48}$$

According to Eq. (6.48), in order to suppress the switching frequency voltage ripple on $C_1$, the switching period must be small, and a large capacitance is preferred.

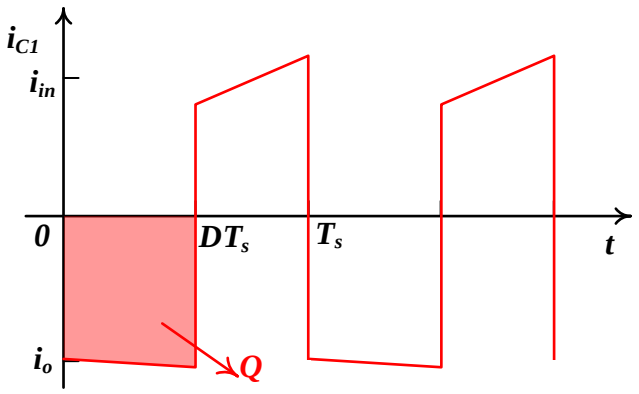


Fig. 6.22. Capacitor current $i_{C1}$ at continuous conduction mode.

With regard to the output capacitor, the switching frequency voltage ripple is negligible. This is because the output capacitance value is typically very large. Twice the line frequency voltage ripple is more critical since it directly impacts the performance of the secondary stage dc/dc converter. The low frequency voltage ripple on the output capacitor can be derived as,

$$\Delta v_o = \frac{P_{in} T_{line}}{\pi C_o V_o} \tag{6.49}$$

where, $T_{line}$ is the period of the grid input.

According to Eq. (6.49), the maximum voltage ripple happens when the input power reaches its peak point. In order to reduce the low frequency voltage ripple, a large value of output capacitor is preferred. However, this would make the electrolytic capacitor bank bulky.

## *6.5 Simulation Results*

### 6.5.1 Simulation Results of the SEPIC PFC Stage

Based on the design considerations discussed in previous subsection, a SEPIC rectifier for power factor correction stage is designed. The designed parameters are summarized in Table 7-1. In the input side, it is applicable to the universal grid. In the output side, it has wide output voltage range (100V-420V). Consequently, the secondary stage dc/dc converter can always operate at unity gain, which is the optimal operating point.

Table 6-1 Designed parameters of the SEPIC PFC rectifier

| Quantity | Symbol | Parameter |
|---|---|---|
| Input voltage | $v_{in}$ | 85V-265V, 50Hz-60 Hz |
| Output voltage | $V_{out}$ | 100V-420V |
| Rated power | $P_{max}$ | 1 kW |
| Input inductor | $L_1$ | 550 μH |
| Output inductor | $L_2$ | 550 μH |
| SEPIC capacitor | $C_1$ | 10 μF |
| Damping capacitor | $C_d$ | 1 μF |
| Damping resistor | $R_d$ | 80 Ω |
| Output capacitor | $C_o$ | 2 mF |
| Switching frequency | $f_s$ | 100 kHz |
| Sampling frequency | $f_{sample}$ | 100 kHz |

In order to verify the design, simulations are performed with parameters listed in Table 7-1. In the simulation, MOSFETs and diodes are assumed as ideal devices. Two digital PI compensators are tuned to achieve the stability of the current loop control and the voltage loop control. Fig. 6.23 demonstrates the operation of the converter at the rated power (1 kW). The input voltage is 120 V, while the output voltage is 420 V. According to Fig. 6.23, the input current follows the input voltage, which demonstrated good power factor. The power factor is measured as 0.9996. The electrical stresses on different components can be find based on the simulation result

at the rated power, so that the power components can be selected accordingly.

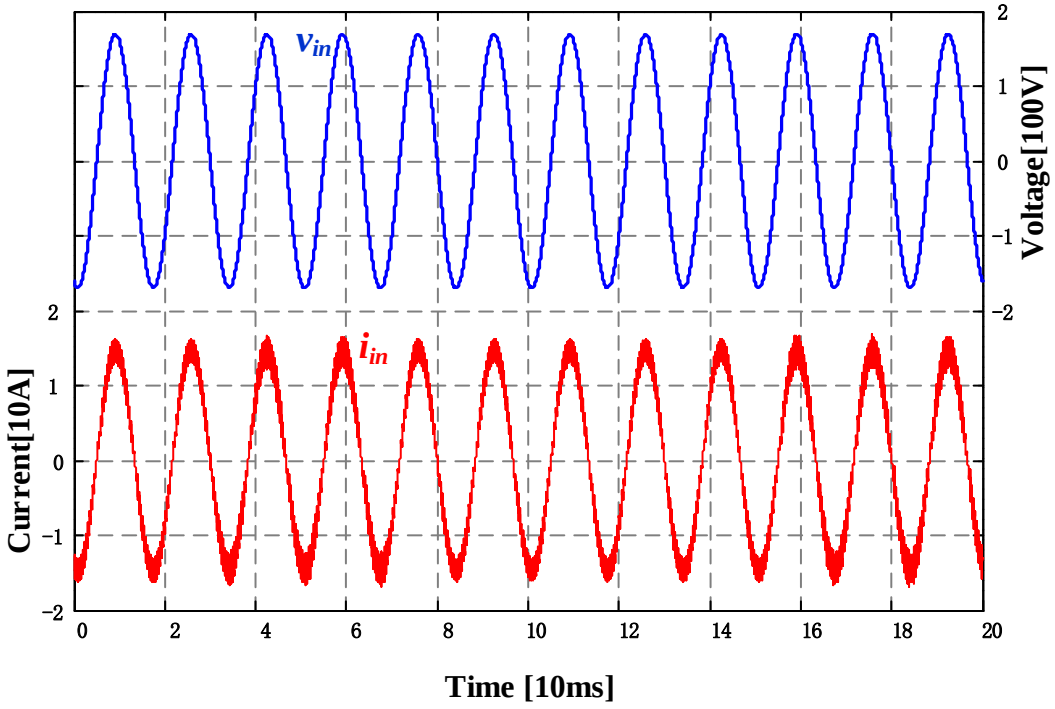



Fig. 6.23. Simulation results of the input voltage and the input current at 1 kW.

Fig. 6.24 shows the simulated waveforms of output voltage ripple, input voltage, and the input current and at the rated power with $V_{out}$ = 420 V. As can be seen in Fig. 6.24, the frequency of the voltage ripple is equal to twice the line frequency. Fig. 6.25 presents the simulated harmonics distribution from the input current. According to Fig. 6.25, the total harmonic distribution is 2.72%. Fig. 6.26 demonstrates the waveforms of input voltage as well as the voltage across the SEPIC capacitor ($v_{C1}$). As can be seen in Fig. 6.26, $v_{C1}$ is roughly equal to the absolute value of $v_{in}$, which agrees with the theatrical analysis in the previous section.

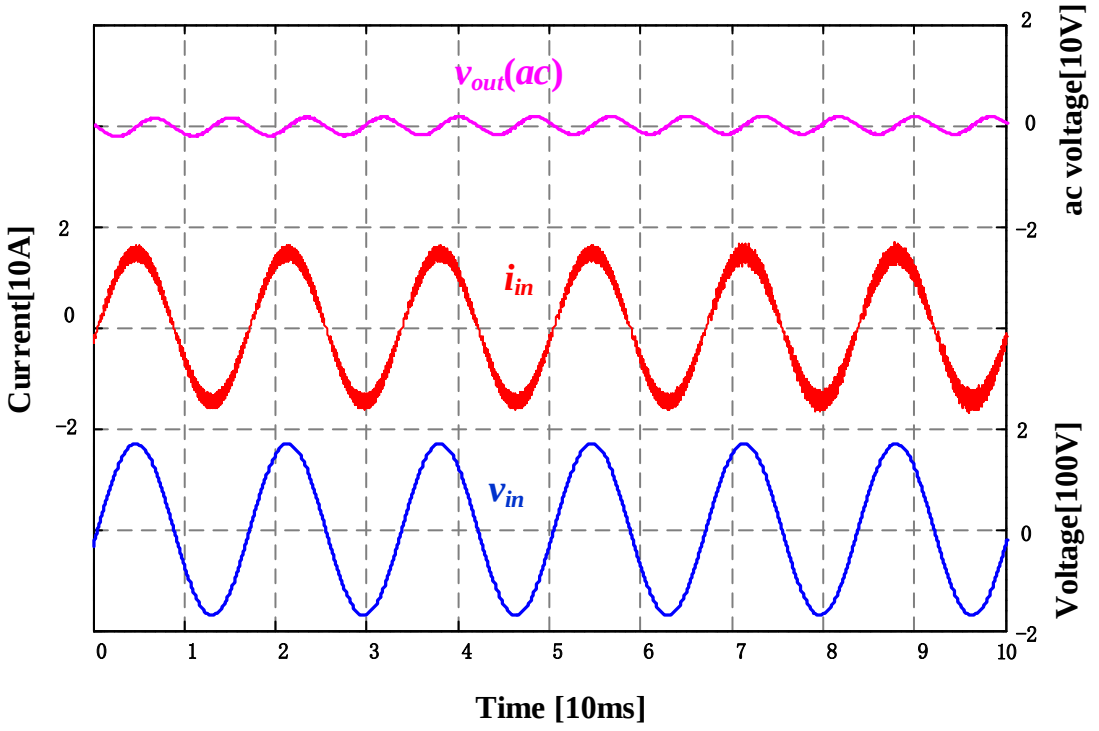



Fig. 6.24. Simulation results of the input current and output voltage ripple with $V_{out}$ =420V.

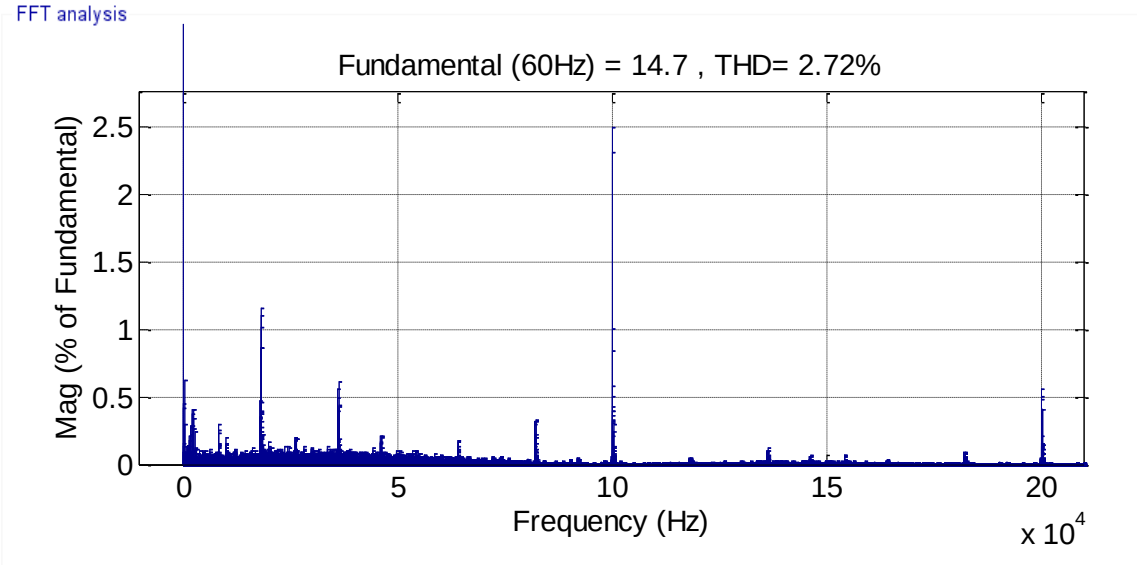



Fig. 6.25. Fast Fourier transform analysis of input current at rated power with $V_{out}$ =420V.

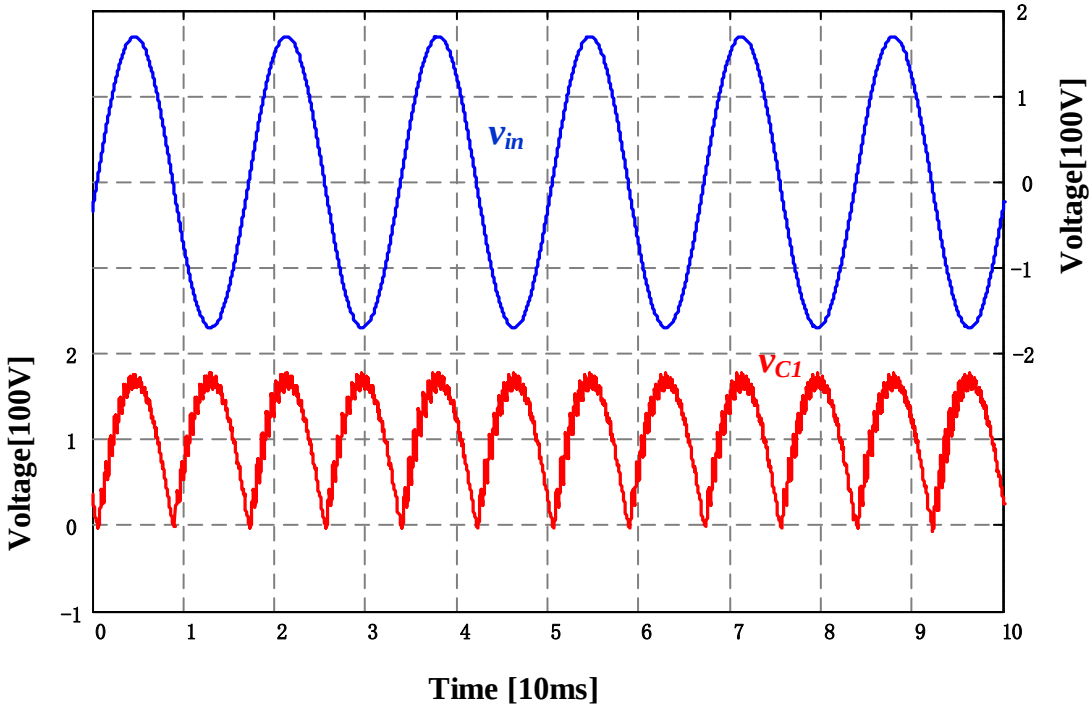



Fig. 6.26. Simulation results of the input voltage and SEPIC capacitor voltage at rated power with $V_{out}$ =420V.

Fig. 6.27 shows the simulated waveforms of input current and output voltage at the beginning of constant current charging mode, where the output voltage is 250 V, and the output power is 600 W. The power factor is measured as 0.999, and the total harmonic distortion is measured as 4.03%

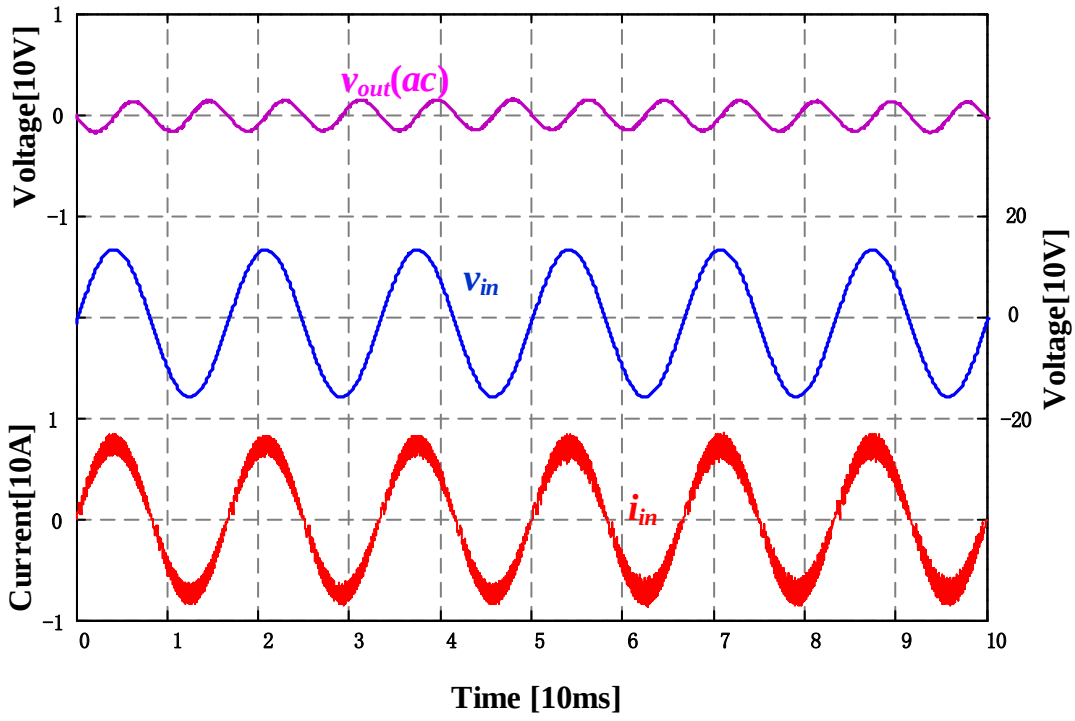



Fig. 6.27. Simulation results of the input current and output voltage at $V_{out}$ = 250V.

Fig. 6.28 shows the simulated waveforms of input current and output voltage at the pre-charge stage. The output voltage is 100 V, and the input voltage is 120 V. The power factor is measured 0.999, and the total harmonic distortion is measured as 6.79%. It should be noted that if the output power is sufficiently low, according to Eq. (6.42), the converter might enter into discontinuous conduction mode.

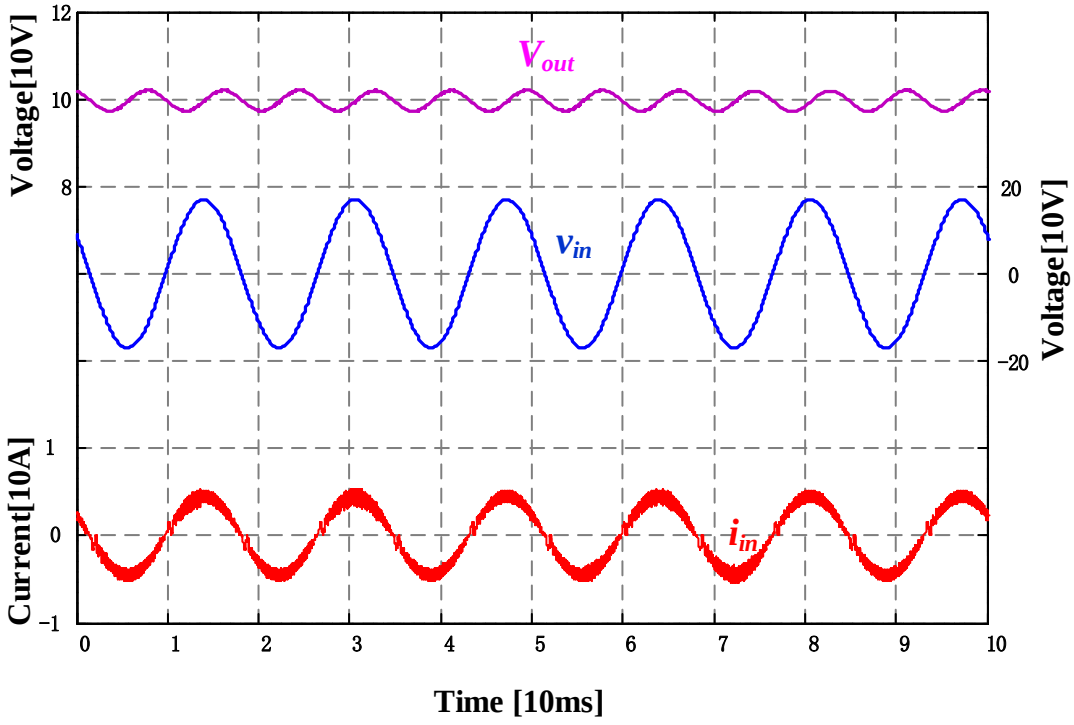



Fig. 6.28. Simulation results of the input current and output voltage at $V_{out}$ =100V.

### 6.5.2 Simulation Results of the LLC dc/dc Stage

With regards to the second stage dc/dc conversion, in order to make a comprehensive comparison, two 3.3 kW rated LLC chargers compatible with 100 V to 420 V battery pack voltage are designed. The design parameters are summarized in Fig. 6.29. Both designs have their $f_p$ equal to 200 kHz. The theoretic analysis as well as design considerations of LLC converter has been published in [121].

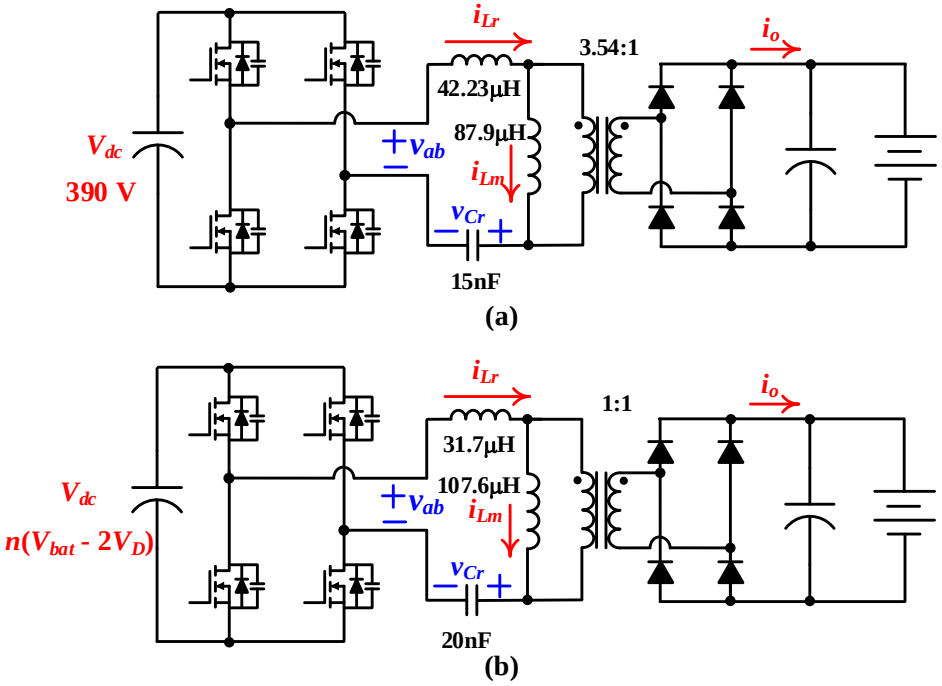



Fig. 6.29. Circuit parameters for efficiency comparison, (a) conventional fixed dc link voltage, (b) proposed variable dc link voltage.

Circuit performances at the lowest battery pack voltage (Point A in the charging profile: $V_{bat}$ = 100 V, $I_{bat}$ = 1.07 A) for both circuits are compared in Fig. 6.30; both the turning off current and circulating current are marked. According to Fig. 6.30, the turning off current of conventional LLC converter is 4.5 A, while the proposed LLC converter has turning off current equal to 1.1 A. This shows that switching losses are significantly reduced in the LLC converter with the proposed approach in comparison to that of the conventional fixed dc link voltage approach. Moreover, the circulating current in the proposed circuit is much smaller than that of the conventional one.

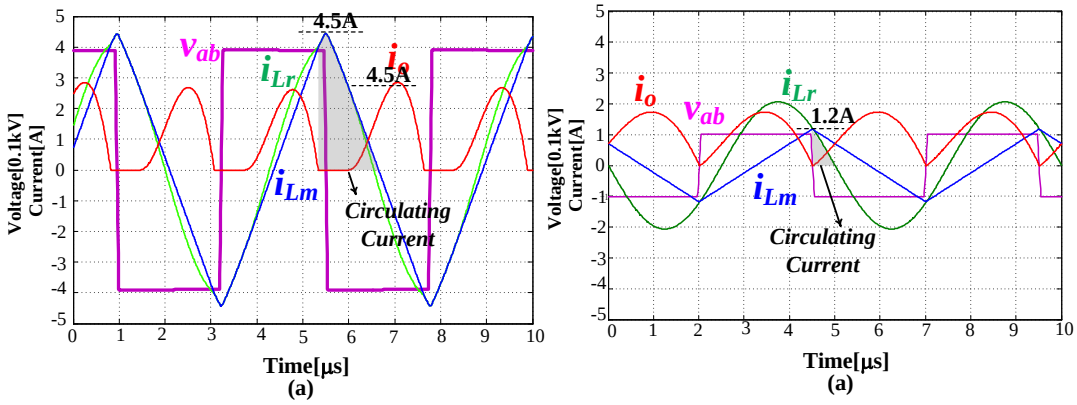



Fig. 6.30. LLC converter performance comparison at the operating point A; a) conventional; b) proposed.

Similarly, circuit performances in the beginning of constant current charging mode (Point B in the charging profile: $V_{bat}$ = 250 V, $I_{bat}$ = 7.86 A), are compared in Fig. 6.31. In comparison to conventional approach, the turning off current is reduced from 14.4 A to 2.9 A. Circulating current is significantly reduced. Moreover, the current stress on the rectifier diodes is also greatly reduced.

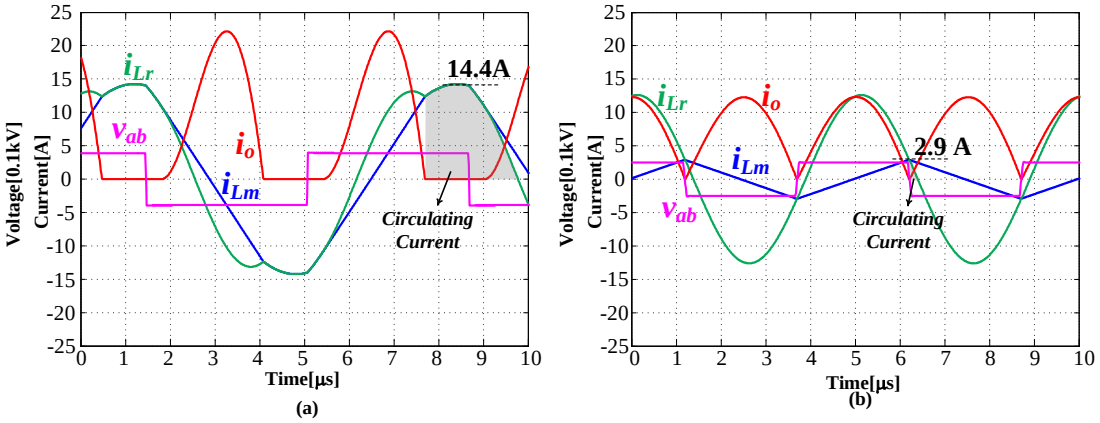



Fig. 6.31. LLC converter performance comparison at the operating point B; a) conventional; b) proposed.

Fig. 6.32 demonstrates the circuit operation at the peak power (Point C in the charging profile: $V_{bat}$ = 420 V, $I_{bat}$ = 7.86 A). In comparison to conventional

approach, the turning off current is reduced from 22.3 A to 5.1 A. Circulating current is significantly reduced. The current stress on the rectifier diodes is also greatly reduced.

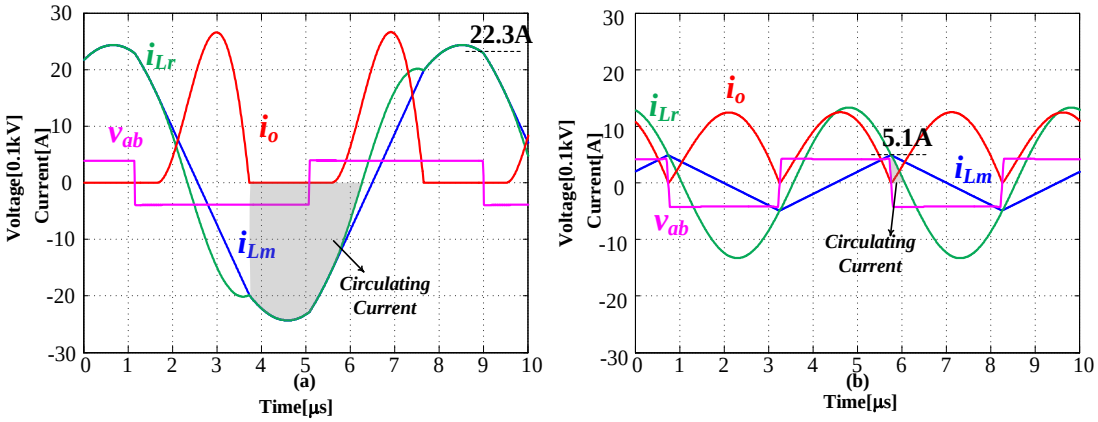



Fig. 6.32. LLC converter performance comparison at the operating point C; a) conventional; b) proposed.

Fig. 6.33 demonstrates the voltage stress on $C_r$ at the peak power (Point C in the charging profile: $V_{bat}$ = 420 V, $I_{bat}$ = 7.86 A). In comparison to conventional approach, voltage stress on $C_r$ is greatly reduced from 2.2 kV to 0.51 kV. Practically, it is unrealistic to build a single film capacitor with 2.2 kV high frequency ac voltage rating. A film capacitor bank with multiple series capacitors must be used, which makes the resonant capacitor bulky.

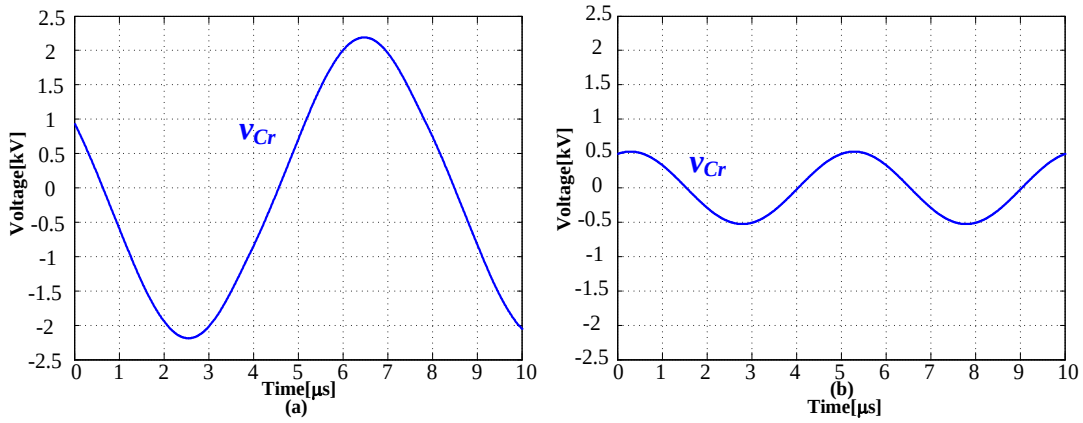


Fig. 6.33. Resonant capacitor voltage stress comparison at the operating point C; a) conventional; b) proposed.

Fig. 6.34 demonstrates the circuit operation at the lightest load (Point D in the charging profile: $V_{bat}$ = 420 V, $I_{bat}$ = 0.78 A). In comparison to conventional approach, the turning off current is reduced from 24.2 A to 4.8 A. The current stress on the rectifier diodes is also greatly reduced. For the conventional approach [see Fig. 30 (a)], although little power (327.6 W) is delivered to the battery, there is still a significant amount of circuiting current in the resonant tank. The circuiting power makes the conduction losses much higher than the power delivered.

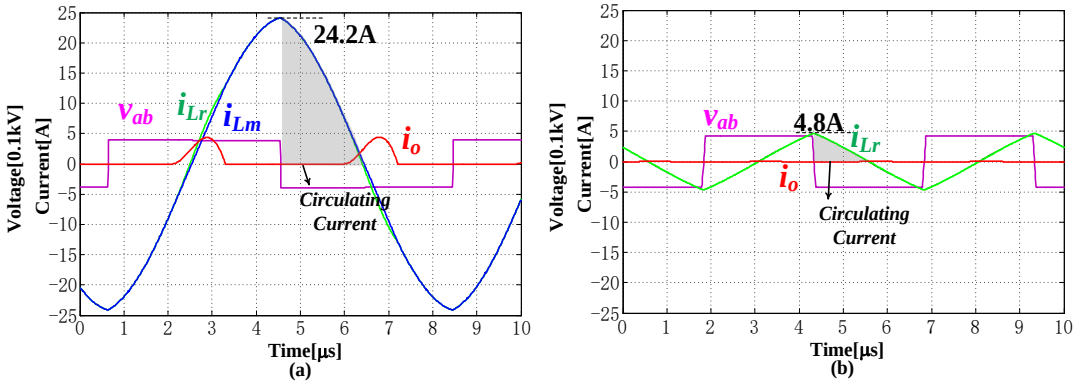



Fig. 6.34. LLC converter performance comparison at the operating point D; a) conventional; b) proposed.

## *6.6 Experiment Results*

### 6.6.1 Experiment Results of the SEPIC PFC Stage

Based on the designed parameters in Section 6.5, a laboratory prototype, with rated power of 3.3 kW is built to verify the validity of the proposed charger. Fig. 6.35 shows the picture of the ac/dc PFC power converter prototype. The system is controlled by a TMS320F28335 DSP controller, as demonstrated in Fig. 6.36. The

switching frequency is set at 100 kHz. It should be noted that both the power MOSFET and the power diode are SiC based.

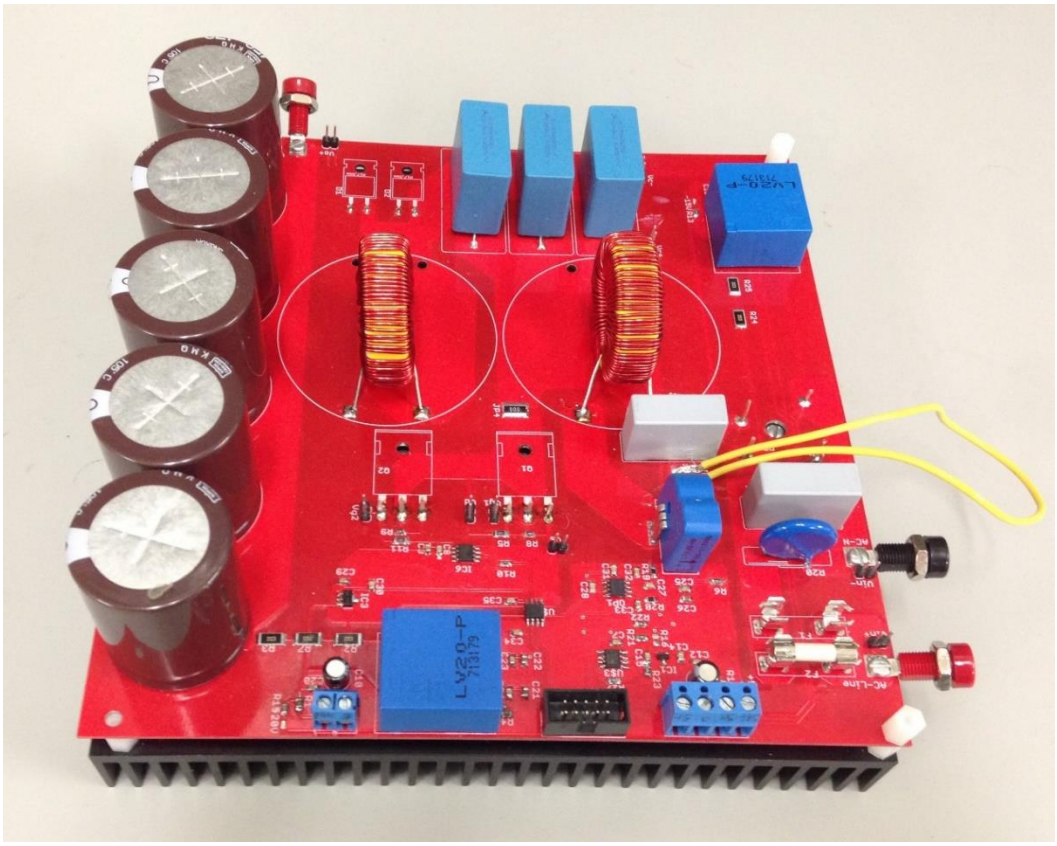


Fig. 6.35. Designed ac/dc SEPIC PFC converter prototype.

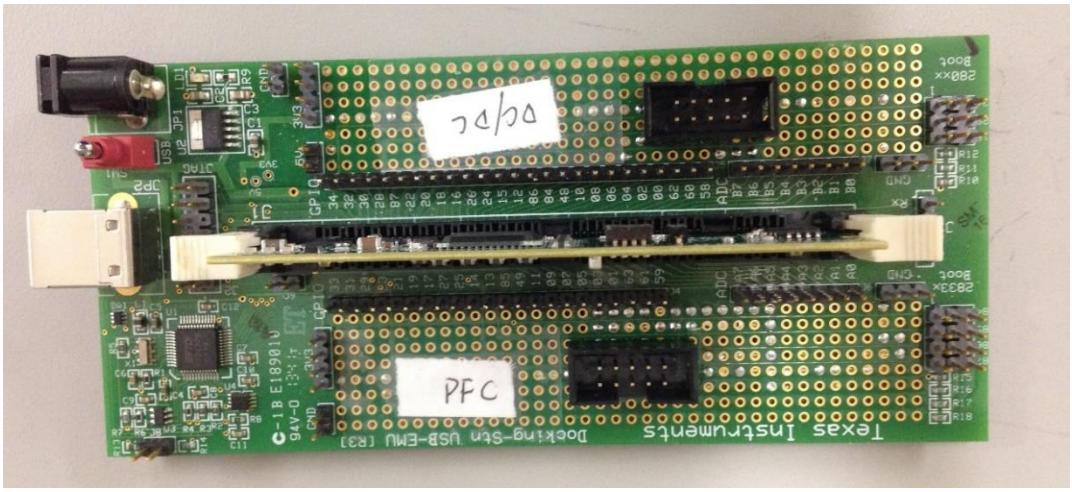


Fig. 6.36. TMS320F28335 DSP development board.

Due to the safety reasons as and power limitation in the lab facility, the designed 3.3 kW ac/dc PFC converter is tested at 1 kW. Figures 6.37-6.39 demonstrate the experimental results of the designed ac/dc PFC converter operating at 980 W. Fig. 6.37 shows the waveform of grid input voltage and input current. The dc link voltage is regulated to be 420 V, which is higher than the peak grid input voltage. As seen in the figure, the input current follows the input voltage with no phase difference. The power factor is recorded as 0.993, while the conversion efficiency is measured as 95.1%.

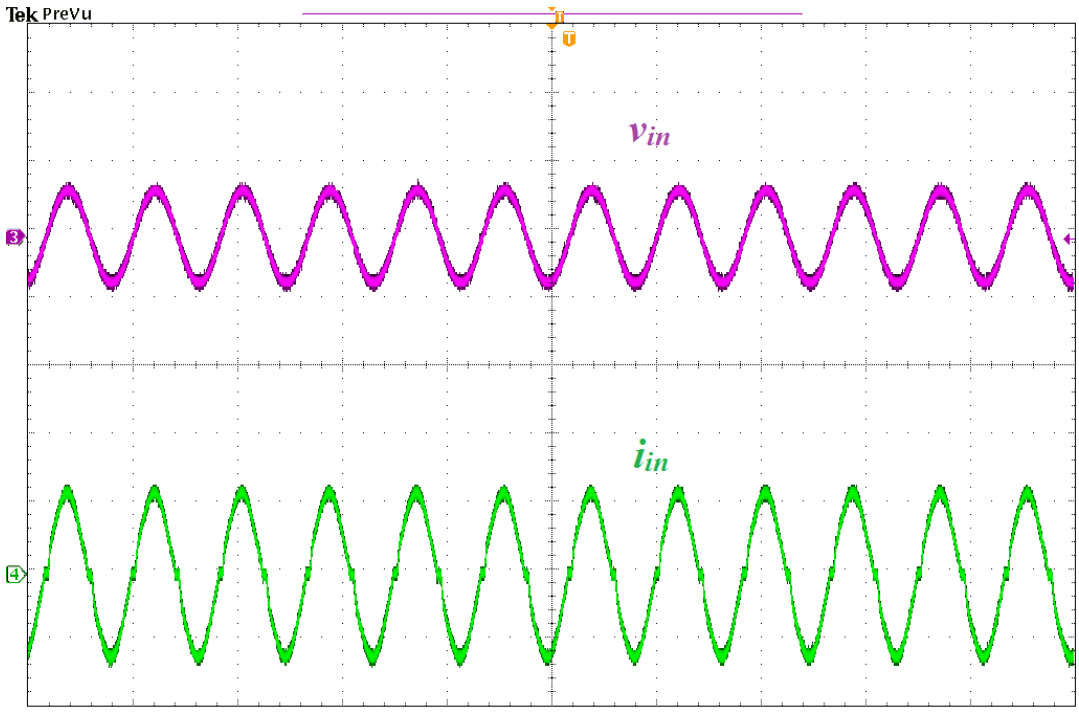



Fig. 6.37. Experimental results of the input voltage and the input current. ($V_{in}$ = 120 V, $V_{dc}$ = 420 V). From top to bottom: $v_{in}$ (250 V/div), $i_{in}$ (10 A/div), time (20 ms/div).

Fig. 6.38 shows the waveform of the dc link voltage, grid input voltage, and

the input current. Channel 1 is captures the dc link voltage in ac coupling mode. The frequency of the dc link voltage ripple is twice the grid frequency. The amplitude of the voltage ripple on the dc link voltage is well suppressed to be around 8 V.

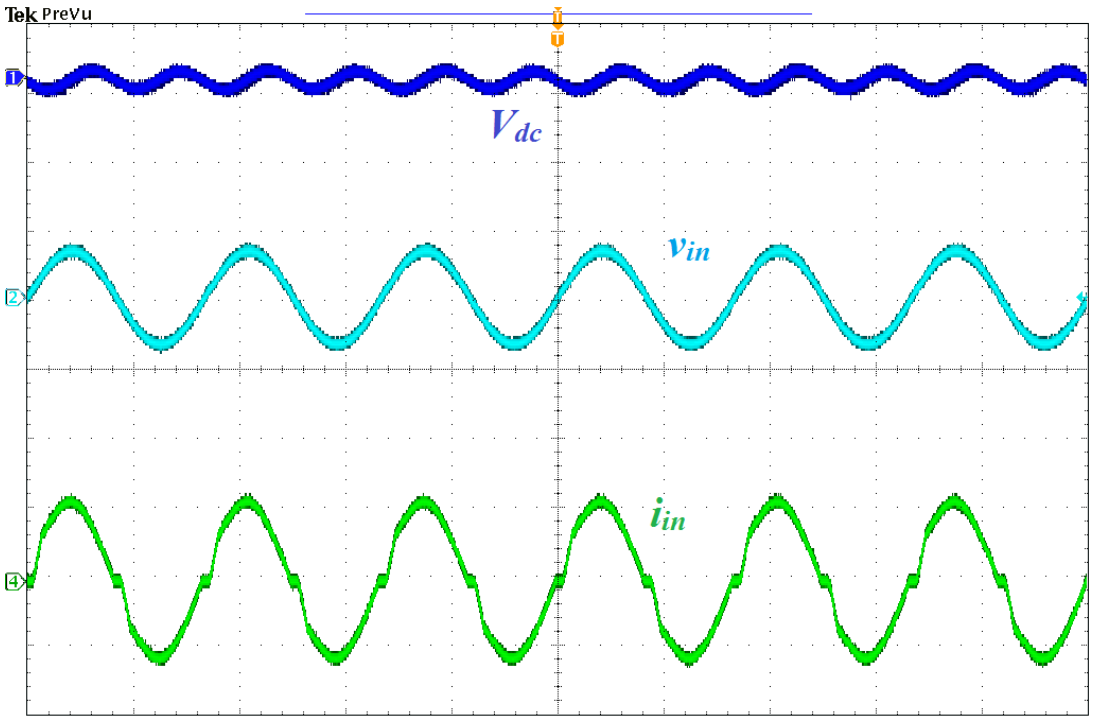



Fig. 6.38. Experimental results of the output voltage, input voltage and the input current ($V_{in}$ = 120 V, $V_{dc}$ = 420 V). From top to bottom: $V_{DC}$ (20 V/div, ac coupling), $v_{in}$(250 V/div), $i_{in}$ (10 A/div), time (10 ms/div).

Fig. 6.39 shows the experimental waveforms of input voltage and SEPIC capacitor voltage. As can been seen in the screenshot, SEPIC capacitor voltage roughly equals to the absolute value of the input voltage. This agrees with the analysis result in the previous section [see Eq. (6.2)].

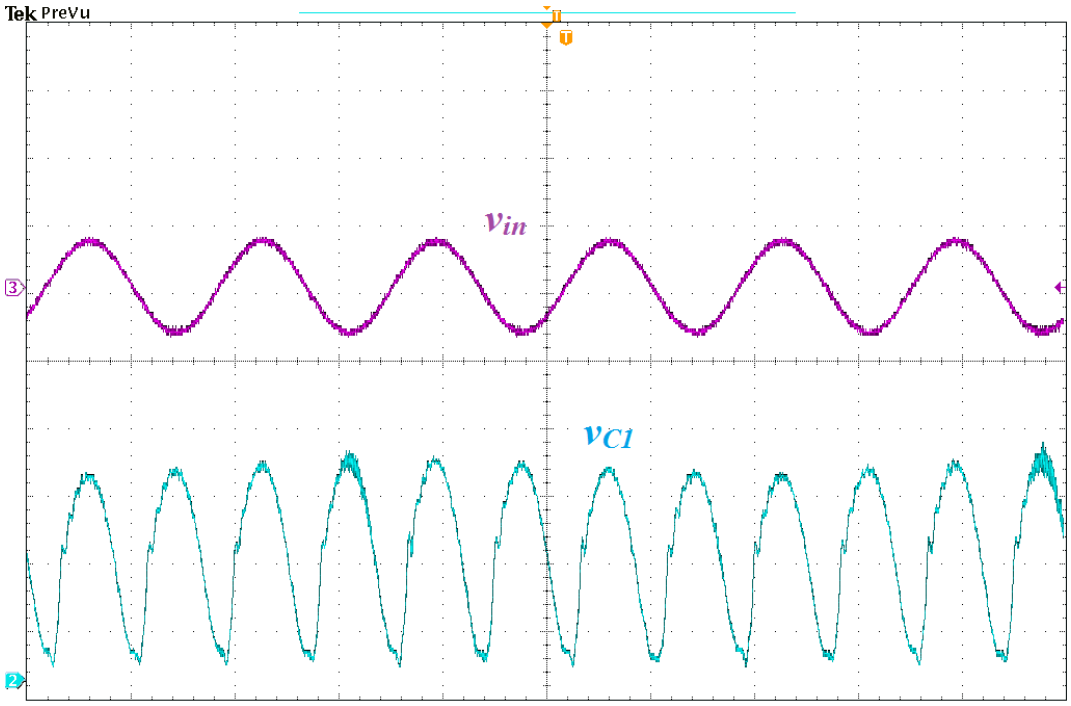



Fig. 6.39. Experimental results of the input voltage, and the SEPIC capacitor voltage. ($V_{in}$ = 120 V, $V_{dc}$ = 420 V). From top to bottom: $v_{in}$ (250 V/div), $v_{C1}$ (50 V/div), time (10 ms/div).

Fig. 6.40 shows the operation of SEPIC converter with 250 V output voltage, while the input voltage is still 120 V, 60 Hz grid. The dc link voltage is smaller than the peak grid input voltage. The power factor at 250 V output voltage is measured to be 0.986.

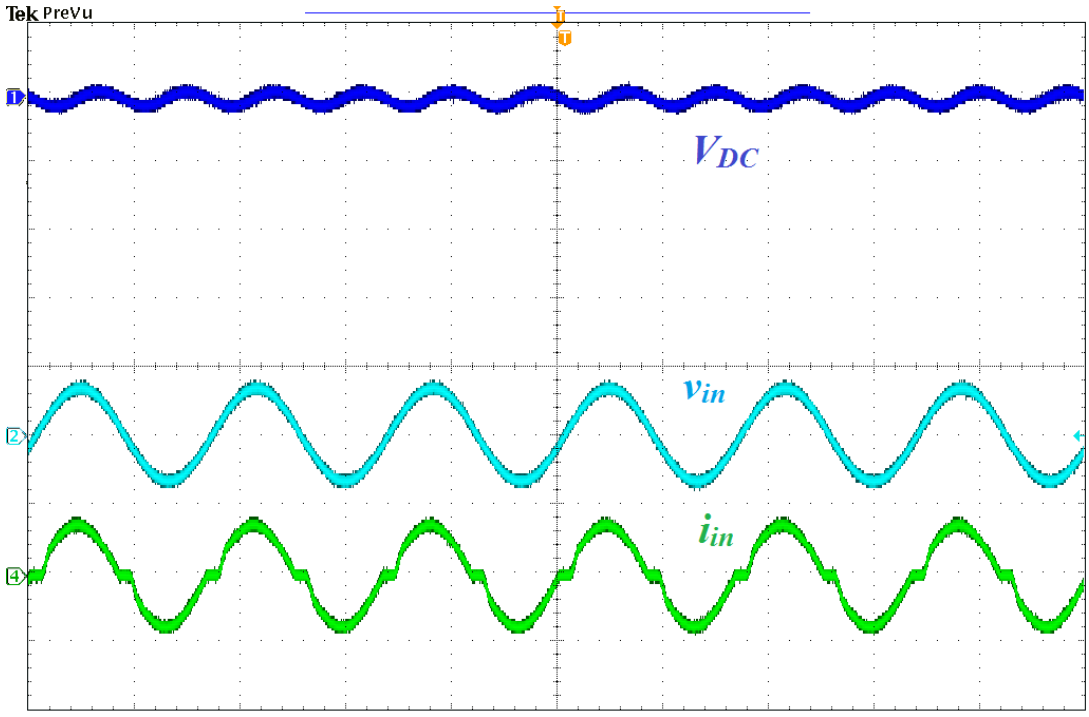



Fig. 6.40. Experimental results of the output voltage, input voltage, and the input current ($V_{in}$ = 120 V, $V_{dc}$ = 250 V). From top to bottom: $V_{DC}$ (20 V/div, ac coupling), $v_{in}$ (250 V/div), $i_{in}$ (10 A/div), time (10 ms/div).

Fig. 6.41 shows the operation of SEPIC converter with 100 V output voltage, while the input voltage is still 120 V, 60 Hz grid. The dc link voltage is smaller than the peak grid input voltage. The power factor at 100 V output voltage is measured to be 0.983. It should be noted that the experimental waveforms well agree with the simulated results. Fig. 6.42 shows the experimental efficiency data of the designed prototype, where the dc link voltage is 420 V.

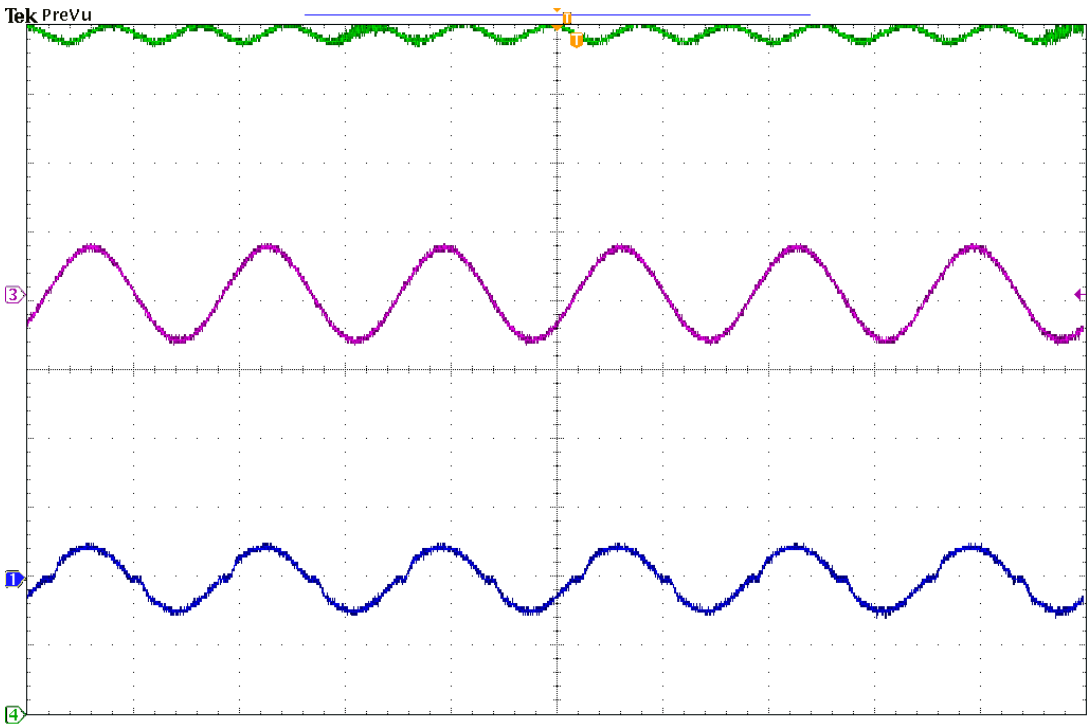



Fig. 6.41. Experimental results of the output voltage, input voltage, and the input current ($V_{in}$ = 120 V, $V_{dc}$ = 100 V). From top to bottom: $V_{DC}$ (10 V/div), $v_{in}$ (250 V/div), $i_{in}$ (10 A/div), time (10 ms/div).

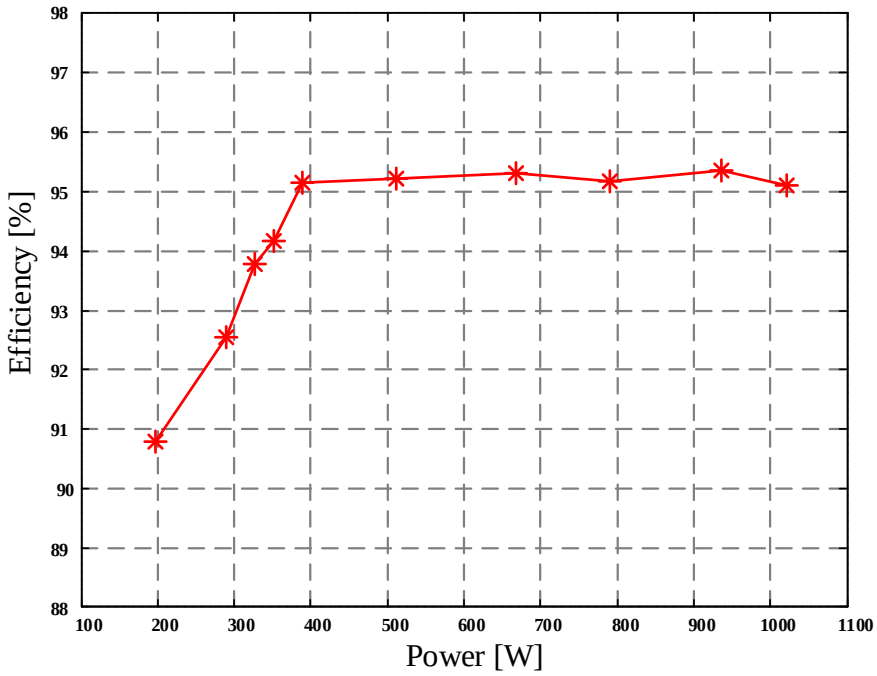


Fig. 6.42. Efficiency versus output power of the designed SEPIC converter.

### 6.6.2 Experiment Results of the SEPIC PFC Stage

Fig. 6.43 shows the picture of the 3.3 kW dc/dc LLC converter prototype. As shown in the figure, only one magnetic component is used in this converter. Both the resonant inductor $L_r$, and the magnetizing inductor $L_m$, are integrated into one single transformer. Ferroxcube ETD59 ferrite magnetic core is used to wind the transformer. Material of the core is 3C90. Designed parameters of the LLC converter is summarized in Table 7-2. It should be noted that all the power semiconductors are SiC based. Film capacitors are utilized as the output filter capacitor. This LLC converter is also controlled by the TMS320F28335 DSP development board from Texas Instruments.

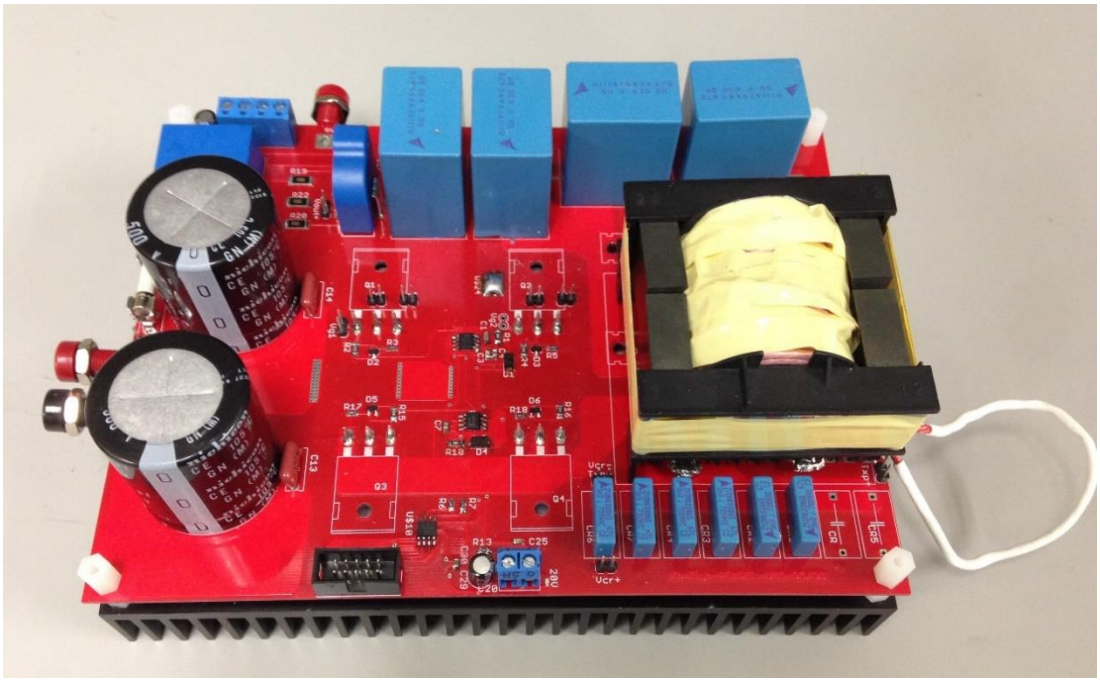


Fig. 6.43. Designed 3.3kW full bridge LLC converter prototype.

Table 6-2 Designed parameters of the 3.3 kW LLC converter

| Symbol | Quantity or Device | Parameter |
|---|---|---|
| $V_{dc}$ | DC link Voltage | 100V-420 V |
| $P_{max}$ | Rated maximum power | 3.3 kW |
| $f_p$ | Primary resonant frequency | 196 kHz |
| $t_{dead}$ | Deadband time | 200 ns |
| $n$ | Transformer turn ratio | 26:26 |
| $L_r$ | Resonant inductor | 32.2 μH |
| $L_m$ | Magnetizing inductor | 102.3 μH |
| $C_r$ | Resonant capacitor | 19.8 nF |
| $S_2$-$S_5$ | Power MOSFETs | CMF10120 |
| *D6-D9* | Power diodes | SCS220AGC |
| $C_o$ | Output filter capacitor | 20 μF |

Fig. 6.44 presents the circuit operation at the precharge stage, as demonstrated in Fig. 1. The battery pack voltage goes down to 100 V. And the charging current is 1.07 A. The normalized voltage gain of the LLC converter is equal to unity, which guarantees that the circuit is operating at the resonant frequency between $L_r$ and $C_r$. This could be clearly observed in Fig. 6.44, where both $i_{Lr}$ and $v_{Cr}$ are close to ideal sinusoidal wave.

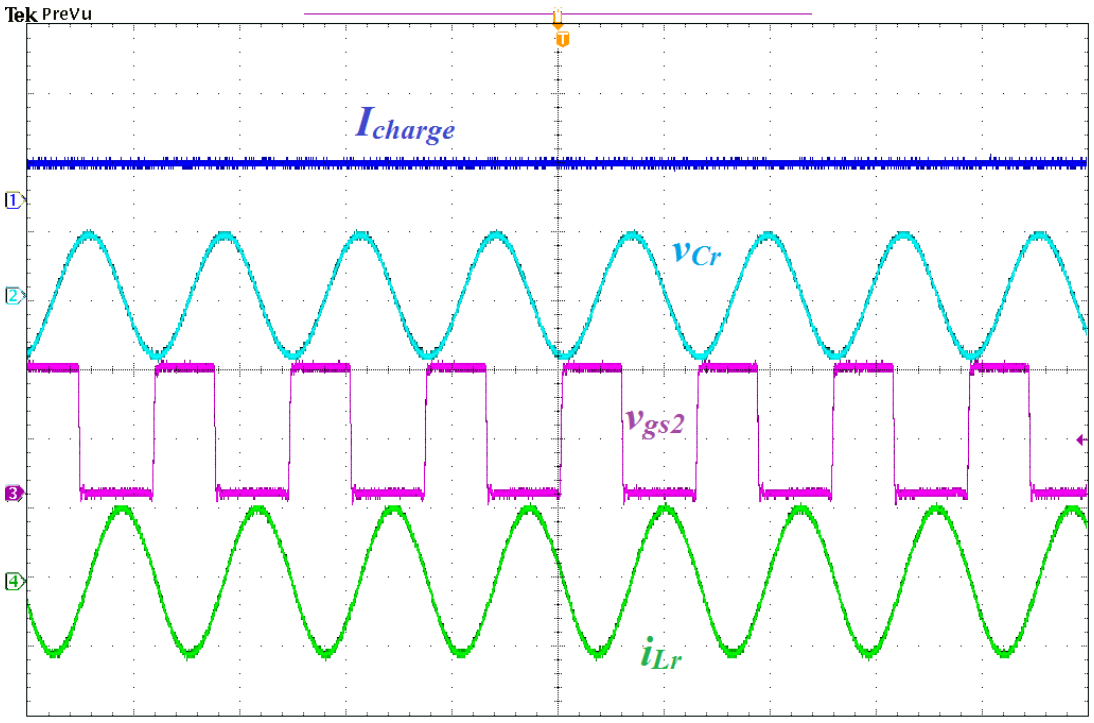



Fig. 6.44. Experimental results of the LLC charger operating at point A ($V_{bat}$ = 100 V, $I_{charge}$ = 1.07 A). From top to bottom: $I_{charger}$ (2 A/div), $v_{Cr}$ (100 V/div), $v_{gs2}$ (10 V/div), $i_{Lr}$ (2 A/div), time (4 μs/div).

Fig. 6.45 presents the circuit operation at point B in the charging profile, as demonstrated in Fig. 6.1. At operation point B, the charger enters into the constant current charging stage. The battery pack voltage is 250 V. And the charging current is 7.80 A. Due to the varying dc link voltage, the circuit is still operating at the resonant frequency between $L_r$ and $C_r$.

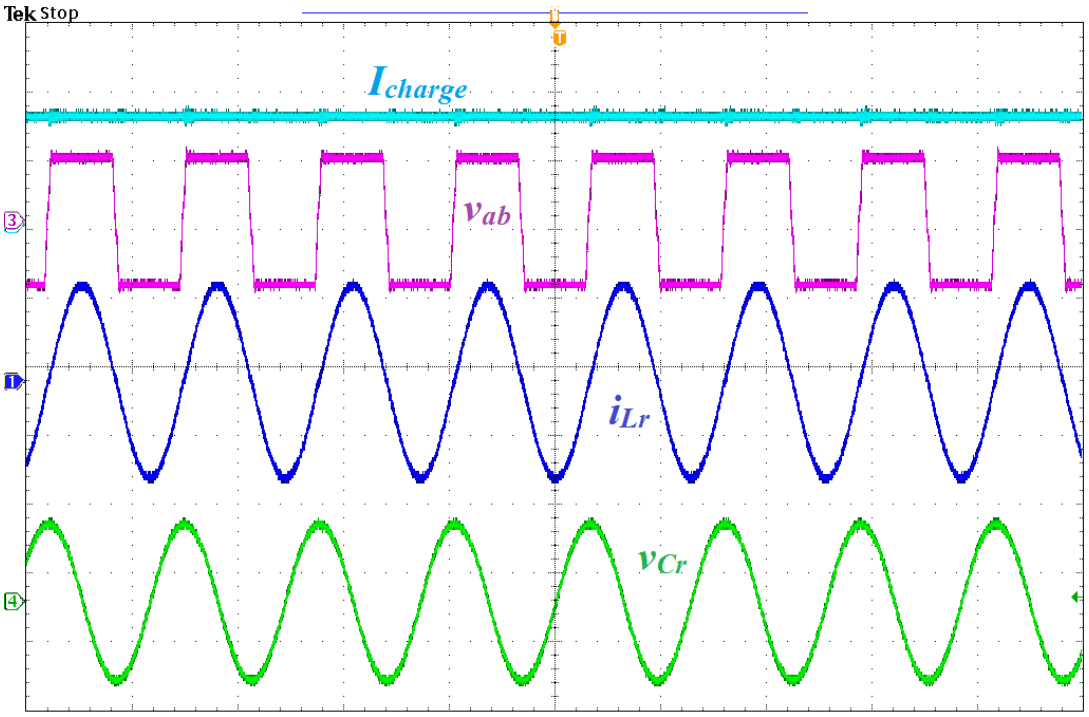



Fig. 6.45. Experimental results of the LLC charger operating at point B ($V_{bat}$ = 250 V, $I_{charge}$ = 7.80 A). From top to bottom: $I_{charge}$ (5 A/div), $v_{ab}$ (250 V/div), $i_{Lr}$ (10 A/div), $v_{Cr}$ (500 V/div), time (4 μs/div).

Fig. 6.46 shows the circuit operation at point C in the charging profile, as demonstrated in Fig. 6.1. At operation point C, the charger enters into the constant voltage charging stage. Both the battery pack voltage and the charging current reach the maximum value. Thus, the converter operates at its rated power. The battery pack voltage is 420 V. And the charging current is 7.80 A. Due to the adopted maximum efficiency point tracking technique, the circuit is still operating at the resonant frequency between $L_r$ and $C_r$.

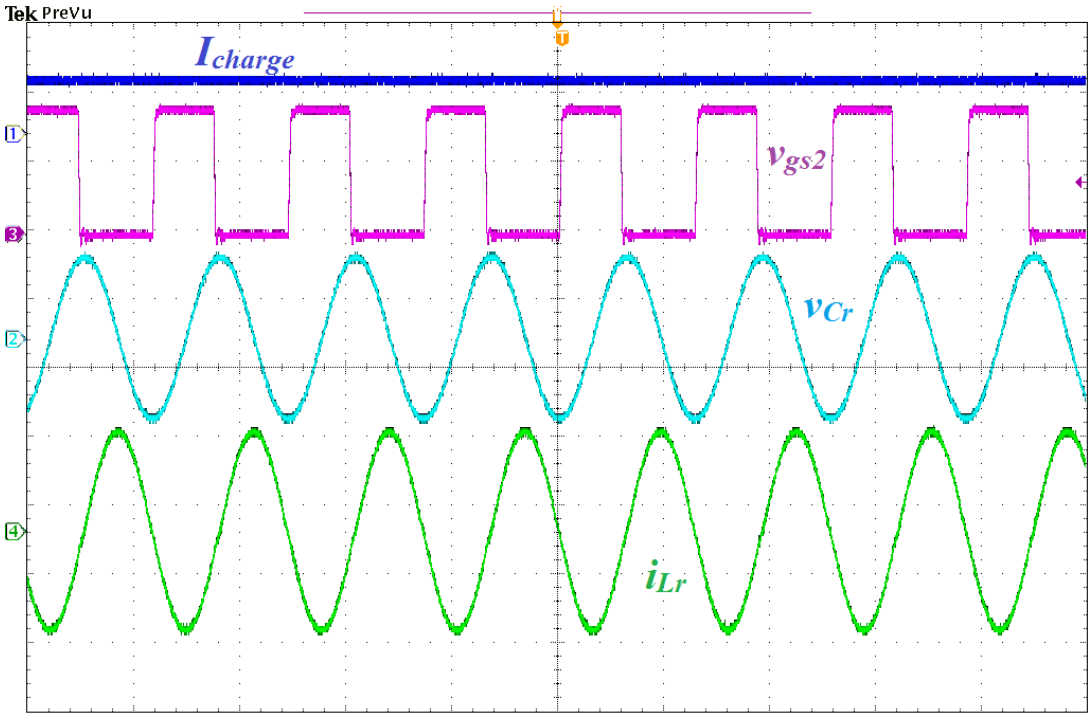



Fig. 6.46. Experimental results of the LLC charger operating at point C ($V_{bat}$ = 420 V, $I_{charge}$ = 7.80 A). From top to bottom: $I_{charge}$ (10 A/div), $v_{gs2}$ (10 V/div), $v_{Cr}$ (500 V/div), $i_{Lr}$ (10 A/div), time (4 μs/div).

Fig. 6.47 shows the circuit operation when the charger finishes the constant voltage charging. The battery pack voltage is still at its maximum value. While charging current reaches the minimum value as 0.78 A. Dc link voltage stays the same as it was in point C. The circuit is still operating at the resonant frequency between $L_r$ and $C_r$.

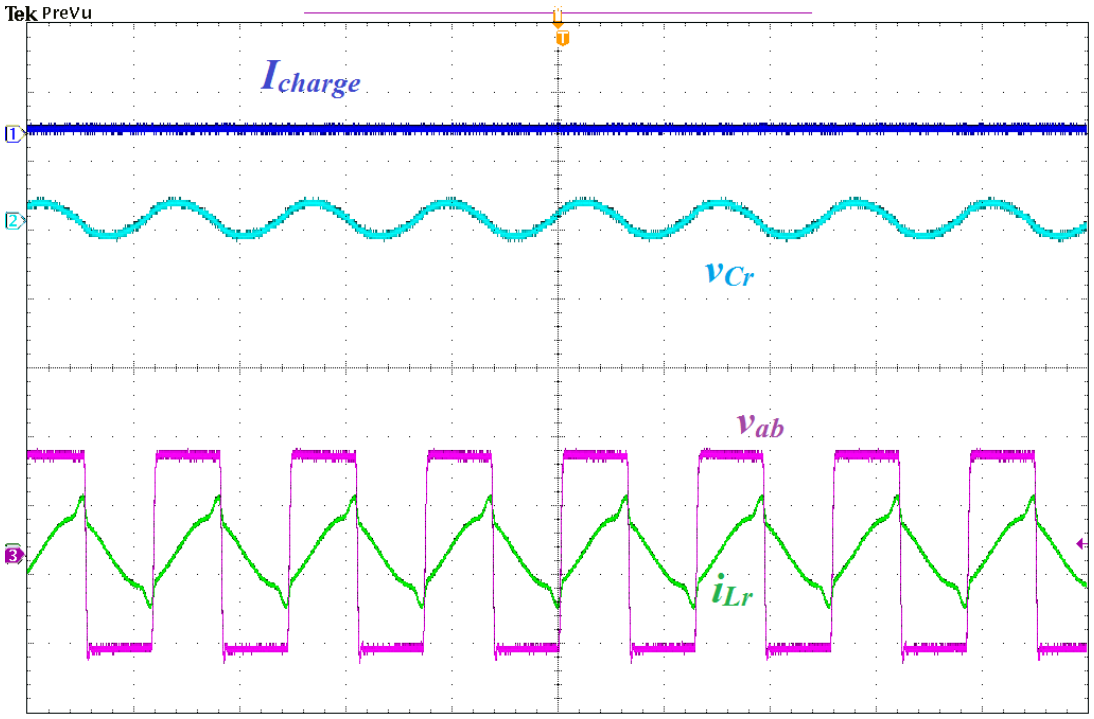



Fig. 6.47. Experimental results of the LLC charger operating at point D ($V_{bat}$ = 420 V, $I_{charge}$ = 0.78 A). From top to bottom: $I_{charge}$ (10 A/div), $v_{Cr}$ (500 V/div), $v_{ab}$ (250 V/div), $i_{Lr}$ (5 A/div), time (4 μs/div).

Fig. 6.48 demonstrates the zero voltage switching feature of the designed LLC converter. As can be seen in the figure, each time before the gate drive signal is applied to the power MOSFET, the drain to source voltage reduces to zero. This means, the power MOSFET is turned on with ZVS. The experimental conversion efficiency is captured and plotted in Fig. 49.

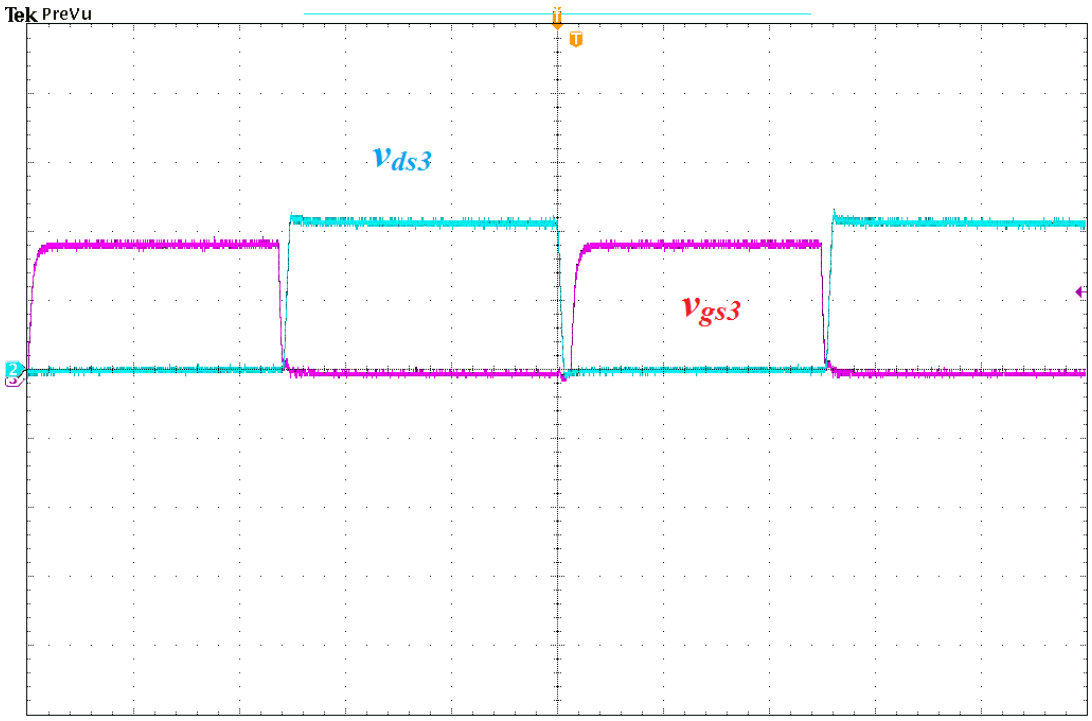



Fig. 6.48. Zero voltage switching of power MOSFET. From top to bottom: $v_{ds3}$ (250 V/div), $v_{gs3}$ (10 V/div), time (4 μs/div).

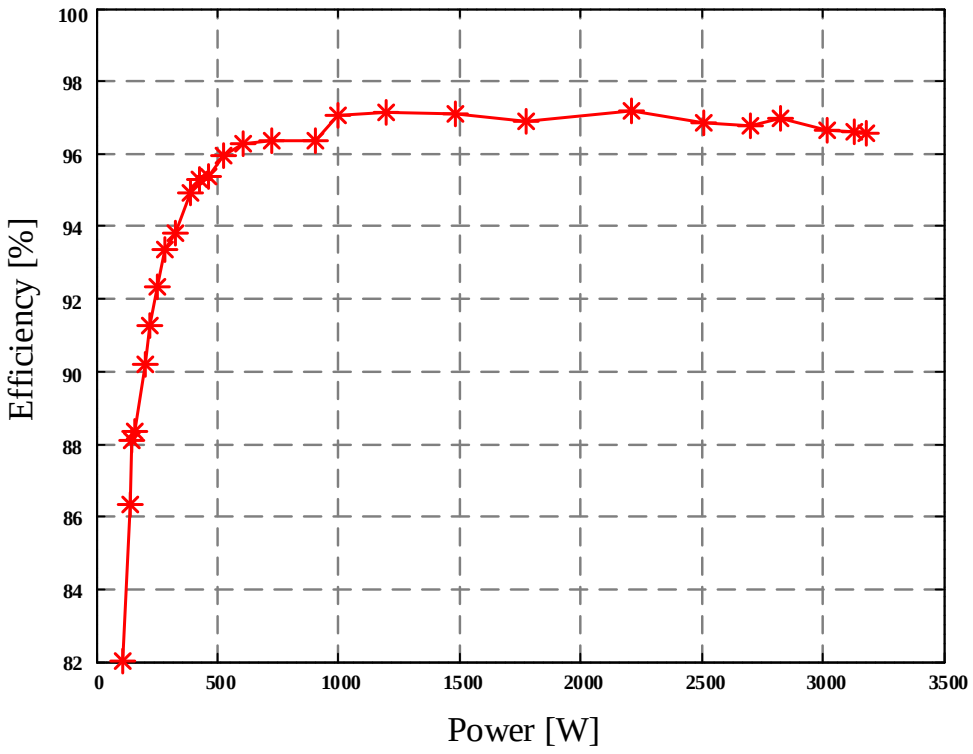


Fig. 6.49. Conversion efficiency of the designed LLC converter.

## *6.7 Summary*

In this chapter, an onboard PEV battery charger based on a SEPIC PFC stage and a LLC topology is proposed. The maximum efficiency point tracking technique for LLC topology is utilized to optimize the conversion efficiency of the charger. Proposed charger is able to charge the deeply depleted battery packs, whose voltage might goes down to 100 V. Since SEPIC topology owns the feature of both boosting the input voltage and chopping the input voltage, it is utilized in the front-end power factor correction stage. Both the steady state analysis and ac small signal modeling of SEPIC topology in PFC application are carried out. Design considerations to ensure CCM operation and to limit the current and voltage ripples are discussed in detail. A 3.3 kW charger prototype, which includes both the ac/dc and the isolated dc/dc stages, is designed to validate the proof of concept. Simulation results and experimental results demonstrate that the designed charger is able to maintain wide dc link voltage range (100V-420V) while keeping the LLC converter operating at its maximum efficiency point.

# Chapter 7 Conclusions and Future Work

## *7.1 Conclusions*

Grid-enabled plug-in electrified vehicles are deemed as one of the most sustainable solutions to profoundly reduce both oil consumption and greenhouse gas emissions. However, fast charging the onboard battery pack more efficiently, conveniently, and with smaller footprint is one of the most important challenges, which determine the acceptability of PEVs among consumers. This research mainly focuses on providing innovative solutions to cope with these challenges by using advanced power electronics topologies, advanced control strategies, as well as advanced power semiconductor devices.

The contributions of this dissertation are summarized as below.

1) We did a comprehensive literature review on the charging infrastructures, battery charging profiles, power storage and power conversion interfaces of PEVs, power electronics configurations suitable for onboard battery charging applications, the state of the art isolated battery chargers, as well as wide Silicon Carbide power semiconductor devices.

2) We proposed a methodology to effectively evaluate the performances of isolated resonant converters in wide output voltage PEV battery charging applications. Four different types of common resonant topologies (SRC, PRC LCC, LLC) are investigated using this proposed method. We found that full bridge LLC topology is the most suitable ZVS topology for high voltage battery charging

applications.

3) Based on the comprehensive topological analyses of PFC and isolated dc/dc topologies, we proposed and developed a level 1 onboard PEV charger configuration. The proposed charger is based on an interleaved boost PFC and full bridge LLC topologies. We optimized the design of the PEV charger for a 320V-420V high voltage battery pack. The optimization is based on reducing the magnet components sizes, and minimizing the total power losses over different load conditions. We developed a 1 kW charger prototype using Silicon power semiconductor devices and analog controllers. The PFC stage achieves 3.61% THD and 96.3% conversion efficiency experimentally. While the dc/dc stage achieves 96.8% peak efficiency.

4) Conventionally, designers set the dc link voltage (the output voltage of PFC stage) as fixed value (390 V). In applications where wide output voltages are required, this would make the design of second stage LLC converter hard to optimize. On the other side, LLC topology is prone to have minimized power losses at its resonant frequency, where its normalized voltage gain equals to unity.

Based on these two facts, we proposed a novel approach to design PEV chargers. In the proposed approach, we set the dc link voltage to be variable to follow the battery pack voltage. Therefore, the operation frequency of the LLC converter is always constrained to be in the vicinity of its resonant frequency. Thus, the conversion efficiency of the circuit is optimized. In order to verify this idea, we designed two LLC converters prototypes using different circuit parameters. The first

prototype has fixed dc link voltage (390 V), while the second prototype has its dc link voltage following the battery pack voltage. We found that the LLC stage of the proposed variable dc link voltage approach is able to provide 2.5% efficiency improvement at the heaviest load condition and 8.9% efficiency improvement in the lightest load condition.

5) Although the proposed variable dc link voltage approach is able to boost the conversion efficiency of the LLC converter over the wide SOC range of the battery pack, it also brings challenges to the design of front end PFC converter. The battery pack voltage might have much wider voltage range than 320V-420V, as adopted in the previous case study. For deeply depleted battery, the voltage of the battery pack might go down to 100V. This makes the boost derivate topologies no longer suitable. Especially for occasions where universal grid input voltages are required.

To address this limitation, we proposed a novel approach to design EV battery chargers. In the front end PFC stage, we proposed utilizing the SEPIC topology, such that the dc link voltage no longer needs to be higher than the peak grid input voltage. In the second stage, we continue to pursue the optimal operating point tracking technique for LLC converter. The proposed charger configuration is able to maintain good efficiency performance for the dc/dc converter, and is able to achieve ultra-wide output voltage range. We designed a level-2 charger prototype using all Silicon Carbide power semiconductor devices and a digital controller to verify this idea. In the experiment, the designed SEPIC PFC converter is able to achieve dc link voltage regulation to charge the battery pack 100 V and 420 V while maintaining good

conversion efficiency, close to unity power factor, and small THD. The designed LLC converter achieves optimized efficiency over wide load conditions. It should be noted that the designed LLC converter integrates the resonant inductor and the magnetizing inductor into one single magnetic core, which helps to reduce both the size and power losses of the converter.

## *7.2 Future Work*

The future work could focus on following three aspects.

1) Interleaved SEPIC PFC converters using coupled inductors

The SEPIC PFC converter prototype presented in chapter 8 utilizes a single-phase configuration, which is suitable for low power levels. However, in order to achieve a higher power charging, the current stress on the circuit components must increase. For the power MOSFETs, we can parallel multiple devices to achieve higher current capability. However, we could not easily parallel multiple power diodes. This is because the on-resistance and forward voltage drop of power diodes exhibit negative temperature coefficients. If paralleled, the mismatch of power diodes would cause the hot device take over majority of the current. Thus, the device could be simply damaged. Moreover, high current stress would make the inductors bulky and hard to design.

In order to eliminate those potential problems, paralleling multiple phases with each phase sharing part of the total current stress becomes a promising solution. We can artificially shift the phase of the gate signals among different phases by a

certain degree ($2\pi/n$, where $n$ denotes the number of phase), which would contribute to reduce the circuit harmonics as well as the current ripples. Moreover, the inductors could be coupled, sharing a common magnetic core. Thus, the count of magnetic devices could be kept the same as that of a single-phase topology. The schematic of a two phase interleaved SEPIC PFC converter using coupled inductors is plotted in Fig. 7.1

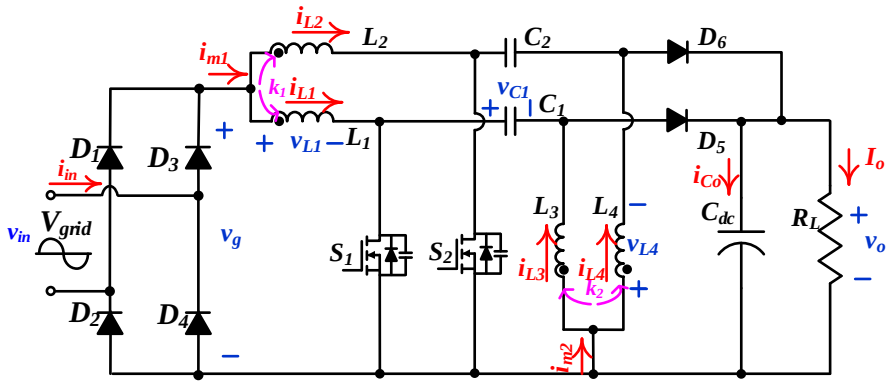



Fig. 7.1. Schematic of interleaved SEPIC PFC converter using coupled inductors.

2) Chargers with Mega Herz switching frequency

In this dissertation, both the interleaved boost PFC converter prototype and the single phase SEPIC PFC converter prototype were switched at 100 kHz, which is slightly higher than the majority of the commercial PFC converters (typically 75 kHz). However, if we can increase the switching frequency to a higher level, the size of the inductors could be further reduced. Fig. 7.2 demonstrates three PFC inductors in the same power level with different switching frequencies. The size reduction effect could be clearly observed. Future work would also focus on increasing the switching frequency of the PFC converter without comprising the conversion efficiency by

adopting ZVS and variable dc link voltage techniques.

Fig. 7.2. PFC inductors switched at 100 kHz, 500 kHz, and 1 MHz (from the left to the right).

The designed full bridge LLC converter prototype is switched at 200 kHz. However, due to its ZVS feature, LLC converter has the potential to be operated at Mega Hz switching frequency [67], [122], [123]. By boosting the switching frequency of the LLC converter, the size of the transformer could be effectively reduced. This size reduction effect could be observed in Fig. 7.3. The transformer on the left is a 3.3 kW 200 kHz transformer winded on an ETD59 core; while the one on the right is a 1.2 kW MHz planner transformer designed by Payton Planar Magnetics [124]. Is should be noted that the planner transformer looks bulky because of its outer heat sink. Future work would also concentrate on designing planner transformer for LLC topology with integrated resonant inductor.

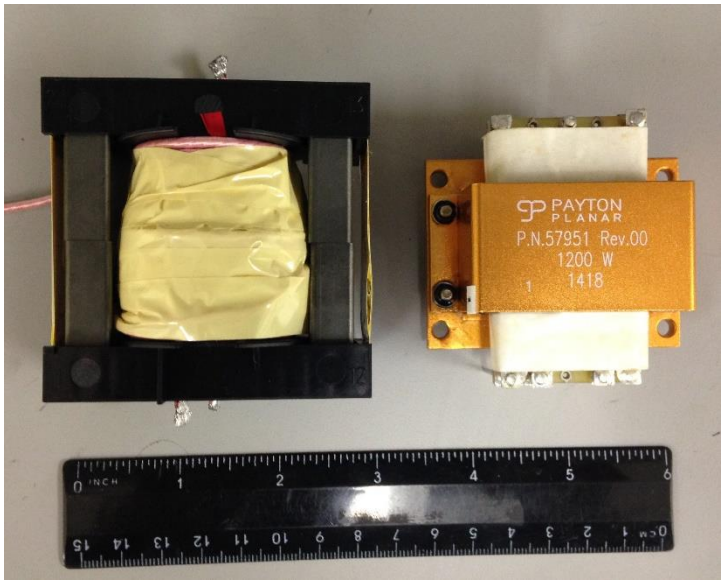



Fig. 7.3. LLC transformers switched at 200 kHz, and 1 MHz (from the left to the right).

3) Bidirectional power flow

Currently, all commercialized onboard chargers have unidirectional power flow from grid to vehicle. However, since most vehicles are parked an average for 95 percent of the time, it is foreseeable that batteries could be used to let power flow from the vehicle to the grid. In this emerging vehicle-to-grid (V2G) technology, onboard chargers are required to have bidirectional power flow capability [125]. When the vehicle is idle, the battery can feed power back to the grid.

In order to achieve the bidirectional power flow, both the front-end ac/dc PFC and the second stage isolated dc/dc topologies must be modified to be bidirectional. Fig. 7.4 (a) is a single phase half bridge bidirectional AC/DC PFC converter, while Fig. 7.4 (b) is a single phase full bridge bidirectional AC/DC PFC converter. Although half bridge topology utilizes only two MOSFETs to achieve voltage

doubling, it requires semiconductor devices with higher voltage ratings. Full bridge topology can alleviate capacitor imbalances, but it comes with higher number of semiconductor devices, which increases the cost and complexity of the control.

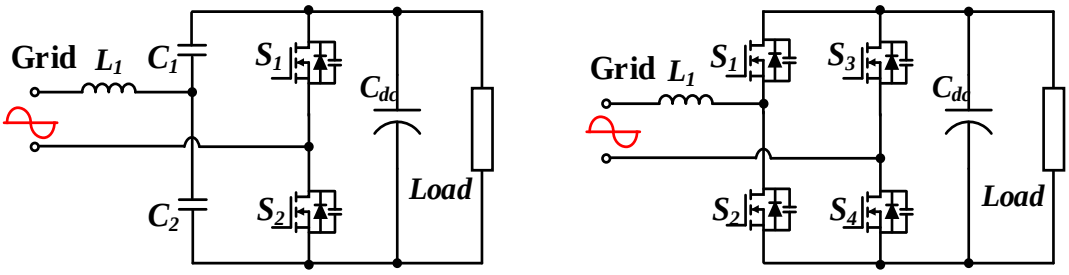



Fig. 7.4. Bidirectional ac/dc PFC stages, (a) half bridge bidirectional boost PFC, (b) full bridge bidirectional boost PFC.

Fig. 7.5 (a) is a bidirectional dual active bridge LLC converter, which is a derivative of full bridge LLC resonant converter. When the energy is transferred from grid to battery, the active bridge on the secondary side of transformer functions as a full bridge rectifier. When the energy is transferred from battery to grid, the secondary side active bridge functions as an inverter and the primary side active bridge functions as a rectifier. Fig. 7.5 (b) is a bidirectional dual active bridge CLLC converter. In this topology, there are two identical inductor capacitor (LC) networks in both the primary side and the secondary side.

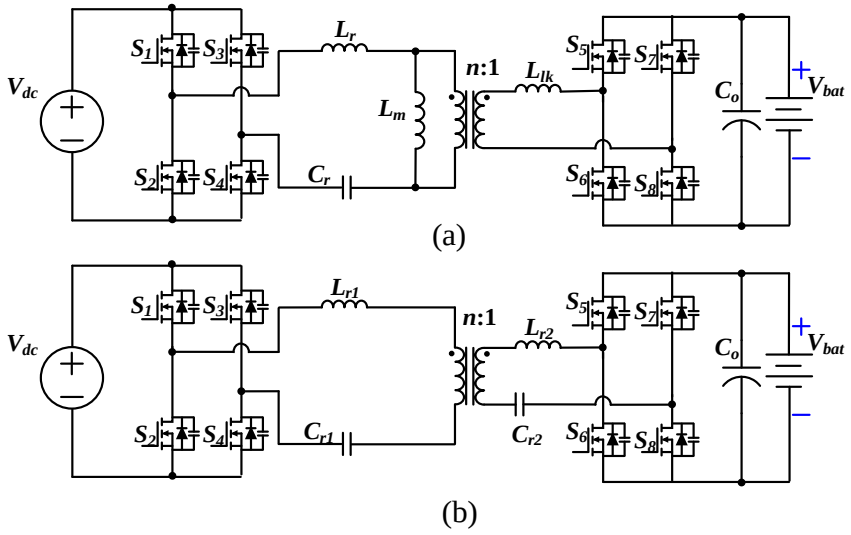



Fig. 7.5. Bidirectional ZVS dc/dc resonant converters.

Bidirectional power flow between grid and vehicle has gained interest from academia and industry. However, it must be noted that it has not been implemented on any commercial PEV in the market. Challenges mainly lie in four aspects: (a) additional cost of power electronics, (b) possible chance of battery degradation due to frequent cycling, which might not be the case in some battery chemistries as a few manufacturers believe slow discharge of the battery when it is fully charged would not have degradation impacts, (c) requirement for metering from the utility company, and (d) lack of precise policies and standards as of July 2014. Future work would pursue on achieving the bidirectional power flow of the onboard chargers, while investigating potential solutions to cope with those challenges.

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