ABSTRACT

Title of Document: CHARACTERIZATION OF TRANSIENT HEATING IN POWER ELECTRONIC DEVICES AND ITS IMPLICATIONS FOR DIE ATTACH RELIABILITY

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Military and commercial interest in the use of power electronics for applications requiring extreme operating conditions and/or placement in extreme environments is driving research to identify and develop packaging technologies that can withstand these conditions. Specifically, there is an interest in the development of packaging technology than can function reliably under transient high power loading conditions. This thesis addresses the unique packaging considerations required for this type of application, with a focus on the implications on the durability of the die attach layer. Simulations of the thermal conditions experienced at the die attach layer for different power pulse magnitudes and durations are presented. A test apparatus and experimental test plan for studying the reliability of die attach materials under high power transient loading is discussed. Studies conducted to validate the test apparatus and characterize die attach reliability are described along with recommendations for further investigation of the reliability issues associated with high power, transient loading conditions.

CHARACTERIZATION OF TRANSIENT HEATING IN POWER ELECTRONIC DEVICES AND ITS IMPLICATIONS FOR DIE ATTACH RELIABILITY

By

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Chapter 1: Introduction

Electronics technology is constantly evolving to meet an ever expanding array of commercial, industrial, and military applications. The consumer product market demands decreased package size and higher processing speeds causing laptop computers, cell phones and tablets to get smaller and faster, with more functionality. These demands for increased functionality density and speed require that the power electronics exhibit a corresponding increase in power throughput and decrease in package size, which in turn results in the need to remove higher heat fluxes from the electronics, often requiring new and higher performance thermal management solutions.

There is also market interest in expanding the operating limits of electronics so they can function effectively in a broader range of environments [1]. Industrial, military and aerospace entities all have an interest in implementing electronics in more extreme environments than our present technology will allow. Developing electronics that function reliably in harsh conditions for space, deep sea oil drilling, or automotive applications, where temperatures are higher than the commercial electronics operating range, is an industry goal. Apart from surviving the higher temperatures, the electronics must withstand wide range temperature cycling, along with other harsh environmental conditions or electrical requirements.

An area where both of these issues are most critical is power electronics. For power

electronics high voltages, currents, and power dissipation and the corresponding thermal implications are the focal point of design considerations. For this reason, power electronics have design rules, material requirements, and structural considerations that differ from standard integrated circuit (IC) packaging. A traditional chip and wire power electronic module is depicted in Figure 1.

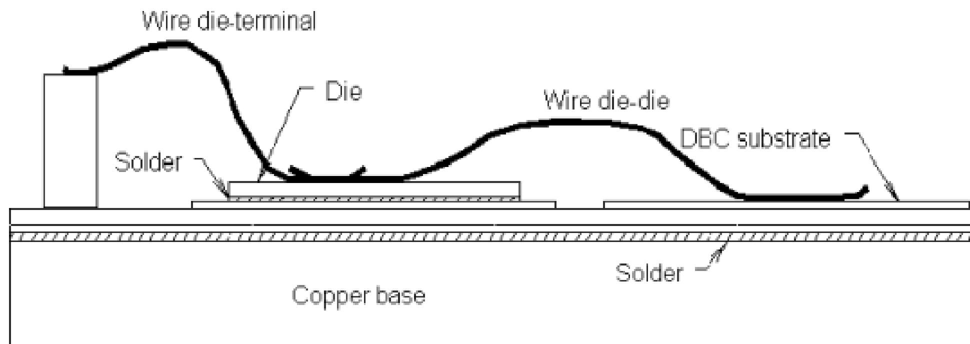


Figure 1: representative power module [2]

In this type of module, a silicon die is bonded to a substrate via a solder attach material. The substrate in Figure 1 is direct bond copper (DBC), where copper is eutectically bonded to both sides of a bulk ceramic layer. The DBC is soldered or brazed to a copper base plate and then joined to a subsequent cooling system, such as a heat sink. As the heat flux increases, all facets of the mechanical design described above require improvement to meet the thermal management and extreme environment challenge. An important step toward meeting this challenge is the shift from silicon dies to silicon carbide dies [3]. While there are many reasons for this material shift, including the higher reverse breakdown strength, increased switching speed, and higher thermal conductivity, the most relevant to meeting the challenge is wider bandgap and

the attendant higher operating temperature capability of silicon carbide. Silicon carbide devices that can function reliably at 500°C have successfully reached the market for applications requiring higher temperature operation than is possible with standard silicon limited to 200°C [3] [4]. Nevertheless, the new SiC technology will not reach full operating temperature potential until the packaging technology is developed that can also withstand the higher temperatures. A key component of the packaging is the die attach layer, which is the first level interconnect between die and substrate, as shown in Figure 1. This layer is used to mechanically secure the die to the substrate, provide a path to dissipate heat, and serve as an electrical backside contact.

Numerous studies [5] [6] [7] [8] [9] [10] have been conducted to evaluate the reliability of a range of die attach materials. These reliability studies, involve accelerated testing designed to be correlated to the actual use conditions, with the end goal of developing models that accurately predict failures in the field. When a new set of use conditions is created, it is necessary to consider the impact these new conditions may have on package reliability.

The research presented in this thesis identifies a new set of use conditions that have not previously been experimentally evaluated or sufficiently considered for their implications on packaging reliability. These new conditions are characterized by very high power flux (1,000 – 50,000 W/cm^2) at the die for very short periods of time (< 100ms). The focus of this research is the transient thermal response of the system and the resultant temperature excursions throughout the package brought on by these new conditions as a

result of the materials and design of the package. Temperature cycling as a result of consecutive "pulsed" loading of this nature may be a relevant contributor to material fatigue, especially with respect to the die attach layer. Conventional reliability studies focus on passive thermal cycling with dwell times of hours or longer.

This study aims to quantify the transient thermal conditions experienced at the die attach layer, and then to use these conditions to develop an experiment to study its effects on the reliability of die attach materials. Die attach reliability is a function of magnitude of temperature change which induces mechanical stress due to differences in thermal expansion rates. First, the pulse cycling frequency range and power flux at which a temperature cycling effect in the die attach is first observed must be determined. Then, it must be determined whether the die attach material choice affects these temperatures. Once the temperature conditions at the die attach layer are quantified in simulations, then an experimental test can be used to subject attach materials to similar conditions in order to assess the impact of pulse power loading on die attach thermal reliability.

Chapter 2: Previous Work

In this chapter, previous studies will be discussed that cover the current understanding of transient thermal loading as well as its effects on the reliability of electronic packages. In addition, work in the area of solders specific for high temperature environments is discussed because of their inherent relevance to the study. Also mentioned are previous works which used monitoring techniques that are relevant to the experimental component of this research project.

2.1 Modeling Transient Thermal Loading Conditions

The increasing frequencies and power levels in power electronics have led to a need to distinguish the effects of transient heating from steady state heating in electronic packages. In 2009, a research effort [11] was conducted which highlighted some differences in thermal profiles and package reliability caused by transient heating under high heat flux for short durations. It was determined that when consideration was made for this transient heating, the optimal design of cooling systems would vary from the established steady state rules. In steady state heat transfer, it is fundamental that a larger convection coefficient correlates to better heat transfer and increased cooling efficiency. With this transient loading, the study found that under high frequency pulsing conditions, further increases in effective convection coefficient (better cooling system) had little effect on thermal performance. Figure 2 shows the data supporting this analysis.

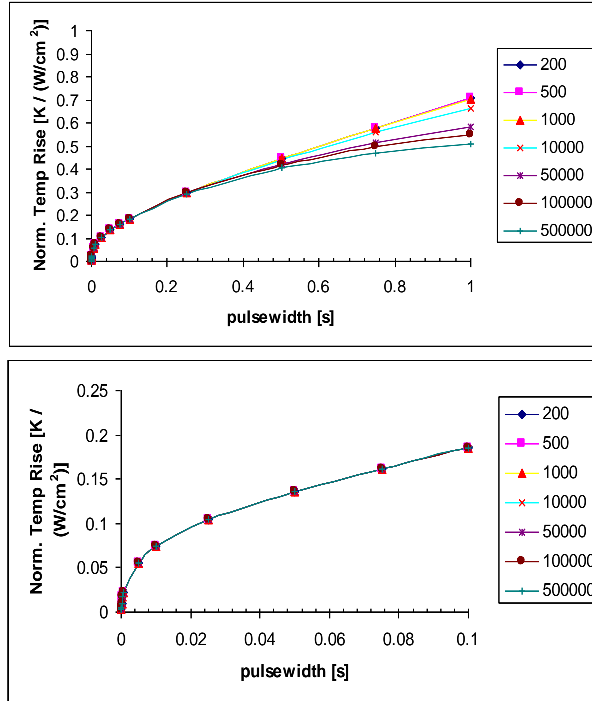


Figure 2: Effect of h_{eff} with decreasing pulse width [11]

Here, pulse width refers to the time that heat is being delivered to the chip stack. Notice that as the pulse width drops below 0.5 seconds, the magnitude of the effective convection coefficient has no discernible impact on the temperature of the chip stack, implying there is little impact on effective cooling.

Instead, the governing parameters for effective cooling shift to the material properties of the chip stack layers, namely their thermal capacitance. This study showed that while thermal capacitance becomes very relevant, the effect of thermal capacitance is highly frequency dependent. This suggests that chip stack design should optimize effective thermal capacitance based on what loading frequency is expected in the application.

Using the 1-D thermal modeling that facilitated these results, new questions developed: How will material selection affect the thermal performance of the package? How will the thermal conditions experienced under these transient loads affect the reliability of the chip stack layers? The research in this thesis addresses these questions, with a specific focus on the die attach layer.

2.2 Die Attach Reliability Models

Before addressing the effects of transient thermal conditions, it is necessary to present the models employed for mechanical fatigue prediction and accelerated life testing under steady state thermal cycling conditions. Common models include the following:

Coffin-Manson model [12]:

$$N_f = C(\Delta T)^{-n}$$

Equation 1

shows the Coffin-Manson model in a general form where the number of cycles to failure (Nf) is a function of the temperature differential (ΔT), a power law coefficient (n) that is empirically determined (usually 2 for metals), and a constant C. Written differently, the temperature differential (ΔT) can be described in terms of the plastic strain induced by thermal expansion mismatch between two bonded materials:

$$N(\Delta \varepsilon_p)^n = C$$

Equation 2

This relationship with plastic strain is the underlying principle of the Coffin-Manson model. This model assumes the device under test experiences slow thermal cycling,

including dwells at both high and low temperatures of sufficiently long duration to assume a steady state condition.

Engelmaier model

The Coffin-Manson model neglects parameters like cycling frequency and temperature range. To account for these a semi-empirical model was developed by Engelmaier [13]. Where the experiment is a function of dwell time (frequency) and average solder joint temperature. Englemaier also used an elastic approximation to define the strain in the attach as

$$\Delta\gamma = \frac{L_D D * \Delta\alpha * \Delta T}{2h}$$

Equation 3 **[13]**

where L_d is the diagonal length of the die attach. $\Delta\alpha$ is the difference in the CTE between the surfaces being joined. ΔT is the magnitude of the temperature cycle and h is the thickness of the die attach layer. Roger Wild [14] calibrated this model for the exponent for tin-lead eutectic solder as

$$c = -0.422 - (6x10^{-4})T_{sj} + (1.74x10^{-2})ln\left(1 + \frac{360}{t_d}\right)$$

Equation 4 **[13]**

where c=exponent Tsj= average die attach temperature, and t_d= dwell time at high temperature.

Norris-Landzberg Model:

$$AF = \frac{N_U}{N_A} = \left(\frac{f_U}{f_A}\right)^{1/3}\left(\frac{\Delta T_A}{\Delta T_U}\right)^2 \Phi(T_{MAX})$$

Equation 5 **[15]**

The Norris-Landzberg Model provides an empirical acceleration factor which correlates number of cycles in the use-condition (subscript "U") with number of cycles needed in accelerated testing (subscript "A"). Fundamentally, this acceleration factor allows the experimentalist to vary parameters of maximum temperature and cycling frequency in order to more quickly cause failures that represent conditions that would otherwise be costly and time-inefficient to replicate. This model has also been calibrated for high lead solder to be

$$\boldsymbol{Nc} = \frac{\mathbf{30}}{(\Delta\boldsymbol{\gamma})^2}\boldsymbol{\gamma}^{1.3}\boldsymbol{exp}\,(\mathbf{1.87} - \mathbf{0.0134}\boldsymbol{T_{max}}\ \ )$$

Equation 6

2.2 High Temperature Solders

The nature of the transient loading with which we are concerned involves very high heat flux for very short periods of time. The industry-wide goal is to extend the operating limits of power electronic devices for these types of extreme applications, so our study benefits from the exploration of high temperature solders along with conventional solders. The following discusses a few solders that are included in the scope of this research effort.

2.2.1 AuSn Solder

AuSn is an appealing choice for high temperature applications because its high melting temperature (280°C) and high flow stress provide excellent fatigue and creep resistance [16] [17]. Its high cost and the challenges associated with its processing have limited its industry wide adoption, but it is a suitable candidate for specialized applications.

2.2.2 Sintered Nano-Silver

A critical limitation of standard die attach methods is the fact that bonding is facilitated by the melting of a material between the two surfaces to be joined. This means that the bonding material must 1) have a melting temperature lower than that which can cause damage to the surrounding layers and 2) will not permit operation of the device above its melting point. This greatly limits material selection, because often materials with desirable thermal and mechanical properties have a high melting temperature. One such material is silver which has a melting temperature of 962 °C. To overcome this process limitation a bonding method called sintering has been employed [18]. It uses high pressure at temperatures significantly below the melting point to facilitate bonding. By applying pressure to silver powder or paste, adequate bonding can be achieved at temperatures as low as 250° C. While theoretically this method is sound, in practice even small flaws or misalignments of the brittle silicon die or substrate material causes cracking of the die and substrate under high pressure. As a result, even stringent process control yields low bonding success rates. To improve the throughput of sintered silver packages, a study was done [19] to reduce silver particle sizes with the reasoning that smaller particle size would reduce the pressure required to achieve a successful bond by substituting surface energy reduction for pressure as a driving force. For this study, nano-scale particles replaced the micro-scale particles commercial employed. The study reported on the reliability of the sintered nano-silver bonds compared to baseline lead-free (SAC305) solder and leaded solder (Pb95Sn5). Variations in sintering pressure, temperature and sintering time were studied. The results showed that the strongest of the sintered samples

endured many more cycles to failure than the baseline solders, and the weakest of the sintered samples was roughly on par with the leaded solder, while outperforming the lead-free solder. Such positive results make the sintered nano-silver a promising candidate for high temperature applications, and so it is selected for further study in our research effort.

2.2.3 SAC305 and Sn3.5Ag

In addition to the high temperature solders, two well established lead free solders are included in the scope of the study. They provide a sound baseline because they have been extensively studied in terms of reliability. RoHS and WEEE legislation [20] banning lead in solders drove a need for a suitable replacement, and both SAC305 and Sn3.5Ag have become prominent, commercially available options.

2.3 Die Attach Failure Mechanisms

Die attach failure mechanisms for steady state thermal cycling are well understood. In general, degradation occurs due to mechanical stress induced because of the global mismatch in thermal expansion of the two surfaces bonded together. The two materials expand and contract at different rates causing a displacement mismatch between the layers. This displacement induces a stress in the die attach. If the stress is large enough, it causes plastic deformation. In addition, if the dwell time is sufficiently long, material creep will occur. Cyclic loading causes accumulation of plastic deformation and creep. In the case of rapid power cycling, void growth is observed. In the case of slow temperature cycling, cracking is observed at the corners of the bonded surfaces, where the thermal mismatch stress is the highest.

In one study [21] both delamination and void growth were observed. In this study, the degradation was tracked, as samples were subject to accelerated aging. Silicon MOSFET devices were used as heat sources. Power was applied to these devices in order to induce the desired temperature increase. Cycling times were fast compared to normal aging standards. A dwell time of 3 minutes was used at a maximum temperature of 100°C. There was a 2 minute fall time to an ambient temperature of 55°C, followed by a 2 minute dwell time at this temperature and a corresponding 2 minute rise back to 100°C. This work illustrated the effect of thermal cycling on die attach degradation.

In this work we see the use of a common method for characterizing thermal performance, which we employ as a rough determinant for quantifying device degradation during the experimental work. This method employs a linear thermal resistance to quantify thermal performance using the following equation:

$$\boldsymbol{Zth} = \frac{\boldsymbol{T_j(t) - T_{ref}}}{\boldsymbol{P}}$$

Equation 7 **[21]**

Here the thermal resistance Z_{th}, is determined by measuring both a reference temperature (i.e. bottom surface of the chip stack), and the junction (or top surface) temperature. P refers to the power input. Higher levels of voiding and cracking result in higher junction temperatures and higher thermal resistances.

Scanning Acoustic Microscopy was used to visually track the degradation, because it is non-destructive. This allows periodic imaging of void and crack growth throughout cycling, without any concern for affecting the cycling process by altering or

damaging the test sample. SAM imaging will be used in the experimental portion of this research. It is further explained in Chapter 4: Experimental Set Up.

Chapter 3: Simulations

Simulations were conducted with two objectives. The first was to determine how the choice of die attach materialwould affect the thermal performance of the chip stack under transient loading. The second was to quantify temperature conditions at the die attach layer for a wide range of transient loading inputs. The quantification of the temperature conditions would then be used to develop an experimental reliability study.

To construct these simulations we defined the thermal inputs based on a characterization of the “pulse” power that creates these thermal inputs. A pulse is described by several parameters. These are the pulse amplitude (voltage and current), the pulse rise time, the pulse fall time, the pulse duration, and the length of time the system is off between pulses. Each of these has an effect on the temperature at the die attach. If the pulse has a long duration and there is a long time between pulses, the temperature of the die attach will rise to a level commensurate with steady-state heat transfer when the pulse is on, and will fall back to the ambient level when the pulse is off. As the pulse duration is shortened, less heat will flow and the die attach temperature will not reach the steady-state level. As the time between pulses is shortened, the heat will not have time to dissipate, and the die attach temperature will not return to the ambient value. Instead, it will slowly step up to a steady-state temperature value with each pulse. Thus, for fast frequency pulses, the temperature cycle magnitude experienced by the die attach will decrease, and thereby the stress on the die attach leading to fatigue cracking will also be reduced. If the pulse frequency

is high enough (i.e. the pulse duration is short enough and the time between pulses is short enough) the die attach will stay constant at some temperature between the steady-state temperature and the ambient temperature and will experience no cycling at all from the pulsing. There may, however, still be some degradation of the die attach due to long duration temperature cycling or from cooling during periods when the system is turned off completely for extended periods of time.

3.1 Simulation Set-Up: General

The simulation utilized an electrical analogue for heat transfer where the dissipated power, or heat flux, is represented as a current source, and the resultant changes in temperature at each successive interface in the package stack are given as voltages at successive nodes. Each of the elements in the stack-up (e.g. die, die attach, substrate) is modeled as a (thermal) resistor in series and in parallel with associated (thermal) capacitance.

Theory of thermal circuit model:

The thermal circuit in its most basic form is a 1-D steady state heat transfer where Fourier's law describing heat through a plane wall can be reorganized to create an Ohm's law analogue for current through a resistor. The relationships are as follows:

$$\boldsymbol{V = IR}$$

Equation 8

$$\boldsymbol{q = -\frac{kAdT}{dx}}$$

Equation 9

Set $V = dT$ Temperature difference across the plane wall is analogous to voltage across a resistor. Set I = q , Current is analogous to heat flux.

Set dx = L where L is the thickness of the layer across which there is a temperature difference. The result is an equivalent resistance, $R = \frac{L}{kA}$, Where the resistance is a function of the material's thermal conductivity and cross sectional area. In this case, as all the die attach materials will have the same thickness, L can be set equal to 1.

To describe the time dependent behavior of heat flow through a material, the properties of that material dictate, and can be modeled with an equivalent capacitance in much the same way that we modeled equivalent resistance.

Mass and specific heat dictate how heat energy is stored in a material. With a lumped mass assumption, the following relationship describes thermal capacitance:

$$C = mcp\Delta T$$

Equation **10**

The package configuration shown in

Figure 3 was used for all simulations. It consists of a die, the backside of which is attached to a DBC AlN substrate with one of five different die attaches (viz. SAC 305, Sn3.5Ag, nanoscale sintered silver, Epotek P-1011, and Au80Sn20). Beyond the substrate, the heat sink is simply modeled as an equivalent convection. All the heat is assumed to be dissipated from the die. The total power dissipated by the device is given as the product of the electrical current and voltage curves using the basic formula:

$$Pdiss = I(t)V(t)$$

Equation 11

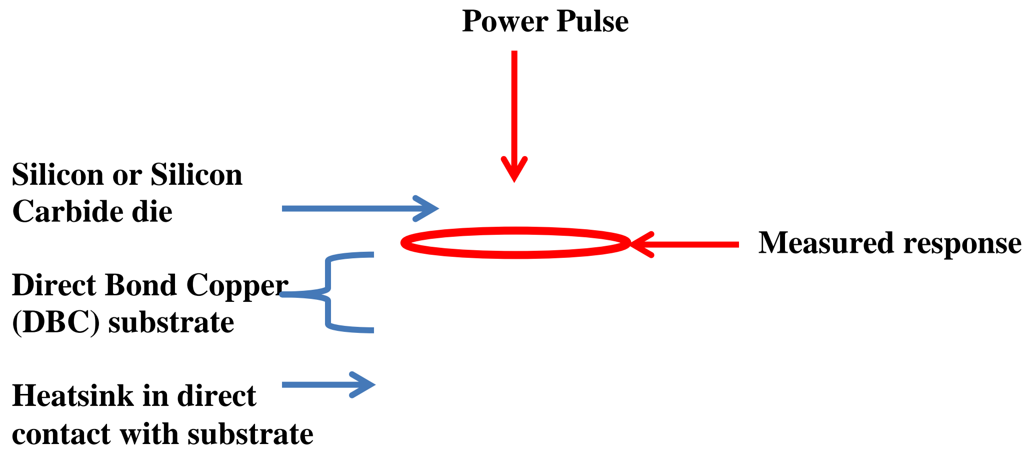


Figure 3: Representative electronic packaging stack [11]

3.2 Effect of Die Attach Material on Thermal Response

3.2.1 Simulation Set-Up

A representative circuit for the entire package stack-up is depicted in Figure 6 below. A representative power pulse is shown in Figure 4. To create the appropriate current source analogue for heat flux, it was assumed that the curves for I(t) and V(t) are approximately sinusoidal with I(t) comprising only the positive half-wave of the sine function. I(t) was assumed to go to zero during the "off" half period. The resulting power curve of I(t)V(t) is a half-sine squared wave. In order to create this kind of source signal in the simulation circuit element shown in Figure 4 was created:

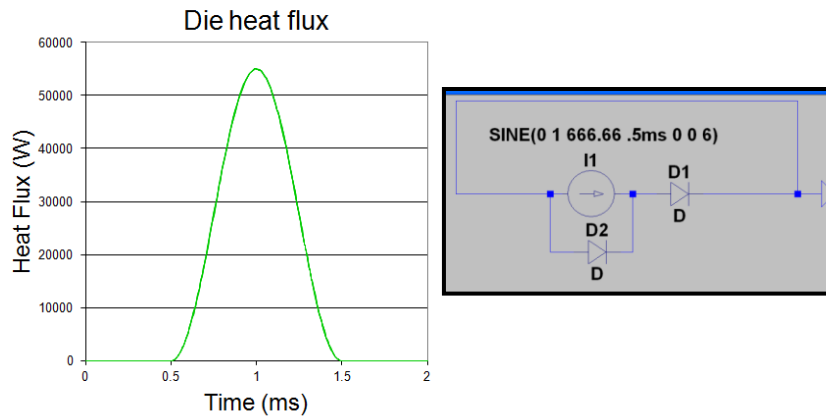


Figure 4: Expected heat flux and circuit to create expected heat flux

The diode D1 allows only the positive half cycle of the sine wave to be transmitted. The antiparallel Diode D2 is used to shunt the current during the negative half cycle when D1 acts like an infinite resistance.

The half wave rectified sinusoid of arbitrary magnitude flowing through diode D1 is then input to a user defined current source in the main model and multiplied by the voltage to yield the $\sin^2$ function of the appropriate magnitude. “Maxpwr” is the magnitude, and I(D1) is the current through the diode D1. The user defined current source, B3, can be seen in Figure 5 and also as part of the overall circuit in Figure 6.

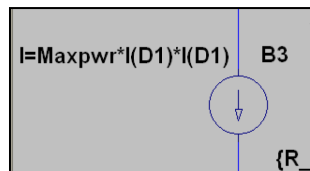


Figure 5: User defined current

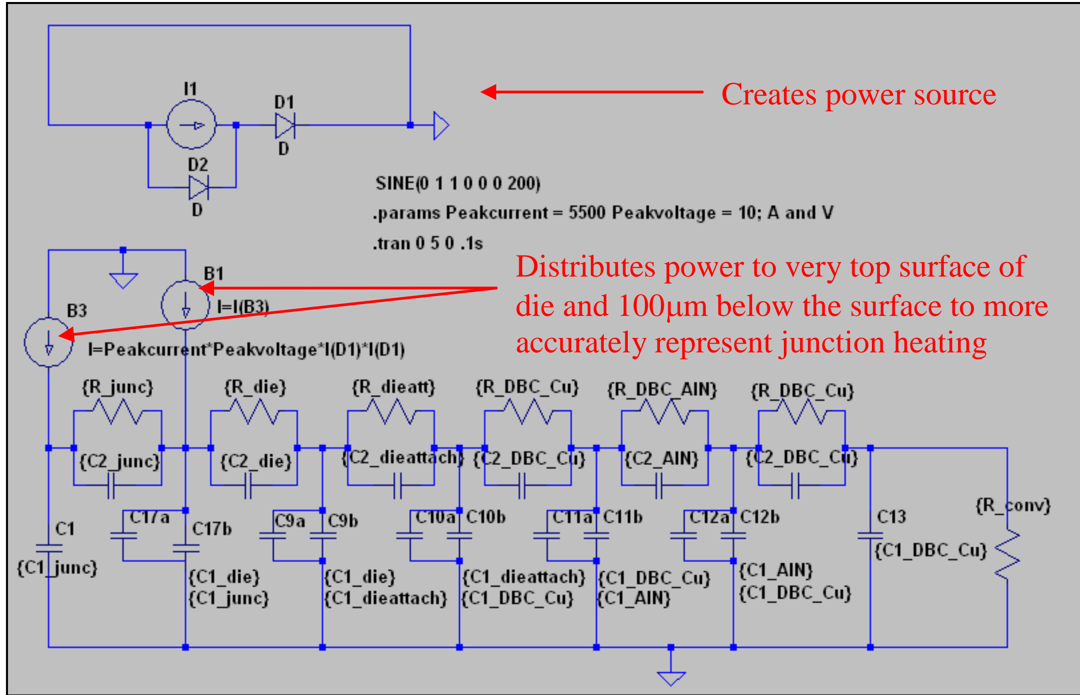


Figure 6: Entire thermal circuit

The circuit is used to determine the effect of pulse frequency on the temperature of the die attach for five die attach materials. The thermal parameters used in the analysis of these die attaches are provided in Table 1.

Table 1: Selected Die Attach Materials [22]

Material	k(W/m*K)	ρ(kg/m^3)	C_p(J/kgK)	ρC_p (J/m^{3}K)
Sn3.5Ag	50	7360	220	$1.6\text{x } 10^6$
Epo-Tek P1011	1.29	3190	628	2.0×10^6
SAC 305	57.26	7400	220	1.6×10^6
AuSn (80/20)	57.3	19720	129	2.5×10^6
nanoscale silver	200	8580	233	2.0×10^6

3.2.2 Results for Silicon Die

The pulse for the silicon devices consisted of the following:

$$\Delta V = 10V$$

$$\text{Max current} = 5500A$$

Figures 7 through 12 show the heat flux and temperature changes for different pulse durations and frequencies. Figure 7 shows the heat flux as a thick dashed line (green), and the resultant Normalized temperature as a grouping of thin solid lines (blue). Calculations were made of the temperature change in each of the five die attach materials as a result of exposure to the pulse. Temperature change was taken at the node directly below the die attach material. The temperature changes for all of the die attach materials are plotted in thin blue solid lines. Figure 7 shows that the results for all die attach materials studied were similar. The reason for this is that the time constant for the heating of a material is a function of its mass times its heat capacity. So assuming that each of the die attaches has the same area and thickness (bondline), the time constant for heating is proportional to ρC_p. As is shown in Table 1, the values for ρC_p normalized to the value of 2.0×10^6 for nanosilver vary from 0.8 to 1.25 with Epotek P-1011 and nanosilver having nearly identical values. This is further brought out in Figure 8 which is an expanded view of the temperature responses of each die attach after a single pulse in the region from 1.27 to 1.29 ms, where the temperature is still increasing. SAC 305 and SnAg which had the lowest ρC_p show the quickest response (highest temperature), while Au80Sn20 which has the highest ρC_p shows the slowest response (lowest temperature), Epotek P-1011 and nanosilver, which have the same ρC_p have the same response. This order of die attach responses is the same for every simulation in the study. SAC305 and SnAg

consistently reach a slightly higher maximum temperature and fluctuation range, and the others follow suit. However, for a single pulse, the differences are less than 2% of the entire temperature excursion. Figure 7 also shows that for a single 1 ms pulse, the die attaches all increase to a similar saturation temperature. However, the pulse is not sufficiently long for the device to reach steady-state. As can be seen in Figure 9, with multiple pulses of 0.75 ms duration with a time between pulses of 0.75, the temperature continues to ratchet upward even after six pulses. Furthermore, after six pulses we see in Figure 10 differences of about 0.15×10^{-3} °C/(W/cm^2), which is approximately 1% of the entire temperature span.

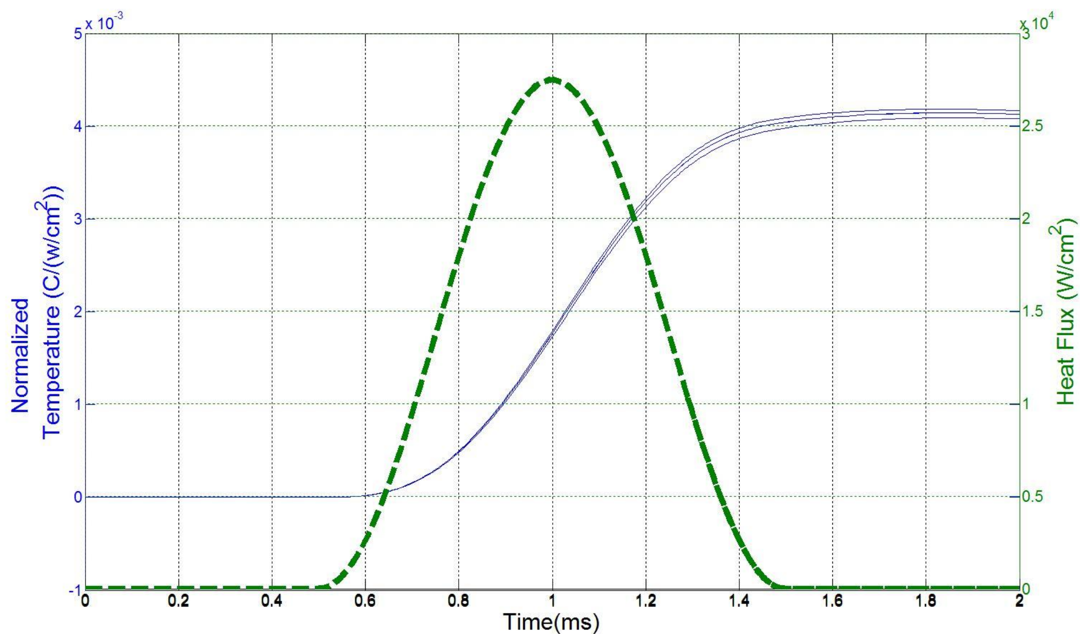


Figure 7: Single pulse, 1ms period

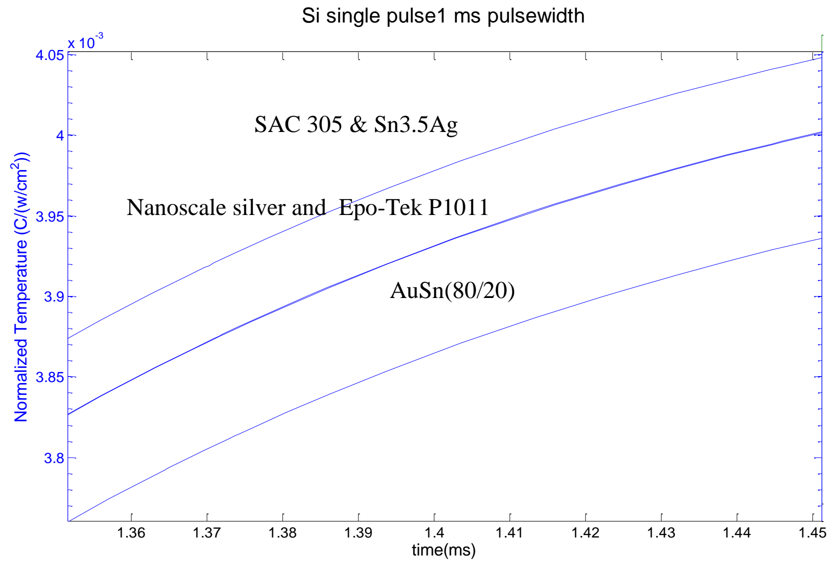


Figure 8: Expanded view of Figure 7 from 1.35 to 1.45 ms.

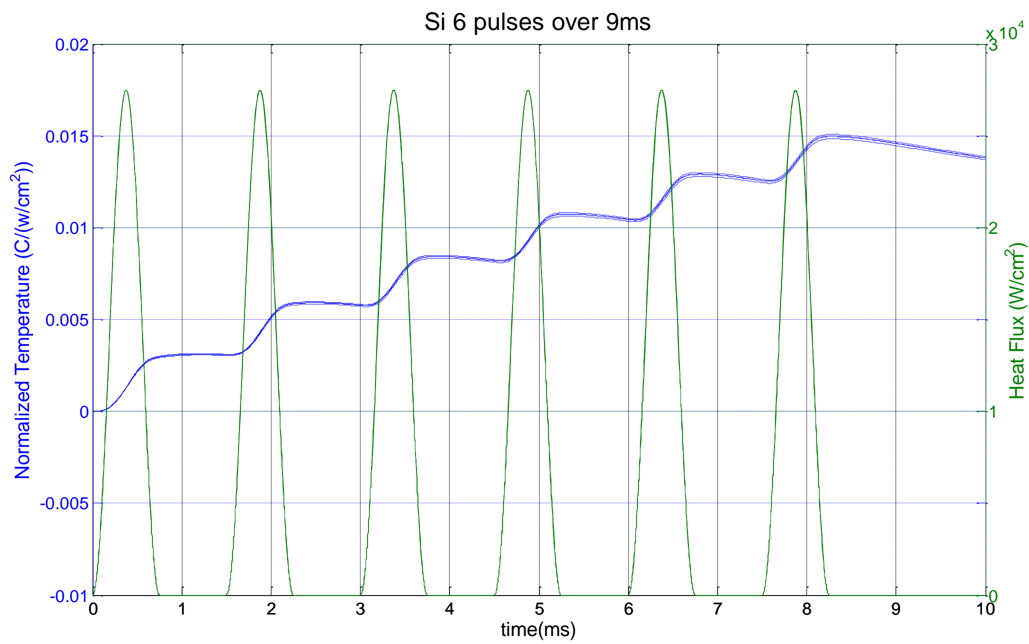


Figure 9: 6 pulses over 9ms

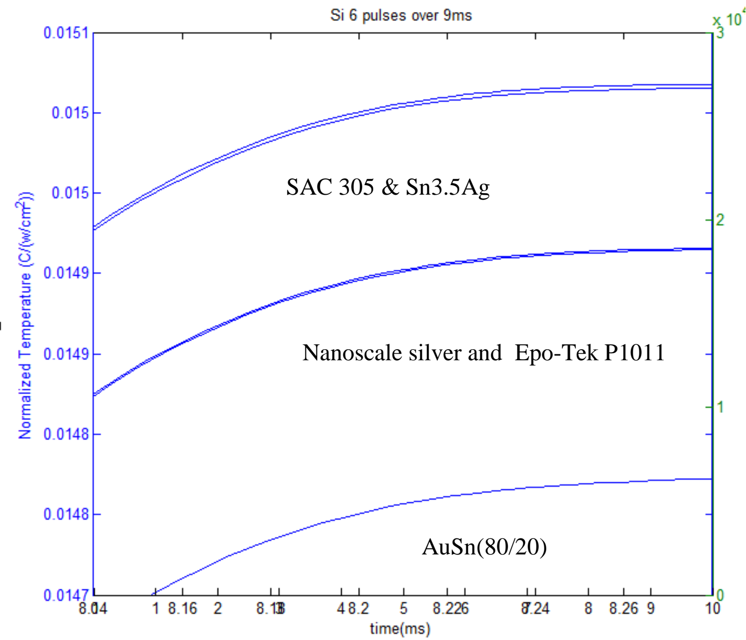


Figure 10: Expanded view of Figure 9 at the sixth pulse

The results for multiple pulses of 0.7 ms duration with 0.7 ms between pulses, as shown in Figure 11, are qualitatively the same as the previous simulation, as are the results for a 1ms duration pulse with 1 ms between pulses, as shown in Figure 12.

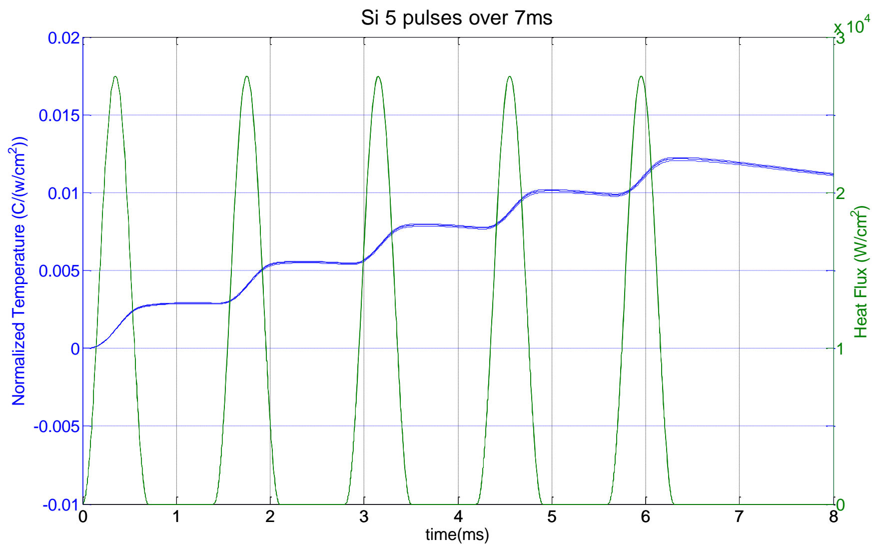


Figure 11: 5 pulses over 7ms

However, Figure 12 also shows that if there are a sufficient number of pulses, a plateau condition will be reached in which the temperature remains at a constant high level with a very small but constant change in temperature over each cycle. It is these small temperature changes we wish to study for their affect on die attach fatigue. At this frequency, there is no significant difference between die attaches after 300ms of cycling. A expansion of these results are discussed in section 3.4 Frequency Study.

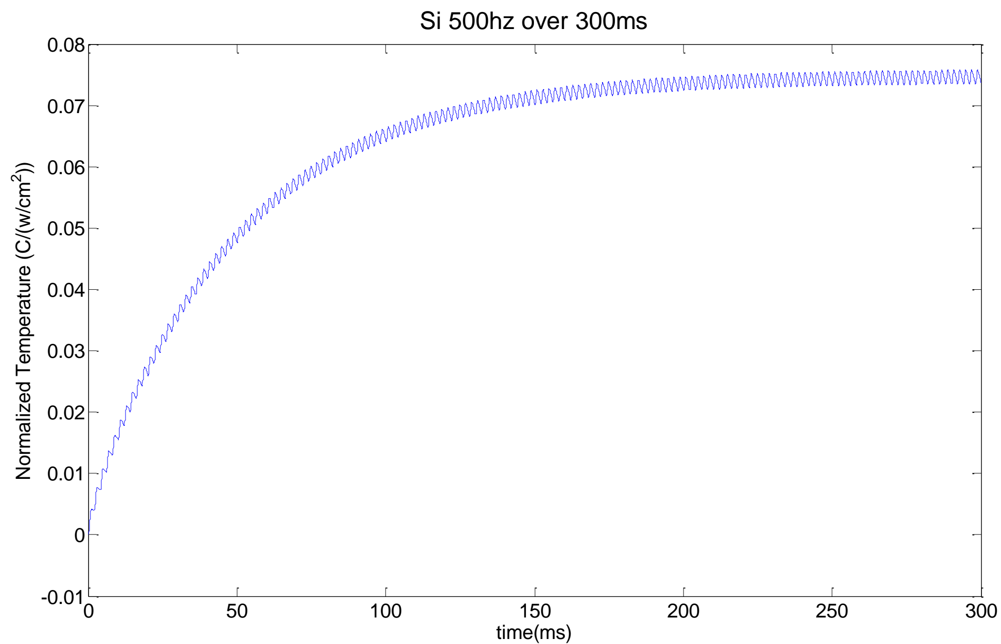


Figure 12: 500Hz for 300ms

3.2.3 Results for Silicon Carbide

The pulse for the silicon carbide devices consisted of the following:

$$\Delta V = 10V$$

$$\text{Max current} = 1300A$$

The results from the silicon carbide simulations are qualitatively similar to those of the standard silicon component. The plots are shown below, and useful numerical data is summarized in the analysis section.

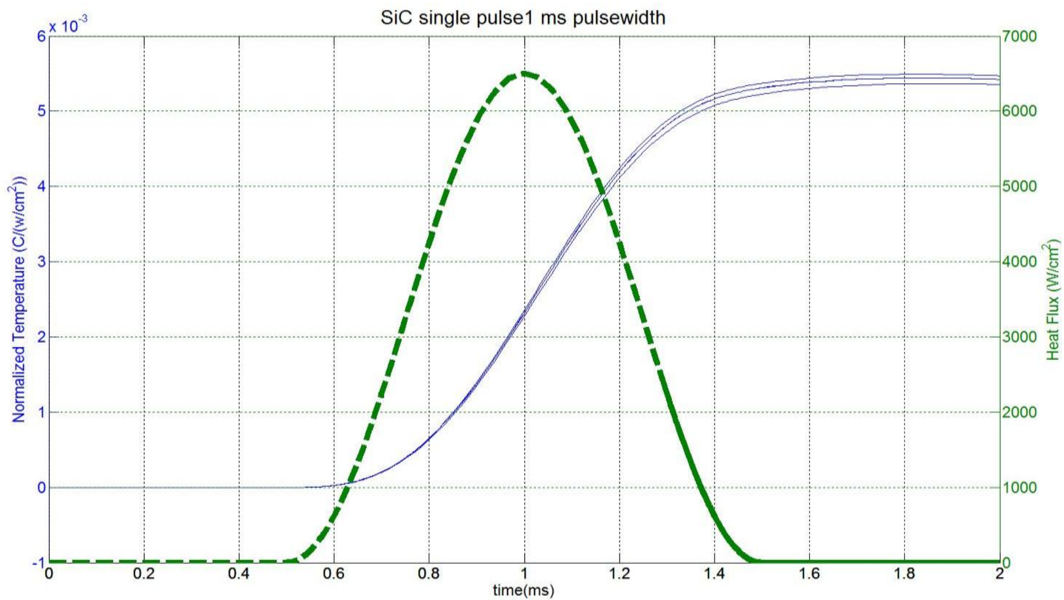


Figure 13: Single pulse at 500 Hz (1 ms half period)

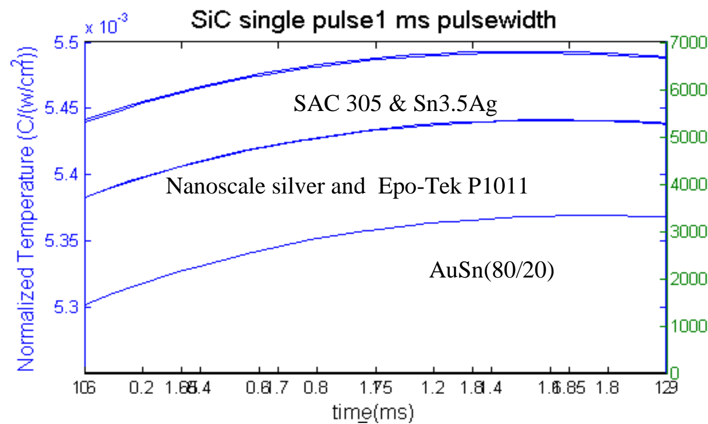


Figure 14: Expanded view of single pulse from 1.6 ms to 1.9 ms

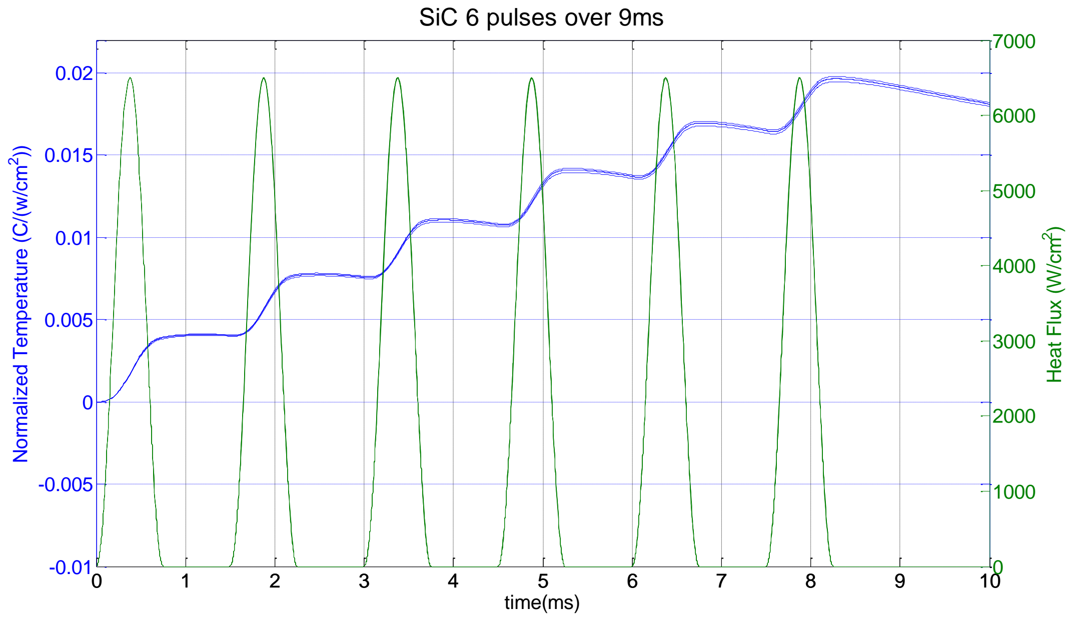


Figure 15: 6 pulses over 9ms

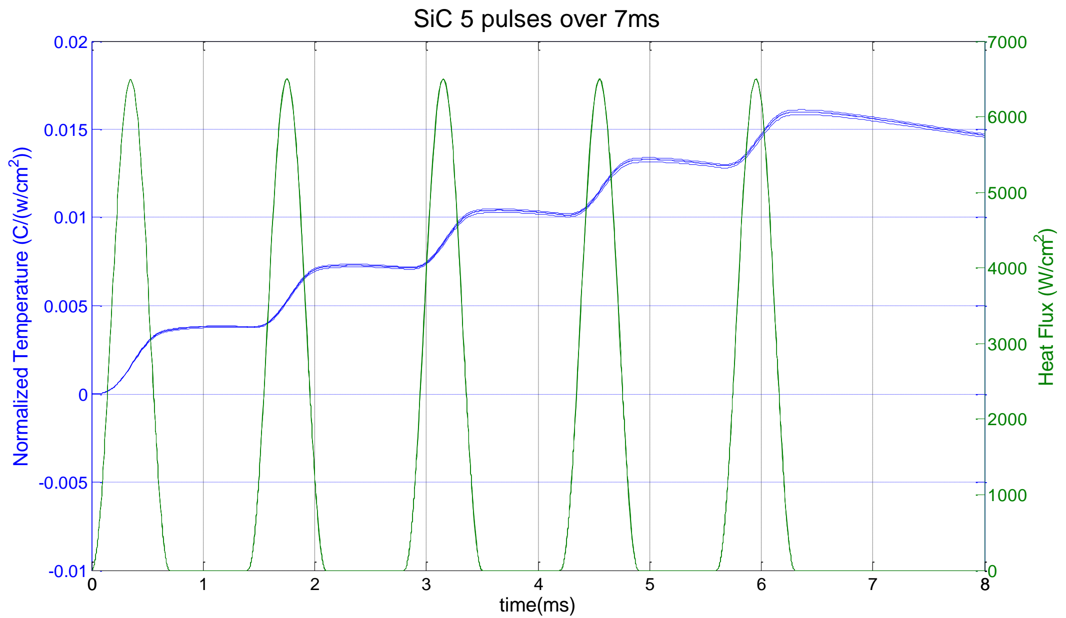


Figure 16: 5 pulses over 7ms

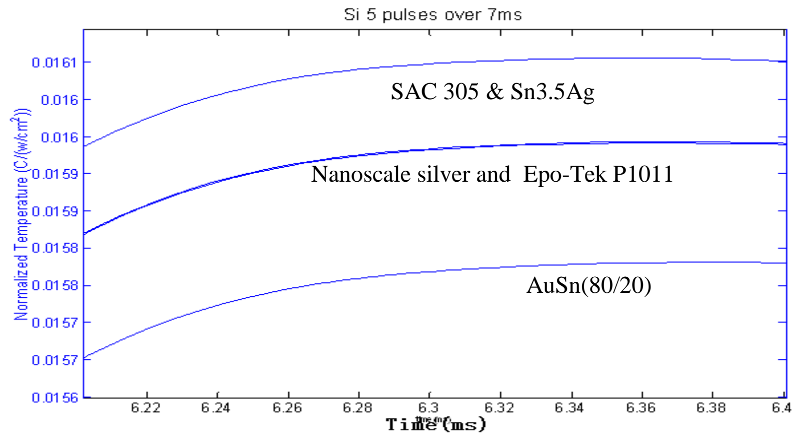


Figure 17: Expanded view of figure 15 after the 5th pulse

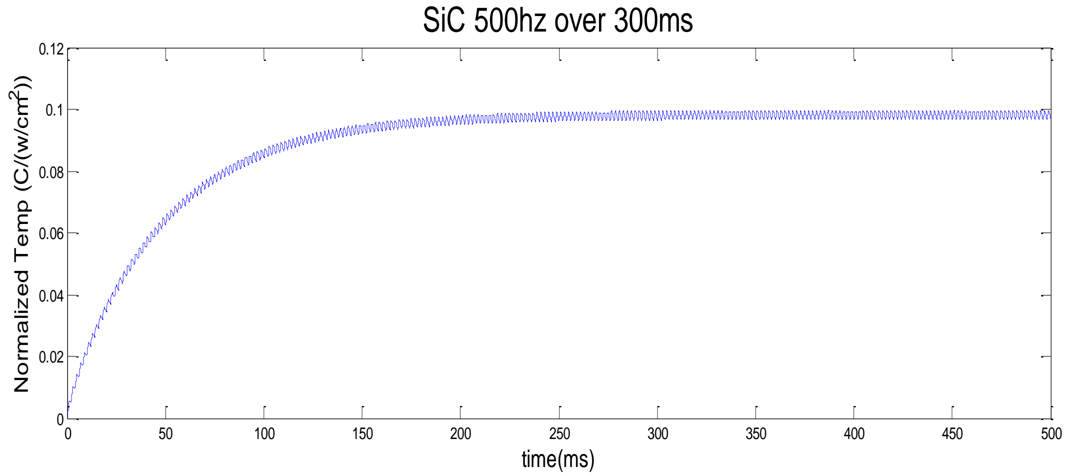


Figure 18: 500Hz for 1.5sec

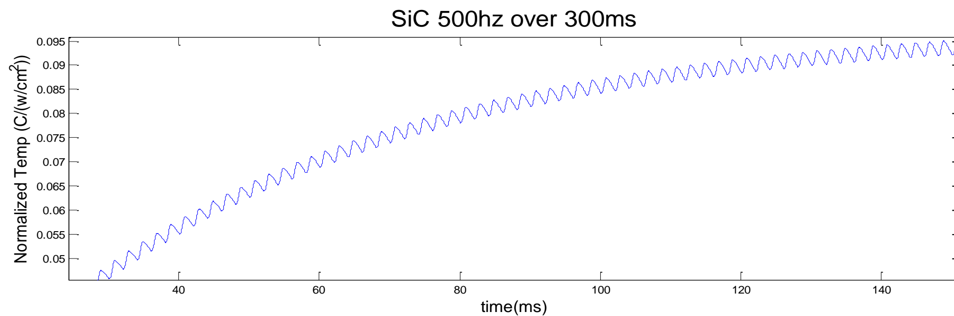


Figure 19: Expanded view of figure 17, as response approaches steady state

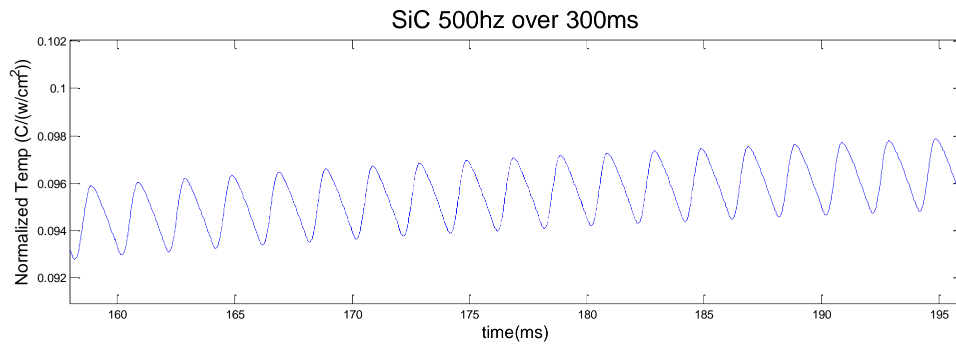


Figure 20: Expanded view of steady state fluctuations from figure 17

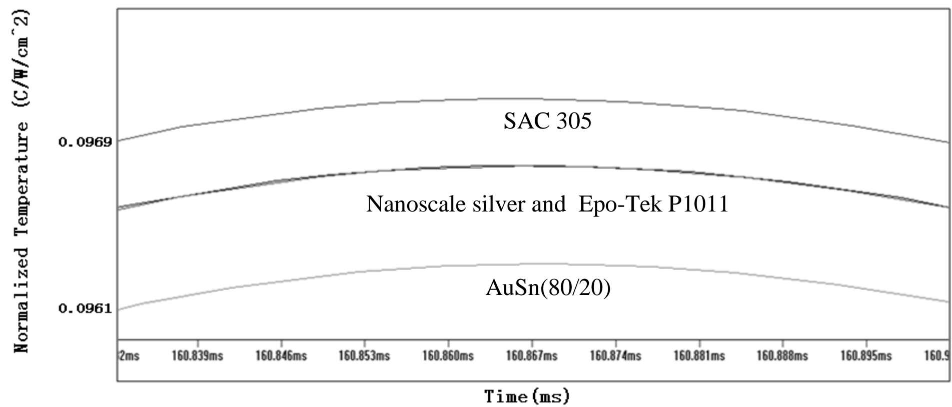


Figure 21: Expanded view of figure 17 to distinguish different die attaches

3.2.4 Analysis

All results support a common conclusion. Among the die attaches studied, the choice of die attach has a relatively small effect on the transient thermal response of the package. Measured against the total temperature fluctuations and the maximum temperature values experienced by the die attach, the variation between die attach materials is quite small. This information is summarized in Table 2 below.

.

Table 2: Die Attach Variation (normalized to power density (W/cm^2))

Simulation	Normalized ΔT/pulse	Normalized max T	Die Attach Variation
Silicon Chip			
Single pulse, 1ms overall	.0042	0.0042	1.8%
6 pulses over 9ms	.0029	0.0154	1.2%
5 pulses over 7ms	.0029	0.0124	2.1%
500Hz for 300ms	.0026	0.0524	<0.5%
Silicon Carbide Chip			
Single pulse, 1ms overall	.0055	.0055	2.0%
6 pulses over 9ms	.0040	0.0201	1.1%
5 pulses over 7ms	.0038	0.0162	1.3%
500Hz for 1.5 sec	.0032	0.0727	0.8%

In Table 2 , Die Attach Variation is measured at a given response peak between the highest response curve (SAC305) and the lowest response curve (AuSn), as shown in Figure 21. Such small variation from one die attach to another can be explained using the ρC_p argument discussed earlier. Using Table 1 it is obvious that thermal conductivity (k) is not a factor that determines the thermal performance of the die attach under pulse power loads. SAC305 and AuSn have nearly identical thermal conductivities but different temperature responses. Furthermore, the thickness of the die attach is only 50 μm, making the bulk thermal resistance quite small. Instead, it is the capacitance, or thermal heating rate of the die attach (proportional to ρC_p) that governs the temperature. Table 1 shows that this product does not vary greatly between materials even though, independently, ρ and C_p vary substantially.

For pulsed power applications, the results suggest that die attach material selection should not be based primarily on thermal material properties. Therefore, further investigation will focus on the relative fatigue resistance of the die attach materials to large numbers of cycles with a relatively small Δ T.

As a side note, Table 2 lends some insight about the extreme temperature conditions that are created with such high power electrical pulses. The die attach interface is shown to have fluctuations as high as 160°C in a single pulse. We arrive at this value by using the values in Table 2 and introducing parameters of 27.5kW for power input (parameter used by the Army Research Laboratory), and $0.72cm^2$ (a typical silicon power device size). These high fluctuations and correspondingly high temperature rises make it important to have a low duty cycle(<<50%) for high power so as to avoid exposing the device to extreme temperatures.

3.3 Thermal Conditions at Die Attach Layer

In the last section, it was shown that die attach material selection had an insignificant impact on the thermal performance of the system under these unique loading conditions. Since all of the die attaches are experiencing the same thermal conditions, it stands to reason that die attach selection for pulse power applications should be based on the reliability of the materials under these conditions. In order to experimentally assess the reliability of these materials, it is necessary to first quantify the thermal conditions expected at the die attach layer. The following is a study of the temperatures and temperature cycling conditions seen at the die attach layer, given a wide range of pulse power inputs.

3.3.1 Simulation Set-up

In order to simulate a wide range of pulse inputs, a flexible input program was created using Matlab. The program outputs a quasi-square wave function with variable parameters that include pulse width, duty cycle, amplitude and number of pulses, along with rise time and fall time. This allows us to fully describe the transient heat flux conditions. A representative input is shown below in Figure 22.

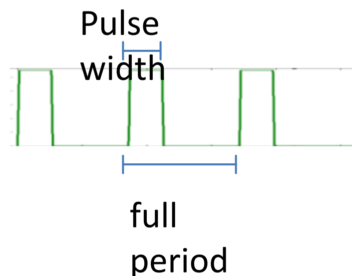


Figure 22: representative pulse input

3.3.2 Results: Thermal Conditions at Die Attach Layer

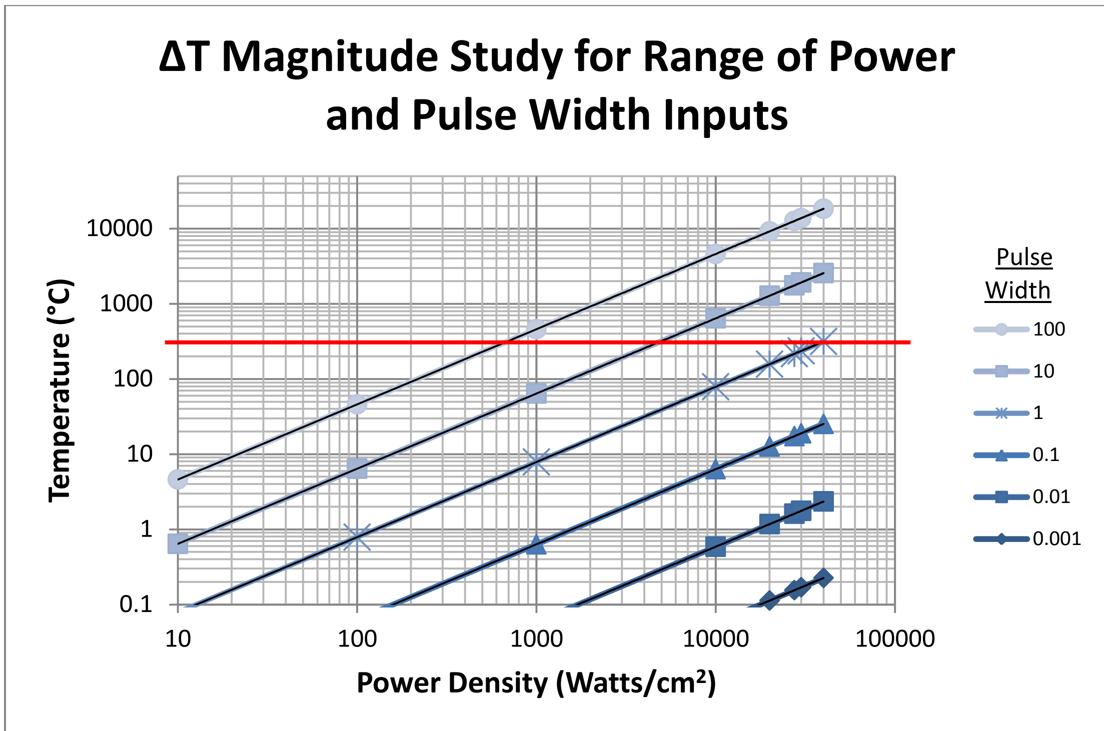


Figure 23: Thermal conditions at die attach layer for a single pulse

Figure 23 shows the change in temperature experienced at the die attach layer for a single pulse, given a wide range of input parameters. Clusters of data points above 10,000 W/^{cm2} are present because data was collected for Power density of 27,500, 30,000, and 40,000 W/cm^2. These were specific parameters of interest based on expected applications by the Army Research Laboratory.

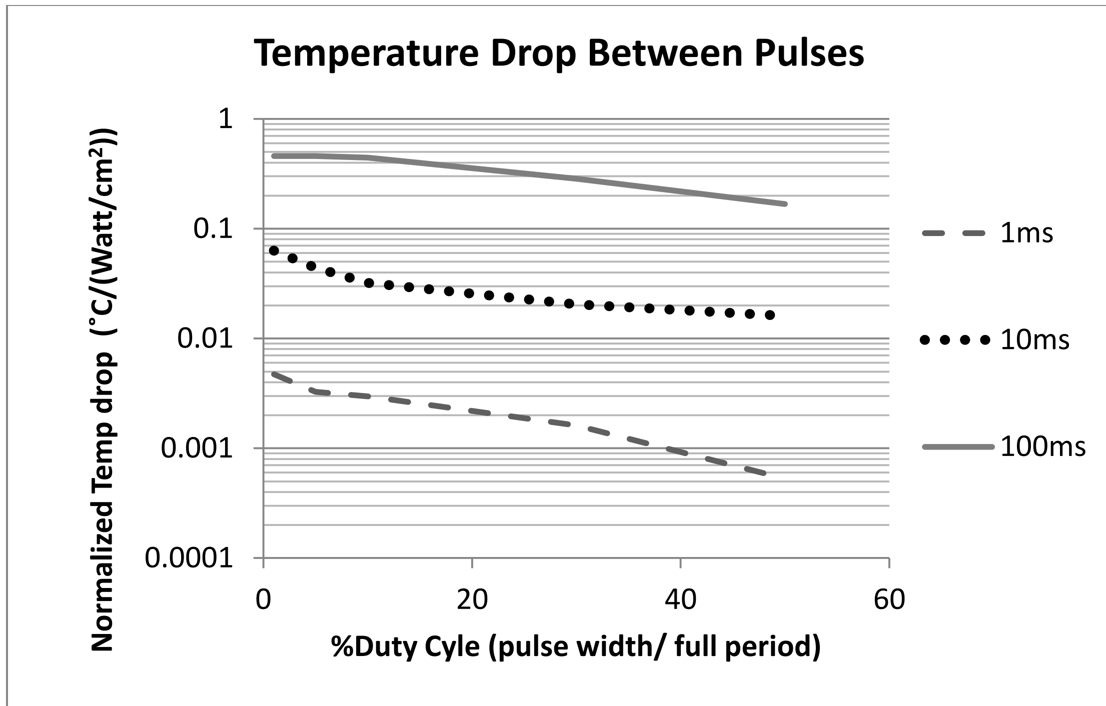


Figure 24: Temperature Drop between pulses as a function of duty cycle

Figure 24 shows the change in temperature as a function of duty cycle for pulse trains. As duty cycle increases, the fraction of time the system has to cool decreases, so the temperature drop is smaller. Here we see again that temperature is largely dependent on pulse width. Also note that pulse widths less than 1ms do not have time to cool, even with a very small duty cycle. For pulse widths less than 1ms, the system would have to off for a duration that is orders of magnitude greater than the pulse width before the temperature of the die attach starts to decrease. At this point the pulse profile is not considered a pulse train, but independent pulses, and is more relevantly considered using the data in Figure 23.

3.3.3 Analysis: Thermal Conditions at the Die Attach Layer

With enormous heat fluxes like 10,000 W/cm^2 and above, we see temperature rises that are unreasonably high when pulse width is longer than 1 ms. These results clearly highlight the limitations packaging technology puts on pulsed power applications. They also show that such high power is still manageable as long as the pulse width is sufficiently short. The red horizontal line indicates the limit of manageable temperature rise. Everything below the red line is relevant for experimental study going forward.

3.3.4 Frequency study

After running the simulation for the parameters of interest, a further investigation was conducted to determine the effect of pulse frequency on die attach temperature rise. Instead of pulse bursts of only a few consecutive pulses, this frequency study inputs a continuous string of pulses. Here the question of die attach material effect is revisited, to determine if temperature differences become relevant. The prior silicon chip parameters were used for these simulations: Current amplitude: 5500A, Voltage amplitude: 10V, h_{eff} = 10,000 W/mK

Results: Frequency Effect on Die Attach Material Selection

Again, the effect of die attach material on transient thermal response was small and independent of frequency. At the frequencies observed, die attach material has no significant impact on the thermal behavior regardless of whether it was high frequency, as shown in Figure 27, or low frequency, as shown in Figure 29. For the high frequency case, the difference in temperature between the different die attaches was only 0.1% of the total temperature rise. For the low frequency case, the

difference in temperature for the different die attaches was only 0.06% of the total temperature rise.

Results: Frequency Effect on Thermal Conditions

The frequency did affect the type of cycling environment the die attach would encounter in use, and therefore the type of stress against which the die attach reliability should be evaluated. Figure 25 shows that for a 0.5 s half cycle pulse, the device nearly has sufficient time to heat to steady-state temperature and cool to ambient with each pulse. There is minimal ratcheting to a constant elevated temperature. This subjects the die attach to a much more severe ΔT condition, but for many fewer cycles (because of the longer period). This is even truer for the 5 s half cycle pulse shown in Figure 29. Figure 26 shows that a 50ms half cycle pulse begins to show more of the ratcheting and reduced ΔT phenomenon, and Figure 27 shows that a 10 ms half cycle pulse has very similar characteristics to the shorter pulses demonstrated in the first part of the work. For the 10 ms half cycle pulse, the ΔT was less than 0.036 °C/W/(cm^2), against a background increase in temperature of 0.545 °C/W/(cm^2). That is a local ΔT of less than 1% of the total temperature increase.

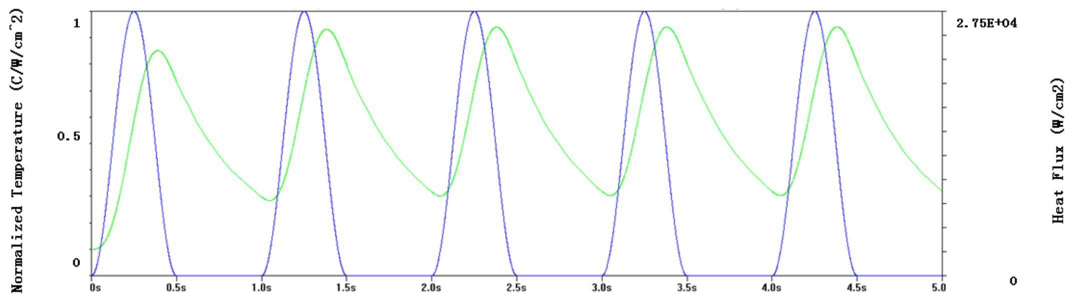


Figure 25: 1Hz (0.5s pulsewidth) for 5sec

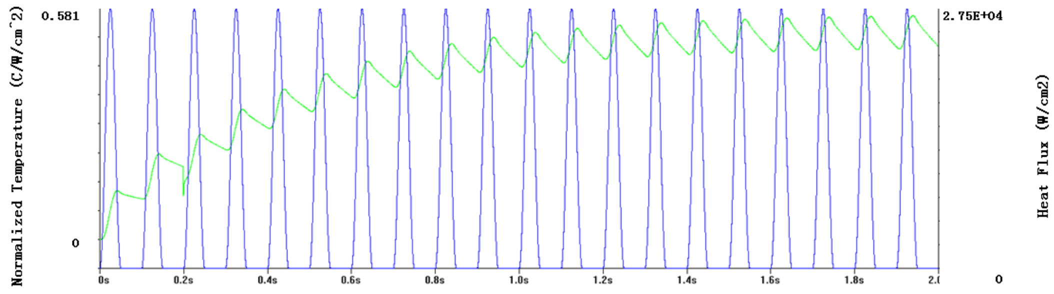


Figure 26: 10Hz (50ms pulsewidth) for 2sec

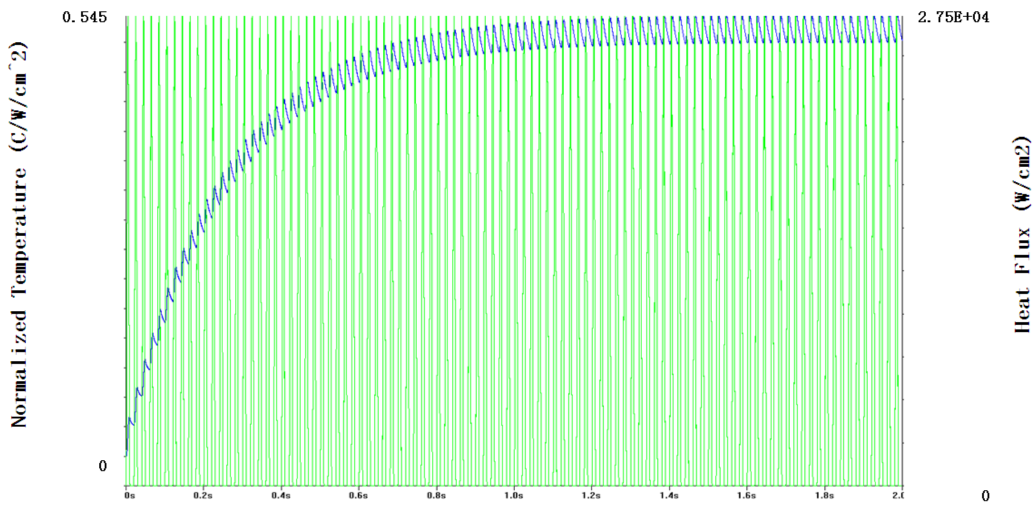


Figure 27: 50Hz (10ms pulsewidth) for 2 sec

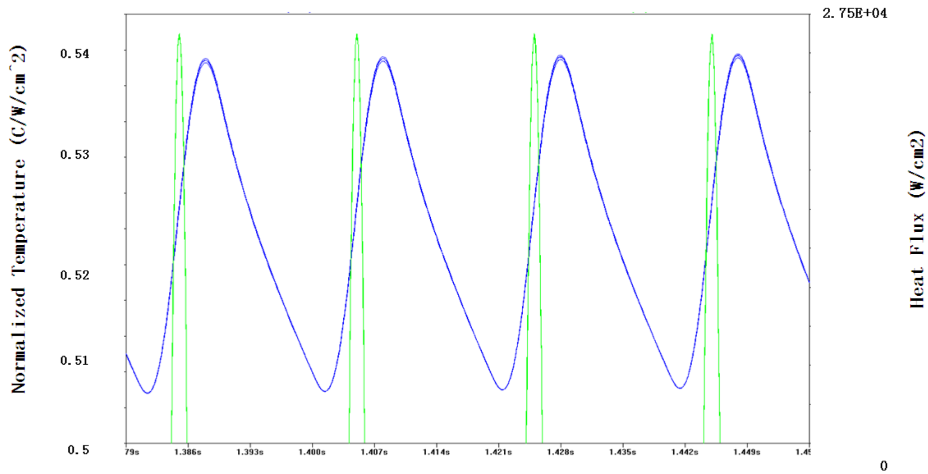


Figure 28: Expanded view of ΔT for 50Hz simulation in steady state

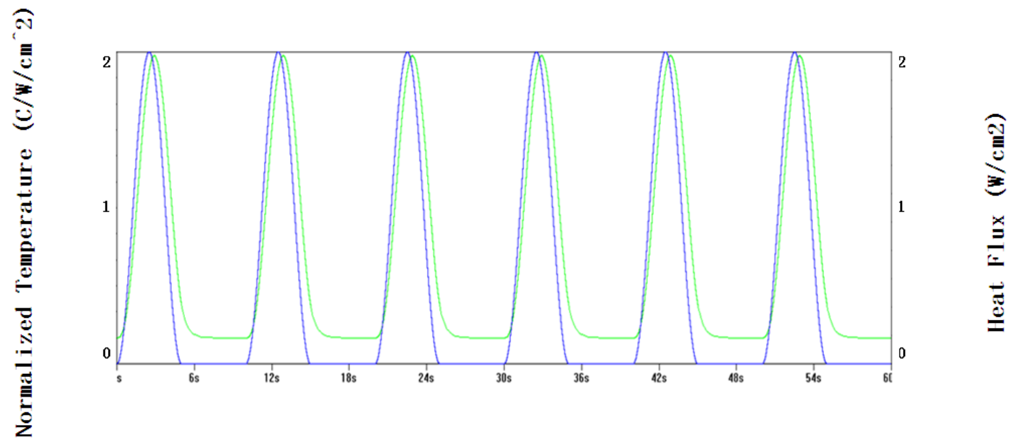


Figure 29: 0.1 Hz for 60sec

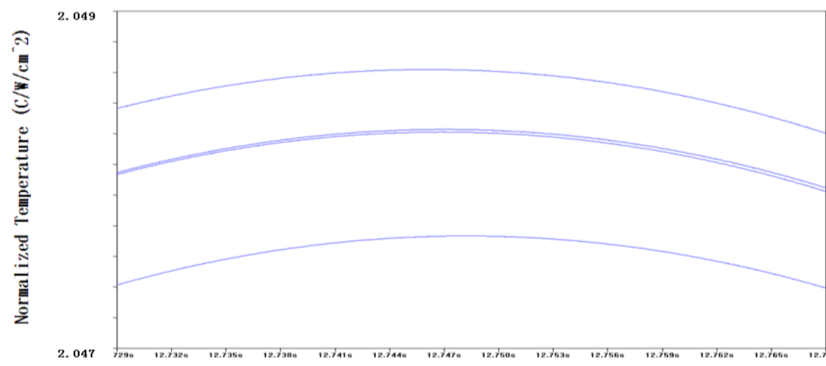


Figure 30: Expanded view of die attach effect in 0.1 Hz simulation

Chapter 4: Experimental Work

The simulations revealed that thermal response of the system is not a function of die attach material. They also allowed us to characterize the thermal conditions experienced by the die attach during high power transient loading. The following is a description of the experimental setup designed to create these thermal conditions, and ultimately assess the reliability of die attach exposed to such conditions.

4.1 Experimental Scope and Rationale

Limitations of current commercially available packaging technologies, processing capabilities and power restrictions motivate us to limit the scope of the experimental component of this research to just a section of the parameters that were simulated. Also, using our understanding of the failure mechanisms associated with thermal cycling, we can adjust the parameters of the experiment even further to a more cost and time effective range. Mechanical failure due to thermal cycling has historically focused on 2 mechanisms: fatigue and creep. Time-independent fatigue is brought on by plastic deformation that accumulates under cyclic loading. Creep occurs when a material experiences a mechanical stress that lower than that which causes plastic deformation, but under which damage is accumulated over time by the material's viscoelastic and viscoplastic response to the stress at a given temperature. While the material is not yielding in its classical definition, material is caused to displace by other creep related mechanisms at a slow rate. The longer a material is under load and the higher the environmental temperature, the greater the fraction of the total damage will be due to creep. Previous studies [23] showed that dwell time for thermal cycles

directly affects fatigue life. It is expected, based on the literature [12] that under a threshold of 15 seconds/half cycle, creep becomes negligible for most metallic solder materials and the only mechanisms for failure are assumed to be due to time-independent plastic deformation. For this reason, we can expect that die attach failure will be characteristically the same for pulse durations on the order of 200-300ms as they would be for much shorter durations. Thus the study should accurately correlate failure mechanisms for very short pulse widths, even if the test conditions are slightly longer than the conditions simulated. This allows the test set-up design to be adjusted to power and cooling levels that are more reasonable and cost effective. Less power and typical cooling capabilities mean the dwell time for each pulse will need to be longer in order to reach the desired cycling temperatures.

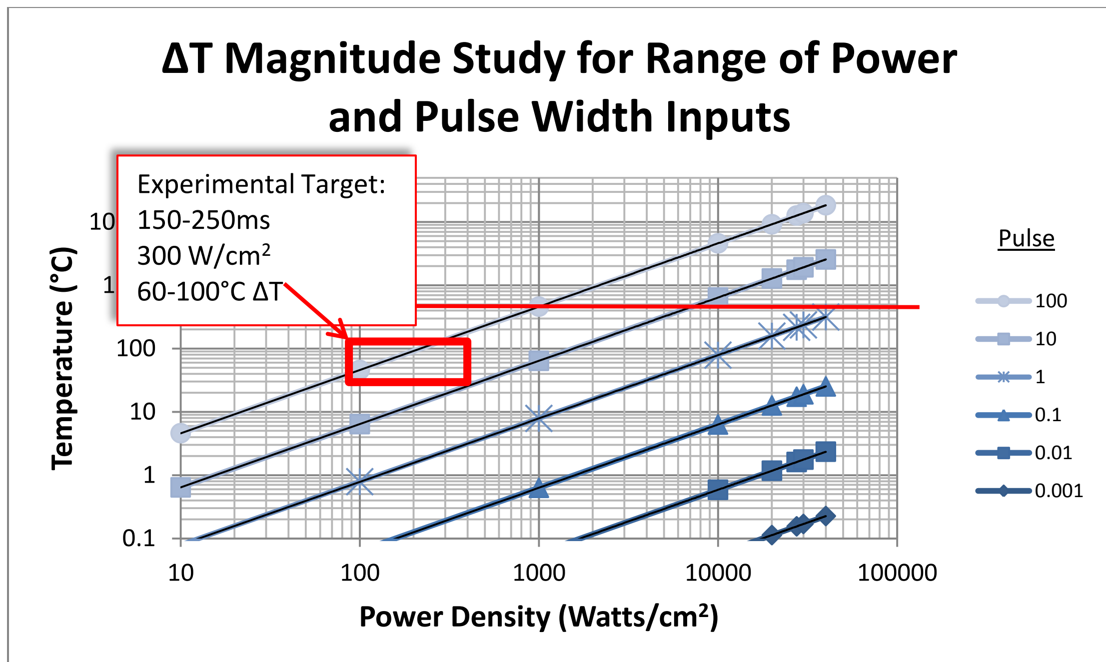


Figure 31: Experimental scope and how it relates to what was simulated

Based on the previously stated, Figure 30 graphically depicts the Experimental scope.

4.2 Physical constructs

4.2.1 Representative Chip Stack

The sample chip stack is selected with the goal of exposing the die attach layer to thermal stresses similar to those expected in actual pulse power electronic devices. The most relevant characteristic is, of course, the CTE mismatch between the two bonded layers. The power electronic devices represented in simulation are silicon or silicon carbide die, with a footprint on the order of 1 cm^2. The substrate would most likely be direct bonded copper (DBC) or bulk copper. The simulations modeled DBC. Table 3 shows the thermal properties of relevant materials.

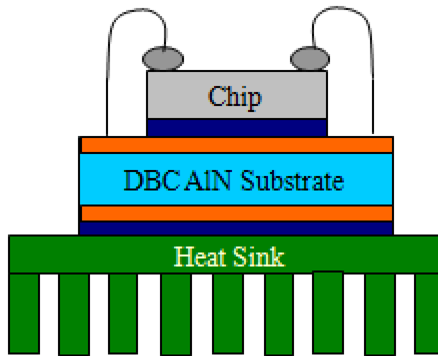


Figure 32: chip stack being experimentally emulated [11]

Figure 32 depicts the chip stack who's characteristics we are attempting to mimic

Table 3: Thermal Properties of Potential Adjacent Materials [24] [25]

Material	K(W/m*K)	C_p (J/g°C)	CTE(μm/m-°C)
Copper	398	0.385	17
Alumina	32.3	0.9	7.1(@127°C)
BeO	130	24.7	7
AlN	80-100	0.74	4
Si	125	.794	3
SiC	2.3-4.9 cm	.92	4

After several attempts with various devices and chip stacks, we ultimately found an adequate solution in the following configuration.

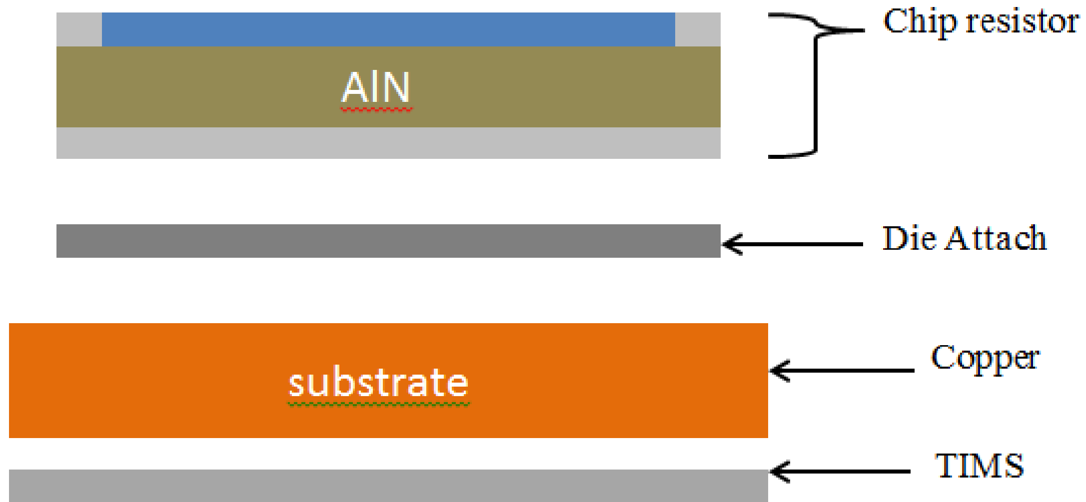


Figure 33: Schematic of experimental chip stack

A chip resistor is selected as the device, because it provides quasi uniform heating so as to minimize hot spots, and more accurately correlate with the 1-D model. The AlN substrate of the chip resistor provides high thermal conductivity needed for rapid heat transfer, and more closely matches the CTE of Si or SiC power devices than Alumina. A copper substrate was selected because it creates sufficient adequate CTE mismatch for failures to occur quickly. Compressible foil is used as a thermal interface material between the copper substrate and the heat sink, because its thermal characteristics are more controllable than a thermal grease, and its conductivity can be higher if enough compressive force is applied. See Figure 34.

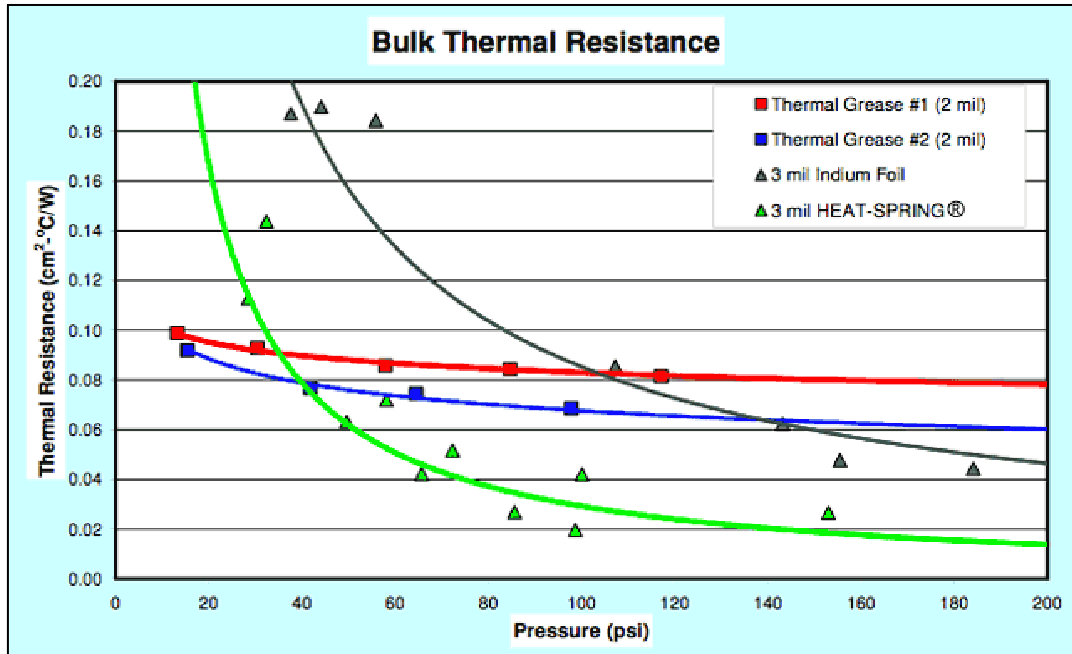


Figure 34: Thermal resistance for compressible foil TIM [26]

The Thermal conductivity of thermal grease varies with each application. The nature of the in-situ monitoring and the thermal cycling characteristics demand a high level of consistency to be effective. Variations in the thermal interface material cause variations in the temperature response of the system that are on the same order of magnitude as the variations we expect for detection of die attach degradation. The compressible TIMS is inherently more consistent because its thickness is constant and uniform. With consistent applied force, the TIM foil is the best candidate for creating repeatable thermal conditions during pulsed loading. The TIM, called Heat Spring®, is made by Indium Corporation. An image of the product is shown in Figure 35 below. Its rippled texture allows it to effectively fill imperfections and gaps between two materials when it is compressed.

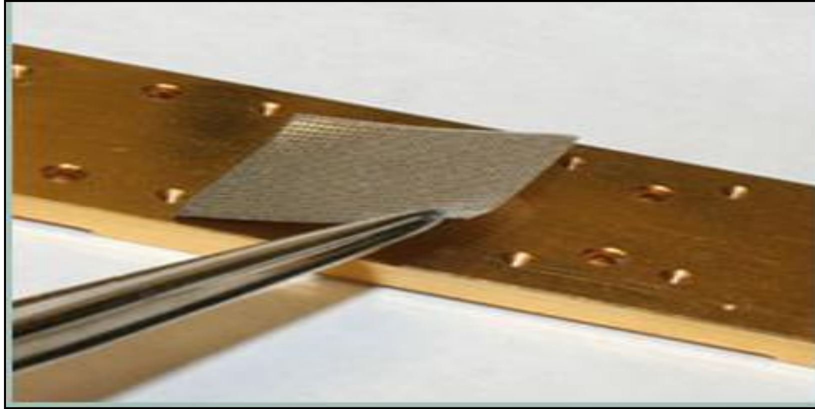
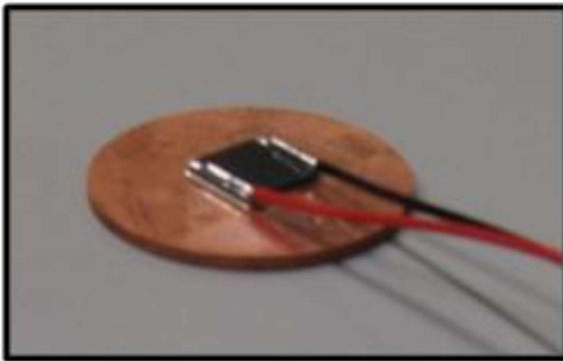


Figure 35: TIM foil being positioned for use [26]

The actual samples as processed are shown below in Figure 36. Here they have not been placed in contact with the heat sink. The TIM (Figure 35) is placed under the copper disc.



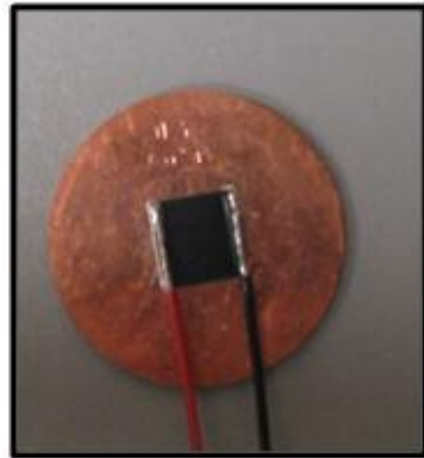


Figure 36: As-processed Resistor Sample

4.2.2 Clamping system

The clamping system is designed to provide constant pressure to the sample during cycling. It must also allow for removal and reinstallation of the sample periodically throughout testing. It is critical that the same amount pressure be applied every time the sample is reinstalled to maintain a constant thermal conductivity throughout the stack. The nature of the in-situ monitoring with the IR camera demands that the thermal signature of each sample does not vary due to any variable other than the degradation of the die attach. Again, slight variations in pressure cause the thermal signature to change on the same order of magnitude as is expected when the die attach degrades. In order to maintain a high level of repeatability, commercially available vice –grips are used. These can be clamped and unclamped easily, but more importantly their clamping force can be preset. Figure 37-Figure 39 below show the clamps.

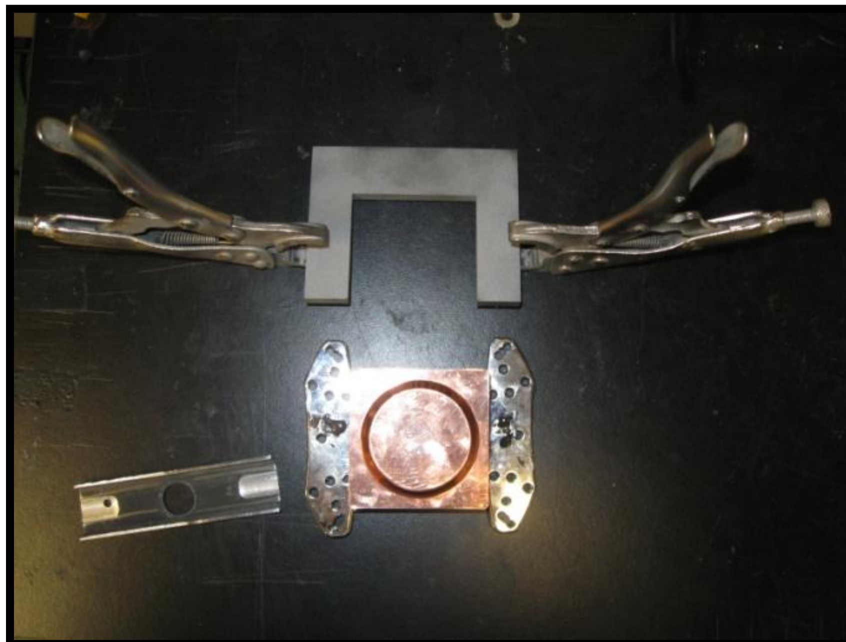


Figure 37: Clamping system components

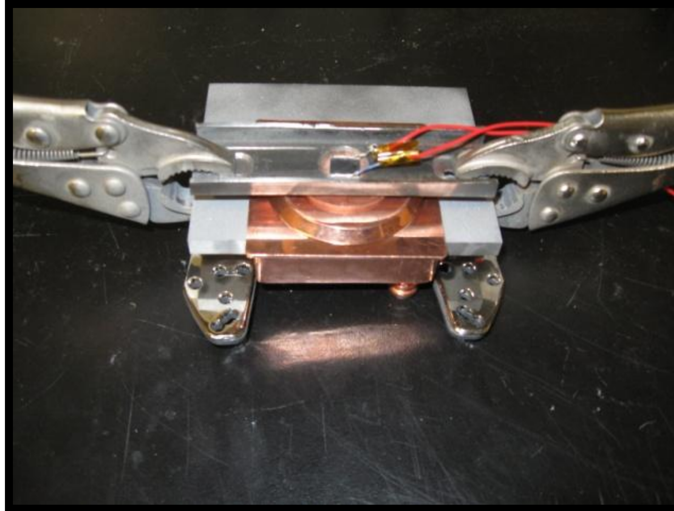


Figure 38: Clamping system assembled with sample in place

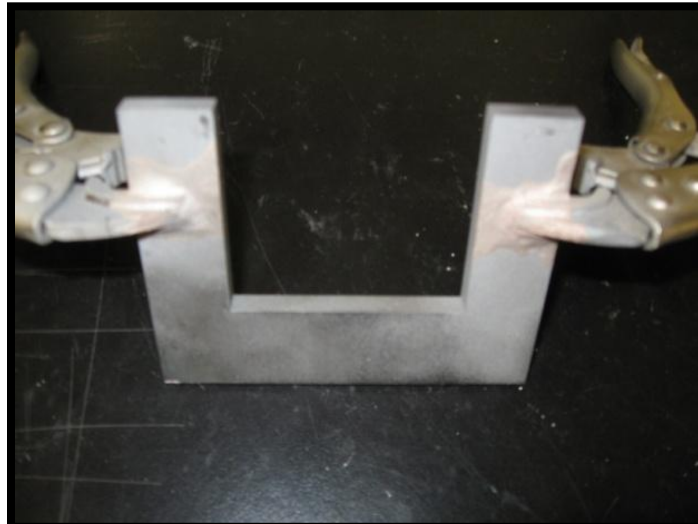


Figure 39: Clamps brazed to Steel bracket

Figure 40: Clamp top plate

The clamps have been bonded to a steel flange using a high temperature brazing process (Figure 39). This process was necessary because the components are case-hardened steel. The flange slides around the cold plate, and it is friction held in place. The top holding plate (Figure 40) is used to secure the sample in place. The hole in the center exposes the top surface of the sample so that it can be observed with the IR camera. Aligning channels are cut on either side in order to ensure the top plate is positioned properly with respect to the top jaw of the clamps.

4.2.3. Switching circuit

The circuit is designed for the specific sample device being used. For this study, a 50ohm resistor is used for the sample, so the switching design and power source are developed to accommodate. Main components of the test bed can be used for other devices, including semi-conductor power devices, but changes of minor design characteristics of the circuit would be required. Figure 41 shows a schematic of the used for this study.

Resistor Circuit

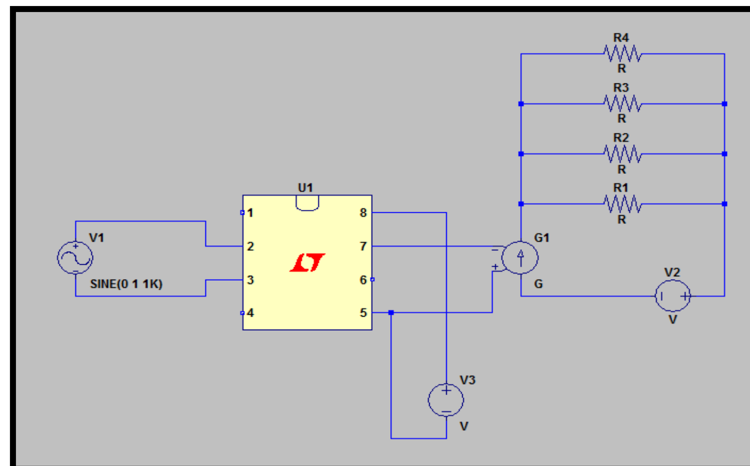


Figure 41: Resistor circuit schematic

The circuit is driven with a pulse signal sent from a waveform generator whose output is digitally controlled based on parameters of pulse width, duty cycle, and amplitude, frequency, pulse-train (number of consecutive pulses), waveform, rise time, fall time, and total duration of pulsing program. Figure 42 shows the front display of the pulse generator.

Figure 42: Digital Pulse Generator

The small voltage signal from the pulse generator is fed to an optically isolating MOSFET switching device called an opto-coupler. This component controls the output to a mechanical relay. While the opto-coupler was originally employed as a necessary isolation component for IGBT switching, it proved a convenient switching intermediary for the mechanical relay, because the switching voltage required for the relay nearly exceeded the output voltage capabilities of the pulse generator. The following describes the inner workings of the optocoupler itself. Figure 43 provides the pin layout for the optocoupler.

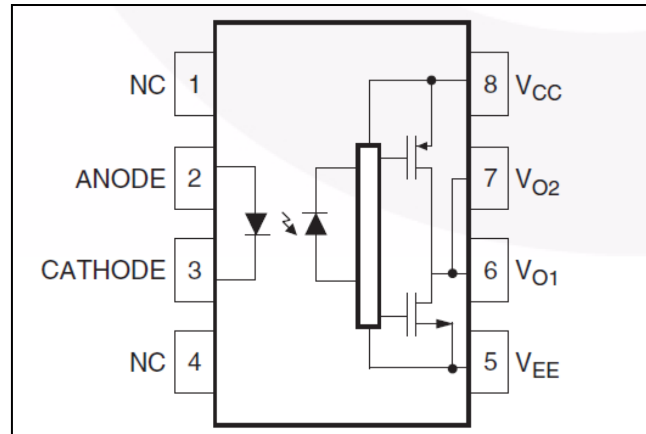


Figure 43: Optocoupler pin diagram [27]

Pins two and three receive the positive and negative input from the signal generator, and they are connected to an LED. Pins five and eight are connected to the positive and negative terminals of a DC Power Supply. This DC Power Supply outputs a voltage sufficiently high to switch the mechanical relay. Pins six and seven are identical and they output a signal corresponding to the input from the signal generator, but with an amplitude determined by the Power Supply. The LED controls the gate voltage of the two MOSFETs in this totem pole configuration. If you consider a standard square wave input by the LED, when the signal is in its high condition the LED is said to be on. In this instance the top MOSFET is also on and the bottom MOSFET is off. Therefore the output pins have a voltage equal to V_{CC}, and it is referenced to V_{EE} from the power supply. When the LED is off, the top MOSFET is also off and the bottom MOSFET is on, which provides the output pins with a zero voltage referenced to V_{EE}. In this way, the output pins and ultimately the voltage across the relay are isolated, while receiving a pulsed signal of sufficient amplitude to cause the relay to switch.

The commercially available chip resistors are rated at 50 ohms. It was calculated that with this resistance, an upper limit of 120 volts AC current would be sufficient to create the thermal conditions we were seeking. The readily available power requirement was one of the many reasons chip resistors were selected for preliminary tests. The power dissipation would be 288W.

A continuously variable Transformer was used to control power input from the 120VAC source. Its mechanical dial allows the user to control Voltage as a percentage of the source voltage. Exact voltage output was measured with a multi-meter.

4.2.4 Chassis

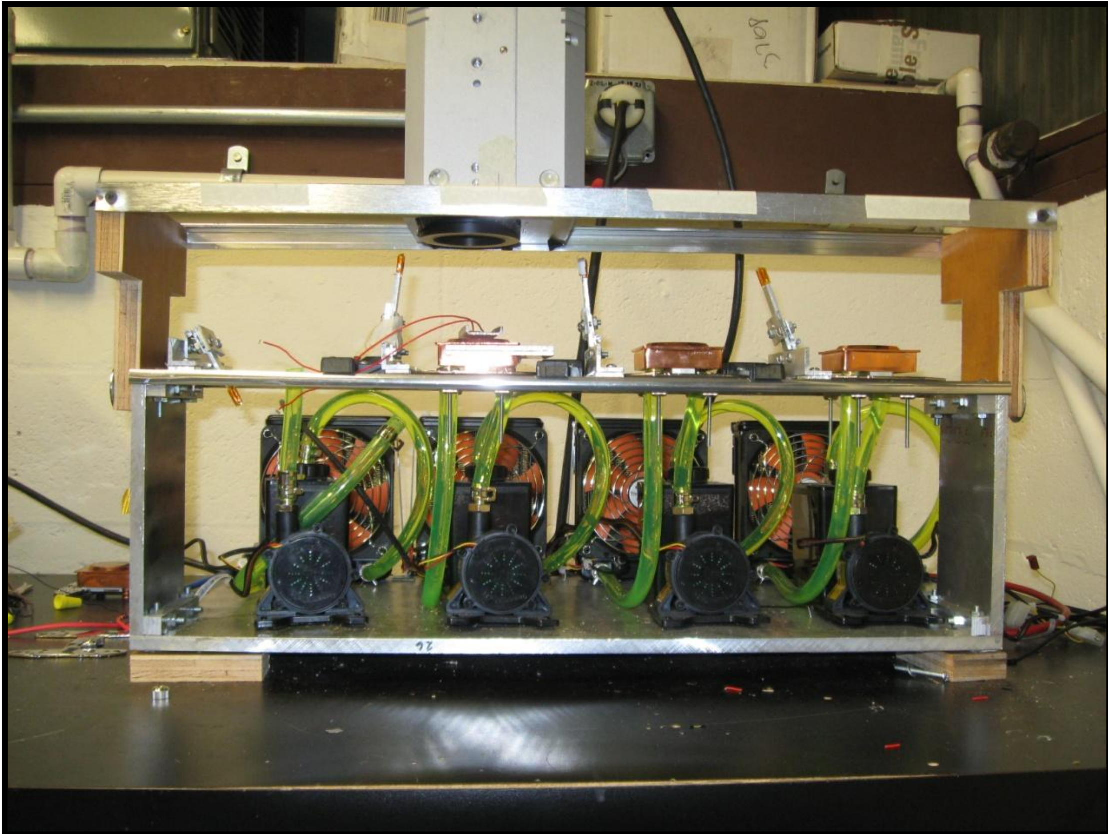


Figure 44: Test chassis

Figure 44 shows the fully assembled chassis. There were numerous design objectives for the chassis. It had to allow for the removal and reinstallation of samples with relative ease. It had to house the cooling system safely to avoid any fluid/electrical interactions and also had the support the IR camera in such a way as to allow consistent measurements, and to be able to move from one sample to another. It was designed to cycle 4 samples at the same time. The IR camera is supported by a rigid sliding channel system, providing ample support as well as flexibility to adjust movement in the x-y plane. The distance from the camera lens to the samples was determined based on the optimal focal range.

4.2.5 In-situ monitoring with infrared camera

Figure 45: Infared camera mounted on top of test chassis

Figure 45 shows the infrared camera mounted on the chassis. In-situ monitoring with the infrared camera allows for direct detection of changes in the temperature at the top surface of the sample. As the die attach degrades the thermal performance of the stack will decrease, causing the sample to heat up [21]. The software associated with the IR camera can record still images as well as videos. It also has a variety of analytic tools to assist in data processing. The IR Camera was calibrated using thermal couples. The top surface of the resistor samples were shown to have consistent emissivity. Surrounding structures and ambient lighting were shown to have a consistent interference affects that were given proper consideration in the calibration.

4.2.6 Scanning Acoustic Microscopy

[28] SAM imaging uses sound waves to create an image just like medical ultrasounds or SONAR systems. When an ultrasonic wave is incident on an interface of interest, part is reflected back (either in phase or out of phase), and part is transmitted based on the difference in the acoustic impedance between the materials on either side of the interface. For electronic packaging this is extremely valuable because it allows one to see cracks and voids inside a package non-destructively. Since cracks and voids consist only of air, the signal is completely reflected out of phase with no transmission, resulting in a bright white spot on an image taken when the transducer is arranged in such a way as to pick up reflected intensity, and a dark black spot on an image taken when the transducer is arranged to pick up transmitted intensity. Cracks and voids of nanometer thickness and micrometer length and width can be discerned. X-ray technology offers a similar non-destructive inspection, but there are some fundamental differences that make SAM imaging far superior for degradation detection. X-ray imaging does not pick up delamination or thin cracks very well because it is based on differences in material X-ray absorbance cross-section and thickness in the vertical direction, neither of which are affected by the presence of a horizontal crack.

4.3 Experimental Results

During validation of the test apparatus, it was determined that several parameters affecting the temperature profile of the chip stack are easily affected by removal and installation of the sample for SAM imaging. Changes in these parameters affect changes in surface temperature on the same order of magnitude as temperature changes indicative of die attach degradation. These parameters include TIM layer thickness and position, compression force magnitude, compression force distribution, small variations in the voltage of the power supply, and resistance in the circuitry, as well as cracking of the AlN substrate. If any of these parameters change slightly, the temperature at the surface of the chip will vary on the same order as the difference we are attempting to measure. Dispite our efforts to control these variables, several attempts to remove the active device periodically throughout cycling resulted in failure of the device or variation in the thermal signature, which distorted the results and negated valuable data. It was decided that removal and installation of the sample and SAM imaging throughout cycling was not yielding sufficient results to justify to risk to the samples. For this reason, the test was conducted without removing the sample or adjusting the chassis throughout the cycling, until the sample was deemed failed. Also, because of challenges encountered in processing samples with AuSn and Nano-silver and SAC305, the test was conducted using Sn3.5Ag. Sn3.5Ag was less prone to processing issues like high void percentage. It was the best candidate for baseline validation of the test procedure and apparatus. The results were as follows:

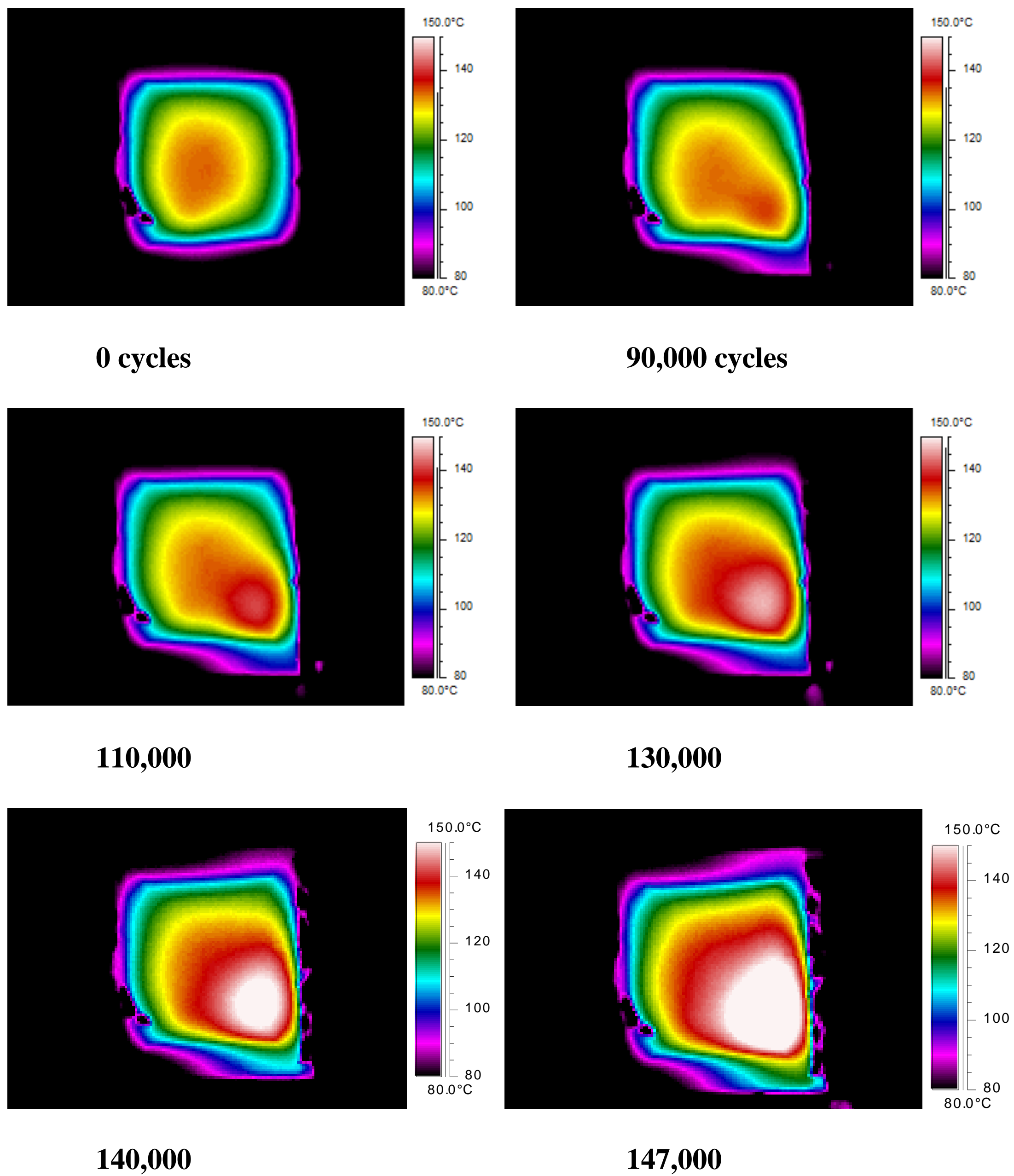


Figure 46: In-situ monitoring of die attach degradation

Figure 46 shows that the pulsed thermal cycling eventually caused the development of a hot spot at the bottom right corner of the sample. As a result, the average temperature of the sample increased to the point where further cycling would have

caused catastrophic failure. For this reason, cycling was terminated at 147,000 cycles. The temperatures are summarized in Figure 47.

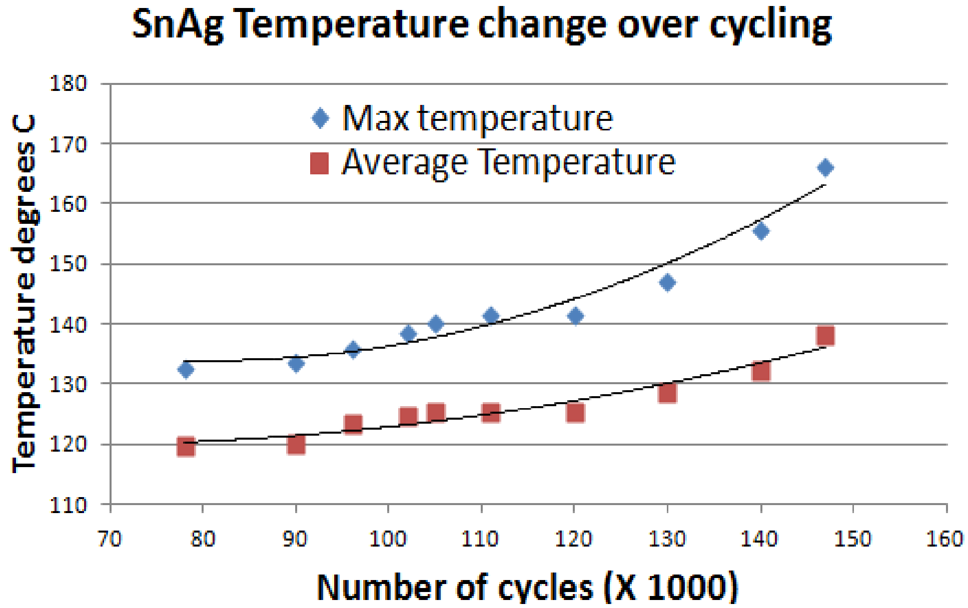


Figure 47: sample temperature variations over cycling

Steady state temperatures were taken at 70% power, incrementally throughout cycling. Figure 46 and the images in Figure 47 depict these steady state readings. The average temperature was calculated over the area of the resistive film. The maximum temperature was extracted from that data which included approximately 4480 data points. The criterion for failure was a 20% increase in T-max. This sample was deemed failed when the maximum temperature reached 158° C. At this point the sample was degrading so rapidly that another 5,000 cycles may have caused the die attach to fail in a way that would have made SAM imaging more difficult. We expected delamination to be the failure mode, and if this had caused enough damage that the die completely detached, SAM imaging would not be useful for detecting the

degradation. For this reason we concluded cycling before catastrophic failure occurred

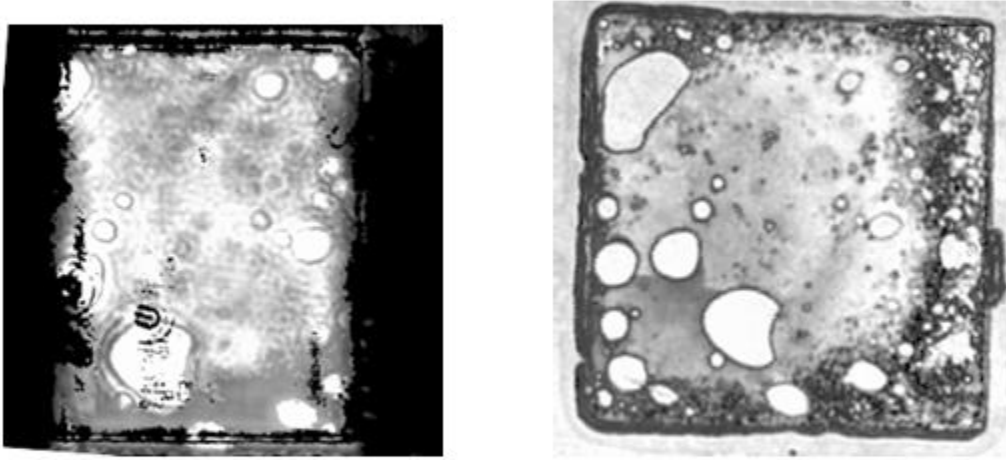


Figure 48: SAM image SnAg. 0 cycles (left). 147000 cycles (right)

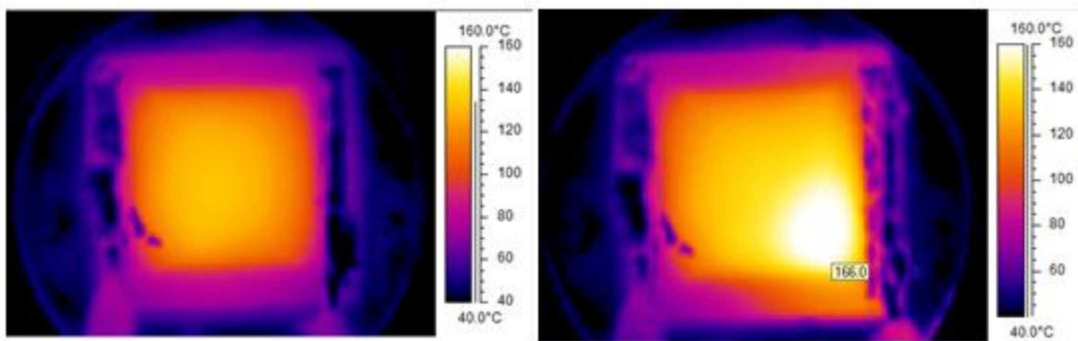


Figure 49: IR imaging SnAg. 0 cycles (left). 147000 cycles (right)

Figure 48 (left) shows the acoustic image of the die attach before cycling commenced, while Figure 48(right) shows the acoustic image of the die attach after 147,000 cycles. The quality of the SAM image prior to cycling is of a lesser quality than that taken after cycling, owing to sample preparation decisions discussed below to limit the effect of imaging on device operation.

The previous device failures occurred in the transition periods between cycling and SAM imaging so it was assumed the samples were affected by the removal and installation in the SAM water chamber, or during sample preparation for imaging. In

short, there were two options for SAM imaging the die attach layer: through the copper substrate or through the resistor. More process control is achieved by imaging through the resistor, but the image quality is not as high as imaging through the copper substrate. To ensure a well-controlled experiment and minimize sources of error it was decided to image the device with the active surface side up, eliminating the need to polish the backside copper, and minimizing the risk of making unnecessary contact with the active top surface by any holding jigs. Because the image was taken from the top side at zero cycles (Figure 48 left), the right and left sides of the image are blacked out by the soldering tabs/wires on the top surface of the device. Figure 48 (right) shows a much improved SAM image, because it was flipped over and the back surface was finely polished. Microsoft Word provides image processing capability that allowed us to invert Figure 48(right), so that it is oriented the same way as Figure 48(left). Figure 49 shows Thermal imaging of the device at the first and last measurement iteration. It clearly depicts the temperature increase and hotspot development in the bottom right hand corner. We can note from these images that the hot spot development is correlated with a drastic dark/light transition in the die attach layer, which indicates a sharp change in material composition, which is indicative of delamination.

Chapter 5. Conclusions

Recent interest in power electronics for applications that induce high power transient heating conditions requires a look at new materials, and new reliability studies tailored to the specific conditions these applications present. While development of

Silicon Carbide power devices is making these new applications possible at the chip level, we do not yet fully understand the impact that they will have on the surrounding packaging. Of particular interest is the die attach layer which often bears much thermal stress.

The work presented in this research effort addresses that knowledge gap by refining a 1-D thermal model and using it to further our understanding of these transient thermal conditions at the die attach layer. With this model, it was determined how die attach material selection affects transient thermal behavior. It was determined that material selection had minimal impact on thermal response, so it became clear that die attach material selection for the design of electronic packages for this unique application should be focused on fatigue resistance/reliability of the material rather than its thermal properties. In order to assess the fatigue life/reliability of die attach materials under this new set of conditions, the research effort involved running numerous simulations to quantify the thermal conditions at the die attach layer for a broad range of transient power inputs, and designing an experimental set up to assess the degradation of die attaches exposed to these unique conditions. A test was completed with Sn3.5Ag that showed failure of the package, and concluded that these unique transient thermal loading conditions do affect the fatigue life of the package.

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