ABSTRACT

Title of thesis: RESONANT CIRCUIT TOPOLOGY
FOR RADIO FREQUENCY
ENERGY HARVESTING

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In this work the operation of a MOSFET based rectifier, composed of multiple stages of voltage doubler circuits used for radio frequency (RF) energy harvesting, is investigated. Analytical modeling of the input stage of the rectifier consisting of short-channel diode-connected transistors is carried out, and the equivalent input resistance obtained is used along with simulation results to improve impedance matching in the harvester. The criteria for voltage boosting and impedance matching, that are essential in the operation of energy harvester under low ambient RF levels, as well as the design considerations for a π-match network to achieve matching to 50 Ω, are elaborated on. In addition their application is demonstrated through simulations carried out using Advanced Design System (ADS) simulator. Furthermore, measurement results of an already fabricated dual-band RF harvester are presented, and the approach taken to improve the antenna design from the harvester chip measured input impedance is discussed. The integrated antenna-harvester system tested was capable of harvesting ambient RF power and generating DC output voltage levels above 1 V.

RESONANT CIRCUIT TOPOLOGY FOR RADIO FREQUENCY ENERGY HARVESTING

by

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Chapter 1

RF Energy Harvesting Survey

Over the past few years there has been a great interest in radio frequency (RF) energy harvesting as a promising source of power for replacing or charging up batteries in different applications including wireless sensor networks and radio frequency identification (RFID) tags [1, 2, 3]. Due to the abundance of RF radiation from television or cell phone towers, sufficient amounts of input power can be extracted in the ISM band, get amplified and converted from AC to DC in an RF harvester.

Several efforts have gone to extracting RF energy directly from the environment [4, 5, 6]. In this thesis, we go beyond the past work by focusing largely on analytical modeling of the rectifier to derive the equivalent input impedance of the circuit. The proposed analytical approach enables us to achieve improved impedance matching between the antenna and the harvester and can be used in conjunction with simulation results to design the harvester with optimum conversion efficiency operating at resonant frequency with maximum voltage boosting.

A harvester consists of an antenna to receive the incoming signals, and the rectifier circuit that is connected to the desired load. An impedance matching network

is generally needed to maximize power transfer between the antenna and the rectifier. The rectifier circuit consists of rectifying elements that convert the AC signal fed from the antenna to a DC signal at the harvester output. A voltage regulator may be implemented between the rectifier output and the load to regulate the undesired ripples. Different configurations have been proposed for the rectifier circuit, that are focused on maximizing the DC output voltage and conversion efficiency of the harvester. Villard voltage doubler is the most widely used rectifier circuit which consists of two diodes or diode-connected transistors and two coupling capacitors, and provides an output voltage that is about twice the input signal amplitude.

1.1 Villard Voltage Doubler

The voltage doubler circuit is essentially composed of two sections in cascade. The first section is a clamped capacitor circuit composed of C_1 and D_1. Assuming ideal diodes, when this circuit is excited by a sinusoid of amplitude V_p, it provides a voltage waveform similar to the input but shifted up by V_p across diode D_1. While the negative peaks are clamped to 0 V, the positive peaks reach $2V_p$. The second section is a peak rectifier circuit that is formed by D_2 and C_2. In response to the voltage across the first diode, this circuit provides a DC voltage of magnitude $2V_p$ across capacitor C_2. Since in the ideal case the output voltage is double the input voltage amplitude, the circuit is called voltage doubler [7].

The basic configuration of a voltage doubler is illustrated in Fig. 1.1. In the

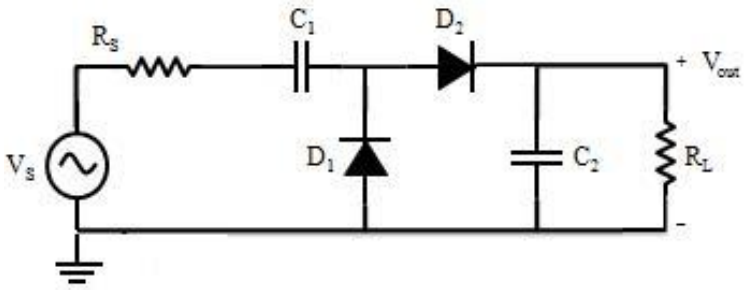

Figure 1.1: Single stage of voltage doubler circuit driving an arbitrary load.

ideal operation, during the negative half cycle of the AC input source, diode D_1 conducts while diode D_2 is off. Thus all the voltage drops across capacitor C_1 and charges it up to the peak amplitude of the input signal. During the positive half cycles D_2 is forward biased while D_1 is reverse biased. Hence both the source voltage and the voltage stored on C_1 drop across C_2 charging it up to a DC value equal to two times the input signal amplitude [8].

Multiple stages of the basic doubler circuit can be cascaded to provide higher output voltages. As depicted in Fig. 1.2, the output of each stage provides the DC input of the next stage, while the direct coupling from the source provides the AC input for each stage. Despite achieving higher output voltage, the increase in number of stages degrades conversion efficiency due to increase in power dissipation. The trade-offs involved in cascading voltage doubler stages have been extensively studied in [1], [5] and [9].

Output voltage and RF to DC conversion efficiency are the two primary per-

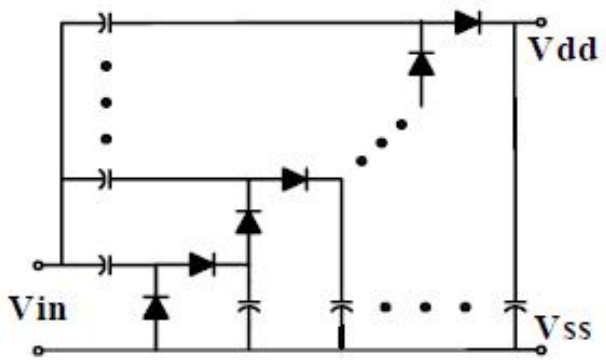

Figure 1.2: N-stage voltage multiplier [10].

formance parameters of an RF energy harvesting circuit. A straightforward DC steady-state analysis of the doubler circuit with real identical diodes yields the following expression for the output voltage [10], [2]:

$$V_{out} = 2n(V_{in} - V_d) \tag{1.1}$$

where n is the number of stages, V_{in} is the amplitude of the input RF signal, and V_d is the voltage drop across each rectifying element, i.e. a p-n junction diode or a diode-connected transistor. For the case of ideal diodes with no threshold voltage, (1.1) simplifies to $V_{out} = 2nV_{in}$ as expected. Conversion efficiency is defined as the ratio of the DC power at the output of the voltage multiplier to the incident RF power available at the antenna [10], [11]:

$$\eta = \frac{P_{dc}}{P_{rf}} = 1 - \frac{P_{loss}}{P_{rf}} \tag{1.2}$$

In addition to the number of stages, other parameters including effectiveness of power matching, the width of the diode-connected transistors, and load impedance

affect the power conversion efficiency in an RF harvester.

1.2 Rectifier Configurations and Devices

Different implementations of diodes have been investigated for RF harvesting. Schottky diodes were originally used due to their inherently low turn on voltage, low conduction resistance and low junction capacitance [12]. Since diodes in the voltage multiplier must have a switching time smaller than the period of the input signal, Schottky diodes are preferred because they are typically faster than normal diodes. Furthermore, higher saturation current can be obtained using Schottky diodes which in turn is shown to result in higher conversion efficiency [9]. However, integration of a Schottky diode is expensive due to its incompatibility with standard CMOS process and has limited applications. As a result, regular p-n junction diodes that are available through a less expensive CMOS process are generally used instead.

On the other hand, using diode-connected transistors, that are compatible with standard CMOS technologies, as rectifying elements has become increasingly popular. Fig. 1.3 depicts an N-stage voltage multiplier implemented by NMOS transistors each with its gate and drain connected together. Transistors with low or zero threshold voltage have been considered [10], even though they have higher leakage current and thus degrade the conversion efficiency of the circuit. In [1], it was demonstrated that regular MOSFETs with proper biasing show a better

performance than low threshold MOSFETs.

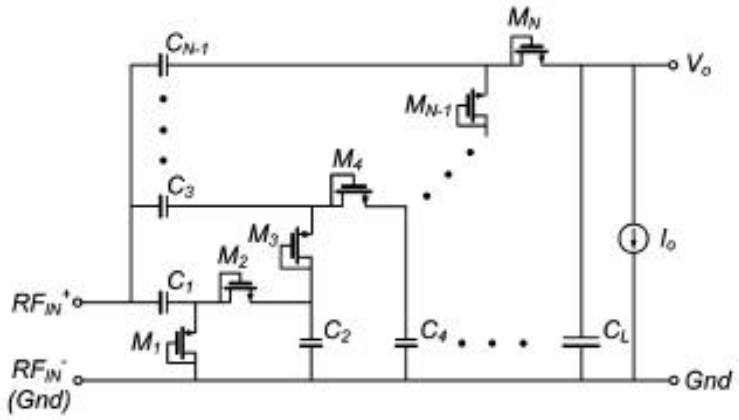

Figure 1.3: N-stage voltage multiplier using diode-connected transistors [13].

The requirement of turning on the diode-connected transistors despite low input voltage amplitudes, has led to different design strategies to reduce the threshold voltage of the transistors. Dynamic gate-drain biasing using an external threshold voltage compensator was discussed in [2]. The rectified output voltage was shown to have the form of $V_R = 2(V_{rf} - V_{th} + V_{bth})$, and thus if the bias voltage V_{bth} was set equal to the threshold voltage of the transistors, RF to DC conversion could be achieved without the influence of V_{th}. A self-driven synchronous rectifier was designed by [6] that used floating gate MOS transistors and could be programmed to maintain the optimum threshold voltage values. However, implementation of floating gates required two polysilicon layers that most CMOS processes do not support. A voltage doubler rectifier using floating gate transistors with NMOS replaced with PMOS was presented in [5]. A MOS capacitor was placed in series with the gate of each diode-connected transistor to design a floating gate device in a standard CMOS process.

The rectifier used in this work is adopted from the circuit developed and implemented in [1] and [14]. As depicted in Fig. 1.4, replacing the second NMOS in the doubler circuit with a floating body PMOS, minimizes the body effect and its corresponding threshold voltage increase. Furthermore, as will be shown in Fig. 1.9, the output voltage is used to create bias voltages at the gates of MOSFETs through a voltage divider network. This technique achieves reduced threshold voltage without incurring additional fabrication costs.

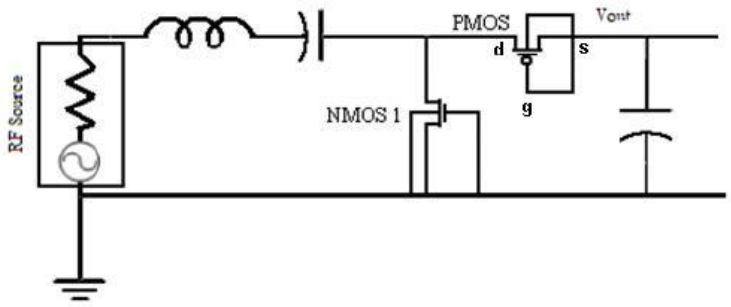

Figure 1.4: One stage of power harvesting circuit analyzed in this work adopted from [1].

1.3 Literature Survey

Joe et al. [15] proposed a simplified diode model and a rectifier circuit model for a low power rectenna rectifying circuit. The models relied primarily on the data obtained from the diode characteristic curve measurements. The zero-bias Schottky

diode model provided relations for diode resistance and capacitance to be matched with the antenna for optimum power transfer at the desired DC output current. The rectifier circuit model consisted of AC and DC equivalent circuits and was used to calculate the RF to DC conversion efficiency.

Yao et al. [10] presented a fully integrated design for a low power and input-independent AC to DC charge pump used in RFID applications. Schottky diodes used in conventional charge pumps were replaced by MOSFET diodes with low or zero threshold voltage. The proposed charge pump comprised of a basic MOS charge pump to convert the input RF signal power into DC voltage, in series with a low power regulator to stabilize the output DC voltage. Moreover, it was shown through the analysis of the diode-connected transistor power loss, that there was a single output current that corresponded to the largest conversion efficiency.

A resonant voltage boosting network followed by a two-stage voltage doubler rectifier was proposed by Yan et al. [3]. Since at low RF power levels the peak voltage of the AC signal is much smaller than the diode threshold voltage, a resonant-tank based voltage boosting network designed for a given frequency to maximize the boosted voltage amplitude, was employed (Fig. 1.5). A Villard voltage doubler circuit consisting of Schottky diodes was also compared with a Dickson voltage multiplier in which the AC signal is coupled to the cascaded stages in parallel instead of in series.

Harrist [8] investigated the effect of stacking voltage doubler circuits to achieve higher output voltages. The overall output voltage was related to the open circuit output voltage of each stage V_0 and the number of stages n through the following equation:

$$V_{out} = \frac{nV_0}{nR_0 + R_L} R_L = V_0 \frac{1}{\frac{R_0}{R_L} + \frac{1}{n}} \tag{1.3}$$

where R_0 is the internal resistance of each stage and R_L is the load resistance. This equation indicates that as the number of stages increases, the increase in the output voltage will be less each time and at a certain point becomes negligible.

RF power harvesting through inductive coupling was found to be a promising alternative source of power for implanted devices in the study by Sauer et al. [16]. Inductive coupling proved efficient over a distance of up to 25 mm between coils, with the primary coil driven with an RF amplifier to create an electromagnetic field, and the secondary coil on the implanted device used to induce a current and hence a voltage depending on the coupling factor and the current through the primary coil. A full-wave rectifier (Fig. 1.6) composed of four PMOS transistors followed by a

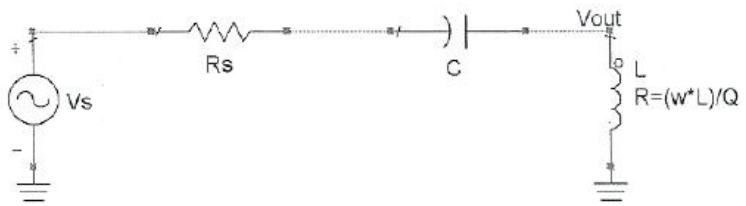

Figure 1.5: Simple resonant tank employed in [3].

low-pass filter was used, and a voltage close to the root mean square of the received sine wave was rectified.

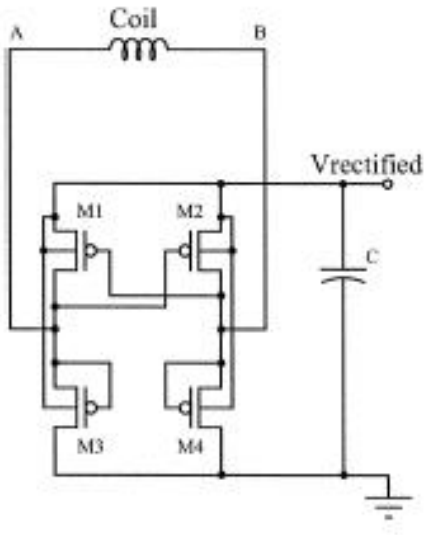

Figure 1.6: Rectifier circuit used for inductive coupling in [16].

Mandal et al. [6] investigated the theoretical issues in the design of power harvesting systems in terms of the trade-off between matching network gain and bandwidth. An optimization metric was defined as a function of the rectifier turn-on voltage and equivalent circuit capacitance, and utilized to obtain optimum number of rectifier stages. The most efficient MOSFET-based rectifier structure designed was a self-driven synchronous rectifier called the four-transistor cell as illustrated in Fig. 1.7. The DC output voltage across V_H and V_L is equal to $V_{DC} = (V_H - V_L) = (2V_{RF} - V_{drop})$, where V_{RF} is the voltage amplitude of V_P or $\bar{V_p}$, and V_{drop} represents the losses due to switch resistance and reverse conduction. In order to independently program NMOS and PMOS threshold voltages, each

simple rectifier cell was subsequently replaced with a floating-gate version, and the optimum threshold voltage pair that maximized the DC output voltage was found.

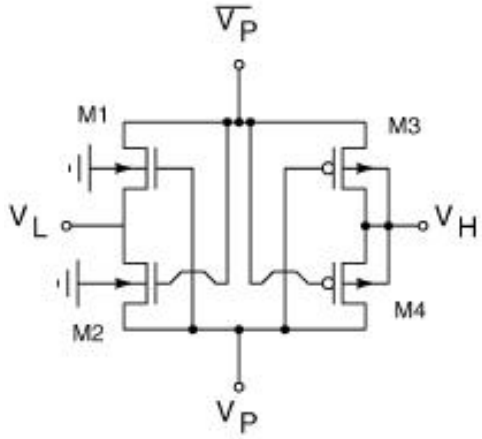

Figure 1.7: Four-transistor rectifier cell developed by [6].

Umeda et al. [2] replaced the conventional rectifier circuit with a rectifier with dynamic gate-drain biasing for each diode-connected NMOS transistor. Since this modification decreased the effective threshold voltage from V_{th} to $V_{th} - V_{bth}$, rectified voltage levels of approximately twice the RF signal amplitude could be obtained. The reference voltage applied between the gate and drain V_{bth}, was supplied from an external secondary battery.

An RF energy harvesting system using floating gate transistors as rectifying elements was designed by Le et al. [5]. In order to maximize the input voltage to the rectifier and thus improve the efficiency of the RF-DC power conversion, a resonator with high loaded quality factor between the impedance of the receive antenna and the rectifier circuit was formed and its effect on the operating bandwidth

was considered. The proposed voltage doubler consisted of PMOS diode-connected transistors and MOS capacitors to create gate-source bias as shown in Fig. 1.8. Due to the trade-off between the size of the transistor and the parasitic capacitance on one hand, and the number of rectifier stages and the effect of the high-Q resonator on the other hand, the number of stages and the transistor width were also optimized.

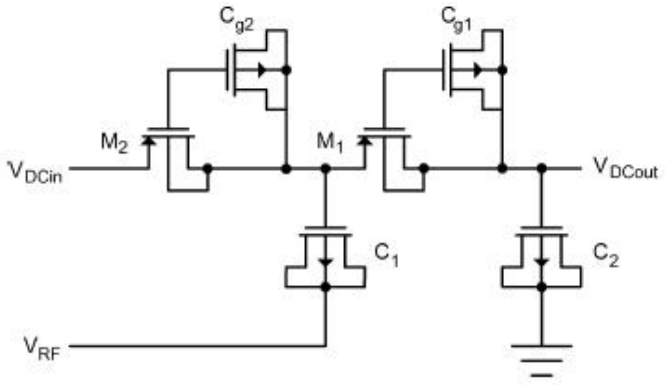

Figure 1.8: PMOS floating gate rectifier studied in [5].

Salter [1] developed an analytical methodology to optimize transistor sizing, number of stacked stages, and threshold voltage for a multi-stage Villard voltage doubler circuit utilizing diode-connected MOSFETs. The DC loop analysis was used to relate the DC output voltage to the input AC voltage, and the AC nodal analysis was employed to relate input AC voltage to input RF energy. Moreover, improvements in the design of RF energy harvesting circuits through on-chip impedance matching were studied. Implementing a matching network resistant to parasitic losses to maximize RF to DC conversion efficiency, utilizing self-biasing through a

voltage divider network to reduce the threshold voltage of diode-connected MOSFETs, and replacing the second NMOS in the doubler with a floating body PMOS to reduce body effect losses, were the primary modifications proposed for an improved power matched Villard voltage doubler circuit (Fig. 1.9).

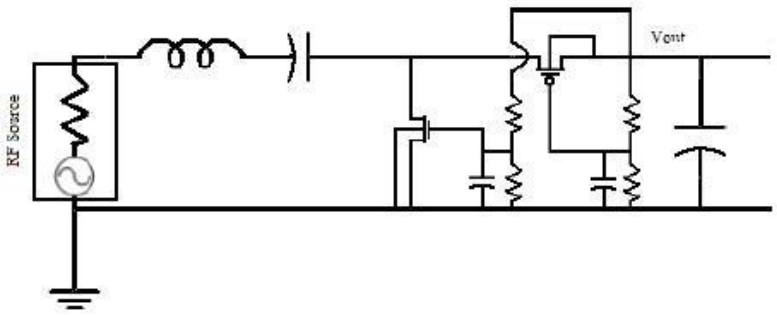

Figure 1.9: Circuit design utilizing sacrificial current biasing and floating body PMOS presented in [1].

In a recent work by Li [14], the floating body PMOS and off-chip DC self-biasing techniques introduced by [1], were incorporated into designing a dual-band energy harvester for 880MHz and 1.8GHz frequencies. On-chip inductors for each frequency were utilized to resonate out the equivalent capacitance of the rectifiers. The enhancement in operation was achieved through voltage boosting that led to output voltages above 1V and conversion efficiencies as high as 0.14 for an input power of only -19dBm.

Barnett et al. [17] presented low-cost impedance matching using an external

shunt inductor, whose value was determined by evaluating the input impedance of multistage rectifiers. The nonlinear current in each diode and the input resistance of the rectifier were obtained by taking the fundamental components of the Fourier series. In a passive UHF RFID transponder designed by Karthaus et al. [12], the printed antenna was power matched to the average input impedance of the voltage multiplier consisting of Schottky diodes. Power losses due to substrate capacitances, and power matching conditions for optimum power supply efficiency and modulation efficiency were discussed.

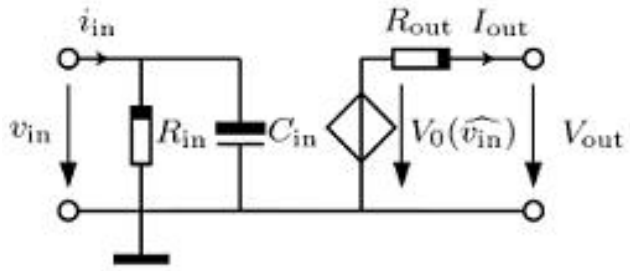

Figure 1.10: Rectifier equivalent circuit used in [11].

Curty et al. [11] developed a model for an N-stage modified Greinacher full-wave rectifier consisting of a voltage doubler and its mirrored circuit in each stage. The steady-state analysis of the rectifier circuit for the ideal and real cases was presented. The equivalent input resistance and capacitance, and the output resistance used in the model were obtained for a constant input voltage amplitude and a constant output current (Fig. 1.10). The numerical approach was based on the extracted I-V and C-V characteristics of a single diode-connected transistor, and showed good agreement with the measurement results.

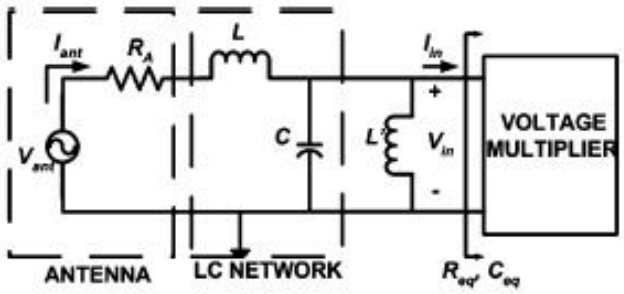

Figure 1.11: Power matching network designed in [9].

An analytical-based model of the N-stage voltage multiplier utilized in passive RFID transponders was derived by De Vita et al. [9]. The equivalent input resistance was expressed in terms of the power consumption of the rectifier circuit consisting of p-n junction diodes and the load, and the average input capacitance was calculated using the SPICE BSIM3 model. The equivalent input impedance of the circuit provided the basis for developing the design criteria for the voltage multiplier and the power matching network (Fig. 1.11). The analysis of matching with variations in the available input power was also presented.

Yi et al. [13] performed a detailed analysis of the N-stage micro-power CMOS rectifier circuit by considering different regions of operation of the diode-connected transistors. Conduction angle, leakage current and body effect were taken into account in deriving analytical expressions for the output voltage and power consumption. Subsequently, different design strategies to achieve maximum voltage or maximum efficiency were discussed.

1.4 Thesis Contributions

This work attempts to investigate the operation of voltage doubler based rectifier circuit used in RF energy harvesting in more detail and make improvements to the design of the harvester system. In particular we present the analytical modeling of the input stage of the rectifier to derive the equivalent input resistance of the circuit. Enhanced impedance matching is then achieved given the input impedance model by using a π-match network and verified through simulation. Besides, the concepts of voltage boosting and resonance that are key to the circuit operation under low levels of RF power, and their interconnection with impedance matching are elaborated. Measurement results of an already designed dual-band energy harvester, including input impedance and output DC voltage at both frequency bands, are provided and compared with simulations. Finally, the methodology for antenna design improvement and the measurement results of the integrated antenna-harvester system are given. The presented analyses set forth the design considerations needed towards an enhanced RF energy harvester.

Chapter 2

Analytical Modeling of the Rectifier Circuit

An N-stage voltage doubler is commonly used as the rectifier circuit in RF energy harvesting. Due to low levels of RF input power, maximum power transfer from the receiving antenna to the input of rectifier through some form of impedance matching network is essential. In an attempt to achieve efficient impedance matching, an analytical model of the input stage of the rectifier circuit is investigated. If the input stage of the rectifier is modeled as an equivalent resistance in parallel with an equivalent capacitance [11, 9, 17], then the goal would be to resonate out the capacitance and to match the resistance with the antenna resistance through a matching network comprised of an inductor and possibly other passive components. Therefore, a precise model that helps us calculate the equivalent input resistance and capacitance can serve as a starting point for harvester design and performance improvement, and can subsequently be verified by simulations and measurements.

2.1 Steady State DC and AC Analysis of the Rectifier Circuit

The expressions for the voltage across and the current through each rectifying element (a p-n junction diode or a diode-connected transistor) are derived in this section by analyzing the operation of a single stage of the voltage doubler circuit.

The results can then easily be extended to multiple stages. The obtained equations will subsequently be used in calculating the power consumed by the circuit and its corresponding equivalent resistance.

There are a number of simplifying assumptions that are made for the presented analysis. The circuit is assumed to be operating in the AC steady state mode. The diodes are initially considered lossless and thus ideal, and later the analysis will be generalized to encompass real diodes. The two coupling capacitors are treated as short circuits in the AC analysis. The condition under which this assumption is reasonable will also be elaborated later. The input power is considered constant, as well as the output current and load. The effect of changing input power level and output resistive load will be addressed in next chapters.

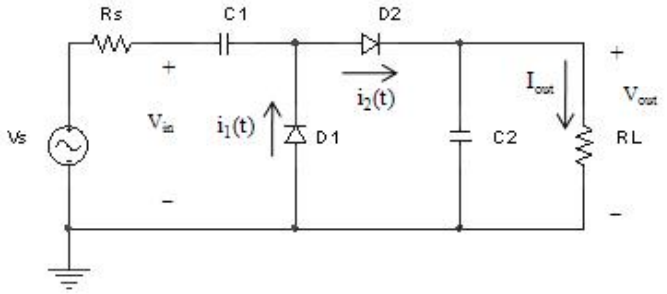

Figure 2.1: Single stage of voltage doubler circuit indicating the current flows.

2.1.1 Single-Stage Voltage Doubler

The doubler circuit that will be analyzed is illustrated in Fig. 2.1. The input voltage to the circuit is a sinusoidal signal $V_{in}(t)$ with amplitude $\bar{V}_{in}$ and angular

frequency ω_0. Denoting the current through diode D_1 by $i_1(t)$ and the current through D_2 by $i_2(t)$, time domain analysis based on conservation of charge yields their relation to the output DC current I_{out}. Assuming ideal diodes that conduct only during half the input voltage cycle when forward biased, in equilibrium we can write

$$\int_0^{T/2} i_2(t)\,dt = \int_0^{T/2} i_{C_2}(t)\,dt + \int_0^{T/2} I_{out}\,dt \tag{2.1}$$

$$\int_{T/2}^{T} i_2(t)\,dt = \int_{T/2}^{T} i_{C_2}(t)\,dt + \int_{T/2}^{T} I_{out}\,dt = 0 \tag{2.2}$$

Noting that in the steady state the amount of charge drawn off by the load from the capacitor during negative half cycles is compensated by the equal amount of charge provided from diode D_2 during positive half cycles, the total current through C_2 sums up to zero. Also since there is no change in the DC voltage across the load, output current is constant. Thus adding the two equalities yields

$$\int_0^{T} i_2(t)dt = I_{out}T \tag{2.3}$$

$$\frac{1}{T}\int_0^{T} i_2(t)dt = I_{out} \tag{2.4}$$

where for simplicity the integration limit for $i_2(t)$ is extended to the entire cycle, even though it is nonzero only during half the period. All the current that passes through D_2 is provided by capacitor C_1 since diode D_1 is reverse biased during this time. In the negative half cycle of the input voltage, D_1 must supply all the charge required by C_1 to recharge C_2 during the positive swing. A similar analysis is presented in [11]. This results in for the following equality to hold

$$\int_0^{T} i_1(t)dt = I_{out}T \tag{2.5}$$

$$\frac{1}{T}\int_0^T i_1(t)dt = I_{out} \tag{2.6}$$

which again assumes $i_1(t)$ being nonzero only during half the period. As demonstrated by (2.4) and (2.6), the output DC current is equal to the average current through each diode during one period. If ideal rectifying diodes are replaced with diode-connected MOSFETs, then the integration limits in these equations must be refined to account for the forward-biased region of operation. This result will be used in the next section to obtain the characteristic DC equation and the equivalent resistance of the voltage doubler circuit.

Kirchhoff's voltage law is applied to the two loops formed during each swing of the input voltage to obtain the steady state voltage across each diode (Fig. 2.2). In the ideal case where the diodes have zero threshold voltage, the DC voltage across the first capacitor is the peak input voltage amplitude $\bar{V}_{in}$ and the voltage across the load capacitor is $2\bar{V}_{in}$. Denoting the voltage across D_1 and D_2 by $v_1(t)$ and $v_2(t)$ respectively, we can write for the negative half cycle

$$v_1(t) = -V_{in}(t) - V_{C1} \tag{2.7}$$

$$v_1(t) = -V_{in}(t) - \bar{V}_{in} \tag{2.8}$$

For the positive half cycle by considering $v_1(t)$ as the new source for the circuit we obtain

$$v_2(t) = -v_1(t) - V_{C2} \tag{2.9}$$

$$v_2(t) = V_{in}(t) + \bar{V}_{in} - 2\bar{V}_{in} \tag{2.10}$$

$$v_2(t) = V_{in}(t) - \bar{V}_{in} \tag{2.11}$$

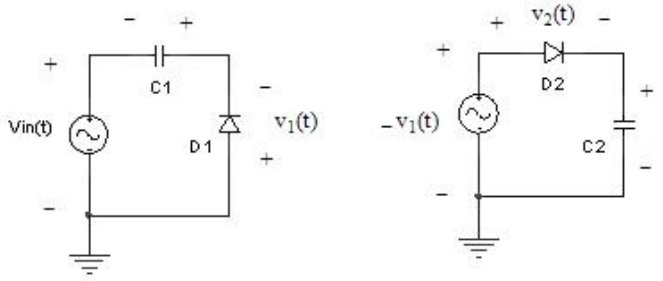

Figure 2.2: Analysis of the doubler circuit during negative voltage swing (left) and positive voltage swing (right).

Therefore, (2.8) and (2.11) represent voltages across diodes neglecting the drops due to threshold voltage. However, in the real case the output voltage does not reach twice the input voltage peak (i.e. the load capacitor does not charge up to $2\bar{V}_{in}$). In this case the voltage across each diode is shifted down (based on the polarity chosen) by a value less than $\bar{V}_{in}$ (correspondingly the first capacitor charges up to a voltage less than $\bar{V}_{in}$). In general the second term in the right-hand side of (2.8) and (2.11) can be replaced by $V_{out}/2$, which reduces to the ideal case value $\bar{V}_{in}$ when output voltage is twice the input amplitude.

2.1.2 Multi-Stage Voltage Doubler

The same analysis can be applied to an N-stage voltage multiplier (Fig. 2.3). A different, but equally valid analysis by studying the DC and AC operation of the circuit can also be employed. In the DC analysis, by considering all the coupling capacitors as open circuit, all diodes are in series, and thus the DC voltage on each

diode is

$$\bar{V}_D = \frac{V_{out}}{2N} \tag{2.12}$$

In the AC analysis, all the coupling capacitors are considered as short and thus the input sinusoidal voltage $\bar{V}_{in}\cos(\omega_0 t)$ drops across each diode (with different polarities for the two diodes in each stage). Therefore, the total voltage across each diode is the summation of the DC and AC voltages

$$v_d(t) = \pm\bar{V}_{in}\cos(\omega_0 t) - \frac{V_{out}}{2N} \tag{2.13}$$

where the plus sign applies to diodes with an even subscript and the minus sign applies to diodes with an odd subscript. This equation will be used for the analyses in the next sections to derive the DC characteristic equation and the equivalent resistance of the voltage multiplier circuit.

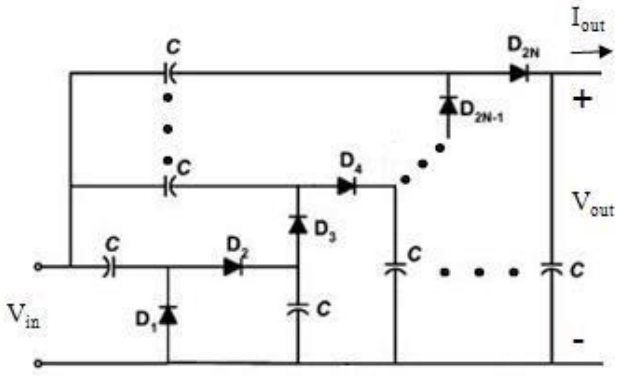

Figure 2.3: N-stage voltage multiplier with the designated input and output voltages.

2.2 Modeling the Input Stage of Voltage Doubler Consisting of p-n Junction Diodes

As mentioned in the beginning of this chapter, the input stage of the rectifier is modeled as a capacitance in parallel with a resistance. The input resistor R_{in} corresponds to the mean power that enters the rectifier during one period T of the input signal. The input capacitor C_{in} comes from the parasitic capacitors associated with the diodes and the layout. Fig. 2.3 shows an N-stage voltage multiplier circuit. A sinusoidal voltage $V_{in}(t)$ with a frequency f_0 and amplitude $\bar{V}_{in}$ is applied at the input of the voltage multiplier. V_{out} and I_{out} represent the DC output voltage and current respectively.

2.2.1 DC Characteristic Equation

The equivalent circuit of each diode can be represented by an ideal diode in parallel with a capacitance C_D, as depicted in Fig. 2.4, neglecting diode series resistance. The steady state solution of the voltage drop across each diode is repeated in (2.14), where the plus sign applies to diodes with an even subscript, and the minus sign applies to diodes with an odd subscript.

$$V_d(t) = \pm\bar{V}_{in}\cos(\omega_0 t) - \frac{V_{out}}{2N} \tag{2.14}$$

Every diode sees at its terminals the input signal shifted down a constant voltage $\bar{V}_D$ equal to $\bar{V}_{in}$ if all diodes are ideal, where $V_{out} = 2N\bar{V}_D$. Moreover, as shown in the previous section, the conservation of charge in steady state results in the following

equality to hold.

$$\int_0^T I_d(t)dt = I_{out}T \tag{2.15}$$

or rearranging

$$I_{out} = \frac{1}{T}\int_0^T I_d(t)dt \tag{2.16}$$

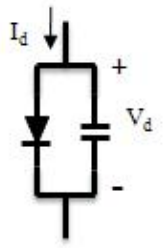

Figure 2.4: Simplified diode model.

Therefore, the DC output current is equal to the average current through each diode. According to the method presented in [9], by using (2.14) and the proposed diode model, the current in each diode is

$$I_d = I_S\left[\exp\left(\frac{V_d}{nV_T}\right) - 1\right] + C_D\frac{dV_d}{dt} \tag{2.17}$$

$$I_d = I_S\left[\exp\left(\pm\frac{\bar{V}_{in}}{nV_T}\cos(\omega_0 t)\right)\exp\left(-\frac{V_{out}}{2NnV_T}\right) - 1\right] + C_D\frac{dV_d}{dt} \tag{2.18}$$

The DC current in each diode, which based on (2.16) is also the DC output current I_{out}, is obtained by integrating both sides of (2.18) over one period and dividing by the period.

$$\frac{1}{T}\int_0^T I_d(t)dt = \frac{1}{T}I_S\left[\exp\left(-\frac{V_{out}}{2NnV_T}\right)\int_0^T \exp\left(\pm\frac{\bar{V}_{in}}{nV_T}\cos(\omega_0 t)\right)dt - \int_0^T dt\right]$$

It can be verified that when each diode is reverse biased, the exponent inside the integral is negative, and thus integration of the exponential function over the entire period introduces negligible error. The exponential of a cosinusoidal function can be expressed using the modified Bessel functions series expansion.

$$\exp(\pm x\cos\theta) = B_0(\pm x) + 2\sum_{n=1}^{\infty} B_n(\pm x)\cos(n\theta) \tag{2.19}$$

Using (2.19) in the rectifier DC equation results in

$$\begin{aligned} I_{out} = \frac{1}{T} I_S \{\exp\left(-\frac{V_{out}}{2NnV_T}\right) [B_0\left(\pm\frac{\bar{V}_{in}}{nV_T}\right)\int_0^T dt \\ +2\sum_{n=1}^{\infty} B_n\left(\pm\frac{\bar{V}_{in}}{nV_T}\right)\int_0^T \cos(n\omega_0 t)dt] - T\} \end{aligned} \tag{2.20}$$

The integral of the harmonic functions over a period yields zero. Therefore, the DC equation is reduced to

$$I_{out} = I_S\left[\exp\left(-\frac{V_{out}}{2NnV_T}\right) B_0\left(\pm\frac{\bar{V}_{in}}{nV_T}\right) - 1\right] \tag{2.21}$$

Noting that the modified Bessel function of the zeroth order is even, and substituting for the output current, the input-output characteristics of the N-stage voltage multiplier is expressed by

$$\left(1 + \frac{V_{out}}{R_L I_S}\right)\exp\left(\frac{V_{out}}{2NnV_T}\right) = B_0\left(\frac{\bar{V}_{in}}{nV_T}\right). \tag{2.22}$$

Therefore, for a given input voltage amplitude and resistive load, output DC voltage can be calculated from (2.22).

2.2.2 Equivalent Input Impedance

The average input power P_{in} to the rectifier can be obtained by summing up the average power P_D dissipated in each diode and the power P_L required by the load [9], if coupling capacitors are considered ideal. The average power dissipated in each diode is given by

$$P_D = \frac{1}{T}\int_0^T V_d(t) I_d(t)\, dt \tag{2.23}$$

If we substitute (2.14) for the voltage term we have

$$P_D = \pm\frac{\bar{V}_{in}}{T}\int_0^T \cos(\omega_0 t) I_d(t)\, dt - \frac{V_{out}}{2NT}\int_0^T I_d(t)\, dt \tag{2.24}$$

$$P_D = \pm\frac{\bar{V}_{in}}{T}\int_0^T \cos(\omega_0 t) I_d(t)\, dt - \frac{P_L}{2N} \tag{2.25}$$

Using (2.18) for the current through the diode, together with the modified Bessel functions series expansion yields

$$\begin{aligned} P_D = \pm\frac{\bar{V}_{in}}{T} I_S \exp\left(-\frac{V_{out}}{2NnV_T}\right) [\, B_0\left(\pm\frac{\bar{V}_{in}}{nV_T}\right)\int_0^T \cos(\omega_0 t)\, dt \\ +2\sum_{n=1}^{\infty} B_n\left(\pm\frac{\bar{V}_{in}}{nV_T}\right)\int_0^T \cos(\omega_0 t)\, \cos(n\omega_0 t)\, dt\,] - \frac{P_L}{2N} \end{aligned} \tag{2.26}$$

To obtain (2.26), the equation for the voltage across diode (2.14) was substituted for the voltage in the term representing the current through the capacitor, and the whole term was canceled after performing the integration. The constant term in the equation for the current through the ideal diode also vanished after integration. It is further observed that the first integral in (2.26), as well as the integral of all the

harmonics of the modified Bessel functions of an order higher than one equals zero too. Therefore, we have

$$P_D = \pm I_S \bar{V}_{in} B_1 \left(\pm \frac{\bar{V}_{in}}{nV_T} \right) \exp\left(-\frac{V_{out}}{2NnV_T} \right) - \frac{P_L}{2N} \tag{2.27}$$

As a result, the average input power is expressed by

$$P_{in} = 2NP_D + P_L = 2NI_S \bar{V}_{in} B_1 \left(\frac{\bar{V}_{in}}{nV_T} \right) \exp\left(-\frac{V_{out}}{2NnV_T} \right) \tag{2.28}$$

where the sign is neglected since the result is always positive regardless of the diode the analysis was based on (modified Bessel function of the first order is odd). Therefore, given an input voltage amplitude $\bar{V}_{in}$, the output voltage is obtained from (2.22) and used in (2.28) to calculate the input power for an N-stage voltage doubler circuit. Now that the mean input power is derived, we can define the equivalent input resistance of the voltage multiplier based on the average power consumption.

$$R_{in} = \frac{\bar{V}_{in}^2}{2P_{in}} \tag{2.29}$$

It is worth mentioning that in this derivation the frequency dependence is gone and the average input resistance does not explicitly depend on frequency. However, as will be discussed in the next chapter, the boosted voltage amplitude right at the input to the harvester denoted by $\bar{V}_{in}$ here, depends on the RLC network quality factor that does depend on the operating frequency. Hence, operation at resonant frequency guarantees maximum input voltage boost which in turn results in a higher output voltage.

Since the diode capacitance is a function of the voltage applied to the diode, we can consider the average value of the diode capacitance within the diode voltage swing, as follows

$$\bar{C}_D = \frac{1}{2\bar{V}_{in}} \int_{-\bar{V}_{in}-\frac{V_{out}}{2N}}^{\bar{V}_{in}-\frac{V_{out}}{2N}} C_D(V_d)\, dV_d \tag{2.30}$$

where $C_D(V_d)$ is the sum of the diffusion capacitance and junction capacitance provided by the SPICE model of the diode. Equivalently the integration can be carried out with respect to time during one period. The equivalent input capacitance of the voltage multiplier is the contribution from all diode capacitances and the parasitic capacitance due to layout.

$$C_{in} = 2N\bar{C}_D + C_{par} \tag{2.31}$$

Therefore, the parallel combination of the resistance and capacitance represented in (2.29) and (2.31) constitutes the input stage model of the rectifier circuit.

2.3 Modeling the Input Stage of Voltage Doubler Consisting of Diode-Connected MOSFETs

In order to model the input impedance of the voltage doubler circuit consisting of diode-connected MOSFETs (Fig. 2.5), a model for the individual transistors should be developed. The rectifier input capacitance is the summation of the effective capacitance of the diode-connected transistors, provided that the coupling capacitors are assumed ideal, and parasitic capacitance due to layout is neglected. The oxide capacitance is calculated using

$$C_{ox} = C'_{ox} W L = \frac{\epsilon_{ox}}{t_{ox}} W L \tag{2.32}$$

The effective capacitance of the transistors in saturation can be attributed mainly to the gate-source capacitance and represented as $C_{gs} = \frac{2}{3} C_{ox}$. In calculating the rectifier characteristic equation and the input equivalent resistance, the leakage current is considered as well, even though calculations show that neglecting it introduces a small error. The following equations show the procedure for obtaining the DC equation for the rectifier. These equations apply to the transistor with an even subscript which is on during the positive input voltage swings and whose current waveform is depicted in Fig. 2.6 (assuming the input voltage is a cosinusoidal function). Neglecting the subthreshold region of operation for the MOSFETs, and analogous to the method used to obtain (2.3), charge conservation can be written as

$$\Delta Q_{sat} = \Delta Q_{load} + \Delta Q_{leak} \tag{2.33}$$

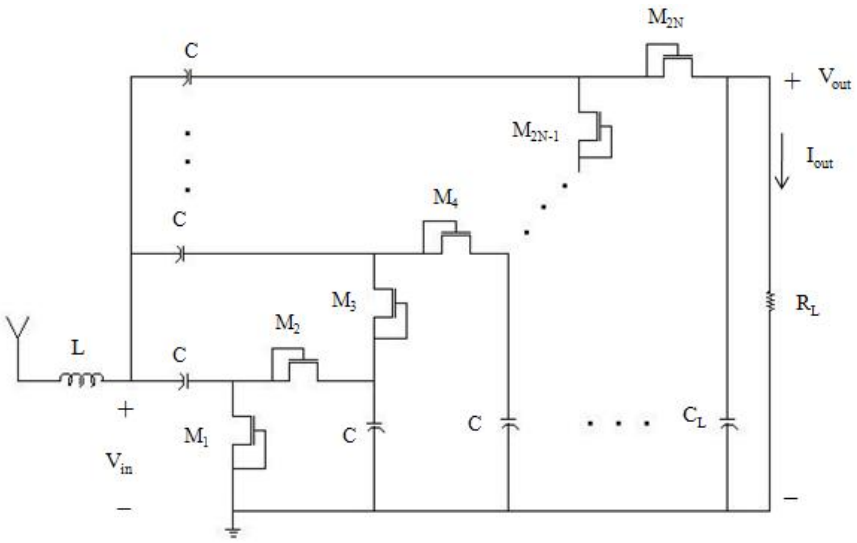

Figure 2.5: N-stage voltage doubler consisting of diode-connected transistors.

which indicates that the charge pumped out of the rectifier is compensated by the charge pumped into the circuit.

The charge due to the saturation region of operation during a half cycle (region where the transistor is considered to be conducting) is expressed by

$$\Delta Q_{sat} = \int_{\frac{-T}{4}}^{\frac{T}{4}} I_d(t)\, dt \tag{2.34}$$

$$\Delta Q_{sat} = \int_{\frac{-T}{4}}^{\frac{T}{4}} \frac{1}{2}\, \mu_n\, C'_{ox}\, \frac{W}{L}\, (V_{gs} - V_{th})^2\, dt \tag{2.35}$$

The voltage across the diode-connected MOSFET is the same as the gate-source bias, and for the diode under consideration according to the discussion in the previous section is equal to

$$V_{gs} = \bar{V}_{in} \cos(\omega_0 t) - \frac{V_{out}}{2N} \tag{2.36}$$

where $\bar{V}_{in}$ is the input voltage amplitude and V_{out} is the DC output voltage. Substituting for V_{gs} in (2.35) and performing the integration yields

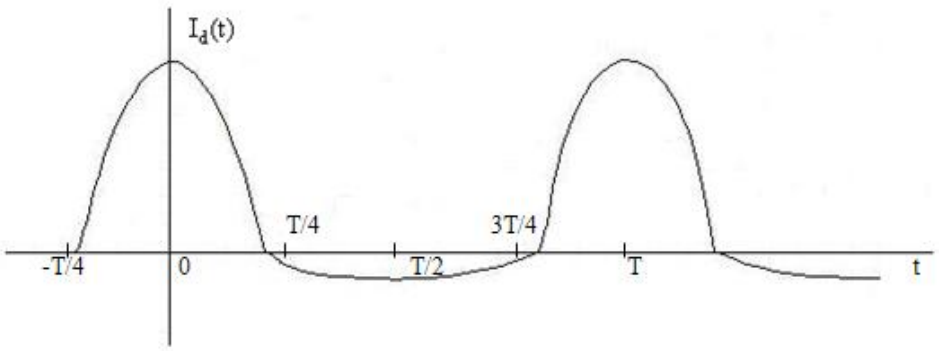

Figure 2.6: Current waveform through the diode-connected transistor.

$$\Delta Q_{sat} = \frac{1}{2}\mu_n C_{ox}^{'} \frac{W}{L} T \left[\frac{\bar{V}_{in}^2}{4} - \frac{2\bar{V}_{in}}{\pi} \left(\frac{V_{out}}{2N} + V_{th} \right) + \frac{1}{2} \left(\frac{V_{out}}{2N} + V_{th} \right)^2 \right] \tag{2.37}$$

Approximating the leakage current by a sinusoidal function similar to the approach in [13], we have

$$\Delta Q_{leak} = 2 \int_{\frac{T}{4}}^{\frac{T}{2}} I_{leak}\, dt = 2 \int_{\frac{T}{4}}^{\frac{T}{2}} I_{pleak}\, \cos(\omega_0 t)\, dt \tag{2.38}$$

$$\Delta Q_{leak} = \frac{T}{\pi} I_{pleak} \tag{2.39}$$

The peak leakage current I_{pleak} can be approximated for each transistor based on the process used. For the charge drawn by the load we know

$$\Delta Q_{load} = I_{out}\, T = \frac{V_{out}}{R_L}\, T \tag{2.40}$$

Therefore, balance of charge yields

$$\frac{V_{out}}{R_L} + \frac{I_{pleak}}{\pi} - \frac{1}{2}\mu_n C_{ox}^{'} \frac{W}{L} \left[\frac{\bar{V}_{in}^2}{4} - \frac{2\bar{V}_{in}}{\pi} \left(\frac{V_{out}}{2N} + V_{th} \right) + \frac{1}{2} \left(\frac{V_{out}}{2N} + V_{th} \right)^2 \right] = 0 \tag{2.41}$$

Equation (2.41) serves to relate the input and output voltages of the rectifier. It allows for the calculation of output DC voltage given the amplitude of the input

voltage to the harvester.

In order to calculate the equivalent input resistance in terms of the power dissipated in the circuit, a method similar to the one discussed in the previous section is employed. The total input power consists of the power consumed by the diode-connected MOSFETs and the load. For each transistor we have

$$P_D = P_{sat} + P_{leak} \tag{2.42}$$

where

$$P_{sat} = \frac{1}{T} \int_{\frac{-T}{4}}^{\frac{T}{4}} I_d \, V_{gs} \, dt \tag{2.43}$$

$$P_{leak} = \frac{2}{T} \int_{\frac{T}{4}}^{\frac{T}{2}} I_{leak} \, V_{ds} \, dt \tag{2.44}$$

When the transistor conducts a reverse leakage current, the drain and source are interchanged. As a result in (2.44) we have

$$V_{ds} = \frac{V_{out}}{2N} - \bar{V}_{in} \cos(\omega_0 t) \tag{2.45}$$

Using the respective current expressions as in (2.35) and (2.38) and carrying out the integrations result in the following equations for saturation and leakage.

$$P_{sat} = \frac{1}{2} \mu_n C_{ox}^{'} \frac{W}{L} \{ \frac{2\bar{V}_{in}^3}{3\pi} + \frac{\bar{V}_{in}}{\pi} \left(\frac{V_{out}}{2N} + V_{th} \right)^2 - \frac{\bar{V}_{in}^2}{2} \left(\frac{V_{out}}{2N} + V_{th} \right)$$

$$- \frac{V_{out}}{2N} \left[\frac{\bar{V}_{in}^2}{4} - \frac{2\bar{V}_{in}}{\pi} \left(\frac{V_{out}}{2N} + V_{th} \right) + \frac{1}{2} \left(\frac{V_{out}}{2N} + V_{th} \right)^2 \right] \} \tag{2.46}$$

$$P_{leak} = 2I_{pleak}\left(\frac{V_{out}}{4N\pi} + \frac{\bar{V}_{in}}{8}\right) \tag{2.47}$$

Having obtained the power consumption due to the transistors, the total input power is given by

$$P_{in} = 2NP_D + P_L \tag{2.48}$$

with

$$P_L = \frac{V_{out}^2}{R_L} \tag{2.49}$$

The input resistance that corresponds to this amount of power dissipation can be evaluated as

$$R_{in} = \frac{\bar{V}_{in}^2}{2P_{in}} \tag{2.50}$$

As described in the beginning of this section, the input capacitance can be computed using $2NC_{gs}$ assuming ideal components.

In the presented analysis, the integration limits in (2.34) and (2.43) as well as the sign of the input voltage used in (2.36) are determined based on the diode under consideration. The foregoing equations were based on a diode with an even subscript that is forward biased during positive input voltage swings. If a diode with an odd subscript is used instead, the equation for the voltage across the transistor changes to the following form

$$V_{gs} = -\bar{V}_{in}\cos(\omega_0 t) - \frac{V_{out}}{2N} \tag{2.51}$$

Subsequently the integration limits change to account for the period during which the transistor is conducting. The integrals for the charge provided and the power consumed in the saturation region, which are the dominant terms in the analyses become

$$\Delta Q_{sat} = \int_{\frac{T}{4}}^{\frac{3T}{4}} I_d(t)\, dt \tag{2.52}$$

$$P_{sat} = \frac{1}{T} \int_{\frac{T}{4}}^{\frac{3T}{4}} I_d\, V_{gs}\, dt \tag{2.53}$$

Performing the integration for the charge by using the new expression for V_{gs} yields the same equation derived earlier. The same argument applies when calculating the power consumed in the saturation region and an identical expression for power consumption is obtained. Therefore, the final results for the input-output characteristic equation and the equivalent input resistance are independent of the transistor for which the analysis was performed.

2.4 Modeling the Input Stage of Voltage Doubler Consisting of Short-Channel MOSFETs

In modern CMOS process the length of the inversion layer channel is well below $1\mu m$. As a result, the previous discussions on the modeling of diode-connected MOSFETs have to be refined to take into account the short-channel effects. The most prominent effect observed in short-channel devices is the velocity saturation due to high electric fields. The drain current equation for the short-channel MOS transistor operating in the saturation region is a linear function of V_{gs}. It can be shown that the current equation in this case becomes

$$I_D = W v_{sat} C'_{ox}(V_{gs} - V_{th} - V_{ds,sat}) \tag{2.54}$$

The on or drive current per width of a MOSFET is a relative figure of merit for the modern CMOS process and is given by [18]

$$I_{on} = v_{sat} C'_{ox}(V_{gs} - V_{th} - V_{ds,sat}) \tag{2.55}$$

$$I_D = I_{on} W \tag{2.56}$$

The drive current is defined for $V_{gs} = V_{ds} = VDD$, and its value for the specific process can be found in the design manuals.

In order to find the expression for $V_{ds,sat}$ dependence on V_{gs}, we notice that the drain current once carrier velocity reaches saturation velocity and current saturates, is given by

$$I_D = \mu_n C'_{ox} \frac{W}{L} \left[(V_{gs} - V_{th}) V_{ds,sat} - \frac{1}{2} V_{ds,sat}^2 \right] \tag{2.57}$$

Equating (2.54) and (2.57) allows us to solve for $V_{ds,sat}$ which yields [19]

$$V_{ds,sat} = (V_{gs} - V_{th}) + \frac{L v_{sat}}{\mu_n} - \sqrt{(V_{gs} - V_{th})^2 + \left(\frac{L v_{sat}}{\mu_n} \right)^2} \tag{2.58}$$

Substituting this expression back in (2.54) yields the final equation for current in saturation mode considering the effect of saturation velocity

$$I_D = W C'_{ox} v_{sat} \left[\sqrt{(V_{gs} - V_{th})^2 + \left(\frac{L v_{sat}}{\mu_n} \right)^2} - \frac{L v_{sat}}{\mu_n} \right] \tag{2.59}$$

Using this equation, we obtain the relation between drain current and V_{gs} as defined earlier for the RF harvester and repeated below for the transistors having even subscript (Fig. 2.5).

$$V_{gs} = \bar{V}_{in} \cos(\omega_0 t) - \frac{V_{out}}{2N} \tag{2.60}$$

Charge conservation is utilized like previous sections to derive the DC characteristic equation for the rectifier

$$\Delta Q_{sat} = \Delta Q_{load} + \Delta Q_{leak} \tag{2.61}$$

ΔQ_{leak} and ΔQ_{load} are determined like before as in (2.39) and (2.40). The charge in the saturation region where the transistor is on, is calculated using

$$\Delta Q_{sat} = \int_{\frac{-T}{4}}^{\frac{T}{4}} I_D(t)\, dt \tag{2.62}$$

with $I_D(t)$ replaced with (2.59) in this case, and V_{gs} replaced with (2.60) as before. However, there is no analytical solution to this integral. The integration can be performed numerically on MATLAB to calculate the charge due to the saturation region for a given output voltage value. Bringing all the terms in (2.61) to one side, the goal is then to find the proper output voltage that satisfies the balance of charge. Using a proper initial guess and tolerance, and knowing the circuit design parameters and the input voltage amplitude to the rectifier, MATLAB fsolve function is used to solve the resulting nonlinear equation and find the output DC voltage.

Likewise in order to calculate the power dissipated in the harvester and thus obtain the equivalent input resistance, the following integration has to be performed

$$P_{sat} = \frac{1}{T} \int_{\frac{-T}{4}}^{\frac{T}{4}} I_D \, V_{gs} \, dt \tag{2.63}$$

which again has no explicit answer and numerical integration is performed instead. The obtained output voltage from the DC characteristic equation is substituted in the expressions for V_{gs} and $I_D(t)$ and the resulting dissipated power in saturation is computed on MATLAB. Identical procedure as in the long-channel case is employed to evaluate the input power to the harvester and subsequently the input resistance. The power terms due to leakage current and output load are found from (2.47) and (2.49) respectively to calculate the total rectifier input power.

$$P_{in} = 2N(P_{sat} + P_{leak}) + P_L \tag{2.64}$$

$$R_{in} = \frac{\bar{V}_{in}^2}{2P_{in}} \tag{2.65}$$

Finally, in real harvester implementation, the parasitic resistance mainly due to the inductor is added to the contribution from the rectifier as found from (2.65) to obtain the total harvester input impedance. As will be investigated in the next chapters, the equations derived in the analysis of the rectifier based on the operation of the short-channel MOSFETs, are capable of reasonably predicting the equivalent input resistance of the rectifier as compared to simulation results.

Chapter 3

Voltage Boosting and Impedance Matching in RF Energy Harvesting

In this chapter the operation of voltage doubler based RF energy harvester is discussed in more detail and different design parameters affecting the DC output voltage and conversion efficiency are studied. The concepts of voltage boosting and impedance matching are elaborated, their relation with resonance condition is determined, and improvement in the matching network will be employed to achieve higher harvester conversion efficiency.

3.1 Analytical Derivation of Matching Conditions

The equivalent input impedance of the RF energy harvester was modeled as a resistance in parallel with a capacitance in chapter 2. Based on the maximum power transfer theory, the maximum RF input power is transferred from the antenna to the harvester in the case where the impedances of the harvester and antenna match, i.e. when they are complex conjugates. Under this condition, all the power available from the antenna is absorbed by the harvester, and half of the input voltage received by the antenna drops across the harvester circuit. Since the impedance of the antenna is often considered as resistive, thus a matching network is required to match the equivalent input resistance of the harvester to the antenna radiation

resistance, and resonate out the input reactance of the harvester. In order to achieve the desired impedance transformation between the antenna and the harvester, it is common that a matching network consisting of a single inductor is designed. The inductor forms a so-called L-match network with the harvester input impedance. In this section the governing equations that indicate the matching conditions are derived. Since the harvester input resistance is always much higher than the antenna radiation resistance, downward impedance transformation applies to the antenna-harvester system.

3.1.1 Downward Impedance Transformer

Fig. 3.1 illustrates a downward impedance transformer circuit. It transforms a higher parallel resistance into a lower series resistance seen at the circuit input. For this L-match network the impedance is calculated as follows

$$Z_{eq} = R_P // \frac{1}{j\,\omega\,C} \tag{3.1}$$

$$Z_{in} = j\,\omega\,L + Z_{eq} = j\,\omega\,L + \frac{R_P}{1 + j\,R_p\,\omega\,C} \tag{3.2}$$

$$Z_{in} = \frac{R_P + (\omega\,L + R_P^2\,\omega^3\,L\,C^2 - R_P^2\,\omega\,C)\,j}{1 + R_P^2\,\omega^2\,C^2} \tag{3.3}$$

Therefore, the real part and the imaginary part of the input impedance are

$$R_{in} = \frac{R_P}{1 + R_P^2\,\omega^2\,C^2} \tag{3.4}$$

$$X_{in} = \frac{\omega\,L + R_P^2\,\omega^3\,L\,C^2 - R_P^2\,\omega\,C}{1 + R_P^2\,\omega^2\,C^2} \tag{3.5}$$

In order to have matching, the value of antenna resistance should be equal to the input resistance. Furthermore, the input reactance must be canceled. Therefore,

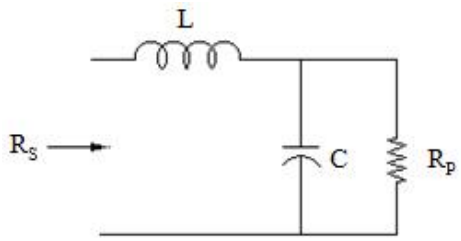

Figure 3.1: Downward impedance transformer.

(3.4) gives the required value for the series source resistance, while equating (3.5) to zero yields the required inductance value.

$$R_S = \frac{R_P}{1 + R_P^2\,\omega^2\,C^2} \tag{3.6}$$

$$L = \frac{R_P^2\,C}{1 + R_P^2\,\omega^2\,C^2} \tag{3.7}$$

It is observed that when $R_P^2\omega^2C^2 >> 1$, these formulas simplify to the basic L-match [20] and resonance equations:

$$R_S = \frac{L}{R_P\,C} \tag{3.8}$$

$$L = \frac{1}{\omega^2\,C} \tag{3.9}$$

This type of L-match network is frequently used in RF design since the intrinsic and parasitic capacitances of the RF circuit can all be incorporated in the parallel capacitance of the network.

3.1.2 Upward Impedance Transformer

There are cases in which it is essential to transform a resistance to a higher value. For example the resistance R_S obtained from the downward network, can

be transformed to a higher practical antenna resistance using an upward impedance transformer network as depicted in Fig. 3.2. In this configuration the input impedance is

$$Z_{eq} = j\,\omega\,L + R_S \tag{3.10}$$

$$Z_{in} = \frac{1}{j\,\omega\,C} // Z_{eq} = \frac{R_S + (\omega\,L - R_S^2\,\omega\,C - \omega^3\,L^2 C)j}{1 + \omega^2\,C(\omega^2\,L^2\,C - 2\,L + R_S^2\,C)} \tag{3.11}$$

The real and imaginary parts of the input impedance are

$$R_{in} = \frac{R_S}{1 + \omega^2\,C(\omega^2\,L^2\,C - 2\,L + R_S^2\,C)} \tag{3.12}$$

$$X_{in} = \frac{\omega\,L - R_S^2\,\omega\,C - \omega^3\,L^2 C}{1 + \omega^2\,C(\omega^2\,L^2\,C - 2\,L + R_S^2\,C)} \tag{3.13}$$

In order to achieve matching, like the previous section the parallel resistance seen at the input should match the source resistance as given in (3.14). At the same time the reactance must be canceled, which yields (3.15) after equating it to zero.

$$R_P = \frac{R_S}{1 + \omega^2\,C(\omega^2\,L^2\,C - 2\,L + R_S^2\,C)} \tag{3.14}$$

$$C = \frac{L}{R_S^2 + \omega^2 L^2} \tag{3.15}$$

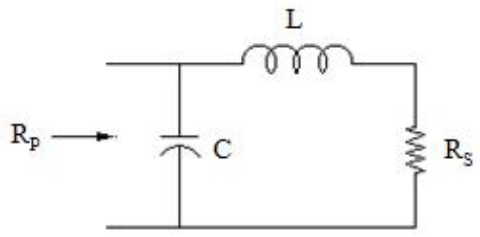

Figure 3.2: Upward impedance transformer.

Substituting for capacitance from (3.15) in (3.14) simplifies the first condition to

$$R_P = \frac{R_S^2 + \omega^2 L^2}{R_S} \tag{3.16}$$

Therefore, if $\omega^2 L^2 >> R_S^2$, then these equations again simplify to the basic L-match and resonance relations.

$$R_P = \frac{L}{R_S C} \tag{3.17}$$

$$C = \frac{1}{\omega^2 L} \tag{3.18}$$

In the design of the matching network, it might become necessary to transform a resistance to a higher value after originally transforming it down. In this case a cascade of downward and upward L-match networks can be utilized to form a so-called π-match network. The analysis of this circuit will be presented in the next sections.

3.2 Equivalent Capacitance of the Harvester System

If the passive IC components used in the design could be considered ideal, then the total capacitance of the harvester could only be attributed to the diode-connected transistors implemented. However, in the real case both the non ideal effects of the coupling capacitors, and the parasitic capacitance due to the non ideal inductor have to be taken into consideration.

3.2.1 Inductor Design

The inductor used typically in the CMOS process for RF design is the planar spiral inductor. For a square configuration, a rough estimate of the inductance value L (in Henries) as a function of the number of turns n and the outer radius of the spiral r (in meters) is given by [20]

$$L = \mu_0 \, n^2 \, r = 1.2 \times 10^{-6} \, n^2 \, r \tag{3.19}$$

A more accurate expression for the inductance of a planar spiral of a regular shape can be represented using

$$L = \frac{\mu_0 n^2 d_{avg} c_1}{2} \left[ln \left(\frac{c_2}{\rho} \right) + c_3 \rho + c_4 \rho^2 \right] \tag{3.20}$$

where ρ is the fill factor defined as

$$\rho = \frac{d_{out} - d_{in}}{d_{out} + d_{in}} \tag{3.21}$$

In these equations d_{in} and d_{out} are the inner and outer spiral diameters respectively, and d_{avg} is the arithmetic mean of the two diameters. The numerical values of coefficients c_n are tabulated and are a function of geometry.

The on-chip spiral inductor can be modeled as an ideal lossless inductor plus the inherent parasitic capacitances and resistances. The conventional single-π model is illustrated in Fig. 3.3. In CMOS technology, the substrate is fairly conductive and is located close to the inductor, giving rise to a parallel plate capacitor that resonates with the inductor. The resonant frequency of this LC combination poses an upper

limit to the useful operating frequency of the inductor [20]. The capacitance formed between the spiral and the substrate can be approximated using a simple parallel plate formula given by

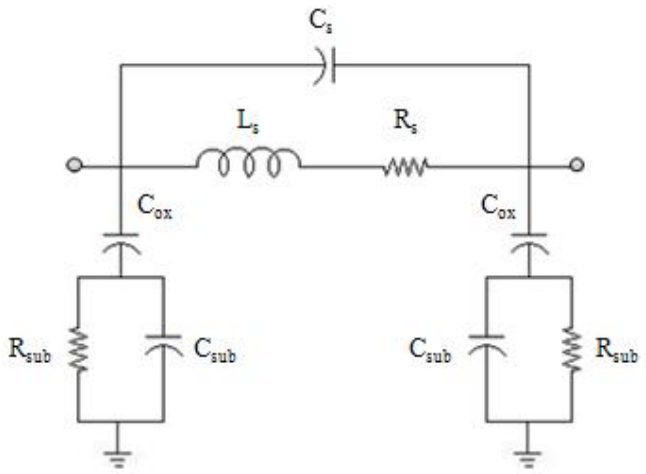

Figure 3.3: Model for on-chip spiral inductor.

$$C_{L,ox} = w\, l\, \frac{\epsilon_{ox}}{t_{ox}} \tag{3.22}$$

where l is the total length of the winding and w is the width of the interconnect. This capacitance must be taken into account in calculating the equivalent input capacitance of the harvester when the inductor is introduced to the circuit for the purpose of impedance matching and voltage boosting. The shunt capacitance across the inductor is another parasitic element that arises from the overlap of the cross-under with the rest of the spiral. The C_s component in the model takes care of this capacitance as well as the less significant turn-to-turn capacitance, and is approximated as

$$C_s = n\, w^2\, \frac{\epsilon_{ox}}{t_{ox}} \tag{3.23}$$

The parasitics denoted by C_{sub} and R_{sub} in the model represent the silicon substrate capacitance and dielectric loss respectively. Resistance R_{sub} is due to the current capacitively coupled to substrate through $C_{L,ox}$. The image current flows in a direction opposite to the current flow in the inductor and thus tends to lower the effective inductance. The capacitance C_{sub} models the capacitance of the substrate as well as other reactive effects related to this image inductance and is formulated as $C_{sub} = w\,l\,C_1/2$, where C_1 is a fitting parameter that depends on the substrate material and the distance between the substrate and the main spiral.

The resistive losses of the inductor can be mainly attributed to the skin effect that causes a nonuniform current distribution in the inductor and decreases the effective cross section, which leads to an increase in the series resistance. In addition there might be considerable losses associated with eddy currents induced in the substrate, and the total series resistance R_s is the sum of these losses and the resistance due to the skin effect. Since the innermost turns contribute negligibly to the total magnetic flux while contributing significant resistance, it is essential to design hollow spiral inductors with the outer and inner diameters giving a fill factor of about 0.5.

In practice we take advantage of the parasitic capacitances introduced by the inductor implementation to increase the total capacitance of the harvester system. This allows us to operate at a specific resonant frequency by designing a much smaller inductance that takes less space on the chip. As mentioned earlier the self-

resonant frequency of the spiral inductor should be considered when designing the RF harvester. The efficiency of an inductor is measured by its Q, which is limited by parasitics. Therefore, the maximum achievable on-chip inductor Q poses another constraint toward the desirable design. One source of degradation of Q is the energy coupled to the nearby substrate, as well as the loss introduced due to the inner turns as mentioned above. The Q can be increased through different layout techniques that tend to reduce the total resistive losses. Inductor quality factor and self-resonant frequency will be examined in more detail in next sections.

3.2.2 Harvester Parasitic Capacitances

The effective capacitance due to each transistor can be mainly attributed to the gate-source oxide capacitance of the diode-connected MOSFETs as indicated in (3.24). In the AC analysis of the circuit, the transistor capacitances for the doubler stages are all in parallel and thus add up.

$$C_D = \frac{2}{3} C'_{ox} WL = \frac{2}{3} \frac{\epsilon_{ox}}{t_{ox}} WL \tag{3.24}$$

In the analysis presented in chapter 2, the coupling capacitors were considered as short circuits at the frequency of interest. In reality though, the non ideality of coupling capacitors is another factor that should be taken into account. The minimum acceptable value for the output capacitance is calculated according to the maximum allowed voltage ripple at the rectifier output [11]. The intermediate capacitors should be designed such that their corresponding impedance value is small

compared to the impedance of the diode-connected transistors. These coupling capacitors act like voltage dividers and unless represented as a short circuit, they decrease the harvester conversion efficiency. The overall input capacitance taking into account the diode capacitance as well as the coupling capacitors can be evaluated for a single voltage doubler stage. Consistent with the notation used in the previous chapter, the doubler circuit is depicted in Fig. 3.4, with the series diode resistances considered negligible and the parallel diode resistances assumed large compared to the impedance due to the capacitance.

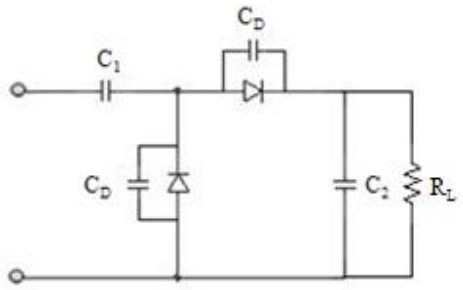

Figure 3.4: Capacitors affecting doubler circuit equivalent capacitance.

Assuming a high resistive load, the input capacitance is evaluated as

$$C_{in} = \frac{C_1 C_D (C_D + 2C_2)}{C_1 C_D + 2C_2 C_D + C_1 C_2 + C_D^2} \tag{3.25}$$

Defining the normalization factors as $\alpha = C_1/C_D$ and $\beta = C_2/C_D$ [11], and noting that in the ideal case the input capacitance reduces to $2\,C_D$, this equation ca be rewritten as

$$C_{in} = C_{in,ideal}\,\frac{\alpha(1+2\beta)}{2(1+\alpha+2\beta+\alpha\beta)} \tag{3.26}$$

It is observed that as α and β increase, the right-hand side of (3.26) approaches the ideal input capacitance.

3.3 Voltage Boosting and Quality Factor

In order to turn on the diode-connected transistors in the rectifier circuit, the low input voltage levels received by the antenna have to be boosted to higher levels at the input of the energy harvester. This boosted signal then enters the harvester and is rectified and further increased depending on the voltage drops across the diodes. As stated earlier, in the AC analysis of the rectifier circuit, all transistors are in parallel, and the input sinusoidal voltage drops directly across each transistor, and thus its corresponding shunt capacitance. As illustrated in Fig. 3.5, the inductor used for the purpose of matching, also forms a resonant boost circuit with the rectifier input stage. As a result, if voltage boosting is achieved through the resonance between the inductor and the input equivalent capacitance, then in the real circuit the boosted signal appears across each individual capacitor and its respective transistor. A sufficiently boosted signal then insures that V_{gs} of each transistor is high enough to overcome the threshold voltage and turn the diode-connected MOSFET on.

As will be elaborated in this section, the level of voltage boosting at the input stage of the harvester depends on the network and inductor quality factor. A general and formal definition of Q is as follows.

$$Q = 2\pi \frac{Energy\,stored}{Energy\,dissipated\,per\,cycle} = \omega \frac{Energy\,stored}{Average\,power\,dissipated} \tag{3.27}$$

The definition presented in (3.27) can be applied to both inductors and LC tanks. The difference lies in the form of the energy stored defined in each case [21]. In an

inductor, the desired energy is stored in the magnetic field as opposed to the undesirable energy stored in the electric field. As a result the net energy stored is found by calculating the difference between peak magnetic and electric energies. Above the self-resonant frequency, the inductor does not provide net magnetic energy to the external circuitry and does not behave as an inductor anymore. In an LC tank, the energy stored is the sum of the electric and magnetic energies, which is equal to the peak magnetic or peak electric energy. The tank resonant frequency is the frequency of oscillation between these two forms of energy, and is infinite for a lossless network.

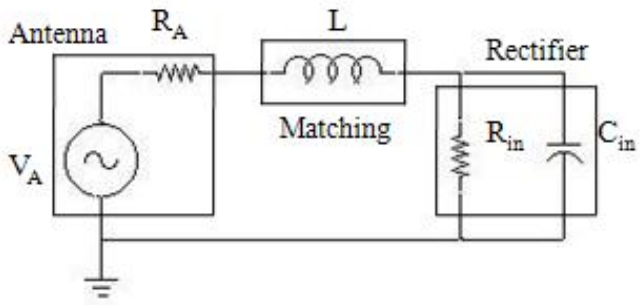

Figure 3.5: Simplified model of the harvester-antenna system.

3.3.1 L-Match Network

As mentioned in the first section when discussing impedance transformations, in order to achieve matching using the L-match network at the operating frequency ω_0, two conditions must be satisfied to insure the cancellation of the input reactance and that the transformed input resistance matches the source resistance. In both downward and upward impedance transformers these conditions can be represented

as

$$R_P\, R_S = \frac{L}{C} \tag{3.28}$$

$$\omega_0 = \frac{1}{\sqrt{LC}} \tag{3.29}$$

These two equations were derived from a more general pair of equations if we had $R_P^2\, \omega_0^2\, C^2 >> 1$ for the downward network, and $\omega_0^2\, L^2 >> R_S^2$ for the upward network. In fact in both cases these conditions follow if $Q^2 >> 1$. Therefore, the quality factors of the downward (parallel) and upward (series) networks are defined as

$$Q_P = \omega_0\, R_P\, C \tag{3.30}$$

$$Q_S = \frac{\omega_0\, L}{R_S} \tag{3.31}$$

The second condition for matching (3.29) is the familiar resonance equation at center frequency ω_0. Therefore, the resonance condition is already embedded in the criteria for matching. It is worth mentioning that (3.28) was also written in this simplified form using (3.29), i.e. the basic L-match formula assumes operation at resonance frequency. Furthermore, at resonance the quality factors can be represented in the following equivalent forms.

$$Q_P = \frac{R_P}{\omega_0\, L} \tag{3.32}$$

$$Q_S = \frac{1}{\omega_0\, R_S\, C} \tag{3.33}$$

Substitution for L/C in (3.28) from the latter equations results in the quality factor for both the upward and downward impedance transformers to be approxi-

mately equal to the square root of the transformation ratio (given $Q^2 >> 1$).

$$Q \approx \sqrt{\frac{R_P}{R_S}} \tag{3.34}$$

Note that in the downward network the resistance seen by the source is R_S while in the upward network this resistance corresponds to R_P, with R_P being greater than R_S.

3.3.2 π-Match Network

As mentioned earlier, based on the design requirements, application of both downward and upward impedance transformers as depicted in Fig. 3.6 might become necessary. In real implementation, the two inductors are combined to form a so-called π-match network. Now we wish to express the design equations used for the π-match circuit in terms of the quality factors to demonstrate the benefit introduced over the simple L-match circuit. By making use of an image resistance at the junction of two inductances, an additional degree of freedom is obtained [20] that allows us to specify the center frequency, quality factor and impedance transformation ratio independently.

After transforming the parallel RC network on the right of the circuit shown in Fig. 3.6 to its series equivalent, the Q of the right-hand L-section becomes

$$Q_{right} = \frac{\omega_0 L_2}{R_I} = \sqrt{\frac{R_{in}}{R_I} - 1} \tag{3.35}$$

Note that we have used the exact relation between the quality factor and the resistance transformation ratio as compared to the approximate relation given in

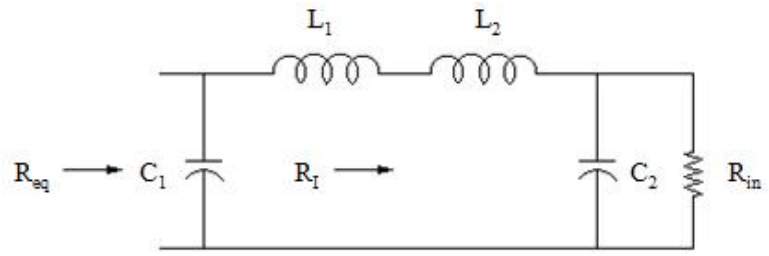

Figure 3.6: π-match network.

(3.34). This is easily obtained by equating the real parts of the series and parallel impedances. Similarly the Q of the left-hand L-section can be written as

$$Q_{left} = \frac{\omega_0 L_1}{R_I} = \sqrt{\frac{R_{eq}}{R_I} - 1} \tag{3.36}$$

As a result the overall network Q is the summation of both quality factors.

$$Q = \frac{\omega_0 (L_1 + L_2)}{R_I} = Q_{right} + Q_{left} = \sqrt{\frac{R_{in}}{R_I} - 1} + \sqrt{\frac{R_{eq}}{R_I} - 1} \tag{3.37}$$

The expression for the overall network Q allows one to find the appropriate value for the image resistance through iteration given the Q-factor as well as the original and transformed resistances. Subsequently the required inductance for the center frequency can be obtained using

$$L_1 + L_2 = \frac{QR_I}{\omega_0} \tag{3.38}$$

To complete the design, the capacitance values are also determined according to the individual quality factors selected.

$$C_1 = \frac{Q_{left}}{\omega_0 R_{eq}}; \quad C_2 = \frac{Q_{right}}{\omega_0 R_{in}} \tag{3.39}$$

As with the case of the downward L-match, parasitic capacitances present in the circuit can be incorporated in the π-match network design. As an extension

of the harvester-antenna system depicted in Fig. 3.5, Fig. 3.7 demonstrates the π-match network used to obtain a more efficient system performance. The matching network is identical to the one shown in Fig. 3.6 with the inductors lumped together, and the equivalent input capacitance replacing one of the capacitors.

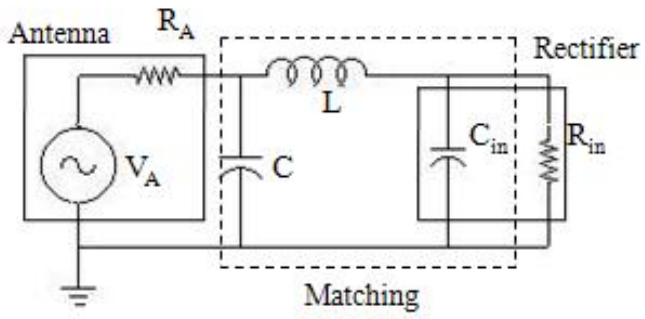

Figure 3.7: Simplified model of the harvester-antenna system using a π-match network.

3.3.3 Ratio of Boosting

Now referring to Fig. 3.8, by considering the downward L-match network which represents the model for the input stage of the rectifier circuit, we want to find out the ratio of boosting when operating at the resonant frequency. This provides us with the amount of source voltage amplification achieved at the input to the rectifier circuit. The parallel input resistance is transformed to an equivalent series resistance that is equal to the antenna radiation resistance in the matched case. The modeled harvester input circuit is depicted in Fig. 3.9. During the operation at resonance we know that the resulting boosted voltage across the capacitor can

be found using

$$\frac{V_{Cin0}(\omega_0)}{V_{in0}} = \frac{\omega_0 L}{R_{eq}} = \frac{1}{\omega_0 R_{eq} C_{in}} \tag{3.40}$$

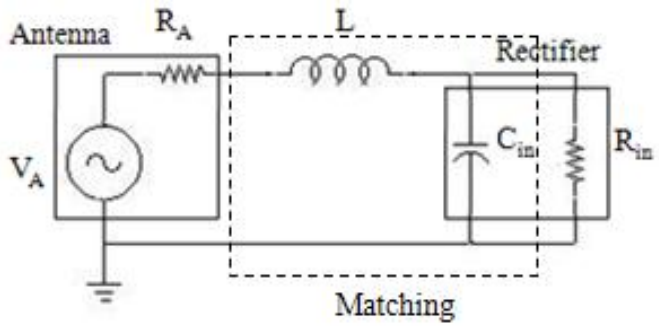

Figure 3.8: Simplified model of the harvester-antenna system using an L-match network.

This relation can be rewritten in terms of the original parallel resistance as

$$\frac{V_{Cin0}(\omega_0)}{V_{in0}} = \frac{R_{in}}{\omega_0 L} = \omega_0 R_{in} C_{in} \tag{3.41}$$

which shows the ratio of the peak voltage across input capacitor to the peak input voltage. This is due to the fact that all the input voltage drops across the resistive element, and the capacitor and inductor continuously exchange the electromagnetic energy with the voltages across them possibly reaching much higher levels than the input voltage depending on the values of the circuit elements. As elaborated at the beginning of this section, this input capacitor is the sum of the equivalent capacitance of all diode-connected transistors. Therefore, the boosted voltage appears across each individual transistor and if high enough pushes the device into the saturation region.

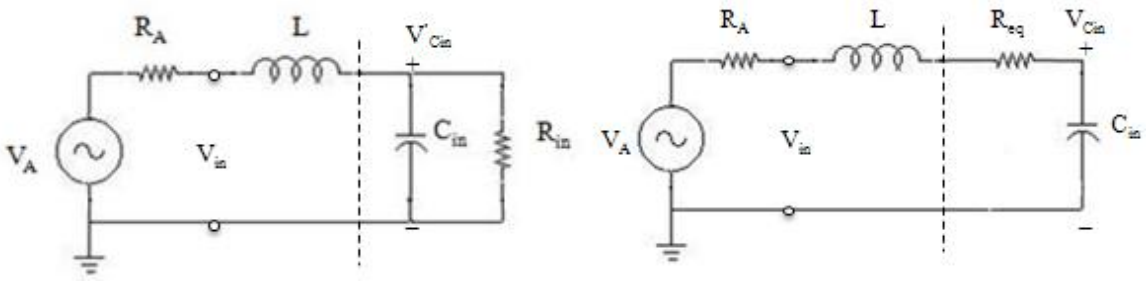

Figure 3.9: Transformed equivalent harvester input circuit showing resonant voltage boosting.

Since the ratio of boosting represented in (3.40) and (3.41) is defined as the circuit quality factor, i.e. $V_{Cin0}(\omega_0) = Q\,V_{in0}$, the design goal is then to operate at the resonant frequency with the highest possible boosted input voltage. According to (3.34), or in terms of our harvester notation $Q = \sqrt{R_{in}/R_A}$, the quality factor is limited by the transformation ratio achievable. This relation assumes matching of harvester resistance to the antenna resistance, i.e. $R_{eq} = R_A$. As demonstrated in the previous subsection, π-match network decouples Q from the transformation ratio by introducing an intermediate resistance, allowing a more flexible design with much higher Q values.

It should be mentioned that in the derivation of equivalent input resistance in chapter 2, it was shown that R_{in} depends on the boosted input voltage amplitude. As a result, (3.40) might in fact be regarded as a nonlinear equation that can be solved for the boosted voltage for a given source voltage. Denoting V_{Cin0} by V_{boost} we thus have:

$$V_{boost} = Q\,V_{in0} = \omega_0 R_{in}(V_{boost})\,C_{in}V_{in0} \tag{3.42}$$

where the source voltage is related to the absorbed RF power from the antenna according to $V_{in0} = \sqrt{2R_A P_{rf}}$.

It can be shown that the ratio of the -3 dB bandwidth to the resonant frequency is equal to the reciprocal of the circuit quality factor.

$$\frac{BW}{\omega_0} = \frac{1}{Q} \tag{3.43}$$

This relation clearly demonstrates the tradeoff between bandwidth and the ratio of boosting which depends on overall Q. For a specific resonant frequency, higher Q is achievable through a narrower bandwidth.

Another design parameter that should be optimized is the conversion efficiency of the RF harvester. As mentioned in the first chapter, RF to DC conversion efficiency is defined as

$$\eta = \frac{P_{dc}}{P_{rf}} = 1 - \frac{P_{loss}}{P_{rf}} \tag{3.44}$$

which can be rewritten in the following form that is used in calculating the conversion efficiency of the simulated circuit in the next chapter.

$$\eta = \frac{V_{DC}^2}{R_L P_{rf}} \tag{3.45}$$

This relation provides a measure of the effectiveness of the circuit to convert AC power to DC power with minimum power dissipation, and indicates that an optimal value for the load resistance should be found to maximize the efficiency.

The expressions derived in chapter 2 for calculating R_{in} illustrated the dependence of the the input resistance on the power consumption due to load. A larger load results in a smaller power consumption, and this subsequently yields a smaller overall P_{in} and thus larger R_{in}. It is observed based on the matching network quality factor, i.e. $Q = \omega_0 R_{in} C_{in}$, that the larger the value for R_{in}, the higher the voltage boosting achieved. However, there is a degradation in the conversion efficiency due to a high resistive load and we would not be supplying enough power to the load. The bottom line is that there is a tradeoff in the R_{in} and R_L values and a good design should take into account the optimum operating conditions under which maximum boosting and maximum efficiency are achieved.

Chapter 4

Simulation Results for the Voltage Doubler Based RF Energy Harvester

In this chapter, Cadence software package is utilized along with RFDE/ADS simulator to simulate the operation of the RF energy harvester using the IBM $0.13\mu m$ CMOS technology. The results obtained for a single stage of the voltage doubler using conventional matching are presented first. Subsequently the design is improved using a π-match configuration for the matching circuit. Finally the simulation results for an already fabricated dual-band energy harvester are presented that utilizes specific circuit enhancements. Harmonic balance analysis is the main method employed to obtain the optimum design parameters for the harvester at the desired operating frequency.

4.1 Single Stage Voltage Doubler Circuit

In order to investigate the operation of the RF energy harvester in terms of resonance and voltage boosting, we start off with a single stage of the voltage doubler circuit with an inductor added in between the source and doubler. The inductor thus forms an L-match network with the equivalent input stage of the doubler and serves to achieve both voltage boosting and impedance matching. Subsequently an additional capacitor is introduced to the circuit to form a π-match network in an

attempt to achieve impedance matching to 50Ω while having the maximum voltage boosting.

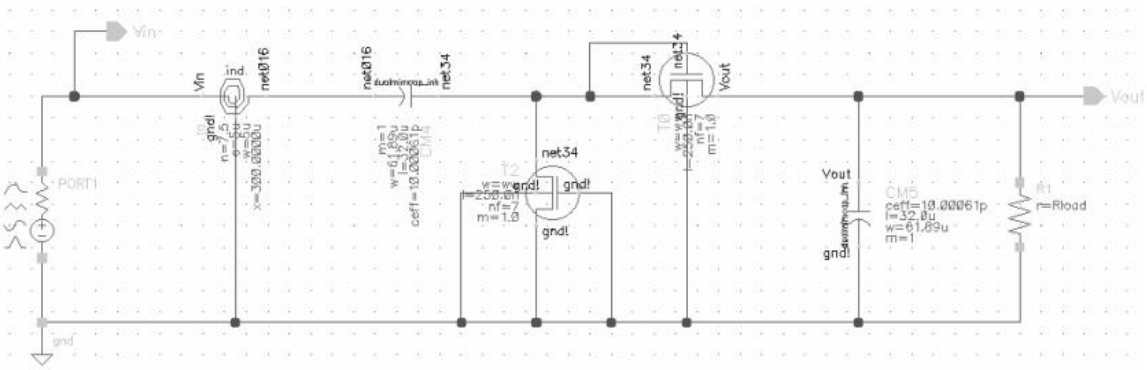

Figure 4.1: Single stage of RF harvester simulated in Cadence.

4.1.1 L-Match

The simulated circuit consisting of two diode-connected NMOS transistors, a planar spiral inductor, resistive load, and a port is illustrated in Fig. 4.1. The port component represents the harvester antenna and sets the source resistance, input power, and operating frequency. The center frequency is selected to be around 2.4 GHz that is a popular ISM band and thus there is high concentration of ambient RF available for potential use in RF scavenging. The inductor should be designed such that its peak Q frequency is higher than the circuit resonant frequency. The threshold voltage for the NMOS transistors in 0.13μm technology is 355 mV, which imposes the minimum voltage requirement across each transistor to turn the device on.

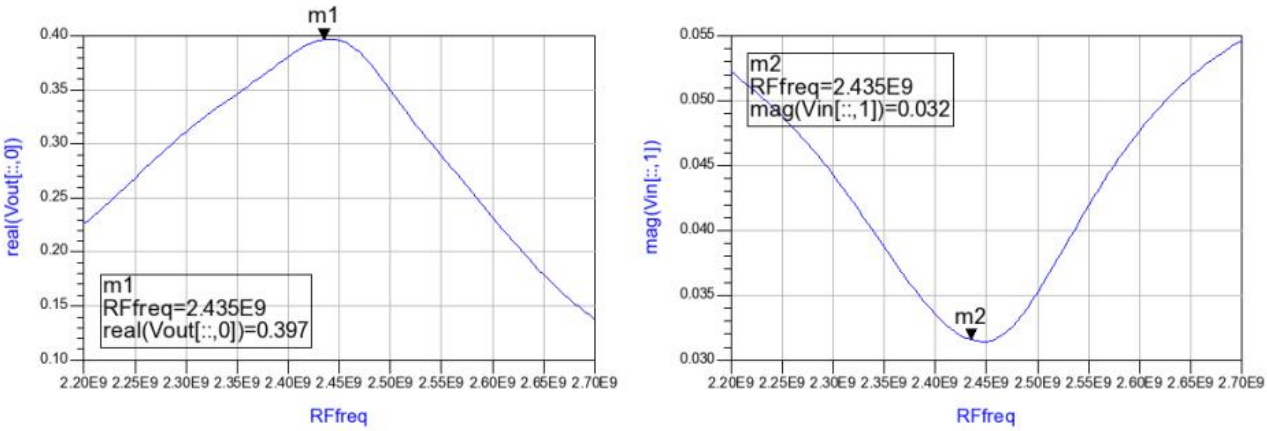

Figure 4.2: Simulated output voltage (left) and input voltage (right) of the RF harvester vs. RF frequency using L-match.

For our simulation, the inductance of 15.4 nH achieves maximum output voltage at 2.435 GHz. As seen in Fig. 4.2, output voltage of 400 mV is achieved from the source voltage of 32 mV at the resonant frequency. This corresponds to total capacitance of 0.28 pF. The main portion of this capacitance comes from the gate to source capacitance of the transistors. Parasitic capacitance due to the inductor and the coupling capacitors accounts for the remaining portion. The optimum transistor width that provides the required capacitance is thus found ($74\mu m/0.25\mu m$). According to (3.45), there is an optimum value for the resistive load that maximizes the conversion efficiency. This is due to the fact that while a higher load increases the output voltage, there is a point where V_{DC} starts to saturate and the rate of increase in R_L is faster than the rate of increase in V_{DC}. The load value of 1 MΩ is

determined such that it satisfies the minimum output voltage requirement with an input power of -16 dBm.

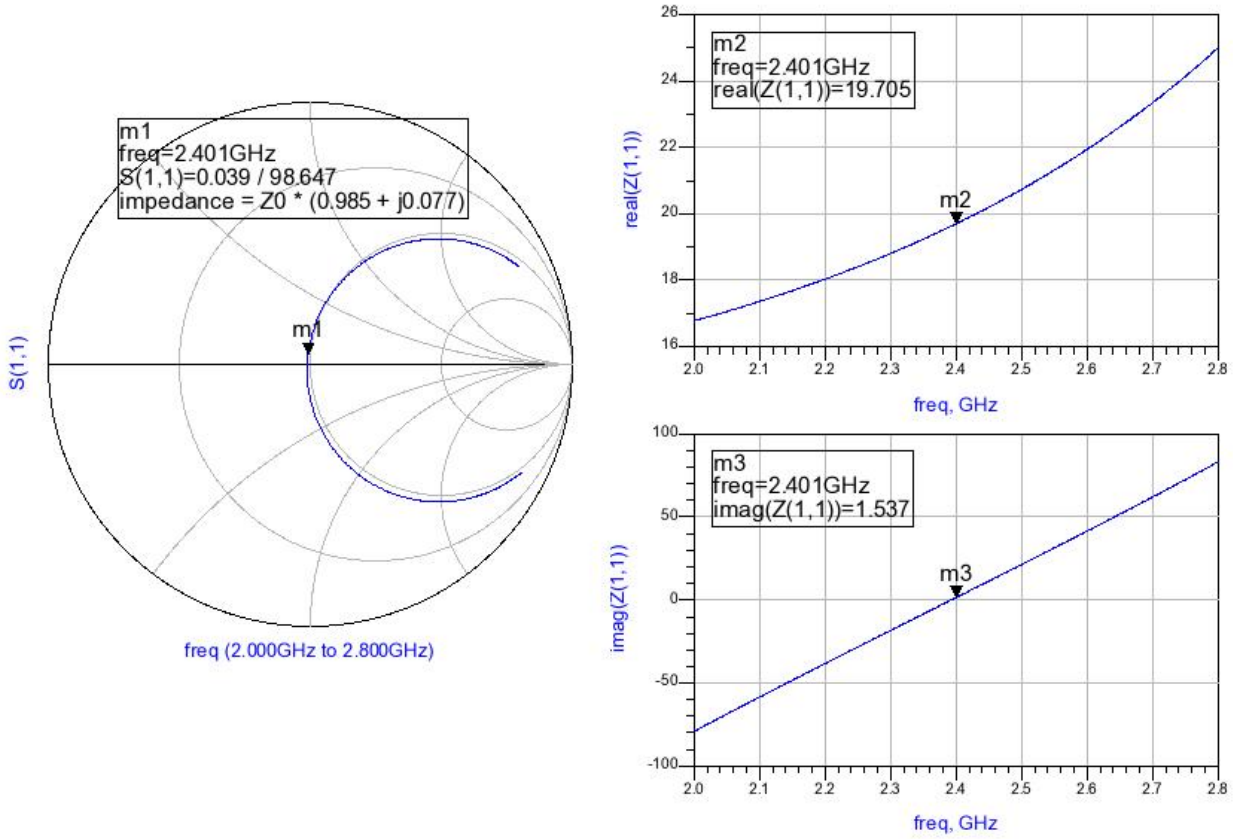

Figure 4.3: Simulated input impedance of the circuit showing real and imaginary components.

The S-parameter simulation results are presented in Fig. 4.3, which indicate matching to 20 Ω at the designed operating conditions. Source resistance sweep also shows that maximum output voltage is achieved with the source resistance of 20 Ω as seen in Fig. 4.4. As a result, if the antenna is designed to have a radiation

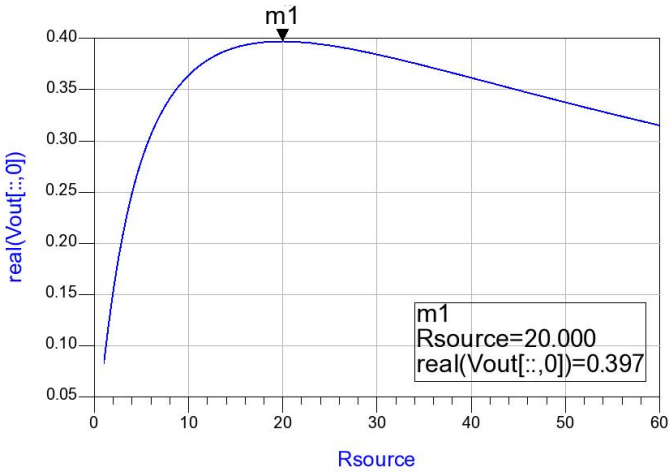

Figure 4.4: Simulated output voltage vs. source impedance at resonant frequency.

resistance of an identical value, minimum energy reflection occurs. This however, poses a problem when connecting the harvester to transmission lines and coaxial cables that have characteristic impedance of 50 Ω.

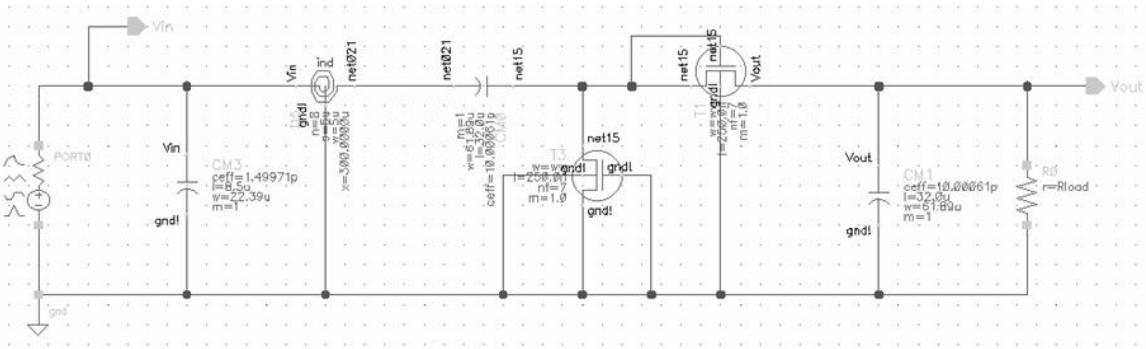

Figure 4.5: Single stage of RF harvester simulated in Cadence with π-match network.

4.1.2 π-match

In order to have an additional degree of freedom that allows us to match to 50 Ω while achieving maximum voltage boosting at the resonant frequency, the conventional L-match is replaced with π-match network by introducing a capacitor between the input terminal of the inductor and ground (Fig. 4.5). As elaborated in the previous chapter, the inductor can now be regarded as two series inductors with one serving to transform down the input resistance of the harvester and the other used to transform the intermediate resistance up to the source resistance.

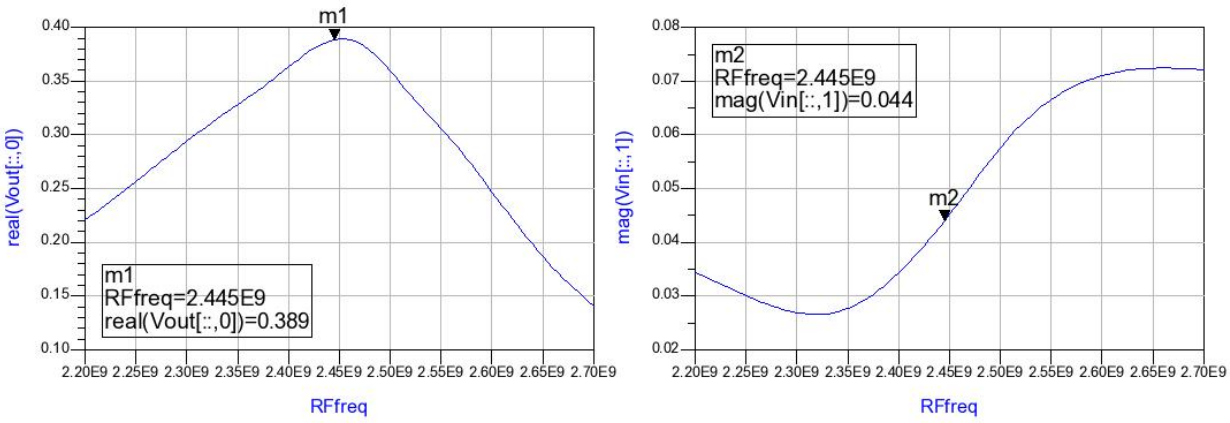

Figure 4.6: Simulated output voltage (left) and input voltage (right) of the RF harvester vs. RF frequency using π-match.

Simulation results for the designed harvester indicate that for the inductance of 16.4 nH and capacitance of 1.5 pF, maximum output is achieved at 2.445 GHz as shown in Fig. 4.6. The transistor dimensions are the same as the previous L-match

case ($74\mu m/0.25\mu m$), with the input power of -16 dBm and load resistance of 1.5 MΩ.

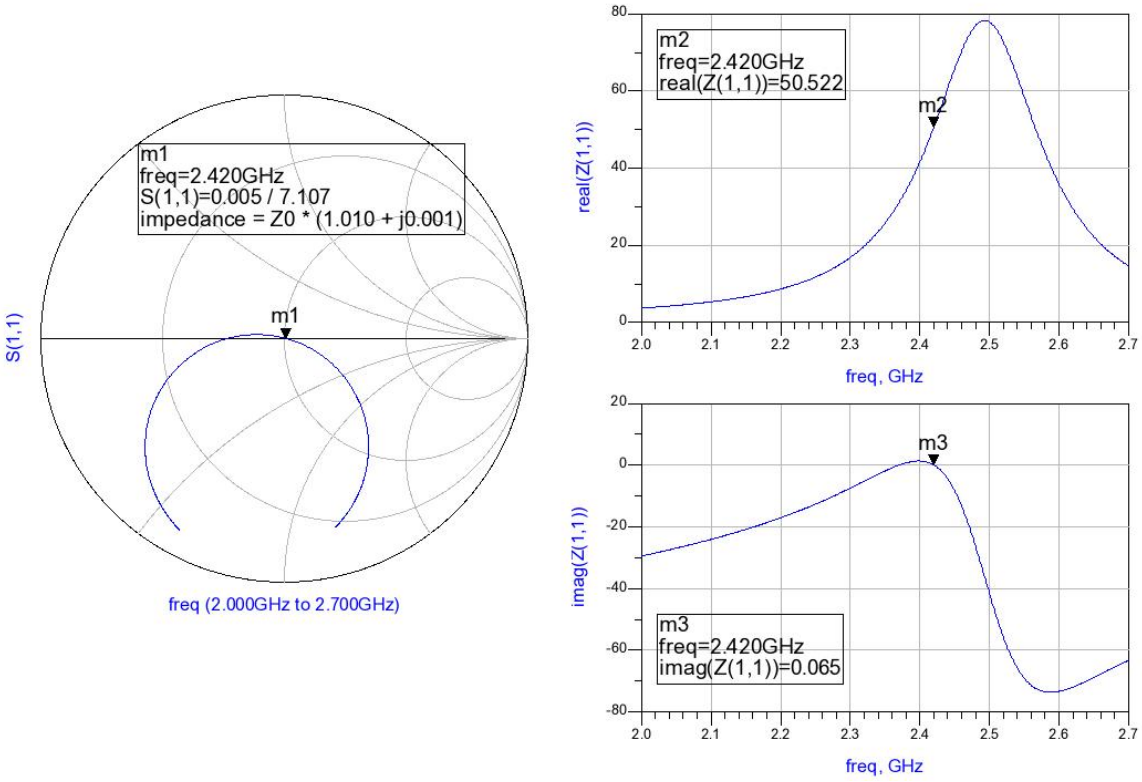

Figure 4.7: Simulated input impedance of the circuit showing real and imaginary components using π-match.

As S-parameter simulation results shown in Fig. 4.7 indicate, the input impedance of the harvester is now shifted to 50 Ω. The negligible imaginary component of the impedance suggests that at 2.42 GHz, the inductance resonates out the total capacitance of the circuit, and thus the remaining real part needs to be matched to the source resistance. Therefore, this methodology can be implemented in RF harvester design to ensure minimum power loss occurs at the input to the

harvester chip from the microstrip lines or receiving antenna. It should be pointed out that after layout, the parasitic resistance introduced by the inductor should also be taken into account. Therefore in general, the total resistance due to the doubler circuit and the inductor should be matched to the source resistance.

4.2 Dual-Band RF Energy Harvester

In order to obtain a higher output voltage from low input power levels, multiple stages of the doubler circuit are stacked together. Moreover, this reduces the requirement on the transistor sizes used for a single stage of the doubler circuit. Additional doubler stages contribute to the total input capacitance of the circuit and obviate the need for wide transistors to provide high capacitance.

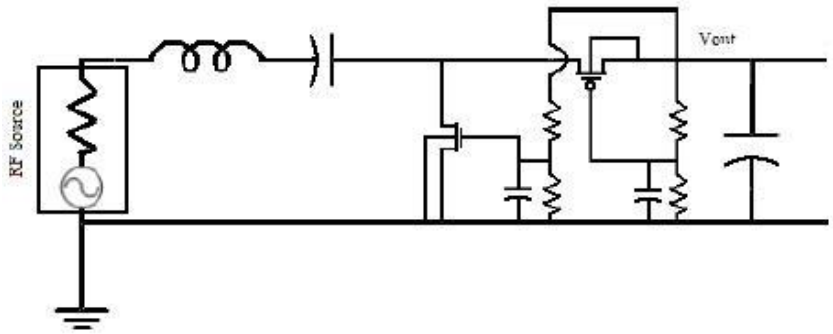

Figure 4.8: Single stage of RF harvester using self-biasing and floating body PMOS presented in [1].

To improve the conversion efficiency of the RF harvester, it is essential to

minimize the power loss in the circuit. One common approach is to reduce the threshold voltage of the transistors, so that they are turned on at a lower voltage level. As discussed in chapter 1, different methods have been implemented to achieve threshold voltage reduction [6, 5]. In this work we use the design proposed by [1], which is shown in Fig. 4.8. The second NMOS transistor used in the conventional design is replaced with a PMOS with floating body to reduce losses due to body effect. Furthermore, DC self-biasing is achieved through resistive networks that act as output voltage dividers to bias the gate and thus decrease the threshold voltage of the diode-connected transistors. Multiple stages of the voltage doubler circuit utilizing these improvements can be cascaded to obtain a DC output voltage level of 1V required for digital electronics applications.

4.2.1 Simulation Results

The proposed design forms the basis for the dual-band RF harvester that is capable of harvesting ambient RF energy in two bands. Fig. 4.9 shows the schematic of the dual-band harvester designed by [14]. It consists of two parallel multi-stage voltage doubler circuits, each designed to achieve a low matched impedance at its operating frequency, and high (ideally infinite) impedance at the other band frequency. The two frequency bands for this design are 900 MHz and 1.9 GHz, in which there is abundant ambient RF concentrated due to ISM band and cell phone communications. The harvester chip consists of the transistors and the coupling

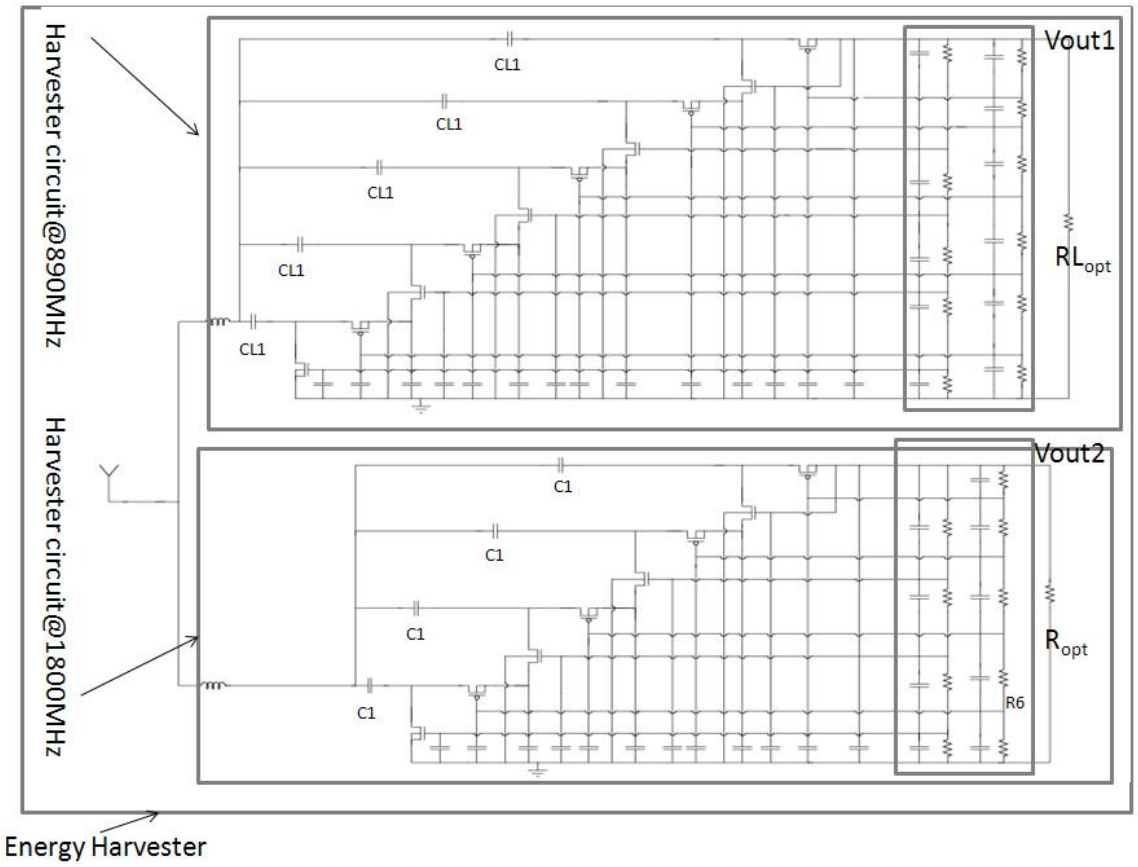

Figure 4.9: Dual-band RF energy harvester proposed in [14].

capacitors, while the network of resistors and capacitors (used for stability) that is encircled for each band is realized off-chip. The output load in each case is optimized to yield maximum efficiency.

Simulation results for the lower and higher bands of the dual-band harvester output voltage and conversion efficiency with -19 dBm input power are presented in Figs. 4.10 and 4.11 respectively. These results will be compared with corresponding measurement results in the next chapter. The simulated input impedance curves are given in Fig. 4.12 which indicate the lower band is matched to 40Ω while the

higher band is matched to 12Ω. The two inductors used for matching and boosting are 21.79 nH and 18.96 nH for the 900 MHz and 1.8 GHz respectively.

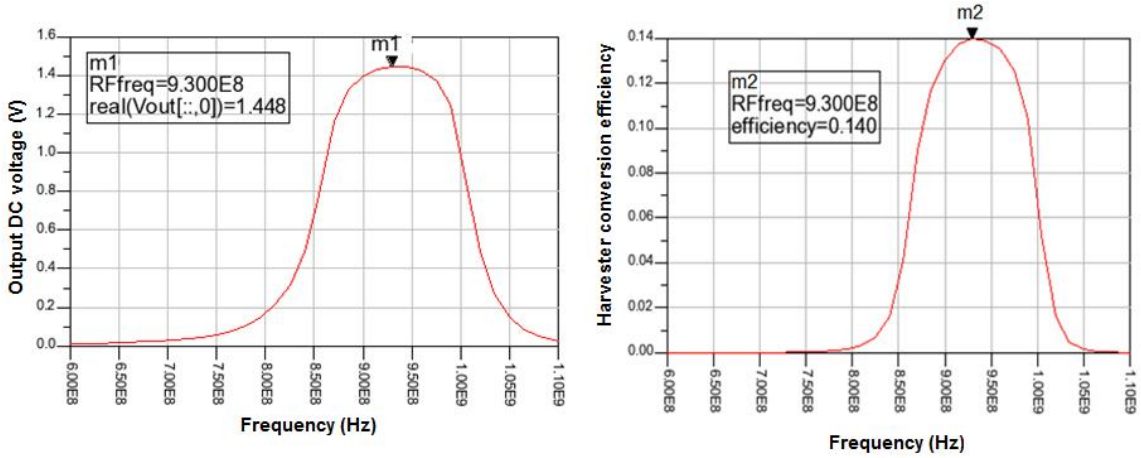

Figure 4.10: Simulated output voltage (left) and conversion efficiency (right) for the lower frequency of the dual-band harvester.

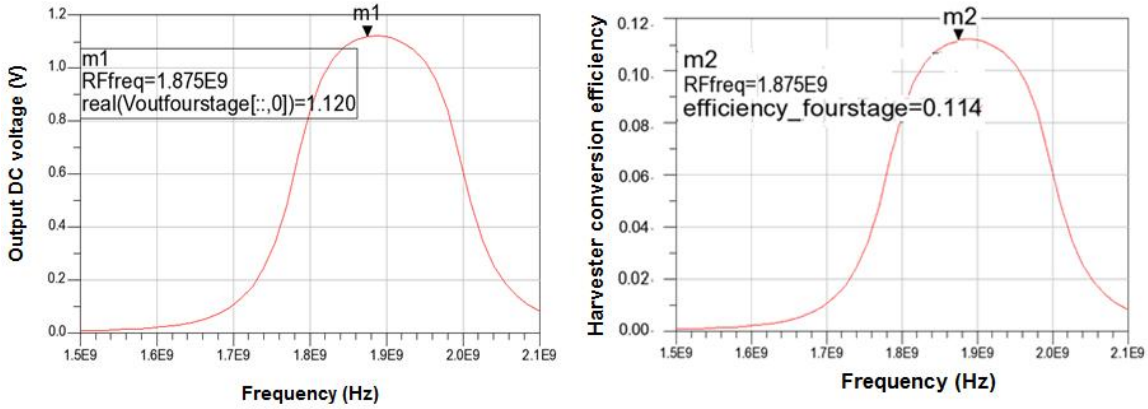

Figure 4.11: Simulated output voltage (left) and conversion efficiency (right) for the higher frequency of the dual-band harvester.

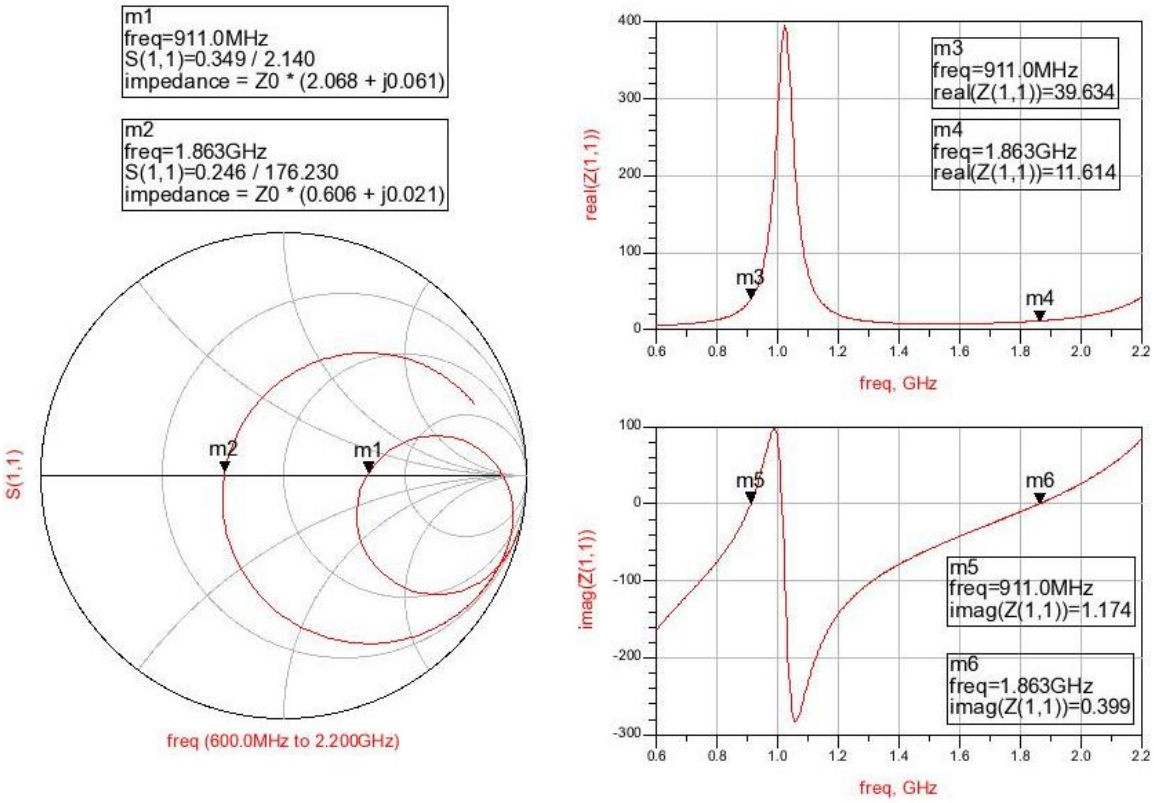

Figure 4.12: Simulated input impedance of the dual-band harvester.

4.2.2 Comparison with Analytical Results

The input resistance found using S-parameter analysis corresponds to the transformed value of the input resistance of the rectifier through the L-match circuit formed by the matching inductor and the input capacitance. The corresponding value of the input resistance is subsequently compared with the value obtained using the analytical method presented in chapter 2 for the identical transistor sizes and circuit parameters. If we demonstrate that the analytical expression is capable of accurately predicting the input equivalent resistance and thus the required source resistance for input impedance matching, then the circuit and device parameters can be designed to achieve an arbitrary match (for example to 50Ω).

The simulation results obtained for the dual-band RF harvester, illustrate the conditions for maximum voltage boosting, while setting the design requirements for impedance matching.For the lower frequency band, inductance of 21.79 nH is used to obtain the maximum output voltage at 930 MHz across the 1.5 MΩ load. Besides, the matched input impedance is about 40 Ω. The boosted input voltage after the inductor with the input power of -19 dBm is 0.27 V, which gets rectified and amplified in the stack of five doubler stages to yield an output voltage of 1.4 V. The DC self-biasing used in the design, serves to decrease the effective threshold voltage of the transistors. We intend to compare the simulated circuit operation with the analytical derivation and its numerical solution introduced in chapter 2. The design parameters are used in the code representing the input-output characteristic equation to obtain the output voltage with the given boosted input voltage and other design parameters. Even though the numerical method is based on the doubler circuit consisting of NMOS transistors, since the width of the simulated PMOS transistors is about twice the width of NMOS transistors, it can be assumed that the circuit overall is composed of identical n-channel MOSFETs with their width equal to 3.78 μm. Moreover, the threshold voltage in this case is replaced with $V_{th} - V_{bias}$ (= 0.11 V). The resulting output voltage is found to be 1.12 V, which is close to the simulated result.

Furthermore, the equivalent input resistance of the harvester circuit is computed from calculation of power terms due to saturation and leakage current as well

as the output load. With the design parameters used in the simulated circuit, the equivalent rectifier resistance obtained from the code is 1.11 KΩ. Furthermore, requirement of operation at resonance yields the circuit total capacitance value which is equal to 1.435 pF. As a result by applying the basic L-match formula derived in chapter 3, the transformed series resistance corresponding to the obtained equivalent resistance is 13.6 Ω. On the other hand, the S-parameter analysis of the spiral inductor alone used in a circuit together with a tuning capacitor suggests that the inductor itself has a parasitic resistance of 37 Ω. Therefore, the contribution of both rectifier and inductor resistance accounts for the total input resistance of the harvester giving a value of 50.6 Ω. As S-parameter simulation results in Fig. 4.12 indicate, at the lower frequency the input impedance is around 40 Ω. Considering the sharp transition in this region, the obtained impedance value yielded a reasonable measure of the harvester resistance that allows us to have a predetermined impedance level for the matching purposes. This result is consistent with the antenna resistance of 50 Ω designed for this band.

Chapter 5

Measurement Results for the RF Energy Harvester

In this chapter the measurement results of the dual-band RF energy harvester chip introduced in the previous chapter and fabricated using the IBM 0.13μm CMOS technology are presented. Initially the chip was tested by direct connection of the harvester PCB to the network analyzer as the power source. The corresponding output voltage and input impedance values were measured at the operating frequency bands of 900 MHz and 1.9 GHz. The input impedance measurements were used to improve the planar monopole antenna design for enhanced impedance matching. Subsequently the harvester-antenna system was fabricated and its resulting output voltage was measured for both bands.

In order to determine the input impedance and energy reflection using the network analyzer, Smith chart and S-parameter graph were utilized respectively. Smith chart allows for measurement of the real and imaginary parts of the input impedance for the harvester board in a specified frequency range. Proper calibration should be carried out to account for the SMA connector and microstrip line before the input to the harvester board. S11 or reflection coefficient is a measure of the amount of RF energy reflected at the feeding point to the harvester. For practical purposes, S11 should be smaller than -10 dB at the harvester resonant frequency.

5.1 Design Considerations for the Receiving Antenna

A dual-band monopole antenna was initially designed based on the impedance requirements imposed by the simulation results of the dual-band harvester. Once the chip was fabricated, the approach taken was to measure the input impedance of the integrated board composed of the harvester chip and the off-chip biasing components with the direct input RF from the network analyzer. After calculating the input impedance right at the input to the chip by using transmission line de-embedding procedure, two new antennas with different frequency and thus impedance characteristics were designed. As will be discussed in the next sections, this helps us improve the harvester system performance.

5.1.1 Measured Input Impedance of the Dual-Band Harvester

The Smith chart is used to verify the input impedance of the harvester chip at the operating frequencies and also to refine the antenna impedance requirements to improve the design for the higher band. The measured input impedance and S11 plots for the lower and higher band are shown in Figs. 5.1 and 5.2 respectively. For each point measured in the Smith chart, the corresponding point is indicated in the S11 plot.

The input impedance values of interest are tabulated in Table 5.1. Subsequently, the de-embedding procedure is applied to consider the effect of the transmission line between the SMA connector and the input pin of the chip, and to

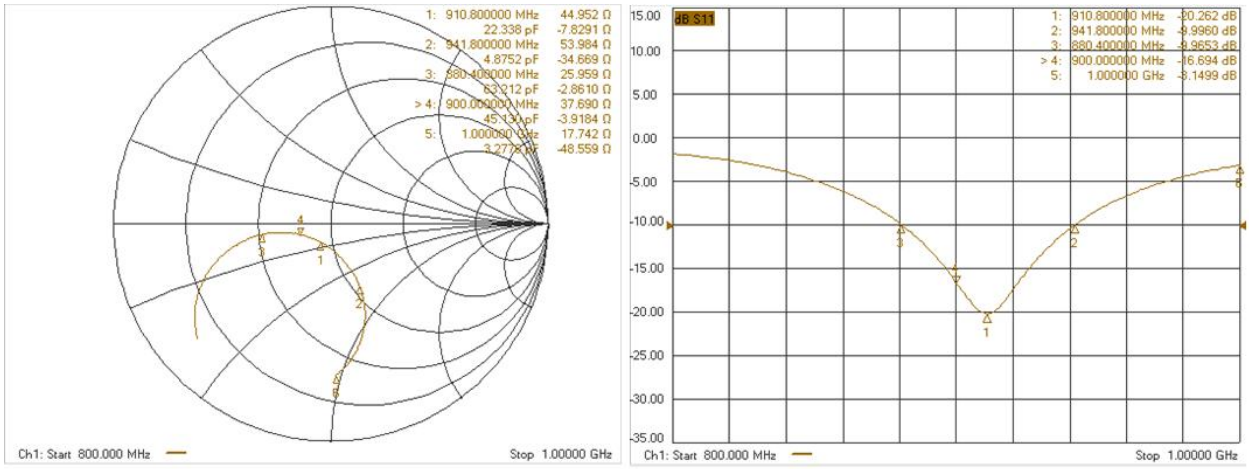

Figure 5.1: Measured input impedance (left) and S11 (right) around 900 MHz frequency band.

calculate the original input impedance of the harvester. The input impedance of a transmission line of length l with characteristic impedance Z_0 terminated in a load impedance Z_L is calculated as

$$Z_{in} = Z_0 \frac{Z_L + jZ_0 \, tan\beta l}{Z_0 + jZ_L \, tan\beta l} \tag{5.1}$$

We need to find the load impedance which is our harvester chip from the measured input impedance Z_{in}. Rearranging this relation gives the load impedance in terms of the input impedance measured and the characteristic impedance of the line

$$Z_L = Z_0 \frac{Z_{in} - jZ_0 \, tan\beta l}{Z_0 - jZ_{in} \, tan\beta l} \tag{5.2}$$

where the propagation constant β is defined as

$$\beta = \frac{2\pi f}{c} \sqrt{\epsilon_{eff}} \tag{5.3}$$

Coplanar waveguide model was used to estimate the characteristic impedance of the transmission line as well as the effective dielectric constant. The coplanar

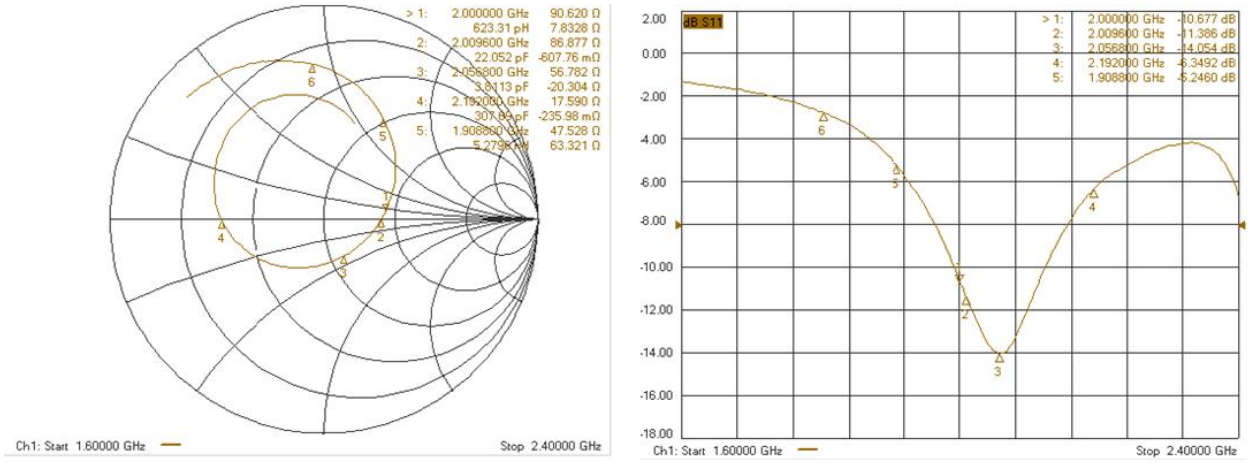

Figure 5.2: Measured input impedance (left) and S11 (right) around 2 GHz frequency band.

waveguide structure for our PCB, and the dielectric constant of FR4 board yielded the characteristic impedance (Z_0) of 78.77 Ω and effective dielectric constant (ϵ_{eff}) of 2.735. For each frequency, the corresponding β can be computed, and used together with the Z_0 found to calculate the load impedance from (5.2). This impedance thus, corresponds to the de-embedded input impedance of the harvester chip. The calculation results are summarized in Table 5.1. Since according to both simulation and measurement results, the lower frequency band is already matched to 50 Ω, the approach mentioned is only implemented for the higher band.

Table 5.1: Measured harvester input impedance (Z_{in}) and corresponding calculated load impedance (Z_L) values for different frequencies.

Frequency (GHz)	Z_{in}	Z_L
1.8032	14.51+44.33j	11.49-17.25j
1.9088	47.53+63.32j	26.27+0.09j
2.0000	90.62+7.83j	70.85+9.75j
2.0568	56.78-20.30j	111.05-26.65j

To have impedance matching, the impedances of the harvester and antenna should be complex conjugate of each other. As observed from the table, the design goal for the antenna aside from providing 50 Ω at 900 MHz, is then to achieve 26 Ω at 1.9 GHz, or 70 - j10 Ω at 2 GHz. Therefore, two antenna designs are proposed that differ in their higher band characteristics.

5.1.2 Dual-Band Antenna Design

The receiving antenna designed for the harvester system was a PCB-based planar dual-band monopole antenna. The antenna must satisfy the impedance requirements imposed by the harvester design to achieve impedance matching and thus minimize the reflection between the antenna and the harvester. Based on the harvester simulation results, the original antenna was designed to provide impedances of 50 Ω at the lower band and 12 Ω at the higher band. Since for the dual-band RF energy harvester under consideration, input impedance for both bands is real, the antenna is designed to provide a radiation resistance equal to the harvester resistive input impedance. Also, the antenna can be easily integrated with the harvester chip on the same printed circuit board [22].

As discussed earlier, measurement results of the harvester input impedance led to two new antenna designs. The basic structure of the dual-band antenna designed for operation in 900 MHz and 1.9 GHz (or 2 GHz) bands is illustrated in Fig. 5.3. The antenna consists of a ground plane on the back and three connected microstrip

	Design A	Design B
L11	17	17
L12	48	48
L2	17.5	16
L3	17.5	19
d1=d2	10	10
d3	0	4.5
g1	3	3
g2	4	4
w1	1	1
w2	0	3

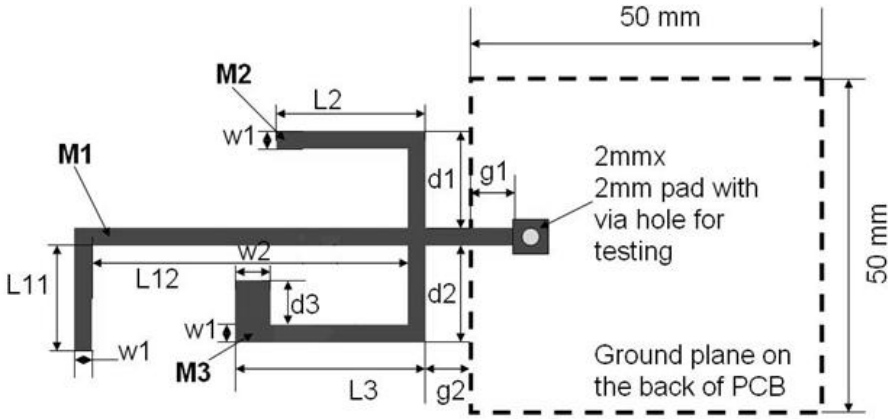

Figure 5.3: Dual-band monopole antenna structure with two sets of design parameters (in mm).

lines on the front of the PCB. The length and geometry of these microstrip lines can be adjusted to provide the desired impedances at different resonant frequencies. For both antenna designs, the central arm (M1) is designed to provide 50 Ω at the lower band, while the side arms (M2 and M3) determine the specific resonant frequency and impedance of the higher band.

The measured S11 and impedance for design A and B are shown in Figs. 5.4 and 5.5 respectively. For design A, the two symmetric side arms provide impedance of 70+j16 Ω at 2GHz, while in design B the different structure of the side arms provides the impedance of 22.55+j0.9 Ω at 1.9 GHz [22].

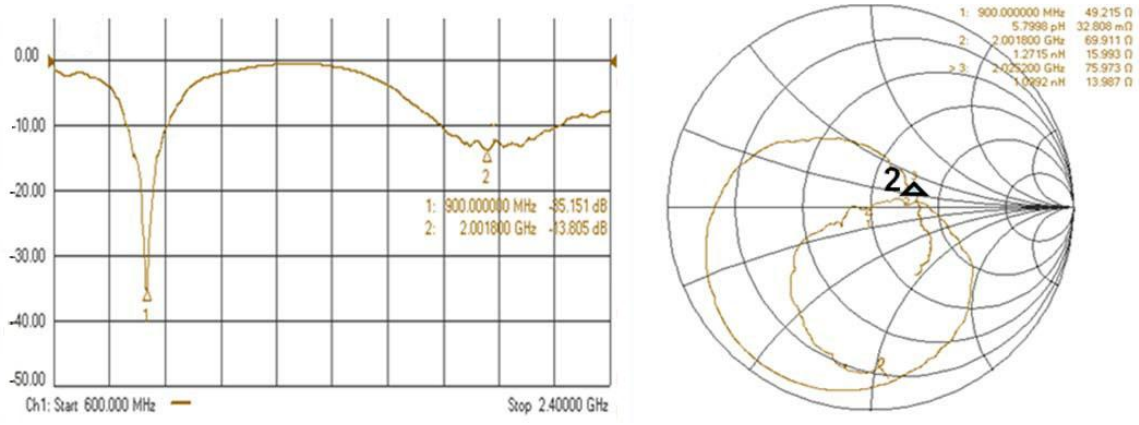

Figure 5.4: Measured S11 and impedance for dual-band antenna design A.

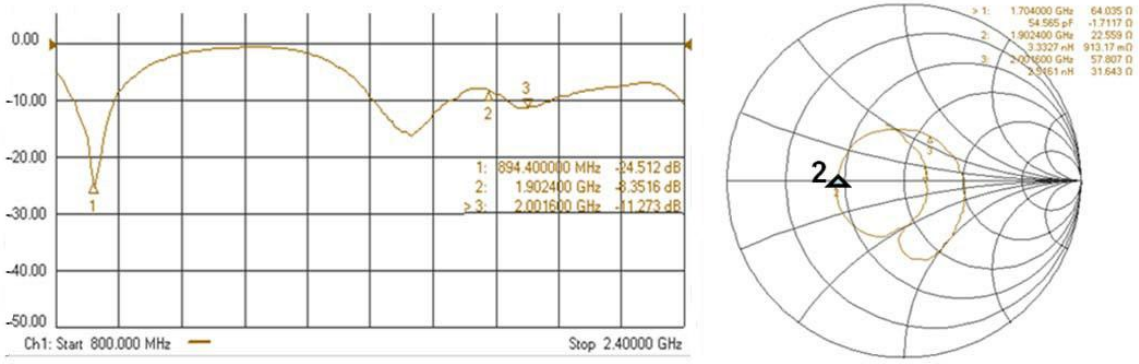

Figure 5.5: Measured S11 and impedance for dual-band antenna design B.

5.2 Measurement Results for the Dual-Band RF Energy Harvester

In this section, plots of the DC output voltage for the desired range of frequencies and the corresponding conversion efficiency found using (3.45) are presented. Furthermore, the effect of the input RF power level and the resistive load is investigated. The harvester board consists of the harvester chip and the off-chip biasing components, with the RF power fed directly from the network analyzer.

5.2.1 Output Voltage and Conversion Efficiency

Initially the dual-band harvester together with the network of off-chip resistors and capacitors as depicted in Fig. 4.9 was tested. Since the off-chip capacitors are for the mere purpose of stability and do not affect the DC voltage or the input impedance, the subsequent experiments were carried out with only the biasing resistor network as well as the load resistor and capacitor, and the network of capacitors was eliminated.

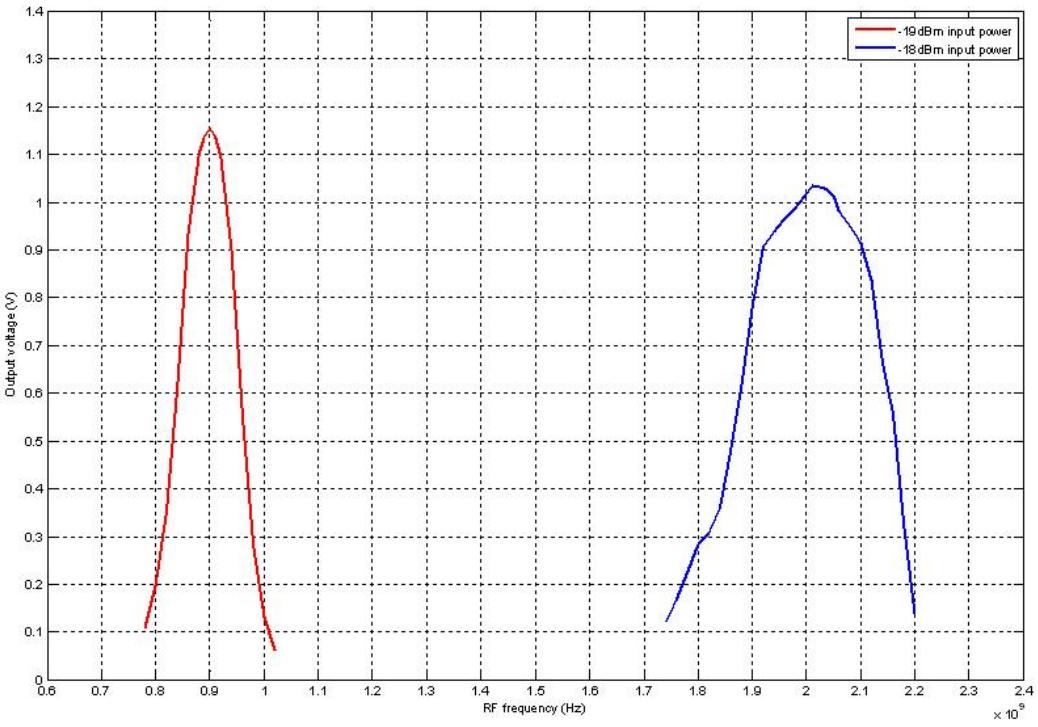

Figure 5.6: Measured output voltage for two bands of the dual-band RF energy harvester.

Fig. 5.6 demonstrates the output DC voltage measured by sweeping the frequency with the two operating frequencies centered at 900 MHz and 2 GHz. Ac-

cording to this plot, the 3-dB bandwidth can be estimated to be 92 MHz for the lower band and 238 MHz for the upper band. It is observed that higher output voltage is achieved at 900 MHz with a lower RF input power level. The reason is that the harvester is designed to be matched to 50 Ω at the lower band, and thus the power loss due to the reflection from the transmission line and the harvester input is lower compared to the 2 GHz band which is not matched to 50 Ω.

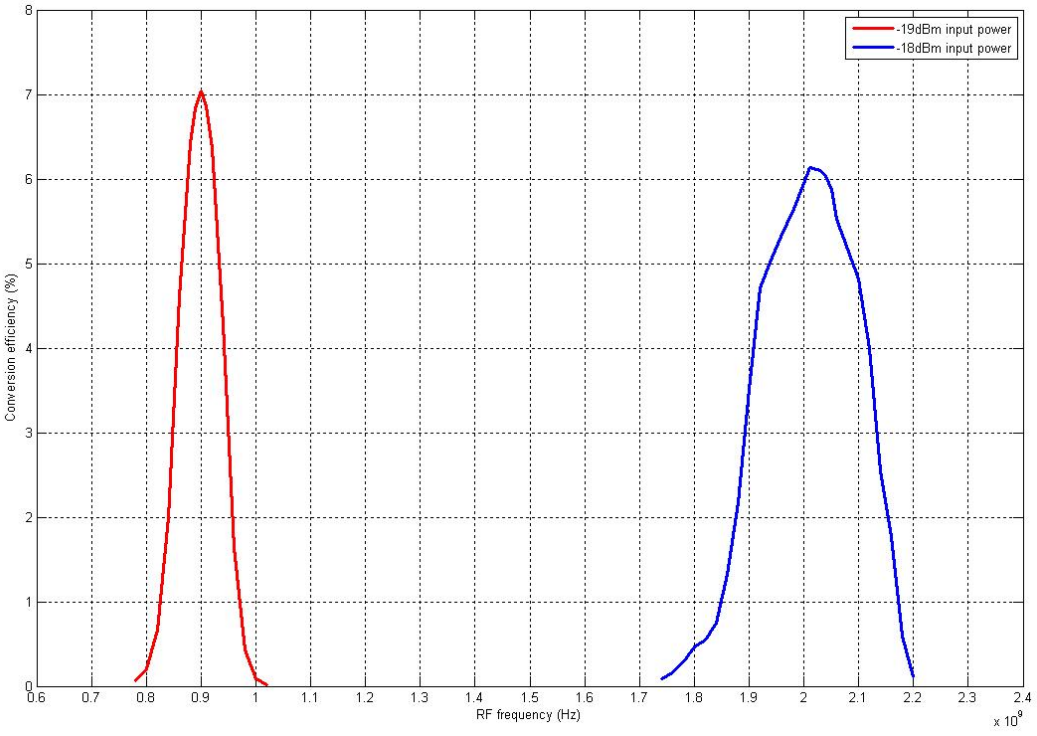

Figure 5.7: Measured conversion efficiency for two bands of the dual-band RF energy harvester.

The resistive loads used for the circuit were 1.5 MΩ and 1.1 MΩ for the lower and upper band respectively, that were optimized to obtain the maximum conversion efficiency. The plot of RF to DC power conversion efficiency calculated from the

measured voltage data is given in Fig. 5.7. The efficiency is about 0.07 for 900 MHz and 0.06 for 2 GHz, which is clearly lower than the predicted simulated values. The parasitics introduced due to chip packaging and PCB layout, degrade the overall efficiency, as well as change the input impedance of the harvester. This in turn causes the reflection coefficient to change and results in the upper resonant frequency to shift to a higher value compared to what predicted by simulations.

5.2.2 Input Power and Output Load Sweep

In the next step, the input power was gradually increased with the frequency band fixed at the value that yielded the highest output voltage. The results are depicted in Fig. 5.8. Intuitively, as input power increases, the input voltage level available becomes higher and thus output voltage increases. However, according to the definition of the conversion efficiency in (3.45), a point is reached where the increase in output voltage is compensated by the increase in input power and efficiency starts to decrease. The optimum input power found is -18 dBm for 900 MHz and -17 dBm for the 2 GHz band, compared to -19 dBm used in the harvester simulations. The simulations for the higher band were performed with the assumption of impedance matching with the source, which justifies the higher power required for this band during the experiments.

The resistive loads for both bands were optimized using simulation to yield the maximum conversion efficiency. In order to observe the effect of changing load

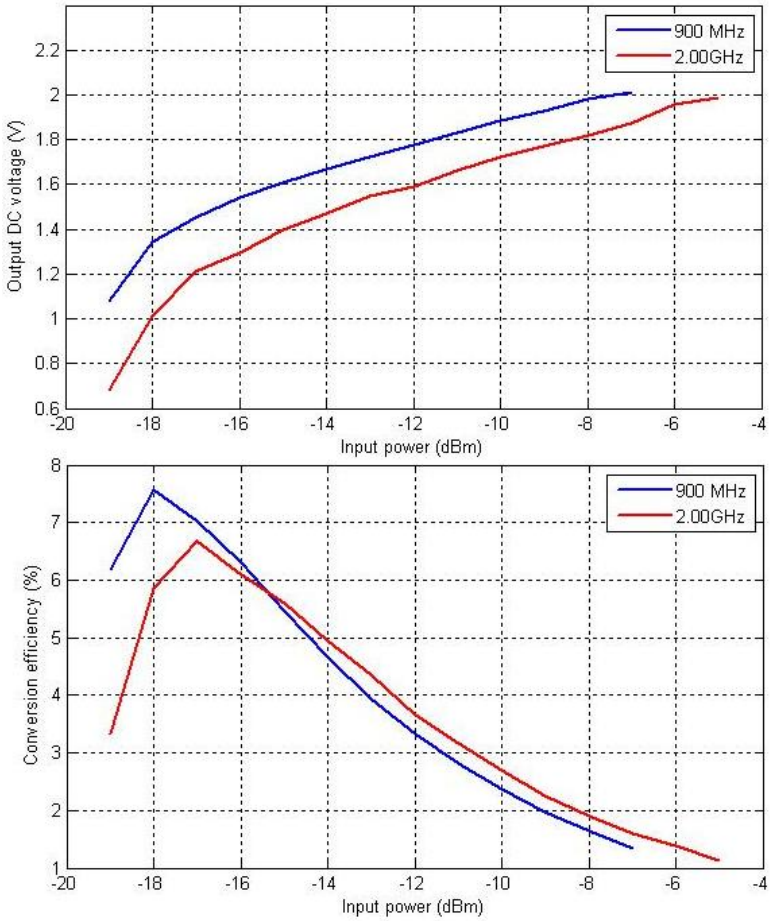

Figure 5.8: Measured output voltage (top) and conversion efficiency (bottom) for both bands vs. RF input power.

on the output DC voltage and conversion efficiency, resistor values were changed by soldering and desoldering the load on the same board. Input power of -19 dBm for the lower band (900-910MHz) and -18 dBm for the upper band (2.00-2.05GHz) was fed in. As seen in Fig. 5.9, as load increases, the output voltage is increased until it starts to saturate. Again there is an optimum point in the efficiency plot, where the rate of increase in the voltage is compensated by the increase in the load. The optimum loads are identical to the values found from simulation, i.e. 1.5 MΩ and

1.1 MΩ for the lower and upper band respectively.

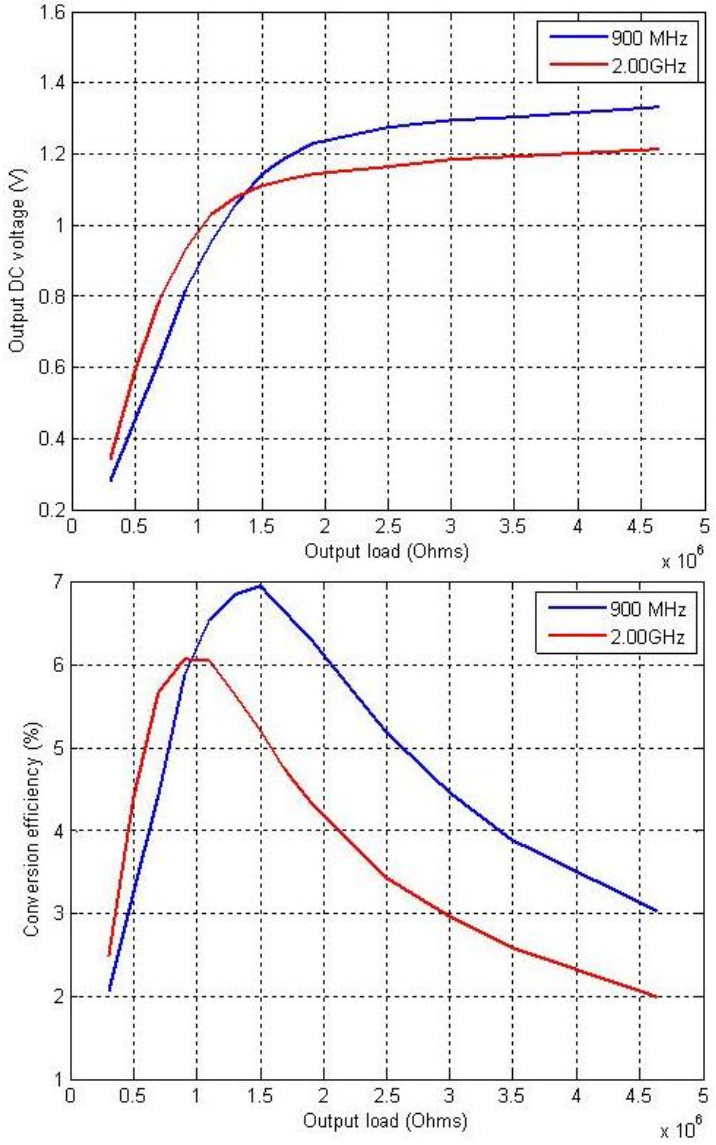

Figure 5.9: Measured output voltage (top) and conversion efficiency (bottom) at both bands vs. load resistance.

5.3 Measurement Results for the Integrated Harvester-Antenna System

According to the approach discussed in the first section, two antennas were designed for the antenna-harvester system. The antenna was subsequently integrated with the harvester on the same board, to form a fully passive RF harvester system that is capable of extracting ambient RF radiation and turning it into DC voltage above 1V. In the integrated antenna-harvester system, the input RF is fed to the chip directly from the planar receiving antenna. The experimental setup consists of a transmitting antenna connected to the network analyzer through a microstrip wire and fed with -3 dBm RF power for the lower band and 0 dBm for the higher band. The harvester system is placed nearby with the orientation of the receiving antenna adjusted to yield at least 1 V output voltage around the peak resonant frequency.

The output voltage as a function of frequency is shown in Fig. 5.10. These measurements were obtained for the system consisting of the dual-band harvester connected to the antenna design A. According to this plot, the 3-dB bandwidth is about 32 MHz for the lower band and 148 MHz for the upper band, which indicates a narrower bandwidth compared to the harvester alone. The maximum voltage for both bands is relatively higher than the measured data for the harvester, which is due to the fact that the input power received by the antenna is probably higher in this case compared to the input power levels used in the measurements of the previous section. Furthermore, the peak voltage for the higher band occurs at around

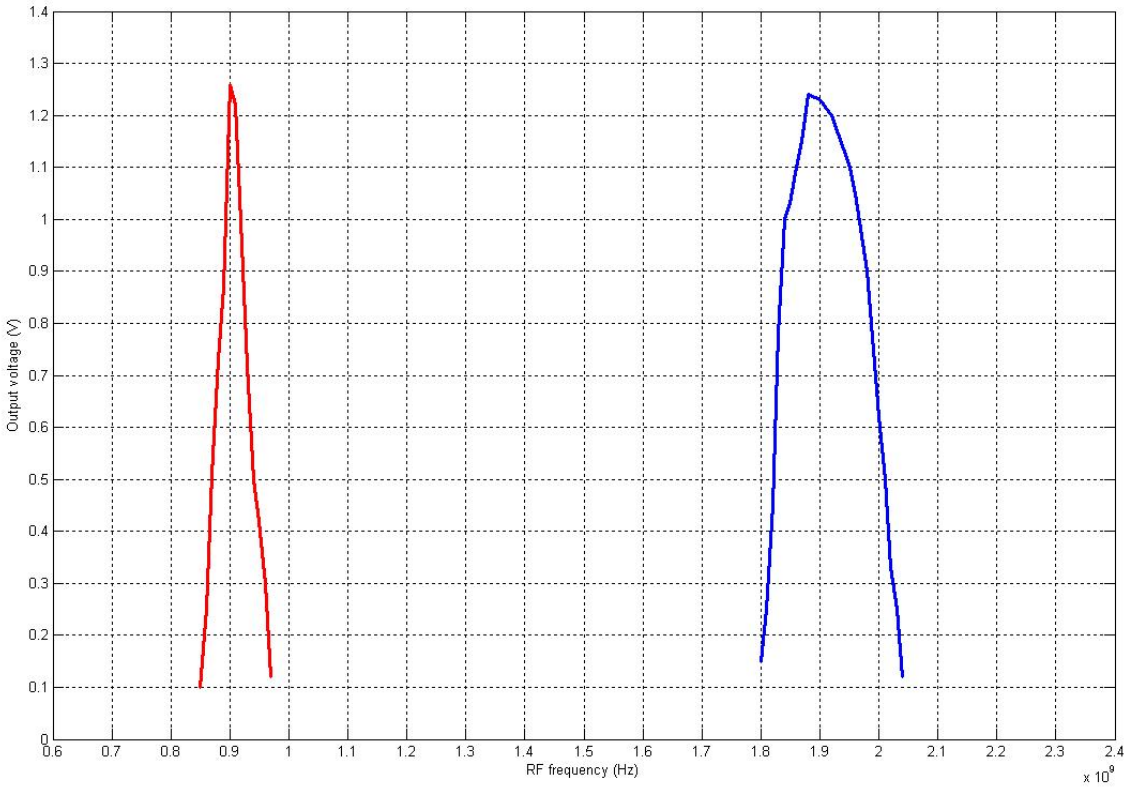

Figure 5.10: Measured output voltage at both bands for the harvester system (with antenna design A).

1.9 GHz, which is closer to the predicted simulation results.

The comparison of the performance of the two antenna designs used for the integrated system is presented in Fig. 5.11. It is observed that the different antenna structure for the higher band shifts the resonant frequency, and thus enables extracting ambient RF at the desired and available band.

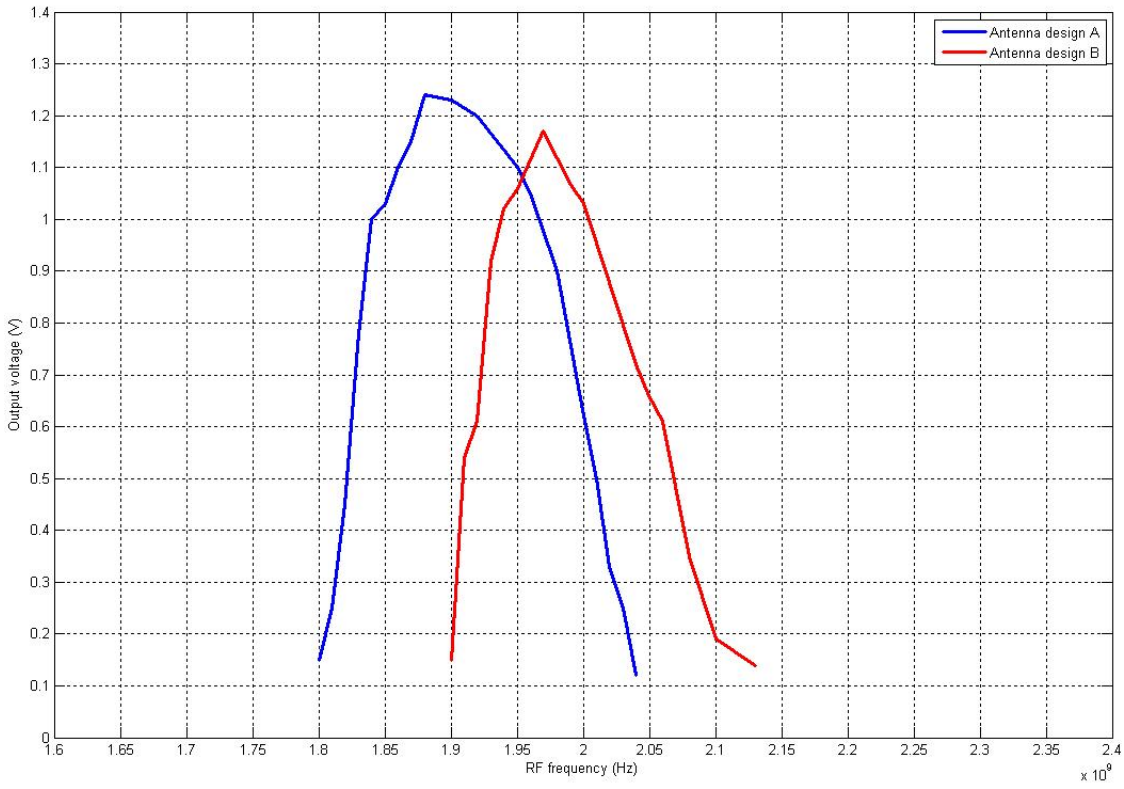

Figure 5.11: Measured output voltage at the higher band for the harvester system with two different antenna designs.

Chapter 6

Conclusion and Future Work

In this work, we have demonstrated the application of impedance matching and voltage boosting techniques in the design of an efficient RF energy harvester. In order for the harvester system to operate at low ambient RF power levels available, it is imperative to design the energy harvester such that it operates at the resonant frequency corresponding to the maximum input voltage boosting. The resonant boost circuit formed by the on-chip inductor and the rectifier circuit input impedance, provides the necessary input voltage amplification to overcome the threshold voltage and turn on the diode-connected transistors.

To minimize the power loss due to reflections between the antenna and harvester, design of a proper impedance matching network is critical. A single inductor is conventionally used to resonate out the input capacitance of the harvester, as well as to form an L-match network to transform the harvester resistance down to the antenna radiation resistance. Therefore, the inductor serves for both the purposes of voltage boosting and impedance matching. The parasitic capacitance and resistance that this inductor introduces to the harvester system, should be taken into account while implementing the design.

Moreover, it was observed that replacing the conventional matching with a π-match network adds an additional degree of freedom to the circuit design, and allows for achieving matching to 50 Ω at the operating resonant frequency. This is particularly important in RF design where the dominant characteristic impedance of transmission lines and microstrip lines is 50 Ω. Besides, designing a receiving antenna that provides a radiation resistance equal to 50 Ω is more straightforward.

In the design of the dual-band RF energy harvester discussed, two parallel circuits were used for the two frequency bands, each comprised of multiple stages of voltage doubler circuit and an on-chip spiral inductor. In the integrated antenna-harvester system, the improved dual-band monopole antenna provided impedances that are complex conjugates of the harvester impedance for each band. An off-chip resistive network was implemented to reduce the effective threshold voltage of the diode-connected transistors through DC self-biasing, and served to turn on the transistors more easily in conjunction with the already boosted input voltage.

In order to enhance the current design of the dual-band harvester, it is essential to investigate possible methods of implementation of on-chip MΩ active resistors. This enables us to design the entire off-chip resistor network used for DC self-biasing of the transistors on-chip, and thus significantly reduce the board area required for the antenna-harvester system.

On the other hand, the implementation of the dual-band harvester in the form

of parallel circuitry each designed for operation at a specific band, suggests the feasibility of the design of a multi-band energy harvester as an extension of the current design. The methodology for the receiving antenna design can also be extended to provide appropriate impedances at desired bands. Depending on the location, different frequency bands with abundant ambient RF power might be available, and thus the RF harvester can prove more reliable being capable to harvest RF power from multiple bands.

Furthermore, the output stage of the harvester is a resistive load optimized to yield the maximum RF to DC conversion efficiency. For practical applications it is needed to power up passive electronic circuitry or to charge up the battery used in a semi-passive system. Therefore, a design strategy should be implemented that allows for efficient storage of the harvested energy depending on the specific application.

Bibliography

[1] T. S. Salter, "Low Power Smartdust Receiver with Novel Applications and Improvements of an RF Power Harvesting Circuit," PhD Dissertation, University of Maryland, College Park, MD, 2009.

[2] T. Umeda, H. Yoshida, S. Sekine, Y. Fujita, T. Suziki, and S. Otaka, "A 950-MHz Rectifier Circuit for Sensor Network Tags With 10-m Distance," *IEEE Journal of Solid-State Circuits*, 2006, vol. 41, no. 1, pp. 35-41.

[3] H. Yan, J. G. Macias Montero, A. Akhnoukh, L. C. N. de Vreede, J. N. Burghartz, "An Integration Scheme for RF Power Harvesting," *Proc. STW Annual Workshop on Semiconductor Advances for Future Electronics and Sensors (SAFE 2005)*, Nov. 2005, pp. 64-66.

[4] T. Salter, K. Choi, M. Peckerar, G. Metze, N. Goldsman, "RF Energy Scavenging System Utilising Switched Capacitor DC-DC Converter," *Electronics Letters*, vol. 45, no. 7, March 2009.

[5] T. Le, K. Mayaram, and T. Fiez, "Efficient Far-Field Radio Frequency Energy Harvesting for Passively Powered Sensor Networks," *IEEE Journal of Solid-State Circuits*, 2008, vol. 43, no. 5, pp. 1287-1302.

[6] S. Mandal, and R. Sarpeshkar, "Low-Power CMOS Rectifier Design for RFID Applications," *IEEE Trans. Circuits and Systems*, vol. 54, no. 6, pp. 1177-1188, June 2007.

[7] A. S. Sedra, K. C. Smith, Microelectronic Circuits, Oxford University Press, Fifth edition, 2004.

[8] D. W. Harrist, "Wireless Battery Charging System Using Radio Frequency Energy Harvesting," Master's Thesis, University of Pittsburgh, Pittsburgh, PA 2001.

[9] G. De Vita, and G. Iannaccone, "Design Criteria for the RF Section of UHF and Microwave Passive RFID Transponders," *IEEE Transactions on Microwave Theory and Techniques*, vol. 53, no. 9, Sep. 2005, pp. 2978-2990.

[10] Y. Yao, Y. Shi, F. F. Dai, "A Novel Low-Power Input-Independent MOS AC/DC Charge Pump," *IEEE International Symposium on Circuits and Systems 2005 (ISCAS 2005)*, vol. 1, May 2005, pp. 380-383.

[11] J.P. Curty, N. Joehl, F. Krummenacher, C. Dehollain, M. J. Declercq, "A Model for μ-Power Rectifier Analysis and Design," *IEEE Transactions on Circuits and Systems*, vol. 52, no. 12, Dec. 2005, pp. 2771-2779.

[12] U. Karthaus, and M. Fischer, "Fully Integrated Passive UHF RFID Transponder IC with 16.7-μ W Minimum RF Input Power," *IEEE Journal of Solid-State Circuits*, vol. 38, no. 10, Oct. 2003, pp. 1602-1608.

[13] J. Yi, W.H. Ki, C.Y. Tsui, "Analysis and Design Strategy of UHF Micro-Power CMOS Rectifiers for Micro-sensor and RFID Applications," *IEEE Transactions on Circuits and Systems*, vol. 54, no. 1, Jan. 2007, pp. 153-166.

[14] B. Li, "Ultra Low Power FSK Receiver and RF Energy Harvester" PhD Dissertation, University of Maryland, College Park, MD, 2011.

[15] J. Joe, M. Y. Chia, "Voltage, Efficiency Calculation and Measurement of Low Power Rectenna Rectifying Circuit," *Proc. Antennas and Propagation Society International Symposium*, vol. 4, Atlanta, GA USA, June 1998, pp. 1854-1857.

[16] C. Sauer, M. Stanacevic, G. Cauwenberghs, N. Thakor, "Power Harvesting and Telemetry in CMOS for Implanted Devices," *IEEE Trans. Circuits Syst.*, vol. 52, pp. 2605-2613, Dec. 2005.

[17] R. Barnett, S. Lazar, J. Liu, "Design of Multistage Rectifiers with Low-Cost Impedance Matching for Passive RFID Tags," *IEEE Radio Frequency Integrated Circuits (RFIC) Symposium*, 2006.

[18] R. Jacob Baker, CMOS Circuit Design, Layout, and Simulation, IEEE Press, Wiley Interscience, Revised Second Edition, 2008.

[19] Y. Taur, T. H. Ning, Modern VLSI Devices, Cambridge University Press, Second edition, 2009.

[20] Thomas H. Lee, The Design of CMOS Radio-Frequency Integrated Circuits, Cambridge University Press, Second edition, 2004.

[21] C. P. Yue, S. S. Wong, "On-Chip Spiral Inductors with Patterned Ground Shields for Si-Based RF IC's," *IEEE Journal of Solid-State Circuits*, vol. 33, no. 5, May 1998, pp. 743-752.

[22] X. Shao, B. Li, N. Shahshahan, N. Goldsman, T. S. Salter, G. M. Metze, "A Planar Dual-Band Antenna Design for RF Energy Harvesting Applications," *International Semiconductor Device Research Symposium (ISDRS)*, Dec. 2011.