ABSTRACT

Title of Document:	ULTRA LOW POWER FSK RECEIVER AND RF ENERGY HARVESTER Bo Li, Doctor of Philosophy, 2012
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This thesis focuses on low power receiver design and energy harvesting techniques as methods for intelligently managing energy usage and energy sources. The goal is to build an inexhaustibly powered communication system that can be widely applied, such as through wireless sensor networks (WSNs). Low power circuit design and smart power management are techniques that are often used to extend the lifetime of such mobile devices. Both methods are utilized here to optimize power usage and sources.

RF energy is a promising ambient energy source that is widely available in urban areas and which we investigate in detail. A harvester circuit is modeled and analyzed in detail at low power input. Based on the circuit analysis, a design procedure is given for a narrowband energy harvester. The antenna and harvester co-design methodology improves RF to DC energy conversion efficiency. The strategy of co-design of the antenna and the harvester creates opportunities to optimize the system power

conversion efficiency. Previous surveys have found that ambient RF energy is spread broadly over the frequency domain; however, here it is demonstrated that it is theoretically impossible to harvest RF energy over a wide frequency band if the ambient RF energy source(s) are weak, owing to the voltage requirements. It is found that most of the ambient RF energy lies in a series of narrow bands.

Two different versions of harvesters have been designed, fabricated, and tested. The simulated and measured results demonstrate a dual-band energy harvester that obtains over 9% efficiency for two different bands (900MHz and 1800MHz) at an input power as low as -19dBm. The DC output voltage of this harvester is over 1V, which can be used to recharge the battery to form an inexhaustibly powered communication system.

A new phase locked loop based receiver architecture is developed to avoid the significant conversion losses associated with OOK architectures. This also helps to minimize power consumption. A new low power mixer circuit has also been designed, and a detailed analysis is provided. Based on the mixer, a low power phase locked loop (PLL) based receiver has been designed, fabricated and measured.

A power management circuit and a low power transceiver system have also been co-designed to provide a system on chip solution. The low power voltage regulator is designed to handle a variety of battery voltage, environmental temperature, and load conditions. The whole system can work with a battery and an application specific integrated circuit (ASIC) as a sensor node of a WSN network.

ULTRA LOW POWER FSK RECEIVER AND RF ENERGY HARVESTER

By

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To my parents for their encouragement, love, and support

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Chapter 1: Introduction

1.1 Motivation

1.1.1 Challenges of Energy Needs for Wireless Devices

Wireless technologies greatly shape communication and continue to play ever more important roles in modern society. There are different wireless services that have been rolled out to meet different market requirements. For example, the Global System for Mobile communication (GSM) provides voice services, the Global Positioning System (GPS) provides location information, and Bluetooth provides data transfers over small distances. For all the above services, mobile devices exist that use regular batteries which can be recharged once every few days.

Wireless transceivers are often implemented in mobile devices to access those wireless services. They serve as bridges between the physical and the digital world. Almost all transceivers in mobile devices use batteries as their power sources. In many potential applications, the fact that the batteries must be recharged every few days using currently applied commercial designs is a serious limitation.

Recently, there has been increased market demand for wireless services such as wireless sensor networks (WSNs) and Smart Dust Systems (SDSs). These systems are typically very low cost wireless ad hoc networks distributed over a relatively small area. These devices sense, transmit, and receive signals. The current infrastructure supports low power protocols such as TDMA [Shen2008]. Figure 1.1.1 shows a SDS node which includes an antenna, transceiver, microprocessor, and ADC. SDSs are characterized by a

low data rate (10 bits/day to 100 Kbits/s), long duration operation (years), and small sizes ($1cm^3$) [Cook2006]. These systems are ideal for applications requiring long duration in particular, and some examples are health monitoring, environmental sensing, fire alarms, security, military intelligence and operations, etc. [Salter2009]

For these applications, the mobile devices are required to be left unattendant for several years without the batteries being recharged [Priyantha2002]. Generally, these applications also have volume limitations as well. For example, each node of a SDS system can be required to be housed in less than $1cm^3$. Thus, there exist power application gaps between the transceiver operational power that is desired and the limited battery storage power that can be contained within the required volume. Furthermore, a low cost for each node is commonly required as well.

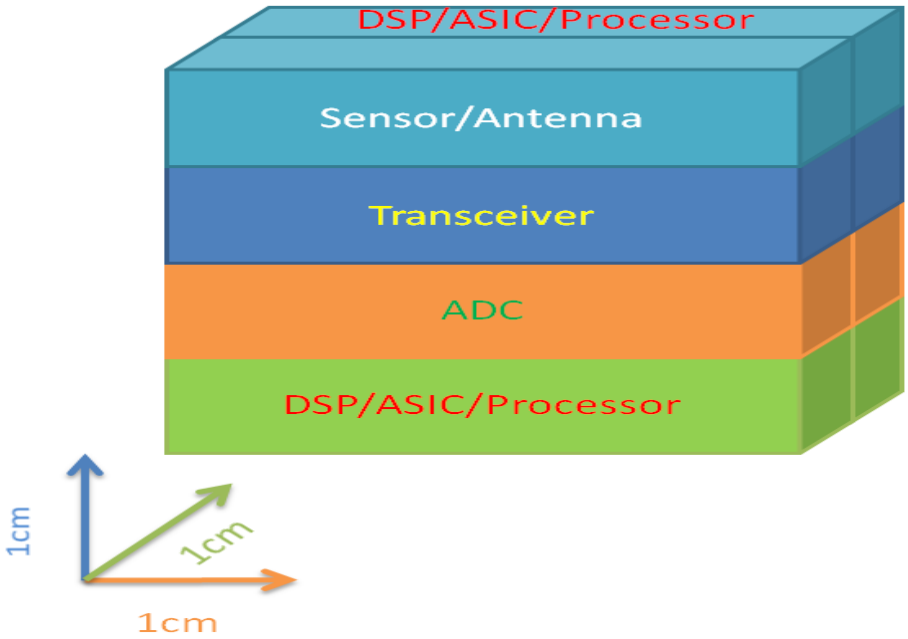


Figure 1.1.1 Sensor node of a Smart Dust System (SDS).

Two methods have generally been used to address the power gap: alternative power solutions and extremely low power transceiver design. Alternative power sources other than batteries will be discussed briefly below.

Various environment energy sources such as solar, vibrational, and electromagnetic waves (RF energy), etc. exist ambiently. The average power can be as high as mW for solar power and tens or hundreds of uW for vibrational and RF power.

On the other hand, as devices continue to be scaled down to smaller and smaller sizes as Moore's law predicts, the required digital energy to switch digital inverters keeps decreasing as well. For example, the switching power of a minimal size inverter in 65nm CMOS technology is as low as 0.08fW. The required power of a transceiver keeps decreasing as well. Table 1 shows the power consumption of available commercial products [Penella2009]. The required power in the sleep mode has been reduced from 3 uW to 0.06 uW. The low power Zigbee transceiver CC2420 [Penella2009] only consumes 0.06uW in sleep mode.

Table 1: Power consumption of low power transceivers [Penella2009].

Commercial transceivers	V_{CC} (V)	P_{active} [a] (mW)	P_{sleep} [a] (µW)
CrossBow, MicaZ OEM	2.1 – 3.6	55	3
Ember, EM 250/260	2.1 – 3.6	108	< 3
FreeScale, MC1320X	2.0 – 3.4	100	< 3
Jennic, JN513X	2.2 – 3.6	102	0.6
Atmel, AT86RF230	1.8 – 3.6	48	0.3
TI, CC2420	2.1 – 3.6	54	0.06

a. Calculated for Vcc = 3 V.

It is very attractive to attempt to harvest some form of environmental energy to help meet these needs. Alternative power sources may be able to help meet the power lifetime requirements for WSN applications.

The sleep mode is not the only consideration, of course. Note, that the data in Table 1 indicates that the *active* power consumption of commercial low transceivers are on the level of tens of milliwatts, which is still tens of times of the largest available environment energy sources. (for what distance) Low power transceivers in a range of 10 meters represent another important and promising solution to meet the power requirements for WSN applications overall. The required energy of nodes of a WSN on each day can be defined as follows:

$$E = [P_{active} \times \eta + (1-\eta) \times P_{sleep}] \times 86400 \quad 1.1$$

Where E, P_{active}, P_{sleep}, and η are the required energy for each day, the required device power in active mode and sleep mode, and percentage of the time that the device spends in active mode, times the number of seconds in a day which is 86400, respectively. The power available from the environment on each day is described by Equation 1.2:

$$E_{avail} = 86400 \times \beta \times P_{env} \quad 1.2$$

where E_{avail}, β, and P_{env} are the harvesting energy for each day, the harvesting efficiency, and the average power density in the environment.

The mobile device can function inexhaustibly if Equation 1.3 holds:

$$\begin{aligned} &E_{avail} \geq E \\ &P_{harvester} = \beta \times P_{env} \geq P_{active} \times \eta + (1-\eta) \times P_{sleep} \end{aligned} \quad 1.3$$

If $P_{sleep} < P_{harvester}$, Equation 1.3 can always be satisfied by adjusting the percentage of sleep time per day . For a 10 uW environment energy source with 10% power conversion efficiency, and taking $P_{sleep} = 0.06$ μW as shown in Table 1, and $P_{active} = 1$mW, then the percentage of active time will need to be chosen to satisfy Equation 1.4:

$$1 - \eta \leq 9.4 \times 10^{-4} \quad 1.4$$

The above discussion concludes that mobile devices can work inexhaustibly if they are only awake 0.1% of the time (86.4 second per day). Such a percentage is sufficient for low-data applications such as environmental monitoring, monitoring of bridges and other structures, etc. The percentage of up-time can be increased by a low power transceiver design which consumes even less power than 1mW.

1.1.2 Strategy

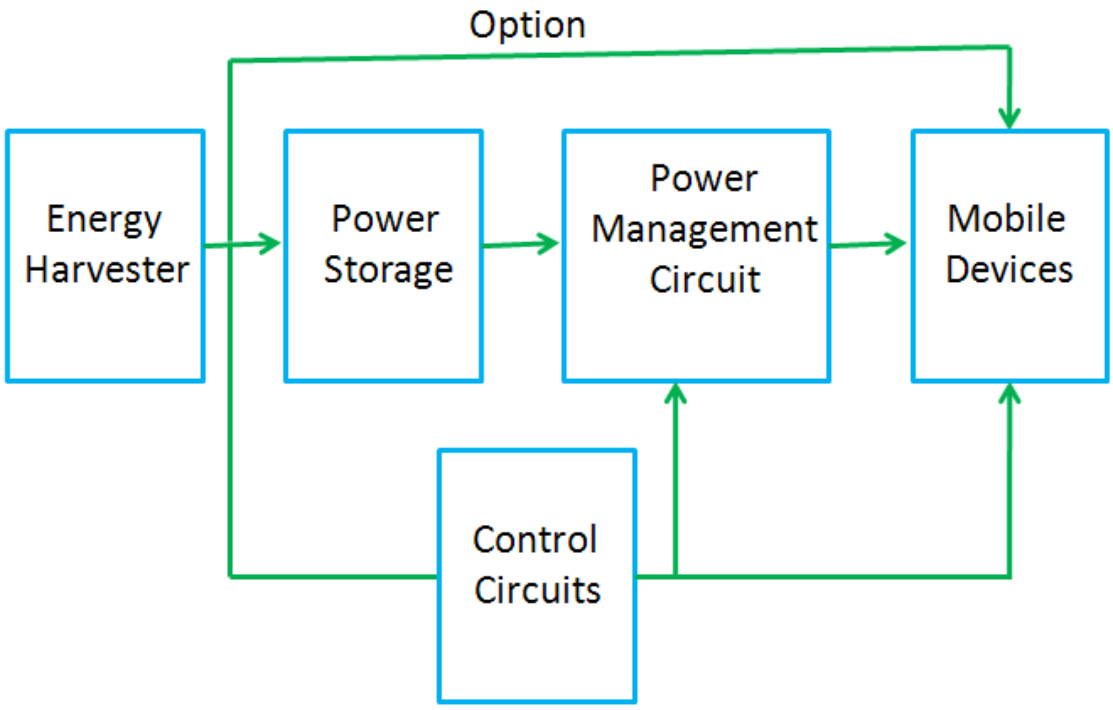


Figure 1.1.2 Scheme for power solutions suitable for nodes of WSNs.

Figure 1.1.2 shows a scheme for future designs of WSN nodes. In this scheme, each node uses harvested energy as a virtual battery. When the devices work in sleep mode, the harvested power is stored and can be used when the devices work in active mode. Furthermore, the low power transceiver needs to be able to maintain low power

consumption in both the active and sleep modes. Most importantly, in sleep mode, the power consumption is required to be less than the harvested power. In this thesis, we follow the above scheme to meet the power requirements for WSN applications.

The strategies used in the thesis can essentially be divided into two different paths based on the scheme. In the first half of the thesis, RF energy harvesting for dual-/multi-band applications has been investigated. In the second half of the thesis, a PLL based ultra-low power receiver has been designed and fabricated which consumes hundred of micro-watts. Finally, a CMOS based transceiver system with on-chip voltage regulators is also provided in the thesis to demonstrate a system on-chip solution.

1.2 Review of Energy Harvesting Technology

1.2.1 Overview

Large scale energy harvesting such as via windmills, watermills, etc. contributes a significant amount of power for commercial consumption in different countries. These methods have been in place for a long period of time. More recently, there is a trend to harvest environmental energy in a limited volume to enable long term mobile applications such as WSNs. Unlike battery power, the harvested energy can be replenished from the environment all the time. The use of ambient power harvesting strategies is emerging as a promising solution for long term wireless applications such as WSNs.

There are different kinds of ambient energy existing in the environment. Solar, vibrational, thermal, and radio frequency electromagnetic wave energy are some of the ambient power sources that can be utilized [Paradiso2005]. Solar energy has the highest power density in sunny weather, but also displays large variability. Its power density varies from 100uW/cm^3 to 100mW/cm^3 [Paradiso2005] depending on the weather conditions, incident angles, etc. Photovoltaic devices can convert solar energy into electrical energy with roughly 25% efficiency [Green1986]. [Atwood2001], [Warneke2001], and [Warneke2002] studied the use of solar energy as a power source for WSN nodes, and [Bertacchini2008] has analyzed solar harvester circuit performance. Other recent publications have reported using harvested solar energy to form battery-less nodes for WSN applications, such as [Guilar2006], [Brunelli2009], [Wang2010], and [Chini2010]. While promising, solar energy is not always available.

Vibrational sources have energy densities of ~100 uW/cm^3 [Paradiso2005]. [Callaway2004] reports research on harvesting vibrational energy from human activity. A vibrational energy harvesting system has been developed by S Roundy and P. K. Wright [Roundy2004]. The cantilever is fabricated using piezoelectric materials. Piezoelectric materials can convert mechanical energy into electrical energy, or vice versa. However, the vibrational power source is very limited in the environment and often is not suitable for WSN applications.

Thermoelectric devices can harvest energy from objects at different temperatures. The conversion efficiency is limited by the Carnot efficiency [Feynman1971]:

$$\eta = \frac{T_H - T_L}{T_H} \qquad 1.5$$

Where η, T_H, and T_L are the maximum efficiency, the high and low temperature, respectively, whose difference represents the differential in temperature between device and environment. [Lawrence2002] proposes a method to convert thermal energy into electrical energy, while [Sodana2004, Sodano2009] reports work to convert thermoelectric energy into electrical energy. However, thermal energy is not widely available or practical for WSN applications.

While the above sources have generally been often thought of for energy applications, RF energy can have many applications as for low power electronics as suggested above as well. Moreover, there is tremendous radio frequency energy in urban areas which can be harvested.

One successful use of harvested RF energy as a power sources has been an implementation designed for passive RFID devices [Namjun2005][Weinstein2005]**.** RFID tags are placed close to RFID readers which transmit RF energy at designed frequency such as 13.56 MHz for near field communication (NFC) applications. There have been medical applications to monitor long term biomedical signals which have used RFID techniques [Qiuting1997][Qiuting1998][Otis2009].

There has also been research on battery-free systems using RF energy [Sample2007][Sample2008]. The literature **[**Joe1998] has provided a lump model for rectifying diodes. More recently, there have been publications on using RF energy as a virtual battery [Avago] [Hama2002]. Other work also explores the possibility to harvest RF power as a virtual battery [Theeuwes2007]; however, their input power is 0dBm which is much higher than the available ambient RF energy. The literature [Seeman2008] reports a power management circuit for harvested energy. Other work investigates the

interface between a low power harvester and a micro-battery to maximize harvesting power [Paing2009]'s. There have also been studies about the possibility to use RF energy to charge a cell phone battery [Harris2004]. Another recent document reports DC to DC conversion in low power applications with efficiency as high as 70%, which might be usable for providing biasing voltages with high efficiency [Ramadass2007]. Some research work also discussed a method to charge a cell phone battery at high RF frequency to minimize charger size [Sabate2000].

Recent work has studied the feasibility of extracting energy from TV or radio station signals, and their work harvested RF energy at 1.584MHz [Sogorb2008]. The energy density of RF power was reported to be ~0.5 μW/cm^2 a kilometer away from a TV tower [Burch2006]. Other reports RF energy density from 0.1 μW to 9.5 μW for different sources such as a TV tower, radar, etc [Khalaf]. Other work reports a similar amount of environment RF power [Fields]. The antenna effective area is given by [Balanis2005]:

$$A_{eff} = \frac{1}{8}\lambda^2 = \frac{1}{8}(\frac{c}{\nu})^2 \qquad 1.6$$

Assuming the frequency of the RF source is 900MHz, the available power is given by:

$$P = P_{den} A_{eff} = \frac{1}{8}(\frac{c}{\nu})^2 P_{den} \qquad 1.7$$

Where P is the available power and P_{den} is the power density of the RF power source, which was 0.5 uW/cm^2 at a distance of 1 kilometer from a TV tower [Burch2006]. The total available power is 69.4 μW (-11.58 dB).

A previous energy survey [Salter2009] shows a range of -30 to -20 dBm of power on average in the Baltimore/DC area. These sources are widely available in urban/suburban

areas and thus represent promising power sources for energy harvesting. Cascade voltage doublers (voltage multipliers) have been used to convert RF energy into DC energy. Previous research [Salter2009][Yao2005][Tan2005] has focused on boosting the input voltage for a narrowband frequency to improve the efficiency. In [Texas2010], Texas Instruments also reported that GSM has a RF energy density of $0.1\mu W/cm^2$ which corresponds to a RF signal of -30dBm.

RF energy harvesting should be relative natural to integrate with CMOS technology. For example, piezoelectric and thermoelectric components need different processes and rectifier circuits to power the electrical circuits. Moreover, RF power sources have strong and accurate frequency pattern; the output voltage from a RF energy harvester can be very stable as long as the amount of the available power is stable [RFpower].

1.3 Review of Low cost, Low Power Receiver Design Methods

In addition to energy harvesting, this thesis also explores very low power transceiver designs, especially for WSN and SDS application. Wireless transceivers serve as bridges between the physical and the digital world to access different services and information. Generally, receivers [Tadjpour2001, Shaeffer1998, Samavati2001, Darabi2001, Steyaert2000, Su2002] demodulate the high frequency input signals and extract low frequency digital signals. The demodulated digital signal is further manipulated via digital signal processing and/or an application specific integrated circuit (ASIC) to extract various forms of video or audio information. Transmitters mix the digital information with a high frequency carrier signal at different frequency channels and

radiate the modulated information through an antenna into the air [Darabi2001, Steyaert2000, Su2002, Hegazi2002].

Historically, Gallium Arsenide (GaAs) devices have been widely implemented in RF front-ends due to their high mobility, high break-down voltage, and reliability. However, these devices cannot integrate with the baseband CMOS digital circuits to provide a system on chip solution and are thus relatively costly [Abidi2004].

As CMOS processes are scaled down, CMOS devices have less and less parasitic capacitances and thus are able to operate and obtain current gain at frequencies as high as 100GHz. Considerable research has been conducted to investigate and improve CMOS circuit performance via innovations such as low noise CMOS LNAs, low phase noise LC CMOS oscillators, etc. Due to those efforts, CMOS based RF front-end transceivers have emerged to dominate the commercial marketplace due to their low cost and excellent integration capabilities with digital systems [Abidi2004]. Currently, CMOS based RF solutions can meet the application requirements for most of RF front ends. A CMOS based PA is still under investigation and remains a topic of major interest in RF design. In this thesis, we mainly focus on CMOS based receiver designs.

Wireless application requirements such as data rate, operation distance, sensitivity, power consumption, and cost determine receiver system architectures. Based on the data rate and power requirements, receiver architectures can be roughly divided into low data rate/high sensitivity applications such as GPS which operate globally, low power/low data rate applications such as WSNs, high data rate/moderate sensitivity applications such as WLANs, Ultra Wideband (UWB) transceivers which provide high data rate service in a small area, and extremely spectrum efficient applications such as GSM transceivers

which provide voice services over large areas. A brief overview of the typically selected architectures for each application is detailed below.

GPS receivers require low data rates (50Hz symbol rate) with extremely high sensitivities (-130 dBm) [Shaeffer1998] [Abidi2004]. Super-heterodyne receiver architectures are widely used in GPS applications.

GSM receivers require spectrum efficiency in order to provide services over large areas and provide service access to everyone. They operate within crowded spectrum traffic and thus need excellent anti-interference capabilities to handle blocks. Super-heterodyne, Weaver, and direct conversion architectures are generally implemented to suppress/reduce the image interferences as well as high power blocks at adjacent frequency channels [Vassiliou2003][Lee2003].

WLAN and UWB receivers generally require high data rates to enable applications with large data transfers between two local devices or streaming video. They generally have high data rates with relative low sensitivity requirements because of the short distances between devices. Those services also operate within industrial, scientific, and medical (ISM) frequency bands. WLAN devices operate at 2.4-2.48GHz or 5.725-5.825GHz [Samavati2001]. UWB technology employs a wide frequency spectrum between 3.1-10.6 GHz under FCC regulation [Razavi2005].

Commercial receiver architectures are designed specifically with high anti-interference capabilities in order to accommodate more customizations. Direct conversion, and Weaver architectures can greatly suppress interference at image frequencies. The power consumption of these architectures is normally a few tens or even hundreds of mW

[Tadjpour2001, Shaeffer1998, Samavati2001, Darabi2001, Steyaert2000, Su2002, Hegazi2002]; thus these designs are not suitable for ultra low power applications.

Super regenerative architectures obtain extremely high voltage gain using positive feedback [Shi2008]. They normally have high gain, low data rates, and low/moderate power consumption [Moncunill-Geniz2005][Chen2007][Shi2008]. This architecture is widely used in non-critical applications such as toys [Shi2008]. Off-chip high quality inductors are commonly used in super-regenerative receivers to improve the system selectivity capability and to obtain lower power consumption. Previous research [Shi2008] reports a super-regenerative receiver using an on-chip inductor with 6.6mW@5GHz and a data rate between 200Kbits/s to 1.2Mbits/s.

On/off key (OOK) architectures are widely implemented for low power applications [Daly2007] due to the simplicity of their receiver designs. OOK architecture only requires a low noise amplifier (LNA) to amplify the signal to a detectable level for the demodulator, such as by a peak detector. OOK demodulators such as peak detectors suffer from large voltage conversion losses (>30 dB) especially under weak signal conditions. They thus require large power amplification at high frequencies. However, high frequency amplification uses considerable power (milliwatt levels). Recently there has been research [Salter2009] on using energy harvesting techniques to lower the OOK demodulation conversion loss, even though the results still show a 30dB loss [Salter2009].

1.3.1 Receiver Architecture Background

Depending on the application, the receivers' sensitivities may vary in a wide range from -130 dBm for GPS applications [2] to -70 dBm for some wireless local area network

(WLNA) applications [Samavati2001]. White thermal noise places a physical limitation on the system sensitivities. The thermal noise power per Hz is k_BT, where k_B is Boltzmann's constant and T is the temperature in Kelvin. The physical limit of receiver sensitivity is described by equation 2.1:

$$P_{in} = -174\text{dBm/Hz} + NF + 10\log B + SNR_{min} \quad 2.1$$

Where -174dBm/Hz is the thermal noise per Hz in decibels. NF is the system noise figure, mainly determined by the first stage of the receiver; the system noise figure can be mathematically described by Friis formulas for noise [Lee2003]. The noise factor is defined as the ratio of the total output noise power to the output noise power due to the input source, and noise figure units are in decibels [Lee2003]. B is the channel bandwidth, and the SNR_{min} is the required signal to noise ratio for a particular bit error rate. B is closely linked with the data rate.

There are different receiver architectures used to meet different application requirements, such as spectrum efficiency, power consumption, block interference, etc. For example, super heterodyne architectures are widely used in global positioning system (GPS) applications due to high interference (block) rejection capabilities. The details of the super heterodyne, direct conversion, and Weaver architectures can be found in [Lee2003].

1.3.2 Low Data Rate, Weak Interference-Rejection, Ultra Low Power Applications

1.3.2.1 ASK Receiver

Figure 1.3.1 shows the block diagram of an amplitude shift key (ASK) receiver. ASK receivers represent the simplest receiver architecture and require minimal circuit blocks. The RF signal is first amplified by LNAs and then demodulated by demodulation circuits such as peak detectors. However, the peak detector has significant conversion loss. A high power gain LNA is thus necessary for high sensitivity applications that have large power consumption.

Recent research [Salter2009] has used energy harvesting voltage doubler techniques to lower the conversion loss; however, a -30dB conversion loss is still reported. Additionally, ASK receivers are spectrum inefficient and have no anti-interference capabilities.

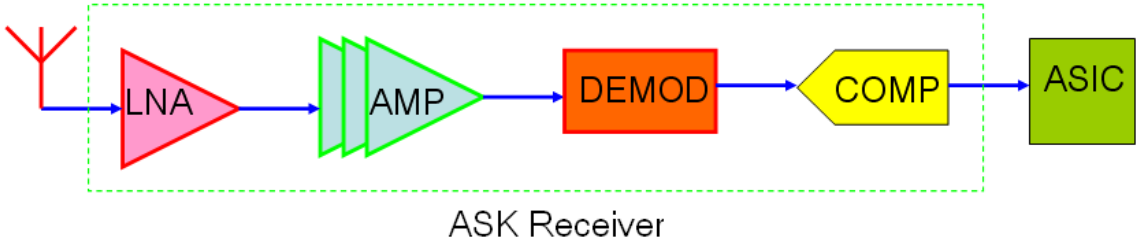


Figure 1.3.1 Block diagram of the ASK receiver.

1.3.2.2 Wake-up Receiver

Figure 1.3.2 shows a block diagram of a wake-up receiver [Pletcher2009]. The wake-up receiver does not require a LNA with large power consumption. A mixer is used to convert the high frequency signal into an intermediate frequency (IF). The amplification is performed at the IF frequency to save power. The system sensitivity is generally low due to the lack of amplification and the mixer's high noise figure. A ring oscillator is used due to its low power consumption. However, this receiver structure has no anti-

interference capabilities either. A 100 MHz IF is chosen to overcome the uncertainty of the ring oscillator frequency and its inferior phase noise. A surface acoustic wave (SAW) resonator is used to boost the input voltage and help with interference problems. Reported results show a power consumption of 52 uW with sensitivity of -72 dBm [Pletcher2009].

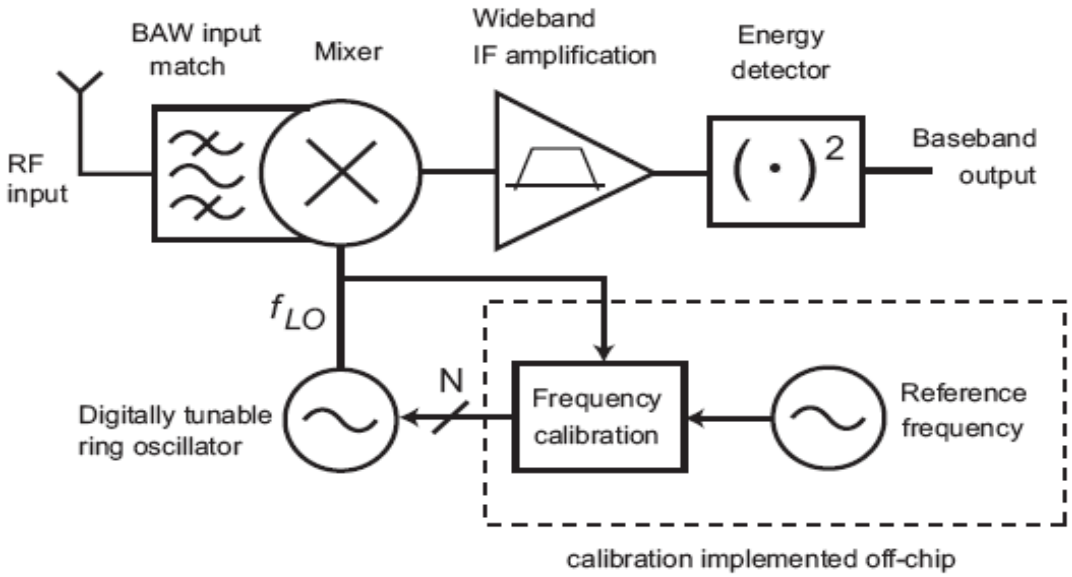


Figure 1.3.2 Wake up receiver block diagram [Pletcher2009].

1.3.2.3 Low Data Rate, Moderate Interference-Rejection, Low Power Application—Super Regenerative Receiver

Figure 1.3.3 shows the circuit diagram of a super regenerative receiver [Moncunill-Geniz2005]. In the super regenerative stage, the quench bias signal generates a negative resistor to compensate the intrinsic resistor of inductor to start oscillation. During other times, the signal is quenched. The envelope detector rectifies the oscillator output and filters out the high frequency signal. G_m-C (transconductor-capacitor) filters are used to

filter out the quench signal and get the demodulation signals. The data rate is less than the quench signal frequency, which is normally less than 500 KHz. The quench signal is a sinusoidal or sawtooth waveform. The data rate of these kinds of receivers is generally low [Moncunill-Geniz2005] and might be suitable for low date rate applications.

Oscillator power consumption is determined by the inductor quality factor. Off-chip inductors (Bulk Acoustic Wave (BAW) devices) have high quality factors that offer low power consumption [Moncunill-Geniz2005]. However, off-chip inductors are costly and also add significant package costs. On-chip inductors offer high integration and low cost but consuming considerable power [Chen2007].

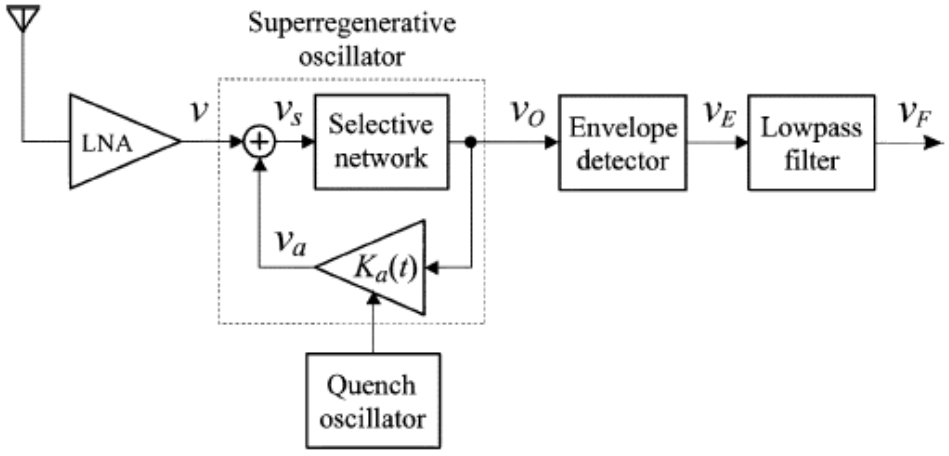


Figure 1.3.3 Super-regenerative receiver architecture [Moncunill-Geniz2005].

1.3.3 This work: PLL Based FSK Architecture

We have surveyed various receiver architectures and summarized their features. Table 2 lists the different architectures detailed above along with their pros and cons for various applications [Shi2008]. A major thrust of this thesis is to introduce a new PLL based

receiver architecture for low power applications such as wireless sensor networks as as a very competitive option when low power is required.

Table 2 Comparison of different receiver architectures.

	Pros	Cons	Applications
OOK architecture	Easy to implement Low power	Poor anti-interference capability Poor selective	Non-critical communication Low power WSN network
PLL architecture	Low power	Poor anti-interference capability Poor selectivity	Non-critical communication Low power WSN network
Super regenerative	Low power	Moderate selectivity Moderate anti-interference capability	Short distance, low data rate links Walkie-talkie Radar application
Direct conversion	No image effect High level integration Low cost	DC offset Transmitter noise interference Flick noise Even order distortion I/Q mismatch	WLANs Cell phone communication Multi-band cell phone communication
Super heterodyne	Superior to interference High power consumption	Low integration due to SAW filter High Cost Limited multiband capability due to SAW filter High power consumption	GPS Cell phone WLAN
Wake-up Architecture	Low Power	Poor anti-interference capability Poor selectivity	Non-critical communication Low power WSN network

Phase locked loops are widely used in communication circuits as frequency synthesizers. In this work, we investigate their application as natural demodulators for low power receivers. Figure 1.3.4 shows the PLL based receiver architecture. A LNA amplifies the small input signal, and the PLL picks up this signal and compares it with

the local oscillator. This PLL has been integrated with a LNA to work as a RF receiver. The receiver can demodulate both FM and FSK signals. Detailed analysis of this receiver is provided in Chapter 2.

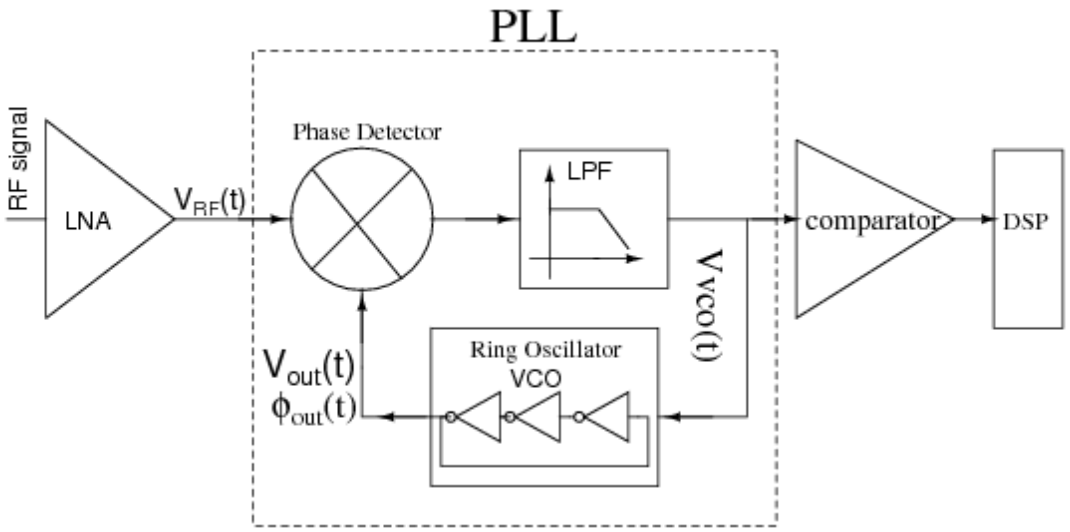


Figure 1.3.4 Block diagram of PLL and its application as an FSK receiver when used with a LNA, comparator, and a DSP.

In order to provide an accompanying system on chip solution, we have designed an integrated transceiver system with on-chip power management circuits to handle the battery voltage variation as a part of this work. A voltage regulator is used to integrate with the transceiver to handle the battery voltage variation due to temperature and load. We have also designed a low power OOK transceiver with on-chip integrated power management circuits. The designed integrated transceiver can work as a node in a WSN. This work is reported in Chapter 3.

1.4 Summary of Contributions

Our contributions are summarized as follows:

- Multi-band RF Energy Harvesting
    - Analysis of voltage doublers.
    - Study of the characteristics of ambient RF power.
    - Study of battery recharging requirements.
    - Provided design specification for energy harvesting in WSN applications.
    - Discussion of theoretical difficulty of wideband energy harvesting.
    - Creation of a multi-band energy harvesting scheme that uses energy harvesters connected in parallel for dual-/multi-band energy harvesting.
    - Use of on-chip inductors to boost voltage for the 890MHz and 1800MHz bands.
    - Use of an improved voltage doubler structure to maximize the conversion efficiency.
    - Use of the matching impedance of the antenna and the harvester circuits as a system parameter to optimize the conversion efficiency.
    - The harvester achieves 14% conversion efficiency at 890MHz and 13.4% conversion efficiency at 1800MHz. The output voltage is over 1V at both frequencies.

- The design harvester can function as two separate power sources when there is RF energy at both frequencies.
- A planar dual-band monopole has been designed, fabricated, and measured. It has an impedance of 50 Ohms at 890 MHz and 14 Ohms at 1800 MHz, respectively. The antenna structure (e.g., the arm lengths and spacing) can be tuned to adapt to other frequency bands and different impedances.

- Dual-band RF Energy Harvesting
  - Dual-band energy harvester for 1800MHz and 2400MHz frequency bands.
  - Antenna coupled voltage boosting technique.
  - On-chip inductor voltage boosting technique.
  - Loop antenna achieves inductive-like behavior at 1800MHz and impedance-like behavior at 2400MHz to match energy harvester.
  - The simulated efficiency of the harvester is 14.4% at 1800MHz and 12% at 2400MHz.

- Ultra-low power receiver design, fabrication and testing
  - Design and analysis of an ultra-low power mixer.
  - Analysis of the power limitations of the LC oscillator topology and implement current starving ring oscillator as a VCO.
  - A FM/FSK receiver using PLL as a demodulator.
  - The power consumption of the PLL can be scaled down as the CMOS technology scales down.

- Integrated transceiver system
    - Pure low power CMOS voltage regulator.
    - Integrated low power OOK transceiver system design.
    - Integrated low power OOK transceiver with voltage regulator co-design

1.5 Thesis Organization

The chapters of the thesis are organized as follows:

In Chapter 2, we introduce a new low power mixer architecture. Detailed analysis and design procedures are given as well. We also discuss the LC oscillator power limitations and show that the low quality inductor requires milliwatts of power to enable oscillations. One conclusion is that ring oscillator topology is more suitable for uW power applications. We then discuss the design considerations for a low power phase locked loop and its application as a receiver.

In Chapter 3, we design a highly integrated pure CMOS based transceiver with an on-chip voltage regulator. This design can work with a battery to provide a system solution for low power mobile applications. The transceiver system is designed and fabricated in a 2x2 chip die using a pure CMOS process.

In Chapter 4, we model and analyze the voltage doubler circuits. The difficulty of the wideband energy harvesting method under low input power is an aspect of importance. A theoretical analysis of the dual-/multi-band energy harvester is developed.

In Chapter 5, we design dual-/multi-band energy harvesters to fully take advantage of the existing multi-band ambient RF energy. The dual-/multi-band energy harvester is co-designed with dual-/multi-band antennas to maximize the harvested energy.

In Chapter 6, we discuss possible future extensions of this work on low power receiver architecture, such as a super-regenerative receiver and a method for low power energy harvesting such as by using a tunable energy harvester.

Chapter 2: Low Power Receiver

In this chapter, we present a new low power phase-locked loop (PLL) based frequency shift key (FSK) receiver. We first present a down-conversion mixer design with single RF and LO input topology that consumes 48µW power. Detailed analysis of the mixer has been provided. We then discuss the power limitations of two major oscillator topologies: LC oscillators and ring oscillators. Our analysis concludes that a LC oscillator structure using on-chip inductors cannot meet wireless sensor network (WSN) power requirements, and thus is not suitable for WSN applications because of its lossy on-chip inductors. A current starving ring oscillator topology is implemented in this work to meet the power specification of WSN systems. Using the presented mixer as a phase-detector and the current starving ring oscillator as voltage controlled oscillator, a low power PLL has been designed and fabricated. The PLL based receiver architecture has been developed and analyzed for FM/FSK receiver applications. The designed circuits have been fabricated through a 0.13µm eight metal layer CMOS process. Dissipating 0.26mW from a 1.2V supply, the fabricated PLL can track radio signals in a wide frequency range from 1.62GHz to 2.49GHz. The combination of the PLL and a low noise amplifier (LNA) can work as a FSK receiver. The energy per bit of the receiver is as low as 0.26nJ, making it attractive for low power applications including WSNs.

2.1 Overview of the Low Power Receiver Architecture

High speed, low power phase locked loops (PLL) are extensively used in frequency synthesis, clock generation, and recovery circuits for microprocessors and wireless communication systems. A PLL can also be used as a natural FM/FSK demodulator for wireless communication receiver applications. Wireless communication ICs are extensively used in mobile cellular devices, portable electronics, and positioning systems. For most of these applications, limited battery power necessitates low power designs. This chapter discusses circuit techniques as well as low power circuit design methodologies to build a high speed, low power PLL, with specific application for ultra low power FSK and FM receivers such as those used in ad-hoc distributed wireless sensor networks (WSN). For such applications, receivers are typically required to be left unattended for extended periods of time (perhaps several months or even years), and thus require maximum power efficiency. In addition, these receivers need to detect extremely low power signals. To help meet these low power requirements, instead of using a digital phase detector [Tak2005, Hu2009, Krishnaswamy2008], we have designed an extremely low power PLL using an analog phase detector for signal demodulation.

Generally, Gilbert cell based mixers are widely used as analog phase detectors in PLLs [NG2006]. However Gilbert cell based mixers (phase detectors) [NG2006, Sullivan1997, Jeng-Han2007] often consume prohibitive amounts of power for WSN applications because of current sources and related stacked structures. The Gilbert cell also uses differential inputs that usually require additional accessory circuitry for low noise amplifiers (LNAs) and voltage controlled oscillators (VCOs). A differential topology of a VCO [Ng06], LNA, or balun [Chiou1997] is often used to meet the differential input

requirements of the Gilbert cell. However, a differential input structure can be vulnerable to phase errors due to device mismatch, and a balun usually occupies a large area on the chip. [Hermann2005] use on-chip transformer to achieve high current gain for a down convert mixer with power consumption of 1.6mW. Other previous reported mixes consume milli-watts or even tens of milli-watts power as well [Tan2003][Hung2006][Vidojkovic2005]. [Klimperink2004] reports a mix with 0.57 milli-watts power consumption. However, part of their power consumption is due to the low supply voltage (0.5V).

In this chapter, a single RF and LO input mixer, which we use as a phase detector for the PLL, is presented and implemented. The phase detector achieves ultra low power consumption and high linearity. The presented phase detector consumes low power due to its single end topology and current re-use. This phase detector also takes advantages of the parasitic capacitors of the MOSFET to filter out high harmonic signals and thus achieve high linearity. Furthermore, constituent PLL circuit components can be simplified as a result of this phase-detector topology.

An oscillator is another essential circuit component in a PLL. LC oscillators and ring oscillators are widely explored for different applications. Both LC oscillators [NG2006] and ring oscillators [Ingino2001] have previously been implemented in PLL applications. LC oscillators are generally used in favor of ring oscillators due to their superior phase noise properties [Hajimiri1999A] [Hajimiri1999B], while consuming milliwatts of power in on-chip topologies [Hajimiri1999A] [Lee2005, Andreani2002]. However, for ultra-low power applications (on the order of 100μW), we find the losses due to on-chip inductors limit the applicability of on-chip LC oscillators.

In this work, we explore the LC oscillator power limitation in detail. An extraction procedure for the values of lump components for on-chip inductors is given in Appendix 2B. Following the same procedure, we extract the lump component values of the on-chip inductor. Our analysis shows that the losses of the on-chip inductor cause the LC oscillator to consume an inordinate amount of power. This disadvantage thus excludes the use of the on-chip LC oscillator in ultra-low receiver applications. Ring oscillators do not suffer from the on-chip inductor losses, and can achieve oscillations while operating at a 100μW power level using 0.13 μm CMOS technology. We thus find that it is preferable to use a current-starved ring oscillator for WSN applications. Similar results have been obtained by other authors for ultra low power receiver applications [Pletcher2009] [Krishnaswamy2008].

The Type-I analog PLL demodulates the RF signal and is at the core of the ultra low power receiver. Often, OOK architectures [Daly2007] or super-regenerative architectures [Chen2007] [Otis2005] are implemented for low power applications. In this chapter, a PLL based architecture is investigated. Compared with the super-regenerative architecture [Chen2007] [Otis2005], the data rate of the PLL based FSK receiver architecture is higher. However, one potential difficulty of OOK and the presented FSK ultra low power receiver is that this design can be susceptible to outside interference. This problem can be solved by using a highly selective surface acoustic wave (SAW) filter to remove the interference [Daly2007].

This chapter consists of five sub-sections. Section 2.2 presents the overview of the Gilbert cell based mixer and its limitations for low power applications. It then presents new mixer circuit components: a mixer/phase detector and an oscillator. Detailed circuit

analysis and design procedures have been given for the presented single input low power mixer. This topology has also been compared with previous mixer design works. Section 2.3 investigates the power limitations of the cross-coupled LC and ring oscillator topologies for 100uW power applications. We conclude that the ring oscillator is preferred for 100uW power applications. This analysis is then followed by a detailed current starving ring oscillator design. The design methodology is given, as well as simulation results. Section 2.4 demonstrates PLL's applications as FM/FSK receivers and presents the simulation results of demodulated FM/FSK signals. Section 2.5 and 2.6 discuss the selectivity and interference of the designed receiver, respectively. Section 2.7 presents the fabricated integrated circuit and the measured results for the PLL, and its performance as a receiver. Section 2.8 summarizes the work and provides conclusions.

2.2 Low Power Mixer Architecture

2.2.1 PLL Architecture

A block diagram of the second-order PLL architecture we used is enclosed in the dashed-line box in Fig. 2.2.1. The analog phase detector (PD) compares the phase difference between RF and local oscillator signals and generates a voltage proportional to the phase difference of the two signals. The phase detector employs a single RF and LO input mixer topology. This topology simplifies voltage-controlled oscillator design for the PLL application. It also simplifies the LNA circuit design when the PLL is used in FM and FSK demodulation. The first order low pass filter (LPF) removes the high frequency signal components from the phase detector and is fundamental in determining the dynamics of the PLL. As will be discussed later, we use a relatively high bandwidth

low pass filter to increase the lock-in range of the PLL to facilitate FM/FSK signal demodulation. A ring oscillator topology is utilized as the VCO to obtain μW power consumption and a large tuning range with reasonable phase noise.

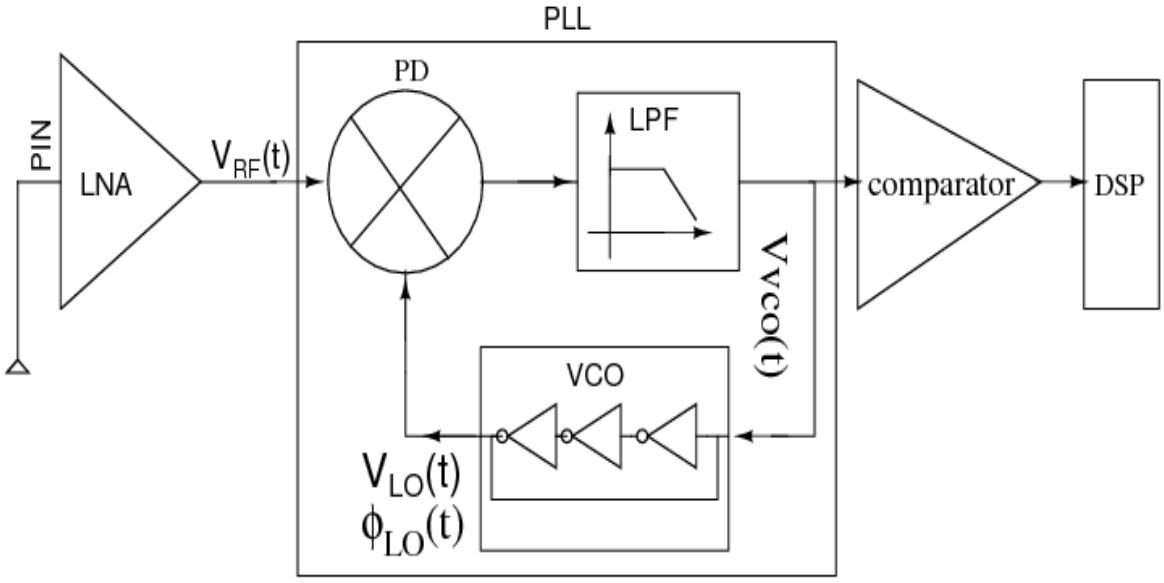


Fig. 2.2.1. Block diagram of PLL and its application as an FSK receiver when used with a LNA, comparator, and a DSP.

2.2.2 Overview of Different Mixer Architectures

Mixers are non-linear circuits widely used in communication circuits to shift signal frequencies up and down for modulation and demodulation. In most receiver applications, a mixer shifts the incident radio signal frequency down to an intermediate frequency to be further processed by the baseband circuits, while in transmitter applications, they multiply the low frequency digital baseband signal with the high frequency oscillator signal to shift up the baseband signals into different communication channels.

Ideally, mixer output is the just the multiplication of the two input signals with some amplification. Figure 2.2.2 shows the schematic of a commonly used Gilbert cell mixer. The Gilbert mixer uses differential structure at the RF input to cancel the white thermal noise at the RF input. It also uses two differential pairs (four transistors) to remove the LO leakage. Gilbert cell based mixers (phase detectors) [NG2006] [Sullivan1997] often consume power at prohibitive levels for WSN applications because of current sources and related stacked structures. The Gilbert cell also uses a differential input, which usually requires additional accessory circuitry to connect with other circuit parts of the receiver. Differential VCOs [NG2006], LNAs, or baluns [Chiou1997] are often used to meet the differential input requirements of the Gilbert cell. However, a differential input structure can be vulnerable to phase errors due to device mismatches, and a single to differential balun usually occupies a large chip area since the balun is usually implemented by on-chip inductors or off-chip transmission lines.

In this chapter, we design a new mixer topology for low power applications. We analyze the new mixer topology and provide small signal analysis results mathematically. Following the mathematical analysis, we gain insight and understanding of the mixing process and develop a design procedure. Finally, the simulated characteristics of the mixer are presented along with a comparison with previously published mixers.

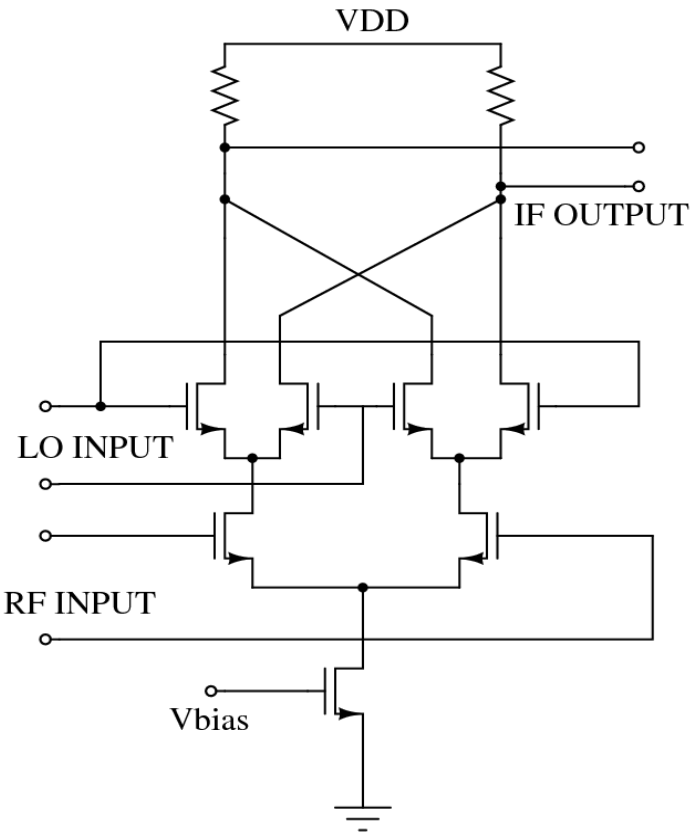


Figure 2.2.2 Schematics of Gilbert cell.

2.2.2 Down-Conversion Mixer Topology

Fig. 2.2.3 (a) and (b) are the schematic of the single RF and LO input mixer. The radio frequency signal and local oscillator signals are connected to the gates of transistors M1 and M2, respectively. The mixer (Fig. 2.2.3a) core consists of three transistors M1, M2, and M3. M1 and M3 work in the saturation region, and M2 is switched on/off by the local oscillator signal. M2 chops (multiplies with a square wave) the RF signal. We used the intrinsic capacitors of M3 to filter out the high frequency harmonic signals to obtain high mixer linearity. Fig. 2.2.3b shows the mixer with one extra transistor (M4) to further filter out high frequency harmonic signals and thus to improve mixer linearity. In addition, since M2 chops the RF signal, only the down-converted signal needs to be

amplified by M3 and M4. Therefore, the frequency limitation of the mixer is due to M1 and M2, which have very large unity gain frequencies, since they are minimum size devices. Thus, the designed mixer can operate at very high input frequencies.

Figure 2.2.3b adds an extra transistor to further filter out the high harmonic signals. Transistor M3 works in the linear region and transistor M4 works in the saturation region. The extra transistor further filters out the high harmonic signal and thus improves the linearity of the mixer. Since M3 works in saturation region, the mixers in Figure 2.2.3 panels (a) and (b) have similar voltage gain.

The presented mixer topology consumes less power due to its single branch structure

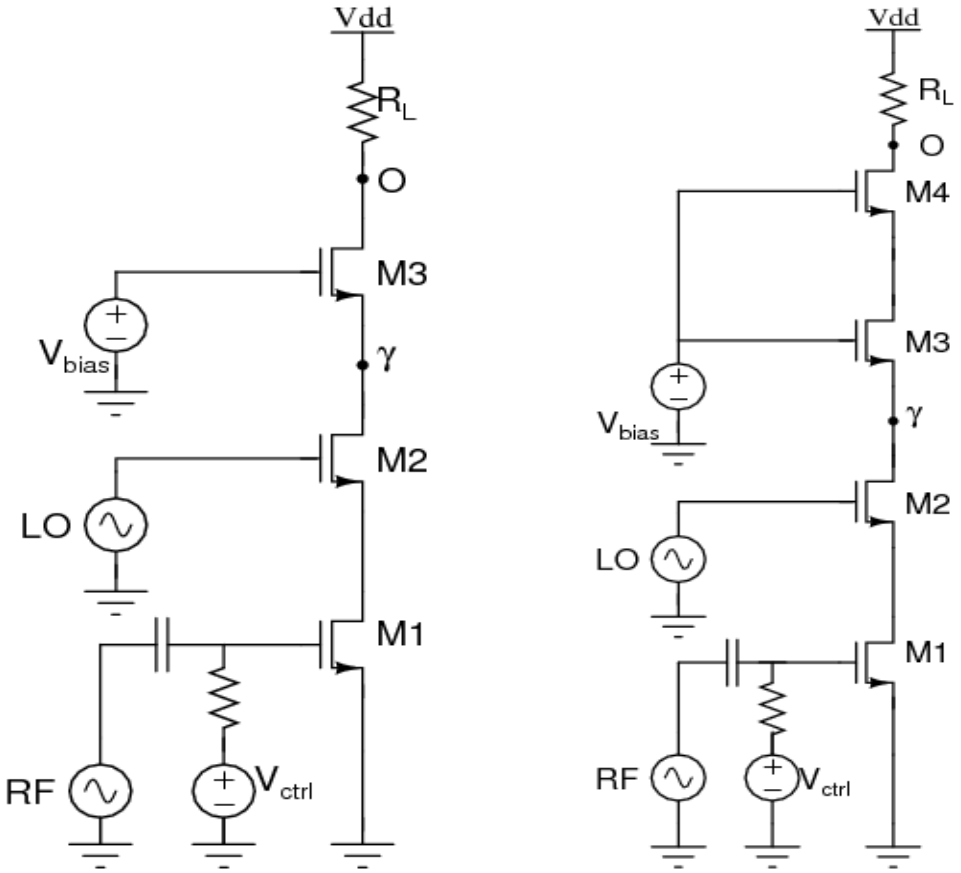


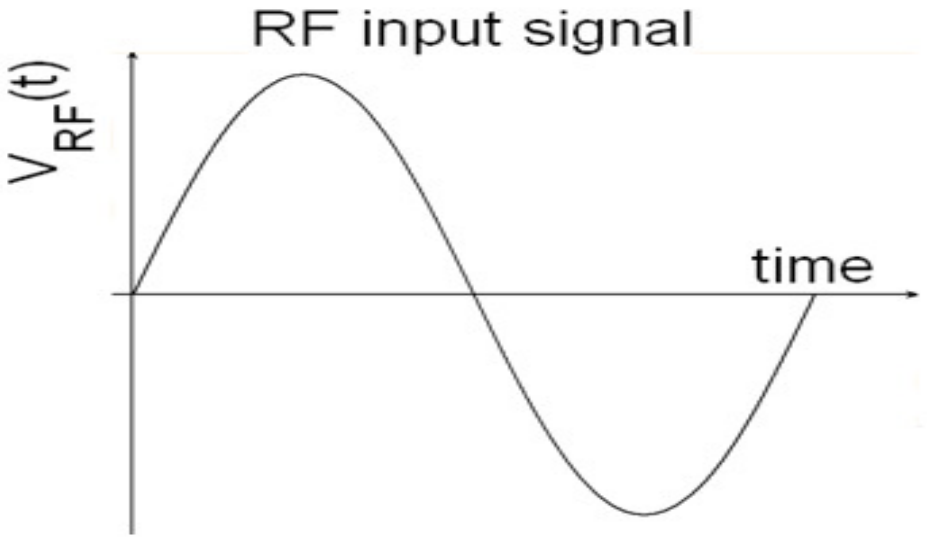
Fig. 2.2.3: The schematic of the mixers (a): Three transistor mixer. (b): Four transistor mixer.

and current re-use. In other words, we use a single current through the structure to multiply, amplify, and filter the signal. In addition, M2 is chosen to be a minimum size device, and it requires minimal power for device switching.

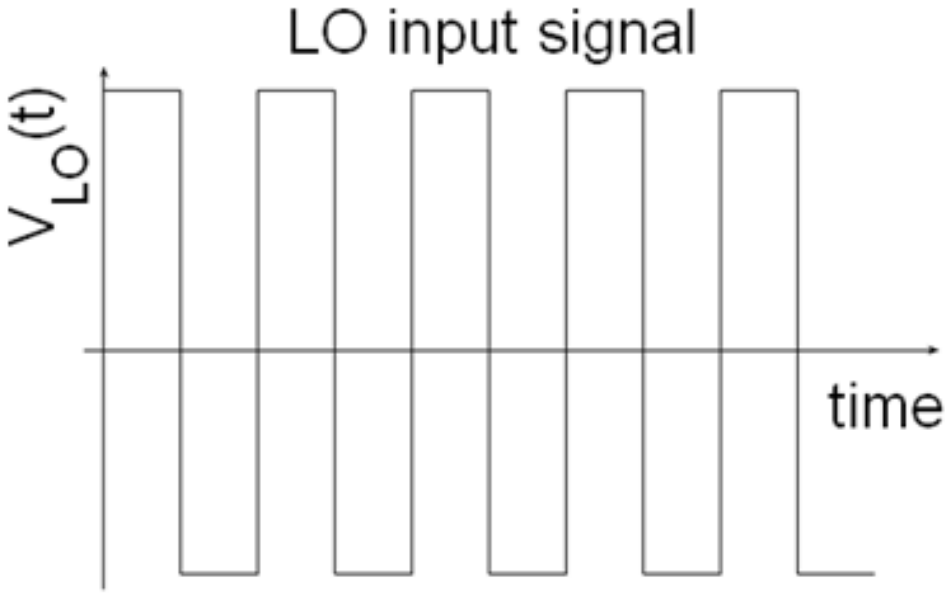
Another attribute of the mixer is that it provides a natural DC bias for the next stage (VCO) of the PLL. More specifically, V_{ctrl} sets the DC bias for M1 and controls the DC output voltage (point O). Since the output has a DC connection to the VCO (after the LPF), V_{ctrl} controls both the DC bias point and the VCO operation frequency with a single bias. This multi-purpose bias thereby also provides the ability of the PLL to track in a wide frequency range.

2.2.3 Design and Analysis of the New Mixer

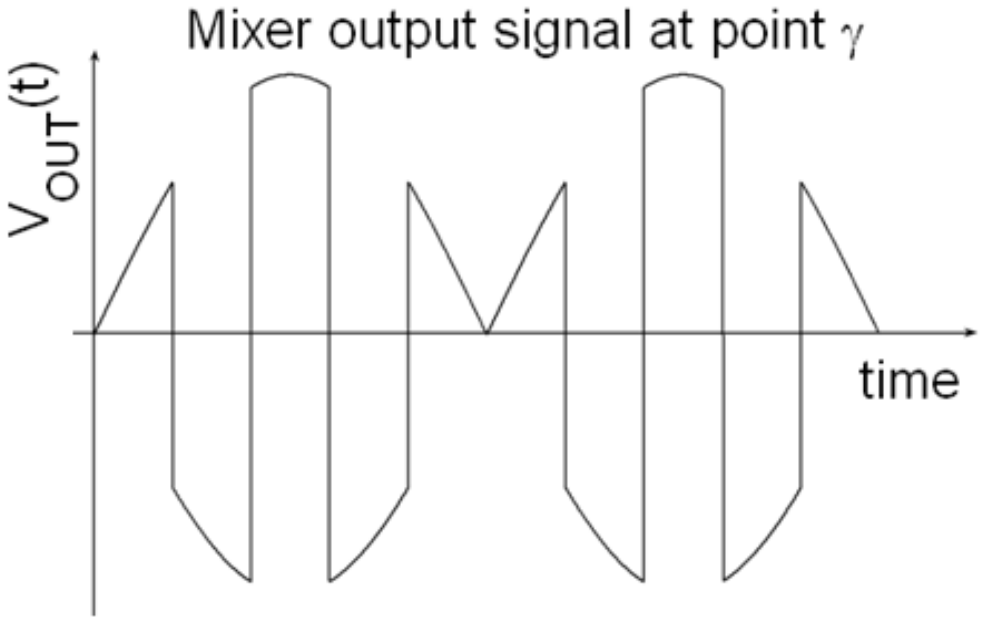
The mixing process is described as follows: The local oscillator signal switches the transistor M2 on and off at the oscillator's frequency.



(a)



(b)



(c)

Fig. 2.2.4: (a): Input RF signal. (b): Local oscillator signal. (c) Output signal

The RF signal applied to the gate of M1 is coupled to the LO signal and appears at the drain of M2 in the form of a function of the LO signal. Figure 2.2.4 shows the

multiplication process. As the local oscillator turns on/off the M2, the output signal looks like the wave at in Figure 2.2.4c. For a purely sinusoidal radio signal, the signal source at point γ can be mathematically described by equation 2.2.1:

$$V_{\gamma'}(t) = V_{RF}\sum \frac{\Delta_n G}{2}(\cos(n\omega_{LO}+\omega_{RF})t + \cos(n\omega_{LO}-\omega_{RF})t), \quad \Delta_n = V_{pp}\frac{\sin\frac{n\pi}{4}}{\frac{n\pi}{2}} \qquad 2.2.1$$

Where G is the magnitude of the gain of the multiplier from the RF input port to the output at point γ, V_γ is the loaded voltage at point γ, and $V_{\gamma'}$ is the open circuit voltage at γ. V_{pp} is the square wave peak to peak voltage.

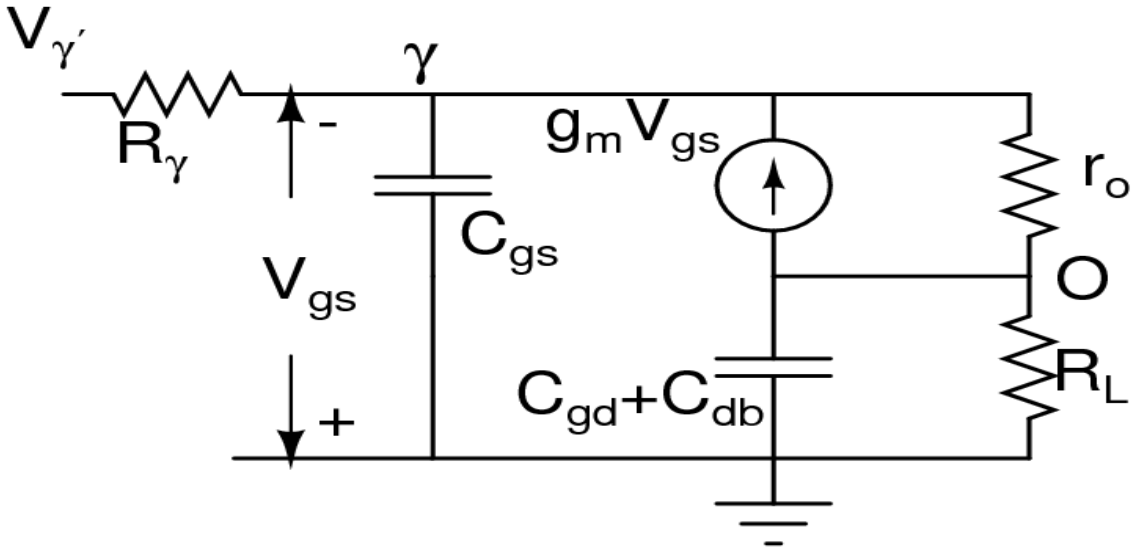


Figure 2.2.5: Equivalent circuit of transistor M3 as seen by voltage source $V_{\gamma'}$ with source resistance $R_{\gamma'}$.

As indicated previously, transistor M3 amplifies the desired low frequency signal and filters out the high frequency harmonic components to improve the linearity of the down-conversion mixer. Figure 2.2.5 shows the small signal equivalent circuit seen at the point

γ, looking into the source of M3. R_γ and r_o are the output resistance looking toward M2 at point γ and the M3 channel modulation resistance, respectively. A detailed small signal analysis can be found in Appendix A.

The small signal voltage gain V_O/V_γ is given as:

$$A = \frac{Z_L(1+g_m r_o)}{(Z_L + r_o)(1+sC_{gs}R_\gamma) + (g_m r_o + 1)R_\gamma} \qquad 2.2.2$$

Where C_t is $(C_{gd}+C_{db})$ and Z_L is $R_L/\!/(1/\omega C_t)$. Since $g_m r_o >> 1$, for low frequency signals the voltage gain is

$$A_{low} = \frac{R_L}{R_\gamma} \qquad 2.2.3$$

For high frequencies,

$$Z_L \approx \frac{1}{sC_t}$$

and the voltage gain is

$$A_{high} = \frac{(1+g_m r_o)}{(1+sC_t r_o)(1+sC_{gs}R_\gamma) + R_\gamma sC_t(g_m r_o + 1)} < \frac{1}{R_\gamma sC} << 1 \qquad 2.2.4$$

Judging by equations (2.2.3) and (2.2.4), the transistor M3 should be designed to be large enough to filter out the high frequency harmonic signals but be small enough to amplify the desired intermediate frequency (IF) signal. To achieve this, the size of transistor M3 has been chosen as 200μm/640nm in this design. Transistors M1 and M2 are chosen to be as small as possible for high frequency application. The ADS simulation results show that the mixer can operate from 1 GHz to 60 GHz using a 1.2V supply voltage. Such a high operation frequency originates from the mixer topology. The signal multiplication process is only performed by the transistors M1 and M2 where minimal

devices have been chosen. This observation is further confirmed by the ADS simulation results of the mixer.

The power consumption is mainly determined by the supply voltage (V_{dd}) and the RF DC bias voltage (V_{ctrl}). Figure 2.2.6 shows the simulation result of the mixer (the input signal are -60dBm@2.2GHz and 1.2V peak to peak square wave@2.195GHz).

ADS simulation results show that the mixer can operate from 1.6 GHz to 60 GHz with a 1.2V supply voltage. The power consumption, which is verified by ADS simulations, is mainly determined by supply voltage (V_{dd}) and RF DC bias voltage (V_{ctrl}).

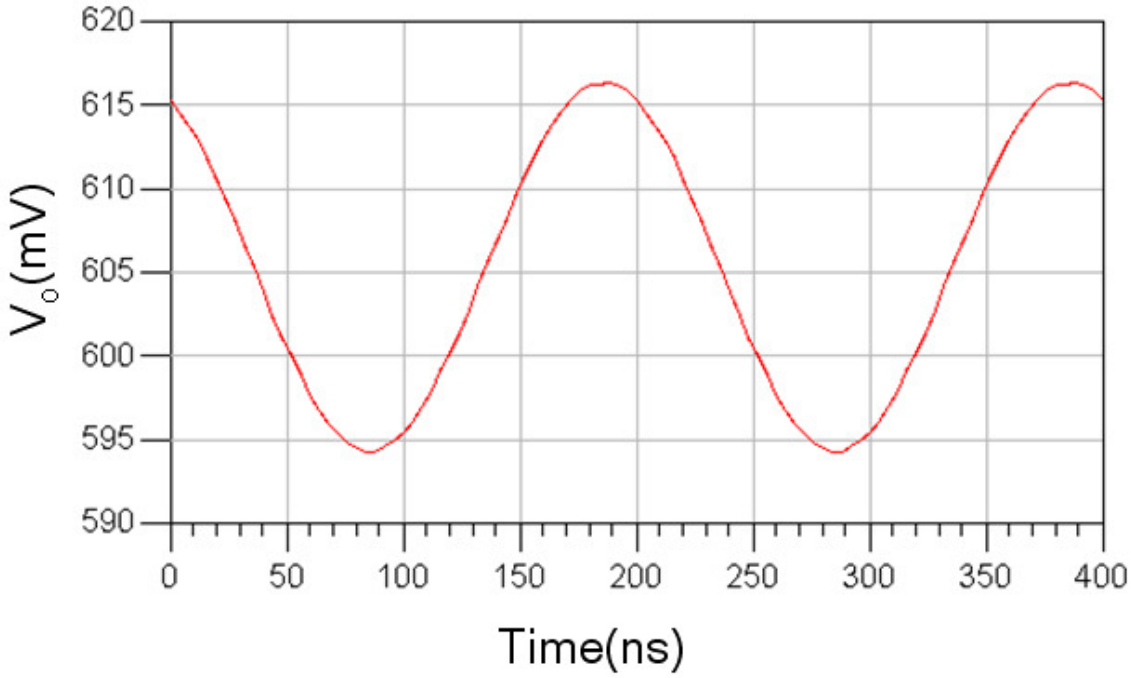


Figure 2.2.6 The 5MHz output signal of the mixer (the input signal are -40dBm@2.2GHz and 1.2V peak to peak.square wave @2.195GHz).

In Fig. 2.2.3b, we show a small revision to the mixer topology by adding an additional transistor M4 to improve linearity. For this circuit, transistor M3 works in the linear region. The operation of this circuit is analogous to that in Fig. 2.2.2a; however, the

addition of the extra transistor M4 acts as a second filter in series with the filtering effects provided by M3, thereby increasing the high-frequency roll-off of the mixer and improving the linearity of the mixer. In addition, it should be pointed out that M4 provides a voltage gain of the down-converted (IF) signal, while in Fig. 2.2.3a, M3 provided the voltage gain. The design in Fig. 2.2.3b commonly achieves a higher linearity than the one in Fig. 2.2.3a, while having a similar voltage gain. These analyses agree with ADS simulation results.

The mixer voltage gain is constrained by the power consumption, so is the noise. M1 is chosen as a minimum length device (L=130nm) to help minimize indirect flicker noise [Darabi2000], as well as to achieve a high unity gain frequency f_T. The transistor M2 is turned on/off by the ring oscillator signal and consumes CV^2f power where C is the M2 gate capacitance, V is the peak to peak voltage of the oscillation signal (LO as shown in Fig. 2.2.3) and f is the oscillation frequency. M2 is chosen to be the minimum size device to minimize the device capacitance and thus minimize the power consumption. Due to the ultra low power constraints, g_{m1} needs to be small to meet the low power requirements. The mixer requires a large resistor at the drain of the transistor M3 as shown in figure 2.2.3 (a) in order to obtain reasonable gain. Furthermore, for the receiver application, the next stage following the mixer is a low pass loop filter, and thus does not load down the AC voltage gain at base-band frequencies. We use a resistor load R_L instead of an active load to eliminate flicker noise of the active load.

To arrive at our circuit, we established several constraints to facilitate design in a 130nm CMOS process for WSN applications. The power is constrained to be less than 50 μW and the voltage amplitude of the down converted signal is required to be at least 50 times

larger than the amplitude of harmonic signals. Furthermore, the output voltage at point O, which is DC connected to the mixer through the low pass filter, needs to vary around a quiescent voltage of 0.6V (half of the V_{dd}) to ease the voltage controlled oscillator design. The bias current is set by the power consumption, $I=P/V_{dd}$. The resistor value (R_L) is calculated using the current and the required voltage gain. The M1 size is calculated from the current, after a single DC bias voltage is applied to both V_{ctrl} and V_{bias}. The minimal device area of the transistor M3 is calculated from equations 2.2.3 and 2.2.4. The precise sizes of the transistors are then refined using ADS, while employing accurate BSIM4 transistor models to optimize performance and satisfy the design constraints. The simulation results agree reasonably well with the analytical results.

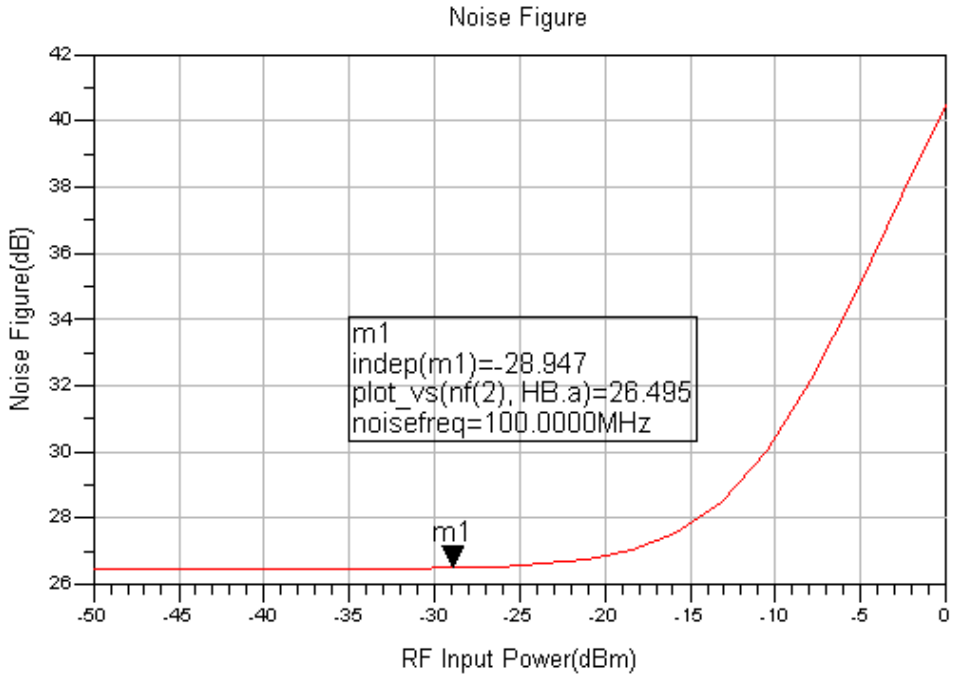
2.2.4 Characteristics of the Mixer

Power consumption, noise figure, conversion gain, and linearity (IIP3) help to evaluate mixer performance. Figure 2.2.7 shows the mixer noise figure, conversion gain, and linearity of the mixer as a function of input power. For our mixer design, simulation results show that the power consumption, voltage conversion gain, noise figure, and IIP3 are 48μW, 8dB, 26.5dB, and 23dB, respectively, as shown in Figure 2.2.7. The mixer figure of merit (*FOM*) can be expressed [Liang2007] as

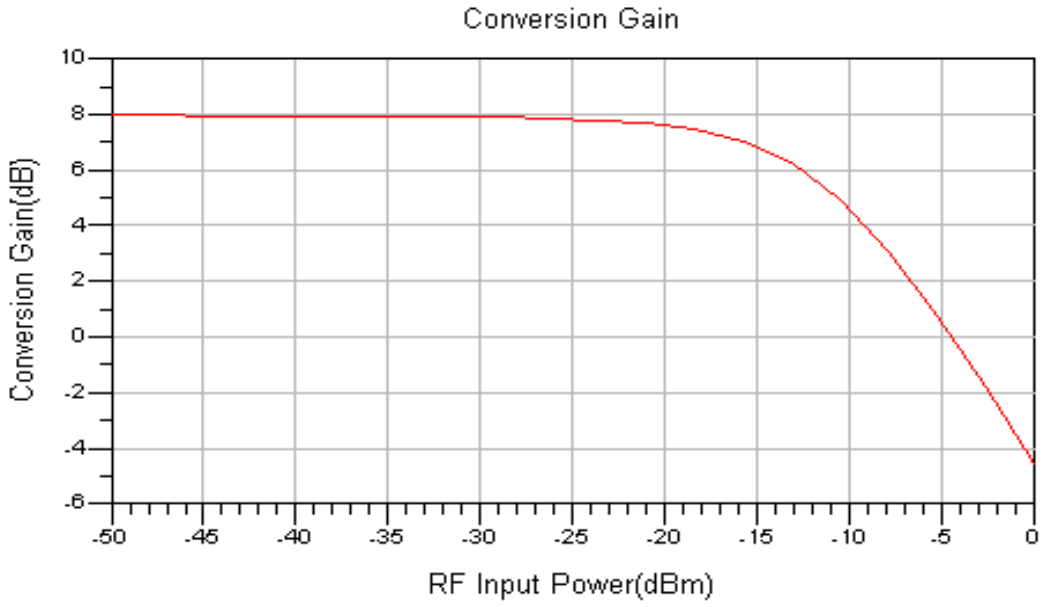
$$FOM = 10\log\left(\frac{10^{G/20}.10^{(IIP3-10)/20}}{10^{NF/10}.P}\right) \qquad 2.2.5$$

Where *G* and *NF* represent voltage gain and the noise figure in dB, *P* represents power consumption in Watts, and IIP3 describes the linearity in dB. It can be seen from equation 2.2.5 that a higher *FOM* indicates better performance. Figure 2.2.7 shows the

simulation results of mixer noise figure, voltage gain, and IIP3 respectively using ADS simulator. Our mixer shows a simulated *FOM* of 27.2. The values for *FOM* found in the literature range from -2.28 to 13.2 [Liang2007]. Table 2.1 summaries and compares this mixer simulation performance with other published results.



(a)



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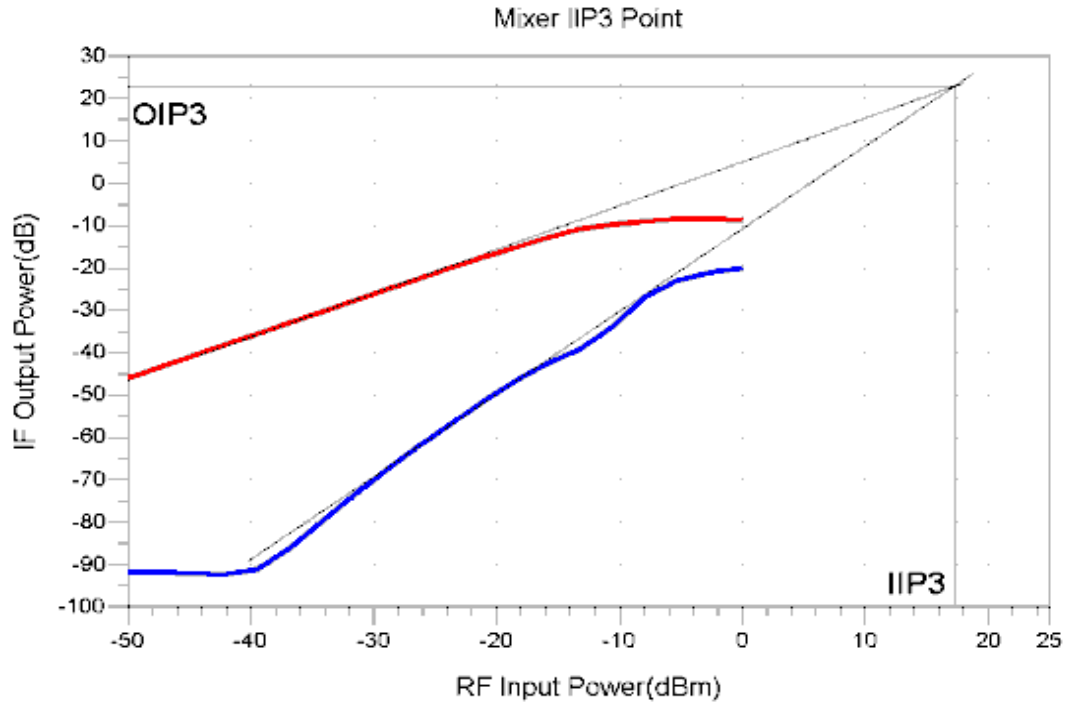


(c)

Figure 2.2.7 (a): Mixer noise figure. (b): Conversion gain of mixer. (c): Linearity of the mixer (IIP3).

Table 2.1 Comparison with previous mixers [Liang2007]

Ref	Process	RF Frequency (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	Power Consumption (mW)/V_{DD}(V)	F.O.M (dB)
52	0.13μm CMOS	2.1–3	14.8	5.4	-2.8	1.6/0.6	9.45
53	0.18μm CMOS	2.4	12.9	15.7	1	8.1/1.8	11.3
54	0.18μm CMOS	0.3-4	14	11	4.1	6.6/1	10.3
55	0.18μm CMOS	2.45	16	13.3	-1	7.2/1.8	6.6
56	0.18μm CMOS	5.25	24.5	8.3	0.03	4.95/0.9	-2.28
26	0.13μm CMOS	0.5-7.5	15	5.7	-5.7	0.48/0.77	13.2
This work	0.13μm CMOS	1-10	26.5	8	23	0.048/1.2	27.2

2.2.5 Phase Detector

The analog mixer works as a natural analog phase detector when the two input signal frequencies are the same. Figure 2.2.8 shows the output voltage varies with the phase difference of the two signals having the same frequency. The phase detector output voltage can be described by equation 2.2.6:

$$Vout = Vdc + A \times V_{rf} \times V_{LO} \times \sin(\phi) \qquad (2.2.6)$$

Where A is the phase detector voltage gain and ϕ is the phase difference of the two input signals of the phase detector. Figure 2.2.9 indicates the simulation result of the phase detector gain (A), which varies with different frequencies. The voltage gain of the phase detector remains constant over the frequency range (1.6GHz to 2.4GHz). Figure 2.2.10 shows the simulation results of the phase detector voltage output for different input

frequencies. The result indicates that the phase detector successfully generates a voltage corresponding to the phase difference across the frequency range of 1.6GHz to 2.4GHz.

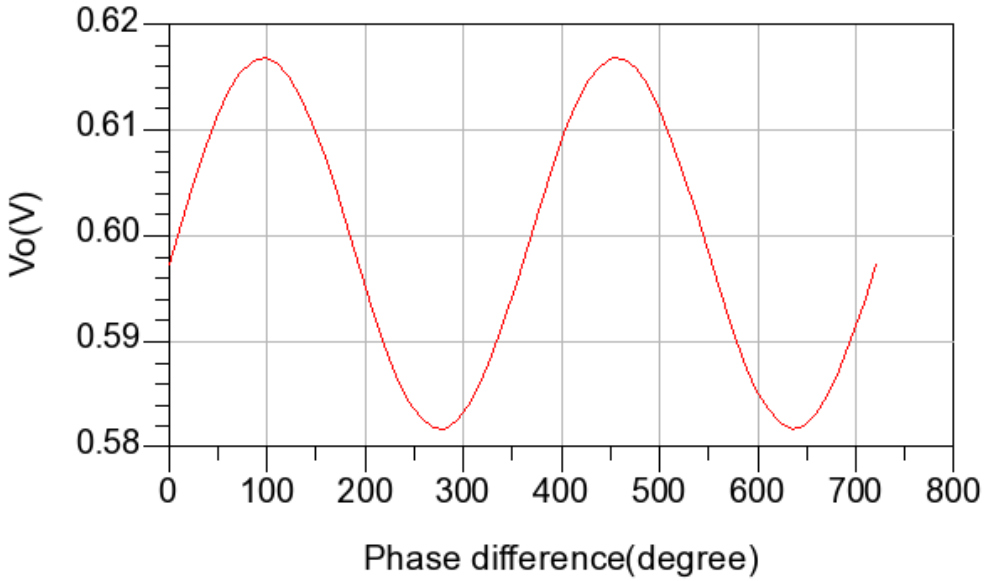


Figure 2.2.8 The phase detector output signal of the mixer (the input signal are -35dBm@2.2GHz and 1.2V peak to peak square wave @2.2GHz with different phase).

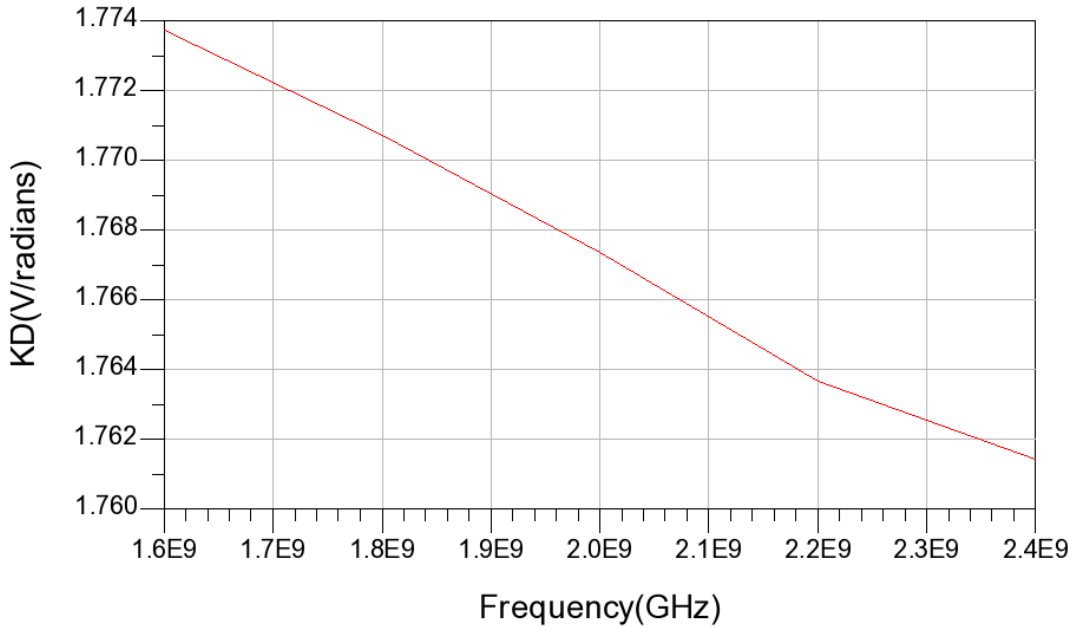


Figure 2.2.9. Phase detector gain varies with frequency.

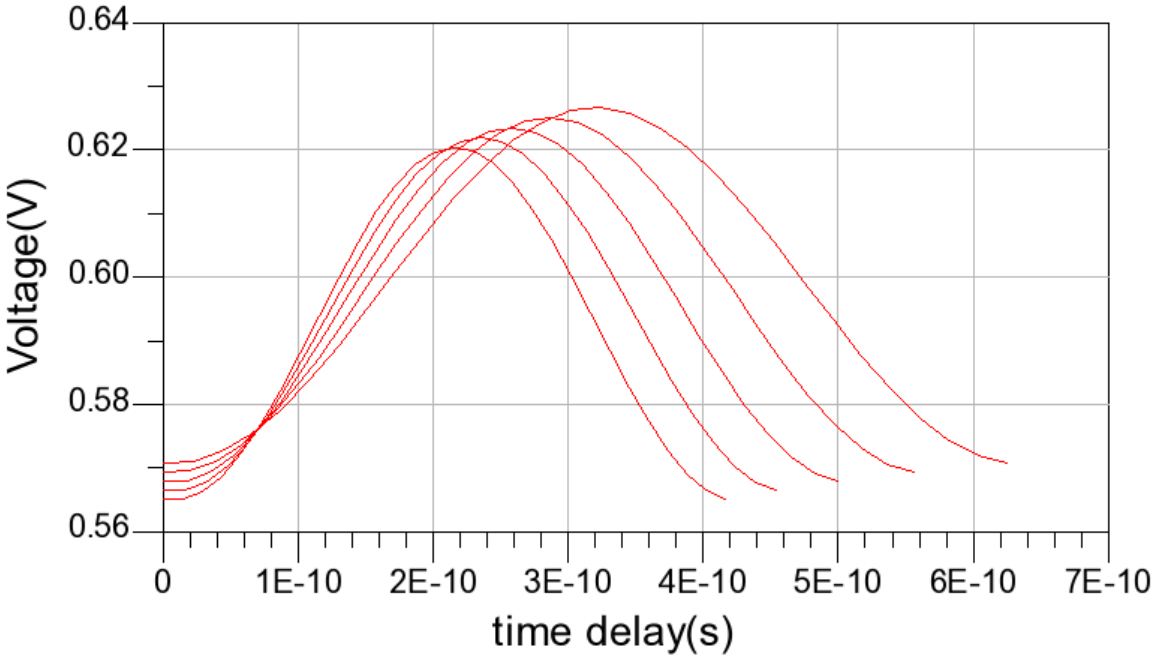


Figure 2.2.10 Phase detector output varies with phase differences for different frequencies (the inputs are 10mV RF signal and 0-1.2 square wave LO signal for frequency 1.6G, 1.8GHz, 2.0GHz, 2.2GHz, and 2.4GHz.

2.2.6 Summary

A low power mixer circuit topology has been designed. A detailed analysis of this mixer circuit has been given. The contribution of this work can be summarized as follows:

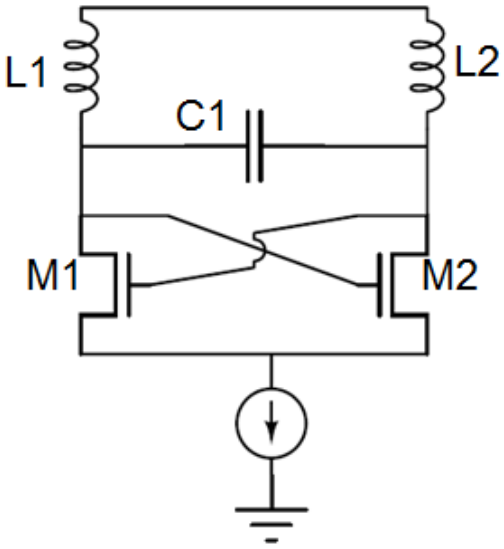
- A novel down conversion mixer topology has been presented with
    - Low power consumption due to current reuse
    - High linearity
    - Wide operation frequency of the mixer
    - Control of the output voltage using DC bias of RF signal
- Simplified the connection circuits such as for VCO and LNA designs because there is a single input topology of the mixer
- Detailed analysis and design procedures of the mixer
    - Detailed small signal model analysis of the proposed mixer
    - Identification of the key parameters to optimize mixer performance
    - Detailed design procedure

2.3 Low Power VCO Design

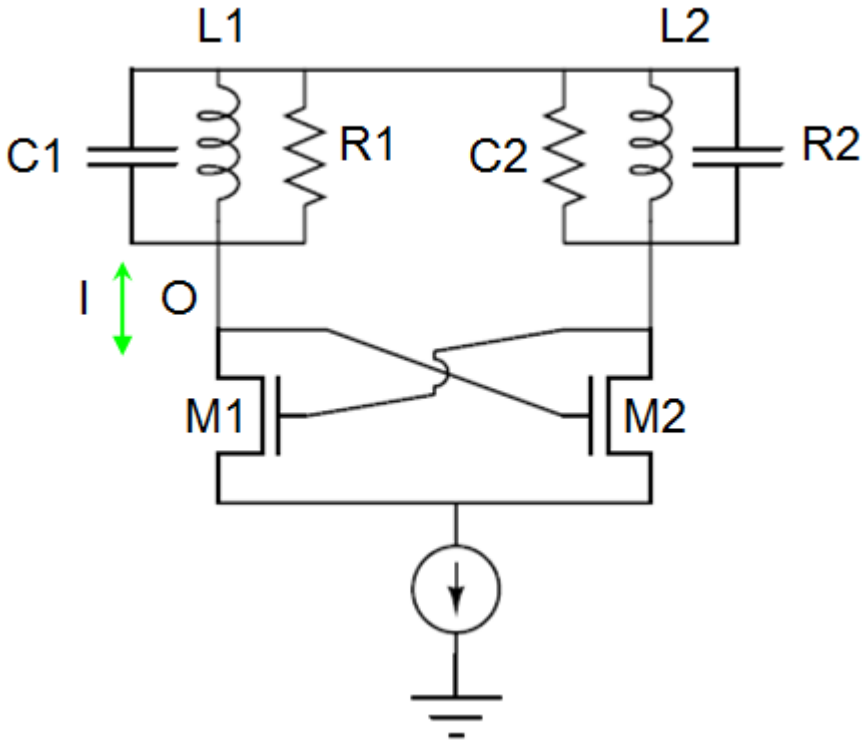
Voltage controlled oscillators generate high frequency carriers for both modulation and demodulation and are one of the key components in FSK/PSK transceivers. They provide the carrier signal to mix with baseband signals to generate different kinds of modulation such as BFSK, 8-FSK, etc. in transmitter circuits. For the receiver, they generate the extremely accurate (less than 10KHz frequency drift) carrier signals to mix down the modulation signal to lower frequencies for further baseband signal processes.

The main VCO topologies are LC based oscillators and positive feedback based ring oscillators.

In WSN applications, we seek extremely low power circuits. LC oscillators are widely used in portable applications due to their superior phase noise characteristics. For a transmitter, low phase noise is necessary to meet FCC spur specifications. For a receiver, low phase noise oscillators help to strongly suppress the out of band interferences. However, all published LC oscillators consume more than mW power[Lee2005] [Andreani2002] [Margarit1999]. Theoretically, a parallel connected lossless inductor with a lossless capacitor can oscillate naturally at resonant frequency with zero power consumption, and they strongly amplify the thermal noise at its resonant frequency and suppress noise power at all other frequencies. However, in reality, there are always losses accompanied with capacitors and inductors. Quality factors can be used to describe the loss characteristics of networks. In order to oscillate using the lossy LC network, the oscillator needs to pump in power to the LC network to compensate for the losses of the network. Figure 2.3.1 is the schematic of the commonly used differential LC oscillator. It uses the transistors M1 and M2 to compensate for the losses of the inductors L1, L2 as well as losses due to capacitor C1, where capacitor C1 is the parasitic capacitance of the transistors M1 and M2. In a simplified case, the on-chip inductor can be modeled by a parallel R,L,C network as shown in Figure 2.3.1b. In the next paragraph, we present a detailed analysis of a LC oscillator to investigate their power limitations.



(a)



(b)

Figure 2.3.1 (a) LC Cross coupled oscillator. (b) LC Cross coupled oscillator using inductor model.

In figure 2.3.1 (b), the resistor R1 represents the losses of the inductors and capacitors. The capacitors in modern CMOS processes have quality factors on the order of hundreds because the electrical field can be limited inside the metal layer of the capacitors and ohmic losses due the metal can be minimized by choosing proper sizes for the capacitors. However, the on-chip inductors have poor quality factors because the magnetic field cannot be constrained inside metal layers: the magnetic field penetrates the lossy silicon substrates which causes significant losses for the inductor. Also, the ohmic losses of the metal are significant because of the skin effects (high frequency current is constrained at the very narrow edge of the metal) [Lee2003]. On-chip inductors typically have a quality factor less than 10 in current CMOS processes. The losses from the capacitors are significantly lower than the losses from the inductors. The inductor losses can be characterized by resistance R_1 as described by equation 2.3.1:

$$R_1 = \omega L_1 Q \qquad 2.3.1$$

Where Q is the quality factor of the LC network.

The output oscillator signal amplitude is defined as V_{ac}. The AC power consumed by R1 can then be described as equation 2.3.2:

$$P_{ac} = \frac{V_{ac}^2}{2R_1} = \frac{V_{ac}^2}{2\omega L_1 Q} \qquad 2.3.2$$

In an extreme case, if the network has no loss, the quality factor is infinite. The power consumption is zero which agrees with previous statements that an LC component oscillate can oscillate with zero power for a lossless network.

In order to oscillate, the oscillators need to pump power into the RLC network via the transistors M1 and M2. The inductor L1 works as shorted in DC, and the DC voltage at

point O is thus equal to V_{DD}. The DC current is controlled by the DC current source as shown in figure 2.3.1. The amount of DC current controls the trans-conductance of the MOSFETs and also the amount of power pumped into the LC tank. In order to maintain oscillations, the following equation needs to be satisfied:

$$g_{m1} > 1/R_1 \tag{2.3.3}$$

The drain current of the mosfet is proportional to the square of the voltage difference between the gate and source when the mosfet works in saturation regions. The current can be estimated as:

$$I = g_{m1}(VDD - Vth)/2 > (VDD - Vth)/(2R_1) = (VDD - Vth)/(2\omega L_1 Q) \tag{2.3.4}$$

$$P_{M1} = VDD * I = VDD(VDD - Vth)/(2\omega L_1 Q) \tag{2.3.5}$$

$$P_{\min} = 2 \times VDD \times I \geq VDD \times \frac{VDD}{\omega L_1 Q} \tag{2.3.6}$$

Equation 2.3.6 clearly indicates that the LC oscillator power is limited by the supply voltage, inductor value, and tank quality factor. For an ideal inductor, the quality factor (Q) is infinite. The required power of the LC oscillator is zero, which agrees with previous statements. Equation 2.3.2 and 2.3.6 also indicate that the required oscillation power is inversely proportional to the inductor value L. If the inductor value is infinite, the power consumption is zero, too. However, there is a limitation on the maximum inductor value based on the design frequency. This is because on-chip inductors have inherent capacitances that cause self-resonance frequencies of on-chip inductors. Since the transistors M1 and M2 can only contribute extra capacitance, the maximum inductor needs to have a resonant frequency larger than the designed frequency to achieve oscillations at the designed frequency. Moreover, the tuning requirements of the VCOs

impose extra requirements on the maximum inductor value that can be chosen. The detailed extraction of the lumped components of on-chip inductors can be found in Appendix B. A simple example is shown below to estimate the minimal required oscillation power for operation at 2.2 GHz.

An inductor with 3GHz self-resonant frequency has been chosen for a 2.2GHz application to provide some tuning range margin. The extracted lumped components of the inductor show a 10 nH inductance for the inds type inductor from the IBM foundry. The extraction results also show the inductor quality factor of the inductor is about 10.

For long channel MOSFET devices, the drain current has a square-law dependence on the gate-source voltage minus the threshold voltage. The minimal oscillator power consumption for an oscillator using a 10 nH inductor under 1.2V supply voltage is

$$P_{\min} = VDD * I = VDD(VDD - Vth)/(2\omega L_1 Q) = 0.26mW \tag{2.3.7}$$

where VDD, Vth, and L_1 are the supply voltage, threshold voltage, and inductor value which are equal to 1.2, 0.6, and 10nH, respectively.

In sub-micrometer technology, the drain current has a linear-law dependence on the gate-source voltage minus the threshold voltage for short channel devices. The DC power required is described by:

$$I = g_{m1}(VDD - Vth) > (VDD - Vth)/(R_1) = (VDD - Vth)/(\omega L_1 Q) \tag{2.3.8}$$

$$P_{\min} = VDD * I = VDD(VDD - Vth)/(\omega L_1 Q) = 0.52mW \tag{2.3.9}$$

As shown above, the required minimal power doubles if the transistors obey linear-law dependence between the drain current and the gate-source voltage.

In the previous analysis, the minimal required power for the LC oscillator is 0.52 mW using the IBM technology. This even does includes the necessary AC power needed to compensate the power consumed by resistors R_1 and R_2 as described by equation 2.3.2.

The equations 2.3.2 and 2.3.5 state that the power consumption approaches zero as the quality of the LC tank goes to infinity. It is clear that the power limitation comes from the lossy inductors.

Furthermore, the required oscillation power cannot be improved by scaling the technology down. The CMOS scaling trend does manage to provide smaller and smaller capacitance devices. However, as we stated before, the parasitic capacitance of the inductors limits the operation frequencies instead of the parasitic capacitors of the MOSFETs. The CMOS technology downscaling thus cannot help reduce the minimal required power of the LC oscillators unless better quality inductors can be manufactured.

We thus conclude that the LC oscillators are not suitable for WSN applications where oscillators with 100uW power consumption are necessary, unless the manufacturing process can provide better quality inductors in the future.

Unlike the LC oscillators, the ring oscillator topology uses positive feedback to provide a 360 degree phase shift with feedback gain which is larger than 1 to generate oscillations. This avoids using lossy inductors and thus makes it possible to meet our 100uW power consumption requirements. The ring oscillator power is described by

$$P = CV^2 f \qquad 2.3.10$$

Equation 2.3.9 indicates that the ring oscillator power is determined by the capacitance of the MOSFET, the supply voltage, and the operation frequency. The CMOS process can

provide smaller capacitances as the CMOS process scales down. It thus possible to achieve 100 uW power consumption by taking advantage of the technology scaling trend.

A CMOS inverter ring oscillator topology is chosen as the VCO in this PLL for its 100 μW range power consumption, compactness, and ease of implementation.

Fig. 2.3.2 is the schematic of the current-starved ring oscillator used as the VCO in the PLL. It uses a minimal three inverting stages in a ring to minimize the oscillator power consumption and to generate oscillations. The input control voltage V_{VCO} sets the drain current I_D that controls the oscillating frequency of the VCO. The higher the current, the faster the capacitances of the transistors can be charged/discharged, which corresponds to different oscillation frequencies. The current I_D is mirrored in 1:140 scale in each inverting stage to minimize the power consumed by the reference current mirror. The output of the ring oscillator V_{osci} is buffered by an inverter to reduce capacitive loading of the next stage.

The sizes of the inverting stage transistors are designed to obtain the switching point at half of the power supply voltage. The symmetry of the rising and falling edges improves the phase noise by lowering the $1/f^3$ corner frequency [Hajimiri1999].

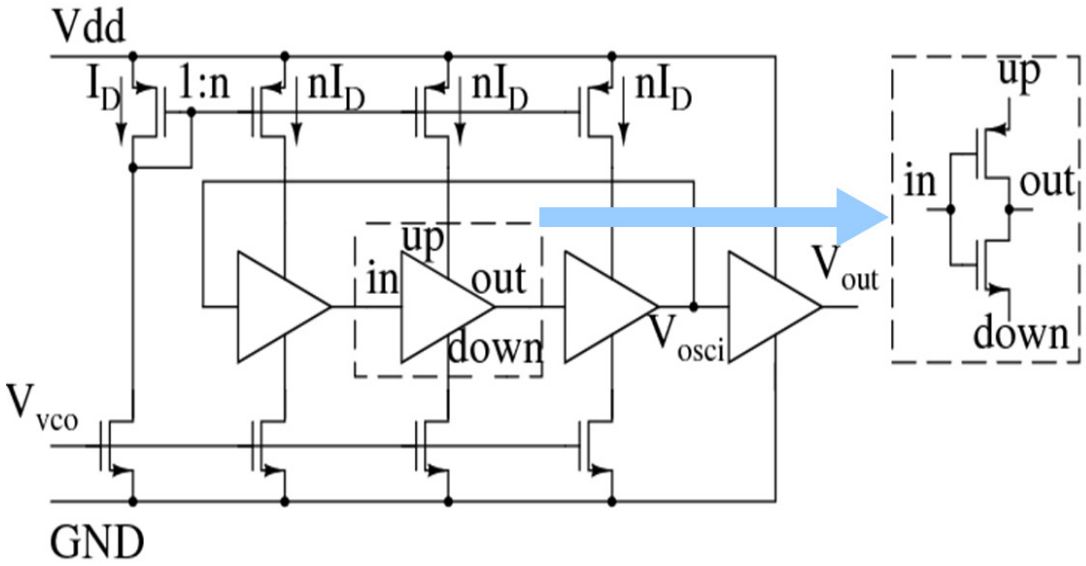


Fig. 2.3.2: The schematic of the current-starved ring oscillator.

In the PLL, the output of the ring oscillator V_{out} is connected to the LO input of the mixer as shown in Fig. 2.3.2. The filter mixer output is connected to V_{VCO} as shown in Fig. 2.2.3(a). V_o (at the mixer output) and V_{VCO} have been designed to make the VCO work at 2.1 GHz frequency, with an upward/downward 600 MHz range available by varying V_{ctrl}, which is equal to a VCO tuning range of 600 MHz. The relationship between the oscillation frequency and the input voltage (V_{VCO}) is shown in Fig. 2.3.3. The extracted layout simulation frequencies are slightly lower than the measured data. The discrepancy may result from process threshold voltage variation of the transistors. The linearity around the PLL working frequency range is sufficient for proper operation. The power consumption of the VCO is 207μW. The area of the VCO layout is 0.001mm^2.

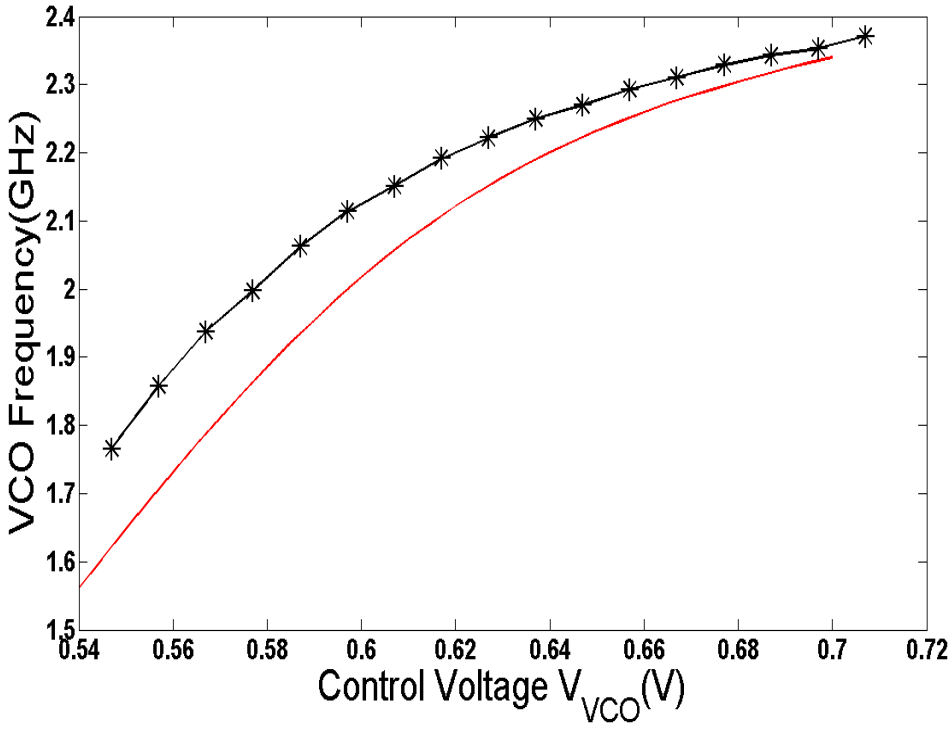


Fig. 2.3.3: Measured (symbols with solid line) and extracted simulated (solid line) VCO tuning characteristics.

2.4 Phase Locked Loop and Its Applications:

Background

Phase locked loops (PLLs) play important roles in modern communication circuits and in digital circuits. In communication circuits, phase locked loops can program the oscillation frequencies [Yan2001][Muer2002] and thus are widely used in modern high performance transceivers for channel selections [Yan2001][Muer2002]. PLLs are also extensively implemented in the digital domain for clock generation [Ingino2001] and recovery circuits [Kishine1999] in microprocessors.

Type I PLLs are composed of a phase detector, low phase filter, oscillator, and frequency divider. In type II PLLs, a charge pump is used to guarantee both the same frequency and the phase between the input signal and the locked signal [Razavi2000].

2.4.1 Theoretical Study of PLL Based Receiver Architecture

The proposed PLL has been integrated with a LNA to work as a RF receiver. The LNA is placed in front of the PLL to meet the receiver sensitivity requirement as well as to provide necessary input matching. The receiver can demodulate both FM and FSK signals. In general, a FM signal is described as:

$$V_{RF}(t) = A\sin(\omega_0 t + M\sin(\omega_s t)) \qquad 2.4.1$$

Where ω_0, ω_s, and M are the carrier frequency, baseband frequency, and modulation index, respectively. When the PLL tracks the input signal, the VCO output voltage is

$$V_{out}(t) = B\sin(\omega_0 t + M\sin(\omega_s t) + \phi) \qquad 2.4.2$$

$$\phi_{out}(t) = \omega_0 t + M\sin(\omega_s t) + \phi \qquad 2.4.3$$

Where B is the VCO amplitude which is constant; ϕ is the phase error. According to the definition of the VCO, the frequency of output signal is proportional to the control voltage of the VCO. So, the control voltage of the VCO is proportional to the derivative of the phase of the VCO oscillation signal and can be described by equation 2.4.4

$$V_{VCO} = \beta\frac{\partial\phi_{out}}{\partial t} = \beta(\omega_0 + M\omega_s\cos(\omega_s t)) \qquad 2.4.4$$

Where β is a constant. Equation 2.4.4 shows that the VCO control voltage is the demodulated signal when the PLL is tracking the input signal.

The loop filter is fundamental in determining the settling sspeed and lock-in range of the PLL. Theoretically, the lock-in range is on the same order of the loop bandwidth, and a larger loop bandwidth means faster PLL settling time, which is preferred in most applications. However, a higher -3dB point frequency in the loop filter increases ripples and also cannot filter out the VCO phase noise beyond the loop bandwidth. In this receiver application, a 100 MHz bandwidth LPF is used to provide a large lock-in range, which is preferred in FM/FSK receiver applications. The simulation results indicate that the PLL obtains a 90 MHz lock-in range for a fixed V_{ctrl}. For receiver applications, $V_{vco}(t)$ is the demodulated signal under the PLL locked condition. Fig 2.4.1 is the simulation result of FM demodulated signal using the radio frequency design environment (RFDE) simulator. This shows that the PLL successfully demodulates a 2.3 GHz FM signal with 16 MHz modulation, and the lock-in time is approximately 80 ns.

Under locked conditions of a binary frequency shift key (BFSK) input signal, the PLL tracks two different frequencies at the modulated signal rate. The values of V_{vco} (which are the demodulated outputs) are constant voltages for each frequency. Fig 2.4.2 indicates the simulation results of the demodulated FSK signal for an input RF 2.3GHz signal, which is digitally modulated by a 5MHz BFSK signal. The data rate is 5 Mbps with a lock-in time of approximately 50ns as shown in Fig. 2.4.2. ADS simulation predicts a data rate as high as 10MHz.

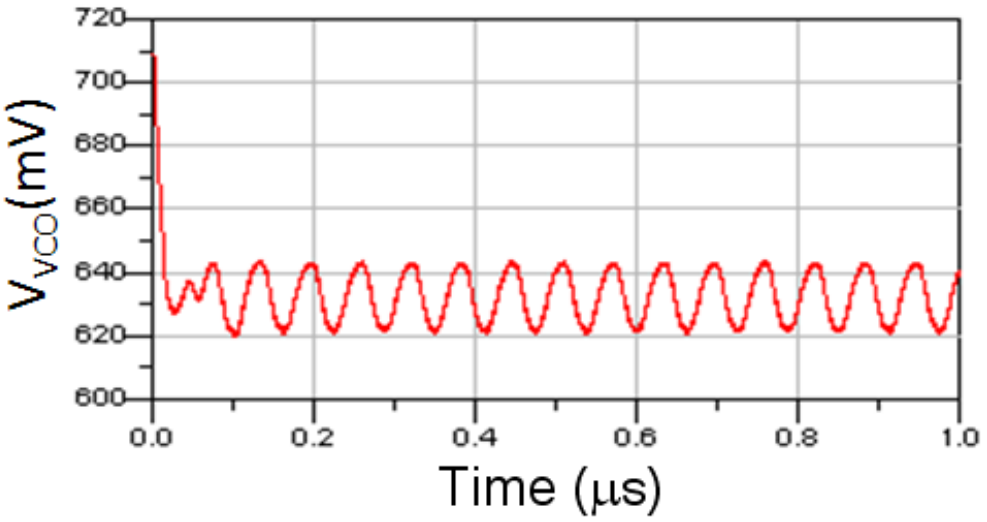


Figure 2.4.1: Simulated demodulated FM signal with 16MHz modulation at 2.3GHz input signal.

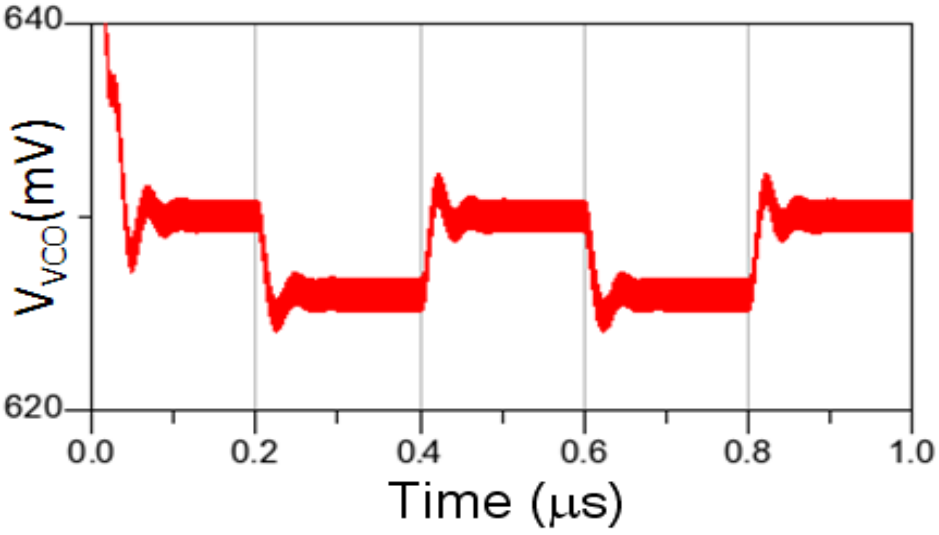


Figure 2.4.2: Simulated demodulated BFSK signal with 5MHz modulation at 2.3GHz input signal.

An matching network can be placed at the interface between the antenna and LNA, and at the interface of the LNA and the mixer to boost the input voltage and improve

system sensitivity. On-chip inductors can be used as part of the matching network to improve sensitivity with high system integration.

It is worthwhile to point out that the power consumption of the oscillator can scale down as the CMOS technology scales down. The power consumption of the oscillator is described by equation 2.3.10. For a fixed frequency and supply voltage, the process scaling trend offers smaller capacitance of MOSFETs and thus smaller oscillation power for ring oscillators. For example, by using 90nm technology, we expect the power consumption of the PLL to be only 25% of the current power consumption.

2.5 Receiver Selectivity

Interference sources (image interference, out of band interference) degrade receiver performance. These interferences need to be removed by different techniques in different receiver architectures. Super heterodyne architectures make use of the superior phase noise of a LC oscillator to greatly depress the interference signals. Figure 2.5.1 demonstrates this suppression process. In this architecture, the signal and the interference mix with the oscillator signal. The RF signal multiplies the oscillator signal to generate the correct baseband signal, which lies within the pass bands of the baseband filter. However, the interference multiplies with the oscillator signal and generates a down-converted baseband signal that is outside of the pass bands of the baseband filter and is thus removed by the baseband filter. However, the multiplication of the image interference with the oscillator signal also lies in the pass band of the baseband filter. Image frequency interference therefore still exists as a problem and needs to be removed by different architectures such as direct conversion or Weaver receiver architectures.

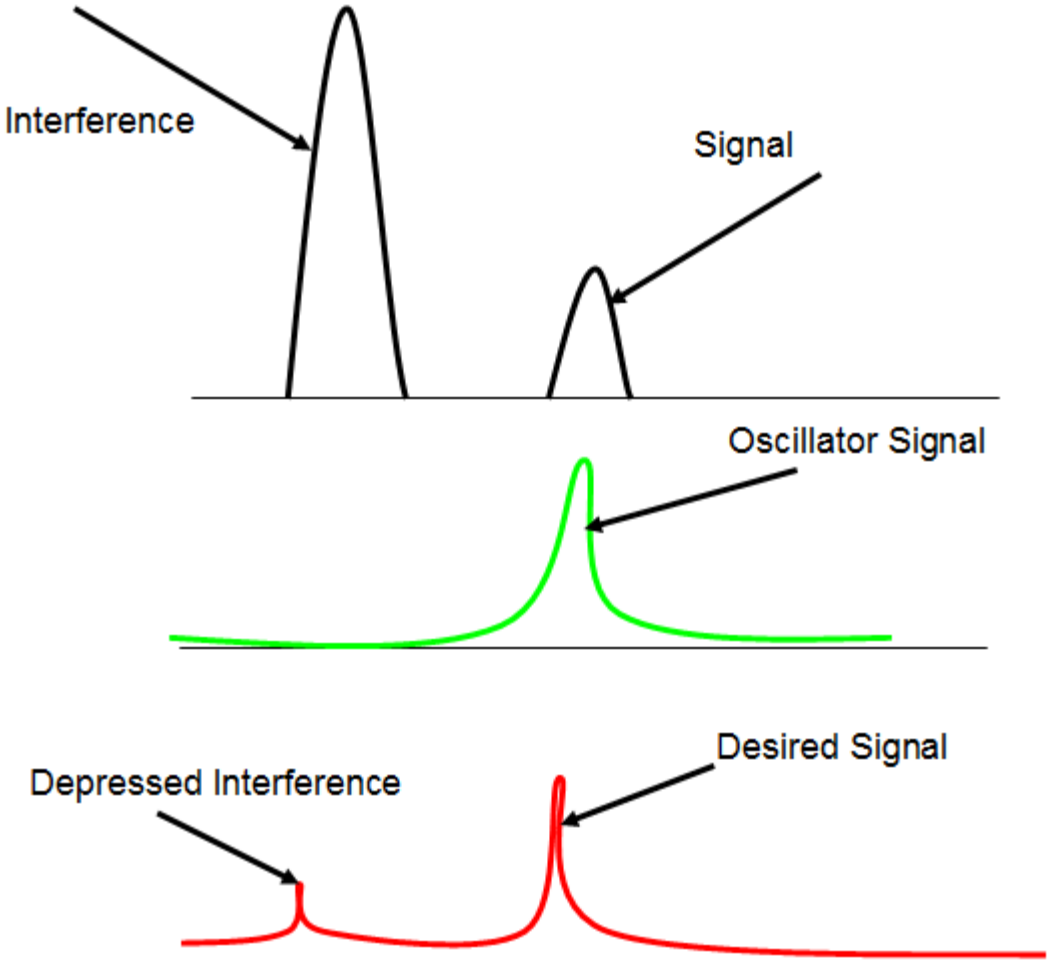


Figure 2.5.1. Interference depression in direct conversion and super heterodyne architectures.

In the PLL based receiver architecture, the interference can drive the PLL into unlocked conditions. Our simulation shows that the PLL can track the input FSK/FM signals when the interference is less than 20% of the signal. Beyond this limit, the PLL loses track of the input signal and thus begins to malfunction. The PLL based architecture does have some weak anti-interference abilities compared with OOK receiver architecture. When the interference signal frequency is away from the desired signal frequency, the PLL RC

filter can filter out the down-converted interference signal and provide some kinds of interference suppression ability. The simulation shows that when the signal is 10 times the RC poles, the receiver can reject an interference signal with twice the amplitude of the input signal.

The PLL based receiver architecture has better interference characteristics compared with the OOK architecture, which does not have any interference rejection capabilities in the demodulation process.

In the super-regenerative architecture, selectivity (anti-interference capability) is achieved through selectivity of the RLC tank, which attenuates the signals away from the resonant frequency. The feedback loop also contributes some selectivity capabilities. In general, the super-regenerative architecture has better selectivity than either OOK or PLL based receiver architectures.

2.6 Receiver Sensitivity

For a receiver system, the system sensitivity is limited by the noise level of the system. The system sensitivity at room temperature can be described by the following equation:

$$P_{min} = -174\text{dBm/Hz} + NF + 10\log B + SNR \qquad 2.6.1$$

Where P_{min}, NF, B and SNR are the system sensitivity, system noise figure, channel bandwidth, and signal to noise ratio. The -174 dBm/Hz component in equation 2.7.1 comes from the white noise at room temperature in 1 Hz. The system sensitivity is generally better at lower temperatures because the thermal noise is lower at lower temperatures.

In the PLL based architecture, the sensitivity is limited not only by the noise level of the system, but it is also limited by the unique characteristics of the PLL based architecture.

As the input signal voltage decreases, the mixer output voltage variation decreases. When the PLL locks onto 2.2GHz, the phase difference between the oscillator and the input signal is zero. When the input signal frequency is shifted away from the designated preferred channel of 2.2GHz, the control voltage of the VCO needs to be either increasing or decreasing depending on the input signal level.

However, the output voltage variation of the mixer, which is the control voltage of the VCO, is proportional to the input RF signal voltage. As the RF signal voltage decreases, the variation range of the VCO control voltage decreases as well. A smaller variation of VCO control voltage corresponds to a smaller VCO lock-in range. When the input signal voltage is too small, the VCO control voltage cannot reach the corresponding voltage to push the VCO frequency to the same signal frequency. The PLL thus fails to demodulate the signal. This PLL based receiver architecture has an extra limitation due to the sensitivity.

The control voltage range of the VCO achieves its maximum voltage when there is a 90 degree phase difference between the LO and RF signals. As the input signal voltage increases, so does the variation of the mixer output voltage. The PLL thus adjust the phase difference of the input RF signal and the tracking VCO signal to maintain the same VCO control voltage. In this architecture, as long as the PLL works, the output voltage has the same amplitude automatically, regardless of the input signal amplitude. The PLL demodulator automatically adjusts the phase difference to maintain the same output voltage as long as the PLL tracks the input signal.

2.7 Receiver Measurement

The prototype chip has been fabricated in a 0.13 μm single-poly eight-metal standard CMOS process. Fig. 2.7.1 shows the microphotograph of the 1x1 mm^2 fabricated chip. A typical common source cascode LNA is included in the die to explore the PLL's application as a wireless receiver. The PLL is fully integrated and its core occupies a 75x45 μm^2 chip area. The total power consumption of the PLL portion of the receiver is only 0.26 mW.

The closed loop PLL spectrum has been measured by a MXA N9020A spectrum analyzer and an Agilent E8267D signal generator. Fig. 2.7.2 shows the closed loop PLL spectrum after the buffer circuit for an input signal@2.232GHz. The measured amplitude agrees with simulated signal amplitude (-15 dBm). The locked VCO output spectrum has phase noise of -95 dBc/MHz@200KHz.

For the VCO, a one-stage common drain buffer is included for impedance matching to facilitate measurement. In Fig. 2.3.3 the oscillator section shows the tuning characteristics of the VCO. The measured tuning range is more than 600 MHz. The power consumption is 207 μW.

Fig. 2.7.4 shows the measured demodulated signal of a 2.23 GHz FM signal with 1 MHz modulation with a modulation index of 8 (see equation 8). Fig. 2.7.3 shows the demodulated signal of a 2.23 GHz signal with 100KHz modulation. The demodulated signal can be seen clearly at the top of the oscilloscope screen; the bottom of the screen shows the signal after a 1 MHz low pass filter. Fig. 2.7.5 shows the PLL central frequency as a function of the mixer control voltage (V_{ctrl}) (left y-axis). This shows that the PLL can track signals continuously from 1.62 GHz to 2.49 GHz by varying the phase-

detector control voltage (V_{ctrl}). Fig. 2.7.5 (right y-axis) shows the PLL tracking frequency range as a function of phase-detector control voltage. For a fixed V_{ctrl}, the lock-in range decreases as the bias voltage moves away from the optimized bias voltage (0.7 V). This variation is attributed to the oscillator and phase-detector, which have their best performance when V_{ctrl} is in the range of 0.65-0.75 V. The measured result shows the maximum lock-in range is 90 MHz, which is close to the pole of the PLL loop filter. This also agrees with the simulation result as stated in sub-chapter 2.4. The PLL can track a signal from -67 dBm to -25 dBm with an on-chip LNA. However, this is highly dependent on the LNA characteristics and can be improved by LNA gain and power optimization. The PLL based architecture weakly suppresses out of band signals through the mixer and PLL loop filters. Suppression of interferance could be increased at the price of lock-in frequency range.

Table I summarizes and compares the PLL performance with that of other recently published PLLs [Tak2005][Hu2009][Krishnaswamy2008]. We exclude the power consumed by frequency dividers in other works to achieve a consistent comparison. We also compare this receiver with other low power receiver designs such as OOK receivers [Daly2007] and super-regenerative receivers [Chen2007] in Table II. The present work achieves a lower energy per bit compared with the OOK receiver [Daly2007] with comparable sensitivity. While the super-regenerative design [Chen2007] has much higher sensitivity than our receiver, our topology uses significantly less energy per bit, which attributes to the efficient power utilization of our mixer and VCO; this also indicates the potential design tradeoff between power and sensitivity.

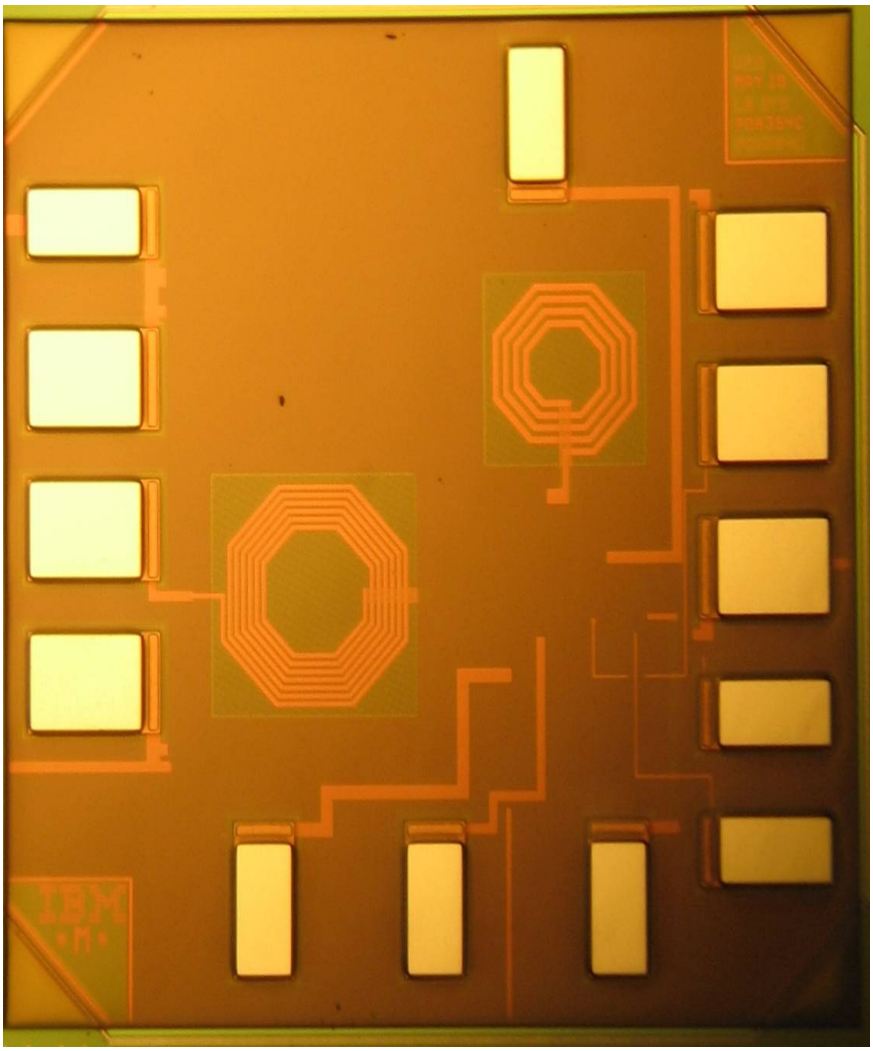


Fig. 2.7.1: Die photo of the PLL test chip integrated with a LNA (1 mm^2).

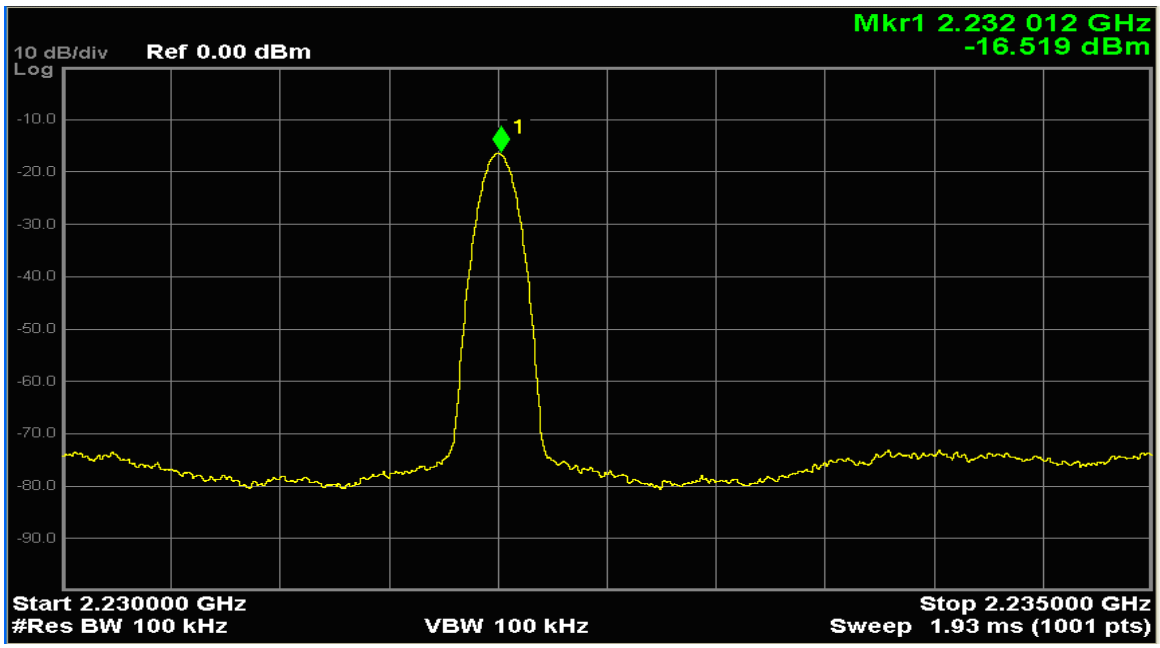


Fig. 2.7.2: PLL closed loop spectrum. (Horiz. 500 KHz/div; Vert. 10dB/div)

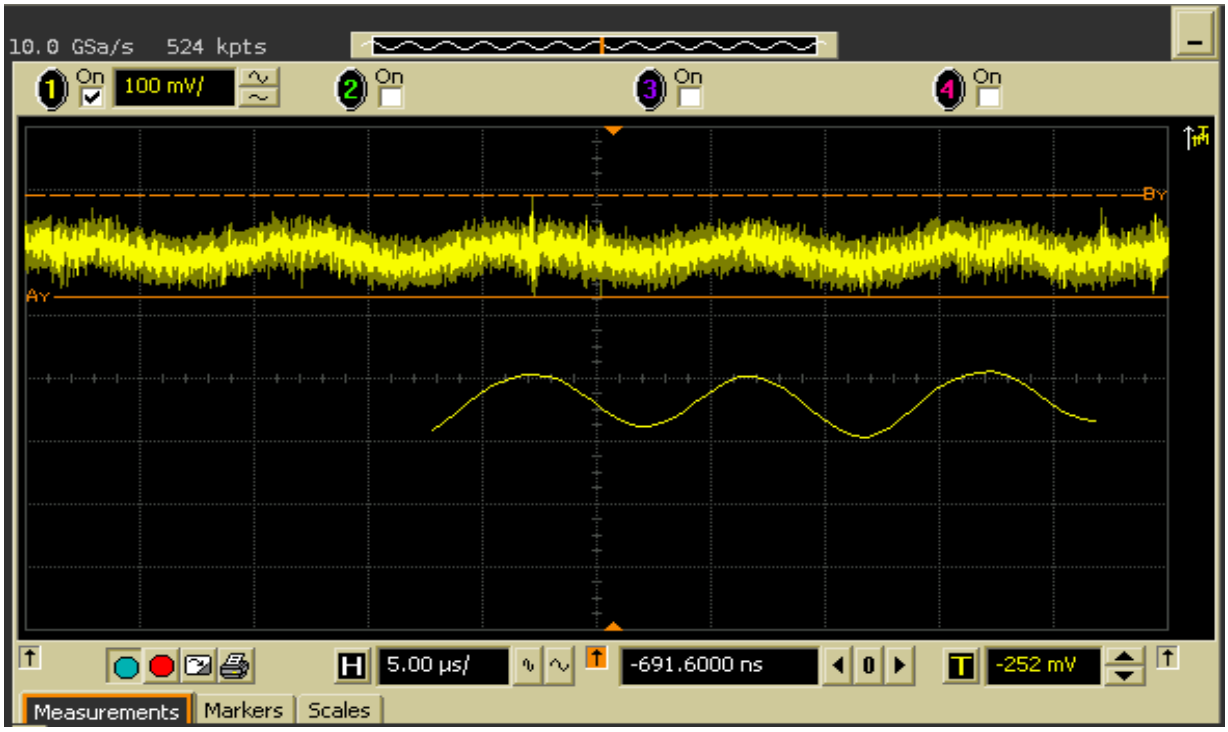


Fig. 2.7.3: Measured waveform of demodulated PLL for 100KHz modulation with 8MHz derivation@2.3GHz. Upper: measured PLL output. Bottom: measured PLL output after a 1MHz oscilloscope digital filter. (Horiz. 1 µs/div; Vert. 10 mV/div (V_{p-p}10mV))

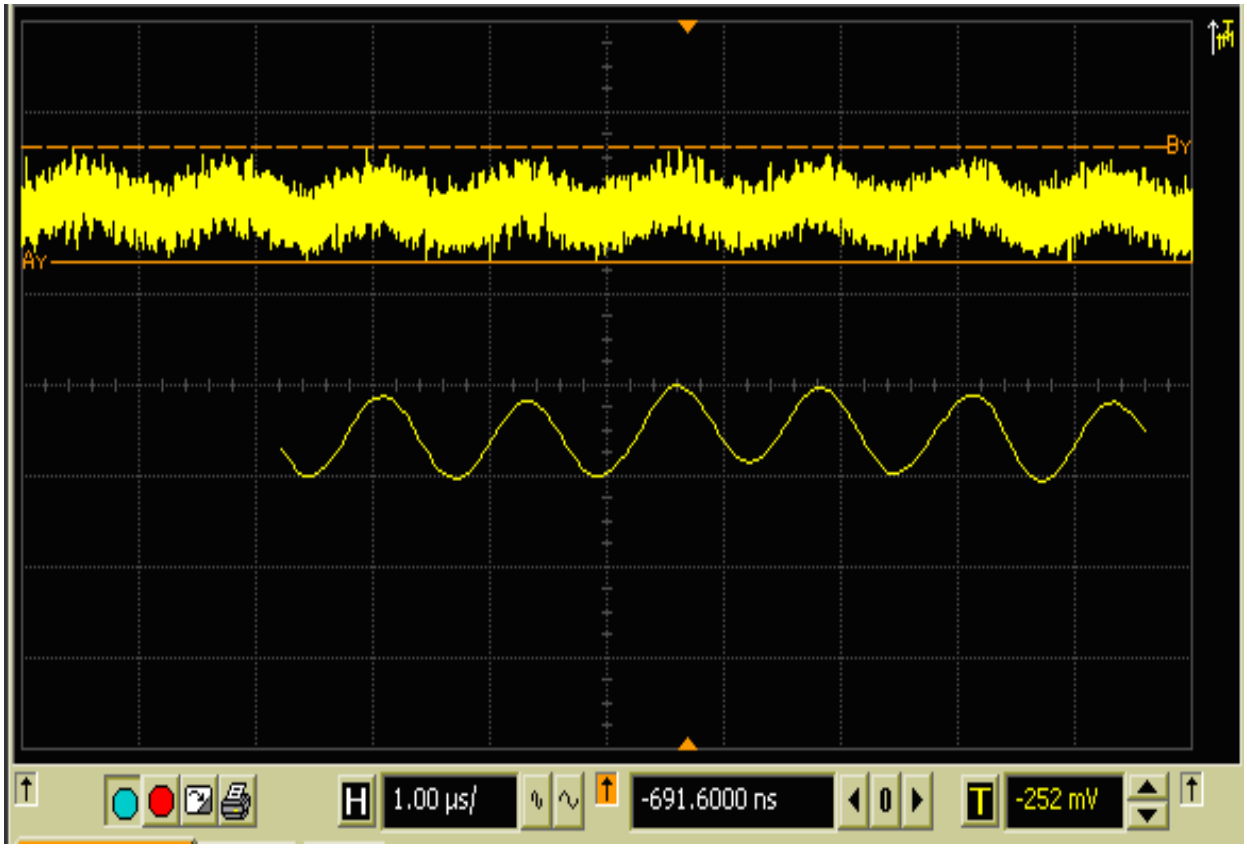


Fig. 2.7.4: Measured waveform of demodulated PLL for 1MHz modulation with 8MHz derivation@2.3GHz. Upper: measuredPLL output. Bottom: measured PLL output after a 1MHz oscilloscope digital filter. (Horiz. 1 µs/div; Vert. 10 mV/div ($V_{p\text{-}p}$10mV))

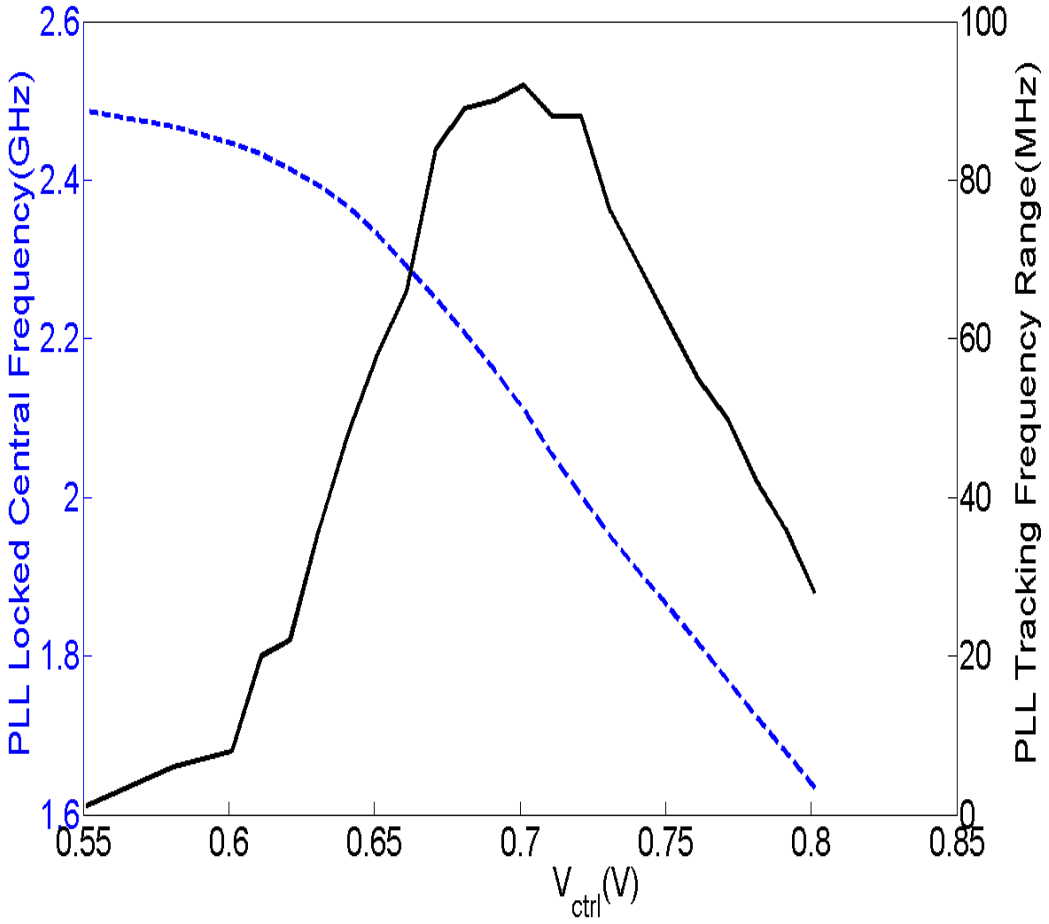


Fig. 2.7.5: Left y-axis: Measured PLL center lock frequency as a function of control voltage (blue dotted line). Right y-axis: Measured PLL tracking range as a function of control voltage (black solid line).

Table I
PLL Performance Comparisons

	[Tak2005]	[Hu2009]	[Krishnaswamy2008]	This Work
Technology	0.18µm	0.13µm	0.18µm	0.13µm
Supply	1.8V	1V	1.2V	1.2V
Frequency	6.3GHz	1.575GHz	24GHz	2.3GHz
Power	14.8mW**	0.56mW**	0.52W	0.26mW
Lock range	N/A	1.35MHz	N/A	600MHz
Phase noise	-104dBc/Hz @200KHz	-120dBc/Hz @200KHz	N/A	-95dBc/Hz @200KHz

**Frequency divider power not included to allow for equitable comparisons

Table II
Receiver Performance Comparisons

	[Daly2007]	[Chen2007]	This Work (No LNA)
Center Frequency	916.5 MHz	2.4 GHz	2.3 GHz
Sensitivity	-37 dBm	-90 dBm	-35 dBm
Power	0.5 mW	2.8 mW	0.26 mW
Data Rate	1 Mbps	500 Kbps	1 Mbps*
Energy per Bit	0.5 nJ	5.6 nJ	0.26 nJ
Interference Suppression Ability	None	Moderate	Weak

*limited by measurement equipment

2.8 Conclusion

In this chapter, we have discussed design procedures for a low power phase locked loop and its applications as a receiver. The PLL requires a mixer as phase detector and a voltage controlled oscillator, as well as other supplementary circuits such as low pass filters.

The power limitations of the Gilbert cell based mixer have been noted. A new mixer topology is given here with detailed analysis for use in ultra-low power applications to meet the low power requirements of WSNs. We then compared the LC oscillator

topology with the ring oscillator topology. Our analysis shows that the power limitations of the LC oscillation mainly arise from its lossy on-chip inductors. We have discovered that a LC oscillator topology cannot meet the 100uW power level requirement of WSN applications because of these lossy on-chip inductors. The power limitation for LC oscillations cannot be improved by utilizing CMOS scaling trends either. A current starving ring oscillator is designed as the VCO for this work with 200 uW power consumption. The power consumption of the VCO can be further reduced with CMOS downscaling to allow for oscillations using even lower power consumption. The contribution can be summarized as follows:

- Design and analysis of an ultra-low power mixer
- Analysis of the power limitations of the LC oscillator topology
- Design of a low power current starving ring oscillator
- A FM/FSK receiver using PLL as a demodulator
- The power consumption of the PLL can be scaled down as the CMOS technology scales down

Chapter 3: Integrated OOK Transceiver with On-Chip Voltage Regulator

3.1 Introduction

Smart Dust Systems (SDS) are ad-hoc distributed network infrastructures which sense the environment, communicate between each other, make decisions, and send back the collected data to a data base-station. There is a large potential for applications of such devices, such as health monitoring systems, environment sensing systems, and temporal wireless services [Salter2007B]. The distributed network uses many wireless nodes; each node is composed of an antenna, a transceiver, a voltage regulator, a battery, and an application specific integrated circuit (ASIC) as a controller. Low cost and low power are two major requirements for successful SDS applications.

Wireless sensor networks (WSN) demand integrated transceiver solutions. Having integrated power management is one aspect of managing functionality on a low power source, and this may include solutions such as voltage regulators with high efficiency. More generally, the transmitter can typically be turned on only when necessary by the digital control circuits. However, the receiver still has to be on at all times to listen to other nodes. In this chapter, we describe a highly integrated transceiver system using standard CMOS technology that meets low power/cost requirements. The unique aspects of these transceivers are their high integration of power management circuits along with a low power transceiver. The system includes an On-Off Keying (OOK) receiver, a transmitter, RF/DC switches, and an on-chip low dropout voltage regulator (LDO) which

provides comprehensive on-chip biasing voltages. The receiver consumes low power while obtaining a high sensitivity by using a Villard voltage doubler with a voltage transformer as a demodulator to significantly improve OOK demodulation sensitivity. The low noise amplifier (LNA) is mandatory for low sensitivity receiver applications. The LNA of the receiver is operated in the sub-threshold region of its MOSFETs to achieve maximum power per gain efficiency. Those techniques lead to a complete, ultra-low power smart dust node, requiring less than 4mW with -60 dBm sensitivity to work within a TDMA network [Chen2008].

OOK receiver architecture is widely chosen for low power applications [Daly2007] due to its simplicity and ease of implementation. Peak detectors are generally implemented in OOK receivers as demodulators. However, one of the major disadvantages of the usage of the peak detectors as demodulators is that there are huge voltage conversion losses along with the signal demodulation, especially in the case of weak input signals, since the demodulation relies on difficult-to-turn-on rectifier diodes. The high conversion losses impose significant voltage/power gain requirements on previous low noise amplifier (LNA) stages since the input RF signal needs to be amplified to a detectable signal level for the peak detector in order to be demodulated. However, LNAs are the most power hungry components in an OOK receiver and commonly consume many milliwatts of power. It is thus necessary to reduce the power conversion losses of the peak detector.

In this work, we address the power and sensitivity tradeoff in two ways: first, the LNA operates at sub-threshold voltage to optimize its gain to power ratio, thereby requiring less power than LNAs where MOSFETs work at saturation regions for the same power

gain. In addition, a voltage doubler circuit and voltage transformer circuit have been used in the demodulation circuit to achieve significant sensitivity improvement compared with the commonly used peak detector without extra power consumption.

This chapter consists of four sections. Section II presents the transceiver system and the interface between the wireless transceiver and the ASIC control unit circuit. Section III describes the power management circuit design in this low power mobile transceiver system. Section III also describes low power receiver circuit techniques along with baseband amplifier design, switch circuits, and the integration between the transceiver and the power management circuits. Section IV presents measured results for the integrated receiver. Section V summarizes the work and provides conclusions.

3.2 Integrated Transceiver System

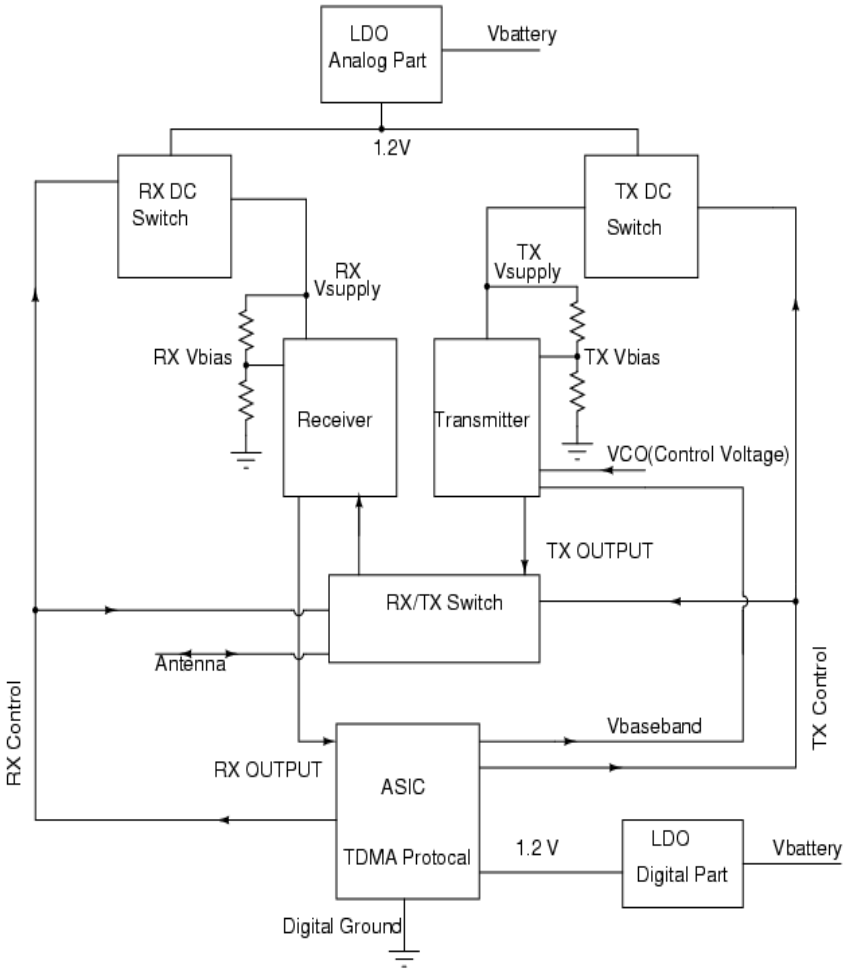


Figure 3.1. Block diagram of the transceiver system and ASIC.

Figure 3.1 is the block diagram of one of WSN nodes. It consists of an integrated transceiver, power management circuits, an application specified integrated circuit (ASIC), and a battery. The transceiver communicates (transmits/receives) wirelessly among different nodes. The power management circuits provide the biasing voltages for the very voltage-sensitive RF and analog circuits as well as digital units. The ASIC implements the time division multiple access (TDMA) protocol [Shen2008] for communication among different nodes. It also switches the transmitter off when necessary as a part of the power management solutions.

The arrow directions in Figure 3.1 represent the direction of signal flows. The battery powers the whole system including the transceiver, the switches, the digital ASIC, and the voltage regulators. The ASIC generates signals to control RX/TX states based on the received information. RX/TX control signals as shown in Figure 3.1 control the operational states of the transceiver through the transceiver RF/DC Switches. The transceiver can work in three states: receiving state (RX on/TX off), transmitting state (RX off/TX on), and quiescent state (RX off/TX off). In the receiving state, the switches turn on the receiver power rail as well as the biasing voltages of the receiver. It also switches off the power rail for transmitter to turn it off too. The receiver demodulates the input signal from the antenna and sends out the demodulated signal (RX OUTPUT) to the ASIC to interpret the information and make decisions. The ASIC makes decisions based on the receiver signal information to either turn on/off the transceiver. In the transmitting state, the switches turn on the supply voltage of transmitter as well as the necessary biasing circuits for the transmitter while turning off the receiver power supply. The transmitter mixes the low frequency information (1MHz) with the voltage controlled oscillator (2.2GHz), amplifies the signal to 0 dBm power level using the power amplifier, and radiates the signal to other nodes through an antenna.

3.3 Transceiver Circuit Designs

3.3.1 Integrated Voltage Regulator

3.3.1.1 CMOS Based Voltage Reference Circuit

Power management is an essential feature of mobile devices due to the limited available power, which is in turn the result of their small size. Mobile applications also

require accurate and stable voltage supplies as well as biasing voltages over the operational ranges of voltage, temperature, and load due to the extremely voltage sensitive analog and RF circuits.

Voltage independent solutions are necessary due to the variation of battery output voltages with time. Temperature independent voltage solutions are mandatory because mobile devices need to work over a range of temperatures from -35 to 85 C. For example, the variation in biasing voltage of the LNA causes different voltage gains and noise figures. A high gain may drive the LNA into the non-linear P1dB region and thus unnecessarily consume high power. A low gain for the LNA may degrade the sensitivity and cause malfunction of the device. Further, the power consumption of mobile devices varies since the transceivers need to work at different states of activity that may consume different power. For a fixed supply voltage, the power variation causes load variation of the voltage regulators. In summary, power management circuits need to provide a solution to guarantee the functionality of mobile devices under this large variety of conditions.

Figure 3.2 shows the schematic of a commonly used low dropout voltage regulator [Teel]. The voltage reference circuits use temperature compensation methods to provide a stable voltage over a temperature range from -30 C to 85 C to fully cover the temperature variation of mobile devices. The voltage reference circuits also provide constant voltages that are independent of the battery voltage variations. The band-gap voltage reference circuits can be implemented in a CMOS process using the parasitic vertical bipolar junction transistors (BJTs) [Leung2002]. Recently, a pure CMOS based voltage reference

circuit [Leung2003] has been implemented without using vertical BJT structure. We have implemented pure CMOS temperature cancellation techniques in this design.

Generally, the output of the voltage reference circuits needs to be connected to high impedance nets in order to function correctly. This cannot provide a load independent solution for mobile device applications. The load independent capability is instead provided by additional voltage regulator circuits using an op-amp and feedback networks as shown in Figure 3.2. The voltage regulator also makes use of the voltage and temperature independent reference voltage generated by the voltage reference circuits to obtain temperature and voltage independence. In this way, the voltage regulator provides a comprehensive power solution for mobile devices. Furthermore, in this design, we need an ultra-low power voltage regulator.

In the voltage regulator shown in Figure 3.2, the op-am senses the voltage difference between the reference voltage and the feedback voltage from the output. In other words, it amplifies the voltage differential (error) and uses the amplified voltage to control the voltage drop on the pass MOSFET to maintain a constant desired output voltage. The output voltage is always lower than the input battery voltage. The pass MOSFET needs to be a large size PMOS device in order to handle high current and also high signal.

The voltage regulator works as follows: when the output voltage is high, the error amplifier generates a high voltage to drive the pass FET into a high impedance state; It thus causes a high voltage drop in the pass FET and thus reduces the output voltage. When the output voltage is low, the error amplifier drives the pass FET into a low impedance state and thus increases the output voltage. The higher the gain is, the closer the output voltage is to the reference voltage. In order to achieve less sensing voltage

error from the error amplifier, the error amplifier gain needs to be high. However, as the voltage gain increases, the system becomes more unstable. There exists a tradeoff between the voltage accuracy, power consumption and stability of the system. A capacitor with a resistor in series is placed at the output of the voltage reference to improve the stability of the voltage regulator (phase margin) as shown in Figure 3.2. For the voltage regulator shown in Figure 3.2, since the current through the battery, the output node and the pass FET are the same, the maximum possible efficiency is limited by Equation 3.3.1:

$$\eta = \frac{P_{out}}{P_{in} + P_q} < \frac{P_{out}}{P_{in}} = \frac{I \times V_{DD}}{I \times V_{battery}} \leq \frac{V_{DD}}{V_{battery}} \qquad 3.3.1$$

Where P_q is the power consumption of the error amplifier and reference circuit in Figure 3.2.

In order to obtain high power efficiency, the voltage drop between the input battery voltage and output supply voltage needs to be as low as possible. In applications where a high voltage drop is necessary, a buck DC to DC voltage converter can be used to convert down the battery voltage to a level close to the required power rail voltages. A buck DC to DC converter can achieve over 90% DC to DC power conversion efficiency. A voltage regulator can generate a stable voltage with high efficiency by using the output voltage of the buck DC/DC converter.

The output voltage in Figure 3.2 is determined by the ratio of resistor R1 versus R2 as well as the reference voltage. This can be described by Equation 3.2:

$$V_{DD} = (1 + \frac{R1}{R2})V_{ref} \qquad 3.3.2$$

The voltage regulator performance is determined by the above characteristics, power consumption, and the costs. Line regulation defines how the capabilities of the voltage regulator vary with input voltage. Load regulation defines how the capabilities of the regulator vary with load. Load regulation is specified in units of μV/mA or ppm/mA. Thermal regulation defines how the regulator behaves as temperature varies. The chip area is often used as a matrix to evaluate the costs, as well. The resistors and capacitor values is chosen using the methodology in [Rincon-Mora].

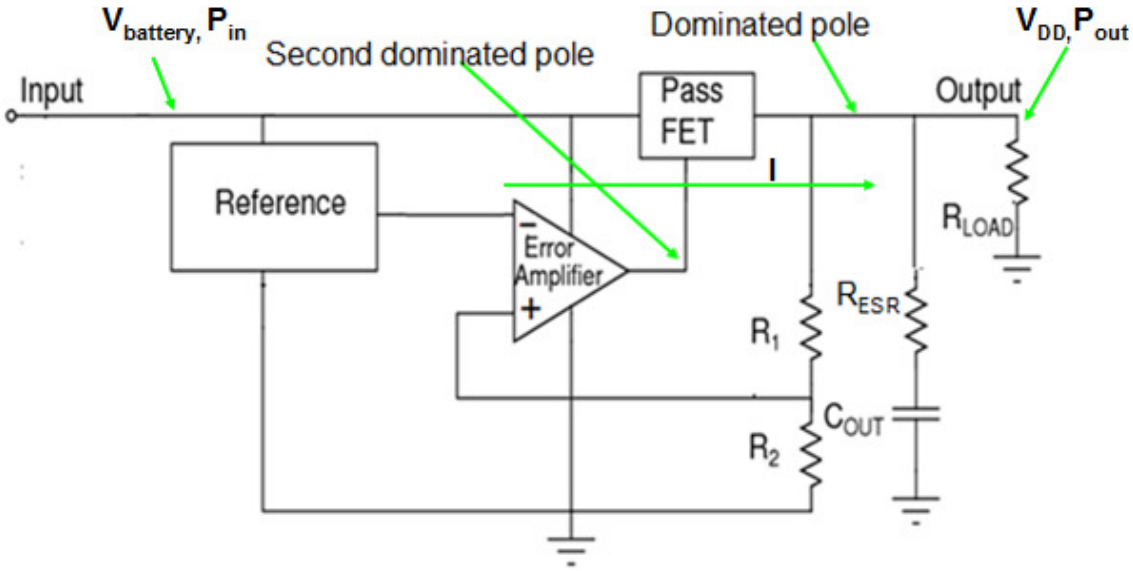


Figure 3.2 Schematic of a voltage regulator.

3.3.1.2 Low Drop-off Voltage Regulator Design

This paragraph presents a pure CMOS voltage reference with temperature compensation. Previous to this, designing a pure CMOS voltage reference has been an active area of research. The IBM process used for chip fabrication offers two different kinds of oxide thickness for CMOS devices: a type of thick oxide MOSFET as well as a type of thin oxide MOSFET. Figure 3.3 shows the drain current as a function of the drain voltage for those two different types of MOSFETs. The MOS33 devices are the thick oxide transistor

devices. Figure 3.4 is the simulated drain current as a function of the drain voltage for the same size MOSFETs but for different oxide thickness. This shows that the MOS33 device has a lower current under the same biasing voltages compared with the thin oxide thickness MOSFET device of the same geometry. Moreover, the I-V curve of MOS33 device (drain current varies with voltage between the drain and the source) is closer to the square-law compared with the I-V curve of the thin oxide devices. It is desired that the MOSFET devices obey square law in order to generate a supply voltage independent current source using the topology in Figure 4.3.4 [Razavi2000]. A voltage independent current is used to generate a voltage-independent reference voltage in Figure 4.3.4; MOSFET33 devices are thus chosen to implement the voltage reference circuit in this design.

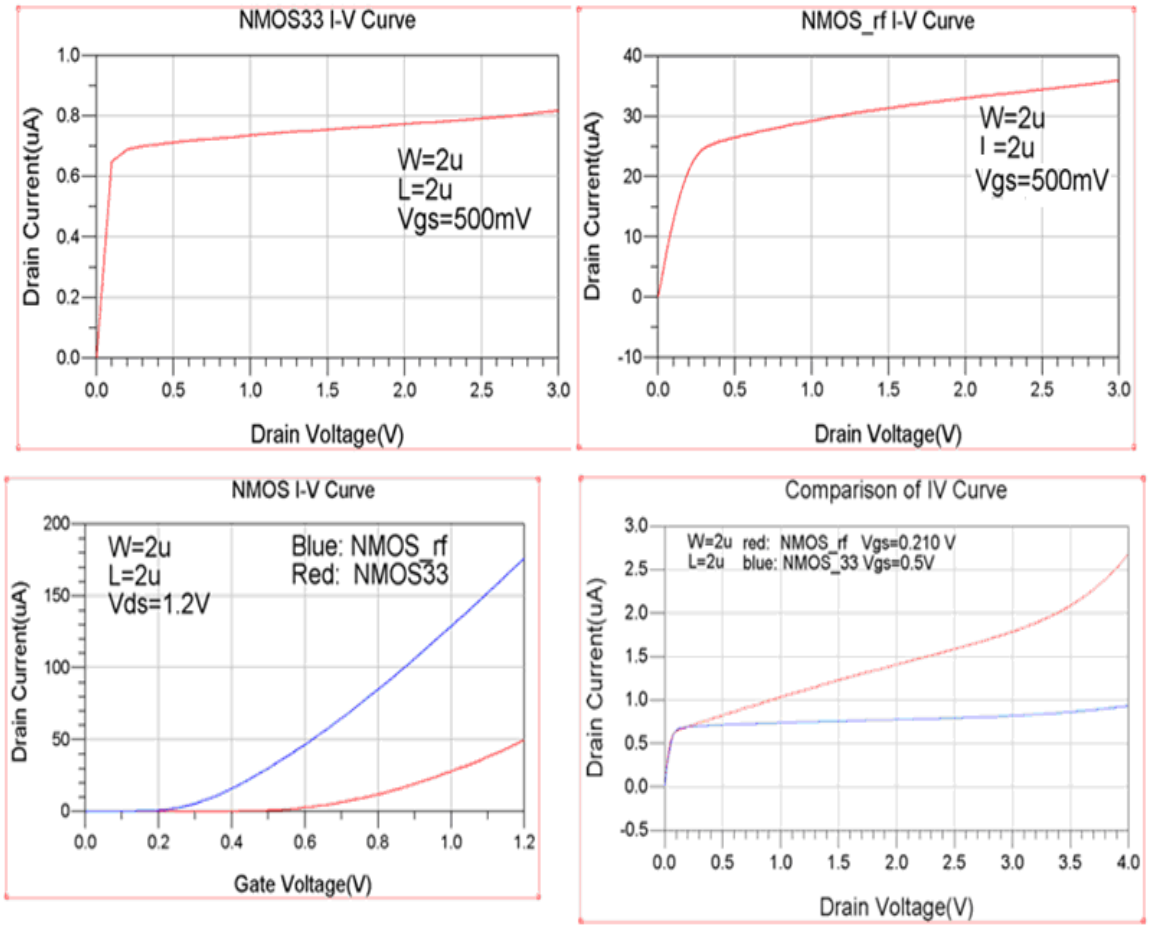


Figure 3.3 MOSFET IV curves.

Figure 3.4 is the schematic of the voltage reference circuit using pure CMOS devices [Leung2003]. It includes three parts: a start-up circuit, a supply voltage independent current source circuit, and a voltage reference circuit. The supply-independent current source circuit can generate either zero current or the designed circuit. The startup circuit is designed to drive the supply-independent current circuit into the designed current state instead of the zero current state. Briefly, when the supply independent current source is at zero current state: the voltage at gate M3 is equal to zero and at gate M2 is equal to VDD. Then, MS2 is on to drive the drain of MS2 to zero voltage and turns on MS3 to drive the

drain and gate voltage of M3 out of zero. The start-up circuit always drives the supply independent current circuit into the desired current states.

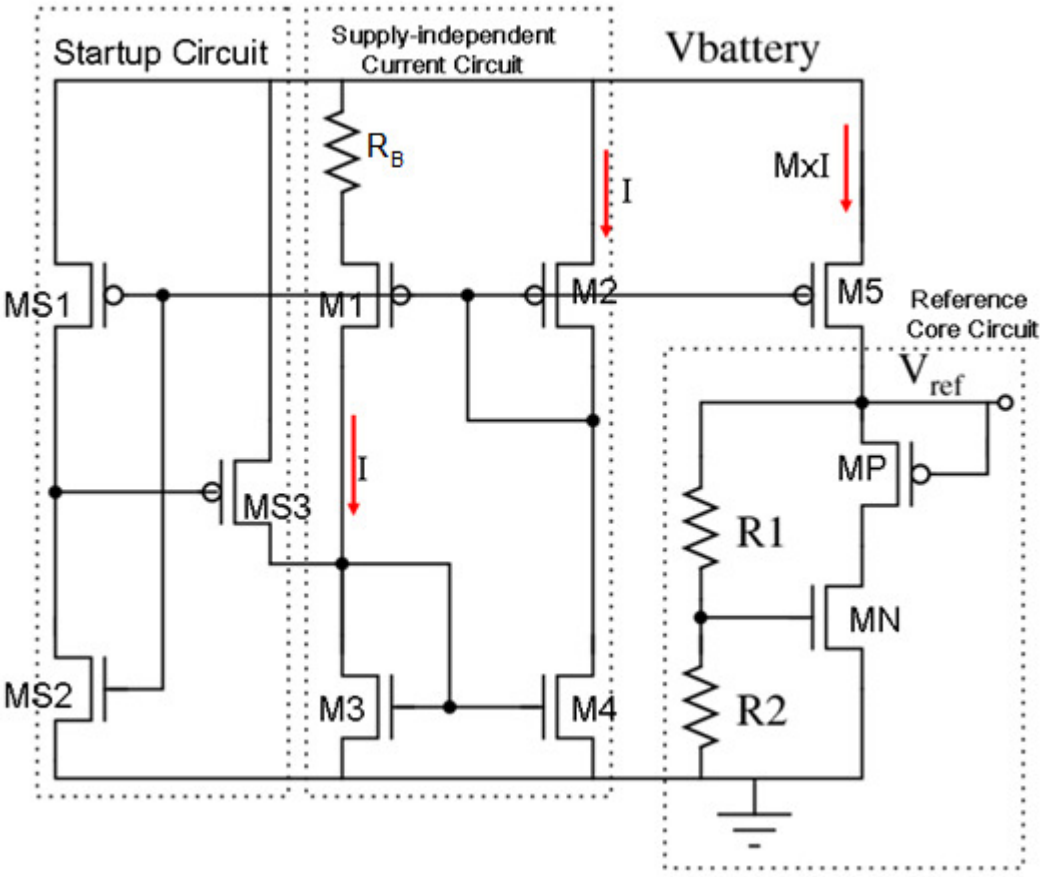


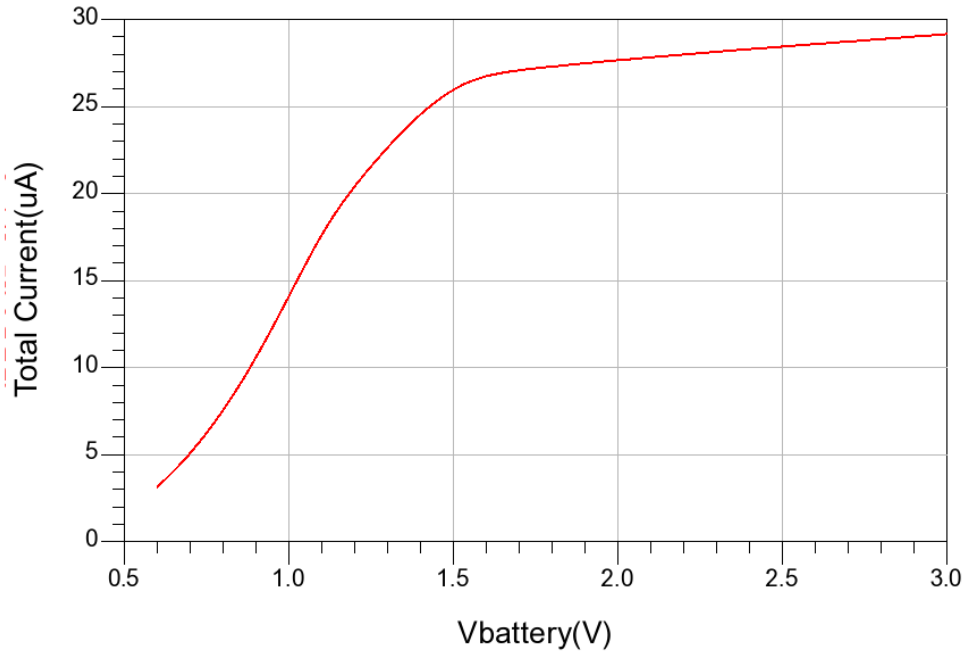
Figure 3.4 CMOS Voltage Reference.

M1, M2, M3, and M4 work together to generate the supply-independent current. The current is only a function of the value of the resistor (R_B) and the size ratio of transistor M1 and M2. The transistor M5 mirrors the supply-independent current source to generate a voltage independent current. Transistors MP and MN provide temperature cancellation by utilizing the characteristics of temperature trends for the threshold voltages of the NMOS and PMOS devices. The circuit obtains a supply and temperature independent

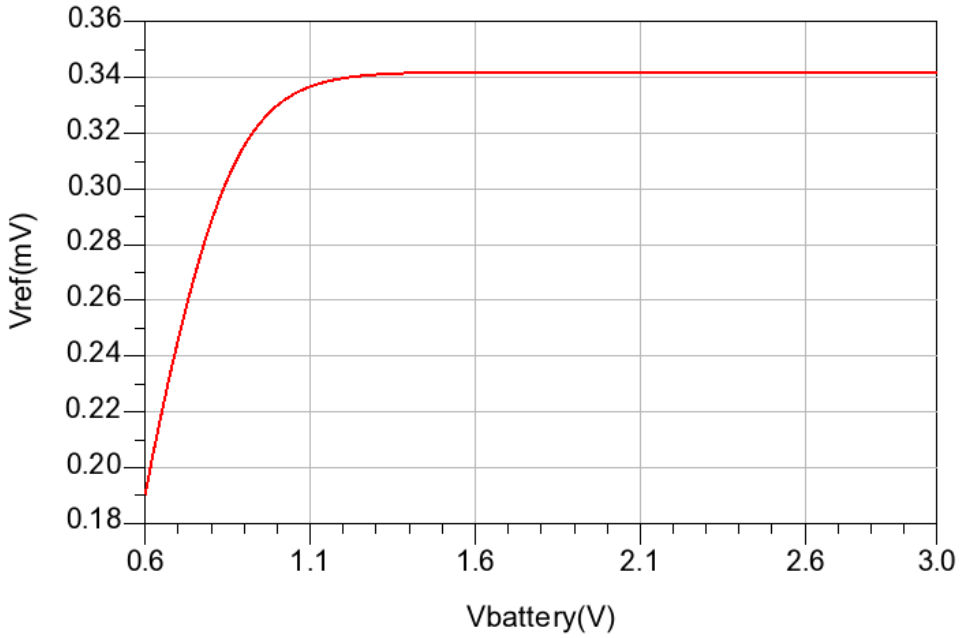
reference voltage. The supply and temperature independent output voltage is described by the following equation 3.3.3 [Leung2003]:

$$V_{\mathrm{Re}f} = [(1+\frac{R_1}{R_2})V_{thn} - |V_{thp}|] + \sqrt{I_B}.[(1+\frac{R_1}{R_2})\sqrt{\frac{1}{\mu_n C_{OX}(\frac{W}{L})_n}} - \sqrt{\frac{1}{\mu_p C_{OX}(\frac{W}{L})_p}}] \qquad 3.3.3$$

Figure 3.5 (a) shows simulation results of the current (power consumption) varying with battery voltages of the designed voltage reference circuits. The current varies from 18 to 28 uA as the battery voltage varies from 1.1 to 3.0 V. Figure 3.5 (b) shows the simulation of the battery voltage dependency of the output voltage. It shows that the output voltage stays constant as the battery voltage varies from 1.1 to 3.0 V. Figure 3.6 shows the simulated temperature dependency of the reference voltage. As the temperature varies from 0C to 85C, the reference voltage obtains a maximum 1% variation.



(a)



(b)

Figure 3.5 (a): Current varies with battery voltage. (b): Reference voltage versus input voltage.

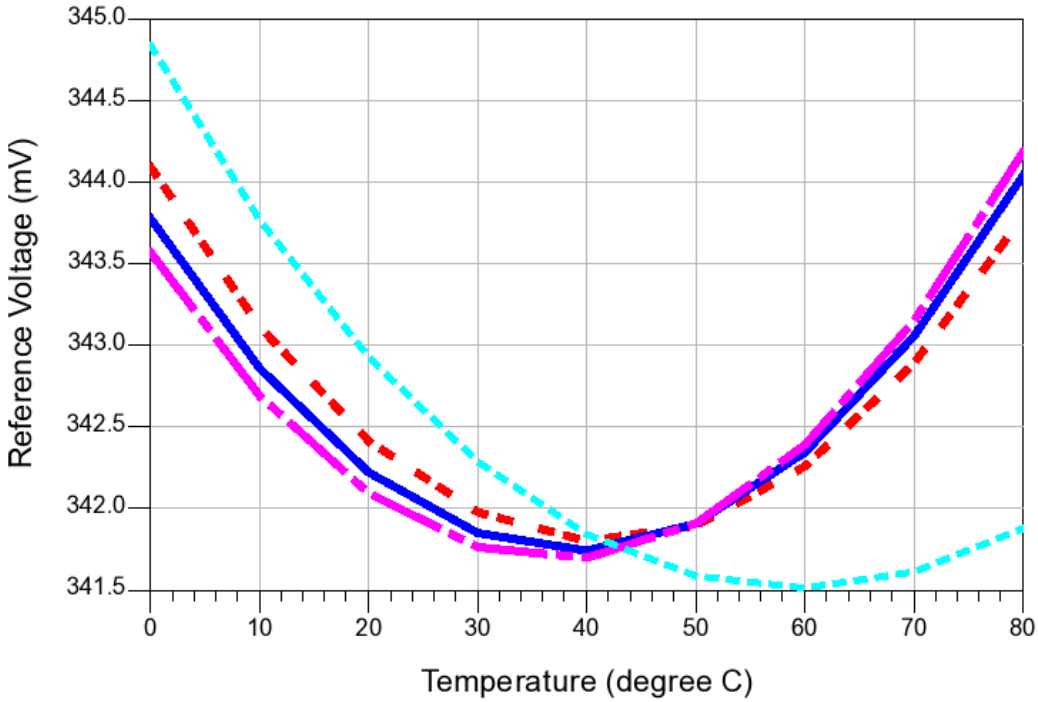


Figure 3.6: Reference voltage varies with temperature. Light blue: Vds=1.4V; Pink: Vdc=3V; Blue: Vdc=2.6V; Red: Vdc=2V.

Figure 3.7 is the schematic of the designed error amplifier. It is a two-stage amplifier: a differential amplifier followed by a common source amplifier. Both amplification stages use active loads to avoid large resistors and thereby reduce the chip area. The voltage gain of the amplifier is controlled by the current source, while the current source is supply voltage independent as shown in Figure 3.7. The start-up circuit is used to reduce the start-up time of the designed LDO. The reference voltage is connected to the high impedance net Vin since it does not have DC current (infinite DC load impedance).

Figure 3.8 (a) shows the simulated LDO output voltage for different battery voltages. It shows that the LDO generates a stable 1.2V for the battery voltage range of 1.35 to 3.3 V. Figure 3.8 (b) indicates the simulated LDO's output voltages for different loads. It shows that the voltage regulator provides a constant 1.2 V output voltage for different loads from 100 to 1000 Ohm. The load range is between 100-1000 Ohm which corresponds to a power consumption range from 1 to 10 mW under a 1.2 V voltage supply.

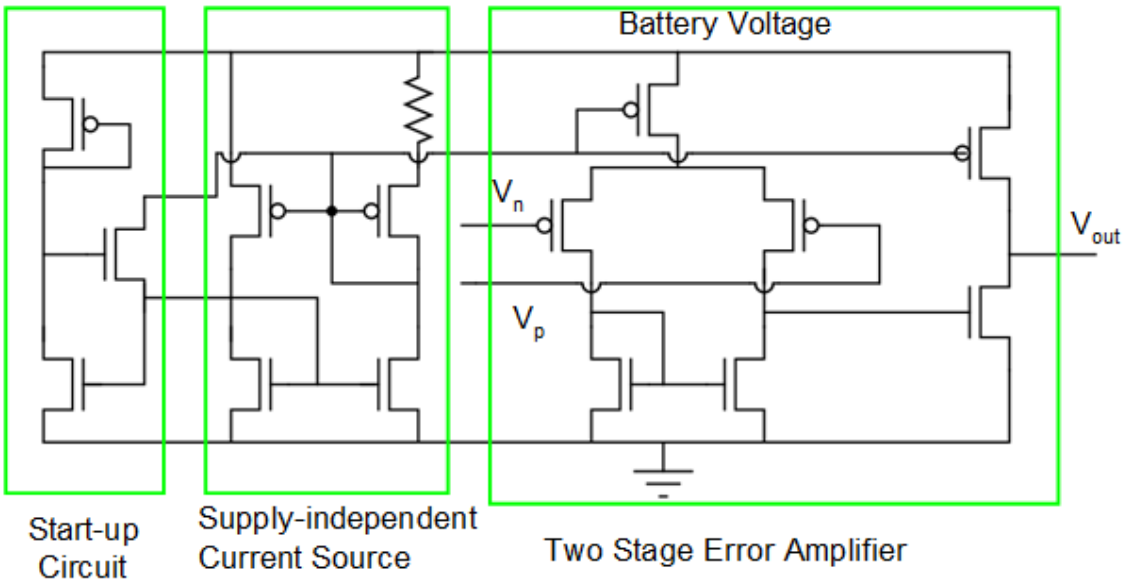
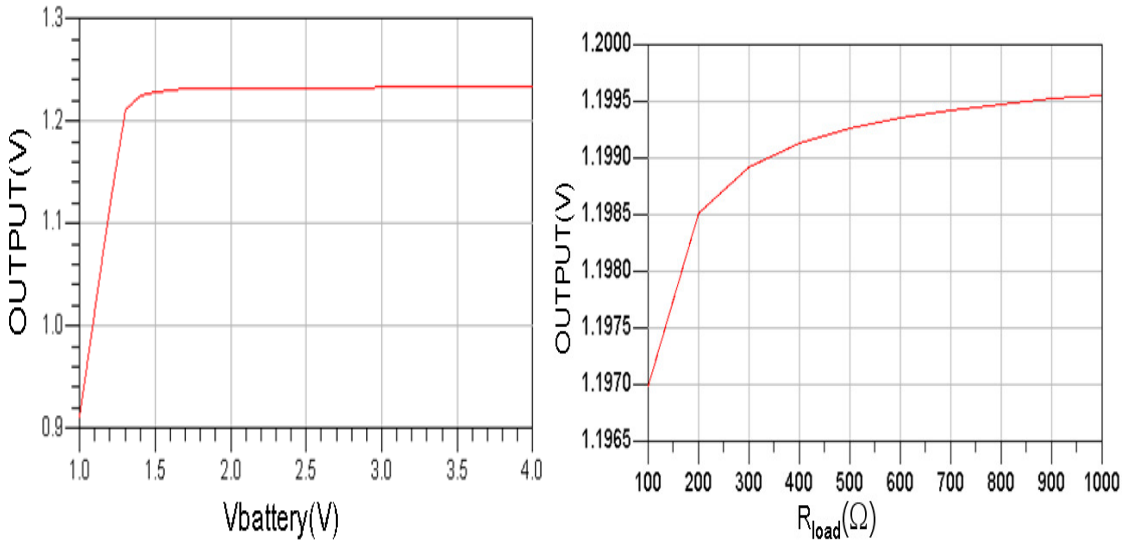


Figure 3.7 Error amplifier.



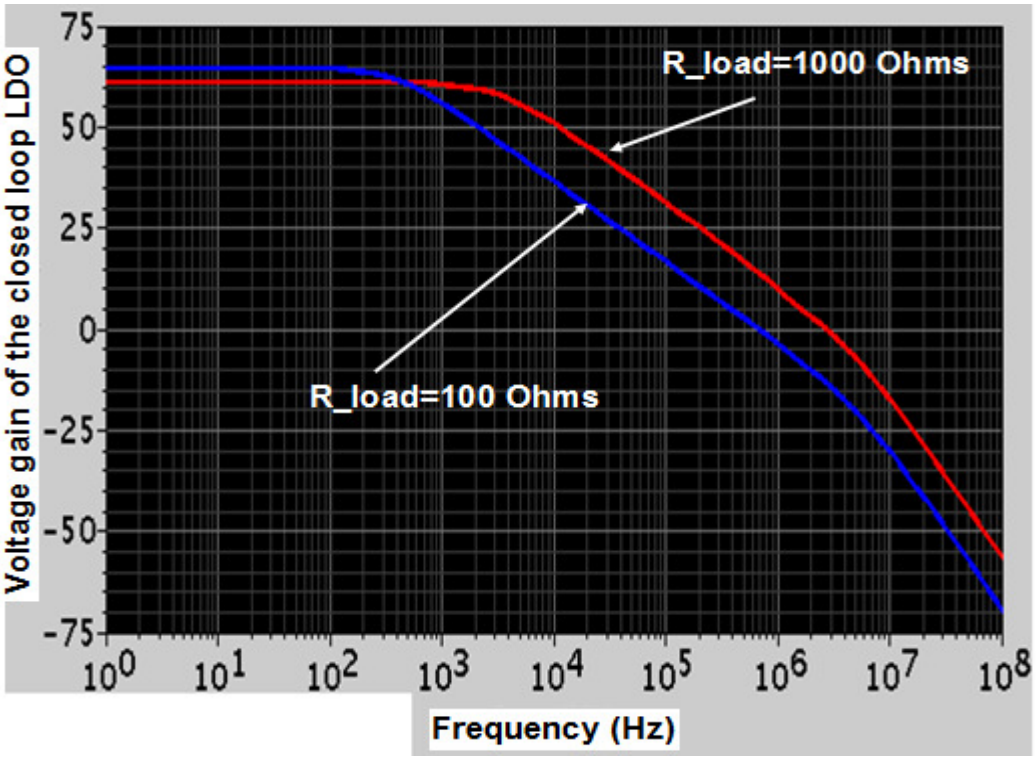
(a) (b)

Figure 3.8 (a): Output voltage as a function of input voltage. (b): Output voltage as a function of load resistor.

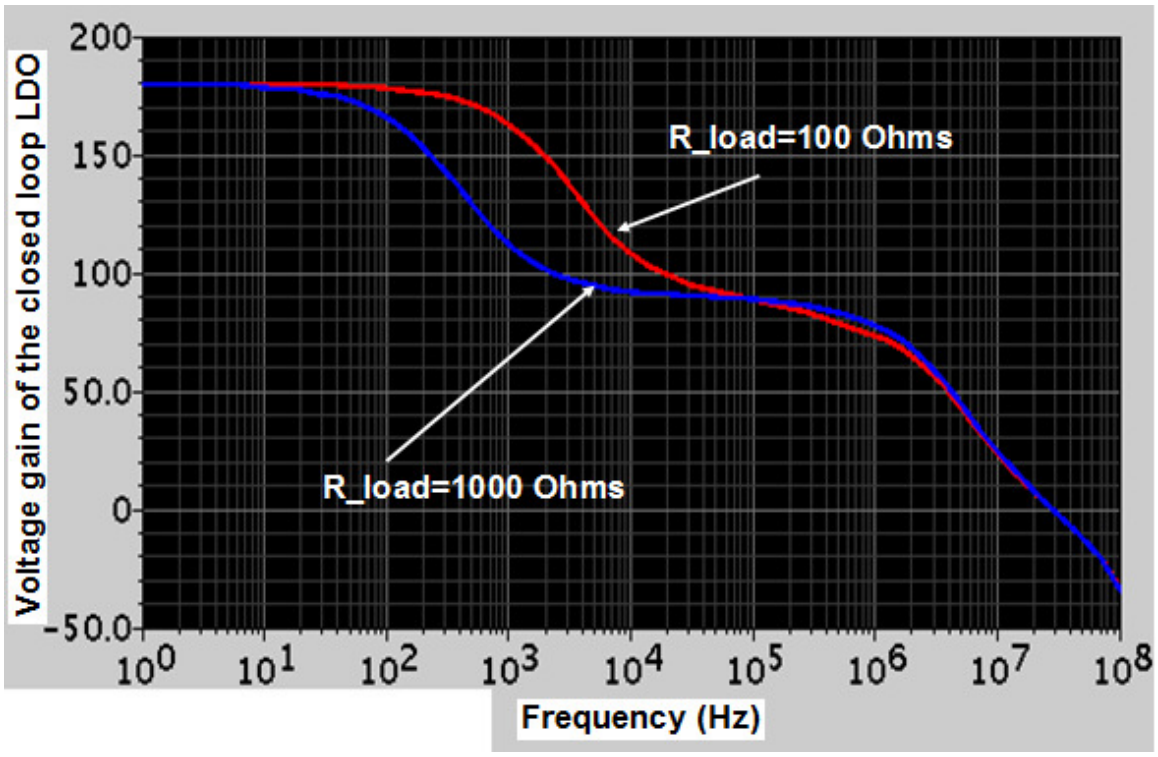
3.3.1.3 Low Drop-off Voltage Regulator Stability Analysis

The voltage regulator needs to be unconditionally stable with different loads (over a range of 100 to 1000 Ohm). The frequency of the noise can be at DC due to LO leakage, at IF frequency (1MHz in this design) due to the current variation caused by modulation and demodulation), and at high frequency due to LO leakage signal as well as current variation. Figure 3.9 shows the simulated voltage gain and phase response of the LDO obtained by applying AC signal at the INPUT as shown in Figure 3.2. The simulation results show that the worst phase margin occurs at 100 Ohm load, which is about 60 degrees.

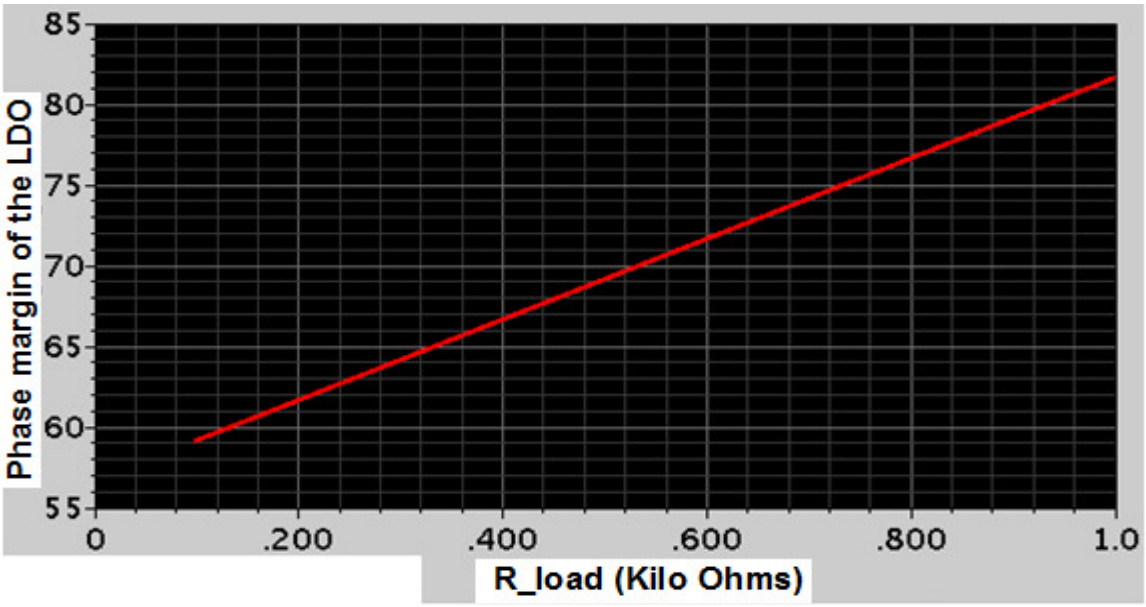
The dominant pole of the voltage regulator comes from the net (OUTPUT) as shown in Figure 3.2 because of the high capacitance at the OUTPUT net (C_{Load}). Normally the power rail metal has non-zero impedance;, also there exists a significant amount of current in the metal of the power rail when the transceiver is on. The AC current along with the non-zero impedance of the power rail metal generates noise for the power supply. The injected noise at the power supply may degrade the receiver performance. Normally a thick top metal is used inside the chip for both the power supply and ground rail. An off-chip capacitor at OUTPUT can provide an AC short for the supply rail noise and improve the transceiver system performance.


75
50
25
0
-25
-50
-75
Voltage gain of the closed loop LDO
R_load=1000 Ohms
R_load=100 Ohms
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)

(a)


200
150
100
50.0
0
-50.0
Voltage gain of the closed loop LDO
R_load=100 Ohms
R_load=1000 Ohms
10^0
10^1
10^2
10^3
10^4
10^5
10^6
10^7
10^8
Frequency (Hz)

(b)



(c)

Figure 3.9. Stability analysis of the voltage regulator as the battery load varies: (a) loop gain of the LDO under two different load scenarios (100 Ohm and 1K Ohm). (b) Phase response of the LDO under the two different load scenarios. (c) Phase margin of the LDO under the different load scenarios.

3.3.2 Receiver Design

On/Off key (OOK) receivers have been reported for use in low power receiver applications because of their simplicity and ease of implementation [Salter2007B, Daly2007]. Figure 3.10 is a block diagram of a typical OOK receiver.

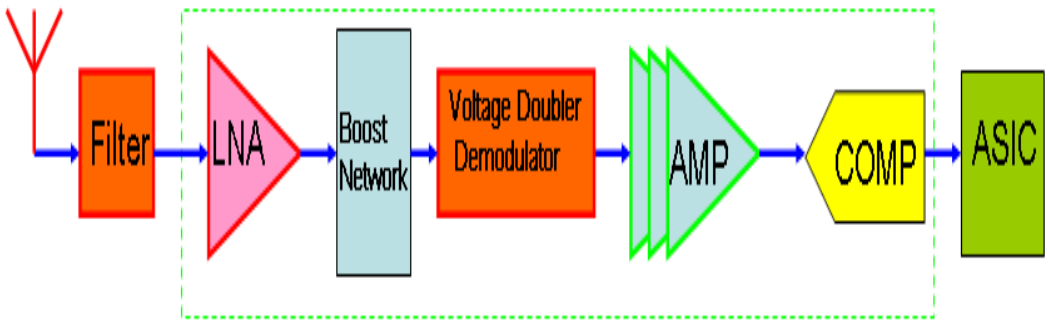


Figure 3. 10 Block diagram of the OOK receiver.

Such a device consists of a surface acoustic wave (SAW) filter, a low noise amplifier (LNA), a peak detector and baseband amplifiers. The SAW filter is placed in front of the low noise amplifier to remove interference signals. The LNA is used to improve the signal to noise ratio and also amplify the input signal to reach a detectable signal level for the demodulation of the peak detector. The transistor of the LNA works at the sub-threshold voltage range to optimize power per gain efficiency, and similar work has been reported previously in [Salter2007B]. The peak detector demodulates the signal after the LNA. It filters out the high frequency carrier signal while conserving the low frequency modulated information. Baseband amplifiers amplify the demodulated signal after the peak detector. The comparator circuit (COMP) works as a 1-bit analog to digital (ADC) converter. It amplifies the demodulated signal into a rail to rail digital signal.

3.3.2.1 Demodulator

The demodulator uses resonant frequency voltage boosting and voltage doubler techniques to greatly improve the receiver sensitivity. Figure 3.11 is the schematic of the demodulation voltage doubler circuit. The components R, L, C, and the parasitic capacitors of the M1 and M2 are analogous to the resistor (R), inductor (L), and capacitor (C) of a series RLC network. The relationship between V_{in} and V_{boost} can be described by equation 3.3.4 (the detailed analysis is explained in Chapter 4):

$$V_{boost} = QV_{in} \qquad (3.3.4)$$

$$Q = \sqrt{\frac{L}{C}} / R$$

Where Q is the quality factor of the RLC network. The simulation results in Figure 3.12 show the voltage boost of the input voltage, Vin. The Vboost is about 8 times of the input voltage Vin, an 18dB receiver sensitivity improvement. (the operation is explained in Chp4)

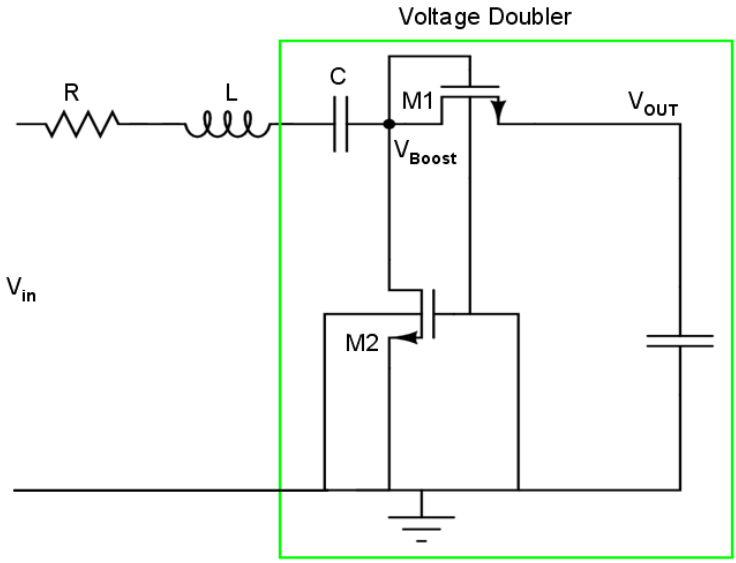


Figure 3.11. Improved voltage doubler demodulator using resonant frequency voltage booster techniques.

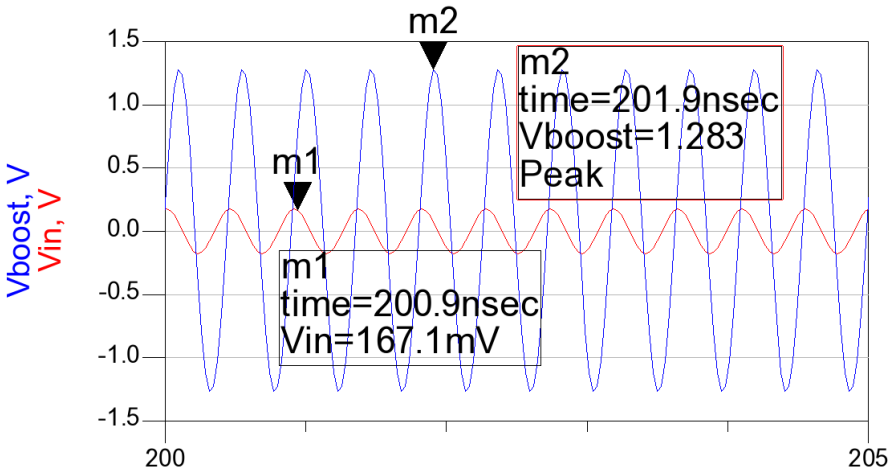


Figure 3.12. Resonant frequency voltage booster simulation results.

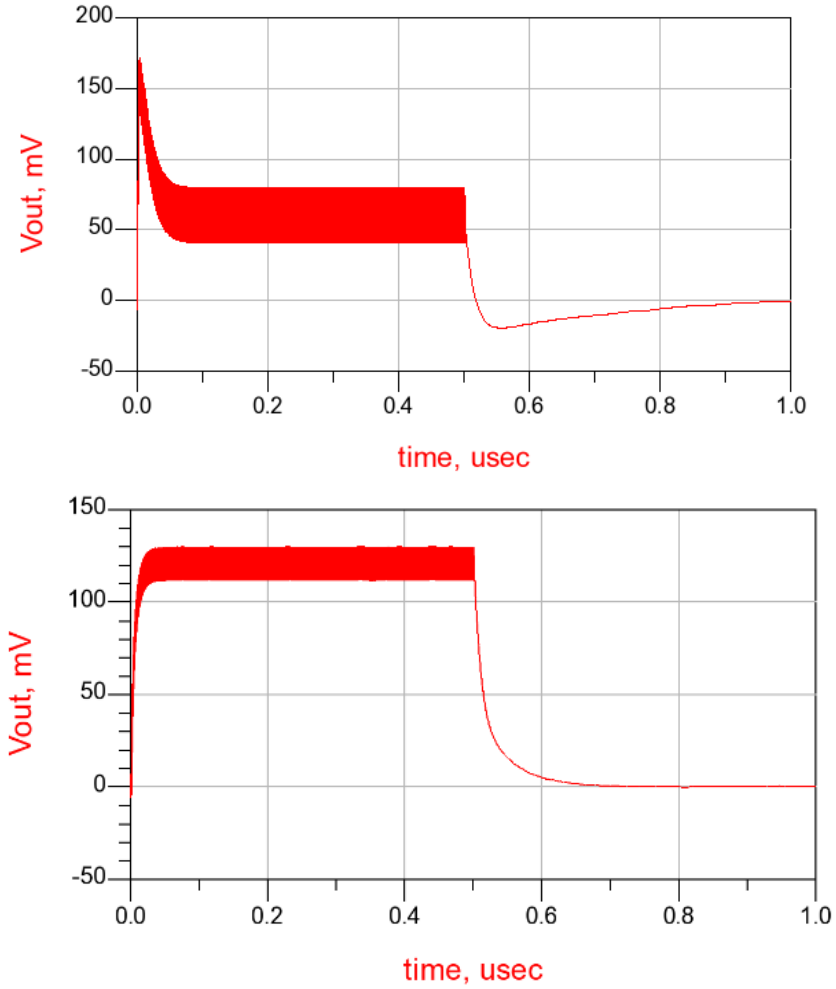


Figure 3.13. (upper) Peak detector demodulated signal. The input signal is an OOK signal with -0.6 to 0.6 peak to peak signal@2.2GHz. (bottom) Demodulated signal from voltage doubler with same input.

A voltage doubler circuit has been implemented to demodulate the signal instead of using a peak detector as a method to improve the voltage conversion gain and system sensitivity. Component C and transistors M1 and M2 form the voltage doubler circuit as shown in Figure 3.11. Compared with a peak detector, the voltage doubler circuit makes full usage of the AC signal. Its output voltage is twice that of the output voltage of the peak detector. The voltage doubler circuit works in the following way: when the signal is positive, the transistor M1 is turned-on and the current I_1 is charging the output capacitor; when the signal is negative, transistor M2 is turned-on and the current I_2 is charging the

capacitor C. In this way, the voltage doubler circuit makes full use of the input AC signal circle and achieves twice the output voltage as the peak detector. Figure 3.13 indicates the simulation results of the demodulation output voltage for both a voltage doubler circuit and peak detector circuit for an OOK input signal with a peak to peak signal@2.2GHz with voltage varying from -0.6 to 0.6V. The simulation shows that the voltage doubler demodulator achieves 130mV output voltage compared with the 70mV output voltage of the peak detector.

3.3.2.2 Low Power Low Noise Amplifier

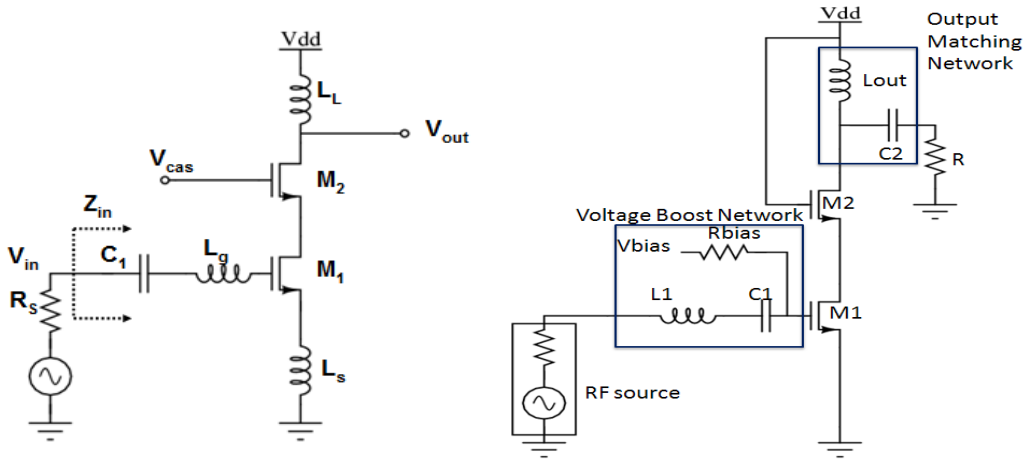


Figure 3.14 (a) CMOS low noise amplifier. (b) The schematic of the designed low noise amplifier specified for low power applications.

Figure 3.14 (a) shows a widely used low noise amplifier circuit for low noise applications. It uses a common source cascode amplifier (transistors M1 and M2) topology to reduce the Miller effect to extend the bandwidth of the amplifier. It also uses inductors L_s and L_g to obtain both power matching and noise matching to obtain low noise performance. This design can obtain a minimal noise figure; however, this topology is not optimized for low power applications where low power consumption is essential. In

Figure 3.14 (a), the inductor L_s is used to help obtain power matching and noise matching. However, the inductor L_s degenerates the circuit power gain. Figure 3.14 (b) shows the schematic of the designed low power LNA, which meets our stated low power design specifications more aptly by removing the degenerate inductor to improve power gain. The power matching is achieved by taking advantage of the parasitic series resistance of the inductor R_g and the inductor itself L1. The lossy on-chip inductor has an intrinsic series resistance that can be used as the necessary gate resistor for the power matching network. The L1 and C1 components, together with transistor M1, form the input matching network. Meanwhile Lout and C2 along with transistor M2 provide an output matching network.

In this design, the transistor M1 in Figure 3.14 is designed to work in the sub-threshold voltage region to achieve maximum power efficiency [Salter2007B]. The theory behind this design is explained based on the following equations. In low power design, a minimum power per gain is preferred. The expression 3.3.5 below reflects a figure of merit representing the power per gain is defined by Equation 3.3.5:

$$\frac{Gain}{Power} = \frac{g_m \times Z_L}{Vdd \times I} \propto \frac{g_m}{I} \tag{3.3.5}$$

Where Z_L is the output impedance, which is 50 Ohm at the designed frequency while VDD is fixed at 1.2 V in this design.

The current in saturation region is simply modeled by Equation 3.3.6:

$$\frac{Gain}{Power} = K \frac{1}{(V_{gs} - V_{th})^n} \tag{3.3.6}$$

Where K is a process constant and n is equal to 1 for a long channel device and is between 0 and 1 for a short channel device. Equation 3.3.6 indicates that the figure of

merit goes to infinity when the override voltage V_{gs} is equal to V_{th}. This is not physical because the MOSFET begins to operate in the sub-threshold voltage region when V_{gs} is close to V_{th}.

In the sub-threshold voltage region, the figure of merit is modeled by Equation 3.3.7:

$$\frac{Gain}{Power} = \frac{K_{sub}}{V_t} \tag{3.3.7}$$

Where K_{sub} is a process constant. Equation 3.3.7 indicates that power per gain figure of merit is a constant in the deep sub-threshold voltage region. The combination of 3.3.6 and 3.3.7 indicates that the power per gain is maximized between the deep sub-threshold voltage region and saturation region. The optimized biasing voltage is close to the threshold voltage. The analysis has been supported by the simulation. Figure 3.15 indicates that the simulated power per unit gain (power/gain) varies with the bias voltage of the LNA. It shows that the LNA achieves its maximum power efficiency at bias voltage 0.39V, which is at a sub-threshold voltage of transistor M1.

Moreover, when the MOSFET works in the sub-threshold voltage region, the type of MOSFET noise that dominates is shot noise instead of channel thermal noise. The shot noise can be described by Equation 3.3.8:

$$\tilde{I}^2 = 2qI_D = 4kT\gamma g_m \qquad I_D = I_S e^{(qV_{GS}/nKT)} \tag{3.3.8}$$

$$n = \frac{C_{ox} + C_{depl}}{C_{ox}} \approx 1.5 \qquad \gamma = \frac{n}{2}$$

This shows that the shot noise can be expressed in proportion to g_m just as thermal noise is, as well. Compared with the noise source of MOSFET biased in the saturation region, this noise source has a different noise factor γ. The noise factor is 0.75 in the sub-

threshold voltage region while it is 0.67 in saturation region. In this way, the noise factor for the new circuit topology is

$$F = 1 + \frac{R_g}{R_s} + \frac{\gamma}{\alpha} g_m R_s (\frac{\omega}{\omega_T})^2 \quad (3.3.9)$$

where R_g is equal to R_s.

Figure 3.16 panels (a) and (b) show the simulated power gain and noise figure of the LNA, respectively. The LNA has a simulated power gain of 13.5 dB with a 3.2 dB noise figure @2.3GHz. In this design, two LNAs are cascaded together to meet the system sensitivity requirements (-65dBm). More stages of LNAs can be cascaded together to achieve a higher sensitivity for the receiver with careful consideration to avoid oscillations due to parasitic feedback. The noise figure of the LNA is dominated by the noise figure of the first LNA stage, which is about 3.2 dB. Figure 3.17 indicates the simulated compression point (P1dB) of the LNA, which measures the linearity of the LNA. The simulated LNA's P1dB is around -14 dBm. The stability of a one stage LNA is determined by the Stern stability factor K and Δ: the amplifier is unconditionally stable if the Stern stability factor K and Δ satisfy Stern - Rollet's [Razavi1997] condition: K > 1 along with Δ < 1, where

$$K = \frac{1 + |\Delta|^2 - |S_{11}|^2 - |S_{22}|^2}{2|S_{12}||S_{21}|}$$

$$\Delta = S_{11}S_{22} - S_{12}S_{21}$$

Figure 3.18 shows the simulated stability factors of the LNA. This shows that the designed LNA is thus unconditionally stable since it satisfies Stern Rollet's condition.

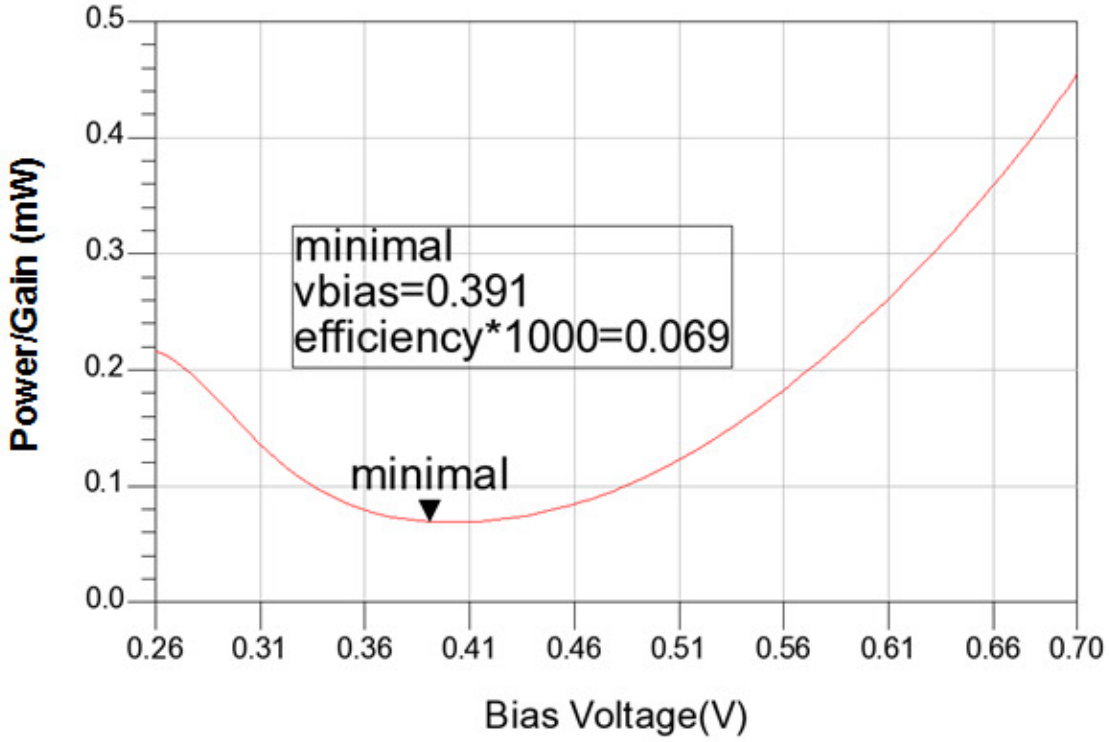
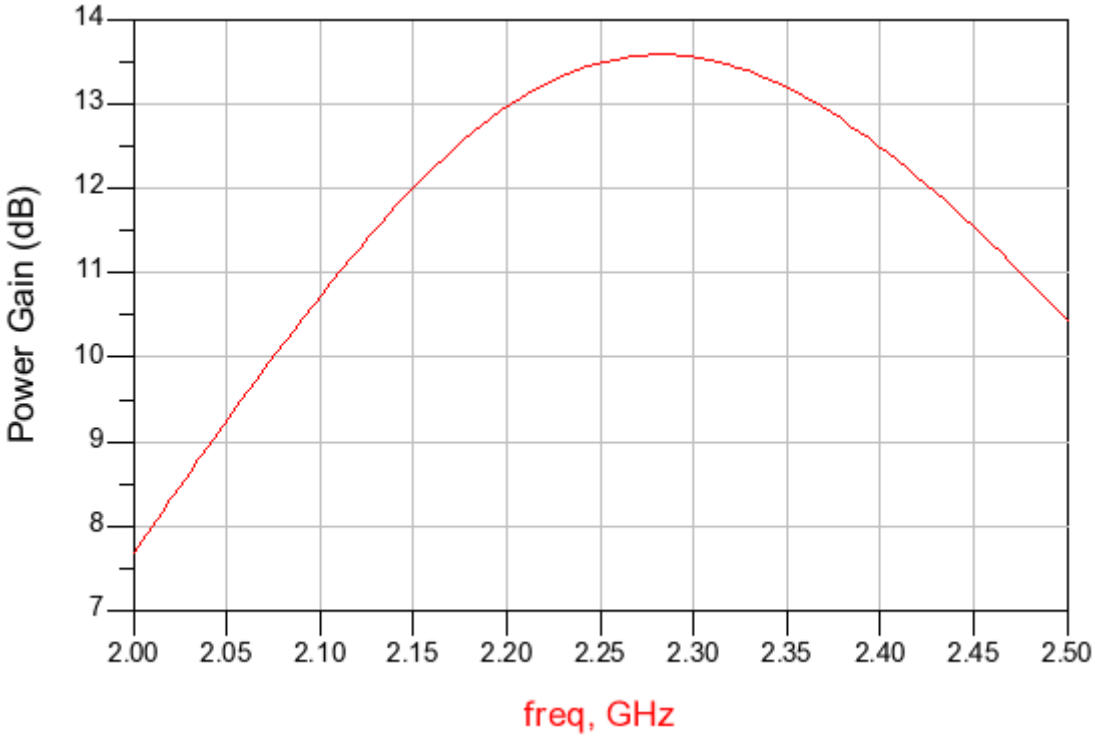
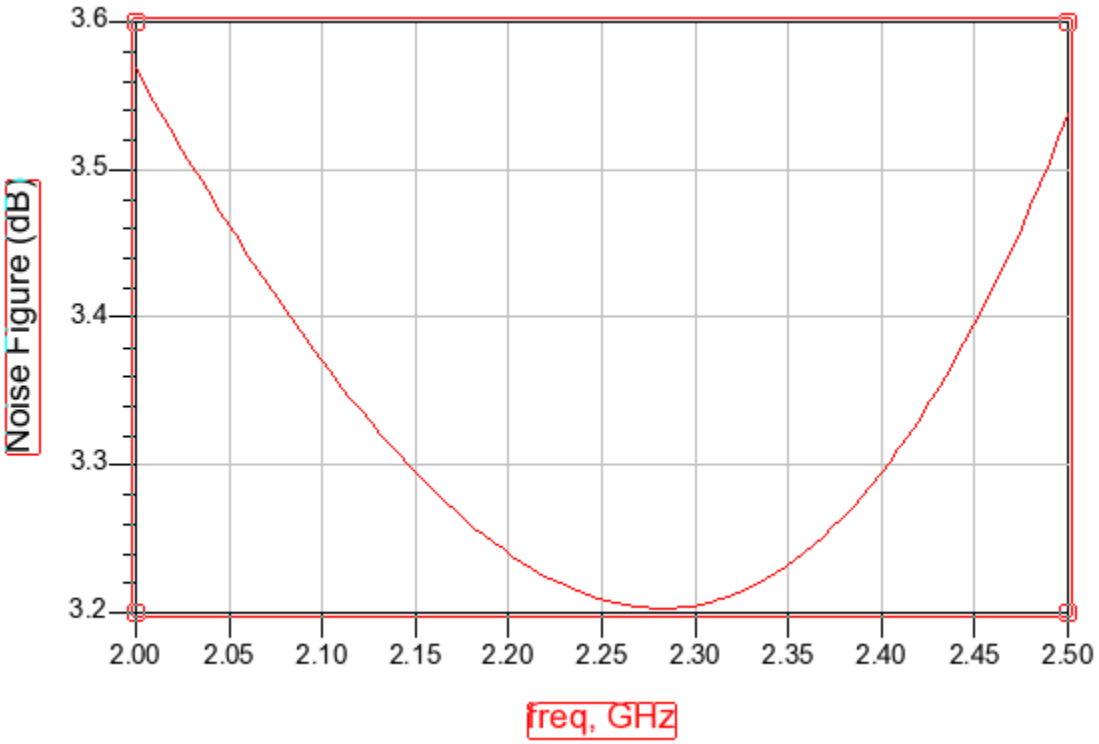


Figure 3.15. LNA power efficiency varies with bias voltage.



(a)



(b)

Figure 3.16. (a): Simulated LNA Power gain; (b): Simulated LNA Noise Figure.

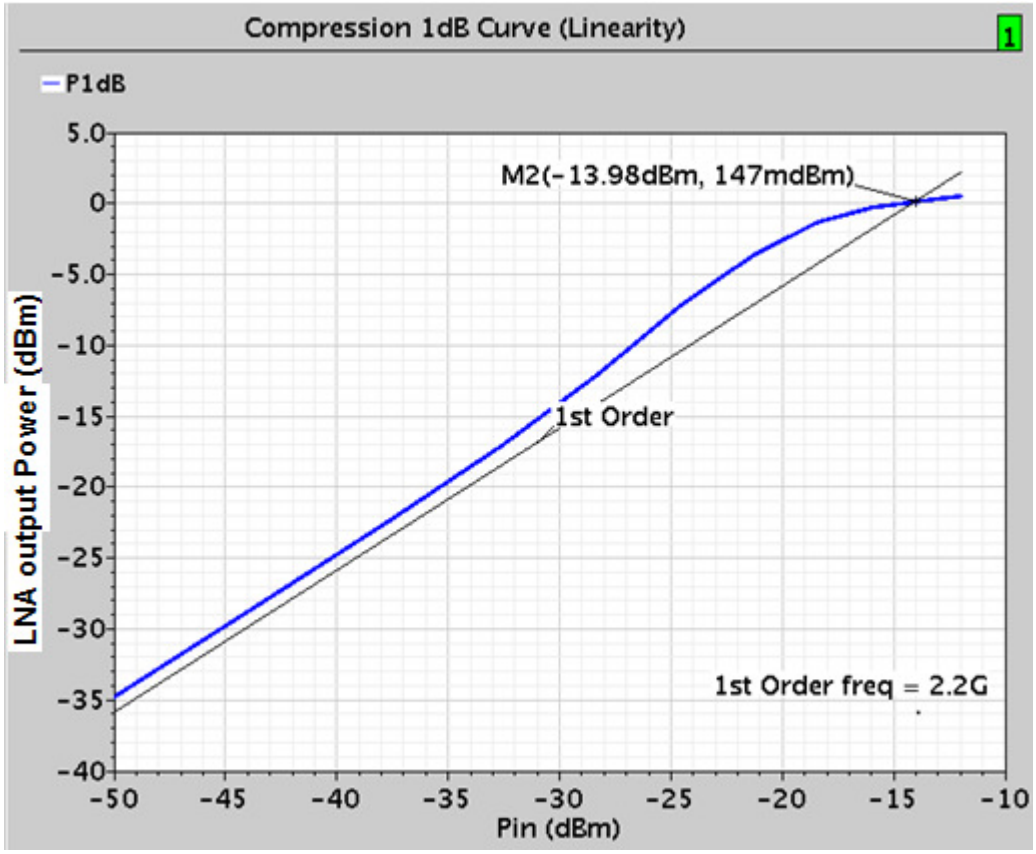


Figure 3.17. Simulated LNA P1dB.

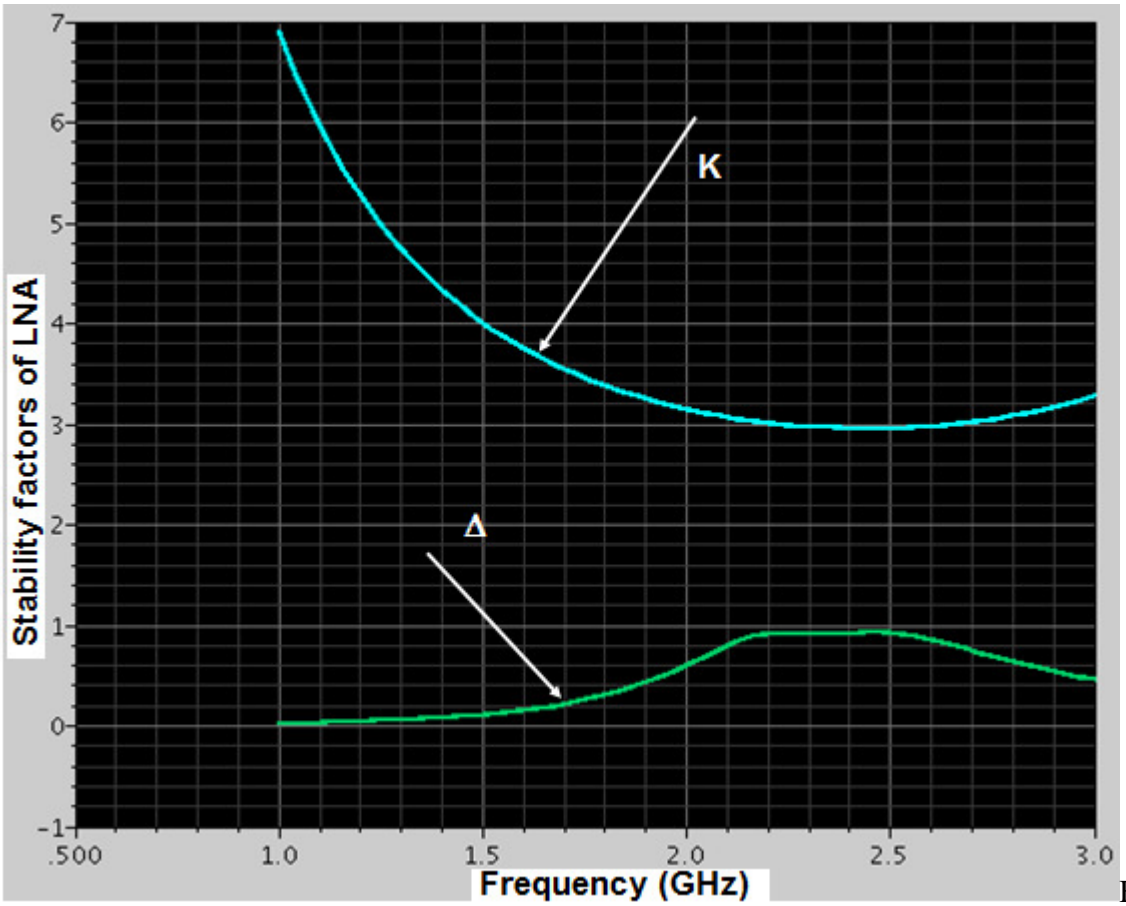


Figure 3.18. Simulated K and Δ of the LNA.

3.3.2.3 Baseband Amplifier & DC Switch

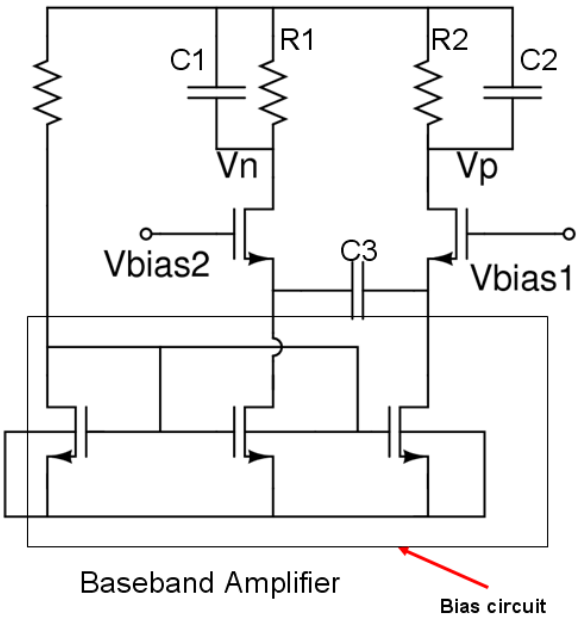


Figure 3.19. baseband amplifier.

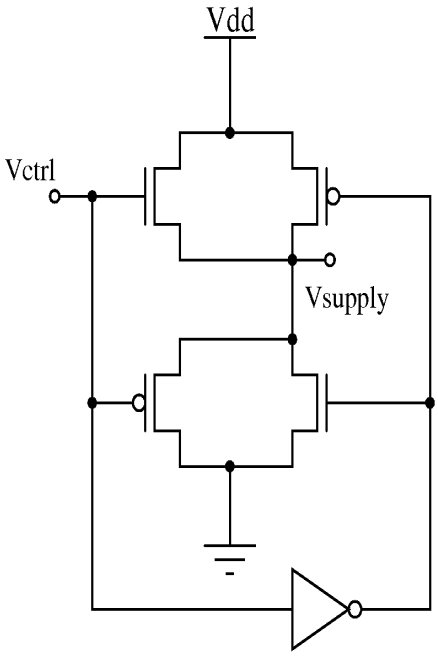


Figure 3.20.DC switch topology.

The baseband circuits amplify the demodulated signal into rail to rail digital signals in order to be further processed by the digital ASIC. The receiver sensitivity improves if the baseband amplifier can distinguish a smaller voltage difference from the demodulation circuits. Since significant amounts of power are needed to amplify the signal at the high carrier frequency, it is important to obtain the best possible voltage distinguishing ability through baseband circuits.

Compared to the large power needs of RF signal amplification, the required power for baseband amplification is relatively low. A common two-stage amplifier can achieve a voltage gain of 1000 with less than 100 uW power consumption. The main difficulty of cascaded multi-stage baseband circuit amplification is due to the threshold voltage mismatch of the MOSFET devices. The first stage of the baseband amplifier is normally a differential amplifier to improve the signal to noise ratio since differential topology

cancels out the common noise signals. However, the threshold voltage mismatch introduces a DC offset that is amplified by the differential amplifier and causes a series DC biasing offset for the second amplification stage. Auto zero techniques [Daniel2004] have been developed to remove the DC offset; however, this commonly consumes mW power and is not suitable for WSN low power applications. For instance, the design here is aimed at achieving a 0.5 mV distinguishing ability with less than 100 uW power consumption.

Figure 3.19 is the schematic of the designed baseband amplifier. It uses differential amplifier topology with an additional capacitor C3 to connect the drains of the two MOSFETs. The capacitor C3 provides a solution to the DC offset problem. The capacitor C3 works as a DC open. The output voltages Vn and Vp are thus determined by two separated bias currents. This is not affected by the threshold voltages of the two MOSFETs. In other work, there is no DC signal gain for this topology. However, at the signal frequency (1MHz), C3 works as a short, and the two bias current sources work as a current source; hence the overall circuit works as a differential amplifier. The circuit achieves a voltage gain of 5 at the 1MHz baseband signal frequency. The capacitors C1, C2 and the resistors R1, R2 filter out the noise at higher frequencies (e.g., the carrier frequency). As a summary, the baseband amplifier has a bandpass voltage gain. It achieves voltage gain at a demodulated signal frequency (1MHz) while having zero voltage gain at DC and carrier frequencies. Figure 3.21 shows AC response of the designed amplifier. Peak voltage gain is obtained at the demodulated signal frequency (1MHz) while the voltage gains at DC and carrier frequency are close to zero. Since the DC offset of the threshold voltage is eliminated to zero by the baseband amplifier, the

amplifier successfully provides a solution for the threshold voltage mismatch problem. It thus enables cascade multi-stage amplification.

However, there is also a limitation on the number of stages that can be cascaded. The limitation of the voltage distinguishing capability of the baseband amplifier comes from the noise factor of the amplifier. The baseband amplifier has a high noise factor due to the high resistances of R1 and R3, which are necessary to reduce the power consumption of the baseband circuit. In this design, four baseband amplifiers have been cascaded together to achieve a minimum detectable baseband voltage of 0.5 mV at approximately 53 μW power level. A similar design can be found in [Pletcher2008].

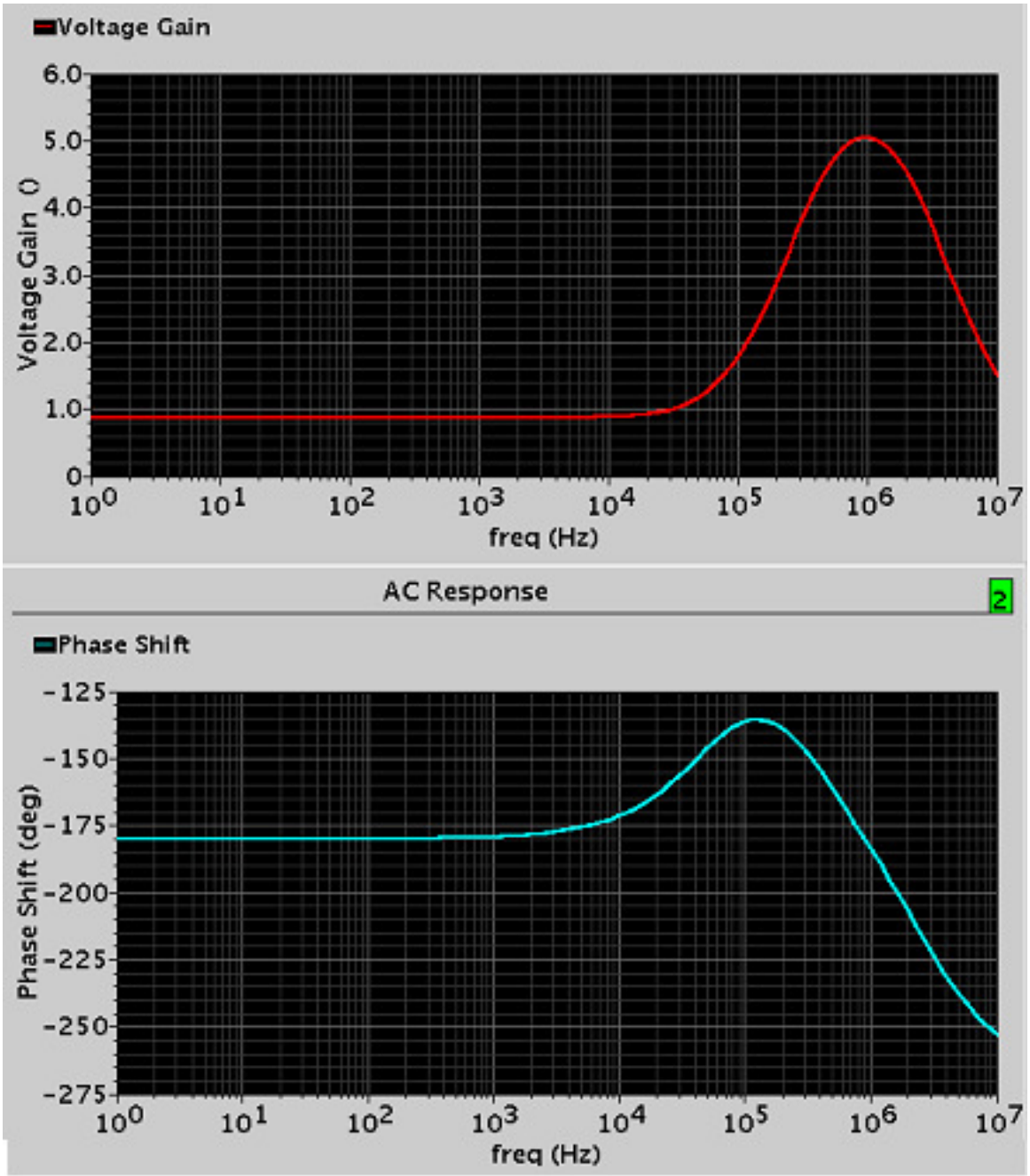


Figure 3.21 Frequency and phase response of the baseband amplifier.

A DC switch is needed to implement the TDMA protocol by switching on/off the transmitter/receiver. When only one of transmitter/receiver is on at one time, the switch not only saves system power but it also enables the TDMA protocol for ASIC control. The DC switch utilizes transmission gates to turn on or off the power voltage of the receiver/transmitter. Transistors with appropriate sizes are selected both to ensure the

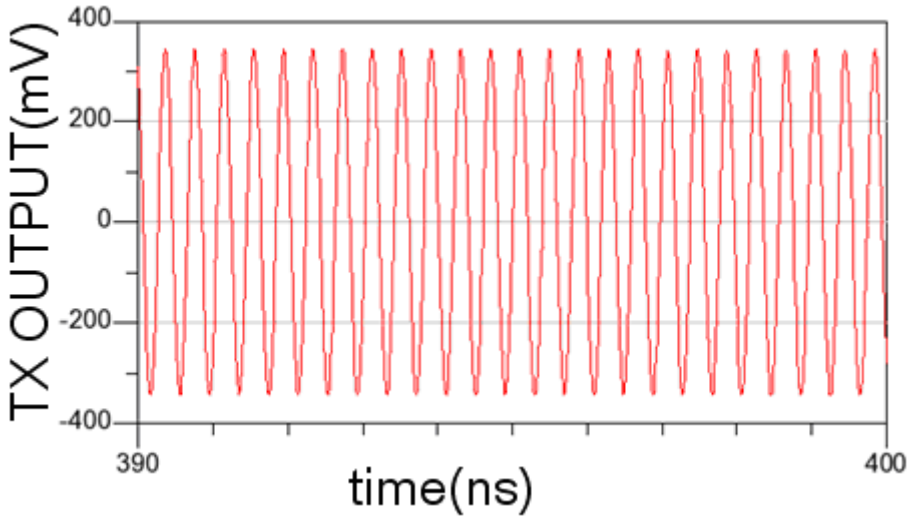
on/off switching speeds and to handle large amount of current. The designed RF switch is similar to previous RF switch work [Zhenbiao2003].

3.3.3 Simulation Results of the Transceiver System with Power Management

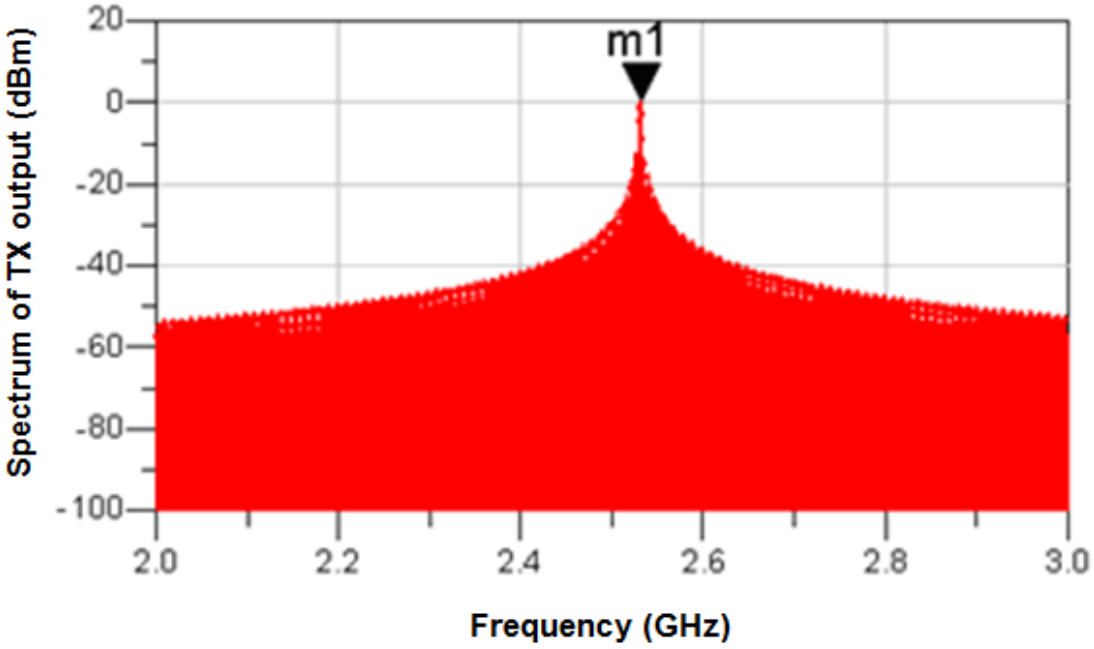
The uniqueness of this work is the integration of the low power voltage regulator circuitry with a low power transceiver. The power management circuits need to handle a large amount current variation in a short time period (from 2 to 10 mA within only 2 μs time) when the transceiver is on. Figure 3.21 (c) shows the LDO output voltage when the transmitter is on. The LDO output voltage has 10 mA voltage variation at carrier frequency; a 1uF off-chip capacitor is included to stabilize the supply voltage to improve the transceiver performance.

The system is designed to work over a 1.35-1.6V battery voltage range in order to achieve a minimal 70% voltage regulator efficiency. However, the chosen MOSFET devices can operate with supply voltages as high as 3.3 V. The additional DC to DC voltage conversion can be obtained through a Buck DC to DC converter with over 90 percentage efficiency. In this work, the buck DC to DC converter is not included.

Figures 3.22 and 3.23 show the simulation results for the LDO with transmitter and receiver, respectively. Figure 3.22 contains the simulation results of the LDO with the transmitter. The results show that the transmitter generates 0dBm output power at 2.2GHz. Figure 3.23 shows that the system obtains a sensitivity of -65dBm. It also indicates that the transmitter is completely off, since TXout is at zero (Figure 3.23 right panel) when the receiver on.



(a)



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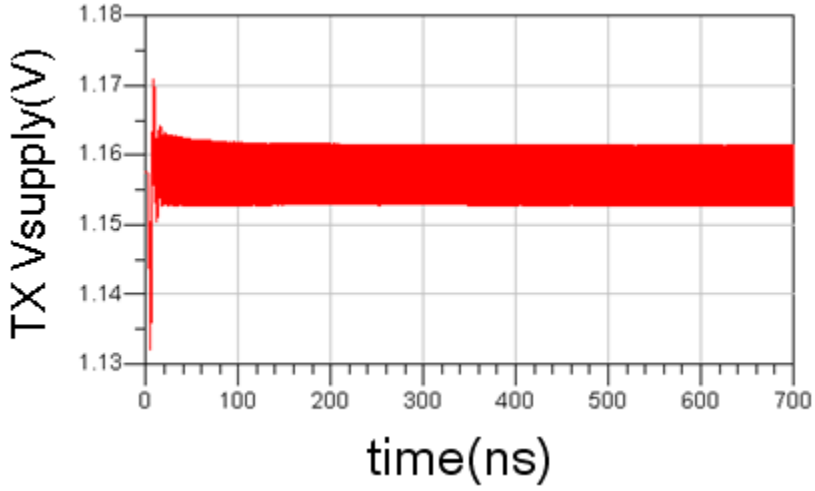


(c)

Figure 3.21 LDO application on TX. (a) : transmitter output. (b): the spectrum of transmitter output signal.(c): LDO output voltage without the off-chip capacitor (1uF).

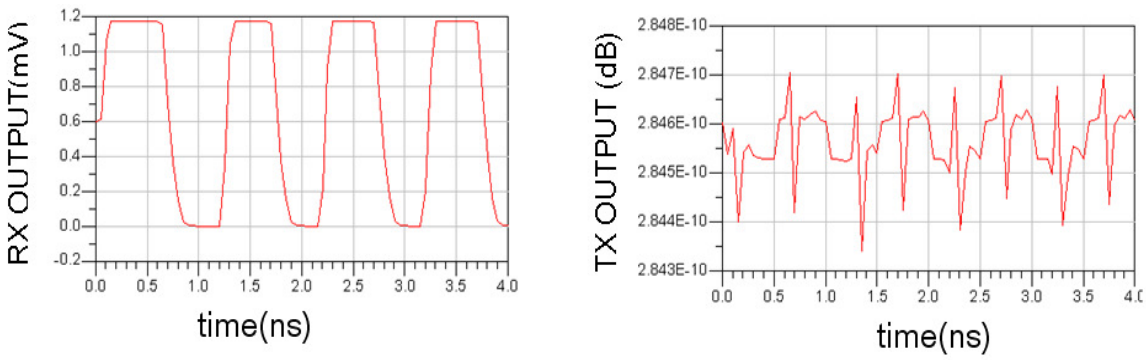


Figure 3.22 LDO Application on RX. Upper left: demodulated output. Upper right: transmitter output signal.

3.4 Measured Results

The prototype chip is fabricated in a 0.13-μm single-poly eight-metal standard CMOS process. Figure 3.24 shows the die photo of the fabricated integrated transceiver, which includes a transmitter, a receiver, DC and RF switches, and a LDO. The chip may work with TDMA ASIC as a node of a SDS.

The receiver has been measured by an Agilent E8267D signal generator and an Agilent DSO81304A digital scope. The receiver has a sensitivity of -60 dBm with power consumption of 4mW@1.4V with 1Mbps data rate. The integrated receiver has been successfully demodulated over a voltage range of 1.35-1.6V. Figure 3.25 shows the demodulated 1MHz signal where the input signal is a 2.2 GHz OOK signal modulated by a 1MHz baseband signal. Previous reports provide the receiver power consumption only by the receiver. This handicaps to the results presented here compared to previous publications since we have also measured and included the system power. We use both sensitivity and energy per bit to evaluate the receiver performance. Table 1 shows the

comparisons. The transmitter performance of the system is not fully tested due to the package requirements of the chip.

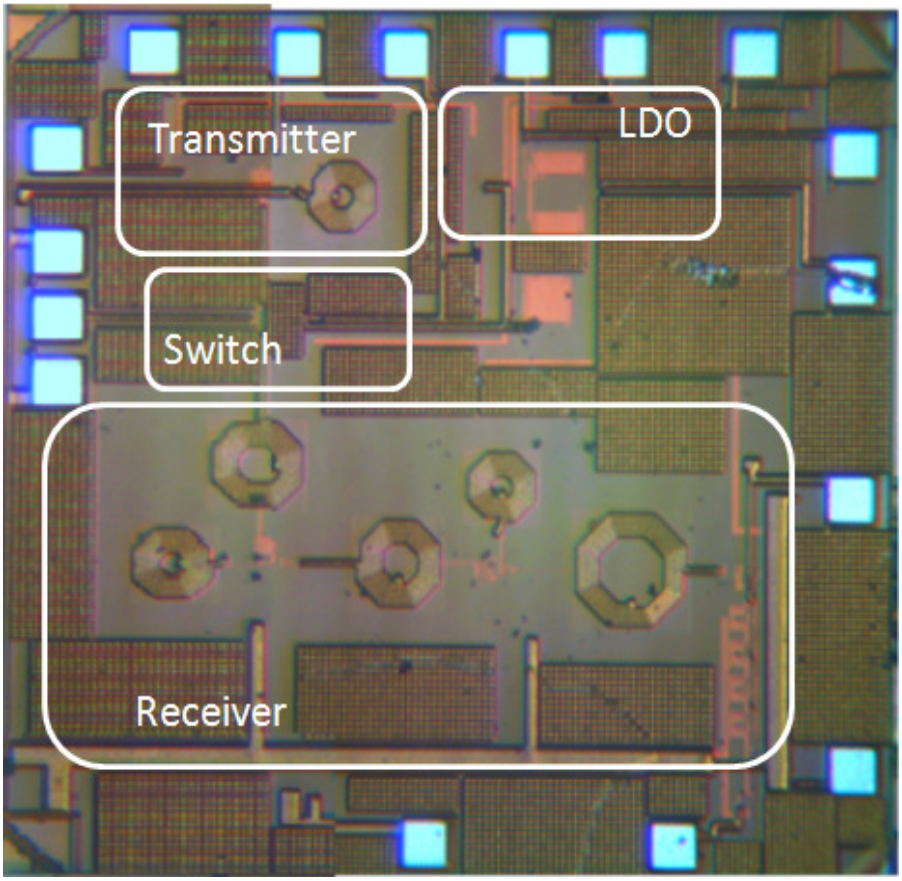


Figure 3.23 Die photo of the OOK transceiver chip (2x2 mm^2).

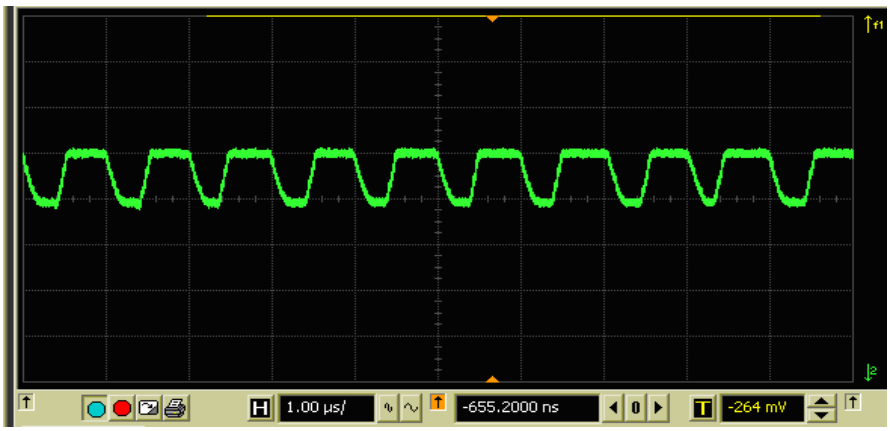


Figure 3.24 Demodulated 1MHz signal, where the input signal is a 1MHz OOK signal with 2.2GHz carrier signal.

Table1. Receiver performance comparisons

Ref	Sensitivity(dBm)	Energy Per bits
3	-65	2.5nJ/bit
7	-95	41.7nJ/bit
8	-94	6nJ/bit
This work	-60	4nJ/bit

3.5 Conclusions

A fully integrated OOK transceiver with on-chip biasing circuits has been designed, fabricated, and tested. The system meets the low cost requirement through high system integration along with the usage of standard pure CMOS process. The transceiver system includes a low power OOK receiver, a transmitter, RF/DC switches, and voltage regulators that provide comprehensive on-chip biasing voltages.

The voltage reference circuit was designed to supply constant voltage under temperature and voltage variation. Temperature independence is achieved by the cancellation of the opposite temperature tendencies of the PMOS and NMOS threshold voltages. The voltage regulator makes use of the reference voltage generated by the voltage reference circuit and an operational amplifier with a feedback network to generate a load independent voltage. A common source low noise amplifier (LNA) is

designed to work at the sub-threshold range of its transistor to achieve maximum power per gain efficiency. A Villard voltage doubler circuit, as well as an on-chip voltage transformer, has been implemented to significantly improve the signal demodulation efficiency and thus improve the system sensitivity with no extra power consumption.

Measurements show that the integrated transceiver system achieves a receiver sensitivity of -60dBm with 4mW@1.4V with all on-chip biasing circuitry and switches. The energy per bit of the transceiver is only 4nJ/bit. This chip can be used as a node of a wireless sensor network with a TDMA ASIC control circuit [Shen2008].

The contributions of this work are listed as follows:

- Pure low power CMOS voltage regulator
- Integrated low power OOK transceiver system design
- Integrated low power OOK transceiver with voltage regulator co-design

Chapter 4: Voltage Doubler Analysis and Theory of Dual-/Multi-Band RF Energy Harvesters

4.1 Overview of Power Harvesting Concept

4.1.1 Motivation in Relation to Wireless Device Power Needs

Most mobile devices use batteries as their sole power sources. Different power management techniques such as smart wake-up procedures are used to keep the electronics sleeping most of the time to extend battery lifetime. Such mobile devices often need to be recharged through a power plug once every few days.

However, in some specific wireless applications, device (battery) sizes are very limited. This includes smart dust systems (SDS), in which the total size is desired to be smaller than 1 cm^3, as well as some medical applications in which the dimensions need to be very small in order to be swallowed and/or to alleviate concerns about poisoning from batteries. Moreover, SDS applications require long operational lifetimes (months or even years) along with these devices' size constraints. However, it is not feasible to replace batteries of this kind due to large maintenance costs. These novel applications thus require new power solutions to meet the system requirements.

Alternatively, renewable power resources in the ambient environment emerge as a promising alternative power solution for some wireless applications. As devices are continually scaled down in size, the required digital energy to switch digital inverters keeps decreasing as well. For example, the switching power of a minimal size inverter in 65nm CMOS technology is as low as 0.08fW. The required power of digital switches is

much smaller than the ambient RF power level, which can be as high as 16.6 μW at 1800MHz [Burch2006]. It is promising to use ambient RF energy as an independent power source for the electronics. An even more promising power solution for WSN applications is to combine both a battery source and energy harvesting power sources together: this can recharge the battery to greatly extend the battery lifetime to meet WSN specifications. Compared with conventional common battery power solutions, environmental power is renewable, free, and clean. Potential wireless sensor networks (WSNs) applications for commercial use are:

- To extend RFID tag range.
- To remove the risks of more dangerous wired solutions in medical devices for wireless bio-medical applications.
- To meet the power specifications of low power mobile devices in a wireless sensor network.

4.1.2 Viability of Available Ambient Energy Sources

Energy harvesting, or scavenging, uses transducers to convert ambient energy from the surrounding environment, such as radio electromagnetic waves, solar, vibrational, or thermal energy, into storable electrical energy to power electrical circuits.

Solar, vibration, and radio energy are the three most commonly available power sources in the environment. Typical solar power density is 100mW/cm^3 in bright sunlight [Paradiso2005]. However, the power density decreases to the ~100uW/cm^3 level in cloudy weather or in an office setting [Chalasani2008]. Previous research [Green1986] reports conversion efficiencies as high as 25%. Solar energy is an ideal power source for outdoor applications, whereas it is very limited for indoor applications.

Vibrational sources, such as those due to wind, are another available environmental power source. This source has a power density of ~100uW/cm^2 [Paradiso2005]. Piezoelectric materials are often used to convert mechanical energy into electrical energy. However, vibrational energy is very limited in some locations.

In urban areas, there are different radio frequency signals widely available to support different kinds of communication services such as TV and cell phone signals, etc. Radio signals are purposely designed to provide services over a large area and can be considered widely available. The RF energy density in an urban area can be as high as 0.5μW/cm^2, which corresponds to an input power level of 16.6 μW (-17.6 dBm) at 1800MHz [Burch2006]. This is higher than the power consumption of a low power mobile device such as the Ti CC2420 in sleep mode [Penella2009]. It is thus promising to convert the available environment RF energy into electrical energy and use this to power mobile devices or store the harvested electrical energy via a rechargeable battery to extend battery lifetimes. Compared with standard battery power sources, harvested energy is continuously renewable and thus has no limitations on operational lifetime. It is free and environmentally friendly as well.

4.1.3 Review of Previous RF Energy Harvesting Work

RF energy harvesting is a process for converting AC (RF) power into DC power. A diode (rectifier) along with a capacitor (peak detector) can convert AC power into DC power. However, a simple rectifier based on a traditional peak detector only makes use of a half signal circle and thus has low conversion efficiency. A more efficient topology is to utilize a voltage doubler structure, which makes use of the full signal cycle. Figure 4.1.1 shows the circuit schematic of a voltage doubler.

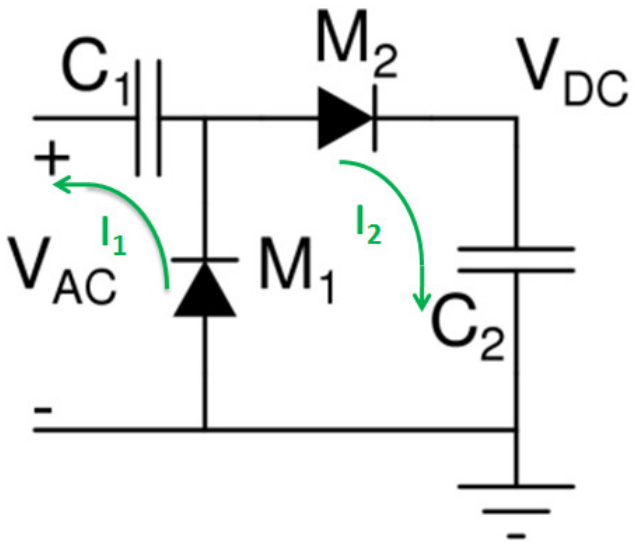


Figure 4.1.1 Diode voltage doubler.

The AC to DC conversion process is as follows: the diodes rectify the AC signal and generate currents I_1 and I_2 to charge the capacitors C_2 and C_1, respectively; in the negative signal circle, M_1 is on and M_2 is off. The RF signal charges the capacitor C_1 through current I_1. In the positive cycle, transistor M2 turns on and transistor M1 turns off, and both C_1 and the RF input signal will power the capacitor C_2 through current I_2. The voltage doubler thus converts RF power into DC power utilizing the full AC signal cycle. The rectifier can obtain high power conversion efficiency when the charging currents (I_1 and I_2) are large, which requires that the input signal voltage be greater than the diode threshold voltage. When the signal voltage is smaller than the threshold voltage, the charging currents I_1 and I_2 decrease exponentially to zero, and so does the conversion efficiency.

However, in any specific ambient RF energy harvesting application where the input power is very limited (10 uW or less), the input signal voltage will be much smaller than

the threshold voltage of typical diodes. This results in very limited AC to DC conversion efficiency.

There are different approaches to address the diode threshold voltage barrier problem to improve conversion efficiency at low input power levels. Schottky diodes normally have 200 mV threshold voltages, which is lower than for PN diodes. Work by Udo Karthaus et al. [Karthaus2003] utilized low forward threshold (200 mV) Schottky diodes to help turn on the diodes under low input power. However, the 200 mV threshold voltage of the Schottky diode is still much larger than the input signal voltage. Furthermore, Schottky diodes typically are not standard devices in CMOS processes.

Another possible kind of diode is a CMOS connected diode, which is widely available in CMOS processes. This has been implemented in several recent publications [Umeda2006], [Nakamoto2006], [Facen2007] [Mandal2007]. The threshold voltage of the CMOS based diodes is 400 mV for standard CMOS devices and 300 mV for low threshold voltage CMOS devices. The barrier of the diode threshold voltage needs to be greatly reduced to fit into a low power energy harvesting scheme.

Toshiyuku Umeda et al. designed the distributor circuits to supply a bias voltage for MOS connected diodes to easily turn on the diodes and thus obtain higher charging current for low input power [Umeda2006]. Their work achieves 0.75% efficiency for -14 dBm input power. However, their distributor circuits require a secondary battery to power the distributed biasing circuits.

Floating gate devices can be used to program gate voltages for very long periods (over ten years unless reprogrammed). They can be fabricated through standard CMOS process without extra cost [Ching-Fang2007]. Srinivasan et al. provides a procedure to program

floating gate devices [Srinivasan2005]. Hiroyuki Nakamoto et al. implemented floating gate devices to pre-set the biasing voltages at the gates of diode-connected MOSFETs[Nakamoto2006]. Their work does not need a secondary power source. However, this method needs an additional procedure to correctly program the biasing voltages. This method also loses the flexibility to adjust the stored DC voltages according to different input signal power strengths.

Salter et al. [Salter2007] use off-chip high impedance resistor networks to provide different DC biasing voltages at the gates of the diode-connected MOSFETs. This technique also does not need a secondary power source. However, this may increase the chip costs due to off-chip biasing networks.

Besides the approach of reducing the threshold voltage, there has been another direction of research aimed toward addressing the threshold barrier problem of diodes by using a voltage transformer to boost input signal voltages. Hiroyuki Nakamoto et al. [Nakamoto2006] and Triet Le et al. [Le2008] use different matching networks to boost the input signal voltages. Previous published works [Salter2009] [Yao2006] use a RLC voltage circuit to boost the signal voltages to turn on the diodes and improve conversion efficiency.

Figure 4.1.2 shows a circuit schematic for a diode-connected MOSFET based voltage doubler [Salter2009]. The gates of transistors M1 and M2 are biased by the networks (R1, R2, C5) and (R3, R4, C6), where C1 and L1 along with the parasitic capacitances of transistors M1 and M2 form the voltage boosting network.

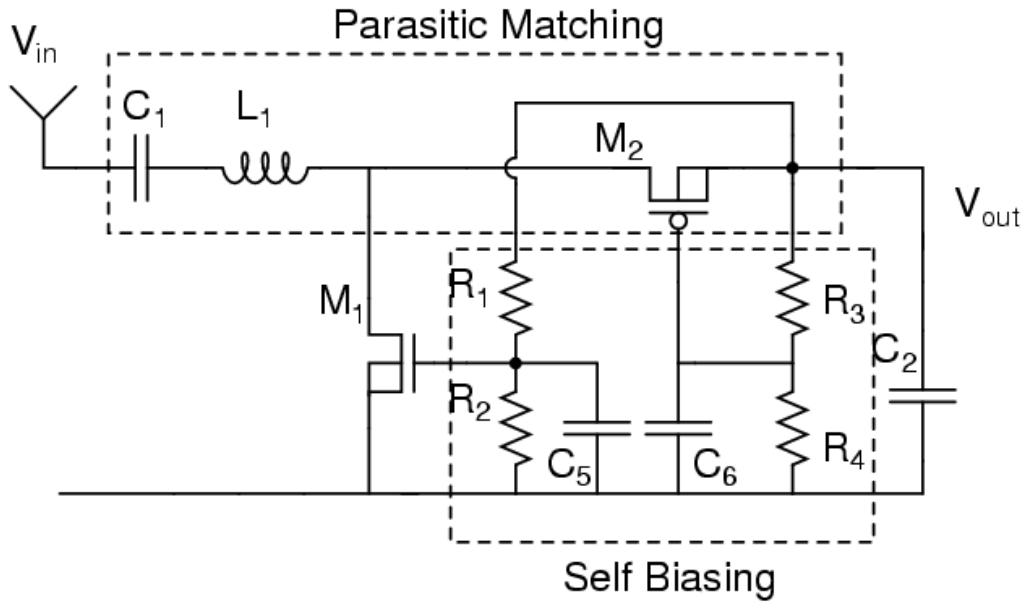


Figure 4.1.2 Improved voltage doubler.

All the previously cited works focus on improving the harvesting efficiency within a narrow frequency range. [Hagerty] reports a wideband energy harvester antenna which operates from 2GHz to 18GHz using a small antenna array. Their antenna array is shown in Figure 4.1.3. The antenna is used for wideband energy harvesting; however, the efficiency is fairly poor.

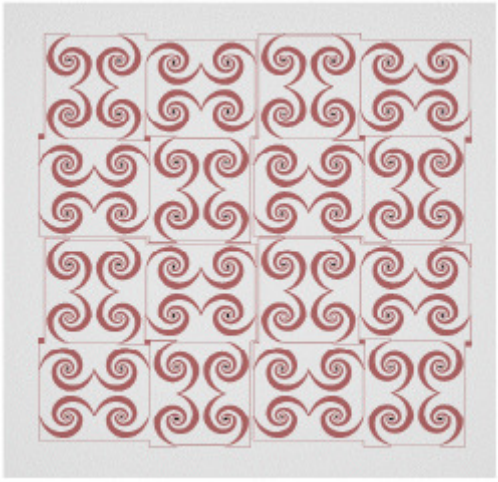


Figure 4.1.3 Antenna array of [Hagerty].

4.1.4 Characteristics of Available RF Ambient Energy Sources

There is ambient radio frequency (RF) electromagnetic power widely available for energy harvesting in urban areas. RF power is spread in different frequency regions at various power levels. For example, FM radio operates within the frequency range from 65-108 MHz. CDMA 2000 operates between 776-794MHz. CDMAone and GSM850 operate at frequencies ranging from 869-960 MHz. GSM1800 operates within 1805-1880MHz. GSM1900, CDMAONE, and WCDMA operate in the 1930-1990 MHz band. WCDMA also operates in the frequency range 2110-2170 MHz. Additionally, there are Bluetooth devices which operate at ISM frequencies which lie between 2400-2480 MHz.

Ambient RF electromagnetic energy is another promising power source for harvesting due to its wide availability in urban areas and the amount of power represented. The ambient RF energy can be harvested to power electronics directly or to charge batteries to extend their lifetimes. A previous survey [Salter2009] analyzes the RF power distribution in the frequency band from 400MHz to 5GHz. The results show there are two primary

power peaks at 900MHz and 1.8GHz. Most of the ambient RF power lies within those two frequency bands.

Previous work [Le2008] reports better than 10% conversion efficiency in a single narrow frequency band (890 MHz) for input power as low as -20 dBm; the same study shows that conversion efficiencies drop rapidly and approach zero when the frequency deviates away from the designed resonant frequency. Such an approach is thus not optimized to harvest all the existing RF ambient energy since the RF power can be widely spread over the frequency domain and there are multiple higher-power peaks within different frequency bands.

4.1.5 Strategy

In this work, we investigate a system architecture to take full advantage of the all the available environmental RF energy. Instead of seeking a maximum efficiency within one narrow frequency band, we are seeking to maximize the amount of power and conversion efficiency at all frequencies at the same time.

Because of the widely distributed energy in different frequency domains, in the remainder of this chapter, we first investigate various existing wideband energy harvesting schemes and demonstrate their theoretical difficulties. We show that dual-/multi-band energy harvesting systems are more suitable for RF energy harvesting because most ambient RF power lies in multiple bands. System specifications are been defined based on mobile device power requirements, and two different harvester architectures are shown to convert RF energy across the multiple frequency bands. Following the presentation of these architectures, designs are evaluated based on the available ambient RF power and aforementioned device requirements.

4.2 Dual-/Multi-Band Parallel Energy Harvester

4.2.1 Narrowband Energy Harvesting Techniques

Narrowband energy harvester performance is mainly evaluated by efficiency, output voltage, and the required minimum input power. A MOSFET connected voltage doubler is widely used to perform the AC to DC conversion. In this section, we provide a detailed discussion about different techniques for low input power RF energy harvesting.

4.2.1.1 Voltage Doubler Using Diode-Connected MOSFETs

Diode-connected MOSFETs are easy to fabricate in a standard CMOS process and thus are a preferred means of lowering chip costs. Figure 4.2.1 shows the circuit schematic of the CMOS connected diode voltage doubler. The C_1 and C_2 components in Figure 4.2.2 function as an AC bypass and a DC block capacitor. The C_1 and C_2 capacitances need to be much larger than ($C_{DB} + C_{GD}$) to avoid any unnecessary AC voltage drop through the bypass capacitors.

The voltage doubler uses currents I_1 and I_2 to charge the capacitors C_1 and C_2 to obtain DC output voltage at capacitor C_2. The gates of the MOSFETs are connected to the source of the MOSFET.

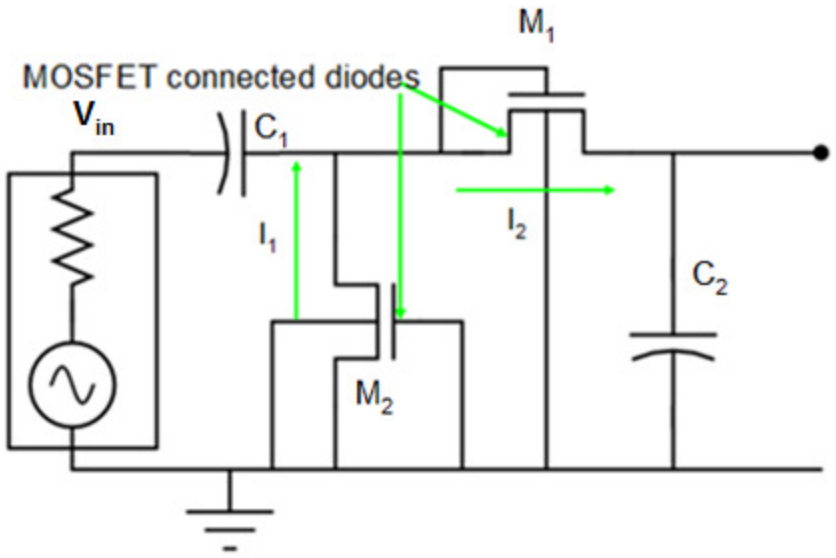


Figure 4.2.1 Voltage doubler using diode-connected MOSFETs.

In order to develop general harvester design guidelines, a MOS connected diode analysis is helpful. Figure 4.2.2 (a) and (b) show the diode-connected MOSFET and the lumped model of the diode connected CMOS, respectively, while R_G models the gate impedance of the MOSFET. The gate resistance is due to poly resistance and can be reduced by layout techniques. The underlying mathematical model can be found in [Xiaodong1998]. R_{ch} models the channel impedance of the MOSFET; this is a function of the threshold voltage of the MOSFET as well as the input signal voltage V_{in}. V_{in} is determined by the input power and the capacitance C_{DB} and C_{GS}. Figure 4.2.2 (c) shows the simplified circuit of the original circuit shown in panel (b), where a transformation of series RC network to parallel RC network is performed. Applying the transformation Equation C.7 in Appendix C under the condition of small gate resistance ($\omega^2 C_p^2 R_p^2 >> 1$),the series connected components R_G and C_{GS} in Figure 4.2.2 (b) can be transformed to be parallel connected, leading to the terms C_{GS} and R_{Gp}:

$$R_{Gp} = \frac{1}{\omega^2 C_{GS}{}^2 R_G} \tag{4.2.1}$$

In order to obtain good conversion efficiency, the power loss due to the gate impedance needs to be minimized. The power loss due to gate impedance is described by Equation 4.2.2:

$$P_{loss} = \frac{V_{in}^2}{R_{Gp}} = \omega^2 C_{GS}{}^2 R_G V_{in}^2 \tag{4.2.2}$$

The power through the diode that is used for energy harvesting is described by Equation 4.2.3:

$$P_{diode} = \frac{V_{in}^2}{\overline{R}_{ch}} \tag{4.2.3}$$

The power loss due to gate resistance needs to be much less than harvesting power:

$$P_{loss} << P_{diode} \tag{4.2.4}$$

By substituting Equation 4.2.2 and 4.2.3 into Equation 4.2.4, we obtain:

$$\omega^2 C_{GS}{}^2 R_G V_{in}^2 << \frac{V_{in}^2}{\overline{R}_{ch}} \tag{4.2.5}$$

Equation 4.2.5 can be further simplified to Equation 4.2.6, which indicates that the parasitic gate resistance needs to be sufficiently small to satisfy Equation 4.2.6.:

$$R_G << \frac{1}{\omega^2 C_{GS}{}^2 \overline{R}_{ch}} \tag{4.2.6}$$

For a well-designed voltage doubler, the unwanted power losses due to R_G (gate impedance) need to be minimized. The gate resistance can be minimized by multi-finger layout techniques. At a power level of -20 dBm, which is the aim of this work, the loss

due to gate resistance is negligible after the use of multi-finger techniques and a careful layout. The layout of the multi-fingered MOSFET is shown in Figure 4.2.5. Thus, the diode-connected MOSFET lumped model can be simplified to Figure 4.2.2 (d) where C_T is equal to the sum of C_{GS} and C_{DB}.

The non-linearity of the diodes is described by the ideal diodes and R_{ch} in the lumped model, as shown in Figure 4.2.2 (d).

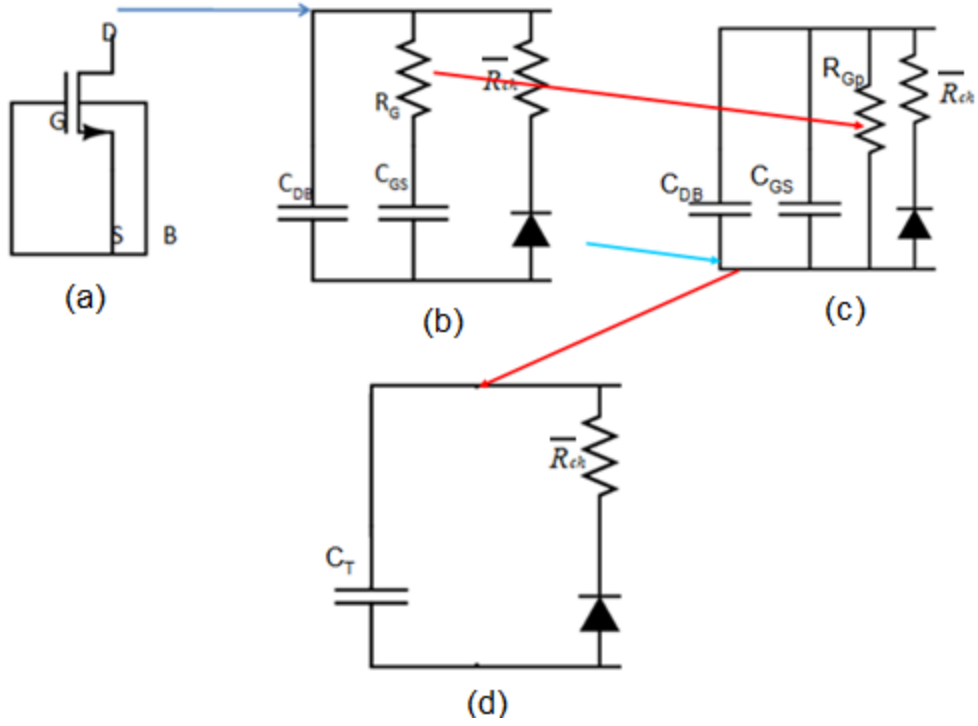
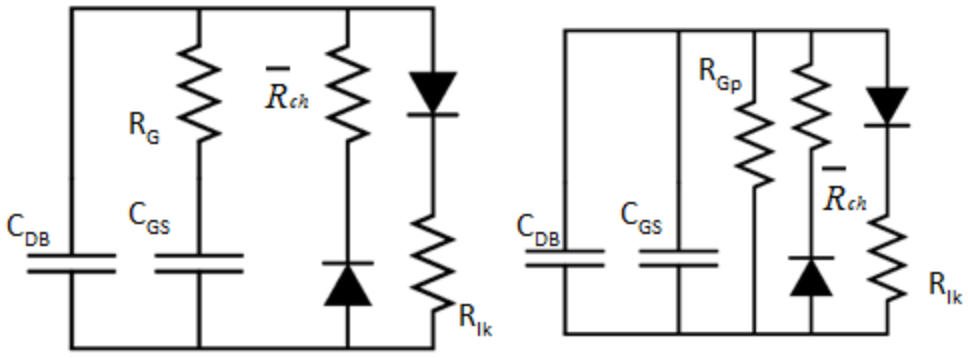


Figure 4.2.2 Model of the CMOS connected diode. (a) Diode-connected MOSFET. (b) Lumped model of the diode-connected MOSFET. (c) Lumped model of the diode-connected MOSFET after series to parallel transformation. (d) Simplified lumped model of diode-connected MOSFET.

The reverse biased leakage current of the diode-connected MOSFET is included in Figure 4.2.3 (a) and (b), where R_{lk} models the leakage of DC current. This is a function of

the threshold voltage, the biasing voltage at the gate, and the input signal V_{in}. The leakage current is much smaller than the DC current at the power input level of interest, and thus the term R_{lk} is ignored in the analysis below, unless otherwise specified.



(a) (b)

Figure 4.2.3 (a) Lumped model of the CMOS connected diode with leakage current. (b) Lumped model of the CMOS connected diode using series to parallel transformation.

By replacing the diode-connected MOSFETs (M1 and M2) in Figure 4.2.1 with the simplified lumped model given in Figure 4.2.2 (d), the equivalent circuit is given in Figure 4.2.4.

With the equivalent circuit ascertained, we can find the maximum DC output voltage of the diode connected voltage doubler as follows. The voltage at node 2 is equal to the voltage at node 1 (input voltage (V_{in})) plus the DC voltage across the capacitor C_1 (V_{C1}):

$$V_2 = V_{in} + V_{C1} \qquad 4.2.7$$

Assuming the diodes are ideal diodes with threshold voltage V_{th}, the diode can only forwardly turn on when the voltage at node 2 is less than the voltage at ground (zero) minus threshold voltage (V_{th}). This can be mathematically described by Equation 4.2.8:

$$V_2 \leq 0 - V_{th} \tag{4.2.8}$$

By substituting Equation 4.2.7 into Equation 4.2.8, the maximum DC voltage across capacitor C_1 is given by Equation 4.2.9:

$$V_{C1} \leq V_{in} - V_{th} \tag{4.2.9}$$

By applying the same methodology to diode D_2, the output voltage V_{out} is given by:

$$V_{out} \leq 2(V_{in} - V_{th}) \tag{4.2.10}$$

For ideal diodes where V_{th} is equal to zero, Equation 4.2.10 indicates the maximum output voltage is twice the input voltage.

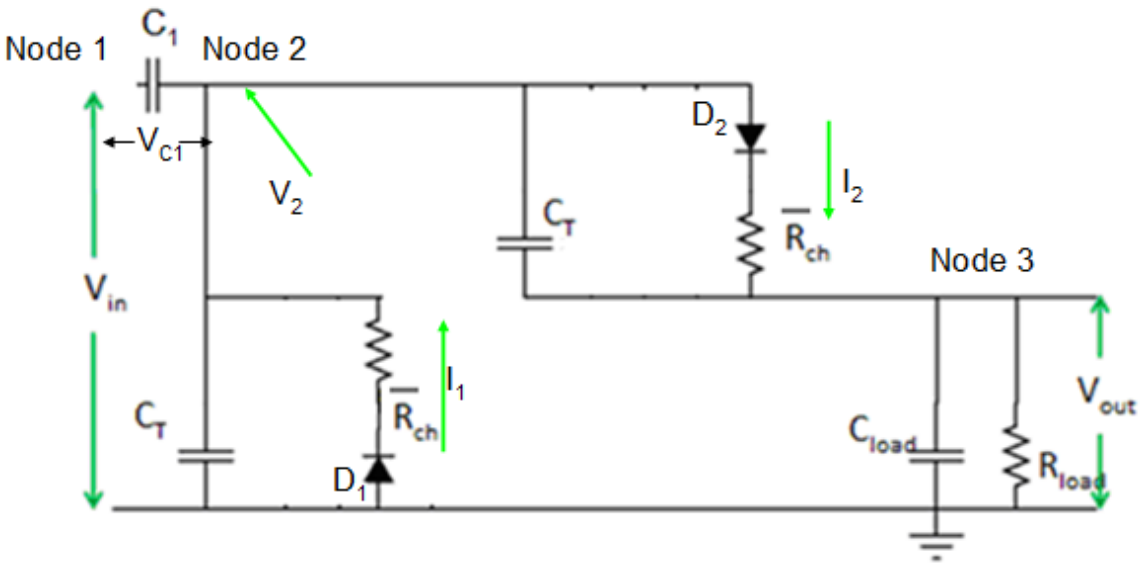


Figure 4.2.4 Equivalent circuit model of the MOSFET connected doubler.

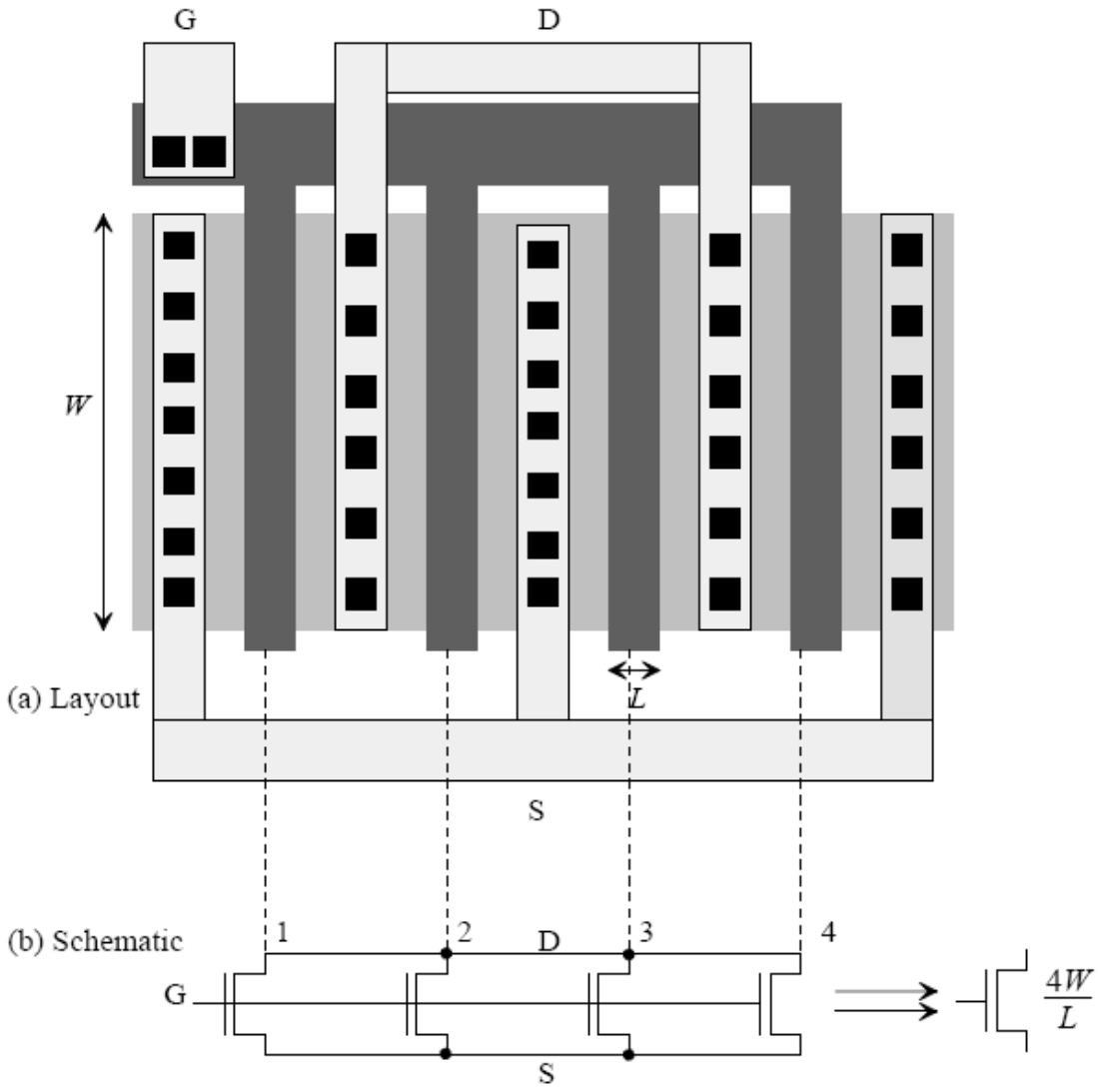


Figure 4.2.5 Layout of multi-fingered MOSFET [Baker2007]

4.2.1.2 Voltage Doubler with Boosting Circuit and Pre-set Biasing Network

The voltage doubler uses currents I_1 and I_2 to charge capacitors C_1 and C_2 as described in Figure 4.2.1. These currents (I_1, I_2) need to be as large as possible to obtain high AC to DC conversion efficiency. The current of a diode-connected MOSFET in the subthreshold voltage region can be described by Equation 4.2.11 [Razavi2000], and V_{ds} is equal to V_{gs} since the gate and drain are connected together:

$$I_1(t) = \frac{W_{eff}}{L_{eff}} \mu C_d V_T^2 \exp(\frac{V_{ds}(t) - V_{th}}{nV_T}) \left[1 - \exp(-\frac{V_{ds}(t)}{V_T}) \right] \quad 0 < V_{ds}(t) < V_{th} \qquad 4.2.11$$

In low RF input power applications, the available ambient energy is on the order of -20 dBm, which corresponds to a 31.6 millivolt input voltage for a 50 Ohm matching resistance. However, V_{th} is a few hundred millivolts for diodes. Since the AC voltage is smaller than the threshold voltage, the current is exponentially proportional to the applied AC voltages and inversely proportional to the threshold voltage as described by Equation 4.2.11. There are two possible solutions for increasing the current: boosting the input AC voltage and/or reducing the DC threshold voltage. Both methods will be discussed in the following sections.

4.2.1.2.1 Boosting Input Voltage

The voltage doubler design has been modified to include voltage boosting circuit components (R_s and L_1) in Figure 4.2.6 (a). The voltage boosting mechanism is analogous to the series RLC network in Figure 4.2.6 (b). At input signal frequency, the matching inductor (L_1) and source resistance (R_S) in Figure 4.2.6 (a) are analogous to R_A and L_A in Figure 4.2.6 (b). As will be explained below, the circuit components in the yellow box function as a high quality capacitor at low input power level (-20dBm) for AC operation. The concept can be explained using the MOSFET lumped model shown in Figure 4.2.2 (d). By replacing the diode-connected MOSFETs (M_1 and M_2) in the yellow box with the simplified lumped model shown in Figure 4.2.2 (d), the AC equivalent circuit in the yellow box in Figure 4.2.6 (a) is given in Figure 4.2.7 (a).

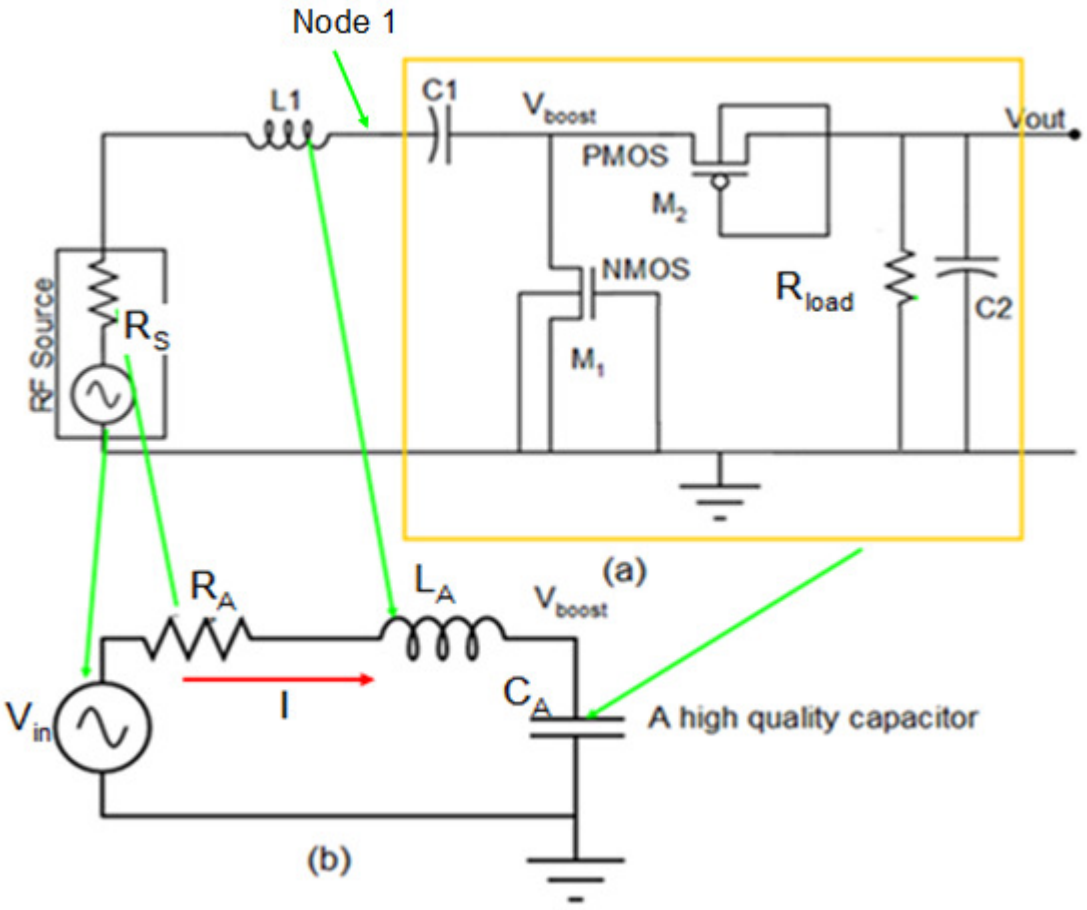


Figure 4.2.6 (a) Voltage doubler with voltage boosting. (b) Analogous series RLC voltage boosting circuit.

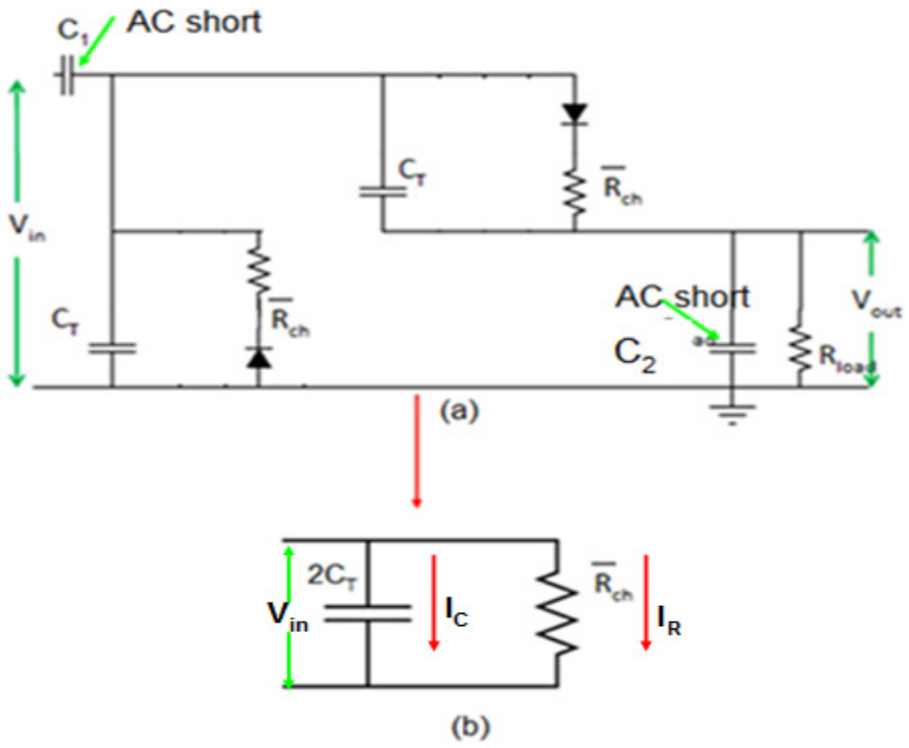


Figure 4.2.7 (a) Lumped model of the MOS based voltage doubler. (b) Simplified lumped model at signal frequency (ω_1)

At input signal frequency ω_1, the circuit in Figure 4.2.7 (a) can be simplified to the circuit in Figure 4.2.7 (b) by replacing the AC coupling capacitors (C_1, C_2) with shorts. The term $2C_T$ in Figure 4.2.7 (b) comes from the parallel connection of the two capacitors (C_T). However, only one diode is turned on, thus the average resistance is equal to R_{CH}.

The voltage boosting mechanism across the capacitor in the RLC network shown in Figure 4.2.6 (b) is described below. At resonant frequency, the current is described by Equation 4.2.12:

$$I = \frac{V_{in}}{R + j\omega_r L_A + \frac{1}{j\omega_r C_A}} = \frac{V_{in}}{R}$$

$$\omega_r = \sqrt{\frac{1}{L_A C_A}} \qquad 4.2.12$$

The voltage across the capacitor C (V_C) at resonant frequency is described by Equation 4.2.13 (the current (I) is the same for series connected RLC network):

$$|V_C| = |I \times Z_C| = \frac{1}{\omega C_A R_A}|V_R| = \frac{1}{\omega C_A R_A}|V_{in}| = Q|V_{in}| \qquad 4.2.13$$

When Q > 1, the voltage across the capacitor is larger than the input voltage at the resonant frequency. This is also known as voltage boosting and Q is known as the quality factor of the network.

With the equivalent circuit ascertained and simulation results obtained, we can demonstrate that the circuit in the yellow box functions as high quality capacitor and thus the voltage boosting mechanisms of Figure 4.2.6 (a) and (b) are the same.

As shown in Figure 4.2.7 (b), the circuit in the yellow box is equivalent to a parallel connected capacitor ($2C_T$) and resistor (R_{ch}). The quality factor of the parallel connected RC network in Figure 4.2.7 (b) which is the equivalent circuit of the yellow box in Figure 4.2.6 (a) is given by Equation 4.2.14 (a)(based on [Lee2003])

$$Q = 2\omega C_T \overline{R}_{ch} >> 1 \qquad \text{(a)}$$

$$\overline{R}_{ch} >> \frac{1}{2\omega C_T} \qquad \text{(b)} \qquad 4.2.14$$

where Equation 4.2.14 (b) is a rearrangement of Equation 4.2.14 (a).

For the parallel RC network, the quality factor can be defined as the ratio of the current through capacitor (I_C) and the current through resistor (I_R).

Since voltages across the capacitor and resistor are the same in Figure 4.2.7 (b), current I_C and I_R is described by Equation 4.2.15:

$$\left|I_R\right| = \left|\frac{V_{in}}{\overline{R}_{ch}}\right| \quad \text{(a)}$$

$$\left|I_C\right| = \left|\frac{V_{in}}{Z_C}\right| = \left|2V_{in}\omega C_T\right| \quad \text{(b)} \qquad 4.2.15$$

By Dividing Equation 4.2.15 (a) with Equation 4.2.15 (b), we obtain Equation 4.2.16:

$$\frac{\left|I_C\right|}{\left|I_R\right|} = \left|\frac{V_{in}}{Z_C}\right| = \left|2\omega C_T \overline{R}_{ch}\right| = Q \qquad 4.2.16$$

Equation 4.2.16 indicates that the ratio of the current through the capacitor and the current through resistor is the quality factor for the parallel connected RC network.

Substituting Equation 4.2.16 into Equation 4.2.14 (a), we obtain the requirement of high quality parallel RC network in the form of the current ratio:

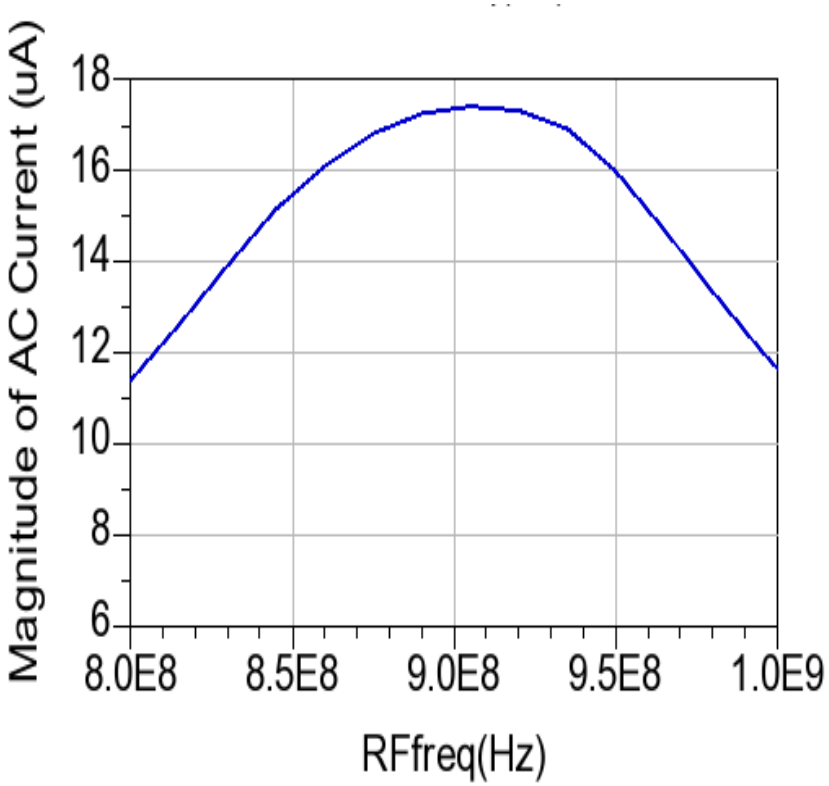
$$\frac{\left|I_C\right|}{\left|I_R\right|} >> 1 \qquad 4.2.17$$

In low input power applications (e.g., at -20 dBm), the relationship between the current through the capacitor and the channel resistance as described by Equation 4.2.17 holds. This statement is validated by the simulation results. Figure 4.2.8 panels (a) and (b) show the simulated current through capacitor (AC) and the current through channel resistor

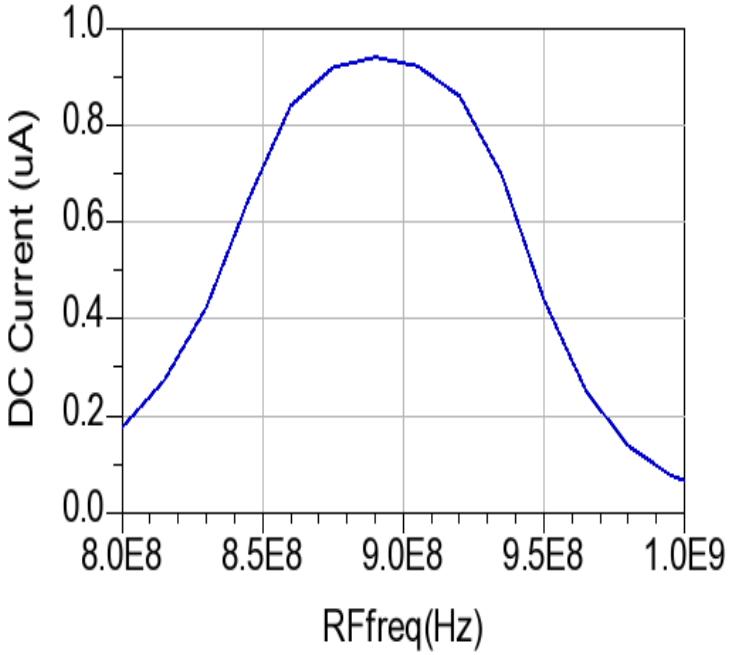
(DC) of the designed voltage doubler for input power of -20 dBm. The AC current shown in Figure 4.2.8 (a) is much larger than the DC current shown in Figure 4.2.8 (b).

Figure 4.2.8 (c) shows the quality factor of the equivalent capacitor for the circuit in the yellow box shown in Figure 4.2.6 (a). The quality factor is about 20 at the resonant frequency, but can be as high as 100 at other frequencies. At the resonant frequency, the voltage boosting generates high voltage and thus the diode obtains high current and has a lower quality factor; the boosting voltage decreases as the frequency moves away from the resonant frequency, which causes less current through diode and thereby realizes a higher quality factor. Of course we want DC current through the diode to be large which will requires the boost voltage to be high. However, high DC current will lower the quality factor and thus cause lower DC current. There thus has an optimal point for maximize the AC to DC power conversion.

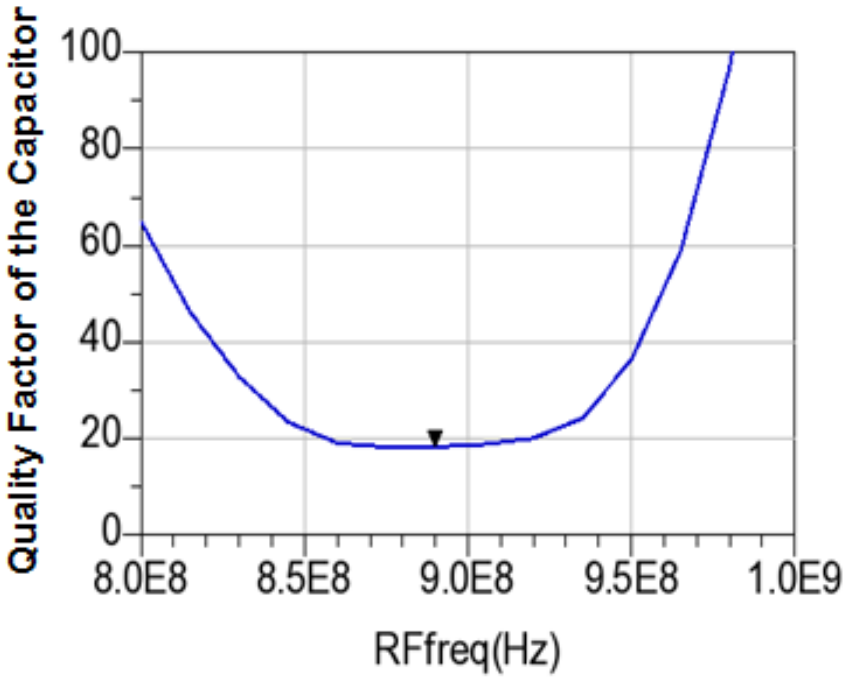
The analysis result that the voltage doubler functions as a high quality capacitor helps to explain measurements taken by Le et al. [Le2008], wherein the impedance from C_T is more than ten times larger than the series impedance at frequency ω_1.


Magnitude of AC Current (uA)
18
16
14
12
10
8
6
8.0E8
8.5E8
9.0E8
9.5E8
1.0E9
RFfreq(Hz)

(a)


DC Current (uA)
1.0
0.8
0.6
0.4
0.2
0.0
8.0E8
8.5E8
9.0E8
9.5E8
1.0E9
RFfreq(Hz)

(b)



(c)

Figure 4.2.8 (a) Magnitude of I_1 for different input signal frequencies. (b) Magnitude of the DC component of I_1 for different input signal frequencies. (c) Ratio of the AC component and the DC component of the current I_1 for different input signal frequencies.

In summary, the voltage across the MOSFET at the input signal frequency is boosted through the RLC network because the diode-connected MOSFET contributes a small series capacitance as shown in Figure 4.2.7 (b). In conclusion, by taking the parasitic capacitance of the MOSFET which is generally unwanted, we can extract RF power at voltages which is way below the standard diode threshold level.

4.2.1.2.2 Pre-set Voltage

Another way to increase the currents I_1 and I_2 is to reduce V_{th} by supplying pre-set gate biasing voltages as shown in Figure 4.2.9 using a self-biasing network. There exists an optimal gate biasing voltage. The reason can be explained as follows: When the pre-set gate voltage is low, the diodes are difficult to turn on and thus there is low current; however, when a pre-set bias gate voltage is higher than the threshold voltage, the diode connected MOSFET turns on all the time and thus stops functioning as a diode. Thus, we need to establish an optimized self-biasing voltage.

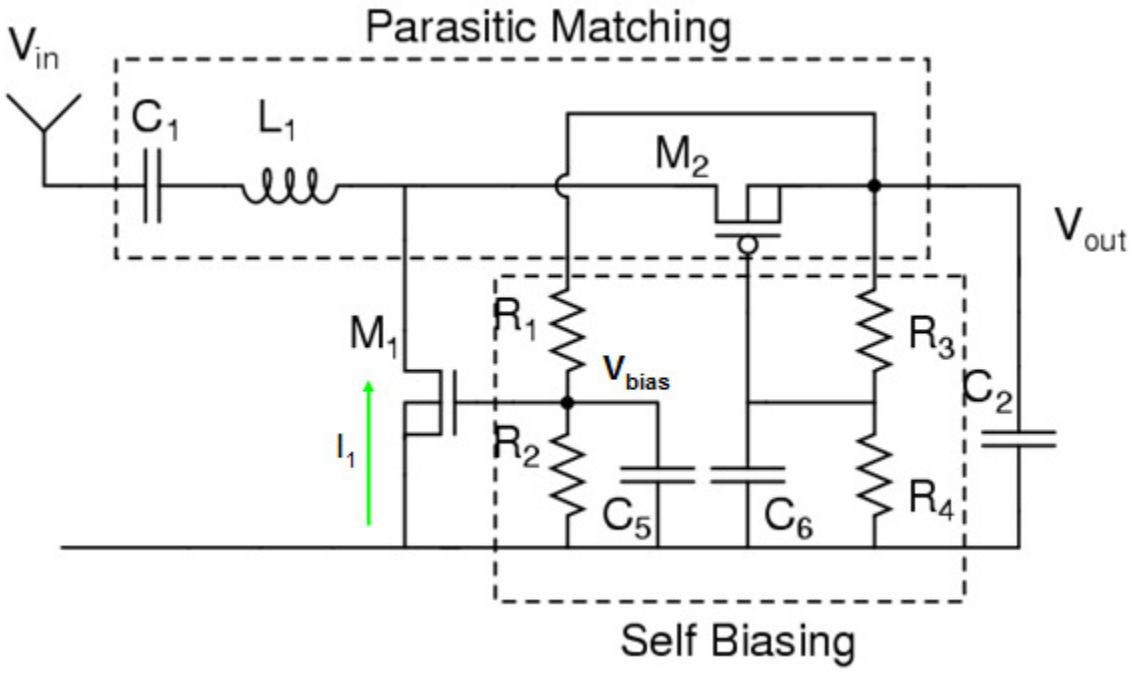


Figure 4.2.9 Voltage doubler with pre-set DC gate biasing.

4.2.1.2.3 Output Voltage

The maximum output voltage of the voltage doubler with boosting network can be calculated in two steps: First, the voltage across the diode-connected MOSFETs is boosted as described by Equation 4.2.13. Next, the voltage doubler then doubles the boosted voltage as described by Equation 4.2.10. Substituting Equation 4.2.13 into

Equation 4.2.10, the maximum output voltage of the single stage voltage doubler with voltage boosting is given by Equation 4.2.18:

$$V_{out} \le 2\times(QV_{in} - V_{th}) \qquad 4.2.18$$

Where Q is the quality factor of the boosting network.

Equation 4.2.18 indicates that the output voltage of the voltage doubler with boosting network increases with the usage of the boosting network.

4.2.1.3 Cascade Voltage Doubler

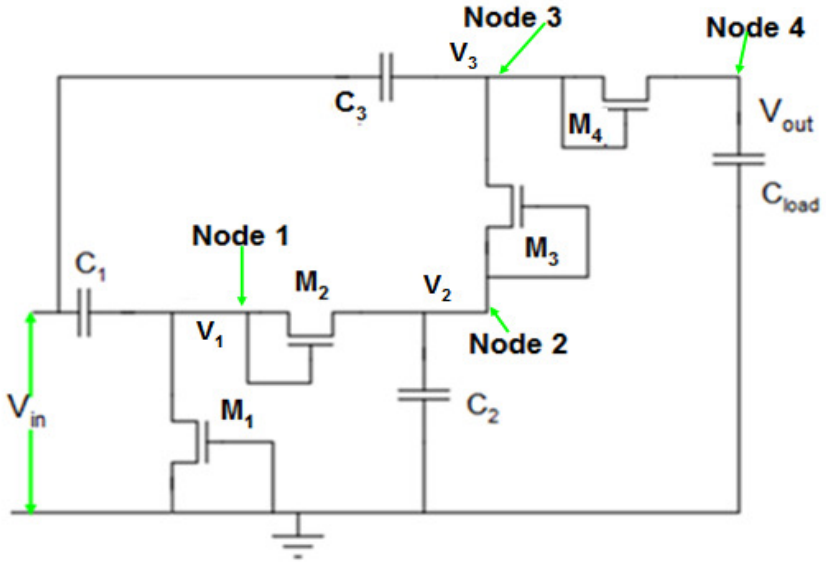
For -20 dBm input power, the output voltage of the voltage doubler is quite a bit lower than the desired 1V level despite all the various additional techniques that have been implemented to boost the voltage. This is because the output voltage cannot exceed twice the input voltage. There are different DC to DC conversion methods capable of generating 1V of output voltage. Salter et al. [Salter2009] used a switch capacitor method to control the discharging duty circle to achieve a 1V output voltage using a one stage voltage doubler. However, the switch capacitor based DC to DC converter needs separate power to generate the control clocks.

The DC to DC conversion can also be implemented by cascading several voltage doublers together to generate 1V output voltage. Figure 4.2.10 (a) is a circuit schematic for a two-stage cascade voltage doubler. Figure 4.2.10 (b) shows the lumped model of the two-stage cascade voltage doubler. The equivalent circuit at AC signal frequency ω_1 can be obtained by replacing the capacitors C_1, C_2, C_3 and C_{load} with AC shorts. The equivalent circuit at frequency ω_1 is shown in Figure 4.2.10 (c). Since each voltage doubler stage is connected in parallel, the input capacitance and resistance are described by the following equations for a multi-stage voltage doubler cascade harvester:

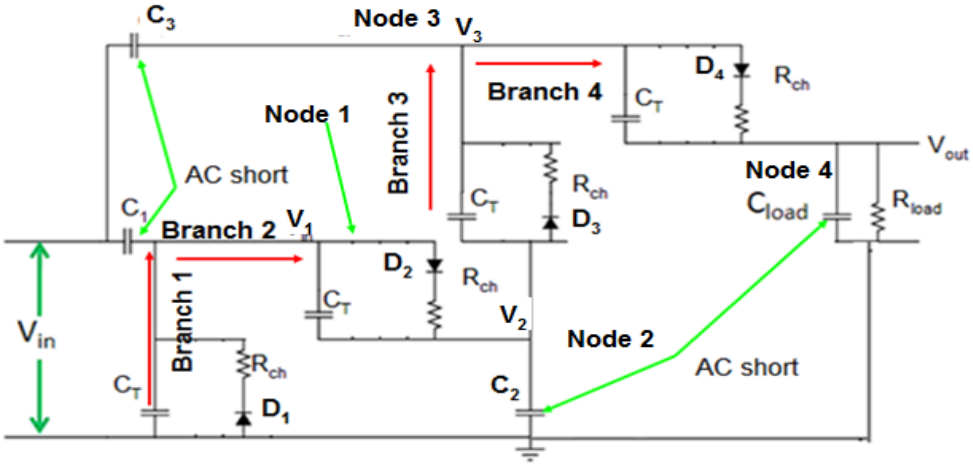
$$C_n = 2n \times C_T$$

$$R_n = \frac{\overline{R}_{ch}}{n} \qquad 4.2.19$$

where n is the number of stages, and C_T and R_T are the input capacitance and resistance respectively, for the one stage voltage doubler.



(a)



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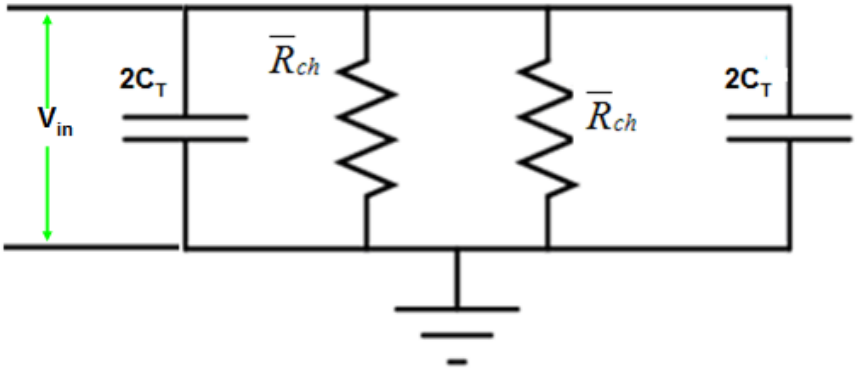


(c)

Figure 4.2.10 (a) A two stage cascade voltage doubler. (b) Equivalent circuit of the two cascade voltage doubler. (c) Equivalent circuit of the two cascade voltage doubler at AC signal frequency.

With the equivalent circuit ascertained in Figure 4.2.10 (b), we can find the maximum DC output voltage of the cascaded diode connected voltage doubler as follows. The voltage at node 2 is the maximum DC voltage for single stage voltage doubler and is described by Equation 4.2.20:

$$V_2 \leq 2(V_{in} - V_{th}) \qquad 4.2.20$$

The voltage at node 3 equal to input voltage (V_{in}) plus the DC voltage across the capacitor C_3 (V_{C3}):

$$V_3 = V_{in} + V_{C3} \qquad 4.2.21$$

Assuming the diodes are ideal diodes with threshold voltage V_{th}, the diode can only forwardly turn on when the voltage at node 3 is less than the voltage at node 2 minus threshold voltage (V_{th}). This can be mathematically described by Equation 4.2.22:

$$V_3 \leq V_2 - V_{th} \tag{4.2.22}$$

By substituting Equation 4.2.20 and 4.2.21 into Equation 4.2.22, the maximum DC voltage across capacitor C_1 is given by Equation 4.2.23:

$$V_{C1} \leq 3(V_{in} - V_{th}) \tag{4.2.23}$$

By applying the same methodology to diode D_2, the output voltage V_{out} is given by:

$$V_{out} \leq 4(V_{in} - V_{th}) = 2 \times (2V_{in} - 2V_{th}) \tag{4.2.24}$$

The same methodology can be applied to a *n*-stage cascaded voltage doubler and the maximum output voltage is given by:

$$V_{out} \leq 2n(V_{in} - V_{th}) \tag{4.2.25}$$

Equation 4.2.25 indicates that the output voltage increases as the number of cascades stages increases. In other words, the cascaded voltage doubler design is capable to generate higher output voltage.

4.2.1.4 Cascade Voltage Doubler with Boosting Circuit

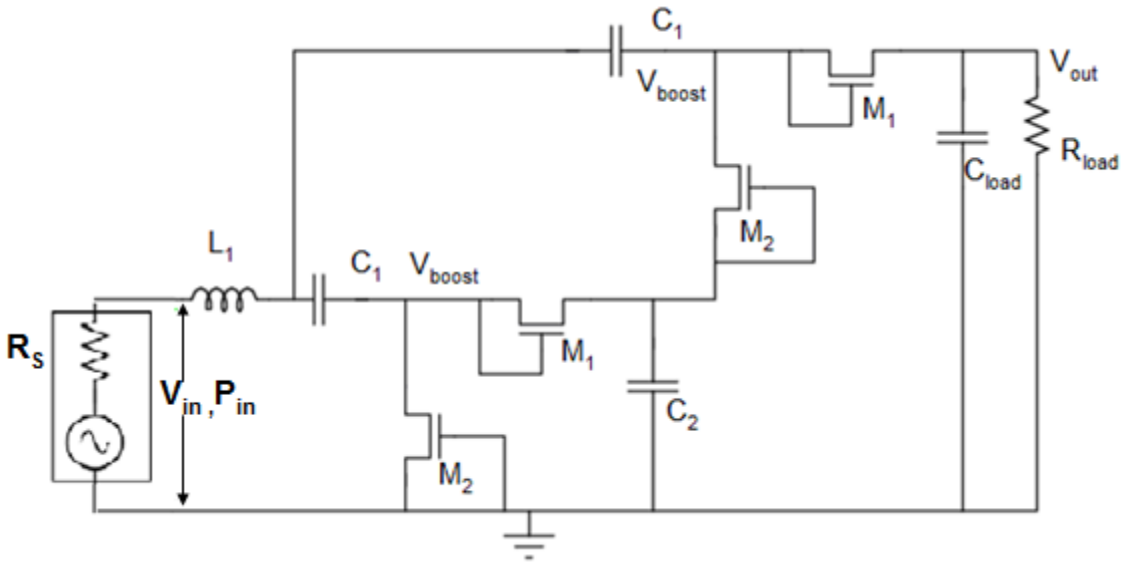


Figure 4.2.11 Cascade voltage doubler with boosting circuit.

In order to obtain high conversion efficiency with the desired DC output voltage (>1V) at power as low as -20 dBm, the methodology of using a cascade voltage doubler design with an additional boosting circuit appears to have promise. Figure 4.2.11 shows the cascade voltage doubler with a boosting circuit. The circuit analysis can be divided into two steps. First, the voltage boosting circuits generates a boosting voltage V_{boost}; second, the cascaded stages perform DC to DC conversion.

The input signal is boosted via the same mechanism as used for the single stage voltage doubler with a boosting network. The boosting voltage is given by Equation 4.2.26 as explained earlier:

$$V_{boost} = \frac{1}{\omega C_{total} R_S} V_{in} = Q V_{in} \qquad 4.2.26$$

Where C_{total} is the capacitance of the cascaded multi-stages voltage doubler and R_s is the antenna impedance.

The output voltage of the cascaded voltage doublers with voltage boosting is calculated similarly to the method in the previous section; the only difference is that the input AC voltage has been boosted. The output voltage can thus be obtained by replacing the input voltage by the boosting voltage in Equation 4.2.25 to obtain:

$$V_{out} \le 2n \times (V_{boost} - V_{th}) = 2n \times (QV_{in} - V_{th})$$
$$V_{boost} = QV_{in} \qquad 4.2.27$$

Where Q is the quality factor of the boosting network, n is the number of cascade stages, V_{th} is the threshold voltage of the diodes, and V_{in} is the input voltage. Equation 4.2.27 describes the relationship among the output voltage, the input power, diode threshold voltage, the number of the cascade stages, and the voltage boosting ratio and demonstrate that the higher the quality factor, the higher the output voltage. This analysis also shows that the larger the number of stages, the higher the output voltage.

4.2.1.5 Antenna Coupled Cascade Voltage Doubler with Boosting Circuit

The matching impedance of the antenna and the energy harvester is generally designed to be 50 Ohm. For example, Umeda et al. [Umeda2006] discuss an antenna designed for 50 Ohm impedance at the resonant frequency. The reason for the 50 Ohm matching impedance is that this choice provides ease of connection between the antenna and energy harvester via a transmission line as well as using SMA connectors. Since the antenna can connect to the energy harvester directly, maximum power transfer between antenna and energy harvester will be achieved if the impedance is matched between the antenna and the energy harvester. The matching impedance of the energy harvester only needs to be the complex conjugate of the antenna impedance. In theory, this value is not limited to 50 Ohm precisely. The matching impedance can be used as a system design parameter to optimize the AC to DC conversion efficiency. This idea is depicted in

Figure 4.2.12 in which the system design allows optimization of the efficiency by varying the antenna impedance. Below is a simple example to show that impedance matching can affect the boosting voltage and thus the conversion efficiency:

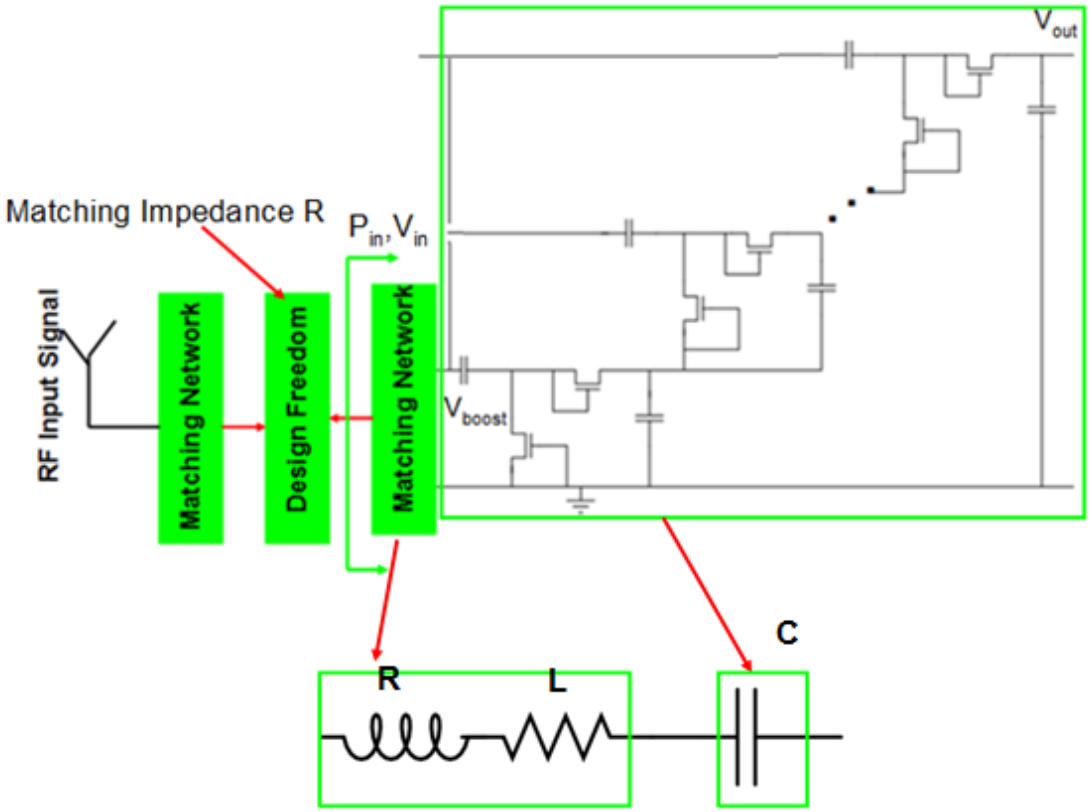


Figure 4.2.12 Antenna coupled cascade voltage doubler with boosting circuit.

The relationship between the input voltage and the input power is described by Equation 4.2.28:

$$P_{in} = \frac{V_{in}^2}{2R}$$
$$V_{in} = \sqrt{2RP_{in}} \qquad 4.2.28$$

Where R is the matching impedance of the system and P_{in} is the signal power at the end of the antenna.

The matching circuit in Figure 4.2.12 is similar as discussed before (the matching network functions as series connected resistor and inductor while cascaded doubler circuit functions as high quality capacitor). The improvement in this topology is that the matching impedance is an optimization parameter instead of standard 50 Ohms as discussed previously. Similar to the previous discussion on voltage boosting, the voltage across the capacitor after the RLC network voltage boosting network is applied at the resonant frequency as given by Equation 4.2.29:

$$V_{boost} = QV_{in} = \frac{1}{\omega_{res} CR}\sqrt{2RP_{in}} = \frac{\sqrt{\frac{L}{C}}}{R}\sqrt{2RP_{in}} = \sqrt{\frac{2LP_{in}}{RC}} \qquad 4.2.29$$

$$\omega_{res} = \sqrt{\frac{1}{LC}}$$

Where R is the matching impedance of the system and P_{in} is the signal power transferred into the harvester.

Equation 4.2.29 shows that the voltage across the capacitor is inversely proportional to the square root of the matching impedance of the system. The lower the series resistance R is, the higher the boosting voltage is. For example, if the antenna is designed to work with 10 Ohm instead of 50 Ohm matching, the voltage across the capacitor can be boosted to a voltage $\sqrt{5}$ times higher than the boosting voltage, while the harvester and the antenna can still operate with 50 Ohm matching. This means the harvesting circuit can generate the same voltage and obtain the same efficiency with 7 dB lower input power than the 50 Ohm matching energy harvester can for low power applications while the power is approximately lower than -10 dBm. Equation 4.2.29 also shows that the boosting voltage can be infinite if the matching impedance of the system is zero.

However, the antenna efficiency decreases to zero with zero-radiation resistance since the antenna efficiency is described by Equation 4.2.30 [Balanis2005]:

$$\eta_{ant} = \frac{R_{rad}}{R_{rad} + R_{Ohm}} \qquad 4.2.30$$

Here η_{ant}, R_{rad}, and R_{Ohm} are the antenna efficiency, antenna radiation resistance , and antenna Ohmic resistances . R_{Ohm} represents power losses due to the antenna metal resistance , which is generally less than 1 Ohm. R_{rad} accounts for the radiated power of the antenna and is determined by the geometry and shape of the antenna. In most designs, R_{rad} is 50 Ohm. In order to achieve sufficient antenna efficiency, the real part of the antenna impedance needs to be larger than a reasonable minimal value. In this design, it has been determined that the real part of the antenna impedance should be larger than 10 Ohms for good performance.

4.2.2 Wideband Energy Harvesting Limitations

Due to the presence of multiple power peaks in the frequency domain of the external RF environment, a particularly attractive RF energy harvesting strategy is wideband energy harvesting, which can convert ambient energy at all frequencies.

Compared with a narrowband energy harvester, a wideband energy harvester needs to meet both the voltage boosting and wideband matching requirements over a wide frequency range. A wideband matching network is required in order to maximize the power transfer from the antenna and the harvesting circuits over a wide frequency range. The voltage boosting requirement is due to the low input power.

It is possible to obtain power matching over a wide frequency range [Ismail2004], but this work does not allow for high voltage boosting. It is also possible to obtain voltage

boosting through a narrow band high quality factor network [Lee2003]. However, it is unlikely that wideband power matching can be attained while also obtaining voltage boosting simultaneously because the bandwidth of the boosting network is described by Equation 4.2.31 [Lee2003]:

$$BW = \frac{\omega_{resonant}}{Q} \tag{4.2.31}$$

where BW is the 3dB bandwith, Q is the quality factor, and $\omega_{resonant}$ is the central resonant frequency. This indicates that the higher the Q, the narrower the frequency bands are. At the -20 dBm power level, our analysis and simulation show that a voltage boosting ratio of 8 is required to obtain over 10% efficiency at 900MHz. From Equation 4.2.31, the bandwidth is about 110MHz, so the wideband design requirement can not be satisfied.

In summary, a wideband energy harvesting network design cannot satisfy the above two requirements for low power energy harvesting simultaneously. Therefore, such a design is not suitable for low power energy harvesting applications.

4.2.3 Analysis of Multiband Energy Harvesting

The above discussion shows that a wideband approach is unlikely to meet the dual requirements for low power energy harvesting applications over a wide frequency band. However, the available RF energy is not equally distributed over the whole frequency region, as shown by a prior survey [Salter2008]. Most of the available ambient RF energy is distributed in various narrow frequency bands (e.g., the GSM band at 1800-1880 MHz). Previous power surveys in the DC/Baltimore area show there are two primary power peaks, existing at 900 and 1800 MHz.

A multi-band energy harvester takes better advantage of the available RF ambient energy sources. We thus investigate the possibility of using a dual-band energy harvesting network to meet the requirements.

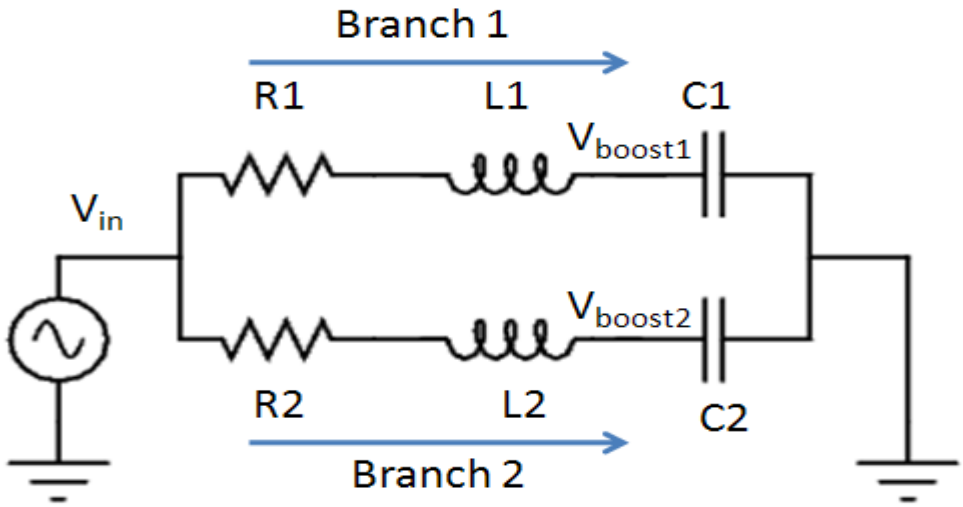


Figure 4.2.13 Schematic of the two parallel RLC dual-band boosting networks.

The idea of the dual band energy harvester is to make the impedance in one branch infinite while the other branch is at resonance, and vice versa. In this way, we obtain both power matching and voltage boosting at two frequencies simultaneously and vice-versa in another frequency. The front matching network of the energy harvester needs to provide power matching as well as voltage boosting. Figure 4.2.13 shows the circuit schematic of the dual-band matching network. The two narrow frequency bands are centered at 900MHz (ω_1) and 1800MHz ($\omega_2 = 2\omega_1$), which are the two highest power peaks in the previous survey.

Branches 1 and 2 in Figure 4.2.13 are designed to resonate at frequencies ω_1 and $2\omega_1$, respectively:

$$\omega_1 = \frac{1}{\sqrt{L_1 C_1}} \quad \text{(a)}$$

$$\omega_2 = 2\omega_1 = \frac{1}{\sqrt{L_2 C_2}} \quad \text{(b)} \qquad 4.2.32$$

At frequency ω_1, the impedances of the two branches are given by R_1,C_1,L_1 and R_2,C_2,L_2 in series, respectively.

$$R_{input1} = R_1 + j\omega_1 L_1 + \frac{1}{j\omega_1 C_1} = R_1$$
$$R_{input2} = R_2 + j\omega_1 L_2 + \frac{1}{j\omega_1 C_2} = R_2(1 - 1.5\, jQ_2) \qquad 4.2.33$$
$$Q_2 = \frac{\omega_2 L_2}{R_2}$$

Assuming an infinite Q_2, Equation 4.2.33 shows R_{input2} is equal to infinite. The network is fully described by branch 1 which is a series connected RLC network. As we discussed before, a series RLC network can provide both power matching and voltage boosting at a single frequency (ω_1). In reality, a matching network with a quality factor of 10 is achievable, and the signal losses due to branch 2 are negligible.

At frequency ω_2, the impedances of the two branches are given in the same way:

$$R_{input1} = R_1 + j\omega_2 L_1 + \frac{1}{j\omega_2 C_1} = R_1(1 + 1.5\, jQ_1)$$
$$R_{input2} = R_1 + j\omega_2 L_1 + \frac{1}{j\omega_2 C_1} = R_2 \qquad 4.2.34$$
$$Q_1 = \frac{\omega_1 L_1}{R_1}$$

Assuming an infinite Q_1, Equation 4.2.34 shows that R_{input1} is equal to infinite. The network is fully described by branch 2 which is a series connected RLC network. As we

discussed before, a series RLC network can provide both power matching and voltage boosting at a single frequency ω_2.

In other words, the topology in Figure 4.2.13 obtains power matching and voltage boosting at two different frequencies.

This approach avoids the l limitation on the bandwidth and voltage boosting of the network described by Equation 4.2.31 because the bandwidth of the matching network is 80 MHz each at the center frequencies instead of being 900MHz (900-1800 MHz) wide, as it is for the wideband matching scheme.

In summary, our analysis shows that it is possible to have two parallel connected RLC networks that obtain power matching and voltage boosting for different narrow bands. Moreover, the dual-/multi-band energy harvesting scheme is also suitable to power distribution based on an ambient RF energy source. In the next chapter, we show how to design and implement muti-band energy harvester.

4.3 Summary

In this chapter, we have investigated the possibility of using ambient power as a source for applications in which devices need to be left unattended for a long times without battery replacement. Specifically, we have discussed a narrowband energy harvester design using CMOS connected diodes and a voltage doubler topology. A detailed analysis of the voltage doubler has been provided, and our analysis and simulation results agree with most previously published results. Following the analysis of the voltage

doubler, we also analyzed the cascaded voltage doubler based harvester concept using matching impedance as a system parameter.

A previous RF energy survey in the Baltimore/Washington area showed that there are spower peaks in multiple frequency bands and that the available ambient power is relatively low (-20 dBm). Various previous works address the scenario of low input power for a single frequency band. However, such studies have not made use of all the available RF energy because ambient RF energy has power peaks in multiple frequency bands.

In order to harvest ambient RF power over a wide frequency region, we first investigated a wideband energy harvesting approach. While wideband matching would be possible with ideal components, voltage boosting requirements cannot be met over a wide frequency region in actuality. Our study also shows that it is extremely unlikely to achieve high voltage boosting over a wide frequency region even with ideal circuit components because of the relationship between voltage boosting and the bandwidth of the matching network. We conclude that wideband energy harvesting is not suitable for low power ambient energy harvesting. The discussed wideband energy harvesting techniques may be usable when high RF power is available.

Dual-/multi-band energy harvesting schemes can also take better advantage of the available RF energy because most of this energy lies across several frequency bands. More importantly, multi-band energy harvesting schemes avoid the limitation between the bandwidth and voltage boosting of a matching network when applied over a wide frequency region. In the next chapter, a design specification is given for two parallel

narrowband harvesters connected together to achieve both power matching and voltage boosting in two different bands.

Our contributions to research on multi-band energy harvesting are summarized as follows:

- Analysis of voltage doublers
- Design specification for energy harvesting in WSN applications
- Discussion of difficulty of wideband energy harvesting
- Creation of a multi-band energy harvesting scheme that uses energy harvesters connected in parallel for dual-/multi-band energy harvesting

Chapter 5: Dual-/Multi-Band RF Energy Harvester Design

5.1 Dual-/Multi-Band Energy Harvester

5.1.1 Design Specifications

Energy harvesters are emerging as a promising power solution for future mobile devices. For this to be workable, harvesters either need to power the electronics or charge the battery to meet the needs of mobile applications such as WSNs. The latest CMOS electronics can be operated with under a 1V DC supply [Ibrahim2011]. The minimal charging voltage of the battery is about 1V as well [Peckerar2011A] [Peckerar2011B]. Here the minimal input power, based on the previous RF energy survey results [Salter2009As], is chosen as -19 dBm. These input power levels are also comparable to most other recent publications [Le2008][Nakamoto2006][Umeda2006]. Based on these requirements, the harvester system specifications are defined as follows:

- The minimal input signal power is -19 dBm.
- A minimum 1V output voltage is required in order to meet battery recharging requirements [Peckerar2011A] [Peckerar2011B].
- The system needs to harvest energy at two or more frequency bands. In this work, the two frequency bands used are at 900MHz and 1800MHz which correspond to the largest power peaks according to previous surveys.

- The design needs to utilize standard CMOS technology in order to lower the costs.

5.1.2 Design for Dual-/Multi-band Energy Harvesting

Because most of the ambient RF energy lies in distinct frequency bands, multi-band energy harvester systems are more suitable for ambient energy harvesting than wideband harvesters. This scheme can also provide separate voltage boosting and power matching at different frequency bands by use of careful design.

Figure 5.1.1 shows the block diagram of the dual-/multi-band energy harvester. The two harvesters have been connected in parallel and placed on a single chip. The parallel combined harvesters obtain low impedances at their designed frequencies in order to maximize the voltage boosting and have much higher impedances at other frequencies; this is intended to minimize power losses through any other path. The same idea can be extended into multiband energy harvesting by adding different frequency energy harvesters in parallel.

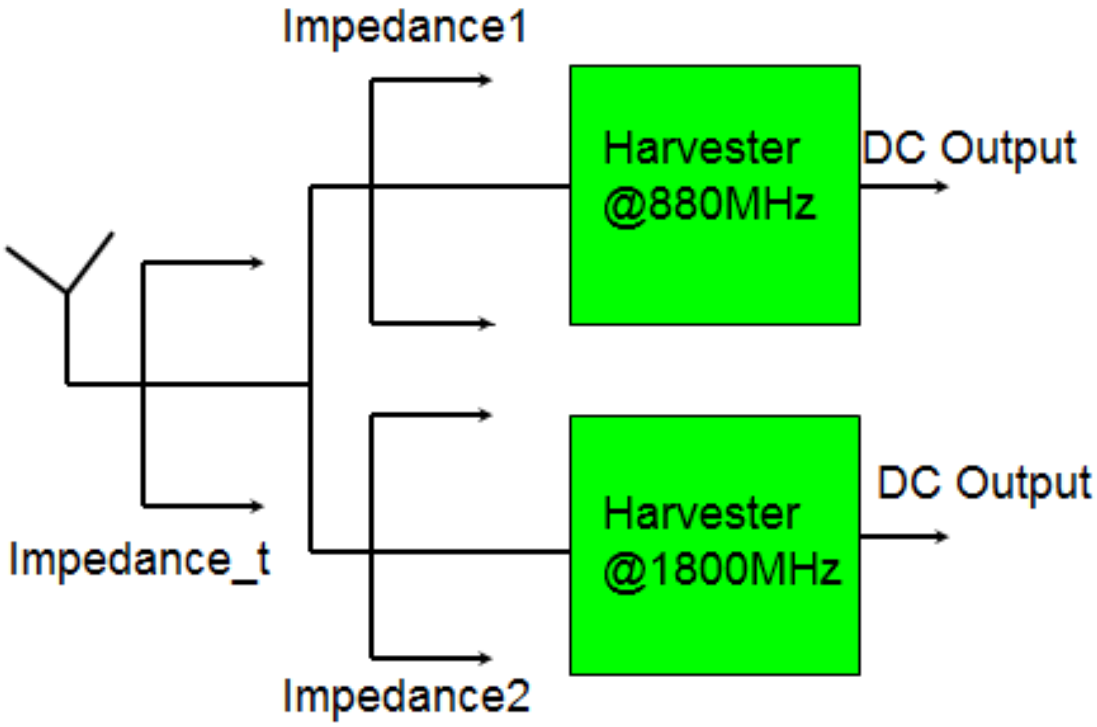


Figure 5.1.1 Structure of the parallel dual-band energy harvester.

The minimal input signal power is only -19 dBm which corresponds to a 35.5 mV input voltage using standard 50 Ohm matching. According to the design specifications listed in section 5.1.2, a minimal 1V output voltage is necessary. The energy harvester thus needs to have 30-fold AC to DC voltage boosting.

The voltage ratio (output voltage vs. input voltage) of a cascaded voltage doubler with voltage boosting can be obtained by rearranging Equation 4.2.18 and is described by Equation 5.1.1:

$$\frac{V_{out}}{V_{in}} = 2n \times (Q - \frac{V_{th}}{V_{in}}) \qquad 5.1.1$$

where Q is the quality factor of the boosting network, n is the number of cascade stages, V_{th} is the threshold voltage of the diodes, V_{in} is the input voltage, and V_{th} is the threshold voltage of the diodes which can be reduced by pre-set biasing voltages as discussed in the

previous chapter. The voltage boosting ratio combines information about the voltage transformer boosting (Q) and the number of cascaded stages.

In this design, we seek to use on-chip inductors to boost the input signal voltage. Current on-chip inductors have quality factors of less than 7. The maximum DC output voltage of a single-stage voltage doubler with -19 dBm input power is calculated by setting threshold voltage V_{th} to zero in Equation 4.2.18:

$$V_{out} < 2 \times V_{boost} \leq\!< 2 \times Q \times V_{in} = 0.497V \qquad 5.1.2$$

In real applications, since diodes always have a threshold voltage barrier even when pre-set bias voltages are provided, the voltage doubler output voltage is always less than twice the input voltage.

The impedance of the energy harvester may be used to optimize the boosting voltage to improve the harvester efficiency. Cascade voltage doublers are capacitor-like and the equivalent circuit can be replaced by a capacitor in series with a small resistor at the signal frequency as shown in Figure 4.2.5 (c). The resistance of the network is much smaller than the impedance of the capacitor, as discussed before. This subsystem functions as a low loss or high Q capacitor. Previous simulations and measurements such as by Le [Le2008] also agree with our analysis results.

Figure 5.1.2 is the circuit block diagram of the antenna coupled cascade voltage doubler with boosting circuit. In order to obtain 1V for a -19 dBm input signal, DC to DC conversion is necessary. Improved DC to DC conversion can be obtained by cascading a few voltage doublers together to obtain 1V DC voltage.

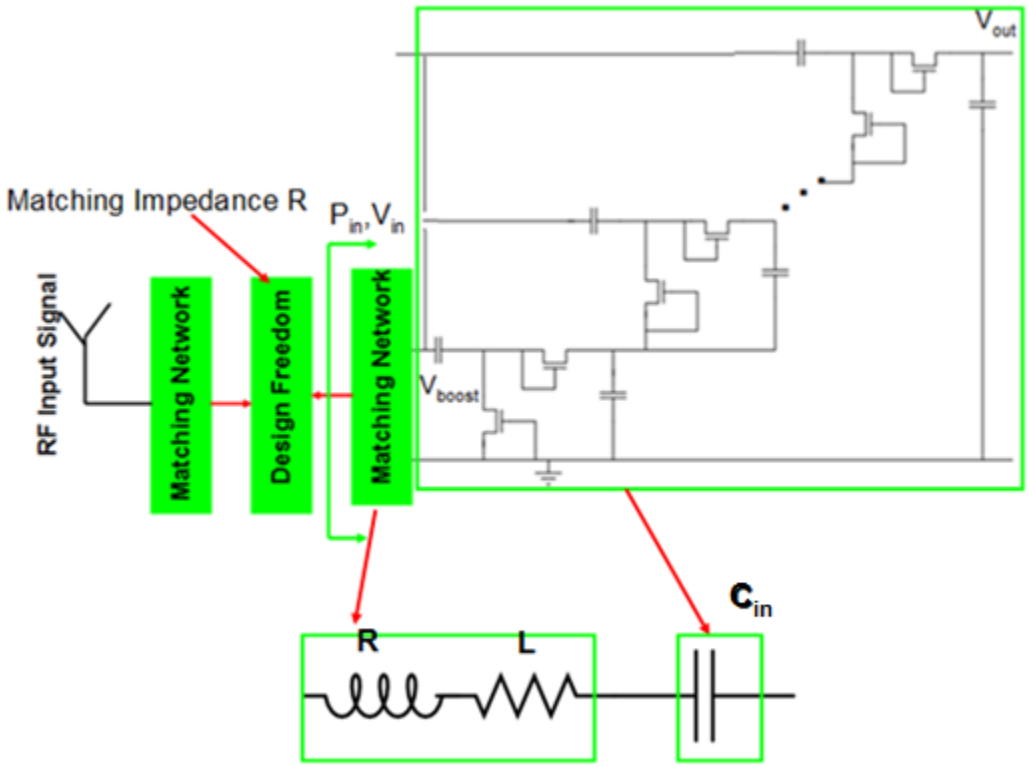


Figure 5.1.2 Antenna coupled cascade voltage doubler with boosting circuit.

Having more stages will lead to more power leakage due to the increased parasitic capacitors and resistors (C_{sub} and R_{sub}) as shown in Figure E.1. Thus, a minimal number of cascading stages needs be chosen to minimize the signal losses to the substrate. The output voltage is as high as twice the input voltage if an ideal diode is available. A minimal three-stage cascade voltage doubler can obtain 1V output for a minimal input power of -19 dBm using ideal diodes, if voltage boosting is also utilized. In reality, due to parasitic losses as well as the threshold voltage of the diodes, simulation results show that a minimum of four voltage doublers are necessary to generate greater than 1V output voltage. While a four-stage cascaded voltage doubler is chosen at 1800MHz to meet the 1V output voltage specification with maximal conversion efficiency, a five-stage cascaded voltage doubler is chosen at 880MHz to meet the specification with maximal

conversion efficiency due to the fabrication limitations on the large on-chip inductor that is required at the lower frequency (880 MHz) for a four stage cascaded voltage doubler.

The required inductor value at the resonant frequency in Figure 5.1.2 can be described by rearranging Equation 4.2.29:

$$L = \frac{1}{\omega_{res}^2 C_{in}} \sqrt{\frac{1}{L\omega_{res}^2 C_{in}}} \qquad 5.1.3$$

Where C_{in} is the input capacitance of the cascaded voltage doubler.

Equation 5.1.3 indicates that for a fixed C_{in}, at the lower resonant frequency (880MHz), a roughly four-fold higher inductor value will be required compared to the band at 1800MHz. The larger value on-chip inductor can not be implemented in the process used for fabrication.

In order to lower the required inductor value at 880MHz, we increase the input capacitance by choosing five-stage cascaded voltage doubler. The equivalent capacitance of the cascaded voltage doubler at signal frequency can be described by the equivalent capacitance of a single stage voltage doubler by using Equation 4.2.19:

$$C_{in} = 2n \times C_T = n \times C_{voltagedoubler} \qquad 5.1.4$$

Where C_{in} and $C_{voltagedoubler}$ are the input capacitance of a n-stage cascaded voltage doubler and input capacitance of a single stage voltage doubler, respectively.

After choosing the number of cascaded stages, we used circuit simulation tools (RFDE/ADS) to optimize the impedance of the harvester resistance at 1800MHz. Our simulation indicates that 12 Ohm impedance can achieve the highest voltage boost and thus the highest conversion efficiency. The extraction results of lump components for the on-chip inductor show that the impedance mainly comes from the on-chip inductor.

These results also confirm that the voltage boosting is limited by the quality factor of the inductors.

Another design requirement is that the impedance of the each harvester needs to be relatively high at the other harvesters' resonant frequencies, so as to minimize signal losses. Theoretically, the higher the quality factor of the network, the higher the impedance at other frequencies will be. For a network with quality factor of 10, the signal losses from parallel resonant circuits can be negligible using ideal components.

Figure 5.1.3 shows the circuit diagram of the designed dual-band energy harvester. The circuits encircled by the orange rectangle use five cascaded voltage doubler circuits to achieve optimized efficiency at 880MHz; the circuits encircled by the blue rectangle used four cascaded voltage doubler circuits to achieve optimized efficiency at 1800MHz. The gates of the MOSFET connected diodes are for biasing using the generated output voltage along with off-chip resistor and capacitor networks (indicated by red rectangles). The biasing voltage is optimized by the cadence software.

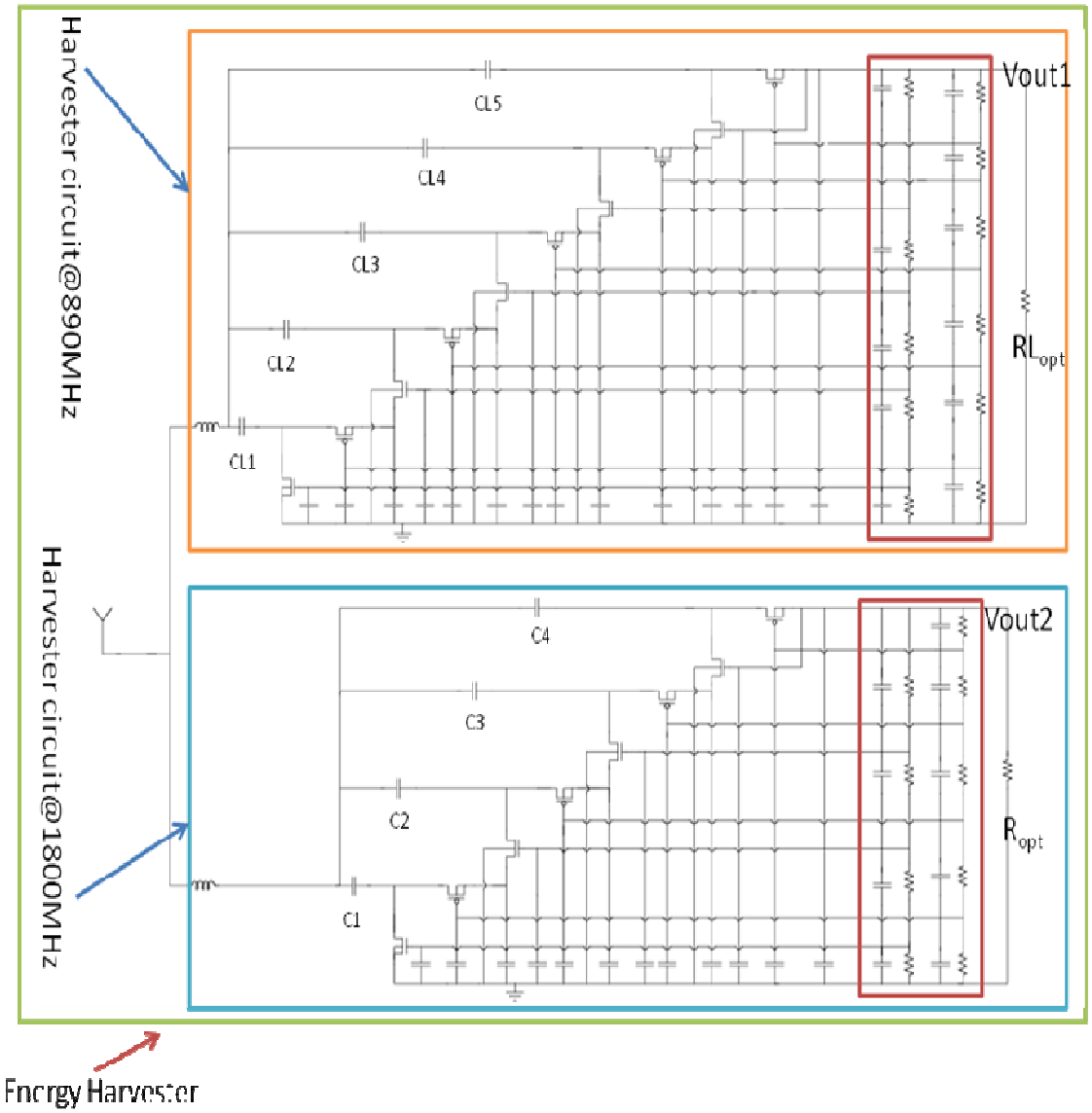


Figure 5.1.3 Designed circuit schematic of dual-band energy harvester.

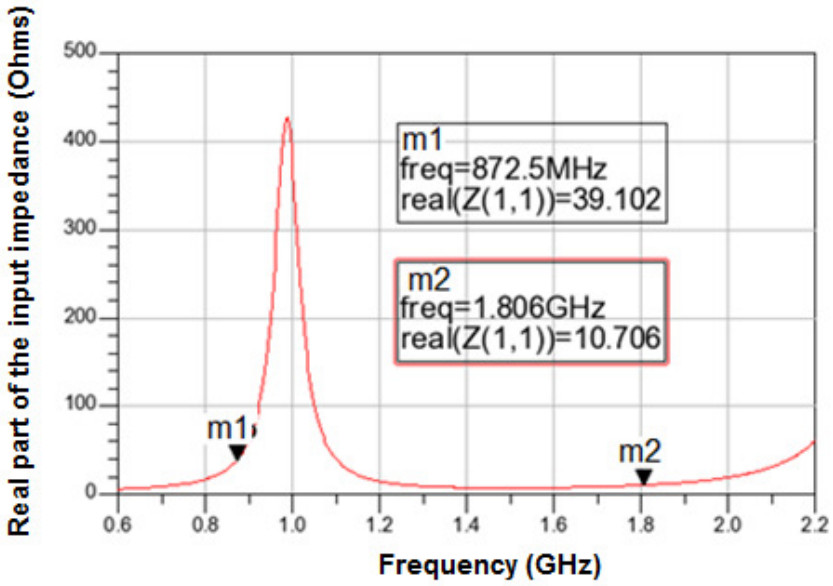
Figure 5.1.4 shows the simulated post-layout impedance of the energy harvester. It shows that the energy harvester has real impedances of 40 and 10.7 Ohm at frequencies of 866MHz and 1809MHz, respectively. The inductor extraction procedure in Appendix B shows the impedance of the inductor itself is 37.66 Ohm at 880MHz. This indicates

that the matching impedance mainly comes from the impedance of the inductor; the quality factor of the harvester is mainly limited by the inductors.

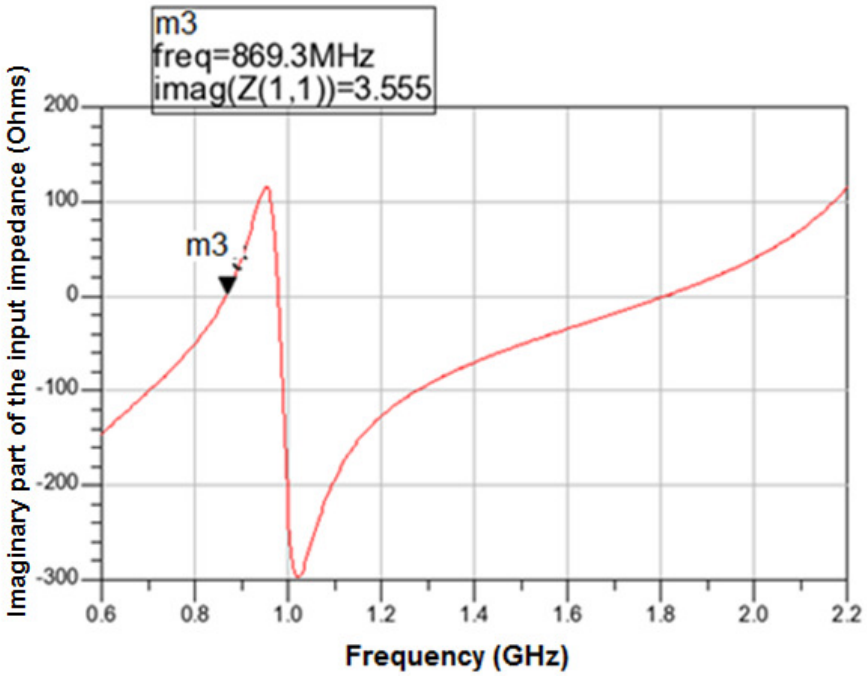
Figure 5.1.5 and Figure 5.1.6 show the post-layout simulated output voltage and efficiency of the dual-band energy harvester, respectively, around the two frequency ranges, 880MHz and 1800MHz, respectively.. It accounts for the lumped elements as well as the parasitics that are introduced when the integrated is actually laid out on a silicon substrate. The simulation results show the harvester output voltage is 1.448V@930MHz and 1.12V@1.875GHz for input power of -19dBm, respectively. The simulated efficiencies are 14%@930MHz and 11.4%@1.875GHz for an input power of -19dBm. This result is comparable to what is found in the literature for single-band harvesting, but is also realized in two bands in this design. The conversion efficiency of the harvester is given by the ratio of the output harvested power to the input power, as shown by Equation 5.1.5:

$$\eta = \frac{\frac{V_{out}^2}{R_{load}}}{P_{in}} \qquad 5.1.5$$

Where V_{out},$R_{load,}$ and P_{in} are the output voltage, load impedance, and input power.

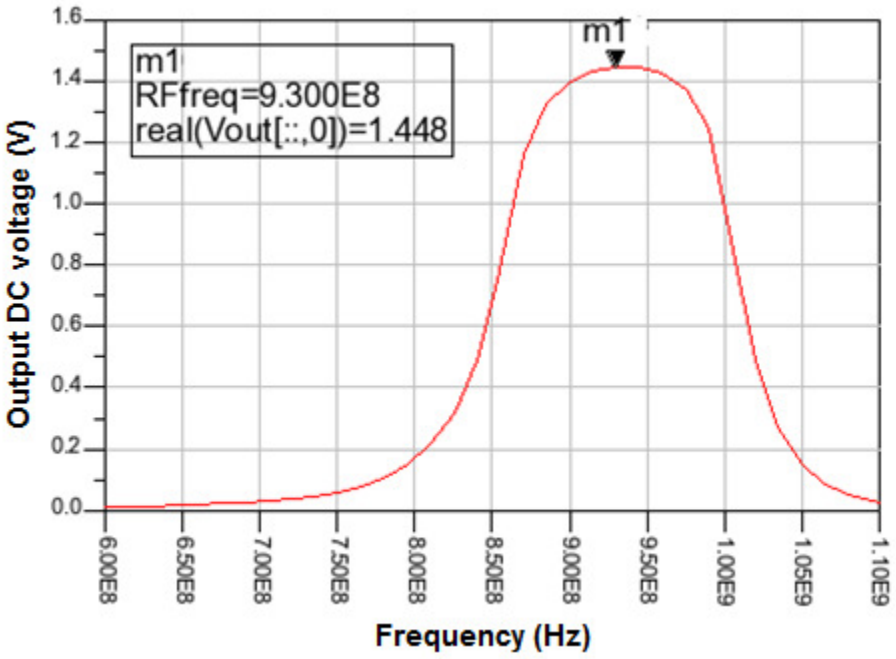


(a)

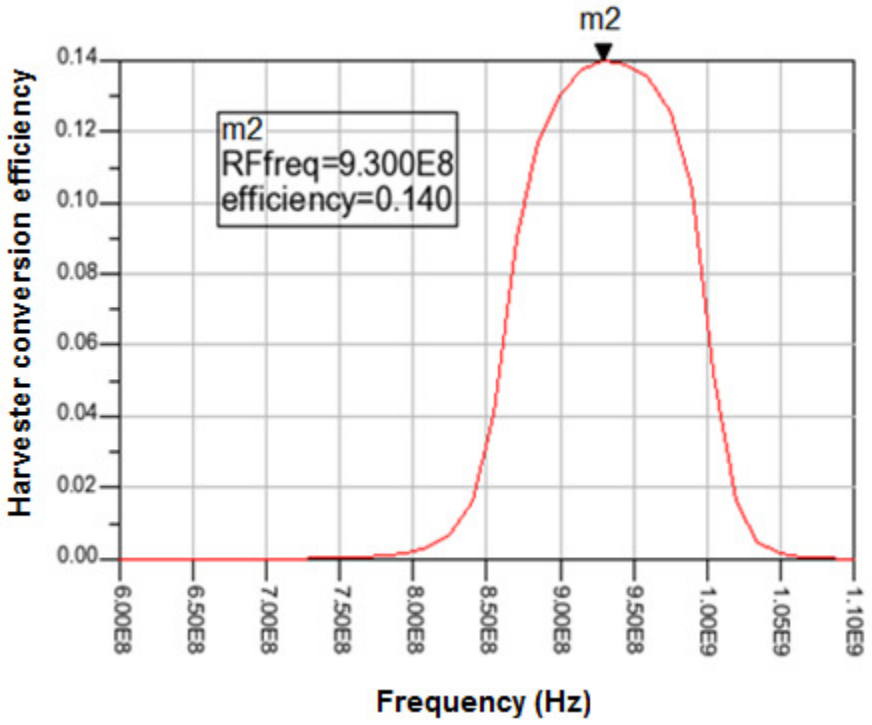


(b)

Figure 5.1.4 (a) Simulated real part of the input impedance of the energy harvester. (b) Simulated imaginary part of the input impedance of the energy harvester. m1,m2 and m3 represent mark 1, mark 2 and mark 3, respectively.



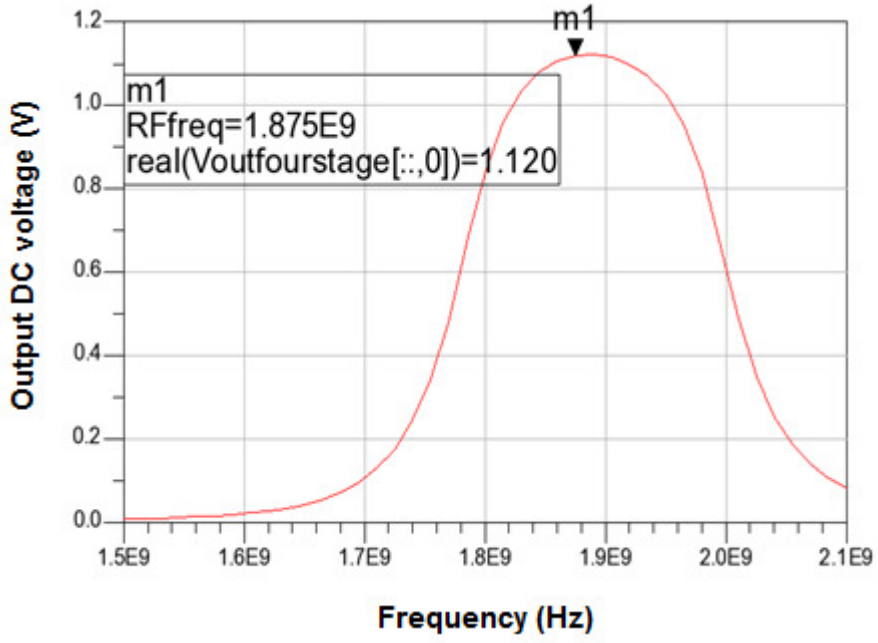
(a)



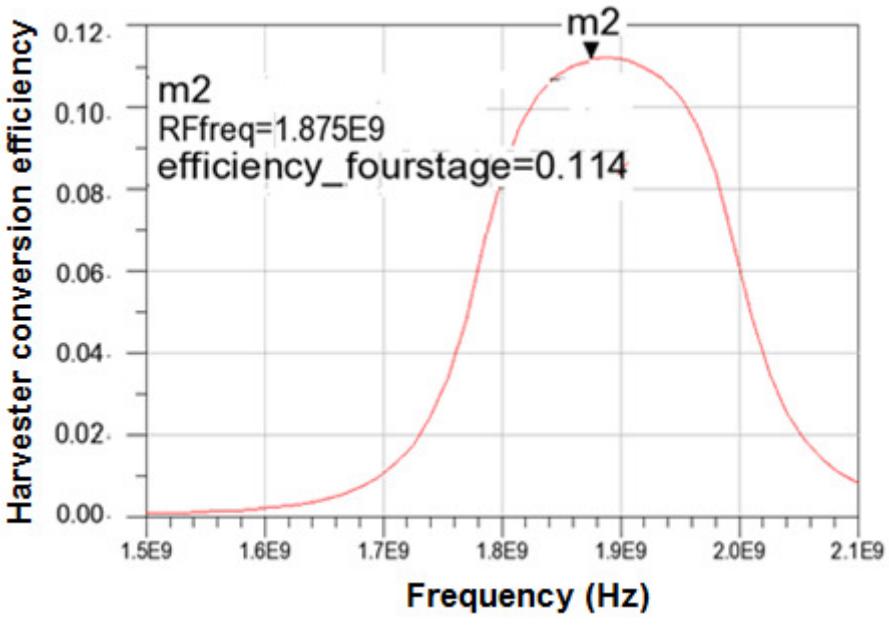
(b)

Figure 5.1.5: (a) The post-layout simulated output voltage for an input power of -19dBm around 880MHz frequency range. (b) The post-layout simulated power

conversion efficiency for an input power of -19dBm around 880MHz frequency range. m1 and m2 represent mark 1 and mark 2, respectively.



(a)



(b)

Figure 5.1.6: (a) The post-layout simulated output voltage for an input power of -19dBm around 1800MHz frequency range. (b) The post-layout simulated power conversion efficiency for an input power of -19dBm around 1800MHz frequency range.

5.1.3 Dual-band Monopole Antenna Design and Fabrication

From the dual-band harvester system requirements, the harvester antenna needs to meet the following requirements:

1. It needs a monopole antenna due to the single end energy harvester design.
2. It needs to have an impedance of 50 Ohm at 880MHz and 12 Ohm at 1800MHz to minimize the reflection between the antenna and the harvester.
3. The antenna also needs to have efficiency over 90 percent to reduce the Ohmic losses of the antenna itself.

[Chen2003] and [Das2006]'s work demonstrate dual-band monopole antenna designs. In our work, in collaboration with Dr. Xi Shao, we developed a modification in which a dual-band antenna is designed to meet the above requirements. Figure 5.1.7 shows the PCB layout of the monopole antenna. The long arm resonates at 880MHz with 50 Ohm radiation impedance while the two folder arms resonate at 1800MHz with 12 Ohm radiation impedance. The length and the folded distance can be modified to resonate at other frequencies with different radiation impedances.

Figures 5.1.8 shows the HFSS S-parameter simulation results of the designed monopole antenna. They show that the antenna S11 is less than -12.5 dB at 880MHz for a 50 Ohm load. They also show the antenna S11 is less than -15dB at 1850 MHz for a 12 Ohm load. The reflection power is fairly low according to the simulated S11, indicating that the antenna is well matched to the designed multi-band harvestor.

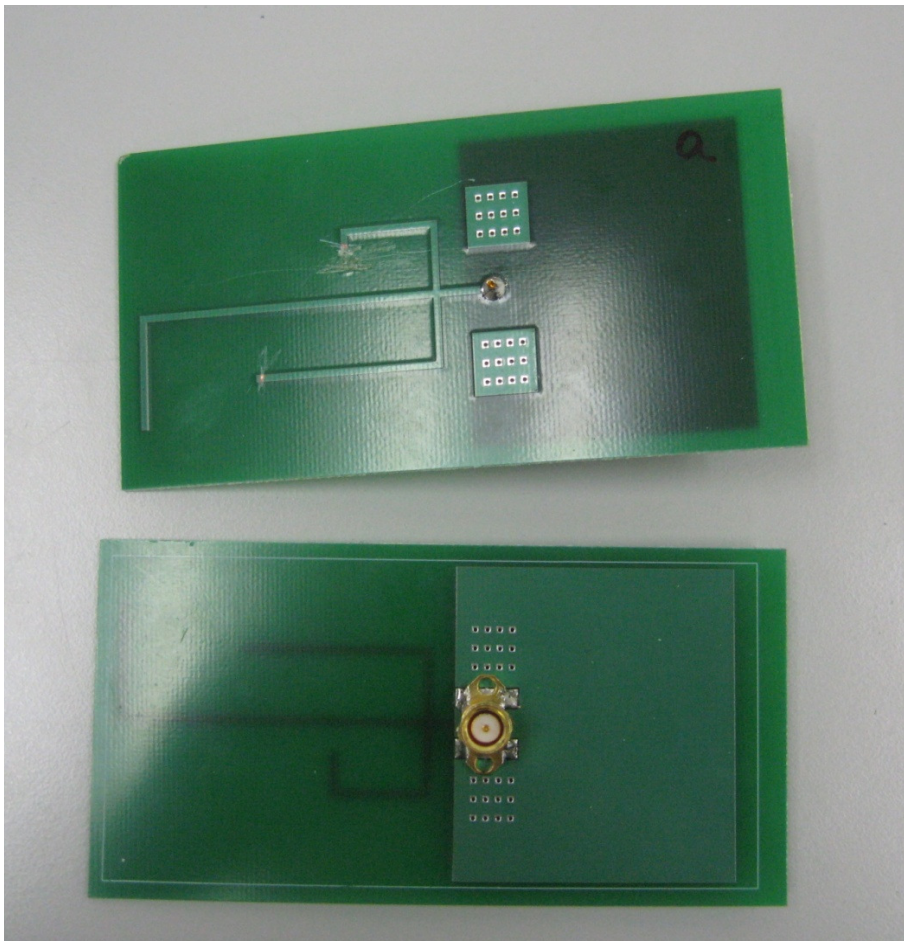
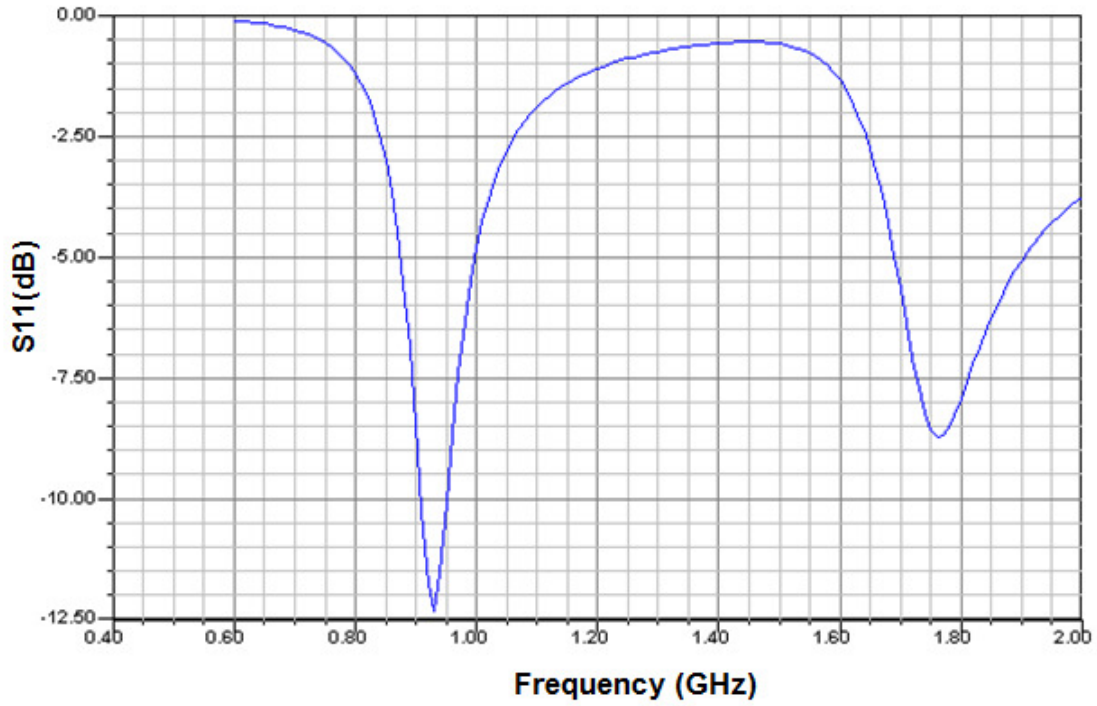
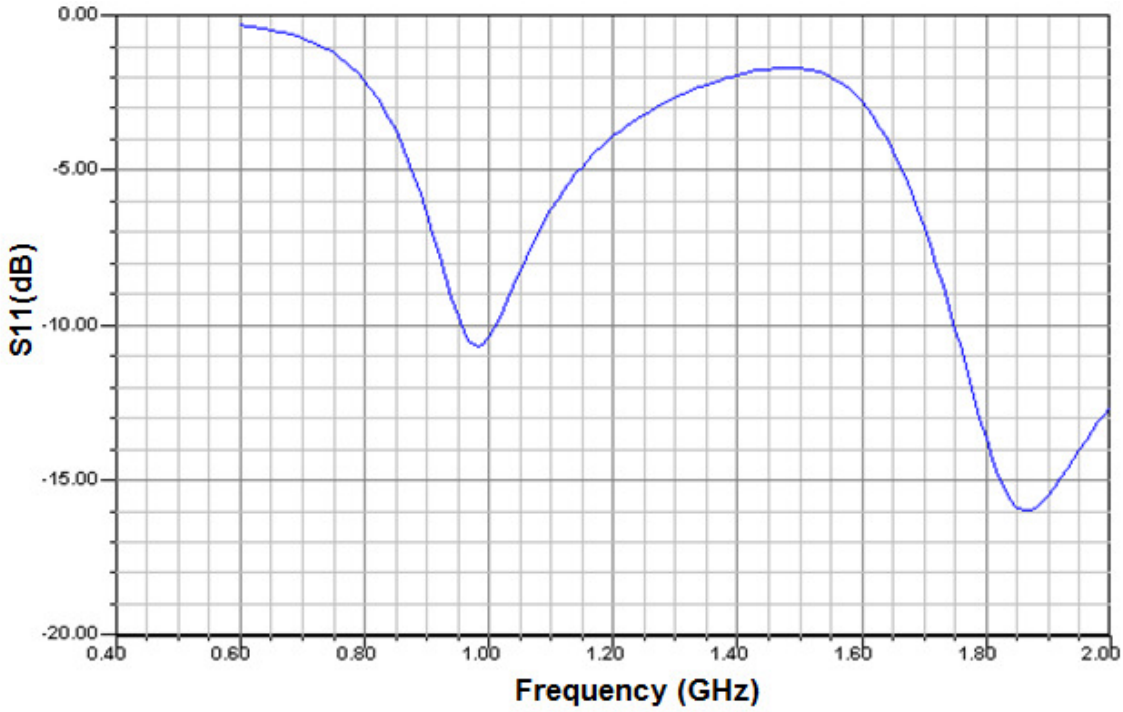


Figure 5.1.7 Photograph of the fabricated monopole dual-band antenna.



(a)



(b)

Figure 5.1.8 (a): Simulated S11 of the dual-band antenna with impedance of 50 Ohm. (b): Simulated S11 of the dual-band antenna with impedance of 12 Ohm.

5.1.4 Measurement and Design Achievements

Figure 5.1.9 shows a photograph of the fabricated dual-band energy harvester chip. The harvester is fabricated using an eight metal layer CMOS process and the chip die is 2x2 mm^2. The chip is packaged using quad flat no leads (QFN) technology. The packaged chip die has 28 pin and the size is 5x5 mm^2.

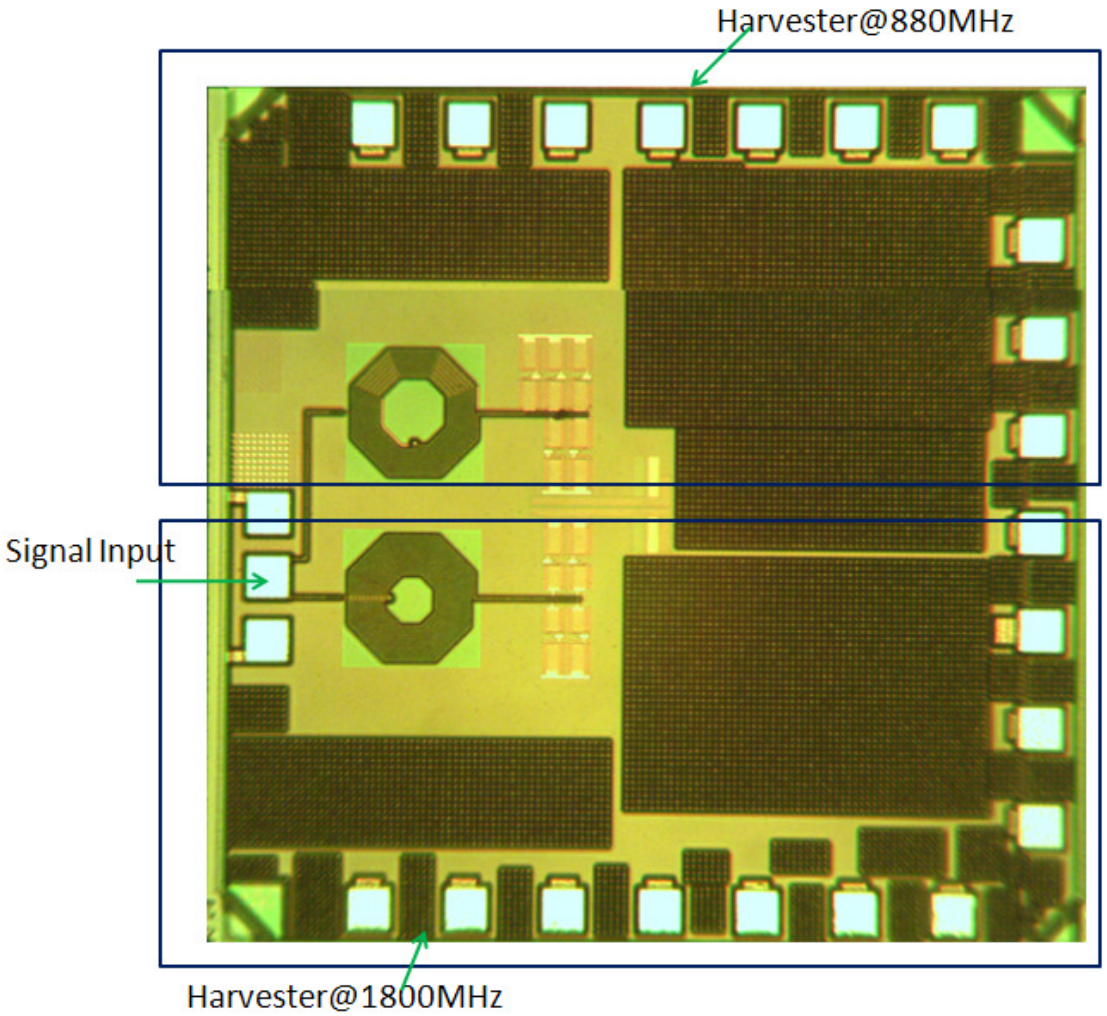


Figure 5.1.9 Photograph of the fabricated energy harvester chip.

A PCB board is fabricated to facilitate the direct connection between the antenna and the measurement of the integrated circuits, as well as to provide biasing voltages. In order to accurately measure the harvester impedance, the PCB board has to be calibrated to

remove the transmission impedance in a manner that is analogous to the calibration of the network analyzer. First, a 50 Ohm transmission line is connected to the RF input of the integrated harvester and to an edge mounted SMA connector. After soldering down the capacitors and the harvester onto the PCB, two zero Ohm resistors are first connected to the ground of the PCB board at the location where the transmission line is connected to the solder chip. A network analyzer is used to measure the phase delay of the transmission line. The process is as follows:

- Two zero Ohm resistors are soldered at the end of the transmission line.
- A network analyzer is used to decouple the phase delay effect of the transmission line.
- The transmission line loss is also obtained using measured S11.

The two zero Ohm resistors are then removed from the PCB board while the network analyzer maintains the phase delay and path losses to de-embed the transmission line effect. After the calibration, the impedance of the harvester can be accurately measured.

The packaged energy harvester circuit is mounted on the surface of the designed PCB board with the necessary biasing networks. Figure 5.1.10 is the photograph of the fabricated dual-band energy harvester, which included the chip, and self-biasing network. Figure 5.1.11 shows that the measured output voltage of the dual-band energy harvester varies with frequency (the input signal is -19.3 at 900MHz and -19.2 at 1900 MHZ). Figure 5.1.12 shows that the measured conversion efficiency of the dual-band energy harvester varying with frequency (the input signal is -19.3 at 900MHz and -19.2 at 1900 MHZ). Figure 5.1.13 shows that the measured output voltage of the dual-band

energy harvester varies with the input power at 900MHz (the input signal is -19.3 at 900MHz).

The measured results show that the harvestor is working essentially as designed. It readily harvests energy at both frequencies with efficiency and output voltages meeting the design specifications of harvesting at -19dBm and generating over 1V DC.

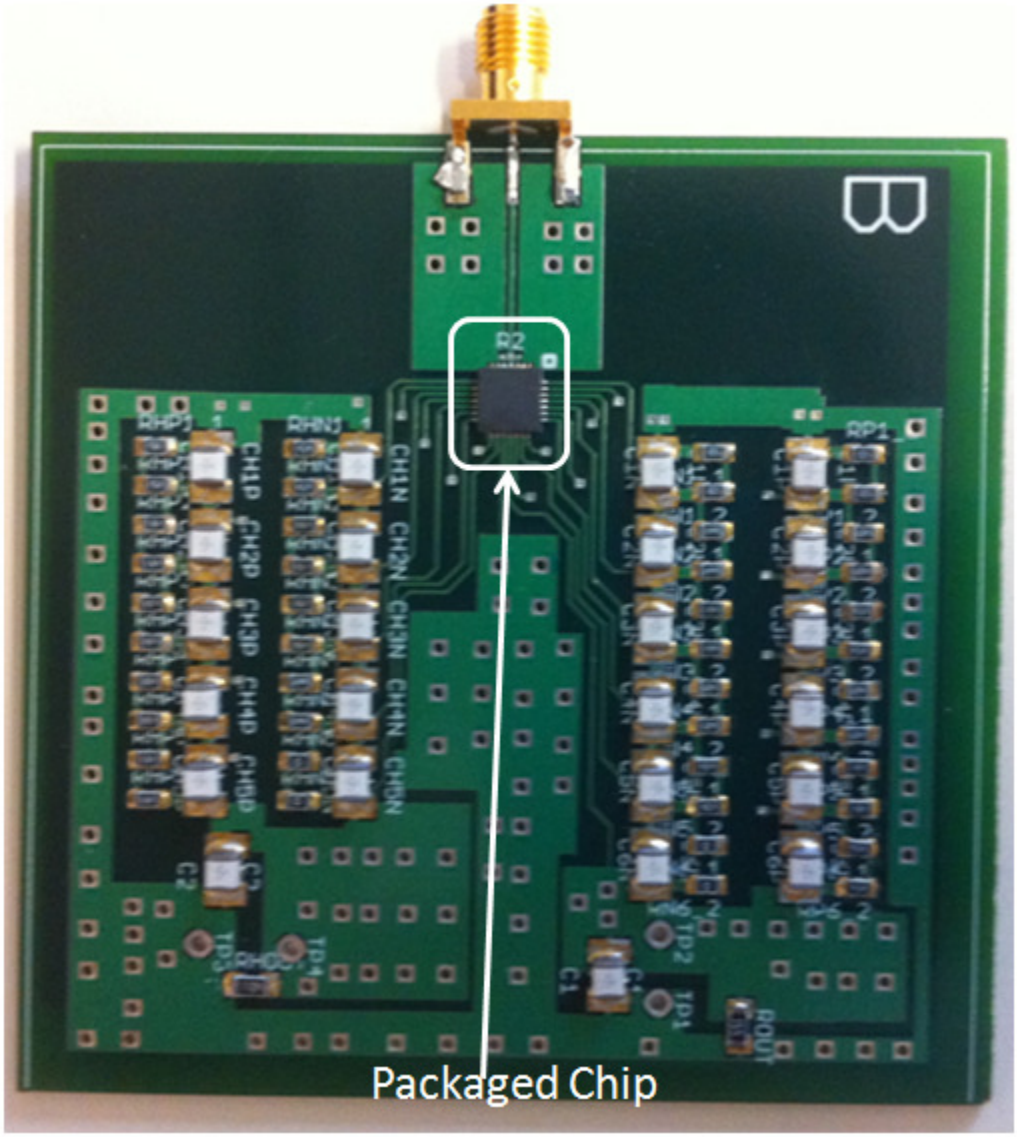


Figure 5.1.10 Photograph of the fabricated energy harvester.

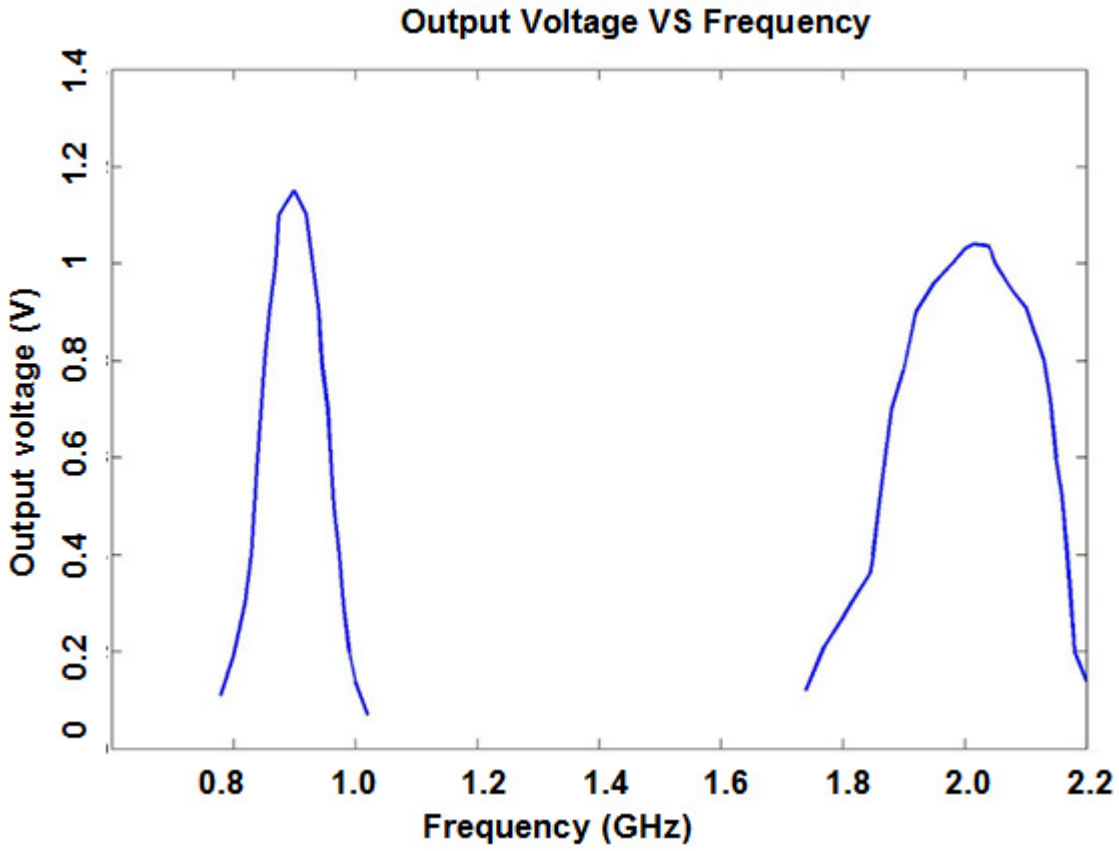


Figure 5.1.11 The measured output voltage of the dual-band energy harvester varies with frequency (the input signal is -19.3 at 900MHz and -19.2 dBm at 1900MHZ).

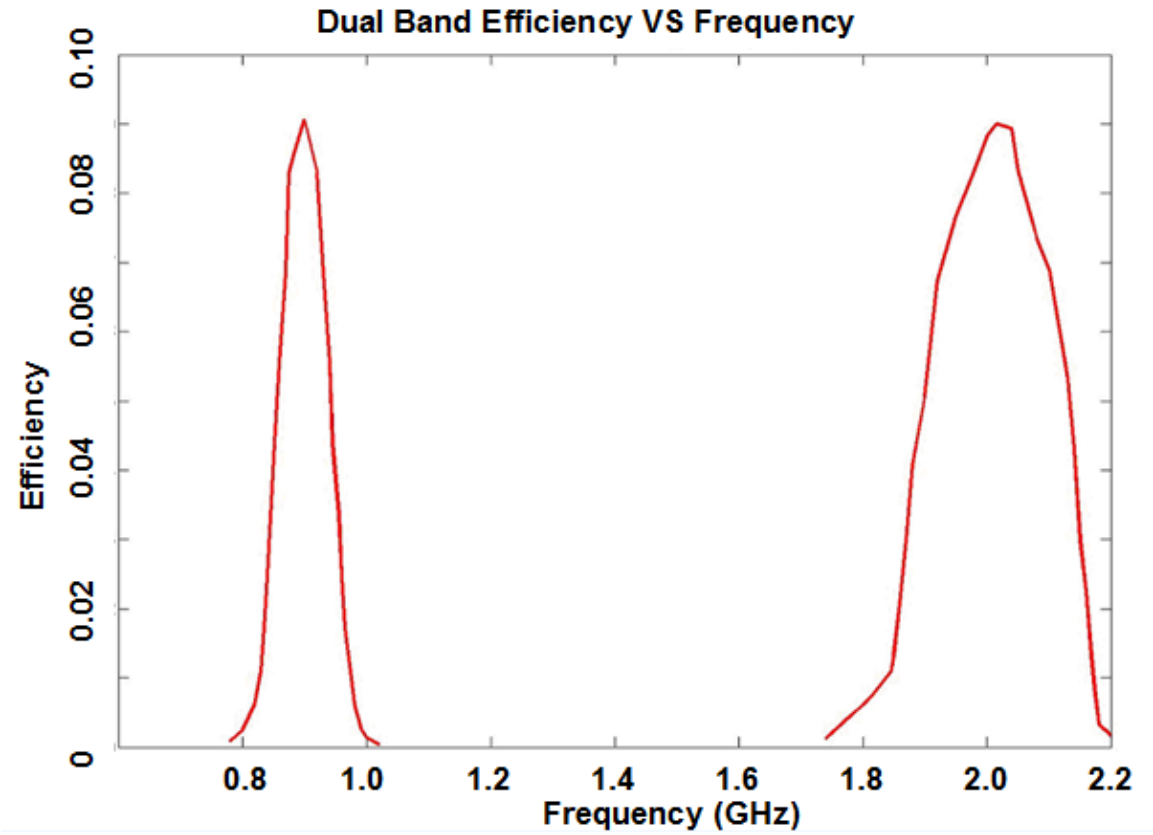


Figure 5.1.12 The measured conversion efficiency of the dual-band energy harvester varies with frequency (the input signal is -19.3 at 900MHz and -19.2 dBm at 1900MHZ).

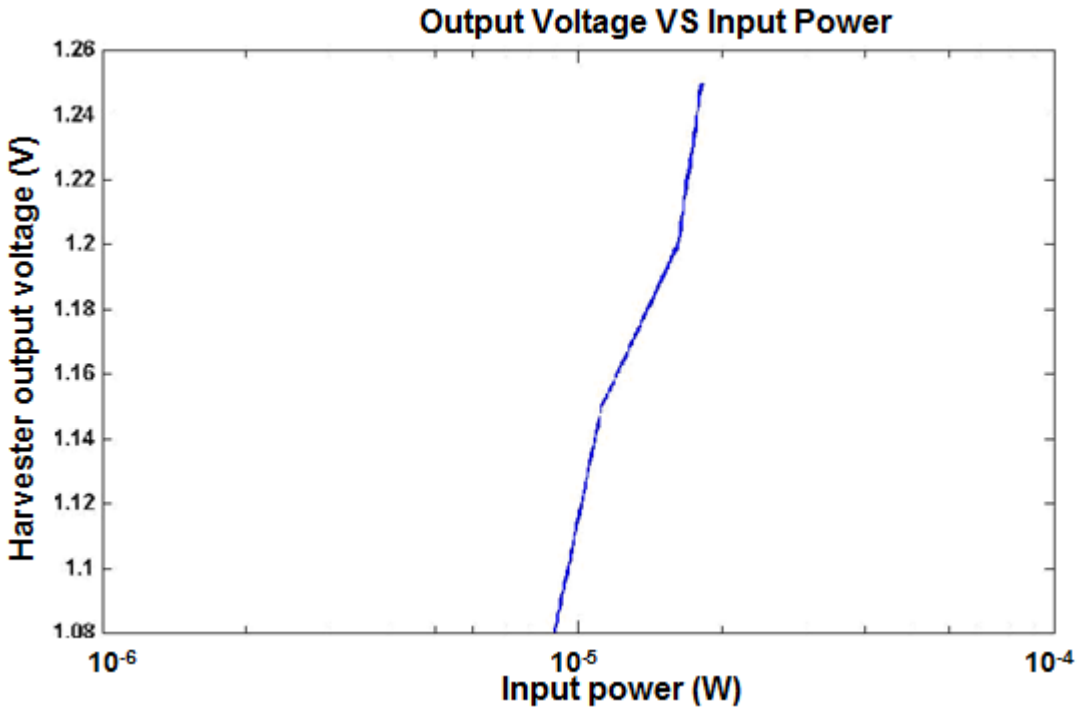


Figure 5.1.13 The measured output voltage of the dual-band energy harvester varies with the input power at 900MHz (the input signal is at 900MHz).

5.2 Dual-Band Antenna Coupled RF Energy Harvester

In this section, we show the design and simulation results of an antenna *coupled* energy harvester in two frequency bands centered at 1800 and 2400 MHz, and using a rather different topology and scheme from that presented above. The general design concept below is not limited to these two particular frequency bands and may be adapted to other dual-band antenna-coupled RF applications. The work here represents a co-design of the antenna and harvestor performed self-consistently

5.2.1 Design of Antenna-Coupled Dual-Band Energy Harvester and Simulation Results

Figure 5.2.1 shows the structure of the antenna coupled dual-band harvester. Here, the energy harvester couples closely with the antenna: the harvester circuit is capacitor-like at 1800MHz while being resistor-like at 2400MHz, and the antenna provides the necessary matching inductance at a frequency of 1800 MHz. The output voltage specification of this design is 0.8V.

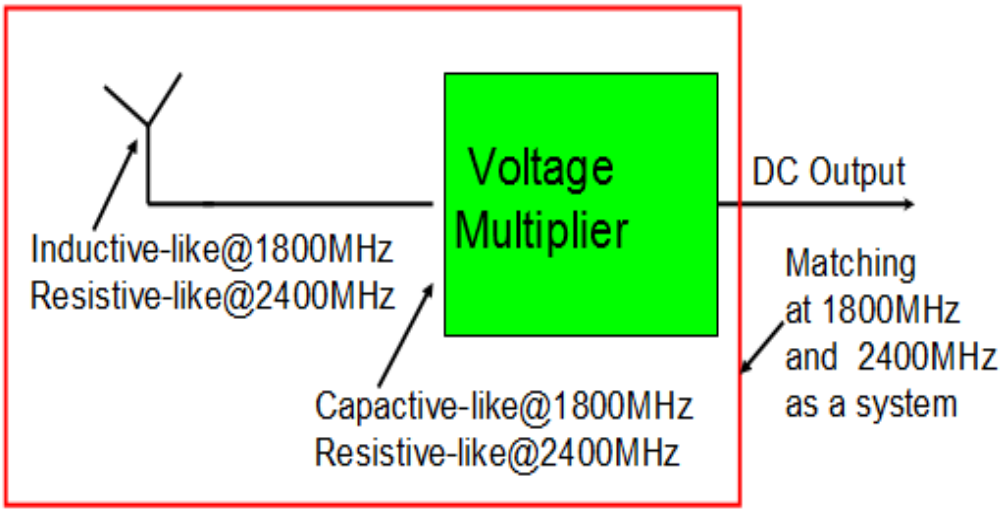


Figure 5.2.1 Structure of the antenna coupled dual-band energy harvester.

The design goals are the same as for the previous multiband harvester: to boost the voltage and to obtain power matching at two different frequencies. In this design, however, power matching and voltage boosting at 2400MHz is obtained using an on-chip voltage transformer only. At the second frequency (1800MHz), the antenna functions as a high quality off-chip inductor which provides the necessary matching and voltage boosting. The designed harvester impedance is 15-125*j* Ohm at 1800MHz and resistance of 25 Ohm at 2400MHz, respectively.

Figure 5.2.2 depicts the circuit diagram of a three-stage energy harvester. The voltage doubler circuit design is similar to the previous narrowband harvester design.

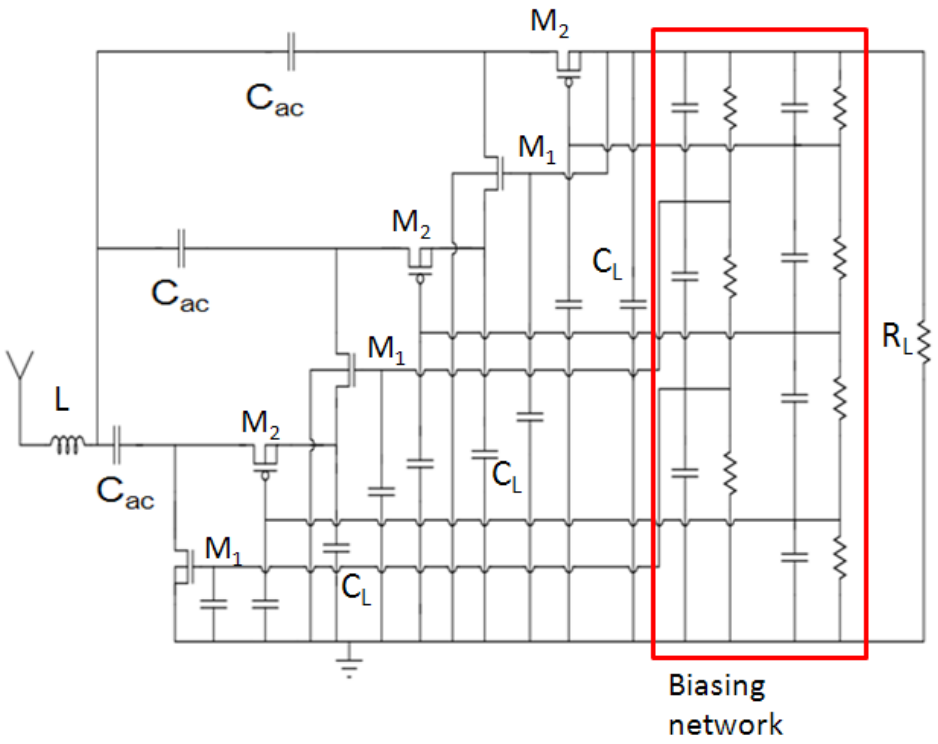
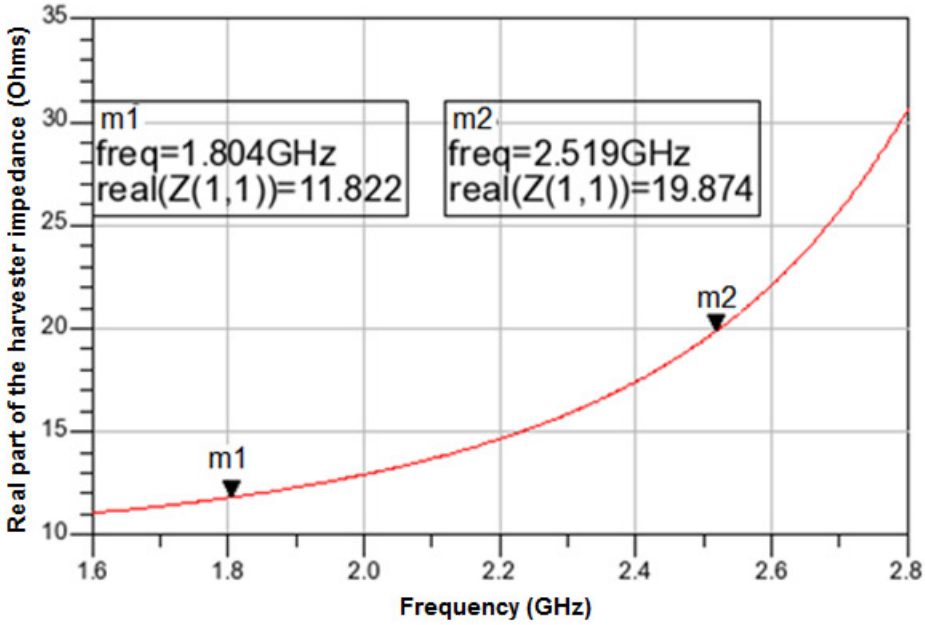


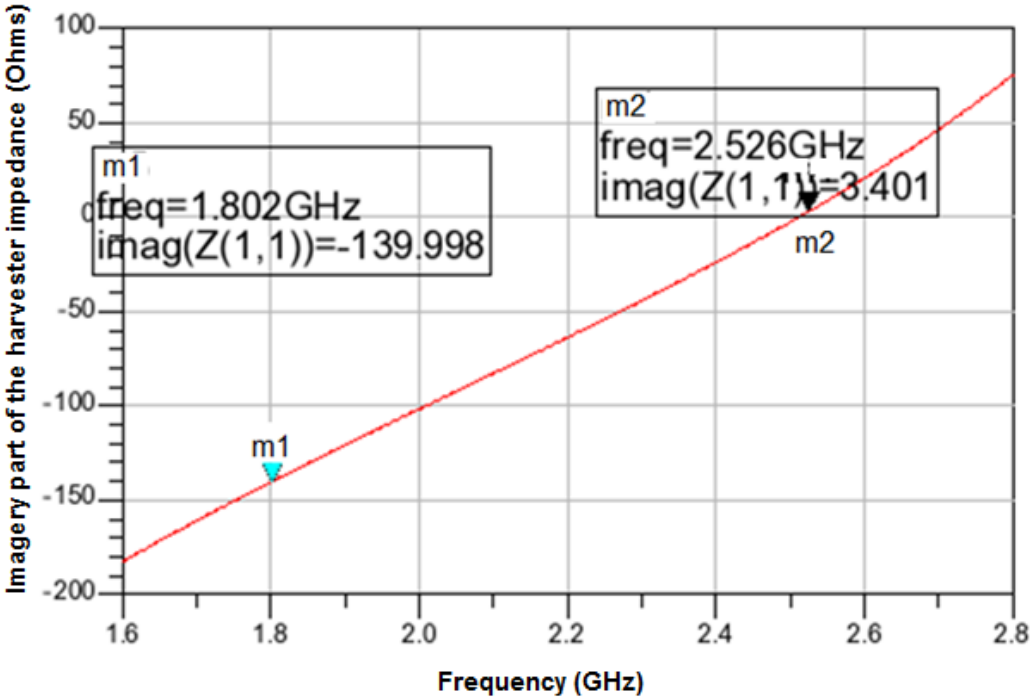
Figure 5.2.2 Circuit schematics of the antenna coupled dual-band energy harvester circuit.

Figure 5.2.3 shows that the simulated harvester impedance is 15-125*j* Ohm at 1800MHz and 25Ohms at 2400MHz. Figure 5.2.4 displays the simulation results for the energy harvester, which generates 0.974V with 14.4% efficiency at 1800MHz while generating 0.85V with 12% efficiency at 2400MHz. The conversion efficiency at 1800MHz is better than the conversion efficiency at 2400 MHz because of the high quality PCB inductor that a PCB antenna provides. Also, at higher frequencies, there are higher parasitic signal power losses. Figure 5.2.5 is a photograph of the fabricated chip

die. The chip is packaged using quad flat no leads (QFN) technology to achieve the lowest parasitic losses. It has 16 pins and the size is 4x4 mm^2.

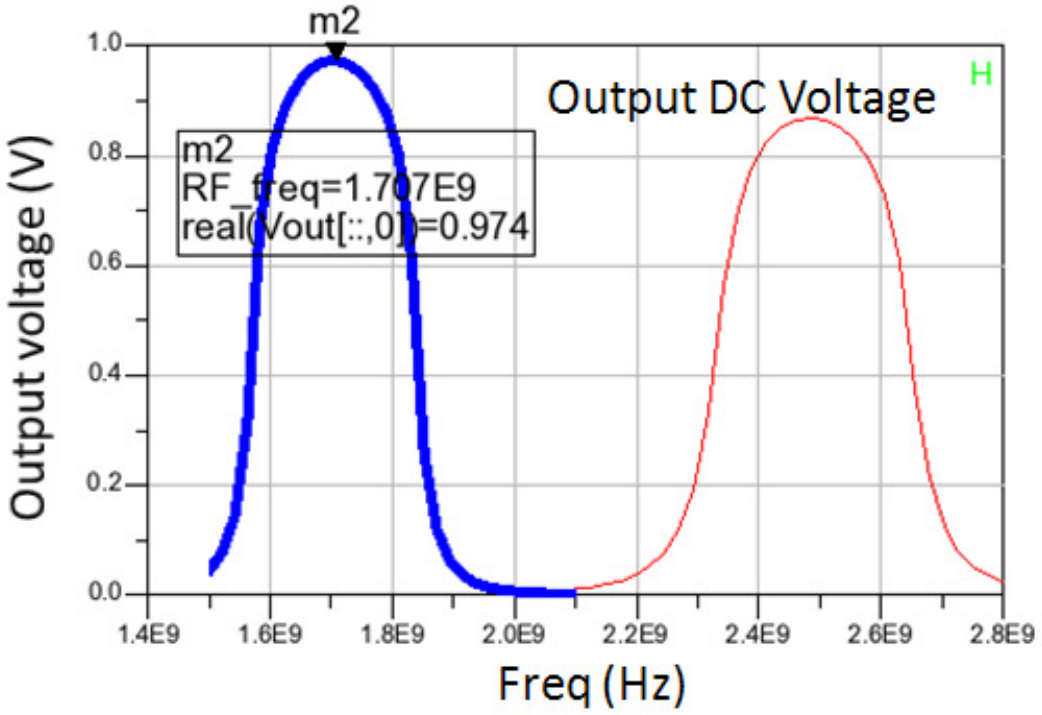


(a)

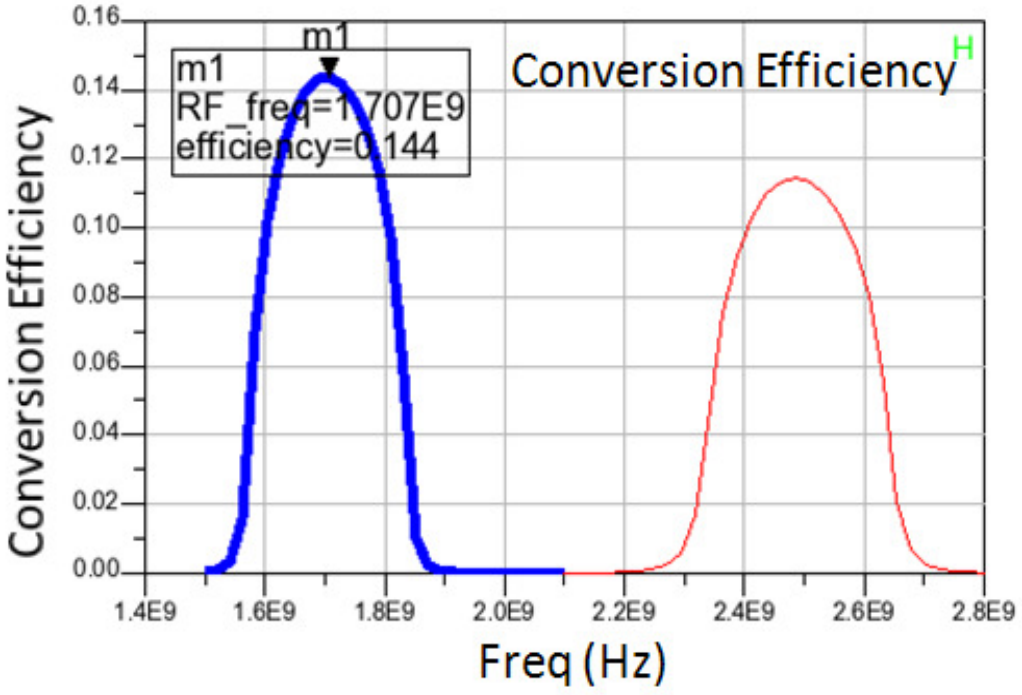


(b)

Figure 5.2.3 (a) Simulated real part of the impedance of energy harvester; (b) Simulated imaginary part of the impedance of the energy harvester.



(a)



(b)

Figure 5.2.4 (a) Simulated DC voltage of harvester for -19dBm input signal; (b): Simulated conversion efficiency of the energy harvester.

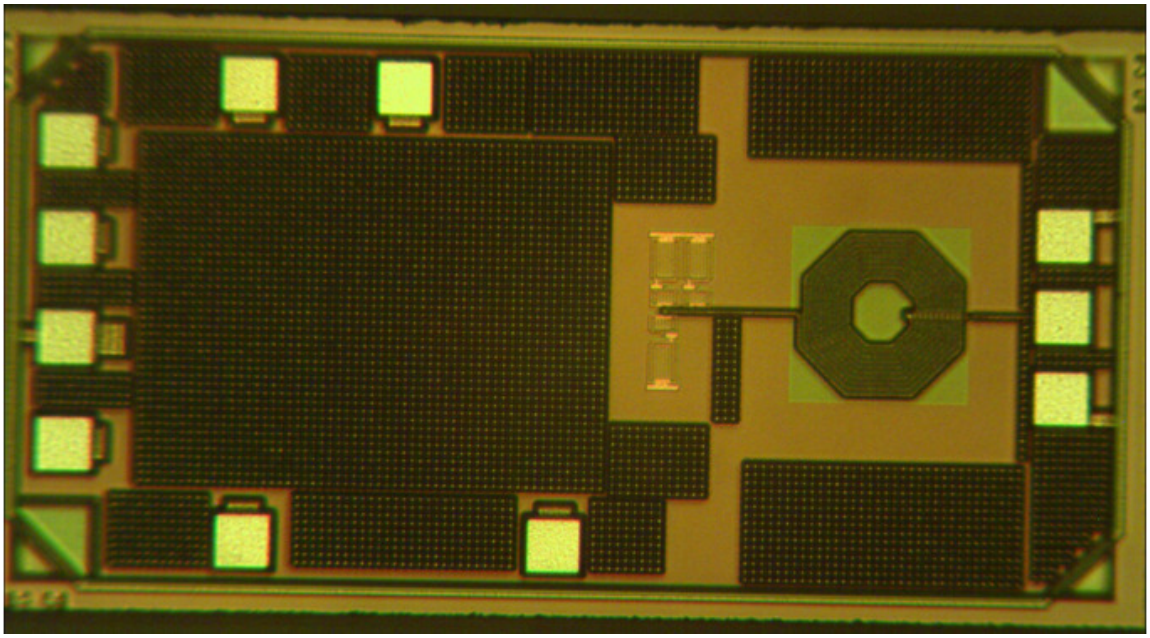
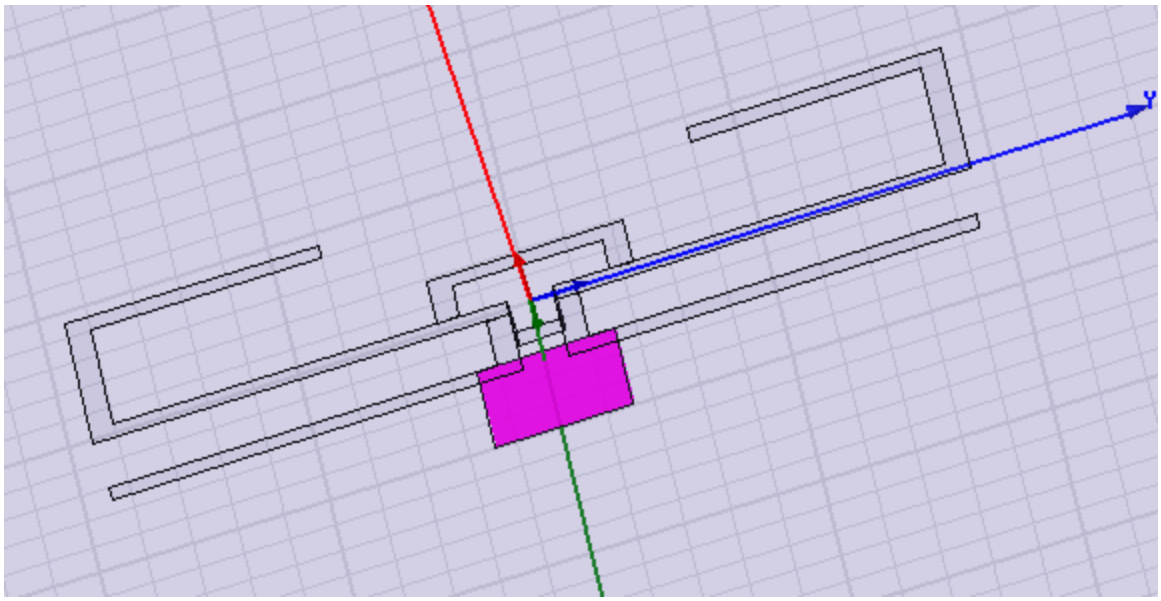


Figure 5.2.5: Photograph of the fabricated energy harvester chip.

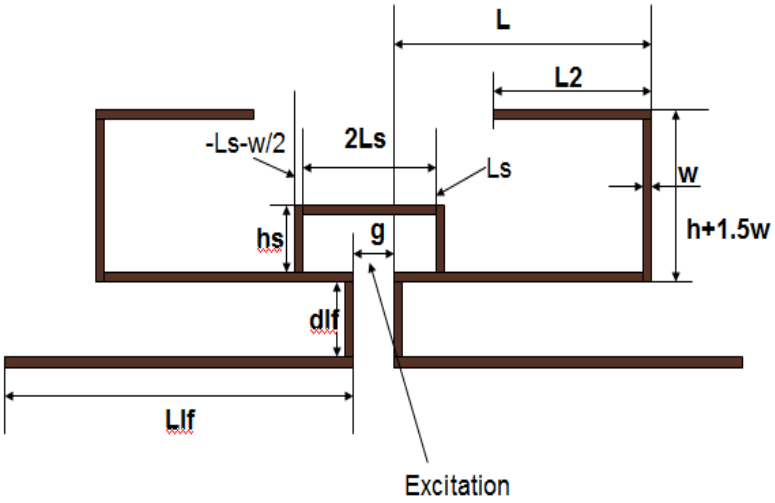
5.2.2 Antenna Design and Simulation Results

The antenna design was performed in collaboration with Dr. Xi Shao. For the presented antenna coupled dual-band energy harvester design, the dual-loop part of the antenna provides inductance to be complex conjugate matched to the reactive impedance of the chip at one frequency. Figure 5.2.6 (a) shows the layout of the off-chip antenna. It consists of two parts: the double-loop part provides high quality factor inductance/impedance matching while the dipole arm part provides the resistive impedance matching. The red rectangle in the antenna diagram takes into account the small metal plane from the package QFN 4x4 chip die. The package chip die is mounted on surface of the PCB board.

Figure 5.2.6 (b) and (c) shows antenna geometry sizes. The antenna with the given geometry has been simulated using high frequency structure simulator (HFSS) software. Figure 5.2.6 (d) shows the simulated radiation impedance of the antenna. The radiation impedance at 1800Mhz is 15+125*j*, which is the result of the loop part of the antenna; the simulated impedance at 2400MHz is 25Ohms, which comes from the dipole structure part of the antenna. Thus, the simulated antenna design achieves the specifications. The antenna design can be adapted to other frequency bands and to match different inductive impedances. For example, by varying the dipole and loop arm length, the operating frequency of the antenna can be tuned. Also, the inductance of the loop part of the antenna can be tuned by varying the area of the two loops.



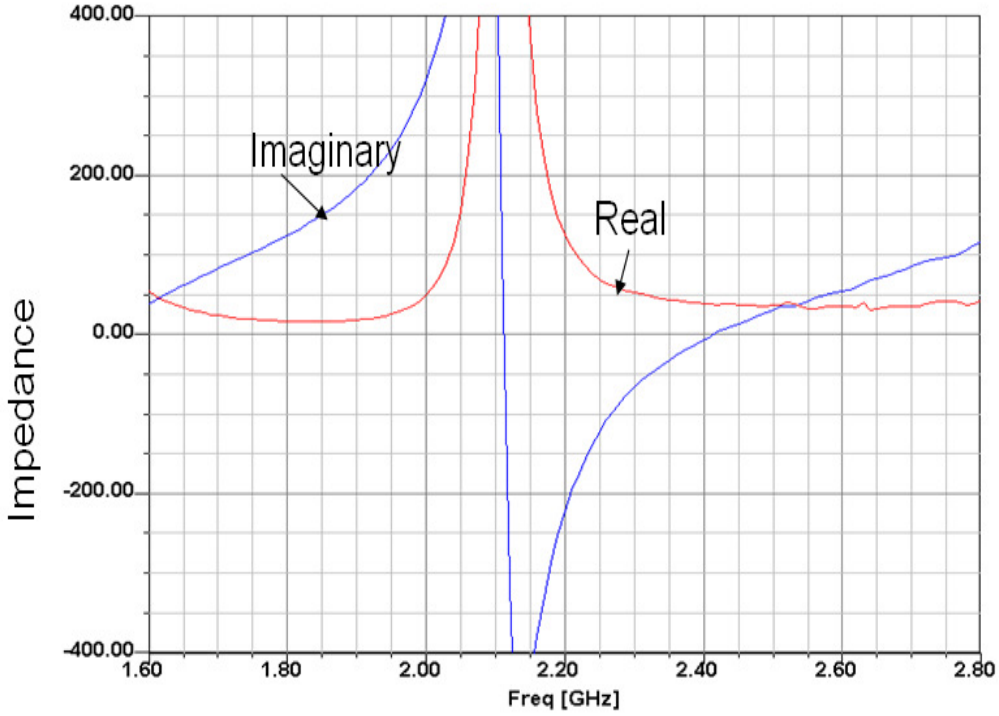
(a)



(b)

Geometry Parameters	Value	Unit
w	1	mm
g	2	mm
L	18	mm
L2	11	mm
Ls	3.5	mm
hs	3.3	mm
Llf	17.8	mm
dlf	4	mm

(c)



(d)

Figure 5.2.6: (a) 3D layout of dual-band loop-dipole antenna providing inductive impedance matching via the antenna loop and resistive impedance matching via the dipole arm. The pink patch on the back of the PCB indicates where the chip is located. Feeding between the antenna and harvester is accomplished through the back of the PCB. (b) Geometric layout of metal strips on top of the PCB. This contains the upper part of the loop and the lower part of the dipole arms operating at two different frequencies. (c) Geometric parameters for the sample design operating at 1800 MHz and 2400 MHz frequency bands. (d) Real and imaginary parts of the designed antenna impedance between 1800 MHz and 2400 MHz frequency bands.

5.3 Summary:

We have investigated the use of ambient RF power as a source for WSN applications in which devices need to be left unattended for extended periods without battery replacement. Dual-/multi-band energy harvesting schemes can take full advantage of the available RF energy within several frequency bands. This overcomes limitations between

the bandwidth and voltage boosting of a matching network when applied over a wide frequency region.

In this chapter, a dual-band energy harvester scheme has been provided with harvesting frequencies at 890 MHz and 1800MHz. The design uses two parallel-connected narrowband energy harvesters and a special dual-band antenna which functions as a load of 40 Ohm @890MHz and 14 Ohm @1800MHz. The energy harvester connects with the antenna directly without a transmission line to better match impedance and improve system efficiency. The matching impedance is optimized to be 40 Ohms @890MHz and 14 Ohms @1800MHz to obtain maximum power transfer between antenna and the energy harvester, as well as to provide maximum voltage boosting at the two different center frequencies. Simulation results show that the energy harvester generates 1.448V @880MHz and 1.12V @1800MHz, respectively, for input signal power as low as -19dBm at both center frequencies. The conversion efficiencies are 14% @890MHz and 13.4% @1800MHz, respectively with a -19 dBm input signal power. Measured results show that the energy harvester generates 1.17V @880MHz and 1.12V @2000MHz, respectively, for input signal power as low as -19.3dBm at both center frequencies. The actual measured conversion efficiencies of the fabricated devices are 9% @890MHz and 9% @2000MHz, respectively with a -19.3 dBm input signal power.

In the last portion of this chapter, a different dual-band topology has been presented in which the antenna has a pure real resistance at one frequency while it functions as a high quality inductor at another frequency band to provide the power matching and the voltage boosting at two different frequencies (1800MHz and 2400MHz bands). The simulated efficiency of the harvester is 14.4% @1800MHz and 12% @2400MHz.

Our contributions to research on multi-band energy harvesting are summarized as follows:

- Study of battery recharging requirements
- Provided design specification for energy harvesting in WSN applications
- Discussion of theoretical difficulty of wideband energy harvesting
- Creation of a multi-band energy harvesting scheme that uses energy harvesters connected in parallel for dual-/multi-band energy harvesting.
- Use of on-chip inductors to boost voltage for the 890MHz and 1800MHz bands.
- Use of an improved voltage doubler structure to maximize the conversion efficiency.
- Use of the matching impedance of the antenna and the harvester circuits as a system parameter to optimize the conversion efficiency.
- This harvester achieves 14% conversion efficiency at 890MHz and 13.4% conversion efficiency at 1800MHz. The output voltage is over 1V at both frequencies.
- The design harvester can function as two separate power sources when there is RF energy at both frequencies.
- A planar dual-band monopole has been designed, fabricated, and measured. It has an impedance of 50 Ohms at 890 MHz and 14 Ohms at 1800 MHz, respectively. The antenna structure (e.g., the arm lengths and spacing) can be tuned to adapt to other frequency bands and different impedances.

- Dual-band energy harvester for 1800MHz and 2400MHz frequency bands.
- Antenna coupled voltage boosting technique.
- On-chip inductor voltage boosting technique.
- Loop antenna achieves inductive-like behavior at 1800MHz and impedance-like behavior at 2400MHz to match energy harvester.
- The simulated efficiency of this harvester is 14.4% at 1800MHz and 12% at 2400MHz.

Chapter 6: Future Work

Summary of the contribution of this work is given on section 1.4 on Chapter 1. Here I talk about possible future work. Below, two possible extensions to the work presented in this thesis are elucidated, although neither has been formally designed or fabricated.

6.1 Super-regenerative receiver

In the introduction to this dissertation, it has been concluded that mobile devices can work inexhaustibly if awake time is only 0.1% (86.4 second per day) and the data rate is 1Mbps. For some WSN applications such as environmental or health monitoring, data rates of hundreds or thousands of bits per second are sufficient. The percentage of awake time can be increased if the data rate is limited well below 1Mbps. Super-regenerative receivers are good candidates to meet these requirements by adjusting the signal width of the quench signal. We briefly discuss the operation principles as follows.

Super regenerative receivers achieve extremely high gain using positive feedback. The operating principles for a super regenerative receiver are shown in Figure 6.1.1. The transfer function can be described by Equation 6.1.1 [Moncunill-Geniz2005]:

$$G(s) = \frac{sL}{s^2 LC + (G_0 - G_a)sL + 1} \qquad 6.1.1$$

The time domain solution is given by Equation 6.1.2:

$$V_o = Ae^{\frac{-(G_o - G_a)L + \sqrt{(G_o - G_a)^2 L^2 - 4LC}}{2LC}t} + Be^{\frac{-(G_o - G_a)L - \sqrt{(G_o - G_a)^2 L^2 - 4LC}}{2LC}t} + \frac{I_{in} L\omega_o}{\omega_o^2 LC + \omega_o L(G_0 - G_a) + 1} e^{i\omega_o t} \qquad 6.1.2$$

It can be clearly seen from Equation 6.1.2 that in the case of $G_o - G_a < 0$, the RLC network will oscillate at any frequency. In the case where $G_o - G_a = 0$, the RLC network will amplifier the signal at the LC tank natural frequency.

The oscillator power consumption is determined by the inductor quality factor. Off-chip inductors (Bulk Acoustic Wave (BAW) devices) have high quality factors that offer low power consumption [Moncunill-Geniz2005]. However, off-chip inductors are costly. They also add significant package costs. On-chip inductors offer high integration and low cost but consuming considerable power [Chen2007].

The selectivity of the super-regenerative receiver architecture is problematoc since the LC tank oscillates at the interference frequency in the super-regeneration stage. There are different ways to improve the receiver selectivity [Moncunill-Geniz2005][Chen2007].

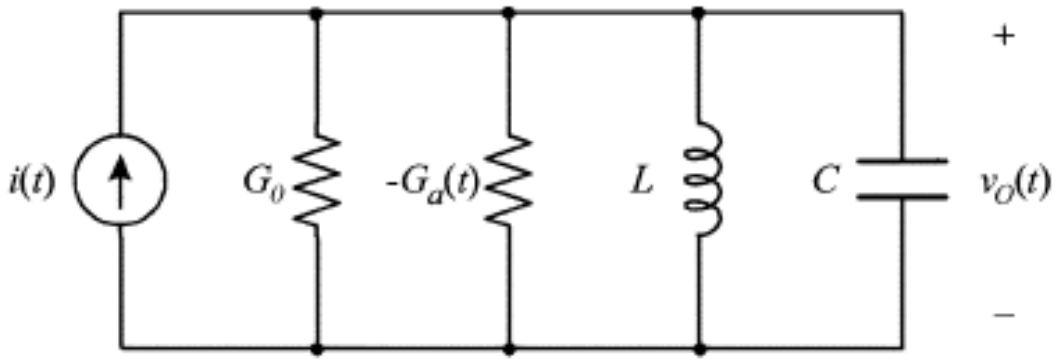


Figure 6.1.1 Operating principle of super-regenerative receiver [Moncunill-Geniz2005].

The negative resistance of the LC tank ($-G_a(t)$) determines the dynamics of the LC tank. Ideally, the LC tank works at exactly the LC natural frequency. It is critical to precisely control this negative resistance since it varies by process and temperature and is extremely sensitive and critical in determining the receiver performance. An external

signal is used to tune the LC tank [Moncunill-Geniz2005]. A high quality off-chip inductor is used to lower the power consumption and improve the selectivity of the LC tank. The selectivity can also be improved by the quench signals. Using external tuning and an off-chip inductor, [Moncunill-Geniz2005] reports a result of a -3dB bandwidth of 3MHz @ 2.4GHz for a sawtooth signal, an effective quality factor of 789. The data rate is determined by the quench frequency. In real experience, quench frequencies are normally ten times larger than data frequencies [Moncunill-Geniz2005]. Amplitude modulation is commonly used in super-regenerative receiver architectures, and Figure 6.1.2 shows the detection process. When there is an input signal, the RLC tank amplifies the signal and then begins to oscillate at other frequencies too. Thus, it is necessary to quench the oscillator once in a while to suppress the oscillations.

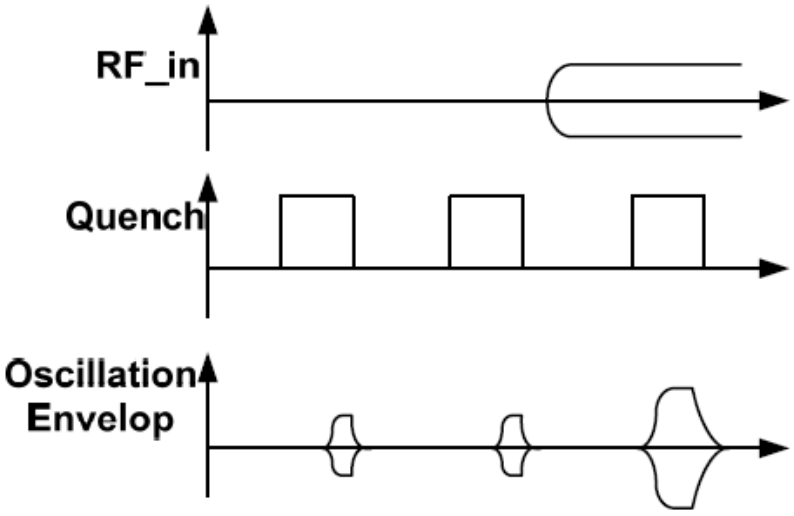


Figure 6.1.2 Response of the super-regenerative receiver.

6.2 Tunable energy harvester

Another approach is to design a tunable energy harvester that has the ability to harvest energy at the strongest energy frequency. Figure 6.2.1 shows the block diagram of a tunable energy harvester. The switches will turn on/off the inductors to match (resonate) different frequencies. The tunable network can be constructed using on-chip inductors, off-chip inductors, on-chip capacitors, and off-chip capacitors. A self-detection technique is needed to harvest energy at the strongest energy frequency. Off-chip inductors can also be used to tune the network to resonate at the strongest power frequency.

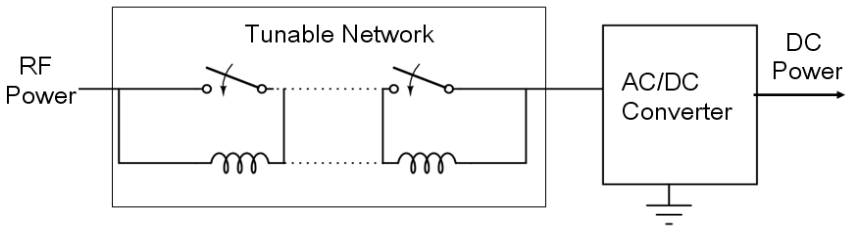


Figure 6.2.1 Block diagram of a tunable energy harvester.

In extremely low power applications such as -40 dBm, it may be necessary to use antenna arrays to collect ambient RF energy to improve harvester sensitivity.

Appendix A

To derive equation 3.2, 3.3 and 3.4

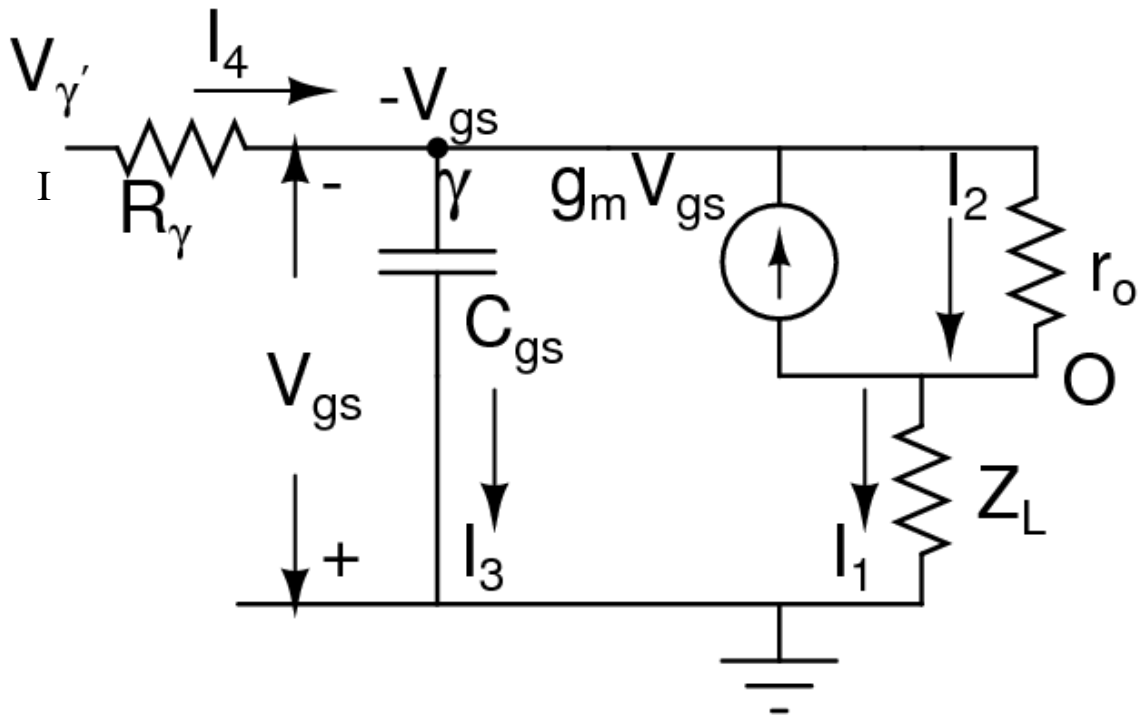


Figure A1: Equivalent circuit of transistor M3 as seen by voltage source V_γ with source resistance R_γ.

where Z_L is $R_L//(1/\omega C_t)$ and C_t is $(C_{gd}+C_{db})$.

KCL at point γ

$$I_4 = I_3 - g_m V_{gs} + I_2 \tag{A.1}$$

KCL at point O

$$I_1 = I_2 - g_m V_{gs} \tag{A.2}$$

KVL between γ and ground

$$I_3 = -j\omega C_{gs} V_{gs} \tag{A.3}$$

KVL across resistor R_γ

$$I_4 = \frac{V_{\gamma'} + V_{gs}}{R_\gamma} \tag{A.4}$$

KVL between I and ground through resistors R_γ, r_o and Z_L

$$V_{\gamma'} = I_4 R_\gamma + I_2 r_o + I_1 Z_L \tag{A.5}$$

Substitute equation 4 into equation 5 to remove I_4

$$-V_{gs} = I_2 r_o + I_1 Z_L \tag{A.8}$$

Substitute equation 3 and 4 into equation 1 to remove I_4 and I3

$$V_{\gamma'} + (1 + g_m R_\gamma + j\omega C_{gs} R_\gamma) V_{gs} = I_2 R_\gamma \tag{A.9}$$

Substitute equation A.8 into equation A.2 , A9 to remove V_{gs}

$$I_1(1 - g_m Z_L) = I_2(1 + g_m r_o) \tag{A.10}$$

$$V_{\gamma'} - (1 + g_m R_\gamma + j\omega C_{gs} R_\gamma) I_1 Z_L = I_2 (R_\gamma (1 + g_m r_o + j\omega C_{gs} r_o) + r_o) \tag{A.11}$$

Substitute equation A.10 into equation A.11 to remove I_2

$$\begin{aligned} V_{\gamma'} &= \frac{I_1}{1 + g_m r_o}(Z_L(1 + g_m R_\gamma + j\omega C_{gs} R_\gamma) + (R_\gamma(1 + g_m r_o + j\omega C_{gs} r_o) + r_o)(1 - g_m Z_L) \\ &= \frac{I_1}{1 + g_m r_o}(R_\gamma(1 + g_m r) + (1 + j\omega C_{gs} R_\gamma)(Z_L + r_o)) \end{aligned} \tag{A.11}$$

KVL between point O and ground

$$V_o = I_1 Z_L \tag{A.12}$$

Substitute equation A.12 into equation A.11 to get the voltage gain

$$A = \frac{V_o}{V_{\gamma'}} = \frac{Z_L(1 + g_m r)}{R_\gamma(1 + g_m r) + (1 + j\omega C_{gs} R_\gamma)(Z_L + r_o)} \tag{A.13}$$

At low frequency $g_m r_o >> 1$ and $j\omega C_{gs} R_\gamma \to 0$

$$A_{low} \approx \frac{Z_L}{R_\gamma} \tag{A.14}$$

At high frequency $j\omega C_{gs} R_\gamma (Z_L + r_o) >> R_\gamma (1 + g_m r)$

$$A_{high} = \frac{(1 + g_m r_o)}{(1 + sC_t r_o)(1 + sC_{gs} R_\gamma) + R_\gamma sC_t (g_m r_o + 1)} < \frac{1}{R_\gamma sC_t} << 1 \tag{A.15}$$

A.12, A.13 and A.14 are equation 2.2.2, 2.2.3 and 2.2.4 in chapter respectively.

Appendix B: Lump Model Extraction of on-chip Inductor

This appendix shows an simple way to accurate extract lump element value based on simulated Y parameter. The schematic of the lump elements of real inductor is shown in figure B1.

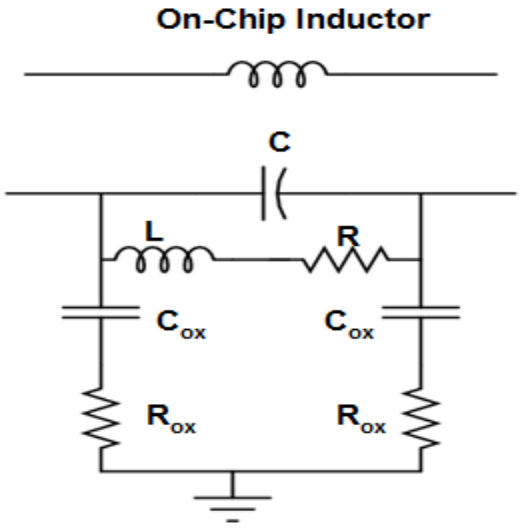


Figure B1. Lump model of on-chip inductor

Where L models the inductance of the on-chip inductor, R models the resistance losses due to the resistance of the metals. The capacitor C models the capacitance of the wind metal lines. The C_{ox} and R_{ox} model the capacitance and losses between the top metal line with the silicon substrates, respectively.

From the simulation results, the Y11 and Y12 can be read out as follows:

$Y11=2.0\,\mathrm{Real}(Y11) = 16\times10^{-4} - 1.857\times10^{-3}j$

$Y12=-1.922\times10^{-4}+2.251\times10^{-3}j$

From the schematic (Fsigure B1),

$$Y_{11} = \frac{i_1}{V_1}|_{V_2=0} = (\frac{R}{R^2+\omega^2L^2} + \frac{\omega^2 C_{ox}^2 R_{ox}}{1+\omega^2 C_{ox}^2 R_{ox}^2}) + j(\frac{\omega C_{ox}}{1+\omega^2 C_{ox}^2 R_{ox}^2} - \frac{\omega L}{R^2+\omega^2L^2})$$

$$Y_{12} = \frac{i_1}{V_2}|_{V_1=0} = -\frac{R}{R^2+\omega^2L^2} + j\frac{\omega L}{R^2+\omega^2L^2}$$

$$\mathrm{Re}al(Y_{11}) = \frac{R}{R^2+\omega^2L^2} + \frac{\omega^2 C_{ox}^2 R_{ox}}{1+\omega^2 C_{ox}^2 R_{ox}^2}$$

$$\mathrm{Im}ag(Y_{11}) = \frac{\omega C_{ox}}{1+\omega^2 C_{ox}^2 R_{ox}^2} - \frac{\omega L}{R^2+\omega^2L^2}$$

$$\mathrm{Re}al(Y_{12}) = -\frac{R}{R^2+\omega^2L^2}$$

$$\mathrm{Im}ag(Y_{12}) = \frac{\omega L}{R^2+\omega^2L^2}$$

$$\omega = 2\pi f$$

Where f is the extracted frequency which is equal to 880MHz in this example. There are four unknown C_{ox} , R ,L and C.

$$\mathrm{Re}al(Y_{12}) = -\frac{R}{R^2+\omega^2L^2} == \text{-}1.922\text{x}10^{-4}$$

$$\mathrm{Im}ag(Y_{12}) = \frac{\omega L}{R^2+\omega^2L^2} = 2.251\text{x}10^{-3}$$

$$\omega = 2\pi f = 5.529\times10^{9}$$

The R and L can be solved by the above two equations:

$$R = 37.66\Omega$$

$$\omega L = 441.03\Omega$$

$$\omega C_{ox} = 3.94\times10^{-4}\Omega$$

$$R_{ox} = 60.52\Omega$$

$$L = 79.77nH$$

$$C_{ox} = 71.33fF$$

The inductor peak Q can be simple estimated by

$$Q = \frac{\omega L}{R} = 11.72$$

The capacitor C is estimated in the following way:

1. Add a negative capacitance in parallel with the real inductor.
2. Calculate the inductance of the network using the S parameter.
3. The calculated inductance need to be flat over the resonance frequency. It increases with the frequency if there is no negative capacitance added. Adjust the negative capacitance value until the calculated inductance value become flat from low frequency to the resonance frequency. The added capacitance is used to cancel the modeled parallel capacitor C as shown in figure B1.

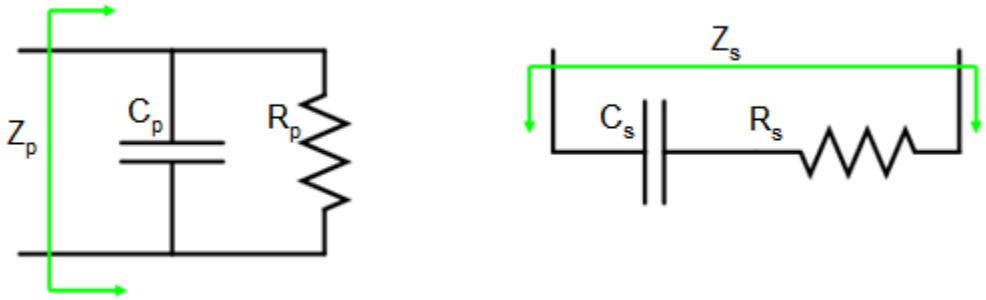
Following the above steps, the capacitor C value can be estimated.

$$C = 255fF$$

Another simple but less accurate estimation is to use the peak Q frequency (f_{peak}) given by the foundry and calculate the capacitor C using the following equation:

$$C = \frac{L}{4\pi^2 f_{peak}^2}$$

Appendix C



(a) (b)

Figure C.1 (a) RC network in parallel. (b) RC network in series.

The transformation between the above series connected RC network and equivalent parallel connected RC network is described below. For the series connected RC network as shown in Figure C.1 (b), the equivalent impedance Z_s is described by Equation C.1:

$$Z_s = \frac{1}{sC_s} + R_s \qquad \text{C.1}$$

Substituting s with jω we obtain:

$$Z_s = \frac{1}{sC_s} + R_s = R_s - j\frac{1}{\omega C_s} \qquad \text{C.2}$$

For a parallel connected RC network as shown in Figure C.1 (a), the equivalent impedance Z_p is described by Equation C.3:

$$Z_p = \frac{1}{sC_p} // R_p = \frac{R_p}{1 + sC_pR_p} = \frac{R_p(1 - sC_pR_p)}{1 + \left|s^2\right|C_p^2R_p^2} \qquad \text{C.3}$$

Substituting s with jω we obtain:

$$Z_p = \frac{R_p(1 - sC_pR_p)}{1 + |s^2| C_p^2 R_p^2} = \frac{R_p(1 - j\omega C_pR_p)}{1 + \omega^2 C_p^2 R_p^2} = \frac{R_p}{1 + \omega^2 C_p^2 R_p^2} - \frac{\omega C_p R_p^2}{1 + \omega^2 C_p^2 R_p^2} j \quad \text{C.4}$$

If

$$\omega^2 C_p^2 R_p^2 >> 1 \quad \text{C.5}$$

then Z_p can be simplified to Equation C.6:

$$Z_p = \frac{R_p}{1 + \omega^2 C_p^2 R_p^2} - \frac{\omega C_p R_p^2}{1 + \omega^2 C_p^2 R_p^2} j \approx \frac{1}{\omega^2 C_p^2 R_p} - \frac{1}{\omega C_p} j \quad \text{C.6}$$

The series connected RC network is equivalent to parallel connected RC network if their impedances are equal:

$$Z_p = Z_s \quad \text{C.7}$$

Substituting Z_p and Z_s into Equation C.6 gives the relationship between R_s, R_p,C_s and C_p as follows:

$$C_s = C_p$$
$$R_p = \frac{1}{\omega^2 C_s{}^2 R_s} \quad \text{C.8}$$

Substituting C8 into C5, the condition of the transformation can be written in form of series resistance and capacitance as follows:

$$\frac{1}{\omega^2 C_s{}^2 R_s^2} >> 1 \quad \text{C.9}$$

Appendix D (Inductor and Capacitor Real Layout Effects)

In ideal cases, the larger the C_{ac}, the smaller the voltage drop due to AC impedance and the better the system performance. In reality, the on-chip C_{ac} has an equivalent circuit as shown in Figure D.1. There are signal paths to ground which cause significant input power leakage to the substrate. The larger the capacitance is, the bigger the parasitic capacitance is and thus the higher the signal losses. There thus exists a design tradeoff between the power losses due to the AC voltage drop (small AC cap) and the power losses due to the leakage paths (big AC cap). The component C shown in Figure D.1 is the designed capacitor, while C_{sub} and R_{sub} correspond to the capacitance between the top metal with the silicon substrate and the losses through the silicon substrate. C_{sub} increases as the capacitor area increases. As the capacitance C increases, C_{sub} increases as well, which causes higher signal losses through the silicon substrate.

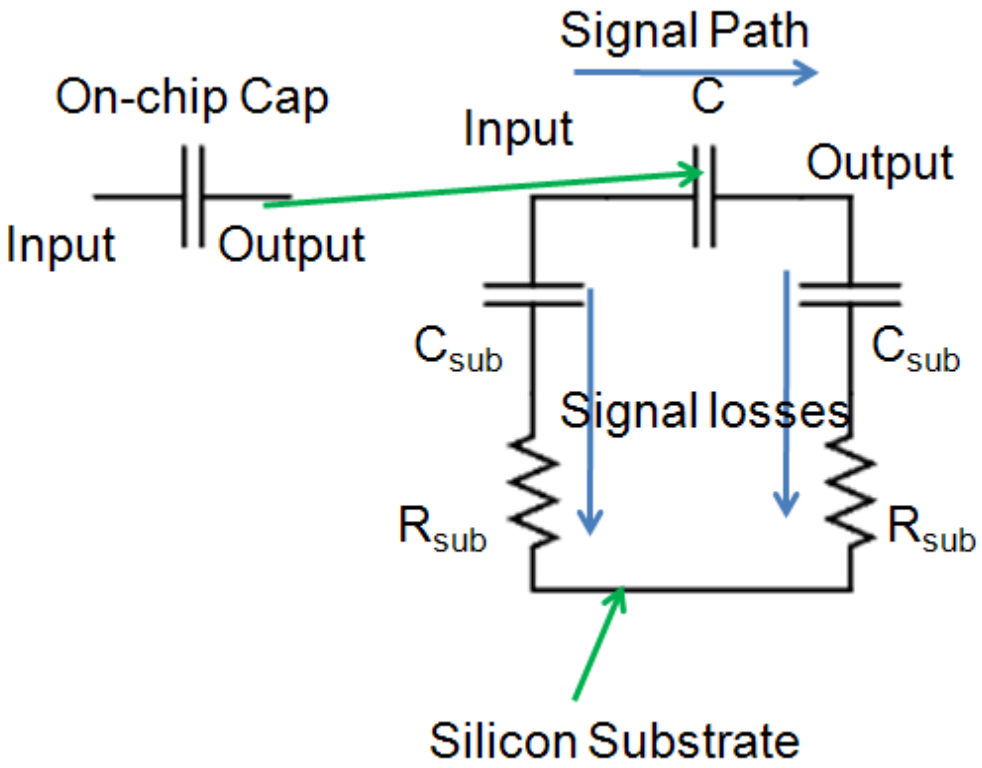
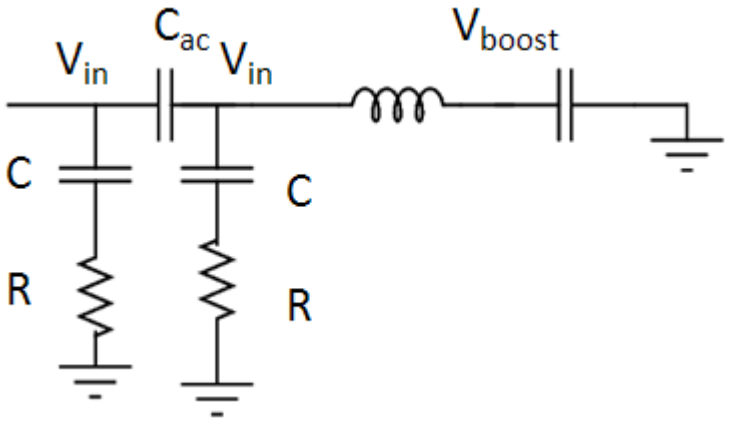


Figure D.1 Lump model of on-chip capacitors.

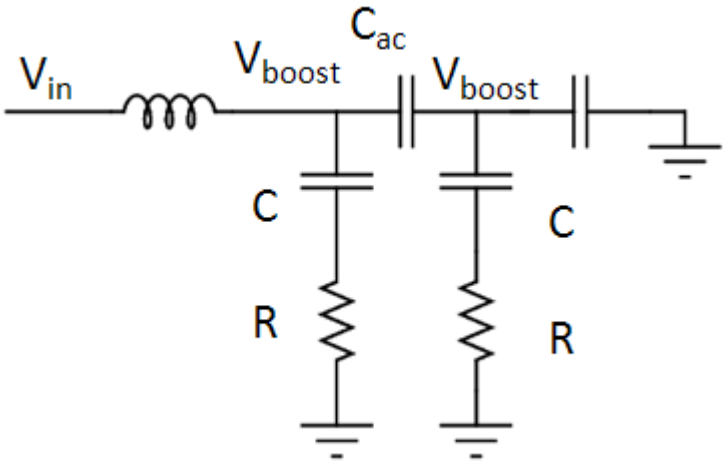
In previous work, Salter et al. [Salter2007C] have switched the position of the matching inductor and AC coupled capacitor (C_{AC}) by placing the capacitor in front of the inductor; in ideal conditions, the switching of the capacitor and inductor does not impact the harvester efficiency at all. The differences in efficiency come from the different parasitic losses under different voltages. Figure D.2 shows the circuit schematics of the two schemes. The power losses through the substrate for the on-chip capacitor or inductor can be described by Equation D.1:

$$P_{loss} = \mathrm{Re}\left(\frac{V_{AC}^2}{R + \frac{1}{j\omega C}}\right) \qquad \text{D.1}$$

The matching topology shown in Figure D.2 (a) has less signal power loss because the boosted signal V_{boost} is much larger than the input signal V_{in}.



(a)



(b)

Figure D.2 comparison of substrate losses occur due to the location switching of the on-chip capacitor and inductor. (a) low substrate loss topology; (b) high substrate loss topology.

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