ABSTRACT

Title of Dissertation: Cause and Effect of Threshold-Voltage Instability on the Reliability of Silicon-Carbide MOSFETs

Aivars Lelis, Doctor of Philosophy, 2011

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A significant instability of the threshold voltage (V_T) in silicon carbide (SiC) MOSFETs in response to gate-bias and *ON*-state current stressing was discovered and examined as a function of bias, temperature, and time. It was determined that the likely mechanism causing this effect is the charging and discharging of gate-oxide traps, located close to the interface of the SiC conducting channel, via a direct tunneling mechanism. High-temperature reverse-bias induced leakage current in the *OFF*-state was identified as a potential failure mode.

A simultaneous two-way tunneling model was developed, based on an existing one-way tunneling model, to simulate the time-dependent and field-dependent charging and discharging of the near-interfacial oxide traps in response to an applied gate-bias stress. The simulations successfully matched experimental results, both with respect to measurement time and to bias-stress time as a function of gate bias.

Experimental results were presented, showing that the V_T instability increases with both increasing gate-bias-stress time and bias-stress magnitude. The measurement

conditions, including gate-ramp speed and direction, were shown to have a significant influence on the measured result, with a 20-μs measurement revealing instabilities three times greater than those at standard 1-s measurement speeds, whereas 1-ks measurements showed shifts only half as large. High-temperature bias stressing was found to cause even more significant increases in the V_T instability. *ON*-state current stressing was found to also increase the V_T instability, due to self-heating effects.

V_T shifts as large as 2 V were reported, with the number of calculated oxide traps switching charge state varying between 1×10^{11} and 8×10^{11} cm^{-2}, depending on processing, stress, and measurement conditions. The standard post-oxidation NO anneal was shown to reduce the number of active oxide traps by about 70 percent.

The dominant oxide trap was identified as an *E′*-center type defect—a weak Si-Si bond due to an oxygen vacancy which has been broken during processing or subsequent device stressing. The large increase in bias-stress induced V_T instability at temperatures above 100 °C was explained by an increase in the number of active *E′*-center type defects.

Existing reliability qualification standards based on silicon device technology are inadequate for SiC MOSFETs and need to be revised, with particular attention paid to the measurement conditions.

CAUSE AND EFFECT OF THRESHOLD-VOLTAGE INSTABILITY ON THE RELIABILITY OF SILICON CARBIDE MOSFETS

by

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Dedication

Mammai un Tētim.

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1 Introduction

1.1 Research goals and thesis outline

Silicon carbide (SiC) is a compound, wide bandgap semiconductor with many superior material qualities that make it very attractive as a replacement for silicon (Si) in high-temperature power electronics. Because a native oxide can be grown on SiC, it is especially attractive for fabricating metal-oxide-semiconductor field-effect transistors (MOSFETs), which are the devices of choice for power systems engineers because they are both voltage-controlled and normally off. However, several outstanding reliability issues still remain, including operational-stress induced instability of the threshold voltage.

The goals of this research have been to study the threshold-voltage (V_T) instability phenomenon in SiC MOSFETs as a function of time, bias, and temperature, and to understand both the cause of this effect, as well as how it affects the reliability of power SiC MOSFETs for high-power converters for both military and commercial applications.

After providing an outline and listing key contributions, Chapter 1 goes on to discuss the military and commercial interest in SiC, and in particular SiC MOSFETs. Chapter 2 reviews the different types of interfacial charge at the SiC conducting channel/gate-oxide insulator interfacial region and how they affect the device characteristics. Basic materials analysis results of the transition regions on both sides of the SiC-silicon dioxide (SiO_2) interface are discussed, followed by a review of the few specific mentions of oxide trap charge in the literature. Given the similarity of the V_T

instability in SiC MOSFETs with that observed previously in irradiated Si MOSFETs, these previously observed effects are summarized and a successful model explaining the Si MOS V_T instability involving direct tunneling of electrons to and from near-interfacial oxide traps is reviewed along with key materials analysis results of the physical and chemical nature of the oxide trap defect from electron spin resonance measurement results. Chapter 3 then discusses the effect of the different types of interfacial charge on the threshold voltage, the theoretical calculation of the oxide field due to the presence of this charge, in particular trapped oxide charge, and how these results are applied by a numerical simulator to more precisely calculate the electric potential and thereby the electric field. This is used as input for the tunneling model discussed in Chapter 6.

Chapter 4 presents the basic experimental results, showing the effect of bias stress, time, and temperature on V_T instability. Chapter 5 presents the effects of measurement speed, and discusses how all these effects are consistent with a tunneling model. Also discussed are the results of subthreshold swing and charge separation analyses. Chapter 6 presents the results of a two-way tunneling analysis, allowing for the simultaneous charging and discharging of near-interfacial oxide traps as a function of gate-bias stress and time, during both the stress and the measurement of that stress. Both the successes and limitations of this model in comparison with experimental results and analysis are discussed. Chapter 7 discusses the V_T instability in SiC power MOSFETs, with special attention to effects at elevated temperatures where these power devices would be expected to operate. Reliability issues are addressed, including potential failure modes and mechanisms. Chapter 8 presents a summary of the study along with the main

conclusions. Also discussed are topics for future work, based on the work presented here.

1.2 Key contributions

- Discovered and communicated the basic V_T instability phenomenon in SiC MOSFETs and its significance as a potential HTRB (high-temperature reverse bias) reliability failure mechanism by increasing *OFF*-state leakage current.
- Demonstrated that this V_T -instability effect is due to the charging and discharging of near-interfacial oxide traps, and discussed how this likely involves interface traps in a two-step process.
- Developed and applied a simultaneous two-way tunneling model to match and explain the experimental results.
- Demonstrated the critical importance of measurement time to accurately determine the number of active switching oxide traps and their effects, given that oxide traps will change charge state due to the bias applied during the measurement as well.
- Discovered a large increase in bias-stress induced V_T instability at temperatures above 100 °C and explained this in terms of a bias-dependent high-temperature increase in the number of active *E′*-center oxide defects.
- Based upon a large variation in high-temperature V_T -instability results, suggested that the flat response of some SiC MOSFETs versus temperature may be due to a balance of oxide charge trapping effects and mobile ion drift.

- Suggested that many traps that are considered to be interface traps may actually be near-interfacial oxide traps. This is important since different types of interfacial charge are likely associated with different physical defects and will therefore respond differently to processing variations.
- Showed the effect of processing on the magnitude of the V_T instability: devices with an implanted channel, such as the power DMOSFET, exhibit a small increase; whereas devices that did not receive a post-oxidation NO anneal of their gate oxide exhibit a significant increase.
- Showed how, given the complex time, temperature, and bias dependence of the V_T-instability effect, existing reliability standards based on Si device technology are likely inadequate for SiC MOSFETs.

1.3 Why SiC MOSFETs?

SiC has many potential material advantages over Si for the development of high-temperature, high-voltage, and high-frequency power switches, including a much wider bandgap (3.26 eV at room temperature vs 1.12 eV for Si), a far higher critical field (2.2 MV/cm vs 0.25 MV/cm for Si), a larger saturation velocity (2×10^7 cm/s vs 1×10^7 cm/s for Si), and a much greater thermal conductivity (3.0-3.8 W/cm·K vs 1.5 W/cm·K for Si) [1,2]. The SiC values given are for 4H SiC, which is the preferred SiC polytype for vertical power devices given its high bulk mobility parallel to the *c* –axis [3, 4]. Although the effective channel mobility of 4H SiC MOSFETs in the lateral direction, perpendicular to the *c*-axis, tends to be intrinsically poorer than for 6H devices (likely

due to the slightly larger bandgap of 4H), this can be remedied with a standard post-oxidation NO anneal [5].

The wide bandgap allows electronic devices to operate at much higher temperatures before the intrinsic carrier concentration overwhelms the extrinsic doping. The much larger critical field means that much higher blocking voltages can be achieved for the same semiconductor thickness, or alternatively, much lower drift-layer resistances can be achieved for the same blocking level [6, 7]. These factors lead to devices with lower conduction and switching losses and increase efficiency, and to devices with increased power density. The much larger thermal conductance is useful in high power applications where devices generate their own heat that must be removed. However, this heat conduction is ultimately controlled by the thermal conductance of the entire package—that includes the die attach, thermal interface, and heat sink—which generally constitutes more than 90 percent of the total resistance in even the best packaging [8]. Operating at higher frequencies and higher temperatures will enable systems with much smaller weight and volume, due to the decreased size of passive system components and decreased cooling requirements. Moving from Si to SiC and replacing mechanical functions with electronics should increase system efficiency, functionality, and reliability.

Military and commercial applications include the power conversion (DC to AC inversion and DC to DC conversion) for hybrid-electric vehicles (HEVs), power generation and distribution, motor control, and power factor correction for power supplies for computers and electronic appliances. It is estimated that the introduction of SiC Schottky diodes into just 1.5 percent of the market has to date already saved in efficiency gains the electricity output of three coal-fired power plants [9]. Looked at

another way, this increased efficiency can lead to an improved standard of living for people all around the world by reducing their energy costs.

SiC MOSFETs are very attractive power switches, being both voltage-controlled and normally off. Bipolar junction transistors (BJTs) are normally off, but are current controlled devices, which require more complicated—and power dissipating—control circuits. Junction field-effect transistors (JFETs) are voltage controlled devices, but are normally on. Power engineers are naturally cautious, and prefer direct, normally off, replacement devices which fail safe. However, SiC BJTs and JFETs are easier to fabricate, and do not have as many materials issues as the SiC MOSFET [7], some of which are described in Chapter 2. (An alternative point of view is put forward by Treu, et al. [10], who argue the case for the power JFET precisely because of the SiC MOSFET reliability issues.) The Doubly-implanted MOSFET (DMOSFET) is the more common type of power MOSFET, given the UMOSFET's (named for its U-shaped trench) etched sidewalls and high-field crowding issues, although the implantations required for the DMOSFET lead to device degradations as well [7].

SiC power DMOSFETs have been successfully demonstrated by various companies, including Cree, GE, and Rohm [11, 12, 13]. Cree in fact has very recently announced the first commercial release of a 20-A, 1200-V device [14], although with limited negative bias and temperature rating [15]. The development of several different power conversion 1200-V modules has also been recently demonstrated, at current ratings of up to 550 A and junction temperatures up to 200 °C [12, 16, 17, 18, 19].

As is the case for Si, a thermal oxide can be grown on SiC [20], enabling the fabrication of MOSFETs. However, interfacial charge trapped at and near the SiC-SiO_2

inversion channel-gate insulator interface is far greater than in the Si case, especially in the upper half of the bandgap [4, 21, 22], and can lead to significant degradation in device performance by substantially reducing the effective channel mobility [5], as well as shifting the threshold voltage [23]. Previous works on SiC MOSFET reliability include an initial oxide processing study on the effects of interfacial charge on oxide breakdown [24]. Although time-dependent dielectric breakdown (TDDB) measurements indicate that the intrinsic gate-oxide strength of SiC MOS structures is similar to that of Si MOS structures [25, 26, 27, 28], with estimated lifetimes of 100 years at 3 MV/cm or higher, concern remains regarding extrinsic failures [26, 27, 28]. The past few years have also led to a general appreciation of V_T instability as an important reliability issue [9, 26, 29, 30].

2 Background

2.1 Review of the different types of interfacial charge

According to the Deal Committee formulation for Si MOS [31], charge at the interface and in the gate oxide can be categorized as due either to fixed oxide charge (Q_F, N_F), mobile ionic charge (Q_M, N_M), interface trapped charge (Q_{IT}, N_{IT}), or oxide trapped charge (Q_{OT}, N_{OT}), with Q representing a net charge per unit area and N representing the net number of charges per unit area for each type of charge. (See Chapter 3 for a discussion of how the actual charge density—which may be, for example, distributed across the oxide— is related to an effective charge density at the interface.) It is likely that this same convention can also be successfully applied to SiC MOS. A modification of the famous figure from Deal [31], indicating the names and locations of the various types of interfacial charge, is presented in Figure 2-1 for SiC.

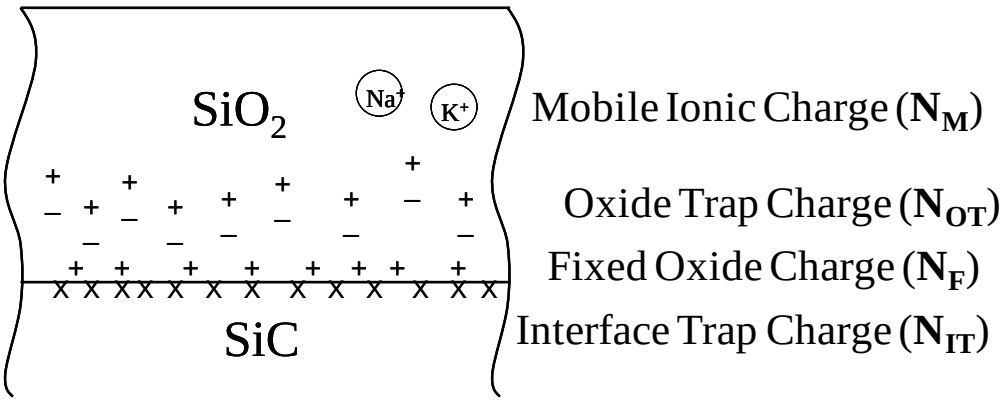

Figure 2-1: A modification of the Deal [31] Si MOS figure, indicating the names and locations of the various types of interfacial charge for SiC MOS.

All the different types of charge, even those in the oxide if they are close enough to the SiC interface, can cause a decrease in the actual channel mobility due to

Coulombic scattering [32, 33]. The net charge, due to the sum of the different types of positive and negative charge present, can also reduce the effective mobility for a given surface potential due to a reduction of free carriers in the channel [34]. The importance of using Hall mobility measurements to separate the actual channel mobility from the presumed effective mobility was popularized by Saks in a series of papers that are summarized in a recent review article [35]. This reduction in channel mobility results in a greater *ON*-state resistance than would otherwise be the case. The net charge will also cause a shift of the threshold voltage (V_T), with a net positive charge causing a negative shift and a net negative charge causing a positive shift (see Chapter 3 for details). Although thinning the gate oxide will reduce the V_T shift caused by this trapped charge, it also invites potential long-term gate oxide reliability issues revealed by time-dependent dielectric breakdown (TDDB) analysis [25, 26, 27, 28]. For an *n*-channel MOSFET, a negative shift will cause an increase in *OFF*-state leakage current and a positive shift will also cause an increase in *ON*-state resistance (see Chapter 7 for a discussion of how this impacts the power MOSFET). Finally, oxide traps, especially those near the SiC interface, are probably the cause of the instabilities observed in the threshold voltage following gate-bias stressing [23, 36, 37, 38, 39, 40, 41, 42, 43, 44, 45, 46, 47, 48, 49, 50, 51, 52, 53], which is the focus of this study.

This interfacial charge may lie on both sides of the SiC-SiO_2 interface, where the conducting channel of the semiconductor meets the gate insulator of the MOSFET. Transition layers have been observed on both sides of this interface using transmission electron microscopy (TEM), electron energy loss spectroscopy (EELS), and X-ray photoelectron spectroscopy [54, 55, 56, 57, 58]. These layers appear to be due to

chemical/compositional changes and extend several nanometers on both sides of the interface. A carbon (C) rich (or Si poor) region on the SiC side of the interface has been reported by several different groups [56, 59]. Recent work employing electron spin resonance techniques have led to an initial understanding of the physical and chemical nature of the interface traps. The dominant defect for thermally grown oxides on SiC appears to be a Si vacancy within the SiC near the interface [60, 61], and the dominant defect for deposited oxides on SiC appears to be a dangling bond right at the interface [62].

Many papers have also reported evidence of an oxide transition layer [57]. This oxide layer may be due to the presence of C [59], or it may simply be that the topology and the geometry of the SiC surface are not suitable for an abrupt oxide interface [63]. It has also been suggested that although the oxide on SiC is stoichiometric SiO_2, there exists a greater strain in the oxide grown on SiC [64]. In SiC these various effects can result in C clusters or C-related dangling bonds, suboxide bonds, and/or other defects which can trap charge—such as an oxygen (O) vacancy related to a broken Si-Si bond, referred to as an E' center [65]. This particular defect, which may very well be the source of the dominant oxide trap [61], will be discussed in much greater detail in a subsequent section of this chapter. It has been reported that the nitrogen (N) from the post-oxidation NO anneal used to reduce the interface trap density may cause additional charge trapping [66].

Numerous papers have addressed the effect of interface traps, particularly on low channel mobility. Modeling papers have found that Coulombic scattering due to interfacial charge is the dominant mechanism limiting channel mobility, but they

generally assumed that this charge was mainly due to interface traps and did not specifically discuss the effect of oxide traps [32, 67]. A recent review article discusses interface traps and SiC in great detail [68]. Oxide traps are mentioned in passing, with speculation that an E' center may be involved. Finding processing steps to reduce N_{IT}, particularly the high density of interface traps (D_{IT}) near the conduction band edge, has been the main focus for the past decade and a great deal of effort has been exerted in finding processing steps that reduce these densities, including the development of the nitrogen post-oxidation anneal [69, 70, 71].

However, the success of this effort in reducing negatively charged interface traps has led, in some cases, to negative threshold voltages which may result in normally-*ON* devices or, at the very least, MOSFETs with high *OFF*-state leakage currents. This is due to the as-yet unreduced large numbers of interfacial and near-interfacial positive charge, which charge separation analysis indicates exceeds 1×10^{12} cm^{-2} in typical SiC MOSFETs [72]. Clearly, more focus is needed on finding improved processing steps to reduce N_F and N_{OT} as well so that the present balance between large numbers of positive and negative trapped charge in *n*-channel SiC MOSFETs, which in general leads to reasonable threshold voltages, is made less precarious. The threshold-voltage instability phenomenon clearly demonstrates that not all the non- N_{IT} trapped charge is fixed and that at least some of this charge must be due to N_{OT} that is close enough to the interface to exchange charge over the time scales observed [23]. In this capacity, V_T instability measurements provide a method for determing the lower bound for the calculation of N_{OT} (see Chapter 5).

In Si MOS, N_F was believed to occur in the first 25 Å of the oxide from the Si interface due to structural defects such as ionized Si, but was not in electrical communication with the Si [31]. Presumably similar fixed charge exists for SiC MOS, but the physical nature of this charge has not yet been identified.

Mobile ions have generally been thought to not be an issue, although the variation in the high-temperature V_T -instability response, discussed in Chapters 4 and 7, may be the result of a variation in the mobile ion content. Since charge-trapping, likely caused by the filling or emptying of near-interfacial oxide traps, and mobile ion drift have opposite effects on V_T for a given bias stress, a small effective V_T shift at high temperature may be due to a balance of these two effects.

Oxidation in the presence of alumina has been recently reported to increase channel mobility [73, 74]. However, many contaminants are introduced into the oxide by this process, including alkali metals such as Na, K, Ca, and Mg, and transition metals such as Fe, Ni, Ti, and Cr. Significant threshold voltage shifts due to mobile ions have been reported as a result, due mostly to the sodium contamination [73].

2.2 Other work related to oxide charge trapping in SiC MOS

In addition to my work on the threshold-voltage instability of SiC MOSFETs due to the charging and discharging of near-interfacial oxide traps described in this thesis (and presented at various international conferences and published in various proceedings and journals [23, 37, 38, 39, 42, 43, 45, 47, 48, 50, 51]), a few other works in the literature have also discussed oxide charge trapping in SiC MOSFETs, and recent work has confirmed the threshold-voltage instability phenomenon described here.

Most of the work on SiC MOSFETs regarding charge trapping at or near the SiC/SiO_2 interface has been related to the low effective mobilities that are typically measured, and processing variations that reduce the interface trap density. Oxide traps or fixed charge are rarely mentioned. Although oxide traps are only rarely discussed in SiC, it is a big issue for Si MISFET devices that have gate insulators made with high-dielectric constant (high-*k*) compounds. With the continued scaling of Si CMOS devices and the accompanying thinning of their gate oxides, the use of alternative dielectrics with high-*k* values has become conventional. Since devices with these alternative gate dielectrics have a lot of oxide traps, it is not surprising that they also have significant threshold-voltage instabilities [75]. One measurement method developed for analyzing the trapping effect in high-*k* Si MISFETs is a fast *I*-*V* (current-voltage) system [76]. This system was replicated by Dr. John Suehle's team at NIST (National Institute for Science and Technology), with whom I began a collaboration after visiting them and realizing that their fast *I*-*V* system would be very helpful in the study of oxide traps in SiC. (The details of the experimental procedure are given in Chapter 4 and some of the experimental results of our collaboration are presented in Chapter 5.) Moshe Gurfinkel, the graduate student in his lab that set-up and used the fast *I*-*V* system became very interested in the study of SiC and made numerous additional measurements providing additional confirmation of the time-sensitive nature of the I_D-V_{GS} characteristics [40, 41].

Marko Tadjer, another graduate student at the University of Maryland, also became interested in the study of the V_T instability of SiC MOSFETs after hearing about my results, and subsequently also presented a study of the bias, time, and temperature effects [46].

Following my presentation at the 2006 Spring MRS meeting [38], I advised researchers from GE regarding their own, subsequent V_T -instability measurements [44]. Even more recently, researchers from Germany [49] and Japan [52] have presented initial studies of shifts in V_T as a function of bias, time, and temperature.

One early paper on SiC MOS charge trapping presented results of measurements on MOS capacitors [24]. It actually assessed the potential of various alternative dielectrics in addition to deposited and thermally grown SiO_2. The researchers from Cree presented results not only on the interface trap density, but the net oxide charge densities as well by comparing their measured and calculated ideal flat-band voltages. They observed hysteresis in their *C-V* (capacitance-voltage) measurements, but attributed that to interface-trap charging.

In their study of the effects of nitridation on properties of the SiC-SiO_2 interface, Afanas'ev, et al. concluded that two different types of traps are present, fast interface traps and very slow states "likely related to defects in the near-interface oxide layer" [77]. Rozen, et al. found that nitridation reduced the interface trap density and susceptibility to electron trapping, but increased hole trapping [66]. Recent work by Kong, Dimitrijev,and Han have concluded that time-dependent variations in SiC MOS capacitor *C-V* characteristics are due to the presence of near-interface oxide traps that are either neutral or positively charged [78]. They adopted a direct tunneling analysis presented previously by Tewksbury, et al. [79] for the study of V_T instability in Si MOSFETs. Even more recent work by Basile, et al. also looking at the time-dependent responses of SiC MOS capacitor C-V characteristics and using constant-current deep-level transient spectroscopy (DLTS) found three types of charge traps: oxide traps, interface traps, and

semiconductor bulk traps [80]. The presence of a SiC bulk trap has also been suggested by Agarwal, et al. [81]. These conclusions are consistent with the materials analysis work mentioned in the previous section.

Several papers over the past decade have addressed the radiation response of SiC MOSFETs [82, 83, 84]. *n*-channel devices have generally exhibited a positive shift whereas *p*-channel devices have exhibited a significant negative shift. This implies that interface trap formation dominates over the creation of oxide traps, although very recent and as yet unpublished results show a negative shift of V_T following the irradiation of an *n*-channel SiC MOSFET under positive-bias stress—implying that the filling of positively-charged oxide traps is dominating the response [85]. Lee, et al. [83] used subthreshold swing analysis to attempt to separate interface traps from oxide traps. The importance of oxide traps is discussed in detail in the next section.

2.3 Review of threshold-voltage instability in irradiated Si MOS

The instability of V_T in SiC MOSFETs is reminiscent of a similar effect observed in irradiated Si MOSFETs described in earlier work [86, 87, 88, 89, 90]. Exposing Si MOSFETs to ionizing radiation was found to lead to the creation of electron-hole pairs in the gate oxide, with some fraction escaping immediate recombination. With a positive bias applied to the gate, the electrons are quickly swept out to the gate electrode and the holes make their way toward the Si-SiO_2 interface via a stochastic-hopping transport mechanism, with many holes becoming trapped in deep trap sites in the oxide near the interface [91, 92]. These trapped holes lead to a negative shift of the threshold voltage. However, this V_T shift is not permanent, and is observed to "anneal" over time, even at

room temperature. That is, especially under the presence of a positive gate bias, the post-irradiation V_T shift becomes less negative over time. This was initially explained by electrons tunneling in from the Si substrate to recombine with the trapped holes. However, it was further observed that if subsequently a negative gate bias is applied, that some of the previously annealed charge would return and V_T would shift back to the left [86, 87].

My colleagues and I at the former Harry Diamond Laboratories (HDL—a pre-cursor of the present U.S. Army Research Laboratory) performed a series of studies to better understand this "reverse annealing," or reversibility, phenomenon [88, 89, 90], and proposed a molecular model to explain this instability, which we attributed to the filling and emptying of near-interfacial oxide traps via a direct tunneling mechanism. This V_T instability in irradiated Si MOSFETs is in many ways very similar to the bias instability observed in as-processed SiC MOSFETs described in this work.

We found that there was a difference in the magnitude of the reversibility depending on the processing. Devices with hardened gate oxides, whose initial post-irradiation negative V_T shift is much smaller than that of unhardened devices, displayed significant "reverse annealing." Devices with unhardened or "soft" gate oxides showed little or no "reverse annealing" [88]. However, at elevated temperature (up to 150 °C), the devices with "soft" gate oxides also began to display significant reversibility of the V_T annealing. The devices with "hard" gate oxides also showed some increase in reversibility, but the percentage change was much smaller [89].

We also found that the amount of reversibility as a percentage of the initial V_T shift was measurement speed dependent. Fast 100-μs ramp *I*-*V* (and *C*-*V* for similarly

processed capacitors) measurements revealed that only a relatively small fraction (about 15 percent for one sample set) of the total initial V_T shift that was annealed was reversible, even though slower 1-s ramp *I-V* measurements gave the impression that such samples experienced a 100 percent reversibility of all the previously annealed charge. We also observed using our fast *I-V* system that if the bias was switched from positive gate bias to negative very early during the original anneal, e.g., after only 1 ms, the device would experience an initial V_T shift back to the left and then resume annealing back to the right, although at a slower rate than under positive gate bias [88]. This time dependence of the measurements is also observed in as-processed SiC MOSFETs (see Chapter 5).

2.4 Review of magnetic resonance work and the HDL oxide hole trap model

Many years ago, Lenahan and Dressendorfer [93] confirmed using electron spin resonance (ESR) techniques, coupled with electrical *C-V* measurements, that the *E′* center was in fact the dominant radiation-induced oxide hole trap in Si MOSFET gate oxides, confirming previous speculation by Marquardt and Sigel [94]. They found that the V_{MG} shift, due entirely to oxide trapped holes since the interface traps are uncharged at the mid-gap surface potential, correlated very well with both the increase in the number of *E′* centers immediately following irradiation, as well as during a subsequent anneal. They also confirmed, by etching back the oxide, that most of the *E′* centers were located near the Si-SiO_2 interface.

The *E′* center consists of two Si atoms, each back-bonded to three different O atoms, and is activated by the breaking of a weak Si-Si bond, which occurs due to an O

vacancy (see Figure 2-2 (a) and (b)). This is due to the Si rich nature of the oxide in the interfacial region [95]. The weak Si-Si bond can be broken either by radiation-induced holes or during processing. As discussed below, it appears that they can also be broken at elevated temperature in the presence of an applied bias [96].

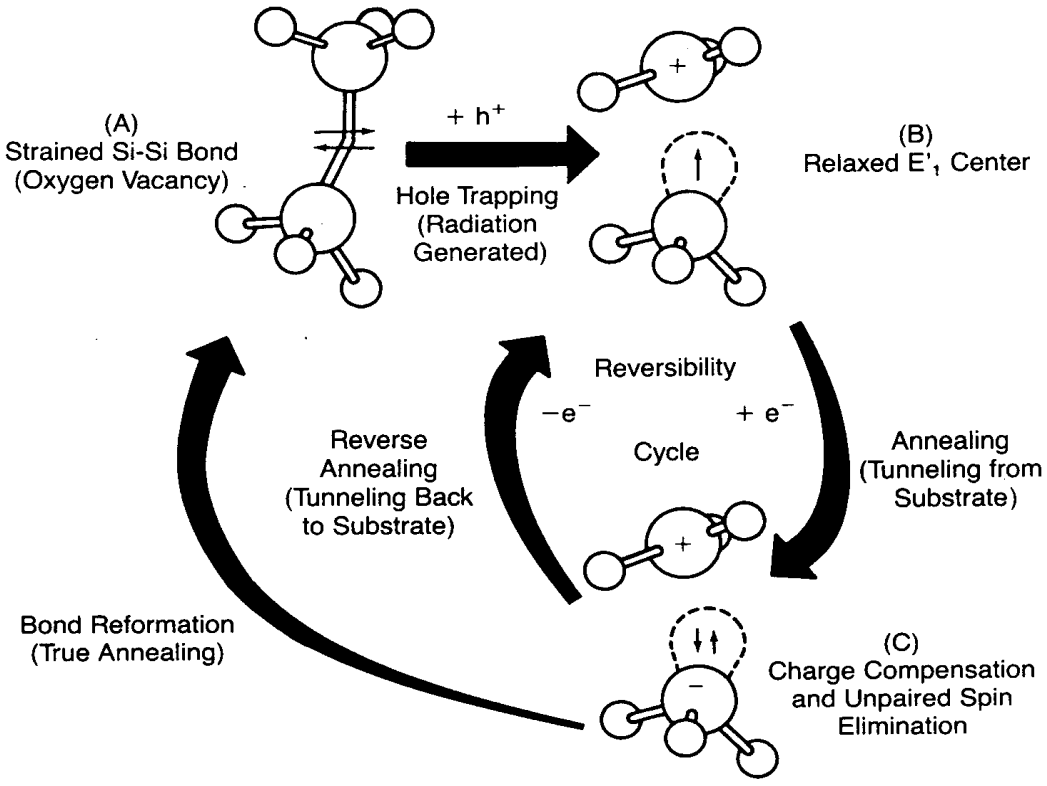

Figure 2-2: HDL (ARL) hole trap model [88].

Figure 2-2 is a depiction of the hole trap model put forward by my colleagues and me at HDL to explain the hole trap "reverse annealing" phenomena, based on the results of Lenahan and Dressendorfer [93]. When the radiation-induced hole breaks the weak Si-Si bond (see Figure 2-2(a)), the hole is captured by one of the Si atoms and the other is left with a dangling bond—see Figure 2-2(b). The ESR measurement detects the unpaired spin of this dangling bond, with different defects identified by their own unique

signatures. During the subsequent anneal, the ESR signal decreased along with the reduction in the V_{MG} shift. This implies that either the bond was reformed, eliminating both the trapped hole and the unpaired spin of the dangling bond, or that a compensating electron tunneling into the oxide was captured by the previously uncharged Si atom, leading to a charge-neutral dipole and the elimination of the unpaired spin by filling both orbitals—see Figure 2-2(c). The reverse-anneal effect was explained simply by one of the electrons tunneling back out, leaving behind the original active E' complex, as depicted in Figure 2-2(b). This model was subsequently confirmed with ESR work performed by Conley and Lenahan, et al. [97, 98], who showed that the E' signal grew larger again under negative bias during the reverse anneal, following a previous decrease under positive bias, and that this process was repeatable—just like the electrical V_T instability. Recent work has incorporated this same model as the first step of a new two-step model to explain negative bias temperature instability (NBTI) effects in Si MOS [99]. This defect has also been suggested to act as a neutral electron trap [100].

It is likely that when the weak Si-Si bond is first broken, the O atoms back-bonded to the positively charged Si atom without the dangling bond relax back to a more planar configuration and that the two Si atoms move further apart, depending upon the existing bond strain [101]. The further apart they move, the less likely that the bond will reform. Only reformation of the Si-Si bond would result in true “annealing” of the trapped positive charge and deactivation of the defect site. Devices with hardened gate oxides are generally under more bond strain and therefore more likely to move apart and not reform [88]. However, as mentioned previously, a significant increase in the V_T instability occurs in devices with unhardened oxides at temperatures above 100 °C, suggesting that

elevated temperature will also cause the two Si atoms to move apart [89]. It may also cause some Si-Si bonds to break, creating active defect sites.

This is essentially the effect that was recently reported by Ryan, Lenahan, et al. who found, using on-the-fly ESR techniques in the study of NBTI in Si MOS, that the number of E' centers increased dramatically with bias at temperature, but not with temperature stress alone [96]. In addition, they found that the number of oxide defects markedly decreased when the sample was returned to room temperature. This is very similar to the V_T instability behavior observed in SiC MOSFETs (see Chapter 7). Since the V_T instability is likely a measure of the number of active near-interfacial oxide traps, these results suggest that the application of a gate bias at elevated temperature will break existing Si-Si bonds and activate additional E' center defects that can act as near-interfacial oxide traps. This argument is made more compelling given that Cochrane, Lenahan, et al. have recently reported that E' type oxide defects have been observed in SiC MOSFETs using electrically detected magnetic resonance (EDMR) techniques under a strong negative gate bias—conditions most conducive to detecting unpaired spins in the E' complex [61]. (This appears to confirm previous speculation regarding the nature of at least some of the near-interfacial oxide traps [21, 23].) They further suggested that in this case the EDMR likely involved spin dependent trap-assisted tunneling between defects on both sides of the interface. If all this is so, then it is important to develop improved processing methods to decrease the number of precursor oxide defect sites—or to decrease the bond strain near the interface.

2.5 Summary

Although most works on SiC MOSFETs focus on interface traps and fixed charge, it is likely that oxide traps, especially those very close to the SiC interface, are responsible for the threshold-voltage instability via a direct tunneling mechanism. It is important to distinguish between interface traps and near-interfacial oxide traps, even though it may be difficult to distinguish between the two during very fast measurements, since it is likely that they are associated with different types of physical defects—and therefore processing variations will affect them differently.

The V_T instability observed in as-processed SiC MOSFETs is reminiscent of a similar instability previously reported in irradiated Si MOSFETs. In that case the dominant radiation-generated defect was found to be an E' center, which consists of a broken Si-Si bond associated with an O vacancy. Even with all the reports of excess C on both sides of the interface, the only oxide defect so far observed using ESR on SiC MOS test structures is an E' type defect. This suggests that the tunneling analysis previously applied to irradiated Si MOSFETs may be successfully applied to as-processed SiC MOSFETs to explain the V_T instability. Furthermore, processing variations that improved radiation hardness in Si MOSFETs may provide insight in how to—and how not to—reduce V_T instability in SiC MOSFETs.

3 Calculation of Oxide Field and Threshold-Voltage Shift Caused by Interfacial Charge

3.1 Introduction: Calculation of electric potential in the gate oxide and the SiC channel region

This chapter describes the calculations employed to determine important input parameters for the tunneling model to be described in Chapter 6. Specifically, it is necessary, given a distribution of charged near-interfacial oxide traps, to determine the electric field in that region of the gate oxide for any applied gate-to-source voltage, V_{GS}. It is also important to determine the corresponding inversion carrier concentration, as that likely plays a role in determining the interface-trap occupation response time, as well as being a possible source of electrons which can tunnel into the oxide to neutralize the likely positively charged near-interfacial oxide traps.

The electric potential is calculated in both the oxide and SiC regions, first analytically, and then more precisely by way of numerical simulation using standard techniques. The analytical solution provides a starting point for the more exact numerical solution. Each will be described in turn, from which the gate oxide field and inversion carrier concentration can be readily derived.

In order to calculate the electric potential in both the oxide and the SiC for a given V_{GS}, it is first necessary to determine the relationship between the applied gate voltage and the potential drops across both the oxide and the SiC. The standard formulation, including the effects of the work-function difference between the poly-Si gate and the

SiC semiconductor, and the effects of trapped charge at the SiC-SiO_2 interface, is as follows:

$$\begin{aligned} V_{GS} &= V_{FB} + V_{OX} + V_{\text{int}} + V_{SiC} \\ &= V_{FB} + V_{OX\_net} + V_{SiC} \end{aligned} \tag{3-1}$$

where V_{FB} is the gate voltage needed to achieve flat-band conditions due to the work-function difference noted above, V_{OX} is the potential drop across the gate oxide due only to inversion channel charge, V_{int} is the voltage shift caused by the presence of the net sum of the interfacial trapped charge present—and which modifies the potential drop across the gate oxide, V_{OX_net}, and V_{SiC} is the potential drop in the SiC.

For the ideal case, where there is no interfacial trapped charge, this reduces to

$$V_{GS\_ideal} = V_{FB} + V_{OX} + V_{SiC} \tag{3-2}$$

Before proceeding to describe each component in detail, it is useful to define the electric potential, ϕ, the bulk potential in the SiC, ϕ_B, and the band bending in the SiC, ψ. The bulk potential in the SiC is calculated from the doping density, and is related to the difference between the intrinsic, mid-gap energy level, E_i, and the Fermi level, E_F:

$$\phi_B = \frac{kT}{q} \cdot \ln\left(\frac{N_a}{n_i}\right) = \frac{E_{i\_bulk} - E_F}{q} \tag{3-3}$$

where N_a is the *p*-type doping in the SiC, n_i is the intrinsic carrier concentration, q is the electronic charge, k is Boltzmann's constant, and T is absolute temperature.

The band-bending can be defined as the amount of deviation from the SiC bulk flat-band condition, which can also be related to the bulk potential and Fermi level:

$$\psi(x) = \frac{E_{i\_bulk} - E_i(x)}{q} = \phi_B + \frac{E_F - E_i(x)}{q} \tag{3-4}$$

The surface potential is the degree of band-bending at the SiC-SiO_2 interface, and can be defined by the deviation from flat-band conditions in terms of the bulk potential, ψ_s (ϕ_B). In other words, at flat-band, there is no band bending and so $\psi_s = 0$. At mid-gap, ψ_s has been bent by one ϕ_B, such that E_i is now equal to E_F and the electron carrier concentration at the surface equals that of the holes. When ψ_s has been bent by two ϕ_B, the surface is at inversion such that E_i is now one ϕ_B below E_F and the electron carrier concentration at the surface is now equal to the hole carrier concentration in the bulk for an *n*-channel MOSFET. Any further increase in the band bending at this point will drive the surface into strong inversion, with a dramatic increase in the electron carrier concentration in the first few nanometers of the SiC. On the other hand, when the surface potential is negative, the surface is driven into accumulation, where the hole carrier concentration increases dramatically.

$$\psi_S = \psi(x=0) = \frac{E_{i\_bulk} - E_i(x=0)}{q} \tag{3-5}$$

The potential, $\phi(x)$, is defined so that when $\phi = 0$ the equilibrium electron and hole carrier concentrations are both equal to the intrinsic carrier concentration, n_i. This implies that the potential at the interface, ϕ_{int}, will equal zero at mid-gap, when $\psi_s = \phi_B$. Thus, the potential in the SiC can be written in terms of the band bending:

$$\phi(x) = \psi(x) - \phi_B = \frac{E_F - E_i(x)}{q} \tag{3-6}$$

And the electron and hole carrier concentrations can be defined in terms of the electric potential:

$$n(x) = n_i \cdot \exp\left(\frac{q \cdot \phi(x)}{kT}\right) = n_i \cdot \exp\left(\frac{E_F - E_i(x)}{kT}\right) \tag{3-7}$$

$$p(x) = n_i \cdot \exp\left(\frac{-q \cdot \phi(x)}{kT}\right) = n_i \cdot \exp\left(\frac{-[E_F - E_i(x)]}{kT}\right) \tag{3-8}$$

3.2 Calculation of the Flat-band voltage, V_{FB}

The individual components of the voltage drop from gate to source can be calculated as follows. The flat-band voltage is due to the difference in the work functions of the poly-Si gate and SiC substrate.

$$V_{FB} = \phi_{ms} = (\chi_{Si} + \frac{E_{g\_Si}}{2 \cdot q} + \phi_{poly}) - (\chi_{SiC} + \frac{E_{g\_SiC}}{2 \cdot q} + \phi_B) \tag{3-9}$$

where ϕ_{ms} is the work-function difference between the "metal" (*p*-type poly-Si) and the semiconductor (*p*-type SiC); χ_{Si} and χ_{SiC} are the electron affinities of the poly-Si and SiC, respectively; E_{g_Si} and E_{g_SiC} are the bandgap energies of Si and SiC, respectively; ϕ_{poly} is the bulk potential of the highly doped *p*-type poly-Si gate, and and ϕ_B is the bulk potential for the *p*-type SiC—which is the normalized difference between the Fermi level, E_F, and the mid-gap level, E_i.

For example, if the SiC *p*-type bulk is doped 1×10^{16} cm^{-3} and the poly-Si is boron doped to 3×10^{19} cm^{-3}, then

$$V_{FB} = \phi_{ms} = (4.05 + \frac{1.11}{2} + 0.555) - (3.60 + \frac{3.26}{2} + 1.424) = -1.494 \text{ V}$$

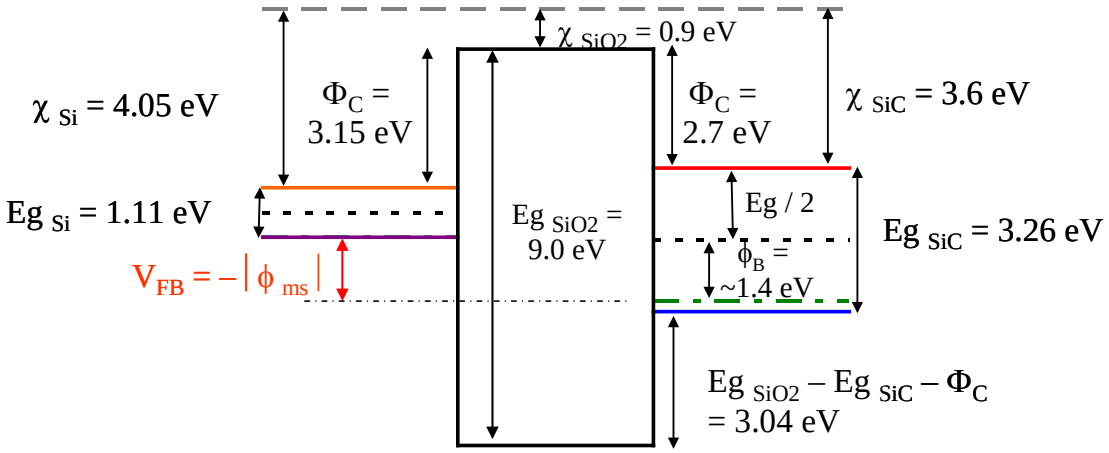

Figure 3-1: Schematic of the energy bands for, from left to right, the *p*-type poly-Si gate, the gate oxide, and the *p*-type SiC.

3.3 Calculation of V_{SiC} and V_{OX} in the absence of interfacial charge

The potential drop in the SiC is the difference between the electric potential at the surface, $\phi(x=0)$, and in the bulk, $\phi(x=bulk)$, which is the surface potential, ψ_s:

$$V_{SiC} = \phi(x=0) - \phi(x=bulk) = \left[\psi(x=0) - \phi_B\right] - \left[-\phi_B\right] = \psi_s \tag{3-10}$$

The electron and hole carrier concentrations, (3-7) and (3-8), respectively, can be re-written in terms of the band-bending. First, note that the equilibrium hole and electron carrier concentrations can be found, for a conventionally doped *p*-type semiconductor, as

$$p_0 = N_a = n_i \cdot \exp\left(\frac{q \cdot \phi_B}{kT}\right) \tag{3-11}$$

$$n_0 = \frac{n_i^{\,2}}{p_0} = n_i \cdot \exp\left(\frac{-q \cdot \phi_B}{kT}\right) \tag{3-12}$$

Therefore, the electron and hole carrier concentrations can be re-written as follows:

$$n(x) = n_i \cdot \exp\left(\frac{q \cdot \phi(x)}{kT}\right)$$
$$= n_i \cdot \exp\left(\frac{q \cdot [\psi(x) - \phi_B]}{kT}\right) = n_0 \cdot \exp\left(\frac{q \cdot \psi(x)}{kT}\right) \tag{3-13}$$

$$p(x) = n_i \cdot \exp\left(\frac{-q \cdot \phi(x)}{kT}\right)$$
$$= n_i \cdot \exp\left(\frac{-q \cdot [\psi(x) - \phi_B]}{kT}\right) = p_0 \cdot \exp\left(\frac{-q \cdot \psi(x)}{kT}\right) \tag{3-14}$$

The electric field at the semiconductor surface can be related to the surface potential by solving Poisson's Equation, as is described in Sze [102], Streetman [103], and surely other standard device physics texts.

$$\frac{\partial^2 \psi(x)}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q}{\varepsilon_s} \cdot \left[p(x) - n(x) - N_a^- + N_d^+\right] \tag{3-15}$$

where ρ is the charge density, ε_s is the permittivity of the semiconductor, and N_d is the *n*-type doping in the SiC (if present).

Poisson's Equation can be solved to obtain the following equation for the electric field:

$$\mathcal{E}(x) = \sqrt{\frac{2 \cdot kT \cdot N_a}{\varepsilon_s}} \cdot$$
$$\sqrt{\left(\exp\left(\frac{-q \cdot \psi(x)}{kT}\right) + \frac{q \cdot \psi(x)}{kT} - 1\right) + \frac{n_0}{p_0} \cdot \left(\exp\left(\frac{q \cdot \psi(x)}{kT}\right) - \frac{q \cdot \psi(x)}{kT} - 1\right)} \tag{3-16}$$

The pre-factor is commonly written in terms of the Debye length,

$$L_D = \sqrt{\frac{\varepsilon_s \cdot kT}{q^2 \cdot N_a}} \tag{3-17}$$

so that

$$\mathcal{E}(x) = \frac{\sqrt{2} \cdot kT}{q \cdot L_D} \cdot \sqrt{\left(\exp\left(\frac{-q \cdot \psi(x)}{kT} \right) + \frac{q \cdot \psi(x)}{kT} - 1 \right) + \left(\frac{n_i}{N_a} \right)^2 \cdot \left(\exp\left(\frac{q \cdot \psi(x)}{kT} \right) - \frac{q \cdot \psi(x)}{kT} - 1 \right)} \tag{3-18}$$

When *x=0*, this relationship provides a way of relating the electric field at the SiC surface to the surface potential (see Figure 3-2):

$$\mathcal{E}_s = \frac{\sqrt{2} \cdot kT}{q \cdot L_D} \cdot \sqrt{\left(\exp\left(\frac{-q \cdot \psi_s}{kT} \right) + \frac{q \cdot \psi_s}{kT} - 1 \right) + \left(\frac{n_i}{N_a} \right)^2 \cdot \left(\exp\left(\frac{q \cdot \psi_s}{kT} \right) - \frac{q \cdot \psi_s}{kT} - 1 \right)} \tag{3-19}$$

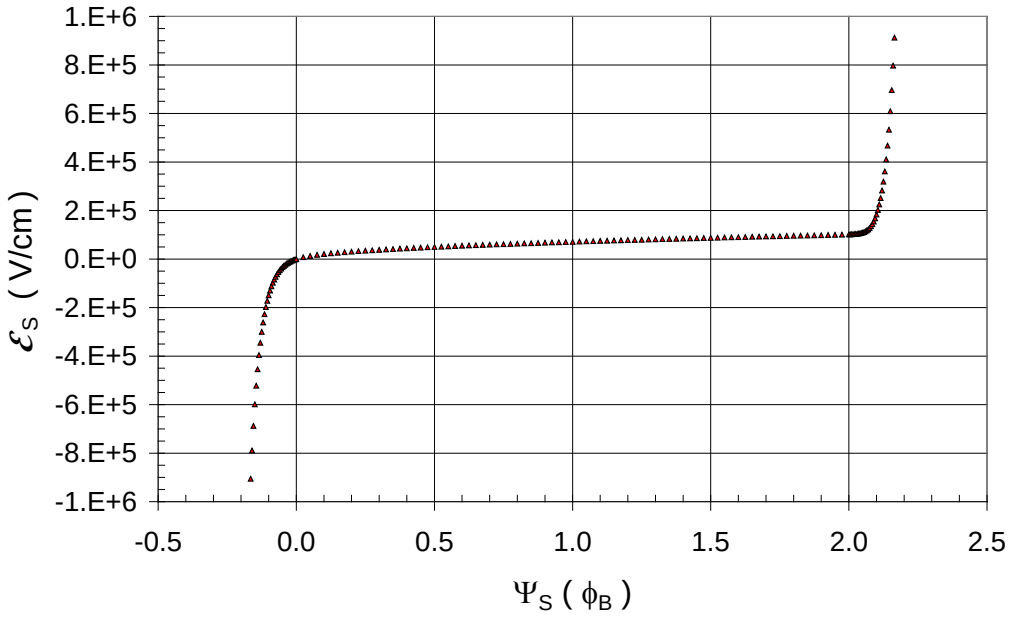

Figure 3-2: Surface electric field for the SiC as a function of the SiC surface potential, in units of the bulk potential, ϕ_B.

This in turn can be used to find the electric field at the gate oxide surface, using Gauss' Law, which can then be used to calculate the voltage drop across the oxide due to the inversion charge:

$$V_{OX} = \mathcal{E}_{OX} \cdot t_{OX} = \left[\frac{\varepsilon_{SiC}}{\varepsilon_{OX}} \cdot \mathcal{E}_{SiC} \right] \cdot t_{OX} = \frac{\left(\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC} \right)}{\left[\frac{\varepsilon_0 \cdot \varepsilon_{OX}}{t_{OX}} \right]} = \frac{-Q_s}{C_{OX}} \tag{3-20}$$

where ε_0, ε_{OX}, ε_{SiC} are the free-space, relative oxide, and relative SiC permittivities, respectively; $\mathcal{E}_{OX}$ is the electric field throughout the oxide and $\mathcal{E}_{SiC}$ is the electric field at the SiC surface; t_{OX} is the oxide thickness; C_{OX} is the oxide capacitance; and Q_s is the surface areal charge density for the semiconductor.

Therefore, the ideal case of (3-2), where there is no interfacial trapped charge, can be re-written using (3-9), (3-10), and (3-20):

$$V_{GS\_ideal} = V_{FB} + V_{OX} + V_{SiC} = \phi_{ms} + \frac{\left(\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_s \right)}{C_{OX}} + \psi_s \tag{3-21}$$

Thus, knowing the surface potential, both the voltage drop across the semiconductor, V_{SiC}, and that across the gate oxide, V_{OX}, can be calculated. However, the modifications to the oxide field (and voltage drop across the oxide) due to interfacial trapped charge, and the spatial distribution of inversion layer charge in the SiC, still need to be found.

3.4 Voltage shift due to interface traps

In the absence of any interfacial trapped charge, the field in the oxide is easily calculated from the surface field in the SiC using Gauss's Law, (3-20), as discussed in Section 3.3 above, once the surface potential is determined. However, in present state-of-

the-art SiC MOSFET devices, there exist significant numbers of interface traps and near-interfacial oxide traps which must be considered when calculating the field and voltage drop across the oxide.

As discussed above in Chapter 2, experimental evidence exists to suggest that not all interface traps exist right at the SiC-SiO_2 interface, but instead also extend into the SiC channel region [60, 61]. A more sophisticated model should take this into account, although that will not be considered here. Traps that extend into the gate oxide are not interface traps, but rather near-interfacial oxide traps. The calculations presented here assume that all interface traps exist exactly at the SiC-SiO_2 interface. In this case, the field in the oxide is modified by this interface trap charge, found by applying Gauss' Law

$$\mathcal{E}_{OX\_B} = \frac{\left(\varepsilon_0 \cdot \varepsilon_{OX} \cdot \mathcal{E}_{OX\_S} - Q_{IT}\right)}{\varepsilon_0 \cdot \varepsilon_{OX}} = \frac{\left(\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S} - Q_{IT}\right)}{\varepsilon_0 \cdot \varepsilon_{OX}} \tag{3-22}$$

where $\mathcal{E}_{OX\_B}$ is the electric field in the bulk of the oxide, $\mathcal{E}_{OX\_S}$ is the electric field at the surface of the oxide, and $\mathcal{E}_{SiC\_S}$ is explicitly the electric field at the surface of the SiC.

The voltage drop across the gate oxide is now modified by the presence of the interface-trap charge:

$$V_{OX\_net} = \mathcal{E}_{OX\_B} \cdot t_{OX} = \frac{\left(\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S} - Q_{IT}\right)}{\varepsilon_0 \cdot \varepsilon_{OX}} \cdot t_{OX} = \frac{-Q_s - Q_{IT}}{C_{OX}} \tag{3-23}$$

where Q_{IT} is surface charge density due to the interface trap charge, and is simply related to the net number of actively charged interface traps

$$N_{IT} = \left|\frac{Q_{IT}}{q}\right| \tag{3-24}$$

Q_{IT} and N_{IT} are calculated from the interface trap density, D_{IT}, as follows. First, mid-gap neutrality of interface traps is assumed, wherein traps below mid-gap are

assumed to be donor-like: positively charged when unoccupied and neutral when filled, and traps above mid-gap are assumed to be acceptor-like: neutral when unoccupied and negatively charged when filled.

For a given surface potential, which determines the energy level at the interface, the fraction of traps that are filled at any energy level, *E*, follow Fermi-Dirac statistics:

$$f_e(E) = \frac{1}{1+\exp\left\{\left(\frac{1}{kT}\right)\cdot\left[E-\left(\frac{E_{g\_SiC}}{2}+q\cdot(\psi_S-\phi_B)\right)\right]\right\}} \tag{3-25}$$

where E_{g_SiC} is the energy band gap of SiC. This relationship is true once equilibrium has been established between the interface traps and SiC substrate [20, 102, 104].

The interface trap density versus bandgap energy is assumed according to the following formulations [32]. On the low, or valence side of mid-gap

$$D_{IT\_v}(E) = D_{IT\_mid\_v} + D_{IT\_edge\_v}\cdot\exp\left\{\frac{-(E-E_{v\_SiC})}{\sigma_v}\right\} \tag{3-26}$$

where $D_{IT\_mid\_v}$ is the assumed interface trap density around mid-gap, $D_{IT\_edge\_v}$ is the assumed interface trap density at the valence band edge, σ_v is the assumed exponential decay factor of the band-edge traps, and E_{v_SiC} is the energy of the valence band edge.

Similarly, on the high, or conductance side of mid-gap

$$D_{IT\_c}(E) = D_{IT\_mid\_c} + D_{IT\_edge\_c}\cdot\exp\left\{\frac{-(E_{c\_SiC}-E)}{\sigma_c}\right\} \tag{3-27}$$

where $D_{IT\_mid\_c}$ is the assumed interface trap density around mid-gap, $D_{IT\_edge\_c}$ is the assumed interface trap density at the conductance band edge, σ_c is the assumed exponential decay factor of the band-edge traps, and E_{c_SiC} is the energy of the conductance band edge. Typical values are given in Table 3-1. A graph of the interface

trap density as defined in (3-26) and (3-27), covering the entire bandgap, is shown in Figure 3-3.

Table 3-1: Typical values used for the parameters of (3-26) and (3-27).

$D_{IT\_mid\_v}$	6.0×10^{13}	($cm^{-2}\cdot eV^{-1}$)
$D_{IT\_edge\_v}$	2.3×10^{13}	($cm^{-2}\cdot eV^{-1}$)
σ_v	0.061	

$D_{IT\_mid\_c}$	6.0×10^{13}	($cm^{-2}\cdot eV^{-1}$)
$D_{IT\_edge\_c}$	2.3×10^{13}	($cm^{-2}\cdot eV^{-1}$)
σ_c	0.061	

Therefore, the total interface trap charge for a given surface potential can be calculated by integrating over the entire bandgap, keeping in mind that for traps below mid-gap, it is the number of unoccupied states that is important.

$$Q_{IT} = q\cdot\int_{E_{v\_SiC}}^{E_{mg\_SiC}} D_{IT}(E)\cdot\left[1-f_e(E)\right]dE - q\cdot\int_{E_{mg\_SiC}}^{E_{c\_SiC}} D_{IT}(E)\cdot f_e(E)dE \tag{3-28}$$

A graph of this result, again using the values in Table 3-1, is shown in Figure 3-4. If this charge were the only contribution to the interfacial charge, it could be written as

$$V_{IT} = V_{\text{int}} = -\frac{Q_{IT}}{C_{OX}} \tag{3-29}$$

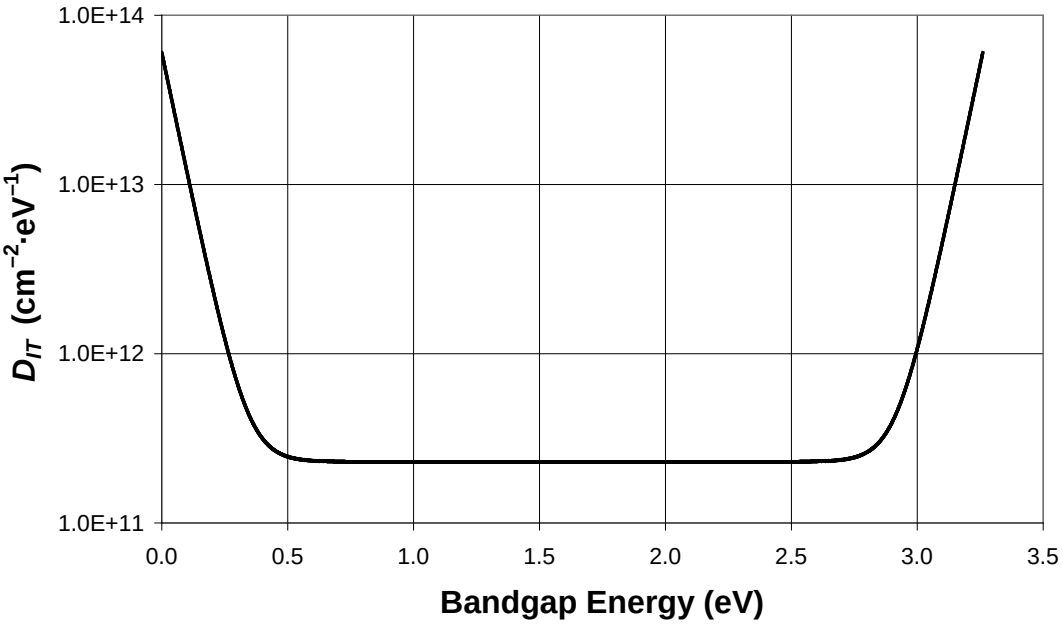

Figure 3-3: Interface trap density versus bandgap energy, calculated using (3-26), (3-27), and Table 3-1.

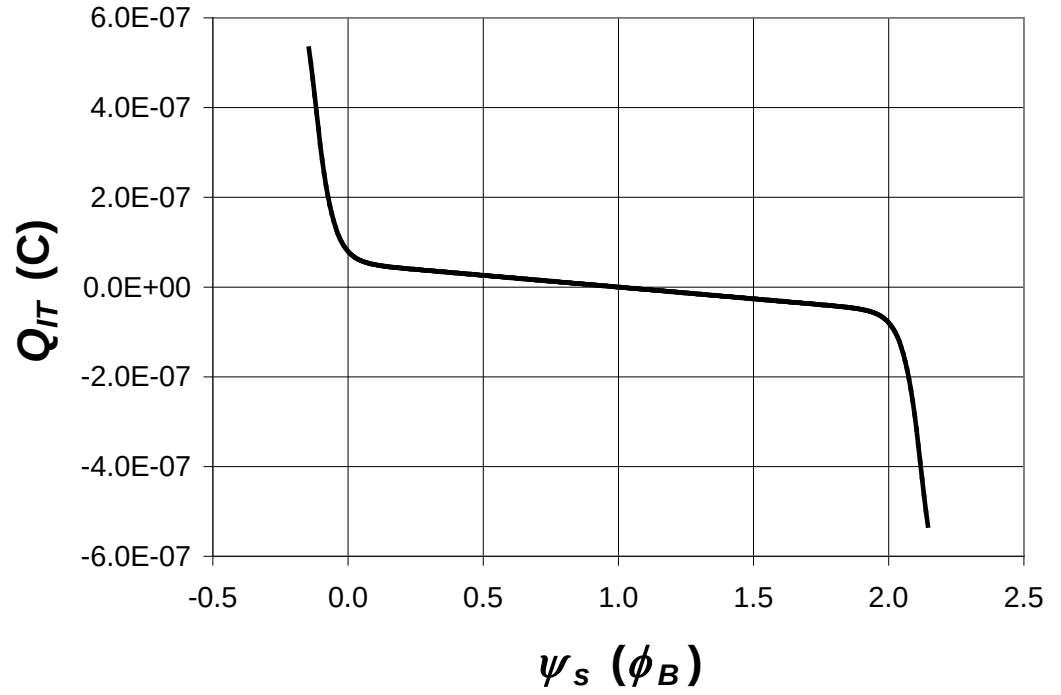

Figure 3-4: Variation of interface trap charge with surface potential, plotted in units of the bulk potential.

The effect of interface traps is to simply change the uniform field across the gate oxide, although that charge is a function of the surface potential and there is a response time associated with filling and emptying the interface traps, which is a function of the SiC carrier concentration at the surface as well as the distance in energy from the bandgap edges [20, 102].

Although fixed charge will not be considered, since experimental evidence suggests it may not be significant (see Chapter 5), the effect of any such charge would be to simply change the uniform field across the gate oxide by an additional factor since fixed charge is generally believed to be located at the oxide interface [31].

$$V_{OX\_net} = \mathcal{E}_{OX\_B} \cdot t_{OX} = \frac{\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S} - (Q_{IT} + Q_F)}{\varepsilon_0 \cdot \varepsilon_{OX}} \cdot t_{OX} = \frac{-Q_s - (Q_{IT} + Q_F)}{C_{OX}} \quad (3\text{-}30)$$

In terms of (3-1), this modified voltage drop across the oxide is the sum of that due only to charge in the semiconductor, V_{OX}, and that due to the sum of the net interfacial charge, V_{int}:

$$V_{OX\_net} = -\frac{Q_s}{C_{OX}} - \frac{Q_{IT} + Q_F}{C_{OX}} = V_{OX} + V_{\text{int}} = V_{OX} + V_{IT} + V_F \quad (3\text{-}31)$$

where V_F is the voltage shift due to fixed charge.

3.5 Voltage shift due to oxide traps, calculation of the oxide trap charge centroid, and its effect on the oxide field

The oxide traps in the gate oxide are the only other type of interfacial trap to be considered. If all the charge in the oxide was right at the semiconductor interface as well,

then the same simple expression could be used to describe the voltage shift due to this type of charge:

$$V_{OT} = -\frac{Q_{OT}}{C_{OX}} = -\frac{Q_{OT}}{\varepsilon_{OX}} \cdot t_{OX} \tag{3-32}$$

where Q_{OT} is the total oxide trap charge per unit area.

This expression is reasonably accurate for thick oxides, or where the charge does not penetrate very deeply into the oxide. But a more accurate analysis requires calculating the charge centroid, which in the case of switching oxide traps will be dependent on the time and bias history of the device. (Since mobile ions are likely not an issue in these devices—although devices with Al gates may be and those exposed to the MEO process definitely are [73, 74]—this type of charge will not be considered here. However, if it was, a similar type of calculation would have to be done since mobile ions are also spread across the oxide.) The expression for the voltage shift is modified as follows

$$V_{OT}(t) = \frac{-Q_{OT}(t)}{\varepsilon_{OX}} \cdot \overline{d_{OX}}(t) = \frac{-Q_{OT}(t)}{C_{OX}} \cdot \left[\frac{\overline{d_{OX}}(t)}{t_{OX}}\right] = \frac{-Q_{OT}(t)}{C_{OX}} \cdot f_{cent.} \tag{3-33}$$

where $\overline{d_{OX}}$ is the centroid of this charge, similar in concept to the center of mass when calculating moments, and $f_{cent.}$ is the charge centroid factor.

If the oxide charge is described by a volumetric oxide trap density, n_{OT}, as follows

$$Q_{OT}(t) = \int_{x_1}^{x_2} q \cdot n_{OT}(x,t)dx \tag{3-34}$$

where $0 \le x_1 < x_2 \le t_{OX}$, then the charge centroid can be calculated using the following expression, which is the integral summation of each bit of charge at each position in the oxide divided by the total charge, Q_{OT}, in the oxide:

$$\overline{d_{OX}}(t) = \frac{\int_{x_1}^{x_2} x \cdot q \cdot n_{OT}(x,t)dx}{\int_{x_1}^{x_2} q \cdot n_{OT}(x,t)dx} = \frac{\int_{x_1}^{x_2} x \cdot q \cdot n_{OT}(x,t)dx}{Q_{OT}(t)} \tag{3-35}$$

Therefore, the shift in voltage can be written as

$$V_{OT}(t) = \frac{-Q_{OT}(t)}{\varepsilon_{OX}} \cdot \overline{d_{OX}}(t) = -\frac{q}{\varepsilon_{OX}} \cdot \int_{x_1}^{x_2} x \cdot n_{OT}(x,t)dx \tag{3-36}$$

For a linearly varying charge distribution versus position in the oxide,

$$n_{OT} = \frac{(n_{\max} - n_{\min})}{(x_2 - x_1)} \cdot (x - x_1) + n_{\min} \tag{3-37}$$

where n_{max} and n_{min} are both charge per volume (see Figure 3-5), the charge centroid due to this charge would be

$$\overline{d_{OX}} = \frac{\int_{x_1}^{x_2} x \cdot q \cdot \left[\frac{(n_{\max} - n_{\min})}{(x_2 - x_1)} \cdot (x - x_1) + n_{\min} \right] dx}{\int_{x_1}^{x_2} q \cdot \left[\frac{(n_{\max} - n_{\min})}{(x_2 - x_1)} \cdot (x - x_1) + n_{\min} \right] dx} \tag{3-38}$$

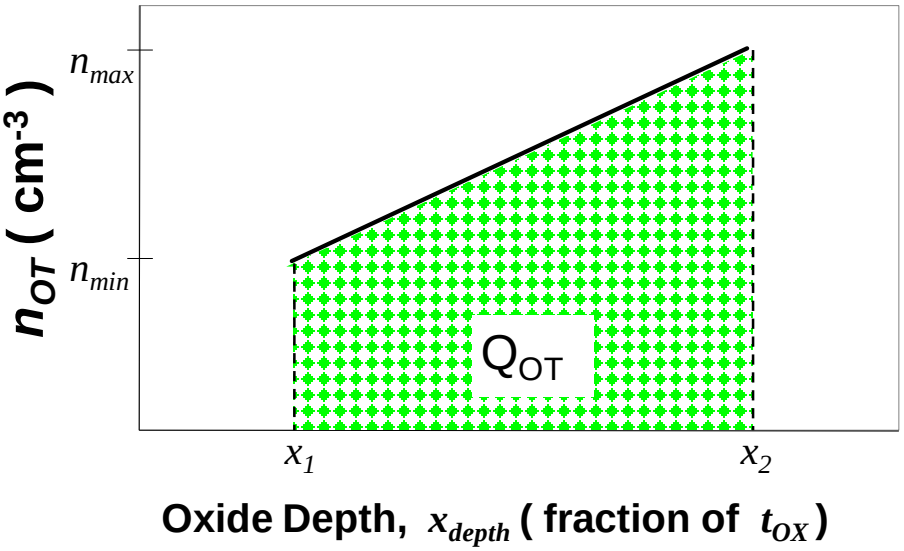

Figure 3-5: Schematic of a general charge distribution in the gate oxide.

A useful, simplified result is when a uniform distribution extends only a certain depth into the oxide (see Figure 3-6). The depth to which the distribution extends can be defined as

$$t_{OT} = t_{OX} - f_{OT} \cdot t_{OX} = (1 - f_{OT}) \cdot t_{OX} \tag{3-39}$$

where $0 \le f_{OT} < 1$, so that $t_{OT} = 0$ when $f_{OT} = 1$. The charge centroid can be readily calculated, using (3-35):

$$\overline{d_{OX}} = \frac{\int_{f_{OT} \cdot t_{OX}}^{t_{OX}} x \cdot (q \cdot n_{const}) dx}{\int_{f_{OT} \cdot t_{OX}}^{t_{OX}} (q \cdot n_{const}) dx} = \frac{(q \cdot n_{const}) \cdot (\frac{t_{OX}^2}{2} - f_{OT}^{\ 2} \cdot \frac{t_{OX}^2}{2})}{(q \cdot n_{const}) \cdot (t_{OX} - f_{OT} \cdot t_{OX})} = \frac{(1 + f_{OT})}{2} \cdot t_{OX} \tag{3-40}$$

which would result in the following voltage shift

$$V_{OT} = -\frac{Q_{OT}}{\varepsilon_{OX}} \cdot \overline{d_{OX}} = -\frac{Q_{OT}}{C_{OX}} \cdot \frac{(1 + f_{OT})}{2} = -\frac{Q_{OT} \cdot f_{cent.}}{C_{OX}} \tag{3-41}$$

where the charge centroid factor for this case is

$$f_{cent.} = \frac{\overline{d_{OX}}}{t_{OX}} = \frac{(1 + f_{OT})}{2} \tag{3-42}$$

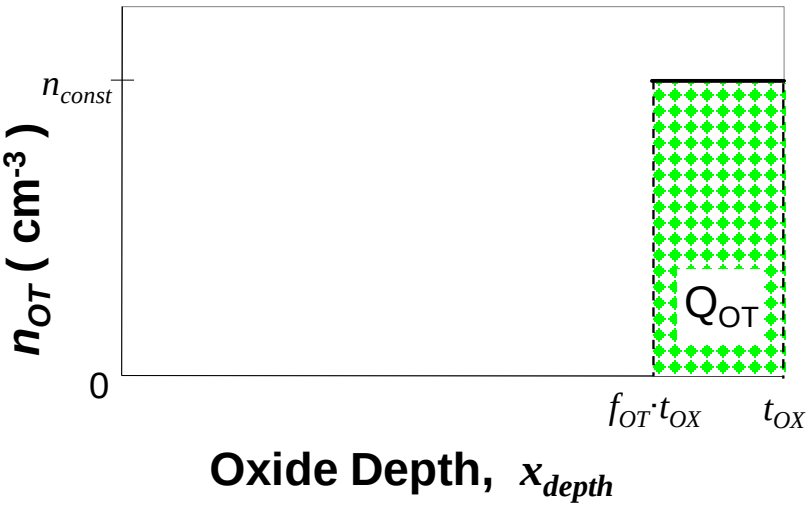

Figure 3-6: Schematic of a rectangular charge distribution in the gate oxide near the SiC interface.

For example, if the charge distribution extends to a depth that is eight percent of the total oxide thickness such that t_{OT} is $0.08 \cdot t_{OX}$ and $f_{OT} = 0.92$, then

$$\overline{d_{OX}} = f_{cent.} \cdot t_{OX} = \frac{(1 + f_{OT})}{2} \cdot t_{OX} = \frac{(1 + 0.92)}{2} \cdot t_{OX} = 0.96 \cdot t_{OX} \tag{3-43}$$

and

$$V_{OT} = -\frac{Q_{OT}}{C_{OX}} \cdot \frac{\overline{d_{OX}}}{t_{OX}} = -\frac{Q_{OT} \cdot f_{cent.}}{C_{OX}} = -\frac{Q_{OT} \cdot (0.96)}{C_{OX}} \tag{3-44}$$

This would be the case for a uniform charge distribution that extended 40 Å into a 500-Å thick gate oxide, which results in a four percent correction in the magnitude of the voltage shift. For example, if the oxide trap density was 1×10^{12} cm^{-2}, then the resulting voltage shift would actually be

$$\begin{aligned} V_{OT} &= -\frac{Q_{OT} \cdot (0.96)}{C_{OX}} = -\frac{Q_{OX}}{\varepsilon_{OX}} \cdot (0.96 \cdot t_{OX}) \\ &= -\frac{1.6 \times 10^{-19}(\text{C}) \cdot 1 \times 10^{12}\ (\text{cm}^{-2})}{3.9 \cdot 8.85 \times 10^{-14}\ (\text{F/cm})} \cdot (0.96 \cdot 500 \times 10^{-8}\ \text{cm}) = -2.224\ \text{V} \end{aligned} \tag{3-45}$$

instead of the –2.317 V that would be calculated if the effects of the spatial distribution of the charge were ignored. This difference is small, and not very important in itself, especially when considering the measurement uncertainty from experimental results. However, the electric field does change significantly within the oxide trap region, and that is important in accurately modeling the tunneling effect, which is discussed in Chapter 6.

Therefore, modifying (3-31) to include the term for oxide trap charge yields:

$$V_{OX\_net} = V_{OX} + V_{\text{int}} = -\frac{Q_s}{C_{OX}} - \frac{Q_{IT} + Q_F + Q_{OT} \cdot f_{cent.}}{C_{OX}} \tag{3-46}$$

Although mobile ions are not considered here, a full description of all the possible charge components, discussed in Chapter 2, affecting the voltage drop across the oxide would be

$$V_{OX\_net} = V_{OX} + V_{\text{int}} = \frac{-Q_s}{C_{OX}} + \frac{-\left(Q_{IT} + Q_F + Q_{OT} \cdot f_{cent.} + Q_M \cdot f_M\right)}{C_{OX}} \tag{3-47}$$

where Q_M is the mobile ion charge, and f_M is its charge centroid.

The modification of the voltage drop across the gate oxide due to a rectangular distribution of oxide trap charge near the interface, given by (3-41), and its resultant effect on the electric field within the gate oxide, can be better understood by way of a graphical example.

Without any interfacial charge, including oxide trap charge, the field in the bulk of the oxide is equivalent to the field at the interface, found from the electric field in the SiC at the interface using Gauss' Law (3-20):

$$\mathcal{E}_{OX\_B} = \mathcal{E}_{OX\_S} = \left(\frac{\varepsilon_{SiC}}{\varepsilon_{OX}}\right) \cdot \mathcal{E}_{SiC\_S} \tag{3-48}$$

and the voltage drop is simply the hatched area shown in Figure 3-7.

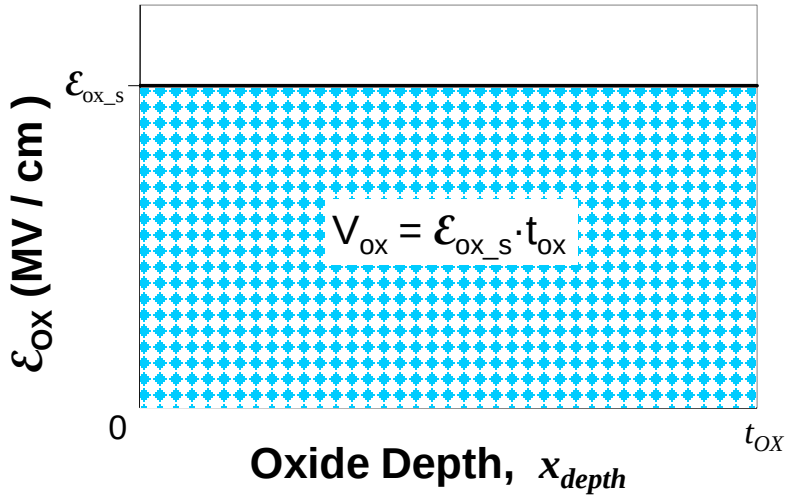

Figure 3-7: Voltage drop across the oxide due to Q_S.

With the presence of a rectangular distribution of interfacial oxide charge, Q_{OT}, as in Figure 3-6, Gauss' Law is modified ala (3-22), giving a modified electric field in the bulk of the oxide:

$$\mathcal{E}_{OX\_B} = \mathcal{E}_{OX\_S} - \frac{Q_{OT}}{\varepsilon_0 \cdot \varepsilon_{OX}} = \frac{\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S} - Q_{OT}}{\varepsilon_0 \cdot \varepsilon_{OX}} \tag{3-49}$$

which can be rewritten as

$$\mathcal{E}_{OX\_S} - \mathcal{E}_{OX\_B} = \frac{Q_{OT}}{\varepsilon_0 \cdot \varepsilon_{OX}} \tag{3-50}$$

The modified voltage drop across the oxide can be readily found graphically, as depicted in Figure 3-8:

$$\begin{aligned} V_{OX\_net} &= V_{OX} + V_{\text{int}} \\ &= V_{OX\_b} + V_{OX\_s} = \mathcal{E}_{OX\_B} \cdot t_{OX} + \left(\mathcal{E}_{OX\_S} - \mathcal{E}_{OX\_B}\right) \cdot \frac{(1 - f_{OT})}{2} \cdot t_{OX} \end{aligned} \tag{3-51}$$

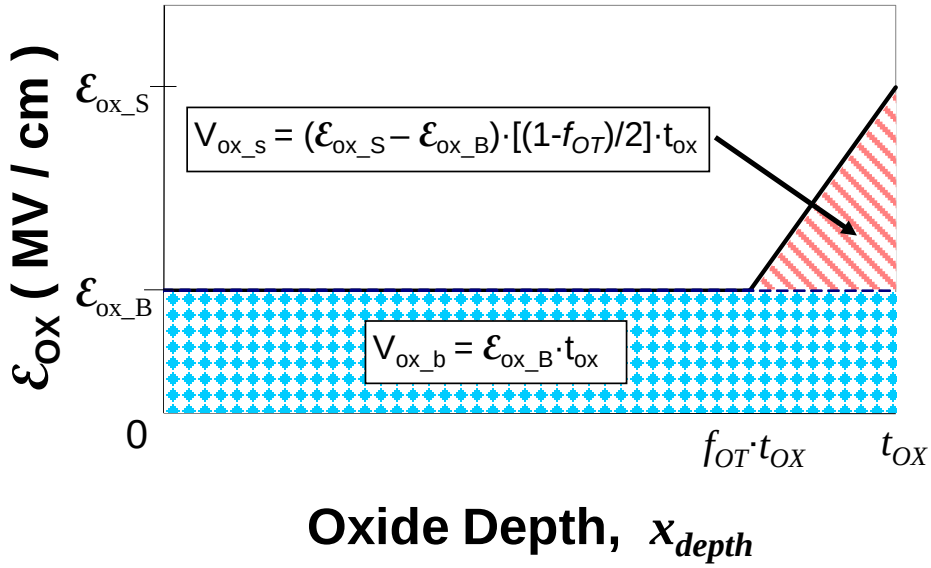

Figure 3-8: Voltage drop across the oxide is modified by a rectangular oxide trap distribution as in Figure 3-6, which changes the bulk field.

This result can also be readily found by calculating the changing oxide field in the interfacial region due to the rectangular charge distribution.

$$\mathcal{E}(x) = \mathcal{E}_{OX\_B} + \int_{f_{OT}\cdot t_{OX}}^{t_{OX}} \frac{q}{\varepsilon}\cdot n_{OT}(x)dx = \mathcal{E}_{OX\_B} + \frac{q}{\varepsilon}\cdot n_{const}\cdot(x - f_{OT}\cdot t_{OX}) \qquad (3\text{-}52)$$

The change in the voltage drop across the oxide due to the presence of this positive trapped charge is the total oxide trap charge times the charge centroid factor. This can be found using (3-47), (3-50), and (3-43) derived above.

$$\begin{aligned} V_{OT} &= V_{\text{int}} = V_{OX\_net} - V_{OX} \\ &= (V_{OX\_b} + V_{OX\_s}) - V_{OX} \\ &= \left\{ \mathcal{E}_{OX\_B}\cdot t_{OX} + \left(\mathcal{E}_{OX\_S} - \mathcal{E}_{OX\_B}\right)\cdot\frac{(1-f_{OT})}{2}\cdot t_{OX} \right\} - \mathcal{E}_{OX\_S}\cdot t_{OX} \\ &= \left(\mathcal{E}_{OX\_S} - \mathcal{E}_{OX\_B}\right)\cdot\left(\frac{(1-f_{OT})}{2} - 1\right)\cdot t_{OX} \\ &= -\left(\mathcal{E}_{OX\_S} - \mathcal{E}_{OX\_B}\right)\cdot\frac{(1+f_{OT})}{2}\cdot t_{OX} = -\left(\frac{Q_{OT}}{\varepsilon_0\cdot\varepsilon_{OX}}\right)\cdot f_{cent.}\cdot t_{OX} \\ &= -\frac{Q_{OT}\cdot f_{cent.}}{C_{OX}} \end{aligned} \qquad (3\text{-}53)$$

This result can also be determined graphically, as shown below in Figure 3-9.

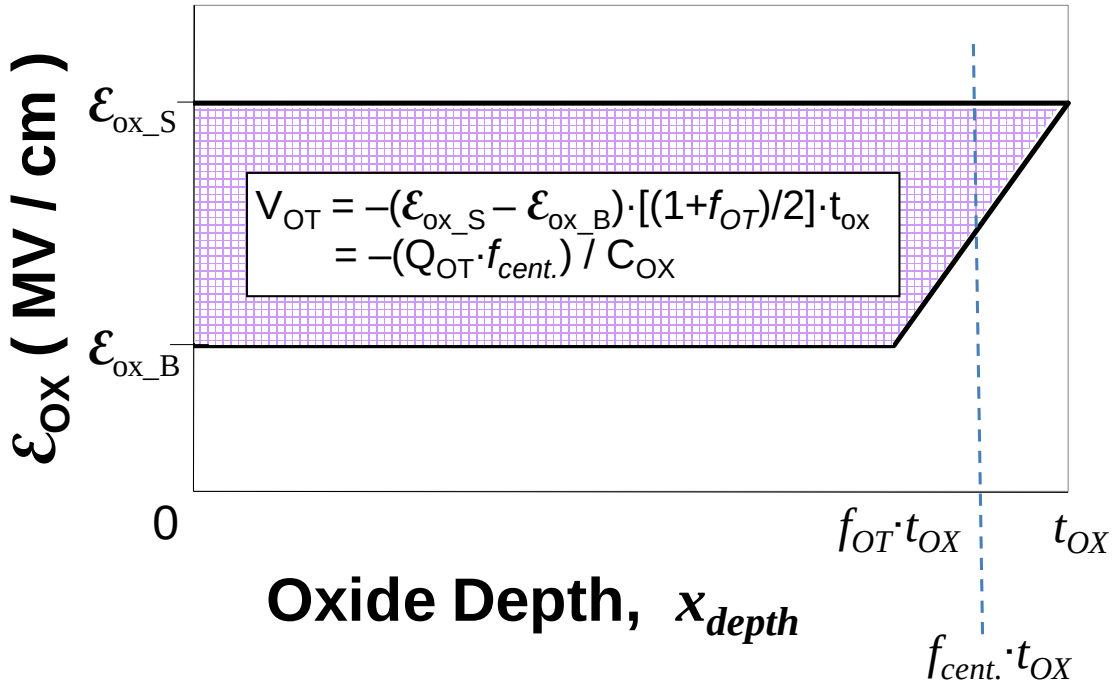

Figure 3-9: The voltage drop across the oxide is modified by the hatched area due to the presence of the rectangular distribution of oxide traps near the interface as depicted in Figure 3-6.

3.6 Effect of interfacial charge on threshold voltage and the gate oxide field

The net interfacial charge described by (3-47) can be normalized as if all the charge was at the interface:

$$V_{\text{int}} = \frac{-Q_{net}\cdot f_{net}}{C_{OX}} = \frac{-\left(Q_{IT} + Q_F + Q_{OT}\cdot f_{cent.} + Q_M\cdot f_M\right)}{C_{OX}} \tag{3-54}$$

Then (3-1) can be re-written, using (3-21), as:

$$V_{GS} = V_{FB} + V_{OX} + V_{\text{int}} + V_{SiC} = \phi_{ms} + \frac{\left(\varepsilon_0\cdot\varepsilon_{SiC}\cdot\mathcal{E}_{SiC\_S}\right)}{C_{OX}} - \frac{Q_{net}\cdot f_{net}}{C_{OX}} + \psi_s \tag{3-55}$$

Thus the threshold voltage can be found from (3-55), by setting the surface potential to two times the bulk potential, keeping in mind the proper occupancy of the interface traps:

$$V_T = V_{GS}(\psi_s = 2 \cdot \phi_B) = \phi_{ms} + \frac{\left(\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S}\right)}{C_{OX}} - \frac{Q_{net} \cdot f_{net}}{C_{OX}} + 2 \cdot \phi_B \qquad (3\text{-}56)$$

The difference between the measured and ideal threshold voltage is due to the shifts caused by the interfacial charge:

$$V_T - V_{T\_ideal} = -\frac{Q_{net} \cdot f_{net}}{C_{OX}} = V_{\text{int}} = V_{IT} + V_F + V_{OT} + V_M \qquad (3\text{-}57)$$

where V_M is the voltage shift due to mobile ions in the gate oxide.

Figure 3-10 shows the effect of trapped charge on the relationship between the applied gate-to-source voltage and the SiC surface potential. For the ideal case without trapped charge, circles indicate the applied gate voltage required to place the device in accumulation, flat-band, mid-gap, inversion, and strong inversion (where the surface potential is -0.1, 0.0, 1.0, 2.0, and 2.1 times the SiC bulk potential, ϕ_B, respectively). The addition of 1×10^{12} cm^{-2} trapped positive oxide charge, as discussed in the previous section, results in a negative shift versus V_{GS} of 2.224 V.

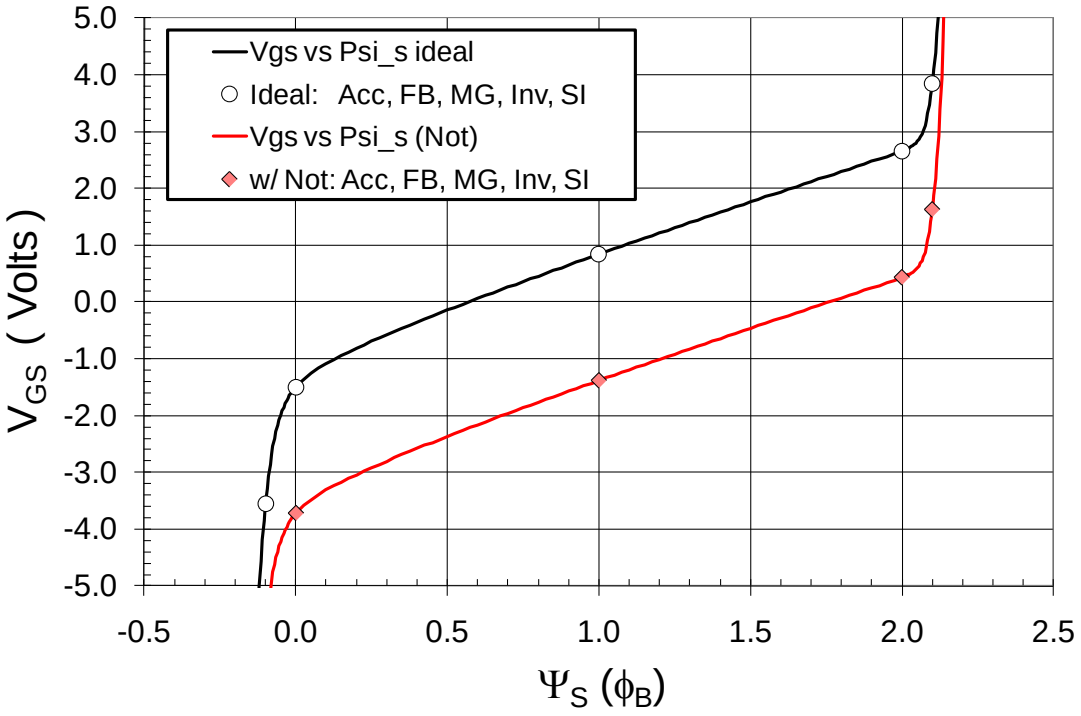

Figure 3-10: Variation in required applied gate-to-source voltage to effect a particular surface potential in a SiC MOSFET (N_a=1×10^{16} cm^{-3}, t_{ox} = 500 Å) for both an ideal device with no trapped charge and one with an oxide trapped charge density of +1×10^{12} cm^{-2}.

The relationship between the oxide field and the gate-to-source voltage, without any trapped charge present, is as follows:

$$\mathcal{E}_{OX} = \frac{V_{OX}}{t_{OX}} = \frac{\left(V_{GS\_ideal} - V_{FB} - V_{SiC}\right)}{t_{OX}} = \frac{\left(V_{GS\_ideal} - \phi_{ms} - \psi_s\right)}{t_{OX}}. \tag{3-58}$$

This result is plotted in Figure 3-11, along with a simpler rule-of-thumb calculation:

$$\mathcal{E}_{OX} = \frac{V_{OX}}{t_{OX}} \approx \frac{V_{GS}}{t_{OX}} \tag{3-59}$$

For a negative value of V_{GS}, where the device is in accumulation, the magnitude of the oxide field is overestimated by V_{FB} / t_{OX}. For the case of positive V_{GS}, where the

device is in strong inversion, the magnitude of the oxide field is overestimated by (V_{FB} + 2×ϕ_B) / t_{OX}. Since ϕ_{ms} ~ -ϕ_B, the approximate values err almost equally for both positive and negative oxide fields.

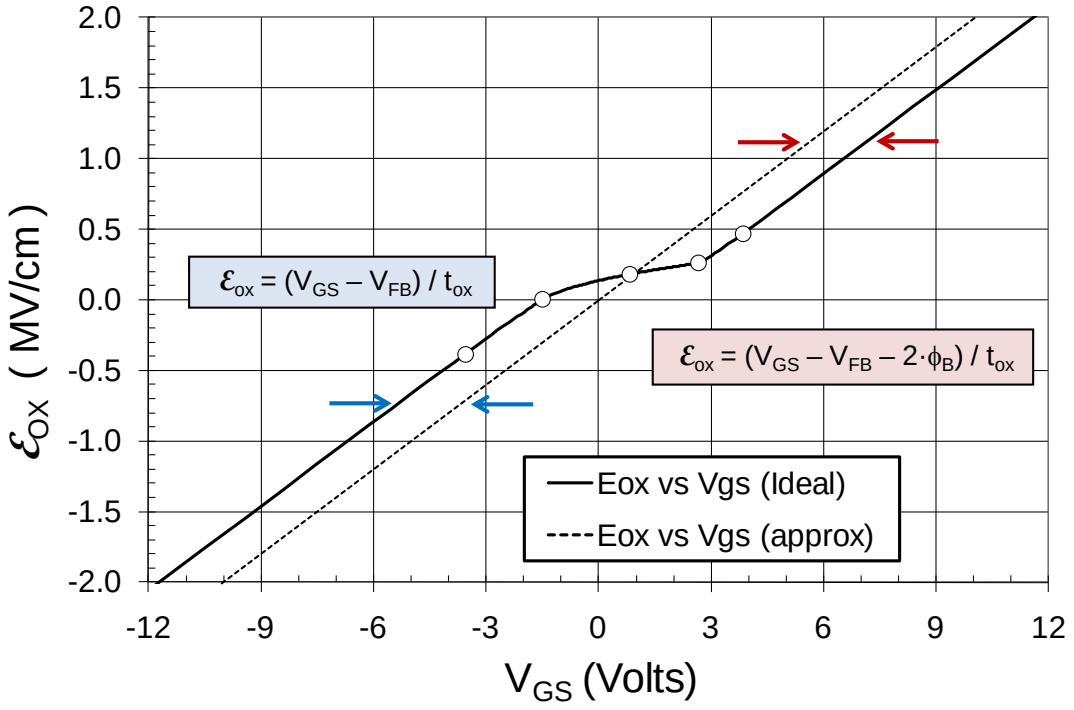

Figure 3-11: Comparison of the ideal relationship between V_{GS} and gate oxide field, without interfacial charge present, and a simpler rule-of-thumb calculation.

For the example given above, where a device has an oxide trap density of 1×10^{12} cm^{-2} with a uniform charge distribution that extends 40 Å into a 500-Å thick gate oxide, the oxide field at the surface and in the bulk, calculated from (3-20) and (3-49), are compared to the ideal value, as seen in Figure 3-12.

A similar negative shift of V_{GS} is seen when plotting the oxide surface field versus applied gate voltage. The curve when trapped charge is present (top, red line with diamonds) is translated 2.224 V to the left of the ideal curve (middle, black line with circles). This figure also shows a comparison of the required applied gate voltage, when

charge in the oxide is present, between the surface oxide field (top, red line with diamonds) and the bulk oxide field (bottom, blue line with squares)—the two are the same when no charge is present in the oxide. For the same applied gate voltage, the two fields always vary by the same amount. Using our example from above, $\mathcal{E}_{OX\_S} - \mathcal{E}_{OX\_B} =$ 0.463 MV/cm.

Whereas the surface fields at the same applied gate voltage are never the same for different amounts of oxide trap charge, the bulk oxide fields in either accumulation or strong inversion are very similar. This in turn has important implications for various testing scenarios, where the oxide is charging during the measurement. It implies that for an oxide reliability test where the bulk oxide field is most important, such as for a TDDB test, charging may not be as important, but for threshold-voltage instability, which appears to be driven by charge tunneling into and out of near-interfacial oxide traps, it is the field in the trapped oxide-charge region which is most important—and that varies greatly with trapped charge.

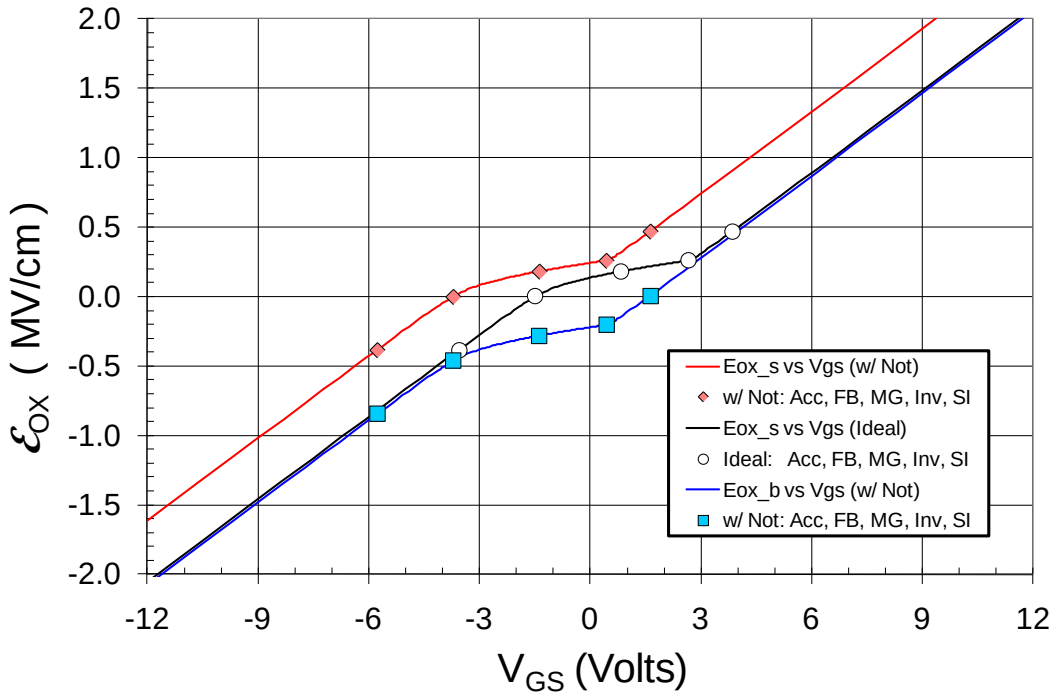

Figure 3-12: Variation in required applied gate-to-source voltage to effect a particular oxide field in a SiC MOSFET (N_a=1×10^{16} cm^{-3}, t_{ox} = 500 Å) for both an ideal device with no trapped charge, where the surface and bulk fields are the same; and one with an oxide trapped charge density of +1×10^{12} cm^{-2}, where the surface and bulk fields are different.

3.7 Numerical simulation of electric potential in the SiC channel region

Now that the effect of interfacial charge has been considered, the gate oxide can be calculated—by first calculating the electric potential. The calculation of the potential can be broken up into two parts: (1) calculation in the SiC—described in this section; and (2) calculation in the gate oxide—described in the next section.

This can be done since the electric potential is known at the boundary points: deep in the bulk of the SiC, at the SiO_2 interface, and at the gate:

$$\phi_{subst} = \psi(x = bulk) - \phi_B = -\phi_B \tag{3-60}$$

$$\phi_{\text{int}} = \psi(x = 0) - \phi_B = \psi_s - \phi_B \tag{3-61}$$

$$\phi_{gate} = \psi(x = gate) - \phi_B = (V_{OX} + V_{\text{int}}) + \psi_s - \phi_B \tag{3-62}$$

These act as boundary conditions for the numerical simulations.

The potential, electric field, charge carrier concentrations, and other variables can be modeled either analytically using the depletion approximation, or numerically using a finite difference code that solves Poisson's Equation. Before employing numerical simulation techniques to determine the exact electric potential and carrier concentrations within the semiconductor, a standard analytical approach was used to obtain an approximate solution to provide a proper starting point for the exact solution.

In order to readily calculate the band-bending—and therefore the electric potential and carrier concentrations—as a function of position within the semiconductor, the depletion approximation can be used wherein the ionized acceptor ions are assumed to be the only source of charge. Poisson's Equation (3-15) is now written as

$$\frac{\partial^2 \psi(x)}{\partial x^2} = -\frac{\rho(x)}{\varepsilon_s} = -\frac{q}{\varepsilon_s} \cdot \left[- N_a^- \right] = \frac{q \cdot N_a^-}{\varepsilon_s} \tag{3-63}$$

Integrating (3-63) twice yields an expression for the spatial variation in the band-bending potential, in terms of the surface potential and surface electric field, which can also be written in terms of the maximum depletion width, W_D—beyond which the field is assumed to be zero.

$$\psi(x) = \frac{q \cdot N_a^-}{\varepsilon_s} \cdot \frac{x^2}{2} - \mathcal{E}_s \cdot x + \psi_s = \frac{q \cdot N_a^-}{\varepsilon_s} \cdot \frac{(x - W_D)^2}{2} \tag{3-64}$$

The depletion approximation also yields a simpler relationship between the surface electric field and the band-bending at the surface over the range of flatband to inversion, which can also be re-written in terms of the maximum depletion width:

$$\mathcal{E}_s = \sqrt{\frac{2 \cdot q \cdot N_a \cdot \psi_s}{\varepsilon_s}} = \frac{q \cdot N_a}{\varepsilon_s} \cdot W_D \tag{3-65}$$

This then gives the electric potential and bending of the energy bands as a function of position in the semiconductor using (3-6), which can be used as a good approximation and starting point for an exact solution using numerical methods, to be discussed next.

The spatial variation in electric potential for various surface potentials is shown in Figure 3-13.

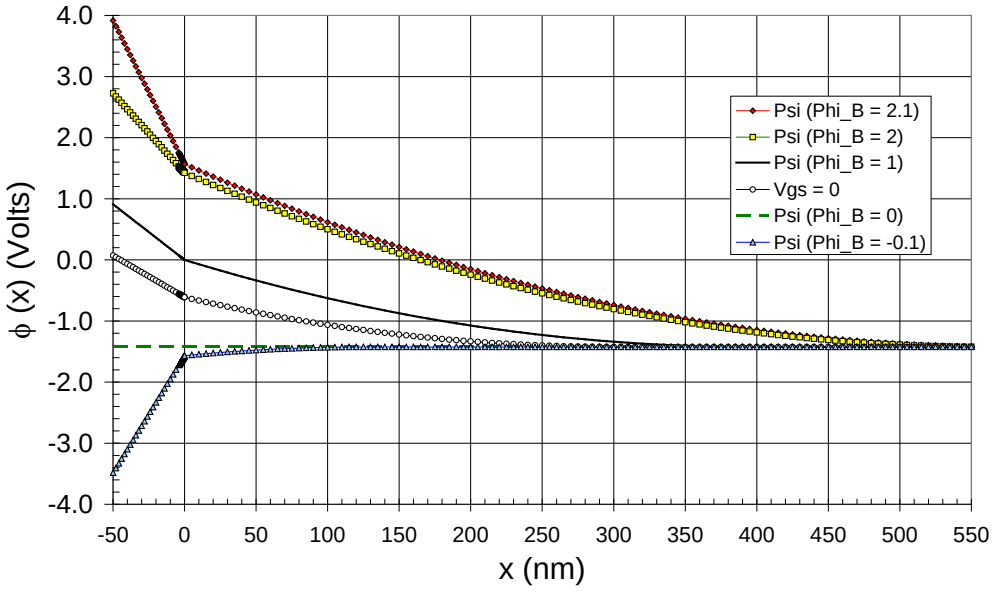

Figure 3-13: Spatial variation of electric potential in both gate oxide and SiC, as a function of surface potential for the following conditions: accumulation ($\psi_s = -0.1 \cdot \phi_B$), flat-band ($\psi_s = 0$), zero potential ($V_{GS} = 0$; $\psi_s = 0.57 \cdot \phi_B$), mid-gap ($\psi_s = \phi_B$), inversion ($\psi_s = 2 \cdot \phi_B$), and strong inversion ($\psi_s = 2.1 \cdot \phi_B$); for $N_a = 1 \times 10^{16}$ and t_{ox} =50 nm.

In a similar manner, the spatial variation in electron carrier concentration can be found using either (3-7) or (3-13)

The numerical simulation of the electric potential in the SiC is performed using standard techniques, as follows. First, a Taylor Series expansion is performed for an incremental change in the electric potential:

$$\phi(x+\Delta x)=\phi(x)+\frac{\partial\phi(x)}{\partial x}\cdot\Delta x+\frac{1}{2}\cdot\frac{\partial^2\phi(x)}{\partial x^2}\cdot(\Delta x)^2+O\cdot(\Delta x)^3 \tag{3-66}$$

where Δx is a small spatial increment and $O(\ )$ represents higher order terms. A similar series expansion can be calculated for an incremental decrease in the electric potential.

$$\phi(x-\Delta x)=\phi(x)-\frac{\partial\phi(x)}{\partial x}\cdot\Delta x+\frac{1}{2}\cdot\frac{\partial^2\phi(x)}{\partial x^2}\cdot(\Delta x)^2-O\cdot(\Delta x)^3 \tag{3-67}$$

Adding (3-66) and (3-67) gives

$$\phi(x+\Delta x)+\phi(x-\Delta x)=2\cdot\phi(x)+\frac{\partial^2\phi(x)}{\partial x^2}\cdot(\Delta x)^2 \tag{3-68}$$

which can be re-written as

$$\frac{\partial^2\phi(x)}{\partial x^2}=\frac{\phi(x+\Delta x)-2\cdot\phi(x)+\phi(x-\Delta x)}{(\Delta x)^2} \tag{3-69}$$

Thus a discretized version of Poisson's Equation (3-15) is

$$\begin{aligned}\frac{\partial^2\phi}{\partial x^2}\Big|_i&=\frac{\phi_{i-1}-2\cdot\phi_i+\phi_{i+1}}{(\Delta x)^2}\\&=-\frac{q}{\varepsilon_s}\cdot\left[n_i\cdot\exp\left(\frac{-q\cdot\phi_i}{kT}\right)-n_i\cdot\exp\left(\frac{q\cdot\phi_i}{kT}\right)+D_i\right]\end{aligned} \tag{3-70}$$

where D is the doping in the channel. For the p-type substrate,

$$D=-N_a \tag{3-71}$$

By defining a function, f, as the difference of the two sides of (3-70),

$$f_i(\phi_{i-1},\phi_i,\phi_{i+1}) = \frac{\phi_{i-1} - 2\cdot\phi_i + \phi_{i+1}}{(\Delta x)^2} + \frac{q}{\varepsilon_s}\cdot\left[n_i \cdot \exp\left(\frac{-q\cdot\phi_i}{kT}\right) - n_i \cdot \exp\left(\frac{q\cdot\phi_i}{kT}\right) + D_i \right] \tag{3-72}$$

and calculating the derivative in terms of ϕ,

$$\frac{\partial f_i(\phi_{i-1},\phi_i,\phi_{i+1})}{\partial\phi_{i-1}} = \frac{\partial f_i(\phi_{i-1},\phi_i,\phi_{i+1})}{\partial\phi_{i+1}} = \frac{1}{(\Delta x)^2} \tag{3-73}$$

$$\frac{\partial f_i(\phi_{i-1},\phi_i,\phi_{i+1})}{\partial\phi_i} = \frac{-2}{(\Delta x)^2} - \frac{q\cdot n_i}{\varepsilon_s\cdot\left(kT/q\right)}\cdot\left[\exp\left(\frac{-q\cdot\phi_i}{kT}\right) + \exp\left(\frac{q\cdot\phi_i}{kT}\right)\right] \tag{3-74}$$

Newton's Method can then be used to find an iterative, self-consistent solution for the electric potential throughout the SiC channel region. Since

$$f'(x) = \frac{f(x+\Delta x) - f(x)}{\Delta x} \tag{3-75}$$

Rearranging terms and setting $f(x+\Delta x)=0$ gives

$$f(x+\Delta x) = f(x) + f'(x)\cdot\Delta x = 0 \tag{3-76}$$

Similarly,

$$\begin{aligned} & f_i(\phi_{i-1}+\Delta\phi_{i-1},\phi_i+\Delta\phi_i,\phi_{i+1}+\Delta\phi_{i+1}) \\ &= f_i(\phi_{i-1},\phi_i,\phi_{i+1}) + \frac{\partial f_i}{\partial\phi_{i-1}}\cdot\Delta\phi_{i-1} + \frac{\partial f_i}{\partial\phi_i}\cdot\Delta\phi_i + \frac{\partial f_i}{\partial\phi_{i+1}}\cdot\Delta\phi_{i+1} = 0 \end{aligned} \tag{3-77}$$

Rearranging terms gives the following expression

$$\frac{\partial f_i}{\partial\phi_{i-1}}\cdot\Delta\phi_{i-1} + \frac{\partial f_i}{\partial\phi_i}\cdot\Delta\phi_i + \frac{\partial f_i}{\partial\phi_{i+1}}\cdot\Delta\phi_{i+1} = -f_i(\phi_{i-1},\phi_i,\phi_{i+1}) \tag{3-78}$$

which can be written in matrix format as:

$$\left[\frac{\partial f_i}{\partial \phi_{i-1}}, \frac{\partial f_i}{\partial \phi_i}, \frac{\partial f_i}{\partial \phi_{i+1}}\right] \times \begin{bmatrix} \Delta\phi_{i-1} \\ \Delta\phi_i \\ \Delta\phi_{i+1} \end{bmatrix} = -f_i(\phi_{i-1}, \phi_i, \phi_{i+1}) \tag{3-79}$$

A similar matrix can be written for the next point:

$$\left[\frac{\partial f_{i+1}}{\partial \phi_i}, \frac{\partial f_{i+1}}{\partial \phi_{i+1}}, \frac{\partial f_{i+1}}{\partial \phi_{i+2}}\right] \times \begin{bmatrix} \Delta\phi_i \\ \Delta\phi_{i+1} \\ \Delta\phi_{i+2} \end{bmatrix} = -f_i(\phi_i, \phi_{i+1}, \phi_{i+2}) \tag{3-80}$$

Combining all *N* equations produces a matrix expression

$$\left[\frac{\partial \overline{f}}{\partial \overline{\phi}}\right] \times \left[\Delta\overline{\phi}\right] = -\left[\overline{f}\right] \tag{3-81}$$

which must be solved for $[\Delta\phi]$:

$$\left[\Delta\overline{\phi}\right] = -\frac{\left[\overline{f}\right]}{\left[\frac{\partial \overline{f}}{\partial \overline{\phi}}\right]} \tag{3-82}$$

Such matrix arithmetic can be readily done using MATLAB software from Mathworks. With each iteration, the new value of the electric potential, $[\phi]$, throughout the semiconductor is updated by the incremental value, $[\Delta\phi]$, calculated as above, for each mesh point within the SiC. For example, for the k^{th} iteration:

$$\left[\overline{\phi}\right]^{k+1} = \left[\overline{\phi}\right]^{k} + \left[\Delta\overline{\phi}\right]^{k} \tag{3-83}$$

When $[\Delta\phi]$ falls below a chosen limit, the system of simultaneous equations is considered to have converged to a solution, yielding a self-consistent value for ϕ throughout the SiC channel region. As was the case for the analytic solution, once the electric potential is found, the carrier concentrations are readily found as well.

3.8 Numerical simulation of electric potential and field in the gate oxide region for a given oxide trap distribution

The tunneling model to be described in Chapter 6 has as one of its inputs the electric field in the gate oxide, which varies spatially due to the charged oxide traps in the interfacial region. This section will describe how the field is determined, given an oxide trap distribution. The first step is to assume a certain volumetric density distribution of oxide traps as a function of oxide depth.

$$n_{OT\_total}(x) = n_{OT\_surf.} \cdot \exp\{-\lambda \cdot x\} \tag{3-84}$$

where λ is the decay factor and $n_{OT\_surf.}$ is the density at the interface, which is related to the assumed total areal density, N_{OT_total}, and depth over which oxide traps exist, t_{OT}, as defined in (3-39):

$$n_{OT\_surf.} = N_{OT\_total} \cdot \frac{\lambda}{1 - \exp\{-\lambda \cdot t_{OT}\}} \tag{3-85}$$

which reduces to

$$n_{OT\_surf.} = \frac{N_{OT\_total}}{t_{OT}} \tag{3-86}$$

when $\lambda = 0$, which is the case for a rectangular distribution. Figure 3-14 illustrates a range of distributions, depending on the value of λ, assuming that all the oxide traps lie within 50 Å of the interface.

When discretizing this oxide trap distribution, an areal density sheet of charge can be calculated at each mesh point, where n_{OT} is the distribution of positively charged oxide traps:

$$dQ_{OT}(n) = q \cdot n_{OT}(n) \cdot dx \tag{3-87}$$

Summing all the increments gives the total oxide trap charge:

$$Q_{OT} = \sum_{n=1}^{N} dQ_{OT}(n) \tag{3-88}$$

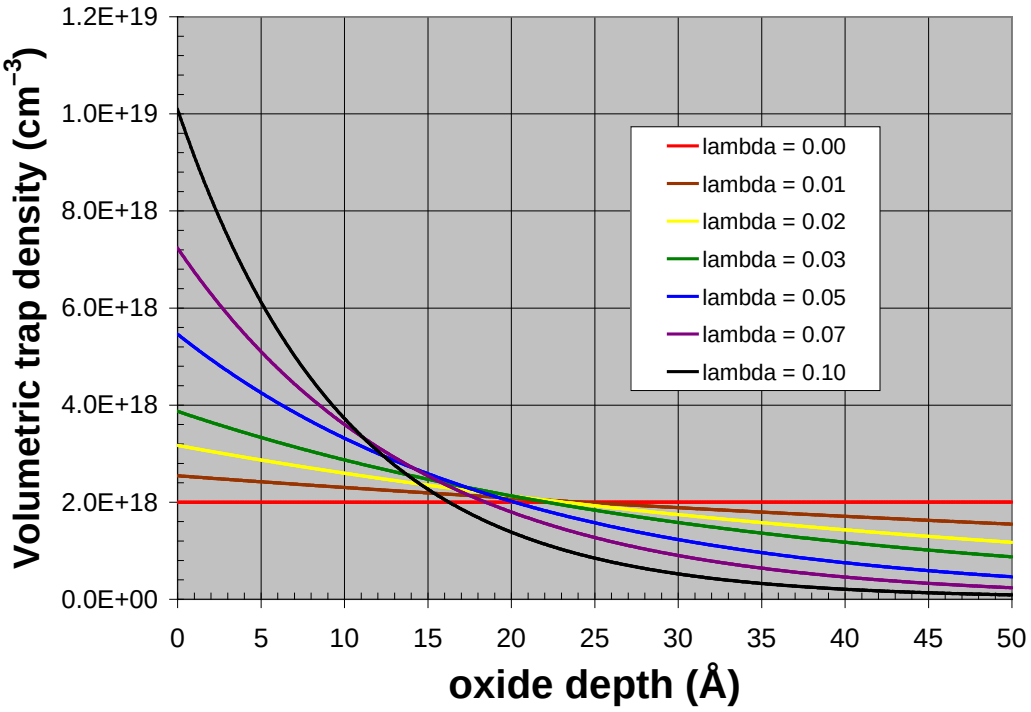

Figure 3-14: Variation of oxide trap distribution versus decay parameter λ, for equal total charge over first 50 Å from the interface.

The charge centroid was calculated in (3-35); the discrete version is

$$\overline{d_{OX}} = \frac{\sum_{n=1}^{N} dQ_{OT}(n) \cdot \left(t_{OX} - n_{OT} \cdot dx\right)}{\sum_{n=1}^{N} dQ_{OT}(n)} \tag{3-89}$$

and the charge centroid factor is found as in (3-42) and V_{OT} as in (3-44).

Although it is possible to solve for ϕ simultaneously throughout both the SiC semiconductor and the gate oxide, by defining the mesh point at the interface using Gauss' Law

$$\varepsilon_{OX} \cdot \frac{(\phi_i - \phi_{i-1})}{\Delta x} = \varepsilon_{SiC} \cdot \frac{(\phi_{i+1} - \phi_i)}{\Delta x} \tag{3-90}$$

it is more convenient to solve for the electric potential separately, in the SiC as described previously, and in the gate oxide as described below. This is possible since (3-19) describes the electric field at the surface exactly due to the surface potential, and the electric potential at the interface is defined by (3-61). However, solving for the electric potential piecemeal does require an iterative method for determining the proper surface potential for a given applied gate-to-source voltage, since the tunneling model seeks to simulate the experimental method of necessarily applying an external bias instead of choosing an internal field or potential.

Newton's Method can once again be employed, but this time solving for ψ_s instead of ϕ, by defining a function, *f*, as the difference of the two sides of (3-55)

$$f(\psi_s) = V_{GS} - \left(\phi_{ms} + \frac{\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S}(\psi_s)}{C_{OX}} - \frac{Q_{OT} \cdot f_{cent.}}{C_{OX}} - \frac{Q_{IT}(\psi_s)}{C_{OX}} + \psi_s \right) \tag{3-91}$$

and calculating the derivative in terms of ψ_s.

Once the surface potential is found for a given V_{GS}, then the electric potential at the interface and gate can be found using (3-61) and (3-62), respectively, and the electric field in the bulk of the gate oxide, where no oxide traps exist, can be found by again applying Gauss' Law

$$\mathcal{E}_{OX\_B} = \frac{\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S} - (Q_{OT} + Q_{IT})}{\varepsilon_0 \cdot \varepsilon_{OX}} \tag{3-92}$$

Next, the electric potential at the edge of the oxide trap region of the gate oxide can be found:

$$\phi_{bulk} = \phi(x = t_{OT}) = \phi_{gate} - \mathcal{E}_{OX\_B} \cdot (t_{OX} - t_{OT}) \tag{3-93}$$

The electric potential as a function of position in the bulk of the gate oxide, which ranges from $x = t_{OT}$ (the furthest distance that oxide traps extend from the SiC interface) to $x = t_{OX}$ (the full thickness of the gate oxide, all the way to the poly-Si gate), is then

$$\begin{aligned} \phi(x : t_{OT} \ldots t_{OX}) &= \phi_{bulk} + \mathcal{E}_{OX\_B} \cdot (x - t_{OT}) \\ &= \phi_{bulk} + \left[\frac{\phi_{gate} - \phi_{bulk}}{t_{OX} - t_{OT}} \right] \cdot (x - t_{OT}) \end{aligned} \tag{3-94}$$

Before solving exactly for the electric potential in the oxide trap region using numerical simulation techniques, an approximate solution is first calculated to provide a proper starting point for the exact solution, assuming a rectangular distribution of filled oxide traps.

$$\begin{aligned} \phi(x : 0 \ldots t_{OT}) &= \phi_{bulk} + \mathcal{E}_{OX\_B} \cdot (x - t_{OT}) \\ &- \frac{1}{2} \cdot \left[\frac{\mathcal{E}_{OX\_S\_IT} - \mathcal{E}_{OX\_B}}{t_{OT}} \right] \cdot (x - t_{OT})^2 \end{aligned} \tag{3-95}$$

where

$$\mathcal{E}_{OX\_S\_IT} = \frac{\varepsilon_0 \cdot \varepsilon_{SiC} \cdot \mathcal{E}_{SiC\_S} - Q_{IT}}{\varepsilon_0 \cdot \varepsilon_{OX}} \tag{3-96}$$

A numerical solution can again be found by solving simultaneously—iteratively using Newton's Method—a set of discretized Poisson's Equations, as in (3-70), in the oxide trap region of the gate oxide

$$\frac{\partial^2 \phi}{\partial x^2}|_i = \frac{\phi_{i-1} - 2 \cdot \phi_i + \phi_{i+1}}{(\Delta x)^2} = -\frac{q}{\varepsilon_{OX}} \cdot \left[n_{OT_i} \right] \tag{3-97}$$

so that the function, *f*, the difference of the two sides of (3-97), is

$$f_i(\phi_{i-1}, \phi_i, \phi_{i+1}) = \frac{\phi_{i-1} - 2 \cdot \phi_i + \phi_{i+1}}{(\Delta x)^2} + \frac{q \cdot n_{OT_i}}{\varepsilon_{OX}} \tag{3-98}$$

and the derivative in terms of ϕ is

$$\frac{\partial f_i(\phi_{i-1}, \phi_i, \phi_{i+1})}{\partial \phi_{i-1}} = \frac{\partial f_i(\phi_{i-1}, \phi_i, \phi_{i+1})}{\partial \phi_{i+1}} = \frac{1}{(\Delta x)^2} \tag{3-99}$$

$$\frac{\partial f_i(\phi_{i-1}, \phi_i, \phi_{i+1})}{\partial \phi_i} = \frac{-2}{(\Delta x)^2} \tag{3-100}$$

Once the electric potential is found, the electric field can be readily calculated:

$$\mathcal{E}_{OX}(n + 0.5) = -\left(\frac{\phi(n+1) - \phi(n)}{\Delta x} \right) \tag{3-101}$$

As a check, the areal charge density at each mesh point can be found from the change in the electric field:

$$dQ(n) = \varepsilon_{OX} \cdot \left[\mathcal{E}_{OX}(n + 0.5) - \mathcal{E}_{OX}(n - 0.5) \right] \tag{3-102}$$

which should be the same value as that found from (3-87). Figure 3-15 graphically shows the relationship between the different variables and their mesh point counters.

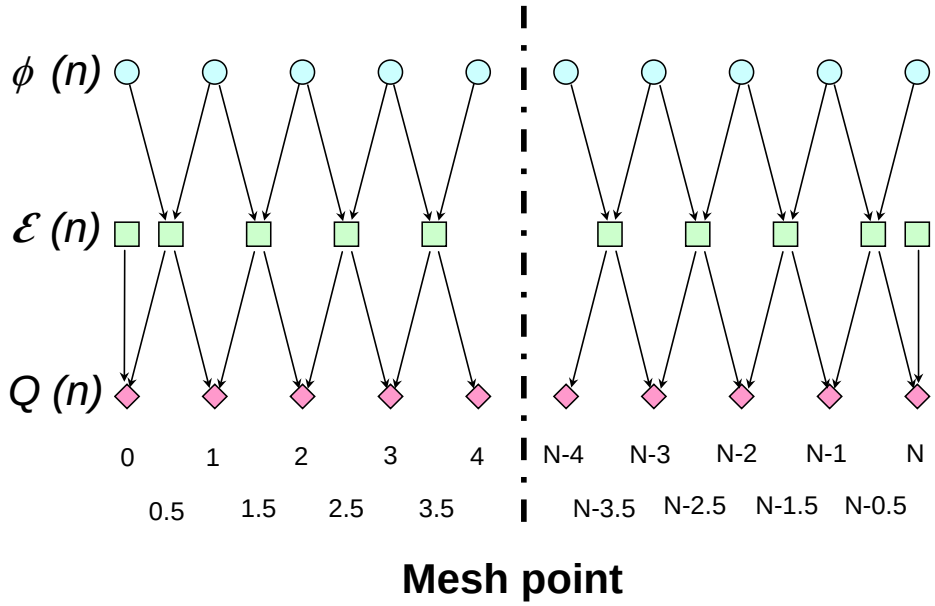

Figure 3-15: Schematic of how the electric field values are derived from the electric potential, and how the charge density values are confirmed by the electric field values.

3.9 Summary of calculations

This chapter has described how the ideal threshold voltage can be found by calculating the voltage drop across the oxide and semiconductor when the surface potential is at inversion, along with the adjustment due to the work function difference between the poly-Si gate and SiC substrate. It further described how the various types of interfacial charge can cause a shift in V_T.

Of particular interest is the determination of the field in the oxide near the interface for a given applied gate-bias and assumed trap distribution and occupancy, since this information is required by the tunneling model to calculate a time-dependent change in the distribution of occupied oxide traps. The process is as follows:

1. Choose desired gate-to-source bias.
2. Determine surface potential consistent with chosen V_{GS} value and assumed charge distribution for both oxide traps and interface traps.
3. Calculate boundary conditions for electric potential at gate, interface, and SiC substrate bulk based on chosen V_{GS} and calculated surface potential, and verify by calculating electric field at interface from the surface potential.
4. Self-consistently determine electric potential throughout the device based on assumed interfacial charge distributions and doping density using numerical simulation techniques. Use approximate solution determined from analytical calculations as starting point.
5. Calculate oxide field from electric potential.

The inversion carrier concentration is also readily calculated once the potential in the SiC is determined.

In addition, it was observed that the bulk oxide field does not vary much at all with trapped charge, and that the actual positive and negative high-field values are only slightly lower than the generally assumed rule-of-thumb value of V_{GS} / t_{OX} —which may be of importance when deciphering TDDB results. However, the oxide field at the surface can change significantly with interfacial charge.

4 Basic Experimental Results of Threshold-Voltage Instability Effect

4.1 Introduction

The experimental results of this study are presented in three parts. The basic threshold-voltage instability effect is presented in this chapter. The time-dependence of the measurements is presented in the following chapter. Finally, the effect of this threshold-voltage instability effect on the reliability of actual SiC power MOSFET devices will be presented in Chapter 7.

This chapter will present basic instability test results on both lateral MOSFET and capacitor test structures. The basic physical mechanisms that are responsible for this phenomenon are discussed.

4.2 The device sample sets

The devices studied in this work came primarily from one leading U.S. manufacturer of SiC devices, which prefers to remain unnamed, although I also studied devices from two other sources and observed similar threshold-voltage instabilities. This instability, which is typically on the order of between 0.25 and 0.5 volts for devices with gate oxide thicknesses of 500 to 1000 Å, following a gate-bias stress of about +/- 1 MV/cm applied for 5 minutes under each polarity, has been observed in both deposited and thermal oxides, in devices with both as-grown and implanted epitaxial SiC at the interface, and in devices on both 4H and 6H SiC. The results presented in this chapter are all on lateral 4H-SiC MOSFETs, along with some 4H-SiC capacitor data.

Other than the obvious improvement provided by the NO post-oxidation anneal, this is not a study of processing variations. The same basic effect was always observed. Although numerous different sample sets were used in this study, they all behaved in the same general way, other than more recent devices showing a general improvement in their characteristics [105].

Figure 4-1shows an image of the primary lateral test chips used in this study (Sample Sets C, D, and E; as described below), with side-by-side as-grown epi (N_a ~ 1×10^{16} cm^{-3}) and implanted epi (N_a ~ 1×10^{17} cm^{-3}) chips available. The implanted epi devices mimic the implanted region of the implanted DMOSFET channel (see Figure 7-1), and generally have lower effective channel mobilities compared to the as-grown epi devices. Figure 4-2 highlights various devices available for testing. There are lateral *n*-channel MOSFETs, with varying gate areas and geometries: wide, short devices—100×3 and 100×5 (channel width by length in microns), 100×100 up to 400×400 so-called "FATFETs" because of their large gate area, and circular geometry enclosed MOSFETs with the source in the center and the drain on the outside that range from 424×1.0 up to 424×20 microns. These test chips also include *n*-type and *p*-type MOS capacitors with areas of 4×10^{-4} cm^2, 9×10^{-4} cm^2, and 16×10^{-4} cm^2. MOS Hall-bar test structures are also included, which could allow for the acquisition of Hall mobility and free carrier concentration measurements, the latter potentially useful in verifying the number of free carriers available to tunnel into the oxide traps under positive bias.

The lateral *n*-channel 4H-SiC MOSFET devices whose instability results are shown in this work came from nine different samples sets (shown in Table 4-1), wherein two of the sample sets had differently processed devices.

Table 4-1: Lateral test structure sample sets used to obtain experimental results presented in Chapters 4 and 5.

Sample Set	t_{OX} (Å)	oxide	growth	N anneal
A	500	LPCVD	410°C LTO + 1200°C Dry	1300°C NH_3
B	600	thermal	1200°C Dry + 950°C Wet	1300°C NH_3
C	1,000	LPCVD	410°C LTO + 1200°C Dry	1300°C NH_3
D	1,300	LPCVD	410°C LTO + 1200°C Dry	1300°C NH_3
E	600	thermal	1200°C Dry + 950°C Wet	1300°C NO
F	600	thermal	1200°C Dry + 950°C Wet	1175°C NO
G	500	thermal	1175°C Dry + 950°C Wet	1175°C NO
G	500	thermal	1175°C Dry + 950°C Wet	none
H	500	thermal	not available	yes
I	500	thermal	1175°C Dry + 950°C Wet	1175°C NO

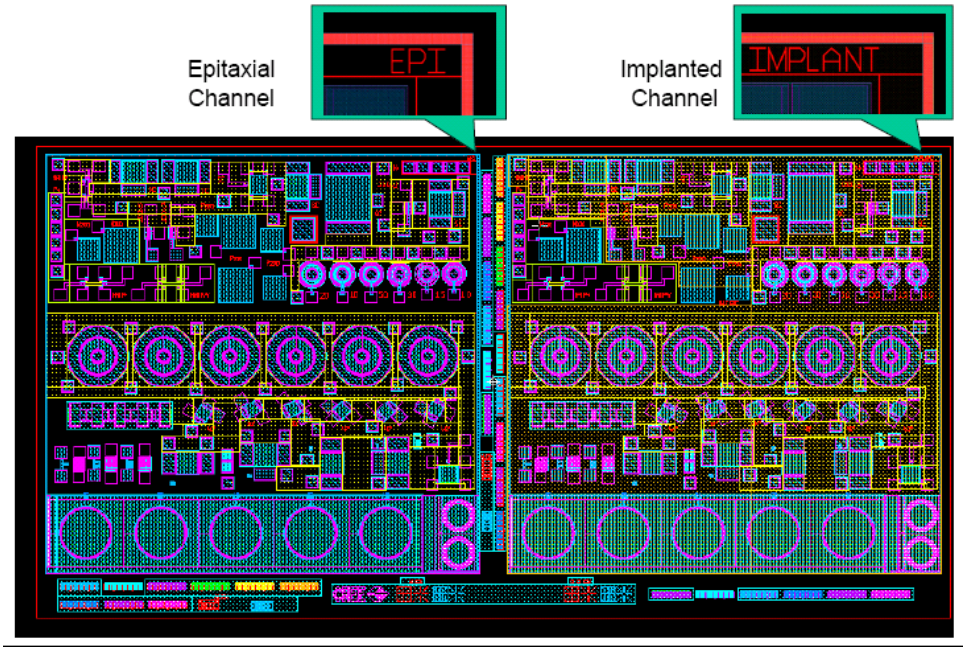

Figure 4-1: Image of the lateral 4H SiC MOS test chip, the main test vehicle for this study.

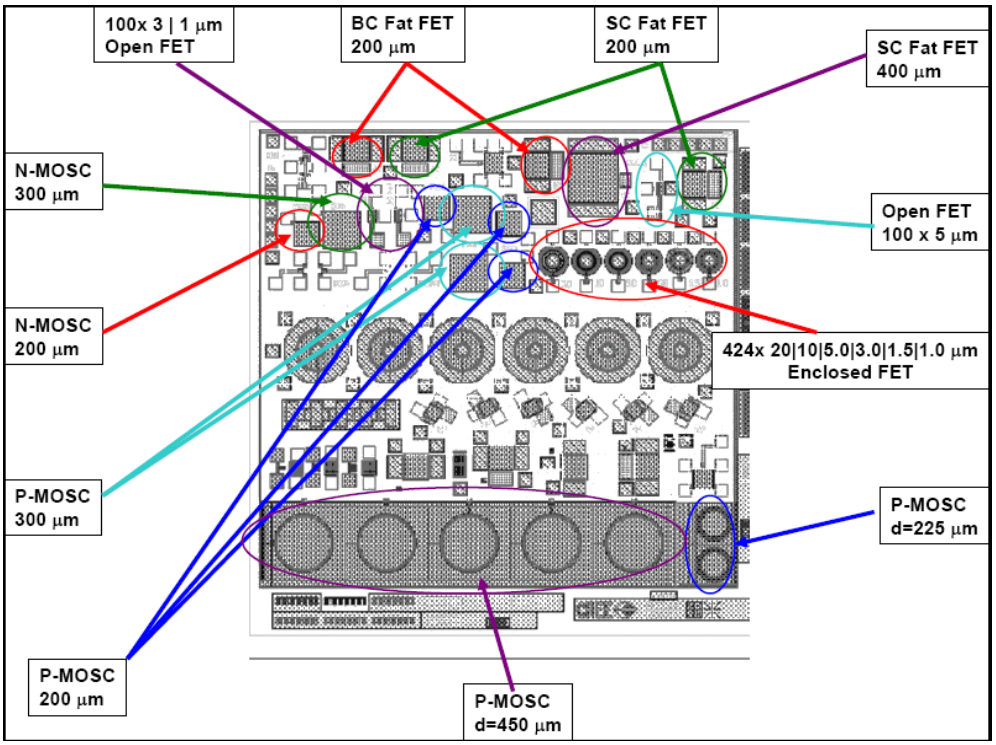

Figure 4-2: Lateral 4H SiC MOS test chip layout with main structures of interest highlighted.

Thus, several different process splits were available for comparison: thermally grown oxides vs deposited (LPCVD) oxides, NO post-oxidation anneal vs no nitridation, and as-grown SiC epi vs implanted SiC.

The gate-bias stressing experiments were performed primarily on lateral 4H SiC MOSFETs with enclosed circular geometries. Because these devices have an enclosed geometry, they did not suffer from parasitic edge leakage and therefore allowed for lower subthreshold current measurements that were important when calculating the subthreshold swing, which will be discussed in the following chapter. Subthreshold swing analysis is useful in determining an upper bound for the interface trap density, and the change in this slope is a measure of the number of oxide trap states that have filled or emptied during the course of the measurement itself, providing a lower bound for the

total oxide trap density. A clean subthreshold current measurement is also useful in extracting the threshold voltage using the inversion current method, as mentioned below. Low edge leakage is also important when making charge-pumping measurements, which is another measurement technique that can provide insight regarding the number of oxide traps and interface traps present.

4.3 Experimental procedure

The standard threshold-voltage instability measurement was performed as follows (see Figure 4-3). Initially, the gate voltage was ramped from negative to positive bias, with 50 mV applied to the drain, using an Agilent 4155 parameter analyzer. The fastest sweep possible with reasonable resolution is around 1 s. It should be noted that once the device has been bias stressed, the initial sweep may be dependent on its previous bias history. Next, a positive bias was applied to the gate for the desired bias-stress time while the other terminals were grounded, again using the Agilent 4155. Following the termination of the positive-bias stress, the gate voltage was ramped from positive to negative bias to determine the shift of the drain current-gate voltage (I_D-V_{GS}) characteristic. A negative bias equal in magnitude but opposite in polarity was then applied to the gate for the same bias-stress time. Finally, the gate voltage was once again ramped from negative to positive bias to measure the return shift.

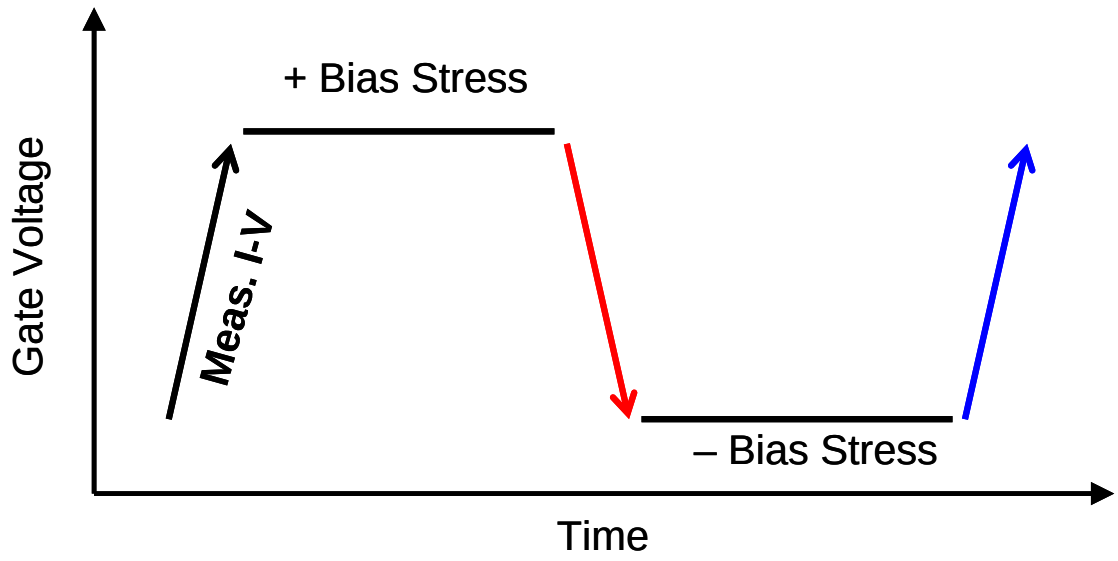

Figure 4-3: Schematic indicating the applied gate voltage versus time during the instability measurements.

Unless mobile ions are involved, a positive-bias stress will result in a positive shift in V_T and a negative-bias stress will cause a negative shift in V_T. This effect can be explained by electrons filling or emptying near-interfacial oxide traps via direct tunneling in response to the electric field. Typically three or four full cycles are applied to the device under test. V_T can be readily calculated by linear extrapolation of the maximum slope to zero current, or by choosing a current level such as the calculated inversion current which occurs in the subthreshold region and then finding the corresponding voltage. The average shift in V_T is then calculated. It was found that either method for calculating V_T results in a similar V_T instability value, and that this measurement is very repeatable, as is discussed below [38].

Because of the linear-with-log-stress-time response described below, I suspected that a tunneling mechanism that is very sensitive to the measurement time was involved. Therefore, I encouraged colleagues at NIST to make measurements with their fast *I-V*

system (a schematic of which is depicted in Figure 4-4) that they developed, which can be used to ramp the gate voltage as quickly as 20 μs. The details of this measurement system, which was developed to look at charge traps in high-*k* dielectric materials and that I realized would be useful in the study of oxide traps in SiC MOSFETs, are described elsewhere [76]. Here I will simply mention that a pulse generator is connected to the gate terminal and a fast op-amp is employed to measure the drain current without changing the drain bias. Both the drain current and gate voltage signals are captured by a digital oscilloscope. The main limitation is that the *I*-*V* sweep is limited to the voltage range during the stress and that the drain bias is also applied during the stress. However, because it is limited to 100 mV, it should not lead to hot carrier injection.

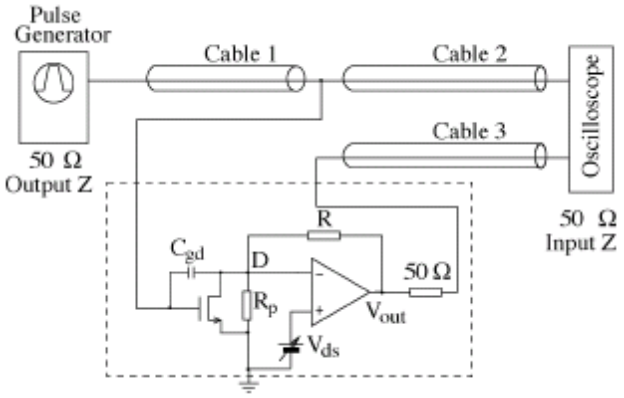

Figure 4-4: Schematic of fast *I*-*V* system employed at NIST.

Similarly, *p*-type MOS capacitors were measured and bias-stressed using an HP 4194 Impedance/Gain-Phase Analyzer. In this case, the gate bias was initially swept up in voltage from accumulation to inversion. The flat-band voltage, V_{FB}, was estimated from the ideal flat-band capacitance, C_{FB}. The *C*-*V* characteristics took a little longer to measure, with each measurement sweep typically taking 2 to 10 seconds to complete.

FATFET *n*-channel MOSFETs were also measured as capacitors in some cases, to confirm the *p*-type MOS capacitor results, by slightly biasing the source and drain positively with respect to the substrate.

Unless otherwise indicated, all the measurements presented in this work were performed at room temperature.

4.4 Basic experimental effect of gate-bias stress induced threshold-voltage instability

Figure 4-5 shows a series of *I-V* characteristics, plotted on both a log (on the left) and linear (on the right) current scale, measured using the Agilent 4155 with a 1-s sweep time after both positive and negative-bias stressing, as described above for an enclosed geometry device from Sample Set D. Three sweeps are apparent for each scale—the initial sweep, all the sweeps following positive-bias stressing, and all the sweeps following negative-bias stressing. In fact, there are twelve curves for each post bias-stressing sweep. In this case, each gate-voltage bias stress lasted for 1,000 seconds, with ±10V applied to the gate of a 130 nm deposited oxide MOSFET.

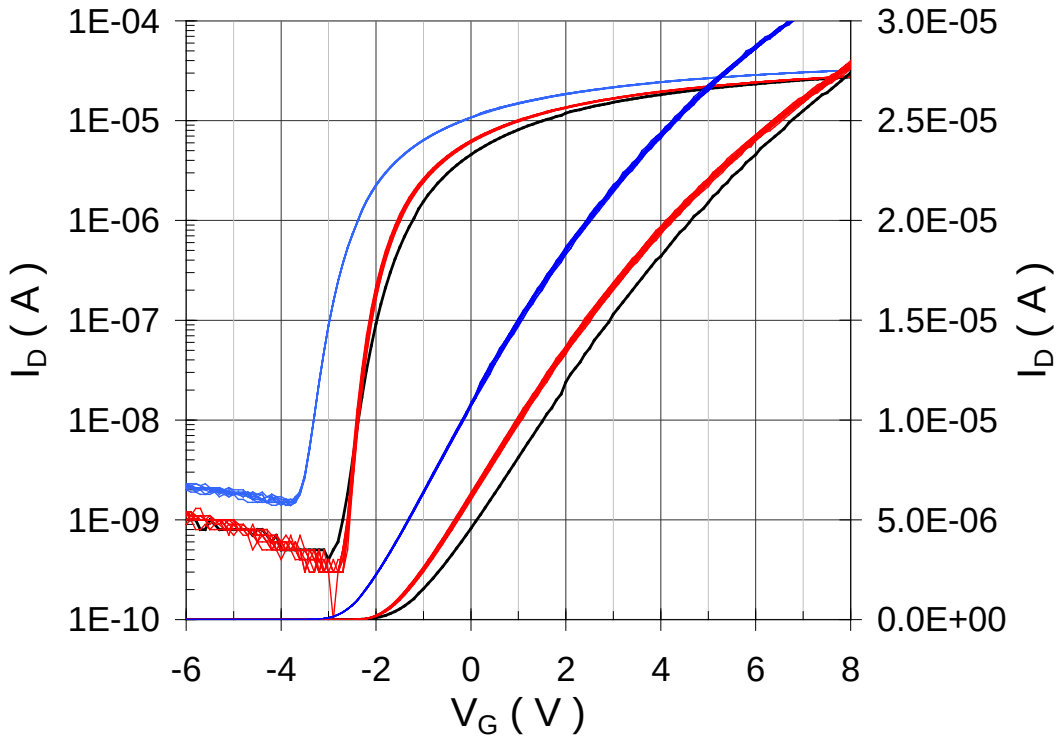

Figure 4-5: Graph of I_D-V_{GS} curves of a SiC MOSFET from Sample Set D with a 130-nm thick deposited gate oxide, plotted on both a log (left) and linear (right) current scale, for a series of twelve full cycles of bias stress (±10 V for 1,000 seconds at each polarity) and measurement as indicated in Figure 4-4. Positive-bias stress causes a shift of the *I-V* characteristic to the right and a negative-bias stress causes a shift of the *I-V* characteristic back to the left.

Figure 4-6 plots the extracted threshold voltage (for both the linear and inversion current methods) versus cumulative stress time. As can readily be seen, the effect of the alternate positive and negative-bias stress is to repeatedly shift the threshold voltage back and forth, with increasing V_T following a positive-bias stress and decreasing V_T following a negative-bias stress. The linear V_T extraction consistently yields a more positive value than does the inversion current method.

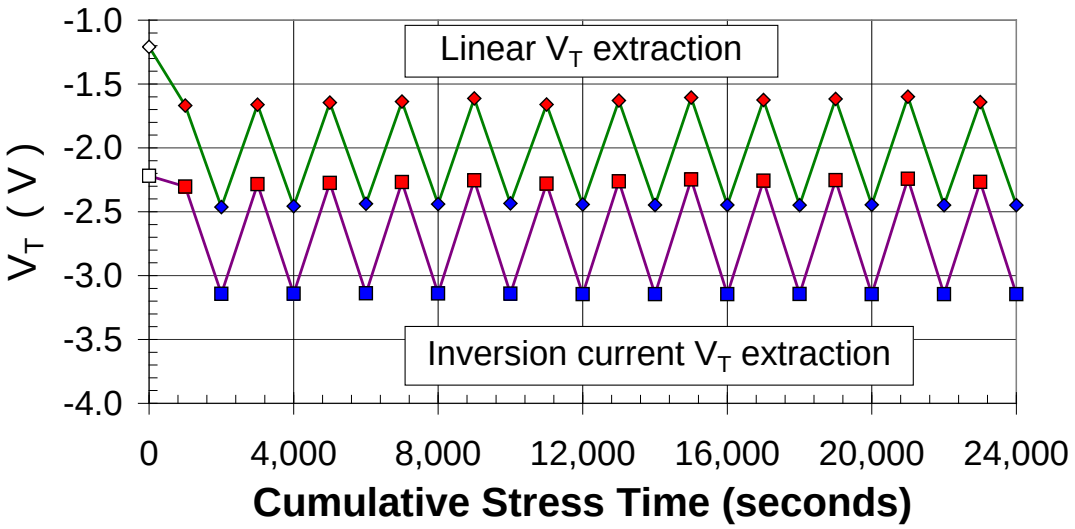

Figure 4-6: Calculated V_T instability of a SiC MOSFET from Sample Set D using both linear extrapolation and inversion current methods following each bias stress and measurement versus cumulative stress time.

Figure 4-7 plots the magnitude of the threshold voltage back-and-forth instability for each bias stress as a function of cumulative stress time using the data of Figure 4-6. In this case it is clear that although the two methods extract different values for V_T, the back-and-forth instability calculated is almost identical, varying by less than ten percent. These instabilities are much larger than those usually observed in SiC MOSFETs since the gate oxide is much thicker for these samples, and the voltage shift is proportional to the oxide thickness (see (3-32)). Thus, the data from these samples very clearly demonstrates this instability phenomenon, which has been observed in SiC MOSFETs with both thermal as well as deposited gate oxides. By comparison, it should be noted that instabilities in as-processed Si MOSFETs with similar oxide thicknesses are typically only a few mV at room temperature.

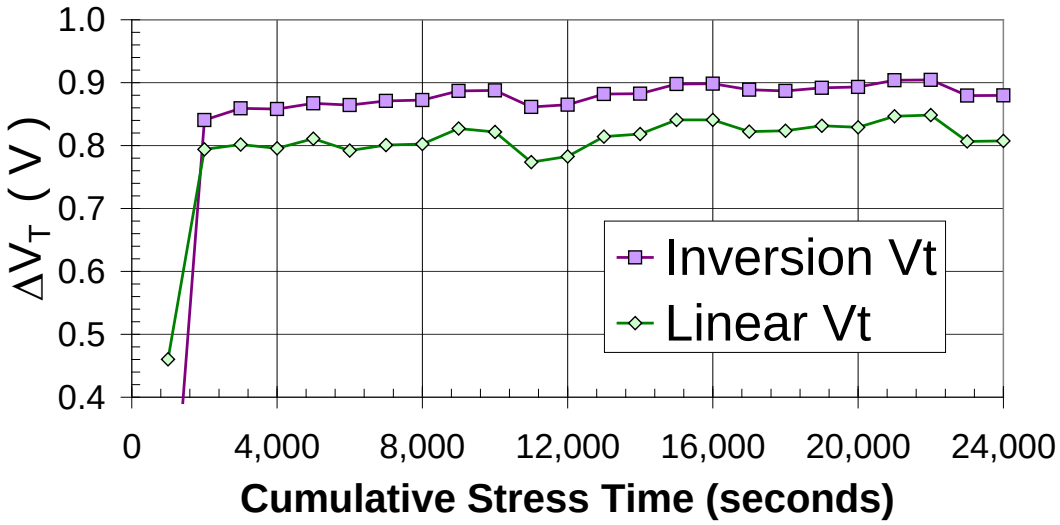

Figure 4-7: Calculated change in V_T of a SiC MOSFET from Sample Set D using both linear extrapolation and inversion current methods following each bias stress and measurement versus cumulative stress time.

It has also been observed that the result is affected by the measurement. Therefore, it is important how the measurement is made. For example, the direction and extent that the gate is swept during the measurement can make a big difference. The importance of sweeping down in gate bias following a positive-bias stress is illustrated in Figure 4-8, which shows the variation in the back-and-forth V_T instability of a SiC MOSFET from Sample Set A, depending on whether the gate bias is swept down or up following a positive-bias stress. This difference occurs due to the strong effect of the gate bias during the measurement, during which time an additional effective bias stress is being applied. When the bias is swept down following a positive gate bias stress, the bias during the sweep is not that much different than that of the stress and therefore oxide traps do not readily change charge state. On the other hand, when the bias is swept up following a positive gate bias stress, the initial bias during the sweep is very much different than that of the stress and more oxide traps will change charge state. How much

they change charge state is also a function of the sweep time, as will be discussed in detail in Chapter 5. Also note that the curves following a negative gate-bias stress are basically identical. This reiterates the repeatability of the basic effect.

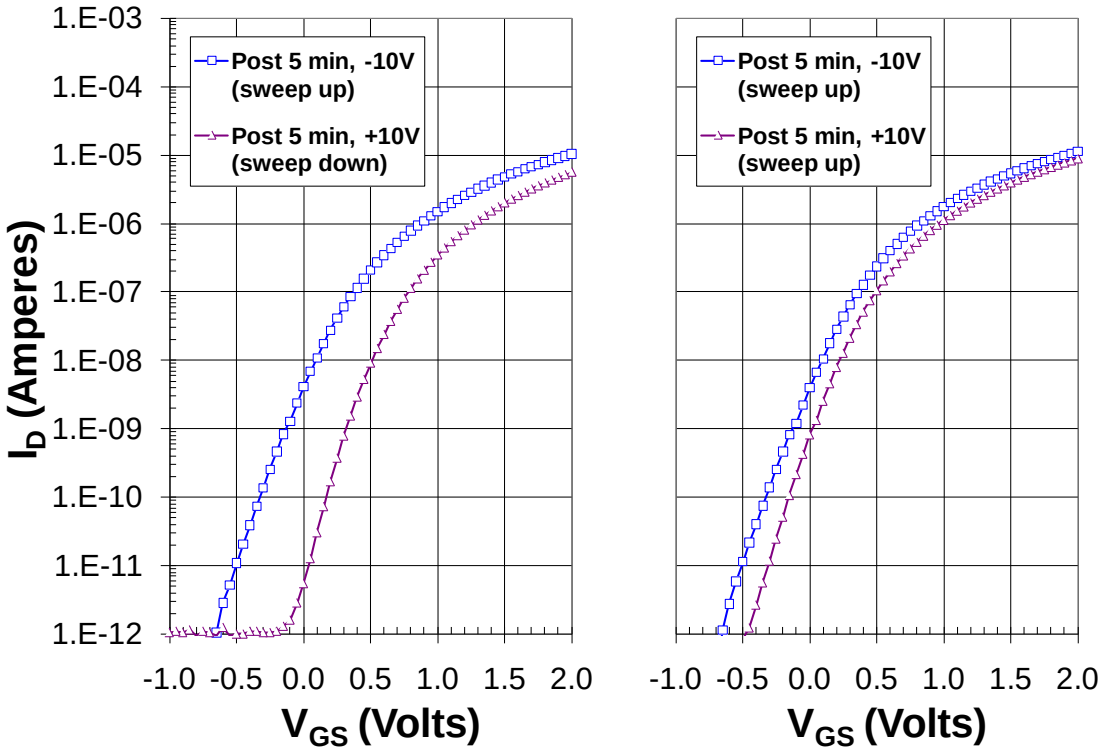

Figure 4-8: Variation in the back-and-forth V_T instability of a SiC MOSFET from Sample Set A, depending on whether the gate bias is swept down or up following a positive-bias stress.

4.5 Effect of bias-stress magnitude

Figure 4-9 shows a plot of the V_T instability (calculated using the inversion current method) for a device from Sample Set D for a variety of different gate-bias stresses, ranging from ±2.5 V up to ±20V versus the bias-stress time, plotted on a log-time scale. The magnitude of the instability clearly increases with the magnitude of the

gate bias stress applied. Although there is noise in this data, which is the result of averaging three bias stresses at each polarity, the overall trend appears to be linear with log time. The ±5 V data looks particularly clean, and is taken out to 100,000 seconds (in other words, to obtain that last data point the bias stress was held for over a day at each polarity before switching). No obvious saturation is observed. The early time data (bias stresses lasting for less than 100 seconds at a time) is strongly influenced by the measurement itself, leading to sub-linear-with-log-time behavior—especially for this data set, for which the Agilent 4155 ramp time had not been optimized and thus took closer to 10 s to complete. This linear-with-log-time behavior is consistent with charge tunneling into and out of oxide traps that are distributed uniformly spatially into the oxide from the SiC/SiO_2 interface.

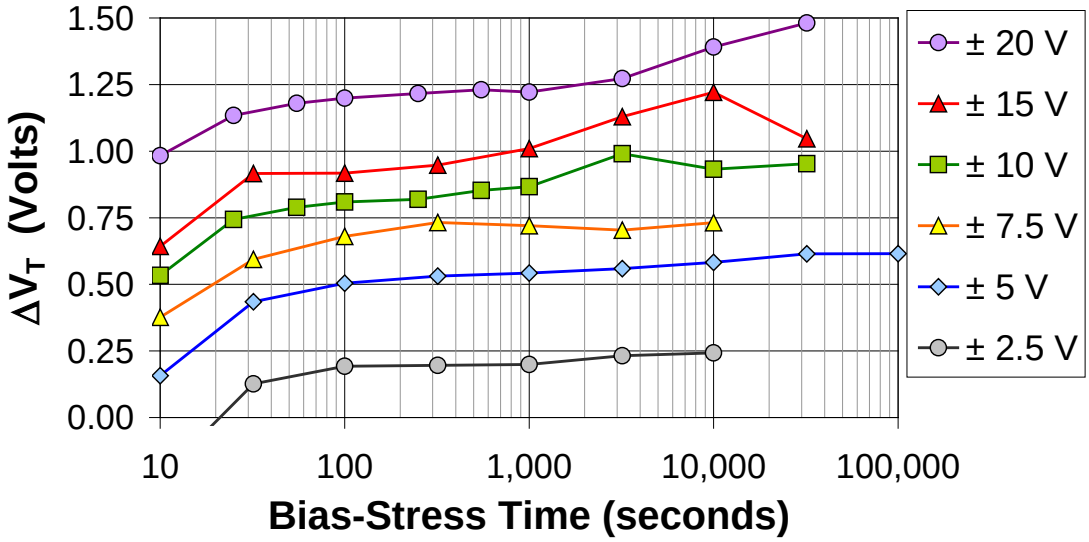

Figure 4-9: Change in V_T of a SiC MOSFET from Sample Set D with a 130-nm thick deposited gate oxide, calculated using inversion current method, versus log stress time for various applied gate biases for a SiC MOSFET with a thick deposited gate oxide.

Figure 4-10 re-plots the data from Figure 4-9, but displays the actual calculated back-and-forth threshold voltage values, showing that for this sample with a deposited oxide, there is a much greater sensitivity to the bias magnitude under negative bias than under positive bias. This information is useful in trying to determine the energy level of the near-interfacial oxide traps, as will be discussed in detail in Chapter 6.

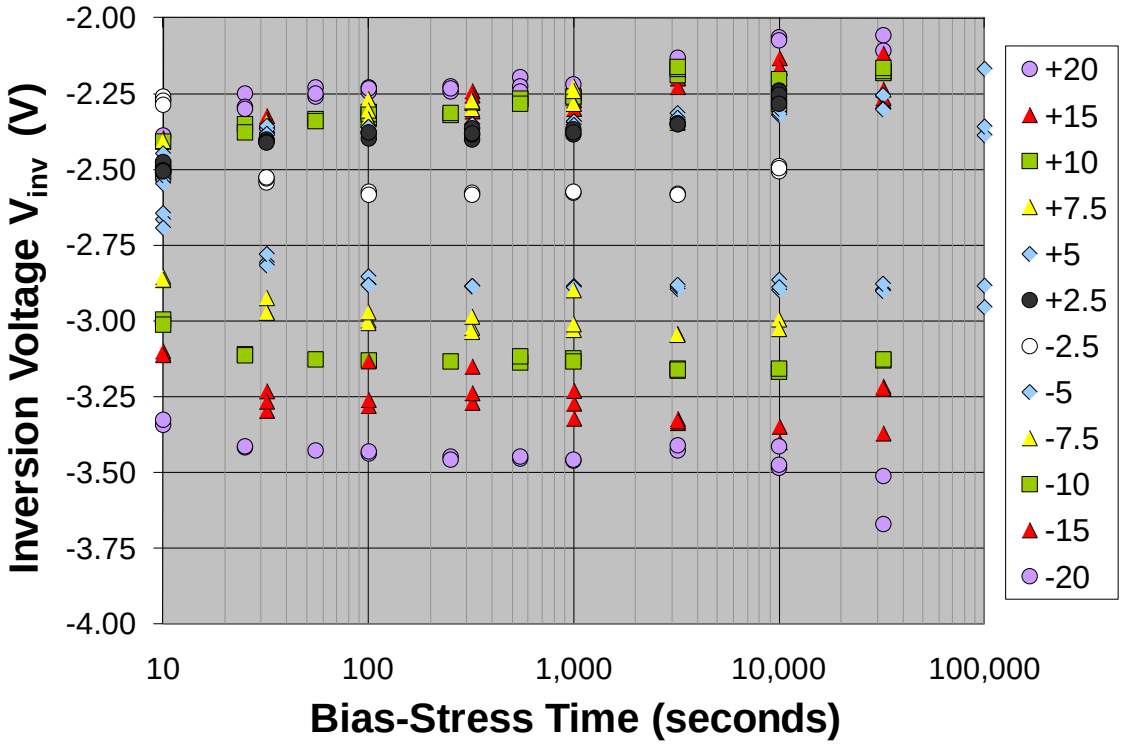

Figure 4-10: Data from Figure 4-9 re-plotted showing variation in V_T of a SiC MOSFET from Sample Set D using inversion current method as a function of both bias magnitude and polarity. This device is older, with a thick deposited oxide.

Figure 4-11 shows the results of a similar experiment, but in this case it is for an enclosed geometry MOSFET from Sample Set I, whose gate oxide was thermally grown. In this case, the much greater sensitivity to the magnitude of the bias occurs under positive bias. Devices from Sample Set H (both with and without an NO post-oxidation

anneal) which also had a thermal oxide were tested in a similar fashion and exhibited similar results. It is interesting to note that although a thermal oxide is more sensitive to positive bias and a deposited oxide is more sensitive to negative bias, both types of oxides exhibit a similar overall gate-bias stress-induced V_T instability. This may possibly be due to different energy levels for their respective oxide traps.

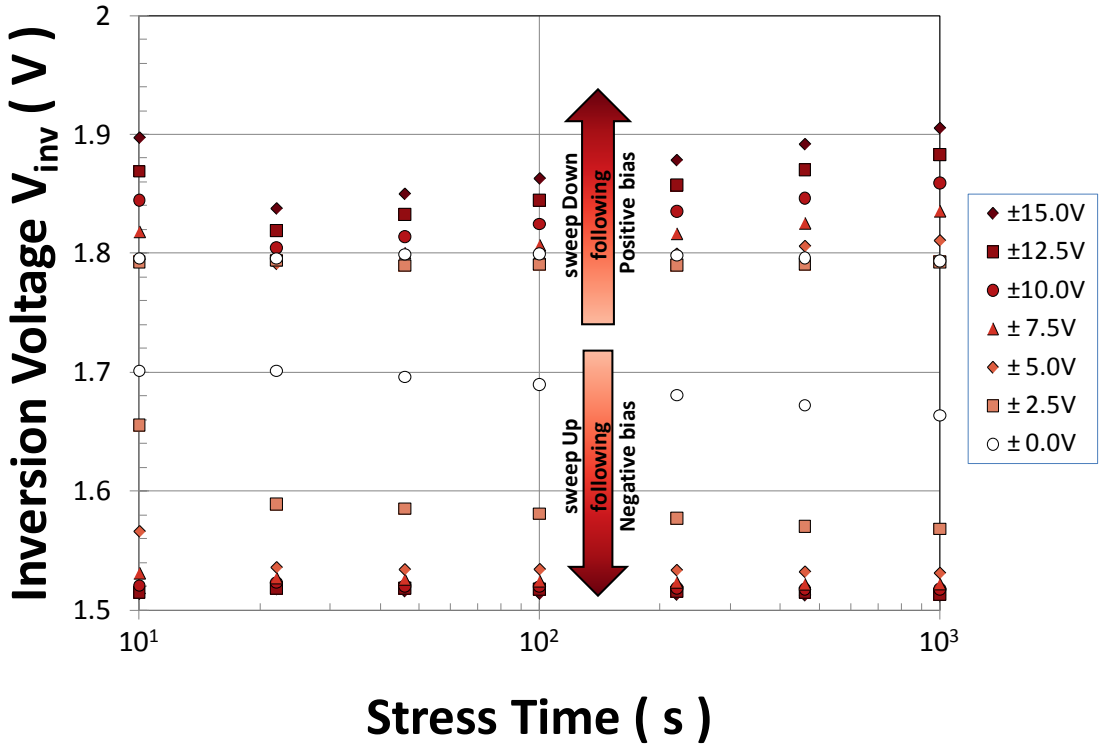

Figure 4-11: Variation in V_T of a SiC MOSFET from Sample Set I with a newer, thermal oxide using inversion current method as a function of both bias magnitude and polarity. This devices is more recent, with a less thick thermal oxide.

Figure 4-12 shows the I_D-V_{GS} instability characteristics of an enclosed geometry 4H-SiC lateral *n*-channel MOSFET from Sample Set F, which has a 60-nm thick thermal gate oxide and received a standard post-oxidation nitrogen anneal using NO, measured using the Agilent 4155 and its 1-s ramp speed.

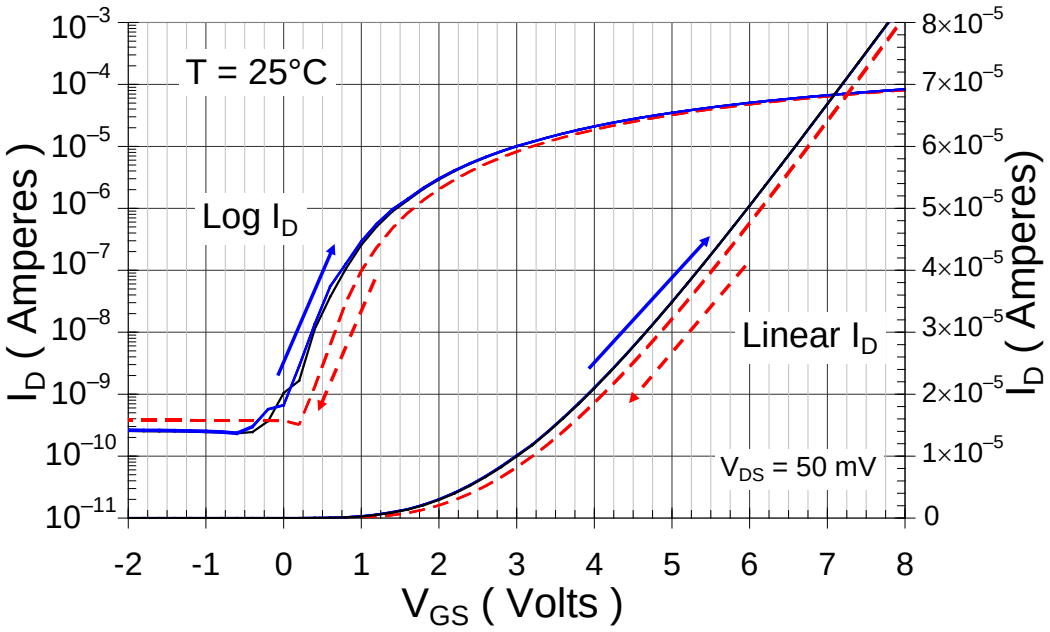

Figure 4-12: Graph of I_D-V_{GS} curves of a lateral 4H-SiC MOSFET from Sample Set F with a 60-nm thick thermal oxide with an NO post-oxidation anneal, plotted on both a log (left) and linear (right) current scale, for three full cycles of bias stress and measurement (±2 MV/cm, 34-ks stress, 1-s ramp).

Figure 4-13 shows the average threshold-voltage instability for various bias-stress times and gate oxide fields (the results from Figure 4-12 are indicated in the upper right data point of Figure 4-13: individual bias stress time of 34,000 s with a gate oxide field stress of ±2 MV/cm, due to an effective gate-bias stress of ±13 V). Once again, a linear-with-log-stress-time response of the V_T instability with applied bias is observed, consistent with electrons tunneling directly from the SiC into oxide traps that are distributed rather uniformly with distance into the insulator. The longer the bias stress time, the deeper into the oxide the tunneling front can reach (see Chapter 6 for a full discussion of the tunneling mechanism). The greater the bias, the more effectively the tunneling process occurs. Under reverse bias, the charge is presumably tunneling out in a

similar manner. The number of traps that are switching charge state to create the instability observed for a 1,000 s bias stress with a ±1.5 MV/cm gate oxide field applied was found for this sample and measurement to be about 1.0×10^{11} cm^{-2} oxide traps:

$$N_{OT} \cong \frac{C_{OX}}{q}\cdot\Delta V_T = \frac{\varepsilon}{q\cdot t_{OX}}\cdot\Delta V_T$$
$$= \frac{3.9\cdot 8.85\times10^{-14}\ (\mathrm{F/cm})}{1.6\times10^{-19}(\mathrm{C})\cdot 600\times10^{-8}\ (\mathrm{cm})}\cdot 0.27\,(\mathrm{V}) = 0.97\times10^{11}\ \mathrm{cm}^{-2} \quad (4\text{-}1)$$

The number of traps that are switching charge state to create the instability observed for a 1,000 s bias stress with a ±1.5 MV/cm gate oxide field applied for the device from Sample Set D shown in Figure 4-9 is calculated to be about 2.0×10^{11} cm^{-2} oxide traps:

$$N_{OT} \cong \frac{C_{OX}}{q}\cdot\Delta V_T = \frac{\varepsilon}{q\cdot t_{OX}}\cdot\Delta V_T$$
$$= \frac{3.9\cdot 8.85\times10^{-14}\ (\mathrm{F/cm})}{1.6\times10^{-19}(\mathrm{C})\cdot 1300\times10^{-8}\ (\mathrm{cm})}\cdot 1.23\,(\mathrm{V}) = 2.04\times10^{11}\ \mathrm{cm}^{-2} \quad (4\text{-}2)$$

The greater number of oxide traps in the older sample may be due to the less sophisticated post-oxidation nitride anneal—using NH_3 instead of NO, the fact that it is a deposited oxide, or simply that the oxidation process was not as optimized.

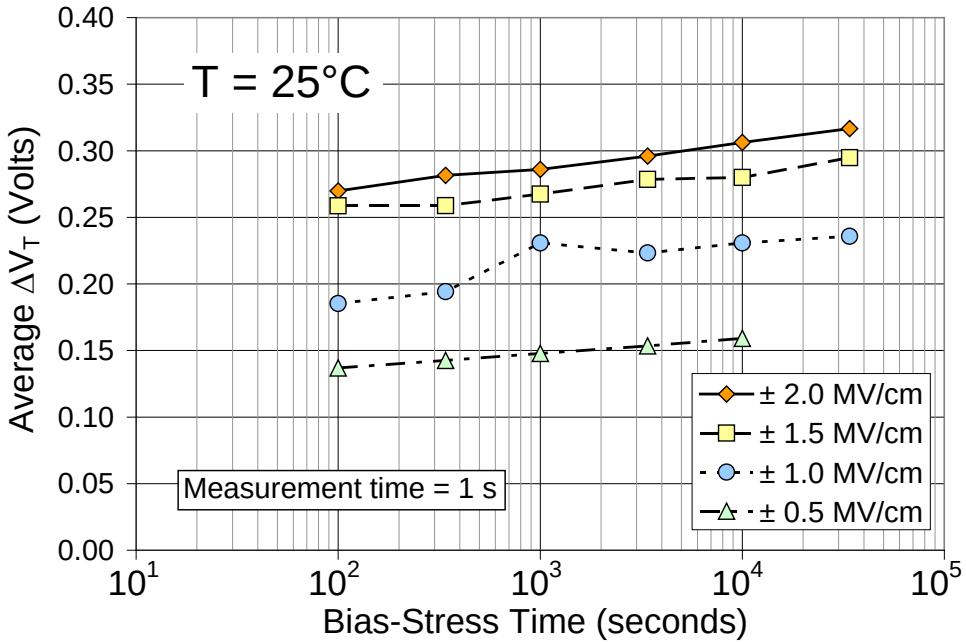

Figure 4-13: Average measured V_T instability of a lateral 4H-SiC MOSFET from Sample Set F with a 60-nm thick thermal oxide with an NO post-oxidation anneal for various bias stresses and times, and 1-s measurement time.

A similar V_T instability of a lateral 4H-SiC MOSFET from Sample Set G with a 50-nm thick thermal oxide with an NO post-oxidation anneal was observed for various bias stresses and times. The ±1.5 MV/cm response should lie somewhere between the ±5 V and ±10 V responses, so that the number of traps that are switching charge state to create the instability observed for a 1,000 s bias stress would be about 1.6×10^{11} cm^{-2} oxide traps:

$$N_{OT} \cong \frac{C_{OX}}{q}\cdot\Delta V_T = \frac{\varepsilon}{q\cdot t_{OX}}\cdot\Delta V_T$$
$$= \frac{3.9\cdot 8.85\times10^{-14}\ (\text{F/cm})}{1.6\times10^{-19}(\text{C})\cdot 500\times10^{-8}\ (\text{cm})}\cdot 0.36\,(\text{V}) = 1.55\times10^{11}\ \text{cm}^{-2} \qquad (4\text{-}3)$$

4.6 Effect of the Post-oxidation NO Anneal on V_T Instability

Figure 4-14 shows the average instability versus gate-bias stress time for several different relative state-of-the-art 4H-SiC MOSFETs from Sample Set G with enclosed geometries and 50-nm thick thermal gate oxides that were thermally grown. The applied bias in each case was ±15 V, and measurement times were about 1 s.

The bottom curve is the response of a control sample that received the standard post-oxidation NO anneal and had an as-grown epi channel. The top curves are the response of a sample that did not receive the post-oxidation anneal. Clearly, the lack of an NO anneal has a strong effect on the magnitude of the V_T instability, resulting in an instability about three times as great. One measurement set was taken out to bias-stress times of 320,000 s, which is over three and-a-half days for each individual bias stress time. Even at these very long times, the magnitude of the instability continues to increase! The total number of oxide traps switching charge state in this case is over 6×10^{11} cm^{-2} oxide traps:

$$N_{OT} \cong \frac{C_{OX}}{q}\cdot\Delta V_T = \frac{\varepsilon}{q\cdot t_{OX}}\cdot\Delta V_T$$
$$= \frac{3.9\cdot 8.85\times10^{-14}\ (\text{F/cm})}{1.6\times10^{-19}(\text{C})\cdot 500\times10^{-8}\ (\text{cm})}\cdot 1.43\,(\text{V}) = 6.17\times10^{11}\ \text{cm}^{-2} \qquad (4\text{-}4)$$

The middle curve is the response of a sample that also received the NO post-oxidation anneal, and whose channel region received an implant to mimic the implanted channel of the DMOSFET (DMOSFET results will be discussed in full in Chapter 7). The result is an instability that is about 33% greater than for the unimplanted sample.

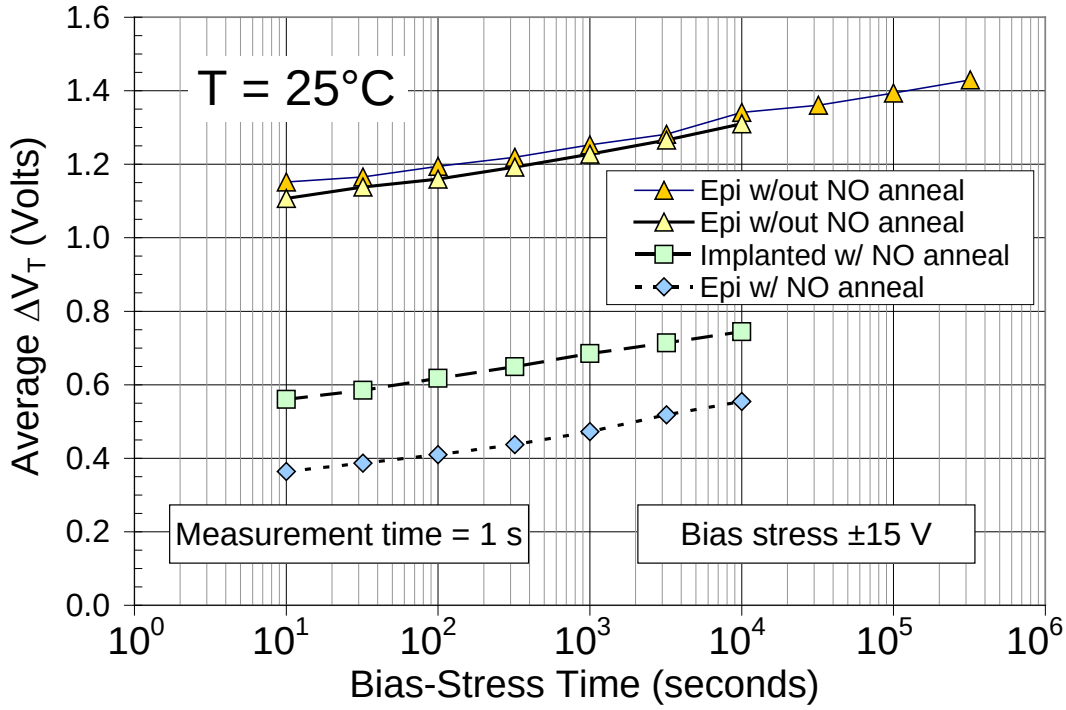

Figure 4-14: Average measured V_T instability of variously processed lateral 4H-SiC MOSFET with 50-nm thick thermal oxides from Sample Set G. The unimplanted device with an NO post-oxidation anneal showed the smallest effect while that without an NO anneal had the largest effect, when stressed with a gate oxide field of ± 3 MV/cm.

The device without the NO anneal had a far larger V_T instability—about three times larger. So the NO anneal decreases the number of switching oxide traps that we observe. This result is consistent with the work of Afanas'ev, et al. [77], who found that the NO anneal reduced the number of slow electron traps that they attributed to defects located in the near-interfacial oxide layer, as well as recent work by Gurfinkel, et al. [106]]. It is interesting to note that previous work on nitrided oxides on Si found that nitridation also appeared to reduce the number of *E'*-type defects [107].

But it is well known that the NO anneal reduces measured interface traps as well [69, 70, 71]. Recent frequency-dependent charge pumping results also indicate that oxide

traps as well as interface traps are reduced by the NO anneal [108]. Interface traps should have a time response in SiC MOSFETs that is faster than that of the measurement times discussed in this work. So the fact that the instability effect increases with increasing stress time indicates that oxide traps are exchanging charge with the SiC. But the tunneling model suggests that those oxide traps which are close to the interface will respond on the same time-scale as the interface traps. It is therefore quite likely that traps near the interface are affecting the interface trap measurements as well. Although it may not make a difference operationally, and it may be impossible to de-convolve the two effects: oxide traps which vary with distance into the oxide and interface traps that vary with energy, there may still be two or more physically distinct defects. For example, recent magnetic resonance studies suggest that the dominant interface trap in 4H-SiC MOSFETs with thermal oxides is a Si vacancy in the SiC near the interface [60, 61]. This is a trap in the SiC, not in the oxide, and is consistent with EELS and TEM results [54, 56].

4.7 One-way instability measurements

In addition to the "back-and-forth" instability measurements described in Section 4.3 and discussed throughout this work, "one-way" instability measurements have also been performed. In this case, the polarity of the gate-bias stress is maintained. For a positive-bias stress as depicted in Figure 4-15, the stress time between measurements increases at a linear-with-log-time rate, and the gate bias is always swept down. (For a one-way negative-bias stress sequence, all the measurements would be made with the gate bias always swept up.)

Figure 4-15 shows how following a long-term negative gate-bias stress of 10^5 s, a 10-s positive gate-bias stress results in a significant shift to the right. Subsequent positive gate-bias stresses result in a further linear-with-log-time shift to the right. This linear-with-log-time shift is explicitly shown in Figure 4-16.

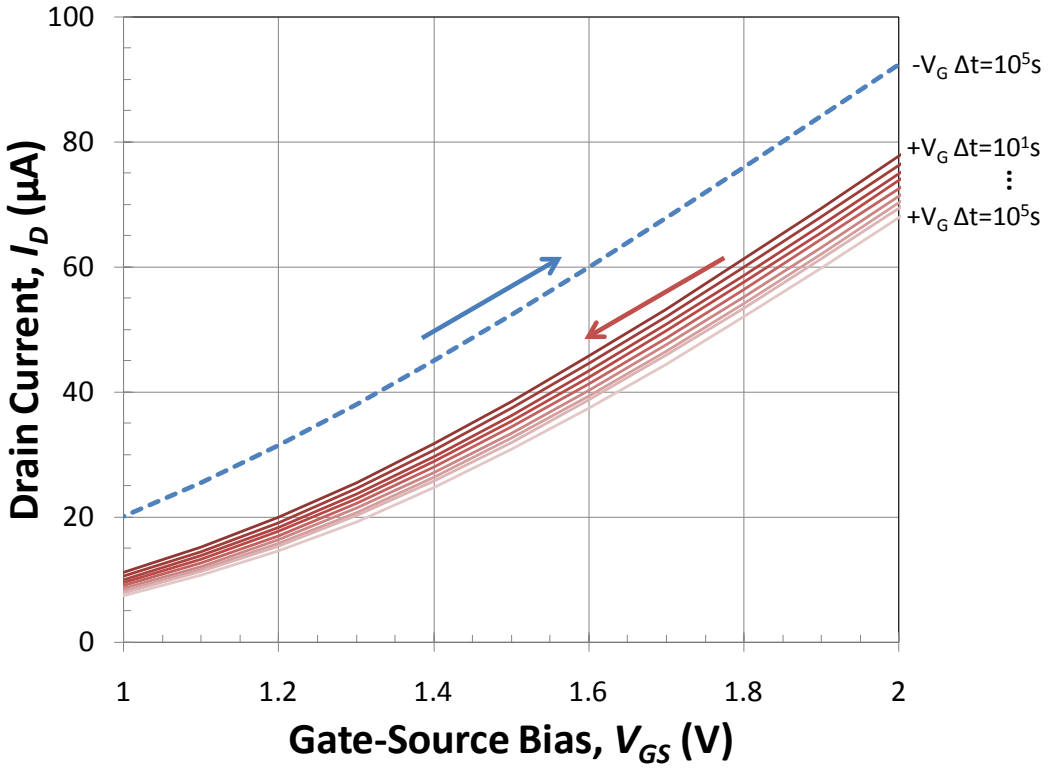

Figure 4-15: I_D-V_{GS} characteristics depicting a one-way V_T instability of a lateral 4H-SiC MOSFET with 50-nm thick thermal oxide and post-oxidation NO anneal from Sample Set G.

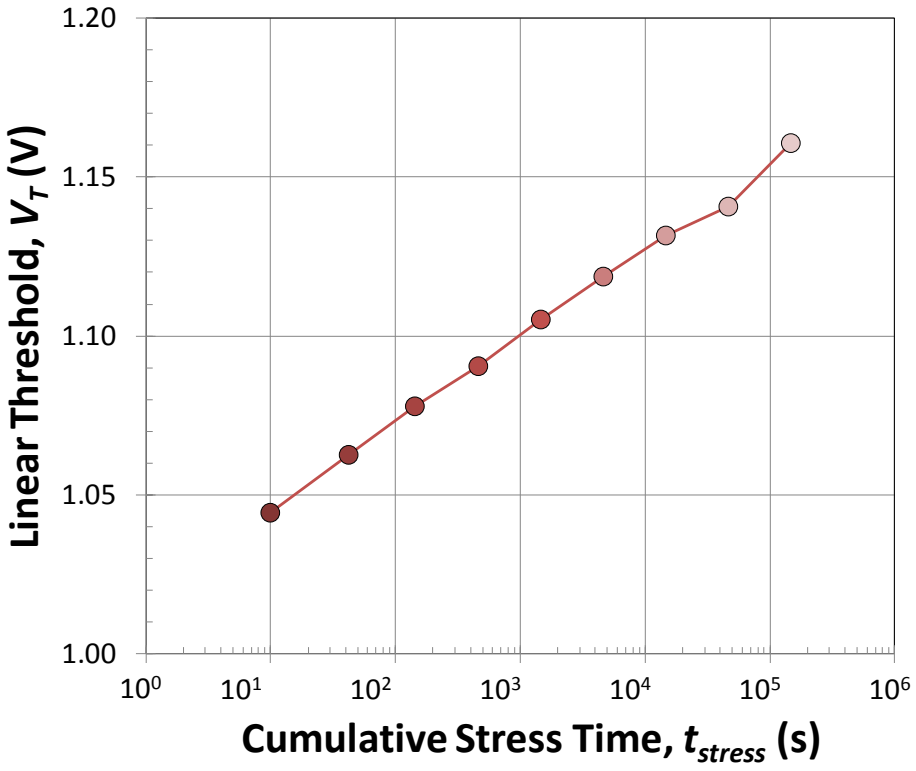

Figure 4-16: Plot of linear-with-log-time one-way V_T instability taken from Figure 4-15 for an *n*-channel MOSFET from Sample Set G.

These results are once again consistent with electrons tunneling to and from near-interfacial oxide traps. The large initial shift is due to many decades of tunneling compressed into the first measurement (see Section 5.2), with the subsequent additional shifts due to the change in oxide trap charge states over a specific oxide depth (see Section 6.2). This linear-with-log-time shift is also observed under negative-bias stress [109] and explains the linear-with-log-time response of the back-and-forth instability measurements.

4.8 Capacitor flatband-voltage instability

The instability in *C-V* characteristics of a *p*-type SiC MOS capacitor with a deposited oxide from Sample Set C, shown in Figure 4-17, illustrates that this instability effect is not limited to SiC MOSFETs, implying that inversion carriers are not necessarily required. As expected, a positive-bias stress causes a shift to the right and a negative-bias stress causes a shift to the left. Once again, the direction of the gate sweep during the measurement is determined by the polarity of the bias: sweep down following a positive-bias stress and sweep up following a negative-bias stress.

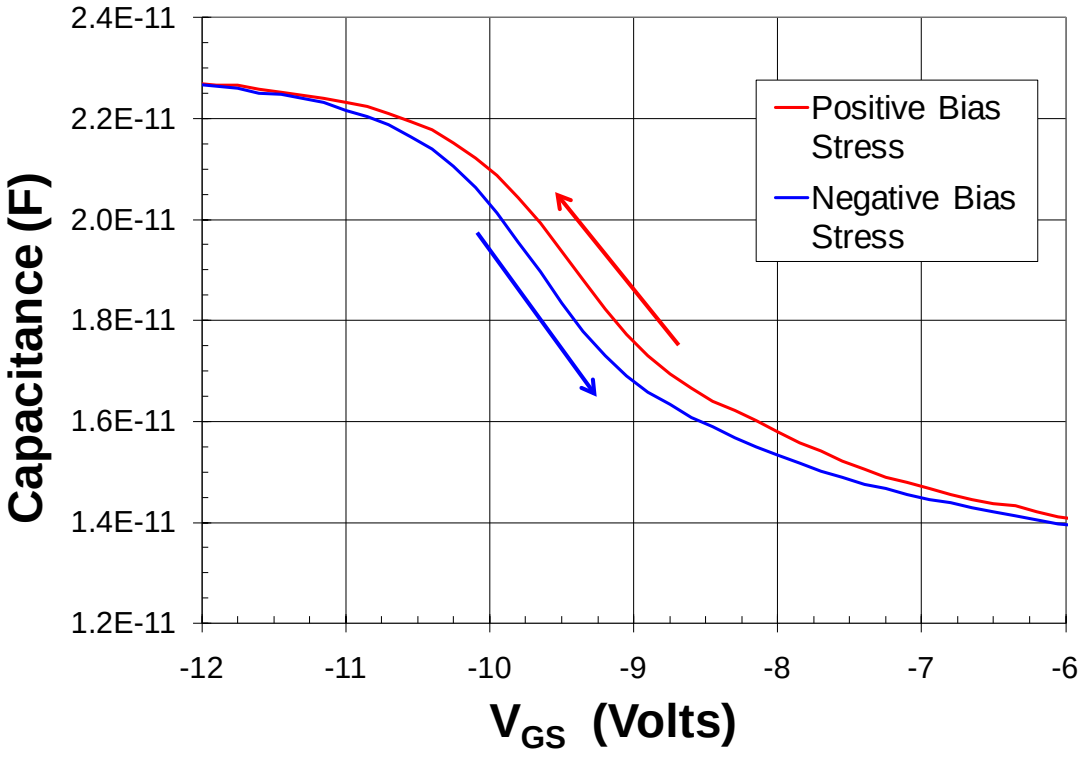

Figure 4-17: Back-and-forth instability in the C-V characteristics of a SiC MOS capacitor from Sample Set C due to back-and-forth gate-bias stressing (–15V and +10 V).

Figure 4-18 shows a comparison of the V_{FB} instability of two different *p*-type SiC MOS capacitors, one from Sample Set B with a thermal oxide and one from Sample Set C with a deposited oxide, versus various gate-bias stress times, again plotted on a log time scale. The capacitors were alternately stressed with +10 V and –15 V. The thermally grown oxides were approximately 60-nm thick and were previously determined to have an oxide trapped charge density of 1×10^{12} cm^{-2} [72]. The 0.6 V instability at 10,000 seconds represents a change in charge of about 2×10^{11} cm^{-2}, or 20 percent of the total "fixed" or oxide trapped charge present—even at room temperature. Interestingly, although the deposited oxide is thicker (around 100 nm), because it experiences a slightly larger shift and the total oxide trapped charge density was found to be only about 0.8×10^{11} cm^{-2}, the fraction of charge responsible for the shift is also about 20 percent in this case.

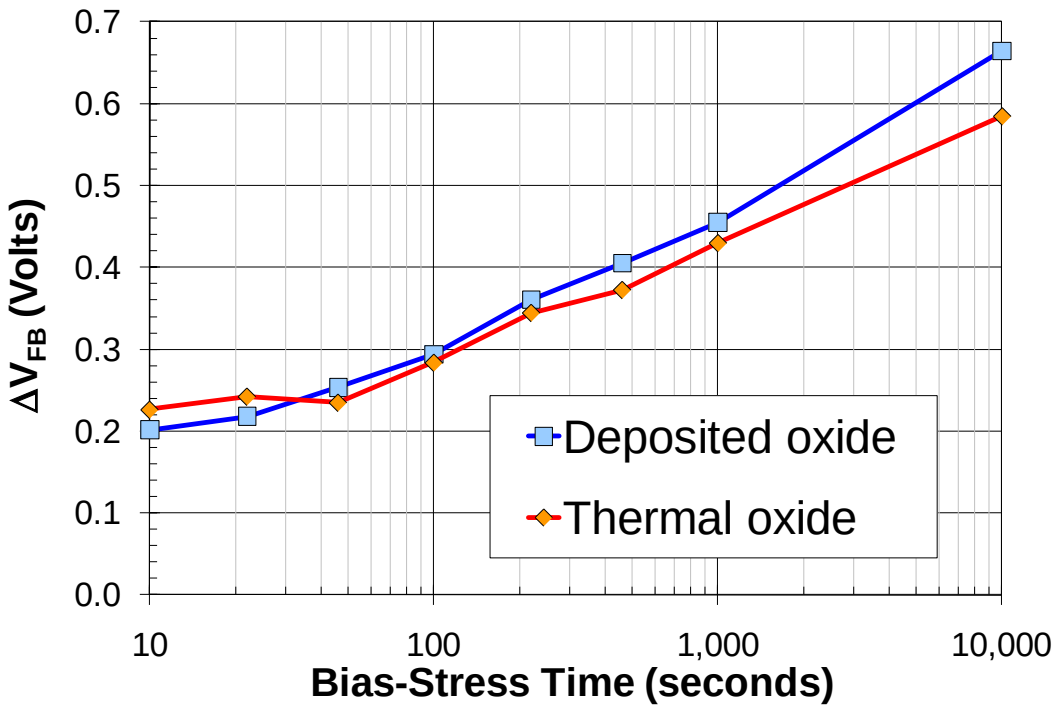

Figure 4-18: Comparison of the change in flat-band capacitance versus log stress time for SiC MOS capacitors with a deposited and thermal oxide with the same bias stress conditions (–15V and +10 V).

Figure 4-19 shows the actual variations in the flat-band voltage due to both positive and negative gate-bias stressing for the *p*-type SiC MOS capacitor with the deposited oxide from Sample Set C whose total back-and-forth instability was shown in Figure 4-18. Clearly, this MOS capacitor is more sensitive to the negative-bias stress. This result is consistent with that of the MOSFET with a deposited oxide whose response is shown in Figure 4-10. Just as Figure 4-11 showed a different response for a thermal oxide, so too the response of a thermal oxide from Sample Set B whose back-and-forth instability is also depicted in Figure 4-18 is different. In this case, there is a rough balance, with each bias polarity contributing approximately half of the shift in flat-band voltage.

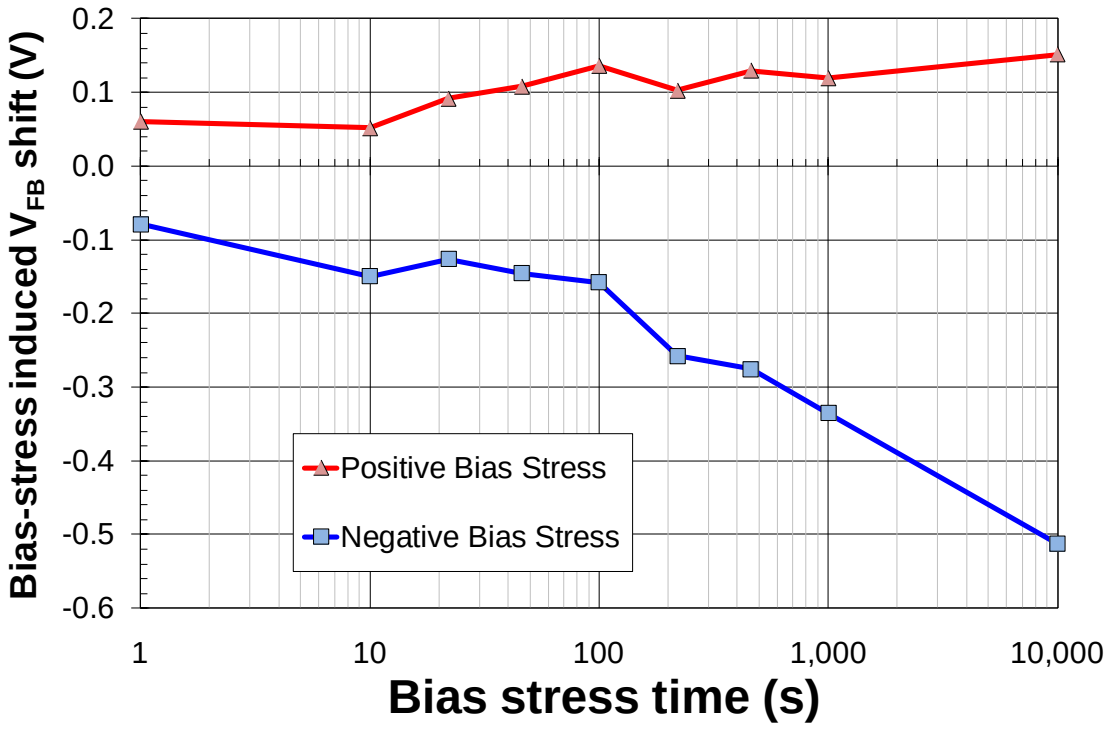

Figure 4-19: Variation in flat-band voltage for a SiC MOS capacitor with a deposited oxide from Sample Set C due to back-and-forth gate-bias stressing (–15V and +10 V).

More recent results by Habersat and Lelis on both *p*-type capacitors and FATFET *n*-channel MOSFETs with thermal gate oxides from Sample Set G exhibit similar instabilities when the source and drain of the MOSFETs are biased slightly positive to the substrate, providing minority carriers to the inversion channel [109]. Although the flat-band instabilities of the FATFETs were about 30 percent greater than that of the MOS capacitors, both of these instabilities are in line with the fast *I-V* and extrapolated V_T instability values presented in Figure 5-5, to be discussed in Chapter 5. They also showed that one-way V_{FB} instability measurements also have a linear-with-log-time response [109].

When comparing one-way V_T and V_{FB} instabilities under both positive and negative gate bias with similar measurement speeds, it was observed that a positive gate-bias stress causes a larger shift in V_T and that a negative gate-bias stress causes a larger shift in V_{FB} (consistent with the results shown in Figure 4-19). This result is also consistent with the notion that the bias applied during the measurement affects that which is measured. V_T is measured with the gate bias slightly positive so that the bias applied during the measurement is of the same polarity as a positive gate-bias stress. Similarly, V_{FB} is measured with the gate bias negative so that the bias applied during this measurement is also of the same polarity as a negative gate-bias stress. To measure V_T following a negative-bias stress or V_{FB} following a positive-bias stress necessarily requires not just a change in bias but a change in polarity as well.

It was further observed by Habersat and Lelis [109] that the NO post-oxidation anneal only had a major effect on V_T under positive-bias stress. The NO anneal did not appear to have any effect on V_{FB} under either bias polarity stress. These results taken together may suggest that the NO anneal affects oxide traps in the upper half of the bandgap and that the flat-band measurements may be measuring traps lower in the bandgap. See Chapter 6 for further discussion of the possible energy levels of these oxide traps.

4.9 Effect of elevated temperature on the V_T instability effect

Figure 4-20 below shows a clean set of V_T instability data for an *n*-channel SiC MOSFET from Sample Set E as a function of temperature for a gate-bias stress time of 180 s and gate bias stress of ± 10 V. This chart shows the threshold voltage determined

using the inversion current method, with the green bar indicating the pre-stress V_T at each temperature, the red bar indicating V_T following a positive-bias stress and the blue bar indicating V_T following a negative-bias stress. (It should be noted that "pre-stress" in this case simply means before bias stresses at that particular temperature. Clearly, the device had been bias stressed previously at lower temperatures. This simply provides context for the back-and-forth instability.) The overall trend in V_T is towards more negative values with increasing temperature, as would be expected due to both the increase in thermal carriers with temperature as well as the filling of fewer negatively charged interface traps at higher temperature. The magnitude of the threshold-voltage instability increases with increasing temperature.

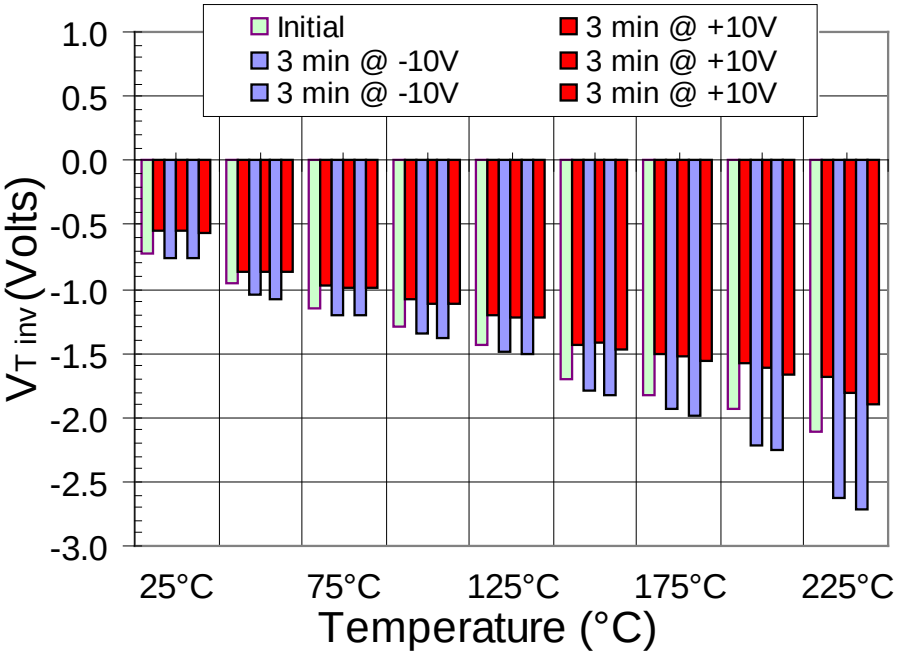

Figure 4-20: Variation of threshold voltage following gate bias stressing as a function of temperature for an enclosed geometry 4H-SiC lateral MOSFET from Sample Set E.

The instability of the I_D-V_{GS} characteristic of a 4H-SiC n-channel MOSFET as a function of temperature is shown in Figure 4-21, for both T = 25 and 200 °C, following the bias and measurement sequence shown in Figure 4-3. For this typical device from Sample Set E, a positive-bias stress caused a positive shift in the threshold voltage and a negative-bias stress caused a negative shift, at both T = 25 and 200 °C. This is the response that we see at room temperature for all the samples, and the effect is very repeatable. Again, it is likely due to charges filling and emptying oxide traps near the SiC interface in response to the bias stress. This result is for one of the four different sample sets studied as a function of temperature (see Figure 4-22) that are fairly representative of the state-of-the-art, processed either from different sources or with variations in the processing (Sample Sets E, F, G, and H). Although the exact details are proprietary, all samples tested had thermal gate oxides with an NO post-oxidation anneal. The main difference appears to be the control of mobile ions in the oxide.

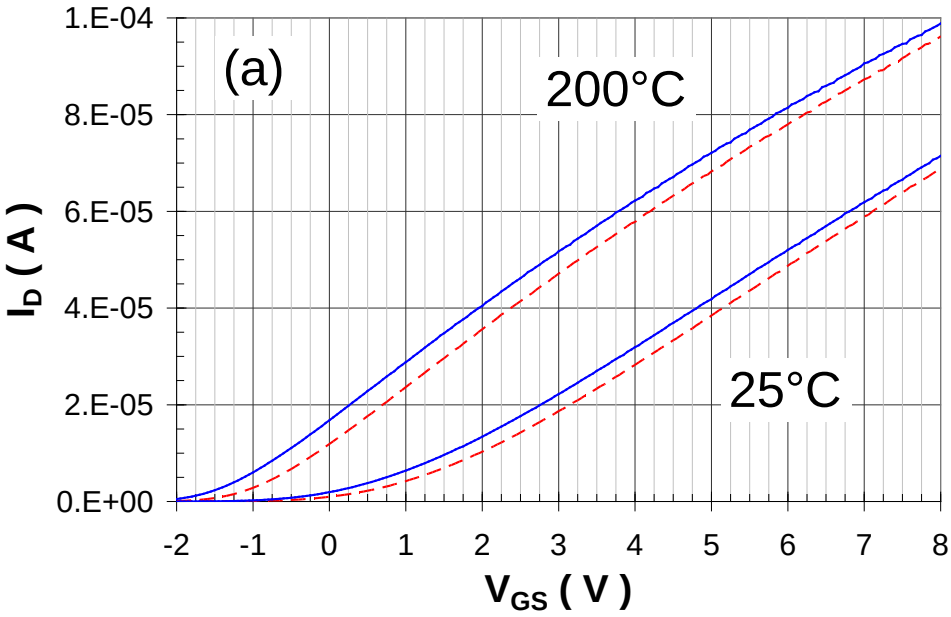

Figure 4-21: Instability of I_D-V_{GS} characteristics at both 25 and 200 °C for Sample Set E following bias stress and measurement sequence shown on the right.

Figure 4-22 shows the average threshold-voltage instability effect as a function of temperature for all four sample sets studied as a function of temperature. In this case, the gate bias stress time was three minutes (180 s), with a gate bias stress that produced an electric field across the gate oxide of about ±2 MV/cm, with the full cycle of stress and measurements (see Figure 4-3) repeated three times and averaged. As can be seen in Figure 4-22, although the room temperature instabilities are fairly consistent ranging from +0.25 to +0.40 V, a wide range of responses is observed at temperatures above 100 °C. The instability increases dramatically above 175 °C for the device from Sample Set E, exceeding 1 V at 225 °C. This response is consistent with that shown in Figure 4-20.

The number of traps that are switching charge state to create the instability observed for Sample Set E vary considerably versus temperature. At room temperature, the number of oxide traps is found to be about 1.5×10^{11} cm^{-2} oxide traps. The number of traps that are switching charge state to create the instability at 225 °C is found to be about 4.2×10^{11} cm^{-2} oxide traps:

$$N_{OT} \cong \frac{C_{OX}}{q}\cdot\Delta V_T = \frac{\varepsilon}{q\cdot t_{OX}}\cdot\Delta V_T$$
$$= \frac{3.9\cdot 8.85\times10^{-14}\ (\mathrm{F/cm})}{1.6\times10^{-19}(\mathrm{C})\cdot 600\times10^{-8}\ (\mathrm{cm})}\cdot 1.15\,(\mathrm{V}) = 4.14\times10^{11}\ \mathrm{cm}^{-2} \qquad (4\text{-}5)$$

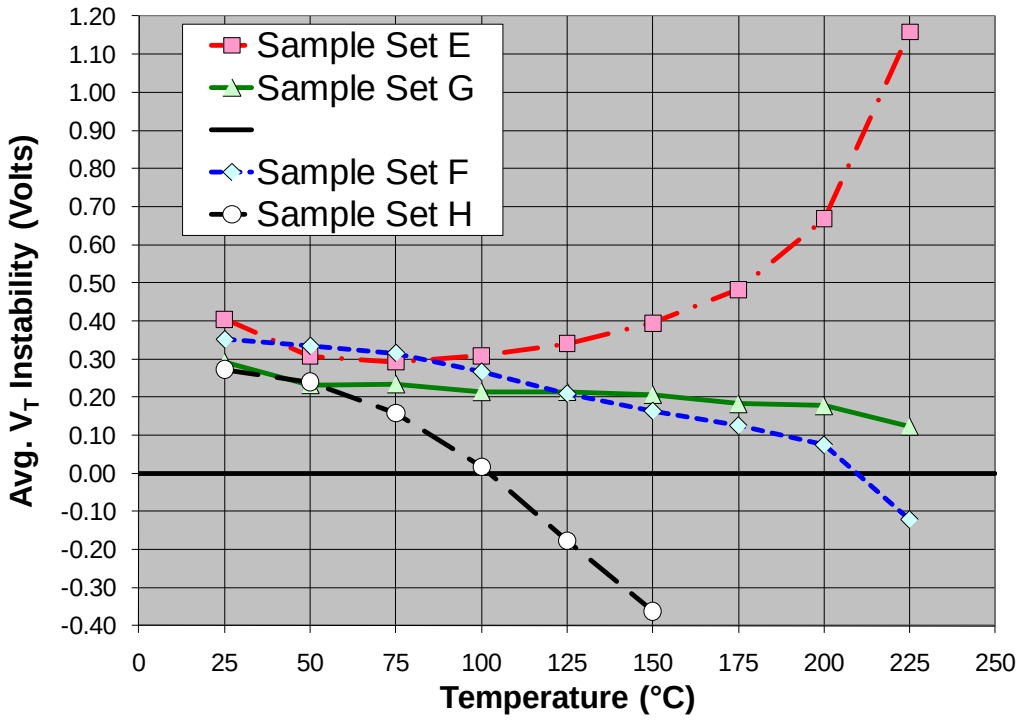

Figure 4-22: Average threshold-voltage instability effect as a function of temperature for several different samples fairly representative of the state-of-the-art. All devices have thermally grown oxides that received a standard post-oxidation NO anneal.

On the other hand, the response becomes negative for the device from Sample Set F above 200 °C. This response is even more dramatic in the case of the device from Sample Set H, where the V_T instability effect becomes negative above 100 °C. The number of traps that are switching charge state to create the instability observed for Sample Set H at room temperature is found to be about 1.2×10^{11} cm^{-2} oxide traps. This is on the low end of the range typically calculated from room-temperature gate-bias stressing. The negative V_T shift at 150 °C will not, by itself, give any sensible numbers for the number of traps that are switching charge state since clearly a second mechanism is at play.

Figure 4-23 shows the instability of the I_D-V_{GS} characteristic for a typical device from Sample Set H at both 25 and 150 °C. At 150 °C, the *I-V* curves shift in the opposite direction, moving more negative following a positive-bias stress and moving more positive following a negative-bias stress.

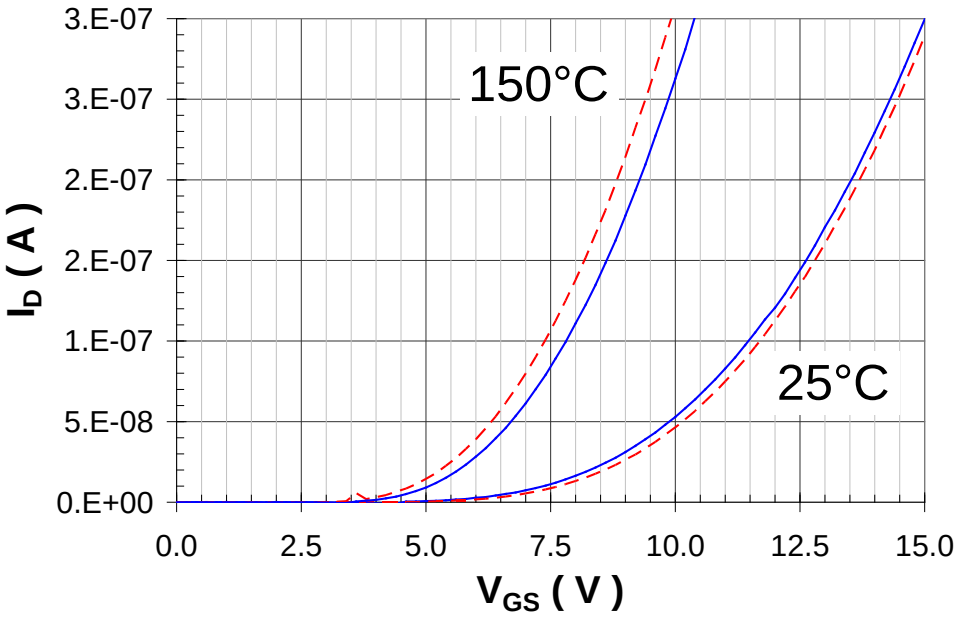

Figure 4-23: Instability of I_D-V_{GS} characteristics at both 25 and 150 °C for Sample Set H. The response at elevated temperature is the opposite of that at room temperature and is likely due to mobile ion drift.

Figure 4-24 shows the response of the device from Sample Set F in more detail, showing the average instability not only as a function of temperature, but of different bias-stress times as well. Not surprisingly, the longer the bias-stress time, the more exaggerated the V_T instability effect. It is important to note that the results shown in Figure 4-22 are for a stress time of 180 s. It is not until longer stress times that the full effect at 200 °C is observed. This effect is explored further in Chapter 7 on the DMOSFETs.

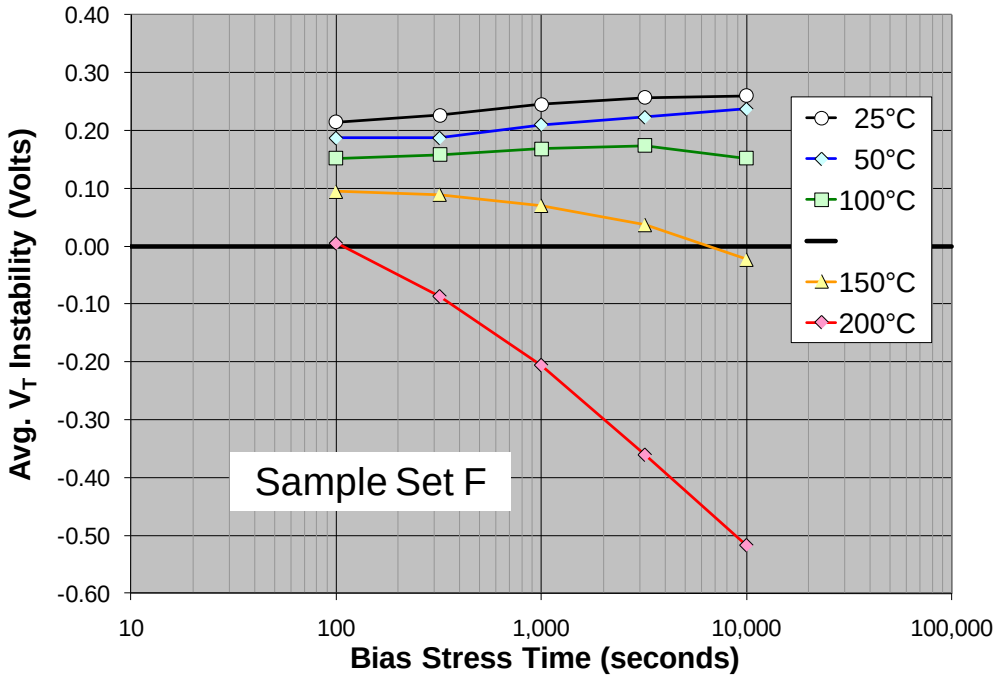

Figure 4-24: Avg. instability of Sample Set F as a function of temperature and bias-stress time.

Since a positive average shift is consistent with charge tunneling into and out of near-interfacial oxide traps, the observation of a negative average shift indicates the presence of a different mechanism. The effect of this mechanism is consistent with mobile ions moving in the oxide in response to the applied gate bias stresses. The two mechanisms are shown in Figure 4-25. The left side of the figure shows the case of a positive gate bias. Electrons are likely to fill traps and/or holes are likely to be emitted, in each case leading to a positive shift in V_T. On the other hand, positively charged mobile ions will drift towards the SiC interface and negatively charged mobile ions will drift towards the gate electrode. In each case the result is a negative shift in V_T, according to (3-47). Since interfacial charge trapping will lead to an increase in net negative charge at the SiC/SiO_2 interface and mobile ion drift will lead to an increase in net positive charge near the interface, it is clear that the two mechanisms will have opposite effects on

the threshold-voltage instability. It is useful to note that the presence of mobile ions in some oxides has also been reported in the literature [44].

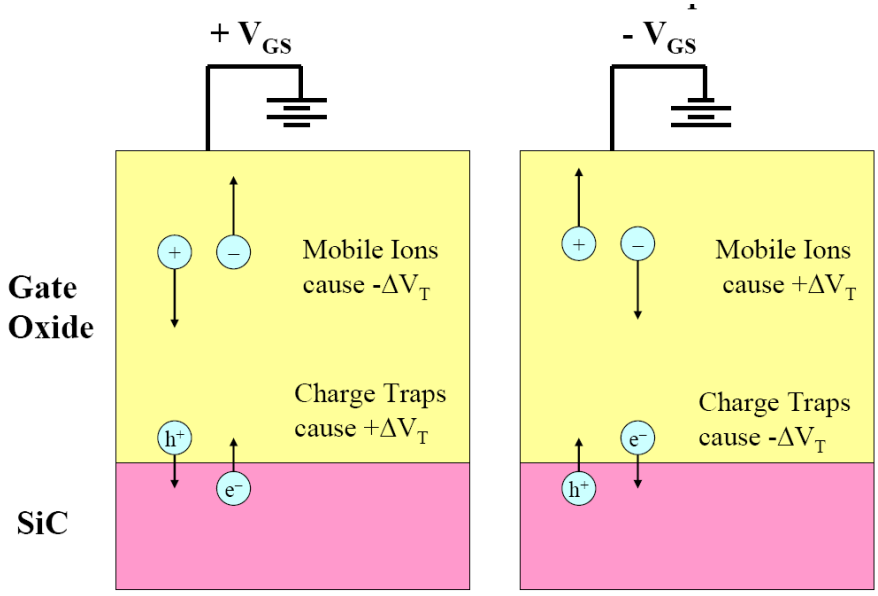

Figure 4-25: Schematic demonstrating the opposing effects of bias stress on charge traps and mobile ions. For example, a positive gate-bias stress will cause a positive shift in the threshold voltage due to interfacial charge trapping, but will cause a negative shift in V_T due to mobile ion drift.

The large non-linear with-log-time V_T instability response as a function of temperature for devices from Sample Set E shown in Figure 4-20 and Figure 4-22, which show an exponential increase in instability with increasing temperature, suggest the presence of a third mechanism, since a direct tunneling process is not expected to have a strong temperature dependence. Although this may involve thermal de-trapping [110, 111], this mechanism cannot by itself explain the back-and-forth instability observed. It is likely that this increase in instability is also due, and maybe primarily due, to an increase in the number of active oxide traps, as discussed both in Chapter 2 in terms of the observed increase in *E′* centers (the only oxide defect observed in SiC MOS

structures) in Si MOS structures with increasing temperature [96], and in Chapter 7 in terms of explaining similar observed increases in V_T instability in similarly processed SiC power MOSFETs [51].

The slight decrease in V_T instability for the device from Sample Set E in Figure 4-22 between 25 and 100 °C may be due to the decrease in the number of filled interface traps at higher temperatures, if a two step tunneling mechanism involving interface traps exists—as discussed in Chapter 6. As mentioned above, the results above 100 °C wherein the instability once again increases can be explained by an increase in the number of active oxide traps.

Although the device from Sample Set G in Figure 4-22 appears to have an ideal response, it quite possible that this is achieved by a delicate balancing of the movement of mobile ions and the filling and emptying of near-interfacial oxide traps. If this is so, then it is of great importance to find charge separation methods such that it can be determined whether both types of defects exist so that both types of defects can be reduced. This is equivalent to stating that further improved testing methods are required to ensure reliable SiC MOSFET device operation (see Section 7.7 for a discussion of reliability testing of SiC power MOSFETs).

4.10 Summary

The basic experimental results of the threshold-voltage instability effect in SiC MOSFETs have been presented. It has been observed that a positive gate-bias stress causes a V_T shift to the right, a negative gate-bias stress causes a V_T shift back to the left, and that this effect is repeatable.

The longer the bias stress time, the larger the instability observed, and the increase proceeds at a linear-with-log-time rate. This result is consistent with electrons tunneling in and out of near-interfacial oxide traps that are distributed relatively uniformly with distance into the oxide (over the range that this can be measured). Linear-with-log-time responses are observed not only in the "back-and-forth" instability, but also "one-way" instability measurements under both positive and negative bias. Standard-room temperature gate-bias stressed V_T-instability results yield switching oxide-trap densities of 1×10^{11} to 2.5×10^{11} cm^{-2}.

The direction of the gate sweep during the measurement is important. Sweeping up in gate voltage (from negative or zero volts up to a positive bias) results in a smaller observed V_T shift than when sweeping down following a positive-bias stress. This is explained by the notion that the bias applied during the measurement also affects the charge occupation of these near-interfacial oxide traps.

Larger gate biases lead to larger shifts, although this effect is sub-linear. Modern devices with thermal gate oxides tend to be more sensitive to the magnitude of the positive gate bias. Older devices with deposited oxides showed greater sensitivity to the magnitude of the negative bias.

MOS capacitors and large-area MOSFETs measured as capacitors show similar flat-band voltage instabilities. The V_{FB} instability is significantly larger under one-way negative gate-bias stress sequences, whereas the V_T instability is significantly larger under one-way positive gate-bias stress sequences. However, the overall V_{FB} instability is larger than the V_T instability, at least when measured with a ramp speed of around 1-10 s. Chapter 5 will show how faster measurements reveal a much larger V_T instability.

A post-oxidation NO anneal significantly reduces the amount of V_T instability, although only due to positive-bias stress. SiC MOSFETs that did not receive the standard post-oxidation NO anneal have a much larger V_T instability, with switching oxide-trap densities as large as 6×10^{11} calculated with standard 1-s measurement speeds. The NO anneal does not affect V_{FB} instability. These results may indicate the presence of two distinct energy levels for the oxide traps, with the NO anneal only affecting the traps near the conduction band edge. This result is very similar to that observed for interface traps, and may be another indication of the difficulty of separating out the effects of oxide traps and interface traps for very fast measurements.

Various responses in V_T instability were observed with increasing temperature. Some devices exhibited an exponential increase in the V_T instability with increasing temperature, especially at long bias-stress times. One possible explanation for this is the activation of additional oxide traps above 100 °C. Switching oxide-trap densities as large as 4×10^{11} were calculated for measurement speeds of around 1 s.

A few, older devices exhibited a large shift in the opposite direction with increasing temperature, shifting to the left following a positive-bias stress and to the right following a negative-bias stress. This type of instability is almost surely due to the presence of mobile ions in the gate oxide.

Some devices show a relatively flat response with temperature. This may either indicate improved gate-oxide processing techniques, or simply an uneasy balance of charge trapping and mobile ion effects. It is important to perform charge separation techniques to either verify the improved oxide processing or to monitor the densities of both types of defects.

5 Measurement Time Dependence, Subthreshold Swing Analysis, and Charge Separation

5.1 Introduction

This chapter discusses the critical issue of the speed of the I_D-V_{GS} measurement, which is necessarily performed to determine the effect of the gate-bias stress. The measurement time matters since a bias is necessarily applied during the measurement. The slower the measurement, the longer the time during which a bias, different than that of the stress itself, is able to affect the charge states of the near-interfacial oxide traps.

It turns out that the speed of the measurement also determines whether and to what extent the subthreshold swing differs between a measurement wherein the gate is swept up following a negative-bias stress or swept down following a positive-bias stress. Again, this is because during slower measurements, the oxide traps can noticeably change charge state, contributing to the stretch-out of the subthreshold I_D-V_{GS} characteristic.

A calculation of a more accurate lower bound for the number of active oxide traps can then applied to the key question of determining the composition of the various types of interfacial charge that cause a shift in V_T both from its theoretical ideal value, as well as during a bias stress and measurement. The implications of a time-varying oxide trap component are discussed.

5.2 Effect of measurement speed on the observed threshold-voltage instability due to gate-bias stress

Figure 5-1 shows a linear-with-log-stress-time extrapolation of bias-stress induced threshold-voltage instability data versus individual stress times to early times and zero instability for a 4H-SiC n-channel MOSFET with a 130 nm-thick deposited gate oxide. (The relatively thick gate oxide for this sample leads to a significant amplification of the measured instability, as (3-33) implies. Thinner gate oxides have correspondingly smaller V_T instabilities.) The full measurement sequence depicted in Figure 4-3 was repeated three times for each stress time and bias plotted versus the average V_T instability. The measurement sweeps took about 1 s and the individual stress times varied from 10 to 100,000 s. A subset of the data from Figure 4-9 is shown for gate bias stresses of ±5 V, ±10 V, and ±20 V, which correspond to electric fields with a magnitude of about 0.4, 0.8, and 1.5 MV/cm, respectively. When fitting a straight line to the instability data versus log time, the results for stresses that lasted less than 100 seconds were omitted, since the measurement times in this case were not much faster than the stress times, clearly affecting the result. One outlier data point for both the ±10 V and ±20V curves was omitted as well.

Extrapolating the data in Figure 5-1 to early stress times predicts that we would have to reduce the stress time to less than 10 ps in order not to see any instability effect. These results are consistent with electrons directly tunneling into and out of oxide traps spatially distributed into the oxide from the SiC/SiO_2 interface. It is interesting to note that in irradiated Si MOS devices with a similar oxide thickness, a similar instability or “reversibility” was observed, as discussed in Chapter 2 [88]. In that case a "tunneling

front," wherein those traps in its wake have been either filled or emptied depending on the field and those beyond it yet unaffected, was determined to move at the rate of about two angstroms per decade of time into the oxide, with the first transitions occurring at about 0.1 ps, giving rise to the linear-with-log-time behavior for a uniform trap distribution [112, 113]. Electron tunneling to so-called E' centers (a broken Si-Si bond due to an oxygen vacancy) in the oxide was determined to be the dominant mechanism in that case [89, 93, 98]. The oxide trap in SiC MOS may well be due to more than one type of defect. Some traps could be associated with C in the transition region that may extend 5 nm or more into the oxide. Some of the oxide traps may be associated with the nitrogen introduced during the post-oxidation NO anneal. However, the only trap definitely identified in SiC is an E'-center type defect [61].

In order to extrapolate to zero instability, the data in Figure 5-1 were extrapolated over twelve decades of time. It is quite remarkable that the three different bias-stress extrapolations all meet within one decade of time—between 1 and 10 ps. Furthermore, it is very suggestive that the extrapolated zero instability times are very close to the initial tunneling transition times of 0.1 ps mentioned above for Si MOS. If this tunneling model to spatially distributed oxide traps is correct for SiC MOS, then Figure 5-1 implies that oxide traps extend at least 36 Å into the oxide from the Si interface, assuming that the tunneling front of 2 Å per decade of time for Si MOS applies to SiC MOS as well, which is reasonable. This distance is compatible with the oxide transition layers or regions for SiC MOS, which are believed to be at least 3-5 nm thick [56, 57, 59]. Figure 5-1 and the tunneling model also suggest that if bias-stress times on the order of microseconds could be applied along with equally fast measurements, then half the V_T instability effect

observed for the very long bias stress times of Figure 5-1 would occur in these extremely short times.

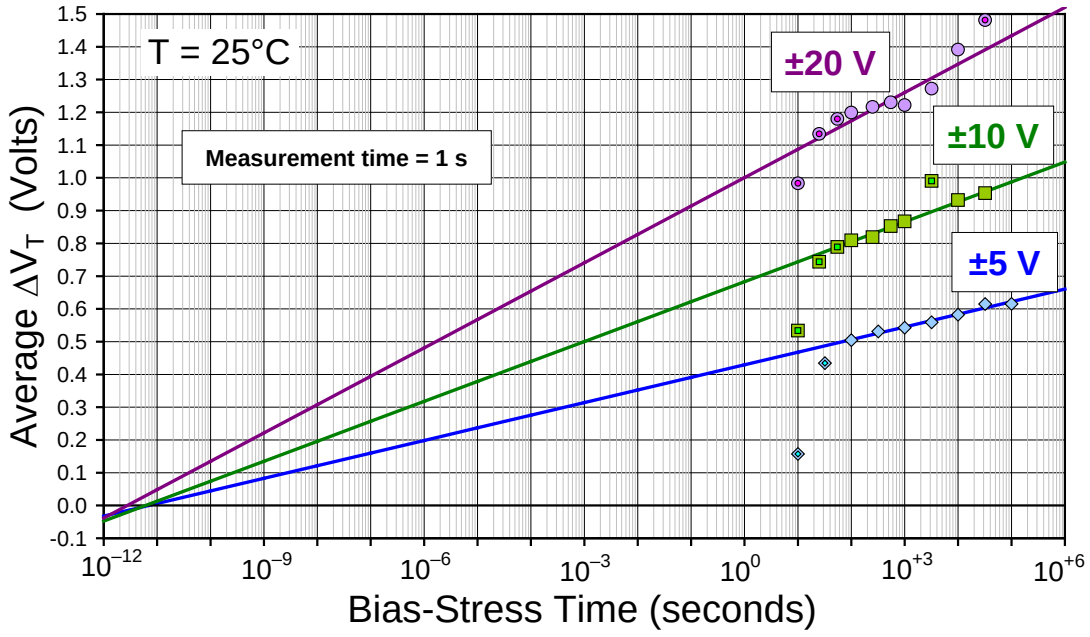

Figure 5-1: Linear-with-log-stress-time extrapolation of the bias stress-induced threshold-voltage instability data versus individual stress times to early times and zero instability of a lateral 4H-SiC MOSFET from Sample Set D with a 130-nm thick deposited gate oxide with a nitrogen anneal. Selective data from Figure 4-9 was used.

This raises the question of the importance of the measurement ramp speed. It was already mentioned above that data for stress times that were close in magnitude to the measurement times were discarded since the measured instability fell dramatically away. The reason for this fall-off is likely that the gate bias applied during the measurement is in effect applying a new stress bias. The slower the gate bias ramp is, the longer that this effective additional bias stress is applied. This would not be terribly significant if the measurement bias was such that it reinforced the stress bias. However, for some portion of the gate sweep the measurement bias will oppose the stress bias. Given that significant

shifts in V_T can occur in very short times, we would therefore expect that varying the measurement time will significantly affect the results. Consider the following thought experiment. Suppose that following the stress bias, an infinitely fast gate sweep could be applied—or at least one that was faster than the first tunneling transition times of 0.1 to 10 ps. In this case, the full effect of the bias stress on V_T would be seen. On the other extreme, suppose that following the stress bias, an infinitely slow gate sweep was applied instead. In this case, the effect of the stress bias would be negligible and only the steady state value for each bias stress along the gate-bias sweep would be measured. In this case, no instability would ever be measured. These results lie in between these two extreme cases, and the faster that the measurement can be made, the more of the effect of the bias stress will be observed.

To verify this, I, along with my colleagues at ARL and NIST at my behest, performed the following set of experiments on the same relatively state-of-the-art 4H-SiC lateral n-channel MOSFETs, mentioned with regard to the *I-V* curves of Figure 4-13, which had a thermal gate oxide and a standard post-oxidation nitrogen anneal using NO.

First, bias stresses were applied for long times and the V_T instability was measured using the Agilent 4155. The average threshold-voltage instability for various bias-stress times and gate oxide fields is shown in Figure 4-13. Once again a linear-with-log-stress-time response of the V_T instability with applied bias is observed, consistent with electrons tunneling from the SiC into oxide traps that are distributed rather uniformly with distance into the insulator. The longer the bias stress time, the deeper into the oxide the tunneling front can reach. The greater the bias, the more effectively the tunneling process occurs. Under reverse bias, the charge is presumably tunneling out in a

similar manner. The number of traps that are switching charge state to create the instability observed for a 3,400 s bias stress with a ±2 MV/cm gate oxide field applied was found for this sample and measurement to be about 1.2×10^{11} cm^{-2} oxide traps.

Next, to investigate the effect of measurement time, a similar sample was measured at NIST using their fast *I-V* system [76], with measurement times ranging from 1 ms to as quick as 20 μs—much faster than the 1-s measurement time for the data in Figure 4-13. Figure 5-2 shows that the fast *I-V* system measured much greater instabilities, even though the bias stress times were 10 s or less and the applied fields were just over 1 MV/cm (around ±7 V). The 1.5 and 2.0 MV/cm curves from Figure 4-13 are re-plotted for comparison and appear in the lower right of Figure 5-2. Clearly, the gate bias applied during the measurement had an important effect on the result.

Also shown in Figure 5-2, extrapolating the linear-with-log-stress-time V_T -instability response (ignoring stress times that once again are close to the measurement time) back to early stress times suggests that we would have to reduce the stress time to 1 ps or less to not see any instability effect. These extrapolations are consistent with those in Figure 5-1, though the zero instability stress time now varies over about four decades of time instead of just one. On the other hand, extrapolating the 20-μs measurement time data out to longer bias-stress times suggests that the V_T instability would be as great as 1 V for a stress time of 34 ks, which would imply an actual lower bound for N_{OT} of 3.6×10^{11} cm^{-2} oxide traps:

$$N_{OT} = \frac{C_{OX}}{q} \cdot \Delta V_T = \frac{\varepsilon}{q \cdot t_{OX}} \cdot \Delta V_T$$

$$= \frac{3.9 \cdot 8.85 \times 10^{-14}\ (\text{F/cm})}{1.6 \times 10^{-19}\ (\text{C}) \cdot 600 \times 10^{-8}\ (\text{cm})} \cdot 1.0\ (\text{V}) = 3.60 \times 10^{11}\ \text{cm}^{-2} \qquad (5\text{-}1)$$

This is three times the number calculated from the data for the much slower 1-s measurement!

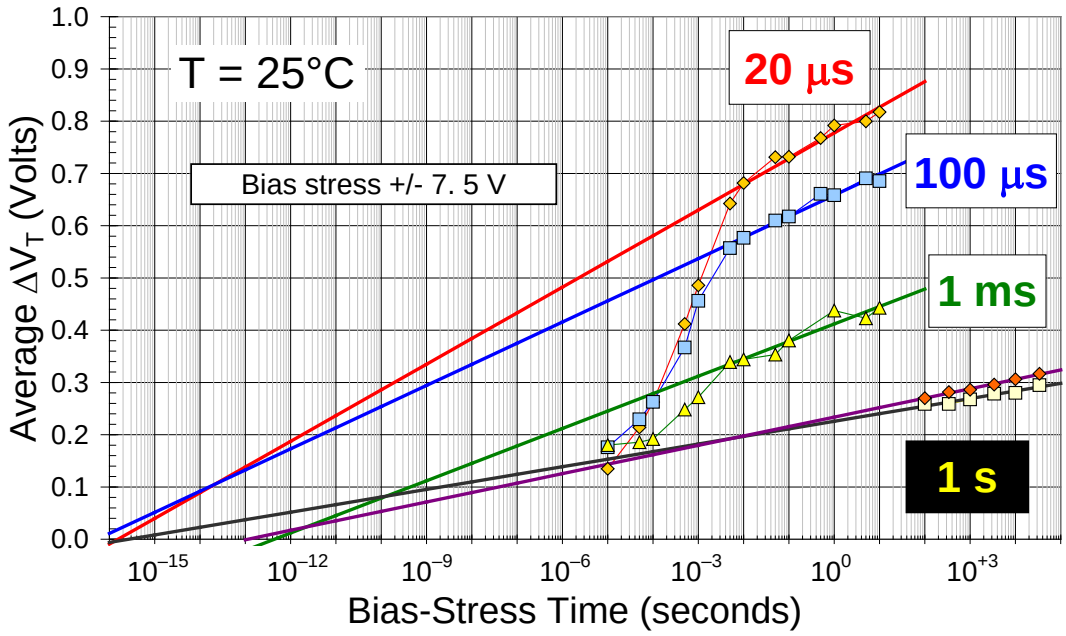

Figure 5-2: Linear-with-log-time extrapolation of the bias stress-induced threshold-voltage instability data to early stress times and zero instability of a lateral 4H-SiC MOSFET from Sample Set F with a 60-nm thick thermal oxide with an NO post-oxidation anneal.

5.3 Stretch-out of the subthreshold I_D-V_{GS} characteristics—a method for determining ΔN_{OT}

Figure 5-3 shows the instability in the subthreshold region of an I_D-V_{GS} characteristic for a 4H-SiC lateral MOSFET, and is in fact a blow-up of the subthreshold

characteristics taken from Figure 4-5. It shows the result of twelve full cycles of biasing, where each cycle consists of first stressing under positive gate bias for 1,000 s at +10 V followed by a measurement sweeping down in gate voltage, and then stressing under negative gate bias at –10 V for an additional 1,000 s followed by a measurement sweeping back up in gate voltage. Although the particular result shown in Figure 5-3 is from a relatively thick 130-nm gate oxide from several years back and does not represent state-of-the-art gate oxides, the large instability in this case clearly demonstrates the basic effect.

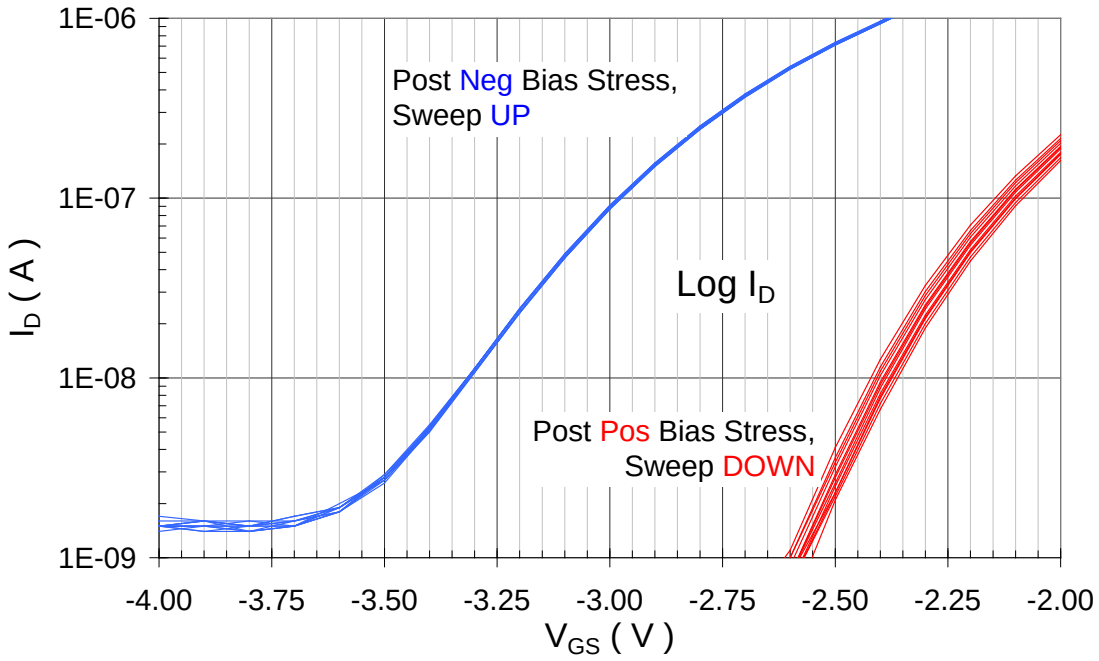

Figure 5-3: Close-up of the subthreshold region of the I_D-V_{GS} characteristic from Figure 4-5 (Sample Set D). Clearly, the curve is more stretched out when sweeping up in gate bias following a negative-bias stress, leading to a greater value of *S*, the subthreshold swing.

It has been found in the course of this analysis of the threshold-voltage instability in as-processed SiC MOSFETs that not only does the I_D-V_{GS} characteristic shift to the

right following a positive-bias stress and back to the left following a negative-bias stress consistent with a change in the number of filled oxide traps [23], but that the slope of the subthreshold *I-V* characteristic is more upright when measured by ramping the gate bias down in voltage following a positive-bias stress than the slope of the subthreshold *I-V* characteristic when ramping the gate bias up in voltage following a negative-bias stress [43, 47, 48, 105] (see Figure 5-3). This is likely due to near-interfacial oxide traps switching charge state during the measurement when a negative gate-bias stress is followed by a positive applied gate bias during the measurement when the surface potential varies from mid-gap to inversion. This implies that part of the effect of the bias-stress instability is mitigated by the measurement itself when comparing the change in voltage required to put the surface potential at inversion:

$$V_{inv\_meas\_down} - V_{inv\_meas\_up} = \frac{q \cdot [\Delta N_{OT\_stress} - \Delta N_{OT\_meas}]}{C_{OX}} \tag{5-2}$$

If instead the subthreshold current is extrapolated down to much lower currents, such as that when the surface potential is at mid-gap, then the change in voltage at that current level should provide a voltage instability value that is closer to that due only to the bias stress without the mitigating effect of the measurement:

$$V_{mg\_meas\_down} - V_{mg\_meas\_up} = \frac{q \cdot \Delta N_{OT\_stress}}{C_{OX}} \tag{5-3}$$

A schematic of this analysis method is shown in Figure 5-4.

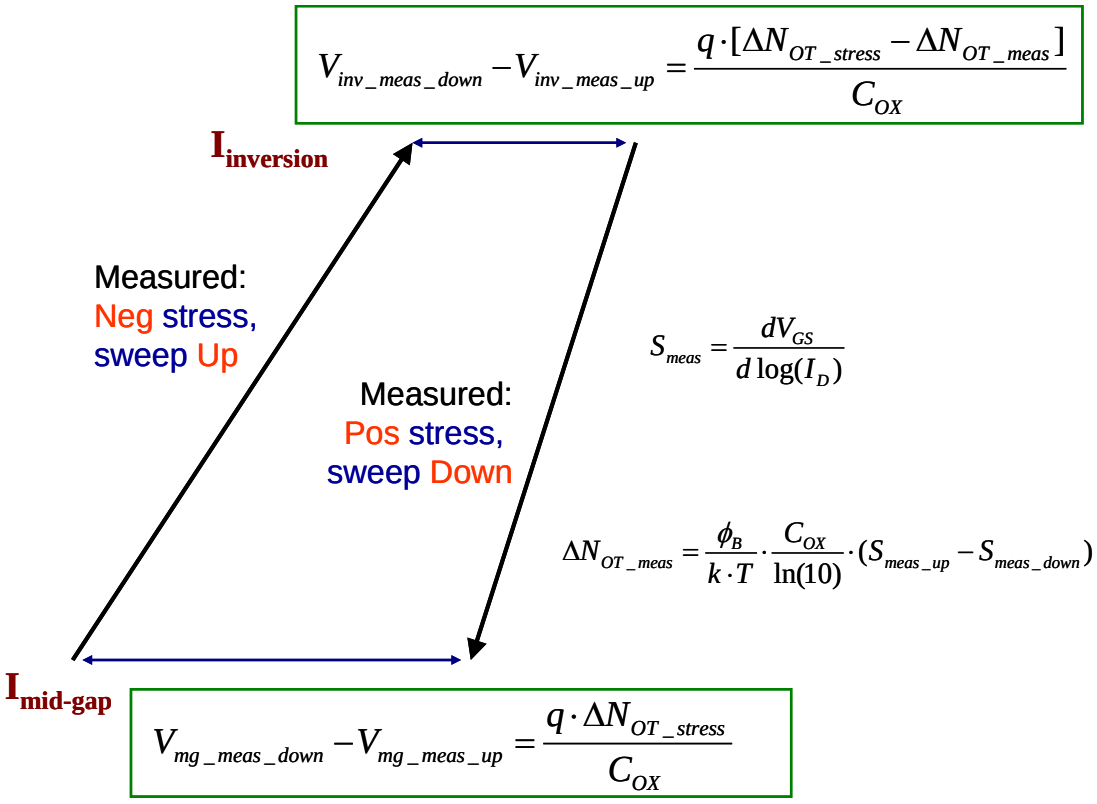

Figure 5-4: Schematic of the subthreshold swing analysis technique, comparing the measured subthreshold swing when the gate is swept up in bias following a negative-bias stress with the subthreshold swing when the gate is swept down in bias following a positive-bias stress.

Thus the analysis of the change in stretch-out of the subthreshold $I_D - V_{GS}$ characteristic can be used to characterize the number of switching oxide traps more directly, providing a larger lower bound for N_{OT}, the number of oxide traps present. This change in slope of the subthreshold *I-V* characteristic following gate-bias stressing is unlikely to be due to a change in the number of active interface traps since this is a low field stress (less than 1 MV/cm) in the case of Figure 5-3. In addition, the effect is very repeatable, and it is highly unlikely that interface traps are being repeatedly activated and passivated at room temperature under these low oxide fields.

Comparing (5-2) and (5-3) indicates that we would expect to see less than the actual number of oxide traps that change charge state due to the bias stress by the number of oxide traps that change charge state during the measurement when considering the change in inversion voltages. The change in the inversion voltage is what has been routinely reported in the literature when discussing the threshold-voltage instability [23]. The fast *I-V* measurements do not allow nearly as much time for changes in the number of occupied oxide traps during the measurement and thus it is reasonable to expect that they would yield values similar to those calculated from the change in mid-gap voltage, with the very important caveat that extrapolations of the slope of the subthreshold *I-V* characteristic are made over twenty orders of magnitude to get down to the theoretical mid-gap current levels for SiC, with few decades of actual data. (It should be noted that the fast *I-V* contains no subthreshold data because of the speed of that measurement.)

Figure 5-5 shows the application of this analysis to the data in Figure 5-2. Variation in the average threshold-voltage instability versus bias-stress time is plotted as a function of measurement time. Clearly, the average instability calculated using the shift in mid-gap voltage with a 1-s measurement is much larger than that calculated using the shift in inversion voltage, and of the same order as that found when measured in tens of microseconds using a fast *I-V* system. It is also clear that this method is not as exact, given the large extrapolations required, and the results using the change in mid-gap voltage are rather noisy. These extrapolated results provide a band or range rather than exact values. But it is striking that at least two-thirds of the actual V_T instability of more than 0.8 V caused by the gate-bias stress is obscured by the counter-shift in voltage that occurs during the slower measurement, just as the direct tunneling model and its linear-

with-log-time response would suggest [112, 113]. The number of switching oxide traps present calculated using either the fast *I-V* measurements or the mid-gap voltage extrapolation method give a much greater lower bound for N_{OT} of 3.6×10^{11} cm^{-2} oxide traps—three times the number calculated using the inversion voltage method.

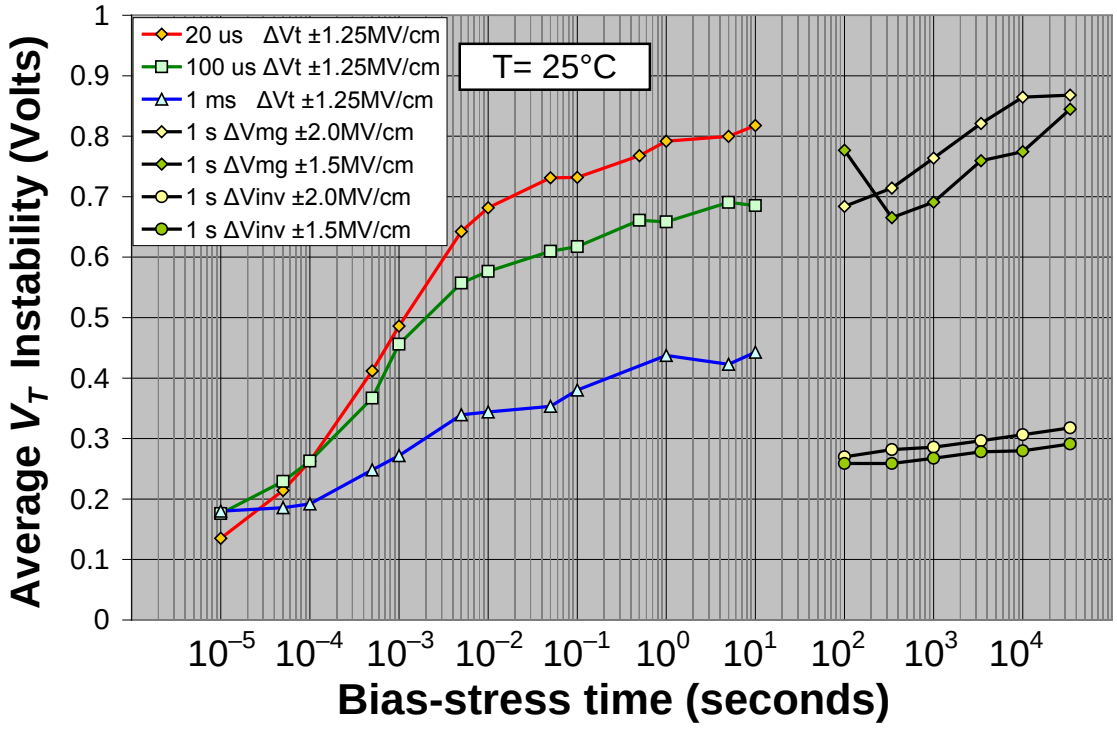

Figure 5-5: Comparison of the effect of measurement time on the calculated instability of the threshold voltage for 4H SiC MOSFETs from Sample Set F with an NO anneal (modification of Figure 5-2). The 1-s measurements (lower right-hand corner) had adequate subthreshold data to calculate the change in mid-gap voltage, which provides a better (and higher) estimate of a lower bound for the number of switching oxide traps, comparable to that from the fast *I-V* measurements.

Figure 5-6 re-plots the data from Figure 4-7 where a 4H SiC MOSFET with a deposited oxide ~1300 Å thick was subjected to twelve full cycles of bias stressing. The

linear and inversion current extraction methods give similar values for V_T, whereas the change in mid-gap voltage indicates a much larger actual instability present. The calculated shifts (using both the mid-gap and inversion voltage methods) are much larger for this sample compared to that in Figure 5-5 because of the much thicker gate oxide, as well as being older and less state-of-the-art. But once again, the change in mid-gap voltage is at least three times as large as the change in inversion voltage commonly used to calculate the V_T instability. However, the uncertainty in the extrapolation based on only a few decades of subthreshold current is also very evident in Figure 5-6 as well.

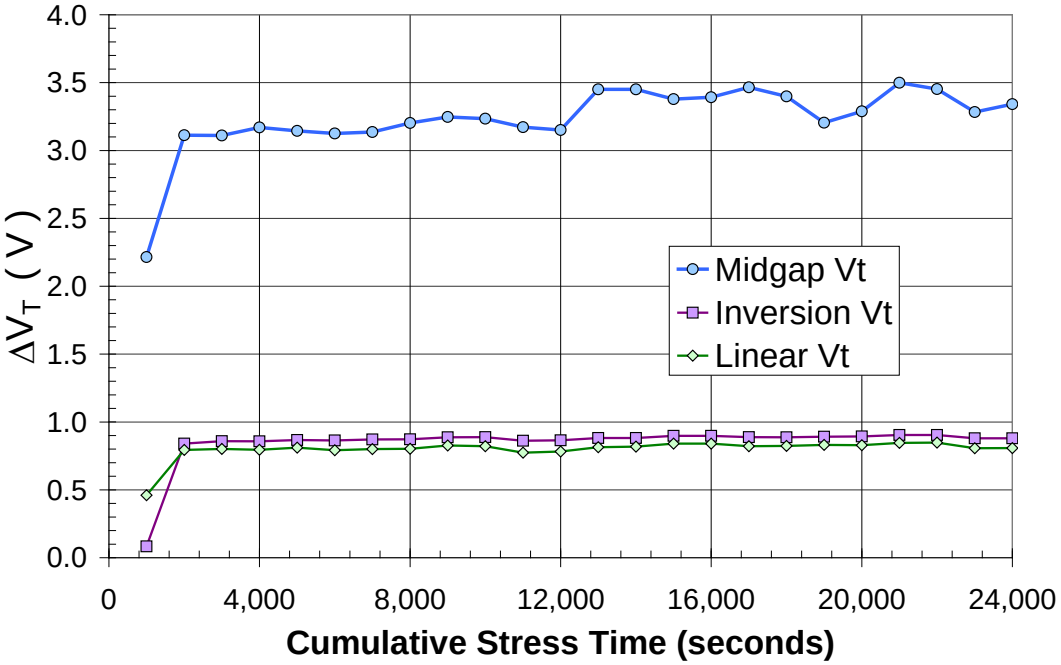

Figure 5-6: Comparison of mid-gap and inversion voltage methods for calculating V_T instability (modification of Figure 4-7 using devices from Sample Set D). Note the noise in the mid-gap calculation due to the large extrapolation.

Figure 5-7 re-plots the change in V_T calculated using the inversion current method shown in Figure 4-6, but with the change in the subthreshold swing, S, added. This figure indicates that following a negative-bias stress and a sweep up in gate voltage, V_T is

observed to shift more negatively and the subthreshold swing value, *S*, increases, which means that the I_D-V_{GS} characteristic is more stretched out. Likewise, following a positive-bias stress and a sweep down in gate voltage, V_T is observed to shift more positively and the subthreshold swing value, *S*, decreases, which means that the I_D-V_{GS} characteristic is more upright. This is consistent with the subthreshold curves of Figure 5-3. Again, this effect is very repeatable.

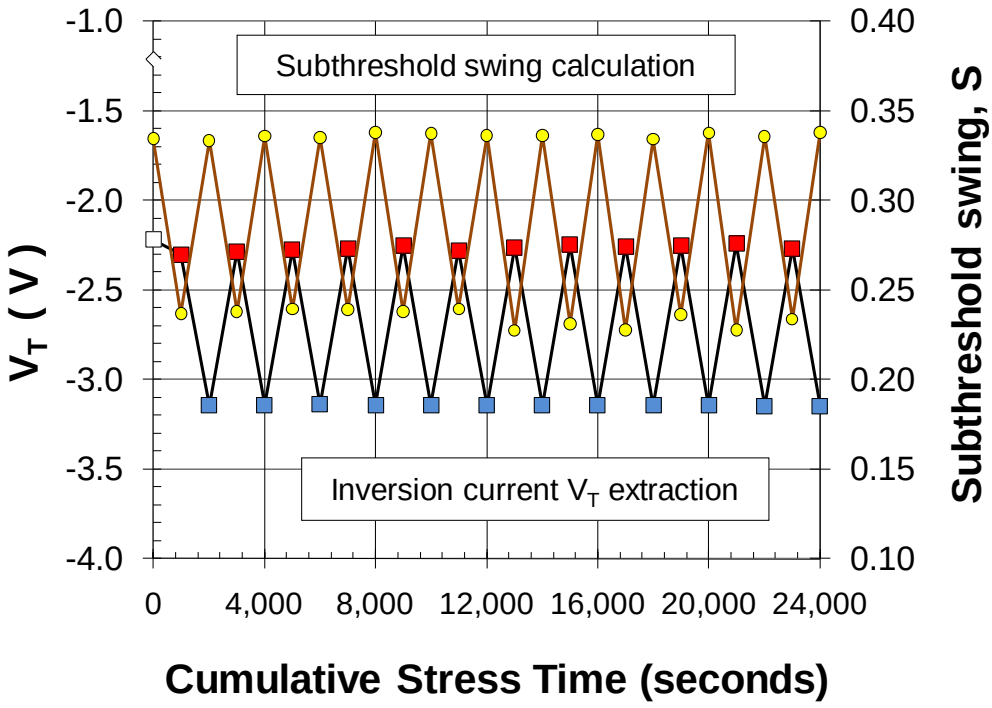

Figure 5-7: Calculated V_T using the inversion current method from Figure 4-6 (Sample Set D), along with the calculated subthreshold swing value, *S*, plotted on the seconday *y*-axis. When V_T shifts more negatively following a negative-bias stress, the subthreshold *I-V* characteristic is also more stretched out (larger *S* value).

Figure 5-8 is a plot of the related changes in charge trap density during the twelve full cycles of bias stress and measurement, calculated from the data of Figure 5-7. The change in oxide trap charge calculated from the change in inversion voltage yields a

value of about 1.5×10^{11} traps per cm^2. The value calculated from the change in mid-gap voltage yields a value in the range of $5.5 \pm 0.3 \times10^{11}$ traps per cm^2. This is because about 4×10^{11} traps per cm^2 are changing charge state during the measurement. Also plotted on this graph is the number of interface traps, using the relationship of (5-35) discussed below in Section 5.4, assuming for the sake of argument that the entire deviation from the ideal subthreshold swing is due to interface traps. The lower set of values for N_{IT} is obtained following a positive-bias stress, when the slope of the subthreshold *I-V* characteristic is more upright. The higher set of values is following a negative-bias stress, when the slope of the subthreshold *I-V* characteristic is more stretched out due to the likely added factor of oxide traps changing charge state. This difference in the set of values for N_{IT} is also seen to be about 4×10^{11} traps per cm^2, as would be expected. This method does not necessarily provide exact values, but may give approximate values that provide some useful information regarding an upper bound for the number of interface traps present since other factors can also contribute to a deviation from the ideal subthreshold swing, including lateral non-uniformities [114]—as well as some oxide traps possibly changing charge state while sweeping down. Regardless, given that the magnitude of the threshold-voltage instability keeps increasing with stress times as great as 3×10^5 s (see Figure 4-14), and that the subthreshold swing changes back and forth depending on the stress and measurement conditions, these are strong arguments that these effects are not due to changes in the number of interface traps but instead are due to oxide traps filling and emptying during both the bias stress and the measurement that follows. Subtracting out the ΔN_{OT} component indicates that the number of interface traps

(the smaller values calculated when sweeping down following a positive-bias stress) are approximately equal in magnitude to the number of switching oxide traps in this case.

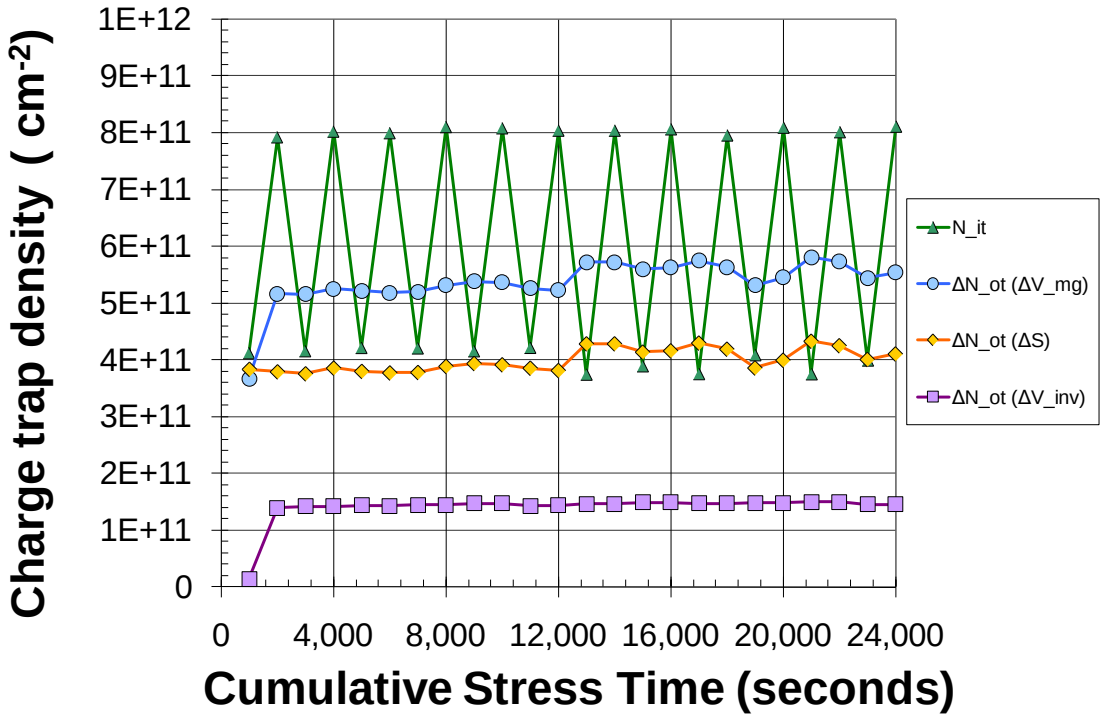

Figure 5-8: Changes in calculated charge trap density when subject to alternating positive and negative gate-bias stresses using the data from Figure 5-7 (Sample Set D). The N_{OT} calculated varies depending on whether the change in inversion voltage or mid-gap voltage is used, and the N_{IT} calculated is distorted by the change in the slope of the *I-V* characteristic due to the change in oxide trap occupation during the measurement.

5.4 Derivation of the subthreshold-swing analysis

This section provides a theoretical justification why the analysis of the subthreshold swing from the subthreshold region of the I_D-V_{GS} characteristic can provide useful insight into the charge trapping effects of SiC MOSFETs. Subthreshold-swing analysis was successfully applied to the analysis of radiation effects in Si MOS a

generation ago [115, 116] and the general concept of the subthreshold swing is briefly discussed in Sze [117].

The subthreshold swing, *S*, can be defined as follows:

$$\frac{1}{S} = \frac{d\log(I_D)}{dV_{GS}} \tag{5-4}$$

which is the inverse of the slope. The subthreshold current is derived in Sze [117]:

$$I_D = \mu_n \cdot \left(\frac{Z}{L}\right) \cdot \frac{\varepsilon_S}{\sqrt{2} \cdot L_D \cdot \beta^2} \cdot \left(\frac{n_i}{N_a}\right)^2 \cdot \left(1 - e^{-\beta \cdot V_{DS}}\right) \cdot e^{\beta \cdot \psi_S} \cdot \frac{1}{\sqrt{\beta \cdot \psi_S}} \tag{5-5}$$

where

$$\beta = \frac{q}{kT} \tag{5-6}$$

μ_n is the electron mobility, Z is the channel width, L is the channel length, and the other terms are as previously defined. The surface potential, ψ_S, is equal to ϕ_B for midgap and $2 \cdot \phi_B$ for inversion. The gate voltage required to put the surface potential at inversion, V_{inv}, is one way to define the threshold voltage (as briefly mentioned in Chapter 4), and the corresponding current can be referred to as the inversion current, I_{inv}. Similarly, the gate voltage required for mid-gap surface potential is the mid-gap voltage, V_{mg}, and the corresponding current is the mid-gap current, I_{mg}. (See Figure 5-9 for a schematic of the subthreshold swing and a summary of the equations derived below.)

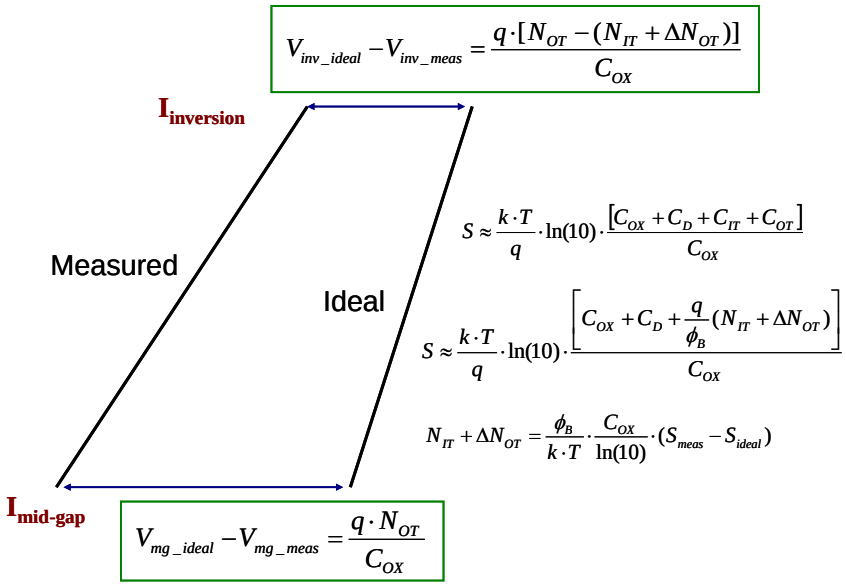

Figure 5-9: Schematic comparing the ideal subthreshold swing with an actual measured subthreshold swing.

Therefore,

$$\frac{1}{S} = \frac{\log(I_{inv}) - \log(I_{mg})}{V_{inv} - V_{mg}} = \log\left(\frac{I_{inv}}{I_{mg}}\right) \cdot \frac{1}{V_{inv} - V_{mg}} \tag{5-7}$$

where I_{inv} and I_{mg} can then be re-written in terms of the subthreshold current expression given in (5-5) so that

$$\log\left(\frac{I_{inv}}{I_{mg}}\right) = \log\left(\frac{\mu_n \cdot \frac{Z}{L} \cdot \frac{\varepsilon_S}{\sqrt{2} \cdot L_D \cdot \beta^2} \cdot \left(\frac{n_i}{N_a}\right)^2 \cdot \left(1 - e^{-\beta \cdot V_{DS}}\right) \cdot e^{\beta \cdot 2 \cdot \phi_B} \cdot \frac{1}{\sqrt{\beta \cdot 2 \cdot \phi_B}}}{\mu_n \cdot \frac{Z}{L} \cdot \frac{\varepsilon_S}{\sqrt{2} \cdot L_D \cdot \beta^2} \cdot \left(\frac{n_i}{N_a}\right)^2 \cdot \left(1 - e^{-\beta \cdot V_{DS}}\right) \cdot e^{\beta \cdot \phi_B} \cdot \frac{1}{\sqrt{\beta \cdot \phi_B}}}\right) \tag{5-8}$$

which simplifies to

$$\log\left(\frac{I_{inv}}{I_{mg}}\right) = \log\left(\frac{e^{\beta \cdot 2 \cdot \phi_B} \cdot \frac{1}{\sqrt{\beta \cdot 2 \cdot \phi_B}}}{e^{\beta \cdot \phi_B} \cdot \frac{1}{\sqrt{\beta \cdot \phi_B}}}\right) = \log\left(\frac{e^{\beta \cdot \phi_B}}{\sqrt{2}}\right) \tag{5-9}$$

so that

$$\frac{1}{S} = \log\left(\frac{I_{inv}}{I_{mg}}\right) \cdot \frac{1}{V_{inv} - V_{mg}} = \log\left(\frac{e^{\beta \cdot \phi_B}}{\sqrt{2}}\right) \cdot \frac{1}{V_{inv} - V_{mg}} \tag{5-10}$$

Written in terms of the natural log, and given that $\beta = \frac{q \cdot \phi_B}{k \cdot T} > 50$ at room temperature,

and is >> $\frac{1}{2} \cdot \ln(2)$, this expression can then be written as:

$$\begin{aligned} \frac{1}{S} &= \frac{1}{\ln(10)} \cdot \ln\left(\frac{e^{\beta \cdot \phi_B}}{\sqrt{2}}\right) \cdot \frac{1}{V_{inv} - V_{mg}} = \frac{1}{\ln(10)} \cdot \left[\ln(e^{\beta \cdot \phi_B}) - \ln(\sqrt{2})\right] \cdot \frac{1}{V_{inv} - V_{mg}} \\ &= \frac{1}{\ln(10)} \cdot \left[\beta \cdot \phi_B - \frac{1}{2}\ln(2)\right] \cdot \frac{1}{V_{inv} - V_{mg}} \approx \frac{\beta \cdot \phi_B}{\ln(10)} \cdot \frac{1}{V_{inv} - V_{mg}} \end{aligned} \tag{5-11}$$

Therefore,

$$S \approx \frac{V_{inv} - V_{mg}}{\left(\frac{q}{k \cdot T} \cdot \phi_B \Big/ \ln(10)\right)} \tag{5-12}$$

The relationship given on p. 447 of Sze [117] for the subthreshold swing is defined in terms of the various capacitances present. For the idealized case of no interfacial trapped charge,

$$S \approx \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left[\frac{C_{OX} + C_D}{C_{OX}}\right] \tag{5-13}$$

where C_D is the depletion capacitance. When interface trap charge is present

$$S \approx \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left[\frac{C_{OX} + C_D + C_{IT}}{C_{OX}}\right] \tag{5-14}$$

In the case of SiC MOSFETs, there is likely an additional component due to changes in the oxide trap charge component with applied bias, leading to an additional capacitive term:

$$S \approx \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left[\frac{C_{OX} + C_D + C_{IT} + C_{OT}}{C_{OX}} \right] \tag{5-15}$$

Since both expressions (5-12) and (5-15) are equal to the subthreshold swing,

$$\frac{V_{inv} - V_{mg}}{\left(\frac{q}{k \cdot T} \cdot \phi_B \Big/ \ln(10) \right)} = \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left[\frac{C_{OX} + C_D + C_{IT} + C_{OT}}{C_{OX}} \right] \tag{5-16}$$

or

$$V_{inv} - V_{mg} = \phi_B \cdot \left[\frac{C_{OX} + C_D + C_{IT} + C_{OT}}{C_{OX}} \right] \tag{5-17}$$

So for the non-idealized case that we can actually measure we can write

$$V_{inv\_meas} - V_{mg\_meas} = \phi_B \cdot \left[\frac{C_{OX} + C_D + C_{IT} + C_{OT}}{C_{OX}} \right] \tag{5-18}$$

and for the idealized case we can write

$$V_{inv\_ideal} - V_{mg\_ideal} = \phi_B \cdot \left[\frac{C_{OX} + C_D}{C_{OX}} \right] \tag{5-19}$$

If we further assume mid-gap interface trap neutrality, such that the interface traps below mid-gap are positively charged when empty and neutral when filled and interface traps above mid-gap are neutral when empty and negatively charged when filled, then when the surface potential is at mid-gap there is no charge contribution from any of the interface traps. This assumption worked very successfully in the analysis of irradiated Si MOSFETs. If this is so for SiC MOSFETs as well, which is not an unreasonable

assumption, then the deviation in the mid-gap voltage from the ideal value is a measure of the total number of oxide traps present. This is not an easy number to pin down since it changes with applied bias and time, as we have shown. Nonetheless, we can write

$$V_{mg\_ideal} - V_{mg\_meas} = \frac{q \cdot N_{OT}}{C_{OX}} \tag{5-20}$$

or

$$V_{mg\_meas} = V_{mg\_ideal} - \frac{q \cdot N_{OT}}{C_{OX}} \tag{5-21}$$

Therefore, (5-18) can be re-written using (5-21) as

$$V_{inv\_meas} = \phi_B \cdot \left[\frac{C_{OX} + C_D + C_{IT} + C_{OT}}{C_{OX}} \right] + V_{mg\_ideal} - \frac{q \cdot N_{OT}}{C_{OX}} \tag{5-22}$$

This can further be re-written using (5-19) and re-arranging terms to get

$$\begin{aligned} V_{inv\_meas} &= \phi_B \cdot \left[\frac{C_{OX} + C_D + C_{IT} + C_{OT}}{C_{OX}} \right] \\ &+ \left\{ V_{inv\_ideal} - \phi_B \cdot \left[\frac{C_{OX} + C_D}{C_{OX}} \right] \right\} - \frac{q \cdot N_{OT}}{C_{OX}} \end{aligned} \tag{5-23}$$

This reduces to

$$V_{inv\_meas} - V_{inv\_ideal} = \phi_B \cdot \left[\frac{C_{IT} + C_{OT}}{C_{OX}} \right] - \frac{q \cdot N_{OT}}{C_{OX}} \tag{5-24}$$

C_{IT} is often defined as $q \cdot D_{IT}$, where N_{IT} is the integral of D_{IT} over the relevant portion of the bandgap (see Section 3.4). Therefore,

$$C_{IT} = q \cdot D_{IT} \cong \frac{q \cdot N_{IT}}{\phi_B} \tag{5-25}$$

Since the cause of the increase of the subthreshold swing, *S*, (equivalent to a stretch-out of the subthreshold portion of the I_D-V_{GS} characteristic) is the action of interface traps being filled, and in the case of SiC MOSFETs of oxide traps being filled as well when sweeping from negative gate bias to positive bias, we can similarly write the capacitance due to oxide traps charging during the gate sweep as

$$C_{OT} = \frac{q \cdot \Delta N_{OT}}{\phi_B} \tag{5-26}$$

Therefore, (5-24) can be re-written as

$$V_{inv\_meas} - V_{inv\_ideal} = \phi_B \cdot \left(\frac{\frac{q \cdot N_{IT}}{\phi_B} + \frac{q \cdot \Delta N_{OT}}{\phi_B}}{C_{OX}} \right) - \frac{q \cdot N_{OT}}{C_{OX}} \tag{5-27}$$

so that the difference between the ideal inversion voltage and the measured value is

$$V_{inv\_ideal} - V_{inv\_meas} = \frac{q \cdot N_{OT}}{C_{OX}} - q \cdot \left[\frac{N_{IT} + \Delta N_{OT}}{C_{OX}} \right] \tag{5-28}$$

In terms of changes in the subthreshold swing, the difference between the measured and ideal values, (5-15) and (5-13) respectively, yields

$$S_{meas} - S_{ideal} = \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left[\frac{C_{IT} + C_{OT}}{C_{OX}} \right] \tag{5-29}$$

or

$$\begin{aligned} S_{meas} - S_{ideal} &= \frac{k \cdot T}{q} \cdot \ln(10) \cdot \left(\frac{\frac{q \cdot N_{IT}}{\phi_B} + \frac{q \cdot \Delta N_{OT}}{\phi_B}}{C_{OX}} \right) \\ &= \frac{k \cdot T}{q \cdot \phi_B} \cdot \ln(10) \cdot \left[\frac{q \cdot (N_{IT} + \Delta N_{OT})}{C_{OX}} \right] \end{aligned} \tag{5-30}$$

The above results are summarized in the schematic shown in Figure 5-9.

If we define S_{meas_up} as the subthreshold swing obtained by sweeping the gate up from negative bias to positive bias following a negative-bias stress, and similarly define S_{meas_down} as the subthreshold swing obtained by sweeping the gate down from positive bias to negative bias following a positive-bias stress, then the difference in these two values yields

$$S_{meas\_up} - S_{meas\_down} = \frac{k \cdot T}{q \cdot \phi_B} \cdot \ln(10) \cdot \left[\frac{q \cdot (\Delta N_{OT\_up} - \Delta N_{OT\_down})}{C_{OX}} \right] \tag{5-31}$$

If we make the further simplifying assumption that there is not much change in the number of oxide traps in the case of S_{meas_down} where the bias is still positive in the subthreshold region following a positive-bias stress, then (5-31) simplifies to

$$S_{meas\_up} - S_{meas\_down} = \frac{k \cdot T}{q \cdot \phi_B} \cdot \ln(10) \cdot \left[\frac{q \cdot (\Delta N_{OT\_up})}{C_{OX}} \right] \tag{5-32}$$

and re-arranging terms yields an expression for the amount of oxide charge changing charge state during the sweep

$$\Delta N_{OT\_meas} = \frac{\phi_B}{k \cdot T} \cdot \frac{C_{OX}}{\ln(10)} \cdot (S_{meas\_up} - S_{meas\_down}) \tag{5-33}$$

This is the expression given in Figure 5-4. Likewise, (5-30) will reduce to

$$S_{meas\_down} - S_{ideal} = \frac{k \cdot T}{q \cdot \phi_B} \cdot \ln(10) \cdot \left[\frac{q \cdot N_{IT}}{C_{OX}} \right] \tag{5-34}$$

when the gate is swept down in voltage, providing a method for calculating the interface trapped charge between mid-gap and inversion

$$N_{IT} = \frac{\phi_B}{k \cdot T} \cdot \frac{C_{OX}}{\ln(10)} \cdot (S_{meas\_down} - S_{ideal}) \tag{5-35}$$

This is the equation that was used to calculate the number of interface traps in Figure 5-8.

The difficulty arises in calculating an accurate value for the subthreshold swing, since the inversion current and mid-gap currents vary from pA to twenty orders of magnitude smaller current at room temperature, and there are only a few decades at best of actual measured subthreshold current. The currents in Si MOS generally ranged from 10^{-7} to 10^{-14} A, allowing for much greater confidence in fitting the slope from measured data. Given the great amount of extrapolation required, it is wise to take the results with several grains of salt. However, in spite of this caveat, reasonable results can be obtained.

The difference in the mid-gap voltage measured following a positive-bias stress by a sweep down in gate voltage and the mid-gap voltage measured following a negative-bias stress by a sweep up in gate voltage can be found using (5-20):

$$\begin{aligned} V_{mg\_meas\_down} - V_{mg\_meas\_up} &= \left[V_{mg\_ideal} - \frac{q \cdot N_{OT\_down}}{C_{OX}} \right] - \left[V_{mg\_ideal} - \frac{q \cdot N_{OT\_up}}{C_{OX}} \right] \\ &= \frac{q \cdot (N_{OT\_up} - N_{OT\_down})}{C_{OX}} \end{aligned} \tag{5-36}$$

or

$$V_{mg\_meas\_down} - V_{mg\_meas\_up} = \frac{q \cdot \Delta N_{OT\_stress}}{C_{OX}} \tag{5-37}$$

Re-arranging terms provides a method for calculating the change in the number of oxide traps occupied due to a bias stress

$$\Delta N_{OT\_stress} = \frac{C_{OX}}{q} \cdot \left(V_{mg\_meas\_down} - V_{mg\_meas\_up} \right) \tag{5-38}$$

This is the equation that was used to extrapolate the number of oxide traps in Figure 5-5 and Figure 5-6.

In a similar manner, the difference in the inversion voltage measured following a positive-bias stress by a sweep down in gate voltage and the inversion voltage measured following a negative-bias stress by a sweep up in gate voltage can be found using (5-28):

$$\begin{aligned} V_{inv\_meas\_down} - V_{inv\_meas\_up} = & \left\{ V_{inv\_ideal} - \frac{q \cdot N_{OT\_down}}{C_{OX}} + q \cdot \left[\frac{N_{IT} + \Delta N_{OT\_down}}{C_{OX}} \right] \right\} \\ & - \left\{ V_{inv\_ideal} - \frac{q \cdot N_{OT\_up}}{C_{OX}} + q \cdot \left[\frac{N_{IT} + \Delta N_{OT\_up}}{C_{OX}} \right] \right\} \end{aligned} \tag{5-39}$$

or

$$\begin{aligned} V_{inv\_meas\_down} - V_{inv\_meas\_up} = & \frac{q \cdot (N_{OT\_up} - N_{OT\_down})}{C_{OX}} \\ & - \frac{q \cdot (\Delta N_{OT\_up} - \Delta N_{OT\_down})}{C_{OX}} \end{aligned} \tag{5-40}$$

that, using the simplifying expressions introduced in calculating (5-33) and (5-38) above, can be re-written as:

$$V_{inv\_meas\_down} - V_{inv\_meas\_up} = \frac{q \cdot [\Delta N_{OT\_stress} - \Delta N_{OT\_meas}]}{C_{OX}} \tag{5-41}$$

Equations (5-37) and (5-41) are a re-statement of (5-3) and (5-2), respectively, thus completing the derivation of the equations used to analyze the experimental subthreshold swing results of Section 5.3 and summarized in Figure 5-4.

5.5 Experimental observation of variation in subthreshold swing versus measurement speed

Not only does the speed of the measurement affect the magnitude of the V_T instability observed, as discussed above, it also affects the stretch-out of the subthreshold slope, which is the inverse of the subthreshold swing defined above. Figure 5-10 shows a series of back-and-forth instability measurements, with a 3,000 s gate-bias stress of ±15 V. The measurement times ranged from around 1 s to 1,200 s. Not surprisingly, the fastest measurement speeds resulted in the largest V_T instability and the slowest measurement speeds with the smallest instability. This narrowing of the envelope of the I_D-V_{GS} characteristics with slower measurement speeds is also depicted in Figure 5-11.

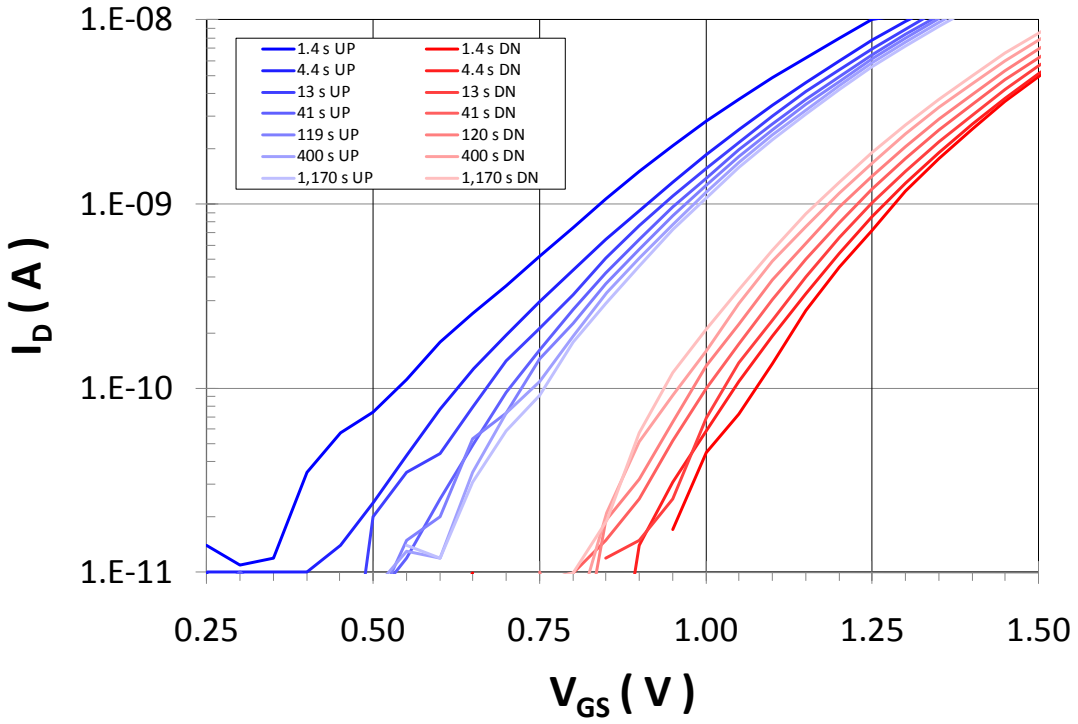

Figure 5-10: Variation in the subthreshold *I-V* characteristics of a 4H-SiC MOSFET from Sample Set I due to a back-and-forth gate-bias stressing sequence as a function of measurement speed. The width of the envelope decreases with increasing measurement speed, as does the stretch-out of the subthreshold *I-V* characteristics.

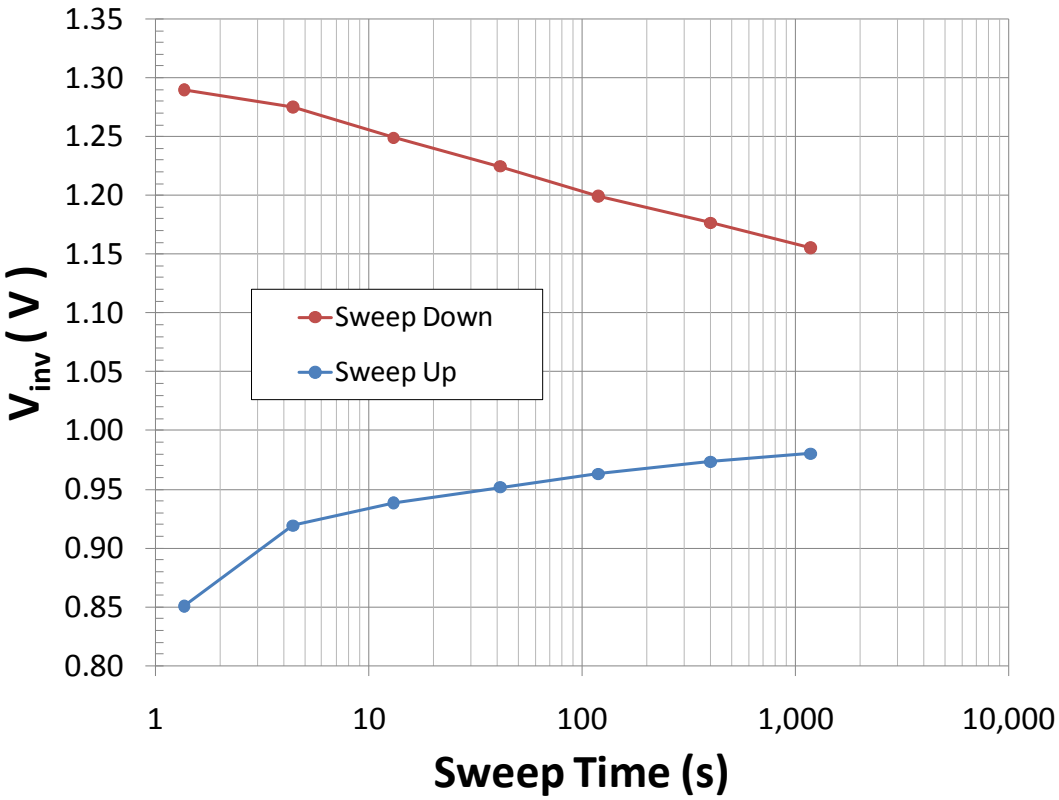

Figure 5-11: Variation in the threshold voltage, calculated using the inversion current method and the data shown in Figure 5-10, as a function of measurement time when sweeping up following a negative-bias stress and sweeping down following a positive-bias stress.

The number of switching oxide traps ranges from around 1.9 $\times 10^{11}$ traps per cm^2 for a 1-s sweep time to as little as 0.8 $\times 10^{11}$ traps per cm^2 for the slowest measurement time of 1 ks.

Accompanying this decrease in V_T instability is a change in the subthreshold swing during the sweep up following a negative gate-bias stress. Not only does the envelope of I_D-V_{GS} characteristics get closer together, but the slopes of these characteristics become more parallel as well. This is shown explicitly in Figure 5-12.

The stretch-out decreases as the measurement takes longer to complete. This makes sense if most of the oxide traps change charge state before they can be measured. It is interesting to note that although the subthreshold swing does not change with measurement time when sweeping down following a positive-bias stress, some oxide traps have clearly changed charge state during the longer measurements since the I_D-V_{GS} characteristics have moved to the left. A similar translation occurs in the opposite direction during the longer measurements when sweeping up following a negative-bias stress. These ideas are discussed further in Section 6.7 regarding the modeling of this effect.

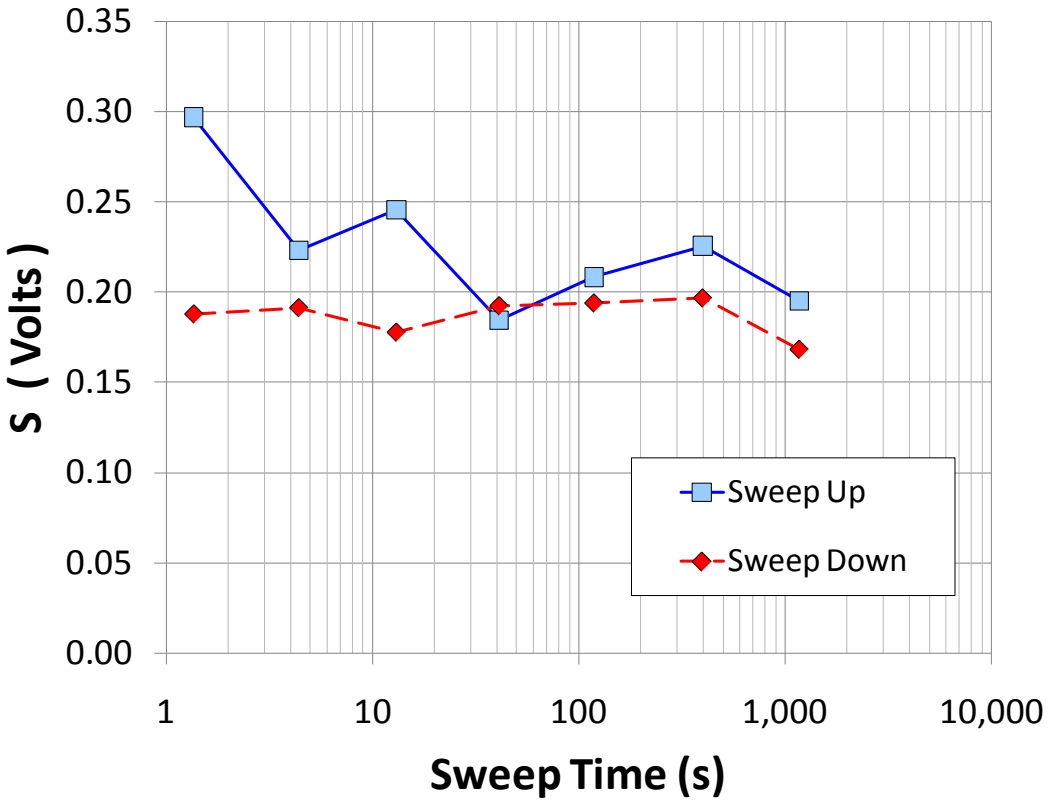

Figure 5-12: Variation in the subthreshold swing, *S*, calculated using the data shown in Figure 5-10, as a function of measurement time when sweeping up following a negative-bias stress and sweeping down following a positive-bias stress.

These results are consistent with the basic view that oxide traps can and do change charge state not only during the bias stress, but also during the measurement, and that faster measurements will result in larger observable shifts in V_T.

5.6 Charge separation analysis

As was discussed in previous chapters, there are potentially four different types of interfacial charge which can affect the threshold voltage: oxide traps, interface traps, mobile ions, and fixed charge. It is useful to be able to analytically separate out the different types of charge in order to fully model the device characteristics as well as to understand the full effects of processing variations. Since these different types of charge are likely due to different types of defects or impurities, it is likely that processing variations will affect them differently.

Charge separation analysis can be difficult, since there are a number of balancing or competing effects. For example, as discussed in Section 4.9, oxide trap filling or emptying can be balanced by mobile ion drift at elevated temperatures. Also, large numbers of negatively charged interface traps, as is the case for *n*-channel MOSFETs in inversion, may be balanced by large numbers of positively charged oxide traps and fixed charge. At very fast times, interface traps and oxide traps may both be changing charge state, thus making it difficult to determine whether a standard interface trap measurement is due to interface traps alone, or to a combination of trap types. In addition, if oxide trap filling and emptying requires a two-step process involving interface traps, as discussed in Chapter 6, then this charge separation analysis will be even more difficult.

The V_T-instability effect due to changes in oxide trap occupation can also affect other measurements designed to extract the interface-trap density. One such situation is for the dual-capacitor method proposed by Dr. Mrinal Das of Cree Research at an informal workshop at ARL several years ago. The basic idea is to compare the measured flat-band voltages for similarly processed *n*- and *p*-type capacitors. The flat-band voltage, V_{FB}, is the voltage at which a flat-band surface potential is achieved in an MOS capacitor. The flat-band capacitance, C_{FB}, can be defined in terms of C_{OX} and the depletion capacitance, C_D.

$$\frac{1}{C_{FB}} = \frac{1}{C_{OX}} + \frac{1}{C_D} \approx \frac{1}{\varepsilon_{OX} / t_{OX}} + \frac{1}{\varepsilon_S / L_D} \tag{5-42}$$

Values for C_{FB} as a ratio of C_{OX} are readily found as a function of oxide thickness and impurity doping [102].

When including the effects of the voltage shift due to oxide trap charging and discharging, the fuller analysis is as follows. Assuming that no mobile ionic charge is present, then the net charge is the sum of the N_{IT}, N_F, and N_{OT}, as discussed in Chapters 2 and 3, and will be the cause of the deviation of the measured flat-band capacitance compared with the ideal value, for both *n*-type and *p*-type capacitors:

$$N_{net\_n} = \frac{C_{OX}}{q} \cdot (V_{FB\_ideal\_n} - V_{FB\_meas\_n}) = -N_{IT\_n} + N_F + N_{OT\_n} \tag{5-43}$$

$$N_{net\_p} = \frac{C_{OX}}{q} \cdot (V_{FB\_ideal\_p} - V_{FB\_meas\_p}) = N_{IT\_p} + N_F + N_{OT\_p} \tag{5-44}$$

The ideal flat-band voltages are presented in Sze, p. 363 [102] for both *n*-type and *p*-type semiconductors:

$$V_{FB\_ideal\_n} = \phi_m - \left(\chi_{SiC} + \frac{E_{g\_SiC}}{2 \cdot q} - \phi_{B\_SiC} \right) \tag{5-45}$$

$$V_{FB\_ideal\_p} = \phi_m - \left(\chi_{SiC} + \frac{E_{g\_SiC}}{2 \cdot q} + \phi_{B\_SiC} \right) \tag{5-46}$$

Therefore, the difference in the ideal flat-band voltages is:

$$V_{FB\_ideal\_n} - V_{FB\_ideal\_p} = \phi_{B\_SiC} - \left(-\phi_{B\_SiC} \right) = 2 \cdot \phi_{B\_SiC} \tag{5-47}$$

The difference in the net charge can be written in terms of measured and ideal flat-band voltages:

$$N_{net\_p} - N_{net\_n} = \frac{C_{OX}}{q} \cdot \left[(V_{FB\_ideal\_p} - V_{FB\_meas\_p}) - (V_{FB\_ideal\_n} - V_{FB\_meas\_n}) \right] \tag{5-48}$$

This can be re-written by grouping the measured and ideal terms:

$$\begin{aligned} N_{net\_p} - N_{net\_n} &= \frac{C_{OX}}{q} \cdot \left[(V_{FB\_meas\_n} - V_{FB\_meas\_p}) - (V_{FB\_ideal\_n} - V_{FB\_ideal\_p}) \right] \\ &= \frac{C_{OX}}{q} \cdot \left[(V_{FB\_meas\_n} - V_{FB\_meas\_p}) - 2 \cdot \phi_{B\_SiC} \right] \end{aligned} \tag{5-49}$$

This difference in net charge can also be written in terms of the charge-trap densities:

$$\begin{aligned} N_{net\_p} - N_{net\_n} &= (N_{IT\_p} + N_F + N_{OT\_p}) - (-N_{IT\_n} + N_F + N_{OT\_n}) \\ &= (N_{IT\_p} + N_{IT\_n}) + (N_{OT\_p} - N_{OT\_n}) \end{aligned} \tag{5-50}$$

Therefore, the difference in the measured flat-band capacitances of similarly processed *n*-type and *p*-type capacitors results in the following relation:

$$V_{FB\_meas\_n} - V_{FB\_meas\_p} = \frac{q}{C_{OX}} \cdot \left[(N_{IT\_p} + N_{IT\_n}) + (N_{OT\_p} - N_{OT\_n}) \right] + 2 \cdot \phi_{B\_SiC} \tag{5-51}$$

So, if not for the presence of switching oxide traps, the number of interface traps could be readily determined. However, since near-interfacial oxide traps are also present, this

method yields the total number of interface traps along with the number of oxide traps that change charge state. This last term is, as demonstrated by the results of this chapter, highly time dependent. The faster the measurements, the larger the lower bound for the number of oxide traps present.

The results of Section 5.3 show how a lower bound can be calculated for the number of switching oxide traps. However, it is still difficult to determine the total number of oxide traps present. If the total number of interface traps can be independently calculated, then (5-51) would provide one method. *C*-*V* analysis on *p*-type capacitors is a standard method for determining the interface trap density [115]. Several methods also exist using the actual MOSFET. These include inferring the interface trap charge from the change in net charge with measurement temperature [118], and charge pumping [108].

Another question is what is the total number of fixed charge? The following analysis provides some insight. Using *n*-channel MOSFETs and *p*-type capacitors, which are readily available, a similar analysis to (5-43) and (5-44) can be performed:

$$V_{T\_ideal} - V_{T\_meas} \cong \frac{q}{C_{OX}} \cdot N_{net\_n} = \frac{q}{C_{OX}} \cdot \left(- N_{IT\_n} + N_F + N_{OT\_n} \right) \tag{5-52}$$

$$V_{FB\_ideal} - V_{FB\_meas} \cong \frac{q}{C_{OX}} \cdot N_{net\_p} = \frac{q}{C_{OX}} \cdot \left(N_{IT\_p} + N_F + N_{OT\_p} \right) \tag{5-53}$$

These equations can be rearranged to calculate the sum of fixed charge and oxide trap charge, if the interface trap charge can be calculated independently, as discussed above:

$$N_F + N_{OT\_n} = N_{net\_n} + N_{IT\_n} \tag{5-54}$$

$$N_F + N_{OT\_p} = N_{net\_p} - N_{IT\_p} \tag{5-55}$$

Recent results by Habersat and Lelis, et al. [105] using the sample sets described in Section 4.2, found that $N_F + N_{OT}$ is a large sum under negative bias (13-20×10^{11} cm^{-3}), but a relatively small sum under positive bias (2-5×10^{11} cm^{-3}), corresponding to (5-55) and (5-54), respectively. These results by themselves are ambiguous since they could be due either to a large number of fixed charge, which was found to be positively charged in Si MOSFETs [31], balanced by a large number of negatively charged oxide traps under positive bias which are uncharged under negative bias; or to a small number of fixed charge with a large number of positively charged oxide traps under negative bias and uncharged under positive bias.

Recent ESR results discussed in Chapter 2 suggest that *E′*-type defects are present in the oxide of SiC MOSFETs. No other electrically active defects in the oxide have been identified to date. *E′* defects were identified as the dominant oxide trap in irradiated Si MOSFETs with similar gate oxide thicknesses, as well as the cause of the V_T instability in those devices. Given that those *E′* defects acted as hole traps, it is not unreasonable that they behave in a similar fashion in SiC MOSFETs as well. If so, then the charge separation results of Habersat, Lelis, et al. suggest that there is not a large number of fixed charge. However, it has also been suggested that the *E′* center may under certain circumstances be able to trap a second electron, thus becoming negatively charged [100]. If this is the case, then the $N_F + N_{OT}$ results discussed above may yet be ambiguous regarding the total number of fixed charge.

5.7 Summary

Key experimental results presented in this chapter are consistent with a direct tunneling process, wherein electrons both fill and empty near-interfacial oxide traps distributed spatially over the first 40 to 50 Å of the oxide. These results include a linear increase in the V_T instability with the log of the stress time, the observation that extrapolating to zero instability occurs at stress times comparable to the first tunneling transition times of around 0.1 ps, and—most importantly—the strong time-dependence of the measurements. The fast *I*-*V* system at NIST allowed measurements as fast as 20 μs to be performed, with the fastest measurements revealing the largest V_T instabilities. The number of switching oxide traps with the fastest measurements was as large as 3.6×10^{11} cm^{-2}. It is not surprising that the speed of the measurement would be so important since a gate bias is necessarily applied during the measurement which in fact applies a bias stress of its own. The slower the measurement, the longer the time for this alternate gate bias to affect the results of the previous bias stress. The standard 1-s measurements could also be slowed down, and measurements as slow as 1 ks were performed, with the slowest measurements resulting in the smallest V_T instabilities and oxide traps densities half as large as those at regular 1-s ramp speeds.

Clearly, the near-interfacial oxide traps can change charge state during the measurement. Further evidence of this is the larger subthreshold swing observed when sweeping up in gate bias following a negative-bias stress compared to that when sweeping down in gate bias following a positive-bias stress. Although some portion of the deviation in the ideal subthreshold swing is certainly due to interface traps changing charge state, the repeated difference in subthreshold swing between sweeping up and

sweeping down is likely due to the complex response of oxide traps, especially since slower measurements showed less of a difference. A detailed analysis of this effect was presented. It was also shown that calculating the instability of the subthreshold I_D-V_{GS} characteristics by extrapolating down to mid-gap current levels resulted in V_T instabilities comparable to those found using the fast *I*-*V* system. In some cases, extrapolated instability calculations have indicated switching oxide-trap densities as large as 5×10^{11} cm^{-2}. These are trap densities comparable to those of interface traps.

Given the strong time-dependence of the response of the oxide traps, it is very difficult to apply analytical techniques in an attempt to separate out the effects of oxide traps and interface traps. It is also clear that not all of the non-interface trap charge is "fixed." Finally, it is important to distinguish between these different types of interfacial charge traps since they are probably caused by different physical defects, and therefore different processing techniques will likely affect them differently.

6 Tunneling Modeling

6.1 Introduction

Given the likelihood of a tunneling mechanism being responsible for the experimental results presented in this work—as discussed in previous chapters, this chapter will discuss the derivation, application, and comparison of a two-way tunneling model with those experimental results. It is important that a two-way model is applied, since depending on the electric field in the oxide and the distribution of charged and uncharged traps at a given spatial depth, electrons are likely to be both tunneling in and out (an electron tunneling out of an oxide trap back to the semiconductor can be equivalently considered to be a hole tunneling into the trap) simultaneously during a given period of time. This model is applied to both the bias stress periods, as well as during the measurement periods, when the gate-to-source voltage, V_{GS}, is being ramped.

The present model can successfully account for the variation in threshold-voltage instability observed as a function of bias-stress time, bias-stress magnitude, and measurement time. However, further improvements are still needed since it does not yet account for the variation in subthreshold swing. As will be discussed, this improvement will likely require the incorporation of a two-step process, with tunneling between near-interfacial oxide traps and interface traps, rather than simply between the oxide traps and the SiC valence and/or conduction bands.

6.2 Background

The modeling of the quantum-mechanical tunneling process of electrons filling and emptying trap states in the insulator will be done using the semi-classical WKB Approximation to solve the Schrodinger Equation. This approximation is named after three physicists, G. Wentzel, H.A. Kramers, and L. Brillouin, who in 1926 independently applied the already known simplification of wave functions to the wave mechanics of Schrodinger's quantum physics. This must be solved self-consistently with Poisson's equation at the interface and into the near-oxide region. The calculations discussed in Chapter 3 present a straight forward way of calculating the potential and field in the oxide.

This study follows the previous work of McLean [113], who applied the well-known WKB model for the direct tunneling of electrons into localized trap states in the insulating gate oxide, but expands upon it by allowing for the simultaneous tunneling of electrons in and out of the near-interfacial oxide traps.

The tunneling transition rate, which is the rate of change of the neutralized, uncharged trap density with respect to time, can be defined as the product of the probability of a tunneling transition and the charged trap density, for a given trap energy level and distance from the interface:

$$T(E,x,t) = \frac{\partial n_{OT\_neut}(E,x,t)}{\partial t} = g(E,x,t)\cdot[n_{OT\_total}(E,x) - n_{OT\_neut}(E,x,t)] \tag{6-1}$$

where $n_{OT\_total}(E,x)$ is the total number of oxide traps for a given trap energy level and distance from the interface, $n_{OT\_neut}(E,x,t)$ is the number of uncharged states where an

electron has neutralized the trapped hole, and *g(E, x, t)*, which is the probability of a tunneling event based on the WKB approximation, is given by

$$g(E,x,t) = \alpha(E,x,t) \cdot \exp[-Z(E,x,t)] \tag{6-2}$$

where the pre-factor $\alpha(E,x,t)$ is the "supply function" of the tunneling electrons and the exponential term controls the tunneling depth, based on the scaled distance *Z(E,x,t)*:

$$Z(E,x,t) = 2 \cdot \int_0^x \beta(E,x',t) \cdot dx' \tag{6-3}$$

with $\beta(E,x,t)$ related to the barrier height facing the tunneling electrons:

$$\beta(E,x,t) = \sqrt{\left(\frac{2 \cdot m_t^*}{\hbar^2}\right) \cdot [V_B(x,t) - E]} \tag{6-4}$$

where m^*_t is the effective tunneling mass, *h-bar* is Planck's constant divided by $2 \cdot \pi$, and $V_B(x,t)$-*E* the potential barrier itself [113].

If the oxide traps are assumed to all exist at a single energy level, E_t, and a trapezoidal approximation is used for the effect of an applied bias [112, 119], then for small variations in time [113]:

$$\beta(x) = \sqrt{\left(\frac{2 \cdot m_t^*}{\hbar^2}\right) \cdot [E_t - q \cdot \mathcal{E}_{OX} \cdot x]} \tag{6-5}$$

Since α varies much more slowly with *E* and *x* compared to the exponential term [113], the tunneling probability function can be re-written as

$$g(x) = \alpha \cdot \exp[-2 \cdot \beta(x) \cdot x] \tag{6-6}$$

Equation (6-1) can be solved for the neutralized trap concentration:

$$n_{OT\_neut}(x,t) = n_{OT\_total}(x) \cdot [1 - \exp(-\alpha \cdot t \cdot \exp[-2 \cdot \beta(x) \cdot x])] \tag{6-7}$$

Therefore, using (6-1), (6-6), and (6-7), the tunneling transition rate is given by

$$T(x,t) = n_{OT\_total}(x) \cdot \alpha \cdot \exp[-2 \cdot \beta(x) \cdot x] \cdot \left[\exp(-\alpha \cdot t \cdot \exp[-2 \cdot \beta(x) \cdot x])\right] \quad (6\text{-}8)$$

The tunneling probability, *g(x)*, tunneling transition rate, *T(x)*, and a normalized distribution of charged traps, $[n_{OT\_total}(x) - n_{OT\_neut}(x)]$, are shown in Figure 6-1 for a given time, *t*. There is a clear peak in the tunneling transition rate, such that the tunneling is localized at a given depth into the oxide for a particular time.

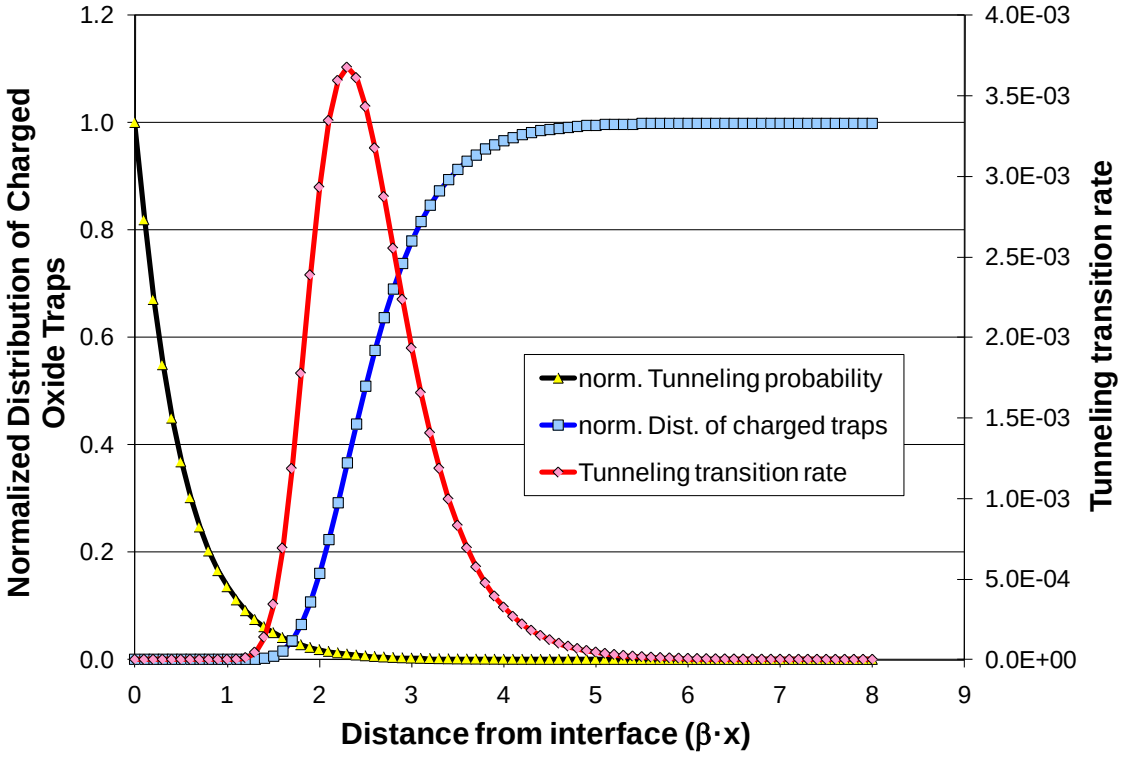

Figure 6-1: The sharp exponential decay in the tunneling probability with distance into the oxide, coupled with the relatively sharp distribution of oxide traps heretofore unaffected by the tunneling and therefore yet to change charge state, results in a sharp peak in the tunneling transition rate, illustrating the concept of a "tunneling front" which moves deeper into the oxide at a linear-with-log-time rate.

If the distribution of traps is assumed to be uniform, then differentiating the tunneling transition rate with respect to distance and setting it equal to zero yields the distance at which the peak tunneling is occurring for a given time *t*:

$$x_{peak} = \frac{1}{2 \cdot \beta} \cdot \ln(\alpha \cdot t) \tag{6-9}$$

Equation (6-9) indicates that the location of this peak moves logarithmically with time into the oxide, which leads to the notion of a tunneling front [112, 113], where most trap states in its wake have changed charge state whereas those beyond remain unchanged. This linear-with-log-time response is what we generally observe for the threshold-voltage instability at room temperature as demonstrated in the experimental chapters of this study. In addition, as noted earlier, this tunneling front was found to move at a rate of about 2 Å per decade of time in irradiated Si MOS [112]. Furthermore, given that the initial tunneling transitions were calculated to occur at around 0.1 ps [120], this means at bias stress times typically applied, this tunneling front is somewhere between 30 and 40 Å into the oxide from the SiC interface. Typical values of β range between 0.55 and 0.75 $Å^{-1}$ so that a typical full-width half-max value of the tunneling transition rate is around 2 Å wide (see Figure 6-1). Clearly, this is a spatially localized phenomenon when considering a one-way tunneling mechanism to oxide traps with a relatively uniform distribution and a single energy level.

Since the tunneling front should be at the interface when the first tunneling transitions occur, the time scale can be set by letting

$$\alpha = \frac{1}{t_0} \tag{6-10}$$

where t_0 is the initial tunneling transition time described above [120]. For every decade of time, the tunneling front moves at a rate of $ln(10)/(2\cdot\beta)$, which yields a tunneling rate of 1.5 to 2 Å per decade of time.

6.3 Two-way tunneling model

For a one-way tunneling process, with a constant bias applied, it may be enough to simply calculate whether the tunneling front has passed or not. However, since the experimental results presented in this study involve switching the bias polarity back and forth, as well as varying the measurement ramp speed, it is important to readily account for constantly varying bias conditions and the possibility that electrons that have previously tunneled in might under a different set of gate-bias conditions now tunnel out (see Figure 6-2 for a schematic of this process). A two-way tunneling model allows for this possibility.

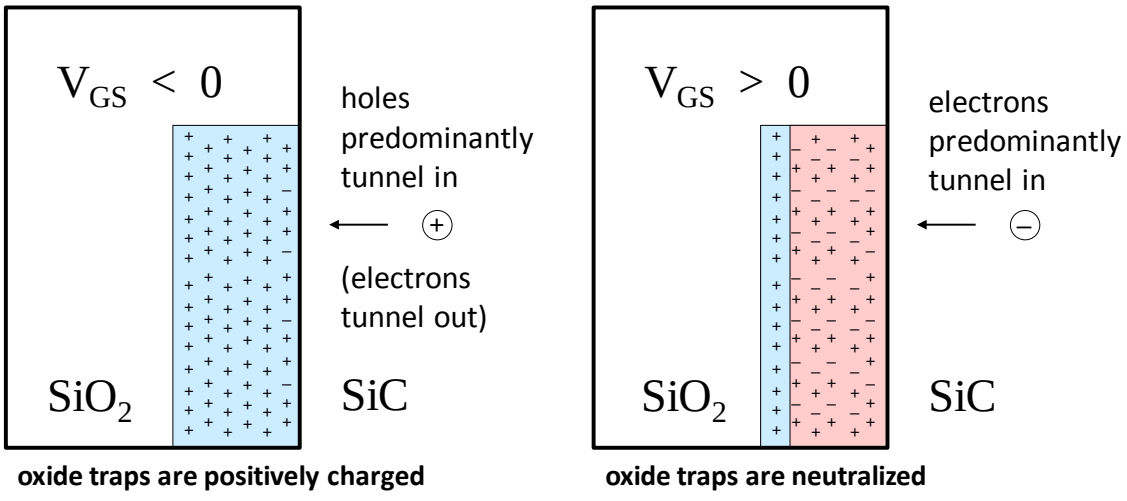

Figure 6-2: Schematic of holes predominantly tunneling in under negative bias to uncover positive charge and electrons predominantly tunneling in under positive bias to neutralize the positive charge.

For such a case, the new distribution of neutralized states can be found from the present distribution as follows, using a similar procedure to that for calculating the time-dependent occupation of interface traps [104]:

$$n_{OT\_neut}(x,t+\Delta t) = n_{OT\_neut}(x,t) + \Delta n_{OT\_neut}(x,t) \tag{6-11}$$

where the change in the neutralized trap distribution is found using (6-1) by taking the difference between the electrons tunneling in and those tunneling out (equivalent to holes tunneling in)

$$\begin{aligned}\Delta n_{OT\_neut}(x,t) = \Delta t \cdot p_{tun\_e}(x) \cdot \left[n_{OT\_total}(x) - n_{OT\_neut}(x,t)\right] \\ - \Delta t \cdot p_{tun\_h}(x) \cdot n_{OT\_neut}(x,t)\end{aligned} \tag{6-12}$$

with the probability of electrons tunneling in given by

$$p_{tun\_e}(x) = \alpha_e \cdot \exp[-2 \cdot \beta_e(x) \cdot x] \tag{6-13}$$

using (6-6), and the probability of holes tunneling in given by

$$p_{tun\_h}(x) = \alpha_h \cdot \exp[-2 \cdot \beta_h(x) \cdot x] \tag{6-14}$$

The values for β are as given in (6-5):

$$\beta_e(x) = \sqrt{\left(\frac{2 \cdot m^*_{t\_e}}{\hbar^2}\right) \cdot \left[E_{t\_e} - q \cdot \mathcal{E}_{OX} \cdot x\right]} \tag{6-15}$$

but with separate values for the effective tunneling mass of electrons and holes ($m^*_{t\_e}$ and $m^*_{t\_h}$, respectively), and for the trap level for electrons and holes, and the opposite sign for the field-modified barrier height for holes

$$\beta_h(x) = \sqrt{\left(\frac{2 \cdot m^*_{t\_h}}{\hbar^2}\right) \cdot \left[E_{t\_h} + q \cdot \mathcal{E}_{OX} \cdot x\right]} \tag{6-16}$$

The effective electron tunneling mass is well know and is given by $0.42 \cdot m_0$ [112, 113, 120, 121], where m_0 is the electron rest mass. The effective tunneling mass for holes varies greatly in the literature [122] and appears to be generally used as a fitting parameter.

From (6-15) and (6-16) it is clear that the deeper in energy level the trap is (larger E_t), the less effect variations in the potential barrier due to the oxide field or trap depth will have. Therefore, the experimental results when varying the stress bias (and therefore the oxide field) presented in Chapter 4 can provide insight into the trap energy level. Under positive bias, where electrons tunneling in will dominate, a larger variation in V_T instability with bias-stress magnitude (as seen in Figure 4-11) implies a shallower energy trap level for electrons. Similarly under negative bias, where holes tunneling in will dominate, a smaller variation in V_T instability with bias-stress magnitude (also seen in Figure 4-11) implies a deeper energy trap level for holes. These results are consistent with a trap level slightly above the conduction band of SiC, which is one of the trap levels proposed for irradiated Si MOS [86, 112, 89, 90]. This trap level is illustrated in Figure 6-3.

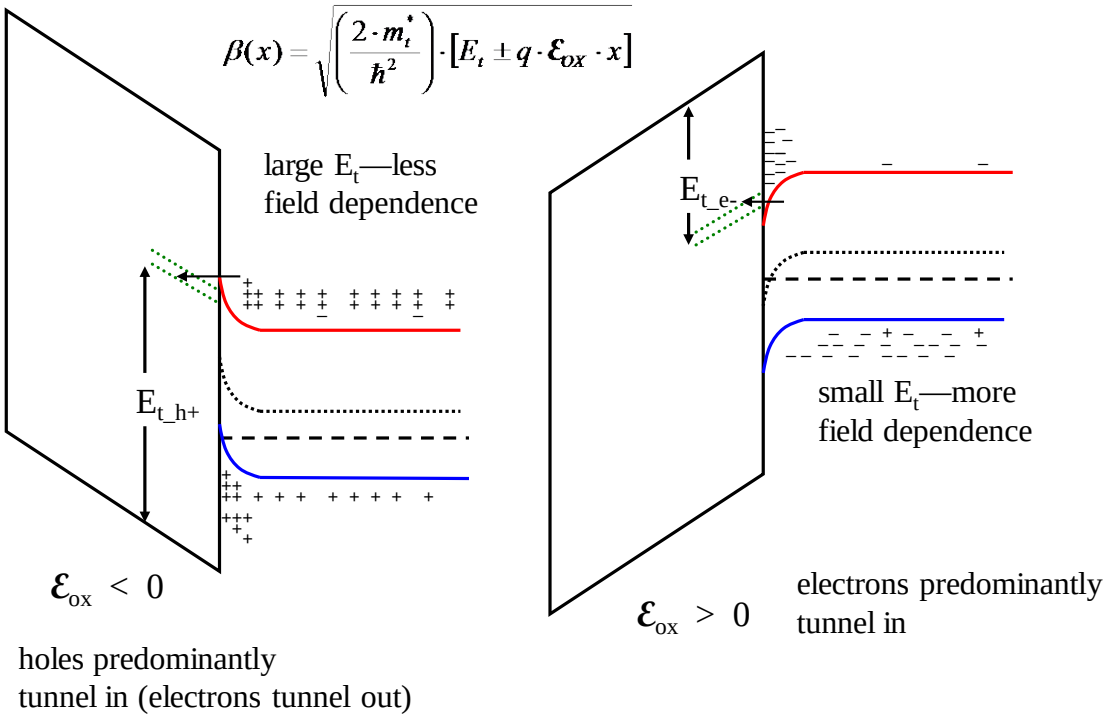

Figure 6-3: Schematic of potential energy level of the oxide traps, and the effects of band bending, based on experimental results.

A trap level across from well below the valence band edge of Si, which would be around the valence band edge of SiC, is another energy level proposed for irradiated Si MOS [120, 112, 89, 90]. This deeper energy level for electrons tunneling in (and shallower trap level for holes tunneling in) is consistent with the larger variation in V_T instability with negative bias-stress magnitude and smaller variation with positive bias-stress magnitude for earlier results on deposited oxide samples (as seen in Figure 4-10). It is also consistent with the recent results on SiC MOS capacitor structures discussed in Section 4.8 [109]. These capacitor instability results may also suggest that both of these trap levels are present.

6.4 Steady-state conditions

As the charge tunnels in and out, it will modify the total amount of oxide charge versus distance from the interface, and therefore the spatial variation in oxide field—as described in Chapter 3. At some point in time, these two processes will achieve a steady state condition between electrons tunneling in and out. This steady state can be found by setting $\Delta n_{OT\_neut}(x)$ in (6-12) to zero, such that:

$$p_{tun\_h}(x) \cdot n_{OT\_neut}(x) = p_{tun\_e}(x) \cdot \left[n_{OT\_total}(x) - n_{OT\_neut}(x) \right] \tag{6-17}$$

or

$$\alpha_h \cdot \exp[-2 \cdot \beta_h(x) \cdot x] \cdot n_{OT\_neut}(x) = \alpha_e \cdot \exp[-2 \cdot \beta_e(x) \cdot x] \cdot \left[n_{OT\_total}(x) - n_{OT\_neut}(x) \right] \tag{6-18}$$

which reduces to

$$\frac{n_{OT\_neut}(x)}{n_{OT\_total}(x)} = \frac{1}{1 + \left(\alpha_h / \alpha_e \right) \cdot \exp[-2 \cdot (\beta_h(x) - \beta_e(x)) \cdot x]} \tag{6-19}$$

If $\beta_h(x) = \beta_e(x)$, then the fraction of neutralized oxide traps is given by $1/[1+(\alpha_h/\alpha_e)]$. Letting $\alpha_h = \alpha_e$, then the fraction of neutralized oxide traps at a particular oxide depth is less than 0.5 when $\beta_h(x) < \beta_e(x)$, and greater than 0.5 when $\beta_h(x) > \beta_e(x)$. Therefore, an oxide trap is more likely to be neutralized when

$$m^*_{t\_h} \cdot \left[E_{t\_h} + q \cdot \mathcal{E}_{OX} \cdot x \right] > m^*_{t\_e} \cdot \left[E_{t\_e} - q \cdot \mathcal{E}_{OX} \cdot x \right] \tag{6-20}$$

This effect is demonstrated in the next set of figures, which plot the fraction of neutralized oxide traps, i.e., those for which an electron has tunneled in to neutralize the trapped positive charge (see Chapter 2 for a discussion of the E' defect and its charge states), versus distance into the oxide. This variation is given for constant oxide fields

ranging from –2 to +2 MV/cm, which covers the general range of the experimental results. Although very useful in understanding the relationship between the trap occupation density as a function of oxide trap depth and field for given values of energy trap level, etc., it does not show an actual distribution of neutralized traps versus oxide depth since the oxide field varies with oxide depth, especially when most of the positively charged oxide traps have not been neutralized (see Chapter 3 and Figure 6-12).

Figure 6-4 plots the variation in the fraction of neutralized oxide traps for a trap energy level adjacent to the semiconductor conduction band (see Figure 6-3). Similarly, Figure 6-5 plots this variation for a trap energy level well below the valence band edge of Si and approximately adjacent to the SiC valence band edge. These calculations demonstrate how trap levels either close to the conduction band or close to the valence band can lead to greater sensitivity to either a positive or negative oxide field, if an appropriate value for the effective hole tunneling mass is chosen.

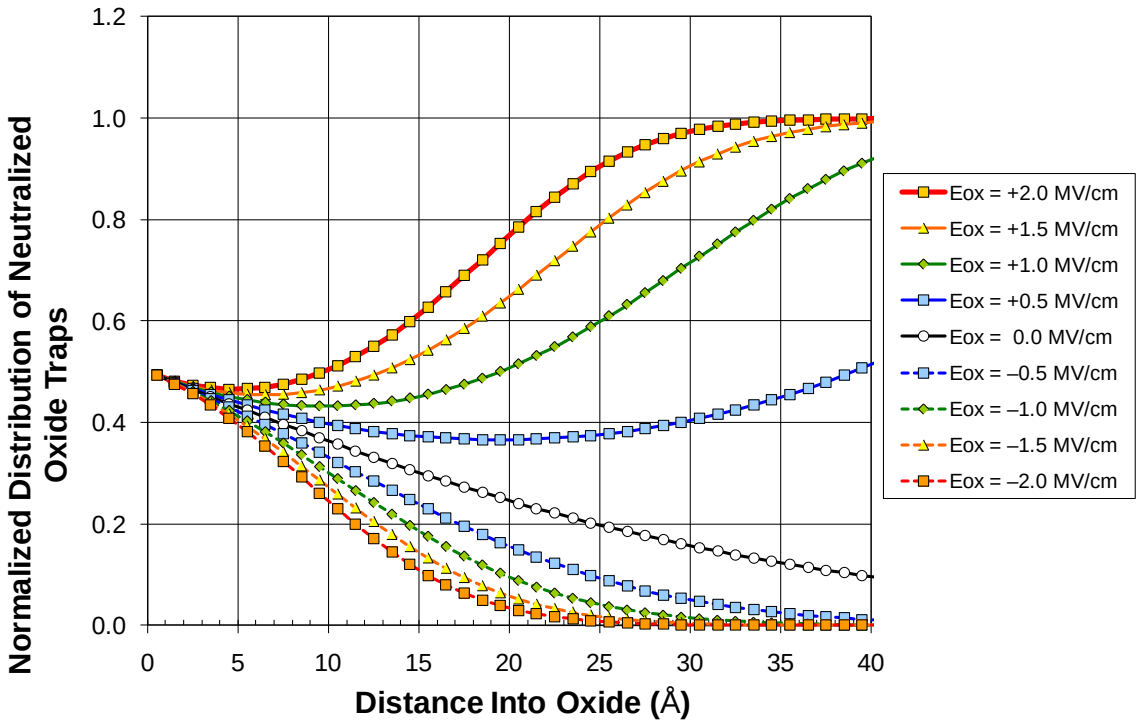

Figure 6-4: Calculation of the steady-state fraction of neutralized (filled with electrons) oxide traps versus oxide depth as a function of constant oxide-field values for the following parameter values: E_{t_e} = 2.7 eV, E_{t_h} = 6.3 eV, and m^*_h = 0.162 (m^*_e = 0.42 and $\alpha_e = \alpha_h$).

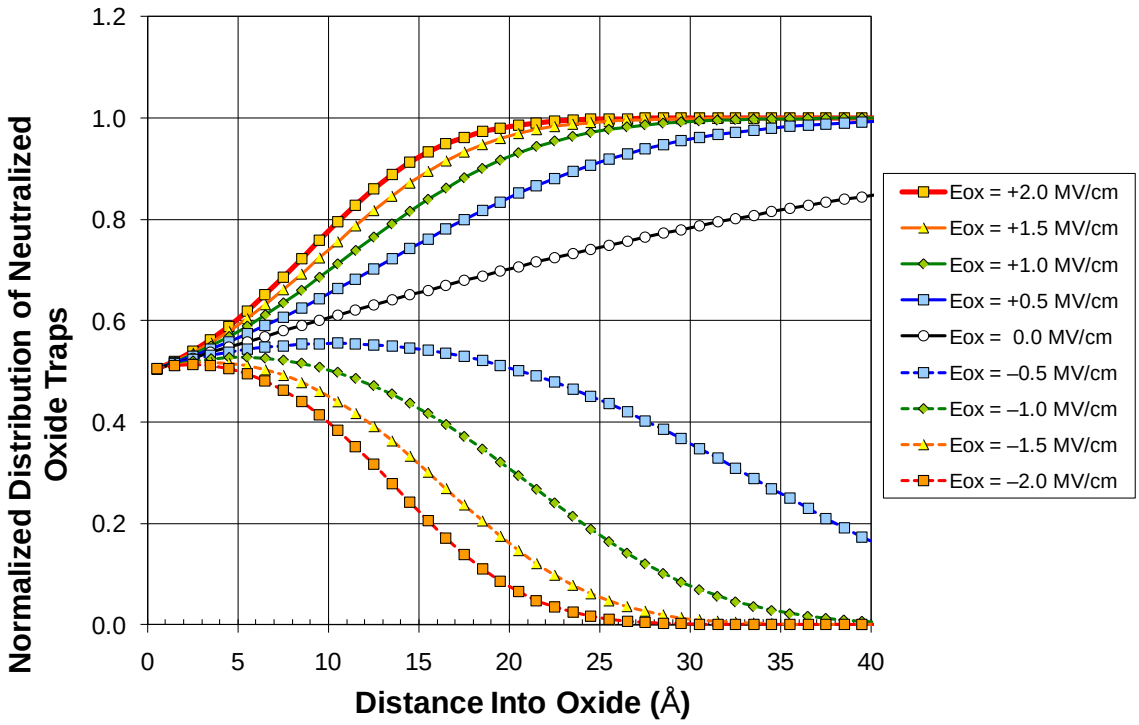

Figure 6-5: Calculation of the steady-state fraction of neutralized (filled with electrons) oxide traps versus oxide depth as a function of constant oxide-field values for the following parameter values: E_{t_e} = 6.0 eV, E_{t_h} = 3.0 eV, and m^*_h = 0.885 (m^*_e = 0.42 and $\alpha_e = \alpha_h$).

There are some difficulties with this approach. The opposite sensitivity to either a positive or negative oxide field can be achieved for the same trap energy levels by changing the effective hole tunneling mass value. Also, for a trap level across from the conduction band, although the number of available holes is always large, the number of available of electrons is dependent on the surface potential. The opposite is true for a trap level across from the valence band. However, it is quite likely that the energy level will change depending on whether the oxide trap is positively charged or neutralized. For example, both Nicklaw, et al. and Goes, et al. showed using density functional theory (DFT) that the trap level could change by over an eV depending on the charge state due

to changes in relaxation or "puckering" of the defect structure [123, [124]]. If it is below the valence band when positively charged and above the conduction band when neutralized (although this change in trap energy is much less likely for a wide bandgap semiconductor such as SiC), then there would be no surface potential dependence for either tunneling transition. Figure 6-6 illustrates the variation in neutralized traps versus oxide depth and field for such a case, again using an appropriate value for the effective hole tunneling mass. (These are the values that were used to obtain reasonable fits to experimental results for variations in measurement time and gate bias stress—to be discussed later in this chapter.)

A more likely scenario is that the oxide trap levels lie within the bandgap for at least one of the trap states, and that this then involves a dependence not only on the surface potential, but also on the responsiveness of the interface traps. This possibility is beyond the scope of this work, but will be considered again when comparing the experimentally observed variation in subthreshold swing with the model.

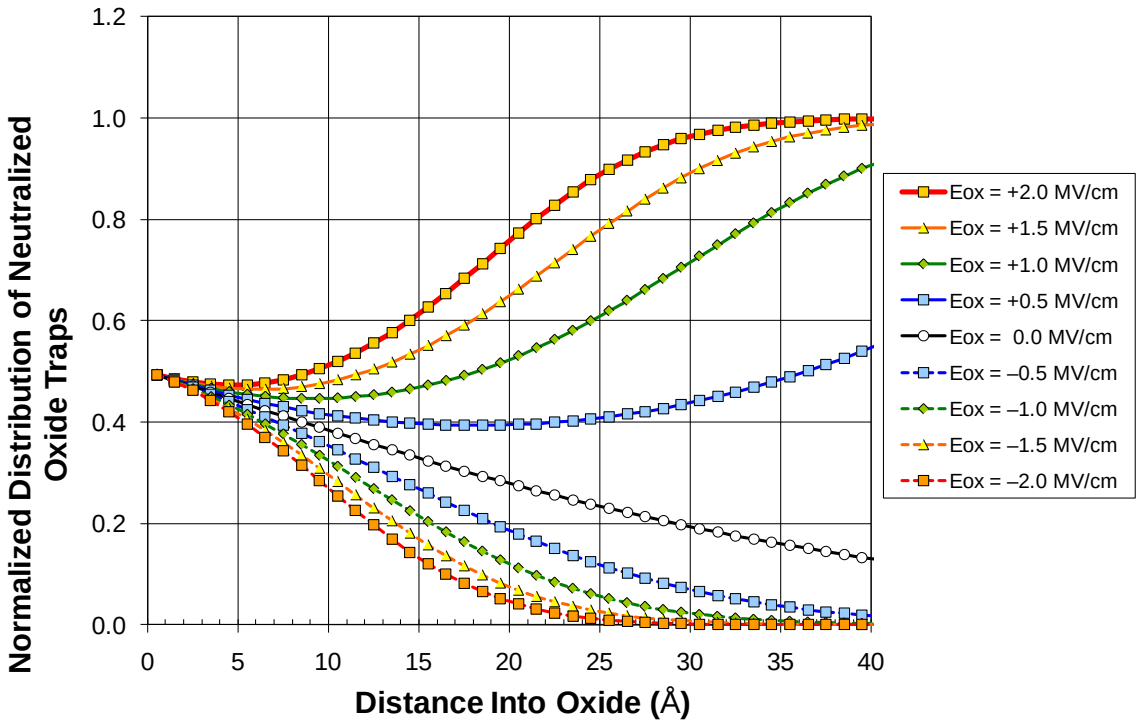

Figure 6-6: Calculation of the steady-state fraction of neutralized (filled with electrons) oxide traps versus oxide depth as a function of constant oxide-field values for the following parameter values: E_{t_e} = 6.0 eV, E_{t_h} = 6.3 eV, and m^*_h = 0.377 (m^*_e = 0.42 and $\alpha_e = \alpha_h$).

6.5 Tunneling time-step increments

As discussed previously, the first tunneling transition rates have been calculated to occur at around 0.1 ps [120]. This then also provides a scale for the time increments used in (6-12). Figure 6-7 shows how the longer the tunneling occurs, the deeper into the oxide the tunneling front has moved. The net change in the charge state of those oxide traps closest to the interface is continuously decreasing. At the same time, the deeper into the oxide, the smaller the net change for a short, fixed time increment such as t_0 = 1

ps. This illustrates the need to take larger and larger time steps for longer tunneling times, since the net change per unit time keeps decreasing.

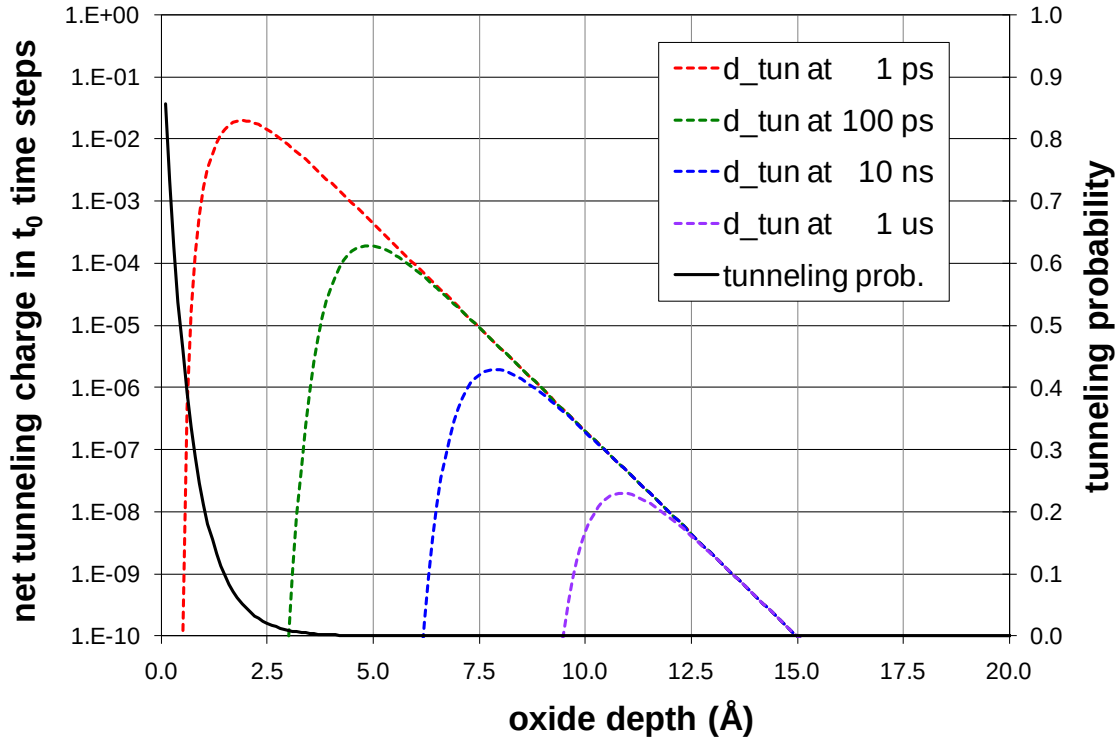

Figure 6-7: Calculation of the variation in net charge tunneling into oxide traps during a time increment of t_0 seconds as a function of total tunneling time.

There is, however, a difficulty with taking larger time steps. Although the occupancy of oxide traps closest to the interface quickly reaches a steady-state, as indicated in Figure 6-7, taking larger and larger time increments for longer and longer tunneling times necessitates taking the difference of very large numbers to calculate the net tunneling charge close to the interface —see (6-12). This difficulty can be avoided by setting the trap occupancy to the long-term steady state values (e.g., as shown in Figure 6-6) once this state has been achieved by the movement of the tunneling front with time.

6.6 Tunneling model mechanics

Figure 6-8 illustrates the basic algorithm for the tunneling model. First, the total number of active oxide traps is defined, along with their spatial distribution (see Figure 3-14 and accompanying discussion). An assumed interface trap distribution is also defined, as well as a schedule of different gate stress biases to apply (including the gate bias ramp applied during the measurement) and for how long. The initial bias stress is set for V_{GS} = 0 V, and is applied for 10^{15} s to ensure that the device begins with an unbiased initial condition.

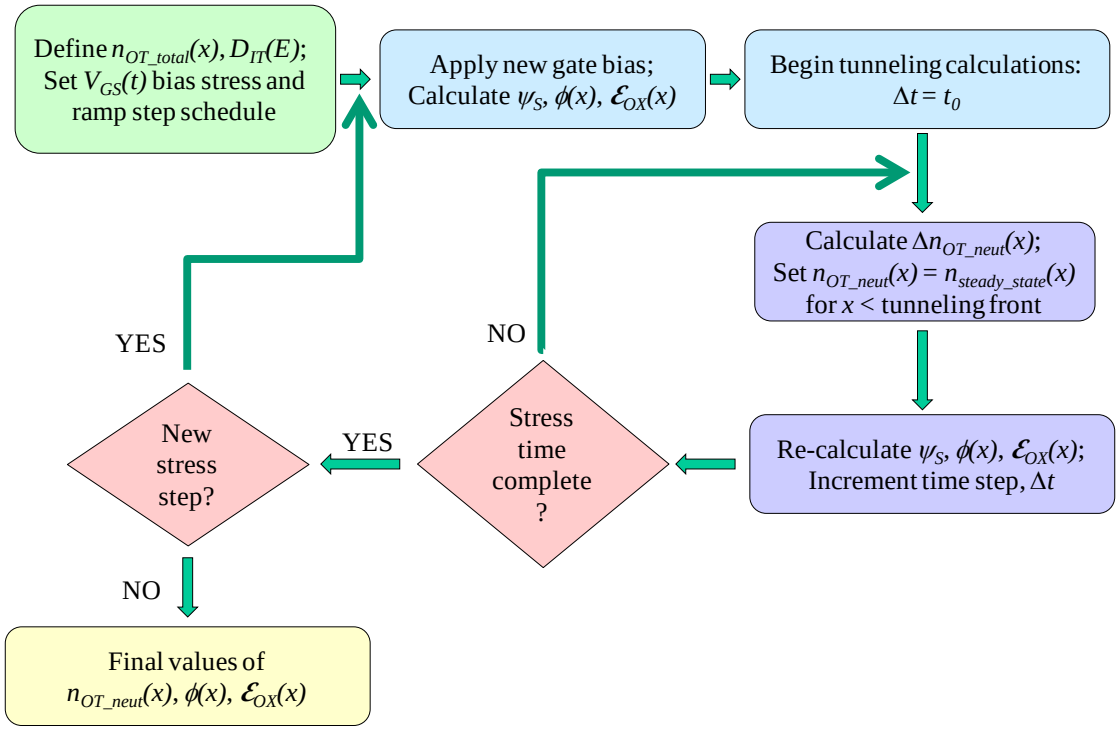

Figure 6-8: Schematic of tunneling model algorithm.

With the application of a new gate bias, the surface potential is found self-consistently with the interface trap and oxide trap occupations. Next, the details of the initial electric potential and electric field are calculated (see Chapter 3). This is followed by the tunneling-calculation loop. With every time step, the change in oxide trap

occupancy is calculated. As the tunneling front proceeds deeper into the oxide, the trap states in its wake are set to the steady-state value for the reasons described above. The surface potential, electric field, etc., are recalculated several times per decade of time, and the time step is incremented as well. This is repeated for all the gate-bias stress steps, including those simulating a measurement.

Figure 6-9 depicts the variation in the positively charged oxide-trap distribution versus oxide depth, first for an initial very long-term unbiased steady-state condition, followed by a gate-bias sweep in the positive direction, and finally for a bias stress of 10^6 s and a bias stress of +15 V. The effect of gate-bias stress during the measurement is shown in 5-V steps, for a 1-s gate ramp.

Initially, under the unbiased condition, most of the oxide traps are positively charged (this is consistent with the neutralized trap distribution shown in Figure 6-6). The application of –5 V at the beginning of the gate-ramp for an initial measurement has the effect of slightly increasing the number of positively charged oxide traps over the first 25 Å of oxide. As the gate bias is swept up, the oxide traps over this range become more and more neutralized as electrons tunnel in. However, the traps deeper in are still unaffected. They are only affected during the long-term positive-bias stress, after which most of the oxide traps to a depth of around 40 Å have been neutralized.

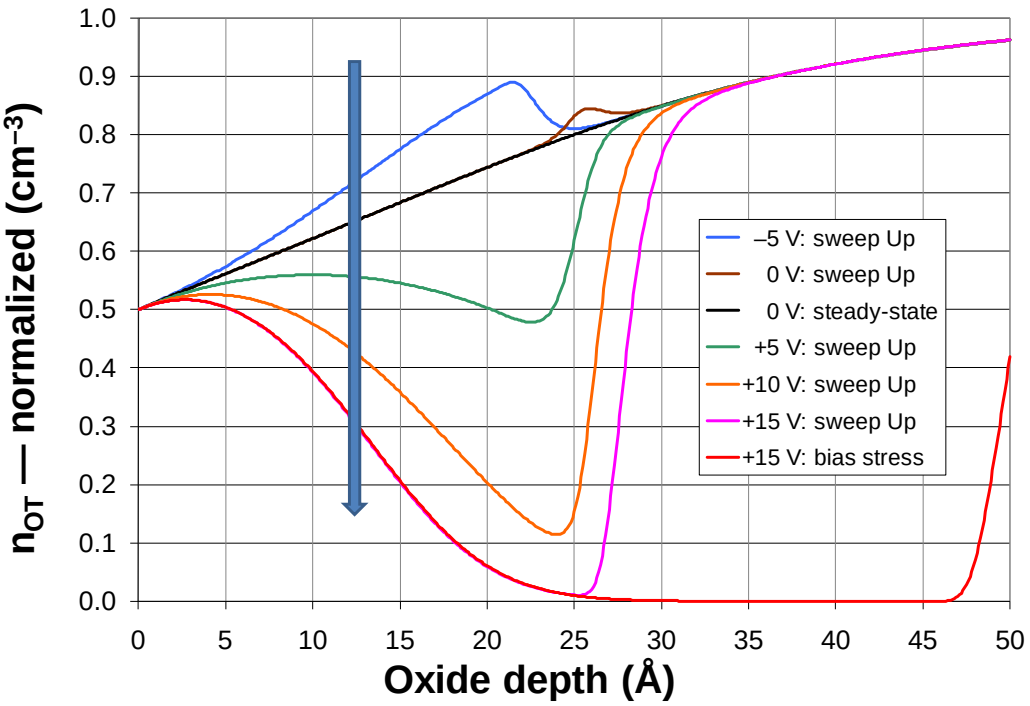

Figure 6-9: Initial variations in the normalized positively charged oxide-trap distribution vs oxide depth as a function of gate bias during both a 1-s measurement sweeping up in gate bias and a subsequent +15 V 10^6-s bias stress.

Figure 6-10 shows the opposite process. Following the long-term positive-bias stress, the gate-bias is swept down, causing oxide traps over the first 25 Å to gradually become positively charged again as holes tunnel in (i.e., electrons tunnel out). Again, it is not until a long-term negative-bias stress that most of the oxide traps out to about 40 Å are positively charged. Figure 6-11 shows this bias stress and measurement sequence in the opposite order. This back-and-forth instability is essentially repeatable, as depicted in Figure 4-7. These calculations of the model show the importance of the measurement in affecting the charge state of the near-interfacial oxide traps. A faster measurement would not affect oxide traps as far from the interface.

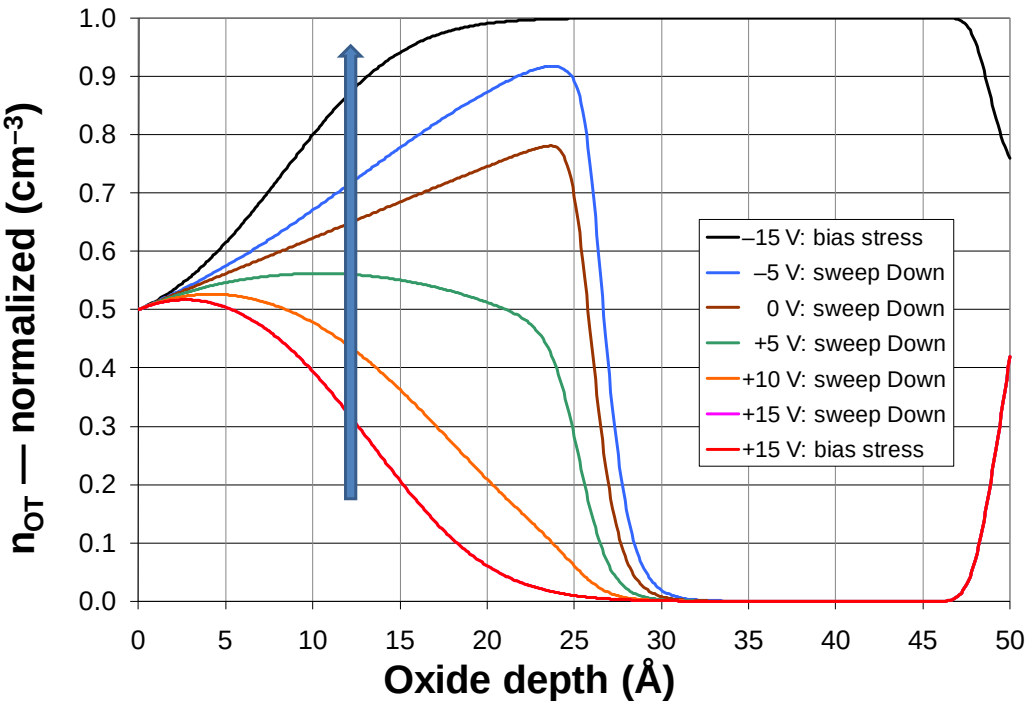

Figure 6-10: Subsequent variations in the normalized positively charged oxide-trap distribution vs oxide depth as a function of gate bias following (1) an initial +15 V bias stress, (2) a 1-s measurements sweeping down in gate bias, and (3) a final –15 V 10^6-s bias stress.

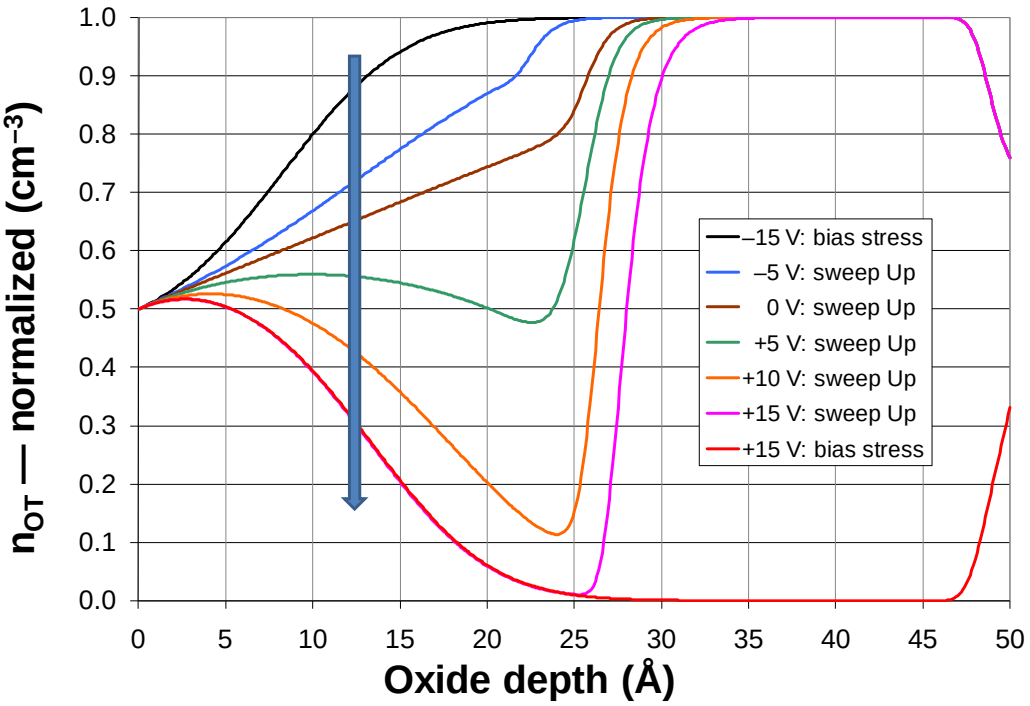

Figure 6-11: Further subsequent variations in the normalized positively charged oxide-trap distribution vs oxide depth as a function of gate bias following (1) an initial –15 V bias stress, (2) a 1-s measurements sweeping up in gate bias, and (3) a final +15 V 10^6-s bias stress.

Figure 6-12 depicts the change in the electric field versus oxide depth for the variations in the positively charged oxide-trap distribution given in Figure 6-11, when the gate bias is swept up during the measurement. As the amount of positively charged oxide traps decreases with electrons tunneling in with the gate bias increasing, the change in the oxide field diminishes. Following a long-term negative-bias stress wherein most of the oxide traps even deep in have been neutralized, the change in oxide field with oxide depth is minimal.

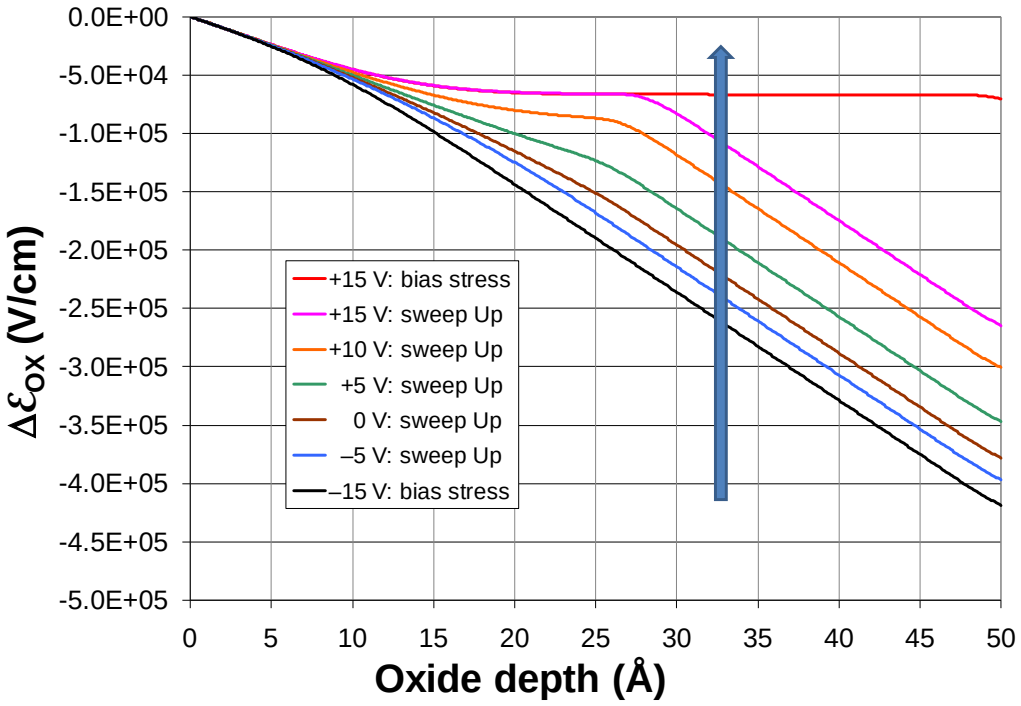

Figure 6-12: Variations in the change in oxide field vs oxide depth due to the variations in positively charge oxide-trap distribution as shown in Figure 6-11.

6.7 Comparison of model with experimental results

Figure 6-13 shows the simulated back-and-forth bias stressing and measurement results of the model, plotting the variation in the V_{OT} component of threshold voltage, defined in Chapter 3 as the voltage shift due to the presence of oxide trapped charge, versus each bias-stress sequence. The first two points show the before-and-after effects of a –15 V gate-bias stress. V_{OT} becomes more negative due to the increase in the number of positively charged oxide traps—see Figure 6-11 and (3-33). This is followed by a sweep up in gate bias, from –5 V to + 15V, in step increments of 0.1 V.

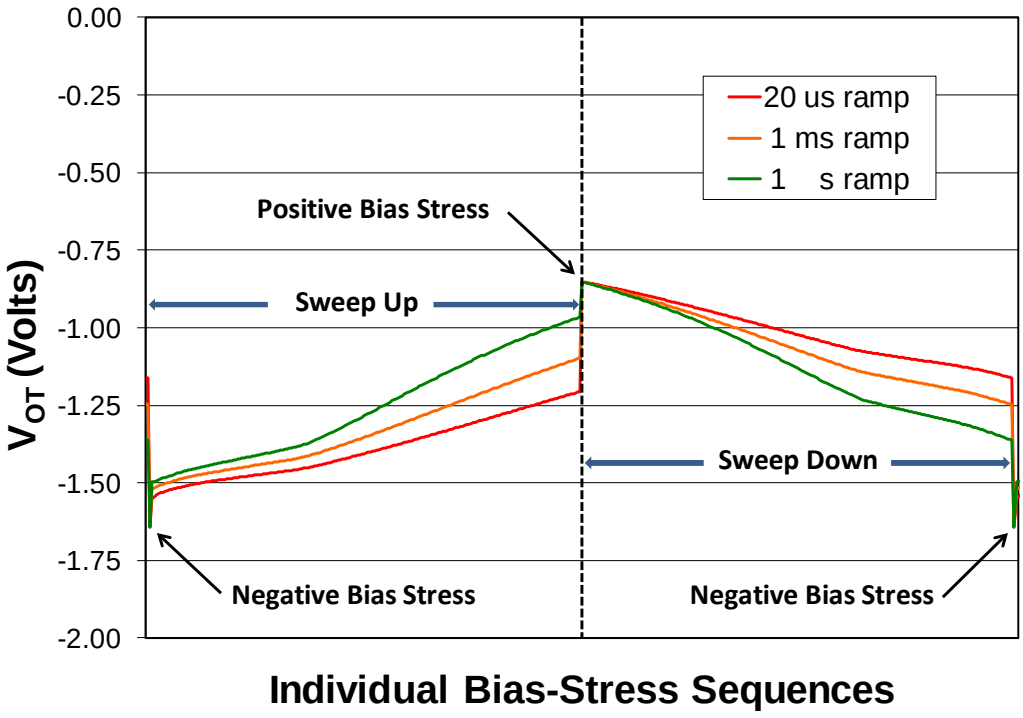

Figure 6-13: Variation in V_{OT}, the voltage shift due to the presence of oxide trapped charge, is plotted versus individual bias stress sequences simulating both the long-term bias stresses, as well as the shorter bias stresses that comprise the measurement ramp for several different measurement times.

The change in V_{OT} following each simulated bias increment of the gate ramp is shown for several different measurement speeds. Since each bias stress step takes longer for the longer measurement speeds, it is not surprising that the simulated 1-s sweep leads to a larger change in V_{OT} during the measurement than does the simulated 20-μs sweep, since more electrons can tunnel in and increase the number of charge neutralized states. This is followed by a +15 V gate-bias stress and 0.1 V decrements in the gate bias to simulate the downward sweep in gate bias for the next measurement. Again, the longer sweep time leads to a larger shift during the simulated measurement.

Since the drain current in the subthreshold region is given as [117]:

$$I_D = \mu_n \cdot \left(\frac{Z}{L}\right) \cdot \frac{\varepsilon_S}{\sqrt{2} \cdot L_D \cdot \beta^2} \cdot \left(\frac{n_i}{N_a}\right)^2 \cdot \left(1 - e^{-\beta \cdot V_{DS}}\right) \cdot e^{\beta \cdot \psi_S} \cdot \frac{1}{\sqrt{\beta \cdot \psi_S}} \tag{6-21}$$

Therefore, the log of the drain current is

$$\log(I_D) = \log[A] + \frac{\beta \cdot \psi_S}{\ln(10)} - \frac{\log(\beta \cdot \psi_S)}{2} \tag{6-22}$$

so that

$$\log(I_D) \propto \psi_S \tag{6-23}$$

This means that a plot of the surface potential versus V_{GS} will look similar in form to that of the log of the drain current versus gate bias. This is shown in Figure 6-14, where the results from Figure 6-13 are re-plotted, matching experimental results from Figure 5-2. The simulated increase in instability with increasing measurement speed is as expected, as is the larger difference under positive bias.

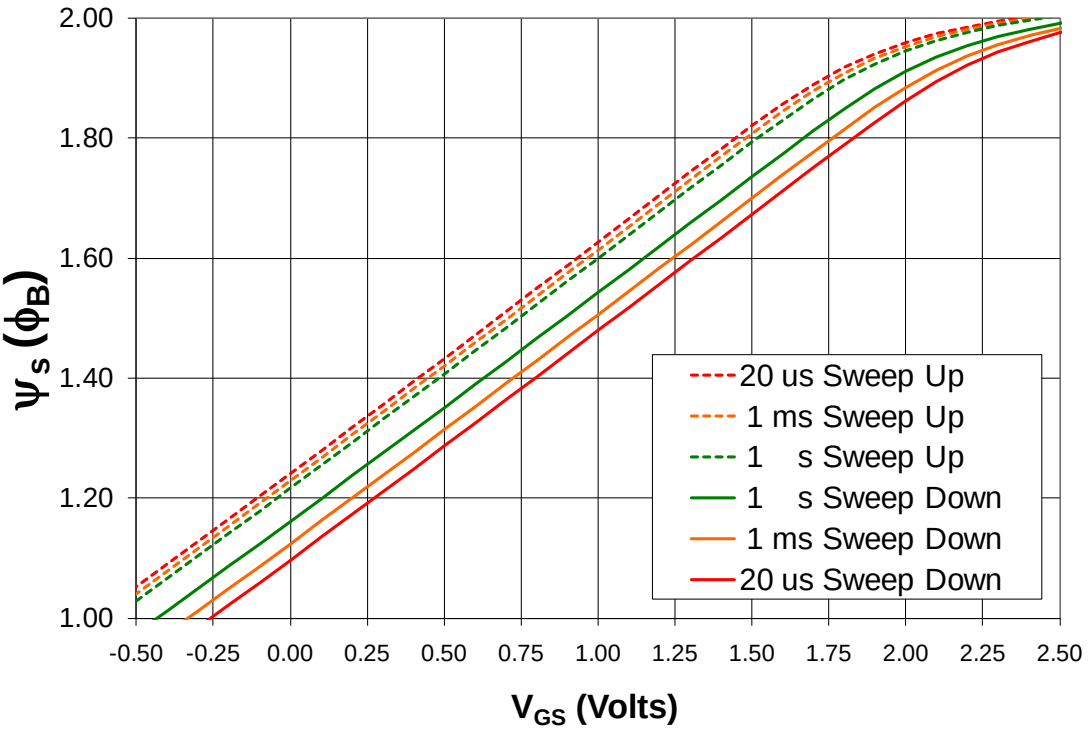

Figure 6-14: Simulated plots of surface potential (in terms of the bulk potential) versus gate bias are similar in form to plots of log(I_D) vs V_{GS}. Model calculations predict larger instabilities for faster measurement ramp speeds, matching experimental.

The normalized variation of instability with ramp speed is explicitly plotted in Figure 6-15 for a bias stress of ±15 V and a bias stress time of 10^6 s. This compares reasonably well with the experimental results of Figure 5-2. For this fit, the following model parameters were used: E_{t_e} = 3.1 eV, E_{t_h} = 3.5 eV, m^*_h = 0.34, m^*_e = 0.42, λ = 0.10, and $\alpha_e = \alpha_h$, which are the same as those used in Figure 6-6. The value for the oxide trap distribution decay parameter, λ = 0.10—described in Figure 3-14, and Equations (3-84) and (3-85)—produces a sharper exponential decay than is likely, but was used to better fit the strong upturn in the experimental data for the fastest measurement times. However, this is based on a linear extrapolation of the experimental data to slightly longer stress times, which is subject to a degree of uncertainty.

Using a value of $\lambda = 0.03$ instead, which defines a milder exponential decay of the total oxide trap distribution, leads to a factor of 2 increase in ΔV_{OT} between 1-s and 20-μs simulated measurements instead of the factor of 3 found experimentally. However, the 1-s experimental measurement led to a calculation of only 1.2×10^{11} cm^{-2} oxide traps changing charge state, which is on the low side of the observed range of results. This may be due to the presence of mobile ions in these slower, room-temperature measurements, given that evidence of mobile ions was observed at elevated temperature for devices from this same sample set (see Figure 4-22 and Figure 4-24), and evidence of room-temperature mobile-ion drift has been observed in other samples. Therefore, the more uniform distribution of oxide traps might actually produce a better fit, if a time-dependent mobile-ion drift component were added to the model.

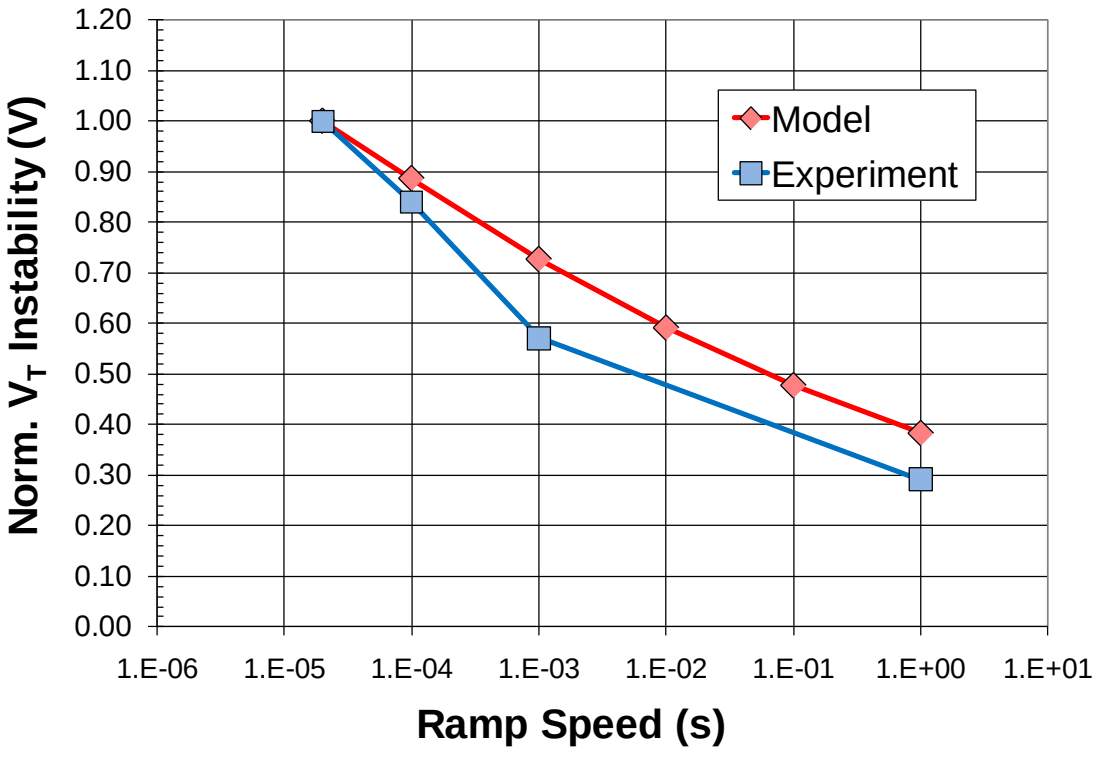

Figure 6-15: Plot of the normalized back-and-forth threshold-voltage instability versus measurement ramp speed, comparing model calculations and experimental results.

The model was also used to simulate the variation in instability for different bias stress magnitudes. Figure 6-16 shows these results, as a function of stress time for simulated 1-s measurements, with significant differences due to the magnitude of the positive-bias stress, but no real difference seen under negative-bias stress. These results are quite consistent with the results of Figure 4-11. It should be noted that the total instability is dependent on the total number of active oxide traps assumed, which in this case was 1×10^{12} cm^{-2}. The same model parameters were used as in the above results, and the oxide trap distribution was set at λ=0.03. This is the more mild exponential decay and gives a fairly linear-with-log-stress-time response.

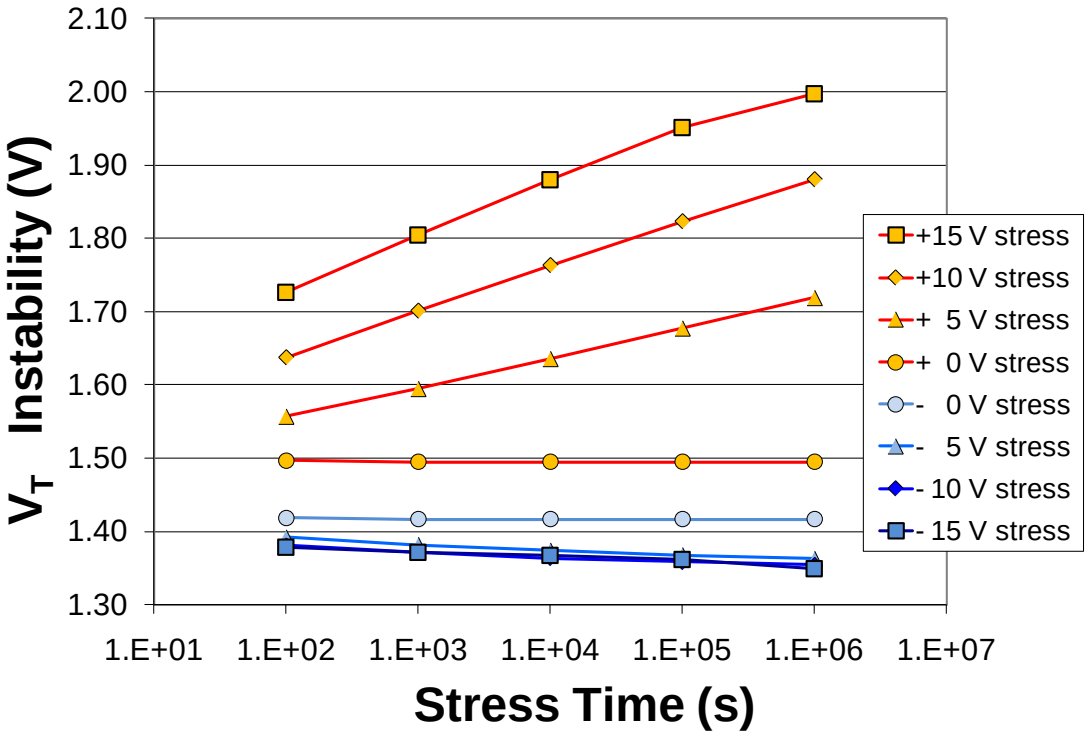

Figure 6-16: Plot of the changes in V_{OT}, the voltage shift due to the presence of oxide trapped charge, versus both positive and negative-bias stress magnitude with a simulated measurement speed of 1 s.

One thing that stands out about the comparison of experimental results with those of the model is that the model does not predict any variation in subthreshold swing between sweeping up following a negative-bias stress and sweeping down following a positive-bias stress—see Figure 6-14. This is contrary to the experimental results presented in Chapter 5 (other than those with very long measurement times).

This larger stretch-out of the subthreshold *I-V* characteristics is assumed to be due to the discharging of some oxide trap states during the measurement that were previously charged during the negative-bias stress. Since the bias applied during the measurement of the subthreshold region is of opposite polarity in this case—instead of being of the same bias polarity for a sweep down following a positive-bias stress—the number of oxide traps changing charge state is likely greater, thus causing a larger stretch-out in this case.

Figure 6-17 presents several possible measurement scenarios. If the measurement is made fast enough, then very few oxide traps will have had time to change charge state and there will be no additional stretch-out. On the other hand, if the measurement is slow enough, then most of the oxide traps will already have changed charge state by the time the subthreshold current rises above the experimental noise floor, representing about the last 20 percent of the change in surface potential from mid-gap to inversion. The fact that we do in fact observe experimentally a stretch-out suggests that the middle case is what actually happens. The problem is that the model does not predict this.

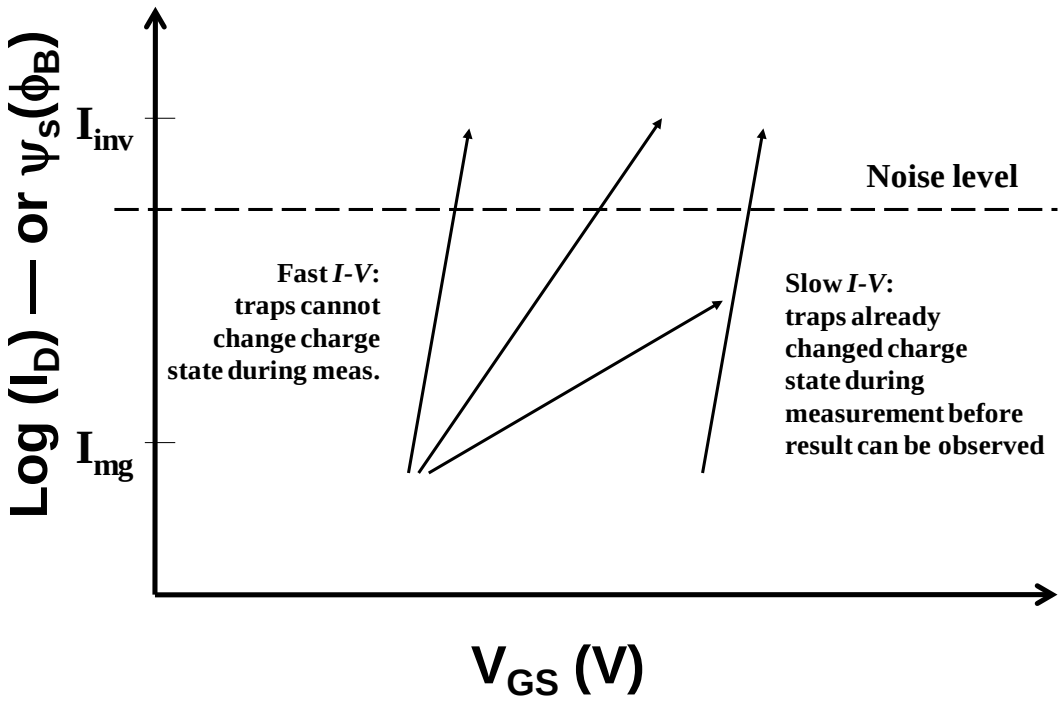

Figure 6-17: Schematic indicating several possible responses of the drain current versus gate voltage in the subthreshold region, depending on the speed of the measurement and the response time of the oxide traps.

What causes this significant change in the charge states over this range of surface potential? Figure 3-2 shows the variation in oxide field versus surface potential. The polarity of the field changes down at flat band. The magnitude of the field remains relatively small until the onset of strong inversion. The inversion carrier concentration is also quite insignificant until just below strong inversion. The only parameter that is changing significantly from mid-gap to inversion is the occupation of interface traps, although for wide band gaps such as SiC, the trap time constant for states near mid-gap is quite large [20, 102]. Another point to consider is the difference in the band gaps of Si and SiC, as shown in Figure 6-18.

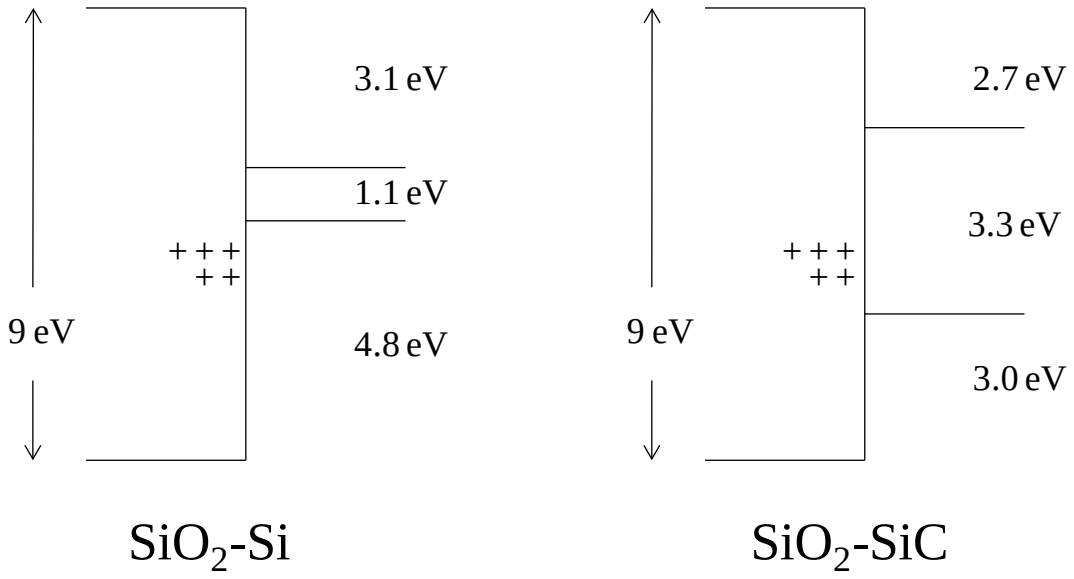

Figure 6-18: Schematic showing a comparison of the band gaps of Si and 4H-SiC and how oxide traps that fall below the valence band edge of Si may actually be within the bandgap of SiC.

Even oxide trap states that lie well below the Si valence band edge may very well lie within the bandgap of SiC. This means that in order to tunnel to or from such states, it will require some sort of two-step process. The most likely scenario for such a two-step process is, for example, where an electron first fills an interface-trap state and then tunnels into the oxide to neutralize a positively charged oxide trap. Since the filling of interface traps is dependent on the surface potential (as well as the interface trap response time), this may very well explain why we experimentally observe this stretch-out of the subthreshold *I-V* characteristics. The model will need to be modified to account for this proposed two-step process. This in turn will require the calculation of the time-dependent occupational density of the interface traps, since this time dependence will determine the number of available filled or empty states from which electrons can tunnel to or from near-interfacial oxide traps.

6.8 Summary

In summary, a well-established tunneling model based on the WKB Approximation was employed to simulate the charging and uncharging of near-interfacial oxide traps. This work extends that model by allowing for a simultaneous two-way process. The calculation of a long-term steady-state level of trap occupation dependent on the distance from the interface and the local oxide field, as well as the assumed energy level of the trap, is of great importance, since it allows for a simple incorporation of the tunneling front concept. Traps in the wake of this front have changed charge state—or more accurately—have achieved their final steady state value. Those traps still ahead of this front have not yet been affected, thus accounting for the time dependence of both the bias stress and of the measurement. Since the probability of tunneling decreases with increasing oxide depth, it is necessary to take increasingly larger time steps at later times in order to facilitate the calculation process.

Examples of the simulated changes in the occupied oxide trap level for a long-term bias stress as well as the bias applied during the measurement were presented, as was the outline of the tunneling model algorithm.

The results of the model were compared with experimental results presented in earlier chapters, and were found to be quite good for the most part in explaining the dependence on measurement time, stress time, and stress bias. However, the model does not account for the additional stretch-out of the subthreshold *I-V* characteristics during a sweep up in bias following a negative-bias stress. It was suggestd that it is likely that at least some of the oxide-trap states lie within the bandgap of SiC, and therefore a two-step

process involving the filling and emptying of interface traps will probably need to be incorporated to improve the present model.

7 Effect of V_T Instability on SiC Power MOSFET Reliability

7.1 Introduction

Given the voltage instability described in the previous chapters, and given the Army's interest in the development of reliable, efficient, voltage-controlled, normally-off, high-power, high-voltage, and high-temperature SiC switches, it is important to ask whether these effects are also observed in the vertical SiC power DMOSFET; and if so, what are the implications for device operation in circuits and systems of interest.

Therefore, following a description of the power devices, experimental results are presented showing that the effects of gate-bias stressing in SiC power DMOSFETs are very similar to those in lateral test structures, and that *ON*-state current stressing leads to an increase in V_T instability. Furthermore, this increase in instability appears to be due to an increase in device temperature from self-heating but the presence of an elevated temperature is significant only when a bias is applied. The V_T instability effect is likely due to electrons tunneling into and out of near-interfacial oxide traps that extend spatially into the gate oxide form the SiC interface, and the increase in V_T instability due to high-temperature bias stressing is quite possibly due to the activation of additional near-interfacial oxide traps. This activation also leads to an increase in stretch-out in the subthreshold *I-V* characteristics following a negative gate-bias stress. Finally, the complex time, temperature, and bias dependence of the I_D-V_{GS} characteristics leads to the conclusion that present reliability test standards for high-temperature gate bias (HTGB) stressing based on Si technology are inadequate for SiC power MOSFETs.

The SiC DMOSFET is formed by first implanting a *p*-well into an *n*-type epi, followed by a second implantation into the *p*-well to form the n^+-source region (see Figure 7-1). This creates a lateral channel followed by a vertical drift region, whose thickness is determined by how much voltage it is required to block, with the drain located at the bottom n^+-substrate. Devices anywhere from 1.2 kV to 10 kV have been demonstrated [11, 12, 125]. This chapter will focus on the effects of the voltage instability on 1.2kV 4H SiC DMOSFETs with a drift layer thickness of about 10 μm. The devices used in this study range in rating (and therefore in size) from 5-A all the way up to 50-A, and were manufactured between 2005 and 2010 and were considered state-of-the-art at the time of manufacture. The older, smaller area devices were used in the initial comparisons of gate-bias instability, whereas the larger, more recent devices were used to assess the more complicated effects of bias and temperature.

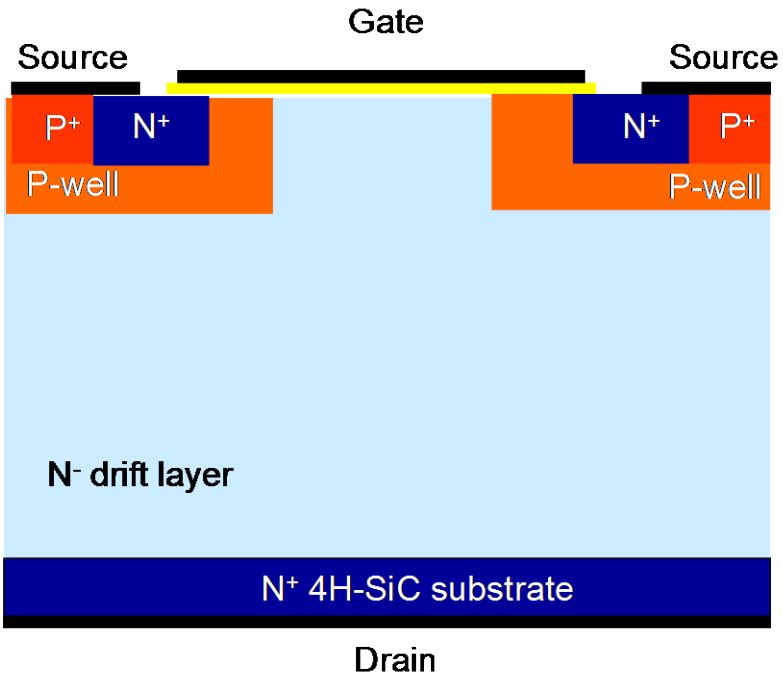

Figure 7-1: Schematic of the power DMOSFET which has a double implant to form the source and channel region [11].

Ideally, power switches such as the SiC DMOSFET will have a very low *ON*-state resistance and very low leakage current in the *OFF* or blocking state. To achieve this, the effective channel mobility should be as high as possible and the threshold voltage should be positive with enough margin so that no subthreshold current flows in the *OFF* state. As discussed in Chapter 2, the presence of interfacial charge can decrease the effective mobility by decreasing the number of free carriers and increasing coulombic scattering. And, of course, it can also shift the threshold-voltage.

It is also very important to keep in mind the results of the fast *I-V* measurements described in Chapter 5, which showed that the gate-voltage ramp speed is directly related to how much instability is recorded. Figure 5-2 implies that the actual V_T shift may be as much as a volt or more, even when a more standard 1-s measurement indicates a V_T shift of no more than a quarter or third of a volt. This greater-than-realized instability can potentially affect the performance and reliability of a power SiC DMOSFET in at least two ways.

First, as is indicated in Figure 7-2, if the threshold voltage is not set high enough, then a negative shift of the I_D-V_{GS} characteristic can lead to a substantial increase in the subthreshold leakage current. For a power DMOSFET, this would mean an increase in drain leakage in the *OFF* state and therefore a decrease in its functional blocking voltage—even when V_T using the linear *I-V* extrapolation appears to be fine. For example, Figure 7-2 shows how a shift of just 0.5 V could lead to a two order-of-magnitude increase in leakage current. The larger actual V_T-instability shift, combined with the well understood phenomenon of decreasing threshold voltage with increasing temperature because of fewer filled interface traps [118] and an increase in thermal

carriers, means that even more margin must be built into the design of the room temperature threshold voltage to remain reliable at elevated temperature.

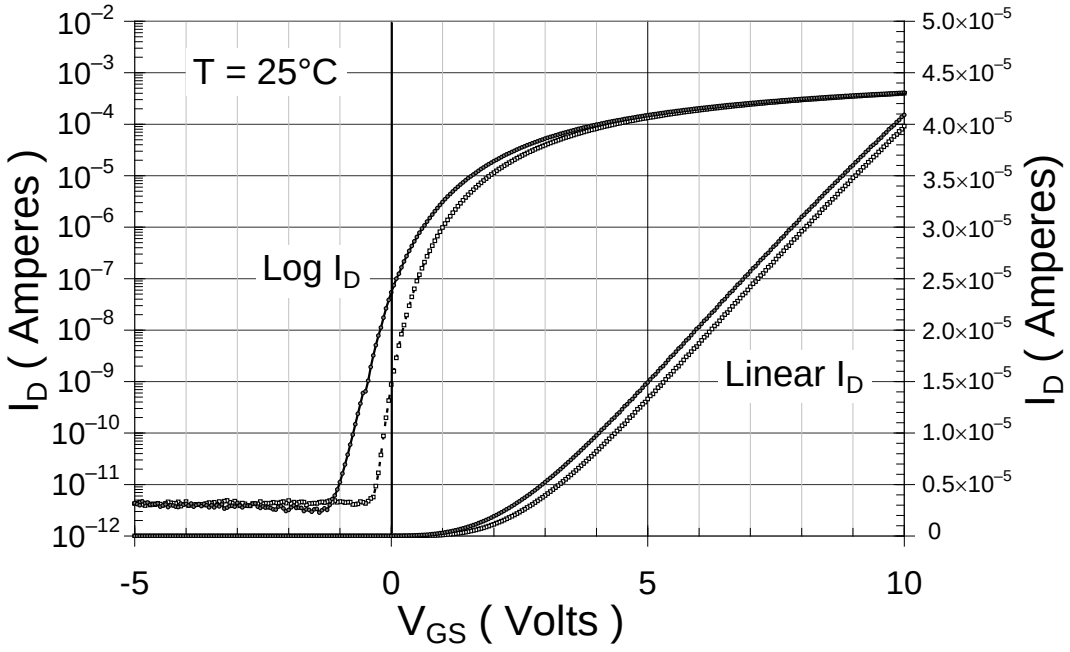

Figure 7-2: Illustration of potential reliability issues due to V_T instability effect. Subthreshold leakage current may increase dramatically in the *OFF* state if the threshold voltage is not set properly.

Second, a positive V_T shift can decrease performance by increasing the resistance in the ON state by increasing the threshold voltage and thus reducing the value of V_{GS}-V_T. While it is critical not to increase the drain leakage in the blocking state, it is also important not to set the threshold too high, especially since increased threshold voltage may be coupled with lower effective mobility [81]. Thus, it is important to accurately estimate the magnitude of the actual threshold-voltage instability so as to find the optimum threshold voltage to achieve the best combination of low *OFF*-state leakage with low *ON*-state resistance. As long as the threshold voltage is set high enough to preclude the onset of subthreshold drain leakage current in the blocking state, then the

primary effect of this instability is to increase the *ON*-state resistance. For well-behaved power DMOSFETs, this would increase the power loss by no more than a few percent.

7.2 Gate-bias stress-induced threshold-voltage instability in SiC power DMOSFETs

This section presents some basic bias-stress induced threshold-voltage instability measurements on fully processed 4-H SiC power DMOSFETs as a function of bias-stress and time—at room temperature. The effects of elevated temperature will be addressed in subsequent sections. The basic experimental procedure was previously described in Chapter 4. In essence, a gate-bias stress was applied for a certain bias-stress time, the effect was measured by ramping the gate bias, and then a gate-bias stress of opposite polarity was applied for the same bias-stress time before re-measuring (see Figure 7-3). The measurements of the I_D-V_{GS} characteristic were all made using an Agilent 4155 parameter analyzer, with a gate-ramp speed of about 1 s and with 50 mV applied to the drain. The source and drain of these three-terminal devices were both grounded during the gate-bias stress. The average V_T instability versus stress time was calculated using two different methods: linear extrapolation to zero current; and the voltage corresponding to a set current.

Under normal operating conditions, when the device is in the ON state, a positive gate bias of 15 or 20 V is applied. In the blocking state, although the gate bias is zero, the large voltage on the drain leads to a negative field across the gate oxide. This effect has been simulated by applying a negative bias on the gate while grounding the drain.

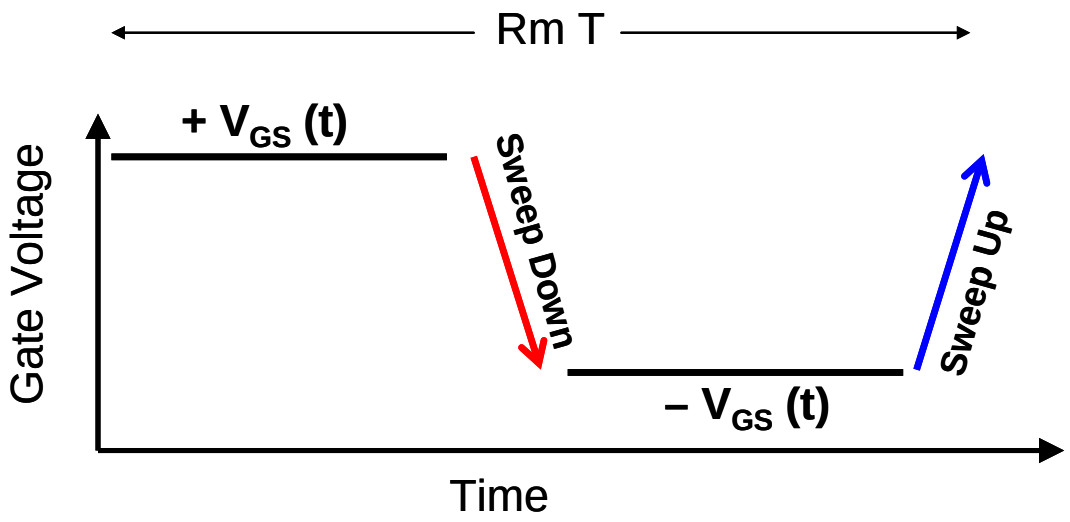

Figure 7-3: Schematic of the test-and-measurement sequence used for the room-temperature gate-bias stress.

Figure 7-4 shows a comparison of the gate-bias stress-induced V_T instability for 5-A DMOSFETs and for lateral MOSFETs with similar gate oxides. The as-processed epi lateral MOSFET has a slightly lower average instability, but the lateral MOSFET with an implanted epi region that simulates the implanted channel of the DMOSFET shows an average instability versus bias-stress time that is right in line with the response of the DMOSFETs. This result gives added confidence that we are looking at the same effect in the fully processed high-power vertical DMOSFETs as in the low-power lateral test structures whose results were presented in Chapters 4 and 5. In particular, these results are consistent with those of Figure 4-14, where the middle curve of that figure shows that the V_T instability of an implanted channel device with an NO anneal, such as might be found in the DMOSFET, is marginally worse than that for an as-grown epi channel device. It should be noted that the more recent state-of-the-art DMOSFETs have much improved V_T instability characteristics from those of just a few years back where gate-

bias stressing at room temperature produced instabilities greater than 1 V even with relatively slow 1-s *I-V* measurements [36].

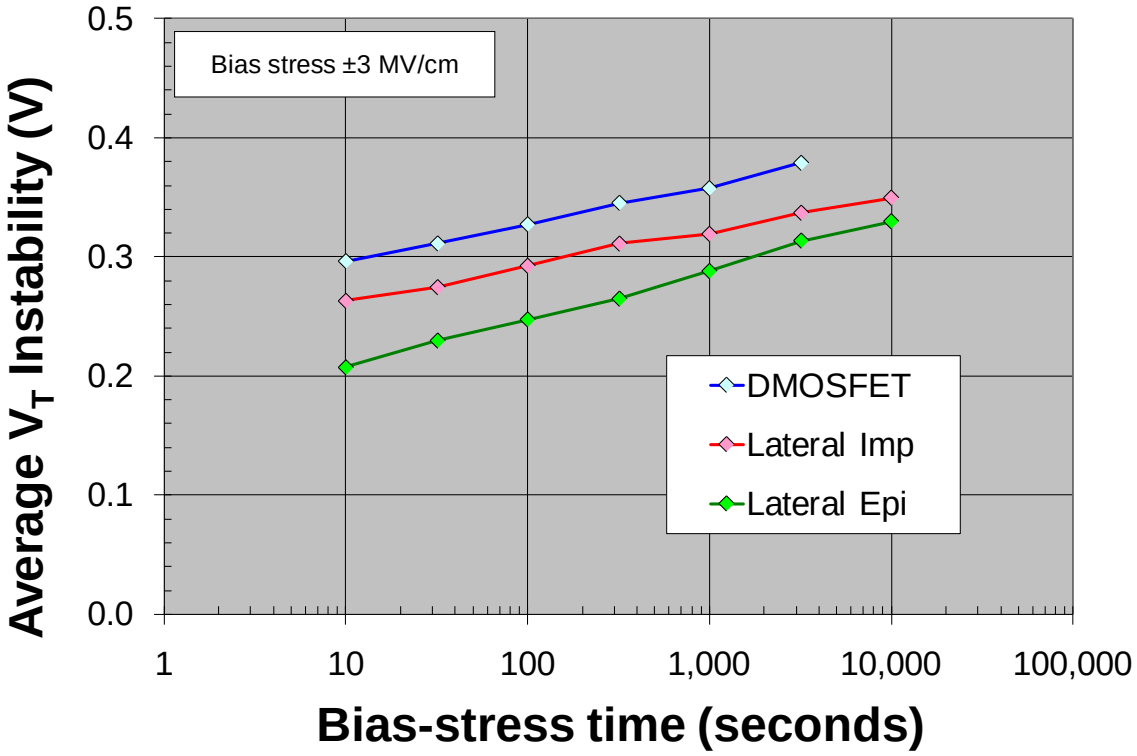

Figure 7-4: Comparison of the average threshold-voltage instability of several 5-A SiC DMOSFETs with that of lateral MOSFETs with and without an implanted channel vs bias-stress time, calculated by finding the shift in the linearly extrapolated V_T.

Figure 7-5 shows the effect of the magnitude of the gate-bias stress on 20-A devices. The bottom curve is of a device stressed with ±15 V on the gate (±2 MV/cm). Stressing with ±23 V (top diamond curve, ±3 MV/cm) applied to the gate leads to an increase in the instability of between 0.1 and 0.2 V. This response is similar to that presented on lateral test structures (see Figure 4-9). Similar variations of V_T shift with stress time on newer 50-A devices have also recently been reported [53]. These similar

results on fully processed SiC power MOSFETs indicate that the same charge trapping and de-trapping effect via a direct tunneling mechanism is in all likelihood occurring.

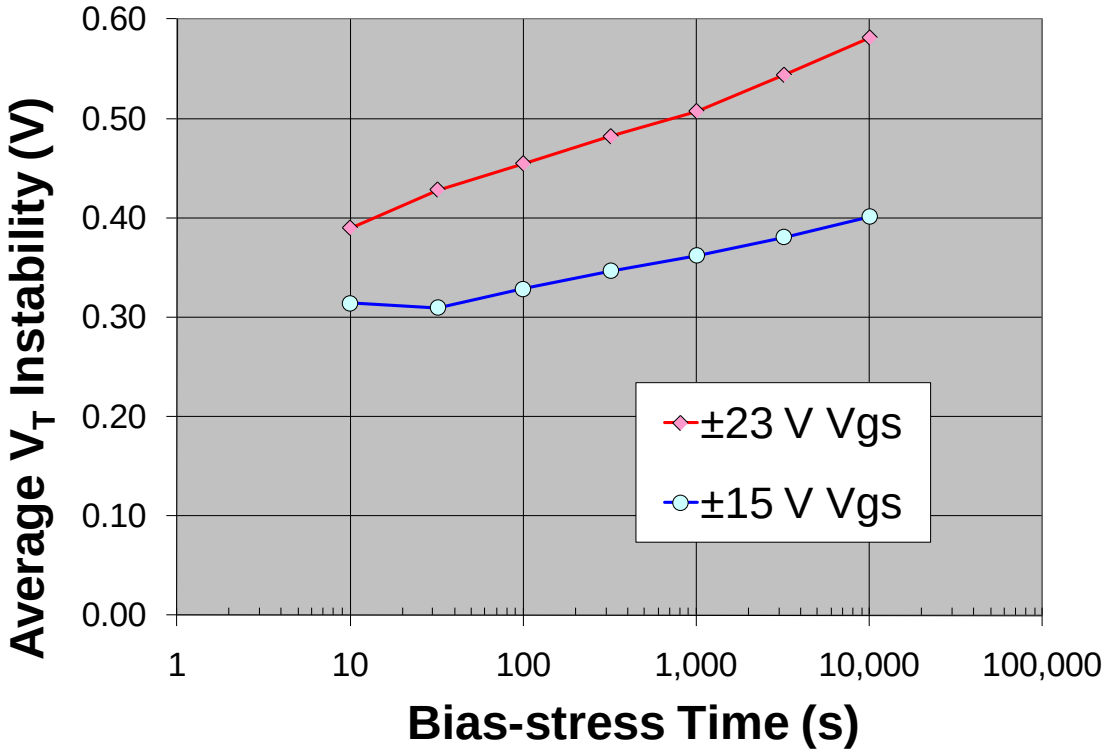

Figure 7-5: Average threshold-voltage instability for the 20-A SiC DMOSFET vs stress time as a function of gate-bias stress, calculated by finding the voltage shift for a constant current of 90 μA.

7.3 Effect of *ON*-state current stress on the threshold-voltage instability in SiC power DMOSFETs

The work in the previous section showed that a simple gate-bias stress at room temperature with no current flowing can cause significant shifts in the threshold voltage of SiC DMOSFETs. Since the actual device stress condition under positive bias is in the

ON state, it is important to investigate the magnitude of the instability with drain current flowing and compare it to a simple gate-bias stress.

An initial investigation of *ON*-state current stressing was reported several years back, and researchers did observe a slight degradation of the *ON*-state I_D-V_{DS} characteristics following several hundred hours of stress time [126]. However, their measurement procedure was such that they likely mitigated a significant part of the response by following a positive bias *ON*-state stress with the measurement of a family of I_D-V_{DS} curves starting with V_{GS} = 0 V. For similar reasons, they did not observe a significant shift in the I_D-V_{GS} characteristics. As discussed in Chapters 4 and 5, the bias applied during the measurement can significantly affect the result of the bias during stress.

Figure 7-6 shows the experimental procedure used for the *ON*-state bias-stress testing. For the *ON*-state stress, in addition to the positive gate bias, a voltage is applied to the drain (typically 1.5 to 2.0 V) of the DMOSFET to allow the rated current to flow from source to drain. The remainder of the sequence is the same for both tests: the gate is swept down in voltage to measure the new I_D-V_{GS} characteristic; a negative gate-bias stress of equal duration to the positive-bias stress is then applied—this time with the source and drain grounded, followed by a final measurement with the gate swept up in voltage. As before, all the measurements were performed at room temperature with an Agilent 4155 using a high power measurement unit, with a small V_{DS} of 50 mV applied. It took approximately 1 second to perform the measurement.

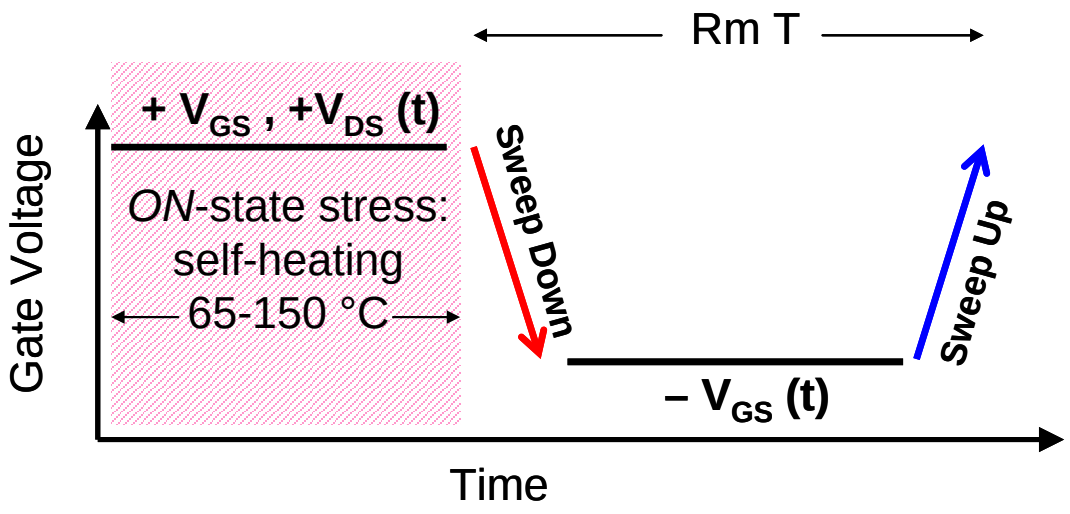

Figure 7-6: Stress-and-measurement sequence employed to investigate the effect of *ON*-state stressing on the threshold-voltage instability of SiC power DMOSFETs (compare with Figure 7-3 for the gate-bias stress-and-measurement sequence).

Figure 7-7 plots the instability due to this *ON*-state stress for a range of stress times, from 100 to 10,000 seconds, and compares it to the instability due to a simple gate-bias stress with no current flowing. The *ON*-state stress does cause a larger instability, increasing by about 20 to 25 percent. The difference between the two stresses increases with increasing stress time; the simple gate-bias stress results show the typical linear-with-log-time response whereas the *ON*-state stress results appear to be accelerating somewhat with increased stress time. This effect is due primarily to an increasing positive shift of the I_D-V_{GS} characteristic during the *ON*-state or positive-bias stress with stress time, indicating that an additional mechanism may be coming into play. On the other hand, there is very little shift to the left compared with the initial values. This last result is consistent with the effect of bias stress polarity for modern thermal oxides shown in Figure 4-11. In this case, the threshold-voltage instability was calculated by comparing the shift in V_{GS} when I_D = 0.1 A.

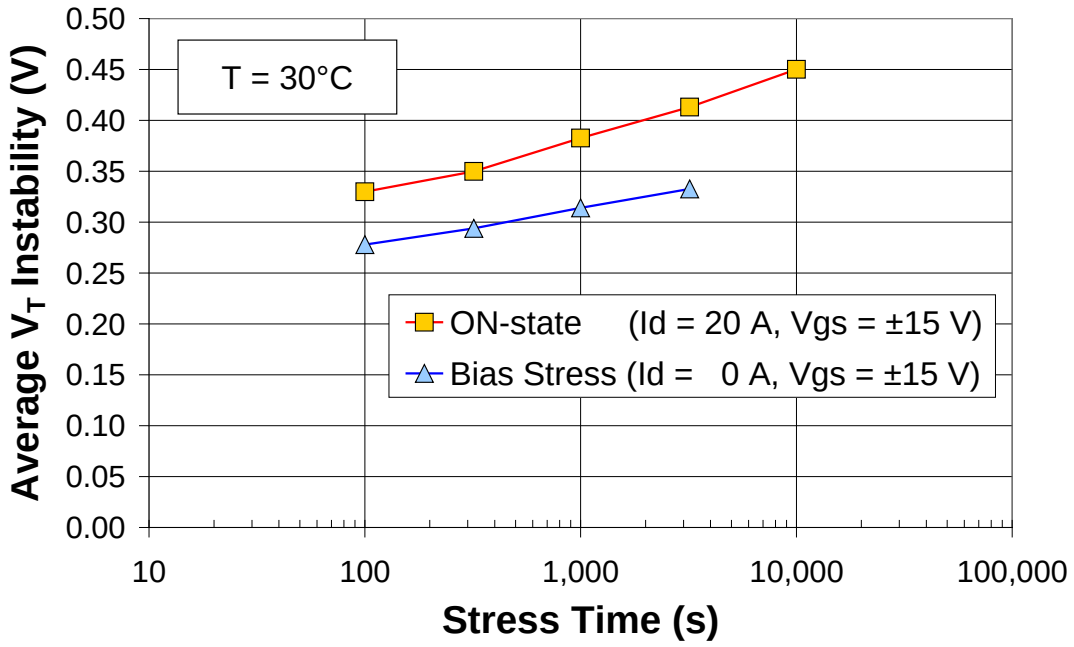

Figure 7-7: Comparison of V_T instability in a DMOSFET due to *ON*-state stressing, with 20 A flowing, and that due to simple gate-bias stressing, with V_{DS} = 0 V. In each case V_{GS} = +15 V was applied during the first half of the stress, and a simple negative gate-bias stress with V_{GS} = –15 V and V_{DS} = 0 V was applied during the second half of the stress.

The threshold-voltage instability can be much larger when calculated by comparing the shift in V_{GS} when $I_D = 1\times10^{-5}$ A, to quantify the effect of the stress on the subthreshold *I-V* characteristics. This is shown in Figure 7-8. A direct comparison shows that the instability of the *I-V* characteristic due to *ON*-state stressing is about twice as large at the much lower current level. This is due to a significant stretch-out of the subthreshold *I-V* characteristics following the negative gate bias stress at longer stress times. This result suggests that under actual operating conditions, an even larger positive threshold voltage margin will be needed to prevent leakage in the *OFF* state.

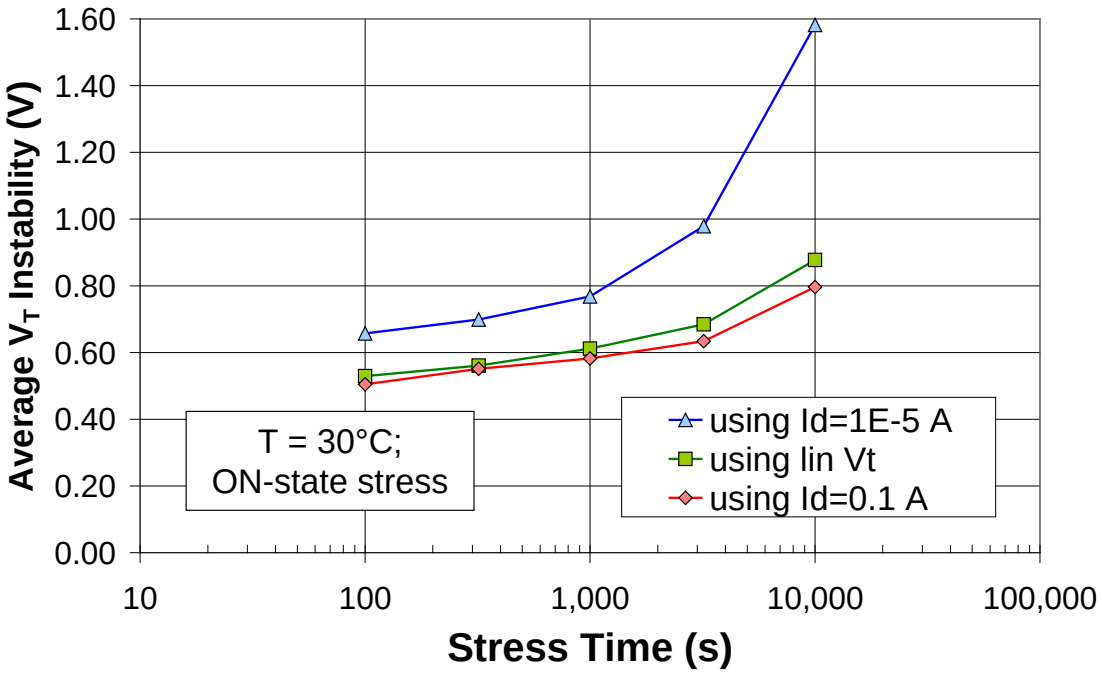

Figure 7-8: Comparison of *ON*-state stress induced voltage instability when measured using three different methods: for I_D = 1×10^{-5} A, for I_D = 0.1 A, and finding V_T by extrapolating the linear *I-V* curve to zero current.

Figure 7-9 shows a comparison of the back-and-forth instability of the actual subthreshold *I-V* characteristics for a state-of-the-art 50-A SiC MOSFET which has been subjected to a very long 10,000-s *ON*-state stress (see Figure 7-6 for the *ON*-state stress experimental sequence), along with 10,000-s gate-bias stress instability measurements before and after the *ON*-state stress (see Figure 7-3 for those gate-bias stress experimental sequences).

It is clear that the application of the *ON*-state stress causes an increased instability in both directions and a significant increase in the stretch-out of the *I-V* characteristic under negative bias. As discussed in Chapter 5, this larger stretch-out when sweeping up in gate bias is likely due to oxide traps filling during the measurement. The increase in

this stretch-out following the *ON*-state stress may be due to an increase in the number of active oxide traps, to be discussed more fully in a later section below.

It is also interesting to note that for the gate-bias stress only sequence (see again Figure 7-3) following the *ON*-state stress sequence, the *I*-*V* characteristic following positive-bias stress has moved significantly back to the left; and the *I*-*V* characteristic following long negative bias-stresses moves even further to the left.

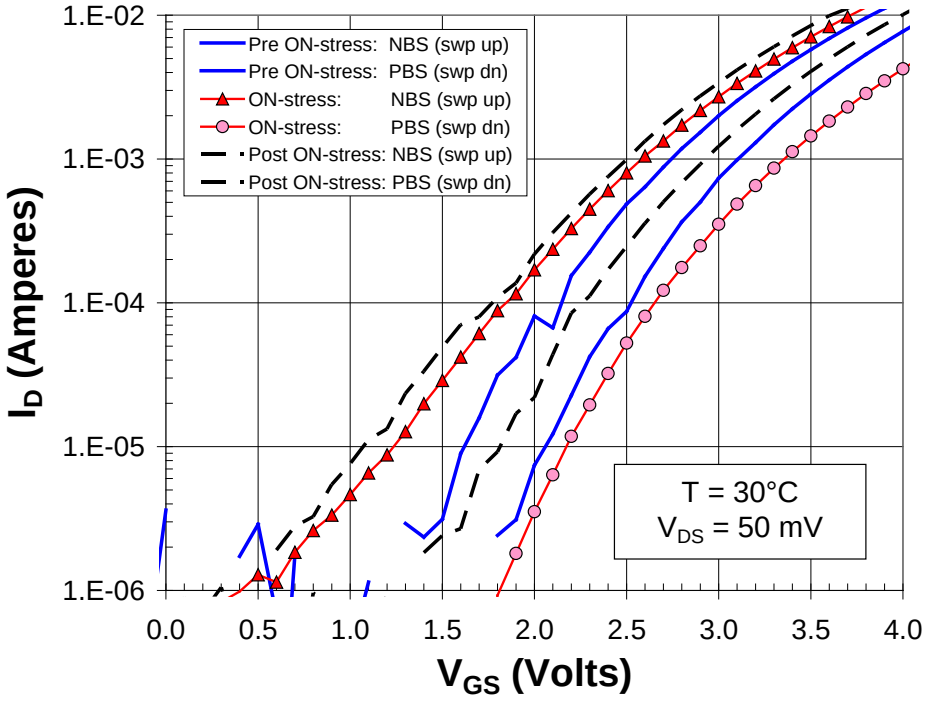

Figure 7-9: Gate-bias stress subthreshold I_D-V_{GS} instability characteristics of a 50-A SiC power MOSFET as the result of an *ON*-state stress test. Pre- and post-*ON*-state-stress measurements are shown as well.

Figure 7-10 shows similar results for a 20-A device, with the gate voltage required to achieve a drain current of 1×10^{-5} A plotted for a sequence of gate-bias instability measurements: before (Pre), immediately after (During), and a day after (Post) the application of an *ON*-state current stress. In this case, the stress time is plotted on a linear time scale and is not re-started at the beginning of each of the three segments, thus

representing cumulative stress time. As a result, the initial increase in the back-and-forth instability of the *I-V* characteristic with increasing gate-bias stress time (first of the three segments) does not look linear. However, the instability clearly does increase with stress time, and that instability increases dramatically with the application of the *ON*-state stress (middle segment).

But as was the case for the results shown in Figure 7-9 above, when the gate-bias stress is repeated a day later (third segment), the *I-V* characteristic following a positive-bias stress has initially moved significantly back to the left before once again moving to the right with increasing bias-stress time. This overnight shift occurred without bias being applied to the gate.

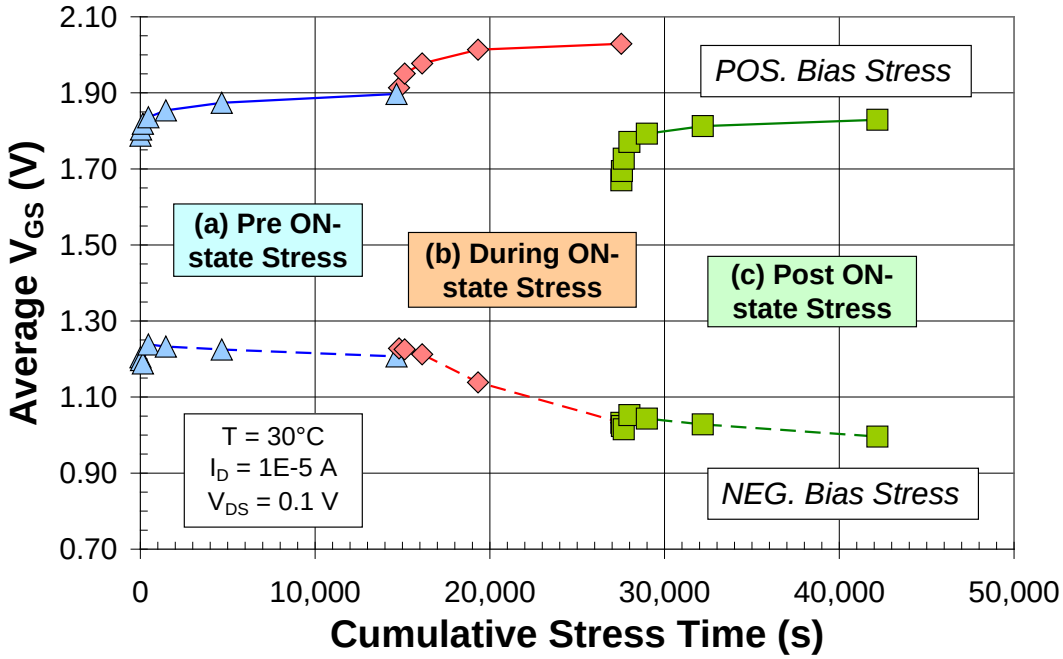

Figure 7-10: Gate voltage required for $I_D = 1\times10^{-5}$ A (with V_{DS} = 0.1 V) of a 20-A SiC DMOSFET during a measurement following both positive and negative-bias stress: (a) before (Pre) an *ON*-state stress, (b) immediately after (During) an *ON*-state stress, and (c) a day after (Post) an *ON*-state stress. The cumulative stress time is plotted on a linear scale.

To further investigate this curious effect, the instability in the gate voltage required to obtain a drain current of 1×10^{-5} A for a 50-A MOSFET is plotted in Figure 7-11 for both an *ON*-state current stress sequence, and for a series of separate 10,000-s regular gate-bias stress sequences immediately following. Again, note the sharp increase in instability under the longest *ON*-state current stress, due to a greater shift of the *I-V* characteristic in both directions, but especially under negative bias. The magnitude of this back-and-forth instability begins to rapidly decrease during the subsequent sequence of 10,000-s gate-bias-only stresses. This is primarily due to a negative shift in the *I-V* characteristic following the positive gate-bias stress, as was seen in Figure 7-9 and Figure 7-10. This type of behavior is only observed following the termination of an *ON*-state stress, suggesting that a different or additional mechanism is affecting the instability in this case. Although a large current flows during the *ON*-state, the drain-to-source bias is no more than 2 V and the field in the gate oxide is no more than 2 MV/cm. This effect may be due either to the deactivation of some oxide traps over time once the device is back at room temperature, or to the possible annealing of some interface traps.

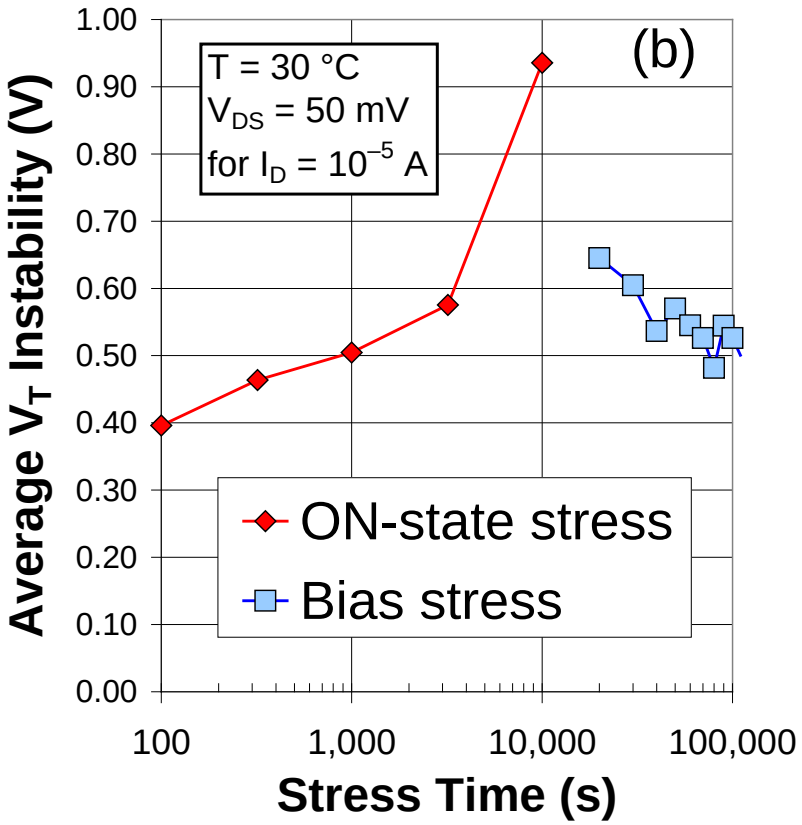

Figure 7-11: Subthreshold instability of a 50-A SiC DMOSFET versus variation in stress time for an *ON*-state stress, followed immediately by several 10,000-s gate-bias stress sequences plotted versus cumulative stress time.

A comparison of the *ON*-state stress-induced instability in the subthreshold region (I_D = 1×10^{-5} A) between the 20-A and 50-A MOSFETs discussed above is shown in Figure 7-12. The 50-A device has a smaller instability. Judging by the results of an infra red (IR) thermal camera [127], these devices clearly underwent self-heating and required active cooling during the *ON*-state testing, with the 20-A device running much cooler (65 °C vs 145 °C) even though the current densities were similar. The results of a second 50-A device, which ran at an intermediate temperature (100 °C), are also shown in Figure

7-12. This suggests that temperature during the stress (all the measurements were made at 30 °C) is likely an important factor.

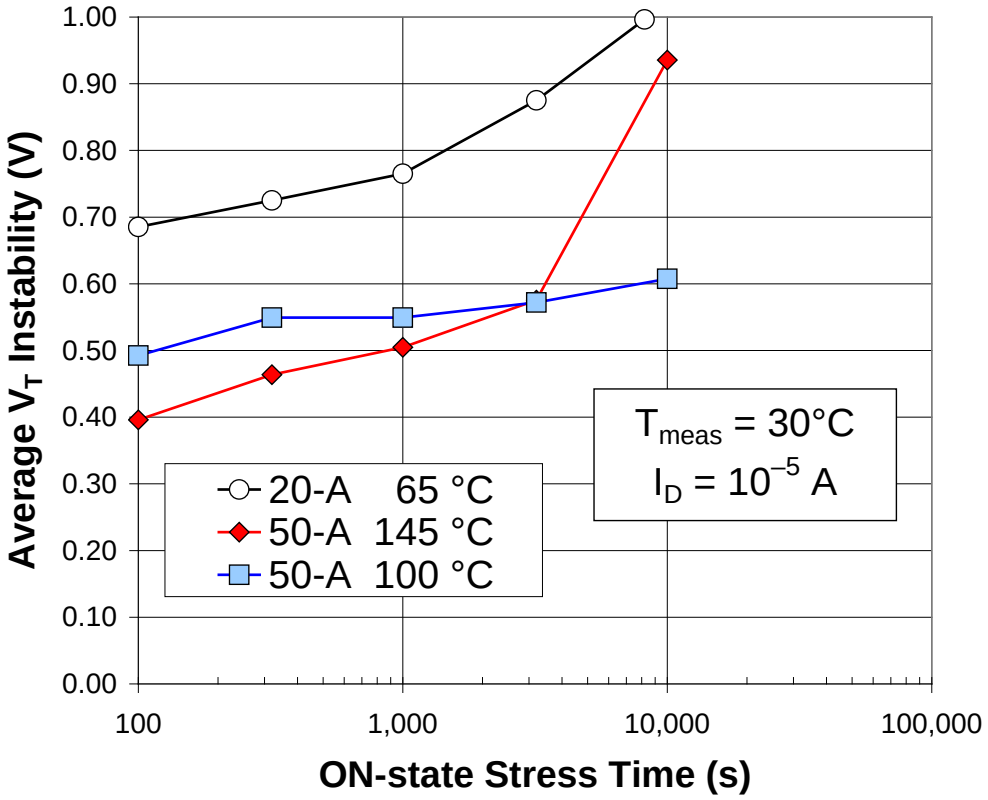

Figure 7-12: Subthreshold instability of various SiC DMOSFETs during an *ON*-state stress. Temperature variation is due to variations in self-heating, measured using an IR thermal camera.

These results suggest that not only does the *ON*-state stressing of a SiC DMOSFET increase the threshold-voltage instability due to increased charge trapping, but that the long-term effect is to shift the whole envelope of back-and-forth subthreshold *I-V* characteristics to the left. Whether the overall effect is to increase the amount of positive oxide trap charge or to decrease the amount of negative interface trap charge, the margin for *OFF*-state leakage current is clearly less following *ON*-state stressing.

7.4 High-temperature emulation of *ON*-state stress

It was shown in the previous section that *ON*-state stressing, where the rated current flows through the channel during the stress, resulted in a larger V_T instability than that due to gate-bias stressing alone. It was also shown that device temperatures increased during the *ON*-state stress and that at the highest device temperature this instability increased noticeably at longer total stress times. In order to confirm that it is the increase in device temperature that is the primary cause of the increased back-and-forth instability effect, a high-temperature emulation of the *ON*-state stress, with no channel current, was performed.

Similar 50-A 4H SiC power DMOSFETs as were used for the *ON*-state stress tests discussed in the previous section were subjected to the following high-temperature and bias-stress testing sequence, as shown in Figure 7-13. The test method used to perform *ON*-state stress measurements was closely emulated (compare with Figure 7-6), except that instead of allowing the rated current to flow through the device, the device under test (DUT) simply had a positive gate-bias stress applied and was heated to 150 °C to simulate the self-heating effect of the *ON*-state stress. Following the positive-bias stress, the DUT was quickly cooled down to room temperature in about one minute and the I_D-V_{GS} characteristic was measured, with the gate swept down in voltage. This was then followed by a negative gate-bias stress at room temperature of equal duration to the positive-bias stress previously applied, with –15 V on the gate and the source and drain again grounded; followed by a second measurement of I_D-V_{GS} with the gate swept up in voltage. Room temperature gate bias stress-and-measure bias instability sequences (see

Figure 7-3) were also performed both before and after the high-temperature-stress test method.

Once again, all the measurements were performed with an Agilent 4155, with a small V_{DS} of 50 mV applied. The threshold-voltage instability in this study was calculated both by comparing the shift in V_T using the standard linear *I-V* extrapolation method to zero current ("V_T method"), as well as by the shift in V_{GS} when $I_D = 1\times10^{-5}$ A ("V_{GS} method") in order to quantify the effect of the stress on the subthreshold *I-V* characteristics.

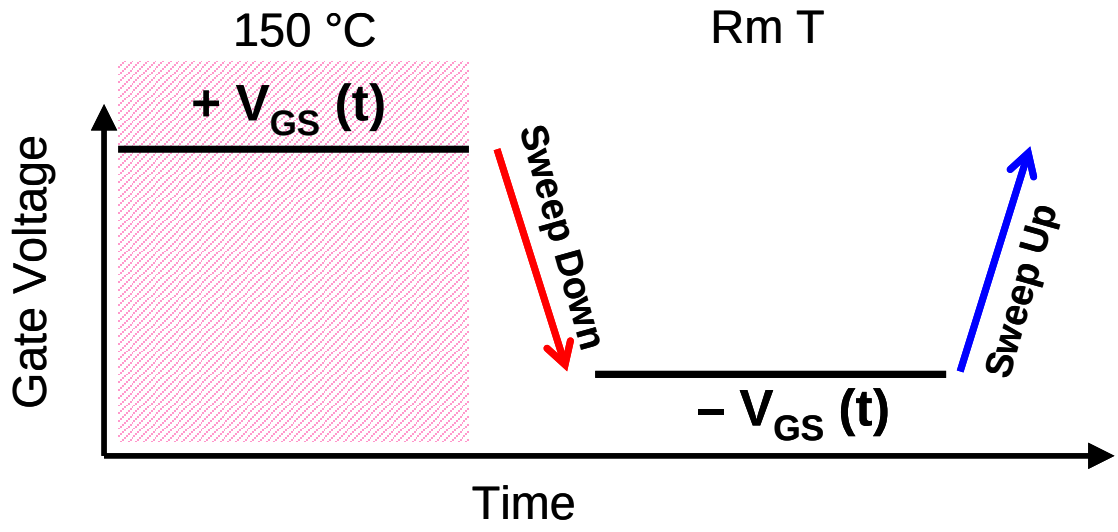

Figure 7-13: Stress-and-measurement sequence employed to investigate the effect of an emulated *ON*-state stressing on the threshold-voltage instability of SiC power DMOSFETs (compare with Figure 7-6).

Figure 7-14 shows the back-and-forth instability of the I_D-V_{GS} characteristics, plotted on a log current scale, when subjected to a 10,000-s high-temperature emulation of the *ON*-state stress. The curve for the room-temperature measurement following the positive gate-bias stress at 150 °C is at the far right (lightly shaded circular symbols) and

the curve following the negative-bias stress is at the far left (darkly shaded triangular symbols). Also shown are room-temperature stress-and-measure bias instability curves for measurements performed both before (solid lines) and long after (dashed lines) the emulated *ON*-state stress sequence, also with stress periods of 10,000 s.

Clearly, the emulated *ON*-state stress causes a significant shift to the right following positive-bias stress as well as a significant shift to the left following negative-bias stress compared to the pre-stress curves. In addition, the subthreshold *I-V* characteristic is significantly stretched-out following the negative-bias stress. In this case, the subthreshold *I-V* characteristic is also clearly stretched-out to some extent following the positive gate bias stress when compared to the pre-emulated *ON*-state stress values. This may be evidence either for a very large increase in the number of active oxide traps, or to the creation of additional interface traps during the high-temperature stress [89, 128].

The post emulated *ON*-state stress measurements, taken long after the high-temperature stress, show a significant shift back to the left following a positive-bias stress, but no discernible change following a negative-bias stress, including the permanent looking stretch-out of the subthreshold *I-V* characteristic. These results are very reminiscent of those for the actual *ON*-state stress.

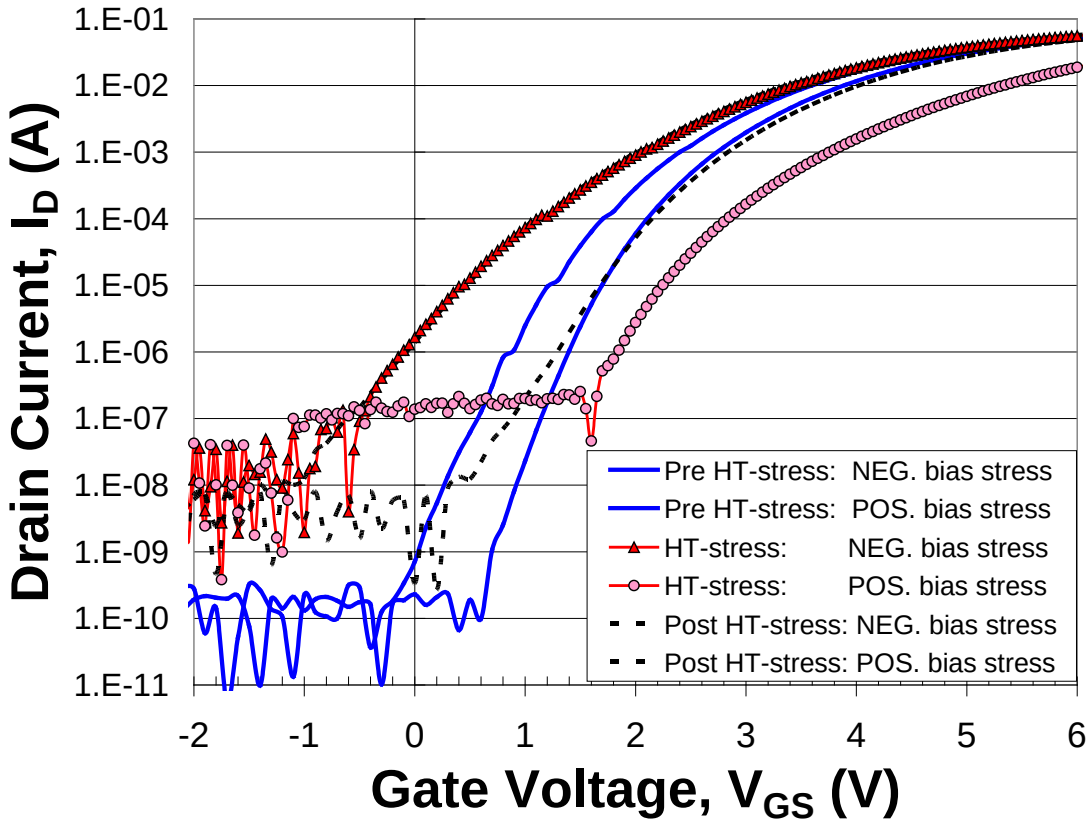

Figure 7-14: Example of the instability in the I_D-V_{GS} characteristics of a power MOSFET as the result of a high-temperature-stress emulation of an *ON*-state stress test. Pre- and post-high-temperature-stress measurements are shown as well.

Figure 7-15 and Figure 7-16 depicts the back-and-forth instability due to the emulated *ON*-state stress depicted in Figure 7-13 as a function of stress time. The total instability is shown in Figure 7-15, and is seen to follow the typical high-temperature result—that the total instability increases faster than the linear-with-log-stress-time rate seen at room temperature (compare with Figure 7-11 and Figure 4-22).

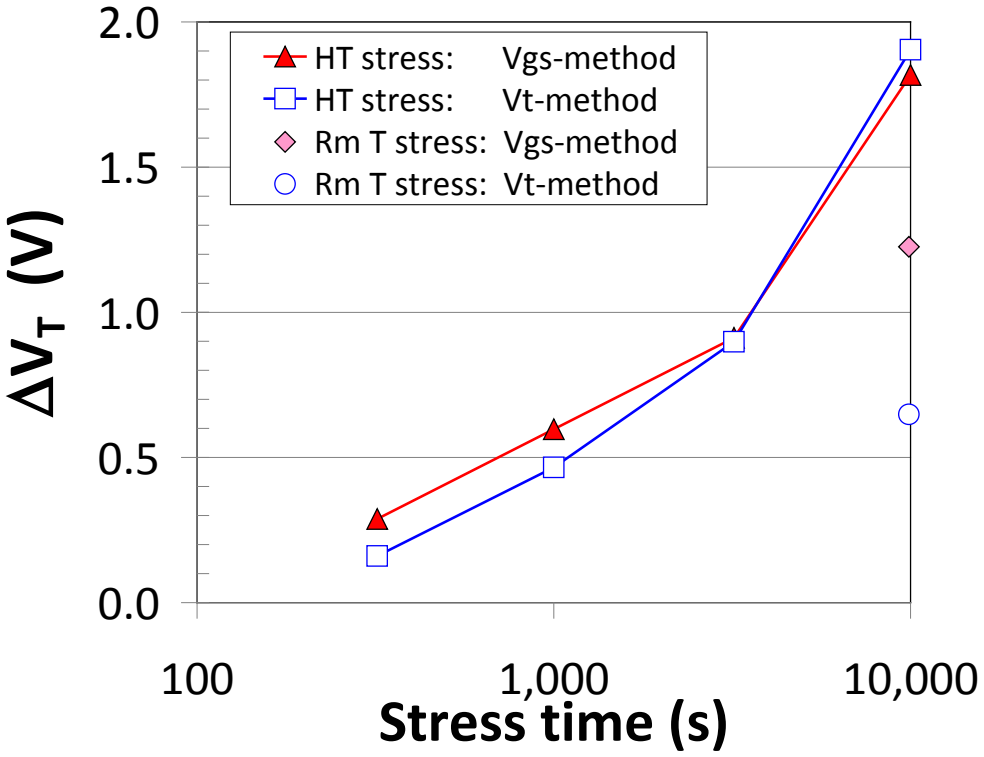

Figure 7-15: Comparison of the total back-and-forth instability of the I_D-V_{GS} characteristics versus stress time for a high-temperature-stress emulation of the *ON*-state stress calculated using both the V_T and V_{GS} analysis methods.

Figure 7-16 shows that the majority of this increased instability is due to a shift to the right under positive bias when measured on a linear current scale, but a shift to the left under negative bias when measured on a log scale. This implies that both the *ON*-state resistance and *OFF*-state leakage current are increasing with increasing high-temperature stress time. It is also interesting to note that although the envelopes of the back-and-forth instability shift differently for the two methods of analysis, the total instabilities increase at the same rate in this case. Figure 7-15 also shows the post high-temperature stress results of a simple room temperature gate-bias stress as described in

Figure 7-3. In this case, there is a noticeable difference, with the back-and-forth instability decreasing sharply when measured on a linear current scale (V_T method).

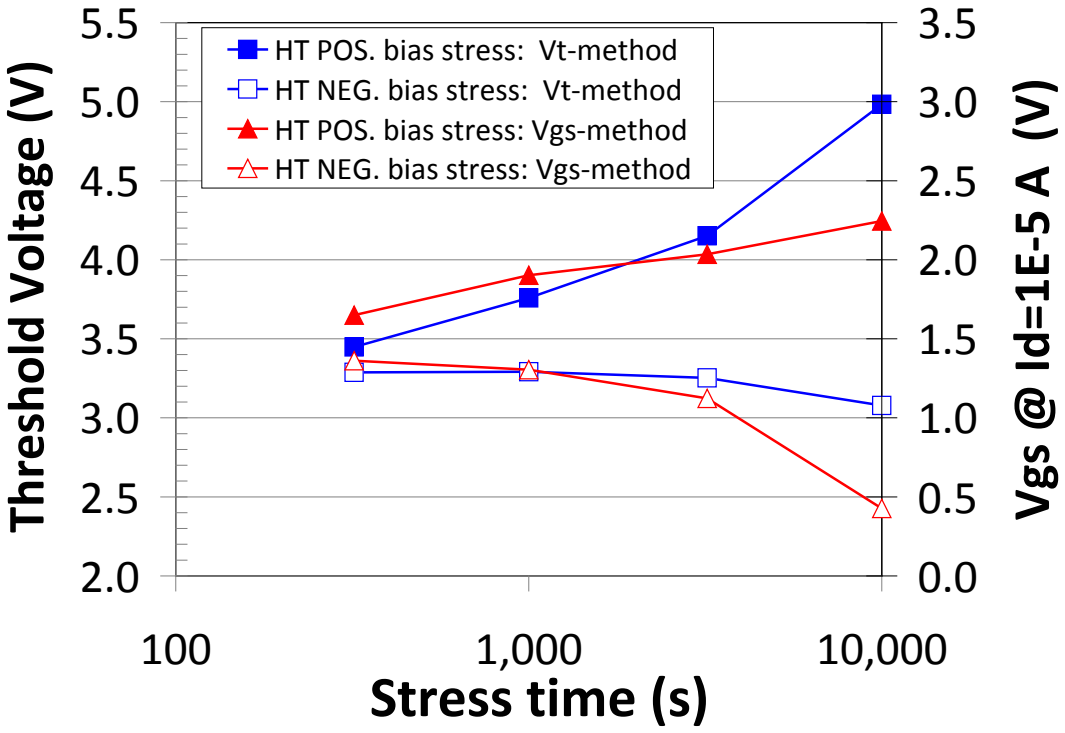

Figure 7-16: Comparison of the shift under both positive and negative-bias stress of the I_D-V_{GS} characteristics versus stress time for a high-temperature-stress emulation of the *ON*-state stress calculated using both the V_T and V_{GS} analysis methods.

In summary, the results depicted in Figure 7-14 through Figure 7-16 are in general very similar to those reported previously for devices subjected to an *ON*-state stress, strongly suggesting that the increased instability observed is due primarily to self-heating and not to the presence of a large current flowing from source to drain.

7.5 Degradation of *ON*-state characteristics

Figure 7-17 shows the *ON*-state I_D-V_{DS} characteristics for a 20-A DMOSFET. The arrow points to the gap between the V_{GS} = 14 V and V_{GS} = 16 V curves. The results reported here show DMOSFET V_T instabilities generally between 0.25 and 0.5 V. This correlates very well with the instabilities observed in similarly processed lateral MOSFETs. We know that the actual instability (difficult to measure because of the counter-acting effect of the gate bias during the measurement) can be three or more times larger. But suppose that the actual shift in V_T is about 1 V. If V_T was originally set to preclude the chance of turning on the subthreshold current in the blocking state, then the practical effect of a threshold-voltage shift would be to reduce the effective gate voltage applied in the *ON* state. But Figure 7-17 shows that even a shift of 1 V would only lead to an increase in V_{DS} of about 0.1 V, from about 1.9 to 2.0 V. This would increase the *ON*-state losses about 5 percent, which should be manageable for power converter applications.

Figure 7-18 in fact shows the change in the I_D-V_{DS} characteristic with V_{GS} = 15 V before and after a 1-hour *ON*-state stress. V_{DS} must increase about 0.1 V following the stress to maintain 20 A of drain current. This is the same result as derived from Figure 7-17, which results in about a five percent increase in $R_{DS,ON}$.

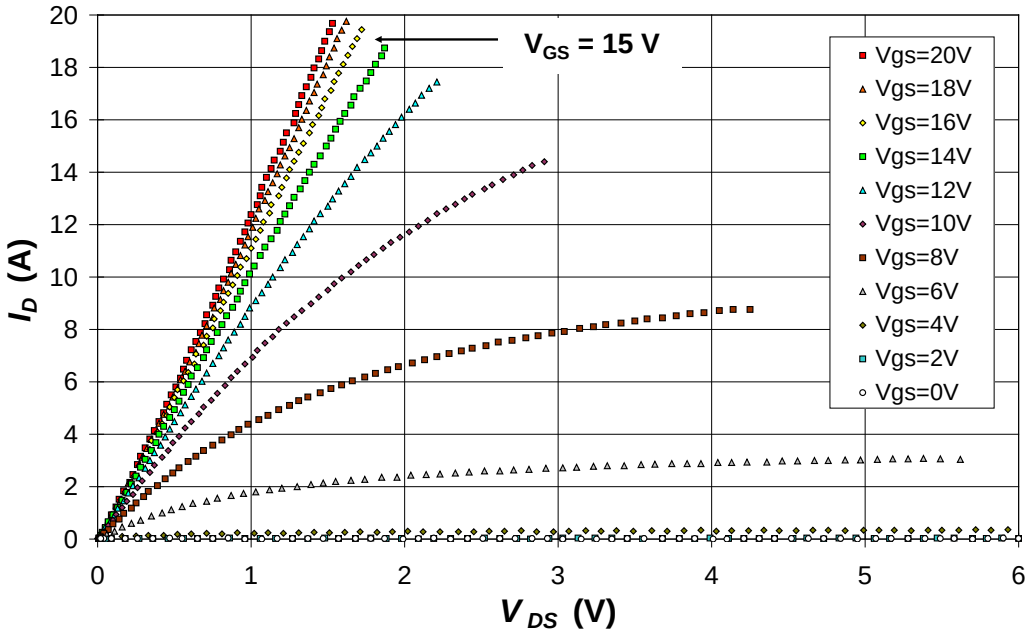

Figure 7-17: *ON*-state I_D-V_{DS} as a function of V_{GS}. The effect of the V_T instability would be to increase the *ON*-state resistance only by a few percent.

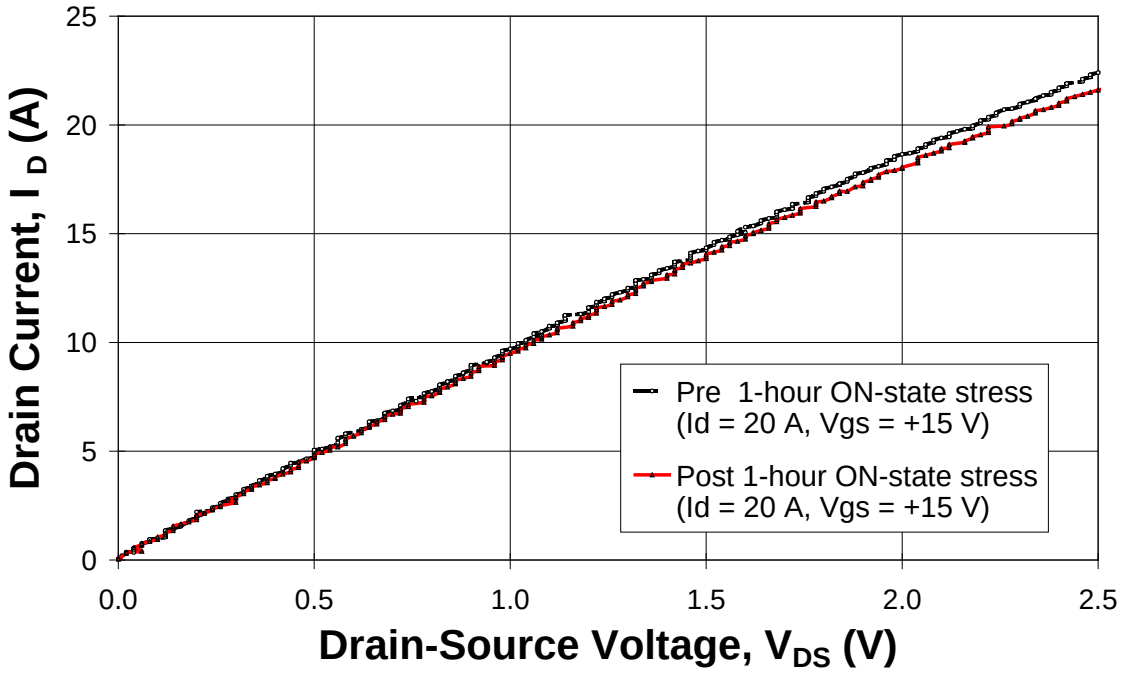

Figure 7-18: A 1-hour *ON*-state stress leads to an increase in *ON*-state resistance. V_{DS} must increase about 0.1 V following the stress to maintain 20 A of drain current.

7.6 High-temperature bias-stress mechanisms

With the significant and super-linear increase with log time of the V_T instability that has been observed when stressing at elevated temperature in both power DMOSFETs (see Figure 7-8, Figure 7-11, and Figure 7-15) and lateral test structures (see Figure 4-22), it is critical to understand and limit the underlying basic mechanism(s). Especially since SiC power MOSFETs are expected to operate reliably at elevated temperatures, and an increased V_T instability can lead to increased leakage current in the *OFF* state and possibly to device failure.

At first glance, this large increase in V_T instability at elevated temperature is unexpected, since the direct tunneling mechanism described in Chapter 6 that successfully explains the V_T-instability effect at room temperature should not be very sensitive to temperature. In this model, electrons are simultaneously tunneling to and from near-interfacial oxide traps that vary spatially with distance from the SiC interface, and with the local oxide field and the fraction of filled or empty traps determining which mechanism dominates.

However, very recent results in the literature may provide key clues to explaining this strong temperature sensitivity. First, it has been reported that *E'*-type oxide defects that are associated with an O-vacancy have been observed in SiC MOSFETs using electrically detected magnetic resonance techniques [61]. No other type of oxide defect has yet to be found using any ESR technique. Since this was the main type of oxide defect in irradiated Si MOSFETs, which showed a similar type of V_T-instability effect that was successfully explained using a tunneling model [88, 89, 90], it is likely that this is the same general mechanism that is occurring in SiC MOSFETs. Especially given the

experimental evidence described in Chapters 4 and 5, including: the linear-with-log-time increase in V_T instability with stress time, the extrapolation to zero V_T instability to stress times comparable with the first tunneling transition times, and the larger observed V_T instability with faster measurement times.

Second, it has also been recently reported using on-the-fly electron spin resonance techniques in the study of NBTI in Si MOS that the number of these E' centers increased dramatically with bias at an elevated temperature of 100 °C, but not with temperature stress alone [96]. In addition, they found that the number of oxide defects markedly decreased when the sample was returned to room temperature. This result may in fact explain the unexpected increase in the V_T instability at elevated temperature.

To further test this theory, the following experiment was very recently performed [51], consisting of a two-step stress sequence (see Figure 7-19). First, the device was subjected to a 150 °C high-temperature stress for varying periods of time, with or without a positive gate bias applied. Second, a simple gate-bias stress-and-measure instability sequence was applied—except that the whole sequence was performed at 150 °C. The positive and negative-bias stress periods were a constant 60-s long, regardless of how long the previous temperature stress was. Room temperature stress-and-measure bias instability sequences were also performed, both before and after the high-temperature-stress test method.

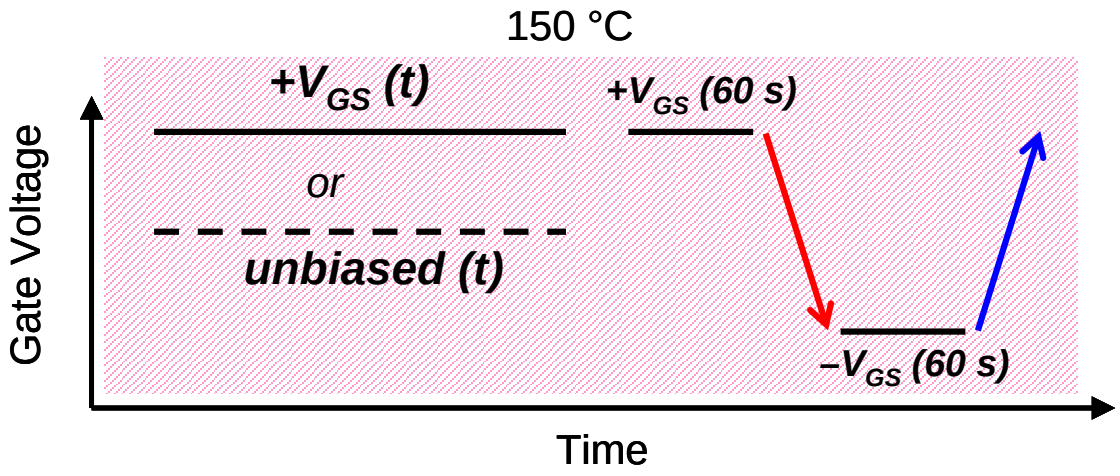

Figure 7-19: Short stress-and-measurement instability sequence to determine effect of high-temperature stress with or without applied gate-bias stress.

Figure 7-20 and Figure 7-21 present the results of this test method, depicted in Figure 7-19, for determining the effects of bias stress at elevated temperature. Figure 7-20 shows that when bias is applied during the time-dependent high-temperature stress, the total back-and-forth instability once again increases super-linearly with log time, as in Figure 7-15 for example, although for this test method it takes one hundred times longer to see a similar increase in the magnitude of the instability since the 60-s stress-and-measurement sequence used to measure the effect is so much shorter. Interestingly, there is practically no increase in the total instability when no bias is applied during the 150 °C time-dependent stress. Figure 7-21 shows that once again there is an increase in both the positive shift following positive bias and the negative shift following negative bias during the stress-and-measurement sequence used to measure the effect of the stress, although in this case there is no noticeable difference regardless of whether the V_T instability is measured on a linear current scale (using the V_T method) or on a logarithmic current scale (using the V_{GS} method) for these high temperature measurements.

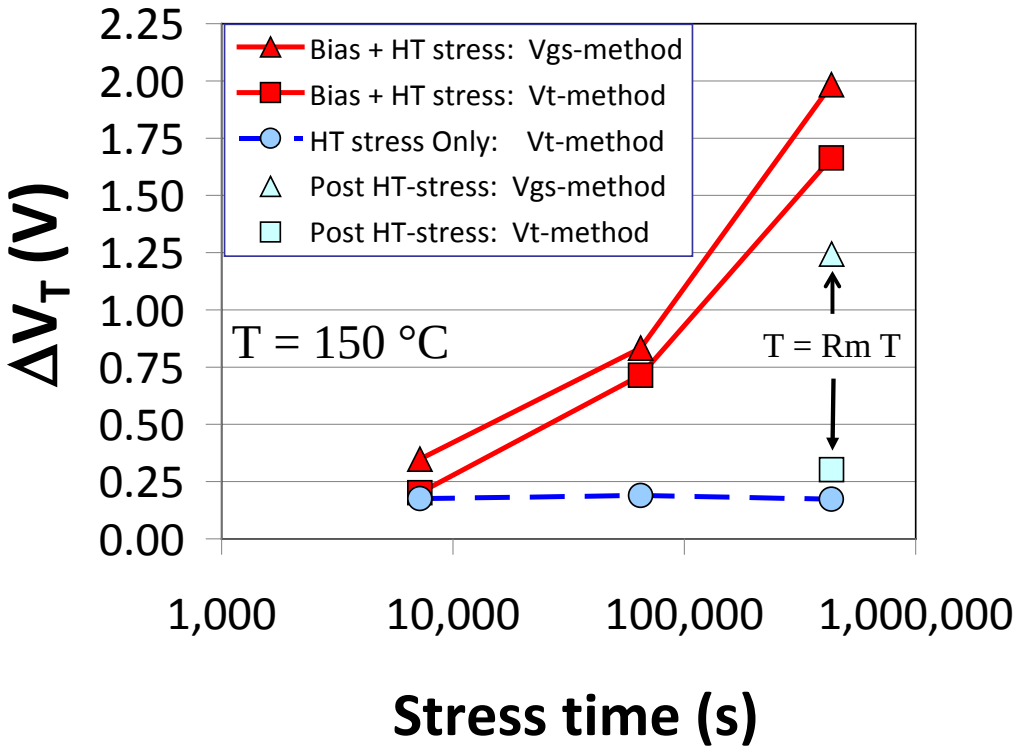

Figure 7-20: Short stress-and-measurement instability sequence to determine effect of high-temperature stress with or without applied gate-bias stress.

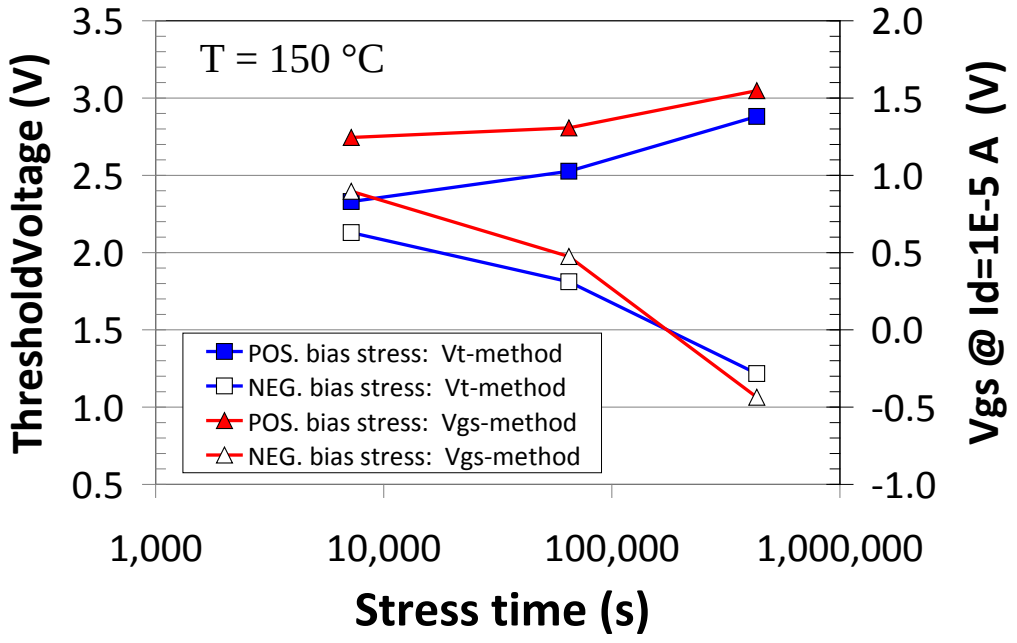

Figure 7-21: Short stress-and-measurement instability sequence to determine effect of high-temperature stress with or without applied gate-bias stress.

These experimental results are consistent with the recent results in the literature. The V_T instability only increases at high temperature when bias is applied, and the subsequent room temperature instability is much smaller, especially when measured using the V_T method. Since the V_T instability is likely a measure of the number of active near-interfacial oxide traps—keeping in mind that faster *I-V* measurements reveal more total traps, these results suggest that this increase in threshold-voltage instability at elevated temperature is due to the activation of additional near-interfacial oxide traps related to the *E'*-center defect. If this is so, then it is important to develop improved processing methods to either decrease the number of precursor oxide defect sites, by somehow increasing the O concentration in the interfacial layer or tying up the dangling bonds as the NO anneal may do, or to reduce the bond strain in this region of the oxide so that pre-cursor Si-Si bonds are less likely to break.

Otherwise, an increased negative shift can give rise to increased leakage current in the *OFF*-state and potential device failure if proper precautions are not met to provide an adequate margin for the threshold voltage. Of course, increasing V_T too much will lead to an unnecessary increase in *ON*-state resistance and reduced device performance. Therefore, it is important to also develop improved test methods that will more accurately ensure device reliability.

If the activation of additional oxide traps can be properly quantified with respect to temperature and oxide field (see Chapter 8: Future work), and if the critical leakage current causing device failure is known, then the time-to-failure due to negative-bias temperature stress could be determined.

The change in the log of the drain current can be found from the change in the threshold voltage in the subthreshold region using Equations (3-56) and (5-4), dependent of course upon the initial threshold voltage and how much voltage shift is required to raise the drain current above the noise floor. The change in threshold voltage due to a change in oxide trap charge is given by (4-1), yielding the following relationship between the change in oxide-trap charge and drain current.

$$\Delta \log(I_D) = \frac{-\Delta V_T}{S} = \frac{q \cdot \Delta N_{OT}}{S \cdot C_{OX}} \tag{7-1}$$

For a uniform spatial distribution of oxide traps, the change in drain current as a function of time is, using (6-9) and (6-10), given by

$$\Delta \log(I_D) = \frac{-\Delta V_T}{S} = \frac{q \cdot \Delta N_{OT}}{S \cdot C_{OX}} = \frac{q}{S \cdot C_{OX}} \cdot \frac{N(t)}{2 \cdot \beta} \cdot \ln\left(\frac{t}{t_0}\right) \tag{7-2}$$

where *N(t)* is the volumetric active oxide-trap density which increases with time at temperature, as a function of applied bias.

A schematic of the increase in the number of positively charged oxide traps with time under negative bias at high temperature, due to both the tunneling front extending deeper into the oxide and an increase in the number of active traps, is shown in Figure 7-23.

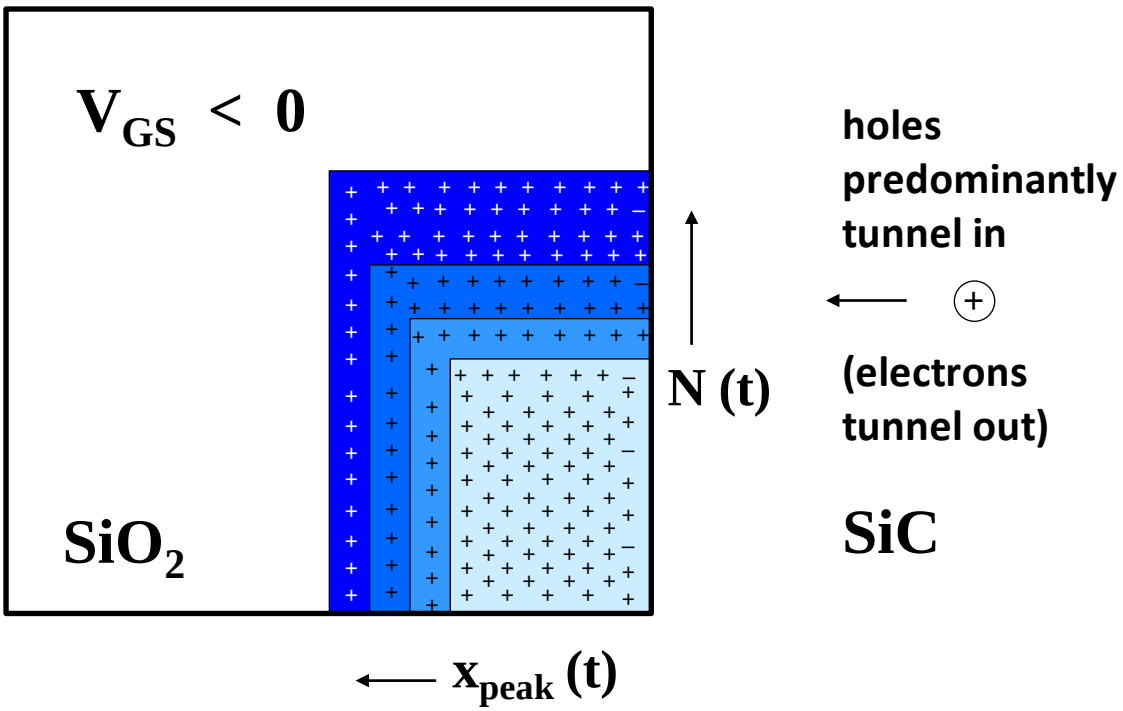

Figure 7-22: Schematic showing the increase in the number of positively charged oxide traps with time under negative bias at high temperature, due to both the tunneling front extending deeper into the oxide and an increase in the number of active traps.

7.7 Reliability testing

The feasibility of using SiC MOSFET devices for power electronics applications has been recently demonstrated with the development of several power converter modules [29, 12]. However, before these devices can be properly qualified, device reliability issues, including the effect of threshold-voltage instability, must first be resolved. Although there exist industrial and military standards for stress test qualification of semiconductor devices (e.g Joint Electron Devices Engineering Council (JEDEC) JESD22-A108C [129], MIL-STD-750E [130], and Automotive Electronics Council (AEC) AEC-Q101 [131]), these standards are not self-consistent and are based

on Si device technology, and therefore do not take into account the complex time, bias, and temperature dependence of the V_T instability in SiC MOSFETs. The consequence of this complex response, the evidence for which has been reported in Chapters 4, 5, and 7, is that how you test and measure will significantly affect your results. Furthermore, it is critical that the testing be relevant to the intended application. This means that the effects of AC switching must be addressed, as well as the effects of operating at elevated temperatures, and that the worst-case operating stress conditions need to be identified. This includes determining whether recent improvements regarding smaller V_T instabilities are being achieved by balancing mobile ion drift with charge trapping effects, and if so, are there any conditions for which this would cause a reliability issue.

Green, Lelis, and Habersat [53] have very recently presented an initial investigation of the effects of HTGB stress on the reliability of 4H-SiC power MOSFET devices within the guidelines of the accepted industrial and military standards for stress-test qualification mentioned above. They showed that a large variation occurs in the I_D-V_{GS} characteristics of a SiC power MOSFET following a one-hour gate-bias stress at 150 °C with V_{GS} = +15 V, depending on whether the measurement is made immediately after rapidly cooling back to room temperature, or after a delay of one hour (see Figure 7-23). To further dramatize the difference, the immediate measurement was made by sweeping down in gate bias, from +15 to 0 V, whereas the later measurement was made by sweeping up in gate bias in the conventional manner. They found that the initial post-stress measurement would result in device failure based on the AEC standard which requires that post burn-in measurement parameters remain within ± 20 percent of their pre-stress values, whereas the second, later measurement with the one-hour delay would

remain within the specifications. The important point is that both measurement procedures are acceptable within the existing standards. This clearly illustrates the effect of the time-dependent nature of the charge trapping on HTGB stress-testing results.

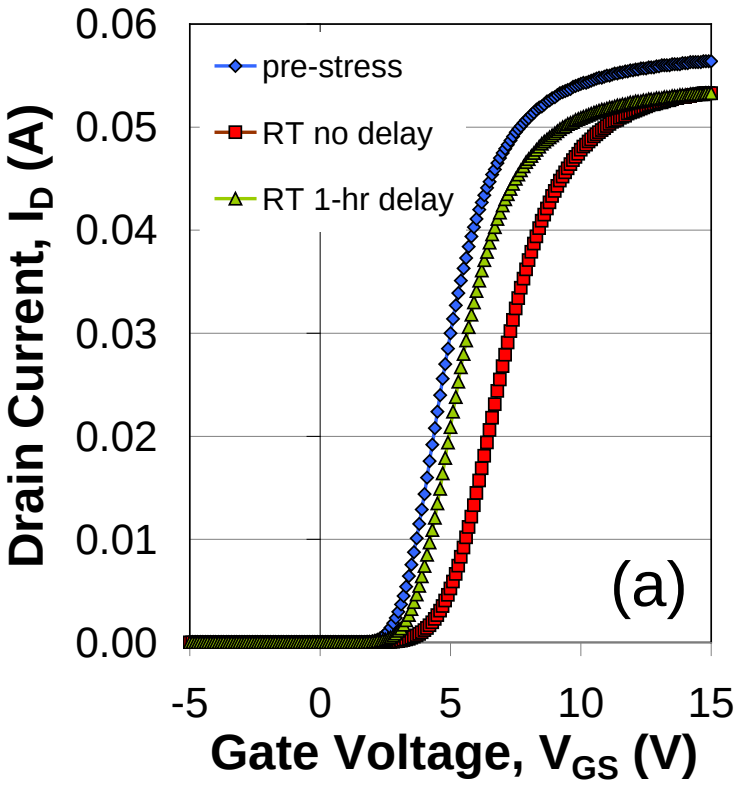

Figure 7-23: Large variation in the device room-temperature I_D-V_{GS} characteristic curves following a positive bias HTGB stress test at 150 °C, depending on measurement delay time.

Figure 7-24(a) shows a variation in response following a one-hour gate-bias stress at 150 °C with V_{GS} = –15 V. Although the variation in V_T between the immediate and one-hour delayed measurements is not as great in this case, the immediate measurement does result in an increase of the *OFF*-state leakage current due to the larger negative shift in V_T. More dramatic is the effect on V_T shift and increased leakage current when measuring at temperature, as shown in Figure 7-24 (b), since V_T naturally decreases with increasing temperature. This underlines the fact that not only do the present test

standards allow for a large variation in HTGB test results for SiC MOSFETs, they also do not address the large temperature effect observed.

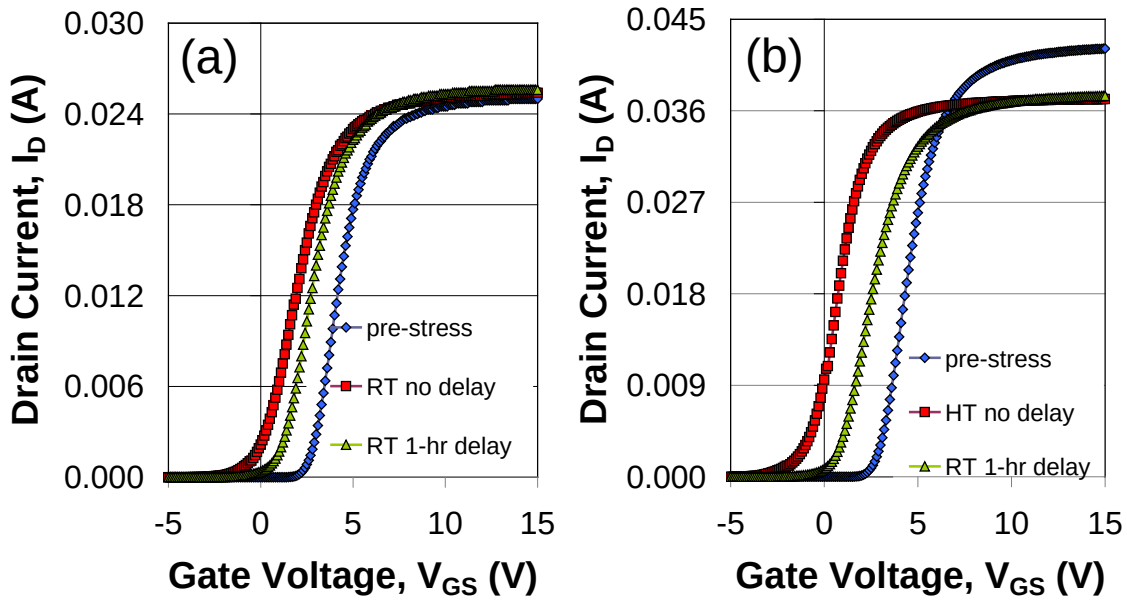

Figure 7-24: Drain current plotted on a linear scale as a function of V_{GS} following a negative bias HTGB stress test comparing (a) immediate room temperature I_D-V_{GS} characteristics with a one-hour delay time and (b) immediate high temperature I_D-V_{GS} characteristics versus a room-temperature measurement with a one-hour delay time.

These results illustrate the need for more stringent test and measurement standards to avoid inconsistent pass/fail results for SiC MOSFETs. For example, the present JEDEC standard [129] requires that post burn-in electrical measurements be completed as soon as possible, but no longer than 96 hours after removal of the bias. The above results of Green, Lelis, et al. [53] show the inadequacies of allowing a full one-hour window for the post-stress measurements when qualifying SiC MOSFET devices. In addition, the complex time, temperature, and bias dependence of the V_T-instability, likely due to the charging and discharging of near-interfacial oxide traps through a direct

tunneling mechanism, causes the drain current versus gate-to-source voltage (I_D-V_{GS}) characteristics to be sensitive to both the measurement sweep speed and direction, neither of which are addressed at all by the present standards.

Although the present standards call for pre- and post-bias temperature stress measurements such as HTGB to be performed at room temperature, it is important to measure at the stress temperature as well since SiC power MOSFETs are expected to operate at these temperatures and the leakage current under negative-bias stress is worse at elevated temperatures. It is also critical that the bias -stress times versus temperature be long enough to allow for the activation of all the elevated temperature mechanisms which may occur under actual operational conditions. Charge trapping effects will get worse, although for some devices this effect may be countered by mobile ion drift. It is also important to determine appropriate accelerated test conditions so that non-operational failure mechanisms are not introduced. Elevated temperature in the range of 150 °C cannot be a test accelerant if the devices are expected to operate at this elevated temperature.

Finally, it is important that tests relevant to the device application are employed, such as AC switching tests under the correct worst-case conditions. For a power MOSFET in a typical power conversion circuit, the device will either be switching *ON* and *OFF*, at a frequency of around 20 kHz, or be held in the *OFF* or blocking state [18]. The most appropriate AC stress test would be one where both the gate bias and drain bias switches as in an actual power conversion circuit: for example, from V_{GS} = +15 V and V_{DS} = +2 V to V_{GS} = 0 V and V_{DS} = +600 V. In lieu of that, it is appropriate to switch V_{GS}

from +15 V to V_{GS} = –5 or –10 V to simulate the negative field that develops across the gate oxide in the blocking mode.

The most appropriate blocking or HTRB stress test would be one that first switches the device *ON* and *OFF* to allow for the greatest activation of additional near-interfacial oxide traps at high temperature under the higher oxide fields in the *ON* state before applying a long-term lower oxide field under negative-bias stress conditions. This should then be followed by another AC stress to see if the stressed device can still withstand transient bias conditions once a large number of oxide traps have been charged.

If the activation rate of additional oxide traps at high temperature and bias can be formulated, then the oxide charge trapping under HTGB and HTRB conditions could be calculated versus time, leading to a prediction of device reliability versus time.

7.8 Summary

The gate-bias stress-induced threshold-voltage instability observed in lateral SiC MOSFETs is also present in fully processed SiC DMOSFETs, and the shifts are comparable in magnitude, and similar in their response to bias-stress time, gate-oxide field, and temperature. Therefore, it is highly likely that the same near-interfacial oxide trapping mechanisms are the cause of the observed instability in both the I_D-V_{GS} and I_D-V_{DS} characteristics of SiC power MOSFETs.

Bias stressing, while also allowing the rated current to flow through the channel of the power MOSFET, results in an increase in the V_T-instability effect compared to gate-bias stressing alone. Although the effect of this *ON*-state stressing is only slightly worse when measured at high-current levels on a linear scale, it is significantly worse

when measured at lower current levels on a logarithmic scale. There occurs both a significant additional positive shift of the I_D-V_{GS} characteristic following a positive-bias stress and a negative shift and increased stretch-out of the subthreshold *I-V* characteristics following a negative-bias stress. The *ON*-state stress results in self-heating, so it is not surprising that similar room-temperature measurement results are obtained when bias stressing at elevated temperature. The initial increase in the positive shift following positive-bias stress goes away over time after the device has returned back to room temperature, and eventually results in a smaller positive shift than before the initial *ON*-state or high-temperature stress. It is not clear whether this is due to the annealing of interface traps or to some more complicated oxide-trap mechanism.

High-temperature stress alone without an applied bias does not increase V_T instability. These results, coupled with recent results in the literature, suggest that this increased instability caused by high-temperature bias stressing is due to the activation of additional near-interfacial oxide traps, which are then free to change charge state with a change in gate bias. Many of these newly activated oxide trap defects likely become inactive again following a return to room temperature—especially over time.

This charge trapping will obviously affect the operation of the power SiC DMOSFET. Even though it is difficult to measure the full effect of any gate bias stress due to the short times needed to change the charge state of those traps closest to the interface, the effect will nevertheless occur. Switching oxide-trap densities as large as 8×10^{11} were calculated when measuring with ramp speeds of around 1 s.

Therefore it is imperative that the threshold voltage be set high enough to preclude increasing leakage current in the *OFF* state, when a negative field will be

established across the gate oxide. This is in addition to any margin designed in for negative shifts at elevated temperature due to fewer charged interface traps as well as the increases in the intrinsic carrier concentration.

While it is critical not to increase the drain leakage in the blocking state, it is also important not to set the threshold too high, especially since increased threshold voltage may be coupled with lower effective mobility. Thus, it is important to accurately estimate the magnitude of the actual threshold-voltage instability so as to find the optimum threshold voltage to achieve the best combination of low *OFF*-state leakage with low *ON*-state resistance.

The application of various existing standard high-temperature bias-stress reliability tests such as HTGB and HTRB, which are designed to assess the long-term effect of these stress conditions on the operating characteristics of a device under test, will likely need to be modified, given the great sensitivity of the SiC MOSFET V_T instability response to bias stress and temperature. Furthermore, it is important to determine the appropriate worst-case test and measurement conditions for a given circuit application, such as power conversion, and also to ensure that mobile ion drift is not masking potential reliability problems caused by charge trapping effects in near-interfacial oxide traps.

8 Summary, Conclusions, and Future Work

8.1 Summary and conclusions of present work

My research led to the initial discovery and reporting of the basic threshold voltage (V_T) instability phenomenon in SiC MOSFET devices, first in lateral test structures and later in fully processed vertical power devices. Although this effect has been primarily studied in MOSFETs on 4H-SiC and with a thermally grown gate oxide, it has also been observed in MOSFETs made on 6H-SiC, MOSFETs with a deposited oxide, and in SiC MOS capacitors. This V_T-instability phenomenon has also been observed in SiC MOSFETs irrespective of manufacturer.

A positive gate-bias stress will cause a positive shift of the I_D-V_{GS} characteristics and a negative gate-bias stress will cause a negative shift. This effect is very repeatable. The larger the gate bias, the larger the shift, although the effect of bias magnitude tends to saturate at higher oxide fields. The longer the gate-bias stress is applied, the larger the instability observed. This increase is generally observed to occur at a linear-with-log-stress-time rate. Extrapolating this linear rate back to zero instability indicates that stress times would have to be reduced to below 1 ps to prevent any V_T shift from occurring.

These effects are consistent with electrons directly tunneling to and from localized near-interfacial oxide traps which extend several nm into the gate oxide. Given the similarity of this V_T-instability phenomenon with that observed previously in irradiated Si MOSFETs with similar gate oxide thicknesses and the successful modeling of that effect with a tunneling model (wherein the first tunneling transition times into the

oxide were calculated to occur at around 0.1 ps), this work applied that model and extended it by allowing for a simultaneous two-way tunneling process. This two-way tunneling model calculates a long-term steady-state level of trap occupation, dependent on oxide depth, localized field, and assumed trap energy level, incorporating the concept of a tunneling front. Traps in the wake of this front have settled to a new steady-state trap occupation level, whereas traps deeper into the oxide and still ahead of this front have yet to be affected by the application of a new gate bias. This mechanism accounts for the time dependence of the stress bias. It also accounts for the sensitivity of the measured V_T instability with measurement time.

It is not surprising that the speed of the measurement would be so important since a gate bias is necessarily applied during the measurement, which in fact applies a bias stress of its own. The slower the measurement, the longer the time for this alternate gate bias to affect the results of the previous bias stress. Standard measurement times are on the order of 1 to 2 s. Faster measurements using a fast *I*-*V* system show a larger V_T-instability effect, with a 20-μs gate ramp showing the largest shift of all. Conversely, slowing down a conventional parameter analyzer to a 1-ks gate ramp showed the smallest shift of all. This difference is caused by oxide traps changing charge state during the measurement.

Another effect likely caused by oxide traps changing charge state during the measurement is the larger subthreshold swing (or stretch-out of the subthreshold I_D-V_{GS} characteristic) when sweeping up in gate bias following a negative-bias stress compared to sweeping down following a positive-bias stress. This difference was also measurement-time dependent, with the much slower 1-ks long measurements showing no

difference at all. Analysis was also presented which showed that the extrapolated *I-V* instability at mid-gap current levels was comparable to the instability observed in fast *I-V* measurements. The magnitude of this V_T instability can be used to calculate a lower bound for the number of oxide traps, based on the number that switch charge state. Standard-room temperature gate-bias stressed back-and-forth V_T-instability results yield switching oxide-trap densities of 1×10^{11} to 2.5×10^{11} cm^{-2}. Fast *I-V* measurements and extrapolated instability have revealed switching oxide-trap densities as large as 3×10^{11} to 5×10^{11} cm^{-2}. These are trap densities comparable to those of interface traps. Very slow 1ks-ramp speed measurements exhibit switching oxide-trap densities half as large as those at regular 1-s ramp speeds.

The only physical defect that has been observed to date in the gate oxides of SiC MOSFETs is referred to in the literature as an *E′* center. The pre-cursor site is a weak Si-Si bond owing to an O vacancy, with each Si back-bonded to three different O atoms. If this Si-Si bond is broken during processing or by operational stress, it can become an active oxide trap. Studies of irradiated Si MOS test structures found that this defect behaves as a hole trap which becomes a neutral dipole if it subsequently traps an electron. It has also been suggested that this defect in its neutral charge state may also behave as an electron trap. The large super-linear-with-log-time increase in the V_T instability observed at device temperatures of 100 °C and above can be explained in terms of a bias-dependent high-temperature increase in the number of active *E′* center oxide defects. Switching oxide-trap densities as large as 8×10^{11} have been calculated with measurement speeds of around 1 s.

If the threshold voltage is set too low, then a negative V_T shift could cause an increase in *OFF*-state leakage current, leading to potential failure of the power MOSFET when trying to block 600 V or more in a typical application. This negative V_T shift can become much greater at elevated temperature, given both the potential increase in the number of active oxide traps and fewer charged interface traps, as well as the decrease in V_T due to the increase in the intrinsic carrier concentration. This identifies high-temperature reverse bias (HTRB) as a potential failure mode, with the significant increase in the number of positively-charged near-interfacial oxide traps the accompanying failure mechanism. If the activation rate of additional oxide traps at high temperature and bias can be formulated, then the oxide charge trapping under HTGB and HTRB conditions could be calculated versus time, leading to a prediction of device reliability versus time.

Based upon a large variation in high-temperature V_T-instability results, it is quite possible that the flat response of some recent SiC MOSFETs versus temperature is due to a balance of oxide charge trapping effects and mobile-ion drift.

A positive V_T shift under positive-bias stress will increase the *ON*-state resistance. An *ON*-state stress, during which the rated current is flowing through the channel, will increase this positive shift, due primarily to elevated-temperature effects caused by the self-heating of the device.

Given the complex time, temperature, and bias dependence of the V_T-instability effect described in this work, existing reliability standards based on Si device technology are likely inadequate for SiC MOSFETs and need to be revised. Particular attention needs to be paid to the measurement conditions. Measurements should be made quickly, without delay, and with a gate bias that is minimally disruptive. In addition, elevated

temperature is problematic as a stress accelerant, since SiC power MOSFETs are expected to operate at temperatures of 150 °C, and even higher-temperature stressing will likely lead to additional defect creation which may not necessarily occur at the operating temperature.

Processing variations have a noticeable effect on the V_T instability. Lateral SiC MOSFETs with an implanted epi channel (which mimic the implanted channel of a power DMOSFET) show a slightly larger instability than devices with an un-implanted channel. SiC MOSFETs that did not receive the standard post-oxidation NO anneal have a much larger V_T instability, with switching oxide-trap densities as large as 6×10^{11} calculated with standard 1-s measurement speeds. The reduction in oxide traps following a post-oxidation NO anneal mirrors the reduction in interface-trap density, which also decreases significantly. One possible explanation for this is that many test procedures designed to measure the number of interface traps are, at least in part, actually measuring the response of near-interfacial oxide traps. Making a distinction between the different types of interfacial charge is important, since they are likely associated with different physical defects, which in turn may respond differently to processing variations.

8.2 Future work

The work presented here can naturally lead to additional future work in a number of different areas. For example:

Validate high-temperature oxide-trap model

Confirm that it is in fact the activation of additional E' center-type oxide trap defects that is causing the large increase in V_T-instability at temperatures above 100 °C. This should be done by correlating a larger array of ESR results—both on Si and SiC MOS type structures, as a function of bias stress magnitude, polarity, and temperature—with a similar array of electrical measurements.

Develop two-step oxide-trap tunneling model

Although the two-way tunneling model can accurately describe the time-dependence of the V_T instability results—as well as the bias magnitude and bias polarity dependence—it does not predict the larger subthreshold swing when sweeping up in gate bias following a negative-bias stress. Therefore, the next step in the development of this simultaneous two-way oxide-trap tunneling model is to include the very likely possibility that interface traps are involved in a two-way process, such that electrons must first fill an interface trap before they can tunnel to a near-interfacial oxide trap, or conversely, that an electron tunneling out from a near-interfacial oxide trap will first fill an available interface trap.

Model transient device behavior for circuit applications

Incorporate this oxide-trap tunneling model into the existing SiC power MOSFET simulator at the University of Maryland to enable accurate prediction of device behavior in circuit applications of great importance, such as that of various power converter systems.

Establish new reliability test standards for SiC power MOSFETs

Given the strong time and bias dependence of the V_T instability effect, and given the lax and inconsistent existing standards for power electronics in terms of test time and procedure, it is important to update these standards for SiC power MOSFETs. This also includes ensuring that reliability tests relevant to the device application are applied, and that the actual worst-case conditions are identified.

In addition, methods need to be developed and applied to verify whether mobile ion drift is in some cases compensating for oxide trapping effects to reduce the V_T instability in some devices at high temperature. Furthermore, if this is, in fact, happening, determine whether this balancing of charge fails under certain conditions, leading to potential reliability issues.

Develop improved processing methods

Given that near-interfacial oxide traps play a critical role in the V_T-instability effect in SiC MOSFETs, which can in turn cause serious reliability issues, it is important to develop processing methods that decrease this defect, or the effect of this defect. Possible ways may include incorporating more O at the interface to prevent the original creation of this defect, reducing the near-interfacial bond strain, or identifying other methods similar to the NO post-oxidation anneal to help prevent the activation of this defect, or possibly to further reduce the interface trap density if these do, in fact, play an integral part in the charging and/or discharging of the oxide-trap defect.

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