ABSTRACT

Title of Document: LOW POWER ADAPTIVE CIRCUITS: AN ADAPTIVE LOG DOMAIN FILTER AND A LOW POWER TEMPERATURE INSENSITIVE OSCILLATOR APPLIED IN SMART DUST RADIO

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This dissertation focuses on exploring two low power adaptive circuits. One is an adaptive filter at audio frequency for system identification. The other is a temperature insensitive oscillator for low power radio frequency communication.

The adaptive filter is presented with integrated learning rules for model reference estimation. The system is a first order low pass filter with two parameters: gain and cut-off frequency. It is implemented using multiple input floating gate transistors to realize online learning of system parameters. Adaptive dynamical system theory is used to derive robust control laws in a system identification task. Simulation results show that convergence is slower using simplified control laws but still occurs within milliseconds. Experimental results confirm that the estimated gain and cut-off frequency track the corresponding parameters of the reference filter. During operation, deterministic errors are introduced by mismatch within the analog

circuit implementation. An analysis is presented which attributes the errors to current mirror mismatch. The harmonic distortion of the filter operating in different inversion is analyzed using EKV model numerically.

The temperature insensitive oscillator is designed for a low power wireless network. The system is based on a current starved ring oscillator implemented using CMOS transistors instead of LC tank for less chip area and power consumption. The frequency variance with temperature is compensated by the temperature adaptive circuits. Experimental results show that the frequency stability from 5°C to 65°C has been improved 10 times with automatic compensation and at least 1 order less power is consumed than published competitors. This oscillator is applied in a 2.2GHz OOK transmitter and a 2.2GHz phase locked loop based FM receiver.

With the increasing needs of compact antenna, possible high data rate and wide unused frequency range of short distance communication, a higher frequency phase locked loop used for BFSK receiver is explored using an LC oscillator for its capability at 20GHz. The success of frequency demodulation is demonstrated in the simulation results that the PLL can lock in 0.5μs with 35MHz lock-in range and 2MHz detection resolution. The model of a phase locked loop used for BFSK receiver is analyzed using Matlab.

LOW POWER ADAPTIVE CIRCUITS:
AN ADAPTIVE LOG DOMAIN FILTER
AND
A LOW POWER TEMPERATURE INSENSITIVE OSCILLATOR APPLIED IN SMART DUST RADIO

By

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Chapter 1: Overview

1.1 Introduction

In the human scientific research history, a lot of fruitful results are inspired by nature. With the development of computer and electronic techniques, more and more scientific research works are closely related to biology, healthcare and life style. In the area of artificial intelligence, computers and electronic devices that can imitate human beings to read, listen and think have been coming true. In other ways, inspired by evolutionism, scientists and engineers have been proposing electronic design techniques based on biology. They apply evolution theory to design novel circuits which adapt to the change of environment as an organism. These kinds of circuits are called adaptive circuits. Nowadays adaptive circuits are being widely used in communications, biomedical engineering and life science.

With the development of adaptive circuits, low power designs are also gaining more and more importance because of the increasing integration capability of the VLSI technology and the diffusion of the battery-operated systems for computer and telecommunication products, which require the reduction of the device weight and size and the increasing of their operative life. Therefore, designs of low power adaptive circuits are getting into a trend to meet the growing demand.

This dissertation explores low power adaptive circuits in two different areas. One is a log domain filter operating at audio frequency for system identification. The other

is about a temperature insensitive oscillator designed for low power radio frequency communication and its application in phase locked loops. Details are discussed in Part I and Part II respectively.

1.2 Contributions

My work in this dissertation can be summarized as follows.

1. Fabricate through MOSIS and test an adaptive first order low pass filter.

2. Investigate the adaptive behavior under the non-ideal condition of a current mirror ratio mismatch.

3. Analyze the harmonic distortion of the first order low pass filter using numerical methods.

3. Design, simulate, fabricate through MOSIS and test a low power CMOS temperature sensor for on-chip temperature gradient detection.

4. Design, simulate, fabricate through IBM and test a low power temperature insensitive oscillator.

5. Design, simulate, fabricate through IBM and test a low power phase locked loop based FM receiver at 2.2GHz in collaboration with colleague Bo Li at the University of Maryland.

6. Design, simulate, fabricate through IBM a low power phase locked loop based BFSK receiver at 20GHz.

7. Analyze the phase locked loop models numerically using Matlab.

PART I

AN ADAPTIVE LOG DOMAIN FILTER FOR SYSTEM IDENTIFICATION USING FLOATING GATE TRANSISTORS

Chapter 2: Background and System Identification

2.1 Introduction and Objective

2.1.1 Background and Motivation

Adaptive signal conditioning is an important and well-established tool used widely in scientific and engineering disciplines such as communications, biomedical engineering and life science. Many complex and demanding applications require adaptive filtering to reject noise and improve signal performance dynamically. For system identification tasks, control laws must use limited information to robustly adjust parameters of the adaptive system to match an unknown system.

Several groups have described filtering applications based on floating gate MOS circuits. Hasler et al. [1] described the auto-zeroing floating gate amplifier (AFGA) and its use in band pass filter structures with very low frequency response capability. Chawla et al. [2] reported two floating gate operational transconductance amplifiers (OTAs) from which a programmable second order transconductor-capacitor filter section was built. Graham et al. [3] presented a programmable array of band pass filters using floating gate elements that perform a frequency decomposition of an audio signal and also allow for analog preprocessing before transformation into the digital domain. Fernandez et al. [4] described a 1V micro-power low pass filter implemented using floating gate metal oxide semiconductor (FGMOS) transistors. Rodriguez-Villegas et al. [5][6][7] designed a 1-V micro-power log-domain integrator,

a 1.25-V micro-power Gm-C filter and a 0.8 V, 360 nW Gm-C biquad based on FGMOS transistors. Minch [8][9][10][11] developed circuits and synthesis techniques using multiple input translinear elements (MITEs) for a variety of signal processing applications. Yamasaki and Shibata [12] reported a high-speed low-power median filter using a majority voting circuit based on floating-gate MOS. Lopez-Martin et al. [13] reported a 1.2V 5μW class-AB CMOS log domain integrator with multi-decade tuning.

Few groups have reported integrated analog adaptive filters. Juan et al. [14] and Stanacevic and Cauwenberghs [15] designed analog transversal finite impulse response (FIR) filters that include adaptation of weights. Ferrara and Widrow [16] designed a time-sequenced adaptive filter which extends least mean square (LMS) adaptive filters to allow slow precise adaptation. Figueroa et al. [17] implemented a 48-tap, mixed-signal adaptive FIR filter that operates at 200MHz and consumes 20mW, providing 19.2 GOPS and 6mA differential output current. Srinivasan et al. [18] designed an adaptive analog synapse circuit implementing the LMS learning rule. Kucic et al. [19] implemented programmable and adaptive analog filters using arrays of floating gate circuits that apply matched filtering and weight perturbation algorithms. Xie and Al-Hashimi [20] describe an analog adaptive filter designed using a wave synthesis technique. Most of these use LMS-based adaptation algorithms which adjust weights iteratively to move along the error surface towards the optimum value. The adaptive filters are discrete FIR filters composed of a tapped delay line and adjustable weights, whose outputs are defined by a weighted sum of input sequences.

2.1.2 Multiple Input Translinear Element

Multiple input translinear elements (MITEs) provide compact and elegant implementations of log domain filters. A MITE produces an output current that is an exponential function of the weighted sum of its input voltages. We can implement such devices using multiple input floating gate transistors operating in weak inversion. A floating gate MOS transistor is a standard MOS transistor whose gate is completely surrounded by insulator. The potential barrier ensures the nonvolatile storage of charge on the floating gate. Since the floating gate has no DC path to ground, external inputs are capacitively coupled. The capacitors are implemented as linear poly to poly capacitors using a second polysilicon layer. The stored charge may be adjusted using hot-carrier injection [21] or tunneling [22], but in this work these mechanisms are not necessary. Fig. 2.1 is a circuit symbol for an ideal N-input MITE. The transfer function of this element is given by:

$$I = I_0 \exp\left[\kappa(w_1 V_1 + w_2 V_2 + \cdots + w_N V_N - V_T)/\phi_t\right] \tag{2.1}$$

where I_0 is a pre-exponential scaling current,

$$I_0 = \frac{2\mu C_{ox}\frac{W}{L}\phi_t^2}{\kappa} \tag{2.2}$$

V_i is the ith input voltage, and w_i is the dimensionless positive weight of V_i. V_T is the threshold voltage of the transistor. κ is the subthreshold slope factor which reflects the capacitive division between gate and substrate and is less than 1. ϕ_t is the thermal voltage kT/q. The pre-exponential current I_0 depends on the carrier mobility μ, gate oxide capacitance C_{ox}, width to length ratio W/L, subthreshold slope factor κ and

thermal voltage $\phi_t = KT/q$. The advantage of using floating gate MOS transistors in weak inversion to implement MITEs is that they can be easily fabricated in standard CMOS processes.

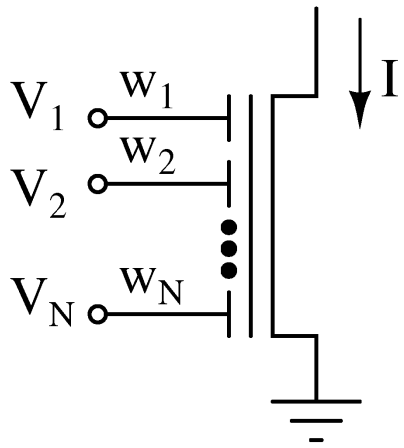


Fig. 2.1: Circuit symbol for ideal N-input MITE.

2.1.3 Research Objective

The research aims at developing a low power adaptive filtering system for system identification. The proposed technique employs adaptive dynamical system theory to derive robust control laws. We started with a first order low pass filter for reference model estimation. Current-mode log domain filter architecture and floating gate MOSFETs operating in subthreshold are combined to realize accurate and stable learning rules for the system parameters.

The current-mode log domain filters are implemented with transistors operating in weak inversion mode. Weak inversion mode is especially suitable for low power circuit design. The current flowing in a unit transistor working in weak inversion is below hundreds of nanoamperes, which is smaller than the values associated with

strong inversion operation. The gate to source voltage drop of a transistor working in weak inversion is around or below the threshold voltage, which makes it possible to use low supply voltages and further reduce power consumption. In addition to the low power dissipation, the exponential transfer function in weak inversion also provides an extended dynamic range and easy tunability.

The model-based learning method models an unknown system by tuning an adaptive estimator to track the operation of the unknown system as shown in Fig. 2.2. By applying the same input signal to both systems and observing the outputs of the unknown and adaptive filters, we generate adaptive updates for system parameters to solve the classical problem of system identification. In addition to nulling the output error, we also estimate the parameters of the unknown system. The method is based on Lyapunov stability and is well suited for adaptive control of analog continuous-time filters. Analog continuous-time filters offer the advantage of smaller filter structures, fewer filter coefficients and faster and higher performance than discrete FIR filters in order to model plants of similar complexity.

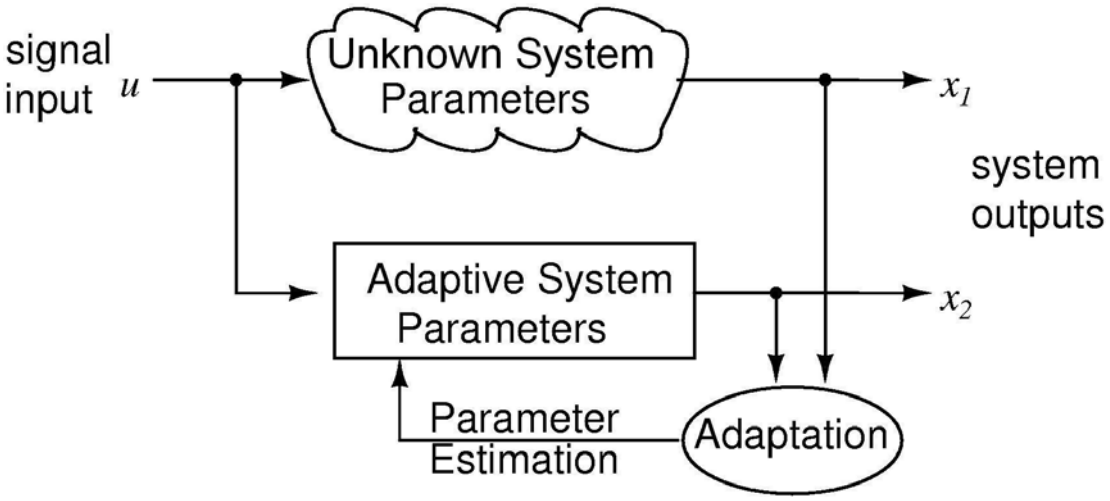


Fig. 2.2: Model-based learning method for the classical problem of system identification.

2.2 System Identification

We derive control laws for a tunable filter which address the classical problem of system identification, depicted in Fig. 2.3: an input signal is applied to both an unknown system (plant) and to an adaptive estimator (model) system which estimates the parameters of the unknown plant. The difference between the plant and the model, the error, is used to adjust the parameters. We design the adaptive laws for adjusting the control parameters so as to ensure stability of the learning procedure, and so that the adaptive laws are amenable to VLSI implementation.

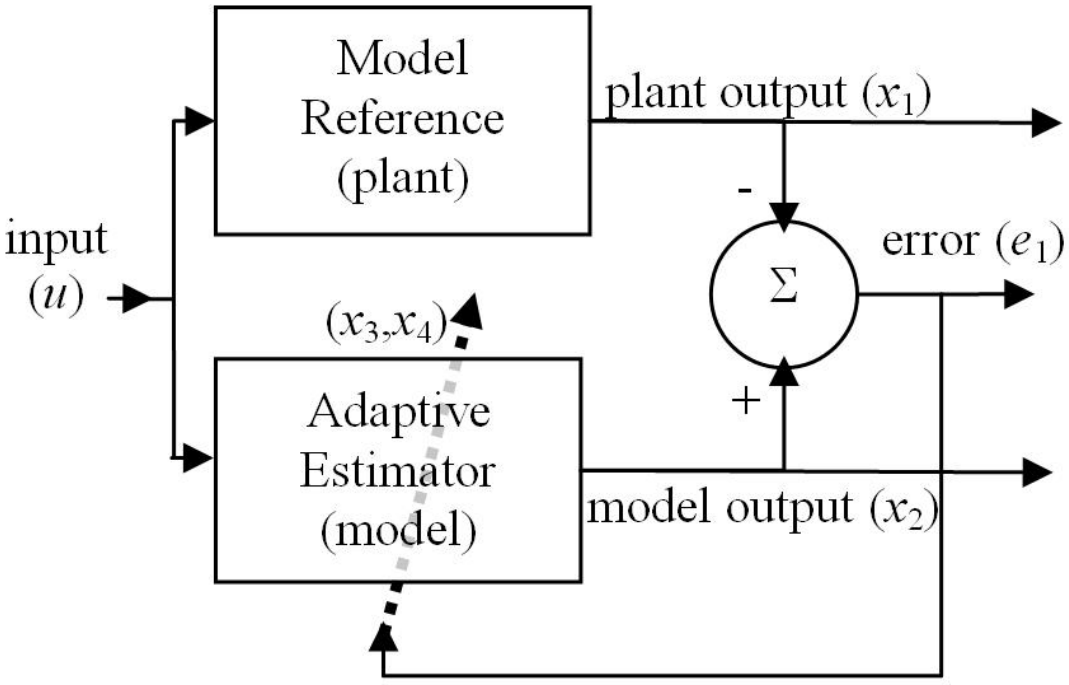


Fig. 2.3: The system identification problem: an input u is applied to both plant and model filters. The error e_1 is the difference of plant and model outputs, (x_1-x_2) and is used to adapt the parameters of the model, x_3 and x_4.

2.2.1 State Variable Representation

The unknown plant and the adaptive model filters are described by the state-variable representation:

$$\dot{x}_1 = -Ax_1 + ABu \qquad \text{plant output} \qquad (2.3)$$

$$\dot{x}_2 = -x_3 x_2 + x_3 x_4 u \qquad \text{model output} \qquad (2.4)$$

where x_1 is the output of the plant, A is the plant cut-off frequency, B is the plant gain, u is the input to both filters, x_2 is the output of the model, x_3 is the estimate of the cut-off frequency, and x_4 is the estimate of the gain.

In order to assess the performance and stability of the adaptation, we construct the error system as the differences between plant and model outputs, between estimated and true cut-off frequency, and between estimated and true gain:

$$e_1 = x_2 - x_1 \qquad \text{output error} \qquad (2.5)$$

$$e_2 = x_3 - A \qquad \text{frequency error} \qquad (2.6)$$

$$e_3 = x_4 - B \qquad \text{gain error} \qquad (2.7)$$

We are interested in adaptive laws that control system parameters so that all errors tend towards zero with time. Thus we can focus on the essential features of the control problem by considering the dynamics of the error system:

$$\dot{e}_1 = \dot{x}_2 - \dot{x}_1 \qquad (2.8)$$

$$\dot{e}_2 = \dot{x}_3 \qquad (2.9)$$

$$\dot{e}_3 = \dot{x}_4 \tag{2.10}$$

under the assumption that the gain and cut-off frequency are fixed or slowly varying. The dynamics of the output error are determined by the system, but we have the flexibility to specify the dynamics of the parameter errors so that the control laws drive the estimates stably to their true values.

2.2.2 Derivation of Control Laws

We employ the direct method of Lyapunov to investigate the stability of the adaptive system and to derive appropriate control laws [23]. We choose a suitable scalar function and examine the temporal derivative of this function along trajectories of the system. A Lyapunov function must satisfy the following three conditions: positive definite, negative definite time derivative, and radially unbounded. These conditions guarantee global asymptotic stability. For system identification of the first order low pass filter we consider the Lyapunov function:

$$V(e) = \frac{1}{2}(e_1^2 + e_2^2 + e_3^2) \tag{2.11}$$

This function satisfies the first and third conditions and has the following temporal derivative, evaluated in terms of the simple adaptive system described above:

$$\begin{aligned} \dot{V}(e) &= e_1\dot{e}_1 + e_2\dot{e}_2 + e_3\dot{e}_3 \\ &= -Ae_1^2 + e_1e_2(-x_2 + Bu) + e_1e_3(e_2u + Au) + e_2\dot{e}_2 + e_3\dot{e}_3 \\ &= -Ae_1^2 + e_1e_2(\frac{\dot{x}_2}{x_3}) + Ae_1e_3u + e_2\dot{e}_2 + e_3\dot{e}_3 \end{aligned} \tag{2.12}$$

Note that the control laws for the cut-off frequency and gain errors ($\dot{e}_2$ and $\dot{e}_3$ respectively) remain unspecified, and we choose them to satisfy the second condition

for the Lyapunov function. There are multiple solutions which provide such a negative time derivative:

$$\dot{V}(e) = -Ae_1^2 \tag{2.13}$$

We choose the following pair of control laws:

$$\dot{e}_2 = -e_1 \frac{\dot{x}_2}{x_3} \tag{2.14}$$

$$\dot{e}_3 = -e_1 Au \tag{2.15}$$

These rules may be simplified further since in current mode log domain filters, many system variables are strictly positive, including the estimate of the cut-off frequency x_3, the plant cut-off frequency A, and the input u. Multiplying the rules by a positive scalar factor affects the rate of adaptation, but not the direction. Thus we can express the control laws simply:

$$\dot{e}_2 \propto -e_1 \dot{x}_2 \tag{2.16}$$

$$\dot{e}_3 \propto -e_1 \tag{2.17}$$

In our implementation the estimate of the cut-off frequency is provided by integrating the product of the output error with the temporal derivative of the model output, and the estimate of the gain is provided by integrating the output error.

In the preceding development we used the Lyapunov method to derive learning rules for the first order low pass system. Learning rules may be derived using other approaches as well, for example the least-mean-square (LMS) method. In the LMS method, learning rules are derived by taking the derivative of the squared output error

with respect to each of the tunable parameters, then setting the learning rules for each parameter to be a negative constant times the error derivative for that parameter. This produces learning rules that cause the system to move down its error gradient. In the special case of the first order low pass system described in this dissertation, the learning rules when derived using the LMS method are the same as the learning rules derived above using the Lyapunov method. However, this is not the case in general. In particular, the learning rules for the second order filter [24] are not the same when derived by Lyapunov and LMS methods.

2.2.3 Investigation of Stability

We investigate the stability of the system with modified control laws. We rewrite the simplified control laws as:

$$\dot{e}_2 = -k_1 e_1 \dot{x}_2 \tag{2.18}$$

$$\dot{e}_3 = -k_2 e_1 \tag{2.19}$$

With these control laws, the temporal derivative of the Lyapunov function (3.10) can be rewritten as

$$\begin{aligned} \dot{V}(e) &= -Ae_1^2 + e_1 e_2 (-x_2 + x_3 u) + Ae_1 e_3 u - e_2 k_1 e_1 \dot{x}_2 - e_3 k_2 e_1 \\ &= -Ae_1^2 + e_1 e_2 \dot{x}_2 \left(\frac{1}{x_3} - k_1 \right) + e_1 e_3 (Au - k_2) \\ &= -Ae_1^2 + \frac{e_2 \dot{e}_2}{k_1} \left(k_1 - \frac{1}{x_3} \right) + \frac{e_2 \dot{e}_3}{k_2} (k_2 - Au) \end{aligned} \tag{2.20}$$

k_1 and k_2 are positive constants, while $1/x_3$ and Au are nonnegative variables that reflect the cut-off frequency and input signal respectively. Therefore k_1 and k_2

cannot cancel $1/x_3$ and Au exactly, so the temporal derivative of the Lyapunov function might not be negative at all instances in time. This raises the possibility that the system may not converge monotonically.

We evaluate this issue through simulation by fixing one variable and observing the adaptation of the other variable for both simplified and exact learning rules. First we examine gain adaptation for a fixed cut-off frequency. Fig. 2.4 shows temporal trajectories of the estimated gain for systems with simplified and exact learning rules, starting from an initial estimate of gain = 3, for true gain = 2 and cut-off frequency = 5e+4 rad/s. In this example, simulation results show that the system with exact learning rules converges to the true gain faster than the system with simplified learning rules. We define the adaptation time as the time necessary for the estimated parameter to converge within 0.1% of the true value. Fig. 2.5 shows the relationship between adaptation time and gain adaptation constant k_2 for the system shown in Fig. 2.4. The dashed line shows the adaptation time using exact learning rules. Point A is the point at which k_2 is closest to the average value $A\bar{u}$.

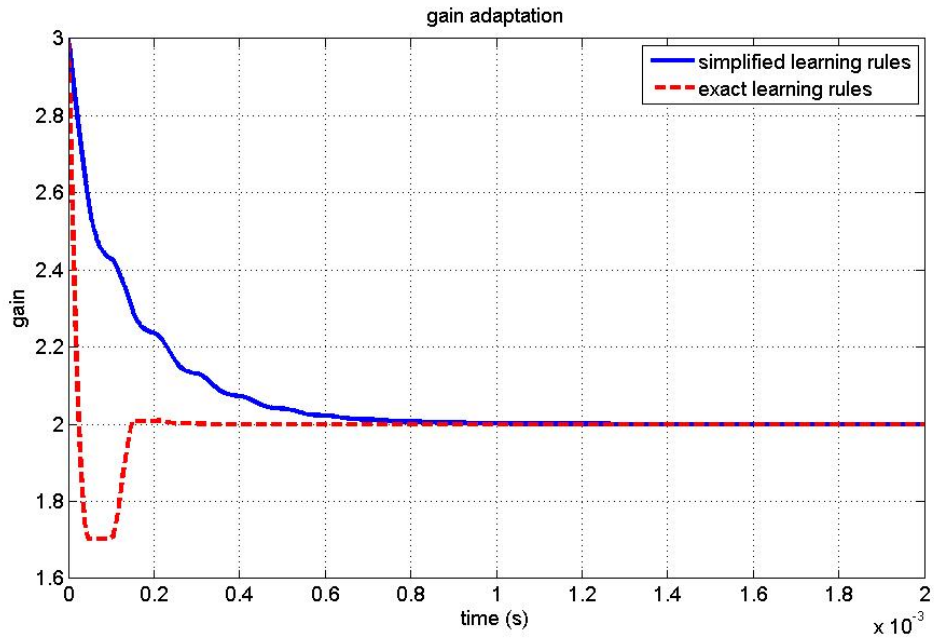


Fig. 2.4: Convergence analysis: gain adaptation with cut-off frequency fixed.

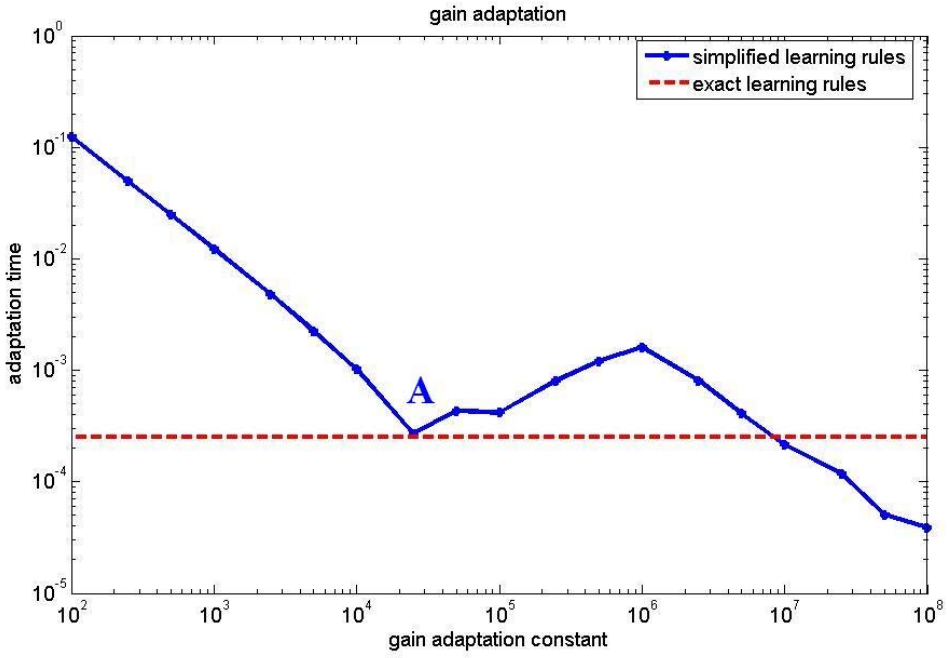


Fig. 2.5: Convergence analysis: adaptation time as a function of gain adaptation constant k_2.

Next we examine cut-off frequency adaptation for a fixed gain. Fig. 2.6 shows temporal trajectories of the estimated cut-off frequency for systems with simplified and exact learning rules, starting from the initial estimate of cut-off frequency = 1e+5 rad/s, for true cut-off frequency = 5e+4 rad/s and gain = 2. Again, the system with exact learning rules converges to the true cut-off frequency faster than the system with simplified learning rules. Fig. 2.7 shows the relationship between adaptation time and cut-off frequency adaptation constant k_1 for the system shown in Fig. 2.6. Again, the dashed line shows the adaptation time using exact learning rules. The average value $1/\bar{x}_3$ is difficult to evaluate accurately, but it is bounded between 5e4 (point B) and 1e5. Point C denotes the largest value of k_1 at which the cut-off frequency converges. This analysis indicates that the two adaptation constants k_1 and k_2 must be selected carefully for fast parameter convergence.

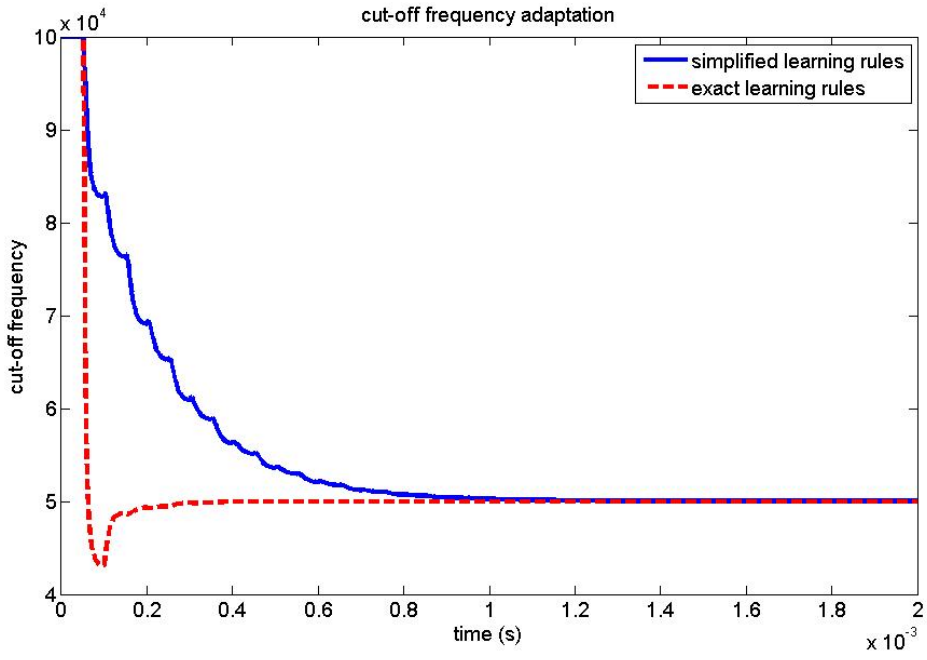


Fig. 2.6: Convergence analysis: cut-off frequency adaptation with gain fixed.

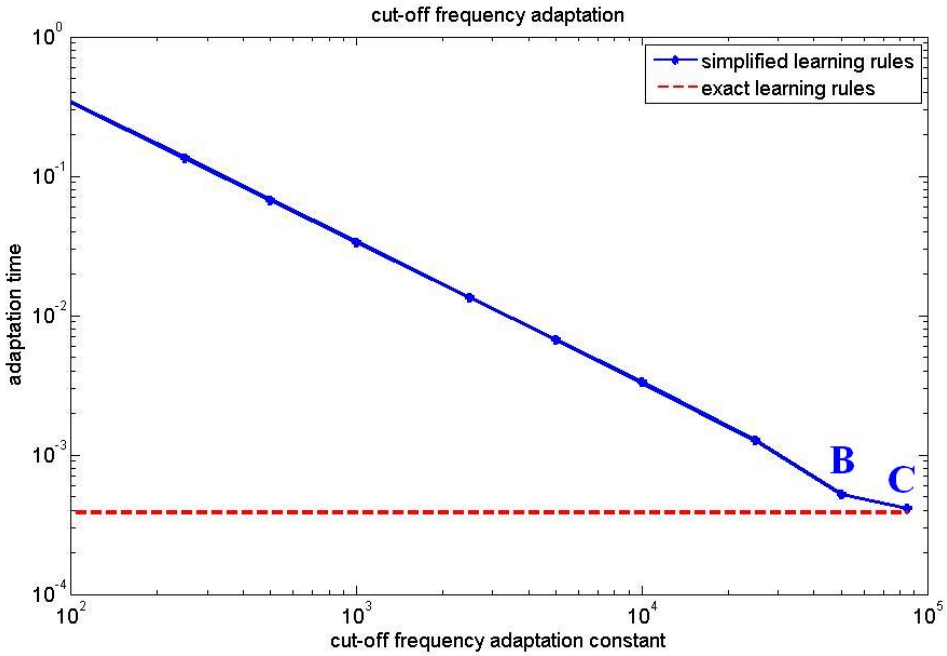


Fig. 2.7: Convergence analysis: adaptation time as a function of gain adaptation constant k_1.

Chapter 3: Circuit Implementation, Simulation and Experimentation

3.1 Analog Circuit Implementation

3.1.1 MITE Implementation of Log Domain Filters

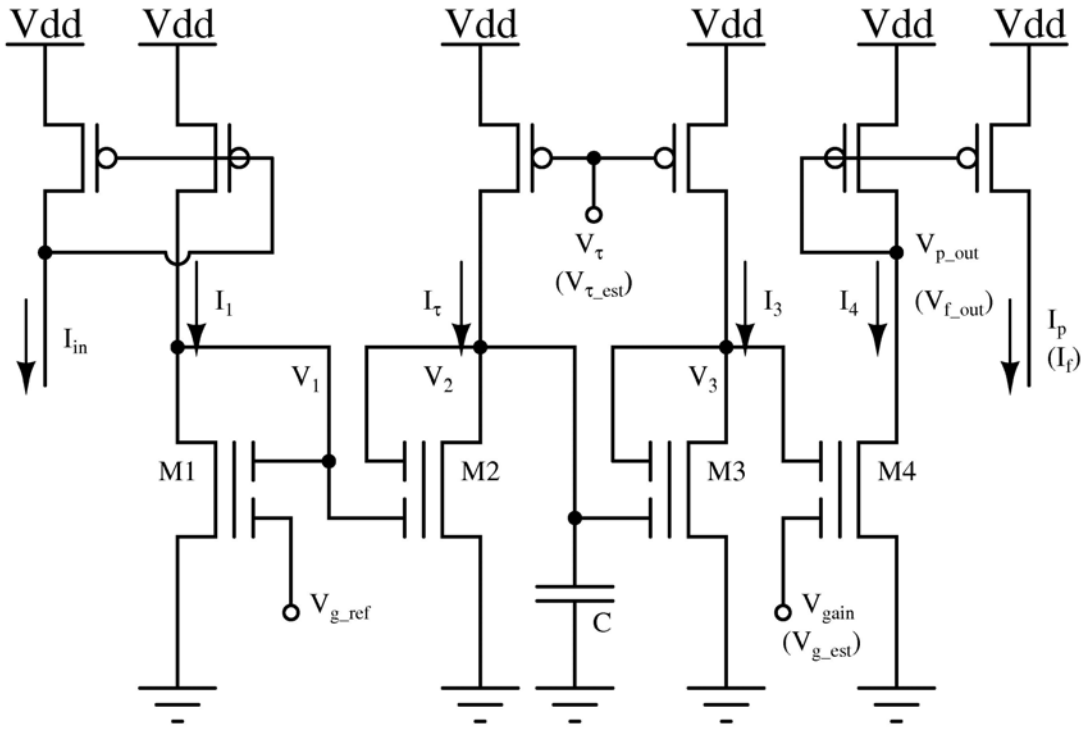


Fig. 3.1: Log domain MITE filter topology for a first order low pass transfer function used for both plant and filter. Labels in parentheses refer to filter variables, the rest to the plant.

Log domain filters are a dynamic extension of classical static translinear circuits. They offer wide tuning range, large dynamic range, and low power operation. The circuit in Fig. 3.1 is used to implement both plant and model systems, with labels in

parentheses representing model parameters. Cascode transistors are not shown for clarity. In subthreshold operation the MITE current is an exponential function of the summed inputs:

$$I_1 = I_p e^{m(V_1 + V_{g\_ref})} = I_{in} \tag{3.1}$$

$$I_2 = I_p e^{m(V_1 + V_2)} \tag{3.2}$$

$$I_3 = I_p e^{m(V_2 + V_3)} = I_\tau \tag{3.3}$$

$$I_4 = I_p e^{m(V_3 + V_{gain})} = I_{out} \tag{3.4}$$

where m is $\kappa q / 2kT$, half the ratio between the subthreshold slope factor κ and the thermal voltage kT/q, and I_p is the pre-exponential constant current related to carrier mobility μ, gate oxide capacitance C_{ox}, width to length ratio W/L, threshold voltage V_T, subthreshold slope factor κ and thermal voltage ϕ_t.

We apply Kirchoff's Current Law (KCL) at the capacitive node to find the relationship between the MITE currents and the capacitive current:

$$C\dot{V}_2 + I_2 = I_\tau = C\dot{V}_2 + \frac{I_{in} I_\tau}{I_4} e^{m(V_{gain} - V_{g\_ref})} \tag{3.5}$$

Since V_2 and V_3 together control a constant current I_3, their time derivatives are opposite in sign but equal in magnitude:

$$\dot{I}_3 = I_3 \cdot m(\dot{V}_2 + \dot{V}_3) = 0 \Rightarrow \dot{V}_3 = -\dot{V}_2 \tag{3.6}$$

We determine the transfer function for the output current I_4 by differentiating it, then substituting our results from KCL and MITE relationships above:

$$\dot{I}_4 = mI_4\dot{V}_3 = -mI_4\frac{I_\tau}{C}\left[1-\frac{I_{in}}{I_4}e^{m(V_{gain}-V_{g\_ref})}\right]$$
$$\dot{I}_4 = \frac{mI_\tau}{C}\left[-I_4 + I_{in}e^{m(V_{gain}-V_{g\_ref})}\right] \quad (3.7)$$

which is a first order low pass transfer function with cut-off frequency $\omega = mI_\tau / C$. The cut-off frequency is proportional to the ratio between bias current and capacitance, easily tuned by adjusting the bias current. The gain is an exponential function of the voltage difference between V_{gain} and V_{g_ref}, easily tuned by adjusting the voltage V_{gain}. The same input current I_{in} is applied to both plant and filter. The output of the plant is I_p. The output of the filter is I_f.

3.1.2 MITE Implementation of Learning Rules

The plant and model are first order low pass filters, each with two adjustable parameters: gain and cut-off frequency. We have implemented the simplified learning rules derived using the Lyapunov method described in Section II. The inputs to the learning rules are the system output error and the temporal derivative of the model output. The temporal derivative of the model output is computed using the circuit shown in Fig. 3.2. A wide range OTA operates as a voltage follower with a capacitive load, with output current

$$I_d = I_{d1} - I_{d2} \quad (3.8)$$

This current relates to the input voltage as

$$I_d = sC_d(1 + sC_d / g_{m12})^{-1} I_f R \quad (3.9)$$

where g_{m12} is the transconductance of transistors M1 and M2 in the OTA. When $s << g_{m12}/C_d$, the output current is approximately the derivative of the input voltage

$$I_d \approx sC_d I_f R \tag{3.10}$$

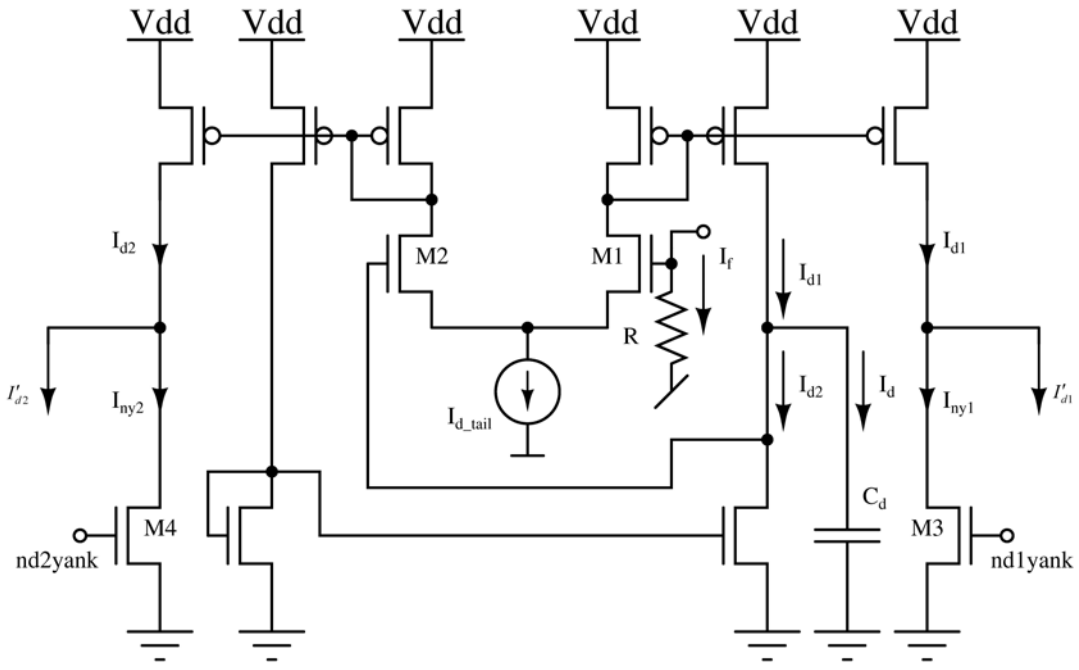


Fig. 3.2: Circuit for computing temporal derivative with mismatch compensation.

To make g_{m12} large, we operate the input devices near threshold. It is not necessary to explicitly convert the filter output current into voltage; we use intermediate node voltage V_3 of Fig. 3.1 directly as input to the temporal derivative computation. Note that since $\dot{I}_f = I_f K \dot{V}_3$, the adaptation rule becomes $\dot{e}_2 \propto (I_p - I_f)\dot{I}_f / KI_f$. Nodes nd1yank and nd2yank in Fig. 3.2 control two NMOS transistors which subtract currents from I_{d1} and I_{d2} respectively to

compensate transistor mismatch. I'_{d1} and I'_{d2} are passed on to the next circuit stage. The outputs of the derivative circuit are the two currents I'_{d1} and I'_{d2}.

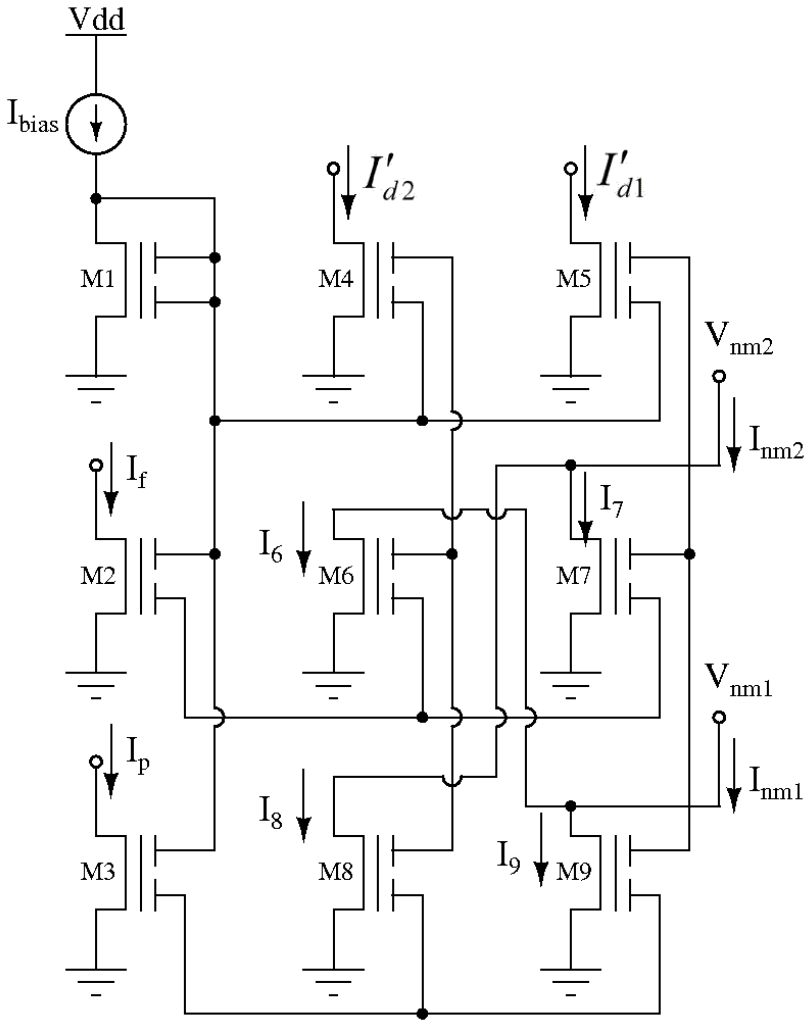


Fig. 3.3: Circuit for four quadrant multiplication.

The cut-off frequency learning rule requires a four quadrant multiplication, implemented using the MITE circuit shown in Fig. 3.3 with inputs I'_{d1}, I'_{d2}, I_p and I_f and outputs I_{nm1} and I_{nm2}. Transistor groups (M1, M2, M4, M6), (M1, M2, M5, M7), (M1, M3, M4, M8) and (M1, M3, M5, M9) form four translinear loops which give:

$$I_6 = I_f I'_{d2} / I_{bias} \tag{3.11}$$

$$I_7 = I_f I'_{d1} / I_{bias} \tag{3.12}$$

$$I_8 = I_p I'_{d2} / I_{bias} \tag{3.13}$$

$$I_9 = I_p I'_{d1} / I_{bias} \tag{3.14}$$

If we apply KCL at nodes I_{nm1} and I_{nm2}, the difference between the currents flowing in the two nodes can be expressed as:

$$\begin{aligned} I_{nm1} - I_{nm2} &= (I_6 + I_9) - (I_7 - I_8) \\ &= \left[\left(I_f I'_{d2} + I_p I'_{d1} \right) - \left(I_f I'_{d1} + I_p I'_{d2} \right) \right] / I_{bias} \\ &= \left(I_p - I_f \right) \left(I'_{d1} - I'_{d2} \right) / I_{bias} \end{aligned} \tag{3.15}$$

The update direction for cut-off frequency of the first order low pass filter $\dot{e}_3 \propto -e_1 \dot{x}_2$ is given by the current difference between I_{nm1} and I_{nm2}.

Schematics for the learning rules and summing nodes are shown in Fig. 3.4: panel (a) shows the integrator for gain adaptation. The inputs to the circuit are the two intermediate node voltages V_{p_out} and V_{f_out} shown in Fig. 3.1. The output of the circuit is the voltage V_{g_est}. Panel (b) shows the cascode arrangement used in all current mirrors to minimize Early effect and current mismatch and to increase gain of transimpedance amplifiers. Panel (c) shows the integrator and differential pair for cut-off frequency adaptation. The inputs to the circuit are two currents I_{nm1} and I_{nm2}. The output of the circuit is the voltage V_{τ_est}.

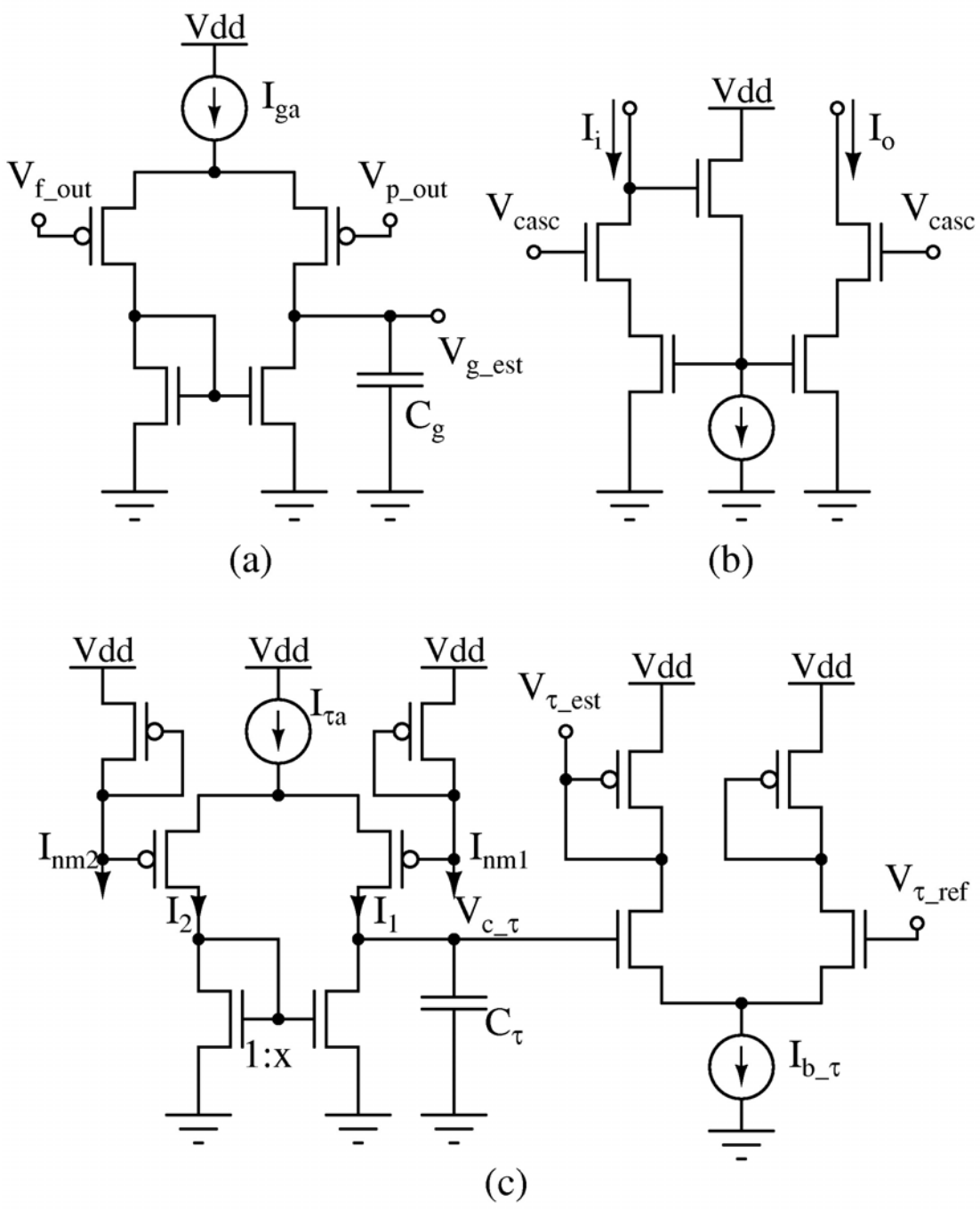


Fig. 3.4: MITE implementation of learning rules for gain and cut-off frequency.

3.2 Simulation and Experimental Results

3.2.1 Simulation Results

We simulate the circuit with HSPICE using BSIM3v3 models for a 0.5μm technology. We use the technique illustrated in Fig. 3.5 to avoid floating-node problems in the simulator [25]. A voltage-controlled voltage source $V_{floating\_gate}$ is connected from ground to the floating gate through a large resistor R. There is no current through R, because $V_{floating\_gate}$ tracks the floating gate voltage itself. This artificial DC path to ground aids numerical convergence in the HSPICE circuit simulator.

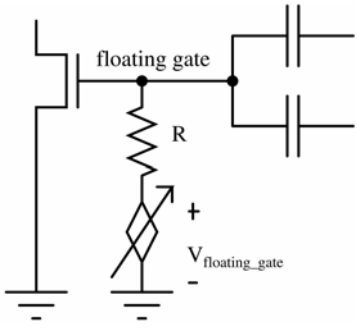


Fig. 3.5: Technique used to avoid floating-node problems in the simulator.

Fig. 3.6 shows adaptation with a 10 kHz square wave as input signal. The square wave pulses from 20 nA to 160 nA. Fig. 3.6 (a) is the error I_e between the plant and filter outputs. Fig. 3.6 (b) shows V_τ and V_{τ_est}. Fig. 3.6 (c) shows V_{gain} and V_{g_est}. We intentionally vary the cut-off frequency of the plant (by a factor of 16) and the gain (by a factor of 11 to see how well the filter adapts. The different V_τ values correspond to I_τ of 40nA from 0-2ms, 80nA from 2-3.5ms, 20nA from 3.5-5ms, 160nA from 5-

6.5ms, and 10nA from 6.5-8 ms. The voltage V_{gain} varies as 1.4V from 0-1ms, 1.5V from 1-2.5ms, 1.35V from 2.5-4ms, linearly increases from 1.4V to 1.5V from 4-5.5ms, linearly decreases from 1.5V to 1.45V from 5.5-7.5ms, and remains constant at 1.45V from 7.5-8ms. For all changes in V_τ and V_{gain}, V_{τ_est} and V_{g_est} accurately track the new values respectively. $I_e \to 0$ when $V_{\tau\_est} \to V_\tau$ and $V_{gain} \to V_{g\_est}$. V_{g_ref} is fixed at 1.5 V. The adaptation rate depends on signal strength, currents I_{ga} and $I_{\tau a}$, and capacitors C_g and C_τ.

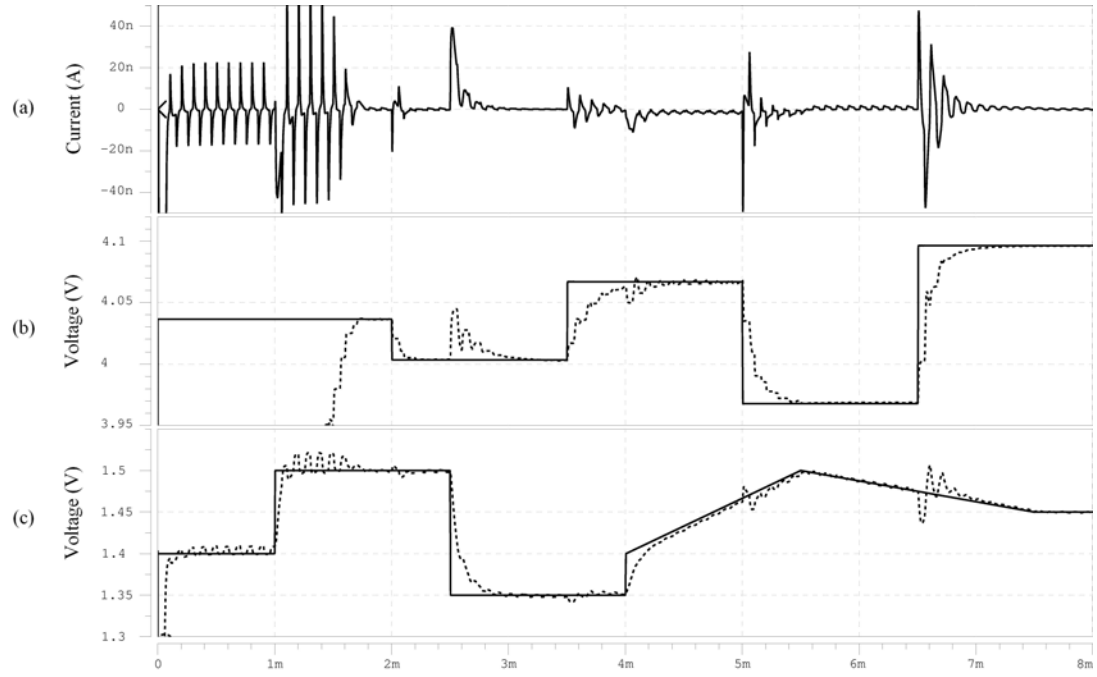


Fig. 3.6: Adaptation of gain and cut-off frequency for a 10kHz square wave input.

We also simulated this adaptive system for a variety of inputs including harmonic sine waves (a combination of sine waves equally weighted at 10kHz, 20kHz, 40kHz, and 80kHz) and geometrically spaced sine waves (a summation of 14 sine waves, whose frequency ratio is an irrational number $2\pi/5$, spanning from 5kHz to 97kHz)

[26]. For those two very different inputs, V_{τ_est} accurately tracks V_{τ} and V_{g_est} tracks V_{gain}, and I_e approaches zero when adaptation is completed.

3.2.2 Experimental Results

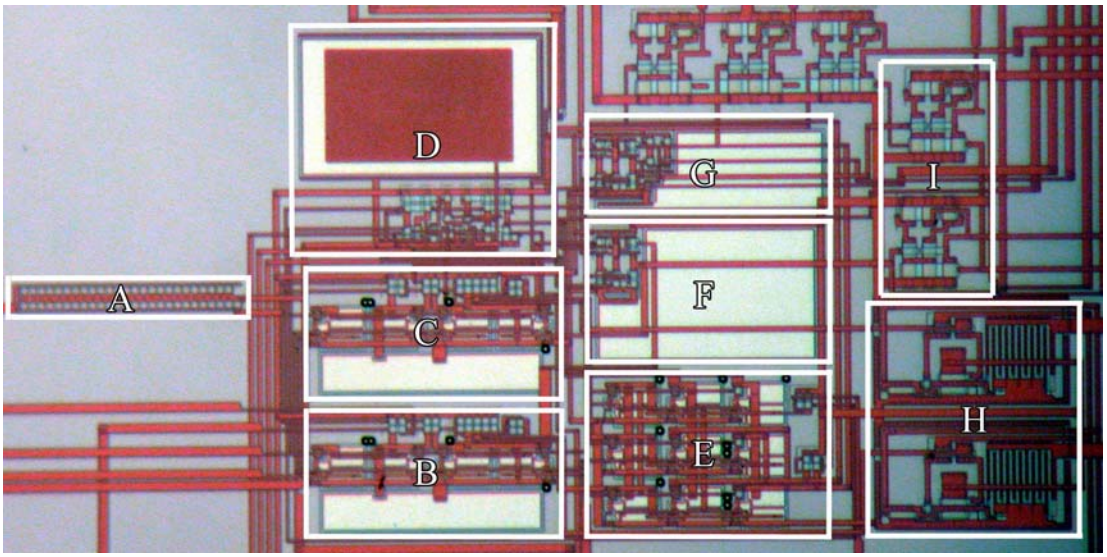


Fig. 3.7: Die photograph of the chip for the adaptive first order low pass filters.

We present measurements from a first order adaptive filter. The chip has been fabricated in a commercially available two poly, three metal 0.5 μm CMOS technology. Fig. 3.7 shows the photomicrograph of the chip comprising plant and model filters, learning circuits, and input/output buffers. These components are highlighted and labeled as follows: Part A comprises two current mirrors that scale down the input currents to both the plant and model filters. Parts B and C are the plant and model filters shown in Fig. 3.1, respectively. Part D is the derivative circuit shown in Fig. 3.2. Part E is the four quadrant multiplication circuit shown in Fig. 3.3. Parts F and G are the integration circuits for gain and cut-off frequency learning rules respectively shown in Fig. 3.4. Part H is a current output buffer with two current

conveyors to amplify the output currents. Part I is a voltage output buffer with two wide range amplifiers to buffer the gain and cut-off frequency control voltages.

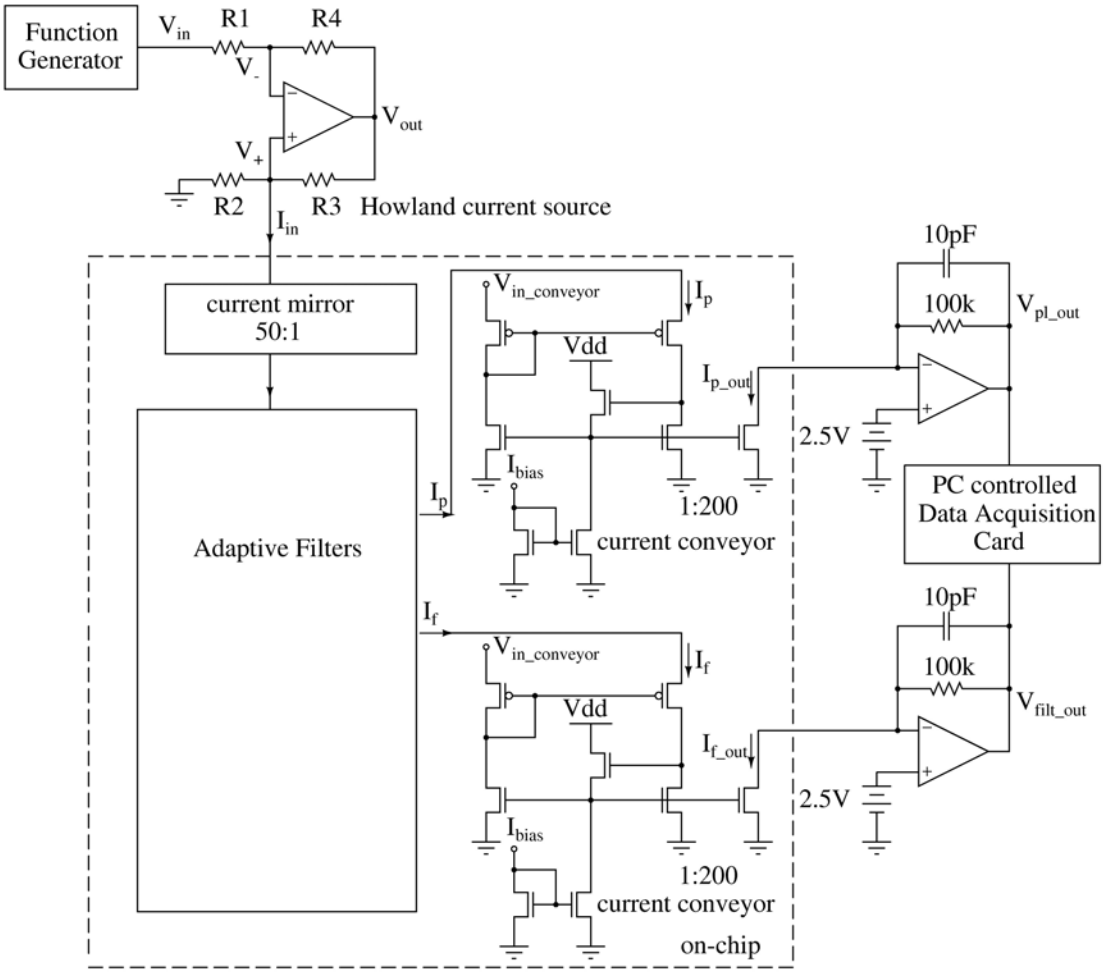


Fig. 3.8: Test setup for the adaptive first order low pass filters including schematics of input voltage-current converter (Howland current source), on-chip current conveyors, and output current-voltage converters.

The test setup is shown in Fig. 3.8. Before every experiment, the chip is exposed to UV light in order to null charges that may accumulate on the floating gate nodes. The input current and output currents are restricted to be less than several hundred nano-amperes in order for all transistors to operate in subthreshold. A 50:1 current mirror is used on-chip to scale down the input currents. A Howland current source [27]

with resistor values of $R_1 = R_2 = R_3 = R_4 = 97.6\,k\Omega$ is used off-chip to convert the input voltages to input currents according to

$$I_{in} = -V_{in}/R_2 \tag{3.16}$$

The resistors generate about 0.7 nA root-mean-square (RMS) noise current at room temperature.

Two identical current conveyors with a 1:200 current mirror are used in the output stage to amplify the output currents. Two op-amps are used with $100\,k\Omega$ resistors in the negative feedback paths, with the positive input node biased at 2.5 V to convert the output currents to output voltages, which can be easily measured with an oscilloscope or appropriate data acquisition cards. The resistors generate about 0.07mV RMS noise voltage at room temperature. Capacitors are used to attenuate the high frequency noise for the output voltages.

We use a 10kHz square wave with amplitude of 0.2 V superimposed on a DC level of 0.3 V as the input voltage to the system, which is converted to an input current with amplitude of 40nA and DC level of 60nA. When the gain and cut-off frequency of the plant filter remain constant, the error between the plant and model outputs does not exceed 4% of the plant output. We intentionally vary the gain and cut-off frequency of the plant filter to see how well the model filter adapts. Fig. 3.9(a) shows the error between the plant and model filter outputs. Fig. 3.9(b) shows the gain voltage V_{gain} and estimated gain voltage V_{g_est} for plant and model filters. Fig. 3.9(c) shows the cut-off frequency voltage V_τ and estimated cut-off frequency voltage V_{τ_est}. For all changes in V_{gain} and V_τ, we observe accurate adaptation of V_{g_est} and V_{τ_est}. The

measured power consumption of the circuits is about 33μW, including both plant and model filters and learning rule circuits. We observe a constant voltage difference of magnitude 0.07V between V_{gain} and V_{g_est}, which has been subtracted from the voltage V_{gain} shown in Fig. 3.9(b). This constant voltage difference results from residual charge on the floating gates in the plant and model filters. The dynamic range for successful gain adaptation is 50, i.e. in practice, the estimated gain tracks the true gain as it varies from 1 to 50. The dynamic range for successful cut-off frequency adaptation is one order of magnitude, i.e., in practice the estimated cut-off frequency tracks the true cut-off frequency as the cut-off frequency varies from 8kHz to 80kHz. The frequency range for the cut-off frequency adaptation can be shifted by changing the bias current I_{b_τ}, the voltage V_{τ_ref}, and the mismatch compensation currents discussed in the next section.

The measured RMS output noise is 15.7mV in Fig. 5.5. This compares to 0.387 mV for simulations without parasitic capacitances, and 12.7mV for simulations with parasitic capacitances. We further investigated which parasitics were most important in contributing to the RMS noise by selectively enabling which parasitic capacitances to include in the simulation. The results are summarized in Table 3.1. We find that the output noise is dominated by contributions arising from one particular parasitic coupling C_{mult} within the circuit, between node V_{nm2} and the floating gate of transistor M9 within the floating gate multiplier circuit shown in Fig. 3.3. The RMS noise when only crosstalk capacitors (i.e. parasitic coupling between signal nodes within the circuits) are enabled is 13.7mV. When all capacitors are enabled, the noise is slightly lower because the effective crosstalk capacitances are reduced by capacitive division.

The noise when all crosstalk capacitors except C_{mult} are enabled is 0.342mV, and the noise when all parasitic caps except C_{mult} are enabled is 0.939mV. C_{mult} is approximately 2fF, caused by a metal wire running over the floating gate.

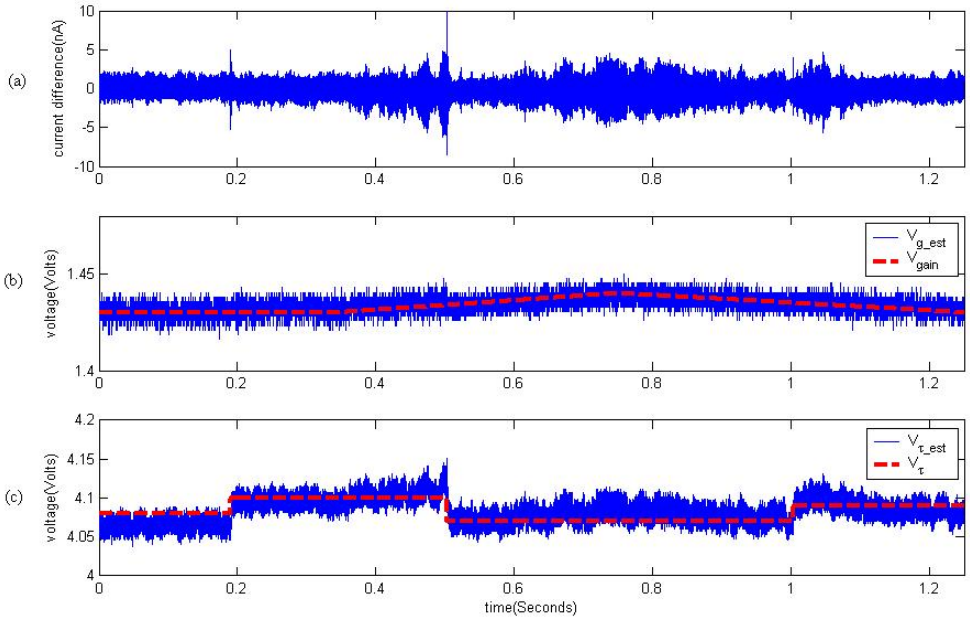


Fig. 3.9: Test results showing adaptation: (a) error of outputs between plant and model filters; (b) gain voltages for plant and model filters; (c) cut-off frequency voltages for plant and model filters.

Parasitic capacitors enabled in simulation	RMS noise
all	12.7 mV
none	0.387 mV
crosstalk capacitors	13.7 mV
crosstalk capacitors except C_{mult}	0.342 mV
all capacitors except C_{mult}	0.939 mV
between floating gates of filters and Gnd	0.398 mV
between floating gates of multipliers and Gnd	0.939 mV
between non-floating gate nodes and Gnd	0.401 mV
between non-floating gate nodes and Vdd	0.387 mV
between Vdd and Gnd	0.387 mV

Table 3.1: Simulated RMS noise voltages when different groups of parasitic capacitors are selectively enabled.

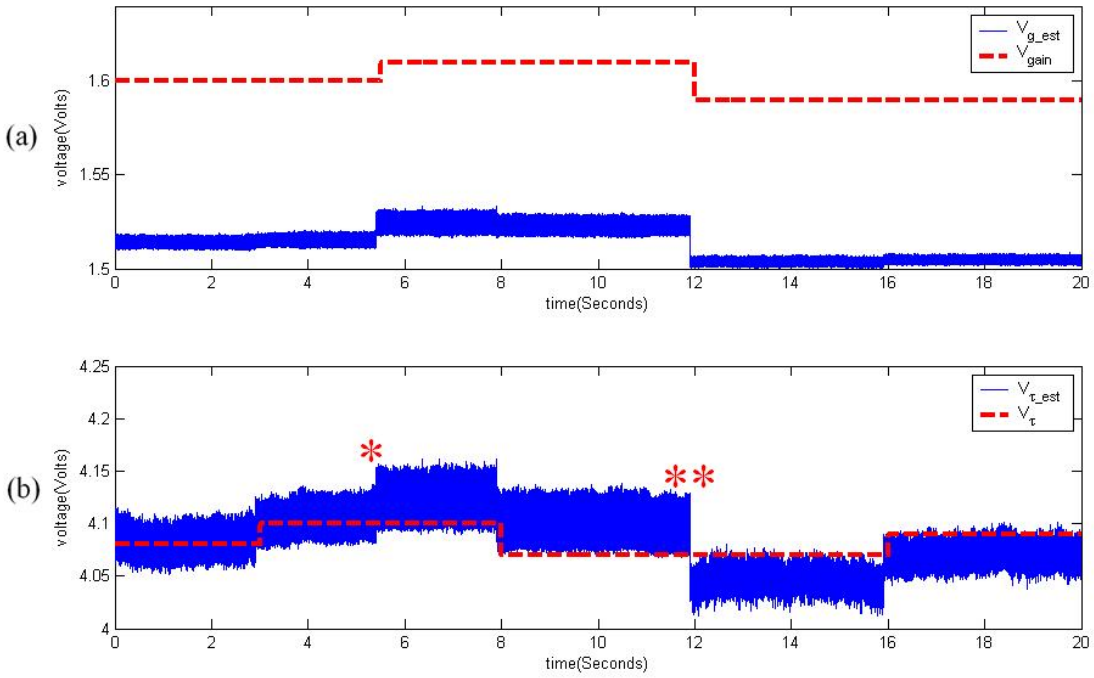


Fig. 3.10: Test results of adaptive filter illustrating the case x>1 for mismatch analysis: changes in gain create artifacts in the estimated cut-off frequency.

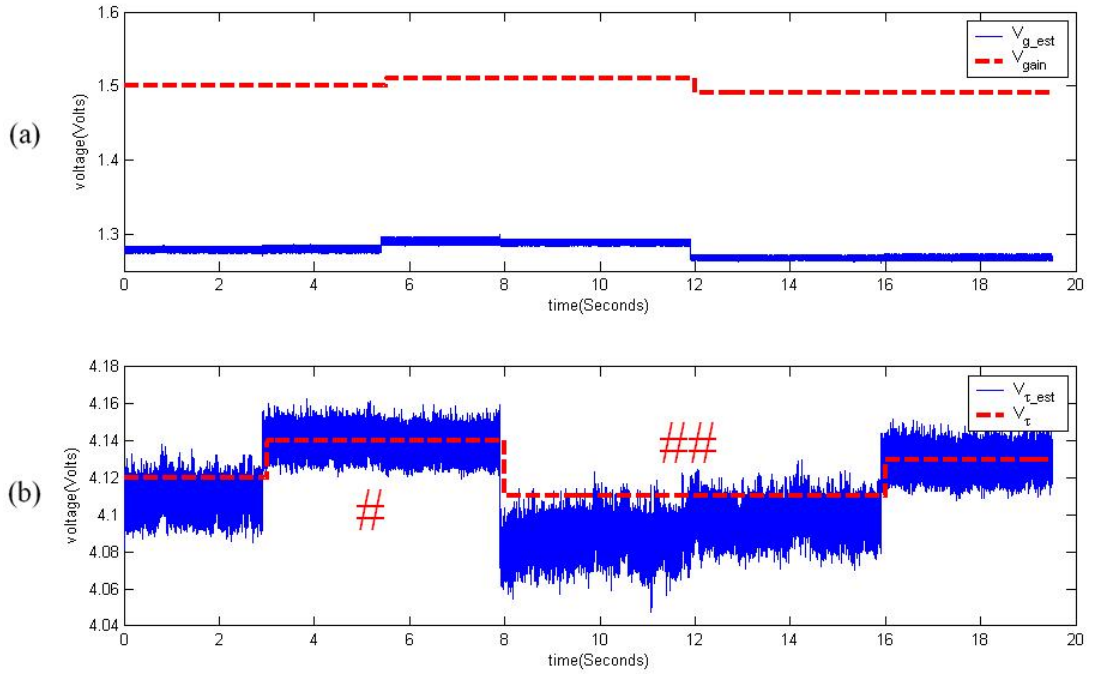


Fig. 3.11: Test results of adaptive filter illustrating the case 0<x<1 for mismatch analysis: changes in gain create artifacts in the estimated cut-off frequency.

Fig. 3.10 and Fig. 3.11 show test results for two different chips over long time periods, which demonstrate the undesirable interaction between adaptation of gain and cut-off frequency which results from mismatch within the analog system. Fig. 3.10(a) and Fig. 3.11(a) show the gain voltages V_{gain} and V_{g_est} for plant and model filters. Fig. 3.10(b) and Fig. 3.11 (b) show the cut-off frequency voltages V_{τ} and V_{τ_est}. In the following section we present mismatch analysis which accounts for the observed discrepancies between V_{τ} and V_{τ_est}.

Chapter 4: Mismatch and Harmonic Distortion Analysis

4.1 Mismatch Analysis

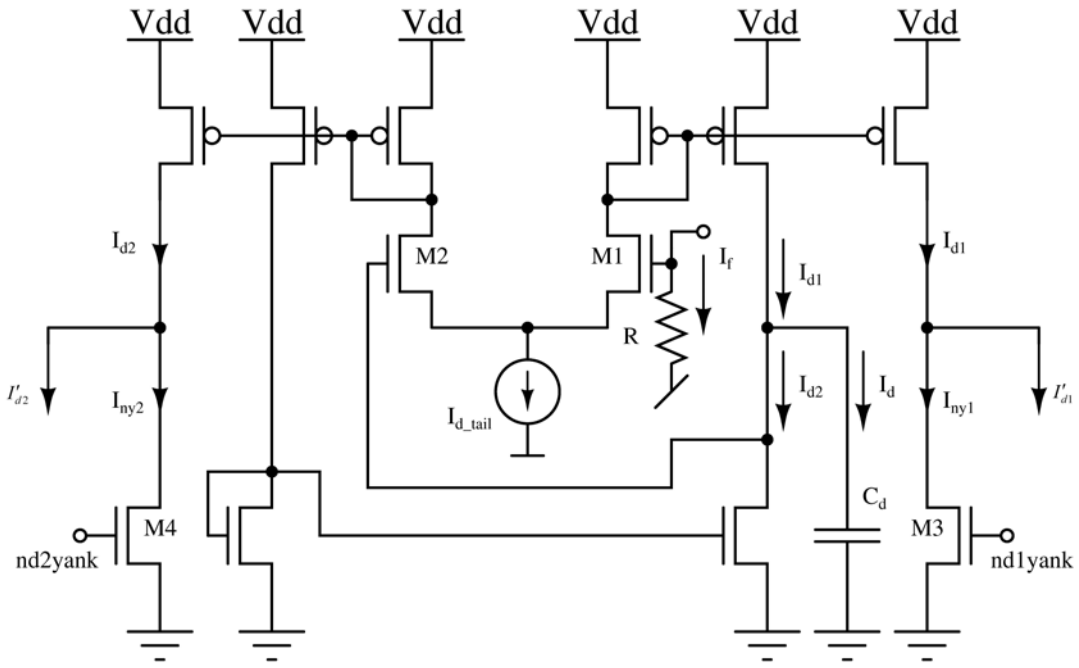


Fig. 4.1: Circuit for computing temporal derivative with mismatch compensation. (shown in Chapter 3 as Fig. 3.2)

The derivative circuit shown in Fig. 4.1 includes two mismatch adjustment NMOS transistors M3 and M4 which provide a constant offset to adjust the currents I_{d1} and I_{d2}. Thus the actual currents passing on to the multiplier circuits in the next stage are I'_{d1} and I'_{d2}. We use the two voltages nd1yank and nd2yank to partially cancel current mirror mismatches in the implementation of learning rules.

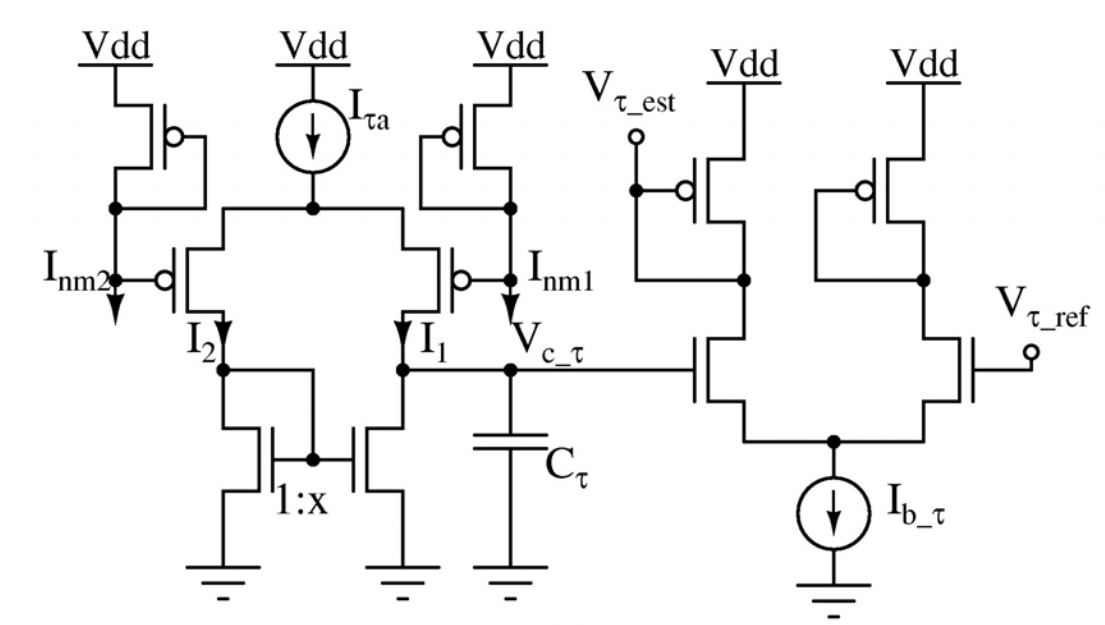


Fig. 4.2: MITE implementation of learning rules for cut-off frequency. (shown in Chapter 3 as Fig. 3.4c).

Consider the implementation of the cut-off frequency learning rule shown in Fig. 4.2. Suppose that the mismatch of this circuit is limited to current mirror mismatch, and that the actual ratio is $1:x$ compared to the ideal ratio 1:1, where x is a constant around 1. Ideally, without mismatch compensation we have

$$I_1 = c\left(I_p I_{d1} + I_f I_{d2}\right)/ I_{bias} \tag{4.1}$$

$$I_2 = c\left(I_p I_{d2} + I_f I_{d1}\right)/ I_{bias} \tag{4.2}$$

where I_p is the output current of the plant filter and I_f is the output current of the model filter. I_{d1} and I_{d2} are the output currents of the derivative circuit, and c and I_{bias} are constants. When mismatch compensation is introduced as in Fig. 4.1, the modified currents I_1' and I_2' that replace the ideal currents I_1 and I_2 are given by:

$$I_1^{'} = c'\left[I_p\left(I_{d1} - I_{ny1}\right) + I_f\left(I_{d2} - I_{ny2}\right)\right]/ I_{bias} \tag{4.3}$$

$$I_2' = c'\left[I_p\left(I_{d2} - I_{ny2}\right) + I_f\left(I_{d1} - I_{ny1}\right)\right] / I_{bias} \tag{4.4}$$

where I_{ny1} is the current flowing in NMOS transistor M3 to ground and I_{ny2} is the current flowing in NMOS transistor M4 to ground for the temporal derivative circuit shown in Fig. 4.1, and c' is a constant.

The tail current of the differential pair for the cut-off frequency circuit $I_{tail} = I_1 + I_2 = I_1' + I_2'$ is constant. This equality holds for all values of I_p and I_f, in particular for $I_p = I_f$, so

$$c' = \frac{I_{d\_tail}}{I_{d\_tail} - I_{ny1} - I_{ny2}} c \tag{4.5}$$

$$I_{d\_tail} = I_{d1} + I_{d2} \tag{4.6}$$

If we further assume that the time required for adaptation t_0 is the same in both cases, and that the mismatch compensation provided by M3 and M4 works well enough to ensure that both cases converge to the same voltage at capacitor C_τ, we obtain

$$\int_0^{t_0} (I_1 - I_2) dt = \int_0^{t_0} (I_1' - xI_2') dt \tag{4.7}$$

For simplicity of analysis, we consider only the case that ($I_{ny1} > 0$, $I_{ny2} = 0$) as observed empirically in all chips tested thus far. We substitute equations (4.1)-(4.4) into (4.7), and find the current I_{ny1}^* which compensates the current mirror ratio mismatch $1 : x$.

$$I_{ny1}^{*} = \frac{I_{d\_tail} I_{bias} \dfrac{x-1}{2} \left[\int_0^{t_0} I_{\tau a} dt - \int_0^{t_0} (I_1 - I_2) dt \right]}{cI_{d\_tail} \int_0^{t_0} (xI_f - I_p) dt + I_{bias} \int_0^{t_0} (I_1 - I_2) dt} \tag{4.8}$$

The current difference $(I_1 - I_2)$ controls the capacitor voltage, which determines the estimated cut-off frequency. Assuming an initial capacitor voltage of 0V, we obtain

$$\int_0^{t_0} (I_1 - I_2) dt = C_\tau V_{c\_\tau} \tag{4.9}$$

If we further assume that the plant and model filters share the same DC current level, i.e. $\bar{I}_p = \bar{I}_f = I_b$, we obtain

$$\int_0^{t_0} I_p dt = \int_0^{t_0} I_f dt = I_b t_0 \tag{4.10}$$

By substituting (4.9) and (4.10) into (4.8), we obtain

$$I_{ny1}^{*} = X \cdot \frac{Y - V_{c\_\tau}}{Z + V_{c\_\tau}} \tag{4.11}$$

where X, Y, and Z are defined as

$$X \equiv \frac{(x-1) I_{d\_tail}}{2} \tag{4.12}$$

$$Y \equiv \frac{I_{\tau a} t_0}{C_t} \tag{4.13}$$

$$Z \equiv \frac{cI_{d\_tail}}{I_{bias} C_t} (x-1) I_b t_0 \tag{4.14}$$

In ideal matched current mirrors,

$$V_{c\_\tau}(desired) = \frac{1}{C_\tau}\int_0^{t_0}(I_1 - I_2)dt \tag{4.15}$$

In mismatched current mirrors,

$$V_{c\_\tau}(actual) = \frac{1}{C_\tau}\int_0^{t_0}(I_1' - xI_2')dt \tag{4.16}$$

We consider three mismatch conditions: $x > 1$, $x < 1$ and $x = 1$. All discussions below are for the case $x > 1$. The results are opposite for $x < 1$. When $x = 1$, there is no mismatch and I_{ny1}^* is zero as we expect.

$x > 1 \Rightarrow X > 0$ and $Z > 0$.

First we examine the consequences of values for $I_{ny1} \neq I_{ny1}^*$ which do not exactly compensate the mismatch. Since $I_{ny1}^* > 0$, we know from (6.11) that $-Z < V_{c\_\tau} < Y$, so $(Z + V_{c\_\tau}) > 0$.

Let us go back to equations (4.7), (4.8) and (4.11). By examining the inequality corresponding with Eqn. (4.7) and its effects on Eqns. (4.8) and (4.11), we find:

$$I_{ny1} > I_{ny1}^* \Rightarrow \int_0^{t_0}(I_1 - I_2)dt < \int_0^{t_0}\left(I_1' - xI_2'\right)dt$$
$$\Rightarrow V_{c\_\tau}(desired) < V_{c\_\tau}(actual) \Rightarrow V_\tau > V_{\tau\_est}$$

When I_{ny1} is too high, the cut-off frequency voltage is underestimated.

Next we consider the effect of a change in gain on the cut-off frequency adaptation. Assuming that V_{τ_est} tracks V_τ accurately and has converged to V_τ, which implies that

$$I_{ny1} = I^*_{ny1} = X \cdot \frac{Y - V_{c\_\tau}}{Z + V_{c\_\tau}} \Rightarrow V_{c\_\tau} = \frac{XY - ZI^*_{ny1}}{X + I^*_{ny1}}$$

$$\Rightarrow \frac{\partial V_{c\_\tau}}{\partial Z} = -\frac{I^*_{ny1}}{X + I^*_{ny1}} < 0$$

$V_{gain} \uparrow \Rightarrow gain \uparrow \Rightarrow I_b \uparrow \Rightarrow Z \uparrow \Rightarrow V_{c\_\tau} \downarrow \Rightarrow V_{\tau\_est} \uparrow$ Therefore an increase in gain causes the cut-off frequency voltage to be overestimated.

Finally we examine the effect of the cut-off frequency on the cut-off frequency adaptation. Here we investigate this problem by differentiating equation (4.11). Assuming that the gain does not change, then X, Y and Z are all constants which gives $\dot{X} = \dot{Y} = \dot{Z} = 0$.

$$\dot{I}^*_{ny1} = X \frac{-\dot{V}_{c\_\tau}(Z + V_{c\_\tau}) - \dot{V}_{c\_\tau}(Y - V_{c\_\tau})}{(Z + V_{c\_\tau})^2}$$

$$= \frac{-X(Y+Z)}{(Z + V_{c\_\tau})^2} \dot{V}_{c\_\tau}$$

$$\frac{\partial I^*_{ny1}}{\partial V_{c\_\tau}} = \frac{-X(Y+Z)}{(Z + V_{c\_\tau})^2} < 0 \qquad (4.17)$$

Therefore $V_\tau \uparrow \Rightarrow V_{c\_\tau} \downarrow \Rightarrow I^*_{ny1} \uparrow$, and an increase in the cut-off frequency voltage requires higher compensation current to balance mismatch.

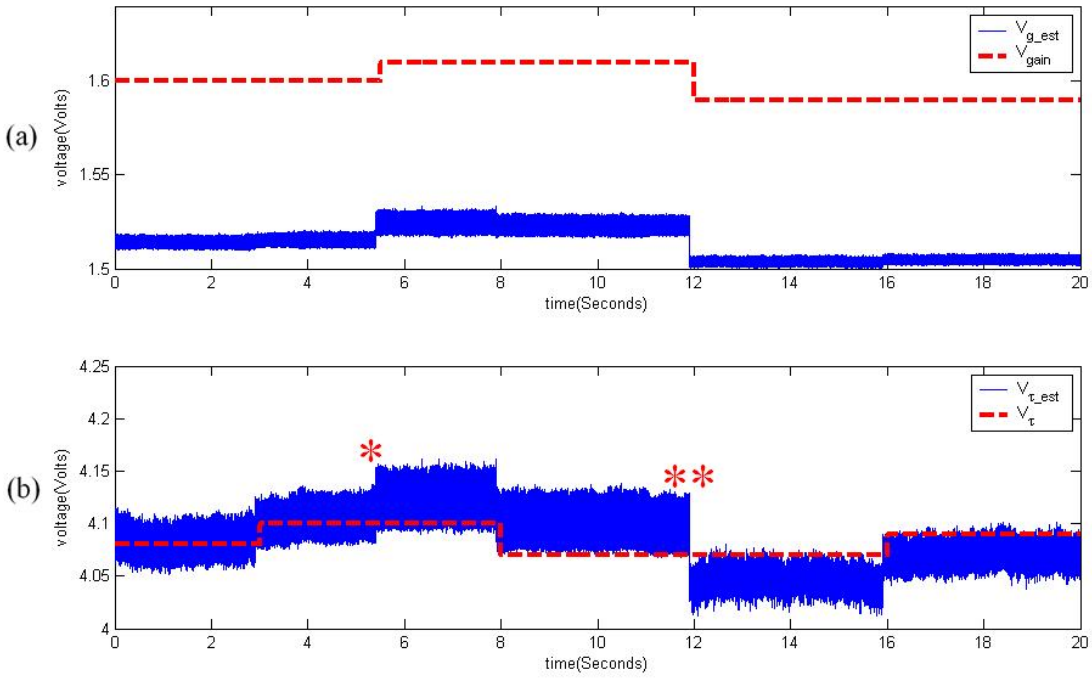


Fig. 4.3: Test results of adaptive filter illustrating the case x>1 for mismatch analysis: changes in gain create artifacts in the estimated cut-off frequency. (shown in Chapter 3 as Fig. 3.10)

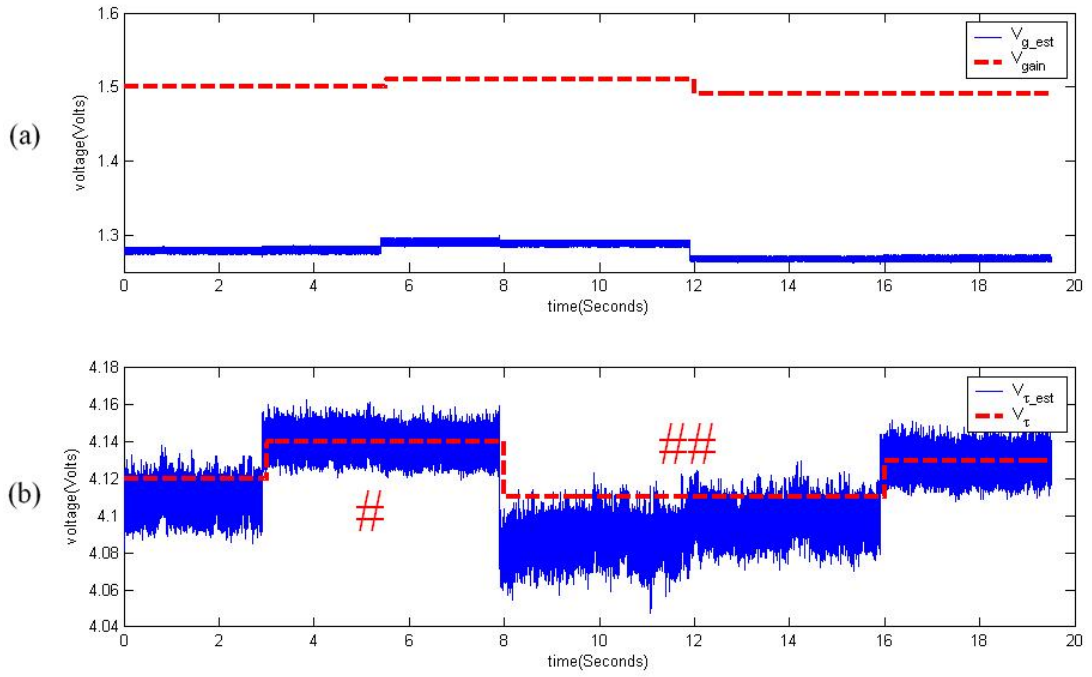


Fig. 4.4: Test results of adaptive filter illustrating the case 0<x<1 for mismatch analysis: changes in gain create artifacts in the estimated cut-off frequency. (shown in Chapter 3 as Fig. 3.11)

Both conditions $x > 1$ and $x < 1$ have been observed in the testing of two different chips from the same run. Illustrative results are shown in Figs. 4.3 and 4.4. In each figure, the current I_{ny1} remains constant. The preceding analysis explains the observed discrepancies in the test results. In Fig. 4.3, for $x > 1$, the estimated cut-off frequency increases as the true and estimated gain increases, although the true cut-off frequency does not change. Likewise the estimated cut-off frequency voltage decreases as the gain decreases when the true cut-off frequency remains the same. In Fig. 4.4, for $0 < x < 1$, the estimated cut-off frequency voltage decreases slightly when the gain increases and increases when the gain decreases, although the true cut-off frequency is fixed. Table 4.1 summarizes the results of the mismatch analysis. Four of the cases in Table 4.1 ($x > 1 / x < 1$, $gain \uparrow / gain \downarrow$) are illustrated by the data in Figs. 4.3 and 4.4 at the locations labeled by symbols (*, **, #, ##).

	I_{ny1} vs I^*_{ny1}	$gain$ vs V_{τ_est}	V_τ vs I^*_{ny1}
$x > 1$	$I_{ny1} > I^*_{ny1} \Rightarrow V_{\tau\_est} < V_\tau$ $I_{ny1} < I^*_{ny1} \Rightarrow V_{\tau\_est} > V_\tau$	$gain \uparrow \Rightarrow V_{\tau\_est} \uparrow$ * $gain \downarrow \Rightarrow V_{\tau\_est} \downarrow$ **	$V_\tau \uparrow \Rightarrow I^*_{ny1} \uparrow$ $V_\tau \downarrow \Rightarrow I^*_{ny1} \downarrow$
$x < 1$	$I_{ny1} > I^*_{ny1} \Rightarrow V_{\tau\_est} > V_\tau$ $I_{ny1} < I^*_{ny1} \Rightarrow V_{\tau\_est} < V_\tau$	$gain \uparrow \Rightarrow V_{\tau\_est} \downarrow$ # $gain \downarrow \Rightarrow V_{\tau\_est} \uparrow$ ##	$V_\tau \uparrow \Rightarrow I^*_{ny1} \downarrow$ $V_\tau \downarrow \Rightarrow I^*_{ny1} \uparrow$

Table 4.1: Effects of the current mirror ratio mismatch on the estimated cut-off frequency and compensating current.

4.2 Harmonic Distortion Analysis

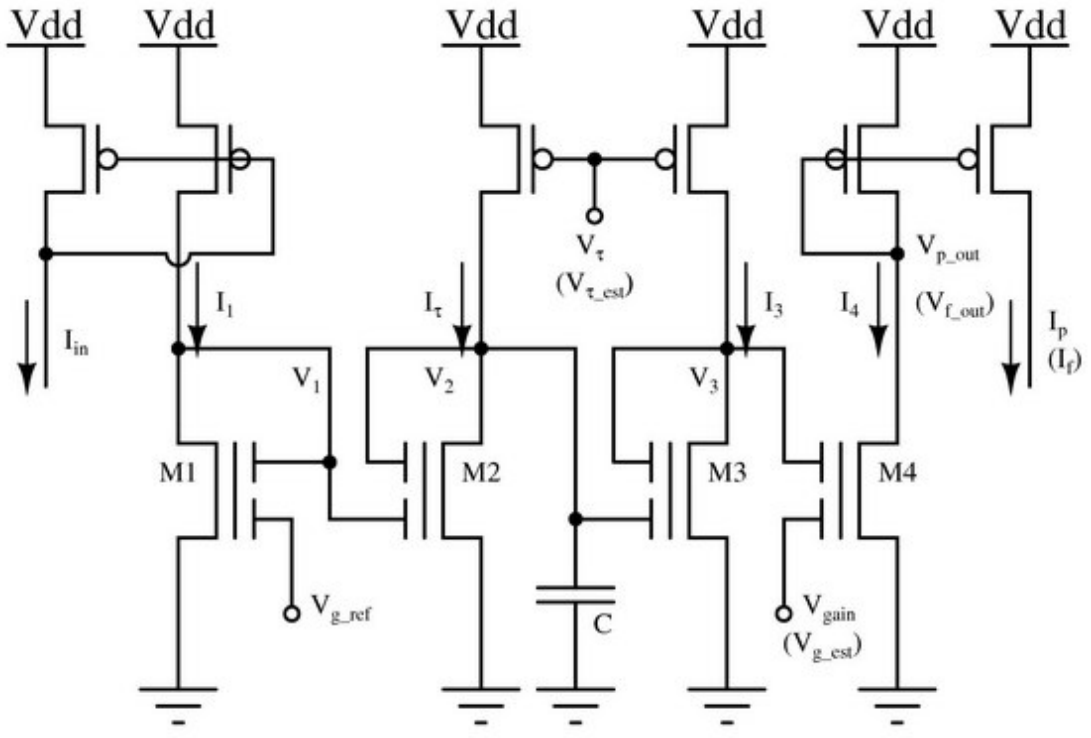


Fig. 4.5: Log domain MITE filter topology for a first order low pass transfer function used for both plant and filter. (shown in Chapter 3 as Fig. 3.1)

The plant and the model filters we used for the adaptive system shown in Fig. 4.5 are linear filters when transistors M1, M2, M3 and M4 operate in subthreshold. If the input current increases, those transistors will operate on the edge between subthreshold region and above threshold region. It will introduce distortion to the output of the filter structure and affect the ability for the whole system to adapt. In this chapter, we set up models in Matlab to analyze the harmonic distortion of the filter in transitional operating range. We use EKV model to estimate the transistor behavior on the edge between subthreshold and above threshold regions, and compare with the results using subthreshold model and above threshold model. This will give a more accurate idea about how the filter works in reality.

4.2.1 Three Transistor Models

We define following parameters to illustrate the three transistor models which will be used to analyze the harmonic distortion.

I_D drain current

V_{GS} gate to source voltage

V_T threshold voltage

W/L width to length ratio

μ carrier mobility

C_{ox} gate oxide capacitance

ϕ_t thermal voltage KT/q

In subthreshold operation the current of a transistor is an exponential function of voltage as in equation (4.18). Here we take the slope factor as 1 for simplicity.

$$I_D = 2\frac{W}{L}\mu C_{ox}\phi_t^2 e^{\frac{V_{GS}-V_T}{\phi_t}} \tag{4.18}$$

In strong inversion saturation operation the current of a transistor follows square law as in equation (4.19).

$$I_D = \frac{W}{2L}\mu C_{ox}\left(V_{GS}-V_T\right)^2 \tag{4.19}$$

The above two operation transfer functions are not smoothly continuous when V_{GS} varies from below threshold voltage to above threshold voltage. Therefore, the

EKV model [28] is developed as a mathematical reconciliation to solve this problem. A simplified EKV model can be written as in equation (4.20).

$$I_D = 2\frac{W}{L}\mu C_{ox}\phi_t^2\left[\ln\left(1+e^{\frac{V_{GS}-V_T}{2\phi_t}}\right)\right]^2 \tag{4.20}$$

Assume $x = \frac{V_{GS}-V_T}{\phi_t}$ and $w = e^{\frac{x}{2}}$ for simplicity.

When w is very small, Taylor series tells us

$$\ln(1+w) = w - \frac{1}{2}w^2 + \frac{1}{3}w^3 - \frac{1}{4}w^4 + \ldots \approx w \tag{4.21}$$

If we substitute equation (4.21) to the EKV model (4.20), we can see that it agrees with the subthreshold model (4.18). The condition of this agreement is that the gate to source voltage V_{GS} is around the threshold voltage V_T, so that both x and w are small enough.

While when x is large, so that $e^{\frac{x}{2}} >> 1$

$$\left[\ln(1+e^{\frac{x}{2}})\right]^2 \approx \left[\ln(e^{\frac{x}{2}})\right]^2 = \left[\frac{x}{2}\right]^2 \tag{4.22}$$

Equation (4.22) makes the EKV model (4.20) the same as the transfer function (4.19) in strong inversion saturation. The condition of consistency is that the gate to source voltage V_{GS} is well above threshold voltage V_T, so that x is big enough. The EKV model itself is continuous across the full range of possible V_{GS} and provides a good estimation of subthreshold range and above threshold range. Therefore, it is very convenient to use EKV model to evaluate circuits operating in moderate inversion.

4.2.2 Circuit Behavior Using Different Transistor Models

Two parameters are defined below for simplicity to analyze the circuit behavior using the three transistor models.

$$I_0 = 2\mu C_{ox}\frac{W}{L}\phi_t^2 \tag{4.23}$$

$$K = \frac{1}{\phi_t} \tag{4.24}$$

4.2.2.1 Low pass filter in subthreshold as designed

We use subthreshold model (4.18) to evaluate the circuit in Fig. 4.5 when transistors M1, M2, M3 and M4 are biased at subthreshold range. The MITE currents flowing across transistors M1, M2, M3 and M4 can be expressed respectively as

$$I_1 = I_0 e^{K\left(\frac{V_1+V_{g\_ref}}{2}-V_T\right)} = I_{in} \Rightarrow e^{K\left(\frac{V_1+V_{g\_ref}}{2}-V_T\right)} = \frac{I_{in}}{I_0} \tag{4.25}$$

$$I_2 = I_0 e^{K\left(\frac{V_1+V_2}{2}-V_T\right)} \Rightarrow e^{K\left(\frac{V_1+V_2}{2}-V_T\right)} = \frac{I_2}{I_0} \tag{4.26}$$

$$I_3 = I_0 e^{K\left(\frac{V_2+V_3}{2}-V_T\right)} = I_\tau \Rightarrow e^{K\left(\frac{V_2+V_3}{2}-V_T\right)} = \frac{I_\tau}{I_0} \tag{4.27}$$

$$I_4 = I_0 e^{K\left(\frac{V_3+V_{gain}}{2}-V_T\right)} = I_{out} \Rightarrow e^{K\left(\frac{V_3+V_{gain}}{2}-V_T\right)} = \frac{I_{out}}{I_0} \tag{4.28}$$

The exponential equations form a relationship among the four MITE currents as

$$\frac{I_{in}}{I_0}\frac{I_\tau}{I_0}e^{K\left(\frac{V_{gain}-V_{g\_ref}}{2}\right)} = \frac{I_2}{I_0}\frac{I_{out}}{I_0} \tag{4.29}$$

which gives an expression of current flowing in transistor M2.

$$I_2 = \frac{I_{in} I_\tau}{I_{out}} e^{K\left(\frac{V_{gain} - V_{g\_ref}}{2}\right)} \tag{4.30}$$

The derivative of the output current I_{out} can be calculated from equation (4.28) as

$$\dot{I}_{out} = I_0 e^{K\left(\frac{V_3 + V_{gain}}{2} - V_T\right)} \cdot \frac{K\dot{V}_3}{2} = I_{out} \cdot \frac{K\dot{V}_3}{2} \tag{4.31}$$

The equation (4.31) can be used to calculate the derivative of V_2 as below since the sum of V_2 and V_3 yields a constant current I_τ in equation (4.27).

$$\dot{V}_2 = -\dot{V}_3 = -\frac{2\dot{I}_{out}}{KI_{out}} \tag{4.32}$$

We apply Kirchoff's Current Law (KCL) at the capacitive node and obtain

$$C\dot{V}_2 + I_2 = I_\tau \tag{4.33}$$

By substituting the expression of $\dot{V}_2$ in equation (4.32) and I_2 in equation (4.30) to equation (4.33), a first order differential equation of the output current is derived as

$$\dot{I}_{out} = \frac{KI_{in} I_\tau}{2C} e^{K\left(\frac{V_{gain} - V_{g\_ref}}{2}\right)} - \frac{K}{2C} I_\tau I_{out} \tag{4.34}$$

The above equation (4.34) has a Laplace form of

$$\frac{I_{out}}{I_{in}} = \frac{e^{K\left(\frac{V_{gain} - V_{g\_ref}}{2}\right)}}{\frac{2C}{KI_\tau} s + 1} \tag{4.35}$$

Equation (4.35) is the transfer function of the filter when all the transistors operate in weak inversion. It is a first order low pass filter as used in the adaptive system. The gain of the low pass filter is $e^{K\left(\frac{V_{gain}-V_{g\_ref}}{2}\right)}$ and the cut-off frequency is $\frac{KI_\tau}{2C}$ in rad/s.

4.2.2.2 Circuit behavior using simplified EKV model

We use a simplified EKV model (4.20) to evaluate the circuit in Fig. 4.5 when transistors M1, M2, M3 and M4 operate in moderate inversion. Simplified by equations (4.23) and (4.24), the MITE currents in transistors M1, M2, M3 and M4 can be formulated as

$$I_1 = I_0\left[\ln\left(1+e^{\frac{K}{2}\left(\frac{V_1+V_{g\_ref}}{2}-V_T\right)}\right)\right]^2 = I_{in} \Rightarrow e^{\frac{K}{2}\left(\frac{V_1+V_{g\_ref}}{2}-V_T\right)} = e^{\sqrt{\frac{I_{in}}{I_0}}}-1 \quad (4.36)$$

$$I_2 = I_0\left[\ln\left(1+e^{\frac{K}{2}\left(\frac{V_1+V_2}{2}-V_T\right)}\right)\right]^2 \Rightarrow e^{\frac{K}{2}\left(\frac{V_1+V_2}{2}-V_T\right)} = e^{\sqrt{\frac{I_2}{I_0}}}-1 \quad (4.37)$$

$$I_3 = I_0\left[\ln\left(1+e^{\frac{K}{2}\left(\frac{V_2+V_3}{2}-V_T\right)}\right)\right]^2 = I_\tau \Rightarrow e^{\frac{K}{2}\left(\frac{V_2+V_3}{2}-V_T\right)} = e^{\sqrt{\frac{I_\tau}{I_0}}}-1 \quad (4.38)$$

$$I_4 = I_0\left[\ln\left(1+e^{\frac{K}{2}\left(\frac{V_3+V_{gain}}{2}-V_T\right)}\right)\right]^2 = I_{out} \Rightarrow e^{\frac{K}{2}\left(\frac{V_3+V_{gain}}{2}-V_T\right)} = e^{\sqrt{\frac{I_{out}}{I_0}}}-1 \quad (4.39)$$

The exponential equations form a relationship among the four MITE currents as

$$\left(e^{\sqrt{\frac{I_{in}}{I_0}}}-1\right)\left(e^{\sqrt{\frac{I_\tau}{I_0}}}-1\right)e^{\frac{K}{2}\left(\frac{V_{gain}-V_{g\_ref}}{2}\right)} = \left(e^{\sqrt{\frac{I_2}{I_0}}}-1\right)\left(e^{\sqrt{\frac{I_{out}}{I_0}}}-1\right) \quad (4.40)$$

which gives

$$I_2 = I_0\left[\ln\left(\frac{e^{\frac{K}{2}\left(\frac{V_{gain}-V_{g\_ref}}{2}\right)}\left(e^{\sqrt{\frac{I_{in}}{I_0}}}-1\right)\left(e^{\sqrt{\frac{I_\tau}{I_0}}}-1\right)}{\left(e^{\sqrt{\frac{I_{out}}{I_0}}}-1\right)}+1\right)\right]^2 \tag{4.41}$$

The derivative of the output current I_{out} can be calculated from equation (4.39) as

$$\begin{aligned}\dot{I}_{out} &= 2I_0\ln\left(1+e^{\frac{K}{2}\left(\frac{V_3+V_{gain}}{2}-V_T\right)}\right)\cdot\frac{\frac{K}{2}\frac{\dot{V}_3}{2}e^{\frac{K}{2}\left(\frac{V_3+V_{gain}}{2}-V_T\right)}}{1+e^{\frac{K}{2}\left(\frac{V_3+V_{gain}}{2}-V_T\right)}} \\ &= I_0\sqrt{\frac{I_{out}}{I_0}}\cdot\frac{K}{2}\dot{V}_3\cdot\frac{e^{\sqrt{\frac{I_{out}}{I_0}}}-1}{e^{\sqrt{\frac{I_{out}}{I_0}}}} = \frac{K}{2}\dot{V}_3\sqrt{I_0 I_{out}}\,\frac{e^{\sqrt{\frac{I_{out}}{I_0}}}-1}{e^{\sqrt{\frac{I_{out}}{I_0}}}}\end{aligned} \tag{4.42}$$

The equation (4.42) can be used to calculate the derivative of V_2 as below since the sum of V_2 and V_3 yields a constant current I_τ in equation (4.38).

$$\dot{V}_2 = -\dot{V}_3 = -\frac{\dot{I}_{out}e^{\sqrt{\frac{I_{out}}{I_0}}}}{\frac{K}{2}\sqrt{I_0 I_{out}}\left(e^{\sqrt{\frac{I_{out}}{I_0}}}-1\right)} \tag{4.43}$$

We apply Kirchoff's Current Law (KCL) at the capacitive node and obtain

$$C\dot{V}_2 + I_2 = I_\tau \tag{4.44}$$

Now we substitute the expression of $\dot{V}_2$ in equation (4.43) and I_2 in equation (4.41) to equation (4.44).

$$-\frac{C\dot{I}_{out}e^{\sqrt{\frac{I_{out}}{I_0}}}}{\frac{K}{2}\sqrt{I_0 I_{out}}\left(e^{\sqrt{\frac{I_{out}}{I_0}}}-1\right)}+I_0\left[\ln\left(\frac{e^{\frac{K}{2}\left(\frac{V_{gain}-V_{g\_ref}}{2}\right)}\left(e^{\sqrt{\frac{I_{in}}{I_0}}}-1\right)\left(e^{\sqrt{\frac{I_\tau}{I_0}}}-1\right)}{\left(e^{\sqrt{\frac{I_{out}}{I_0}}}-1\right)}+1\right)\right]^2=I_\tau \quad (4.45)$$

The first order differential equation of the output current $\dot{I}_{out}$ is formulated in a very complex form. In order to simplify the formula, a new variable related to the output current I_{out} is defined as

$$y=e^{\sqrt{\frac{I_{out}}{I_0}}}-1 \quad (4.46)$$

And the derivative of the new variable is

$$\dot{y}=e^{\sqrt{\frac{I_{out}}{I_0}}}\frac{\dot{I}_{out}}{2\sqrt{I_0 I_{out}}} \quad (4.47)$$

By substituting equations (4.46) and (4.47), the differential equation (4.45) can be simplified as

$$\dot{y}=\frac{KI_0}{4C}y\left[\ln\left(\frac{e^{K\left(\frac{V_{gain}-V_{g\_ref}}{2}\right)}\left(e^{\sqrt{\frac{I_{in}}{I_0}}}-1\right)\left(e^{\sqrt{\frac{I_\tau}{I_0}}}-1\right)}{y}+1\right)\right]^2-\frac{KI_\tau}{4C}y \quad (4.48)$$

4.2.2.3 Circuit behavior in above threshold region

We use above threshold model (4.19) to evaluate the circuit in Fig. 4.5 when transistors M1, M2, M3 and M4 are forced to strong inversion saturation operation.

Let us assume $I_{abv} = \mu C_{ox} \frac{W}{2L}$ for briefness. The MITE currents flowing in transistors M1, M2, M3 and M4 can be expressed respectively as

$$I_1 = I_{abv}\left(\frac{V_1 + V_{g\_ref}}{2} - V_T\right)^2 = I_{in} \Rightarrow \frac{V_1 + V_{g\_ref}}{2} - V_T = \sqrt{\frac{I_{in}}{I_{abv}}} \qquad (4.49)$$

$$I_2 = I_{abv}\left(\frac{V_1 + V_2}{2} - V_T\right)^2 \Rightarrow \frac{V_1 + V_2}{2} - V_T = \sqrt{\frac{I_2}{I_{abv}}} \qquad (4.50)$$

$$I_3 = I_{abv}\left(\frac{V_2 + V_3}{2} - V_T\right)^2 = I_\tau \Rightarrow \frac{V_2 + V_3}{2} - V_T = \sqrt{\frac{I_\tau}{I_{abv}}} \qquad (4.51)$$

$$I_4 = I_{abv}\left(\frac{V_3 + V_{gain}}{2} - V_T\right)^2 = I_{out} \Rightarrow \frac{V_3 + V_{gain}}{2} - V_T = \sqrt{\frac{I_{out}}{I_{abv}}} \qquad (4.52)$$

The square law equations form a relationship among the four MITE currents as

$$\sqrt{\frac{I_{in}}{I_{abv}}} + \sqrt{\frac{I_\tau}{I_{abv}}} + \frac{V_{gain} - V_{g\_ref}}{2} = \sqrt{\frac{I_2}{I_{abv}}} + \sqrt{\frac{I_{out}}{I_{abv}}} \qquad (4.53)$$

which gives

$$I_2 = I_{abv}\left(\frac{V_{gain} - V_{g\_ref}}{2} + \sqrt{\frac{I_{in}}{I_{abv}}} + \sqrt{\frac{I_\tau}{I_{abv}}} - \sqrt{\frac{I_{out}}{I_{abv}}}\right)^2. \qquad (4.54)$$

The derivative of the output current I_{out} can be calculated from equation (4.52) as

$$\dot{I}_{out} = 2I_{abv}\left(\frac{V_3 + V_{gain}}{2} - V_T\right) \cdot \frac{\dot{V}_3}{2} = I_{abv}\sqrt{\frac{I_{out}}{I_{abv}}} \cdot \dot{V}_3 \qquad (4.55)$$

The equation (4.55) can be used to calculate the derivative of V_2 as below since the sum of V_2 and V_3 yields a constant current I_τ in equation (4.51).

$$\dot{V}_2 = -\dot{V}_3 = -\frac{\dot{I}_{out}}{\sqrt{I_{abv} I_{out}}} \tag{4.56}$$

We apply Kirchoff's Current Law (KCL) at the capacitive node and obtain

$$C\dot{V}_2 + I_2 = I_\tau \tag{4.57}$$

Now we substitute the expression of $\dot{V}_2$ in equation (4.56) and I_2 in equation (4.54) to equation (4.57).

$$-C\frac{\dot{I}_{out}}{\sqrt{I_{abv} I_{out}}} + I_{abv}\left(\frac{V_{gain} - V_{g\_ref}}{2} + \sqrt{\frac{I_{in}}{I_{abv}}} + \sqrt{\frac{I_\tau}{I_{abv}}} - \sqrt{\frac{I_{out}}{I_{abv}}}\right)^2 = I_\tau \tag{4.58}$$

The first order differential equation of the output current $\dot{I}_{out}$ is formulated in a very complex form. In order to simplify the formula, a new variable related to the output current I_{out} is defined as

$$z = \sqrt{\frac{I_{out}}{I_{abv}}} \tag{4.59}$$

And the derivative of the new variable is

$$\dot{z} = \frac{\dot{I}_{out}}{2\sqrt{I_{abv} I_{out}}} \tag{4.60}$$

By substituting equations (4.59) and (4.60), the differential equation (4.58) can be simplified as

$$\dot{z} = \frac{I_{abv}}{2C}\left(\frac{V_{gain} - V_{g\_ref}}{2} + \sqrt{\frac{I_{in}}{I_{abv}}} + \sqrt{\frac{I_\tau}{I_{abv}}} - z\right)^2 - \frac{I_\tau}{2C} \tag{4.61}$$

4.2.3 Numerical Analysis of the Circuit Behaviors

In the previous section we obtain three differential equations (4.34) (4.48) and (4.61) using subthreshold, EKV and above threshold models respectively. The differential equation (4.34) derived using subthreshold model is a first order low pass filter. The characteristic of the circuit operating in weak inversion can be studied analytically, while the differential equations (4.48) and (4.61) derived using EKV and above threshold models are both complicated. Although it is still difficult to tell the circuit behavior analytically from the differential equations, it is simplified enough to use mathematical tools to study the characteristic numerically.

Here is a brief description of the analysis process. We set the input current I_{in} as a sinusoid signal at certain frequency ω with time t as

$$I_{in}(t) = I_{const} + 0.5 I_{const} \sin(\omega t) \tag{4.62}$$

We can solve all the three differential equations (4.34) (4.48) and (4.61) using function ode45 from Matlab. The solution $I_{out}(t)$ is a function of time t at a certain frequency ω. Since Matlab solves a differential equation using iterative methods with an initial point and certain resolution, the solution is not necessarily evenly distributed in time t. So we resample the solution data $I_{out}(t)$ and transform the time domain data to frequency domain using fft function of Matlab. The first order response, second and third order harmonic distortions are recorded for each frequency ω of the input current. If we sweep the frequency ω and redo the process several times, an AC sweep frequency response will be generated with second and third order harmonic distortion. We draw some conclusions by comparing the first order frequency response,

the second and third order harmonic distortion results generated using different models in different current ranges.

Before analyzing the circuit behavior numerically using the above method, we need to know the exact current ranges of weak, moderate and strong inversion. We set up three functions in Matlab of the drain currents of a transistor using the three models. The parameters related to process are taken from the MOSIS website. The thermal voltage is set as 26mV at room temperature. The width to length ratio is set at 1 for simplicity. The gate to source voltage V_{GS} is varied from 0 to 1V to calculate the drain currents using the three functions. Let's denote the drain current using subthreshold model as I_{sub}, the drain current using EKV model as I_{EKV} and the drain current using above threshold model as I_{above}. The range of weak inversion is defined as I_{EKV} differs I_{sub} less than 10%. The range of strong inversion is defined as I_{EKV} differs I_{above} less than 10%. And the range in between is for moderate inversion. Fig. 4.6 shows the three $V_{gs} \sim \log(I)$ curves using EKV, subthreshold and above threshold models. The diamond point and circle point in the Fig. 4.6 divide the figure to three current ranges. For a unit width to length ratio transistor in AMI05 process, the weak inversion current should be less than 1.58nA at the diamond point in Fig. 4.6 and the strong inversion current should be more than 781.34nA at the circle point in Fig. 4.6. And any currents between the diamond point 1.58nA and the circle point 781.34nA should be considered as moderate inversion.

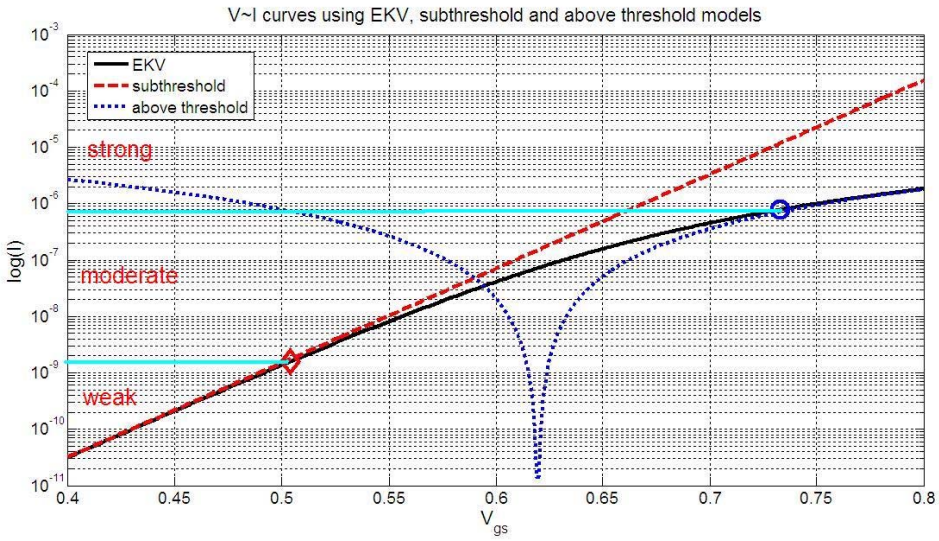


Fig. 4.6 The relationship between the gate to source voltage and the drain current using the three different models.

We vary the DC bias I_{const} of input current I_{in} and the time constant current I_{τ} as 1nA, 10nA, 100nA, 1μA. The amplitude of the input current I_{in} is half of the DC bias for each range as denoted in equation (4.62). The expression $e^{\frac{V_{gain}-V_{g\_ref}}{2\phi_t}}$ is defined as the gain from subthreshold derivation. Some interesting phenomena have been observed from the analysis and will be shown below respectively.

1. If the subthreshold model is implemented in all the current ranges, the second order and third order harmonic distortion are both -70dB of the first order response, with the gain varies at 1, 10 and 100. The reason behind it is that the subthreshold model leads to an ideal linear filter of the system. The harmonic distortions should be zero and independent of gain ideally. The tiny -70dB may be generated by calculation rounding up. Clearly, the ideal results do not show the reality of the circuit when the currents are out of weak inversion range.

2. When the gain equals 1, the second order and third order harmonic distortion are still -70dB, whatever models are used. However, the first order response varies using different models at different current levels. Fig. 4.7 shows the first order response calculated with different models at 1nA, 10nA, 100nA and 1μA current levels. The response using EKV and subthreshold models almost overlap when the current level is 1nA. With the increasing of current levels, the response using EKV model moves towards the response using above threshold model. When the current level reaches 1μA, the response using EKV and above threshold models overlap. Therefore, in reality the cut-off frequency does not increase as much in scale with the increasing of current I_τ as derived using subthreshold model.

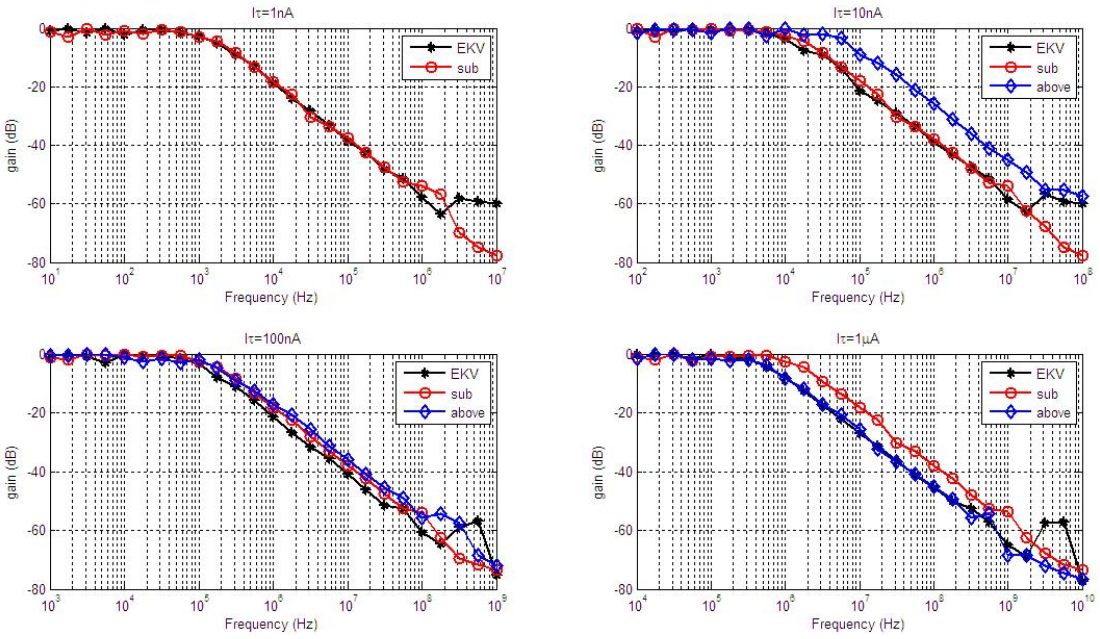


Fig. 4.7: The first order response using different models at 1nA, 10nA, 100nA and 1μA current levels.

3. When the gain $e^{\frac{V_{gain}-V_{g\_ref}}{2\phi_t}}$ increases as 1, 10, 100, the actual low pass gain of the first order response does not increase as much in scale shown in Fig. 4.8. That is

because the currents are larger and enter moderate or even strong inversion region. The exponential current law is gradually replaced by square current law. The difference $V_{gain} - V_{ref}$ will not generate gain as effectively as on the exponential power. All the data in Fig. 4.8 are evaluated using EKV models.

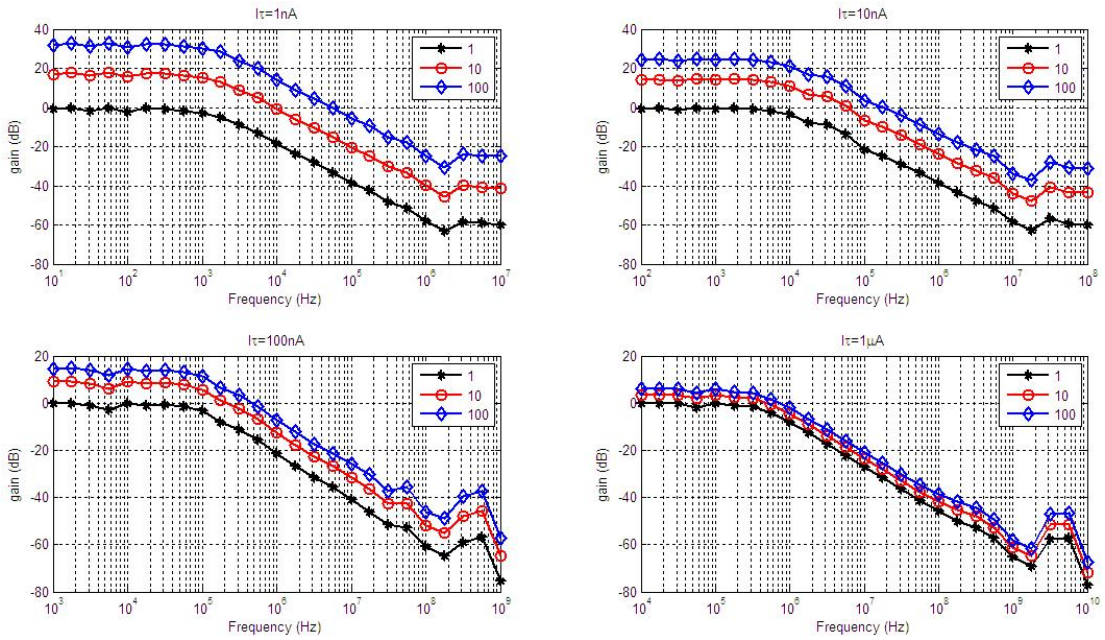


Fig. 4.8: The first order response of $e^{\frac{V_{gain}-V_{g\_ref}}{2\phi_t}}$ varies from 1, 10 to 100 at 1nA, 10nA, 100nA and 1μA current levels using EKV models.

4. When the gain $e^{\frac{V_{gain}-V_{g\_ref}}{2\phi_t}}$ is 10 and 100, the second and third order harmonic distortions at the pass band are shown in Fig. 4.9 evaluated using the EKV model. Both harmonic distortions are higher when the gain is higher. The harmonic distortions increase when the current level increases from weak inversion, and then decrease when the current is heading to strong inversion. The harmonic distortions are highest in moderate inversion. The distortion reduction from moderate to strong inversion may be explained by the decreasing of the actual gain of the first order response.

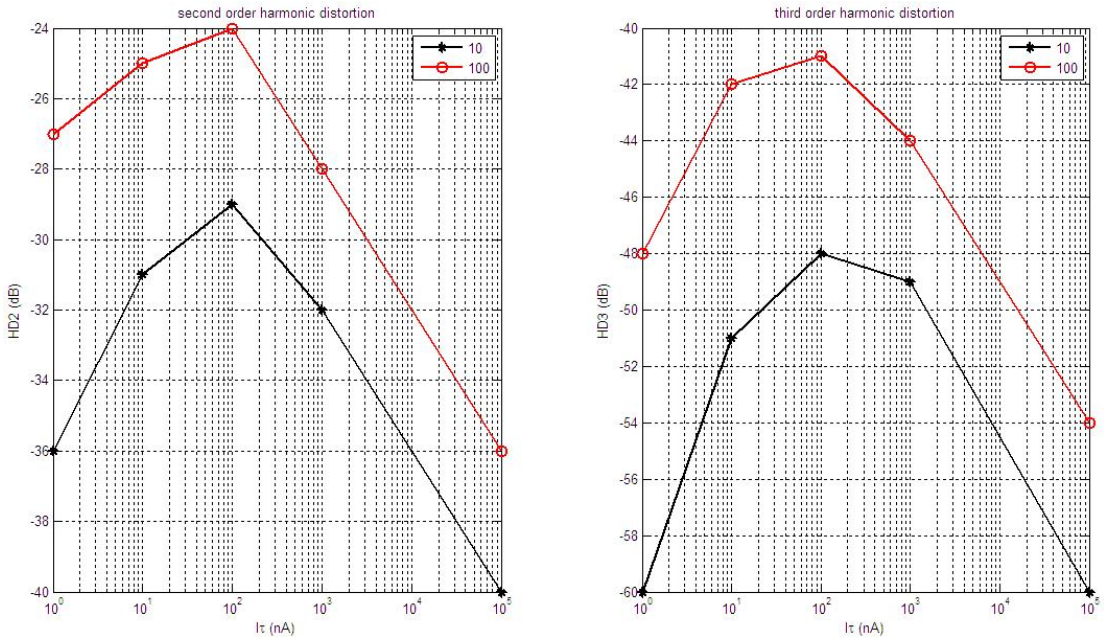


Fig. 4.9: The second and third order harmonic distortions at the pass band when the gain is 10 and 100 using the EKV model.

4.3 Summary

We have described adaptive first order low pass filters implemented using a log domain architecture with floating gate transistors operating in subthreshold, along with MITE circuits which integrate the learning rules for system identification. We chose to implement adaptive filters using a log domain topology because log domain filters are compact current mode IIR filters that operate with low power, have wide tuning range, large dynamic range, and capability for high frequency operation. Further, we've developed robust learning rules based on Lyapunov stability. These learning rules are implemented using MITE structures, highlighting the elegance and symbiotic nature of the design methodology.

We have presented experimental results that demonstrate the success of our adaptive system design using this model-based learning method. We have also

presented test results and analysis of the effects of current mirror mismatch on the parameter estimation. The mismatch analysis accounts for the observed discrepancies between the experimental results of the reference and the model filters. The circuit behavior and harmonic distortions in moderate inversion have been evaluated using EKV model with mathematical tools.

PART II

A LOW POWER TEMPERATURE INSENSITIVE OSCILLATOR APPLIED IN SMART DUST RADIO

Chapter 5: Introduction and Previous Work

5.1 Background and Goal

5.1.1 Smart Dust Review

Smart dust is a wireless communication network of tiny micro-electro-mechanical systems (MEMS) sensors which can detect anything from light and temperature, to vibrations, etc. The sensors are intended to be the size of a grain of sand, or even a dust particle. When clustered together, they would automatically create highly flexible, ultra low power networks with applications ranging from climate control systems to military detections of enemy movements, poisonous gas or radioactivity.

The low power wireless communication network is implemented by modern radio frequency integrated circuits. In spite of the good performance of signal transmitting and receiving, these devices are required to have low cost, small size, and long battery life. The smart dust research project focuses on low power RF transceiver system design.

Transceiver systems can be categorized by the modulation scheme. Amplitude-shift-keying (ASK), on-off-keying (OOK) and frequency-shift-keying (FSK) are three popular modulation schemes at present. The OOK modulation is a special case of ASK modulation where no carrier is present during transmission of a zero. It is widely used

for its simplicity and low implementation costs. It has the advantage of allowing the transmitter to idle during the transmission of a "zero", therefore conserving power.

The OOK transceiver system is made of a transmitter block and a receiver block. Both blocks consist of a RF part and a baseband part. The baseband part does not require high frequency operation and can be implemented in standard CMOS technology. In the transmitter block shown in Fig. 5.1, the baseband part compresses, encodes and modulates the signals to be transmitted and passes them to the RF part for transmitting. The RF part multiplies signals by a high frequency carrier, amplifies the mixed signals and sends them out through the antenna. In the receiver block shown in Fig. 5.2, the RF part receives the signals from the antenna, suppresses the noise, amplifies the signals and translates the signals to the baseband frequency. The baseband part then demodulates, decodes and decompresses the signals.

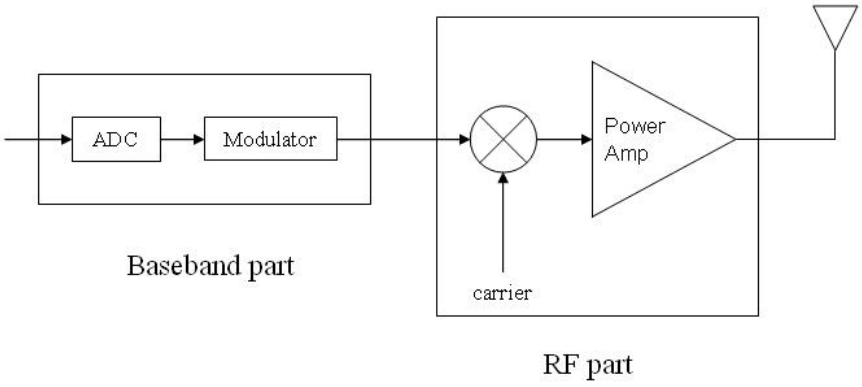


Fig. 5.1: Transmitter Block.

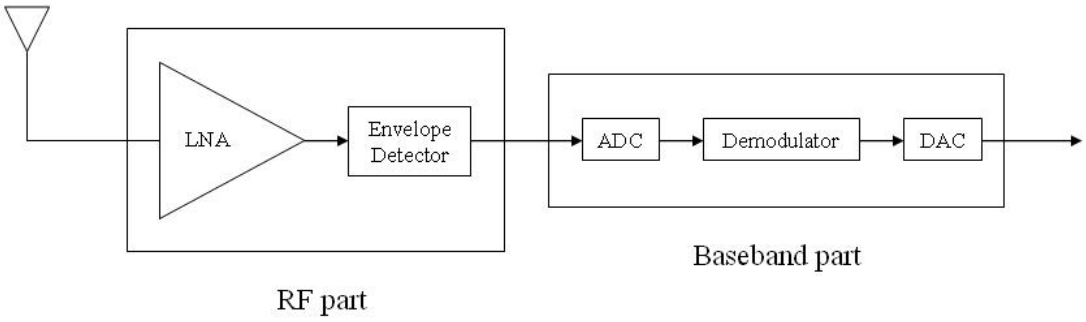


Fig. 5.2: Receiver Block.

Generally speaking, the FSK modulation is believed to have better performance in the presence of interfering signals. However, it is more difficult and expensive to implement. Accurate frequency control is required so a phase locked loop (PLL) is typically used.

A phase locked loop (PLL) is a negative feedback control system which that generates a signal that has a fixed relationship to the phase of a reference signal. A PLL circuit responds to both the frequency and the phase of the input signals, automatically raising or lowering the frequency of a controlled oscillator until it is matched to the reference in both frequency and phase. PLLs have wide applications in radio, telecommunication and computers. They may generate stable frequencies, recover a signal from a noisy communication channel, or distribute clock timing pulses in digital logic designs such as microprocessors.

5.1.2 Research Goals

There are two main research goals in this part of work. One is focused on designing oscillators for ultra low power OOK transmitter systems in 2.2GHz

frequency band. The other aims at designing PLLs for FSK receiver systems, in collaboration with Bo Li, for both 2.2GHz and 20GHz frequency bands.

5.1.2.1 Temperature insensitive oscillators for OOK transmitter systems

This goal aims at designing carrier frequency generation circuits for ultra low power OOK transceiver system. The circuit is a voltage controlled oscillator with frequency tunability around 2.2GHz. The stability of the output frequency is required despite of the change of environments such as temperature, humidity, etc.

Crystal oscillators are famous for their frequency stability therefore they are widely used in applications which require constant frequency output such as watches, clocks, radios, computers and cell phones. A crystal oscillator uses the mechanical resonance of a vibrating crystal of piezoelectric material to create an electrical signal with a very precise frequency. The most common type of piezoelectric resonator used is the quartz crystal, so oscillator circuits designed around them were called crystal oscillators. Quartz crystals are manufactured for frequencies from a few tens of kilohertz to tens of megahertz. The resonant frequency depends on size, shape, elasticity, and the speed of sound in the material. Despite their high frequency stability, quartz crystal oscillators suffer from their limited frequency range and tunability. For a VCO around 2.2GHz, it is not a good choice whether in frequency range or tunability.

Currently, the commonly used LC tank oscillators consume power in milli-watts and large chip area due to the planar layout of the inductor in integrated circuit. Andreani et al. [29] presented a LC quadrature voltage controlled oscillator (VCO) of

a current consumption of 25mA from a 2V power supply and a die area of about 0.8mm^2. Tiebout [30] proposed a low phase noise differentially tuned quadrature VCO with a total power dissipation of 20mW at 2.5V power supply voltage and a die area about 1.1mm^2. Zanchi et al. [31] demonstrated a 2V 2.5GHz VCO with wide band low noise automatic amplitude control (AAC) loop with a current dissipation of 7mA. Tsang and EL-Gamal [32] designed an area-efficient LC-based 12GHz VCO consuming 7.7mW with a die area 0.24mm^2. Hajimiri and Lee [33] demonstrated a 1.8GHz LC oscillator dissipating 6mW using on chip spiral inductors. Margarit et al. [34] presented an 800MHz low noise low power VCO with AAC consuming 1.6mA from a 2.7V power supply.

Another less power hungry and smaller substitute is a CMOS ring oscillator. Betancourt-Zamora et al. [35] designed a 1GHz injection-locked ring oscillator that consumes 350μW of power and occupies 0.012mm^2 of die area. Bautista and Aranda [36] described a low power and high speed CMOS VCO consuming 7.01mW with a die area of 5231μm^2. Severino de Paula et al. [37] demonstrated a high swing low power CMOS differential VCO with a chip area of 2520μm^2 and a power consumption of 11.38mW. Yan and Luong [38] presented a 900-MHz CMOS low-phase-noise VCO that dissipates 15.4mV of power with a die area about 0.013 mm^2. Badillo and Kiaei [39] proposed a low phase noise 2.0V 900MHz CMOS VCO dissipating 18.95mW and taking 6750μm^2 of chip area. Park and Kim [40] described a low-noise 900MHz VCO consuming 10mA from a 3V power supply with a die area of 0.01mm^2. Some of the previous designs of ring oscillators may consume power in milli-watts for

using different amplifier structures, but the chip area is still greatly saved compared with LC tank oscillators.

Despite of the advantages of smaller size and less power consumption, CMOS ring oscillator oscillate at different frequencies in different environments due to the temperature dependence of CMOS transistors. Fig. 5.3 shows the simulation result of a three stage current-starved ring oscillator at different temperatures from 0°C to 50°C. The instability of the oscillating frequency of a CMOS ring oscillator makes it less applicable in precise channel-selected wireless communication.

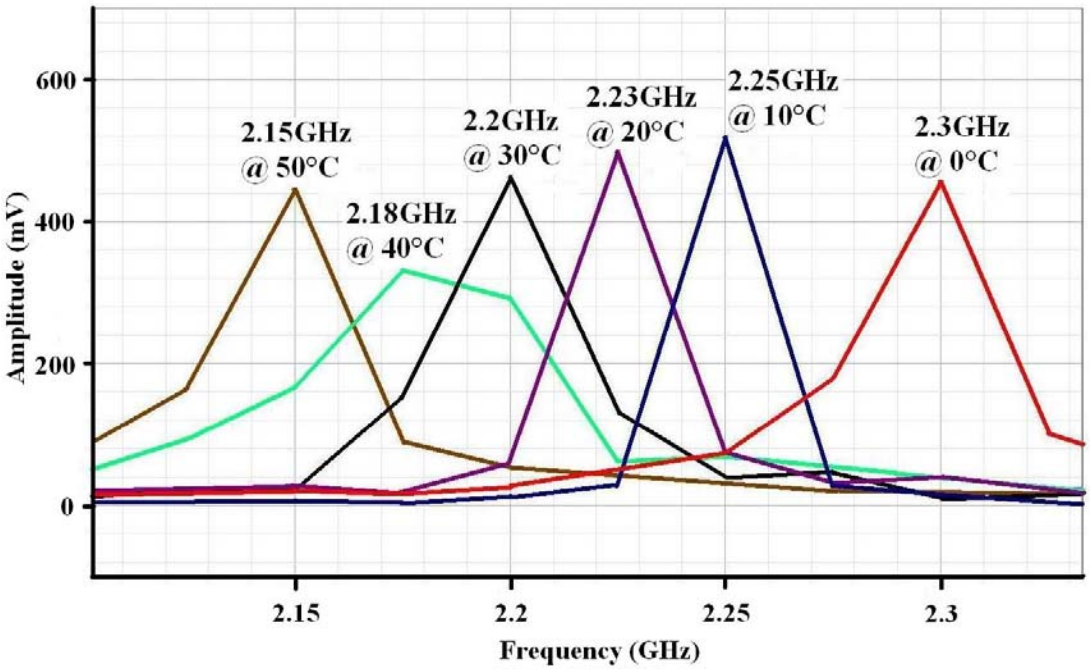


Fig. 5.3: The simulation result of a currents-starved ring oscillator at temperatures 0°C, 10°C, 20°C, 30°C, 40°C and 50°C.

We propose a temperature insensitive ring oscillator implemented in CMOS technology. The power consumption is much smaller compared to LC tank oscillators and the chip area is greatly reduced. The instability of the output frequency is

compensated by a temperature adaptive block also implemented in CMOS technology. Simulation results show the circuit oscillates at the target frequency 2.2GHz between 0°C and 50°C. Experimental results show that the frequency stability in the range from 5°C to 65°C has been improved 10 times with compensation and at least 1 order smaller power is consumed than current published temperature compensated voltage controlled oscillators.

A 2.2GHz OOK transmitter in use of this voltage-controlled oscillator (VCO) is presented and the wireless network of this transmitter and another custom designed receiver shows successful signal transmitting and receiving up to 2.8Mbps in one meter.

5.1.2.2 Phase-locked loops for FSK receiver systems

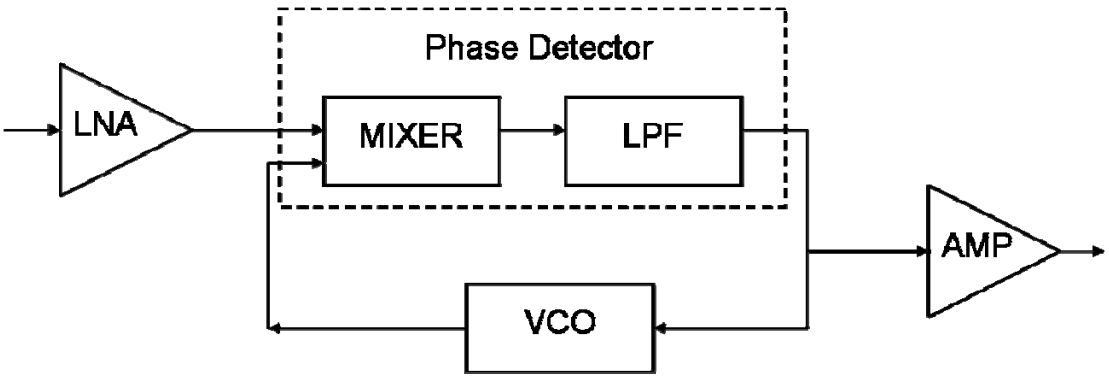


Fig. 5.4: Structure of a FSK receiver using phase-locked loop.

This goal is focused on designing low power phase-locked loops (PLL) and their application as frequency demodulators in FSK receiver systems. Fig. 5.4 shows the block diagram of a FSK receiver. The input signal is amplified by the low noise amplifier (LNA) and serves as the reference signal of the PLL. The PLL tracks the frequency information of the reference input and the amplifier outputs the

demodulated signal at a specific power. The circuit is implemented with as low a power structure as possible to minimize the power dissipation. This work was performed in collaboration with Bo Li.

Many groups have been making efforts on developing radio frequency phase locked loops used for low power wireless communication systems. Yan and Luong [41] illustrated a 900MHz monolithic CMOS dual-loop frequency synthesizer for GSM receivers with power dissipation of 34mW using 0.5µm CMOS technology. Park and Ray [42] designed a 1.6GHz CMOS PLL consuming 90mW in a 0.6µm CMOS process. Park et al. [43] presented a 1.8GHz self-calibrated PLL with power consumption of 60mA using 0.35µm CMOS technology. Shu et al. [44] developed a 2.4GHz ring-oscillator-based CMOS frequency synthesizer with dual-PLL architecture dissipating 49.5mW in a 0.35µm CMOS process. Da Dalt et al. [45] demonstrated a compact triple-band low-jitter LC PLL dissipating 19.5mW with a programmable coil using 0.13µm CMOS technology. Hung and Kenneth [46] illustrated a fully integrated 1.5V 23mW 5.5-GHz CMOS Phase-Locked Loop in a 0.25µm digital CMOS process. Boerstler et al. [47] designed a 10.4GHz wide-band PLL with power consumption of 40mW in 90nm partially depleted silicon-on-insulator CMOS technology. Tiebout et al. [48] presented a 13GHz PLL with 60mW power consumption in a 0.13µm CMOS process. Ding and Kenneth [49] developed a 20GHz PLL in 0.13µm CMOS technology dissipating 22.5mW from a 1.5V power supply. Ng et al. [50] demonstrated a 1-V 24GHz 17.5mW PLL in a 0.18µm CMOS process. Most of the previous work has power dissipation in tens of milli-watts.

We propose a 2.2GHz PLL using a current-starved ring oscillator in a FM receiver, and a 20GHz PLL for use with a LC oscillator for BFSK receiver application. The 2.2GHz design has micro watts power consumption and the 20GHz design dissipates only 1.77mW. The power consumption of both designs is at least 1 order smaller than previous published PLLs. The simulation and experimental results demonstrate the success of frequency demodulation around each frequency range. A PLL model analysis is presented numerically using Matlab tools near the end of this work.

5.2 Previous Work: A Low Power CMOS Temperature Sensor for On-chip Temperature Gradient Detection

5.2.1 Introduction

Decreasing feature sizes and increasing package density cause self-heating of chips to become an important factor. Self-heating induces temperature non-uniformity on-chip, which may threaten reliability and functionality of the circuits. Significant attention in recent years has been paid to thermal models [51][52][53] and to incorporating non-uniform thermal effects into computer-aided-design (CAD) tools [54][55]. Such models are rarely verified using experimental data obtained from fabricated chips. While on-chip measurements of local temperature present an obvious opportunity to verify such models and CAD tools, they also present a subtler opportunity to incorporate feedback from sensory data into techniques for temperature management and performance optimization. In order to address this opportunity, it is first necessary to develop techniques for monitoring temperature on-chip.

Requirements for sensors in such applications include not only high accuracy, but also compact layout area and very small power consumption so as not to generate extra heat and change the primary temperature gradients. We report a tiny 1.5V low power CMOS temperature sensor and demonstrate its application for on-chip temperature gradient detection.

Many groups have explored a variety of designs for CMOS temperature sensors. Szajda et al. [56] reported a low noise, high resolution silicon temperature sensor for use in an invasive tissue property measurement probe. Bakker and Huijsing [57] developed a micro-power CMOS temperature sensor with digital output realized by a sigma-delta converter robust from digital interference. Tuthill [58] presented a switched-current, switched-capacitor temperature sensor as part of multi-channel data acquisition system. Chen et al. [59] designed a time-to-digital-converter-based CMOS smart temperature sensor for high-accuracy portable applications. Luh et al. [60] reported a high-speed CMOS on-chip temperature sensor for the purpose of quickly detecting circuit overheating. Most designs are based on traditional proportional-to-absolute-temperature (PTAT) principles and utilize bipolar transistors or lateral bipolars.

Few groups reported on-chip temperature gradient detection. Shih et al. [61] describe a sensitive, wide-range MOS temperature sensor for on-chip temperature detection. The sensor requires large layout area and special fabrication techniques to grow ultra thin oxide. In this part, we present a CMOS temperature sensor based on the temperature dependent characteristics of the threshold voltage of MOS transistors and mobility of carriers. The tiny nano-power design is suitable for detection of

temperature gradients on small chips and compatible with any commercially available CMOS technology.

5.2.2 Temperature Sensor Design

5.2.2.1 Circuit design

The transfer function of a MOS transistor working above threshold in the saturation region is described by the equation

$$I_D = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{GS} - V_T)^2 \qquad (5.1)$$

As the temperature increases, both the carrier mobility μ and the threshold voltage V_T decrease. The mobility tends to decrease the current, whereas the threshold voltage tends to increase the current. The consequence of these two temperature dependent parameters is a zero temperature coefficient bias point in the transconductance characteristics of MOS transistors as shown in Fig. 5.5 for a 3.6µm/3.6µm (W/L) diode-connected NMOS transistor simulated with HSPICE using BSIM3v3 model for a commercially available 0.5µm CMOS technology.

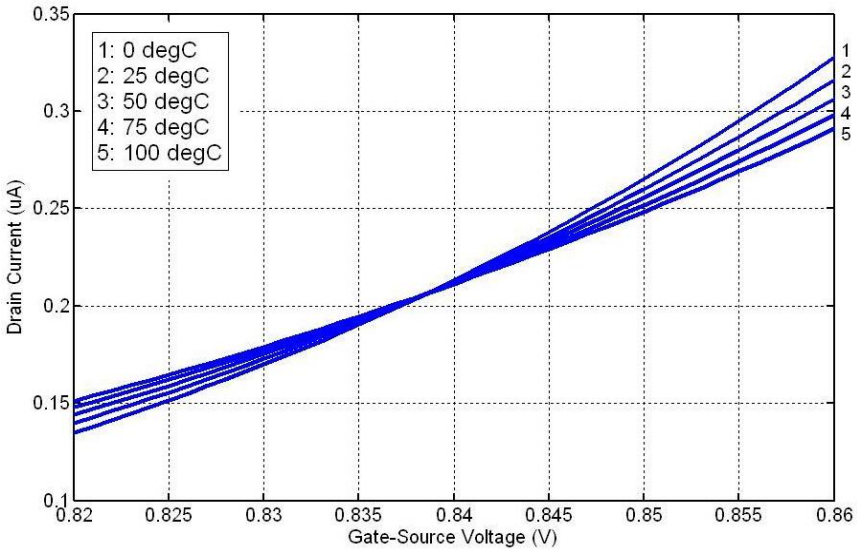


Fig. 5.5: Simulated transconductance characteristics of a 1.8µm/3.6µm diode-connected NMOS transistor.

Filanovsky and Lim [62] derived the temperature dependence of gate voltage for a saturated NMOS transistor with the mobility temperature coefficient $\alpha_\mu = -2$

$$V_{GS} = V_{GSF} + \alpha_{VT} T\left(1 - \sqrt{I_D / I_{DSF}}\right) \tag{5.2}$$

where (V_{GSF}, I_{DSF}) is the common intercept point for transfer functions of the transistor at different measured temperatures. α_{VT} is the threshold voltage temperature coefficient. If we can achieve a constant temperature-invariant drain current I_D, we obtain a linear relationship between the gate to source voltage and the temperature. Although the zero temperature coefficient bias point is not well defined for PMOS transistors, as discussed by Filanovsky and Lim [62], simulations show that in practice it is good enough for this application. Considering the low-power and small-area requirements for our temperature sensor design, we use a PMOS transistor to generate the temperature-invariant current source. The schematic of the temperature sensor is shown in Fig. 5.6.

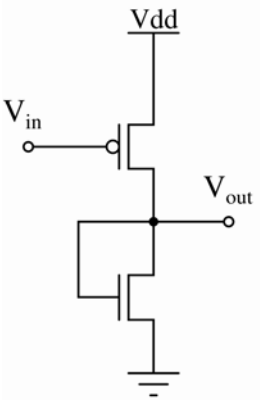


Fig. 5.6: Schematics of the temperature sensor.

Although Equation (5.2) was derived for MOS transistors operating in strong inversion, it is also possible to observe similar behavior for transistors operating in moderate inversion. In some applications, operation in moderate inversion is preferable in order to reduce power consumption and minimize the likelihood of self-heating. Simulation results show that the linearity of the temperature sensor is improved for operation in moderate inversion. The linearity of the temperature sensor strongly depends on the temperature-invariance of the PMOS current. The variance of the "constant" PMOS current is larger when the transistor is biased in strong inversion, which results in better linearity in moderate inversion. The RMS error is 1.13e-4V at a bias current of 59.7nA in moderate inversion, whereas the RMS is 1.23e-4V at a bias current of 1.54μA in strong inversion.

Two implementations of the circuit have been fabricated and tested: one version using 4/2 minimum size transistors for both NMOS and PMOS, with input voltage connected to ground; and a second version using 6/12 PMOS transistor and 12/12 NMOS transistor with input voltage 0.3V. The second version achieves higher accuracy, probably because of larger transistor sizes and reduced short channel effects.

5.2.2.2 Experimental results

The temperature sensor was tested in a chamber formed using two pieces of aluminum acting as thermal masses as shown in Fig. 5.7. A chip size groove was machined inside the thicker piece and sprayed for electrical insulation. A small temperature controller (Analog Devices Inc.), was placed in the chamber alongside a temperature sensor chip with open lid. The thinner piece of aluminum is connected to electrical ground, and a hole has been machined in it to hold the sensor for the hot plate. The thicker piece of aluminum with the chip inside is placed face down on the thinner piece in order to stabilize the temperature during testing. Insulation spray is used to protect the chip only at places that the pins or the die may contact the aluminum. Wires are used to connect the sensor chip to off-chip buffers and data acquisition cards. A hot plate is used for heating the aluminum chamber.

Fig. 5.7: Experimental setup for the temperature sensor.

The temperature chamber is heated to 100 ºC, then the hot plate is switched off and measurements are acquired once every 20 seconds for 1000 minutes as the sample cools. 892 out of 3000 data points are used for sensor calibration so that data are distributed evenly over the temperature range. Fig. 5.8 (upper panel) shows experimental results from the second version of the temperature sensor along with a least-square linear fit to the data, where the temperature T is in degrees Celsius and the output voltage V is in volts. Fig. 5.8 (lower panel) shows the deviation between the measured data and the linear fit. The maximum error is 0.2531ºC. The standard deviation is 0.0965ºC over the range from 24.9272ºC to 97.0242ºC. The performance of this temperature has been compared with previous designs in Table 5.1.

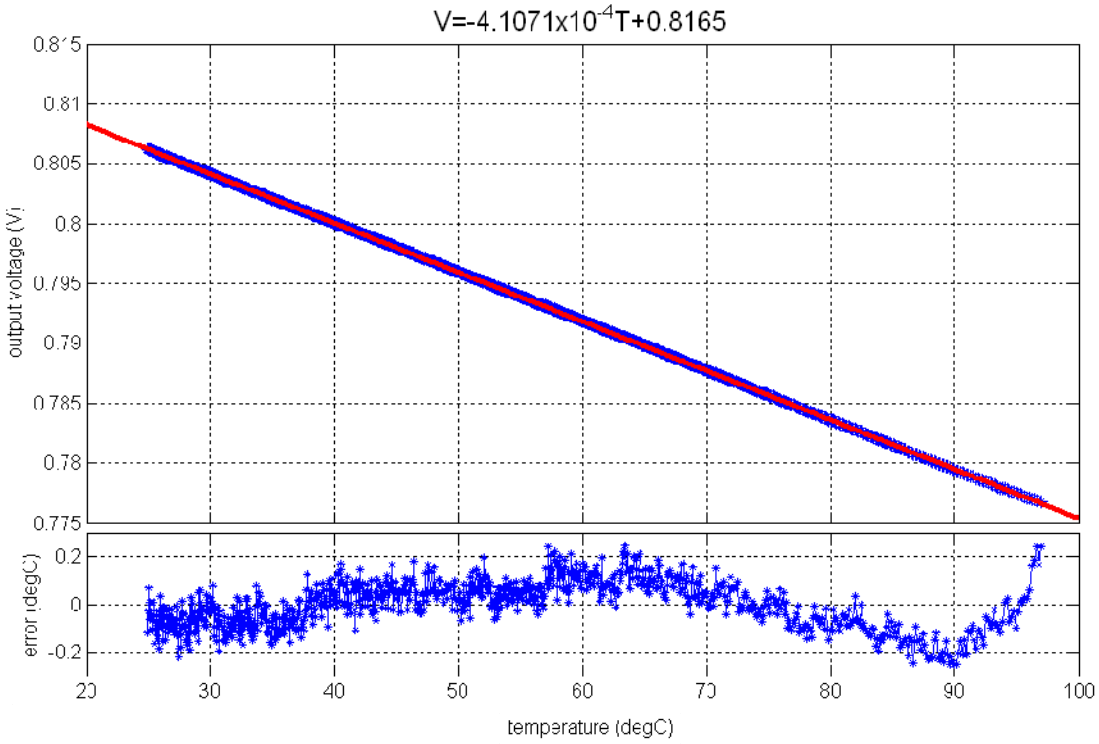


Fig. 5.8 Experimental results of a single temperature sensor.

Sensor	Error (°C)	Power	Voltage	Area	Range (°C)	Process
[57]	±1	7μW	3V	1.5 mm^2	-40~120	2μm
[58]	±1	1μW	3V	3.32 mm^2	-55~125	0.6μm
[59]	-0.7~+0.9	10μW	3.3V	0.175 mm^2	0~100	0.36μm
[60]	±2.7	0.35mW	3.3V	0.034mm^2	0~150	0.6μm
this work	±0.25	60nW	1.5V	64.8μm^2	25~97	0.5μm

Table 5.1: Performance comparison between this work and previous temperature designs.

5.2.3 On-Chip Temperature Gradient Detection

A custom chip with heat generation devices and an array of temperature sensors was designed, fabricated and tested. Fig. 5.9 shows the chip photo. It occupies 1.5mm by 1.5mm in 0.5μm CMOS technology. There are three 500Ω resistors, nine voltage-controlled oscillators and nine temperature sensors in an array on the chip. The resistors and the temperature sensors are labeled in Fig. 5.9.

The voltage-controlled oscillators did not generate enough heat to detect a sustained temperature difference. The die package is a good heat conductor and the temperature gradients dissipate very quickly. Heating resistors at different locations did generate sustained temperature gradients across the chip, which was detected by the array of sensors.

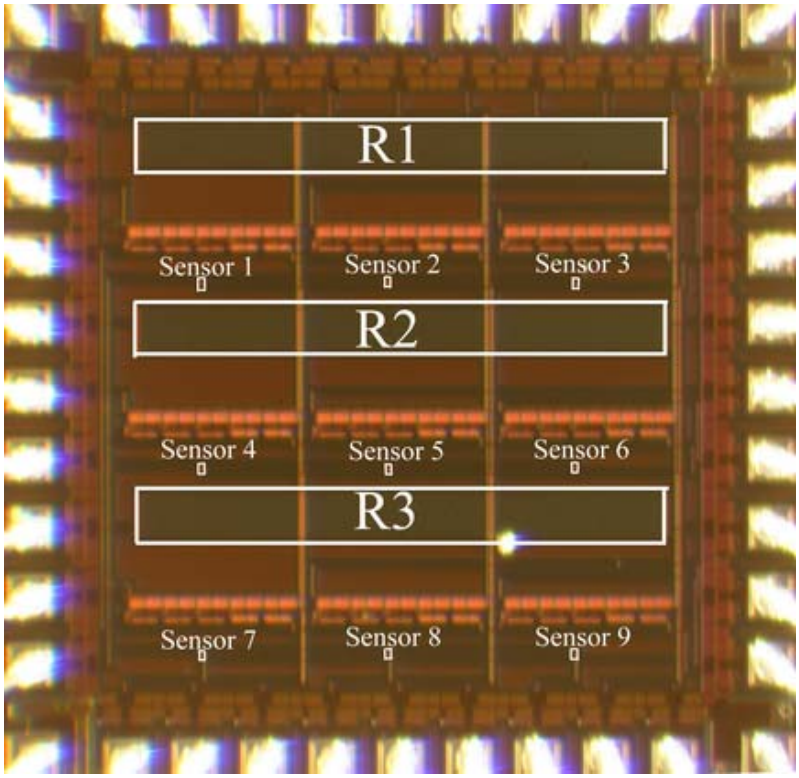


Fig. 5.9: The photo of temperature gradient detection chip.

The experimental procedure for establishing and detecting temperature gradients is as follows. The chip is first placed into the aluminum chamber and all nine temperature sensors are calibrated. A PC-controlled data acquisition card records measurements. After calibration the chip is removed from the chamber, the heat generation devices are powered, and the outputs of the temperature sensors are observed. We conducted four experiments corresponding to different thermal conditions, and the results are described in detail below. The mismatch between different temperature sensors is canceled in calibration.

Case 1: R3 only.

We first apply 10V bias across the resistor R3 and leave resistors R1 and R2 off. Fig. 5.10 shows the on-chip temperature measurements every 6 minutes during the 30-

minute experiment. After 30 minutes, the nearest three sensors 4, 5 and 6 are heated to more than 29ºC. Sensors 7, 8 and 9 are heated to around 28.8 ºC. The farthest three sensors 1, 2 and 3 are heated to around 28.4 ºC.

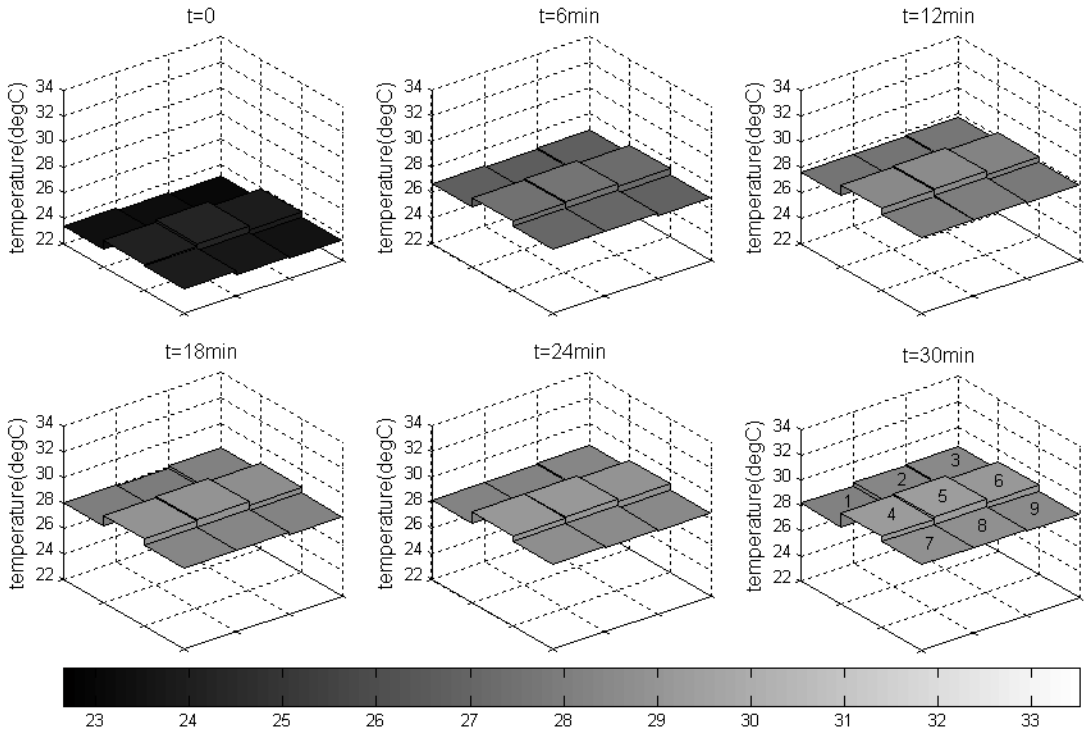


Fig. 5.10: On-chip temperature while heating R3 for 30 minutes.

Case 2: R2 only.

Next a 10V bias is applied across resistor R2 and 0V is applied to resistors R1 and R3. The on-chip temperature measurements every 6 minutes over a period of 30 minutes are shown in Fig. 5.11. The data confirm expected trends: This time the nearest three sensors are sensors 1, 2 and 3, which show the highest temperature of around 29ºC. The farthest three sensors are sensors 7, 8 and 9, which show the lowest temperature of below 28ºC. The remaining three sensors 4, 5 and 6 show an intermediate temperature around 28.5ºC.

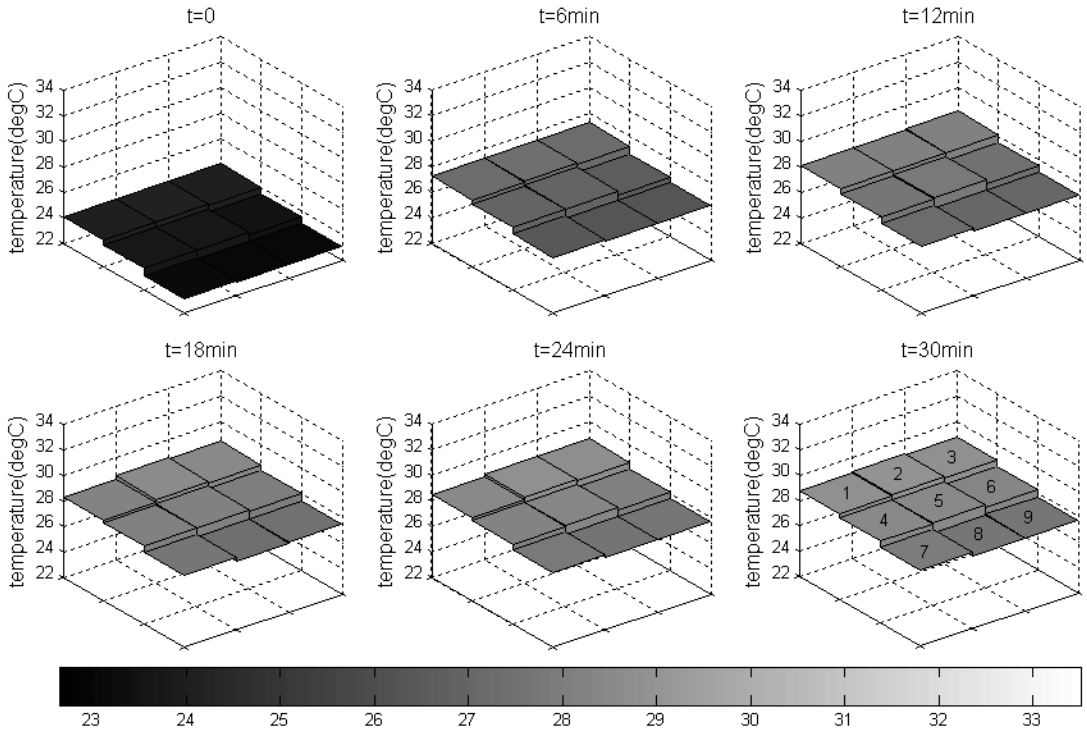


Fig. 5.11: On-chip temperature while heating R2 for 30 minutes.

Case 3: R1 only.

Next we apply a 10V bias across resistor R1 with R2 and R3 off. As for the previous two experiments, we monitor temperature for 30 minutes and record data shown in Fig. 5.12. Highest temperatures are found in sensor group (1, 2 and 3) and lowest temperatures in group (7, 8 and 9), as expected.

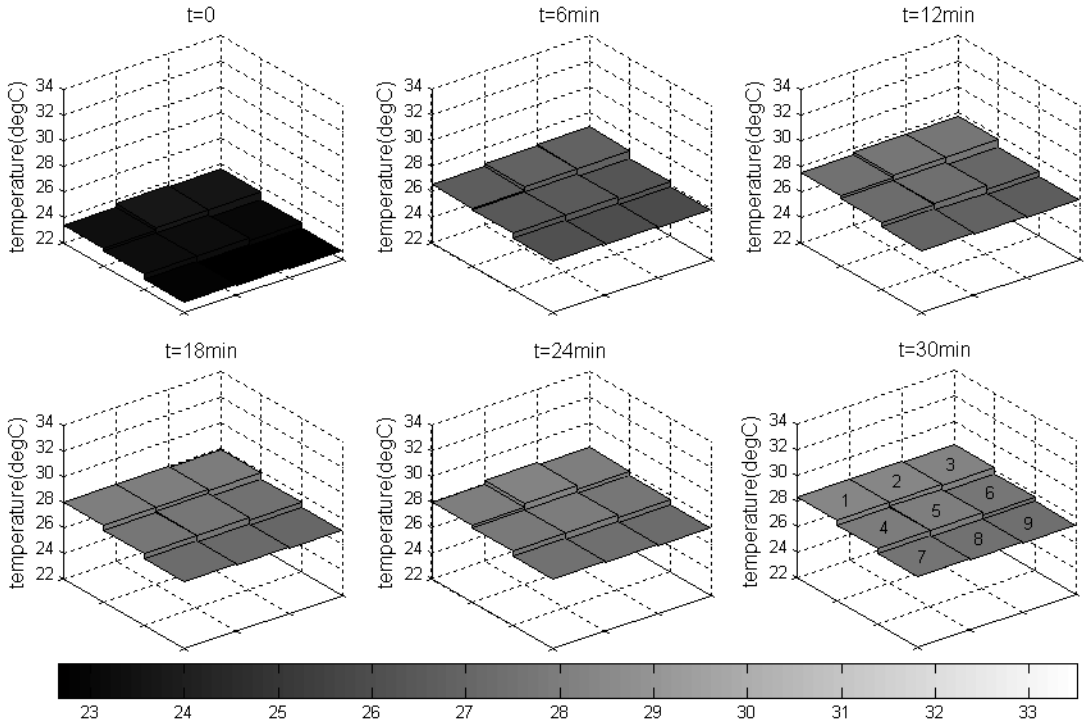


Fig. 5.12: On-chip temperature while heating R1 for 30 minutes..

Case 4: R2 and R3.

Finally we apply 10V biases across two resistors, R2 and R3. We expect the on-chip temperature to be higher after 30 minutes, since the temperature in this case results from the superposition of heated resistors R2 and R3. The regions between resistors R2 and R3 where sensors 4, 5 and 6 are located should be the hot spots. Sensors 1, 2 and 3 are closer to the heat source than sensors 7, 8 and 9, so the temperature of sensors 1, 2 and 3 should be higher than that of sensors 7, 8 and 9. These trends are confirmed in the data shown in Fig. 5.13.

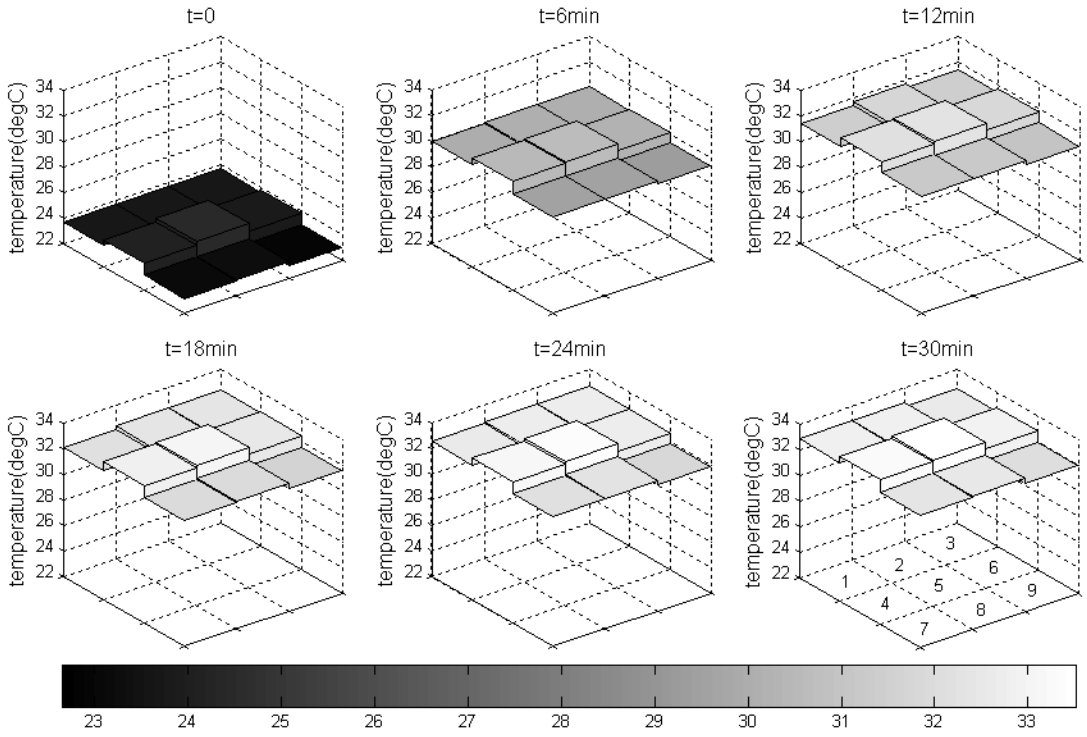


Fig. 5.13: On-chip temperature while heating both R2 and R3 for 30 minutes.

5.2.4 Summary

We have described a tiny low power 1.5V temperature sensor applied to detection of on-chip temperature gradients. The temperature sensor exploits the temperature dependence of carrier mobility and threshold voltage of MOS transistors. The tiny scale and the nano-power consumption result from the simplicity of the design.

We have presented experimental results which demonstrate the successful detection of on-chip temperature gradients generated by the dissipating heat of resistors. Such detection of temperature gradients has wide-ranging applications in CAD design, reliability, 3D heterogeneous integration, as well as lab-on-chip and cell-based sensing systems.

Chapter 6: A Low Power Temperature Insensitive Oscillator Using CMOS Transistors

6.1 Circuit Design

6.1.1 Current-starved ring oscillator

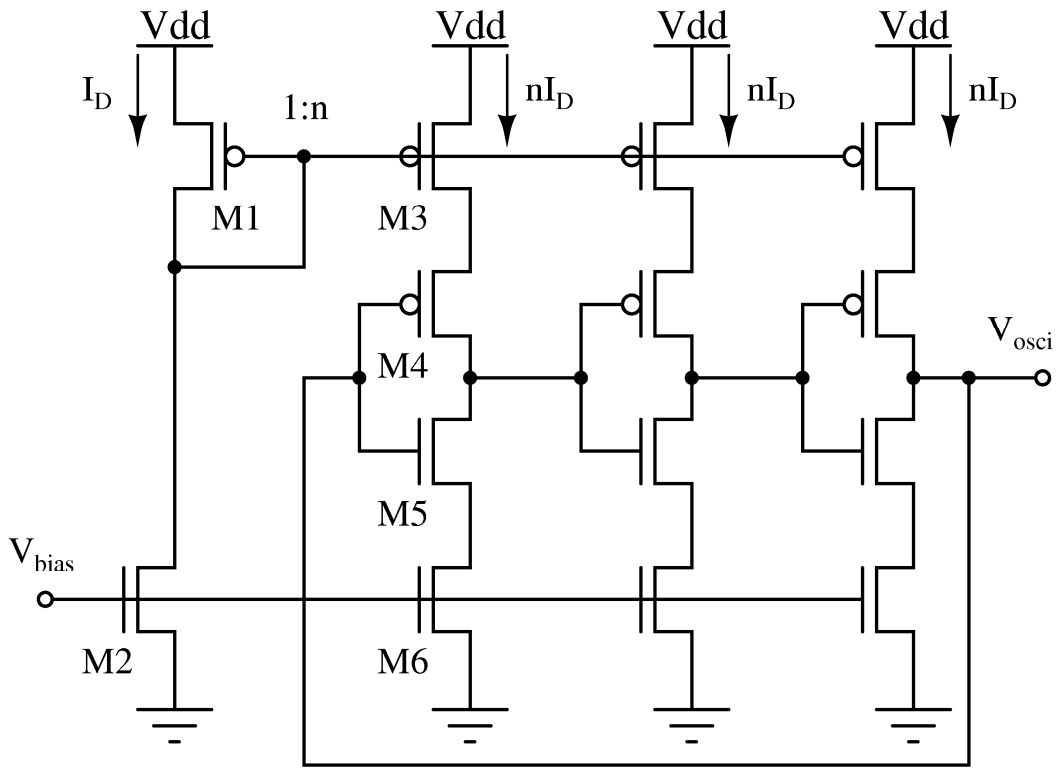


Fig. 6.1: The schematic of the current-starved ring oscillator.

The schematic of the current-starved ring oscillator is shown in Fig. 6.1. It has three inverting stages in a ring to generate oscillation. Transistors M4 and M5 operate

as an inverter, while transistors M3 and M6 operate as current sources, which limit the current available to transistors M4 and M5. The input control voltage V_{bias} set the drain currents I_D of transistors M1 and M2 that controls the oscillating frequency of the VCO. The current I_D is mirrored in scale 1:n in each inverting stage to save power.

The sizes of the inverting stage transistors are well designed to make the switching point at half of the power supply voltage, which makes the noise margins equal. The symmetry of the rising and falling edges improve the phase noise by decreasing the $1/f^3$ corner frequency [63]. The W/Ls of transistors M1 and M2 are much smaller than those of other current source transistors, which limits the power dissipation.

We assume the capacitive load after each inverting stage is C_{tot}, and switching point is V_{sp}. Then the time it takes to charge C_{tot} from zero to V_{sp} with the constant current nI_D is given by

$$t_1 = C_{tot}\frac{V_{SP}}{nI_D} \tag{6.1}$$

While the time it takes to discharge C_{tot} from the power supply voltage V_{dd} to V_{sp} is given by

$$t_2 = C_{tot}\frac{V_{dd} - V_{sp}}{nI_D} \tag{6.2}$$

The oscillating frequency of the current-starved ring oscillator is

$$f_{osc} = \frac{1}{3(t_1 + t_2)} = \frac{nI_D}{3C_{tot}V_{dd}} \tag{6.3}$$

When the power supply voltage V_{dd} and the capacitive load C_{tot} are fixed, the oscillating frequency is proportional to the current flowing in each inverting stage.

The output of the current-starved ring oscillator is normally buffered though an inverter. Attaching a large load capacitance on the output of the oscillators can significantly affect the oscillating frequency or even lower the gain of the oscillator enough to kill the oscillation.

The average power dissipation can be derived by the average current drawn from the power supply V_{dd}. The total average current on the three inverting stages is

$$I_{avg} = 3\frac{C_{tot}V_{dd}}{T_{osc}} = 3C_{tot}V_{dd}f_{osc} \tag{6.4}$$

So the total average power consumed by the current-staved ring oscillator is

$$P_{avg} = V_{dd}\left(I_{avg} + I_D\right) = 3C_{tot}V_{dd}^2 f_{osc}\left(1+\frac{1}{n}\right) \tag{6.5}$$

For design of a target oscillating frequency with a given process with fixed power supply voltage V_{dd}, minimizing the gate capacitance helps to decrease the power consumption. Using smaller size of transistors for M1 and M2 also saves the bias power.

This current-starved ring oscillator circuit has been selected in applications of a designed 2.2GHz OOK transmitter and a 2.2GHz FM receiver for low power consumption and compact size. However, the oscillation frequency has an upper limit related to the fabrication process.

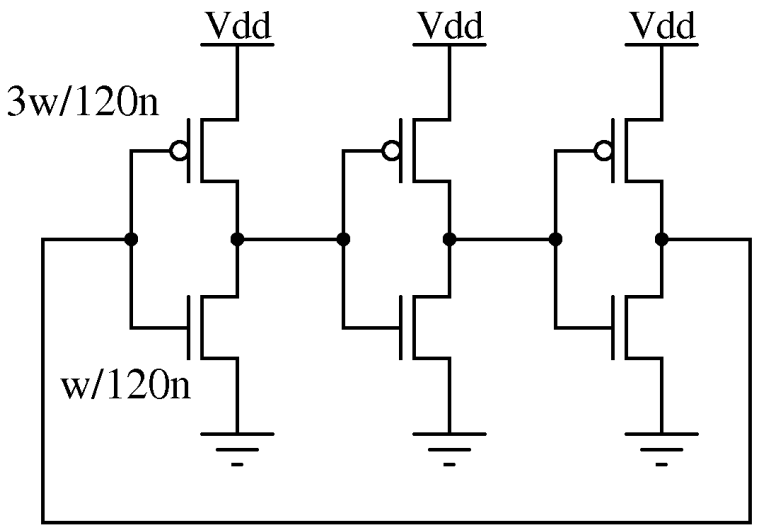


Fig. 6.2: A simple 3-stage inverter-based ring oscillator in 0.13μm IBM 8RF LM process.

In order to study the frequency limit of the circuit, we start from the simple k-stage inverter-based ring oscillator. Suppose each inverter generates a delay time t, the frequency of the oscillator is 1/(2kt). To increase the frequency, minimum delay and fewer stages are preferred. k=3 is the minimum stage number for oscillation. Fig. 6.2 shows a simple 3-stage inverter based ring oscillator. The length of both PMOS and NMOS transistors are set at 120nm, the minimum of channel length. The width of PMOS transistor is set at 3 times of the width of NMOS transistor w for the symmetry of the rising and falling edge of the signal. The intrinsic switching speed of a MOSFET is determined by the intrinsic process characteristic time constant. The estimation using the above threshold transfer function gives resistance inversely proportional to the transistor width and capacitance proportional to the transistor width, which generates a constant intrinsic speed of a certain process. However, the real implementation of the short channel MOSFET is much more complicated than the simple square law transfer function. The simulated oscillation frequency of the 3-stage

oscillator is plotted with NMOS transistor width w in Fig. 6.3. The frequency increases first with the transistor width w increasing because more current is available for charge and discharge to minimize the delay, and decreases after the transistor width w is increasing to a certain degree because the increasing gate capacitance starts to dominate.

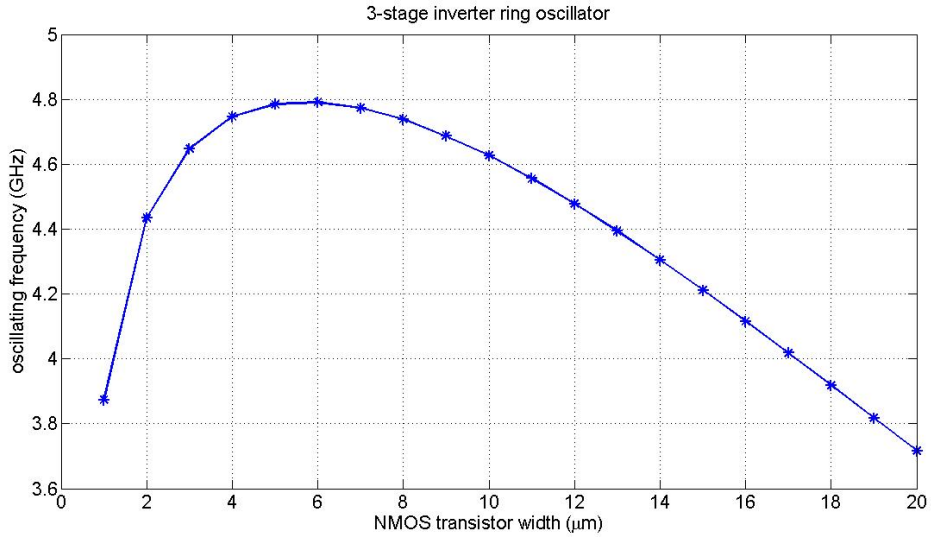


Fig. 6.3: Relationship between oscillation frequency and NMOS transistor width in a 3-stage inverter ring oscillator in 0.13μm IBM 8RF LM process.

The bias current nI_D of the current-starved ring oscillator shown in Fig. 6.1 is to starve the inverters from large power consumption. And the control of frequency by the voltage V_{bias} is achieved by how starved the inverters are forced. Fig. 6.4 shows the oscillation frequency of the current starved ring oscillator with the change of bias currents. The width of the bias NMOS transistors (e.g. M6 in Fig. 6.1) is varied in Fig. 6.4(a) and the voltage V_{bias} is varied in Fig. 6.4(b). The oscillation frequency increases at first with the increasing of bias current and reaches the summit when the inverters are not starved at all. The bias current cannot overcharge the inverter to infinite level

to achieve infinite high oscillation frequency. Both the branch current and the oscillation frequency are limited to the level of the basic inverter ring structure. Therefore, the maximum frequency in this case is under 4GHz. Manipulating the size of the transistors or using a multi-finger transistor may increase the oscillation frequency to about 7GHz in this process. For ultra high frequency application such as a 20GHz FM receiver, the structure is not feasible.

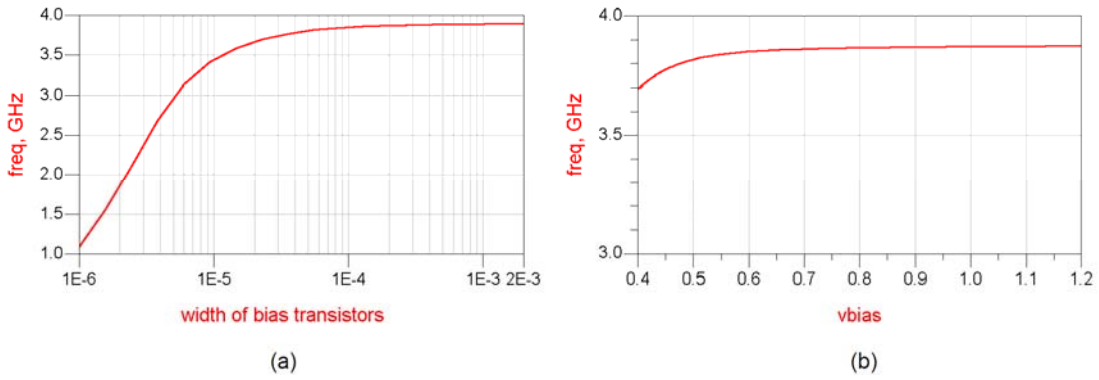


Fig. 6.4: The oscillation frequency of the current-starved ring oscillator with the change of bias current.

6.1.2 Temperature adaptive block

In Chapter 5, we mentioned an equation about temperature dependence of gate voltage of a saturated NMOS transistor:

$$V_{GS} = V_{GSF} + \alpha_{VT} T\left(1 - \sqrt{I_D / I_{DSF}}\right) \qquad (5.2)$$

where (V_{GSF}, I_{DSF}) is the common intercept point for transfer functions of the transistor at different measured temperatures. α_{VT} is the threshold voltage temperature coefficient.

For a designed circuit as in Fig. 6.1, current mirror ratio n, capacitive load C_{tot} and power supply voltage V_{dd} are fixed. According to Equation (6.3), in order to achieve a

constant target oscillating frequency at different temperatures, the drain current I_D of transistors M1 and M2 remains the same in spite of the temperature change. The constants V_{GSF}, I_{GSF}, α_{VT} and I_D of transistor M2 makes the gate voltage V_{bias} a linear function of temperature T to obtain a constant target frequency. The simulation result agrees with this derivation. Fig. 6.5 shows the required gate voltages V_{bias} to generate a 2.2GHz oscillation at different temperatures.

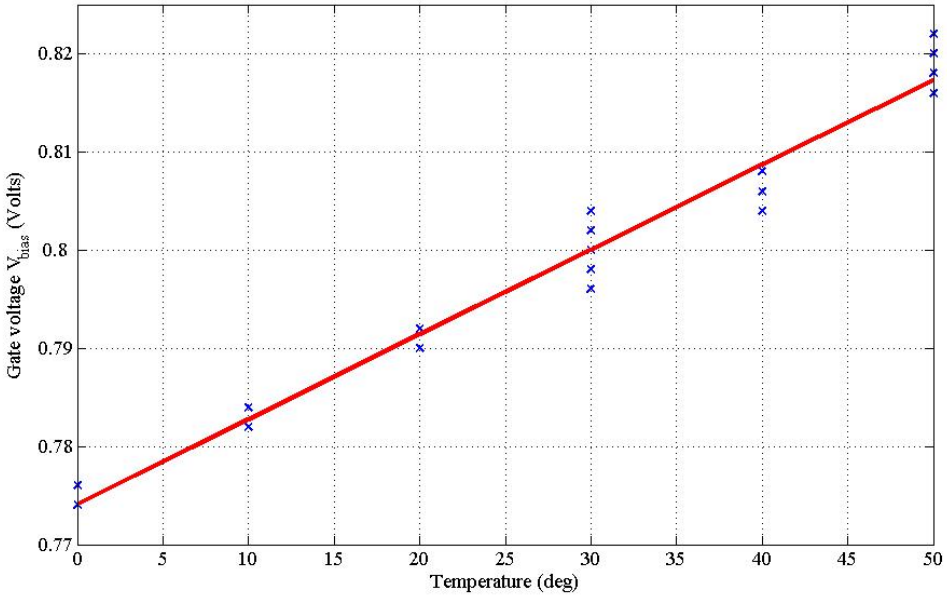


Fig. 6.5: The required gate voltages V_{bias} to generate a 2.2GHz oscillation at temperatures 0°C, 10°C, 20°C, 30°C, 40°C and 50°C.

Recall that the temperature sensor designed in Chapter 5 gives an output voltage linear to temperature. We can make use of this output voltage and generate the required gate voltage V_{bias} by building a temperature independent linear gain block. The circuit is shown in Fig. 6.6.

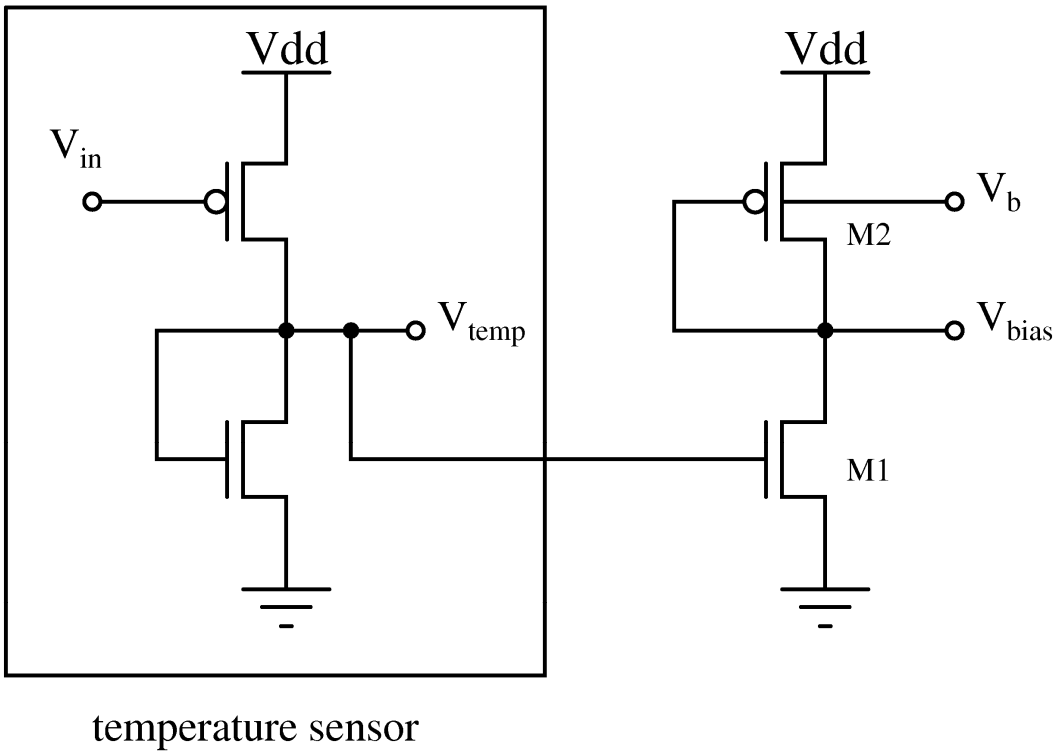


Fig. 6.6: The temperature adaptive block consisting of a temperature sensor and a temperature independent linear gain circuit.

Transistors M1 and M2 operate in saturation region. Ignore the channel modulation, the current flowing in transistor M1 is

$$I_{M1} = \frac{1}{2}\mu_n C_{ox} \frac{W_n}{L_n}\left(V_{temp} - V_{thn}\right)^2 \tag{6.6}$$

and the drain current of transistor M2 is

$$I_{M2} = \frac{1}{2}\mu_p C_{ox} \frac{W_p}{L_p}\left(V_{dd} - V_{bias} - \left|V_{thp}\right|\right)^2 \tag{6.7}$$

The Kirchhoff's current law tells us these two currents I_{M1} and I_{M2} are equal, which gives

$$\sqrt{\frac{\mu_n \frac{W_n}{L_n}}{\mu_p \frac{W_p}{L_p}}} = \frac{V_{dd} - V_{bias} - |V_{thp}|}{V_{temp} - V_{thn}} \tag{6.8}$$

Recall that in the model we used to derive Equation. (5.2), we assume the mobility of carriers as:

$$\mu_n = \mu_{n0}\left(\frac{T}{T_0}\right)^{-2} \qquad \mu_p = \mu_{p0}\left(\frac{T}{T_0}\right)^{-2} \tag{6.9}$$

Substitute Equation (6.9) to Equation (6.8), we obtain a positive constant on the left side. Assume the positive constant is x, then

$$V_{bias} = -xV_{temp} + xV_{thn} + V_{dd} - |V_{thp}| \tag{6.10}$$

Assume the transfer function of the temperature sensor is

$$V_{temp} = b - aT \tag{6.11}$$

where a and b are positive constants. Also recall the thermal effect on threshold voltage we used in the model is

$$\begin{aligned} V_{thn} &= V_{thn0} + \alpha_{VTn}(T - T_0) \\ |V_{thp}| &= |V_{thp0}| + \alpha_{VTp}(T - T_0) \end{aligned} \tag{6.12}$$

Substitute Equations (6.11) and (6.12) to Equation (6.10), we obtain

$$\begin{aligned} V_{bias} = &\left(ax + \alpha_{VTn}x - \alpha_{VTp}\right)T + \ldots \\ &\left(V_{dd} - |V_{thp0}| + \alpha_{VTp}T_0 + xV_{thn0} - x\alpha_{VTn}T_0 - bx\right) \end{aligned} \tag{6.13}$$

This is a linear expression of voltage V_{bias} in terms of temperature T. By tuning the W/Ls of transistors M1 and M2 in Fig. 6.6, we can manipulate the constant x to change the slope. The intercept can be tuned by changing the N-well potential V_b using the body effect on threshold voltage.

6.1.3 Output buffer

In radio frequency testing, the most widely-used probe has an impedance of 50Ω. In order to maximize the power transfer and minimize the reflections from the probe, the output impedance should match the impedance of the probe. This requires an output buffer with output impedance as 50Ω. We use a source follower circuit with an appropriate resistor to implement the circuit. The schematic is shown in Fig. 6.7. The inverter before it is a buffer to avoid a large capacitive load. The output buffer power dissipation is related to the power transferred to next stage. For a -13dBm output power, the simulated power consumption is around 1.7mW.

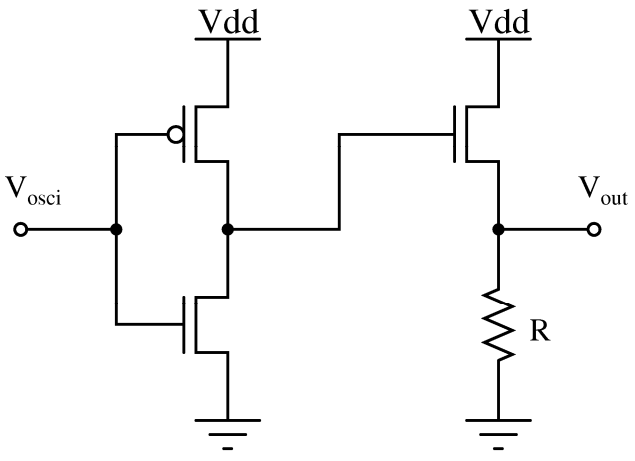


Fig. 6.7: The output buffer for impedance matching.

6.2 Simulation Results

Fig. 6.8 and Fig. 6.9 show the DC sweep of temperature. Fig. 6.8 shows the temperature sensor output voltage V_{temp} with respect of temperature T. Fig. 6.9 shows the temperature adaptive block output voltage V_{bias} with respect of temperature T. Both voltages show good linearity with temperature. Compare Fig. 6.9 and Fig. 6.5, V_{bias} has been well tuned to satisfy the temperature insensitive requirement.

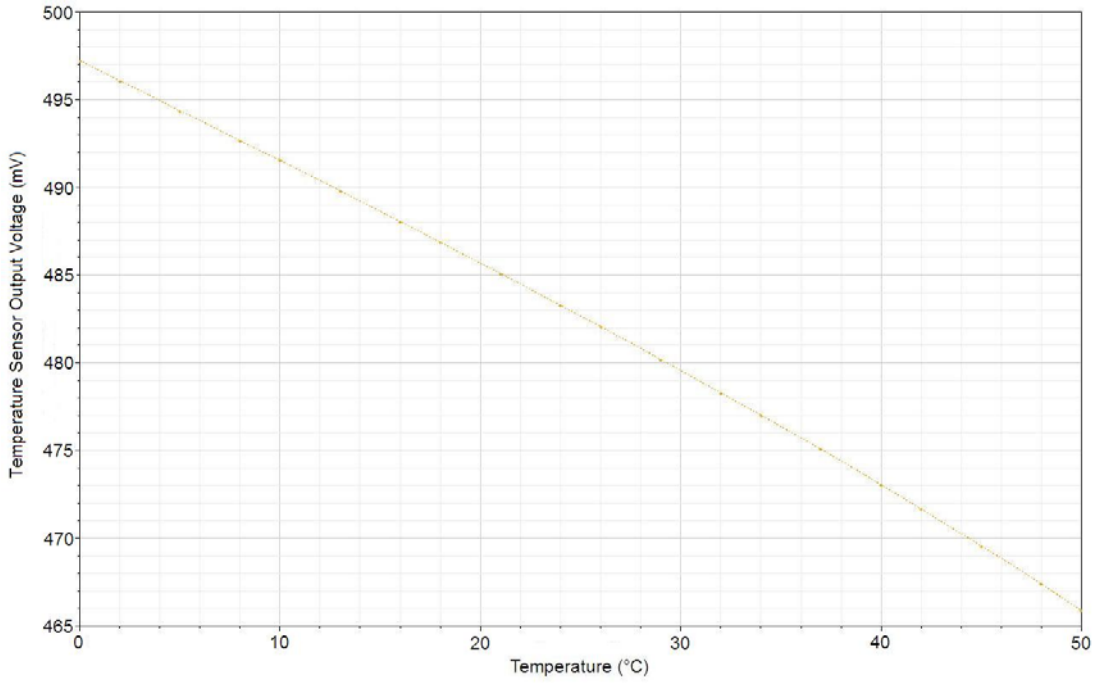


Fig. 6.8: Temperature sensor output voltage V_{temp} with respect of temperature T.

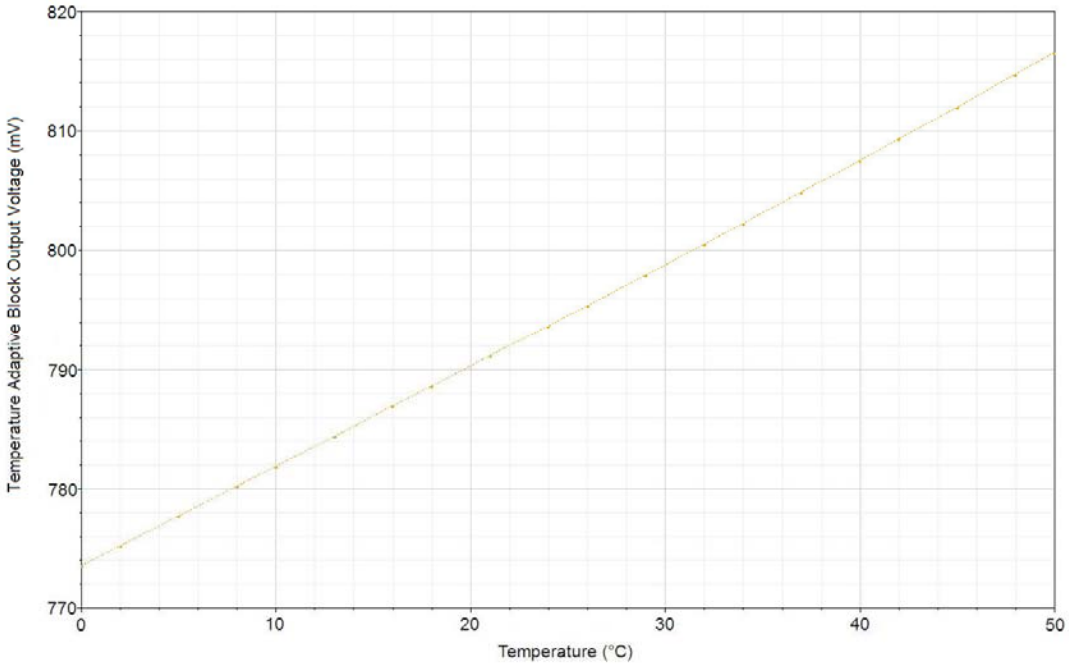


Fig. 6.9: temperature adaptive block output voltage Vbias with respect of temperature T.

Fig. 6.10 shows the spectrum of output voltage V_{out} at temperatures 0°C, 10°C, 20°C, 30°C, 40°C and 50°C. The circuit oscillates at a constant target frequency 2.2GHz with the help of the temperature adaptive block. The power consumption of the current-starved oscillator with a load inverter is around 300µW. The temperature adaptive block dissipates 32µW.

Fig. 6.11 shows the real part of output impedance of the buffer at different temperatures. The output buffer power dissipation is related to the power transferred to next stage. For a -13dBm output power, the simulated power consumption is around 1.7mW.

All the circuits are simulated with appropriate bypass capacitors, ESD protection circuits and pads.

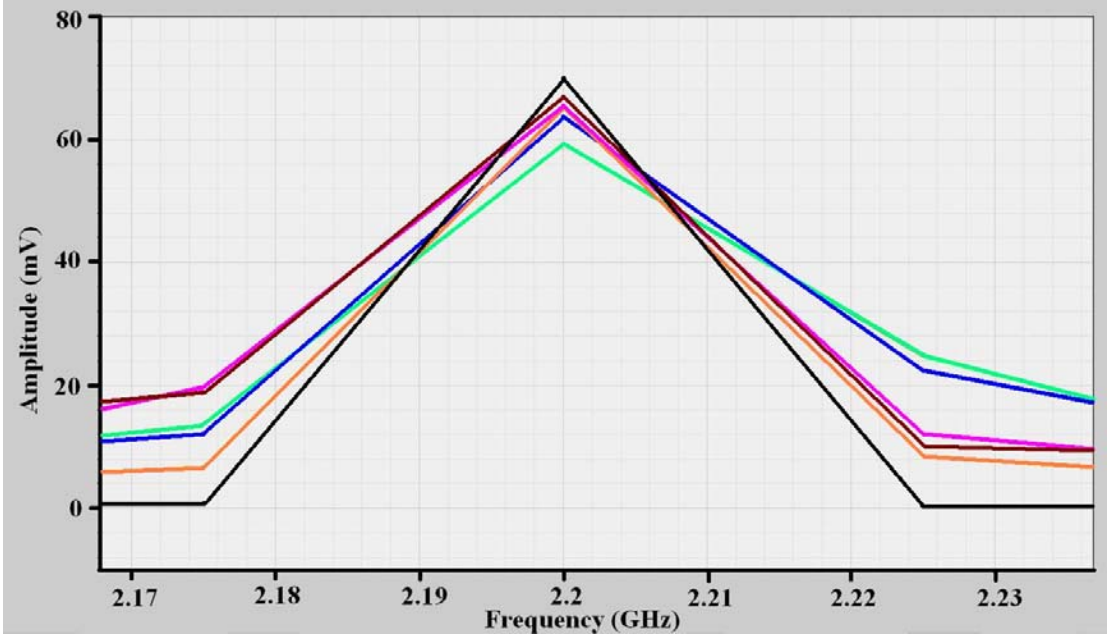


Fig. 6.10: Spectrum of output voltage Vout at temperatures 0°C, 10°C, 20°C, 30°C, 40°C and 50°C.

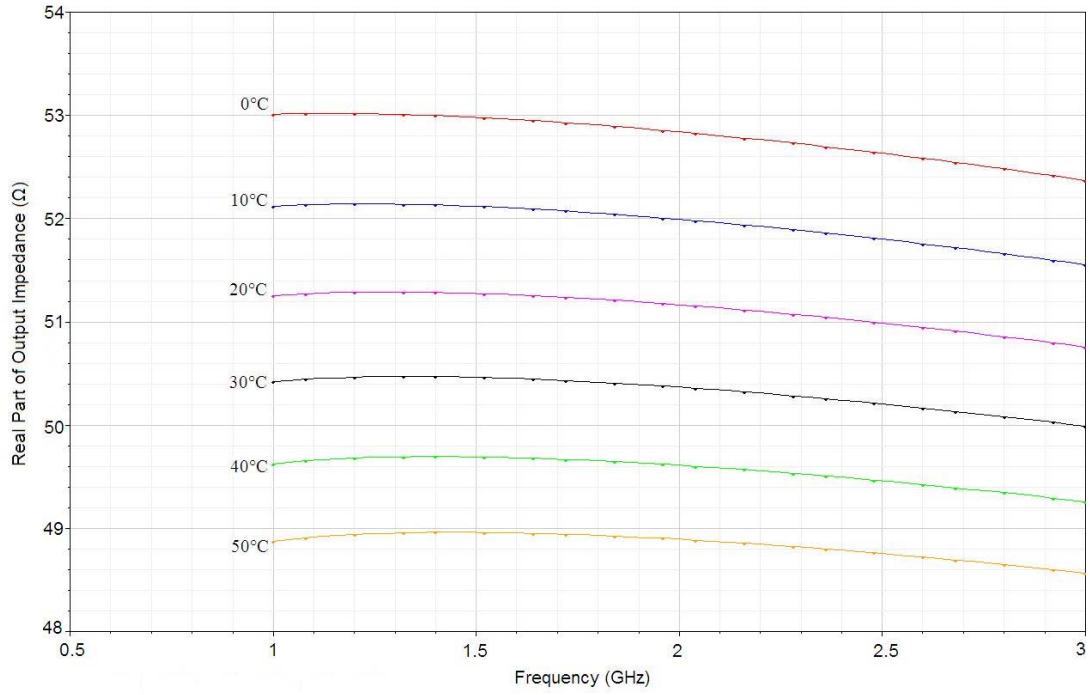


Fig. 6.11: real part of output impedance of the buffer at temperatures 0°C, 10°C, 20°C, 30°C, 40°C and 50°C.

6.3 Layout and Experimental Results

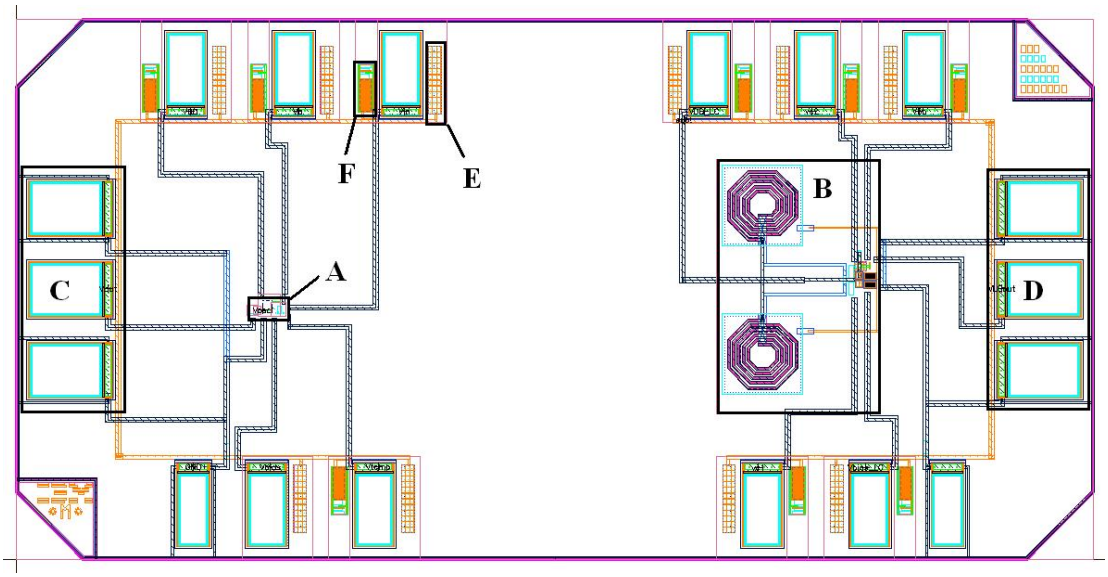


Fig. 6.12: Layout of the temperature insensitive oscillator.

Fig. 6.12 is the layout of the temperature insensitive oscillator. Part A is the temperature sensor. Part B is the temperature independent gain block. Part C is the current-starved ring oscillator. Part D is the inverter. Part E is voltage follower buffer.

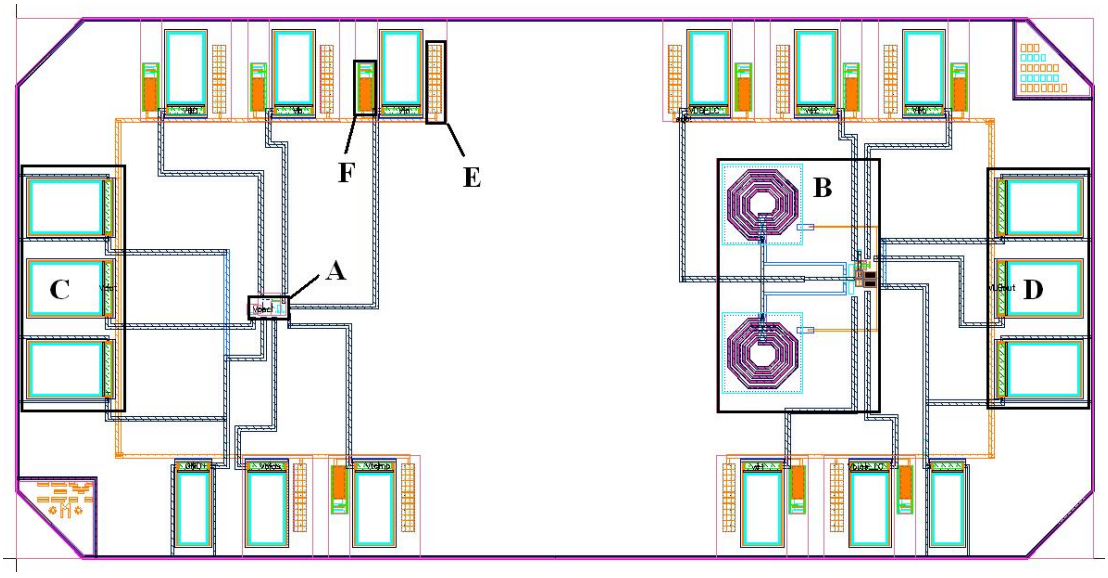


Fig. 6.13: Whole chip layout.

Fig. 6.13 shows the whole chip layout. Part A is the temperature insensitive oscillator. Part B is a differential LC oscillator. Part C and Part D are ground signal ground (GSG) pads for outputs of the two oscillators. Other pads are connected to bypass capacitors (e.g. Part E) and ESD protection circuits (e.g. Part F) when necessary.

Fig. 6.14 shows the test results of current-starved ring oscillator at room temperature. Fig. 6.14(a) shows the output spectrum when the voltage V_{bias} is 0.75V as required in simulation for 2.2GHz. Due to layout parasitic capacitance and resistance, the actual tested oscillation frequency is only 1.397GHz with power of -17.47dBm. With the voltage pushing as high as 1.6V, the oscillation frequency can reach 2.235GHz with the power of -16.12dBm shown in Fig. 6.14(b). 1.6V is the maximum acceptable voltage on the 0.13μm IBM 8RF LM thin gate transistors. The power of the output signal is about -3dBm lower than designed. This phenomenon has been observed in all the tests including LNA and power amplifier tests using the same set of equipments. The power lost is believed to be related to the test environment.

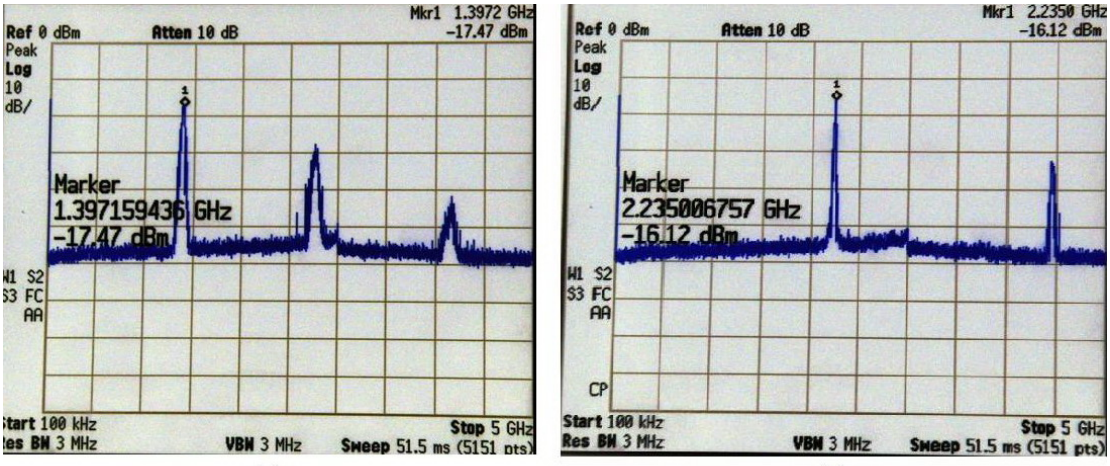


Fig. 6.14: Test results of the current-starved ring oscillator at room temperature.

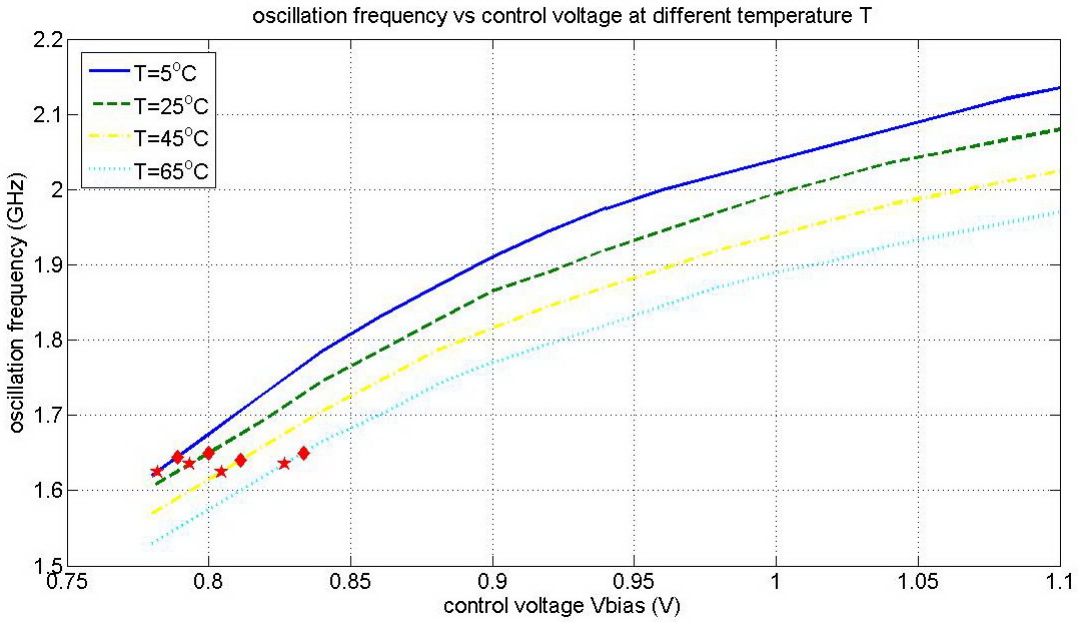


Fig. 6.15: The relationship between oscillation frequency and control voltage at temperatures 5°C, 25°C, 45°C, 65°C.

The temperature insensitivity has been tested using a temperature chunk with the probe station. The bare die was put on the chunk which is connected to a temperature controller. First, the control voltage with oscillation frequency relationship was tested at different temperatures. Fig. 6.15 shows the results at 5°C, 25°C, 45°C, 65°C. Without the temperature compensation, the temperature variance is about 100MHz around 1.6GHz when the control voltage is 0.8V and the temperature is from 5°C to 65°C. That translates into a 6.25% frequency variance around 1.6GHz. The diamond and star points in the figure show two groups of oscillation frequency at different temperatures with the temperature compensation. The two group data are measured with different bias voltage V_b in Fig. 6.6. Each group has a frequency variance of 10MHz, one group frequencies are centered at 1.63GHz and the other group frequencies are center at 1.645GHz. That translates into a 0.6% frequency variance

and temperature coefficient of 100ppm/°C. The temperature insensitivity has been improved about 10 times with automatic compensation. The experimental results has been listed and compared with previous work in Table 6.1. This work outperforms the previous work by improving the sensitivity with much less of power dissipation. The only comparable work [68] is an LC oscillator with large chip consuming 10 times more power. The oscillation frequency is lower than the target frequency 2.2GHz due to layout parasitics, and can be improved in later design by taking the parasitics into account.

	frequency	sensitivity	temperature range	power	process
[64]	1.3~1.8GHz	500 ppm/°C	0°C ~70°C	23mW	0.5µm
[65]	700MHz	86.5 ppm/°C	15°C~125°C	8.3mW	0.6µm
[66]	400MHz	212 ppm/°C	0°C~85°C	138.6mW	0.25µm
[67]	800MHz	609 ppm/°C	-20°C~100°C	18.95mW	0.25µm
[68]	10GHz	133 ppm/°C	-50°C~100°C	3.7mW	0.18µm
this work	1.645GHz	100 ppm/°C	5°C~65°C	332µW	0.13µm

Table 6.1: Experimental results of temperature sensistivity compared to previous works.

6.4 Application in 2.2GHz OOK Transceiver

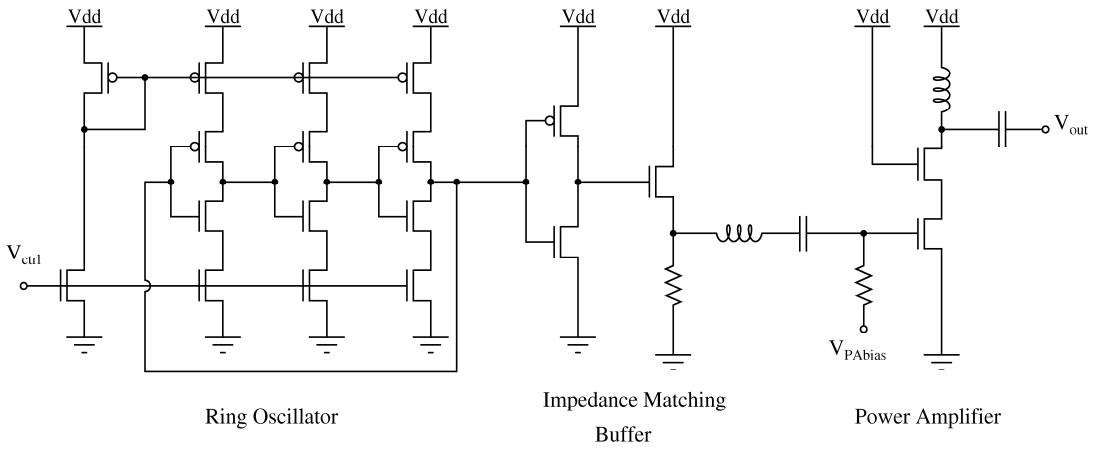


Fig. 6.16: Schematics of the 2.2GHz OOK transmitter.

The voltage-controlled oscillator shown in Fig. 6.1 has been applied in the 2.2GHz OOK transceiver wireless communication system. The full circuit of the transmitter in the wireless system is shown in Fig. 6.16. With an impedance matching circuit and a power amplifier, the transmitter can generate a modulated signal of 0dBm at 2.2GHz. With the baseband signal connected to V_{ctrl} at tuned amplitude, the transmitter saves space and power of a NAND mixer before the power amplifier circuit.

The transmitter layout is designed on a 1mm by 1mm chip shown in Fig. 6.17(a) and fabricated in 0.13µm IBM 8RF LM process. The chip is assembled in a 5mm by 5mm QFN 16-pin packaged shown in Fig. 6.17(b).

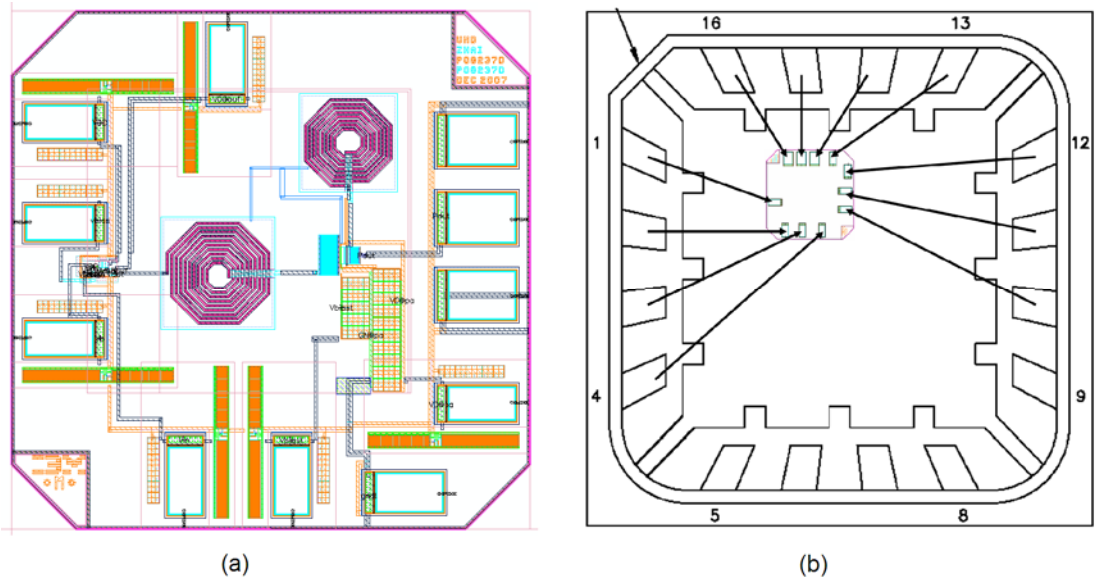


Fig. 6.17: (a) Chip layout of the 2.2GHz OOK transmitter. (b) Assembly diagram of the chip package.

A PC Board is designed to test the transmitter. The schematic and layout of the PC Board is shown in Fig. 6.18. The 2-layer PC Board has one ground plane to

provide shielding, enables heat dissipation, and reduces stray inductance. The increased parasitic capacitance also helps to bypass power supply noise. Regulators, potentiometers and capacitors are placed on the PC board to provide stable power supply and bias voltages.

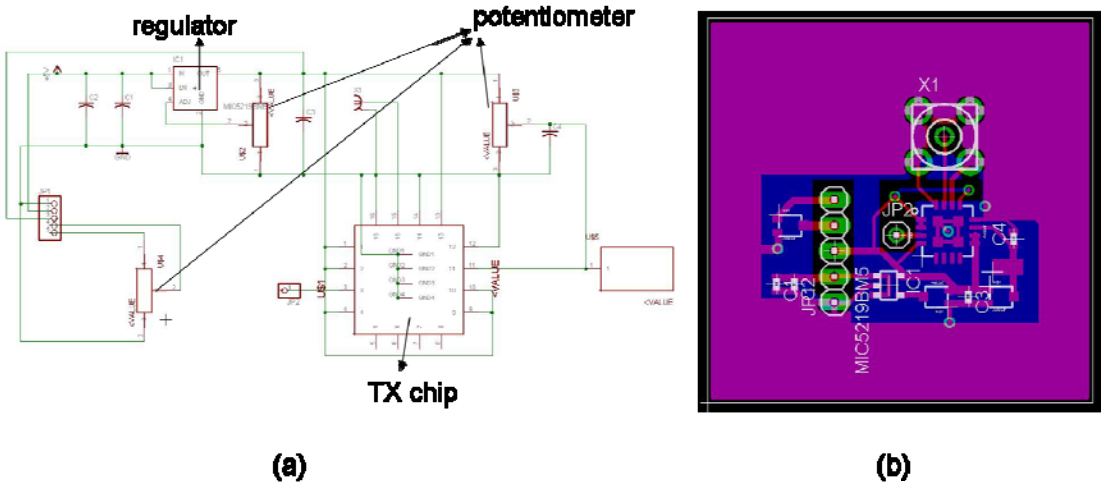


Fig. 6.18: (a) Schematic of the PC Board design. (b) Layout of the PC Board.

There is a designed stencil with each designed PC Board. With the stencil aligned on the PC Board, solder paste can be applied on the place as wanted by a blade. Then the packaged chip and all the surface mount components are placed on the PC Board with solder paste using an optically aligned pick and place machine. Finally, the populated PC Board is placed in a re-flow oven and the solder paste will melt at the controlled temperature 230F until the solder paste shines. When the solder is cool, all the components are well fixed to the PC board without damage. The whole process is demonstrated in Fig. 6.19. After the PC Board is cool, through hole components can be soldered on it by hand. Fig. 6.20 shows a PC Board with the transmitter chip and all the other components on it. The PC Board is 1.5 inches by 1.5 inches in dimension. Fig. 6.21 shows the frequency response of the transmitter output.

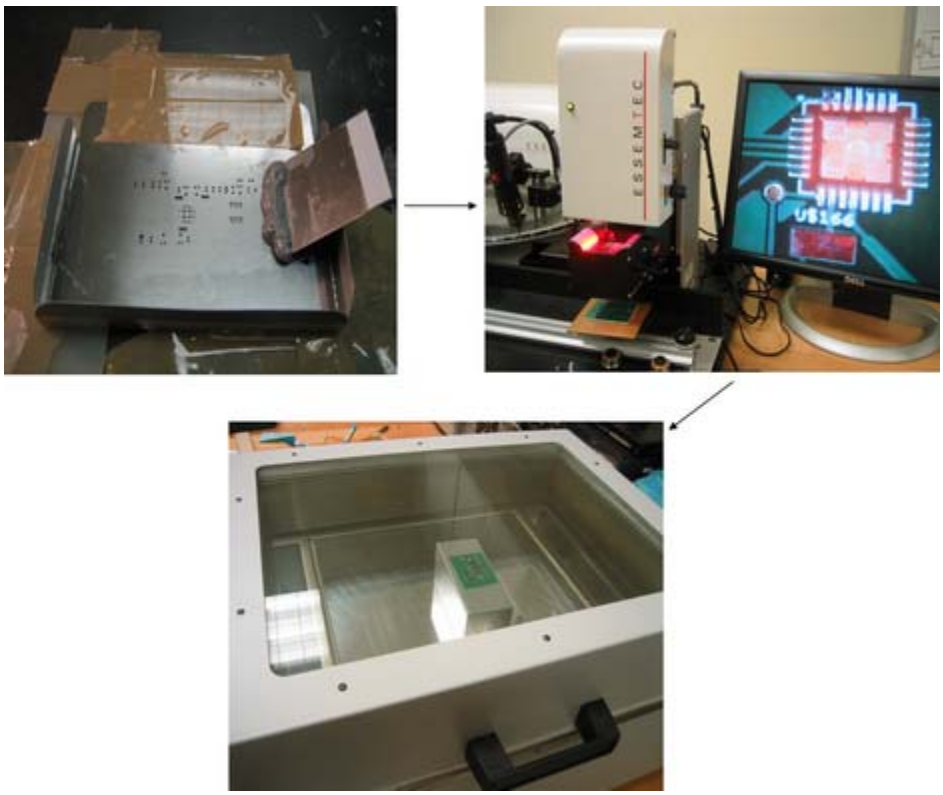


Fig. 6.19: The process to solder surface amount components on PC Boards precisely.

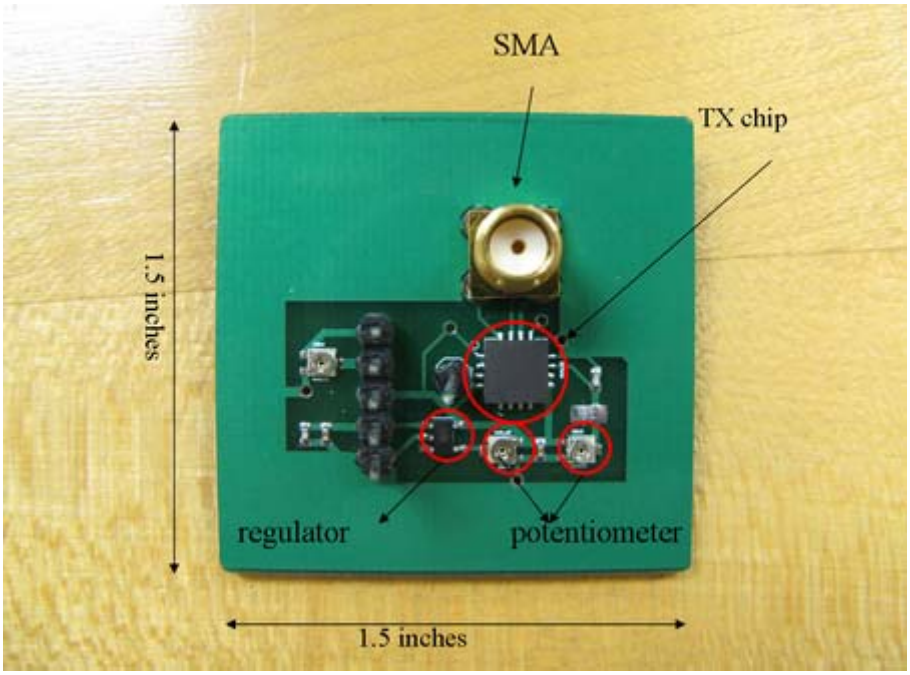


Fig. 6.20: A picture of the PC Board with all components soldered.

Fig. 6.21 shows the frequency response of the transmitter output when V_{ctrl} voltage is set at 0.8V. The circuit transmits a -2dBm signal at 2.2GHz. The spectrum has two spurs at 2.2GHz ± 25MHz. The phase noise is -100dBc/Hz at 25MHz, which is good enough for OOK transceiver system. Fig. 6.22 shows the output signal in the time domain. The green line is the baseband signal and the yellow line is the transmitter output signal. When the baseband digital signal changes from 0 to 1, it takes about 150ns for transmitting a stable output signal. That means the baseband modulation frequency can be as high as 3MHz. The PC board dissipates 4.8mW power at 2.2GHz, more than half of the power is consumed on the power amplifier.

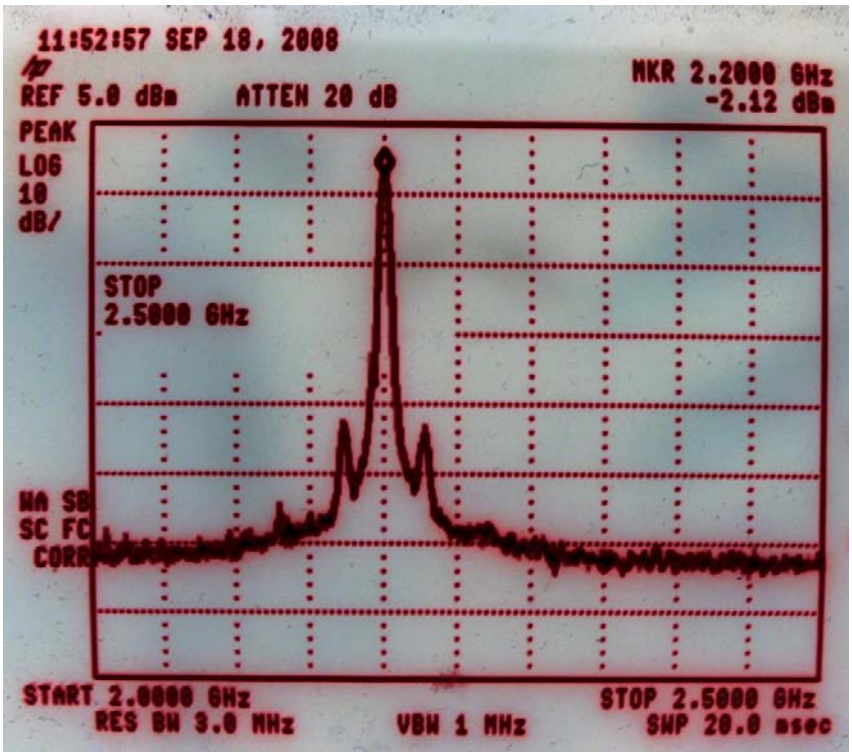


Fig. 6.21: frequency response of transmitter output.

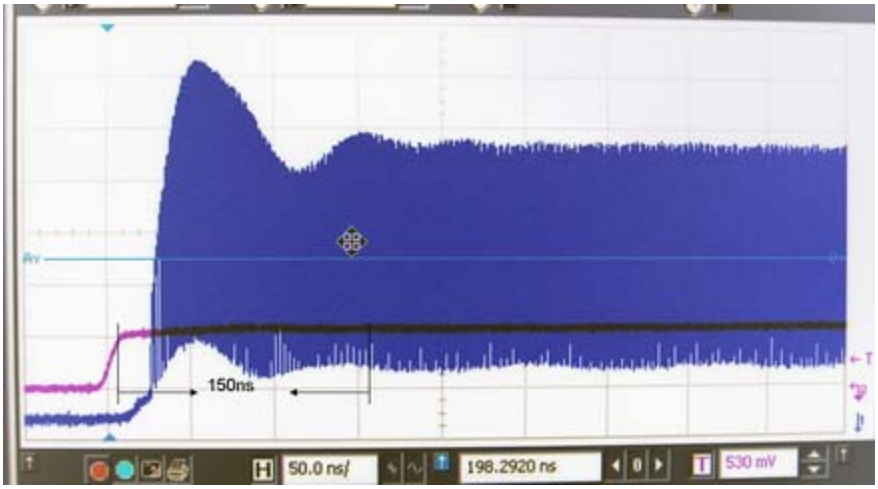


Fig. 6.22: Transmitter output signal output when the baseband signal changes from 0 to 1.

We test the signal transmission by pairing the transmitter with a custom 2.2GHz OOK receiver chip designed by my colleague Bo Yang. Both the receiver chip and the transmitter chip are taped on insulated foam for convenient movement. Two commercial SMA antennas are used at the receiver input and the transmitter output. The distance between the transmitter and receiver can be as far as one meter without interference in between for good transmitting and receiving of signals. Fig. 6.23 shows the experimental results of the transceiver system at different frequencies. The top blue line is transmitter baseband input signal and the bottom yellow line is the receiver output signal. Fig. 6.23 (a~f) are results when the baseband signal is at 20kHz, 100kHz, 400kHz, 700kHz, 1MHz, 1.4MHz respectively. With the baseband frequency increasing, the receiver output signal changes from sharp edge pulse to almost triangle signal because the rising and falling time becomes more dominant in a period. The output swing remains at about 1V when frequency is up to 1.4MHz. The experimental results demonstrate that the wireless system of the transmitter and receiver function successfully when the baseband is lower than 1.4MHz and the distance between the

transmitter and receiver is not more than one meter. The upper limit of the baseband frequency is believed to be bounded by the receiver design.

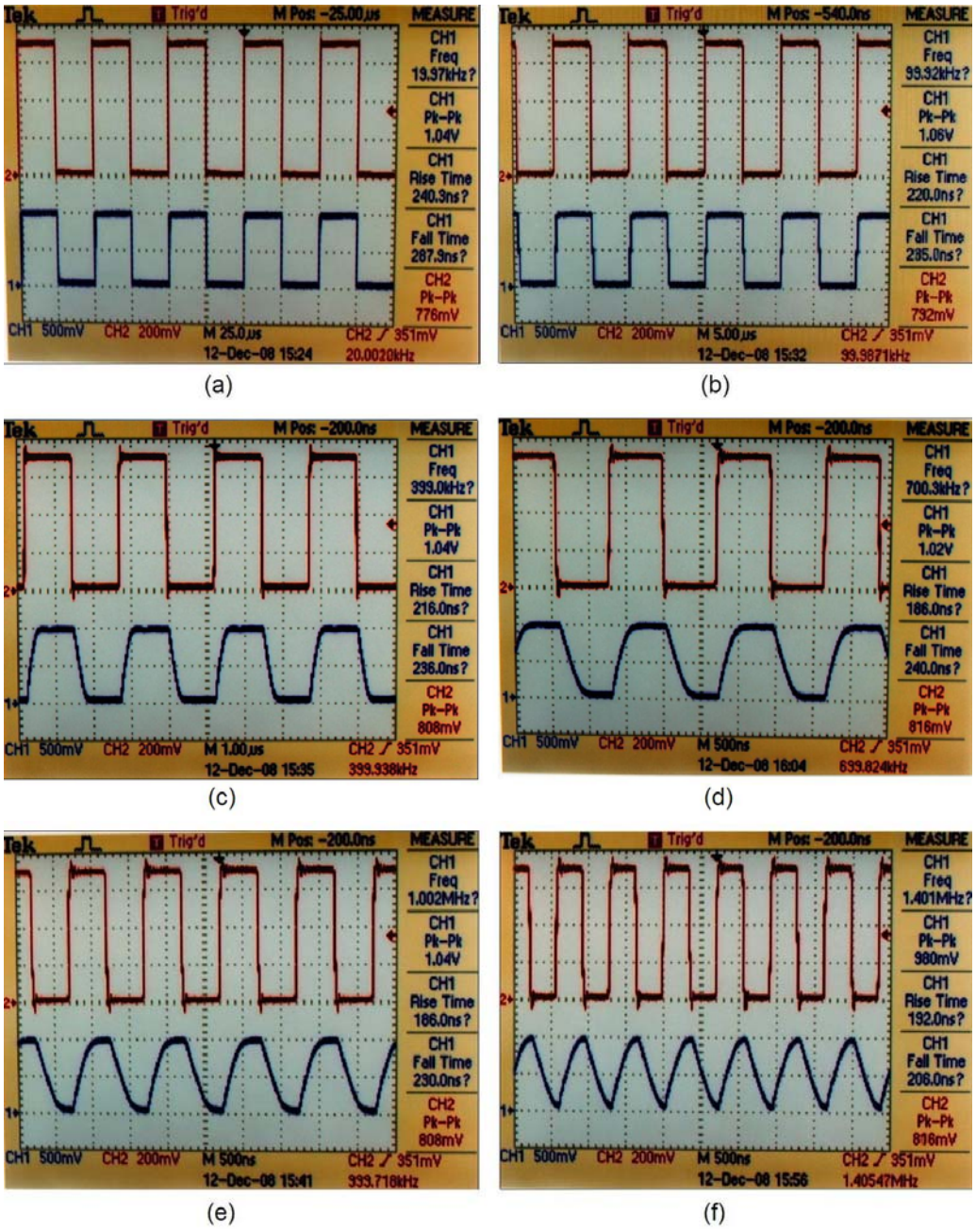


Fig. 6.23: Experimental results of the custom transceiver system when the baseband signal is at 20kHz, 100kHz, 400kHz, 700kHz, 1MHz and 1.4MHz.

6.5 Summary

We have described a low power temperature insensitive oscillator for radio frequency wireless communication. We chose to implement the oscillator using CMOS transistors instead of LC tank because CMOS ring oscillators are compact and operate with low power and have large full power supply output range. Although CMOS ring oscillators have so many advantages, the temperature dependence of the transistor behavior makes the oscillating frequency unstable in different environments, which is not acceptable for most wireless communication. In order to compensate the floating of the oscillating frequency, we've design a temperature adaptive block. The block contains a temperature sensor to measure the temperature and adjust the required bias voltage accordingly.

We have presented simulation results that demonstrate the success of locking the target oscillating frequency. The power consumption is 332μW, which is much smaller than current published LC oscillators. We have also presented a chip layout in IBM 8RF LM 0.13μm CMOS technology. The area of the temperature insensitive oscillator is about $0.002mm^2$. The experimental results show that the frequency stability with respect of temperature variance from 5°C to 65°C has been improved 10 times with temperature adaptive block. The performance of temperature compensation of the output frequency is better than the previous work. The power consumption is at least 1 order smaller than current published temperature compensated voltage controlled oscillators.

The VCO has been applied in a 2.2GHz OOK transmitter and the wireless network made of the transmitter and another custom receiver shows successful signal transmitting and receiving up to 2.8Mbps in one meter.

Chapter 7: Low Power Phase Locked Loop Based FM Receivers

7.1 A Low Power 2.2GHz Phase Locked Loop used for FM Receiver

7.1.1 Circuit Design

The structure of a FM receiver using phase locked loops (PLL) is shown in Fig 5.4. Besides the first low noise amplifier (LNA) stage, the PLL and the output amplifier is illustrated in this chapter for 2.2GHz wireless communication. Fig. 7.1 shows the block diagram of the PLL and the output amplifier.

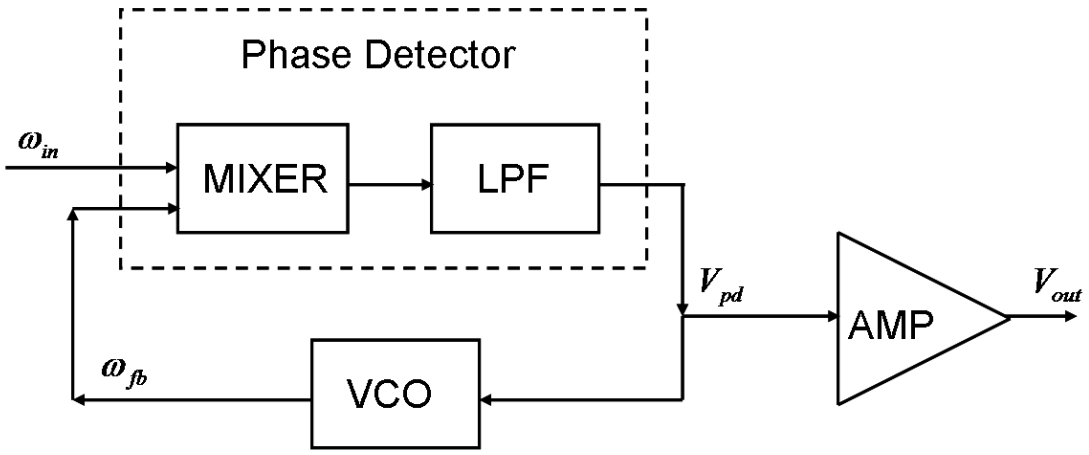


Fig. 7.1: The block diagram of the PLL and output amplifier.

The PLL is made up of three blocks, a mixer, a low pass filter and a voltage controlled oscillator. The mixer and the low pass filter together constitute a phase detector which translates the phase difference between the input signal and feedback signal into a voltage signal V_{pd}. When the PLL is locked, the frequency of the

feedback signal ω_{fb} tracks the frequency of the input signal ω_{in}. And the VCO input V_{pd} is proportional to the frequency of the feedback signal ω_{fb}. Therefore, the frequency information of the input signal ω_{in} is carried by V_{pd} and amplified at the later stage to the output V_{out}. The circuit design of each block in Fig. 7.1 is presented in this section respectively. (This work was performed in collaboration with University of Maryland colleague Bo Li.)

7.1.1.1 Phase detector

The design of phase detector is a collaborated work with my colleague Bo Li. The phase detector consists of a single branch mixer and a low pass filter. The mixer multiplies the two input signals V_{in} and VCO_{out} and generates the phase difference information. The low pass filter tampers the high frequency noise on the phase difference information. The circuit schematic of the phase detector is shown in Fig. 7.2.

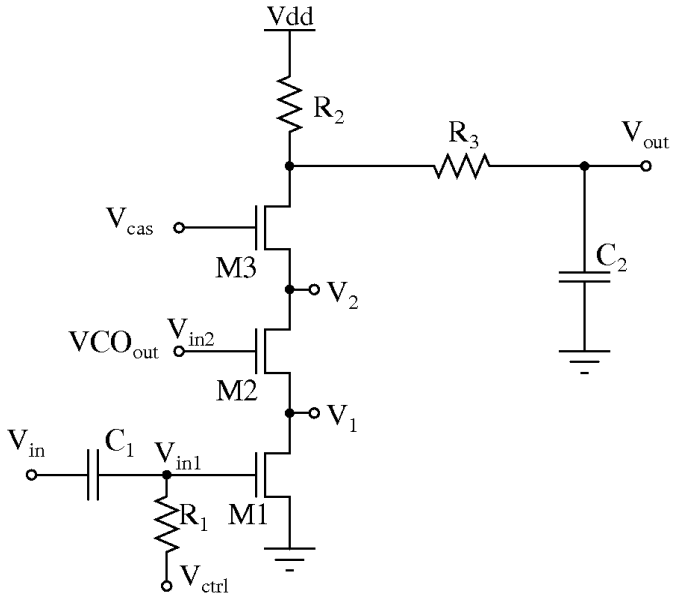


Fig. 7.2: The schematic of the phase detector used in 2.2GHz low power PLL.

The mixer is made up of three transistors in a single current branch from Vdd. The two inputs V_{in1} and V_{in2} are fed by the RF input signal from the LNA with AC coupling and the VCO output respectively. According to Kirchhoff's current law, the current flowing in transistors M1 and M2 are the same. Assume both M1 and M2 are in saturation region and ignore the channel length modulation of M2, the current can be expressed as

$$I = \frac{1}{2}\mu C_{ox}\frac{W_1}{L_1}(V_{in1} - V_T)^2(1+\lambda V_1) = \frac{1}{2}\mu C_{ox}\frac{W_2}{L_2}(V_{in2} - V_1 - V_T)^2 \quad (7.1)$$

μ is the electron mobility and C_{ox} is the gate oxide capacitance. $\frac{W_1}{L_1}$ and $\frac{W_2}{L_2}$ are width to length ratio of the transistor M1 and M2. V_T is the threshold voltage of the NMOS transistor. λ is the channel length modulation parameter.

And the drain voltage of the transistors M1 can be derived as

$$V_1 = V_{in2} - V_T - \sqrt{\frac{2I}{\mu C_{ox}\frac{W_2}{L_2}}} \quad (7.2)$$

Substitute equation (7.2) to equation (7.1), the current across transistor M1 is rewritten as

$$I = \frac{1}{2}\mu C_{ox}\frac{W_1}{L_1}(V_{in1} - V_T)^2\left(1+\lambda\left(V_{in2} - V_T - \sqrt{\frac{2I}{\mu C_{ox}\frac{W_2}{L_2}}}\right)\right) \quad (7.3)$$

In equation (7.3), the electron mobility μ, the gate oxide capacitance C_{ox}, the width to length ratios $\frac{W_1}{L_1}$ and $\frac{W_2}{L_2}$, threshold voltage V_T and the channel length modulation parameter λ can be taken as constants. With proper low pass filtering, only the low frequency term $\frac{1}{2}\mu C_{ox}\frac{W_1}{L_1}(-2V_T V_{in1})\cdot(\lambda_1 V_{in2})$ is left to implement the multiplying of the two inputs V_{in1} and V_{in2}. With the resistor R_2 on the top of this current branch, the multiplying information is transformed from current I in equation (7.3) to the output voltage.

Besides the low pass filter made up of resistor R_3 and capacitor C_2, the cascode transistor M3 also helps amplifying the low frequency signal and dampening the high frequency harmonics. The small signal equivalent circuit of the transistor M3 is illustrated in Fig. 7.3. R_{in} is the output resistance looking towards transistor M2 at the source of the transistor M3. r_o is the channel length modulation resistance of the transistor M3. (Analysis here performed in collaboration with colleague Bo Li.)

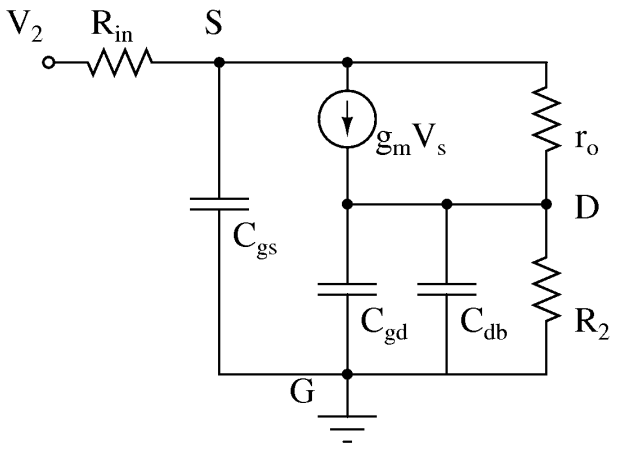


Fig. 7.3: Small signal equivalent circuit of transistor M3 in the schematic of the phase detector.

Transistor M3 here serves as a common gate amplifier. The load at the drain of the transistor is defined as

$$Z_L = C_{gd} \left\| C_{db} \right\| R_2 = \frac{R_2}{1 + s\left(C_{gd} + C_{db}\right)R_2} \tag{7.4}$$

The small signal voltage gain defined as

$$A_v = \frac{V_d}{V_2} = \frac{\left(g_m r_0 + 1\right)Z_L}{\left(1 + sC_{gs}R_{in}\right)\left(Z_L + r_0\right) + R_{in}\left(g_m r_0 + 1\right)} \tag{7.5}$$

For low frequency harmonics, resistance dominates at the load so that

$$Z_L \approx R_2 \tag{7.6}$$

Since $g_m r_0 >> 1$, the small signal voltage gain can be approximated as

$$A_{low} \approx \frac{R_2}{R_{in}} \tag{7.7}$$

For high frequency harmonics, capacitance dominates at the load so that

$$Z_L \approx \frac{1}{s\left(C_{gd} + C_{db}\right)} = \frac{1}{sC_t} \tag{7.8}$$

C_t is the total capacitance at the drain of transistor M3. The small signal voltage gain can be rewritten as

$$A_{high} \approx \frac{g_m r_0 + 1}{\left(1 + sC_{gs}R_{in}\right)\left(1 + sC_t r_0\right) + sR_{in}C_t\left(g_m r_0 + 1\right)} < \frac{1}{sR_{in}C_t} << 1 \tag{7.9}$$

According to equations (7.7) and (7.9), the common gate amplifier implemented by transistor M3 can be designed to have large gain at low frequency and minimal gain

at high frequency. The transistor M3 not only amplifies the low frequency multiplying signal, but also filters out high frequency noise before the low pass filter.

The beauty of the single branch phase detector is that only one current is drawn from the power Vdd to realize all the mixing, amplifying and filtering function, which results in low power consumption. Both input signals are fed into a gate of a small transistor for large resistive and small capacitive load. The input signal from the LNA to the phase detector has an AC coupling structure. The bias voltage V_{ctrl} controls the DC current of the phase detector and varies the output DC voltage of the phase detector accordingly. This output voltage is fed into the VCO and changes the free running frequency of the PLL. The tuning of the bias voltage V_{ctrl} makes it possible to shift the frequency of the RF input signal from one frequency channel to another. The power of the phase detector is mainly determined by the power voltage Vdd and the bias voltage V_{ctrl}. (The work in this section was performed in collaboration with my colleague from University of Maryland, Bo Li, and has been submitted for publication [69]).

7.1.1.2 Voltage controlled oscillator

The current starved CMOS ring oscillator is used in the design of the low power PLL for its micro-watt power consumption, compactness and simplicity. Large output swing is also a selling point of this oscillator, because a larger input to the phase detector leads to easier locking and wider lock-in frequency range. In contrast, the quality factor of most on chip inductors at 2.2GHz frequency range is below 20. Therefore, most LC oscillators [29-34] suffer from milli-watt power consumption and

large chip area. Moreover, Ring oscillator based VCO can oscillator in a wide frequency range compared with LC counterpart. In this work, we seek the extremely low power goal with acceptable phase noise for the application in the PLL.

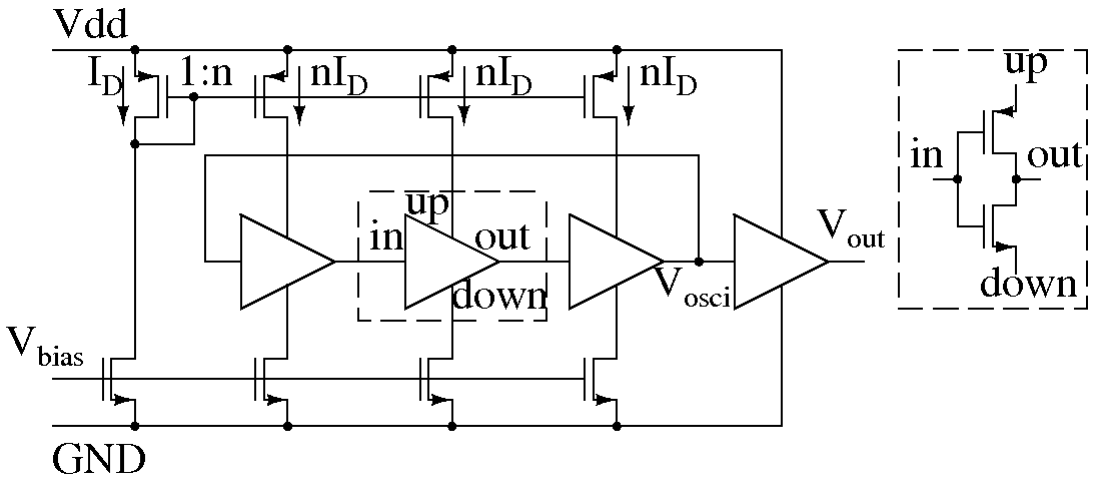


Fig. 7.4: The schematic of the current starved ring oscillator.

Fig. 7.4 shows the schematic of the current starved ring oscillator used as the VCO in the PLL. The same architecture has been used in the design of temperature insensitive oscillator. However, the voltage to frequency relationship is different in this design. By varying the parameters of the transistors, we design the VCO to oscillate at 2.2GHz with the input around 0.6V, which is half of the voltage Vdd. The voltage to frequency relationship should be considered together with the design of the phase detector, because the output DC voltage of the phase detector corresponds to the free running frequency of the VCO.

7.1.1.3 Output amplifier

The output amplifier design is shown in Fig. 7.5 below. The circuit is a two stage amplifier implemented by a common-source differential pair and a common source

amplifier. Cascode transistors are used in both gain stages to achieve higher bandwidth. The output amplifier has a gain of 50 at 16MHz and the power consumption of it is only 139μW.

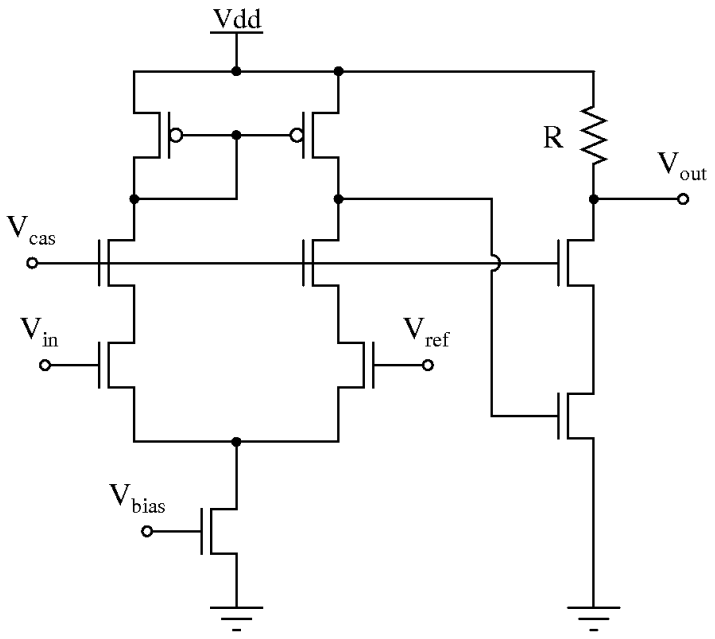


Fig. 7.5: The schematic of the output amplifier.

7.1.2 Simulation results

All the circuits of the phase detector, current starved ring oscillator and the output amplifier are simulated using Cadence RFDE simulator with the IBM 0.13μm 8RF LM CMOS technology.

We first simulate the phase detector with two input signals at different frequency with the same phase. This simulation tests the multiplying and low pass filtering of the circuit. A -35dBm RF signal at 2.2GHz and a rectangular wave at 2.195GHz oscillating from 0 to 1.2V have been fed into the phase detector. Table 7.1 shows the harmonics of the output V_{out} in Fig. 7.2 at different frequencies. Except the DC

components 0.605, the biggest harmonic is the one of 0.011 at 5MHz, which is the frequency difference of the two input signals. The second largest harmonic is at 2.2GHz with the amplitude 7.739e-5 as less than 1% of the amplitude at 5MHz. The circuit calculates the frequency difference and dampens the other frequency harmonics successfully.

freq	M_OUTPUT
0.0000 Hz	0.605 / 0.000
5.000 MHz	0.011 / 25.867
10.00 MHz	1.319E-5 / -130.168
2.190 GHz	9.618E-9 / 125.991
2.195 GHz	7.391E-6 / 60.036
2.200 GHz	7.739E-5 / -107.019
2.205 GHz	1.766E-10 / -135.583
4.385 GHz	1.409E-8 / -83.290
4.390 GHz	8.462E-7 / -173.972
4.395 GHz	5.705E-8 / -114.364
4.400 GHz	1.310E-7 / -5.989
4.405 GHz	4.328E-10 / -146.407
6.585 GHz	2.312E-6 / -113.089
6.590 GHz	5.559E-9 / -72.008

Table 7.1: The harmonics at different frequencies of the phase detector output when the phase detector is fed with two input signals at 2.2GHz and 2.195GHz.

Then the phase detector is simulated with two input signals at the same frequency 2.2GHz with different phase. The simulation tests the phase difference detection of the circuit. A -35dBm RF input at 2.2GHz with variable phase and a pulse at 2.2GHz oscillating from 0 to 1.2V have been fed into the phase detector circuit. Fig. 7.6 shows the relationship between the phase detector voltage output and the variable phase in radians of the input RF signal. With the phase difference varying about π from 0.254 to 3.364, the output of the phase detector changes from the maximum 0.604V to the minimum 0.568V. The output of the phase detector is a sinusoidal function of the phase difference between the two input signals. In half cycle, the voltage output

function of the phase difference is monotonic. And the phase difference can always converted into any one of the monotonic half cycles. So the voltage output is monotonic with the phase difference variation. Therefore, the phase difference is detected by the voltage output of the phase detector circuit.

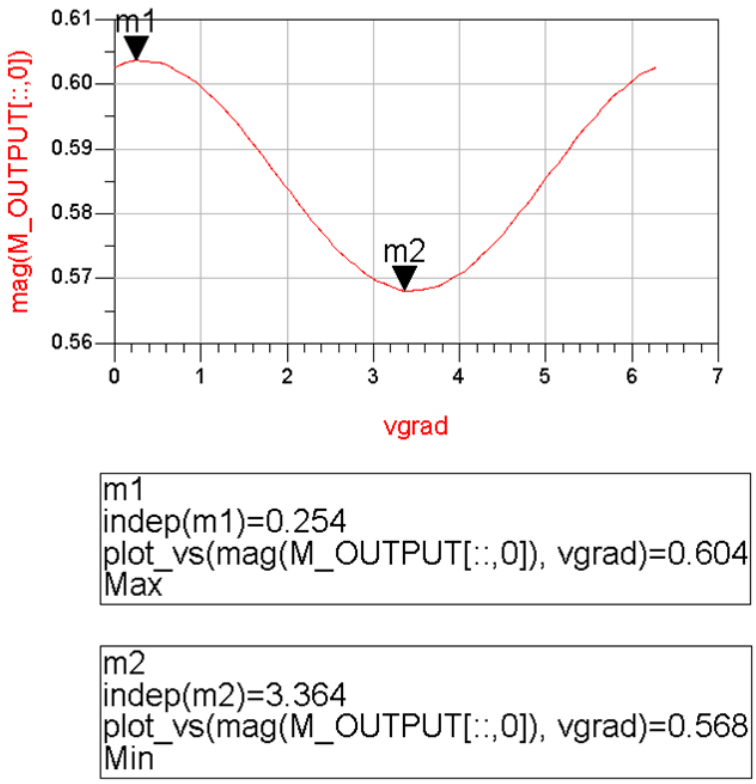


Fig. 7.6: The relationship between the phase detector output and the phase difference between the two input signals when the phase detector is fed with two inputs at the same frequency 2.2GHz.

The performance of the phase detector is evaluated by four important characteristics, noise figure NF, power consumption P, conversion gain G and the linearity IIP3. A figure of merit (FOM) is defined in [70] as

$$FOM = 10\log\left(\frac{10^{G/20}\cdot 10^{(IIP3-10)/20}}{10^{NF/10}\cdot P}\right) \tag{7.10}$$

The conversion voltage gain and the noise figure are expressed in dB and the IIP3 is expressed in dBm. The power consumption is expressed in watts. Lower noise figure and power consumption and higher voltage gain and IIP3 result in better performance of the mixer.

Table 7.2 illustrates the comparison of some previously published low power mixers and this work. Of all the listed work, our phase detector has the lowest power consumption as 48µW and highest figure of merit of 27.2 dB using simulation results.

Ref.	Process	Frequency (GHz)	NF (dB)	Gain (dB)	IIP3 (dBm)	Power (mW)	FOM (dB)
[70]	0.18µm CMOS	2.4	12.9	15.7	1	8.1	11.3
[71]	0.13µm CMOS	2.1-3	14.8	5.4	-2.8	1.6	9.45
[72]	0.18µm CMOS	0.3-4	14	11	4.1	6.6	10.3
[73]	0.18µm CMOS	2.45	16	13.3	-1	7.2	6.6
[74]	0.18µm CMOS	5.25	24.5	8.3	0.03	4.96	-2.28
[75]	0.18µm CMOS	0.5-7.5	15	5.7	-5.7	0.48	13.2
this work	0.13µm CMOS	2.2	26.5	8	23	0.048	27.2

Table 7.2: The performance comparison of this work and some previous published low power mixer.

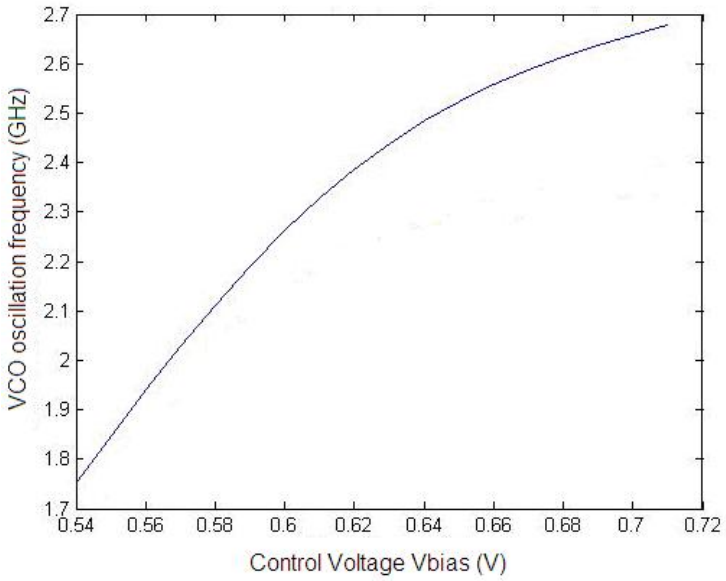


Fig. 7.7: The relationship between the VCO control voltage V_{bias} and the VCO oscillation frequency.

Fig. 7.7 shows the simulation result of the current starved ring oscillator. The relationship between the VCO control voltage V_{bias} and the VCO oscillation frequency is pretty linear from 1.7GHz to 2.5GHz, which is sufficient for operation for the PLL working frequency. The power consumption of the VCO is 207μW.

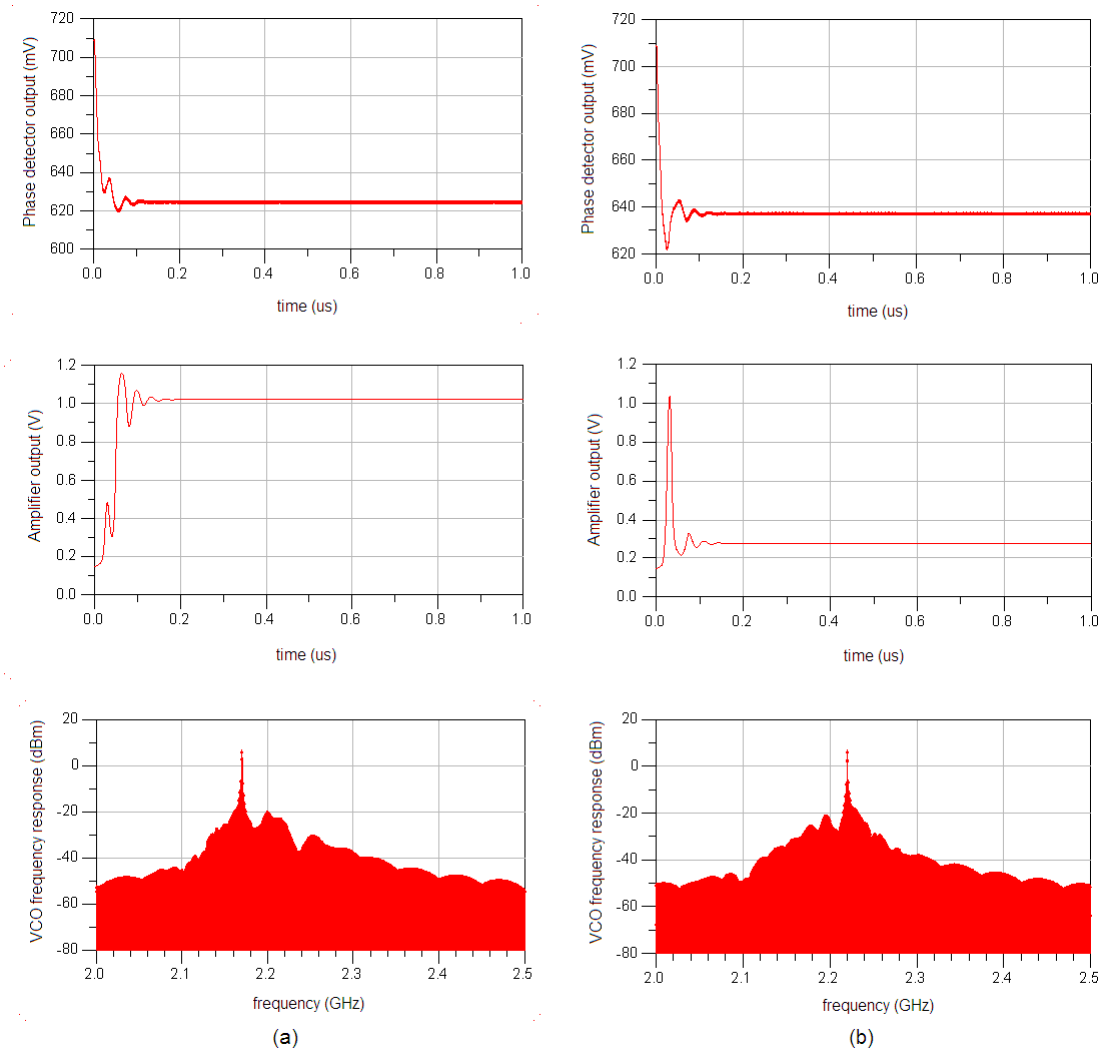


Fig. 7.8: Simulation results of the PLL with single frequency input signals: (a) The input signal has a frequency of 2.17GHz; (b) The input signal has a frequency of 2.23GHz.

With a fixed bias voltage V_{ctrl} at 0.6V in Fig. 7.2, the PLL has a single frequency lock-in range of 50MHz from 2.17GHz to 2.23GHz shown in Fig. 7.8. The three figures on the left are the simulation results when the frequency of the input signal is 2.17GHz. The three figures on the right are simulation results for the input signal of 2.23GHz. For both frequencies, the PLL manages to lock to its input frequency in 100ns. The amplifier output shows high as 1V for 2.17GHz input and low as 0.3V for 2.23GHz input. The VCO output frequency tracks the input frequency accurately.

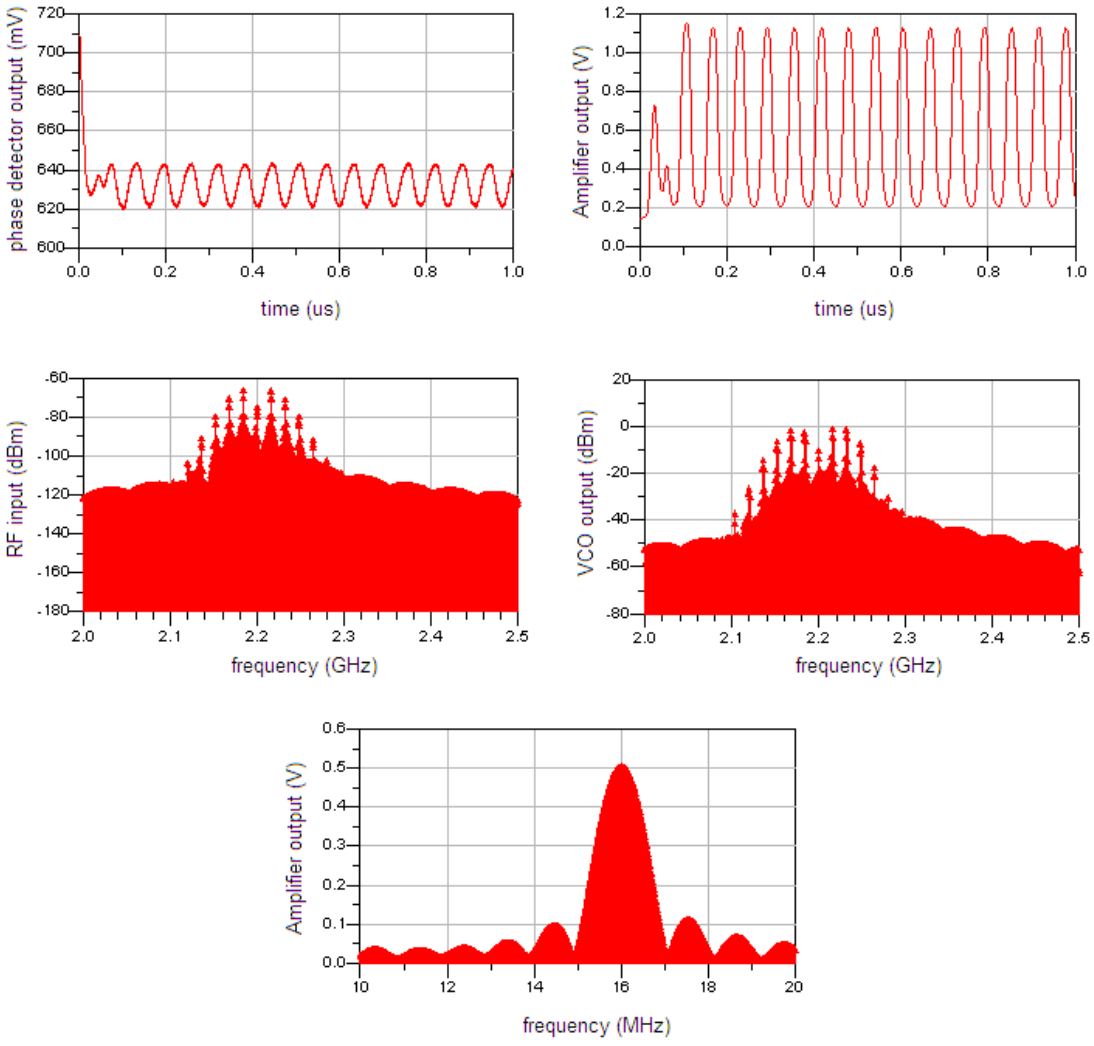


Fig. 7.9: Simulation results when the input signal is a sinusoidal frequency modulated RF signal.

Besides the single frequency locking simulation, the PLL is also simulated with a 16MHz sinusoidal frequency modulated RF input. The simulation results are shown in Fig. 7.9. Both the phase detector and the amplifier show sinusoidal output in less than 100ns same as the frequency modulation. The RF input and the VCO output shows same frequency response, which demonstrates the successful locking of the PLL. The amplifier output frequency response has the most significant harmonic at 16MHz, which expresses the frequency modulation information.

7.1.3 Layout and Experimental Results

The layout of the PLL with output amplifier is shown in Fig. 7.10. Part A is the phase detector and part B is the current starved voltage controlled oscillator. A common drain amplifier buffer in Part C is added at the VCO output for output impedance matching. Part D is the output amplifier.

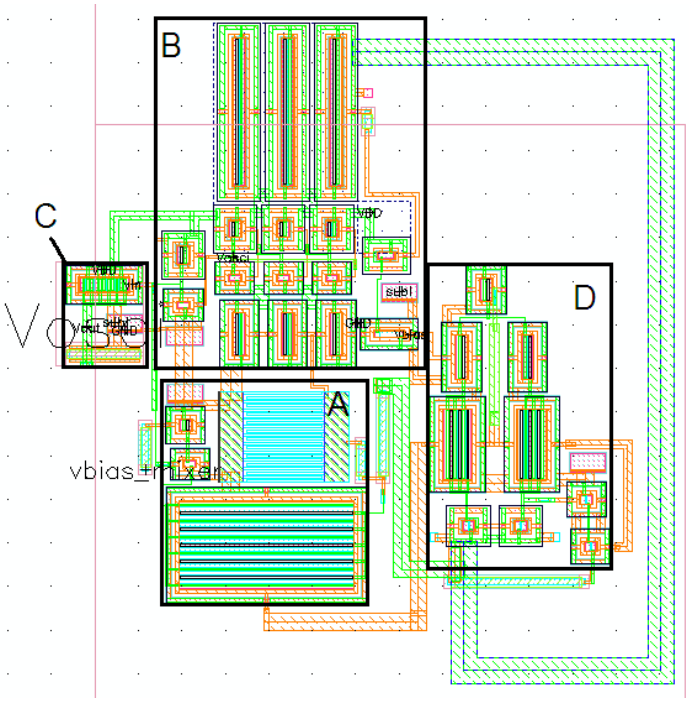


Fig. 7.10: The layout of the designed PLL with output amplifier.

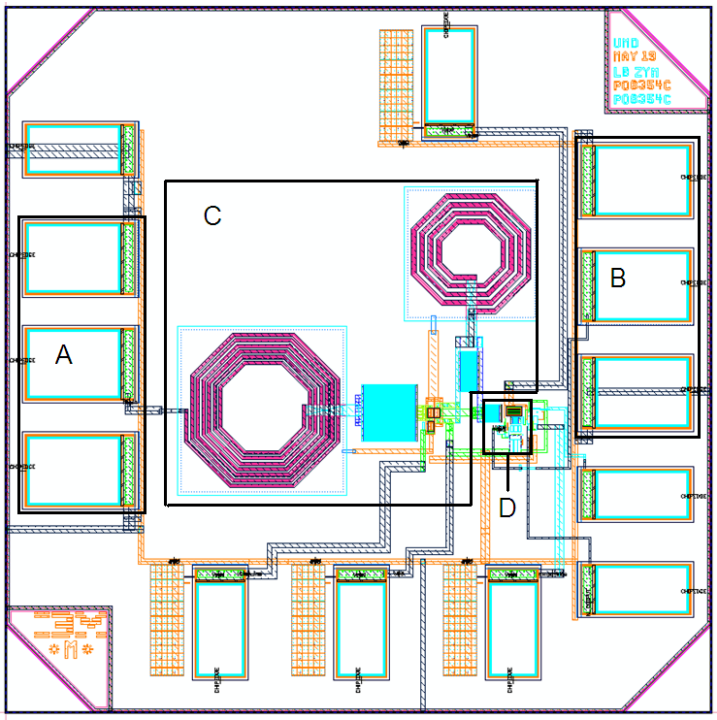


Fig. 7.11: The whole chip layout of the low power 2.2GHz FM receiver.

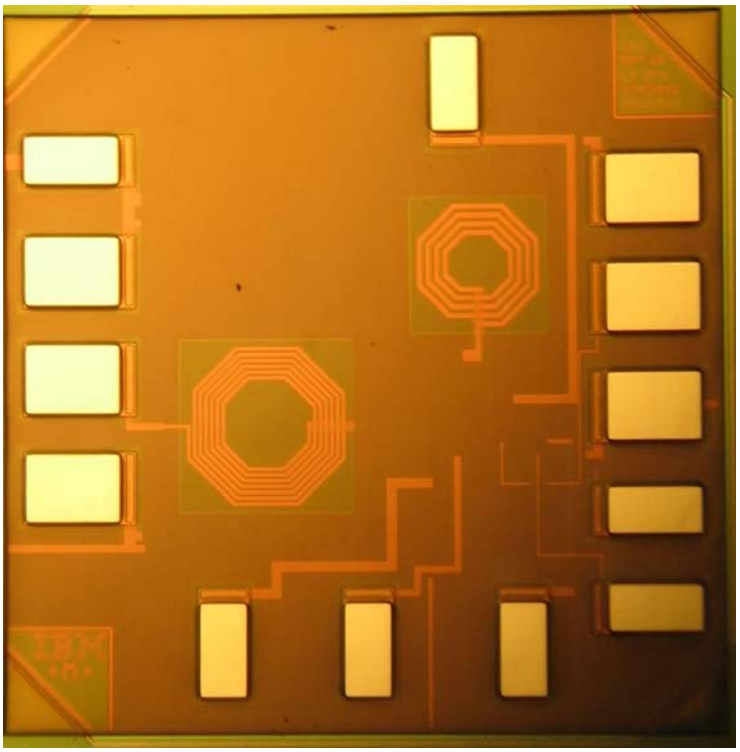


Fig. 7.12: The microphotograph of the low power 2.2GHz FM receiver.

A 2.2GHz custom designed LNA is included in the layout of the FM receiver chip for amplifying and input impedance matching. Previous experimental results show that the LNA has a 25dB gain at 2.2GHz with 3.3dB noise figure. Fig. 7.11 shows the whole chip layout of the FM receiver. Part A and part B are GSG pads for the -60dBm RF input signal and VCO output signal. Part C is the common source cascode LNA with two giant inductors. Part D is the designed PLL with amplifier. The chip is a 1mm by 1mm chip in 0.13µm IBM 8RF LM CMOS process. The PLL has a chip area of 75µm by 45µm. The total power consumption of the PLL is only 0.26mW. The microphotograph of the chip is shown in Fig. 7.12.

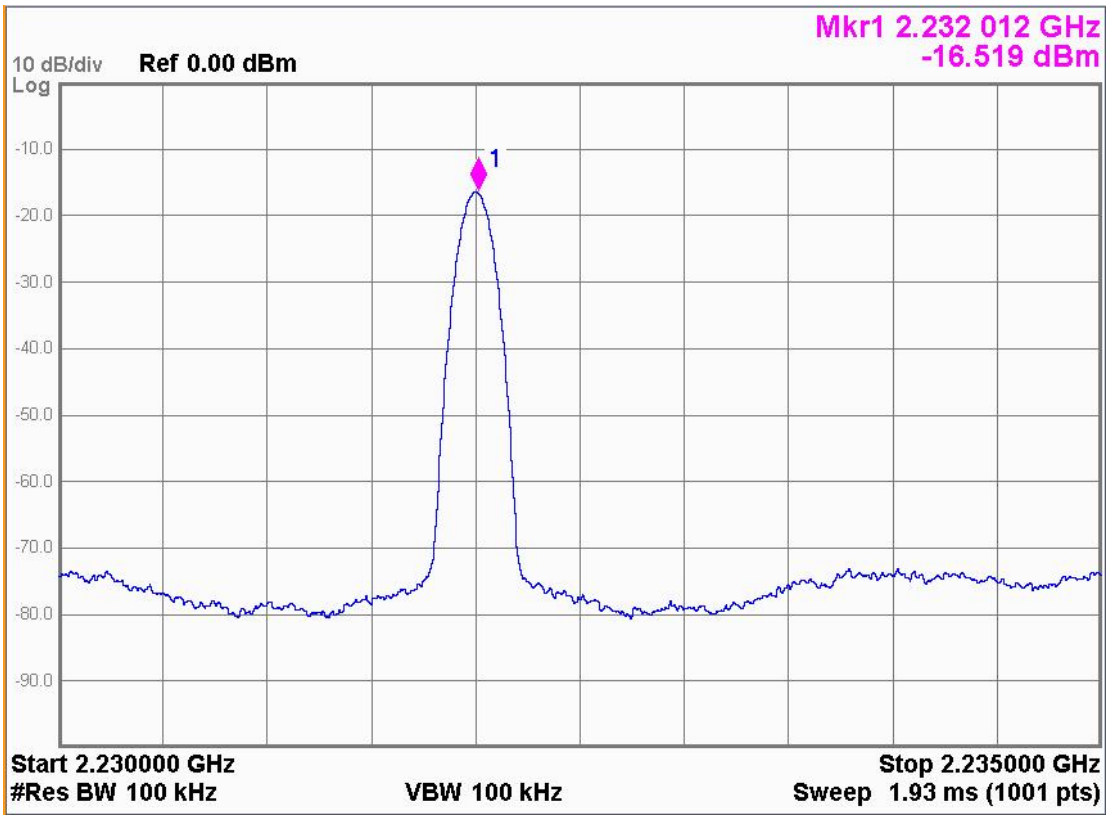


Fig. 7.13: Measured VCO output spectrum of the PLL with a -60dBm 2.232GHz RF input.

The -60dBm RF input signal is fed into the LNA on the chip using Agilent E8267D signal generator. And the VCO output is tested by the MXA N9020A spectrum analyzer. The test results have been presented in [69]. We first test the chip with a single frequency RF input. Fig. 7.13 shows the measured spectrum of the VCO output of the PLL with a 2.232GHz input. The VCO output tracks the frequency information of the RF input at 2.232GHz. The power of the output signal -16dBm agrees with simulation. The phase noise is -113dBc/Hz at offset 1MHz and comparable with other PLLs [41][44][47][48][49] implemented using LC oscillators.

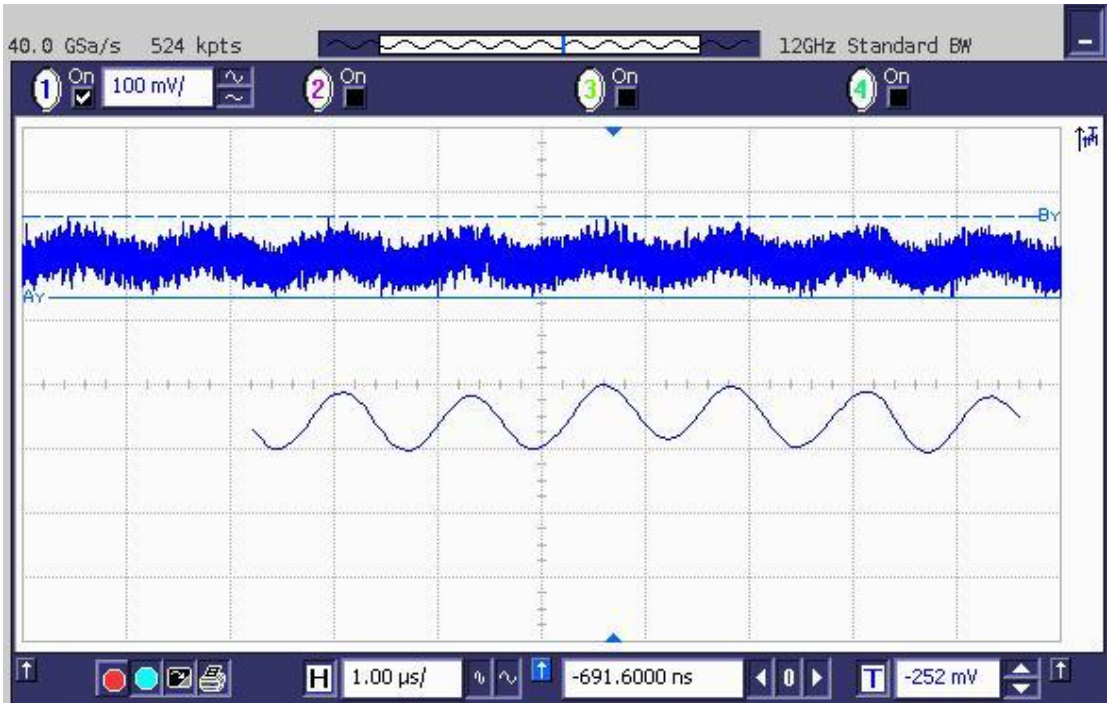


Fig. 7.14: Measured amplifier output with time before and after a 1MHz low pass filter with an 800kHz modulated 2.23GHz RF input.

Then the chip is tested with a 2.23GHz input signal with frequency modulation. The Tektronix TDS7404 oscilloscope is used to test the amplifier output. The noisy signal on the top in Fig. 7.14 is the demodulated output from the amplifier. With the

help of a device built-in 1MHz low pass filter, the clean signal is shown on the bottom in Fig. 7.14. We also use the spectrum analyzer to observe the phase detector output directly when the input is a 1MHz frequency modulated signal at 2.23GHz. Fig. 7.15(a) is the background when no signal is connected to the spectrum analyzer. And the phase detector output is shown in Fig. 7.15(b). Since the impedance is not matched to facilitate measurement, great loss is seen in the gain of the 1MHz harmonic. However, the harmonic 1MHz is still dominant and can be clearly seen on the screen, demonstrating the success of frequency demodulation [69].

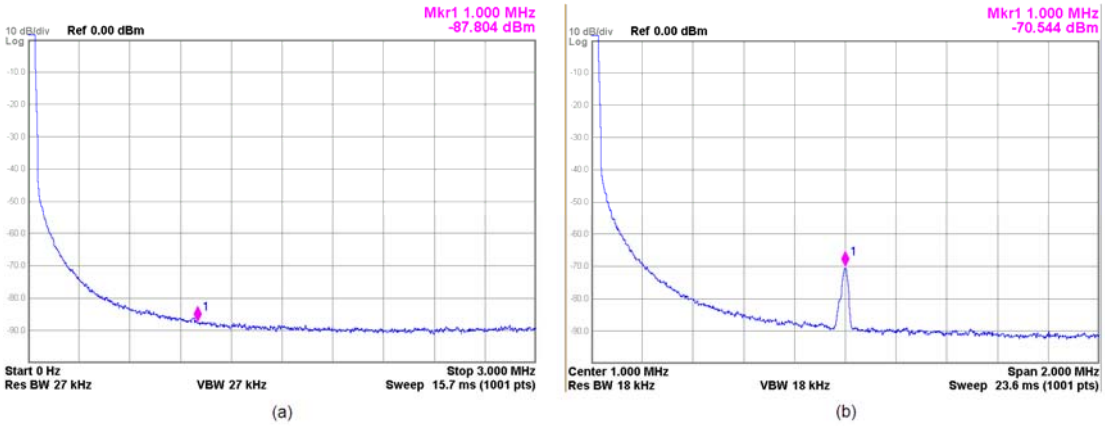


Fig. 7.15: Measured spectrum of the phase detector output with a 1MHz modulated 2.23GHz input.

7.1.4 Summary

We have described an ultra low power phase locked loop for wireless communication at 2.2GHz. The designed PLL can be used with a LNA and an output amplifier to form a FM receiver. A single branch phase detector is used in the PLL because only one current is used for mixing, amplifying and filtering the input signals and the power dissipation greatly reduced. The current-starved CMOS ring oscillator

is used as a VCO because of its low power consumption, wide output range and compact size.

The simulation results have been presented to demonstrate the success of frequency demodulation. The power consumption of the PLL is 260μW, which is much smaller than current published PLLs in bluetooth frequency range. We have also presented a chip layout in IBM 8RF LM 0.13μm CMOS technology. The area of the low power PLL is about 0.003mm^2. The experimental results show that the FM receiver in use of the designed PLL has a lock-in frequency range of 90MHz around 2.2GHz. Both the lock-in frequency range and the center lock frequency can be tuned by the bias voltage V_{ctrl} in the phase detector. Successful sinusoidal frequency demodulation and comparably low phase noise at the VCO output have been observed in the test.

7.2 A Low Power 20GHz Phase Locked Loop used for BFSK Receiver

7.2.1 Overview

A low power 2.2GHz phase locked loop has been designed in section 7.1 and its application as a FM receiver has been explored. The circuit has low power consumption and high integration and can be used for smart dust communication. However, one important requirement of the smart dust network is the compactness of the transceivers. The antenna is a significant part of the transceiver and its size is usually much larger than the integrated circuits. In order to minimize the antenna size, a higher frequency wireless communication network is preferred. In this section, a low power phase locked loop at 20GHz is presented with its application as a binary

frequency shift keying (BFSK) receiver. The higher frequency band provides the possibility of not only compact antenna, but also high data rate communication in short range. With the communication frequency pushed to 20GHz, more unused frequency ranges are available with less interference.

A current-starved CMOS ring oscillator has been used in both OOK and FSK 2.2GHz transceiver designs. The circuit has great advantages in compact size, low power and larger output range. However, as illustrated in Chapter 6, the structure is not applicable for 20GHz communication because its oscillation frequency has an upper limit around 7GHz in the available 0.13μm IBM 8RF process. An LC oscillator is necessary for the design at 20GHz. The cross-coupled LC oscillator is a popular structure in VCO design. Some analysis has been done for this structure for better understanding.

7.2.2 Analysis of a Cross-coupled LC Oscillator

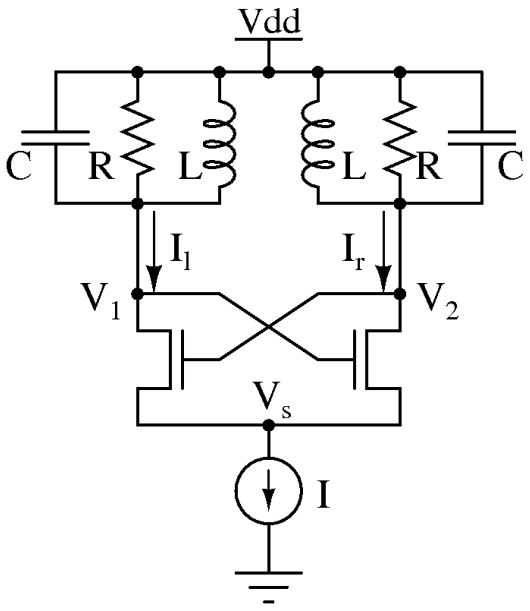


Fig. 7.16: The schematic of a cross-coupled LC oscillator.

Fig. 7.16 shows the schematic of a cross-coupled LC oscillator. The circuit is made up of two non-ideal LC tanks, with two cross-coupled identical NMOS transistors in a differential pair. Assume the transconductance of the two identical NMOS transistor are both g_m . The oscillation requirement will be evaluated in this section from three perspectives. We first start with a feedback perspective, and then discuss the circuit from an energy perspective. Finally we illustrate it from a negative conductance perspective using small signal approximation.

7.2.2.1 Feedback

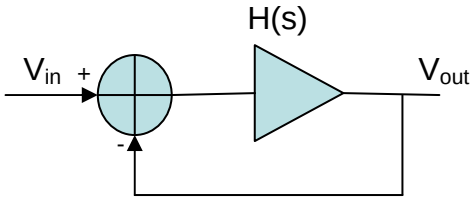


Fig. 7.17: A negative feedback system.

Consider the negative feedback circuit shown in Fig. 7.17, where

$$\frac{V_{out}}{V_{in}}(s) = \frac{H(s)}{1+H(s)} \tag{7.11}$$

The Barkhausen criteria [76] tell us that if the negative-feedback circuit has a loop gain that satisfies two conditions:

$$|H(j\omega_0)| \geq 1 \qquad \angle H(j\omega_0) = 180° \tag{7.12}$$

Then the circuit may oscillate at ω_0. Actually if we factor the negative feedback to phase, the loop has a total phase shift of 360°.

Now we reconsider the LC oscillator in Fig. 7.16, the source of the two NMOS transistors V_s can be treated as an AC virtual ground. Therefore, the circuit can be redrawn as in Fig. 7.18.

At resonance frequency $\omega = \frac{1}{\sqrt{LC}}$, the phase shifts by the load L and C cancel each other. The total phase shift of the feedback loop is 360° because of two negative gains in the loop. In order to satisfy the Barkhausen criteria, the loop gain must meet the following requirement:

$$(-g_m R)^2 \geq 1 \Rightarrow g_m R \geq 1 \tag{7.13}$$

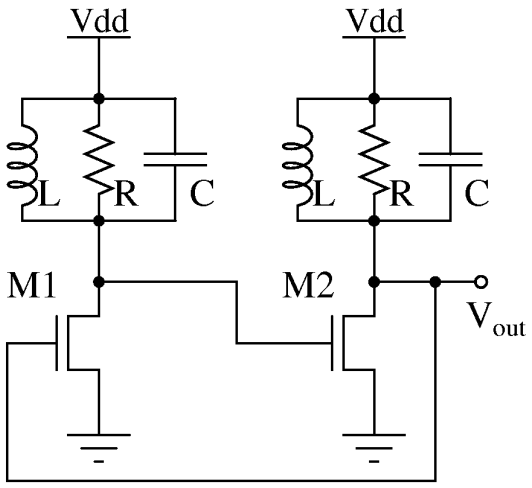


Fig. 7.18: The cross-coupled LC oscillator circuit redrawn in feedback perspective.

7.2.2.2 Energy

In order to analyze the cross-coupled LC oscillator circuit in Fig. 7.16 from an energy prospective, we start with the currents flowing in each branch of the circuit. The currents on the left tank capacitor, resistor and inductor are defined as I_{Ll}, I_{Rl} and

I_{Cl} flowing from V_{dd} to V_1 respectively. The currents on the right tank capacitor, resistor and inductor are defined as I_{Lr} , I_{Rr} and I_{Cr} flowing from V_{dd} to V_2 respectively.

For DC analysis, inductors can be taken as short circuits. The two identical transistors have the same bias current $I/2$ flowing through them and the DC bias of the output voltages has the following relationship.

$$V_1 = V_2 = V_{dd} \tag{7.14}$$

For AC analysis, the output V_1 and V_2 are sinusoidal signals with opposite phase. Now Let us consider both AC and DC signals and assume

$$V_1 = A\sin(\omega t + \phi) + V_{dd} \tag{7.15}$$

Here A is the amplitude of the output signal V_1, ω is the angular frequency and ϕ is the phase of it. Then

$$V_2 = -A\sin(\omega t + \phi) + V_{dd} \tag{7.16}$$

The currents on the capacitors can be obtained as

$$I_{Cl} = C\frac{d(V_{dd} - V_1)}{dt} = -AC\omega\cos(\omega t + \phi) \tag{7.17}$$

$$I_{Cr} = C\frac{d(V_{dd} - V_2)}{dt} = AC\omega\cos(\omega t + \phi) \tag{7.18}$$

The currents on the resistors can be written as

$$I_{Rl} = \frac{V_{dd} - V_1}{R} = -\frac{A}{R}\sin(\omega t + \phi) \tag{7.19}$$

$$I_{Rr} = \frac{V_{dd} - V_2}{R} = \frac{A}{R}\sin(\omega t + \phi) \tag{7.20}$$

And the currents flowing in the inductors can be expressed as

$$I_{Ll} = \frac{1}{L}\int (V_{dd} - V_1)dt = \frac{A}{L\omega}\cos(\omega t + \phi) + \frac{I}{2} \tag{7.21}$$

$$I_{Lr} = \frac{1}{L}\int (V_{dd} - V_2)dt = -\frac{A}{L\omega}\cos(\omega t + \phi) + \frac{I}{2} \tag{7.22}$$

When $\sin(\omega t + \phi) = \pm 1$, all the dynamic energy is store in the two capacitors because both the capacitors have been charged to its maximum voltage difference. When $\sin(\omega t + \phi) = 0$, all the dynamic energy is stored in the two inductors.

When $\sin(\omega t + \phi) = 1$, the output V_1 is at its maximum of $(V_{dd} + A)$ and the output V_2 is at its minimum of $(V_{dd} - A)$. The currents I_{Cl} and I_{Cr} on the capacitors are both zero and the currents I_{Ll} and I_{Lr} on the inductors are both $I/2$. The currents flowing in the left and right resistors are $-A/R$ and A/R respectively. Assume the two NMOS transistors are operating in saturation region, and according to the Kirchoff's current law, the currents flowing in the two transistors can be formulated as

$$I_l = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{dd} - A - V_s)^2 = \frac{1}{2}I - \frac{A}{R} \tag{7.23}$$

$$I_r = \frac{1}{2}\mu C_{ox}\frac{W}{L}(V_{dd} + A - V_s)^2 = \frac{1}{2}I + \frac{A}{R} \tag{7.24}$$

If we divide equation (7.23) by equation (7.24), such relationship can be obtained as

$$\frac{(V_{dd} - A - V_s)^2}{(V_{dd} + A - V_s)^2} = \frac{IR - 2A}{IR + 2A} \tag{7.25}$$

The amplitude A of both the outputs V_1 and V_2 can be derived from equation (7.25) as

$$A^2 = IR(V_{dd} - V_s) - (V_{dd} - V_s)^2 \geq 0 \tag{7.26}$$

Where V_s is the source voltage shown in Fig. 7.16. The inequality in equation (7.26) gives us

$$\frac{I}{V_{dd} - V_s} R \geq 0 \Rightarrow g_m R \geq 1 \tag{7.27}$$

7.2.2.3 Negative conductance

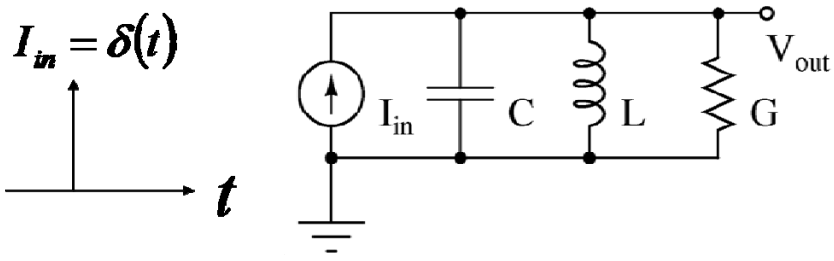


Fig. 7.19: A non-ideal LC tank with conductance G.

Now we analyze the cross-coupled LC oscillator in a negative conductance perspective. We first illustrate why a negative conductance is necessary for a non-decaying oscillation. Consider a LC tank with a conductance G shown in Fig. 7.19. Assume the input current I_{in} is an impulse, in Laplace domain the voltage output of the circuit can be expressed as

$$V_{out}(s)=\frac{Ls}{LCs^2+LGs+1}=\frac{\frac{s}{C}}{\left(s+\frac{G}{2C}\right)^2+\frac{1}{LC}-\frac{G^2}{4C^2}} \tag{7.28}$$

When $\frac{1}{LC}-\frac{G^2}{4C^2}>0$, we assume

$$\alpha=-\frac{G}{2C} \quad \omega^2=\frac{1}{LC}-\frac{G^2}{4C^2} \tag{7.29}$$

Then the time domain voltage output can be expressed as

$$V_{out}(t)=\frac{1}{C}e^{\alpha t}\cos(\omega t)+\frac{\alpha}{C\omega}e^{\alpha t}\sin(\omega t) \tag{7.30}$$

For a non-decaying oscillation, the power of the exponential term must be equal or greater than zero. Therefore, the conductance G must be zero or negative.

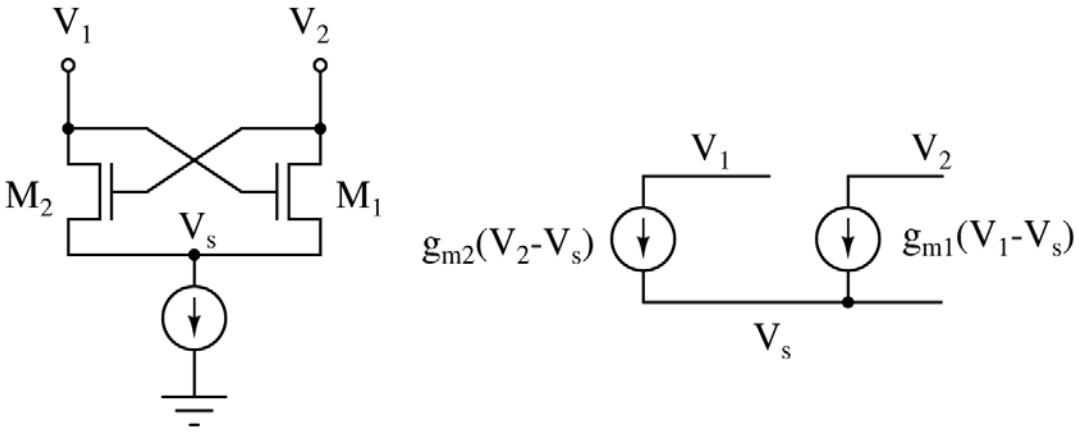


Fig. 7.20: Small signal equivalent circuit of the transistors in the cross coupled LC oscillator.

Let's go back to the cross coupled LC oscillator circuit shown in Fig. 7.16. The small signal equivalent circuit of the two cross coupled NMOS transistors is shown in Fig. 7.20. This part of the circuit is a negative resistance which is used to balance the

inherent resistance on the LC tank to generate non-decaying oscillation. The proof is shown below.

If we define the equivalent voltage as $V = V_1 - V_2$, then the equivalent small signal current I from V_1 to V_2 can be expressed as

$$I = g_{m2}(V_2 - V_s) = -g_{m1}(V_1 - V_s) \tag{7.31}$$

The equivalent resistance of this part of the circuit is calculated as

$$\begin{aligned} \frac{V}{I} &= \frac{V_1 - V_2}{I} = \frac{V_1 - V_s}{I} - \frac{V_2 - V_s}{I} \\ &= \frac{V_1 - V_s}{-g_{m1}(V_1 - V_s)} - \frac{V_2 - V_s}{g_{m2}(V_2 - V_s)} \\ &= -\frac{1}{g_{m1}} - \frac{1}{g_{m2}} = -\frac{2}{g_m} \end{aligned} \tag{7.32}$$

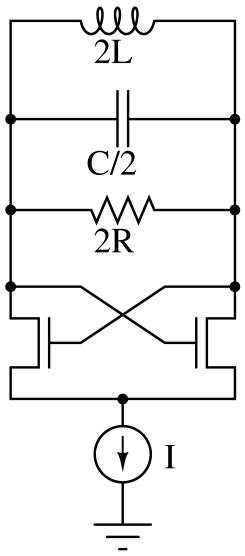


Fig. 7.21: The cross-coupled LC oscillator equivalent circuit for negative conductance analysis.

In small signal analysis, the cross-coupled LC oscillator circuit can be redrawn in Fig. 7.21. According to the negative conductance requirement of non-decaying oscillation, the conductance of the circuit must obey the following rules.

$$-\frac{g_m}{2}+\frac{1}{2R}\le 0 \Rightarrow g_m R \ge 1 \tag{7.33}$$

In summary, we have analyzed the oscillation requirement of the cross coupled LC oscillator from feedback, energy and negative conductance perspective and obtain the same conclusion in equations (7.13) (7.27) and (7.33). The multiplication of the transconductance of the NMOS transistor and the inherent resistance of the LC tank must be equal or greater than one to trigger the circuit to oscillate.

7.2.3 Circuit Design

The diagram of the PLL used for FM receiver has been shown in section 7.1. The designed low power PLL for 20GHz BFSK receiver has the same structure as its 2.2GHz alternative. However, since binary frequency shift keying is used in this design, the output of the receiver should be digitized to differentiate the transmitted zeros and ones. The circuit design of each block is presented below.

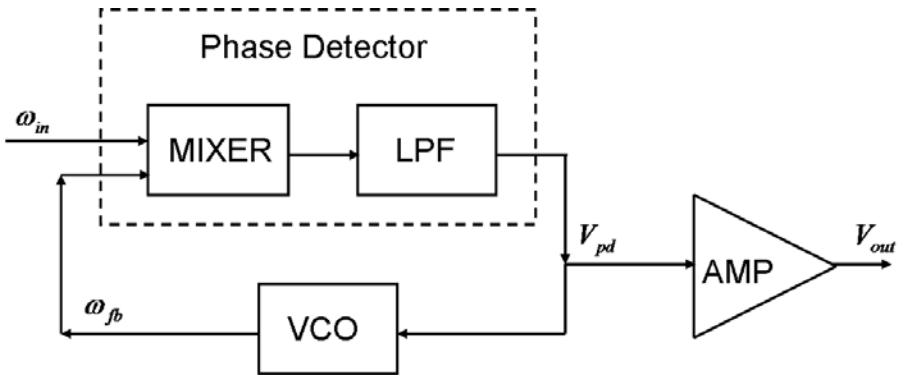


Fig. 7.22: The block diagram of a PLL and output amplifier used for FM receiver. (shown in section 7.1 as Fig. 7.1).

7.2.3.1 Voltage controlled oscillator

Fig. 7.22 shows the circuit schematic of the voltage controlled oscillator (VCO) in the low power 20GHz PLL. 0.13μm IBM 8RF dual metal technology is used in this design. An MA metal option consisting of additional thick dielectric and metal layers above the basic CMOS back of the line option is applied in designing inductors with low resistance and low parasitic capacitance. The tunable capacitors are implemented by a thin oxide NFET in an N-well with N+ source and drains shorted together. The inductance is first selected with largest quality factor around 20GHz. The capacitance is chosen afterwards by relating the inductance to the frequency. Since it is a circuit operating at 20GHz, parasitic capacitance might be dominant. Actually, the gate capacitance of the two cross-coupled transistors must be counted in the design of the tunable capacitors.

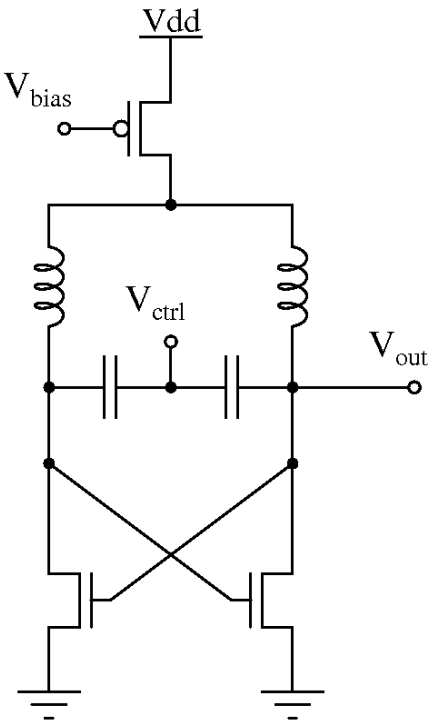


Fig. 7.23: The circuit schematic of the VCO for the low power 20GHz PLL.

The circuit is biased on the top instead of on the bottom as usual in Fig. 7.16. As analyzed in section 7.2.2, the output of the LC oscillator in Fig. 7.16 has DC offset around the power voltage Vdd. If that structure is used in implementing the PLL, a power consuming AC coupling structure is necessary for connecting the output around Vdd to the input of the phase detector. In contrast, top biasing shifts the output signal of the VCO from Vdd to the middle of Vdd, which make it easier for the phase detector to take as the input. Even without the power consideration of the AC coupling circuit, the LC oscillator with bottom biasing dissipates more power than the circuit with top biasing. This is probably due to the idea that it may take more power for a circuit to shoot over the power voltage Vdd.

7.2.3.2 Phase detector

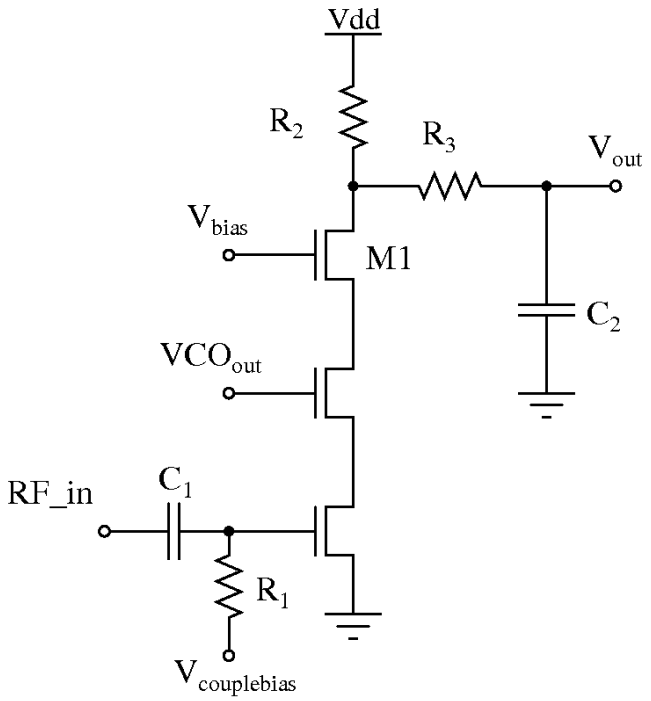


Fig. 7.24: the schematic of the phase detector circuit used in low power 20GHz PLL.

The same structure phase detector is used in this design as in 2.2GHz application shown in section 7.1. Fig. 7.24 shows the schematic of the phase detector circuit. It is made up of a single branch mixer and a low pass filter. The large cascode transistor M1 in Fig. 7.24 helps block and filter out high frequency harmonics and reuses the current from Vdd to save power. Both the RF input from LNA and VCO output are fed into transistor gates for large input impedance. The bias voltage $V_{coouplebias}$ of the AC coupling determines the DC current flowing in the branch, and determines the power consumption of the phase detector. It also provides the possibility of changing the center lock-in frequency of the PLL by varying the output DC voltage of the phase detector. Again parasitic capacitances cannot be ignored while designing the capacitor C_2 of the low pass filter. Gate capacitance of the later stage output amplifier must be considered for calculation.

7.2.3.3 Output amplifier

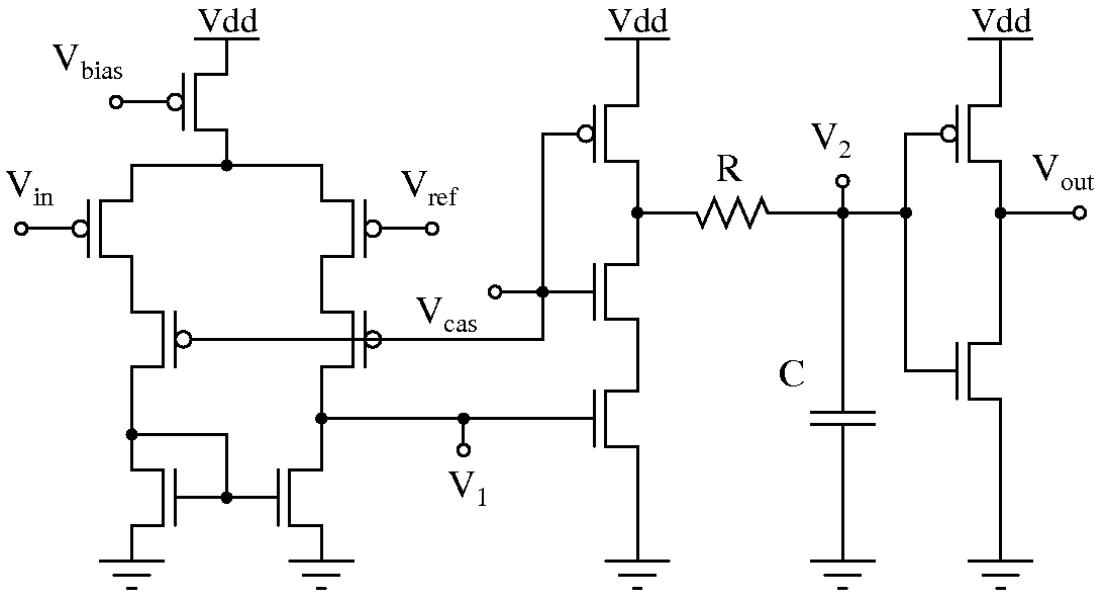


Fig. 7.25: The schematic of the output amplifier used in the low power 20GHz BFSK receiver.

The output amplifier is composed of a two-stage cascode common-source amplifier with a low pass filter and an inverter to generate rail to rail output. The cascode structure enlarges the operation bandwidth of the circuits. The low pass filter reduces the ripples on the output signal before the inverter stage to avoid false data bits. And the inverter itself amplifies and digitizes the signal.

7.2.4 Simulation Results and Layout

The low power PLL with output amplifier is simulated with 0.13µm IBM 8RF DM technology using the RFDE simulator of Cadence software. The simulation results of each circuit block and the total PLL will be presented in this section.

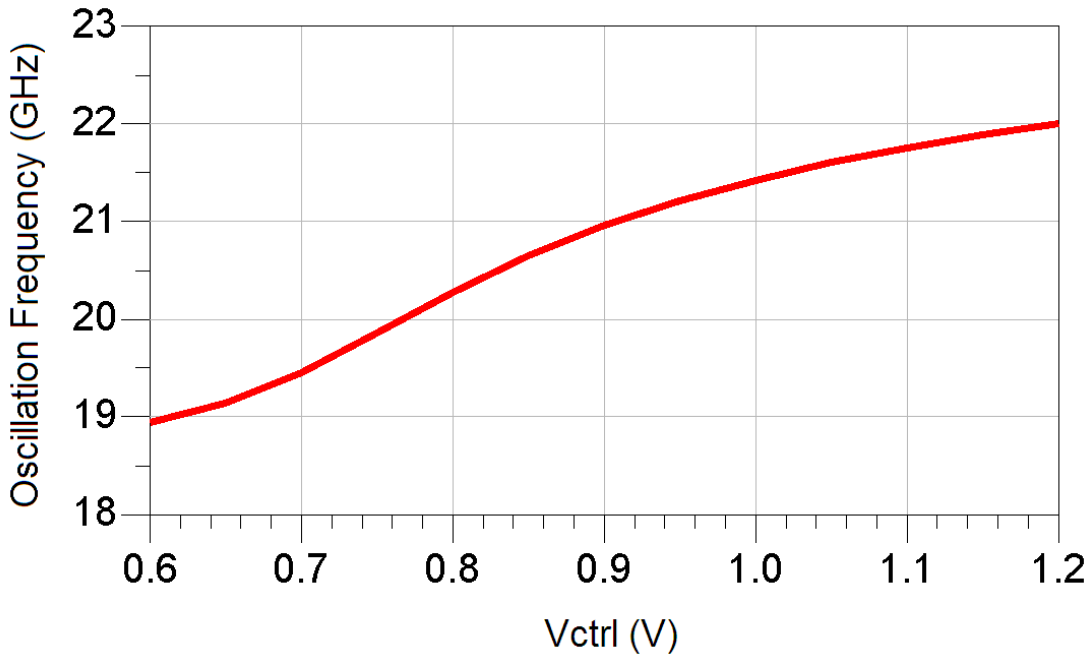


Fig. 7.26: The simulated relationship between the control voltage and the oscillation frequency of the cross-coupled LC oscillator.

The cross coupled LC oscillator is simulated with a sweep of control voltage from 0.6V to 1.2V. Compare to the DC voltage Vdd=1.2V on the other end of the

tunable capacitors, the gate to diffusion voltage drop is changed from 0.6V to 0V, which takes the silicon surface in the Nwell under the gate from accumulation to depletion. Therefore the capacitance decreases with the control voltage V_{ctrl} in Fig. 7.23 and the oscillation frequency increases with the control voltage V_{ctrl} . The simulated relationship between the control voltage V_{ctrl} and oscillation frequency is shown in Fig. 7.26. The linearity around the 20GHz is good enough for operation. The power consumption of the cross-coupled LC VCO is 1.75mW.

freq	Vout
0.00000 Hz	0.8556 / 0.0000
5.0000 MHz	0.0050 / 115.8866
10.000 MHz	2.4143E-6 / 149.8255
15.000 MHz	1.2596E-8 / -137.7468
20.000 MHz	7.9212E-11 / -56.4971
25.000 MHz	3.0873E-13 / -123.4422
30.000 MHz	8.6375E-15 / -107.0931
35.000 MHz	2.7577E-16 / -117.6220
40.000 MHz	1.5903E-16 / -136.7882
45.000 MHz	7.1325E-17 / -104.0338
50.000 MHz	4.5149E-17 / -177.2320
20.725 GHz	6.1085E-16 / -168.5335
20.730 GHz	2.7461E-13 / -34.4167
20.735 GHz	9.0989E-11 / 80.1731
20.740 GHz	1.5517E-8 / 175.6015
20.745 GHz	4.9273E-5 / -127.1314
20.750 GHz	4.1545E-9 / 57.4819
20.755 GHz	5.9875E-11 / -33.2337
20.760 GHz	4.1967E-13 / 130.7341
20.765 GHz	1.3995E-15 / -164.1246
20.770 GHz	1.5735E-17 / -51.2224
20.775 GHz	1.5032E-17 / 109.2959
20.780 GHz	8.8744E-18 / 108.9650

Table 7.3: The harmonics at different frequencies of the phase detector output when the phase detector is fed with two input signals at 20.745GHz and 20.75GHz.

The phase detector is first simulated with two inputs at different frequencies with the same phase. A 20.75GHz -36dBm RF input signal with 0.4V DC offset and a 20.745GHz sinusoidal signal oscillating from 0.3V to 0.8V are fed into the phase detector as the RF reference input signal and the VCO output. The harmonics at

difference frequencies of the phase detector output is shown in Table 7.3. Of all the frequencies, the harmonic at 5MHz, which is the frequency difference of the two input signal, has the largest value and even the second largest harmonic has magnitude smaller than 1% of it. The simulation results show that the phase detector has good performance in multiplying the input signals and filtering the unwanted high frequency harmonics.

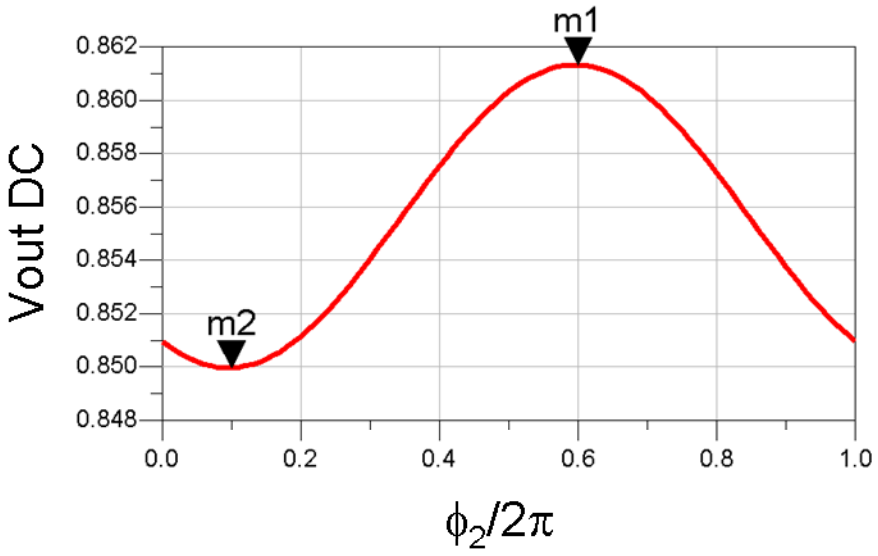


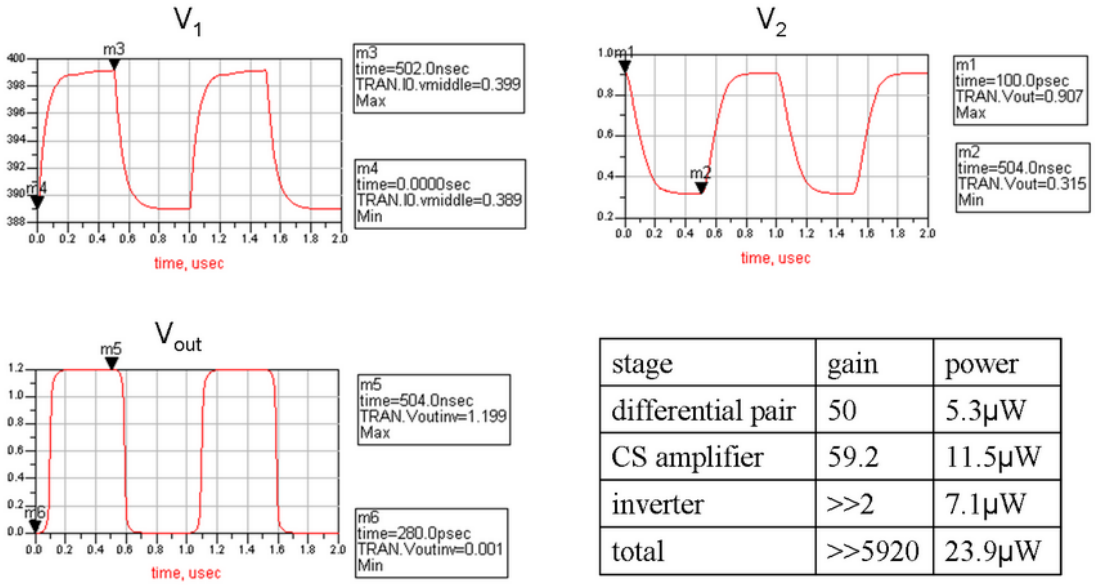
Fig. 7.27: The DC voltage of the phase detector output with the phase difference of the two inputs when the phase detector is connected with two signals at the same frequency with difference phase.

Then the phase detector is simulated with two input signals at the same frequency with difference phase. A 20.75GHz -36dBm RF input signal with zero phase and 0.4V DC offset and a 20.75GHz sinusoidal signal oscillating from 0.3V to 0.8V with phase ϕ_2 are fed into the phase detector as the RF reference input signal and the VCO output. The simulation is a DC sweep of the phase difference ϕ_2. Fig. 7.27 shows the relationship between the phase detector output DC voltage and the phase difference ϕ_2. With the phase difference ϕ_2 varying from 0.1π to 0.6π, the output DC voltage

increases from the minimum to the maximum monotonically as a sine wave. Any phase difference can be converted to any one of the half cycle to keep the monotonicity, so that the phase detector DC output is a good representation of the phase difference. Table 7.4 shows the harmonic list of the phase detector output. The DC component is dominant and any other harmonic is small enough to be neglected. This result again proves the mixing function of the phase detector. The power consumption of the phase detector is only 4.6μW.

freq	Vout
x=0.000	
0.0000 Hz	0.851 / 0.000
20.75 GHz	4.927E-5 / -127.135
41.50 GHz	7.806E-7 / 70.230
62.25 GHz	1.495E-7 / -61.003
83.00 GHz	1.965E-8 / 131.346
103.8 GHz	5.940E-9 / -52.220
124.5 GHz	6.070E-10 / 117.264

Table 7.4: The harmonics at different frequencies of the phase detector output when the phase detector is fed with two input signals at the same frequency 20.75GHz with different phase.



stage	gain	power
differential pair	50	5.3μW
CS amplifier	59.2	11.5μW
inverter	>>2	7.1μW
total	>>5920	23.9μW

Fig. 7.28: Simulation results and performance table of the output amplifier.

The output amplifier is simulated with a 0.2mV peak-to-peak square wave input. With appropriate biasing and referencing, the first stage difference pair generates a voltage gain of 50 at V_1 in Fig. 7.25 with 5.3μW power dissipation. The second stage common source amplifier enlarges the voltage gain further and the last stage inverter pushes the final output to rail to rail from 0 to 1.2V. The simulation results and the performance table of the output amplifier are shown in Fig. 7.28. The total power dissipation of the output amplifier is 23.9μW.

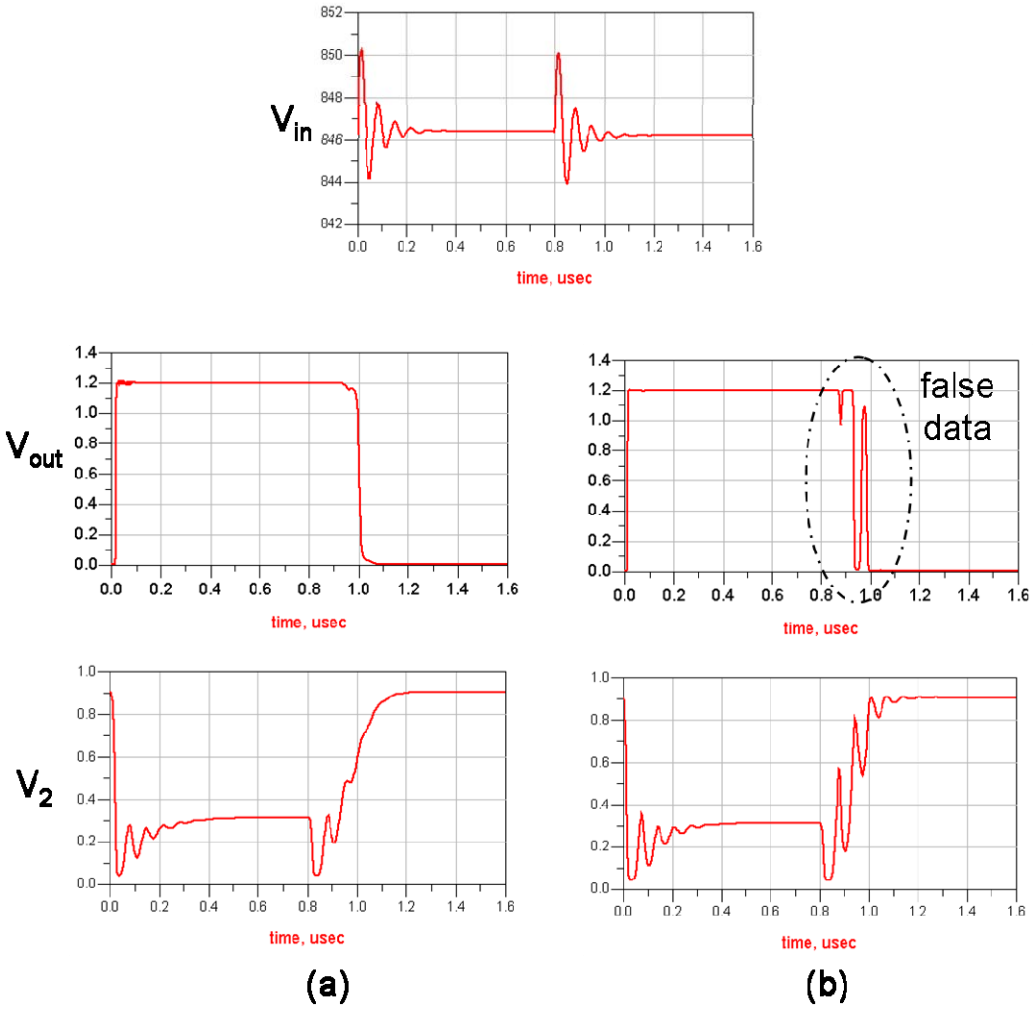


Fig. 7.29: The comparison of the simulation results of the output amplifiers with and without the low pass filter.

Fig. 7.29 shows a typical phase detector output of the circuit on the top. Since the voltage difference between the two states is small, the oscillation ringing during each locking is comparably large. Without the help of the low pass filter shown in Fig. 7.25, the ringing on the voltage is also amplified and generates false data bit after the inverter as shown in Fig. 7.29 (b). The output is clean and accurate after inserting the low pass filter between the second amplifying stage and the inverter as shown in Fig. 7.29 (a).

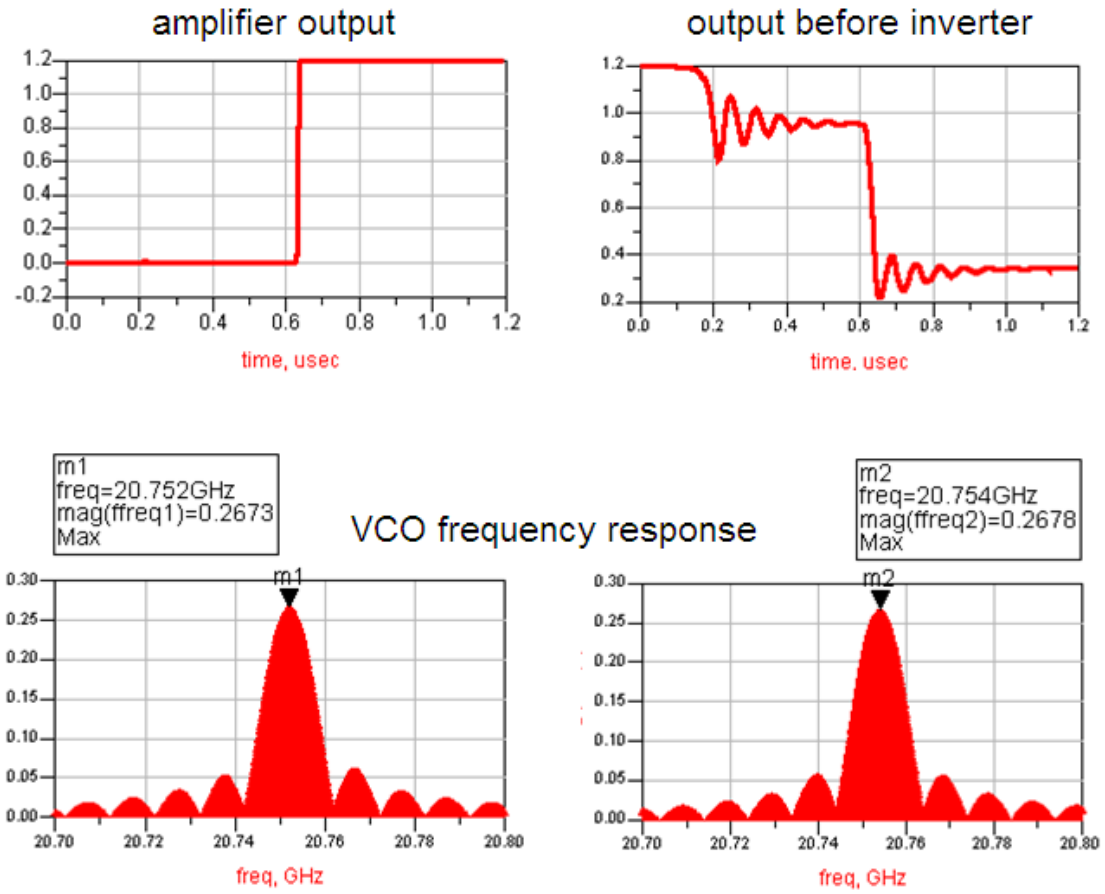


Fig. 7.30: The simulation results of the PLL with amplifier for a -36dBm BFSK input signal with frequency change at 0.6μs from 20.752GHz to 20.754GHz.

The PLL with amplifier is first simulated with single frequency input. When the phase detector is biased the same voltage $V_{couplebias}$, the PLL has a static single frequency lock-in range of 35MHz from 20.719GHz to 20.754GHz for a -36dBm RF input signal. The PLL can trace the frequency in 0.5μs and the power consumption of the PLL with amplifier is only 1.77mW, which is much smaller than the previous PLLs [46-49] at this frequency range.

For BFSK application, not only the static lock-in frequency range is important, the minimum frequency difference the PLL can detect is also a concern. Fig. 7.30 shows the simulation results of the PLL with amplifier for a -36dBm BFSK input signal with frequency change at 0.6μs from 20.752GHz to 20.754GHz. The simulation is only run for 1.2μs because the software must take a lot of samples for a 20GHz signal and a longer time causes Cadence crash during the simulation. The PLL can detect the two different frequencies and show the change at the output rail to rail in digital form. The lock-in time of the PLL is 0.5μs, which means the BFSK receiver in use of the PLL can receive a data rate as high as 2Mbps. With the 35MHz static lock-in frequency range around 20GHz and the 2MHz minimum detection frequency, the PLL can be used in a 17-channel BFSK receiver.

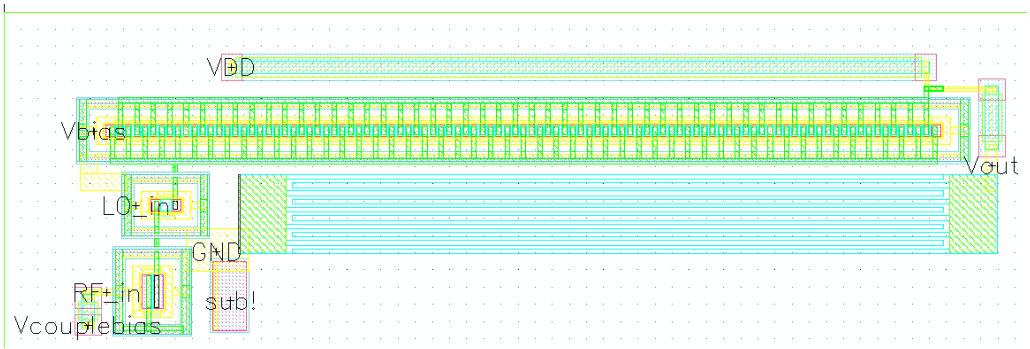


Fig. 7.31: The layout the phase detector.

The PLL is fabricated in the 0.13μm IBM 8RF DM process. A high frequency LNA is added to the design for input signal amplification and impedance matching. The layout of the phase detector and the output amplifier is shown in Fig. 7.31 and Fig 13.17 respectively. The PLL with the output amplifier layout is shown in Fig. 7.33. Both the phase detector and the amplifier are much smaller than the VCO implemented by on-chip giant inductors. All the non-inductor devices are put in the middle of the two inductors for layout symmetry.

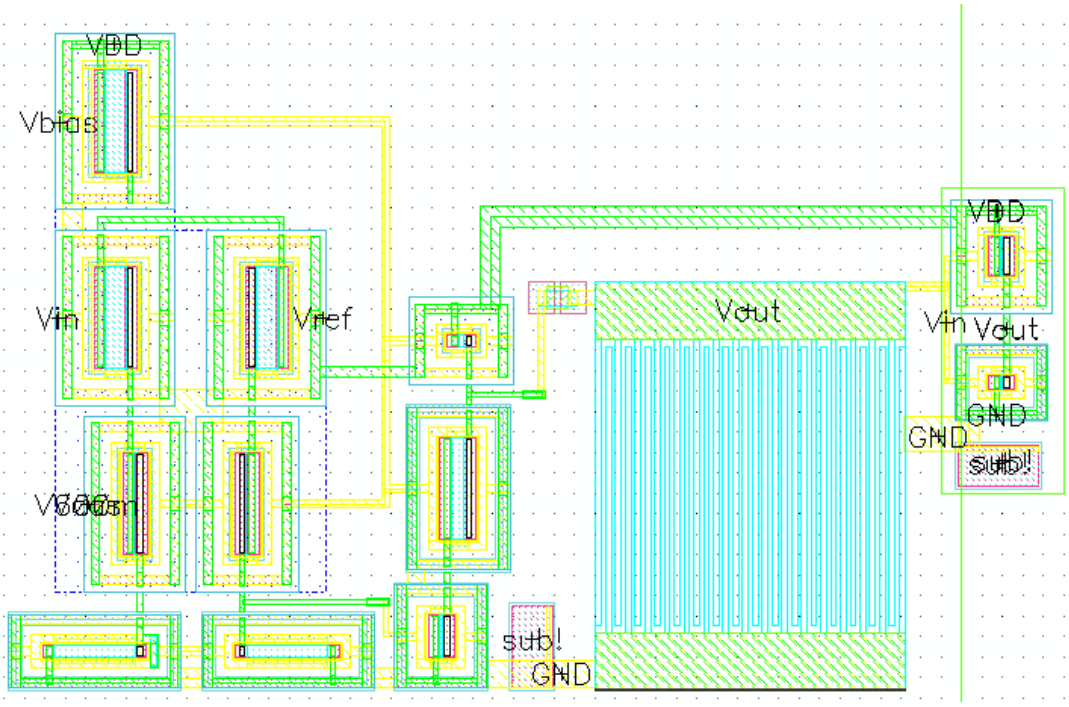


Fig. 7.32: The layout of the output amplifier.

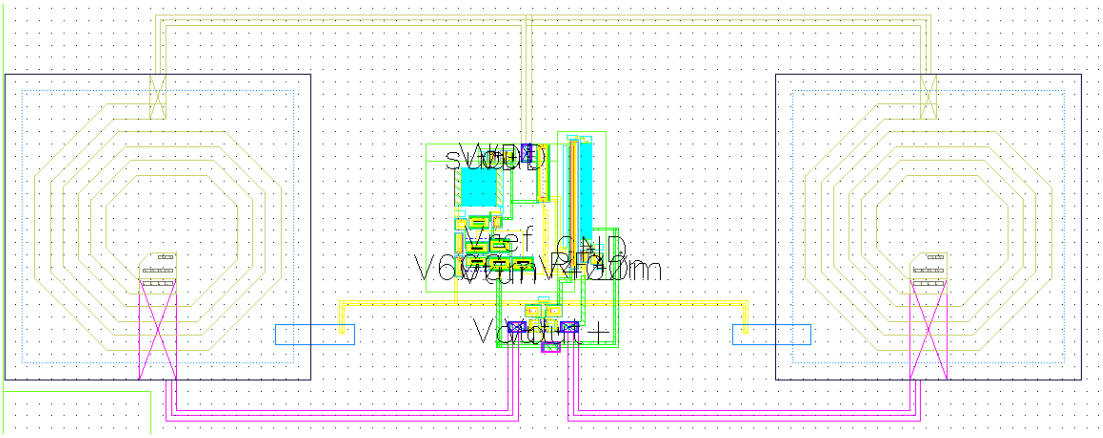


Fig. 7.33: The layout of the PLL with output amplifier.

Fig. 7.34 shows the chip layout of the 20GHz BFSK receiver using the designed PLL. The chip has an area of 2mm by 1mm in the 0.13μm IBM 8RF DM process. Part A is the added three-stage high frequency LNA. Part B is the designed PLL with output amplifier. Part C is the GSG pads for the input signal to the LNA. Part D is a bypass capacitor used for DC pads when necessary.

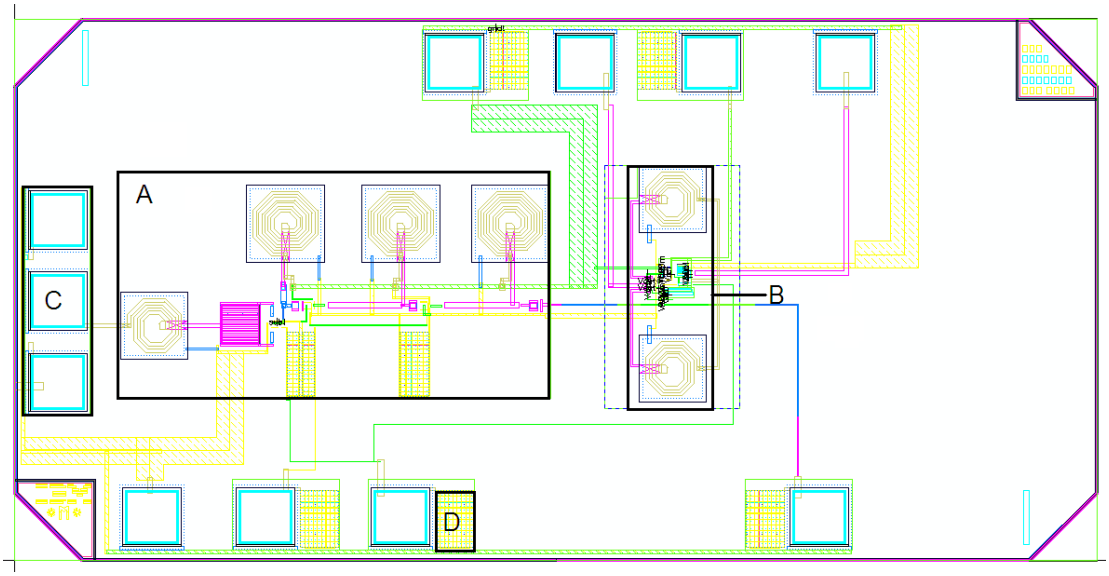


Fig. 7.34: The layout of the total chip.

7.2.5 Summary

We have described an ultra low power phase locked loop for smart dust wireless communication at 20GHz. With the added custom designed LNA, the PLL with output amplifier realize the frequency demodulation function in a BFSK receiver. We chose the single branch structure to implement the phase detector because only one current in this structure is used for mixing, amplifying and filtering the input signals so that the power consumption is greatly saved. The cross-coupled LC oscillator is selected as VCO for its practicability at frequencies as high as 20GHz.

The simulation results have been reported to demonstrate the success of frequency demodulation. The power consumption of the PLL is 1.75mW, which is much smaller than current published PLLs [47][48][49][50] in frequency range around 20GHz. Simulation results show that the PLL can lock from 20.719GHz to 20.754GHz in 0.5μs with 35MHz lock-in frequency range. The output amplifier with large gain is designed to realize 2MHz frequency detection resolution.

We have also presented a chip layout of a BFSK receiver in use of the designed PLL with IBM 8RF DM 0.13μm CMOS technology. A three-stage 20GHz LNA is added to facilitate measurement and amplify the input signal. The BFSK receiver is expected to be able to demodulate 2Mbps signal on a 20GHz carrier with an RF input as small as -60dBm.

7.3 PLL Model Analysis Using Matlab

7.3.1 Traditional Linear Analysis

In the preceding chapters, specific designs of PLLs have been explored in applications of radio frequency low power receivers. Both the 2.2GHz and 20GHz FM receiver structures can be illustrated in the Fig. 7.35. The PLL between the first LNA circuit and the last amplifier stage transforms the frequency variation information of the input signal to voltage variation. A simple PLL is made up of a phase detector and a voltage-controlled oscillator (VCO). The phase detector compares the phase of the input signal after LNA V_{LNA} and the feedback signal V_{fb}, and outputs the phase difference $(\phi_{in} - \phi_{fb})$ in terms of voltage V_{pd} to the VCO. The VCO takes the voltage V_{pd} as input and generates a feedback signal V_{fb} whose frequency is proportional to the output voltage of the phase detector V_{pd}. The phase detector is implemented using a mixer circuit and a low pass filter.

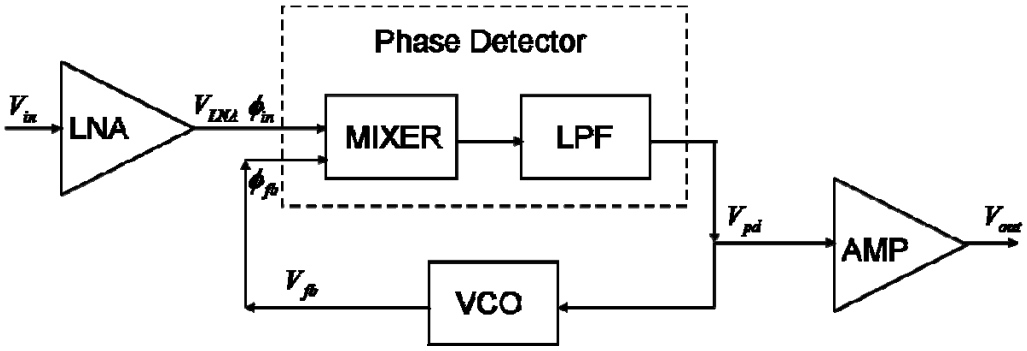


Fig. 7.35: Block diagram of FM receiver using Type I PLL.

The PLL in locked status can be treated as a linear feedback system. The input of the system is the phase of the input signal $\phi_{in} = \frac{\omega_{in}}{s}$, and the output of the system is V_{pd}. The open loop gain is $\frac{K_{pd}}{1+s/\omega_{LPF}}$, where K_{pd} is the gain of the phase detector and ω_{LPF} is the -3dB frequency of the first order low pass filter. The feedback gain is K_{VCO}/s. So the transfer function of the PLL can be expressed as

$$\frac{V_{pd}}{\omega_{in}} = \frac{K_{pd}}{K_{pd}K_{VCO} + s + s^2/\omega_{LPF}} \tag{7.34}$$

Assume there is a sudden increase $\Delta\omega$ in the frequency of the input signal at $t = 0$, $\omega_{in} = \Delta\omega u(t)$. Two parameters below are defined to solve V_{pd} in time domain.

Natural frequency $\omega_n = \sqrt{K_{pd}K_{VCO}\omega_{LPF}}$ (7.35)

Damping ratio $\zeta = \frac{1}{2}\sqrt{\frac{\omega_{LPF}}{K_{pd}K_{VCO}}}$ (7.36)

Substitute equations (7.35) and (7.36), the transfer function in frequency domain is written as

$$\frac{V_{pd}}{\omega_{in}} = \frac{\omega_n^2/K_{VCO}}{s^2 + 2\zeta\omega_{in}s + \omega_n^2} \tag{7.37}$$

The time domain derivative equation is expressed as

$$\frac{d^2V_{pd}}{dt^2} + 2\zeta\omega_n\frac{dV_{pd}}{dt} + \omega_n^2V_{pd} = \frac{\omega_n^2}{K_{VCO}}\omega_{in} \tag{7.38}$$

The eigen value of the derivative equation is

$$\lambda_{1,2} = -\zeta\omega_n \pm \sqrt{1-\zeta^2}\,\omega_n i \tag{7.39}$$

When $\zeta < 1$, the system is under damped. The solution has the form as

$$V_{pd}(t) = Ae^{-\zeta\omega_n t}\sin(\sqrt{1-\zeta^2}\,\omega_n t + \theta) + C \tag{7.40}$$

A, θ and C are constants determined by the boundary conditions below.

$$V_{pd}(\infty) = \Delta\omega / K_{VCO} + V_{pd}(0^-) \Rightarrow C = \Delta\omega / K_{VCO} + V_{pd}(0^-) \tag{7.41}$$

$$\left.\frac{dV_{pd}(t)}{dt}\right|_{t=0} = 0 \Rightarrow \sin\theta = \sqrt{1-\zeta^2} \quad \cos\theta = \zeta \tag{7.42}$$

$$V_{pd}(0^+) = V_{pd}(0^-) \Rightarrow A = -\Delta\omega / \left(K_{vco}\sqrt{1-\zeta^2}\right) \tag{7.43}$$

So the voltage V_{pd} has an under-damped solution as shown in Fig. 7.36(a) with damping factor of $\zeta\omega_n = \frac{1}{2}\omega_{LPF}$ and frequency of $\sqrt{1-\zeta^2}\,\omega_n$.

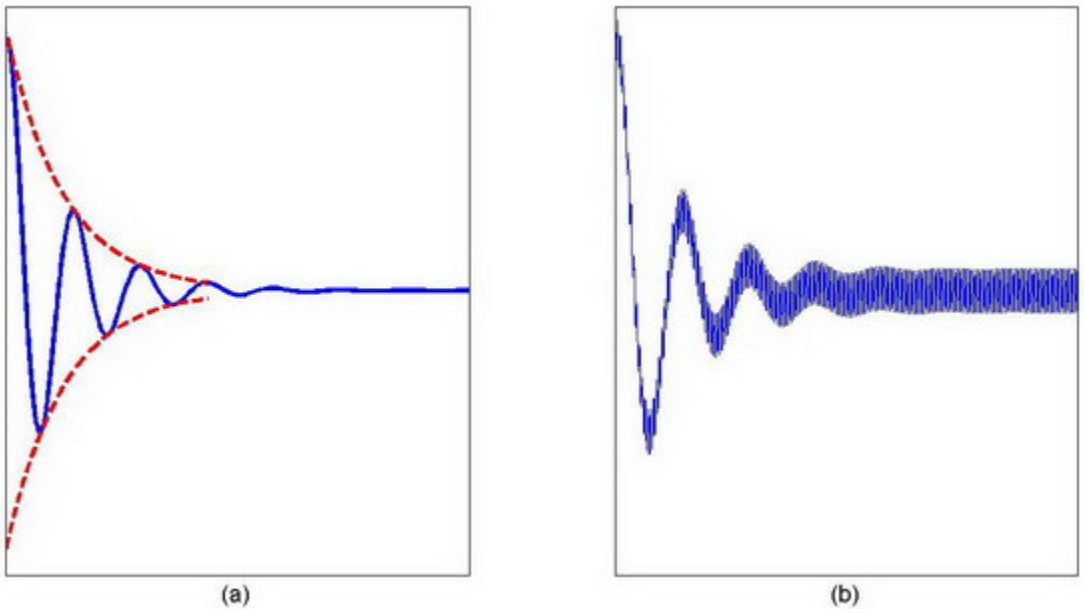


Fig. 7.36: Examples of output signal from a PLL showing the locking process: (a) ideal interpretation. (b) real interpretation.

However, Equation (7.34) assumes ideal phase detection of $K_{pd}(\phi_{in} - \phi_{fb})$ in the mixer block. In reality, accurate implementation of this calculation is almost impossible. Some approximation calculation models have been used to generate phase difference information. The use of approximation models generates unwanted high frequency spectra, and they can not be filtered out completely. So the real output of the system V_{pd} still has high frequency components as shown in Fig. 7.36(b) even after the settling time and the damping is finished. The high frequency oscillation can be not analyzed using the linear model in equation (7.34). In the next few sections, Matlab software is used to analyze the PLL system. Different models of mixers and low pass filters are evaluated. And the effect of the linearity of the voltage-controlled oscillator on PLL is also studied.

7.3.2 Matlab Analysis Methodology

The Matlab analysis method is explained in this section with a PLL example of multiplier mixer, first order low pass filter and a linear VCO. Other models will be evaluated later and compared to this example.

The multiplier mixer model is the simplest and most widely used model for mixer design. Now we explain why it can be approximately used to calculate the phase difference. Assume there are two sine wave signals $x = \cos(\omega_x t + \theta_x)$ and $y = \cos(\omega_y t + \theta_y)$, according to trigonometry, the multiplication of the two signals is

$$f(x,y) = \frac{1}{2}\cos[(\omega_x - \omega_y)t + (\theta_x - \theta_y)] + \frac{1}{2}\cos[(\omega_x + \omega_y)t + (\theta_x + \theta_y)] \qquad (7.44)$$

When the frequency of the two input signals ω_x and ω_y does not differ much, $\cos\left[\left(\omega_x-\omega_y\right)t+\left(\theta_x-\theta_y\right)\right]$ is a harmonic with much lower frequency than $\cos\left[\left(\omega_x+\omega_y\right)t+\left(\theta_x+\theta_y\right)\right]$. With an appropriate low pass filter, $\cos\left[\left(\omega_x+\omega_y\right)t+\left(\theta_x+\theta_y\right)\right]$ will be filtered out and the phase difference of $\left(\omega_x-\omega_y\right)t+\left(\theta_x-\theta_y\right)$ is generated as $\frac{1}{2}\cos\left[\left(\omega_x-\omega_y\right)t+\left(\theta_x-\theta_y\right)\right]$. When k is an integer and $\left(\omega_x-\omega_y\right)t+\left(\theta_x-\theta_y\right)$ is between $(2k-1)\pi$ and $2k\pi$, the cosine function is monotonically increasing, which represents the phase difference $\left(\omega_x-\omega_y\right)t+\left(\theta_x-\theta_y\right)$ itself. Since there is no ideal low pass filter in the world, a small amount of the harmonic $\cos\left[\left(\omega_x+\omega_y\right)t+\left(\theta_x+\theta_y\right)\right]$ is left on the output of phase detector and generates oscillation even as the PLL is in locked steady state.

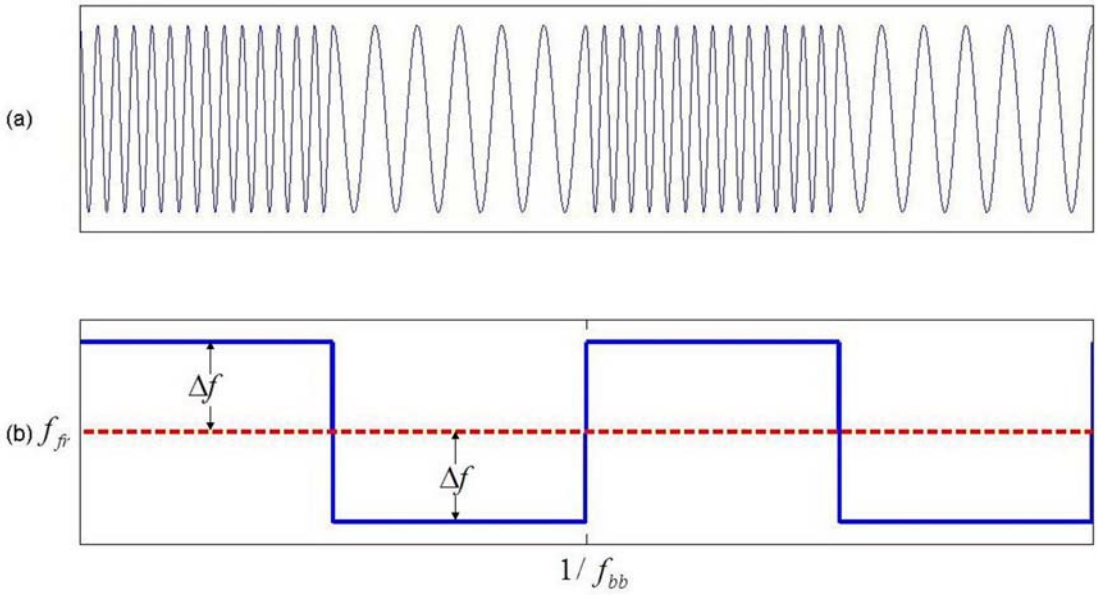


Fig. 7.37: (a) A typical sine wave input signal to BFSK receiver. (b) The frequency of the input signal.

A Matlab program is written to investigate a PLL system composed of the multiplier mixer and basic first order low pass RC filter. A typical input signal to a BFSK receiver is a sine wave, and the frequency of the wave is a pulse function at the baseband frequency f_{bb} as shown in Fig. 7.37. In the simulation, the free running frequency f_{fr} is set at 100Hz for fast simulation. The frequency variance is denoted as Δf. The base band frequency f_{bb} is set as 0.5Hz corresponding to 1bps rate, which provides long enough time for locking at both frequencies $\left(f_{fr}-\Delta f\right)$ and $\left(f_{fr}+\Delta f\right)$. The product of the gains of mixer and VCO is defined as the loop gain, and denoted as $K=K_{pd}K_{vco}$, which plays an important role on the behavior of the system. The time constant of the low pass filter is denoted as $\tau=RC$. Δf, K and τ are the most three crucial parameters to set the property of the PLL system.

For evaluation of the system, three more parameters are defined as below.

f_{lock}: The lock-in frequency range is defined as the largest frequency variance, with which the PLL can still lock within one period $1/f_{bb}$ of the pre-set base band signal. The larger the lock-in frequency, the larger the frequency variance the system can bear.

t_{set}: The settling time is defined as the time it takes the output signal to reach within $\pm 1\%$ of the steady state at each baseband cycle. Since the baseband signal is a pulse, there are two steady states as up and down, so that there are two settling time t_{set_up} and t_{set_down}. The settling time should be the maximum of t_{set_up} and t_{set_down}.

And the smaller the settling time, the faster the base band signal can reach, the faster the data bits can be received.

σ_{osci} : The standard deviation is defined as the maximum standard deviation of the output signal in both up and down steady states. The standard deviation at each steady state is the same as $1/\sqrt{2}$ times of the oscillation amplitude. The smaller the standard deviation is, the cleaner the output signal is, and the less noisy the PLL system is.

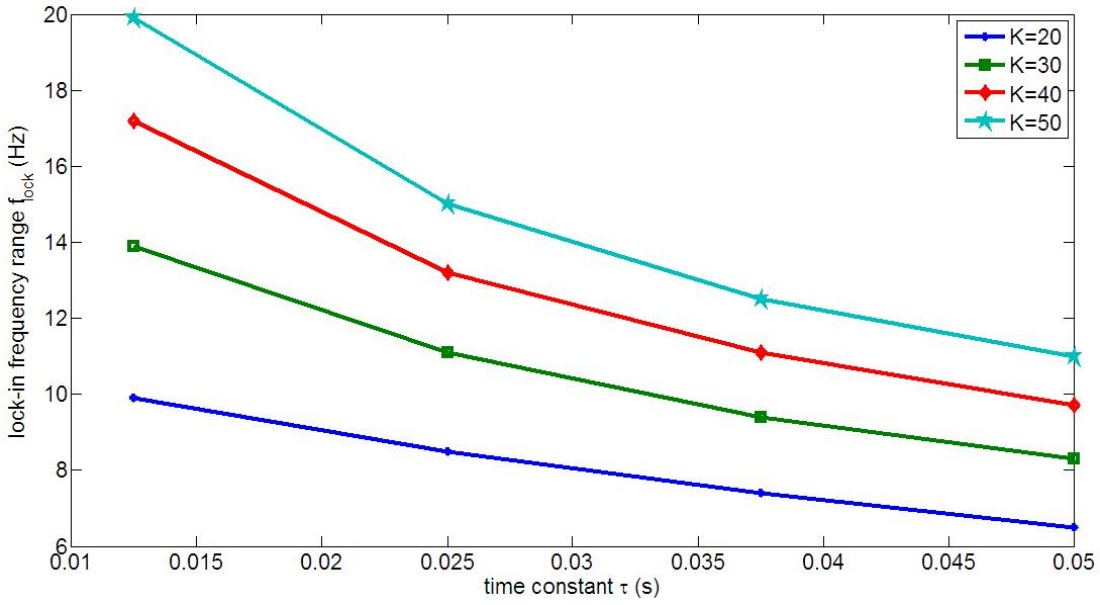


Fig. 7.38: Lock-in frequency range f_{lock} variation with time constant τ at different value of loop gain K .

First the lock-in frequency range f_{lock} is studied with varying the loop gain K and time constant τ . Fig. 7.38 shows the trend of f_{lock} with τ at different K values of 20, 30, 40 and 50 with dot, square, diamond, and pentagon respectively. The lock-in frequency is evaluated at accuracy of 0.1Hz. Increasing the time constant τ reduces

the lock-in frequency range f_{lock}, while increasing the gain product K widens the lock-in frequency range f_{lock}.

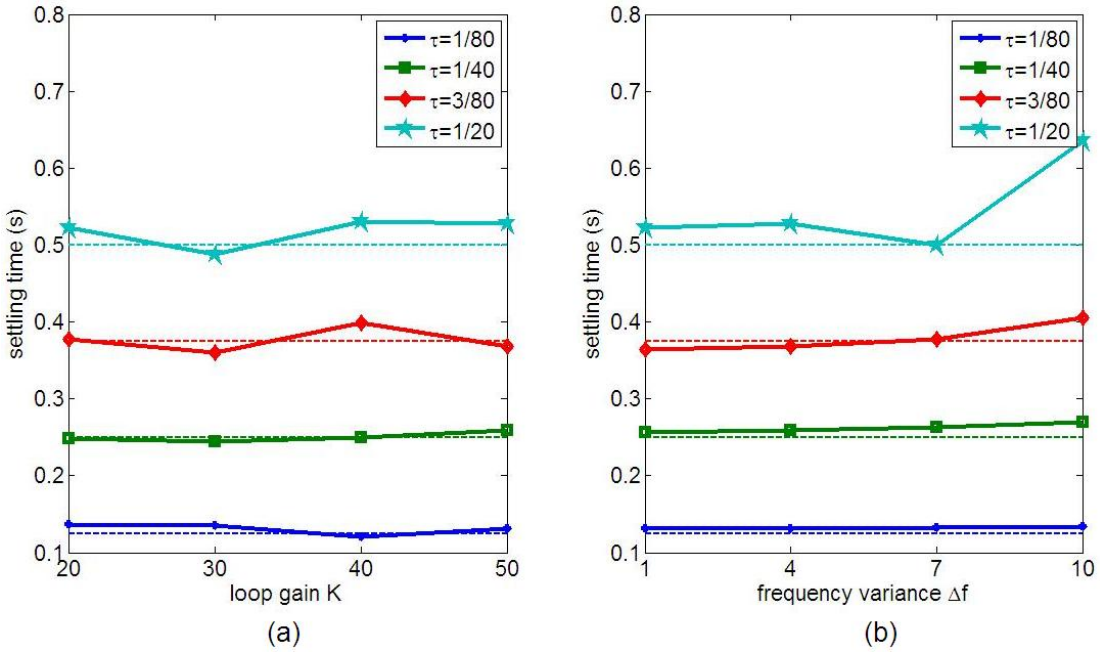


Fig. 7.39: (a) The settling time t_{set} change with respect to loop gain K at different time constant τ when $\Delta f = 4$. (b) The settling time t_{set} change with respect to frequency variance Δf at different time constant τ when $K = 50$. The dotted line is 10 times of the corresponding time constant τ.

Then the settling time t_{set} is illustrated with varying the loop gain K, time constant τ and the frequency variance Δf. The relationship between t_{set} and K, between t_{set} and Δf at different time constant τ are plotted in Fig. 7.39(a) and (b). The dot, square, diamond and pentagon stand for time constant values of 1/80, 1/40, 3/80 and 1/20 respectively. The settling time t_{set} has strong dependence on the time constant τ. The dotted line near each group of data is actually 10 times of the time constant τ. The dependence on loop gain K and frequency variance Δf is not clear.

A slight increase of settling time t_{set} is observed with increasing of the frequency variance Δf, but the change is not strictly monotonically increasing.

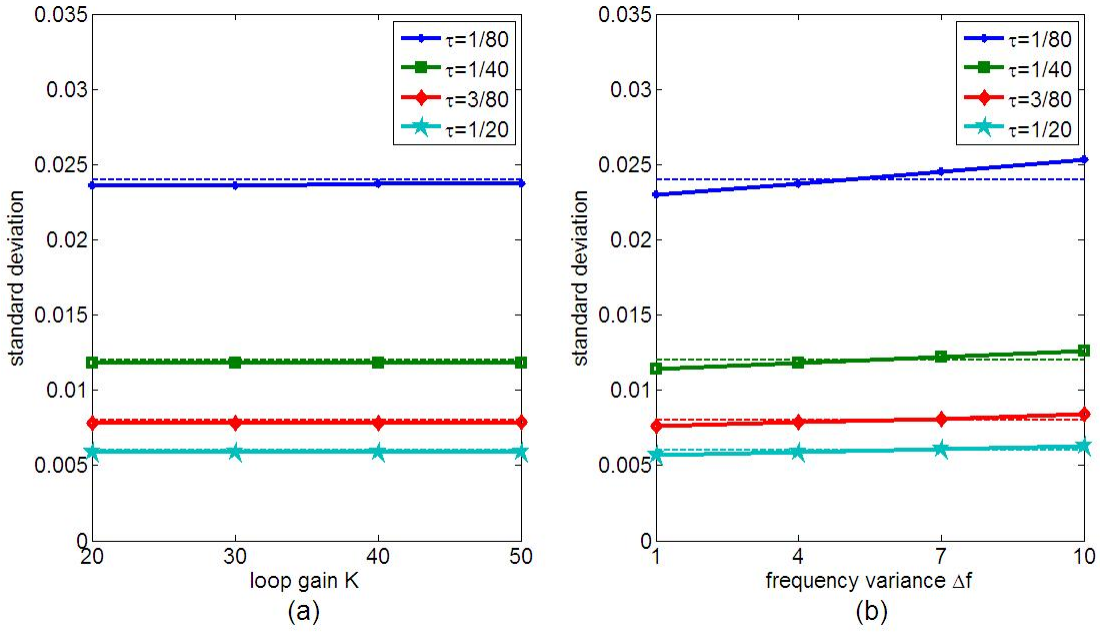


Fig. 7.40: (a) The standard deviation σ_{osci} change with respect to loop gain K at different time constant τ when $\Delta f = 4$. (b) The standard deviation σ_{osci} change with respect to frequency variance Δf at different time constant τ when $K = 50$. The dotted line is 0.003 divided by the corresponding time constant τ.

Finally the standard deviation σ_{osci} is investigated with varying the loop gain K, time constant τ and the frequency variance Δf. The relationship between σ_{osci} and K, between σ_{osci} and Δf at different time constant τ are plotted in Fig. 7.40(a) and (b). The dot, square, diamond and pentagon stand for time constant values of 1/80, 1/40, 3/80 and 1/20 respectively. The standard deviation σ_{osci} is inversely proportional to time constant τ. The dotted line near each group of data is actually 0.0003 divided by time constant τ. The standard deviation σ_{osci} is believed to remain constant with

the change of loop gain K and slightly increases with the frequency variance Δf, and the increasing is monotonic.

In conclusion, the simplest type I PLL made up with a multiplier mixer, first order low pass filter and a linear VCO has characteristics as below.

1. The lock-in frequency range f_{lock} decreases with the time constant τ and increases with the loop gain.

2. The settling time is proportional to the time constant τ at several loop gains K and several frequency variances Δf.

3. The standard deviation is inversely proportional to the time constant τ, remains the same at different loop gains K, and slightly increases with frequency variance Δf monotonically.

7.3.3 Model Evaluation

In last section, the simplest type I PLL is studied using Matlab numerically. We will use the same method to evaluate PLLs with other mixer, low pass filter and VCO models in this section. By comparing their characteristics with the basic model we studied in the previous section, we will not only obtain optimization schemes for specific applications, but also understand the non-ideal effects on the system due to any non-linearity. We will start from different low pass filter models, and then explore some non-linear VCOs. Various mixer models will be evaluated at last.

7.3.3.1 Low pass filter models

The first order low pass filter is used in the simplest PLL discussed in section 7.3.2. It has one pole at $1/\tau$ and clearly the time constant τ plays an extremely important role in the PLL system. It affects the lock-in frequency range, the settling time and steady state standard deviation very much. In this part, we will try to add one zero or one pole to the single pole low pass filter model and observe the changes to the system.

1. Adding one zero.

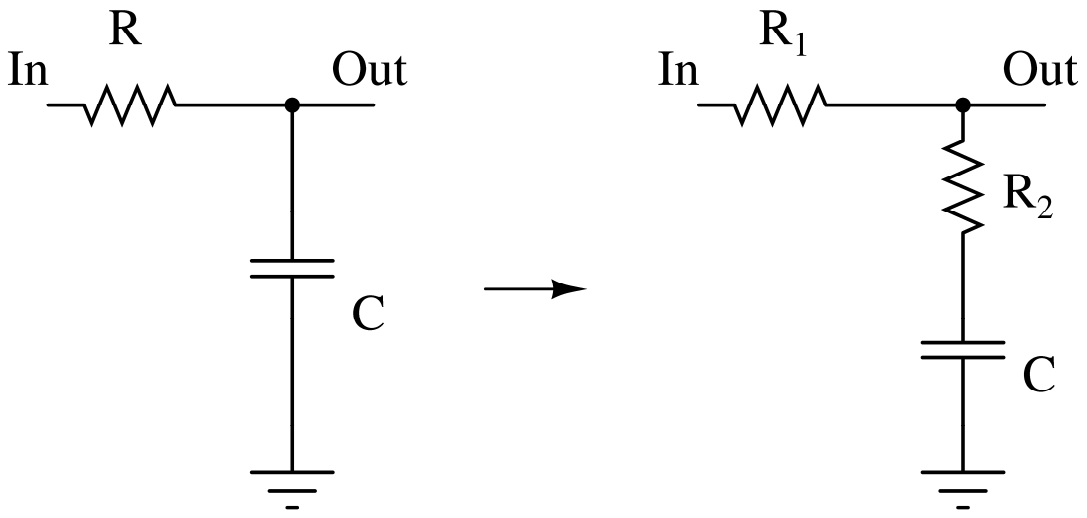


Fig. 7.41: Schematics of one pole low pass filter and the one pole one zero low pass filter.

By adding one zero to the low pass filter model as in Fig. 7.41, the transfer function of the low pass filter changes from equation (7.45) to equation (7.46).

$$\frac{V_{out}}{V_{in}} = \frac{1}{RCs+1} \tag{7.45}$$

$$\frac{V_{out}}{V_{in}} = \frac{R_2Cs+1}{(R_1+R_2)Cs+1} \tag{7.46}$$

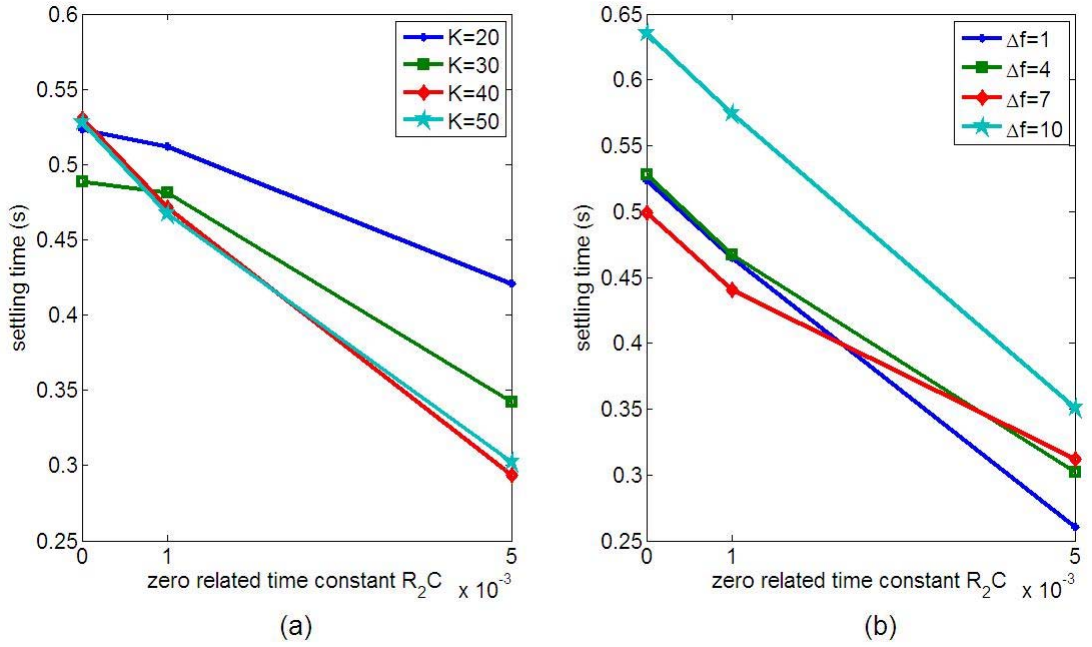


Fig. 7.42: (a) The settling time t_{set} change with respect to R_2C at different loop gain K when $\Delta f = 4$. (b) The settling time t_{set} change with respect to R_2C at different frequency variance Δf when $K = 50$.

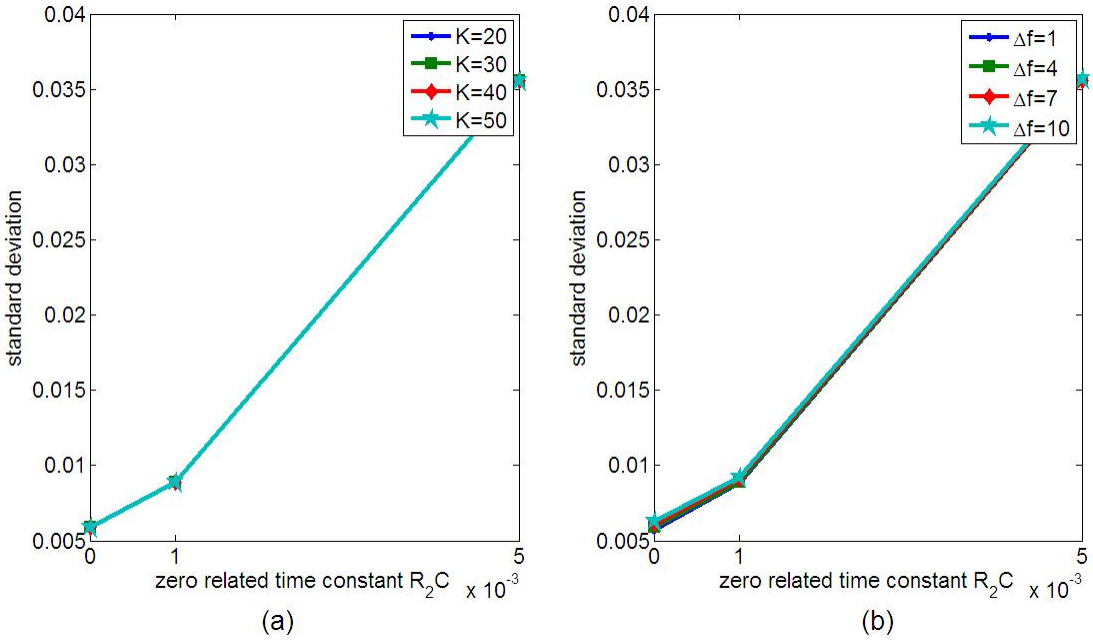


Fig. 7.43: (a) The standard deviation σ_{osci} change with respect to R_2C at different loop gain K when $\Delta f = 4$. (b) The standard deviation σ_{osci} change with respect to R_2C at different frequency variance Δf when $K = 50$.

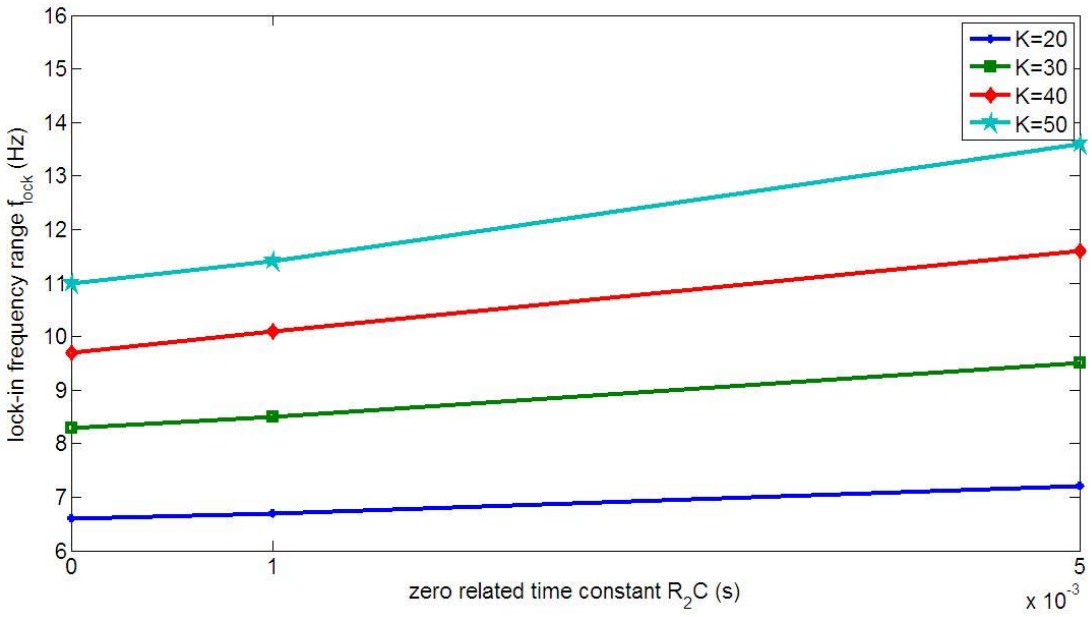


Fig. 7.44: Lock-in frequency range f_{lock} variation with zero related time constant R_2C at different value of loop gain K.

In order to compare the results with single pole model, we keep the pole related time constant $\tau = RC = (R_1 + R_2)C$ the same at 1/20, and vary the value of the zero related time constant R_2C from 0, 1/1000 to 1/200. Fig. 7.42(a) and (b) shows the settling time change with respect to zero related time constant R_2C at different loop gain K and frequency variance Δf. Fig. 7.43(a) and (b) shows the steady state standard deviation change with R_2C at different loop gain K and frequency variance Δf. Fig. 7.44 shows the lock-in frequency range f_{lock} with R_2C at different loop gain K of 20, 30, 40 and 50.

The three figures above tell us the added zero to the low pass filter enlarges the lock-in frequency range and shortens the settling time of the PLL at the price of increasing the steady state standard deviation. If an application cares more about the

settling time and lock-in frequency range than the noise, this model might be an useful approach. However, if all the parameters are important, the model is worse than the simplest one pole low pass model. This is shown in Table 7.5. The performance of the one pole one zero filter model has narrower lock-in frequency range, longer settling time and larger standard deviation than the comparative one pole model. The two examples show that it is better to increase the pole frequency than to add a zero.

	one pole RC=3/80		one pole one zero $(R_1+R_2)C=1/20$ $R_2C=1/1000$		one pole RC=1/40		one pole one zero $(R_1+R_2)C=1/20$ $R_2C=1/200$	
lock-in frequency range	K	f_{lock}	K	f_{lock}	K	f_{lock}	K	f_{lock}
	20	7.4	20	6.7	20	8.5	20	7.2
	30	9.4	30	8.5	30	11.1	30	9.5
	40	11.1	40	10.1	40	13.2	40	11.6
	50	12.5	50	11.4	50	15	50	13.6
settling time	0.3682		0.4671		0.2585		0.3022	
standard deviation	0.0079		0.0089		0.0118		0.0356	

Table 7.5: The performance comparison between one pole low pass filter model and one pole one zero model.

2. Adding one more pole.

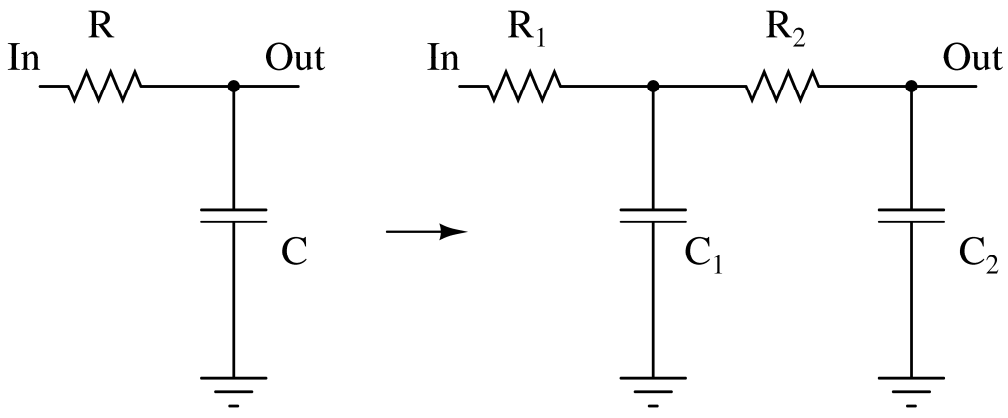


Fig. 7.45: Schematics of one pole low pass filter and two-pole low pass filter.

The two-pole low pass filter is implemented by cascading two stages of on pole low pass filter as shown in Fig. 7.45. In order to compare the results with single pole model, we keep the first pole the same as $\tau = RC = R_1C_1$ at 1/40 and vary the second pole time constant R_2C_2 from 0, 1/1000 to 1/400. Fig. 7.46(a) and (b) shows the settling time change with respect to zero related time constant R_2C_2 at different loop gain K and frequency variance Δf. Fig. 7.47(a) and (b) shows the steady state standard deviation change with R_2C_2 at different loop gain K and frequency variance Δf. Fig. 7.48 shows the lock-in frequency range f_{lock} with R_2C_2 at different loop gain K of 20, 30, 40 and 50.

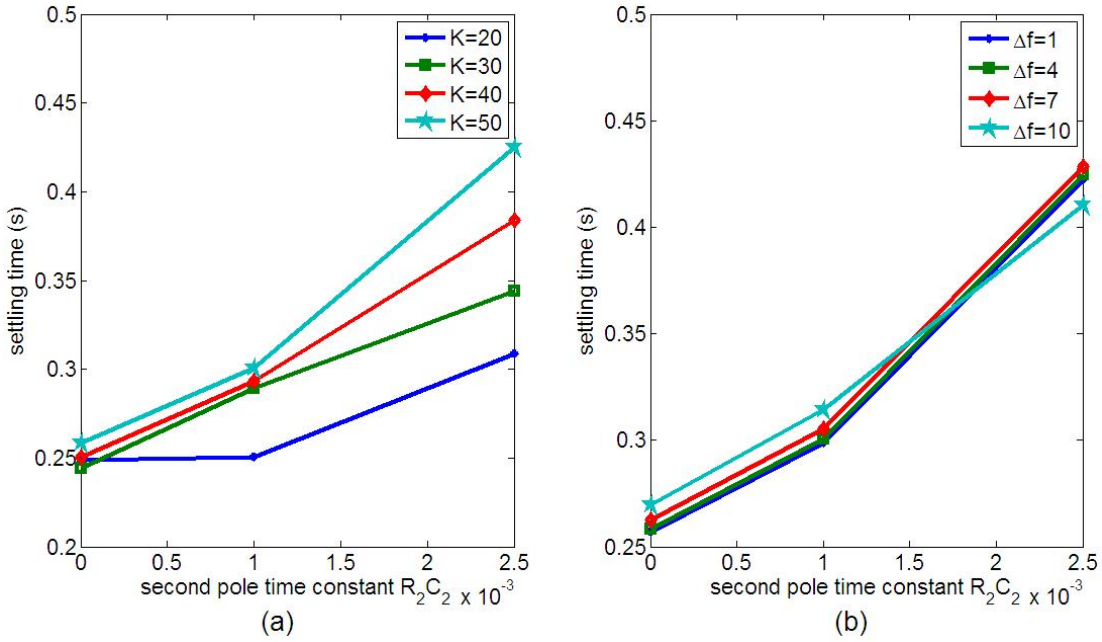


Fig. 7.46: (a) The settling time t_{set} change with respect to R_2C_2 at different loop gain K when $\Delta f = 4$. (b) The settling time t_{set} change with respect to R_2C_2 at different frequency variance Δf when $K = 50$.

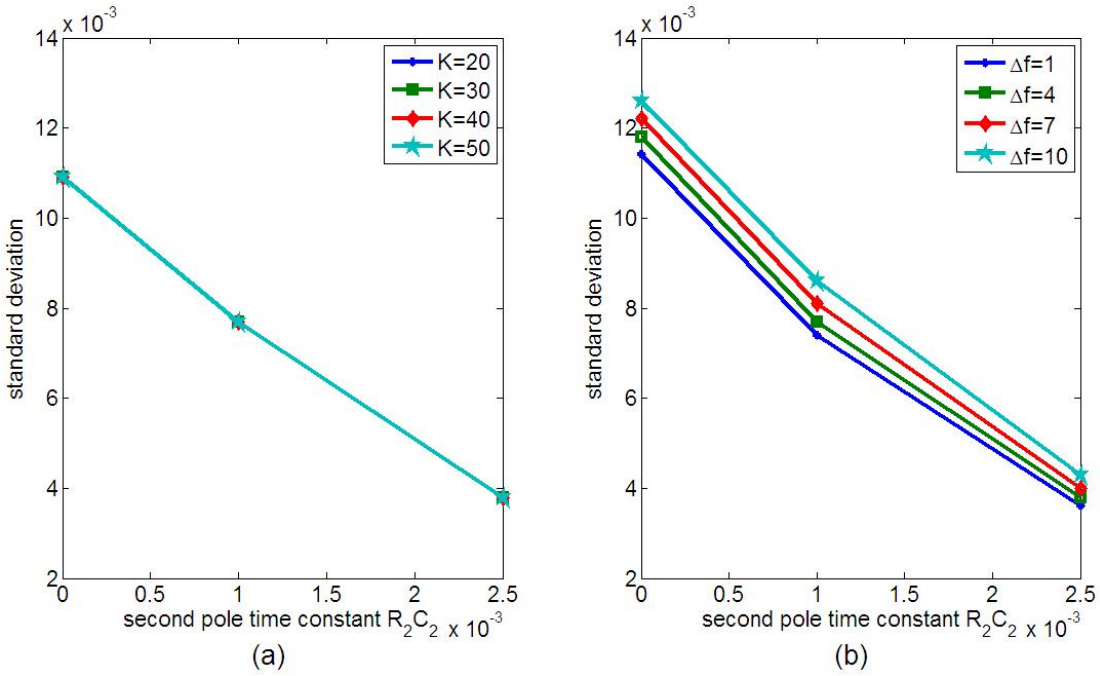


Fig. 7.47: (a) The standard deviation σ_{osci} change with respect to R_2C_2 at different loop gain K when $\Delta f = 4$. (b) The standard deviation σ_{osci} change with respect to R_2C_2 at different frequency variance Δf when $K = 50$.

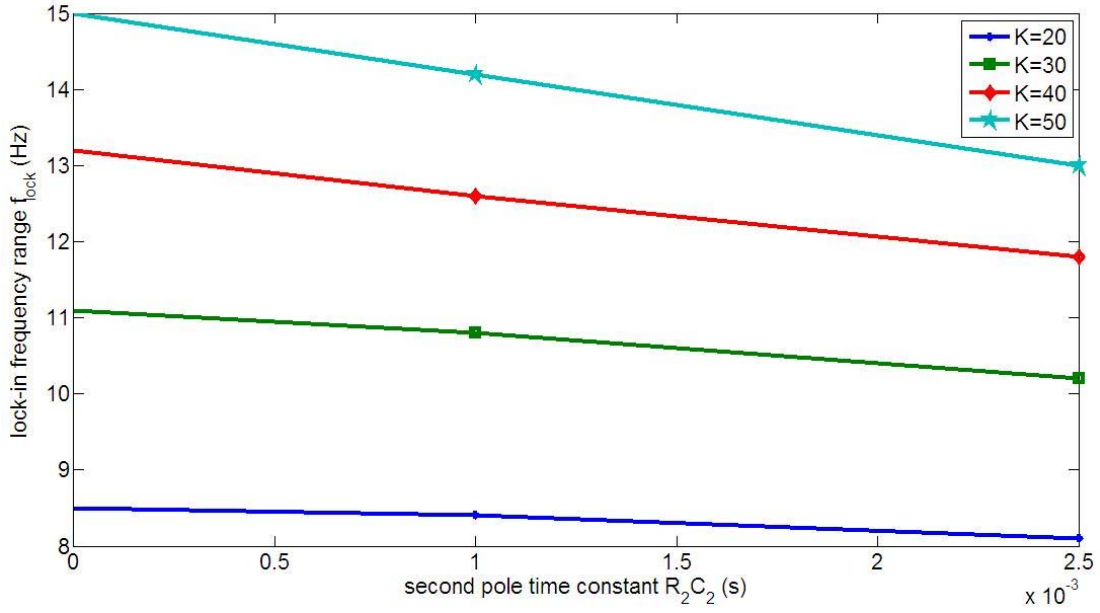


Fig. 7.48: Lock-in frequency range f_{lock} variation with zero related time constant R_2C at different value of loop gain K.

The three figures above tell us the added pole to the low pass filter lowers the steady state standard deviation at the price of shrinking the lock-in frequency range and prolonging the settling time of the PLL. This two-pole low pass model is a good approach for a low noise system. With clever selection of the two pole time constants, the two-pole low pass model has larger lock-in frequency range, shorter settling time and lower standard deviation compared to the one pole filter model. The performance comparison is shown in Table 7.6. The two examples show that it is better to add one pole than to decrease the pole frequency.

	one pole RC=3/80		two-pole R_1C_1=1/40 R_2C_2=1/1000		one pole RC=1/20		two-pole R_1C_1=1/40 R_2C_2=1/400	
lock-in frequency range	K	f_{lock}	K	f_{lock}	K	f_{lock}	K	f_{lock}
	20	7.4	20	8.4	20	6.6	20	8.1
	30	9.4	30	10.8	30	8.3	30	10.2
	40	11.1	40	12.6	40	9.7	40	11.8
	50	12.5	50	14.2	50	11	50	13
settling time	0.3682		0.3005		0.5280		0.4248	
standard deviation	0.0079		0.0077		0.0059		0.0038	

Table 7.6: The performance comparison between one pole low pass filter model and two-pole model.

7.3.3.2 Nonlinear VCOs

The linear VCO model is used in the simplest PLL discussed in section 7.2.2. The transfer function can be expressed as

$$f_{out} = f_{fr} + K_{VCO}V_{in} \tag{7.47}$$

Well the VCO might not be linear in reality. A higher order terms of V_{in} is a good approximation to simulate the nonlinearity. We take one additional second order term and one additional third order term as examples to demonstrate the nonlinear VCO effect on the PLL system.

1. A second order term.

With an additional second order term of V_{in}, the transfer function of the VCO changes to

$$f_{out} = f_{fr} + K_{VCO}V_{in} + k_2 V_{in}^2 \tag{7.48}$$

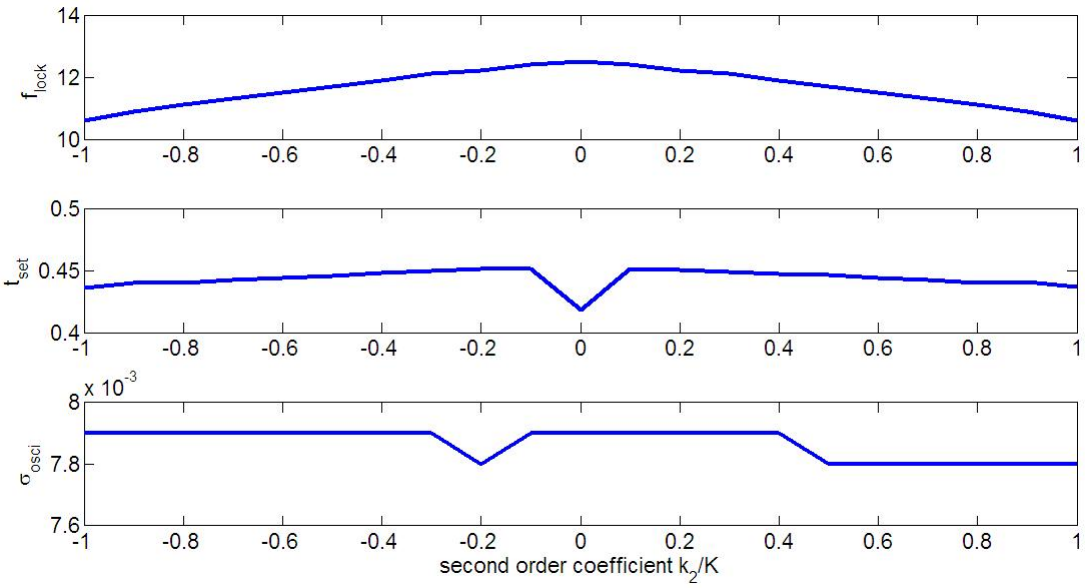


Fig. 7.49: The lock-in frequency range f_{lock}, settling time t_{set} and standard deviation σ_{osci} change with the second order coefficient k_2 when the loop gain $K = K_{VCO} = 50$.

For simplicity, the gain of the VCO K_{vco} is selected as the same as the loop gain K, so that the gain of the phase detector K_{pd} is 1. The second order coefficient k_2 is selected from -100% to 100% of K_{vco}. Fig. 7.49 illustrates the changes of the lock-in

frequency range f_{lock}, the settling time t_{set} and the steady state standard deviation σ_{osci} with respect to the ratio of k_2 over K when $K = 50$. The lock-in frequency range f_{lock} shrinks with the increase of the absolute value of k_2. The settling time t_{set} increases about 8% with non-zero k_2 and decreases with the increase of the absolute value of k_2 in this case. Both the lock-in frequency range f_{lock} and the settling time t_{set} are symmetrical to the line of $k_2 = 0$. The standard deviation almost remains the same with the variance of k_2.

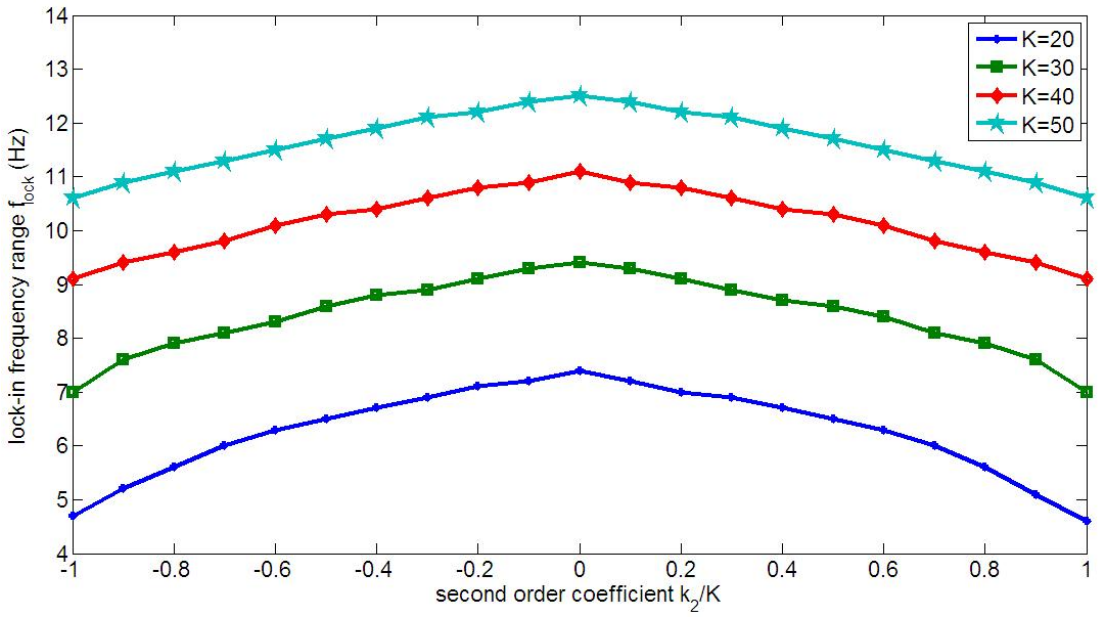


Fig. 7.50: The lock-in frequency range f_{lock} change with respect to k_2 / K at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$.

Fig. 7.50 shows the lock-in frequency range change at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$. With the decreasing of the loop gain K, the shrinking effect of f_{lock} with the absolute value of the ratio k_2 / K becomes more prominent.

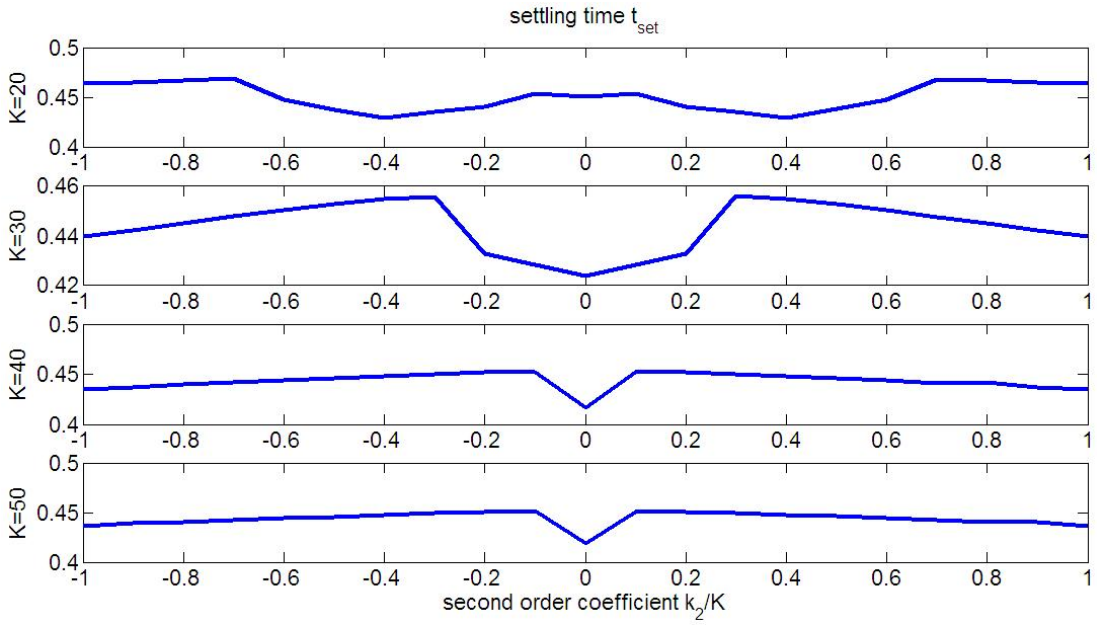


Fig. 7.51: The settling time t_{set} change with respect to k_2 / K at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$.

Fig. 7.51 demonstrates the settling time change at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$. All of the curves are symmetrical to the line of $k_2 = 0$. The curves of loop gains at 40 and 50 monotonically decrease with the increasing of the absolute value of the ratio k_2 / K. But the curves of loop gains at 20 and 30 are not monotonic functions. The standard deviation σ_{osci} at all the loop gains remains constant.

The second order nonlinearity decreases the lock-in frequency range f_{lock} and increases the settling time t_{set} of the PLL system, but has no effect on the steady state standard deviation σ_{osci}. The effect on the lock-in frequency range f_{lock} is more notable with smaller loop gain. This conclusion can be applied to all even order nonlinearity.

2. A third order term.

With an additional third order term of V_{in}, the transfer function of the VCO changes to

$$f_{out} = f_{fr} + K_{VCO}V_{in} + k_3V_{in}^3 \tag{7.49}$$

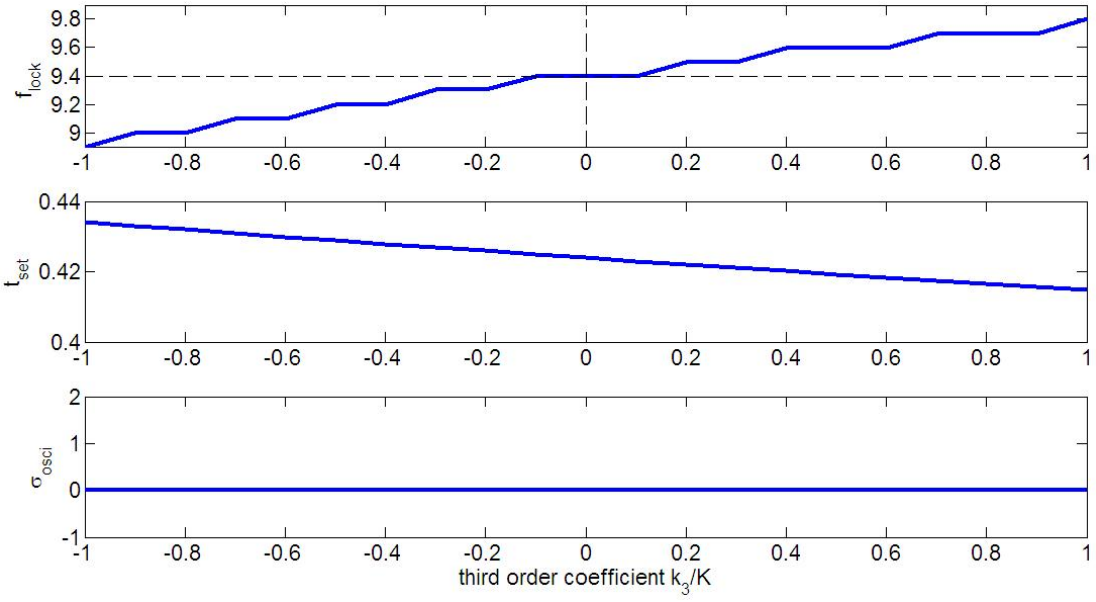


Fig. 7.52: The lock-in frequency range f_{lock}, settling time t_{set} and standard deviation σ_{osci} change with the third order coefficient k_3 when the loop gain $K = K_{VCO} = 30$.

Same as in second order discussion, the gain of the VCO K_{vco} is selected as the same as the loop gain K for simplicity. The third order coefficient k_3 is selected from -100% to 100% of K_{vco}. The second order coefficient k_2 is selected from -100% to 100% of K_{vco}. Fig. 7.52 illustrates the changes of the lock-in frequency range f_{lock}, the settling time t_{set} and the steady state standard deviation σ_{osci} with respect to the ratio of k_3 over K when $K = 50$. The lock-in frequency range f_{lock} widens with the

increasing of k_3 and is symmetrical to the point of $k_3 = 0$. The settling time t_{set} decreases with k_3 and the standard deviation almost remains the same with the variance of k_3.

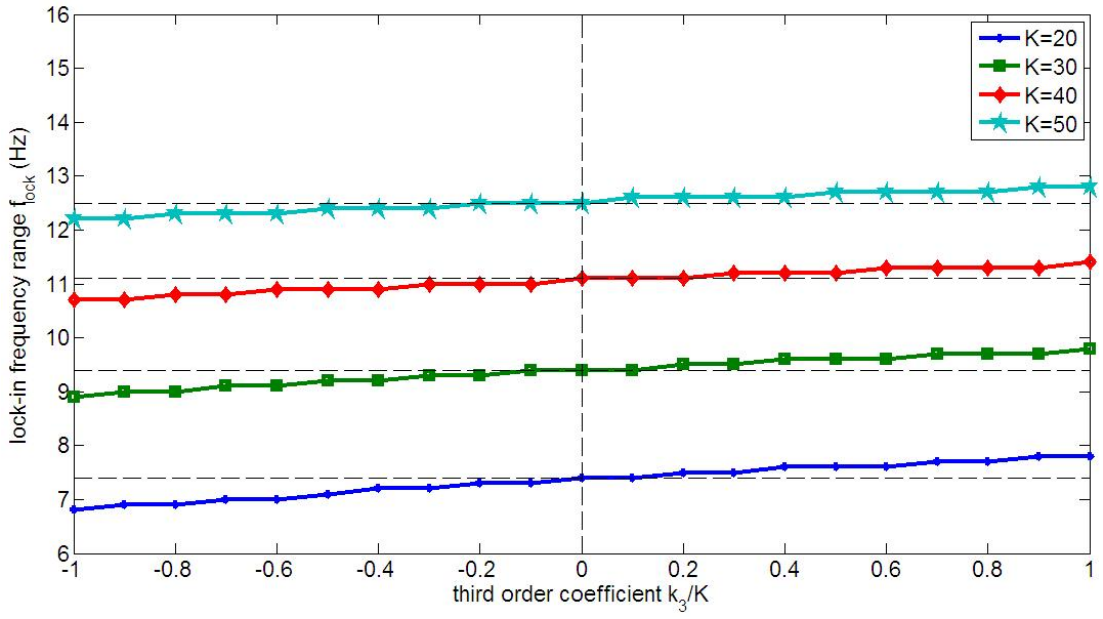


Fig. 7.53: The lock-in frequency range f_{lock} change with respect to k_3 / K at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$.

Fig. 7.53 shows the lock-in frequency range change at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$. With the decreasing of the loop gain K, the change of f_{lock} with the ratio k_3 / K becomes more prominent.

Fig. 7.54 demonstrates the settling time change at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$. The curves are not monotonic with the ratio k_3 / K. The standard deviation σ_{osci} at all the loop gains remains constant.

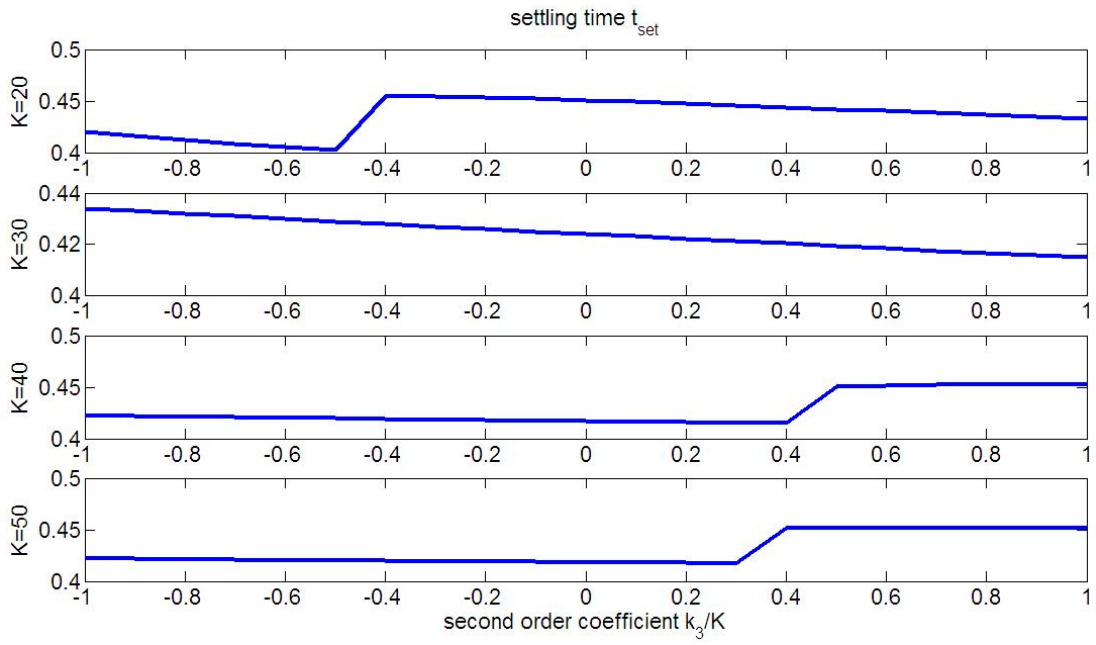


Fig. 7.54: The settling time t_{set} change with respect to k_3 / K at different loop gains of 20, 30, 40 and 50 with the same frequency variance $\Delta f = 4$.

The positive third order nonlinearity increases the lock-in frequency range f_{lock}, while the negative third order nonlinearity decreases the lock-in frequency range f_{lock}. The effect on the lock-in frequency range f_{lock} is more notable with smaller loop gain. The third order nonlinearity has no effect on steady state standard deviation σ_{osci}. The dependence of the settling time t_{set} on the third order nonlinearity is uncertain. This conclusion can be applied to all odd order nonlinearity.

7.3.3.3 Mixer models

The multiplier mixer is used in the simplest PLL discussed in section 7.2.2. The transfer function can be expressed as:

$$f(x, y) = xy \tag{7.50}$$

x and y are sinusoidal functions with unit amplitude and zero DC offset in the simulation. Actually the DC offset and the amplitude affects the evaluation of the PLL system. A non-zero offset generates more steady state standard oscillation and a smaller amplitude downgrades the lock-in frequency. For radio frequency low power transceiver design, the unit amplitude is a good maximum approximation since most of designs use power voltage under 1.6V. Under these circumstances, several other mixer models are proved to be valid. These models are formulated as below.

$$f_1(x,y) = x^3 y \tag{7.51}$$

$$f_2(x,y) = y * \sin(x) \tag{7.52}$$

$$f_3(x,y) = y * \left(e^x - 1\right) \tag{7.53}$$

$$f_4(x,y) = y * \tan(x) \tag{7.54}$$

$$f_5(x,y) = y * \log(x + 1.0001) \tag{7.55}$$

These models are first guessed from basic mathematical functions of x, and simulated to test the validity. Even functions of x in general are not valid as mixer models because the output cannot differentiate between opposite signs of x. For the range [-1,1] of x, all the functions of x obey the following rules:

1. Monotonically increasing with x.

2. Greater than zero with positive x and zero at $x = 0$

The equation (7.55) is an exception of the second rule. $(x + 1.0001)$ is used instead of $(x + 1)$ for the validity of calculation when $x = -1$. It is like adding a very

small DC offset to x. x and y are interchangeable in all the models without violating the validity of the PLL system. And except the model in equation (7.55), the lock-in frequency range f_{lock} is the same between the two xy-interchanged models. The exception is believed to be the result of the added small DC offset.

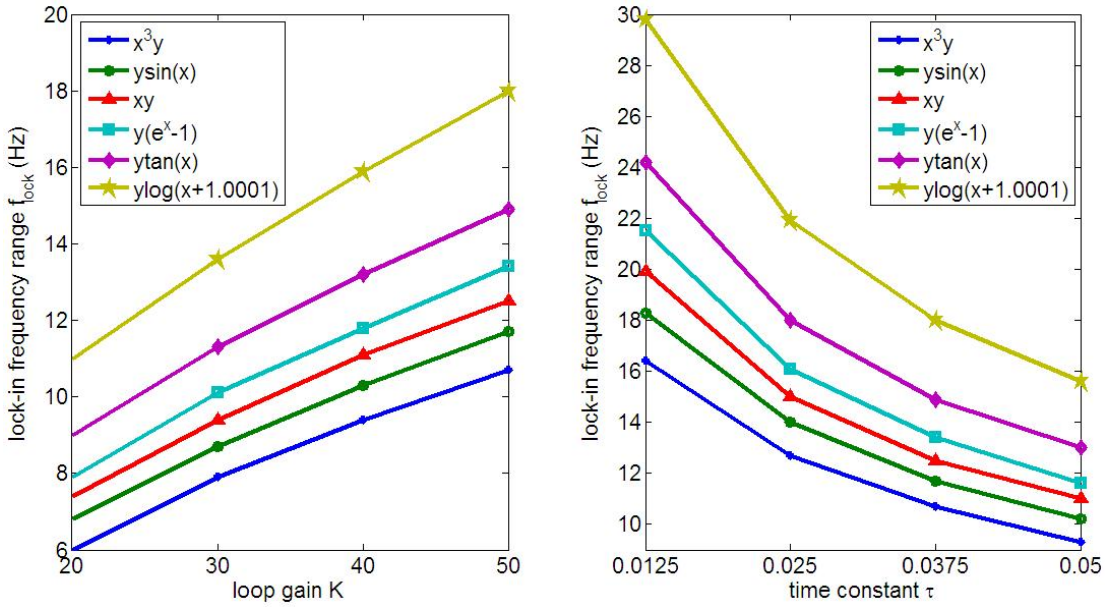


Fig. 7.55: The lock-in frequency range f_{lock} change with loop gain K when $\tau = 3/80$ and with time constant τ when $K = 50$ using different mixer models.

Fig. 7.55 illustrates the lock-in frequency range f_{lock} of all the mixer models with the variance of loop gains and time constants. Of all the mixer models, the lock-in frequency range f_{lock} increases with loop gain K and decreases with time constant τ. f_{lock} increases in the order of cubic, sinusoidal, linear, exponential, tangent and logarithm functions.

Fig. 7.56 shows the settling time t_{set} and the steady state standard deviation σ_{osci} of all the mixer models with the variance of time constants. Of all the mixer models,

the settling time t_{set} depend on the time constants linearly and do not differ much. The standard deviation σ_{osci} increases in the order of cubic, sinusoidal, linear, tangent, exponential and logarithm functions. The difference between the tangent and exponential functions is very small though.

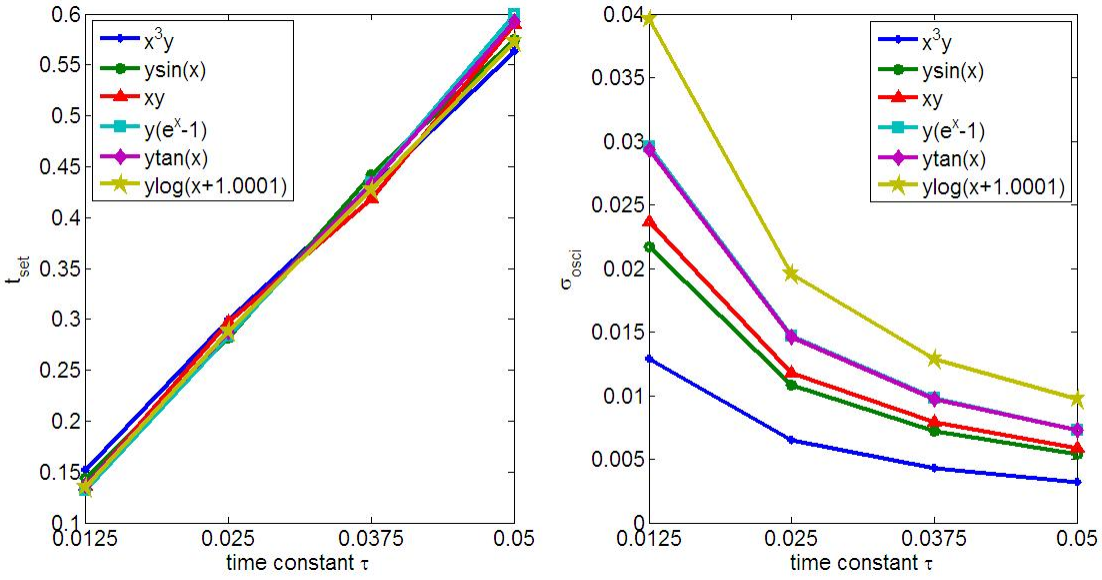


Fig. 7.56: The settling time t_{set} and steady state standard deviation σ_{osci} change with time constant τ when $K = 50$ and $\Delta f = 4$ using different mixer models.

Fig. 7.57 explains the lock-in frequency range f_{lock} and the steady state standard deviation σ_{osci} at different time constants in bar plot using different mixer models. Generally speaking, the mixer model with wider lock-in frequency range f_{lock} ends up with higher standard deviation. The exception between the tangent function and exponential function is trivial. If a PLL system needs wider lock-in frequency range, the models on the right may be good choices. If a PLL system requires low noise and high sensitivity, the models on the left should be considered. An appropriate model can be selected for specific application according to the trends shown in Fig. 7.57.

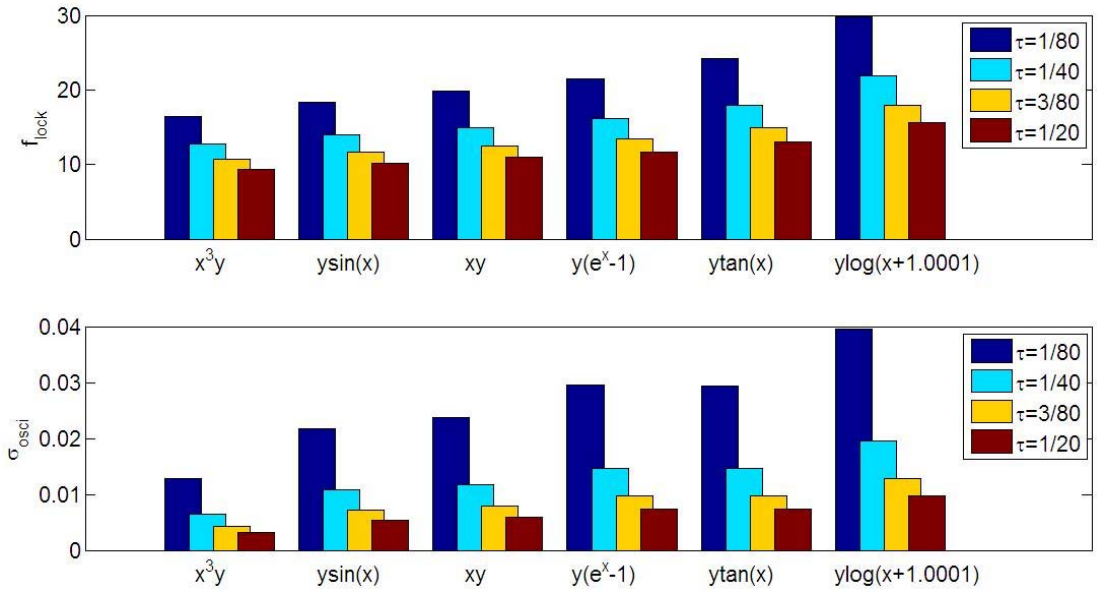


Fig. 7.57: The lock-in frequency range f_{lock} and steady state standard deviation σ_{osci} of all the mixer models at different time constants 1/80, 1/40, 3/80 and 1/20.

7.3.4 Summary

We have described a method to analyze the models of a PLL system used for BFSK receiver. Compared to the traditional linear analysis, we chose Matlab to simulate the PLL system numerically.

We started with the simplest PLL model made up of multiplier mixer, first order low pass filter and linear VCO models to demonstrate the effectiveness of the method. The dependence of the lock-in frequency range on loop gains and time constants is demonstrated. The trade-off between the settling time and steady state oscillation is presented.

Other mixer and low pass filter models are also evaluated using the simulation method and compared to the simplest PLL model. The multiple pole low pass filter model shows better performance than the single pole model with suitable selection of

poles. A trade-off between lock-in frequency range and steady state oscillation is presented among different mixer models. With the help of the analysis, appropriate solutions may be obtained for specific applications.

Besides the mixer and low pass filter models, nonlinear VCO models are also evaluated in odd and even orders separately. The nonlinearity of VCO affects the lock-in frequency range and settling time of a PLL system and has no effect on the steady state oscillation. With the help of nonlinear analysis of VCO models, we will have better understanding of the BFSK receiver using PLL system in reality.

Chapter 8: Future Work

8.1 Adaptive Filters for System Identification

We have completed the design of a first order model based low pass filter for system identification. Solid learning rules of the parameters have been derived using Lyapunov stability based on the first order low pass filter model. Parameter computation has been implemented using simple analog circuits.

Aside from the most popular first order low pass model, there are numerous other filter structures which are also widely used in real life. For example, a high pass filter is an indispensable part to design a tweeter in audio speaker applications. A band pass structure as a second order filter has been used extensively for frequency selection in both wireless transmitting and receiving applications.

Based on those different filter models, novel learning rules of new parameters can also be invented by choosing different appropriate Lyapunov functions. This work can be extended to more comprehensive adaptive filter structures in the future according to the demand of real applications.

8.2 Low Power Smart Dust Radio

Based on the current work accomplished in this dissertation, we propose several future research directions for the smart dust radio.

The ultra low power wireless network of smart dust has broad applications. The circuit performance or even functionality in extreme environments is critical in some specific applications. A temperature insensitive oscillator has been developed to stabilize the frequency fluctuation at different temperatures in this dissertation. Other blocks of the circuits such as the LNA or the power amplifier are also affected by temperature. Further research on the system operation in special environments is suggested for a robust implementation. How temperature influences the system and how to compensate the corresponding changes is an important topic in system realization.

The ultimate goal of the smart dust radio is to design wireless sensor networks as small as a dust. One centimeter cube is an initial step in achieving this point. Sharing the same available CMOS process between the transceiver analog circuits and digital communication circuits, we make it possible to integrate all the electronic parts on the same chip. In addition, the on-chip antenna is very useful minimizing the size of a single wireless sensor node. Customized shape of the large capacity battery is a feasible approach to finalize the design as well.

In regard to the circuit design of the transmitter and receiver, there are also some possible improvements to be made. The performance of the circuits is subject to the voltage change of the battery without a good voltage reference circuit. Moreover, several bias voltages need to be supplied by voltage dividers independent of the power supply variation. Voltage referencing is necessary between the battery and the implementation circuit to guarantee the functionality. A differential structure may be

more preferable to reject supply noise induced by the integration of digital blocks. All these improvements may significantly enhance the robustness of the system.

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