ABSTRACT

Title of Document:	NEW MATERIAL FOR ELIMINATING LINEAR ENERGY TRANSFER SENSITIVITIES IN DEEPLY SCALED CMOS TECHNOLOGIES SRAM CELLS
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As technology scales deep in submicron regime, CMOS SRAM memories have become increasingly sensitive to Single-Event Upset sensitivity. Key technological factors that impact Single-Event Upset sensitivity are gate length, gate and drain areas and the power supply voltage all of which impact transistor’s nodal capacitance. In this work, I present engineering requirement studies, which show for the first time, the tread of Single-Event Upset sensitivity in deeply scaled SRAM cells. To mitigate the Single-Event Upset sensitivity, a novel approach is presented, illustrating exactly how material defects can be managed in a way that sets electrical resistance of the material as desired. A thin-film high-resistance value ranging from 2kΩ/□-3.6MΩ/□, and TCR of negative 0.001%/°C is presented. A defect model is presented that agrees well with the experimental results. These resistors are used in the cross-coupled latches; to decouple the latch nodes and delay the regenerative action of the cell, thus hardening against single even upset (SEU).

NEW MATERIAL FOR ELIMINATING LINEAR ENERGY TRANSFER SENSITIVITIES IN DEEPLY SCALED CMOS TECHNOLOGIES SRAM CELLS

By

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Dedication

To those who have made this work possible, my parents and my children (Gikuyu, James and Githinji). Your patience with me as I engaged in this research was a great source of encouragement.

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The opportunity to do my research work at two premier institutions namely: the University of Maryland at College Park, Maryland, and at the Naval Research Laboratory in developing mitigation techniques for radiation hardening of deeply scaled CMOS technology is one I will always be grateful for. There are many people who inspired, guided and assisted me. I want to express my sincere gratitude to my adviser Dr. Martin Peckerar for choosing me as one of his students, and subsequent guidance in this research work. Thank you for all your support and guidance during my time at University of Maryland, College Park. Dr. Peckerar has been a mentor, a teacher and a unique source of encouragement. It has been both an educational and enriching experience to work with Dr. Peckerar and his Group here at the University. To the members of my defense committee, I am deeply indebted for the way you all agreed to serve in my defense committee and the constructive advice and information you offered to me.

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Special thanks go to Dr. Robert Walters of the Naval Research Laboratory and Dr. Rokutaro Koga of Aerospace Corporation of California, for their support in getting heavy ion radiation at Berkeley National Laboratory. The results of the heavy ion radiation experiments make the case of using the radiation hardening mitigation technique, using the material developed in this research indispensable.

To Dr. Michael Liu, I owe more gratitude than I can express, for doing everything possible to facilitate electrical characterization of $In_x Al_{1-x} N$ film resistor. To be more specific, it was Dr. Liu who guided in developing an encapsulation layer of film resistor at Honeywell Aerospace at Plymouth, Minnesota. His guidance and persuasion made it possible for the film to be allowed for characterization using the same tools that are used in the Honeywell's CMOS process. I would further like to express my gratitude for financial support from The United States Naval Research Laboratory, the people of Mathakwaini, Nyeri-Kenya, Mr. James Williams Sr., and Global Defense Technology and Systems. Finally, I pay special tribute to Mr. James Williams Sr., for his unwavering encouragement throughout my academic career.

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Chapter 1: Introductory Summary

Section 1.1: The Problem of Linear Energy Transfer Sensitivities

Subsection 1.1.1: Effects of Scaling on SEU Sensitivities

As the scaling of integration for memory circuits continue, the Single Event Upset (SEU) of logic states due to ionizing radiation is considered a basic limitation. In an SEU event, a single charged particle, (such as a cosmic ray, a recoiling nuclear reaction product) strikes a sensitive node of a memory cell and generates sufficient charge to change a logic state of the cell.

For a Static Random Access Memory (SRAM) cell, a useful hardening technique is to decouple the inverters with cross-coupling latch resistors. High value polysilicon resistors have traditionally been used to introduce the feedback delay [1]. When an SEU event disturbs a vulnerable node, the RC delay to the other inverter of the cell postpones the complete change of state of the cell, thereby giving the restoring "on" transistor time to source current, and recovers the disturbed node. For each single event which is characterized by the effective Linear Energy Transfer (LET) of the incident ion, there exists a value of RC feedback delay that would enable proper circuit recovery. The delay time is mainly determined by the characteristics of the resistor, since capacitance is expected to be tightly controlled [2] and is determined

by the technology node. Thus for deeply scaled technology node, large resistor value is required to increase the delay time.

As technology scaled below 0.25 microns, some manufacturers replaced the feedback resistor approach with transistor hardened SRAM cells. The factors which dictated the transition are: (1) Unreliable manufacturing process for a high-value resistor creating large variations of resistance, (2) High temperature coefficient of resistance (TCR) of polysilicon material in temperature range between -55˚C and 125˚C, (3) Large-value resistors occupied considerable chip space which is incompatible with high density requirement.

The goal of this work is to manufacture a resistor which offers high sheet rho, has very low temperature coefficient of resistance, be thermally stable and be compatible to CMOS process in deeply scaled technologies. Results presented in chapter 3 show that a thin-film high-value resistor has been fabricated that is scalable in magnitude to offer resistor values ranging from 2kΩ/□ to 3.6MΩ/□. Furthermore, the resistor film has very low TCR of 0.0116%/°C. The principle guiding the resistor growth is dependent on choosing the material defects, namely the point defects, extended defects and the DX centers. Because the conductivity of the material is determined by the nature and amount of the defects, there is no area penalty suffered in using high resistance value. This resistor film has enormous implications for radiation hardening of highly scaled integrated circuits (ICs). Plans are underway to integrate the resistor film in 180 nm, 90 nm, 45 nm and 40 nm technologies.

Subsection 1.1.2: SEU Mitigation Using Cross-Coupled Latch Resistor

When an energetic particle strikes a sensitive region in an SRAM (typically the reverse-biased drain junction in the "off" state n-channel transistor), charge collection at the junction results in a transient current in the struck transistor [3]. As the current flows through the struck transistor, the restoring p-channel transistor attempts to source current in an effort to balance the particle-induced current. Figure 1.1 below illustrates the two competing processes. However, the restoring transistor has a finite channel conductance causing the current through the restoring transistor to induce a voltage drop at its drain. The induced voltage transient in response to the single event current transient provides the mechanism that causes the upset in SRAM cell. The voltage transient is analogous to a write pulse and it is what causes the wrong memory state to be latched into the memory cell.

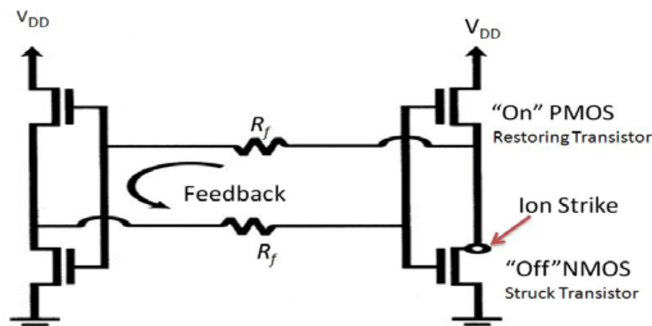


Fig. 1.1: Competition between the feedback process and the recovery process determines the SEU response of SRAM cells

The four transistor drain nodes interior to the SRAM are the possible locations that are sensitive to SEU strike. In figure 1.2, the strike and the recovery of the node is illustrated. The recovery time (τ_R), is the time needed to recover following an ion strike. It provides a measure of the ion induced voltage transient. Physically it is the

time required to dissipate the deposited charge. Following the ion strike, the circuit takes time (τ_F) to respond to the voltage transient triggered by the ion strike. τ_F is primarily determined by the size feedback resistor and the nodal capacitance.

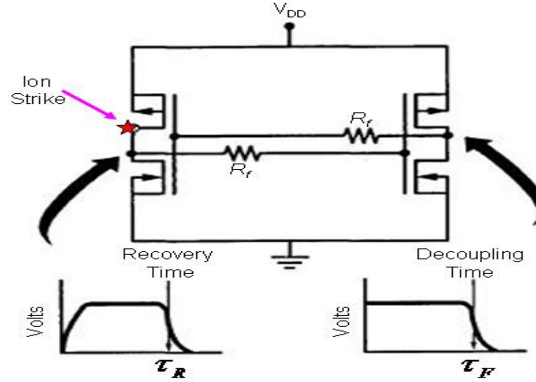


Fig. 1.2: τ_R is the time required for charge to dissipate following the ion strike. τ_F is a measure of circuit response and is determined by the value of R_F. That is, $\tau_F = R_F C$.

For the purpose of radiation hardening, τ_F is a design parameter. In the SRAM memory design, the feedback resistor is used to increase τ_F, holding the circuit from responding until well past the τ_R. The threshold occurs approximately when $\tau_R = \tau_F$. When considering charge collection process, it is important to consider whether the struck junction is located inside a well or in the substrate because the well substrate junction provides a potential barrier that prevents charge deposited deep within the substrate from diffusing back to the struck drain junction. For instance, for an outside-the -well "off" strike, since the struck drain is not located in the well, charge deposited deep in the substrate can diffuse back to the drain junction. Such a node provides for the most sensitive strike location [4]. For an inside-the-well "off" strike, the initial drift current pulls down the struck node potential, triggering the upset

process. As the transient progresses, the holes deposited in the p-well are collected at the p-well ties, raising the well potential and leading to injection of the electrons by the source.

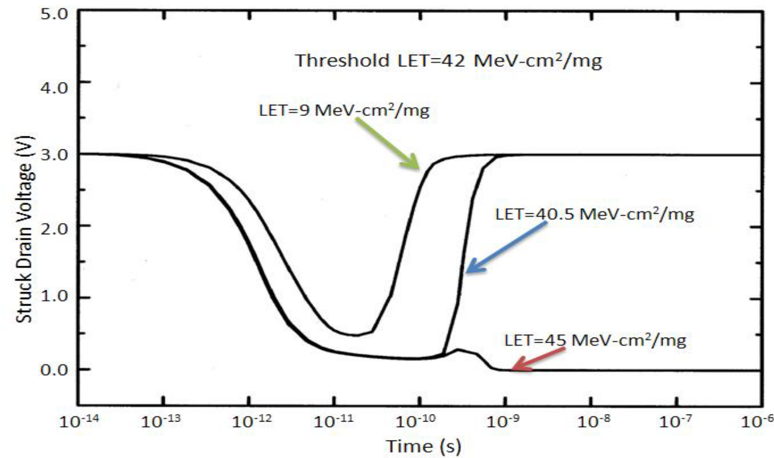


Fig. 1.3: The struck drain voltage transient for the ion strike with LET well below, just below and just above the SEU threshold. Even the ion strike with LET well below threshold is capable of causing momentary flip the voltage of the struck node [5].

The effect is initiation of the inside-the-well bipolar action. Electrons collected by the substrate do not contribute to upset because the substrate is connected to V_{DD}. Nonetheless, electrons collecting at the n-drain constitute a bipolar current in the same direction as the initial photocurrent and do contribute to the upset process [6].

Figure 1.3 above shows how even an ion particle strike whose energy is way below the upset threshold can still cause a momentary voltage flip at the struck node. Whether an observable SEU occurs depends on which happens faster: the feedback of the voltage transient through the opposite inverter or the recovery of the struck node voltage as the single event current pulse dies out. While the drift process is

responsible for the rapid initial flip of the cell, the long term charge collection by diffusion prolongs the recovery process. From view of technology, the recovery time depends on restoring transistor current drive and the minority carrier lifetimes in the substrate [7], [8]. The cell feedback time is the time required for the disturbed node voltage to feedback through the cross-coupled inverters, and latches the struck device in the flipped state. This time is related to the cell write time and in its simplest form, it can be viewed as the RC delay in the inverter pair. We observe that this RC time constant is a critical parameter in determining SEU sensitivity in SRAM in that the smaller the RC delay, the faster the cell can respond to voltage transients including write pulses and hence more the SRAM is susceptible to SEUs.

Subsection 1.1.3: Effect of Technology Scaling on Charge Sharing

One of greatest concerns of SEU is how technology trends continue to impact device susceptibility. Deep scaling affects radiation hardening strategies, an issue that has become of great interest for ground-based as well as aircraft microelectronics. Important technology parameters that continue to influence SEU sensitivity include: gate length, gate and drain area and power supply voltage.

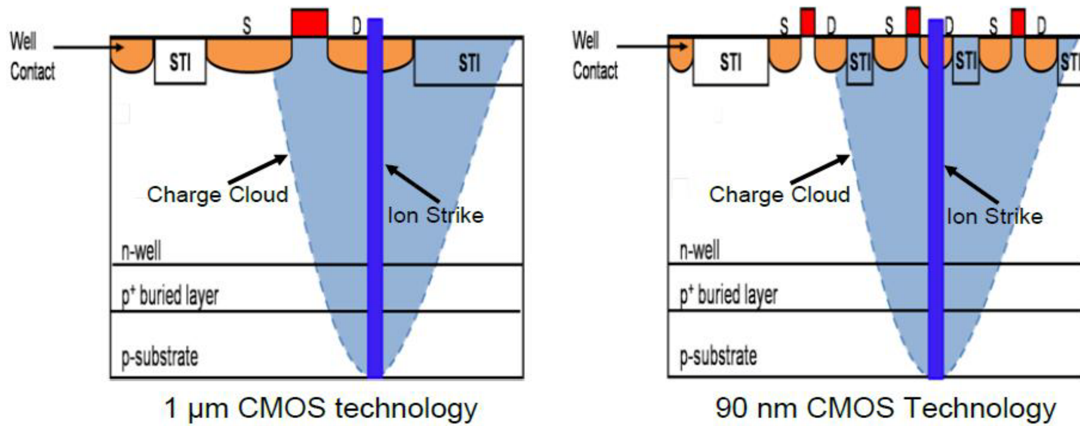


Fig. 1.4: Comparison of charge cloud following an ion strike in a 1μm and 90nm technologies. In 90nm node, charge cloud created by an ion strike is easily shared between two adjacent cells.

With technology scaling, the SRAM junction area has been minimized to reduce capacitance, leakage and cell area. However, the cell junctions are now much closer to each other such that a strike that may only have affected one note in 1μm technology node is now capable of affecting several nodes in 90nm technology node. The phenomena is illustrate in figure 1.4 above and figures 1.5 and 1.6 below.

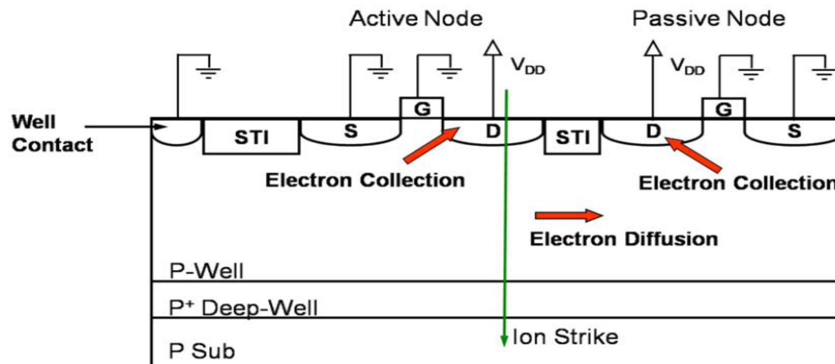


Fig. 1.5: Nodal charge sharing as transistor density has increased

As a consequence of technology scaling, more and more transistors are close together, resulting in charge sharing among the nodes (shown in figure 1.5) and the parasitic bipolar action which can greatly influence the amount of charge collected.

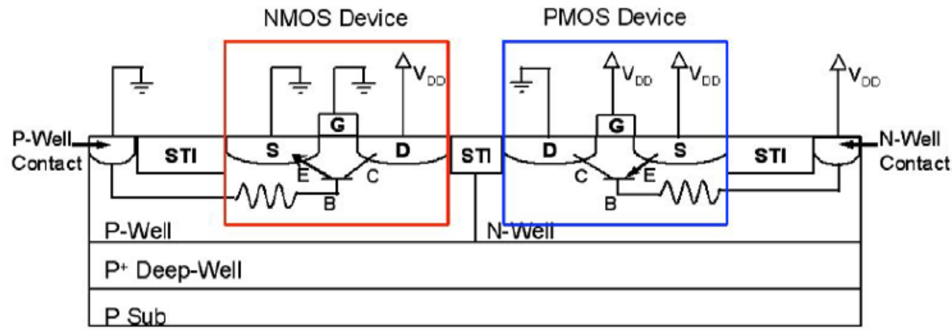


Fig. 1.6: Parasitic bipolar effect. NMOS has NPN while PMOS has NPN

Analysis of possible charge sharing induced SEUs is presented in chapter 2 based on heavy ion irradiation experiment that was recently concluded at Lawrence Berkeley National Laboratory. Direct ionization is the primary charge deposition method for upsets caused by heavy ions, where a heavy ion is considered to be any ion with atomic number equal or greater than 2.

Section 1.2: Controlling Material Defects to Growth High-Value Resistors

Subsection 1.2.1: Background of Atomic and. Electronic Defects

In all semiconductors materials, lattice defects change the electronic properties of the material locally, and this result in electronic energy states in the band gap of the semiconductor. Semiconductor technology actually relies completely on this fact. When we dope a semiconductor, we incorporate extrinsic point defects in predetermined concentrations, in defined regions of the crystal. Defects can have one or more energy states in the band gap of its host semiconductor. Such states could then be occupied by one or more electrons, not occupied at all. It is worth to note the difference between atomic defects as opposed to electronic defects. While intrinsic atomic defects are generally thermally excited, electronic defects can be can be

thermally or optically excited. Persistent Photo Conductivity (PPC) occurs as a result of optical excitation. Another major difference between atomic and electronic defects is that while atomic defects are typically considered in reference to physical position in the lattice, and their concentration can be directly related to the number of atoms, electronic defects are referenced to the density of electronic states of a given energy per volume of a crystal which is not a constant quantity but one that changes with temperature and composition.

Subsection 1.2.2: Role of Atomic and Electronic Defects

Atomic defects arise from doping whether it is intentional or not. In the indium aluminum nitride thin-film resistor, the silicon is the intended dopant. Silicon substitutes for aluminum and indium in the binary AlN and InN compounds, and it was established to do the same in the ternary $In_xAl_{1-x}N$ compound. It is very difficult to purify nitrogen which is used for the growth on the nitride. In the past, InN film grown by RF sputtering has shown very high concentration of oxygen and we determined that to be case for RF magnetron sputtered grown $In_xAl_{1-x}N$ film. Oxygen substitutes for nitrogen. If the growth processes is nitrogen deficient, the material is likely to have a high concentration of nitrogen vacancies, providing readily available sites that oxygen can occupy. The resulting effect is to increase oxygen solubility limit in the material. Similarly, if the growth processes in deficient of aluminum or indium compared to the concentration of nitrogen, there is a sharp increase of aluminum/indium vacancies which increases the solid solubility of silicon because more lattice sites are available.

The formation atomic and electronic defects can be understood based on Pauling's Rules [9]. For structures with large fraction of ionic bonding character, minimum electrostatic energy is achieved when cation-anions attractions are maximized and like-ion electrostatic repulsed minimized. In other words, cations are surrounded by the maximum number of anions as the first nearest neighbors and vice versa. However, either cations or anions seek maximum separation from other cations or anions as their second nearest neighbors. Consequently, when sufficient anions are not available to shield cation or vice versa, charged electronic states will form as immobile defects in place of the missing anion or cation. These defects do not anneal out during annealing steps since they are part of the total electrostatic energy balance and their concentration is a function of the coordination number of the anion or cation they are shielding.

Point defects in solid solution can also associate that binds them together as a pair or as a set. An example of such an association can be expressed as:

$$Si_{Al}^{\bullet} + V_{Al}^{'''} = \left(Si_{Al}^{\bullet} - V_{Al}^{'''}\right)^{''} \tag{1.1}$$

$$2Si_{Al}^{\bullet} + V_{Al}^{'''} = \left(2Si_{Al}^{\bullet} - V_{Al}^{'''}\right)^{'} \tag{1.2}$$

$$3Si_{Al}^{\bullet} + V_{Al}^{'''} = \left(3Si_{Al}^{\bullet} - V_{Al}^{'''}\right)^{x} \tag{1.3}$$

In such defect association, the aluminum vacancies would compensate the silicon dopant. If we were to assume that they system had no other defects except these two, the presence of the aluminum vacancies would set the low limit of the sheet rho

because for $In_xAl_{1-x}N$ to be conductive, the atomic-electronic defect complex formation would have to be first satisfied when such defect association leads to lower energy state of the system.

In $In_xAl_{1-x}N$ material, nitrogen used in the growth process may have oxygen impurity. During growth process, impurity oxygen is preferentially incorporated in the film because formation of In_2O_3 leads to a lower energy state as compared to InN. The chemical reactions of these two compounds are given as:

$$2In + 3O \longrightarrow In_2O_3 + \Delta H_{In_2O_3} \qquad (1.4)$$

$$In + N \longrightarrow InN + \Delta H_{InN} \qquad (1.5)$$

where $\Delta H_{In_2O_3}$ is -222.47kCal./mol and ΔH_{InN} is -4.8kCal./mol at 25°C.

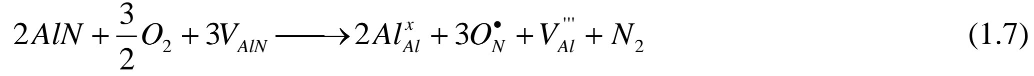
As reactions (1.4) and (1.5) take place, oxygen readily occupies the nitrogen site, releasing electrons as follows:

$$\frac{1}{2}O_2 + V_N^x \longrightarrow O_N^{\bullet} + e \qquad (1.6)$$

The electron released when oxygen atom occupies a nitrogen vacancy is free to roam around and can participate in electrical conduction.

The interaction of oxygen with aluminum vacancies has significant effect in controlling the material electrical conductivity. Let us consider the reaction of aluminum with oxygen in absence of aluminum vacancies. The oxygen defect is based on octahedrally coordinated aluminum atoms. However, at lower nitrogen concentration, the materials consists of oxygen atomic defects surrounded by

aluminum vacancies as proposed by Slack [10, 11]. The defect formation can be represented in Kroger-Vink notation as follows[10]:



$$2AlN + \frac{3}{2}O_2 + 3V_{AlN} \longrightarrow 2Al_{Al}^{x} + 3O_N^{\bullet} + V_{Al}^{'''} + N_2 \qquad (1.7)$$

In the reaction above, oxygen is shielded by the aluminum vacancies the ratio of 3:1. The implication to electrical conductivity is twofold: 1), the defects shielding of the oxygen atoms limit restricts formation of highly insulating Al_2O_3, and 2), those aluminum vacancies are no longer able to compensate silicon donor dopant.

Subsection 1.1.3: Role of Lattice Defects (DX Centers)

A DX center has a large energy barrier for the capture of an electron leading to a non-equilibrium occupation of electron levels at low temperature. Its existence can be viewed as a vacancy-interstitial pair at a threefold coordinated site. It is highly localized and negatively charged following capture of an electron. The vacancy-interstitial bond is like sp^2, and it has been suggested that the metastability of point defects is an intrinsic property of sp-bonded semiconductors [12]. Other than atomic or electronic defects that we have already encountered, $In_xAl_{1-x}N$ material has lattice defects also known as DX centers. Studies on the electronic properties of group-IV such as Si, Ge and Sn or group-VI dopants such as S, Se and Te , as substitutional dopants in III-V ternary semiconductors alloy systems [12-15] show that the donor gives rise to two electronic states: 1), the shallow level with normal substitutional configuration and, 2), a localized state (DX center) which arises from a lattice distortion at or near the donor atom. The atomic distortion that leads to the formation of the DX, involves a large lattice displacement which causes the breaking of a

donor-lattice bond. This lattice displacement in turn causes appearance of energy barriers for electron capture onto the emission from the localized state.

The following are some important common characteristics of DX centers:

1) DX is present in n-type material regardless of the choice of the donor.
2) The number of DX centers is of the same order of the number of donor atoms [16, 17].
3) DX centers determine the carrier concentration because DX formation leads to capture of an electron from two substitutional sites
4) DX is the dominant electron trap [16, 18, 19], with electron capture and emission being thermally activated.

It follows that the main contribution of these traps is compensating donor impurity, significantly reducing the number of ionized impurity in the material. Compensation of free carriers, thermal binding energy of the dominant donor level and the concentration of vacancy defects strongly depend on the ternary alloy composition. To make the film conductive, the approach is to alloy aluminum with indium. When silicon occupies indium site $Si_{In}^{\bullet}$, the $(Si-N)$bonds are less strained given that indium has a much larger ionic radius. The larger ionic radius also means that indium has weaker electrostatic attractions with its first nearest neighbors and hence the bonds are much less strained and therefore not prone to DX formation. Furthermore, indium can be coordinated with 4, 6 or 8 first nearest neighbors while the coordinated number for aluminum is 4 when surrounded by nitrogen and 6 if its first nearest neighbors are oxygen.

Section 1.3: Engineering Requirement Deeply Scaled CMOS SRAM Cells

Subsection 1.3.1: Pspice Analysis for Single Event Upsets

In this section, it is shown that the size of cross-coupling feedback resistor can be determined early in during the circuit design phase. The determination can be done without incurring the cost associated with the 3D simulation and even more importantly, it does not need to wait for device post-characterization.

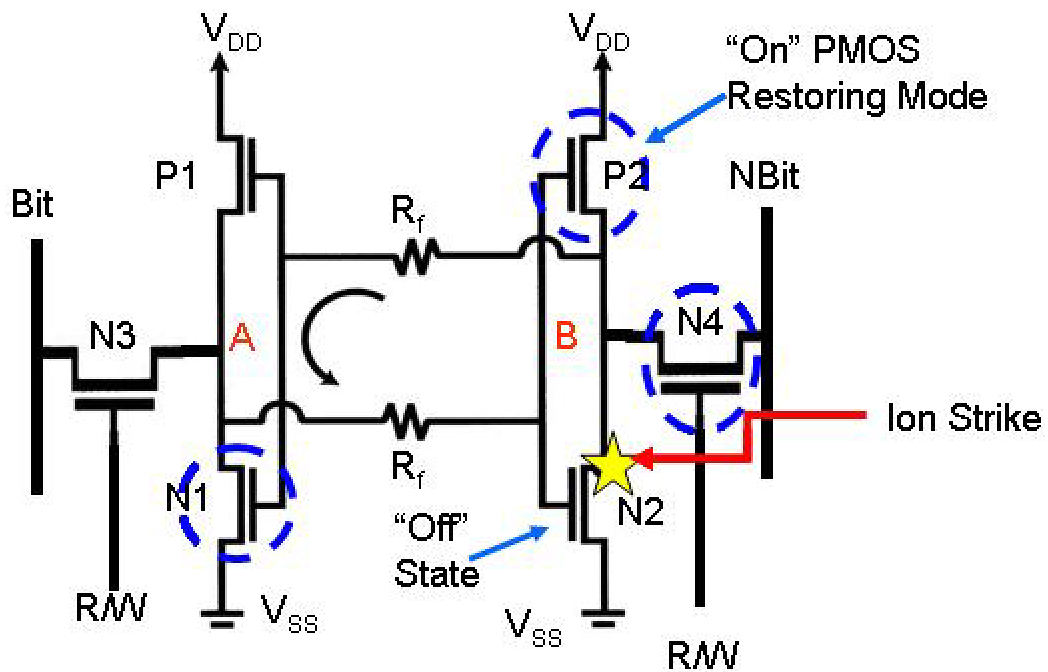


Fig. 1.7: Hardened 6T-SRAM studied in for Pspice simulation. The circuit was the same topology used in heavy-ion and pulsed-laser irradiation

The circuit shown in figure 1.7 above was used for modeling feedback resistor and it was the same topology as the 4M SOI SRAM exposed to heavy-ion and pulsed-laser irradiation. We discuss the results of heavy-ion and pulsed-laser irradiation in chapter 2. With this model, the voltages of nodes A and B have the same standard exponential

behavior with time, as does any RC system. For example, node discharging is described by:

$$V(t) = (V_0 - V_i)e^{-t/RC} + V_0 \qquad (1.8)$$

while the node charging is modeled by:

$$V(t) = (V_i - V_0) \times (1 - e^{-t/RC}) + V_0 \qquad (1.9)$$

where

V_i voltage transient resulting from ion strike

V_0 initial capacitor voltage ($0V<V_0<V_{dd}$)

R is the R_F

C equivalent inverter input capacitance (N and PMOS gate capacitance)

Subsection 1.3.2: Procedure for Pspice Simulation

The ion strike was simulated by a current (i) pulse which had a triangular shape of the same size of the base. The magnitude of the deposited charge was varied by changing the height of the triangle which was the current's amplitude. Using the IBM's Process Design Kit, I simulated the resistor requirement for effective mitigation of 180nm, 130nm and the 90nm CMOS SARM technologies. The results are shown in figure 1.8 below. We observed that although SRAMs built with 130 nm are less sensitive to low LET strikes compared with 90 nm technology, 130 nm technology SRAMs are more sensitive to high ion strikes of LET of 90MeV-cm^2/mg and above. This observation was not expected. Indeed, SRAM design using 130nm technology is also more sensitive than 180 nm technology. To mitigate against these soft errors, the simulation

shows that an SRAM made on 180 nm technology requires 200 kΩ resistor to forestall an upset, 130nm technology requires 1.2 MΩ resistor and 90 nm needs a 400 kΩ resistor.

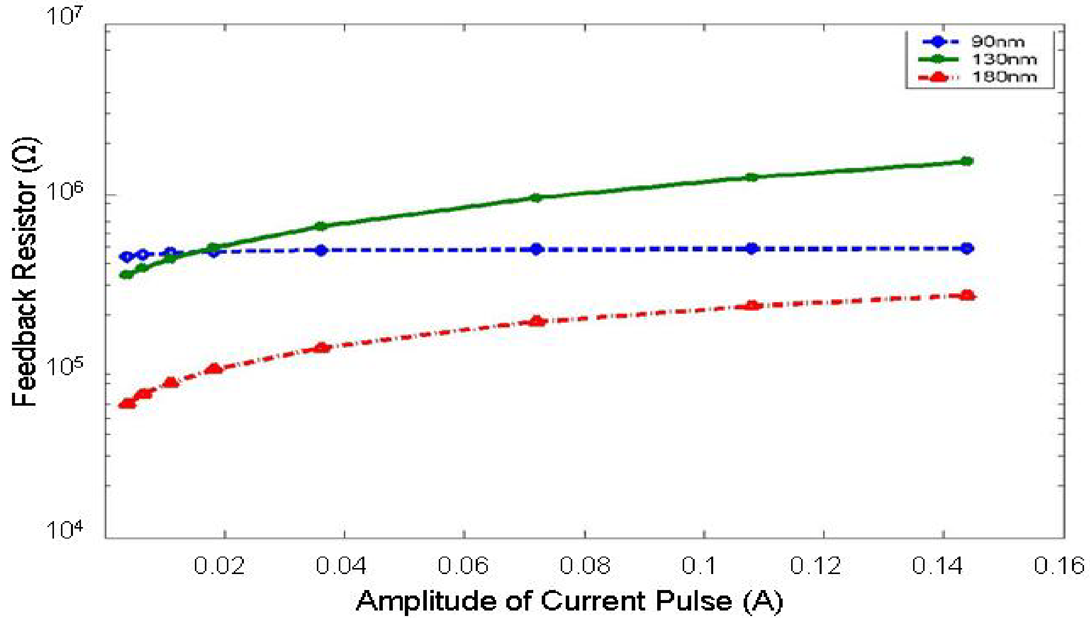


Fig. 1.8: Comparison of feedback resistor values for 180 nm, 130 nm and 90 nm technologies.

<u>*Subsection 1.3.3: Effect of Technology Scaling*</u>

The three technology SRAM were then simulated with the $R_F = 0$. Choosing the same amount of current, four different ionizing particles were simulated to establish how long a transient could last. The data is tabulated in table 1.2 below. It is shown that for these deeply scaled technology SRAMs, all transient last but for only a few picoseconds. If for instance we consider a 97 MeV-cm2/mg ionizing particle striking a 90 nm SRAM cell, all that is needed to determine the size of RF is the gate-drain capacitance of transistors P1 and N4. For this technology, this capacitance is a fraction of a femto farad.

Table 1.1	
90 nm Technology	
LET Threshold	Transient Duration
20 MeV-cm^2/mg	2.91 ps
40 MeV-cm^2/mg	3.38 ps
60 MeV-cm^2/mg	3.79 ps
97 MeV-cm^2/mg	4.328ps
130 nm Technology	
20 MeV-cm^2/mg	2.08 ps
40 MeV-cm^2/mg	2.24 ps
60 MeV-cm^2/mg	2.30 ps
97 MeV-cm ^{2}/mg	2.68 ps
180 nm Technology	
20 MeV-cm^2/mg	1.32 ps
40 MeV-cm^2/mg	1.59 ps
60 MeV-cm^2/mg	1.76 ps
97 MeV-cm^2/mg	2.23 ps

Single-event upset Transient duration for different technology nodes

The circuit response time is delayed by:

$$R_F C = \tau \tag{1.10}$$

where τ is the transient duration. If for example the nodal capacitance is 0.2fF, it requires a cross-coupled feedback resistor of 21.6 kΩ to mitigate a transient that lasts for 4.328ps. If capacitance is less, even a larger resistor would be required.

Section 1.4: Contribution:- New Material for Mitigating LET Sensitivities

Subsection 1.4.1: $In_xAl_{1-x}N$ Material Growth

Mitigating deeply scaled CMOS technology SRAM cells from linear energy transfer sensitivities requires feedback cross-coupled latch resistors of very high value, low temperature coefficient of resistance and capable to be integrated in CMOS process with the least possible intrusion into the CMOS process. For deeply scaled submicron

technologies, the nodal capacitance is within a fraction of femto farad range. Engineering design requirement show that a typical transient last for only a few picoseconds. To hold the circuit in the original state until the transient dies out, a cross-coupled resistor in tens of kilo-ohm/sq is required. I have successfully fabricated this resistor, with resistance ranging from 2kΩ/ □ to 3.6MΩ/□, and TCR of negative 0.0012%/°C. Because the thin -film is grown at room temperature, the growth process guarantees compatibility with CMOS process.

Subsection 1.4.2: Resistor Definition and Delineation

The resistor film was patterned using Chlorine/Argon plasma which is commonly used in etching silicon nitride in CMOS. The etch recipe is fully compatible with CMOS process, provides for minimal intrusion in the CMOS process

Subsection 1.4.3: Resistor Annealing Encapsulation

To protect the resistor from encroaching hydrogen, an effective encapsulating layer of silicon nitride was developed. The encapsulating layer is grown using low temperature PECVD. With this encapsulating layer, the resistor value and the temperature coefficient of resistance were effectively maintained even after two annealing cycles of 410°C lasting for a total of six hours.

Section 1.5: Contribution:- Determination of Engineering Requirements

Subsection 1.5.1: Engineering Requirement for 180 nm CMOS SRAM Cell

I present engineering design requirement for effective mitigation of SEU sensitivities 180 nm CMOS technology SRAM cells. At the limiting cross-section, the analysis shows that a cross-coupled etch resistor of more than 200kΩ is required.

Subsection 1.5.2: Engineering Requirement for 130nm SRAM Cell

I present engineering design requirement for effective mitigation of SEU sensitivities in 130 nm technology node SRAM. 130 nm technology node is more sensitive to SEU sensitivities. At LET of 97 MeV-cm2/mg, this node would need a cross-coupled resistor of more than 2MΩ and even that is not sufficient since it is does not appear to reach limiting cross-section

Subsection 1.5.3: Engineering Requirement for 90 nm SRAM Cell

Engineering design requirement for 90nm CMOS technology SRAM node is presented. For this node, I show that for effective mitigation of single event upsets, a resistor of 400kΩ is required. If for instance alloy composition yielding sheet rho of 30kΩ/□ is chosen only 13 squares would be needed. A comparison with a lightly doped polysilicon resistor with typical sheet rho of 200Ω/□, 2000 squares would need to be used. To account for temperature variation, the resistor must be increased by a factor of ×4, which means that over 8000 squares would be needed. Such huge resistor would consume significant amount of die space and would simply not be practical.

Section 1.6: Contribution: New Approach to SEE Testing

Subsection 1.6.1: Complete Removal of Silicon Substrate

I present new approach to SEE testing which is necessary for deeply scaled technologies. As technology scaling continues, SRAM cell requires very small charge deposition to change state. For 90 nm SOI-SRAM, irradiation with heavy ion revealed upset even for the lowest energy ion at LET of only 0.89 MeV-cm^2/mg. To qualify this part, a new approach was required that would accurately determine the charge deposited, eliminating difficulties related to range and straggle. To overcome these difficulties, I have developed a technique whereby the silicon substrate is completely removed by use of the xenon difluoride (XeF_2) [20]. The selectivity ratio of Si to SiO_2 is 1000:1 and therefore, the buried oxide acts as a natural etch stopper. The complete removal of the substrate provides direct access to the sensitive volume by heavy ions and protons. The technique facilitates use of low energy ion accelerators, micro-beams and low energy protons.

Subsection 1.6.2: Smaller Spot-size Absolutely Critical for Submicron Cells

Complete substrate removal approach allows use of single photon absorption. The ability to use single photon absorption offers potential for use of smaller spot size which leads to accurate knowledge of charge deposited. The procedure permits direct comparison of single photon absorption, two photon absorption and low energy proton irradiation. As technology continue to scale deeper in submicron regime, SEE

testing will demand testing the devices with lower ionizing particles that will not be available in higher energy accelerators. Currently, there are only a few places available in world where these low energy accelerators are available.

Subsection 1.6.3: Ability to use Low Energy Accelerators and Protons

As technology scales further in submicron regime, current SEE testing facilities will no longer be useful for parts qualification because devices continue to upset from ionizing particles of extremely low energy. For 90 nm SOI 4M SRAM, the device was found to upset even at 0.89 MeV-cm^2/mg which was the lowest available ion of 10 MeV/amu cocktail. To address this challenge, I have demonstrated a new approach to SEE testing where a silicon substrate is completely removed, providing for direct access to the sensitive area. By removing the substrate, a known amount of charge can be deposited at the sensitive area using low energy proton, neutron or heavy ion, providing means of establishing the threshold of upset due to SEU. Such capability has not been available until now.

Chapter 2: Engineering Design Requirements

Section 2.1: Causes of Ionizing Radiation

Subsection 2.1.1: Cosmic Rays

The three main sources of cosmic rays are Solar Cosmic Rays, Galactic Cosmic Rays and the Terrestrial Cosmic Rays. The Galactic Cosmic Rays are believed to have originated somewhere outside the solar system and are assumed to be remnants of nova and supernova explosions. The major constituents of Galactic Cosmic Rays are the protons and alpha particles which represent 83% and 13% respectively. The remaining particles are largely constituted of heavy ions which are highly energetic and generally cannot be stopped by spacecraft shielding. Consequently these heavy ions while few in percentage composition are highly potent in causing SEEs in electronic components. The Solar Cosmic Rays consists mainly of protons, but they too have helium and heavier elements. The Terrestrial Cosmic Rays originate from the earth's atmosphere and have protons, neutrons, pions, muons and electrons.

Space radiation environment is a major consideration when designing electronic components for use in space. The importance of the challenge posed by radiation environment is highlighted by the unavailability of replacement or repair for these components in the event of failure. Consequently research of survivable electronics due to harsh radiation environment is of critical importance when consideration is made on the criticality of space missions, with particular emphasis to system

availability and reliability. The main contribution to space radiation comes from cosmic rays, solar flares and trapped radiation such as Van Allen belts. Each of these radiation components becomes significant for particular mission depending on the satellite's orbit and orientation.

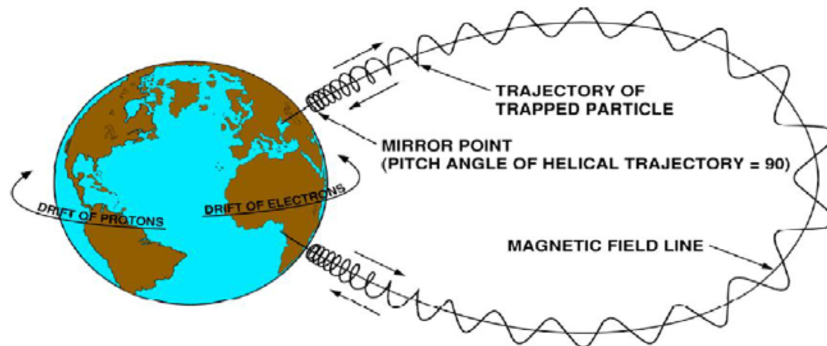


Fig. 2.1: Motion of particles in the Earth's magnetosphere [21].

The earth's magnetic field can affect the trajectory of charged particles evolving in the near-earth space. Some charged particles become trapped in the geomagnetic field lines and follow relatively predictable and stable trajectories as shown in figure 2.1 above. The trapping phenomenon leads to an accumulation of particles in specific areas of the magnetosphere commonly referred to as the Van Allen Belts, named appropriately after Van Allen who discovered them. Recent work has shown that there are two radiation belts; the inner and an outer belt. The distribution is shown in figure 2.2 below. The inner belt extends up to 2.5 Earth radii, where one earth radius is 6380 km. This belt consists of energetic protons of up to 600 MeV and electrons of several MeV energy.

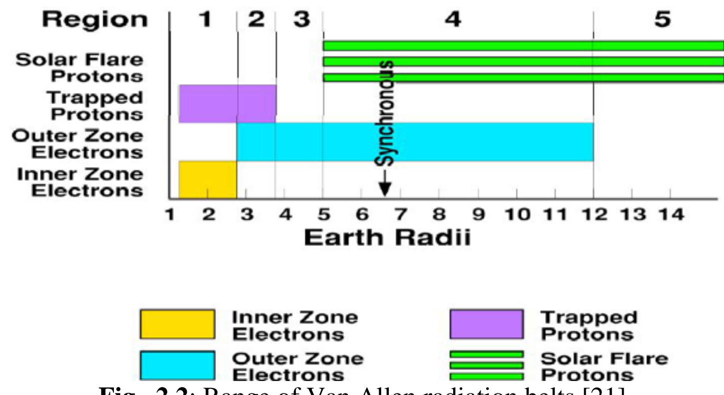


Fig. 2.2: Range of Van Allen radiation belts [21].

Although the origins of these trapped particles are not well understood, they are believed to originate from solar flares, Galactic Cosmic Rays (GCR) from interplanetary space as well as reaction products of GCR with nuclei atoms in the earth's upper atmosphere.

The proton belt is major source of single event effects (SEE) for spacecrafts because these protons have fairly long range. The South Atlantic Anomaly is associated with the proton belt. It exists because of the tilt of the earth's magnetic pole from the geographic pole and the displacement of the magnetic field from the center, causing a dip in the earth's magnetic field over the South Atlantic Ocean. The dip results in a bulge at the underside of the inner belt, thus allowing cosmic rays and other charged particles to reach lower into the atmosphere causing a major spike in proton flux of energy greater than 30 MeV. The proton flux causes significant SEE for satellites, aircrafts as well as satellites flying in the area.

Another important constituent of ionizing radiation is the flux of neutrons. Neutrons originate from galactic cosmic ray events. When galactic cosmic rays interact with

the Earth's atmosphere, they produce complex cascade of secondary particles which in turns penetrate deep into the atmosphere, creating tertiary particle cascades. At terrestrial altitudes, there is high concentration of protons, muons, neutrons and pions, of which less than 1% is said to reach the sea level [22]. Neutrons exist in proportionately higher percentage. Because neutron reactions have higher LETs, their contribution for SEUs in devices used for terrestrial applications is much higher. The neutron flux is strongly dependent on altitude and it increases with altitude; for instance, a rise in altitude from sea level to 10 000 ft, the neutron cosmic ray flux increases by a factor of 10. This tread is maintained and starts to saturate at 50 000 ft [23], [24]. However, the concern is no longer just for terrestrial applications. There is sufficiently high level of neutron concentration even at sea level. Figure 2.3 below shows the cosmic differential neutron flux at sea level. It shows how many neutrons over the given energy range are incident on a device at sea level.

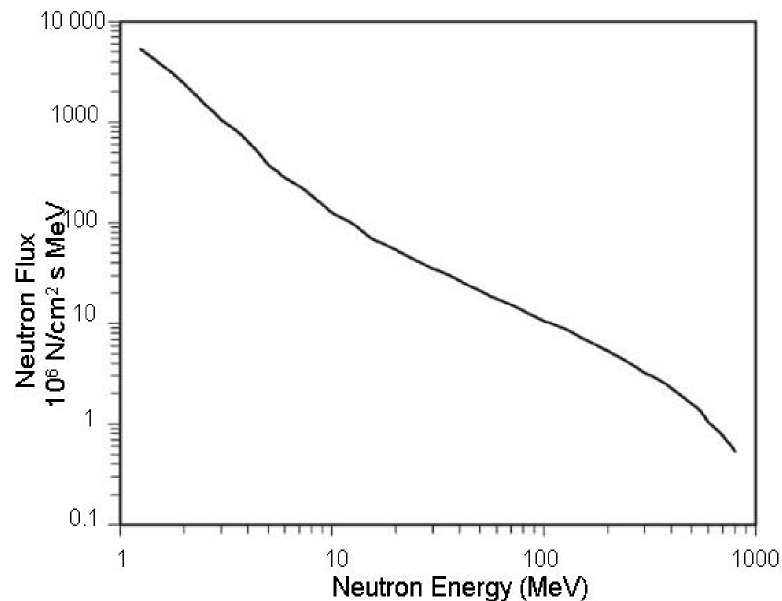


Fig. 2.3: Cosmic ray differential neutron flux as a function of neutron energy at sea level [22, 25].

The table 2.1 below summarizes some of the reaction products that arises when neutrons interact with a silicon nucleus [26].

Table 2.1

Reaction Product	Threshold Energy (MeV)
$^{28}Al + p$	4.00
$^{27}Al + d$	9.70
$^{24}Mg + n + \alpha$	10.34
$^{27}Al + n + p$	12.00
$^{26}Mg + {}^{3}He$	12.58
$^{21}Ne + 2\alpha$	12.99
$^{25}Mg + \alpha$	2.75

Reaction products and threshold energies for $n + {}^{28}Si$ reactions [25].

Unlike alpha particles and other heavy ions, shielding is not a practical means of mitigating soft errors. To put the challenge of shielding against neutron in perspective, concrete has been shown to shield cosmic radiation at an approximate rate of 1.4× per foot [27]. It is simply not practical to use shielding against upsets from cosmic radiation. Cosmic ray induced SEUs must be dealt by reducing device sensitivity which is the subject of this thesis.

Single Event Effects (SEE) in microelectronic devices is caused when a highly energetic particle such as protons, neutrons, alpha particles or other heavy ions strike a sensitive region of a circuit. Depending on several factors, a ionizing particle may do any of the following: it may cause no observable response, it may cause a transient disruption of the circuit operation, may cause a change of logic state or even cause a

permanent damage to the device or the integrated circuit. Cosmic ray induced upsets were reported as early as 1975 [28] in a bipolar J-K flip-flop operating in a communication satellite. A few years later, the occurrence of soft errors in terrestrial microelectronics was reported [29]. While earlier researchers attributed memory upsets to direct ionization [28], [30], at NSRE conference in 1979, it was reported that memory upsets had been caused by proton and neutron indirect ionization effects [31], [32].

Subsection 2.1.2: Direct Ionizing Radiation

There are two primary methods by which ionizing radiation releases charge in a semiconductor device: direct ionization by the incident particles itself and ionization by secondary particles created by nuclear reactions between the incident particle and the struck device. In this section, I address the direct ionization mechanism. When an energetic charged particle passes though a semiconductor material, it frees electron-pairs along its path as it losses energy. When all its energy is lost, the particle comes to rest in the semiconductor having travelled a total path length referred as the particle's range. This interaction between the energetic particle and the travelled path is illustrated in figure 2.4, which shows the energy deposition by a chlorine ion, with energy of 210MeV in silicon. The graph is plotted using the Stopping and Range of Ions in Matter (SRIM) code[33]. Within the radiation community, the term linear energy transfer (LET) is frequently used to describe the energy loss per unit path length of a particle as it traverses through a material. LET is dependent on the mass and energy of the particle as well as the target material. It has units of MeV/cm^2/mg

because the energy loss per unit length in MeV/cm is normalized by the density of the target material (in mg/cm^3). By normalizing the energy loss per unit length with the density of the material, the LET is conveniently quoted independent of the target material.

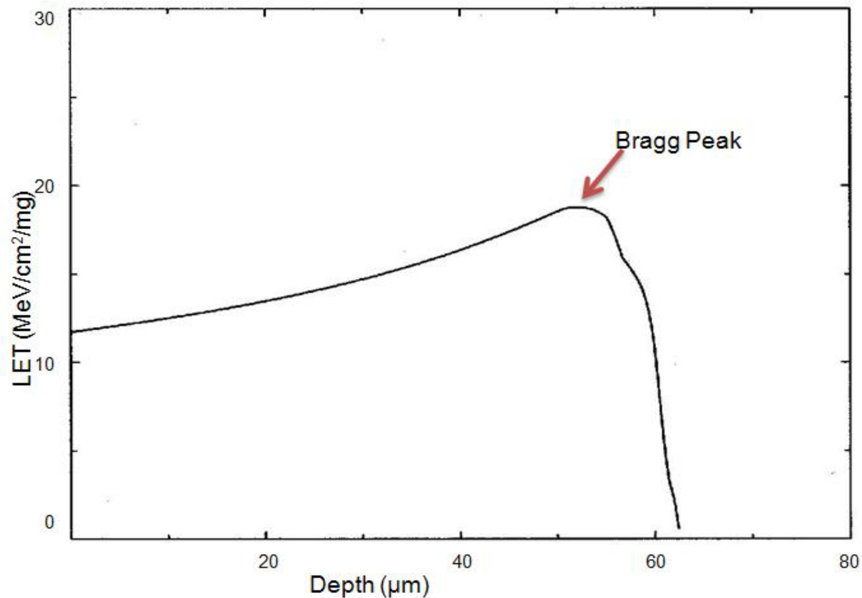


Fig. 2.4: LET versus depth for 210-MeV Chlorine ions in silicon target [5]

We can relate the LET of a particle to its charge deposition per unit length. In silicon, an LET of 97 MeV-cm^2/mg corresponds to a deposition charge of 1 pC/μm. Charge collection generally occurs within a few microns of the junction. Typically, the collected charge (Q_{coll}) during these single events is from 1.3 to several 100fC depending on the ion type, ion trajectory and its energy over the path through or near the junction. In silicon substrate, one electron-hole pair is produced for every 3.6eV of energy lost by an ion.

The reverse-biased junction is the most charge-sensitive part of the circuit. This is especially if the junction is floating or weakly driven by a small drive transistor or high resistive load sourcing current to maintain the node at its current state. Figure

2.5 below shows what typically happens during ionizing radiation event. At the onset, part (a) shows a cylindrical track of electron-hole pairs of a submicron radius and a very high charge concentration that forms as the particle traverses through the junction.

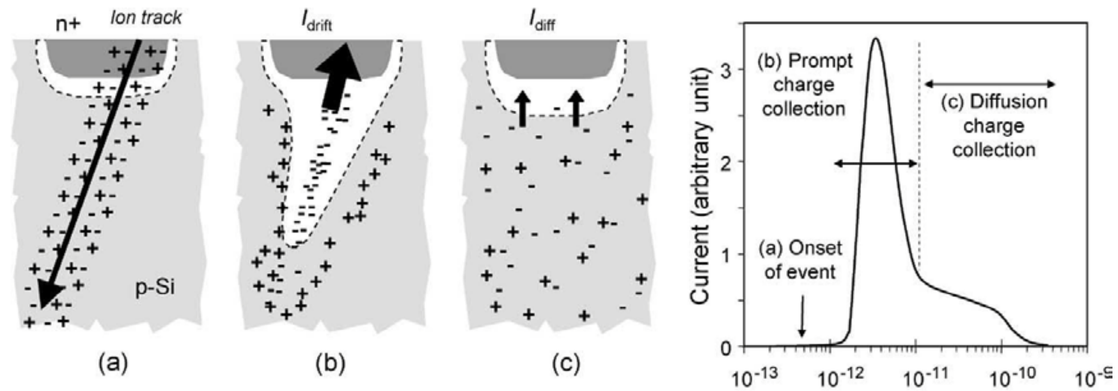


Fig. 2.5: Charge generation and collection of a reverse-biased junction and the resultant current due to an ion strike[25].

As the resultant ionization track comes close to the depletion region, carriers are rapidly collected by the electric field creating a large voltage and current transient at the node. There is an immediate distortion of the electric field into a funnel shape [34]. This funnel greatly enhances the drift collection efficiency by extending the high field depletion region deep into the substrate as shown in (b). The size of the funnel is a function of the substrate doping, with more distortion for less doped substrate. The drift phase of electron-hole collection is referred to as the "prompt" collection phase and takes only a few nanoseconds followed by the diffusion phase shown in (c). The diffusion phase is estimated to last for hundreds of nanoseconds until all carriers have been collected into the depletion region, recombined or diffused away from the junction area. The farther away from the junction that a strike occurs, the less the amount of charge that is collected and the less is the likelihood that the strike will result in an upset.

Ionizing radiation can deposit charge in silicon semiconductor either by directly depositing charge itself or indirectly by interaction with the nucleus of silicon. When charge is deposited in the material, it collects at the reverse-biased junction of the drain. There is an immediate distortion of the electric filed leading into a funnel. The funnel greatly enhances the drift collection efficiency.

Subsection 2.1.3: Indirect Ionizing Radiation

Lighter particles such as protons, electrons, neutrons or pions do not usually produce enough charge to cause upsets by direct ionization. However, they can produce significant upset rates due to indirect ionization. As a high energy proton or neutron enters the semiconductor lattice, it may undergo an inelastic collision with the target nucleus. Possible nuclear reactions include: 1) elastic collision that produces Si recoils; 2) the emission of alpha or gamma particles and recoil of Mg nucleus and 3) spallation reaction in which the target nucleus breaks up into two fragments such as the case where Si breaks up into C and O ions, each of which can recoil. Figure 2.6 illustrates two possible spallation reactions resulting from proton reaction with silicon nucleaus.

Fig. 2.6: In (A), alpha particle is released with recoil of Mg nucleus. In (B), a spallation reaction occurs with fragmentation of silicon atom into carbon and oxygen.

Any of these products is capable to deposit energy along its path length by direct ionization. In general, since these particles are much heavier that the original proton or neutron, they typically deposit much higher charge densities as they travel and therefore are capable of causing SEU. Nuclear elastic, inelastic and spallation collisions creates charge by indirect ionization. Though these nuclear fragments do not travel as far as primary ions go, they could deposit more energy than primary ions do.

Section 2.2: Device Response to Ionizing Radiation

Subsection 2.2.1: Bulk verses Silicon-on-Insulator Technologies

When a particle strikes a transistor, the most sensitive regions are the reverse biased p/n junctions. The high electrical field present in the reverse biased junction depletion region efficiently collects the particle induced charge process through drift processes, leading to a transient current at the junction contact. Just as important, a strike near a depletion region can also result in significant transient current as electron-hole pairs diffuse in the vicinity of the depletion region where they are collected. Figure 2.7 illustrates an ion strike at a bulk-CMOS transistor.

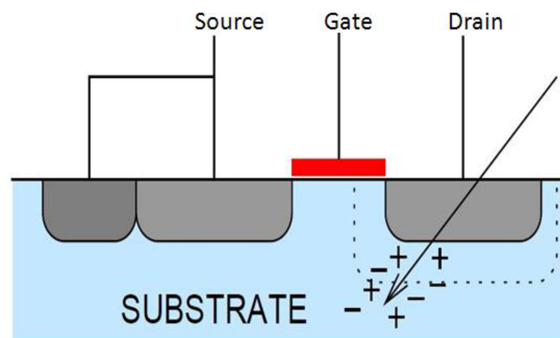


Fig. 2.7: Heavy ion strike in a bulk technology. The most sensitive areas are the depletion regions at the transistor drain.

An approach that is generally used in mitigating against SEU is the reduction of charge collection at sensitive nodes. Typically this has been done by introducing extra doping layers to limit substrate charge collection. In advanced SRAM technologies, triple well [35], and quadruple well [36] structures have been previously suggested to reduce SEU sensitivity.

SOI technology offers more robust devices compared to bulk devices because of reduced charge collection volume. The collection volume is reduced by fabricating device on thin silicon layer that is dielectrically isolated from the substrate as shown on figure 2.8 below.

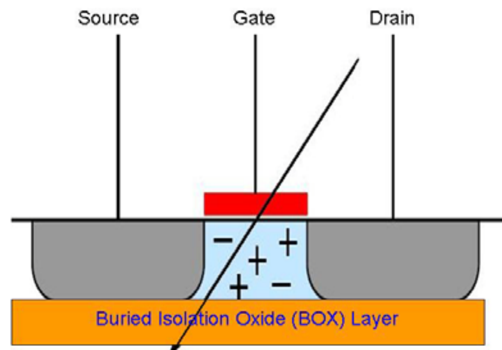


Fig. 2.8: Heavy ion strike and SOI technology. For SOI-CMOS, the hole-electron pairs injected into the transistor body may trigger a bipolar action, resulting in a current flow that is even greater than the injected current.

The buried oxide typically limits charge collection to the within the to silicon substrate. SOI devices have their own short coming as far as SEU sensitivity is concerned. Experimental measurements have evidenced an amplification mechanism between the deposited charge (Q_d) by the heavy ion and the collected charge (Q_c) by the device. Charge deposited in the body region, such as by an ion strike to the gate region can trigger a bipolar mechanism [37], [38]. Due to the dielectric isolation of the floating body, the holes are collected by the source while the electrons are

collected by the drain of the struck transistor. During an SEU event, the same amount of charge is collected in both the source-body and the body-drain junction. In practice, the bipolar amplification of the liberated charge in the SOI body is what creates sensitivity for these devices. Following an ion strike to the body of an n-channel of the transistor, electrons can be collected at the source or drain node. However, holes are trapped in the body and can only escape via a body contact. The presence of excess holes in the body region can forward bias the source/body junction, triggering the lateral parasitic NPN bipolar transistor, leading to snapback, a sustained high-current condition similar to latch up.

Because of the dielectric isolation of the floating body, the holes are collected by the source while the electrons are collected by the drain of the struck transistor. During an SEU event, the same amount of charge is collected in both the source-body and the body-drain junction. Figure 2.9 below illustrates the bipolar effect. The holes in the well raise the well potential and lower the source/well potential barrier causing the source inject electrons in the channel. The injected electrons are then collected at the drain where they add to the original particle induced current leading to enhanced SEU sensitivity. The phenomenon is called bipolar amplification because the source acts as the emitter, the channel acts as the base while the drain functions as the collector.

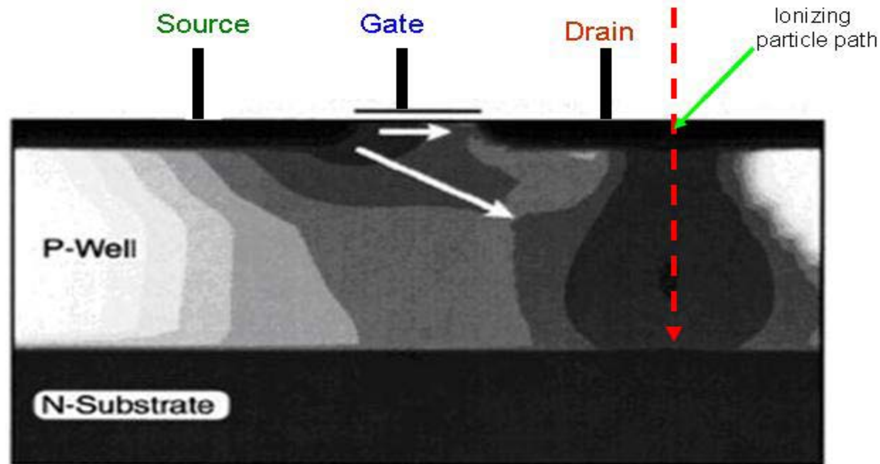


Fig. 2.9: Electron concentration contour inside an n-channel MOS transistor following an ion strike [3]. The bipolar effect is evidenced by the contours emanating from the source, showing that the source is injecting electrons into the p-well where they may be collected at the substrate or the drain node.

As the technology scales deep in submicron node, channel length has greatly been reduced, effectively reducing the base width allowing more electrons to reach the collector. The result has been enhanced bipolar amplification with scaling. Use of body ties to reduce floating-body effect can reduce triggering of bipolar effect and hence improve SEU performance [38].

Bulk and SOI-CMOS are sensitive to ionizing radiation but among the two, SOI-CMOS is more robust. In bulk CMOS, sensitivity is primarily due the electron cloud funnel that forms at the drain p/n junction. The problem is prolonged by the diffusion process that can last way long after the transient has passed. In SOI-SRAM, the sensitivity is primarily due to bipolar amplification that occurs because the ionizing radiation may cause rise to the body potential which lowers the source/well potential barrier causing the source to inject electrons in the channel.

Subsection 2.2.2: Circuit Response to Ionizing Radiation

If an SEU takes place, a current transient followed by a voltage transient results at the struck node. If know the recovery time as a function of LET and the cell capacitance or the dependence of the decoupling time of cross-coupled resistor, we can completely characterize the circuits SEU response. The circuit below in figure 2.10 shows the competing processes. Following an ion strike, the recovery processes is started by the load PMOS in an attempt to neutralize the deposited charge at the node. Unfortunately, the PMOS transistor has a finite current drive and therefore it will take a given amount of time to recover.

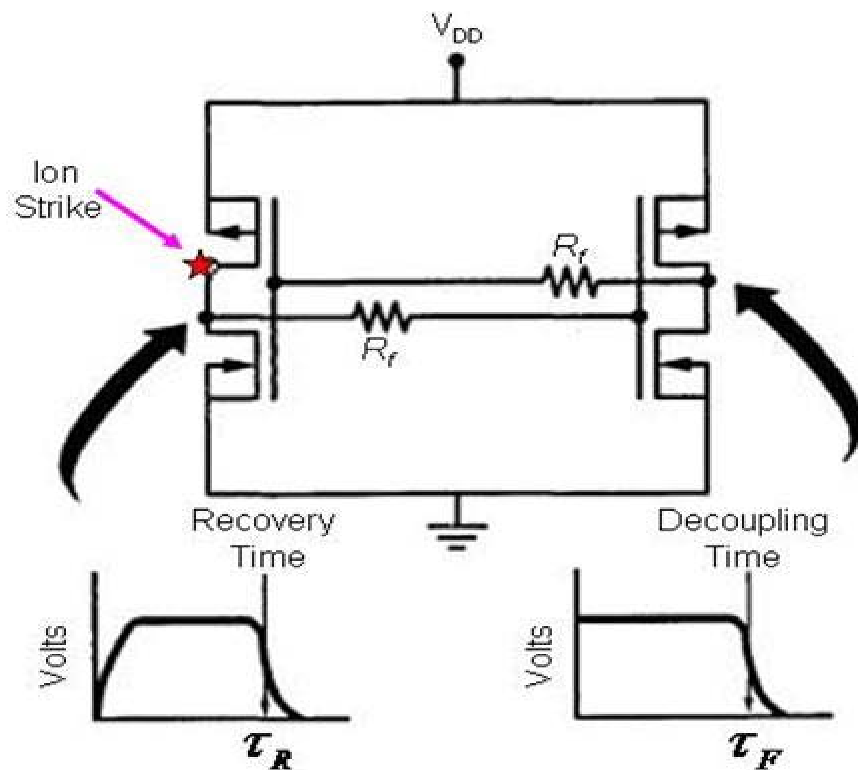


Fig. 210: SRAM topology showing cross-coupled resistors RF. The transient on the left node represents where the cell recovers from the strike while the transient on the right inverter represents where the SEU takes place.

At the same time, with the advent of the ion strike, a voltage transient occurs at the struck node which is reflected at the gate of the NMOS transistor of other inverter. This potential

drop triggers the NMOS transistor to turn off, which in turns triggers flipping of the state of the node. When designing for radiation environment, a determination of the limiting LET (this is the LET above which no more upsets takes place) cross-section of single-event upset is made for unhardened cell. Once this determination is done, a feedback resistor can be evaluated for the limiting LET. We simulated each event with different ion energy (described in the next section) until we determined the limiting LET.

Subsection 2.2.3: Conclusion

Accurate characterization of SEU sensitivities requires a good model for device and circuit response. For CMOS transistor in an SRAM configuration, an ion strike at the drain of a transistor is considered to be most sensitive because the drain/body junction is reverse biased providing a strong electric field that sweeps the electrons towards the drain contact while holes are swept towards the body. Holes swept into the body raise the body potential which leads to lowering of source/body barrier leading to injection of the holes into the source and consequently the source injects electrons into the channel of the transistor as well as the drain. The circuit response has recovery and feedback response. If the recovery time is larger than the feedback time, the bit flips

Section 2.3: Modeling Single-Event Errors in CMOS

Subsection 2.3.1: Background on Modeling

When modeling system sensitivity to Soft Error Rates (SER), there are four primary components for consideration [39]:

1. Modeling the radiation environment

2. Modeling charge transport in the device
3. Modeling circuit response
4. Modeling the manifestation of errors in a system.

In this work, we limit ourselves to modeling the circuit response to excess charge and the specific soft-errors under consideration are the SEUs. In describing energy loss in a material as the ionizing particle traverses through, the term ***linear energy transfer (LET)*** *is used to describe the energy loss per unit length of a particle as it passes through the material.* The LET is expressed in pC/μm where 1 MeV-cm^2/mg ≈ 0.01 pC/μm in silicon [40, 41]. For 3-D simulators such as Crème MC, it is necessary to run several simulations until convergence is achieved. Depending on the CPU speed and computer power, the simulation could run for days, weeks or months [40, 42]. In the next section, I present results of simulation using Pspice which provides results similar to what is available using 3-D simulators without the time and expense that is associated with the 3-D simulators.

Subsection 2.3.2: Modeling the Induced Transient Current

In order to model the circuit response to the excess charge following a strike by an ionizing particle, we need to have a model realistic model of the ion strike. Srinivasan simulated a transient current induced by an alpha particle and found the current waveform could be modeled by a double exponential function of the following form [39, 43, 44]:

$$I(t) = \frac{Q_{Total}}{\tau_f - \tau_r}\left(e^{-\frac{t}{\tau_f}} - e^{-\frac{t}{\tau_r}}\right) \qquad (2.1)$$

where τ_f is the decay time or the collection-time constant of the junction, τ_r is

the rise time and Q_{Total} is the total charge. However, the concept of critical charge is used to describe the SEU sensitivity [45]. In this regard, the SEU occurs when the collected charge is greater than the critical charge, but does not necessarily involve total charge collected. The distinction being that, charged continues to be collected long after the bit has flipped. The critical charge is expressed as follows [40, 46]:

$$Q_{Critical} = \int_0^{T_F} I_D dt \tag{2.2}$$

where T_F is the time when the device changes state. It is the time when the $V_{In} = V_{Out}$ for one inverter. This is the feedback condition for the SRAM to change state.

In previous work, it was shown that the critical charge is proportional to the charge stored on the capacitance of the struck node [47]. In this work, it was proposed that the critical charge is a sum of the charge stored at the nodal capacitance and the sourced by the PMOS transistor. More precisely, the critical charge should be given as:

$$Q_{Crit} = C_N V_{DD} + I_{DP} T_F \tag{2.3}$$

where C_N is the total nodal capacitance, V_{DD} is the power supply, I_{DP} is the maximum PMOS drain conduction current and T_F is the time following the strike until the device flips.

For the purpose of simulation we found equation 2.3b to be sufficient in modeling the current transient. The current pulse had a triangular shape with the base of the triangle being the sum of the rise and fall times while the height of the triangle was the magnitude of the pulse.

Subsection 2.3.3: Simulation Results and Analysis

The ion strike was simulated by a current (i) pulse which had a triangular shape whose base length is the sum of the rise and fall time. The magnitude of the deposited charge was varied by changing the height of the triangle which was the current's amplitude. Using the IBM's Process Design Kit, I simulated the resistor requirement for effective mitigation of 180nm, 130nm and the 90nm CMOS SARM technologies. Figure 2.11 is the circuit featuring thin-film high-sheet rho cross-coupled feedback resistor proposed for mitigating linear energy transfer sensitivities. The finding of the simulation shows that as technology scales deep in submicron regime, the SEU sensitivities have worsened and will continue to worsen if the proposed mitigation technique is not applied.

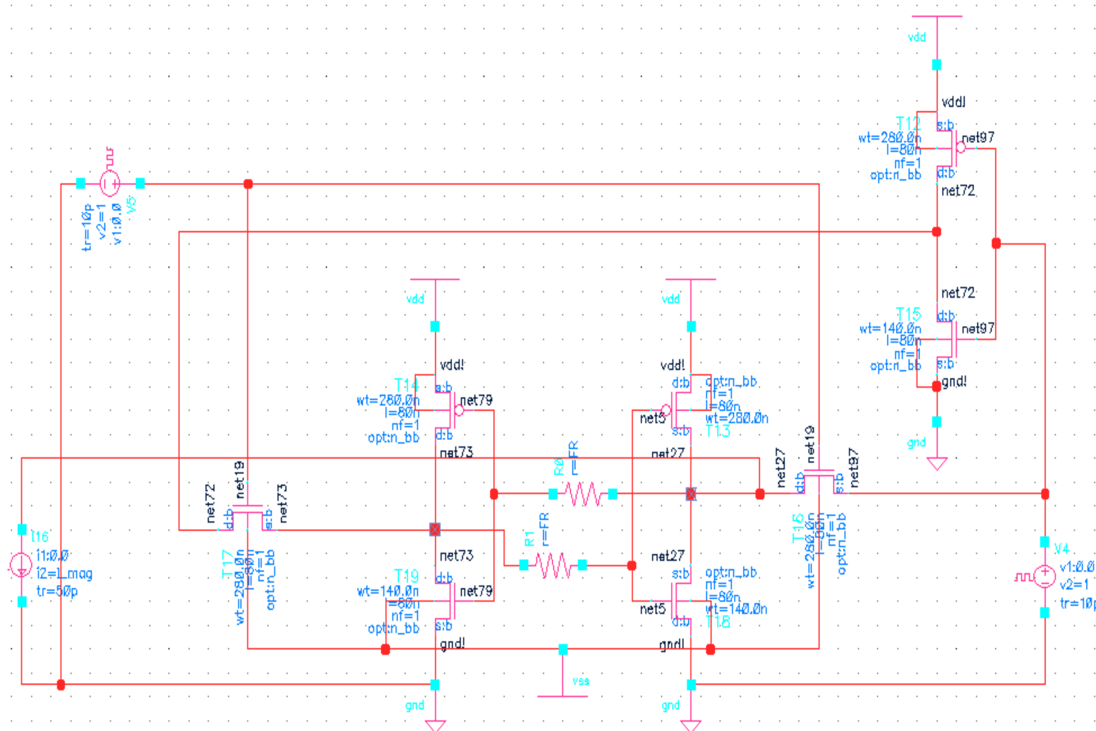


Fig. 2.11: 6T-SRAM circuit featuring cross-coupled feedback resistor. Ion strikes of various energies were simulated by changing the magnitude of the current pulse.

For the simulation the feedback RC time constant depends on the technology nodal capacitance and the feedback resistor applied. In figure 2.12, we use a cross-coupled resistor of 1.24MΩ and simulated ion strikes with the following energies: 40 MeV-cm^2/mg, 60 MeV-cm^2/mg and 97 MeV-cm^2/mg. It is observed that for 1.24MΩ feedback resistor, 90 nm technology SRAM will survive an ion strike of 40 MeV-cm^2/mg, it would barely survive a 60 MeV-cm^2/mg strike but it would flip state if hit by 97 MeV-cm^2/mg ion strike.

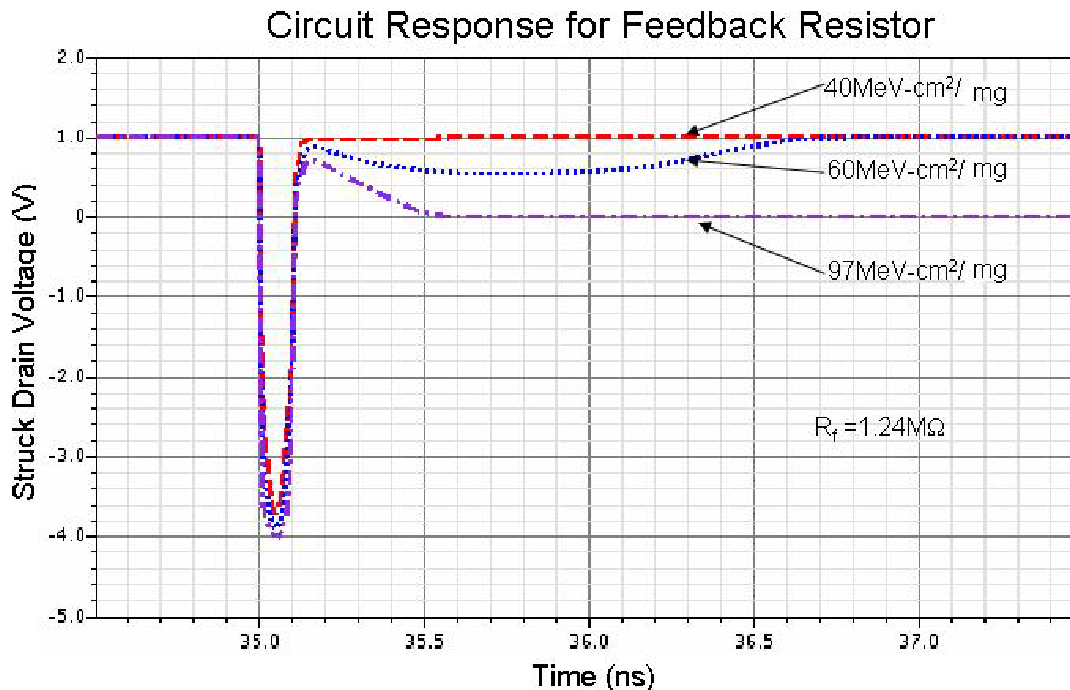


Fig. 2.12: Circuit response for a 90 nm CMOS technology node featuring a feedback resistor of 1.2 MΩ.

The other part of simulation involved using different resistor values for a particular strike of an ion with 34.65 MeV-cm^2/mg. The circuit response is shown in figure 2.13 below. It was observed that a resistor of 452kΩ would sufficiently mitigate an ion of 34.65 MeV-cm^2/mg, while a resistor of 448kΩ wo uld be at the threshold of upset. A

resistor of 444kΩ would not be sufficient to mitigate an ion strike of 34.65 MeV - cm^2/mg.

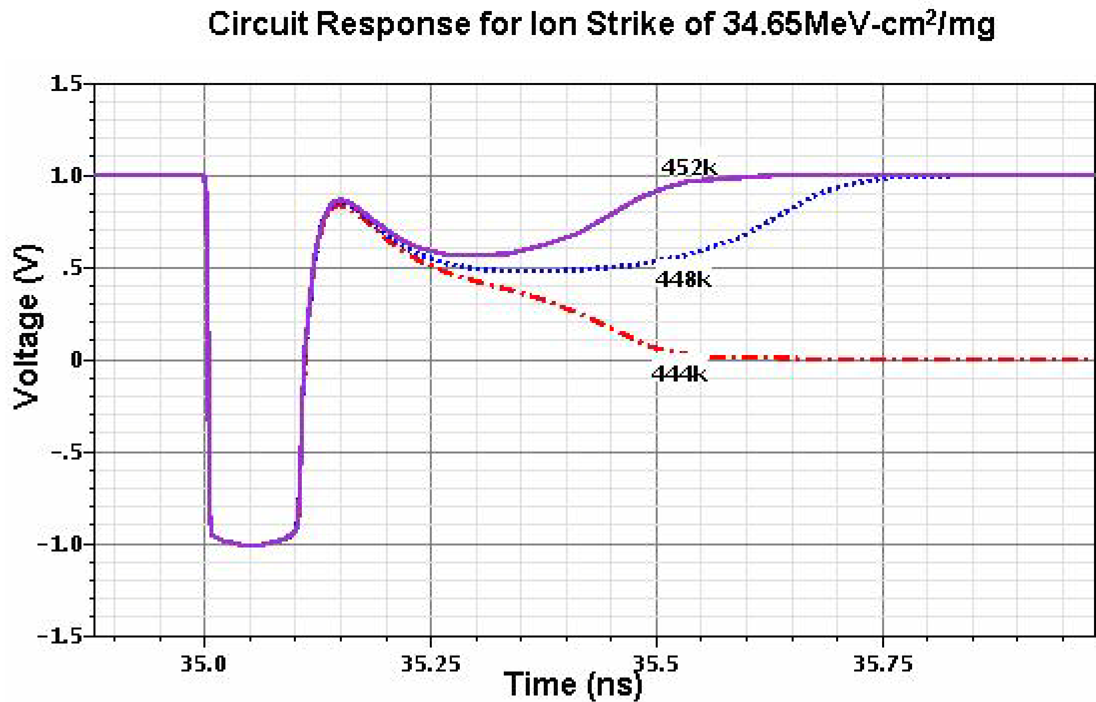


Fig. 2.13: Circuit response of a 90 nm CMOS technology node featuring a 34.65 MeV-cm^2/mg ion strike for R_F of 452kΩ, 448kΩ and 444kΩ.

In figure 2.14, the tread of SEU sensitivity for 180 nm, 130 nm and 90 nm technology nodes is shown. 130 nm technology nodes appear to be more sensitive for reasons other than technology scaling. The sensitivity of 130 nm SRAM has been validated by experiments [48, 49] and the cells have been shown to be particularly leaky.

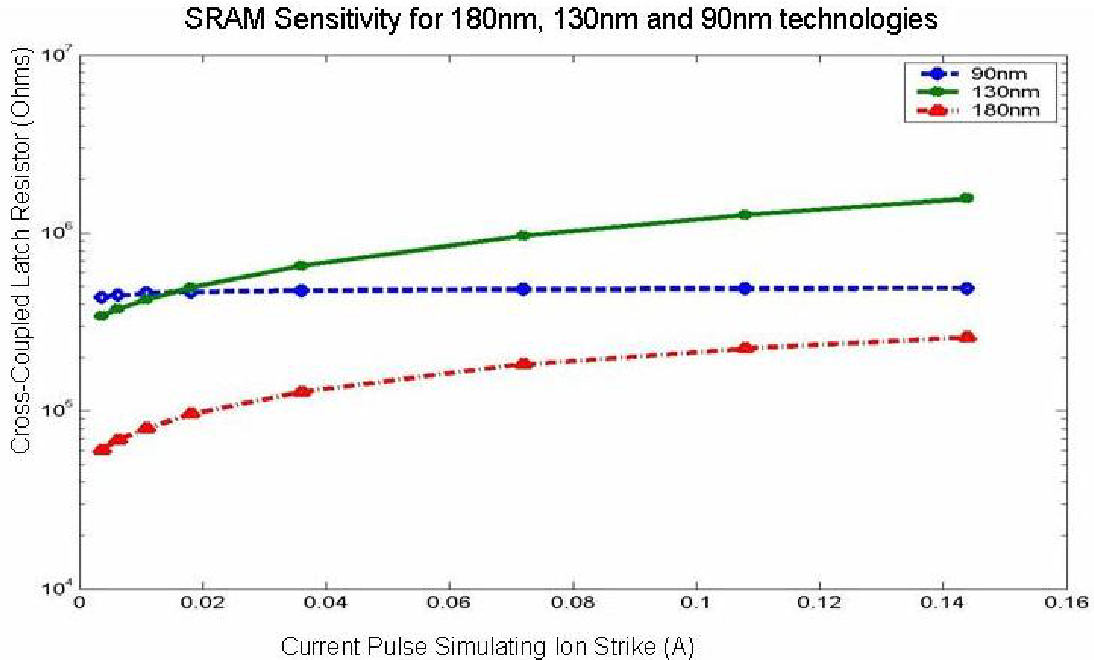


Fig. 2.14: Comparison of sensitivities for SRAMs of different 180 nm, 130 nm and 90 nm nodes.

To mitigate against these soft errors, the simulation shows that an SRAM made on 180 nm technology requires 200kΩ resistors to forestall an upset, 130nm technology requires 1.2 MΩ resistor and 90 nm needs a 400kΩ resistor.

The three technology SRAM were then simulated with the $R_F = 0$. Choosing the same amount of current, four different ionizing particles were simulated to establish how long a transient could last. The data is tabulated in table 1.2 below. It is shown that for these deeply scaled technology SRAMs, all transient last but for only a few picoseconds. If for instance we consider a 97 MeV-cm2/mg ionizing particle striking a 90 nm SRAM cell, all that is needed to determine the size of R_F is the gate-drain capacitance of the technology node. For this technology, this capacitance is a fraction of a femto farad.

Table 1.1	
90 nm Technology	
LET Threshold	Transient Duration
20 MeV-cm^2/mg	2.91 ps
40 MeV-cm^2/mg	3.38 ps
60 MeV-cm^2/mg	3.79 ps
97 MeV-cm^2/mg	4.328ps
130 nm Technology	
20 MeV-cm^2/mg	2.08 ps
40 MeV-cm^2/mg	2.24 ps
60 MeV-cm^2/mg	2.30 ps
97 MeV-cm ^{2}/mg	2.68 ps
180 nm Technology	
20 MeV-cm^2/mg	1.32 ps
40 MeV-cm^2/mg	1.59 ps
60 MeV-cm^2/mg	1.76 ps
97 MeV-cm^2/mg	2.23 ps

Single-event upset Transient duration for different technology nodes

The circuit response time is delayed by:

$$R_F C = \tau \qquad (2.4)$$

where τ is the transient duration. If for example the nodal capacitance is 0.2fF, a feedback resistor of 21.6kΩ is required to mitigate a transient that lasts for 4.328ps. If capacitance is less, even a larger resistor would be required.

Section 2.4: Experimental Validation of SEU Sensitivity

Subsection 2.4.1: Background on the Heavy Ion Experiment

Significant amount work based on theoretical simulation using Crème MC has been done to show the contribution of nuclear reactions to heavy ion single event upset cross-section[50]. In this chapter, experimental evidence of both nodal charge sharing and upsets due to secondary reaction is investigated. The SRAMs evaluated in this work were 90nm CMOS SOI technology. The SOI wafers had silicon substrate of only 70nm and the buried oxide thickness was 145nm. The gate oxide of the core devices is 1.3nm and the oxide for the I/O devices is 5nm. For these devices, the dielectric metal stack from the passivation layer to device silicon layer is 5.8µm. The SRAM cells were designed such that transistors N1=N2, P1=P2 and N3=N4. The gate areas of N1, P2 and N4 are different and their contributions to the SRAM's sensitive volume are not the same. The volume of N1, P2 and N4 are V1, V2 and V4. The transistor's length and width dimensions for transistor P2 is $l=w= 0.11\mu m,$ transistor N1, $l=0.125\mu m,$ $w=0.12\mu m$ and transistor N4, $l=0.125\mu m,$ $w=0.12\mu m$. Other important device parameters are calculated based on these dimensions and are tabulated in table 2.2 below. In the table, $\sum wl$ is the sum of the gate areas of the three vulnerable transistors and $t\sum wl$ is sum of the volume of the three transistors. The 1cm^2 in one cell is equivalent to 1cm^2/bit.

Table 2.2

t(cm)	$\sum wl$ *(cm^2)*	*V1(cm^3)*	*V2(cm3)*	*V4(cm^3)*	*a(cm)*	$3\pi a^2$ *(cm^3)*
7.0×10^{-6}	4.91×10^{-10}	1.54×10^{-15}	0.847×10^{-16}	1.05×10^{-16}	6.49×10^{-6}	3.97×10^{-10}

Figure 2.15 illustrates the sensitive nodes in a 6T SRAM cell structure.

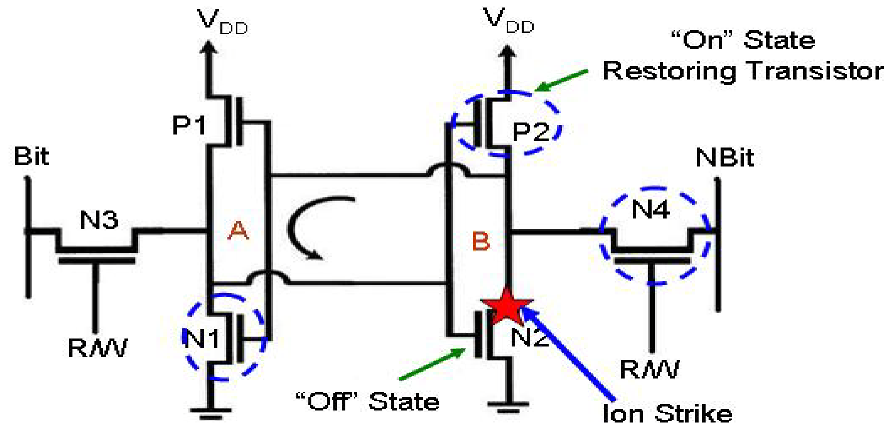


Fig. 2.15: A 6T SRAM cell used to identify vulnerability of off-MOS transistor for 90nm SOI SRAM. V_{DD} = 1.0V

A 90nm 4M SRAM from Freescale Semiconductor was irradiated with a cocktail of 10MeV/amu ions at Lawrence Berkeley National Laboratory's 88" Cyclotron. A wide range of Effective LETs was used by selecting different ions and varying the angle of incidence. The heavy ion cocktail contained the following ions: B, O, Ne, Si, Ar, Cu, Kr and Xe. For each test run, a checker pattern was written to the memory, the device was exposed to a preset fluence of heavy ions in the range of $10^6/cm^2$ to $10^7/cm^2$. After each exposure, the memory was read back and the output was compared with the original pattern counting the errors whenever a bit mismatch was detected.

Subsection 2.4.2: Relating Upset Cross-Section to Physical Cross-Section

For SOI technology, the sensitive volume is related to the parasitic bipolar body, which is often described as the rectangular parallelepiped. The bipolar body is well defined, and is given by the product of the device length *(l)*, device width *(w)* and the thickness of the SOI substrate. For the purpose of the analysis of the limiting cross-

section for the heavy ions irradiation, three equivalent spheres were used, all with similar radius *"a"* to represent the three bipolar body volumes of the three vulnerable "off" MOS transistors in the SRAM. The effective volume is equal to the sum of the three transistors, $(V_{Effective} = V1 + V2 + V4 = \sum wlt)$ where $V_{Effective}$ is the sensitive volume. The physical cross-section for the heavy ions for the three equivalent spheres representing the three SOI MOS "off" transistors is therefore $3\pi a^2$. It has been previously demonstrated that the limiting proton induced upset cross-section $\sum \sigma_{PL}$, of an SRAM correlates with the physical cross-section [51]. The limiting cross-section can be expressed as follows:

$$\sum \sigma_{PL} \approx \sigma N_2 R(3\pi a^2)\text{, cm}^2\text{/bit} \qquad (2.5)$$

where $(3\pi a^2)$ is the physical cross-section of the incoming heavy ion for the three equivalent off-transistors in the SRAM cell and σ, N_2 and R are the proton-silicon reaction cross-section evaluated to be $6 \times 10^{-26}\text{ cm}^2$, N_2 is the silicon density of silicon dioxide which is $2.3 \times 10^{22}\text{ cm}^{-3}$ and R is the range of the recoils typically 10μm respectively. The analysis of the data presumes that this relationship largely holds since it is not dependent on the mass or any other characteristics of the proton.

Subsection 2.4.3: Analysis of Heavy Ions Data

The results of the experiment for the different ions and the change in the angle of incidence are contained in table 2.3 below. In the analysis, the data was classified in two categories: 1), normal incidence only, and 2), all angles including the normal incidence. Since the silicon substrate is only 70nm, the expectation is that if the upset cross-section obtained is larger than the physical cross-section, then the total number

of upsets primarily includes single-event multiple bit upsets due to nodal charge sharing. If on the other hand the upset cross-section is much larger than the cross-section obtained for just the normal incidence case, then the new cross-section so obtained must include a significant amount of upsets due to secondary reactions arising from neutron reaction with heavy metal and silicon atoms. The reason here is that these fragments have extended range of reaction with silicon for strikes away from the normal incidence.

TABLE 2.3

Ion	Angle	LET	Fluence
B	0	0.89	1.0×10^7
B	42	1.2	7.43×10^6
B	60	1.8	5.0×10^6
O	0	2.19	1.0×10^7
O	29	2.5	8.75×10^6
O	43	3.0	7.31×10^6
Ne	0	3.49	1.0×10^7
Ne	29	4.0	8.75×10^7
Ne	39	4.5	7.77×10^6
Ne	46	5.0	6.94×10^6
Si	0	6.09	1.0×10^7
Si	29.5	7.0	8.70×10^6
Si	40	8.0	7.66×10^6
Si	47	9.0	6.82×10^6
Ar	0	9.74	1.0×10^7
Ar	27.6	11.0	8.86×10^6
Ar	41	13.0	7.55×10^6
Ar	55	17.0	5.73×10^6
Ar	59	19.0	5.15×10^6
Cu	0	21.17	1.0×10^7
Cu	28	24.0	8.83×10^6
Cu	41	28.0	7.55×10^6
Kr	0	30.86	1.0×10^7
Kr	39.5	40.0	7.71×10^6
Kr	52	50.0	6.15×10^6
Xe	0	58.78	1.0×10^7
Xe	33	70.0	8.39×10^6
Xe	49	90.0	6.56×10^6
Xe	58	110.0	5.30×10^6

The cross section shown in figures 2.2 and 2.3 was a fit to a Weibull cumulative density function. First, the data was fitted using the three 3-parameter lognormal distribution and then used the limiting cross-section determined in the lognormal distribution to use the 4-parameter Weibull distribution. For lognormal distribution, the upset cross-section is expressed as:

$$\sum \sigma_H = 0.5 \sum \sigma_{HL} \left[1 + erf(z)\right], \text{ cm2/bit for } z \geq 0 \tag{2.6}$$

$$\sum \sigma_H = 0.5 \sigma_{HL} erfc(-z), \text{ cm2/bit for } z < 0 \tag{2.7}$$

Where, $z = \dfrac{\ln(L) - m}{\sigma_d \sqrt{2}}$ and $f(z) = \dfrac{\exp(-z^2)}{\sigma_d \sqrt{2\pi}}$

m is the average value of $\ln(L)$ and σ_d is the standard deviation of $Ln(L)$ [52, 53]. L is the effective LET in MeV-cm2/mg corrected with $1/\cos\theta$ where θ is the angle away from the plane of incidence. Based on the data in table II above, $m = 2.52$ and $\sigma_d = 1.35$ and $\sum \sigma_{HL} = 2.0 \times 10^{-9} cm^2 / bit$.

Using the value of $\sum \sigma_{HL}$ from lognormal distribution the data was fit to the Weibull cumulative density function which is expressed as:

$$\sum \sigma_H = \sum \sigma_{HL} \{1 - \exp\left(\frac{L - L0}{W}\right)^S, \text{ cm}^2\text{/bit for } L > L0 \text{ and} \tag{2.8}$$

$$\sum \sigma_H = 0 \text{ for } L \leq L0$$

where L is the effective LET, W and S are shape adjustment parameters. To fit Weibull curve to the data, the following values were used: $L_0 = 0.75 MeV - cm^2 / mg$, $W = 27 MeV - cm^2 / mg$ and $S = 1.65$ which is a dimensionless parameter.

Section 2.5: Sorting Primary from Secondary Ionization

Subsection 2.5.1: Ion Normal to Plane of Incidence

The upset cross-section for normal incidence verses the LET is shown in figure 2.16 below. We show that the total cross-section $(\sum \sigma_{HI})$ is about $2.0 \times 10^{-9} cm^2 / bit$. By extrapolation, the let threshold (LET_{th}) which is $L1$ in the equation for log-normal is approximately 0.75 MeV-cm^2/mg. For silicon, 97 MeV-cm2/mg corresponds to approximately 1pC/μm, indicating that for this SOI SRAM, the critical charge (Q_{crit}) is only 0.53fC/μm.

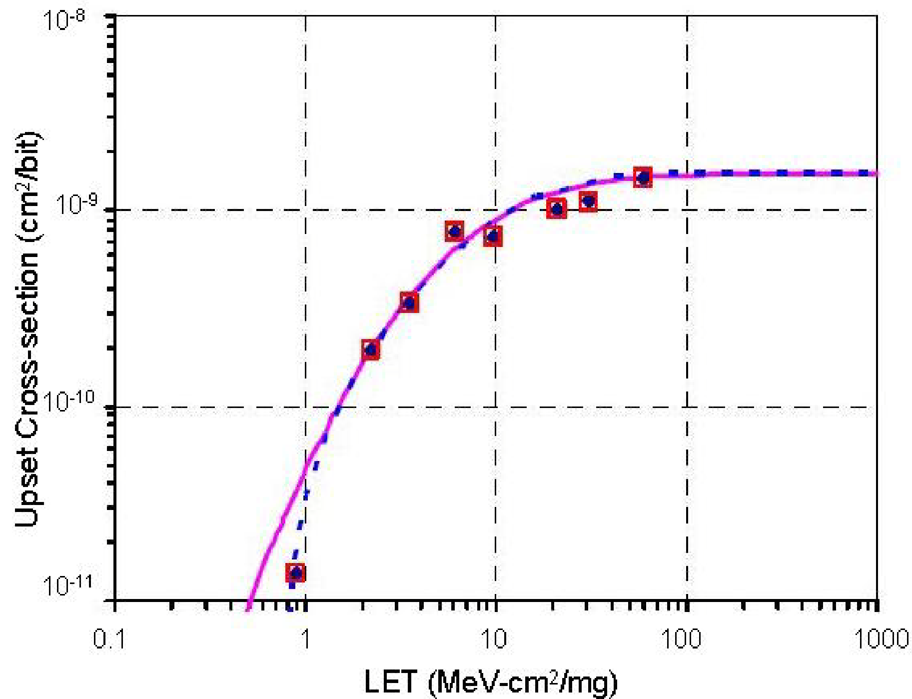


Fig. 2.16: Upset cross-section for irradiation done with beam normal to the plane of the device for the same 90nm SOI SRAM

In table 2.2 above, it was shown that physical cross-section is only 3.97×10^{-10} cm^2 but we see that the limiting upset for incident ions strikes is at least $\sigma = 2 \times 10^{-9}$ cm^2/bit. The limiting upset cross section is 5 times more than the physical cross-section!

Subsection 2.5.2: Ion at All Angles

In figure 2.17 below, upset cross-section for angled strikes only is shown. Weibull fit is shown by the dash line while the log-normal distribution is shown by the pink line. The highest upset cross-section observed value is 2.15×10^{-9} cm^2 for XE ion at 58 degrees angle relative to the plane of incidence at effective LET of 114 MeV-cm^2/mg. The data shown in square frames is data of normal incidence that is also shown in figure 2.16 above. The lognormal distribution is shown with the solid pink curve for the upset cross-section.

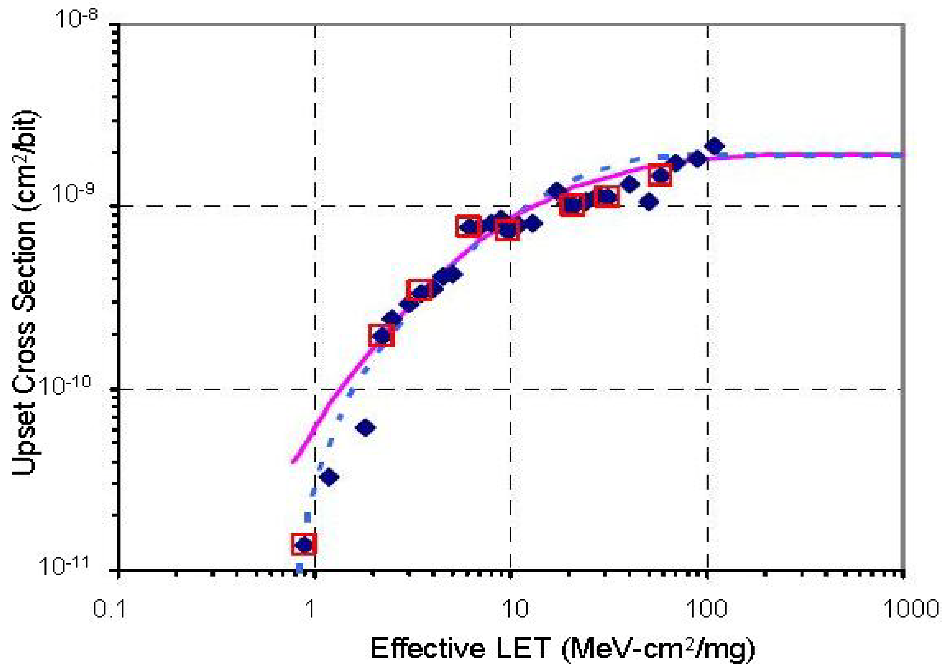


Fig. 2.17: Upset cross-section for irradiation done at angles for the 90nm SOI SRAM. V_{DD} is 1V

Using the Weibull curve, the threshold LET (LET_{th}) can be extrapolated from either figure 2.16 or figure 2.17.

Subsection 2.5.3: Primary verses Secondary Ionization

In further analysis of information we can gather from figure 2.16 above, the ratio of upset limiting cross-section to upset cross-section at L0.25, L0.5, L0.75 and L1. The subscripts indicate the percentile of upset cross-section compared to the limiting upset cross-section. For example, L0.25 refers to the cross-section at 25% of the limiting cross-section. Further the ratio of primary ion upset cross-section was taken to that of secondary ion upset cross-section. The data is reported in table 2.4 below.

Table 2.4

$\Sigma\sigma_H/\Sigma\sigma_{HL}$	0.25	0.5	0.75	1.0
$\Sigma\sigma_H$	3.88×10^{-10}	7.75×10^{-10}	1.16×10^{-9}	1.6×10^{-9}
L	L0.25 ≈ 3.74	L0.5 ≈ 7.85	L0.75 ≈ 16.5	L1.0 = 1000
$\Sigma\sigma_H/\Sigma\sigma_{HL1}$	1	2	3	4
$\Sigma\sigma_{H2}/\Sigma\sigma_{HL1}$	0	1	2	3

In the table, $\sum \sigma_H = \sum \sigma_{H2} + \sum \sigma_{HL1}$, where σ_{HL1} is the upset cross-section due to primary ion strikes and σ_{H2} is the contribution from secondary ions. We show that at L=L0.5, $\frac{\sum \sigma_{HL2}}{\sum \sigma_{HL1}} = 1$ and $\frac{\sum \sigma_H}{\sum \sigma_{HL}} = 0.5$ which corresponds to the threshold LET as defined in[52]. At $\frac{\sum \sigma_{HL2}}{\sum \sigma_{HL1}} = 1$, the amount of secondary ion contribution is equal to primary ion contribution. We see from figure 2.2 above that at the limiting upset cross-section $(L = L1)$, note that L1=1000 MeV-cm^2/mg, the ratio of secondary ion to

primary ion contribution is 3:1 and the upset limiting cross-section is 4 times the physical cross-section.

Considering the effect of angled strikes, table 2.5 below has even more alarming results for 90nm SOI SRAM with no extra mitigation for SEUs. At the limiting LET, we find that the cross section is 5 times greater the physical cross-section. That is, $\frac{\sum \sigma_H}{\sum \sigma_{HL1}}$. The ratio of secondary ion strikes to primary ion strikes is 4:1.

Table 2.5

$\Sigma\sigma_H/\Sigma\sigma_{HL}$	0.2	0.4	0.6	0.8	1.0
$\Sigma\sigma_H$	3.80×10^{-10}	7.61×10^{-10}	1.14×10^{-9}	1.52×10^{-9}	2.0×10^{-9}
L	L0.2 ≈ 3.99	L0.4 ≈ 8.84	L0.6 ≈ 17.5	L0.8 ≈ 38.6	L1.0 = 1000
$\Sigma\sigma_H/\Sigma\sigma_{HL1}$	1	2	3	4	5
$\Sigma\sigma_{H2}/\Sigma\sigma_{HL1}$	0	1	2	3	4

The charge at L0=0.75 MeV-cm^2/mg was calculated to be approximately 0.53fC*/um*. The single event upsets are dominated by single-event multiple-bit upsets where the primary striking ion is able to strike several nodes and deposit charge, sufficient to course upsets along it path. The challenge is even greater if the increase in upset cross-section is due to secondary ions arising from elastic and inelastic corrosions. The challenge posed by these errors is expected to get worse as technology get to 45 nm and beyond.

Section 2.6: New Approach to SEE Testing

Subsection 2.6.1: Experimental Approach

The objective of this experiment was to remove the uncertainty in the LET of the ion that reaches the sensitive volume by reducing or eliminating straggling effects as well as the removing the uncertainty related with determining precisely the thickness of the substrate. The procedure of doing the experiment involved cutting a hole in an empty package that a die was to be mounted on. The die was mounted over the hole and wire-bonded. An epoxy was applied to completely cover the mounted wire-bonded chip to stabilize the part. Figure 2.18 below illustrates the procedure.

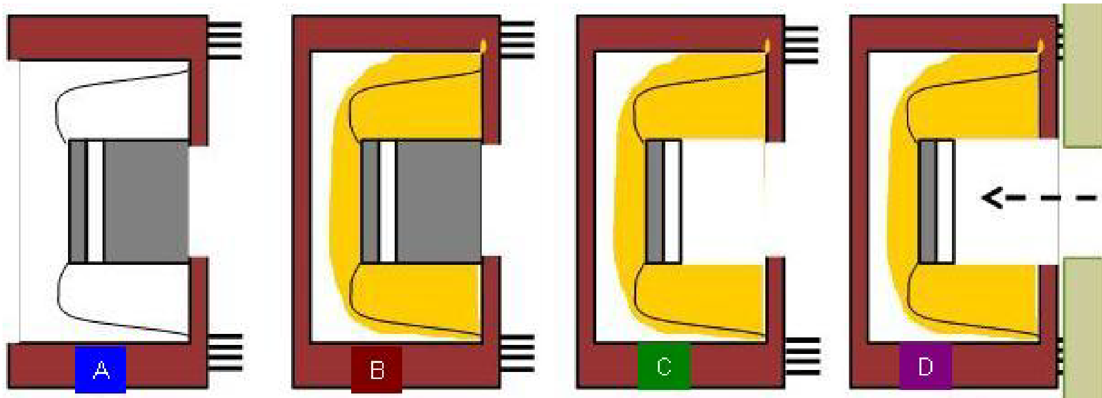


Fig. 2.18: (A), the device mounted inside the package directly over the hole; (B) the device is stabilized by embedding it in epoxy; (C) the silicon substrate is completely removed; (D) the package mounted on the test board containing the hole in the package through which laser pulse can gain access

The package was sealed and placed in a XeF_2 etcher to remove Si substrate. The XeF_2 etch system (shown in figure 2.19) is based on a pulse type system where an etch cycle is takes place every 15 seconds followed by a pulse during which the etch products are evacuated and the processes is repeated.

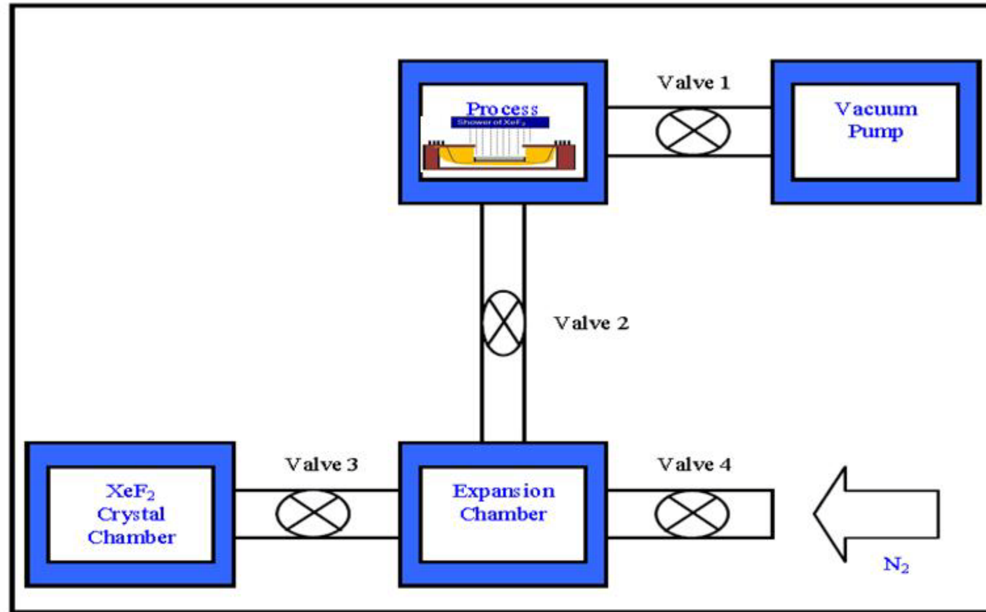


Fig. 2.19: XeF2 Etch system. The sample is loaded is loaded in processes chamber at the top between valve 2 and valve 1.

First, the processes and expansion chambers are purged with nitrogen and pumped down to the base pressure of approximately 50mTorr. Then the sample is loaded into the process chamber with valve 2 closed. Once the sample is loaded, valve 3 is opened expanding XeF_2 vapor from the crystal chamber into the expansion chamber, etching the sample by connecting to the expansion chamber to the processes chamber. The system is alternately purged with N_2 after each etch cycle to evacuate the etch products. Since the selectivity ratio of SiO_2 to Si is 1:1000, the buried oxide was a natural etch stopper. The photomicrograph in figure 2.20 shows the memory blocks under the microscope.

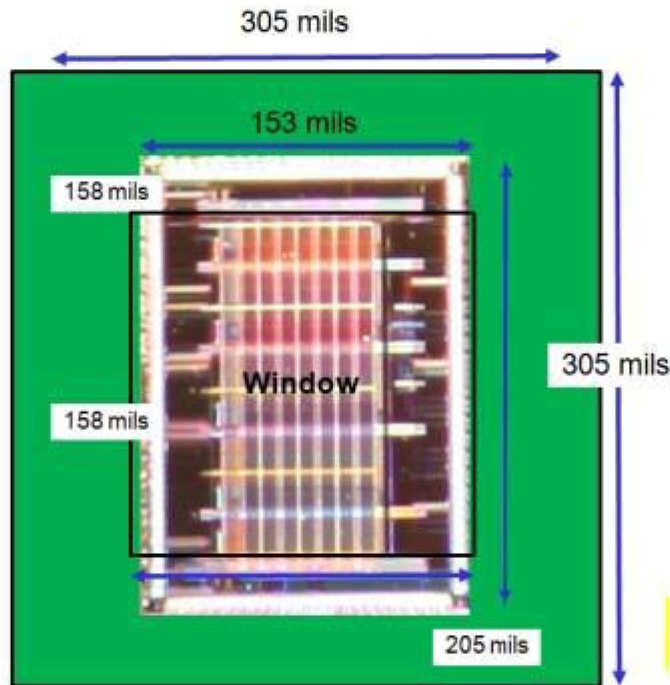


Fig. 2.20: Photomicrograph through the hole in the back side of the package showing the memory block structures. The memory blocks are clearly visible through the remaining thin oxide layer

The SEUs are generated by exposing the back side of the etched SRAM to ionizing laser pulses of different energy, varying the power until SEU threshold is determined. Figure 2.21 shows a column of bits that changed state as I moved the laser beam vertically. Knowing the physical layout of the device, one can chose which bit you wish to upset. While the primary utility of pulsed laser approach lies in its ability to precisely inject a known amount of charge into a well defined location, the development of the substrate etching methodology creates a unique opportunity that has up to now not been available, for developing a mechanism of depositing charge without the limitations associated with traversing the silicon substrate.

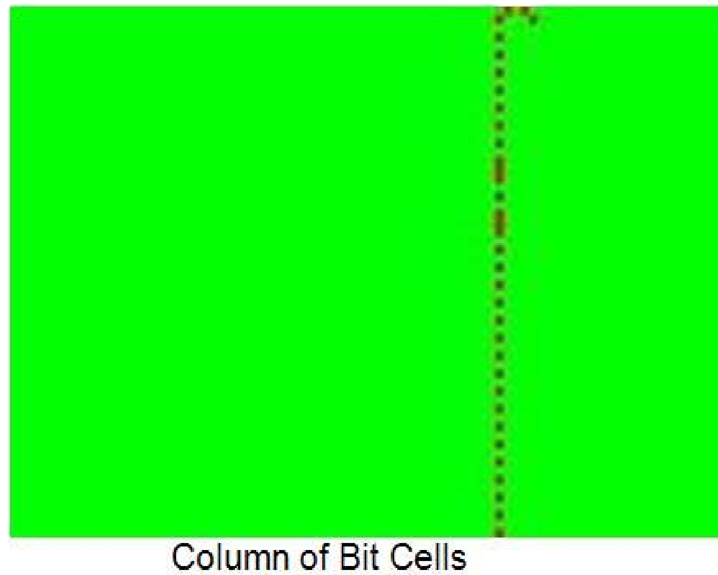


Fig. 2.21: The vertical column on the bit map shows bits that were upset as I moved the laser beam vertically. One can choose the bit-cell to upset by moving the joy-stick vertically or horizontally to the desired location.

Subsection 2.6.2: Single Photon and Two Photon Approach

Above band-gap laser pulses of wavelength of 590nm were focused were focused onto the active region from the back side as illustrated in figure s using a 100X microscope objective lens. The focused spot with a nominal Full-Width at Half-Maximum diameter of 1.1 µm was located at the memory array in a region far placed from the control circuitry. The intensity of the incident laser pulse was moved in both x-y directions until the least amount of energy that could cause an upset was determined. The approach resulted in an SPA SEU threshold of 0.42 pJ which translates to 7.5fC/μm. This charge translates to equivalent LET of 0.73 MeV-cm^2/mg. The approach for SPA SEU testing is described in [54]. The procedure described in section 2.3.2 above was repeated for the same device using laser pulse whose wavelength is 1260 nm. About 120 femto-seconds optical pulses were focused through the buried oxide using a 100X microscope objective, resulting in a near-

Gaussian beam profile with a typical diameter of about 1.6µm at the focus. Since the carrier deposition varies as the square of the distance of irradiance, this corresponds to a Gaussian carrier density distribution with an approximate diameter of 1.1µm at FWHM. The approach followed is that described at [55, 56]. The absorption spectrum of silicon is shown in figure 2.22 below

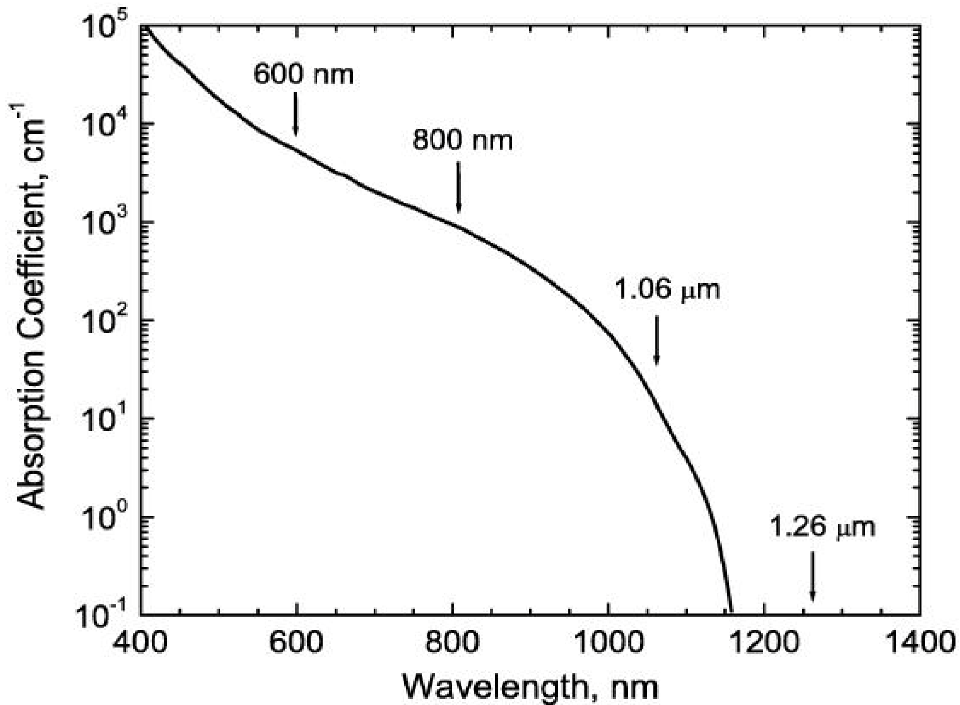


Fig. 2.22: Absorption spectrum of silicon in the visible and near-infrared region. When the silicon substrate is completely removed up to the BOX layer, the only consideration for absorption was for 700Å active device layer. This demonstrates the capability of the technique. Figure from [56].

In this experiment, I demonstrated that sufficient carrier densities can be generated by two-photon and single-photon absorption in silicon. Because of the large band gap of silicon dioxide, the material is transparent to optical beam and consideration for absorption need only be made for silicon substrate.

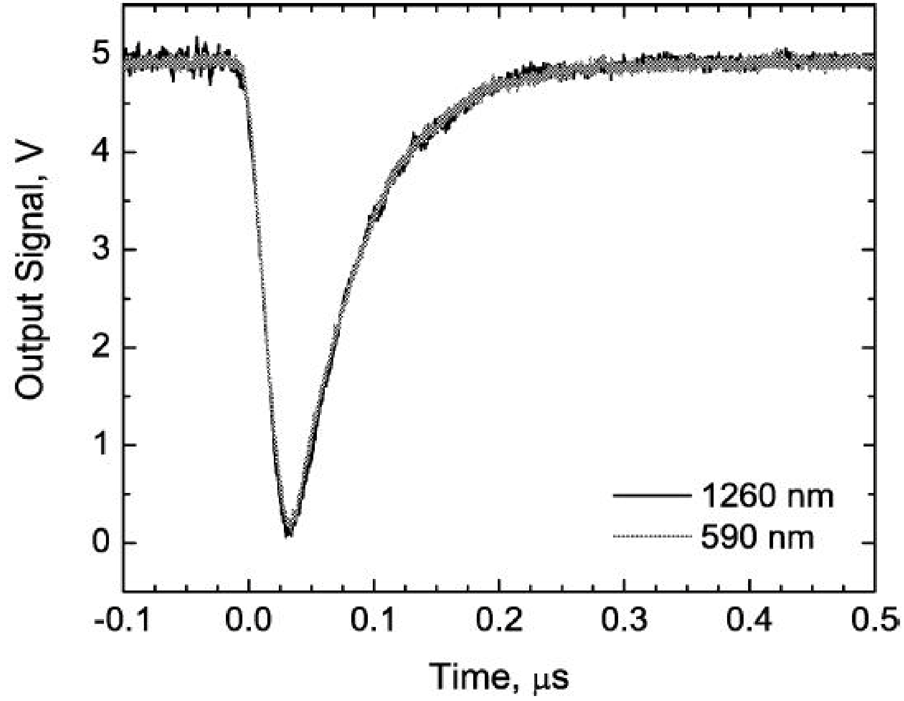


Fig. 2.23: Laser-induced single-event transient using 1260 nm wavelength for single photon absorption and 590 nm for two-photon absorption.

In this experiment, generation of the laser-induced transient pulse, shown in figure 2.23 above, required 1.2 pC of charge at 590 nm, and 0.63 nJ pulse at 1260 nm wavelength.

Subsection 2.6.3: Analysis of the deposited Charge

There are three primary equations that relate the pulsed laser propagation with carrier generation in a semiconductor material [57, 58]:

$$\frac{dI(r,z)}{dz} = \alpha I(r,z) - \beta_2 I^2(r,z) - \sigma_{ex} N I(r,z) \qquad (2.9)$$

$$\frac{d\Phi(r,z)}{dz} = \beta_1 I(r,z) - \gamma_1 N(r,z) \qquad (2.10)$$

$$\frac{dN(r,z)}{dt} = \frac{\alpha I(r,z)}{\hbar\omega} + \frac{\beta_2 I^2(r,z)}{2\hbar\omega} \tag{2.11}$$

where I is the irradiation pulse, N is the density of generated free carriers, Φ is the phase, α is the linear absorption coefficient, β_2 is the two-photon absorption coefficient, σ_{ex} is the absorption coefficient of laser-generated free carriers. Coefficient γ_1 describes the real component of free carriers, z is the depth of the material and β_1 is proportional to the real part of χ .

For SPA (above-bandgap) carrier generation, the I^2 in equation (2.11) is so small and can be neglected [56] leading to the familiar Beers law for laser beam irradiance as a functional of depth in the semiconductor. The generated carriers can be calculated by considering only the first term in equation (2.11), leading to the following expression:

$$N(z) = \frac{\alpha}{\hbar\omega}\exp(-\alpha z)\int_{\infty}^{\infty} I_0(z,t)dt \tag{2.12}$$

For a Gaussian beam, the intensity I is given by:

$$I(r,z) = \frac{2P}{\pi w^2}\exp\left(-2r^2 / w^2\right) \tag{2.13}$$

where the longitudinal dependence of the beam radius $w(z)$ is given by:

$$w(z) = w_0\left[1+\left(\frac{\lambda z}{\pi w_0^2 n}\right)^2\right]^{1/2} \tag{2.14}$$

where z is the longitudinal position relative to the beam radius (w_0) at

FWHM, P is the pulse power, n is the linear refractive index of the medium and λ is the wavelength of the light.

The calculation of the charge deposited on the transistor is derived from the overwrap area of the transistor and the Gaussian laser beam. In calculating the energy deposited at the sensitive area of the transistor, I made the following assumptions: 1), the laser beam energy can be considered to be evenly distributed at Full-Width at Half-Maximum (FWHM), 2), The beam size had small enough spot-size to affect only one transistor in the bit-cell and 3), at LETth, the energy is small enough that charge sharing is negligible. Figure 2.24 shows the correlation of pulsed laser irradiation (in red) with the heavy ions (blue) for 1M SRAM made by Sandia National Laboratory.

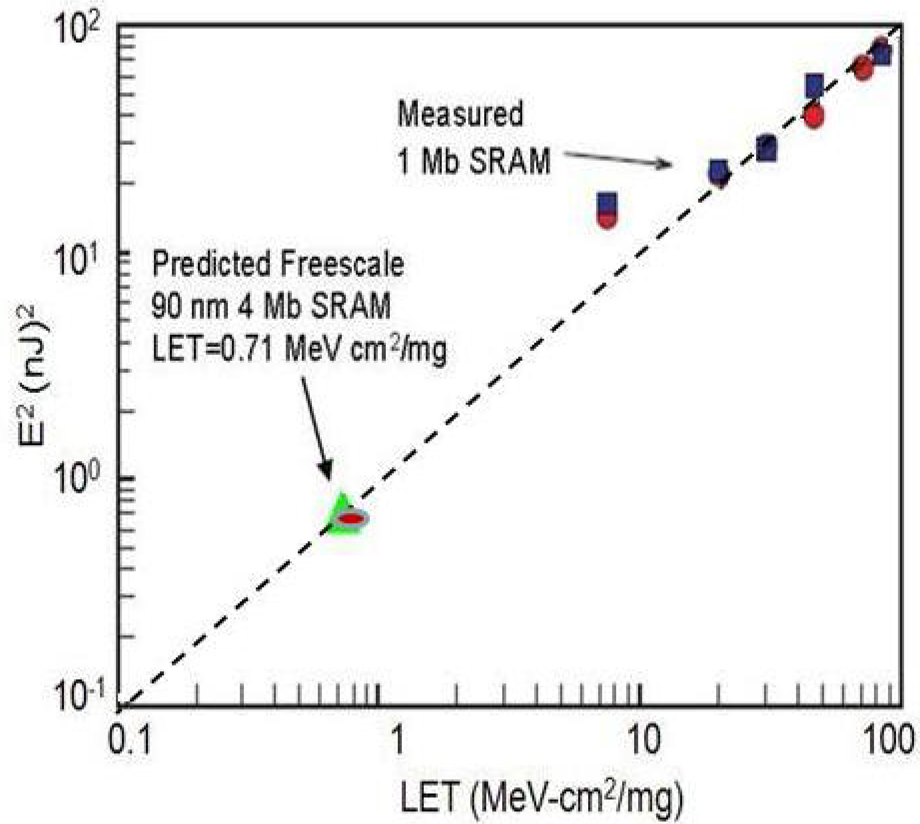


Fig. 2.24: SEU threshold as determined by Two photo Absorption (TPA) laser irradiation for 90nm SOI SRAM[20] and 0.35µm SOI SRAM[59].

The analysis determination of energy deposited which is experimentally measured and knowledge of the area of the irradiated transistor. At Full-Width at Half-Maximum, the energy deposited was measured as 0.42 pJ. Evaluating the area covered by the beam at FWHM, the analysis follows as:

$$A_{Surface}(\lambda)=\left(\int_{\infty}^{\infty}e^{-\lambda x^2}dx\right)\times\left(\int_{\infty}^{\infty}e^{-\lambda y^2}dy\right)$$

$$A_{Surface}(\lambda)=\iint e^{-\lambda\left(x^2+y^2\right)}dxdy$$

$$A_{Surface}[\lambda]=\int_0^{2\pi}d\theta\int_0^{\infty}re^{-\lambda r^2}dr \tag{2.15}$$

$$A_{Surface}(\lambda)=2\pi\left[\frac{e^{-\lambda r^2}}{2\left(\frac{1}{2\sigma^2}\right)}\right]_0^{\infty}=2\pi\sigma^2$$

$$A_{Surface}=1.133\times10^{-12}m^2$$

The transistor dimensions were given as follows: $L=0.2\mu m$ and $W=0.11\mu m$. Therefore the area of the exposed transistor is given by:

$$l\times w=2.2\times10^{-14}m^2 \tag{2.16}$$

The energy deposited onto the transistor area is simply the energy deposited in the overwrapped region which is given as:

$$\frac{A_{Trans}}{A_{FWHM-Surface}}\times0.42pJ=\frac{2.2\times10^{-14}}{1.133\times10^{-12}}\times0.42pJ=0.0194\times0.42pJ \tag{2.17}$$

The final step involves accounting for reflections at the BOX surface and also at silicon active area surface which are shown in figure 2.25 below. At Full-Width at Half-Maximum, the energy deposited was measured as 0.42 pJ

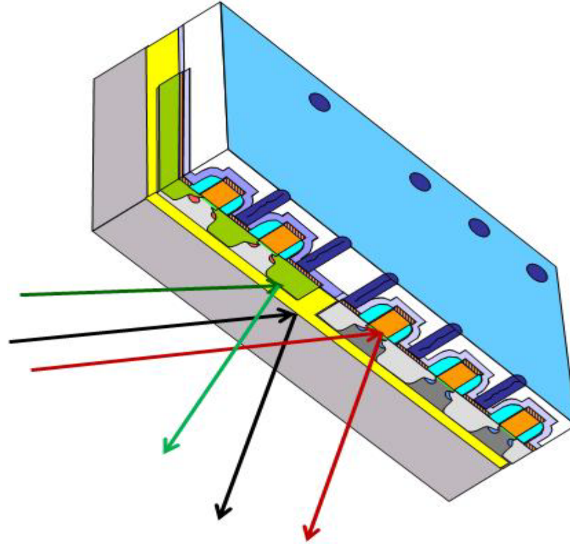


Fig. 2.25: Reflections that must be accounted for accurate determination of energy deposited on the active area.

Following this approach, an LET of 0.71 MeV-cm^2/mg was determined which closely collaborated with the LET_{th} of 0.75 MeV-cm^2/mg that was determined from heavy ions. As technology scales further, TPA technique will become harder to use and much smaller spot-size will need to be used. Figure 2.26 shows transistor layout for IBM's 45 nm technology node. We show that smaller spot-size allows for irradiation of single transistor using SPA technique. SPA allows for direct determination of the charge deposited.

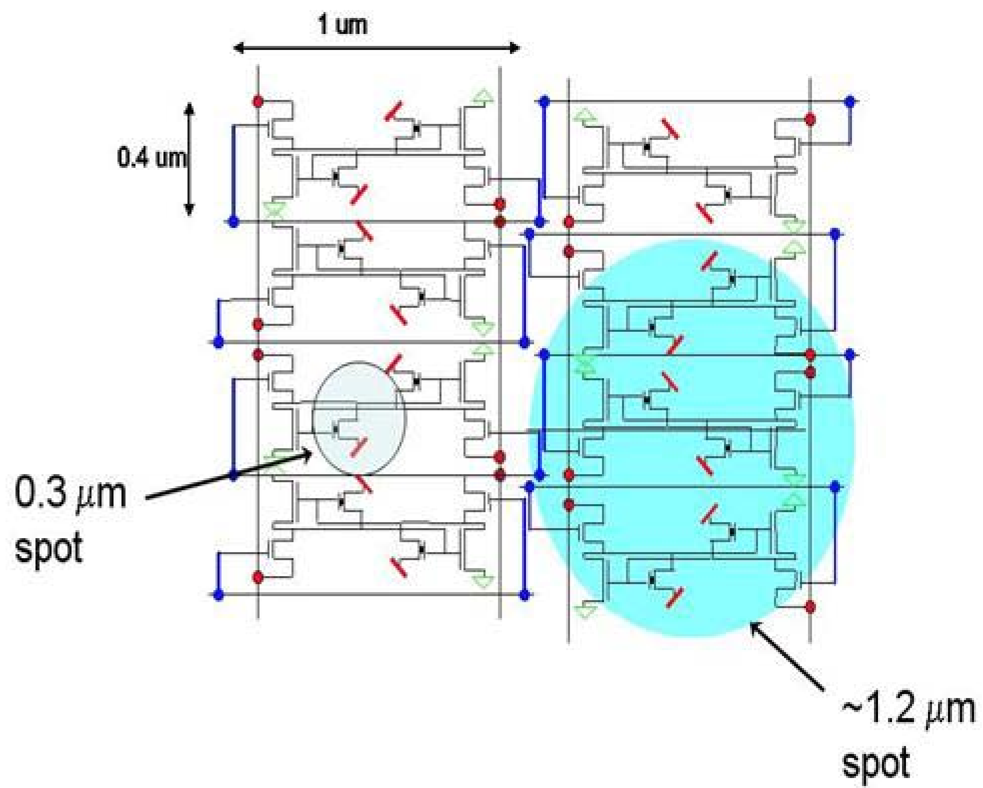


Fig. 2.26: Removal of substrate allows use of visible and UV SPA laser irradiation. For IBM 45 nm technology shown in the figure, TPA would cover more than 16 transistors as indicated by ~1.2μm spot-size. With substrate removed, one can focus on a single transistor.

Chapter 3: $In_xAl_{1-x}N$ High-Value Resistors Material

Section 3.1: Background of Material Defects in Aluminum Nitride

Subsection 3.1.1: Defect State Transformation

To understand the electrical properties of $In_xAl_{1-x}N$, material properties of its binary components need to be well understood. In this section, I review the role of DX centers, which are extended defects, characteristic to aluminum containing alloys if doped with group IV or group VI elements. Thin AlN film grown on silicon has been shown to have high interfacial quality, good thermal stability, low temperature coefficient, little sensitivity to post anneal conditions and low leakage current. With a direct band gap of about 6.2eV, AlN has the widest band gap among semiconductors known to date. It has near zero electron affinity and has demonstrated a field-emission display [60]. For material exhibiting field-emission, the control of n- or p-type conduction is essential. Unfortunately, growth of highly conductive n- or p-type AlN layers has so far proven to be very challenging because of the large number of crystal defects such as threading dislocations as well as point defects. In general, doping properties of group-IV atoms in group III-V compound are much more complex than those of group-II or group-VI atoms. For group-II and group-VI compounds, the doping efficiency is primarily determined by the electronic structure of the dopant and typically limited by its solid solubility. However, a group-IV atom is likely to become a donor when incorporated on the cation site or an acceptor if incorporated on the anion site. Consequently, group-IV elements have inherent

problem of self-compensation. In gallium and aluminum nitride compounds where there are large differences between atomic radii of cations and anions, one could expect that self-compensation is blocked by strain effects. In competition with the strain effects is the process of electron transfer from donors to acceptors. Wide energy band gap of nitrides lead to energy gains which enhance self-compensation. From previous work relating to Si in $Al_xGa_{1-x}As$, it is known that for Si, from a certain Al content and up, can lower its energy by a large lattice relaxation with the capture of a second electron [12]. This process takes place in the DX transformation represented as:

$$2d^0 \longleftrightarrow d^+ + DX^- + U \tag{3.1}$$

where d denotes a substitutional shallow impurity and DX the displaced deep state. The superscripts specify the charge states and U is the correlation energy. In the case of oxygen in $Al_xGa_{1-x}N$ alloys, high pressure experiments have shown that for Al contents $x \geq 0.35$, oxygen exhibits DX behavior [61]. The transformation of a dopant from substitutional to DX state is shown in figure 3.1 below. The red spheres represent Al atoms, blue spheres represent N atoms while green spheres are the silicon atoms on aluminum sites (Si_{Al}).

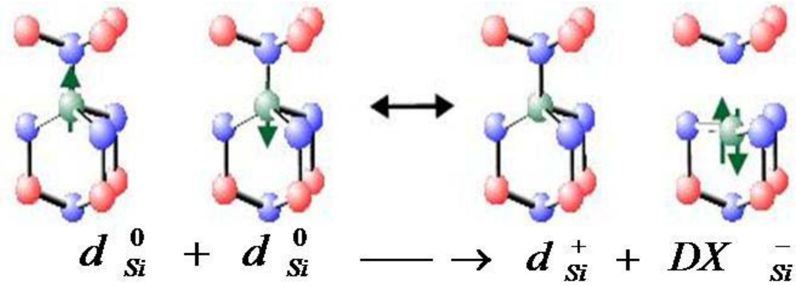


Fig. 3.1: Following large lattice relaxation of DX formation, an electron is transferred between two substitutional donors d^0, leaving a positively charged substitutional donor d^+. The process is accompanied by lowering of the total energy by . Figure after [62].

When silicon atom enters the AlN lattice, it substitutes for an aluminum atom or it fills a aluminum vacancy (V_{Al}^{3-}) site, with its first nearest neighbors being nitrogen as illustrated in figure 3.2 below. However, the silicon atom is not exactly tetrahedrally coordinated as bond *b2* is more stretched that bond *b1*. Due to uneven strain $(b2 > b1)$, b2 breaks causing silicon atom to take a DX configuration shown in figure 3.1 above and figure 3.2 below. The lattice relaxation is an exothermic processes and is the preferred state for Si_{Al} in alloys containing high concentration of Al. As mentioned earlier, the lattice relaxation resembles a vacancy-interstitial pair where the silicon appears to have left a substitutional site to an interstitial site but leaving a vacancy behind.

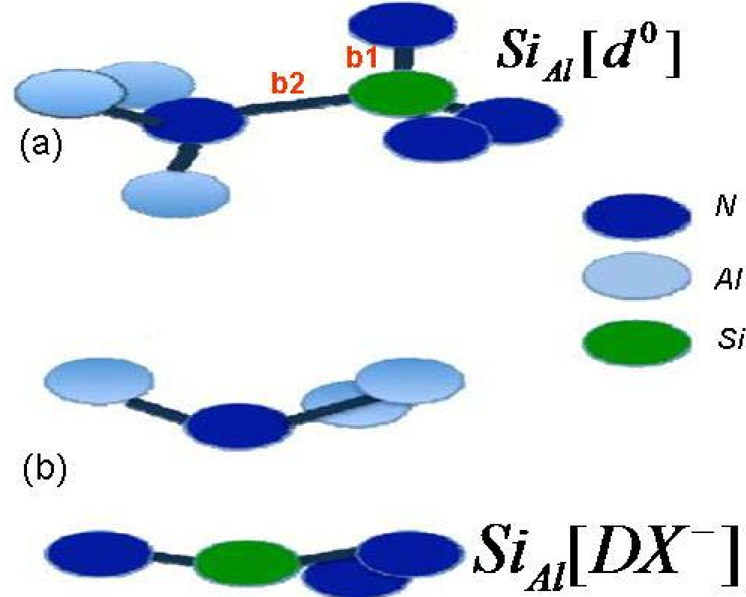


Fig. 3.2: In (a), silicon atom occupies a substitutional site. In (b), the breaking of bond b2 leads to large lattice relaxation and silicon atom's subsequent transformation to DX configuration. Figure after [63].

Several theoretical studies for Al containing materials such as AlN [64], $Al_xGa_{1-x}As$ [65],[19],[13],[66, 67], $AlAs$ [68],[66], $InGaAlAs$ [69],[70], $InGaAlP$ [71] and $Al_xGa_{1-x}N$ [72],[73] have all shown DX centers for Si_{Al} and O_N dopants, with the correlation U energy in the range of 0.325eV to 1eV. The reason why there is such a variation appears to be more attributable to the method of calculation method adopted among which there is the plane-wave pseudopotential method based on Density-Functional Theory Local Density Approximation (DFT-LDA) [72], [74],[75] Quantum Molecular Dynamics (QMD) [63] and Density Functional Theory Generalized Gradient Approximation (DFT-GGA)[76]. In figure 3.3 below, both electronic and lattice energy are shown for $Si-DX$ configuration in AlN [64]. The lowest parabola represents the DX^- state, which is occupied by two electrons. The parabola above the ground state is a thermodynamically metastable DX^0 state plus an electron in conduction band. In the work sited, authors estimated

the energy barrier (E_b^c) from d^0 to DX^- as about 200meV while the donor energy E_d is 60meV. The activation energy (E_A), for temperatures above 160 K was evaluated as 320meV which is the sum of $E_d + E_{th}$. E_o^1 and E_o^2 are optical transition energies.

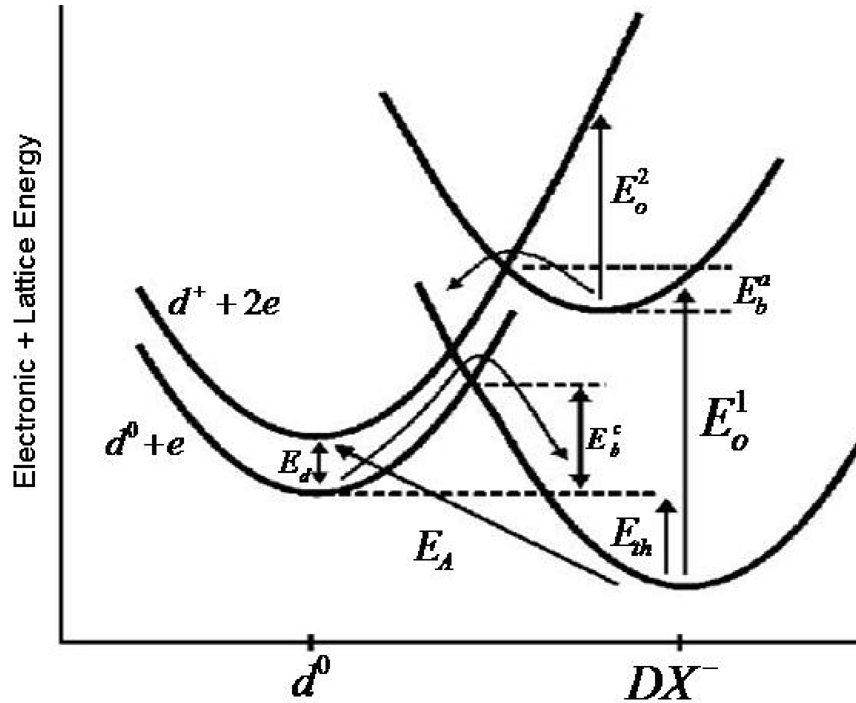


Fig. 3.3: Schematic configuration-coordinate diagram for the Si DX center in AlN [64]. The lowest right parabola is the stable DX state. E_d is the ionization energy of shallow donor, E_b^c is the barrier energy between d^0 and DX^-.

Silicon and oxygen DX centers formation in Al containing alloys constitute an important component in setting electrical properties of $In_xAl_{1-x}N$ resistor film. There are other defects specific to AlN that are just as important and I review them next.

Subsection 3.1.2: Role of Point Defects as Compensating Centers

A review of point defects in AlN is necessary in order to gain understanding of the microscopic electronic and atomic structure of $In_xAl_{1-x}N$ film. Recently, there has been theoretical studies done of native defects and impurities in AlN, following a

demonstration of highly efficient blue and green light-emitting diodes. First-principle pseudopotential calculations were performed by several authors [72],[63],[76, 77] who reported formation energies of various charge states of the N and Al vacancies and of the O and Si impurities in AlN. Gorczyca et al. expanded the study to include formation of $Mg-O$ and $Mg-V_N$ complexes and showed that such structures could play vital role in self compensation when attempting to dope AlN [78]. A low value of the formation energy indicates that a high equilibrium concentration of the defect while a high value implies a low concentration. The implication is that for a given temperature and in the limit of low concentration, one can expect the defect to obey an Arrhenius type of behavior, meaning that the logarithm of the concentrations are proportional to the formation energies.

Native defect formation and doping properties in AlN has been studied using quantum molecular dynamic [63], density function theory[72], [76] and plane wave pseudopotential [73] calculations. In general, it has been shown that doping properties of group-IV atoms in III-V compounds are much more complex than those in group-II or group-VI compounds because in the latter cases, the doping efficiency is determined by the electronic structure of the dopant and limited by its solid solubility. Since a group-IV atom can become a donor or acceptor depending on whether it replaces a cation or an anion, there is characteristic nature of self compensation. In AlN compound where there is a large difference in atomic radius between the cation and anion, one could expect that the carbon atom should substitute for nitrogen since the two atoms have almost similar atomic radii, while replacement of much larger Al

induces large lattice strain energy. However, electron transfer from donor to acceptor is in competition with strain effects. Because of the wide band gap of AlN, strain effects leads to large energy gain which enhances self-compensation.

In theoretical calculations, the formation energy of a native or an impurity defect in AlN in charge state q is [76]:

$$E_{form}(q) = E^{tot}_{defect}(q) - E^{tot}(bulk) - n_{Al}\mu_{Al} - n_N\mu_N + qE_F \quad (3.2)$$

where $E^{tot}_{defect}(q)$ is the total charge of the supercell containing the defect, $E^{tot}(bulk)$ is the total energy of a similar supercell of pure crystal in bulk, n_{Al} and n_N are the number of Al and N atoms, μ is the chemical potential and E_F is the Fermi energy. During growth process, the chemical potentials depend on the source of the atoms involved, and hence on the experimental conditions. Systematic investigation of point defects including the vacancies, interstitial and antisites in AlN has been reported[76]. Figure 3.4 below illustrates the trap levels for these defects in the energy gap.

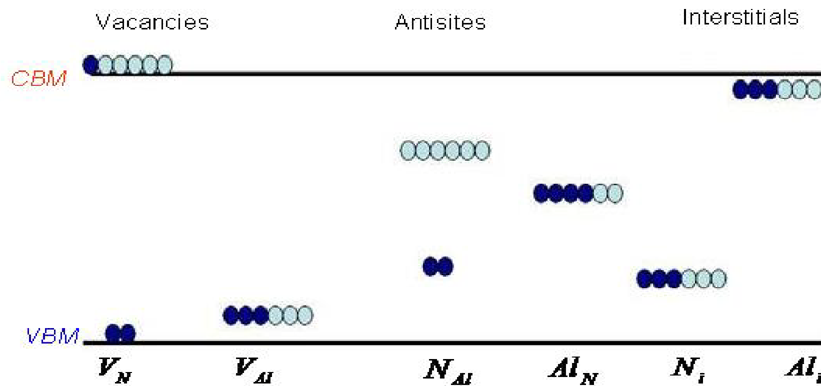


Fig. 3.4: Schematic representation of defect-induced electronic states in AlN. Filled and open circles denote electron and holes respectively. After [76].

Figure x6 shows that the aluminum vacancy (V_{Al}) creates a triplet state in the lower part of the band gap which is occupied by three electrons and can be filled with three more electrons therefore acting as a triple acceptor. Figure 3.5 show that experimental conditions determine the concentration of a particular defect. To the left, the figure shows nitrogen-rich environment while aluminum-rich growth environment is showed to the right.

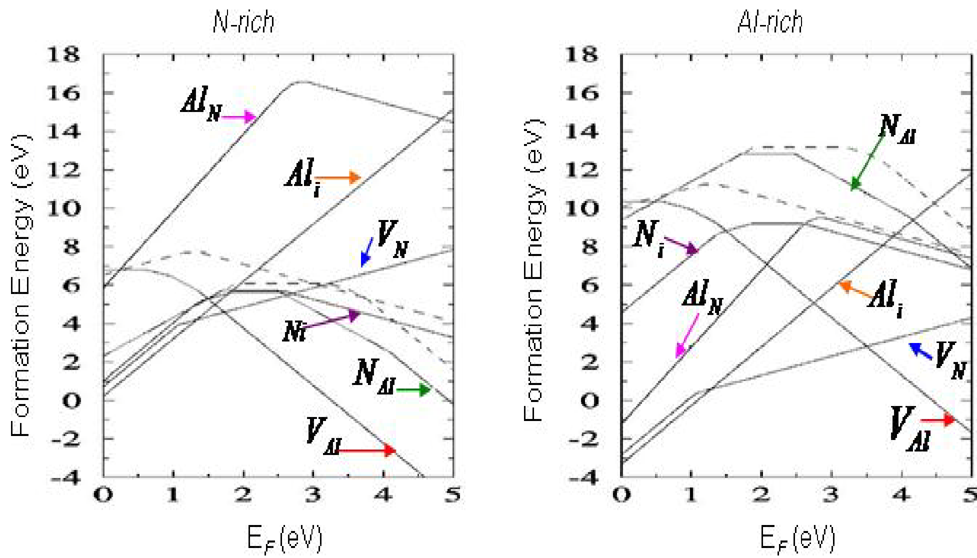


Fig. 3-5: Defect formation energies based on LDA calculation for native point defects in AlN. The left panel shows nitrogen-rich conditions while the right panel shows aluminum-rich conditions. $E_F = 0$ corresponds to *VBM* [76].

Under n-type conditions, nitrogen vacancies have very high formation energies under nitrogen-rich environment compared to aluminum-rich environment. The concentration of nitrogen vacancies is bound to be much less under nitrogen-rich environment. However, whether the conditions are nitrogen-rich or aluminum-rich, aluminum vacancies (V_{Al}^{3-}) are acceptors have the lowest formation energy under n-type conditions. These vacancies are expected to compensate donor impurities, thus limiting the electron concentration if Si or O impurities are present. The rest of the

other defects have relatively high formation energies which means they exist in relatively small concentrations. Although the small concentration of these defects cannot dominate the electronic structure of AlN or that of ternary $In_xAl_{1-x}N$, the total aggregate of these smaller concentration can have significant effect by acting as electron sink holes as the Fermi level moves toward mid gap. Such an effect can be very significant in controlling the Temperature Coefficient of Resistance (TCR) of the resistor film.

Subsection 3.1.3: Defect Complexes are electron Traps or Donors

The role of defect complexes is not very different from native defects but as illustrated in figure 3.7 below, the formation energy of $V_{Al} - O_N$ complex is clearly lower than that of isolated cation vacancy. Typically, the most logical constituents for defect complex are positively charged donor-like defects and negatively charged cation vacancies with acceptor character, which are likely to attract each other due to electrostatic attractions.

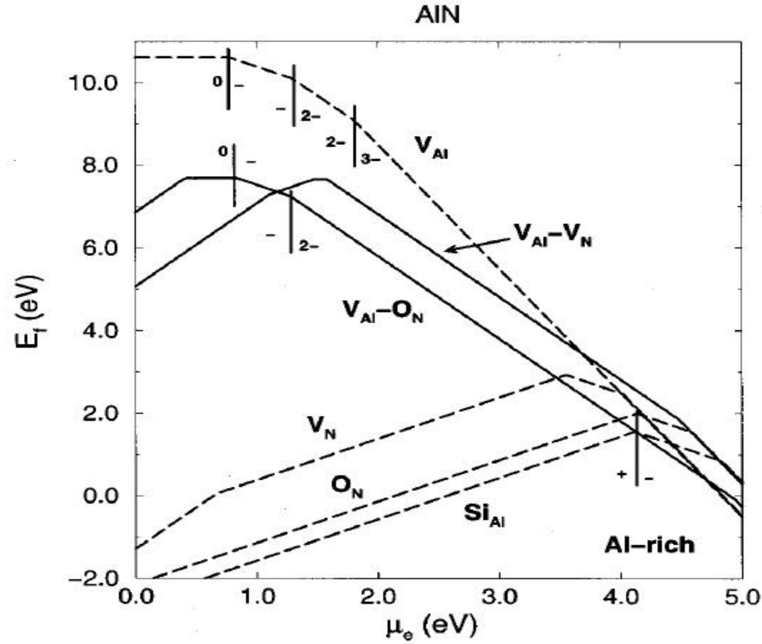


Fig. 3.7: Formation energies and ionization levels for defects in AlN. The $V_{Al} - O_N$ defect complex has formation energy that is lower than that of an isolated cation vacancy. Figure after [72].

The formation energy of $(V_{Al} - O)$ complex suggests that under n-type conditions, it is the dominant complex which is doubly negatively charged. In Kroger-Vink notation, the formation of this complex is given by:

$$V_{Al}^{'''} + O_N^{\bullet} \longrightarrow \left(V_{Al}^{'''} - O_N^{\bullet}\right)^{''} \qquad (3.3)$$

Although not shown, other possible defect complexes from the same constituent defects include:

$$V_{Al}^{'''} + 2O_N^{\bullet} \longrightarrow (V_{Al}^{'''} - 2O_N^{\bullet})^{'} \qquad (3.4)$$

as well as :

$$V_{Al}^{'''} + 3O_N^{\bullet} \longrightarrow (V_{Al}^{'''} - 3O_N^{\bullet})^{x} \qquad (3.5)$$

Similar defect complex reaction is expected relating to nitrogen vacancies (V_N^{3-}) and silicon $(Si_{Al}^{\bullet})$ donor atom.

Section 3.2: Background of Material Defects in Indium Nitride

Subsection 3.2.1: Role of Fermi Stabilization Energy

Indium nitride is of considerable interest because of its small effective mass, leading to a large electron mobility and high carrier saturation velocity. Much of the interest has been because of it potential in high speed and high frequency electronic devices. In this section, I consider the same properties and show how if incorporated with those we found in aluminum nitride, cross-coupled latch resistor circuits can be made for mitigating single event upsets in SRAM memories for space and nuclear applications. Recently, theoretical [79-82], and experimental [83],[84, 85] studies have shown that the fundamental band gap of InN is about 0.7eV, far less than had been previously believed to be at 1.9 eV to 2.2eV. This finding has been made possible because better computation tools and growth techniques have recently become available. The issue of the true band gap $(0.7eV)$ has recently been resolved by the demonstration of an unusually large Burstein-Moss shift at high electron concentration. The seemingly inherent n-type conductivity can be attributed to the location of the Fermi stabilization energy (E_{FS}) high in the conduction band of InN, such that native defects are primarily donor-like as explained by the amphoteric defect model (ADM) [86, 87]. According to this model, the formation energy of a native defect is dependent on the location of the Fermi level (E_F) with respect to the Fermi stabilization energy (E_{FS}), which is defined as the average energy level of the native defects. The formation energy of the donor-like/acceptor-like defects decreases for $E_F < E_{FS} / E_F > E_{FS}$. When defects are formed in the material, E_F moves

toward E_{FS}, eventually pinning E_F at E_{FS} with the formation of donor and acceptor defects at equal rates. Because E_{FS} is located high in the conduction band in InN [86], induced native defects are primarily donor-like and consequently, they should be expected to play a significant role in setting electrical properties in $In_xAl_{1-x}N$ film resistor if they exist in large concentrations.

Subsection 3.2.2: Cluster and Complex Defect Formation in InN

There has been renewed interest in InN which is evidenced by the recent body of theoretical investigations[79],[80, 88] aimed at understanding its electronic properties since evidence became clear that indeed, the energy band gap is far smaller than had been previously believed. Unlike the case in AlN, no evidence of DX center formation has been found in InN. As we saw in the AlN, the N and cation vacancies have the lowest formation energies and oxygen and silicon atoms are donors and are easily incorporated. The major difference between AlN and InN structures is that as shown in figure 3.8 below, in InN, defects tend to be more stable as complexes. The indium antisite and nitrogen vacancy cluster results in local In-rich regions. It was also shown that indium vacancies prefer to cluster together in 2 or 3 indium vacancies, where the $2V_{In}$ complex could be described as a N-split interstitial plus a mixed vacancy complex, $V_N + 2V_{In}$ [80]. Under N-rich conditions, the nitrogen interstitial is a triple donor while under In-rich conditions, the indium antisite in charge state 4+ has the lowest formation energy in p-type material. For n-type material, the nitrogen vacancy complexes are more favorable. Although indium vacancy clusters have higher formation energies, it was shown that formation of large

indium vacancy cluster is quite possible because the formation energy decreases significantly (per vacancy), with increasing number of vacancies in a cluster. Furthermore, it is also possible for these clusters to form under none-equilibrium growth conditions.

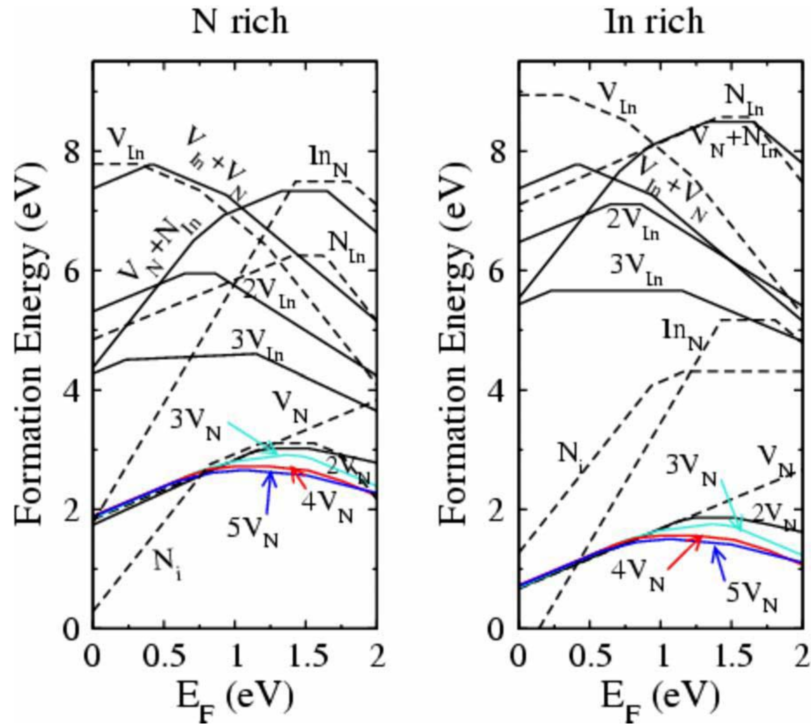


Fig. 3.8: Formation energies as a function of the Fermi level for anions and cation vacancies, antisites, *N* intersitial and complexes in *InN* [80]. The zero of the Fermi level corresponds to top of *VBM*.

In figure 3.9, the formation energies for the vacancy complexes are given per vacancy. For p-type material, the figure shows that the single nitrogen vacancy V_N^+ has the lowest formation energy.

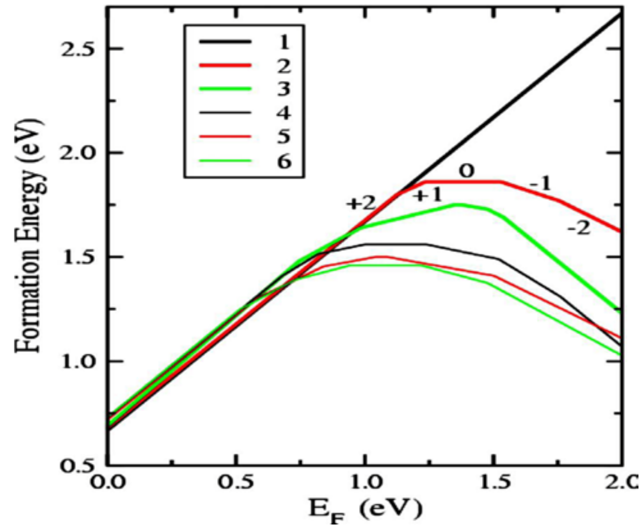


Fig. 3-9: Formation energies per vacancy as a function of the Fermi level for the nitrogen clusters in *InN*. Kinks in the curves shows transitions between charge states [79].

In a more n-type material, lower positively, neutral and negatively charged complexes are predicted. The formation energy per vacancy of the vacancy complex or cluster decreases with the increasing number of vacancies except for the highest positive charge sates.

Subsection 3.2.3: Conclusion

The formation of Fermi stabilization energy high in the conduction band creates highly conductive paths in In-rich regions of the $In_xAl_{1-x}N$ because native defects are primarily donor-like. The issue of defect clustering is also of great significant because as we show in section 3.5, annealing eliminates some of these defects if they are not immobile. If clustering of these defects results in regions of In-rich regions, following the anneal process, the loss of these defects should result in a much more conductive film because of higher indium concentration. The film would behave resistor in parallel, with electrons choosing the path of the least resistance.

Section 3.3: Point Defects: Energy and Configuration

Subsection 3.3.1: Vacancy-Impurity Binding

Lattice defects play important role in solid state reaction because diffusion processes in solids are determined by the concentration and mobility of such defects. Lattice defects, vacancies and interstitial atoms take part in a variety of processes leading to phase changes, precipitation, order-disorder formation and chemical reactions. At any temperature where the vacancies are mobile, the excess vacancies tend to anneal out of the sample. Whenever there is a positive binding energy between vacancies and impurity atoms, some of the vacancies will be bound to the impurities, thus forming impurity-vacancy complexes.

The presence of point defects is better understood when electrostatic forces are considered in a material. In any structure with large fraction of ionic bonding character, minimum electrostatic energy is achieved when cation-anion attractions are maximized and like-ion repulsion is minimized. In other words, cations prefer to be surrounded by the maximum number of anions as first-nearest neighbors and vise versa. At the same time, cations prefer to maintain maximum separation from other cations that are their second-nearest neighbors. This means that ions of like charge prefer to be electrostatically shielded from one another as much as possible by anions or vacancies of opposite charge. It follows to maintain electrostatic potential balance, vacancies and/or interstitial atoms are positions in the lattice to provide shielding of cations or anions of like charges. If these defects are electron donors, they will increase the concentration of the electrons in the conduction band. If on the other

hand these defects are electron acceptors the converse is true. Below, figure 3.10 illustrates formation of schottky and frenkel pair. These defects may form to relief the electrostatic strain. Usually, either of these defects would be more favored but not both. Charged defects could also form to create relief due to electrostatic forces. The following are two such examples:

$$N_N^x = V_N^{3+} + \frac{1}{2}N_2(g) + 3e' \tag{3.6}$$

$$Al_{Al}^x = Al_i^{3+} + 3e' \tag{3.7}$$

In equation (3.6) nitrogen atom leaves its site and is released in as gas leaving a vacant site and three electrons able to roam freely. In the case of equation (3.7), if the aluminum interstitial defect formation is more energetically stable, aluminum can leave its site and take on interstitial position while releasing its electrons. In either case, the material becomes more conductive than if these defects did not form. A detailed treatment on the rules governing formation of these defects by Chiang et al, [9].

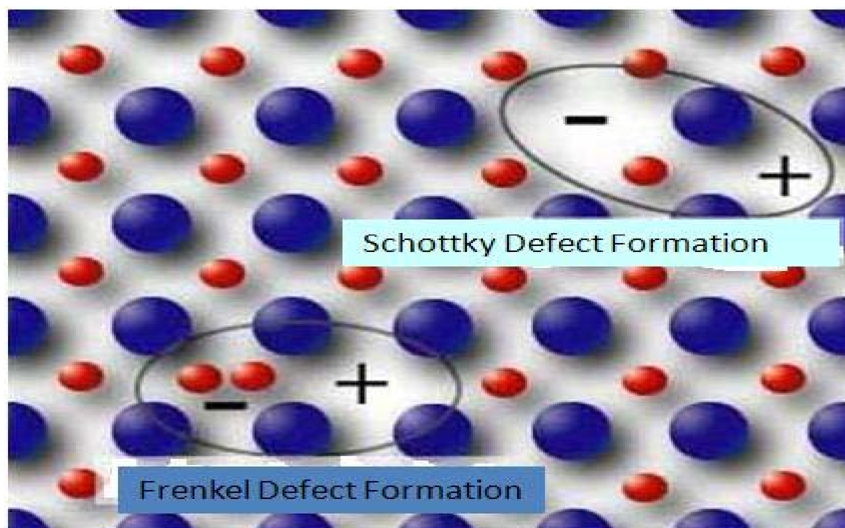


Fig. 3.10: Schottky and frenkel pair defects. To minimize electrostatic energy, these defects may form to shield a cation or anion from repulsion by second-nearest neighbor

As the defects form they are configured to be positioned throughout the material and the position each defect takes depends on the coordination number of the atom they will be shielding. If for example, M is the coordination number of an impurity atom, then if one excludes multiple complexes, each complex considered in the calculation pre-empts M lattice sites and hence, the number of ways of arranging C complexes on $M \times N_d$ sites (N_d is the impurity concentration) is given by[89]:

$$W = \frac{(MN_d)}{(MN_d - CN_d)!C!} \tag{3.8}$$

where C is the number of complexes.

Application of stirling's formula and minimization of the free energy with respect to C gives:

$$\frac{C}{N_d - C} = M \exp\left(-\frac{E_S^f}{kT}\right) \tag{3.9}$$

where E_S^f is the energy required to remove an atom which is nearest neighbor to an impurity and place it on the surface. E_S^f can be expressed as the difference between the energy of formation of the vacancy, E^f, and the binding energy, E_B, of a vanacny to an impurity atom. Hence:

$$E_S^f = E^f - E_B \tag{3.10}$$

it follows that equation (3.24) can be expressed as[89]:

$$\frac{C}{N_d - C} = Me^{\frac{E_B - E_S^f}{kT}} = MV_{free}e^{\frac{E_B}{kT}} \tag{3.11}$$

where V_{free} is the concentration of free vacancies in the crystal.

Two important energy terms give rise to the binding energy of a defect to an impurity. One is the change in the strain energy around the impurity and the other is the electrostatic interaction between the defect and the impurity. If the atomic size of the impurity differs from that of the host atom, the strain surrounding the impurity atom may be relieved by placing a defect adjacent to the impurity. One would expect that the strain interaction between an oversized atom and a vacancy to be bound in the regions of compression while interstitials in the regions of dilation.

Subsection 3.3.2: Effect of Vacancy-Impurity Binding on Annealing

When vacancy concentration is high, excess vacancies move to and are eliminated at sinks. In absence of impurities and for a random distribution of vacancies, this decay is exponential. When on the other hand the vacancies are trapped at impurity sites to form complexes, the simple kinetics is disturbed. In consideration of the kinetic situation, the mobility of the impurity-vacancy complex relative to the vacancy is important. If the complex is trapped by the impurity, these can be eliminated from the kinetics system because they can only be part of the system upon decomposition of the complexes. In the opposite case which is characterized by high complex mobility, the complexes carry both the vacancy and the impurity to segregation and elimination sites. In the later case, the impurity is segregates at dislocations or precipitation nuclei which becomes important part of the annealing process.

Vacancy migration with immobile complex formation may be represented by the following chemical reaction:

$$V + N_{unbound} \underset{K_2}{\overset{K_1}{\longleftrightarrow}} C \tag{3.12}$$

$$V \xrightarrow{K_3} Sinks \tag{3.13}$$

where *V, N*$_d$ and *C* ate the concentration of vacancies, unbound impurities and vacancy-impurity complex respectively. K_1, K_2 and K_3 are the corresponding rate constants. The physical meaning of equation (3.13) is that vacancies disappear by migrating to a fixed number of sinks.

Subsection 3.3.3: Energetic Stability of Crystalline Structure

Understanding that defect incorporation in a crystal or a polycrystalline structure is an essential component part of energetic stability for a system is vital in understanding why some materials are more prone to have the defects than others. When we consider energetic stability of a system, *Madelung constant* is the definition we attribute to the energy of a particular structure relative to isolated constituent atoms of molecules. If for example we consider M atoms of a binary compound such as AlN in which the cation valence is Z_C and the anion valence is Z_A, after chemical reaction, the electrostatic energy of the system is given by [9]:

$$E_C = M \sum_j \frac{Z_i Z_j e^{2b}}{4\pi\varepsilon_0 R_{ij}} + \frac{B_{ij}}{R_{ij}^n} \tag{3.14}$$

where B_{ij} is an empirical constant, R_{ij} is the separation between any two atoms and n is ~10 [9].

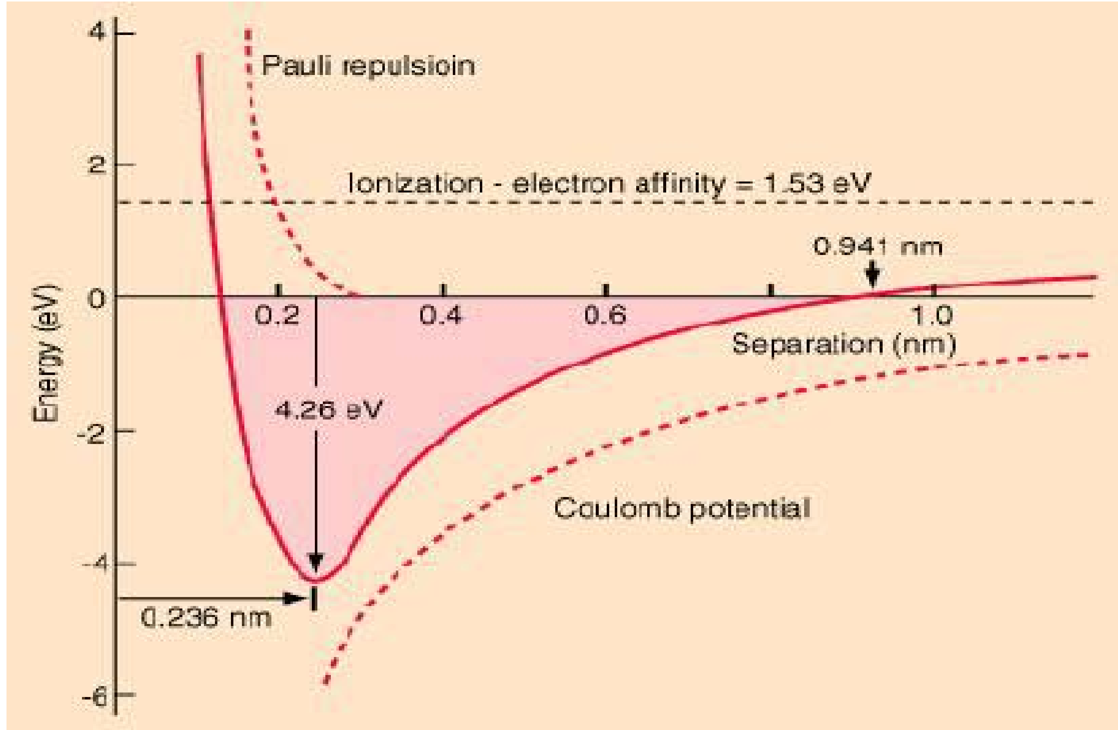


Fig. 3.11: Contribution of electrostatic attraction and repulsion due to Pauli exclusion to the ionic bond energy, where R is the ion separation. For ternary or quaternary material forms, there several different ions and R is different for different ion resulting in defects formation to shield ions from the next nearest neighbors

Equation (3.29) evaluates to:

$$E_C = M\left[\alpha \frac{Z_C Z_A e^2}{4\pi\varepsilon_0 R_0} + C'\right] \tag{3.15}$$

where α is the *Madelung constant* and is the summation of electrostatic interactions given by[9]:

$$\alpha = -\sum_j \frac{(Z_i / |Z_i|)(Z_j / |Z_j|)}{X_{ij}} \tag{3.16}$$

where R_0 is the sum of ionic radii of Al and N $R_0 = R_A + R_C$ and C is given by[9]:

$$C = -\sum_j \frac{B_{ij}}{X_{ij}^n} \tag{3.17}$$

In equation (3.15) C is the sum of the short-range repulsive interaction. We see from equation (3.15) that the energy is at a minimum at a separation R_0. If an impurity of significantly larger ionic radius in incorporated, there is local disruption of energy of interaction. To recover, electronic defects of opposite sign surround the impurity with much larger nucleus to shield it from repulsion coming from the second nearest neighbors. These defects are immobile and cannot be annealed out by heating. In the immobile mode, these defects form complexes which may trap electrons from impurity donors or depending on their charge states, they could likewise add to the electrons causing the material to be more conductive. The effect of annealing has been shown that it could lead to impurities moving to segregation sites, a move that could make the doped material to become more resistive, with the defects moving to annihilation sites.

Section 3.4: Formation of Ternary $In_xAl_{1-x}N$ Alloy from Binary Compounds

Subsection 3.4.1: Utility of Vegard's Law and Its Application

In early application of x-ray diffraction to the analysis of crystal structures, Vegard observed that in many ionic salt alloys, a linear relationship exits at constant temperature between the crystal lattice and concentration. This relationship is what came to be known as the Vegard's law. An essential issue in the theory and practice of alloy formation is the way microscopic crystal structures of alloys depends on the atomic properties and relative concentrations of the constituent elements. There are several factors that could affect properties of crystal structures. They include: (a) the relative atomic sizes of the elements, (b) the relative volume per valence electron in

the crystal of the pure elements, (c) the Brillouin-zone effects and, (d) the electrochemical differences between the elements. The physical properties of the ternary compounds are usually investigated based on Vegard's law. Examples of such properties include the material band gap and lattice parameters

In subsequent extension of this law to metallic alloys, the majority of the systems have been found to deviate in second order perturbation. For a ternary alloy $A_xB_{1-x}N$, the dependence of the fundamental gap on the mole fraction is close to linear and is usually approximated as:

$$E_g(x) = xE_g(AN) + (1-x)E_g(BN) - bx(1-x) \quad (3.18)$$

where the deviation from Vegard's law is taken into account through the bowing factor b. Figure 3.12 below is the plot of the energy band gap based on equation (3.31).

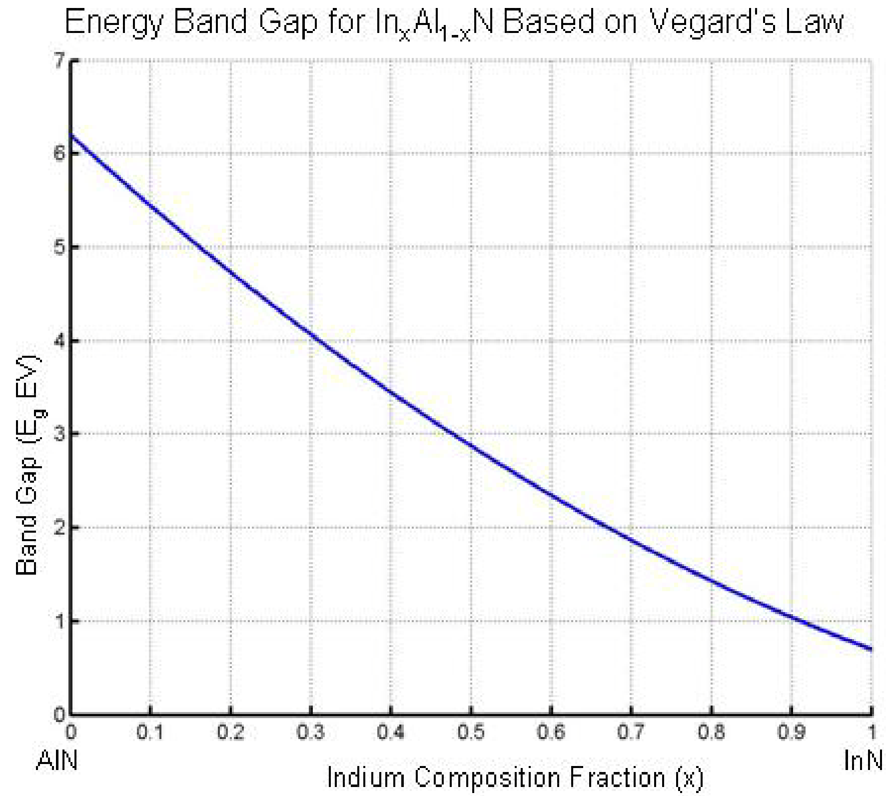


Fig. 3.12: Calculated energy band gap of $In_xAl_{1-x}N$ based on Vegard's law.

In developing the model for evaluating sheet resistance for $In_xAl_{1-x}N$, we have relied on the use of Vegard's law in estimating other material properties. Previously, we reported results of resistivity measurements and predicted the material band gap based on the Vegard's law [90]. Within the energy band, there are several traps that act as shallow and deep donor traps. Figure 3.13 shows some of the most important traps determing the electrical properties of the $In\ Al_{1-x}N$ alloy. Aluminum vacancies are acceptor traps and they primarily compensate donor dopant.

Fig. 3.13: Energy band diagram of $In_xAl_{1-x}N$ film resistor[90, 91]

In modeling the electrical characteristics of the film, consideration must be made on existence of multiple dopants, in this case, both silicon and oxygen were present. Silicon was intentionally introduced in the material but oxygen got in the material as an impurity to nitrogen reactant. The two elements are relatively similar in the sense that both can act as shallow as well as deep level trap centers and hence they can be viewed as amphoteric traps. The oxygen deep level trap (DX_O^-) and silicon deep level trap (DX_{Si}^-) are quite alike, the only difference being that the DX_O^- is 570meV[74] below the substitutional level while DX_{Si}^- is thought to be 320meV[64] below the substitutional level. The aluminum vacancy (V_{Al}^{3-}) is said to be within 0.5-1.7eV[73] above the VBM. Other defects that are important are the nitrogen and indium vacancies. While nitrogen vacancies are donors under n-type conditions, existence of indium vacancies provides voids that silicon atom can move in to rather than stay in interstitial locations in the film. In subtitutional position, silicon is a donor

The simulation model considers the effect of co-doping using Si and O. Studies have shown that both of these dopants for DX centers in Al containing alloys. The DX trap level for O is located at 570 meV below donor substitutional level [74] while Si DX trap level is 320 meV below the donor substitutional level [64]. For the purpose of simulation, we set the concentrations of both silicon and oxygen at $10^{18}cm^{-3}$, We set the number of available sites available for occupation by $V_{In}^{'''}$, $V_{Al}^{'''}$ and $V_{N}^{\bullet\bullet\bullet}$ as $10^{20}cm^{-3}$. Other physical constants are tabulated in table H below while the rest of material parameters were derived using Vegard's law.

Subsection 3.4.2: Determination of Material Physical Properties

Having determined the band gap, we then need to determine the number of allowed states both in the conduction band and the valence band. To proceed, we need to determine the number effective density of states. The effective density of states at the conduction and the valence band edges, respectively are given by the following expressions:

$$N_c = 2 \times \left(\frac{2\pi m_e^* kT}{h^2} \right)^{3/2} \tag{3.19}$$

and

$$N_v = 2 \times \left(\frac{2\pi m_h^* kT}{h^2} \right)^{3/2} \tag{3.20}$$

where m_e^* and m_h^* are the effective masses of electrons and holes. Based on Vegard's law, the effective masses of electron and positron based were evaluated. The results are plotted in figure 3.14 and figure 3.15 below.

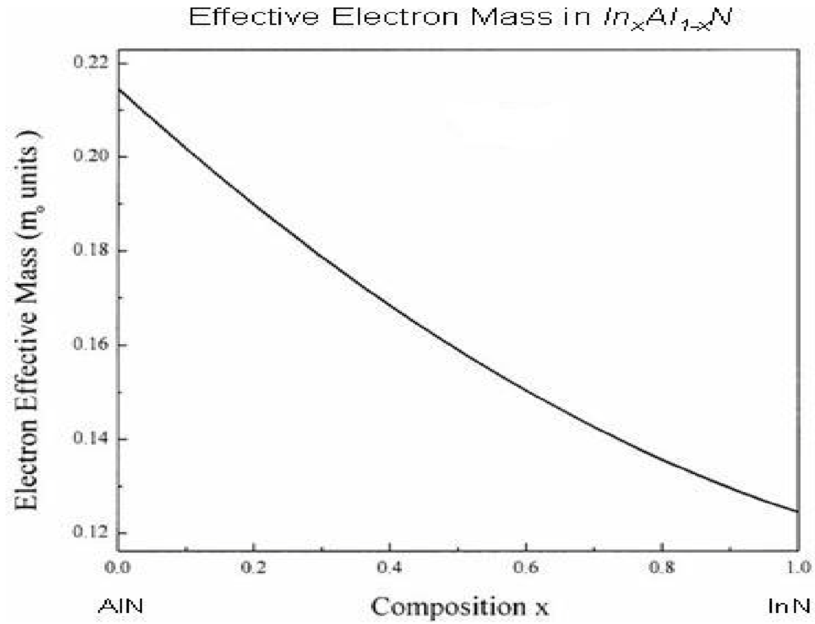


Fig. 3.14: Effective Electron mass in $In_xAl_{1-x}N$ calculated using Vegard's law.

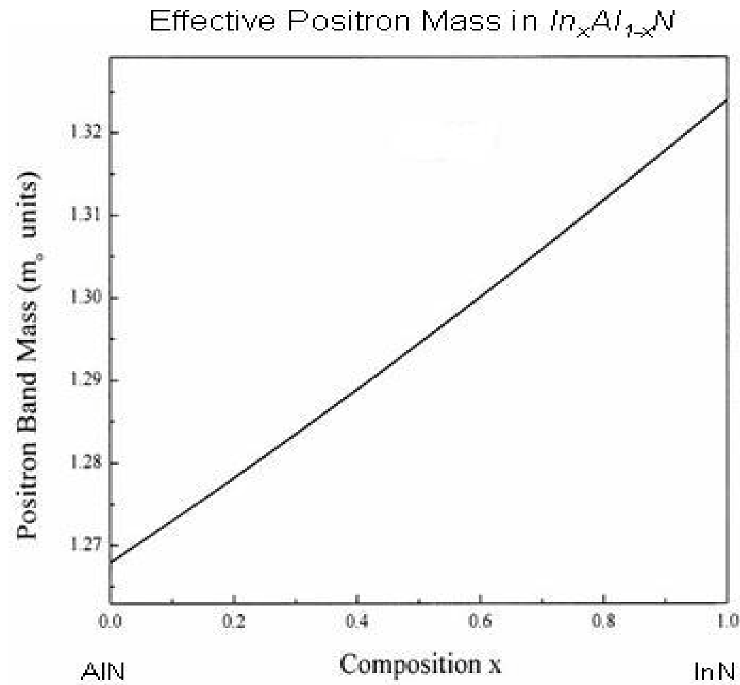


Fig. 3.15: Effective positron mass in $In_xAl_{1-x}N$ calculated using Vegard's law.

An important property of electrons or holes in crystals is their distribution at thermal equilibrium among the allowed states. In evaluating the ways to populate allowed

energy states with particles subject to the Pauli Exclusion Principle leads to Fermi-Dirac distribution function $f_D(E)$ given by the following relation:

$$f_D(E) = \frac{1}{1 + \exp[(E - E_F)/kT]} \tag{3.21}$$

where E_F is the Fermi level. Another step in determining the actual concentrations is to evaluate the Fermi level E_F which is given by:

$$E_F = E_C - \frac{kT}{q}\ln\left(\frac{N_C}{N_d}\right) \tag{3.22}$$

for an intrinsic semiconductor. To evaluate donor binding energy E_d , we use the expression give by:

$$E_c - E_d = \frac{m_e^* q^4}{8(\varepsilon_0 \varepsilon_r)^2 h^2} \tag{3.23}$$

which for $In_x Al_{1-x} N$ at $x = 0.6$, $m_e^* = 0.15 m_0$ and therefore $E_c - E_d$ is $0.0029 eV$. Thus, $E_d = 3.149 eV$.

Subsection 3.4.3: Evaluating Free Carrier Concentration

The presence of ability of both silicon and oxygen to transition between shallow and DX centers requires that electron concentration model consider these trap's occupancies as the Fermi level change with temperature.

The formation of DX centers follows loss of two substitutional atoms with one giving up an electron to become N_D^+ with the one gaining the electron becoming N_{DX}^- since it has captured the electron. We propose that what is left after these two

atoms pair up is what can participate in conduction. This relation follows from DX formation as presented above and is repeated in figure 3.16 below for convenience.

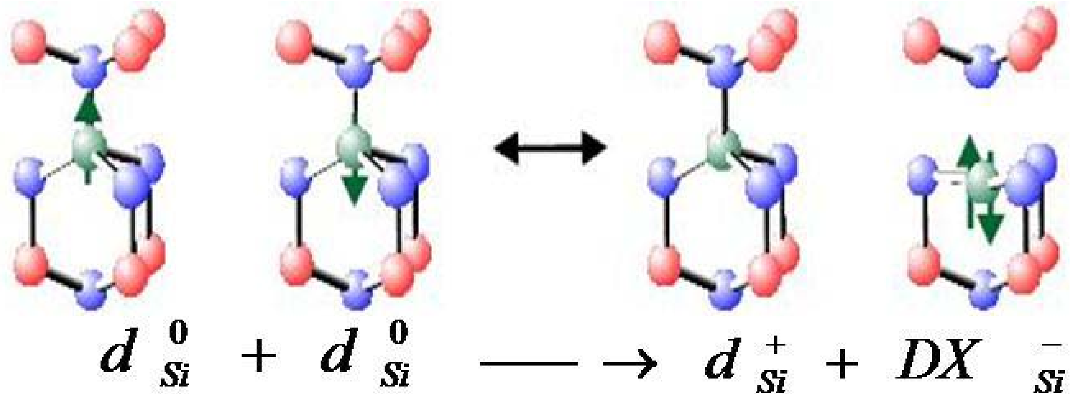
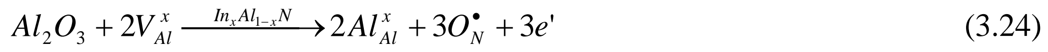


Fig. 3.16: DX trap formation to the right takes an electron from one of the substitutional silicon atoms, effectively depriving the loosing atom ability to donate electron in the conduction band even though the loosing atom still remains in substitutional level. Figure after [62].

Further analysis of DX formation and its impact in electrical properties of a material is presented in the appendix section.

Another important consideration is that of point defects. Among the defects that are of interest are the aluminum vacancies, indium vacancies, nitrogen vacancies as well as antisites and interstitial. When these defects form during the growth processes, they become locked in the film and they or the complexes they form can act as donors, acceptors or be amphoteric depending on the position of the Fermi level. Studies have shown that in n-type doped material, nitrogen vacancies prefer forming complexes or clusters [79]. The formation of such nitrogen vacancy clusters creates local indium-rich regions with metallic-like bonding. The indium-rich or aluminum-rich regions can form the basis of interstitial indium or aluminum defects. Stampfl et al., have reported that in AlN that for the substitutional nitrogen antisite (N_{Al}), a doubly occupied singlet state in the band gap forms as well as an empty triplet state

higher in the band gap which can trap six electrons. Depending on the position of the Fermi level, N_{Al} can act as an acceptor or a donor. The authors also reported that the aluminum antisite (Al_N) and nitrogen interstitial behave the same way. The aluminum interstitial (Al_i) introduces a triplet state in the upper part of the band gap which is occupied by three electrons and is a donor[76]. To appreciate the effect of these defects, consider Al_2O_3 incorporation in $In_xAl_{1-x}N$. Aluminum can either take a substitution position or it could take an interstitial position.



$$Al_2O_3 + 2V_{Al}^{x} \xrightarrow{In_xAl_{1-x}N} 2Al_{Al}^{x} + 3O_N^{\bullet} + 3e' \qquad (3.24)$$

or if it is substitutional and interstitial,

$$Al_2O_3 + V_{Al}^{x} \xrightarrow{In_xAl_{1-x}N} Al_{Al}^{x} + Al_i^{\bullet\bullet\bullet} + 3O_N^{\bullet} + 6e' \qquad (3.25)$$

Or if no aluminum vacancies available, it could be just interstitial written as:

$$Al_2O_3 \xrightarrow{In_xAl_{1-x}N} 2Al_i^{\bullet\bullet\bullet} + 3O_N^{\bullet} + 9e' \qquad (3.26)$$

Oxygen takes a nitrogen site accompanied by release of a single electron per site. As part of future work, a complete model will need to include the point defects as well as the complexes they form. Currently, there is no reported data for the traps of these defects.

Table 3.1

Parameter	InN	AlN	
ε_r	15.3[92]	15.3[92]	
ε_0			$8.85\times10^{-14}\,F/cm$
Mass Density	$6.8g/cm^3$	$3.260g/cm^3$	$\rho_{InAlN}=5.384g/cm^3$, x=0.6
Molar Mass	$128.8g/mol$	$40.99g/mol$	MW_{InAlN} =93.7g/mol X=0.6
Boltzmann's Constant			$k=1.38\times10^{-23}\,J/K$
Avogadro's Number			$N_A=6.02\times10^{23}\,molecules/mol$
Planck's Constant			$6.63\times10^{-34}\,J-s$
m_e^*	0.12	0.27	
m_h^*	1.325	1.268	
Si donor			$N_D=10^{18}\,cm^{-3}$
O donor			$N_D=10^{17}\,cm^{-3}$
$E^-_{DX_{Si}}$			$280meV$
$E^-_{DX_O}$			$300meV$

In the model that is proposed in the appendix, we include defects whose trap levels are known or can be estimated from literature. We propose the effective electron concentration to be given by:

$$n = N_{d^+_{Si}} + N_{d^+_{OX}} + O^{\bullet}_N - N_{DX^-_{Si}} - N_{DX^-_{OX}} - N_{V'''_{Al}} - p \qquad (3.27)$$

Section 3.5: Modeling Carrier Transport and Sheet Resistance

Subsection 3.5.1: Electron Mobility Model

In order to model the sheet resistivity, a model of carrier transport was needed that includes both doping concentration and temperature dependence. The first consists in adequate approximation of the doping level dependence of the mobility at room temperature on the base of the well known Caughey-Thomas approximation:

$$\mu_0 = \mu_{\min} + \frac{\mu_{\max} - \mu_{\min}}{1 + \left(\frac{N}{N_{ref}}\right)^{\alpha}} \tag{3.28}$$

where $\mu_{\min}$, $\mu_{\max}$, N_{ref} and α are fitting parameters. $\mu_{\max}$ is the mobility in the undoped samples, $\mu_{\min}$ is the mobility in degenerately doped sample, α is a measure of how quickly the mobility changes from $\mu_{\max}$ to $\mu_{\min}$ and N_{ref} represents the carrier concentration at which the mobility is half way between $\mu_{\max}$ and $\mu_{\min}$. To address the issue of temperature dependence, the effect of the temperature dependence of the low-field mobility can be written as:

$$\mu_0(N,T) = \mu_{\max}(T_0) \times \frac{F(N) \times (T/T_0)^{\beta}}{1 + F(N) \times (T/T_0)^{\alpha+\beta}} \tag{3.29}$$

where $$F(N) = \frac{\mu_{\min}(T_0) + \mu_{\max}(T_0) \times (N_{ref}/N)^{\delta}}{\mu_{\max}(T_0) - \mu_{\min}(T_0)} \tag{3.30}$$

where $T_0 = 300K$ and $\mu_{\min}$, $\mu_{\max}$, N_{ref}, α, β and δ are fitting parameters of equation (3.45). Just as other material parameters have been calculated, the parameters in equation (3.45) of both binary compounds are used to calculate the parameter of $In_xAl_{1-x}N$ for a given composition based on Vegard's law.

Subsection 3.5.2: Evaluating Sheet Resistance

In figure 3.17 below, the sheet resistance for $In_x Al_{1-x} N$ based on the proposed model is presented. The sheet resistivity variation with temperature in the temperature based on the model is shown in green. The experimental data is shown in blue. The plot show very good agreement between the model and the experimental data for temperature starting from about 260K to 398K. It can be argued that for the temperature range of typical device operation, there is a pretty good agreement. In table 3.2, we tabulate measured sheet resistance along with experimental data for negative 55°C to positive 125°C.

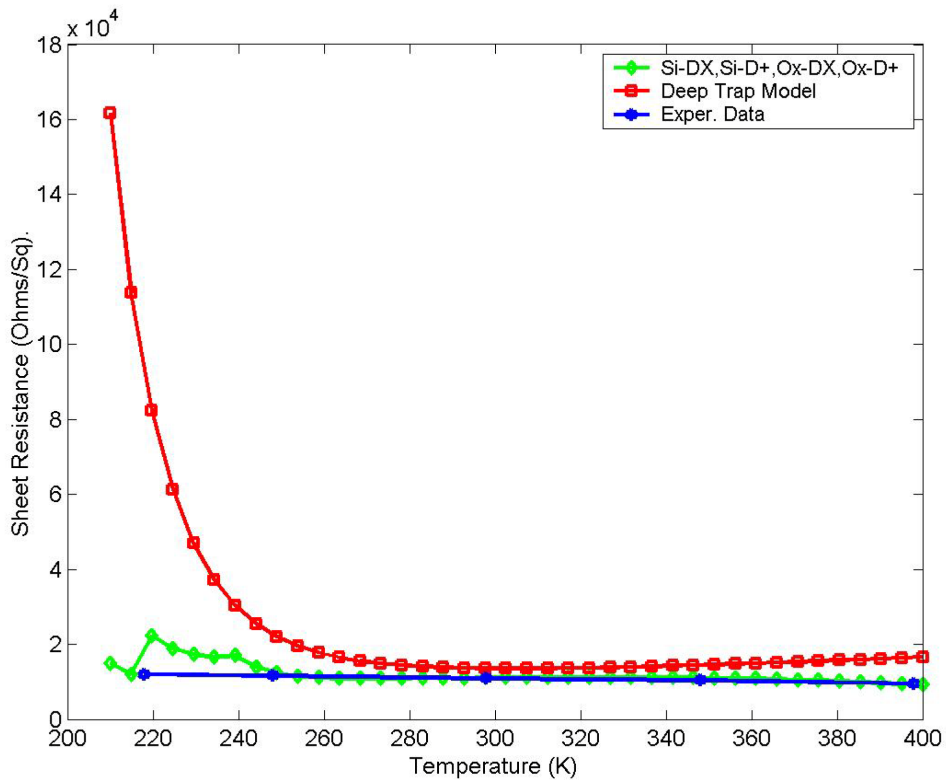


Fig. 3.17: Change of sheet resistance from 200K to 400K is less than $\times 2$.

Table 3.2	Experimental	Simulation
	Rsh (Ω/Sq)	Rsh (Ω/Sq)
-55 ˚C	11989.8	13750
-25˚C	11604.7	11750
25˚C	10837.4	10750
75˚C	10332.2	8400
125˚C	9544.3	7500

The Temperature Coefficient of resistance (α) is given by:

$$\frac{R_{Final} - R_{\mathrm{Re}\,ference}}{R_{\mathrm{Re}\,ference} \times 100} = \alpha\left(T_{Final} - T_{\mathrm{Re}\,ference}\right) \quad (3.31)$$

where R_{Final} is the resistance at the higher temperature (in our case it was resistance at 125ºC) and $R_{\mathrm{Re}\,ference}$ is the resistance at the reference temperature (we chose reference temperature at 25ºC). Simulated and experimental data is tabulated in table 3.2. Looking at the simulated data, at 298K, the sheet resistance is 10750Ω/Sq. At 398K, the sheet resistance is about 7500Ω/Sq. The *TCR* written in percentage increase per degree rise is:

$$\alpha_{Sim} = \left[\frac{7500 - 10750}{107500 \times 100}\right] = -0.003\%/^{\circ}C \quad (3.32)$$

which compares fairly well with the experimental value of:

$$\alpha_{Ex} = \left[\frac{9544.3 - 10837.4}{10837.4 \times 100}\right] = -0.0012\%/^{\circ}C \quad (3.33)$$

The proposed model agrees with experimental results for temperatures above 250K. For temperature below 240K, the model breaks down because the calculation shows that there are more DX centers than free carriers. This is to be expected in part because of carrier freeze out. At this point in time, questions about the true structure

of sputtered grown $In_xAl_{1-x}N$ warrants further investigation. For example, if AlN is grown using low temperature RF sputtering processes, do the properties of the film contain some of the properties of the same material when grown at higher growth temperature processes like MOCVD? Is the material a combination of zinc-blend and wurtzite structures or is it structurally totally different form altogether? If it is a mixture of these two structures, do alloys of a material that exhibits these two structures also show the properties of the two structures? These are important questions because theoretical studies have not been consistent in that different work show different trap levels[12, 15, 62, 63] and some authors report finding to traps at all in zinc-blend AlN [74]. Furthermore, even when traps have been identified, there is significant scatter related to computational methodologies. For instance, several first-principles studies have addressed the issue of whether silicon undergoes DX transition as we have reported. Park and Chadi found the $\alpha - BB$ configuration to be most favorable in AlN [12, 15] and several other researchers have confirmed this finding[62-64] while Van de Walle et al., contradicted this finding [74].

The problem arises from the fact that AlN and InN exists in two configurations; the wurtzite structure and zinc-blend form. There is very limited amount of research comparing the properties of these two structures[76, 93]. Deriving from the available work, AlN has a higher band gap in wurtzite structure than in zinc-blend. A direct consequence of this deviation is that the upper defect state of nitrogen vacancy lies below the conduction band minimum in zinc blend material thereby acting as a donor trap while in wurtzite structure, the defect is said to be above the CBM. This effect

complicates determination of the exact level of traps in the band gap of a polycrystalline form. Further work is necessary to develop more understanding of the composition of structure of wurtzite and zinc-blend forms $In_xAl_{1-x}N$. We propose this as an action item in future work.

Subsection 3.5.3: Conclusion

Although there are many defects that could affect the electrical conductivity, surprisingly very good agreement was found between the experimental data and the model, although only three defects were included in the model. There are other defect interactions that are not included in the model but which may account for the reason why the model does not fit perfectly well at temperatures below 240K. Two or more defects can interact in such a way that alters the electrical transport in the material. Recent studies suggests that complexes such as $V_N - N_{In}$ and $V_N - V_{Al}$ have substantial binding energies and that their formation energies are lower than their respective cation vacancies under metal-rich conditions [94] [95], [96]. The number and type of complexes that can form are plenty and the modeling of their contribution to electrical transport becomes even more complicated when we consider the fact that these defects or ions may have more than one diffusion path. For example, the grain boundary diffusion may be many times faster than lattice diffusion. We have not included the effect of such coupling in the model. The compensation by these defects has the effect of taking more electrons from participating in electrical conduction as well as slowing the charge carriers.

Section 3.6: Resistor Patterning with Chlorine Based Plasma

Subsection 3.6.1: Effect of Chlorine Exposure to the Resistor Film

The need to analyze the effect of chlorine adsorption in the $In_xAl_{1-x}N$ film became necessary because chlorine plasma is one of the few etchants known to etch AlN . In the next chapter, it will be shown that exposure to chlorine reduce the sheet resistance. The chemical reaction of the formation of AlN can be expressed as follows:

$$Al + N \longrightarrow AlN + \Delta H_{AlN} \qquad (3.34)$$

where ΔH is the heat of formation and it is assumed that bonds have been broken for $N - N$ molecules and Al atoms. The chemical reaction for $AlCl_3$ can be expressed as:

$$Al + 3Cl \longrightarrow AlCl_3 + \Delta H_{AlCl_3} \qquad (3.35)$$

In expression (3.34), the heat of formation is -57.7kCal/mole at 25°C [97]. In expression (3.35), the heat of formation is -163.8kCal/mole at 25°C [97]. Another important reaction that is worth consideration is that of $InCl_3$. The chemical reaction for indium and chlorine can be represented as:

$$In + 3Cl \longrightarrow InCl_3 + \Delta H_{InCl_3} \qquad (3.36)$$

where the ΔH_{InCl_3} is the heat of formation which is -128.5kCal/mol at 25°C [97].

Subsection 3.6.2: Preferential Etch of AlN over InN

As a result of the difference in formation energy, attempt to etch $In_xAl_{1-x}N$ film with chlorine based etchant leads to preferential removal of aluminum atoms, creating a porous front in the resistor film that is exposed to the etchant. Selective removal of

aluminum atoms should result in increased electrical conductivity because *DX* trap centers are formed between silicon and nitrogen atoms. These silicon atoms have their next nearest neighbors as aluminum atoms.

Subsection 3.6.3: Conclusion

To account for the anticipated reduction in sheet resistivity, alloy composition can be adjusted upward so that more aluminum is present. This would make sure that after the resistor film is etched, the film would still have the required minimum value for the feedback resistor. Further experimental studies correlating the film thickness and exposure time to chlorine etcher will be necessary, in order to develop a process for various resistor values using different alloy composition. Another alternative to changing alloy composition would be to use a longer resistor.

Chapter 4: Film Growth, Characterization and Analysis

Section 4.1: Material Growth and Electrical Characterization

Subsection 4.1.1: RF magnetron Sputtered Growth

The aluminum-indium alloy film was grown using RF magnetron sputtering system. The material was co-sputtered using three targets for aluminum, indium and silicon. Silicon target provided n-type dopant. The deposition temperature was set at room temperature and the pressure was maintained at 5mTorr. Nitrogen was provided in nitrogen/argon plasma.

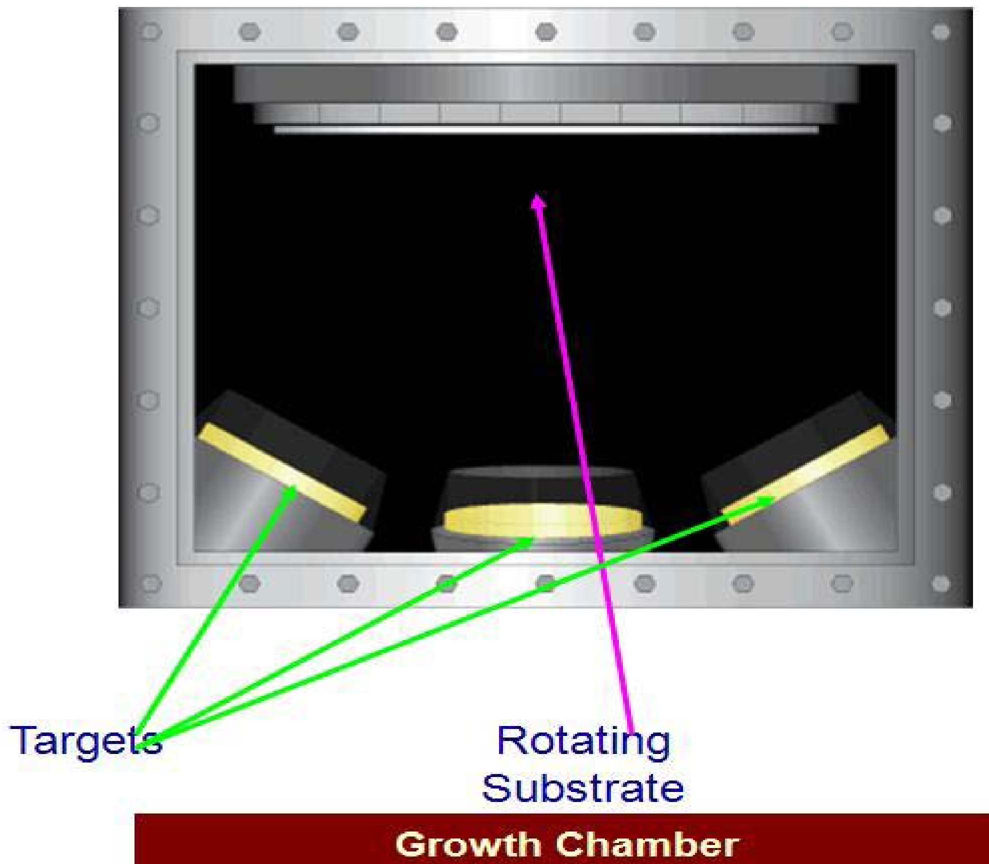


Fig. 4.1: RF Magnetron multi-sputtering tool. Using 3 targets allows control of sputtering rates of Al, In and Si. Nitrogen is provided in N/Ar plasma. Sputter growth was done at 5mTorr during growth

The amount of silicon dopant was roughly held constant throughout the deposition by maintaining the same power at the RF target. Our initial assumption was that we could estimate the film composition as proportional to the power on a given sputtering target. The powers on each sputtering target determine the deposition rate of the material.

Subsection 4.1.2: Electrical Characterization using 4-Point Probe Station

For the initial sets of film growth, the objective was to establish how change in indium-aluminum alloy composition affected the sheet resistance of the film alloy. Results of the experiment are tabulated in table 4.1 below.

Table 4.1

Sample	Metal Comp	Plasma Comp	Sheet Resistance
1	Al80/In20	Ar80/N20	3592kΩ/☐
2	Al60/In40	Ar70/N30	2.8kΩ/☐
3	Al60/In40	Ar60/N40	7.3kΩ/☐
4	Al60/In40	Ar80/N20	32.4kΩ/☐
5	Al20/In80	Ar80/N20	12.7kΩ/☐
6	Al20/In80	Ar70/N30	2.2kΩ/☐

This set of data was for the film before annealing. Samples 1, 4 and 5 were grown under similar plasma composition of 80% argon and 20% nitrogen. For these samples, the aluminum target had the power set so as to yield 80%, 60% and 20% aluminum.

Considering samples 1, 4 and 5, it can be seen that a change of 80% to 60% in percentage aluminum composition of sample 1 and 4 resulted in two orders of magnitude change in sheet resistance, i.e., from 3.6MΩ/☐ to 32kΩ/☐. Further reduction of aluminum composition from 40% to 20% in samples 4 and 5 resulted in

$\times 3$ factor change from 32.4kΩ/□ to 12.3kΩ/□. The amount of nitrogen was then varied while keeping the metal composition constant. It is shown that a change of nitrogen composition from 20% to 30% (in samples 2 and 4) results in an order of magnitude reduction of sheet resistance from 32.4kΩ/□ to 2.8kΩ/□. Similar tread is shown in samples 5 and 6. For this set of samples, the film was grown in 20% nitrogen for sample 5 and 30% nitrogen for sample 6. A factor of six reduction of sheet resistance (i.e., from 12.7kΩ/□ to 2.2kΩ/□.) when nitrogen composition was increased from 20% to 30% is shown. In general, when metal composition was held constant, increase in percentage nitrogen composition resulted in lowered sheet resistance while an increase in percentage aluminum composition with nitrogen composition constant resulted in increase in resistance.

In the next set of data, we investigated the effect of annealing the film resistor. Table 4.2 below shows sheet resistance of the film before and after annealing. The film was annealed for 3 hours at 410°C and allowed to cool down to room temperature for 30 minutes. The film was then annealed again for 3 hours. For this set of samples, there was a reduction of the sheet resistance by a factor of $\times 3$ and a reduction of TCR by a factor of $\times 5$. There was no change observed after the second 3-hour annealing session.

Table 4.2			
Resistor Film Prior to Annealing			
Sample	Alloy %	**Rs (kΩ/□)**	TCR(%/°C
S9-1AG	Al60/In40	30.0 kΩ/□	-0.00529
S9-OBSi	Al/60/In40	32.5 kΩ/□	-0.00599
S9-2BG	Al60/In40	31.5 kΩ/□	-0.00549
Annealed for 3Hrs at 410°C			
	Alloy %	**Rs (kΩ/□)**	TCR(%/°C
S9-1AG	Al60/In40	8.99 kΩ/□	-0.00152
S9-OBSi	Al60/In40	9.00 kΩ/□	-0.00143
S9-2BG	Al60/In40	8.89 kΩ/□	-0.00182

The resistor film was then grown on a six-inch wafer which had 2000Å of PECVD silicon nitride. Similar growth conditions as discussed above were repeated. The results of that part of experiment are reported in table II above. The samples were annealed for 3 hours at 410°C. The samples were left to reach thermal equilibrium for 72 hours and electrical measurements were repeated in room temperature. The results of the experiment are recorded in table the second part of table II above.

We performed a series of deposition runs on 6" wafers provided by Honeywell Aerospace Corporation, Plymouth Minnesota. The objective was to use same wafers used on Honeywell's SOI CMOS process. The wafers were coated with a layer of 2000Å of silicon nitride. The film was grown using the same deposition parameters and all the four wafers were characterized at Honeywell Aerospace, Plymouth MN. The samples coated with silicon nitride grown using PECVD. Following a nitride deposition, the film samples were annealed in forming gas for 3 hours at 410°C and removed from the furnace and allowed to cool to room temperature. After the samples

were allowed to cool for 6 hours, they were put back in the furnace for 2 3-thirty minute runs at 410°C with a 15 minute break in between.

Electrical measurements were taken using a temperature controlled four-point probe. Figure 4.1 shows the sheet resistance measurement at the following temperatures: -55ºC, -25ºC, 25ºC, 75ºC and 125ºC. At -55ºC, the resistance is about 12.4kΩ/☐, at -25ºC, the resistance is about 11.7kΩ/☐, at 25ºC, the value is about 10.8kΩ/☐, at 75ºC, it is about 10.3kΩ/☐ while at 125ºC, the resistance dropped to 9.5kΩ/☐.

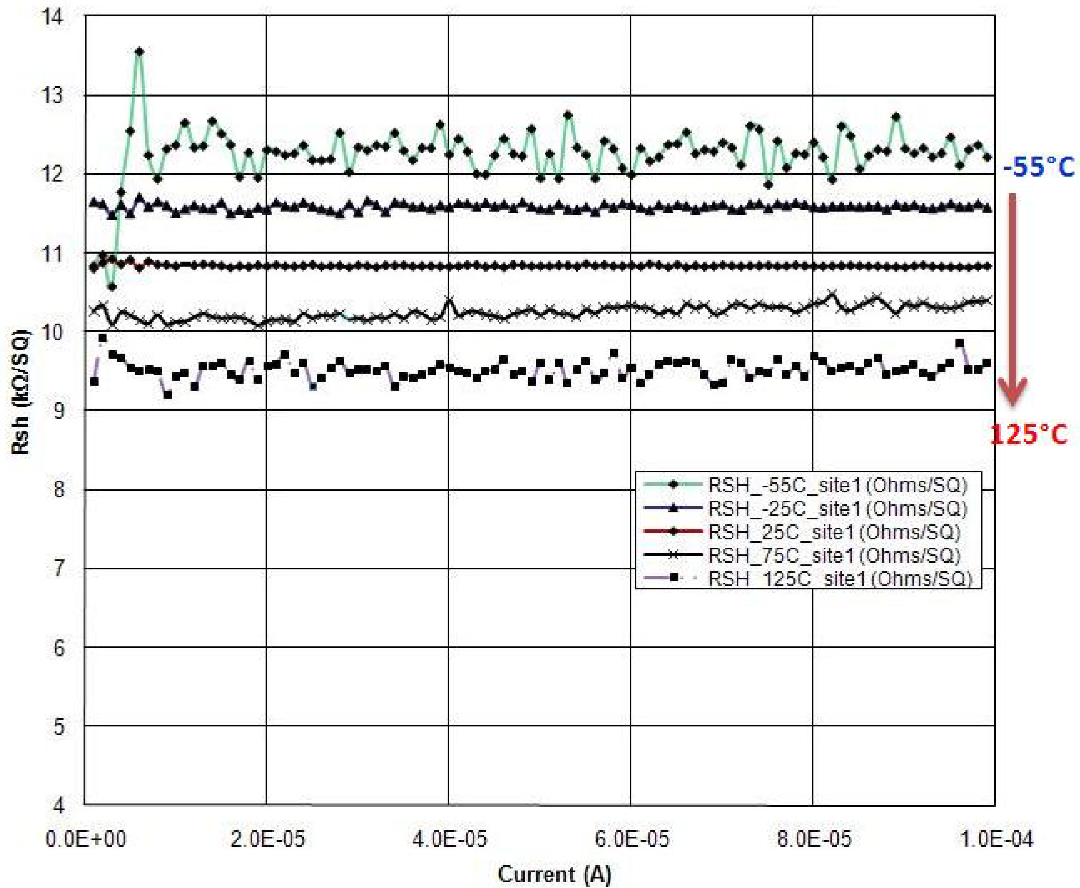


Fig. 4.1: Sheet resistance as a function of current impressed on the sample during the resistance measurement.

Evaluating the temperature coefficient of resistance (TCR) over the temperature range from 25˚C to 125˚C,

$$\alpha_{Ex} = \left[\frac{9544.3 - 10837.4}{10837.4 \times 100} \right] = -0.0016\%/^{\circ}C \qquad (4.1)$$

The TCR is a remarkable milestone for the growth process and integration in CMOS process. It is many orders of magnitude lower than what is realistically achievable using lightly doped polysilicon resistor while the magnitude of the sheet resistance is orders of magnitude higher than what is typically achievable using lightly doped polysilicon resistor.

Subsection 4.1.3: Material Chemical Characterization

The goal of this experimental analysis was to determine the depth profile of indium, aluminum and nitrogen containing samples on silicon. The XPS data was qualified using sensitivity factors and a model that assumed a homogeneous layer. The analysis volume is the product of the analysis area (spot size) and the depth. The photoelectrons are generated within the X-ray penetration depth, but only photoelectrons within the top three photoelectrons escape depths are detected. Typically, 95% of the signal originates from this depth. Table 4.3 provides the atomic concentrations of elements detected while table 4.4 shows the relative distribution. The detection limit was about 0.5 to 1.0%. Factors that affect detection limit are: 1). the weight of the elements, where the heavier elements generally have lower detection limits, 2). Interference, which can include photoelectron peaks and Auger electron peaks from other elements and 3). the background electrons, which is typically due to signals from electrons that have lost energy to the matrix. The depth

The depth profile suggested film consistent with $In_xAl_{1-x}N_yO_{1-y}$ where for sample 10A, x=0.76 and y=0.15. Oxygen content was rather high even though it was not intentionally supplied. We later found that the gas lining was improperly connected and that what we had believed to be pure nitrogen was in fact densely condensed air. The presence of oxygen is however not problematic because like silicon, it is shallow donor, but equally able to transition to deep level trap. The analysis of its role in $In_xAl_{1-x}N$ follows exactly like that of silicon, the only difference being the trap level being at 0.570eV[98] compared to silicon's 0.32eV[64] below the donor substitutional level.

Table 4.3: Chemical analysis of indium aluminum oxynitride based on XPS data

SAMPLE 10A						Sample 10C					
Depth (Å)	N%	O%	Al%	Si%	In%	Depth (Å)	N%	O%	Al%	Si%	In%
0	12.2	45.1	4.1	0	38.7	0	16.9	46.1	4.1	0.4	32.5
25	8.6	40.5	9.1	1.3	40.5	25	8.5	39.2	13.9	0	38.5
50	8	42.3	11.3	0.3	38.1	50	8.9	42.3	14.3	0.4	34.2
75	7.9	43.1	11.7	0	37.3	75	7.3	43.2	16.1	0	33.4
100	7	42.8	12	1.7	36.6	100	8.5	43.1	15.9	0.3	32.2
125	8.4	42.6	11.8	0.7	36.6	125	8.5	42.8	16.2	0	32.6
150	7.2	43.6	11.7	0.7	36.8	150	7.4	42.8	16.7	1.2	31.9
175	7.4	42.8	12.4	1.3	36.1	175	8.2	42.4	17.5	0.1	31.8
200	8.2	43	11.8	0.7	36.4	200	8.9	41	19.1	0.6	30.5
225	7	44	11.5	0.4	37.1	225	9	40.5	19.5	0.7	30.4
250	7.8	43.2	11.5	0	37.6	250	8.3	41	20.9	0.3	29.5
275	7.8	43	10.8	0.3	38.2	275	8.5	40.1	21.7	0.2	29.4
300	7.6	40.1	11.8	1.1	39.4	300	9.8	38.1	23.4	0.8	27.9
325	7	41.3	13.5	7	31.2	325	10.3	43.8	20.2	16.7	9.1

[a] Normalized to 100% of the elements detected. XPS does not detect H or He. This data was obtained from analysis performed by Evans Analytical Group, New Jersey

Table 4.4: Average Concentrations (in %)[a] and Ratio

Sample	From 50-300Å	N	O	Al	In
10A	Average (Std. Dev.)	7.6 (0.5)	42.8 (1.0)	11.6 (0.4)	37.3 (1.0)
10C	Average (Std. Dev.)	8.5 (0.7)	41.6 (1.6)	18.3 (2.8)	31.2 (1.9)
10A	Ratio	2.0	11.2	3.0	9.8
10C	Ratio	2.0	9.8	4.3	7.4

[a]Does not include silicon concentration which was less than one atom% over these depths.

Figure 4.2 of below shows the profile spectra of sample 10A. We find that the film chemical composition is fairly uniform up to an approximate depth of 350Å. The depth profile result indicates that RF magnetron sputtering is a viable option for growing the film resistor.

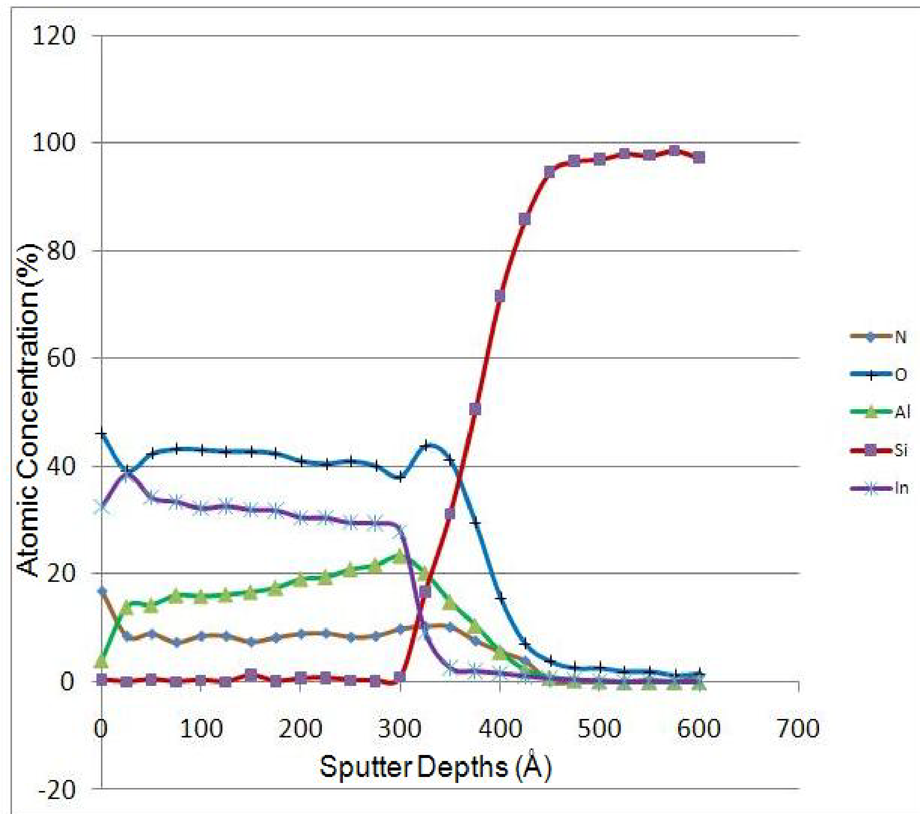


Fig. 4.2: Profile spectra of sample 10A. This was generated using data of table 4.3

Figure 4.3 below shows the survey spectra of chemical elements in the film. The only element that was not expected is oxygen. Oxygen was incorporated as a nitrogen impurity. The enthalpy of formation of In_2O_3 is -221.2kcal mol^{-1}. Compared to the enthalpy of formation of InN at -34 kcal mol^{-1}, oxygen is preferentially incorporated in the film. Furthermore, as mentioned earlier, Oxygen is an n-type dopant whose formation energy of incorporation into the $In-N$ lattice is very low.

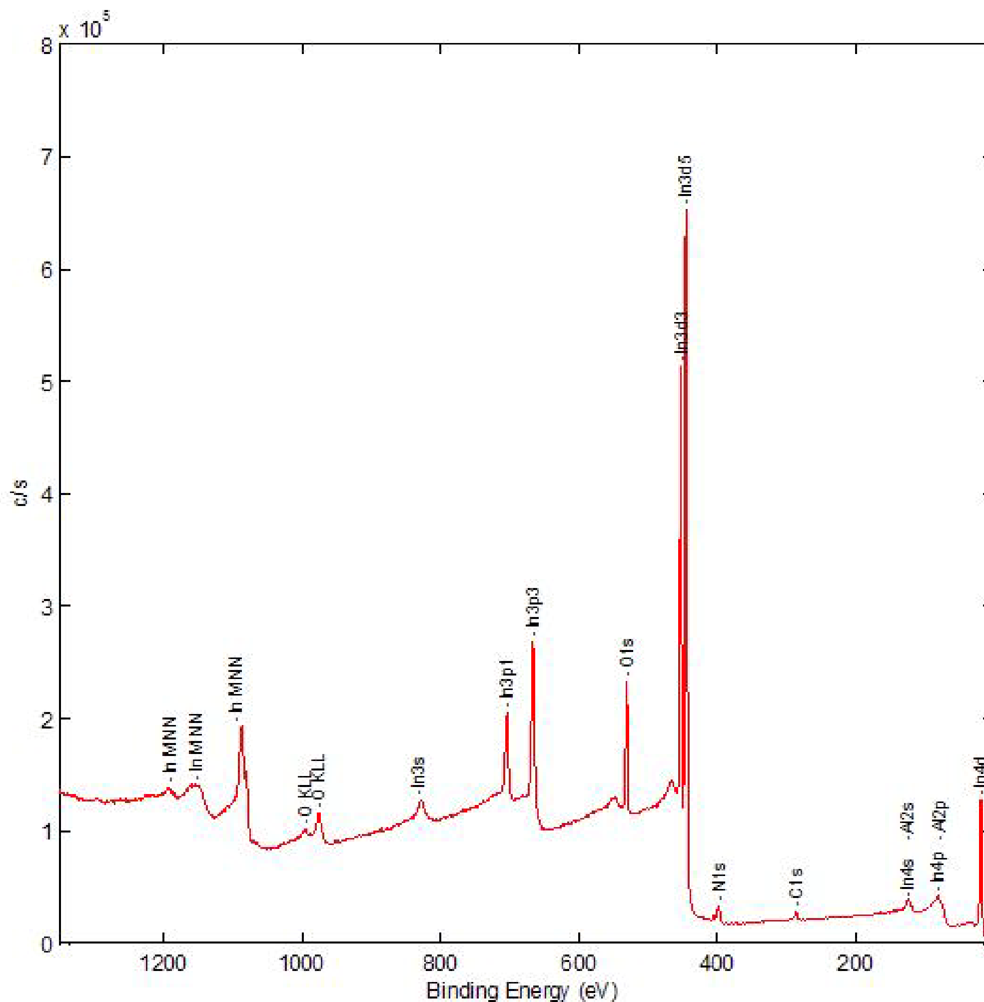


Fig. 4.3: Survey spectra various elements found in the resistor film. Analysis done at Evans Analytical Group, New Jersey

Section 4.2: Choice of Annealing Environment

Subsection 4.2.1: Annealing in Forming Gas

The discovery of a resistor film with the requisite sheet resistance and low TCR is ideal for use in deeply scaled CMOS technology SRAM cells is a major milestone. We have also established that developing a realistic integration process in the CMOS process is just as important as the discovery of the film. To address the issue of film integration in the CMOS process, we performed a series of annealing experiments to establish the favorable condition for integration. In the first instance, electrical characterization of three wafers was done and then the samples were annealed the film in forming gas. The sheet resistance for the samples before annealing is shown in table 4.5 below . The film samples were annealed in three distinct environments: the argon ambient, the nitrogen ambient and in the forming gas (H_2+N_2 ambient) with the aim of establishing a preferred annealing environment for CMOS processing. Table 4.5 below tabulates the result of the experiment.

Table 4.5: Sheet Resistance (Ω/Sq)Prior to Annealing

0BSi25	25˚C	21959.02172
1BG25	25˚C	208280.2972
2BG25	25˚C	25726.96108

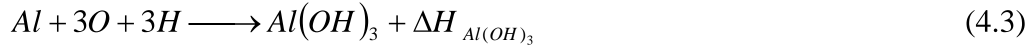
The film was annealed in forming gas (hydrogen and Nitrogen) for two 3-hour sessions at 410°C with a break of two hours between the annealing sessions. After 72 hours, electrical characterization of the samples was done using a temperature controlled 4-point probe station. Temperature range for which the devices were heated or cooled were from -55°C to 125°C. The three sampled had the sheet resistivity increase beyond the detection limit (10^{13} Ω/Sq) of the 4-point probe. The

rise in sheet resistance is attributable to hydrogen-enhanced oxidation of aluminum, leading to formation of highly resistive $Al-(OH)_3$. In the presence of hydrogen, oxygen forms an insulating aluminum oxide that exists in $Al-O$ and $Al-OH$ bonding configurations. The following chemical reactions are believed to lead to the formation of $Al(OH)_3$. Considering the formation of AlN, the reaction proceeds as:

$$Al + N \longrightarrow AlN + \Delta H_{AlN} \tag{4.2}$$

where $\Delta H_{AlN} = -57.7kCal/mol$ at 25°C.

The formation of $Al(OH)_3$ would proceed as:



$$Al + 3O + 3H \longrightarrow Al(OH)_3 + \Delta H_{Al(OH)_3} \tag{4.3}$$

where $\Delta H_{Al(OH)_3} = -304.8kCal/mol$ at 25°C.

Another equation that we need to look at is that of formation of NH_3. Formation of NH_3 should proceed as follows:

$$N + 3H \longrightarrow NH_3 + \Delta H_{NH_3} \tag{4.4}$$

where $\Delta H_{NH_3} = -10.96kCal/mol$ at 25°C.

It is intuitive that in presence of oxygen and hydrogen, AlN will form $Al(OH)_3$ according to the following equation:

$$AlN + 3O + 6H \longrightarrow Al(OH)_3 + NH_3 \tag{4.5}$$

where it is assumed that energy to break $Al-N$ is provided.

The reaction is exothermic with energy balance of -315.76kCal/mol. Such oxidation phenomenon was previously observed in aluminum gallium arsenide [10, 11].

Subsection 4.2.2: Silicon Nitride Necessary to Encapsulate the Film

In order to avoid hydrogen-enhanced oxidation, we encapsulated the film in silicon nitride using Plasma Enhanced Chemical Vapor Deposition (PECVD) growth process. Silicon nitride is an ideal choice for film encapsulation because it is commonly used in CMOS process and its use does not introduce additional constraints in device processing. It is well matched with silicon oxide and it is an effective barrier to most elements including hydrogen. Its growth process is described as:

$$3SiH_4(gas) + 4NH_3(gas) \longrightarrow Si_3N_4(solid) + 12H_2(gas) \quad (4.6)$$

Although hydrogen is released as a reaction by product, the formation of initial layer of the silicon nitride film is sufficient to create sufficient barrier against further hydrogen gas released. For the purpose of protecting the resistor film, we found a 2000Å thick layer of Si_3N_4 to be sufficient.

Subsection 4.2.3: Conclusion

The film had unexpectedly high amount of oxygen although oxygen had not been deliberately included. The high amount of oxygen was not found to affect the electrical properties adversely. Oxygen occupies nitrogen sites and is surrounded by aluminum vacancies rather than coordinated to aluminum atoms. In this configuration, presence causes net gain of electrons available for electrical conduction since the aluminum vacancies are held away from n-type silicon donor.

Furthermore, in presence of indium, oxygen forms In_2O_3 which itself is a semiconductor whose fundamental energy band gap is 3.78eV. Exposure of the film resistor to forming gas in elevated temperature causes a chemical reaction whose end products are $Al(OH)_3$ and NH_3 creating material that is insulating. The high temperature anneals out the aluminum vacancies and highly reactive and diffusive hydrogen reacts with oxygen and aluminum. To mitigate this effect, a layer of silicon nitride was grown to encapsulate the film. A thin layer of PECVD grown silicon nitride was found to be an effective in maintaining the integrity of resistor. In absence of hydrogen, oxygen is found to be benign and actually is an effective donor.

Section 4.3: Resistor Etched by Chlorine/Argon Plasma

Subsection 4.3.1: Choice of Electron Resonance Plasma Etcher

Aluminum-nitrogen bonds are very strong with bond strength of 11.52eV. Consequently, conventional dry etch methods such as RIE are not very useful in etching AlN . We had limited success in our attempt to etch $In\ Al_{1-x}N$ resistor film. We etched the $In_xAl_{1-x}N$ film using Electron Cyclotron Resonance (ECR) plasma etcher. The etching chemistry was Cl_2/Ar plasma. In addition to having higher plasma densities, ECR employs lower operating pressures and DC biases that are controlled separately independent of the plasma source. The result is higher etching rates, vertical sidewalls and lower etching induced damage. The mechanism that limits the etch rate under RIE conditions is the initial breaking of the bonds that precedes etch product formation. At the higher ion fluxes available in the ECR

discharges, the rate of etch product formation is much faster, and efficient sputter-enhanced desorption of these products leads to high etch rates.

Subsection 4.3.2: Resistor Delineation

The van der pauw method was used to form structures on a 6-inch wafer where the film had been deposited. The objective of this part of experiment was twofold: 1). To develop an appropriate film delineation method and 2). Understand what effects the delineation processes has on the resistor film. In this part of experiment Cl_2/Ar plasma was used to etch the film after the van der pauw patterns were formed by optical lithography. The same plasma also etches Si_3N_4 encapsulating layer.

Subsection 4.3.3: Conclusion

The Cl_2/Ar plasma was found to be an effective etcher of $In_xAl_{1-x}N$ film. However, it was found that there was a reduction in sheet resistivity by roughly a factor of two. The reduction of sheet resistivity will need to be accounted, 1) during the design phase so that more squares can be used or, 2) during the resistor growth phase so that alloy composition can be adjusted by increasing the aluminum composition to account for preferential etching of aluminum.

Section 4.4: Factors Affecting Sheet Resistance

Subsection 4.4.1: Effect of Annealing On Sheet Resistance

Following encapsulation of the film and annealing, sheet resistance was measured at about one-third of the pre-annealed level. Figure 4.4 below shows sheet rho

measurements for one of the wafers over the temperature range of -55°C to 125°C. The sheet resistance reduction phenomenon was observed in all the six wafers. We attributed the drop in sheet resistance to formation of donor defects in the InN sub-lattice. Nitrogen defects (V_N) are a likely candidate since they have the lowest formation energy.

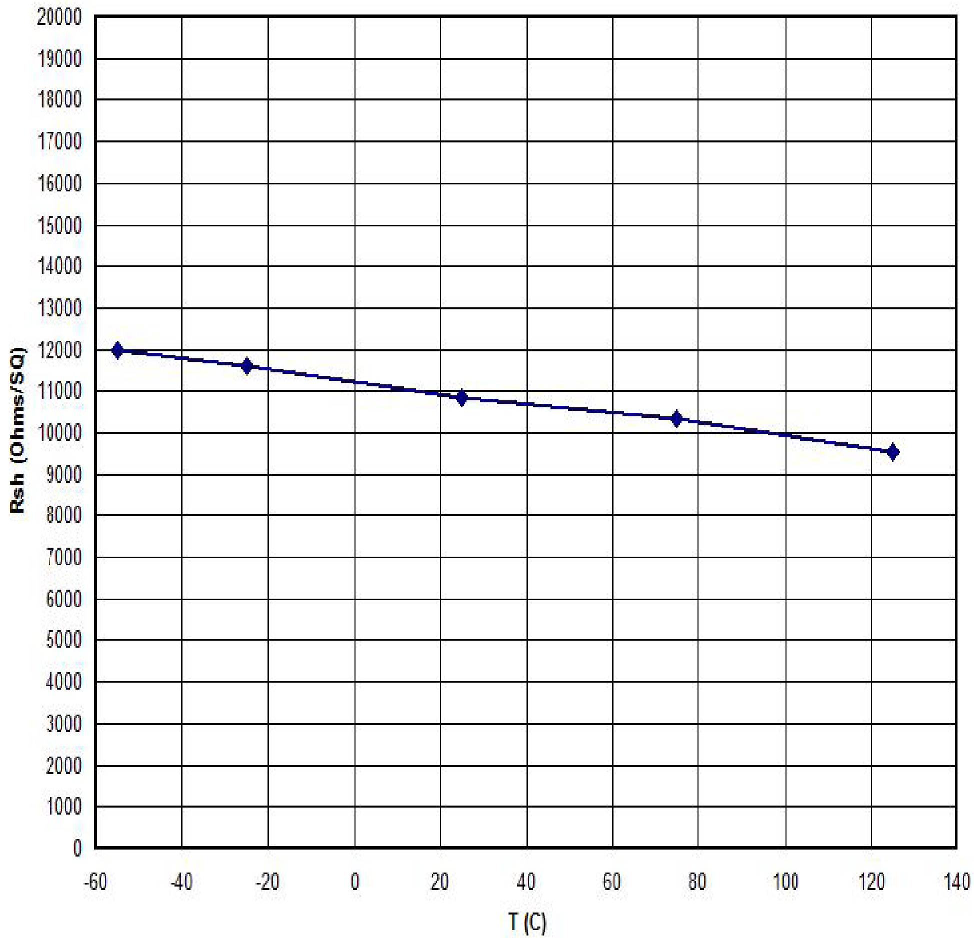


Fig. 4.4: Sheet resistance measurement for film resister following 3-hour anneal at 410°C without Chlorine plasma etching. At T=25°C, R=10800Ω/Sq; at T=125°C, R=9600Ω/Sq. The TCR =0.00111%/°C

The nitrogen defect induces defect states in the conduction band, and prefers to form "vacancy clusters" giving rise to locally In-rich regions [80, 99]. While the formation of this defect was reported high for intrinsic InN [100], it is worth noting that the

fundamental band gap of InN is only 0.7 eV while the band gap of $In_xAl_{1-x}N$ for x=0.6 is 3.2 eV. Another possibility is the formation of oxygen-indium vacancy $(O_N - V_{In})$ complex. It has been established that indeed O_N^+ and V_{In}^- prefer forming on neighboring sites forming a $(O_N^\bullet - V_{In}^{'})^x$ complex [88]. The result is that an acceptor $V_{In}^{'}$ would release the electron and pair up with a donor oxygen impurity.

Subsection 4.4.2: Chlorine's High Negative Electron Affinity

As stated above, Cl_2 / Ar plasma was used for resistor pattern definition. We observed a further reduction of sheet resistance by almost a factor of $\times 2$. We show the results of the effect in figure 4.5 below, sheet resistance measurement taken on the same wafer as the one shown in figure 4.4 above.

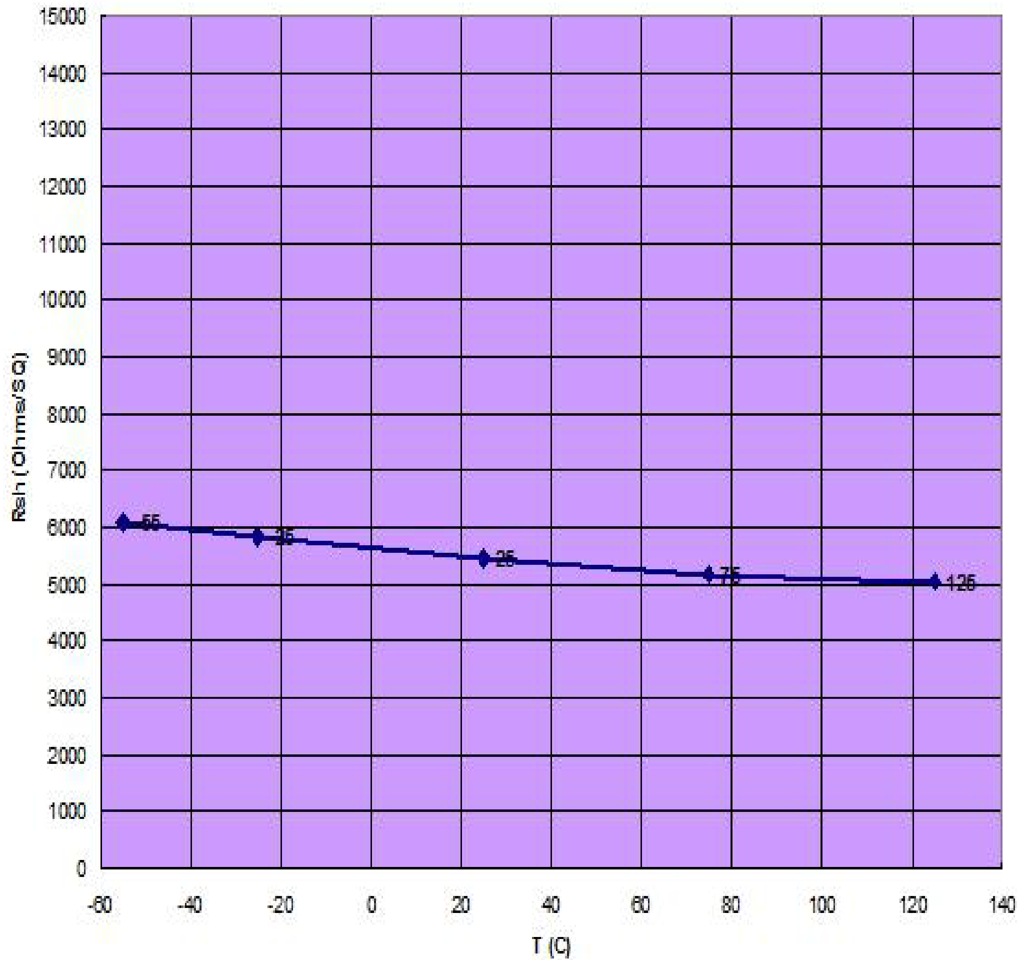


Fig. 4.5: Sheet resistivity was measured using Van der Pauw structures. A certain reduction of sheet rho was observed, by a factor of ×2 compared to the resistor film with not chlorine etching. At T=25°C, R=5500Ω/Sq; at T=125°C, R=5100Ω/Sq. TCR= -0.0007%/°C.

The sheet resistance was found to decrease by roughly by a factor of $\times 2$. The observation was not unexpected for two reasons: 1), the etch rate of AlN is expected to be much faster than that of InN because of higher electron affinity of chlorine from Al atom as compared to In atom, leading to Cl_2 preferentially congregating around the Al atoms. 2), the lower volatility of $InCl_3$ as compared to $AlCl_3$ leads to less formation of $InCl_3$ leaving the resistor film to have much higher concentration of InN which is not affected by DX^- seen in AlN.

Subsection 4.4.3: Conclusion

The $In_xAl_{1-x}N$ film resistor has been grown and characterized. The RF magnetron sputtering growth process is ideally suited for low temperature growth process requirements imposed by CMOS processing. The magnitude of the resistor can be completely determined by film alloy composition and the doping level. For x=0.6, resistor film was grown with sheet resistance of 10kΩ/sq -12kΩ/sq. For MIT Lincoln Laboratory 180 nm process needing 50kΩ/sq to 75kΩ/sq, just about 5 squares of this resistor film would be needed. However, even fewer squares can be used by varying the alloy composition. From design perspective, the reduction of sheet resistance observed during film delineation is not a problem because this variation can be accounted for by starting with an alloy with higher aluminum composition. It is however, a consideration that needs to be borne in mind during processing.

Chapter 5: Alternatives Materials to $In_xAl_{1-x}N$ Resistors

Section 5.1: Diffused and Implanted Polysilicon Resistor

Subsection 5.1.1: Diffused Polysilicon Resistor

To appreciate the choice of $In_xAl_{1-x}N$ thin film for cross-coupled latch resistors, I will briefly review the properties of polysilicon and diffused resistors as well as their growth conditions in an effort to establish what choices exist for deeply scaled submicron CMOS technologies. Typical value of sheet resistance for n^+ polysilicon is 311Ω/Sq and 330Ω/Sq for p^+. Diffused resistor is even worse, with only 60Ω/Sq for n^+ and 135Ω/Sq for p^+ doping [101-103]. Other authors have reported slightly higher values[104], [105], but there is no report of tens of kilo-Ohm resistors that we have demonstrated using $In_xAl_{1-x}N$ thin film resistor.

The polysilicon resistor films are made up grains with sizes ranging from 50 to 300nm. The diffusion of the dopants within the grains is comparable to that of single-crystal silicon but, the dopant atoms diffuse much more rapidly along grain boundaries and then diffuse into the grains. Because the grains are typically small, much shorter time is necessary for the dopant which is entering from all sides of the grain to fully diffuse into the grain. Consequently, the overall diffusion is controlled by the grain boundaries, the grain structure and the preferred orientation of the film. It follows that these quantities depend upon such deposition conditions as the films

temperature, deposition rate, film's thickness and post deposition annealing conditions. It has been found that phosphorous or arsenic can precipitate at the grain boundaries, resulting in reversible changes of resistivity upon annealing. Thus, the final resistivity of the film eventually depends not just on the doping level in the grains, but also upon the grain size, any precipitates at the grain boundaries and the presence of other defects that can reduce the mobility of the carriers.

The diffused resistors are typically grown using shallow trench isolation (STI) processes. Silicon film is deposited using low pressure chemical vapor deposition (LPCVD) at about 550°C. Once poly gates are formed, the n+ and p+ source/drain regions are formed by ion implantation. A source/drain RTA follows to activate dopants, typically at temperature around 1000°C. Following the anneal, a protective layer is formed to prevent keep the resistor layer dopant from out diffusing during the further process steps.

Subsection 5.1.2: Implantation Polysilicon Resistors

To grow a polysilicon film resistor, typically a polysilicon film is deposited by low pressure chemical vapor deposition (LPCVD) at about 625°C. To control the implant depth and avoid the loss of impurities during anneal steps, the polysilicon film is covered with LPCVD oxide (TEOS) prior to implantation and anneal. The dopant is then implanted, with the profile of dopant implantation dose depending on the implantation energy. Following implantation, the samples are annealed using the Conventional Furnace Anneal (CFA) or the Rapid Thermal Anneal (RTA).

The requirement of such resistors in linear circuits is very stringent. Of critical importance is the control of the nominal film resistance and its thermal stability with respect to changes in process and anneal conditions. Polysilicon resistors have typically shown thermal instabilities that are influenced by grain size and properties of grain boundaries in material. The effect of furnace anneal cycles on resistivity of phosphorous, arsenic and boron doped polysilicon films has been reported [106, 107]. By successively annealing the same samples, the resistivity was found to increase and decrease repeatedly for arsenic and phosphorous doped samples. Further work has also been reported by Suarez et al. The tables 5.1 and 5.2 below shows the effect of annealing in, I) CFA at 900°C for 20 minutes, II) Same as I but followed by 770°C for 90 minutes + 700°C for 40 minutes, III) same as II but followed by 550°C for 60 minutes, and IV) same as III but followed by RTA at 1000°C for 5 seconds. The films were 100-nm thick and had doping concentration of 8×10^{15} cm^{-3}. Table 5.1 shows resistor film doped with arsenic while table 5.2's sample were doped with phosphorous for similar a doping level.

Table 5.1[108]

Thermal Stability of Poly Resistors (Ω/Sq)

Temp.	Anneal Condition			
(°C)	I	II	III	IV
25	325	370	450	160
50	325	369	444	155
75	290	328	371	145
100	287	315	350	142
125	284	308	340	140
150	281	315	345	140

Table 5.2[108]				
Thermal Stability of Poly Resistors (Ω/Sq)				
Temp.	Anneal Condition			
(°C)	I	II	III	IV
25	151	165	181	94
50	155	165	175	94
75	155	165	182	96
100	155	165	180	98
125	156	166	181	98
150	157	169	182	99

In figure 5.1 below, the data shows the behavior of the resistor films after a lower temperature CFA follows a 5 second RTA. The resistance increases as the CFA is reduced to 550°C.

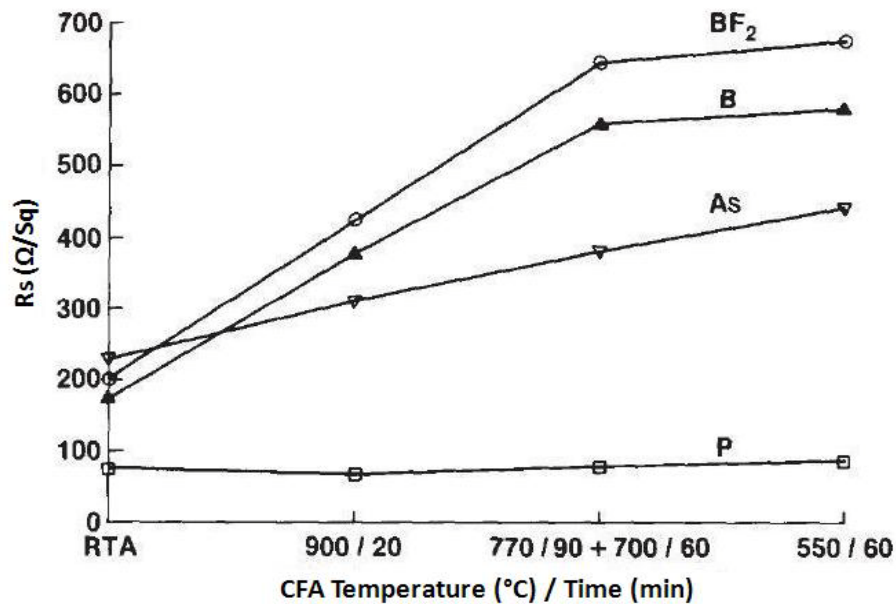


Fig. 5.1: Increase in film resistance when RTA is followed by CFA at decreasing temperature. A final 550°C anneal causes a significant increase in sheet rho[108].

In figure 5.2 below, it is shown that the resistance decreases dramatically when an RTA at 1000°C follows the thermal cycle sequence.

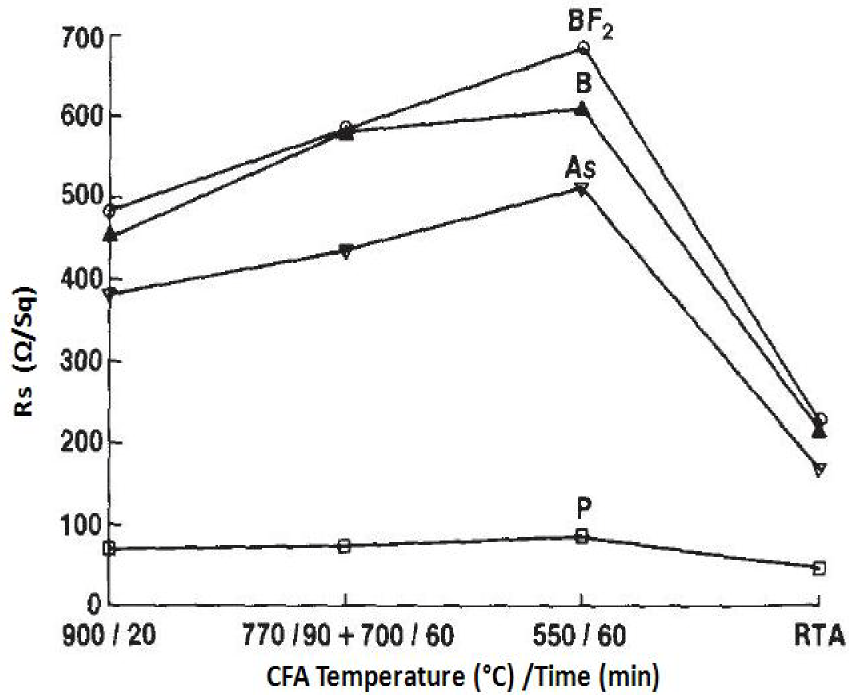


Fig. 5.2: Initial increase in film resistance as the CFA temperature is reduced from 900°C to 550°C. Rapid decrease after RTA [108].

The authors reported that changes shown in both figures 5.1 and 5.2 were reversible indicating serious thermal instability. Effort has been made to stabilize these lightly doped polysilicon resistors that has produced limited success.

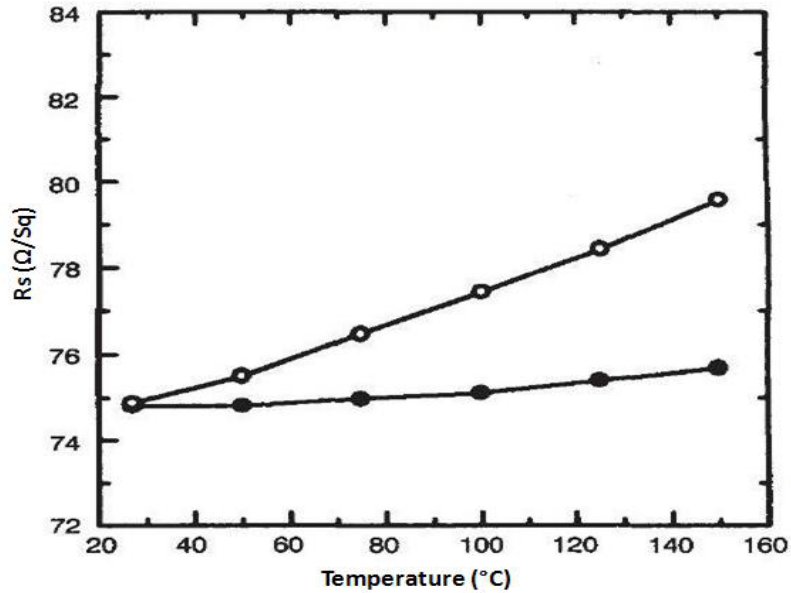


Fig. 5.3: Sheet resistance variations against temperature for phosphorous-only doped phosphorous-arsenic co-doped polysilicon resistor [109].

Figure 5-3 shows how co-doping has been applied in stabilizing the polysilicon resistor against temperature[109]. For this film, the doping level was 4×10^{15}cm^{-2}. The graph shown with open circles is that of resistor film that phosphorous-only doped while the graph shown in solid circles is for phosphorous-arsenic doped polysilicon. While limited success was achieved in achieving lower TCR, in the overall, we that for this resistor, the sheet resistance is only in tens of ohm/sq.

Subsection 5.1.3: Effect of Varying Implantation Depth

Other efforts such as use of co-implantation while adjusting the doping profile and adjusting the depth of implantation have been reported [105]. Use of co-implantation aims at creating enough vacancies and interstitials to covert ordered crystalline into disordered material at a controlled depth. Grains re-growth occurs in subsequent annealing steps[110]. Grain re-growth affects the sheet resistance and the TCR by changing the polysilicon average grain size and the number of grain boundaries per

unit length. Figure 5.4 and figure 5.5 below shows the effect of co-implantation of argon, xenon or fluorine in a boron implanted polysilicon resistor film. There four regimes represented in the figures; 1) without co-implantation, 2) low co-implantation dose but far below the amorphization level, 3) high dose and far above amorphization level with low implantation energy to create shallow amorphous layer of about one-half the polysilicon depth (~750Å), and 4) high dose, far above amorphization level dose level with high implantation energy to create deep amorphous layer at approximately 1350Å.

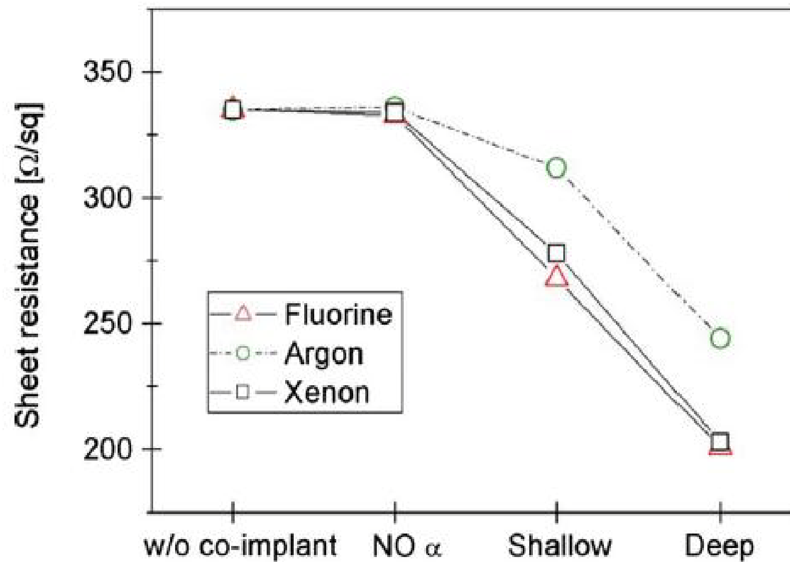


Fig. 5.4: The graph shows sheet resistance of heavily doped polysilicon. As shown on the right side of the figure, deeper amorphous co-implantation decreases the sheet resistance [105].

Even with all these efforts, using polysilicon resistor film would require use of large area of a die to make a latch resist of magnitude in the range of tens of kilo ohms.

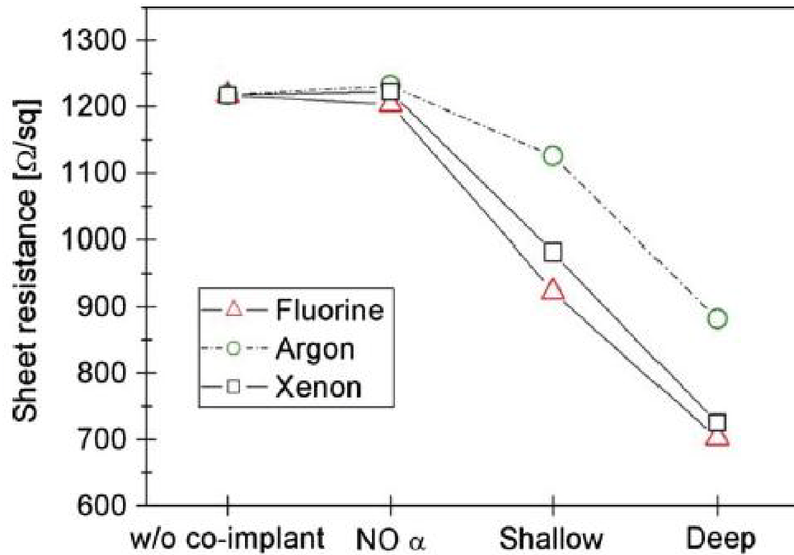


Fig. 5.5: The Graphs show sheet resistance of lightly doped polysilicon resistor. Deep level implantation degrades the sheet resistance [105].

Other than the fact that use of such die space is not compatible with high density requirements that come with deeply scaled CMOS technologies, there are serious processing issues that would limit use of these polysilicon resistors as well. Next we look at CMOS processes and look at the limitations for using the polysilicon resistors.

Section 5.2: Factors Dictating Choice of Feedback Resistors

Subsection 5.2.1: CMOS Thermal Budget

To be able to appreciate the material and the growth process that has been suggested in mitigating deeply scale submicron CMOS technology SRAM cells against single event upsets, we must understand the processing temperature constrains in CMOS processing. In this section, we review some of the more temperature sensitive CMOS fabrication steps, up until the level the integration of the film has been recommended.

The review assumes that shallow trench isolation (STI) has been done, followed by p-well and n-well implantation and drive in. It is further assumed that thermal oxide growth by rapid thermal processing furnace is done followed by gate polysilicon deposition (done using LPCVD) and gate definition using RIE.

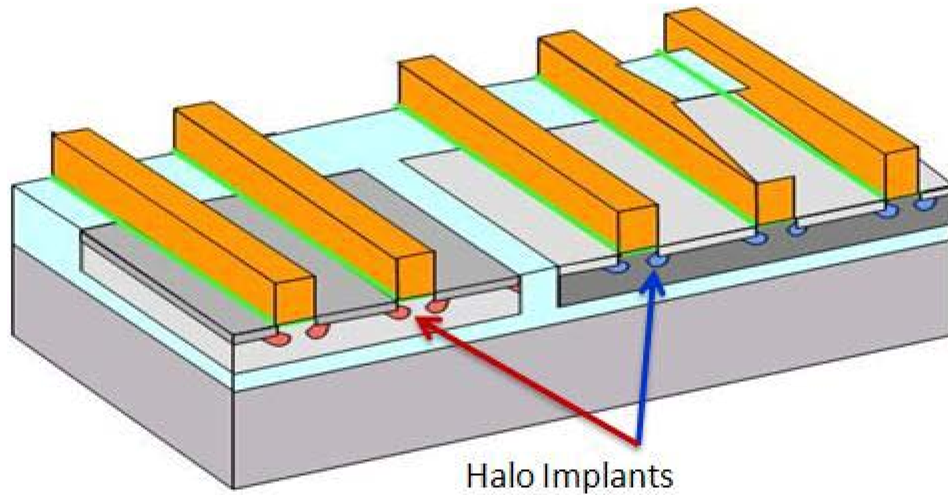


Fig. 5.6: Halo implants done at about 30 degrees to control Short Channel Effects (SCE).

Figure 5.6 show the next step of the processes that involves halo implants, usually done by implanting arsenic. This step is done at an implant angle of about 30 degrees and the wafer is rotated in all directions. The aim for this step is to control short channel effects (SCE) that would otherwise cause unacceptably high leakage currents even when the voltage is off. This step can be done prior to source-drain extension shown in figure 5.8.

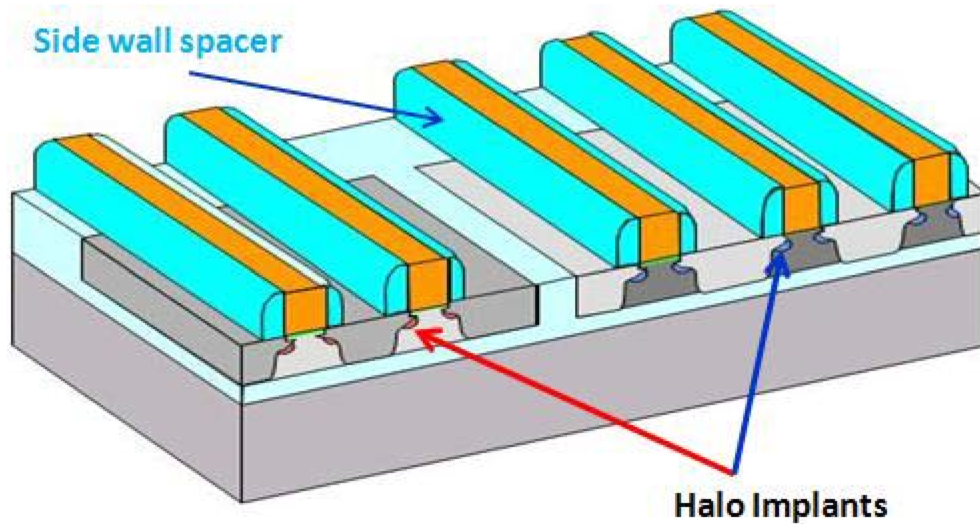


Fig. 5.7: Halo implants following RTA. The anneal process must be done by RTA to limit diffusion of halo implants. Sidewall spacer is silicon nitride deposited using LPCVD

Figure 5.7 shows how the halo implants looks after RTA processes. It is noted here that the process used is RTA but not conventional furnace. RTA must be used to keep diffusion of the implants from spreading too far under the gate. Figure 5.7 also shows sidewall spacers deposited using LPCVD nitride. In figure 5.8, source-drain implant is shown.

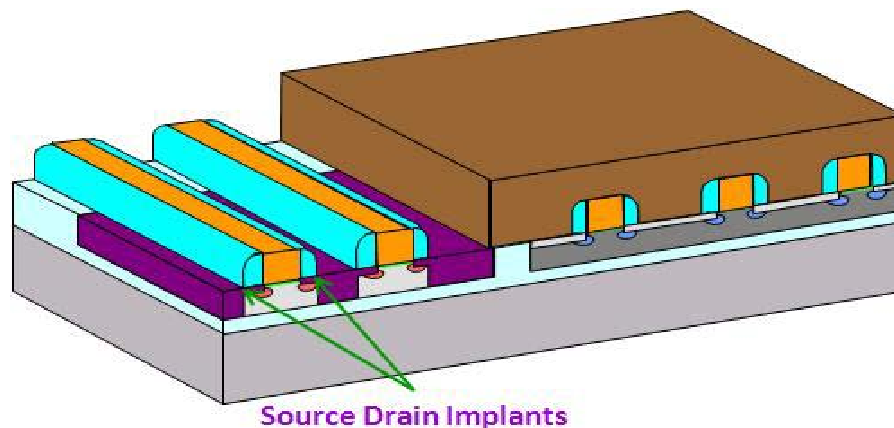


Fig. 5.8 Source-Drain implants used to reduce source-drain resistance. The gate is also exposed so that after implantation the gate becomes p^+ or n^+.

In this step, the implant is either p^+ or n^+ and is done to keep resistance low. This implantation is deeper than the original shallow implant and terminates at buried

oxide (BOX) after the anneal process. The gate is also exposed to the p^+ or n^+ so that it becomes p^+ or n^+ after the implant step.

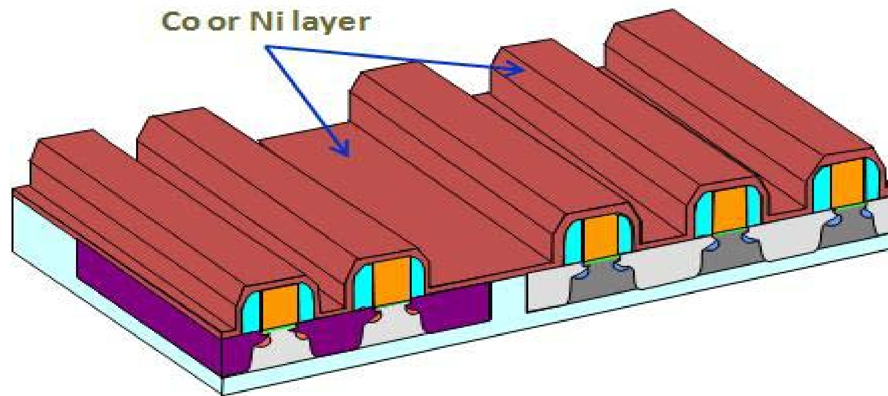


Fig. 5.9: Co or Ni deposited over gate oxide.

Cobalt or nickel is deposited to reduce gate contact resistance. The metal is annealed using RTA. For Co, the anneal temperature is 700°C while nickel must anneal at lower temperature. If nickel is used, all following processing steps must be done at less than 450°C because higher temperature increases resistance nickel silicide. In figure 5.10, silicon nitride barrier is deposited. Silicon nitride is an effective barrier of almost any diffusant and is used to keep some of the most harmful contaminants like Na from diffusing into the active device area.

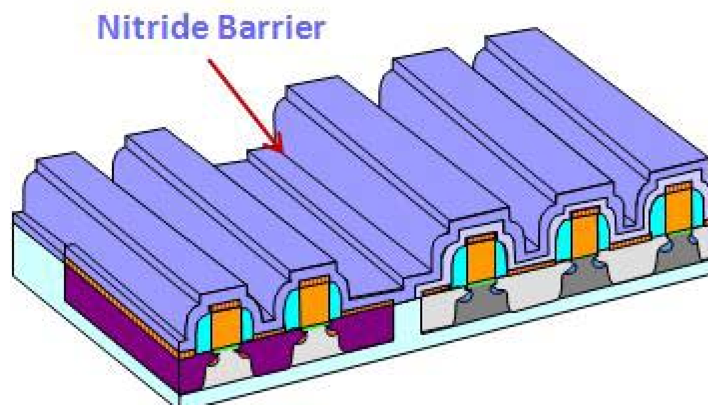


Fig. 5.10: Nitride barrier keeps area with active devices free of contaminants such as Na.

Following successful deposition of the nitride barrier, SiO_2 shown in figure 5.11 is then deposited using low pressure process commonly referred to as Sub-Atmospheric Chemical Vapor Deposition (SACVD) at temperature not above 450°C.

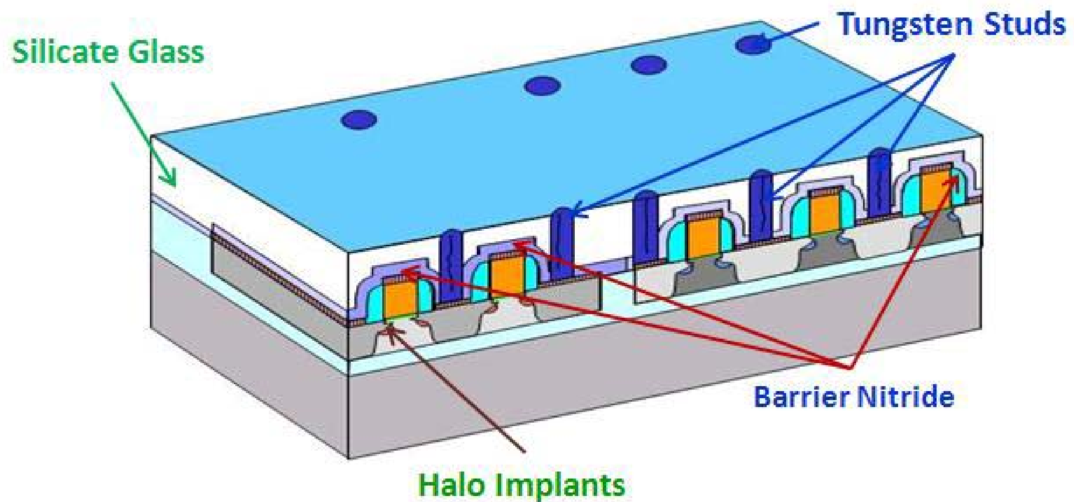


Fig. 5.11: Once holes are opened, TiN liner is deposited using CVD, followed by deposition of Tungsten also using VCD. From this step on, one refers to back end of the line. Further processing must avoid temperatures above 450°C.

It is at this stage that vias are opened and tungsten is deposited using WF_6 as gas which when reduced forms tungsten studs. These studs make contact to source, drain as well as to the gate. Processing steps after this step are referred to be back end of line (BEOL).

Subsection 5.2.2: $In_xAl_{1-x}N$ Resister Film Implementation

The implementation of the film resistor is must be done in away the preserves the integrity of the CMOS process. Specifically, the doping profiles for the halo implants and source/drain extension must maintain design specifications. The resistor film is patterned on silicon nitride layer deposited on top of silicon oxide, and another layer of silicon nitride is deposited to separate the film from the next layer of silicon oxide. This step is expected to limit the extent of hydrogen enhanced oxidation.

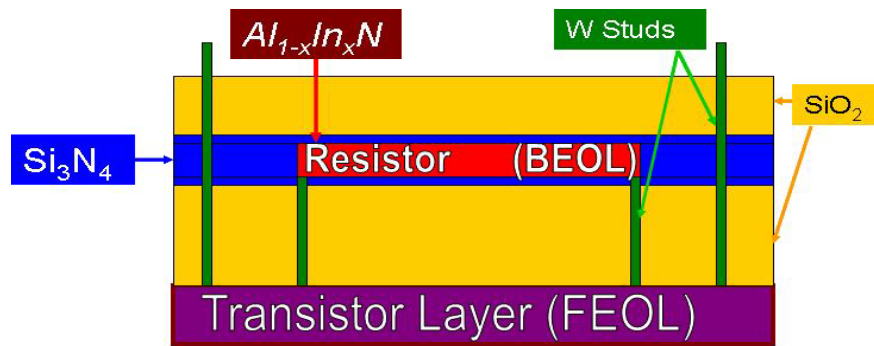


Fig. 5.12: The film is encapsulated with silicon nitride to prevent hydrogen enhanced oxidation

The resister film integration in the CMOS process is to be done after the step shown in figure 5.11 and before the one shown in figure 5.13 below. By moving the feedback resistors to a separate level that does not interfere with transistor processing, this scheme can be applied with significant improvement in density. On the hand, growth of diffused silicon or polysilicon resistor is simply not practical for CMOS technology on account of the constraints imposed by CMOS thermal budget.

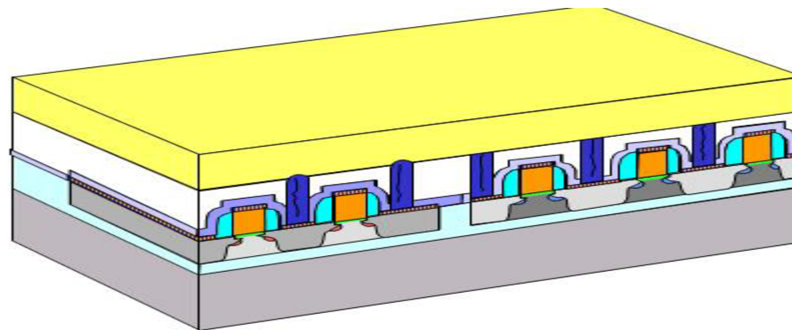


Fig 5.13: SiO_2 or Fluorine-doped tetra-ethyl-ortho-silicate (FTEOS) deposited by PECVD.

Growth of polysilicon resistor would require deposition temperature of 620°C followed by annealing at very high temperature of 1000°C for 30 minutes [111]. Growth of diffused resistor would not do much better either. The annealing temperature for diffused resistor has been reported at over 900°C for 10 minutes [111]. While the growth temperatures for these polysilicon resistors is clearly outside

the allowable CMOS temperature range, the sheet resistance realized is very low, specifically at 100-200Ω/□[104], 200-1200Ω/□[105], 74-80Ω/□[109], 40-300Ω/□[101] and 76-1100Ω/□[106].

Subsection 5.2.3: $In_xAl_{1-x}N$ Resistor is the Clear Choice

High value polysilicon resistors were traditionally used in nuclear and space hardened SRAM cells to decouple the latch nodes and delay the degenerative action of the cells, thus hardening against SEUs. The approach was successfully used through the 0.5µm technology node and 1M SRAM design. As the technology moved to the 0.25µm design node and below, the approach using of polysilicon resistor was abandoned in favor of active delay elements (transistors) such as BAE's 12-T cell and other design using 10-Tand 16-T designs. The transition was dictated by the following:

1) The high temperature coefficient of resistivity in lightly doped polysilicon requiring the design to account for over ×4 variation in resistivity over temperature range of -55 and 125C,

2) The use of polysilicon resistor at the gate level consumes significant die space, a factor that is clearly not compatible with high density requirements.

Use of a active delay elements such as 10-T, 12-T or 16-T SRAM cells are not practical either for deeply scaled technologies for two primary reasons:

1) The cell size is too large to support a 4M SRAM and beyond and

2) These cells are affected by increased SEU sensitivities due to reduction in critical spacing and the introduction of new upset mechanism s in scaled technologies

A new thin film high value resistor based on $In_xAl_{1-x}N$ alloy has been developed as the ultimate alternative to polysilicon and diffused resistors, as well as active delay elements in mitigating deeply scaled submicron CMOS technology SRAM from SEUs. The film sheet resistance is scalable from a fewΩ/Sq to MΩ/Sq depending on the design need. The resistor film has demonstrated incredibly low TCR less than negative 0.009%/°C for the temperature range of -55°C to 125°C and even lower TCR of negative 0.0012%/°C for temperature range of 25°C to 125°C.

A model for $In_xAl_{1-x}N$ resistor material has been developed based on material's point and extended defects. It was shown that DX^- centers are the dominating defects in setting the electrical properties of this film from temperature of 240K and above. Other defects that play significant role are the aluminum vacancies, aluminum interstitials, indium vacancies as well as nitrogen vacancies. The model traced the experimental results fairly well for sheet resistance with TCR of negative 0.003%/°C.

Chapter 6: Summary, Conclusions and Future Work

Section 6.1: Radiation Effects and Mitigation Strategies

Subsection 6.1.1: Operating in Radiation Environment

Electronics bound for space and nuclear environments subject to ionizing radiation. The radiation generates charge in the semiconductor leading to single event effects (SEEs). One of the SEE that is of primary concern in logic devices is the SEU. Of the two primary methods that a charge may be deposited is the direct ionizing and indirect ionization. Direct ionization occurs when an upset is triggered by the primary ion strike while indirect ionization takes place when a primary ion strike interacts the nucleus of silicon of metal layers including tungsten studs that connect the active devices to the outside. In deeply scaled submicron CMOS technology SRAMs, the problem of SEU has gotten worse with scaling of the technology node and scaling of core voltage. If not appropriately mitigated, the problem of SEU can course loss of valuable data or functionality, compromising mission or catastrophic loss.

Lightly doped polysilicon resistors were effectively used in cross-coupled latch of the SRAM cell to mitigate the problem of SEU for technology node of 0.5µm and above. As technology moved to 0.25µm node, the technique was abandoned in favor of transistors used as active delay elements because polysilicon resistors had very high TCR and very low sheet rho per square. High TCR required a design to account over a ×4 excursion in resistance and furthermore, consumed significant real estate on the

die. Use of such space is not compatible with high density requirements of deeply scaled technologies. Nonetheless, use of active delay elements has become too problematic because such use leads in the cell size becoming too large which cannot support large memory of 4M and beyond, the added transistors suffer from ever-increasing SEU sensitivity due to reduction in critical spacing and the introduction of new upset mechanisms. Even more critical to space applications, the system consumes too much power which is a limiting factor in space, where power is limited.

Subsection 6.1.2: Novel Material for Mitigating SEU

Anew material has been developed to mitigate the effects of SEU in space and nuclear environment. The material is based on III-V ternary alloy based on indium nitride and aluminum nitride binaries. The A model for the thin-film, high sheet rho material has been presented. For these resistors, electrical properties are primarily determined by point defects and the *DX* center traps for the temperature range that a device would typically be operated at. The magnitude of the resistor is completely determined by the alloy composition and the doping level of the material with no area penalty whatsoever. The resistor model agrees exceedingly well with experimental data for temperatures above 240K. From first principles, the simulated sheet resistance agrees remarkably well with our experimental results. Sheet resistance from 2kΩ/□ to over 3.5MΩ/□ has been reproducibly demonstrated. By changing either the alloy composition, doping level or both, sheet resistance of any magnitude can be realized.

Subsection 6.1.3: Choice of Resistor Material for Submicron CMOS

The choice of resistor material for deeply scaled submicron CMOS technology SRAM cells is governed by the following:

1. Magnitude of sheet resistor (Rs in kΩ/□)
2. Temperature Coefficient of Resistor
3. Thermal stability due to exposure to post anneal processing
4. CMOS thermal budget

These four conditions must all be met to meet the growing need for a practical SEU mitigation method for deeply scaled submicron CMOS technology memory and other digital logic applications.

Section 6.2: Validation of SEU Sensitivities in Submicron CMOS

Subsection 6.2.1: Validating By Pspice Simulation

A circuit response of a 6T-SRAM cell using IBM's 90nm, 130nm and 180nm process design kits has been presented. Simulation results indicate high level of vulnerability for these technologies to single event upsets. It has been demonstrated that deeply scaled submicron CMOS technology SRAM cells are highly prone to single event upsets even at strikes of LET of only 34.65MeV-cm^2/mg. Based on the circuit model, it has been shown that several hundreds of kilo ohm resistor may be required to stop SEU from taking place for an ion strike of only 34.65MeV-cm^2/mg LET.

Subsection 6.2.2: Validation by Irradiation with Heavy Ions

To support the use of cross-coupled latch resistors in deeply scaled CMOS SRAM cell technologies, we present a study on 90nm node 4M SRAM memory that was irradiated using a cocktail of 10 MeV/amu ions. The cocktail contained the following ions: B, O, Ne, Si, Ar, Cu, Kr and Xe. For the 4M SRAM, a LET threshold of 0.75MeV-cm^2/mg was determined. The study showed that for the SRAM under study, the upset cross-section was 4-5 times the physical cross-section suggesting occurrence of single-event multiple-bit upsets. Such upsets are due to nodal charge sharing causing upset in the neighboring cell as well as upsetting the cell that was hit. Other reasons that could cause increase in upset cross-section are upsets due secondary reaction products arising from nuclear elastic and inelastic collisions that create nuclear fragments that are more energetic that the primary striking particles.

Subsection 6.2.3: Validation by Irradiation with Pulsed Laser

In an effort to further validate the need for SEU mitigation with the film resistor, a new method of SEU testing using single photon and two photon irradiation has been presented. The goal for this test was to find ways that permits unencumbered access to the active region of the SOI 90nm 4M SRAM, enabling pulsed-laser and heavy ion single-event effects testing without limitations and complications associated with traversing the silicon substrate. XeF_2 was used to etch the substrate down to the buried oxide. Single event upset measurements were performed using above-band gap single-photon absorption and sub-band gap two-photon absorption.

Section 6.3: Future Work on Pulsed Laser Irradiation

Subsection 6.3.1: Pulsed Laser Irradiation

As previously shown, for 90 nm SOI-SRAM, an LET threshold of 0.71MeV-cm^2/mg was observed. The LET threshold observed in pulsed laser irradiation collaborated SEU sensitivities previously observed using heavy ions whose LET threshold had been found to be 0.75 MeV-cm^2/mg. What the results show is that the pulsed laser irradiation approach is just as good as the more expensive heavy ions irradiation. However, certain issues need to be addressed relating to general utility of the approach in the SEE community. In the next summary segment, we look at these issues and the future work that I plan to do.

Subsection 6.3.2: A Study to Address Effects of Substrate Removal

A question that remains to be answered is the role of the substrate in determining the SEE sensitivity of the SRAM. That is, does the removal of the substrate change the LET_{th} of the memory? Changes to the LET_{th} could arise from 1) additional heating due to the low mass, ii) coupling of charge, deposited an ion in the substrate, through the buried oxide to another sensitive transistor, and iii) loss of control of the SOI transistor threshold voltage (V_{th}) through removal of back contact. These concerns will be addressed by testing additional devices. In the next segment, I will discuss the approach for this experiment.

Subsection 6.3.3: Verification of Threshold Voltage in 90 nm SOI-SRAM

So as to determine if there is variation of the threshold voltage after removing the substrate, I plan to use photo-resist to selectively etch silicon on some parts of the SRAM. By covering half of the backside of the chip with photo-resist, silicon areas not covered with the photo-resist can be completely removed just the same way as it has reported. The photo-resist should then be removed and the remaining silicon can be etched to any desired thickness, compatible with the range of the ions intended for use in irradiation. At the completion of this step, it should then be possible to measure the LET thresholds in regions where only part of substrate has been etched away and compare the threshold voltage with the parts whose substrate is still intact. The preparation of this experiment will be tedious given that in order to access the die area, the experiment will have to be done before packaging and bonding has been done but it can be done.

Section 6.4: Future Work – Improvement of the Resistor Model

Subsection 6.4.1: Improvement on Theoretical Analysis

Modeling of electronic properties of a ternary semiconductor presents several challenges. From the theoretical standpoint, two approaches seem to dominate the *ab initio* techniques: the cluster expansion and the supercells approach. The first technique determines the properties of a ternary alloy by studying a set of ordered crystal structures in clusters[112]. In this framework, one can expand any property of disordered alloy from the properties of the clusters. The suppercell approach relies on

the study of large crystal cells where atoms of different species are placed randomly at different sites. In general, this would require a study of a larger sample of atoms than the cluster approach, since each cell can contain up to several hundreds of atoms. For the group III-V binaries of ternary alloys, some studies have been done which I have heavily referenced above. The two analytical approaches generally yield significant scatter of data and it is often difficult to tell which among the data is accurate. For the purpose of resistor simulation, it was necessary to pick the data that more closely reflected the experimental results.

Subsection 6.4.2: Comparative Study of Cubic verses Wurtzite Structures

The theoretical studies approach the analysis from either a pure zinc-blend or wurtzite structures. The limitation of such analysis is that neither of these structures fits material grown using RF magnetron sputtering because the film grown is not a pure crystalline material but rather polycrystalline. For polycrystalline structures, crystalline structure consists of variously orientated crystal planes and grain lines and boundaries. There are crystals of varying size which are randomly organized owing to the growth and production conditions. i.e. heat and time for crystals to develop as opposed to purely crystalline structures which form an organized crystalline structure, with well organized grain boundaries. The analysis of the type of traps and their level and state of occupancy is such that, while a particular condition is found when a material is in cubic form, it may be lacking when the same material is considered in wurtzite form.

Subsection 6.4.3: Review of Assignment of Trap Levels

Another challenge emerged in evaluating of trap levels. Even when only one form of polytypic material is considered, the calculation method applied may overestimate or underestimate the trap levels. This is likely to be the primary reason why the model does not replicate the experimental data for the entire temperature range for which the experiment was done. The problem of overestimation or underestimation of material properties in ternary alloys was identified[113, 114] and an attempt was made to combine First-Principles Total Energy Calculation (FPTEC) with Generalized Quasichemical Approach (GQA) to analyze gap fluctuations in $InAlN$ alloy leading to a concept of minimum gap and average gap of the material. We believe that a major effort need to be made to link the properties of wurtzite and cubic structures with the aim of establishing the electronic properties of this material and explain how the material exists in a mixed form. As part of future work, there is a need to improve on the theoretical analysis in assigning trap levels especially when dealing with material that may have more than one crystal structure form among the crystal mixture.

Section 6.5: Future Work- Integration on MITLL 40nm and 150nm Process

Subsection 6.5.1: Integration in 150 nm MITLL CMOS Process

MIT Lincoln Laboratory has identified 150nm fully depleted SOI, 64K SRAM cell structure in which the thin-film high-value resistance material will on. Figure 6.x1 shows the cross-section of a cartoon drawing and the cell layout. For the SRAM, the

design requirement for cross-coupled resistor latch is 25kΩ/□ and will need a total of 50kΩ to 75kΩ. If this resistor were to be implemented using a polysilicon resistor of a typical sheet resistance of 100Ω/□, a total of 750 squares would have been needed, taking valuable space on the die. Using the material that has been presented, only two squares will be needed!

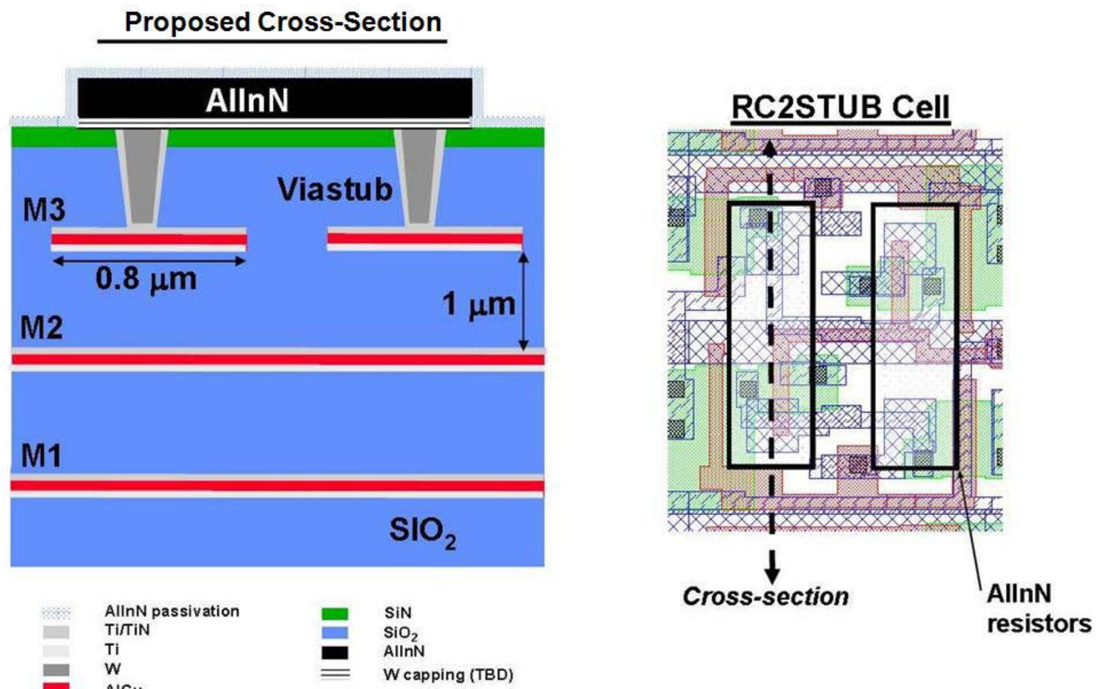


Fig. 6.1: Structure of the SRAM showing how the resistor film will be integrated in an FDSOI 64K SRAM

The feedback resistor paste is to be implemented on the planar surface level connecting the tungsten studs with the underlying devices. A silicon nitride layer will be deposited to encapsulate the resistor film, followed by another layer of silicon oxide. The second layer of tungsten studs formed is to connect the film resistor to the first metal level. Device processing continues as is typically done in CMOS processing. By moving the feedback resistors to a separate level that does not interfere with transistor processing, the resistor film is implemented without affecting transistor density.

Subsection 6.5.2: Integration in 40 nm MITLL CMOS Process

The integration process at MIT Lincoln Laboratory will use a 3-metal FDSOI CMOS wafers with non-planarized passivation layer over the contact pads. The layer will have 1000 nm novellus SiO_2 deposited and planarized using chemical mechanical polishing (CMP) followed by a capping layer of 100 nm Si_3N_4. To access the SRAM cell, via-stub lithography will then follow. The area to be opened is a 0.8 µm × 0.8µm plug above each inverter. The next step will include a via-stub etch, etching Si_3N4 and SiO_2 with metal layer 3 being the etch stop. The vias are to be filled in the following sequence: 30 nm titanium followed by 75 nm titanium nitride followed by another 500 nm of tungsten.

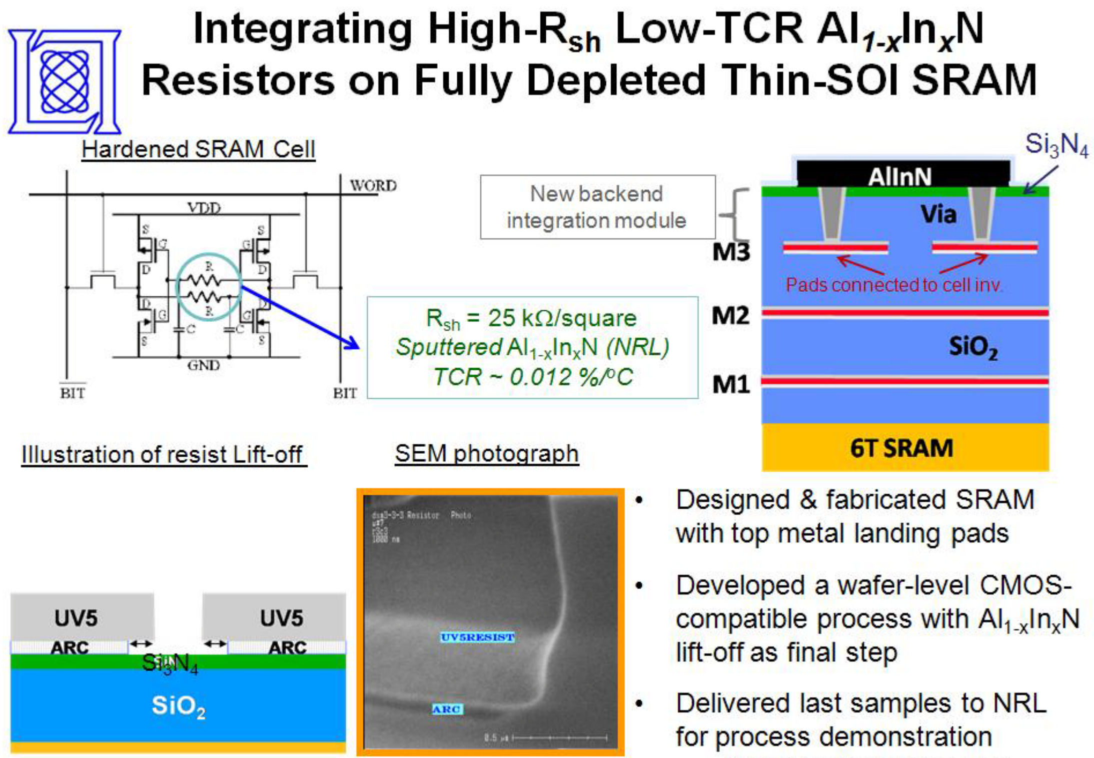


Fig. 6.2: Integration module proposed for $In_xAl_{1-x}N$ resistor on MITLL 40 nm CMOS Process. The integration process was presented at Defense Threat Reduction Agency's review on April 2, 2010 by MIT-LL.

The last step will be followed by CMP of the tungsten followed by another layer of 75 nm titanium nitride. At this stage, resistor lift-off lithography will be done to pattern the resistor stub as shown in figure 6.1 above. The wafers will then have the $In_xAl_{1-x}N$ film deposited followed by lift-off process. At this point the integration process at MITLL process will be deemed complete and the wafers will be ready for dicing, packaging and boding.

Subsection 6.5.3: Integration in IBM's and BAE's CMOS process

The process flow described in section 6.5.2 above will be adopted will some modification to optimize it for IBM 45 nm CMOS process at Albany Nanotech Facility and SUNY Albany. BAE McLean, Virginia, is in the processes of satisfying the resistor material for their 90 nm process. BAE had opted to use TaN film resistor but the effort failed because the film failed to adhere to the SiO_2 surface [115]. The said difficulty is not expected to be a factor in $In_xAl_{1-x}N$ thin-film high-value resistor because the films alloys well with Si_3N_4 which itself alloys very well with SiO_2 interface.

Section 6.6: Future Work:-Verification of Design Radiation Hardness

Subsection 6.6.1: Heavy Ion Irradiation

As technology scaling continues, low-LE particles will dominate SEU sensitivities. To validate the efficacy of cross-coupled latch resistors, high-energy low-LET ions will be used to characterize the SRAM bit-cells. A set of SEU experiments will need

to be done to provide estimates of upset rates in various space environments, including low Earth Orbit (LEO), geostationary orbit and deep space.

Subsection 6.6.2: Low Energy Proton Irradiation

We have already established that even at 90 nm technology, less that 3000 electrons are all it takes to upset the SRAM due to direct ionization from alpha particles, protons or heavy ions. Because of high concentration of these particles, detailed understanding of circuit response to SEU is critical. Experiments to evaluate the efficacy of cross-couples latch resistors hardening against SEU events will be conducted at NASA's low energy proton facility.

Subsection 6.6.3: Two-Photon and Single-Photon Laser Irradiation

The upset rates will be correlated with Two-Photon and Single-Photon experiments. Use of substrate removal will permit deposition of energy at selected locations. Use of SPA technique will provide for smaller spot-size. Use of the technique should facilitate use of UV and deep UV light, providing for capability of using less energy for deeply scaled technologies

Appendices

The ability of both silicon and oxygen to transition between shallow and DX centers requires that electron concentration model consider these trap's occupancies as the Fermi level change with temperature. Following the formulism of Theis et a.[17], the concentration of ionized silicon or oxygen donors is given by:

$$N_D^+ = \frac{N_D}{1 + \exp\left[\left(E_D^h - E_F\right)/kT\right] + \exp\left[2\left(E_{DX}^- - E_F\right)/kT\right]} \qquad \text{(A1)}$$

And the concentration of DX centers is given by:

$$N_{DX}^- = \frac{N_D \exp\left\|2\left(E_{DX}^- - E_F\right)/kT\right\|}{1 + \exp\left[\left(E_D^h - E_F\right)/kT\right] + \exp\left[2\left(E_{DX}^- - E_F\right)/kT\right]} \qquad \text{(A2)}$$

where E_D^h and E_{DX}^- are the Gibbs energies for transfer of an electron from the appropriate level to the CBM, and are defined ad as positive if the level lies below the band edge. E_F is the Fermi level. In the model, we reason that:

$$N_D = N_D^0 + N_D^+ + N_D^- \qquad \text{(A3)}$$

where N_D^0 is the density of donors in the neutral hydrogenic state. In this model a distinction is made between N_D^0, N_D^+ and N_{DX}^-. The formation of DX centers follows loss of two substitutional atoms with one giving up an electron to become N_D^+ with the one gaining the electron becoming N_{DX}^- since it has captured the electron. What is left after these two atoms pair up is what can participate in conduction. This relation follows from DX formation as presented above and is repeated in figure 3.14 below for convenience.

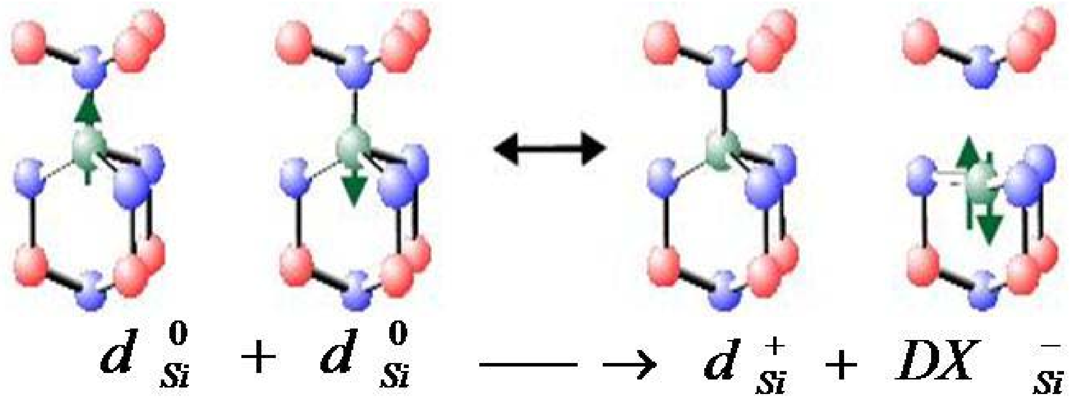


Fig. 3.14: DX trap formation to the right takes an electron from one of the substitutional silicon atoms, effectively depriving the loosing atom ability to donate electron in the conduction band even though the loosing atom still remains in substitutional level. Figure after [62].

If the dopant donor was the only source of electron concentration, then the concentration of electrons that are still available to participate in the conduction band is given as:

$$n = N_D \frac{1 - \exp\left[2\left(E_{DX} - E_F\right)/kT\right]}{1 + \exp\left[\left(E_D^h - E_F\right)/kT\right] + \exp\left[2\left(E_{DX} - E_F\right)/kT\right]} - p \qquad \text{(A4)}$$

Glossary

AlGaN……………………………………………….…Aluminum Gallium Nitride

AlN…………………………………………………………Aluminum Nitride

BEOL……………………………………………………Back End Of the Line

BOX…………………………………………………………….Buried Oxide

CBM…………………………………………………Conduction Band Minimum

CFA…………………………………………………Conventional Furnace Anneal

CMOS…………………………………Complementary Metal Oxide Semiconductor

DFT-LDA……………….…Density Functional Theory-Local Density Approximation

DFT-GGA… …..Density Functional Theory-Generalized Gradient Approximation

DX………………………………………………………………………….Donor X

ECR…………………………………………………Electron Cyclotron Resonance

EDAC…………………………………………Error Detection and Correction Code

FDSOI……………………………………..Fully Depleted Silicon on Insulator

FWHM……………………………………………….Full Width at Half Maximum

GCR………... ……………………………………………Galactic Cosmic Ray

HSQ……………………………………………………Hydrogen Silsesquioxane

InN……………………………………………………………….Indium Nitride

LET………………………………………………………Linear Energy Transfer

LET_{th}…………………………………………....Linear Energy Transfer Threshold

LPCVD………………………………..Low Pressure Chemical Vapor Deposition

MBU…………………………………………………………Multiple Bit Upset

MeV……………………………………………………..Million Electron Volt

NSRE……………….Conference…Nuclear and Space Radiation Effects Conference

PECVD……………………………….Plasma Enhanced Chemical Vapor Deposition

PMMA……………………………………………..PolyMethyl MethAcrylate

QMD……………………………………………Quantum Molecular Dynamics

RF…………………………………………………………Radio Frequency

RIE…………………………………………………………Reactive Ion Etch

RHBD…………………………………………..Radiation Hardened by Design

RTA…………………………………………………….. Rapid Thermal Anneal

SACVD………………………………Sub-Atmospheric Chemical Vapor Deposition

SCE……………………………………………….……Short Channel Effect

SEE……………………………………………………Single Event Effects

SEFI………………………………………… Single Event Functional Interrupt

SEU………………………………………………………..Single Event Upset

SIMS…………………………………….…Secondary Ion Mass Spectroscopy

SOI………………………………………………………..Silicon On Insulator

SPA…………………………………………………Single Photon Absorption

SRAM…………………………………………...Static Random Access Memory

SRIM……………………………………… **S**topping and **R**ange of **I**ons in **M**atter

STI……………………………………………………. Shallow Trench Isolation

TCR………………………………………Temperature Coefficient of Resistance

TMR……………………………………………Triple Modular Redundancy

TPA……………………………………………………...Two Photon Absorption

VBM………………………………………………Valence Band Maximum

XPS……………………………………………...X-ray Photoelectron Spectroscopy

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