TECHNICAL RESEARCH REPORT

Built-In Self-Test and Fault Diagnosis for Analog Circuits in the Frequency Domain

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T.R. 95-15

Sponsored by
the National Science Foundation
Engineering Research Center Program,
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and Industry

Built-In Self-Test and Fault Diagnosis for Analog Circuits in the Frequency Domain

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Abstract

Due to the increasing complexity of analog circuits, finding out whether an analog circuit meets the required specifications is a difficult and time consuming task. We propose a complete Built-In Self-Test and Fault-Diagnosis circuit based on the frequency domain specifications for analog circuits in order to reduce the time and effort for testing. This built-in circuit supports a automated yes or no testing when used in production test. Furthermore, the ability to access internal blocks inside an analog circuit provides a fault diagnosis ability when an engineer wants to find out the cause of faulty circuits. Coupled with extra multiplexers, this circuit can be used to detect faults in analog parts in a mixed signal circuit.

1 Introduction

The increasing density and complexity of integrated circuits makes testing more difficult, especially for analog circuits. Analog testing often requires testing a large number of specifications to determine whether the circuit is faulty. Furthermore, the testing of all of these specifications may provide very limited information on the identity of faults when specifications are failed. This is because some analog blocks may be deeply embedded in a circuit. The cost of testing can however be reduced if the testing of several specifications is automated by on-chip test circuitry, cutting the time required to connect signals and measure responses. Furthermore on-chip test circuitry can provide information on the location of faults when they occur.

The problem of gaining access to internal nodes has been approached in several papers [1, 2, 3] through adding extra circuitry to increase observability. This work has introduced analog scan cells or an analog testing bus in order to make internal test points visible from external test pins. This paper goes beyond these approaches by putting some of the test measurement and analysis hardware on chip so that during production test all that is required is the evaluation of a single bit to determine if a circuit meets specifications. Specifically, in this paper, a Built-In Self-Test(BIST) circuit is presented for frequency domain measurements, where the frequency range supported is the telecommunication range from 0 to 4K Hz. However, the design can be used for a higher frequency range, but different capacitor ratios would be needed. The circuit also provides a fault diagnosis capability by increasing the observability of blocks.

This paper is divided into 4 sections. The BIST circuit in the frequency domain and fault diagnosis through the access to internal circuit blocks are described in section II. A filter bank which implements a wavelet transform [4] is used as an example in section III. We conclude in section IV.

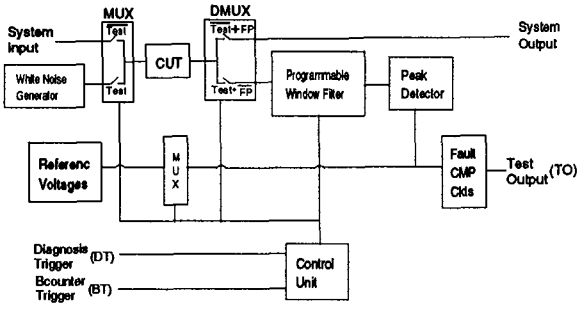


Figure 1: BIST circuit in frequency domain

2 BIST in the Frequency Domain

In the frequency domain, the specifications for analog circuits are often gain within a certain frequency range or at a specified frequency point. For example, in a bandpass filter, a minimum gain is required in the frequency range of the passband; maximum allowable gain is specified in the rejection frequency range; total harmonic distortion and maximum allowable ripple at a certain frequency region are also specified. Therefore, in our frequency domain BIST circuit, we provide the ability to detect a gain in a certain frequency range or at a frequency point. The block diagram of the complete BIST circuit in the frequency domain is shown in Figure 1, which includes 7 parts, (a) a white noise generator, (b) a programmable window filter, (c) a peak detector, (d) a reference voltages, generator, (e) a fault comparison circuit, (f) a control unit and, (g) multiplexers.

The white noise generator is used to generate white noise to feed into the circuit under test (CUT). White noise has a flat spectrum which is used to trigger the response at any frequency. The frequency range of interest is selected by the programmable window filter as shown in Figure 2. This programmable window filter has two major parts , a programmable lowpass filter and a programmable highpass filter. Other switches in this programmable window filter are used to select the frequency range needed. For example, for the rejection region the required frequency range can be obtained by either the lowpass filter or the highpass filter alone. In this case, either S1 & S2 conduct or S4 & S5 conduct. If a gain specification in a certain frequency range is of interest, the lowpass filter combined with the highpass filter can provide a window filter. In this case, S1, S3 and S5 conduct. The programmable lowpass filter coupled with the highpass filter can form a window filter with any center frequency.

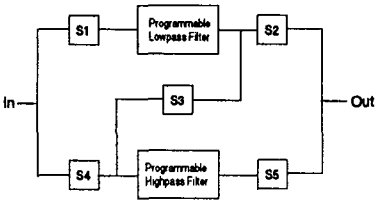


Figure 2: programmable window filter

Once the spectrum of interest in a certain frequency range is obtained through the movement of the programmable window filter , the peak detector is used to select the maximum magnitude of the frequency response in the range of interest. This maximum frequency response is then compared with the reference voltage generated from the reference voltage generator.

The multiplexer and demultiplexer in the upper part of Figure 1 are used to select the mode of circuit operation, either the normal or the testing mode. In the testing mode, the yes or no production test is automatically performed. However, the responses of internal circuit blocks for fault diagnosis purposes can be displayed if an external signal, diagnosis trigger (DT), is set. The FP signal, generated from the control unit, in the upper demultiplexer is used to control the path for fault diagnosis. In the fault diagnosis mode, the response of each internal block is sequentially connected to the system output using the external signal, BT. The multiplexer in the lower part of Figure 1 determines the required reference voltage for different specifications. Finally, the control unit generates all the required control signals, including those which identify the filter type and the capacitor ratios for the programmable window filter. Only three extra external pins, DT , BT, and TO in Figure 1, are required for this BIST circuit. A detailed discussion of the circuits of each part follows.

2.1 White Noise Generator

The white noise generator [5] is used as a signal source in this paper. A white noise generator has a wideband flat spectrum. It triggers any frequency response at any frequency point. This circuit could be either implemented using discrete components or as an integrated circuit. Our current implementation relies on an external source.

2.2 Programmable Window Filter

As shown in Figure 2, the programmable window filter consists of two major parts, a programmable lowpass filter and a programmable highpass filter. From the cascade of these two parts, the movable window filter can be built. The programmable lowpass filter is shown in Figure 3, where $C_1 = C_2 = C_{o1} = C_{o2} = C_{a1} = C_{b1} = 1$, $C_5 = H$ and $C_7 = C_{6_1} = C_{6_2} = \ldots = C_{6_n} = 0$. The capacitors, $C_{3_1}, \ldots, C_{3_n}$ $C_{A_1}, \ldots, c_{A_n}$ $C_{B_1}, \ldots, C_{B_n}$ are determined using Table 1. The unit capacitance in this design is 1 PF. H, the designed gain, and the Q factor are both 1 in this design. All of these factors are adjustable to fit different requirements. The circuit is a charge differencing (CD) biquad [4] . This CD biquad reduces the capacitance ratio from $\frac{1}{WT}$ to $\frac{1}{\sqrt{WT}}$,

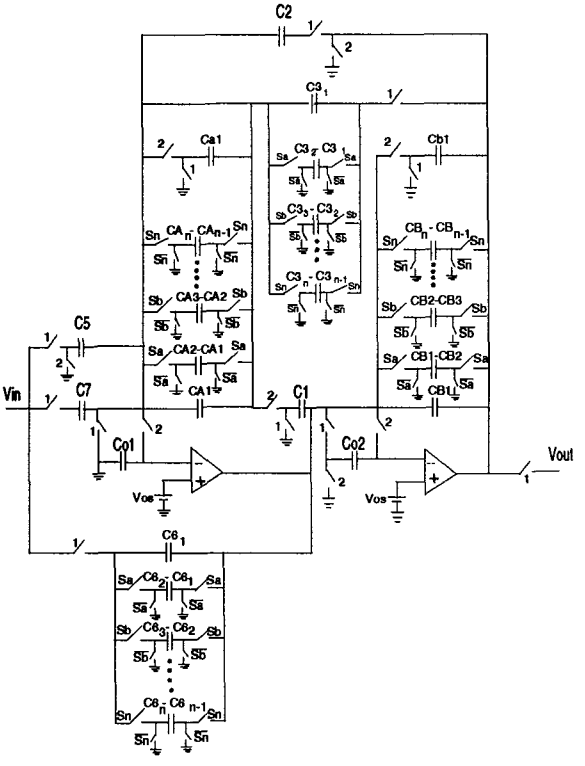


Figure 3: Programmable lowpass and highpass filter

where W is the center frequency and T is the sampling period. This property is very useful when a low center frequency W is needed. The center frequency is determined by the capacitance ratio which is programmable through the control of the switches S_a to S_n. In Table 1 the capacitor ratios needed to implement the different center frequencies with different control switches are shown.

As mentioned in the introduction, we support the frequency range from 0Hz - 4KHz. However, applications in the high frequency range can be implemented through the change of the ratios of capacitors. In the high frequency region, conventional biquads can be used to replace the CD biquads since such a circuit is simple and the capacitance spread ratio is acceptable.

The programmable highpass filter is architecturally the same as the lowpass filter, and is therefore also shown in Figure 3, where $C_1 = C_2 = C_{o1} = C_{o2} = C_{a1} = C_{b1} = 1$, $C_5 = C_7 = 0$ and $C_{6_1}, \ldots, C_{6_n}$ are determined by Table 1. The cutoff frequency is determined by the controlled switches. The capacitance ratio for different center frequencies is also shown in Table 1.

In reality, these two circuits can be simplified once the application of the CUT is known. Only a small number of the ratios of capacitances are needed. Extra switches and capacitors can be removed. The simulation results of a programable lowpass filter with a cutoff frequency at 1kHz and a highpass filter with cutoff frequency at 2K are shown in Figures 4 (a) and (b) respectively. The window filters, whose center frequencies are moved from 1K to 2.2K with a step size of 0.2K, formed by the cascade of the programmable lowpass filter with the

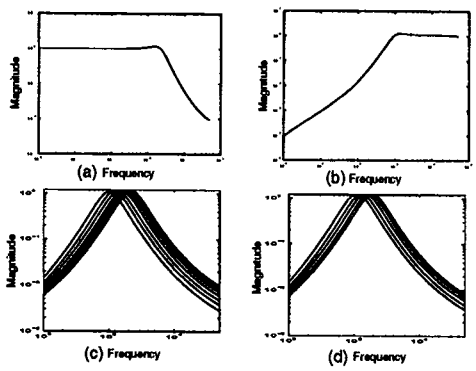


Figure 4: Filter responses

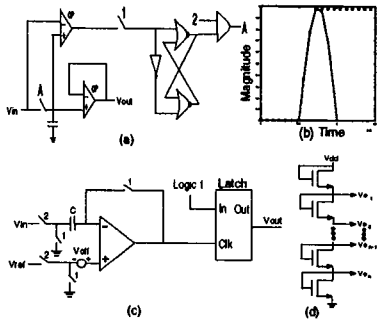
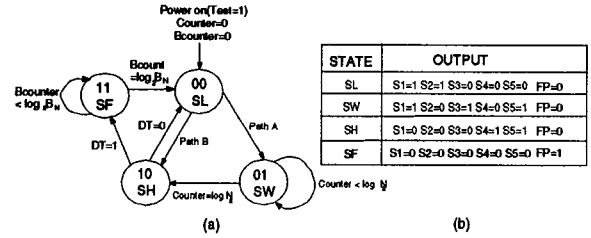


Figure 5: Auxiliary circuits

programmable highpass filter are shown in Figure 4 (c) and Figure 4 (d). The window width is zero in Figure 4 (c) and is 0.2K Figure 4 (d).

2.3 Peak Detector, Comparison Circuit and Reference Voltage Generator

The peak detector is used to detect the peak response at a certain frequency point or in a frequency range [6]. This is useful when the the specifications are required to meet a maximum limit. However, the minimum limit can be checked through the movement of the window filter with the peak detector. The detailed peak detector circuit is shown in Figure 5 (a). The time domain simulation of this circuit is shown in Figure 5 (b), where an input sinewave is sampled and held at its highest voltage level. The selected maximum response is then checked against the specification with a comparison circuit. The specification used to compare is determined by the control unit and the multiplexers. The circuit for fault comparison is offset compensated and the design is shown in Figure 5 (c). The reference voltage generator is a voltage divider which generates the desired voltage reference according to the requirements of the specifications. One traditional design is shown in Figure 5 (d).



STATE	OUTPUT
SL	S1=1 S2=1 S3=0 S4=0 S5=0 FP=0
SW	S1=1 S2=0 S3=1 S4=0 S5=1 FP=0
SH	S1=0 S2=0 S3=0 S4=1 S5=1 FP=0
SF	S1=0 S2=0 S3=0 S4=0 S5=0 FP=1

Figure 6: State diagram of control unit

2.4 Control Unit and Multiplexer

The control unit is implemented by a state machine. The state diagram is determined by the specifications of the CUT. A general state diagram is shown in Figure 6 (a). From this diagram, there are four states, SL, SW, SH and SF, which represent different filter configurations, the lowpass filter, the window filter, and the highpass filter in the production testing mode, and the fault diagnosis mode. Each state controls the configuration in the programmable window filter through the switches $S_1, \ldots, S_5$ in Figure 4 as shown in Figure 6 (b). In the production test mode, there are two paths in this diagram. Using path A, the low frequency rejection is first tested(SL), followed by the passband(SW), where the window is moved to check the ripple. While testing the passband, the counter in the state diagram is used to generate the control signals, $S_a, \ldots, S_n$ in Figure 3. In order to move the programmable window, Log_2N flip flops and some logic gates are needed to form the counter and decoder, where N is the number of center frequencies used. Finally, after the passband is tested, the high frequency rejection is tested(SH). Otherwise, using path B an abreviated test can be performed without window movement.

The Bcounter in the state diagram generates the control signals, $b_1, \ldots, b_{B_N}$, which make different blocks observable. Unlike the counter, Bcounter is increased by 1 only when a pulse is applied to the external input pin, Bcounter trigger (BT). This allow the engineer to observe the faulty block as long as he likes. B_N is the number of blocks and $b_1, \ldots, b_{B_N}$ are all zero if in the production mode.

2.5 Fault Diagnosis

To obtain the fault diagnosis capability, the circuit under test(CUT) needs extra multiplexers(MUX) in order to allow internal block access. However, the extra MUXs should not affect the original circuit topology when the circuit is not in the testing mode. The extra MUXs are inserted as shown in Figure 7. Through the control signals, $b_1, b_2, \ldots, b_{B_N}$, each block in the circuit can be scanned sequentially in the fault diagnosis mode.

3 Case Study : A Parallel Filter Bank

A filter bank [4], including one highpass filter, three biquads, and one sum-gain amplifier, is used as an example. This circuit implements a wavelet transform. Four specifications, passband response, leftside rejection, rightside rejection and a gain at a desired frequency f_i, are of interest, and these specifications are shown in Figure 8. In order to verify the capability

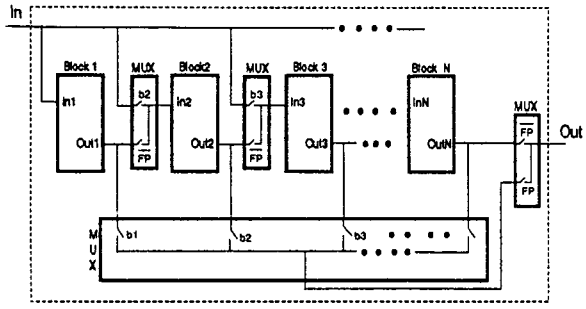


Figure 7: CUT for fault diagnosis

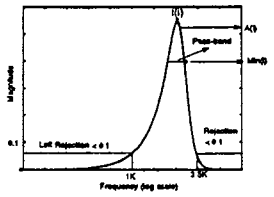


Figure 8: Specifications

of this circuit, the operational amplifier(OP) in the sum-gain block(SGA) is assumed to have a lower gain, 40 dB(100), due to manufacture fluctuations, where the original desired gain is 60dB(1000).

The response of the good circuit versus the faulty circuit is shown in Figure 9 (a). From this figure, we know that the lower gain in the OP of the SGA has drastically changed the circuit's response, and it fails the specifications required. As mentioned in the section on the control unit, the response of the CUT is first connected to the lowpass filter, which results in the spectrum shown in Figure 9 (b). From this figure, we know that the faulty circuit fails the specification on the left-side rejection region and the lowpass filter is able to extract this information. Then, the state machine changes the configuration to the window filter. The response of the window filter being applied to the output of the CUT, with a center frequency of 2.2K, is shown in Figure 9 (c). From this figure, the specification at f_i also fails. Finally, a highpass filter is applied to the output of the CUT to extract the response in right side rejection range and the response is shown in Figure 9 (c). Apparently, the faulty circuit has a much higher response in magnitude in this range and violates the specification. Most of the faults will not cause all of the specifications to fail. However, failing to meet any of the specifications will result in a logic 1 at the testing output.

4 Conclusion

In this paper, we propose a complete BIST and fault diagnosis circuit, which provides fast production testing and useful fault diagnosis capability. Simulations of the proposed built-in circuit show the faulty response of the faulty circuit can be detected. The integrated circuit implementation of this circuit is being fabricated.

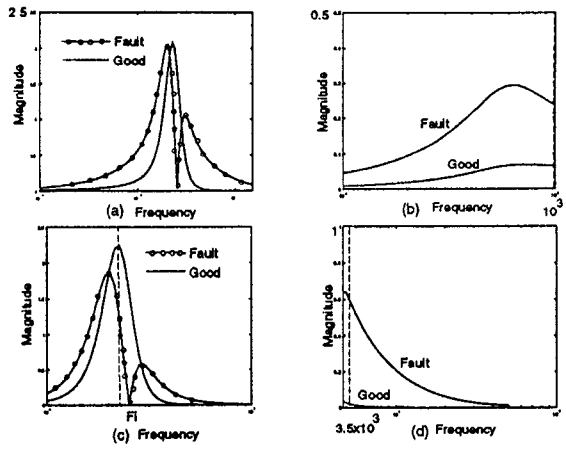


Figure 9: Simulation Results

Center f	C_{a_i}, C_{b_i}	C_3	C_6	index i
200	9.4986	9.4746	9.4509	i=1
400	6.5880	6.5548	6.5216	i=2
600	5.3017	5.2615	5.2218	i=3
.	.	.	.	.
.	.	.	.	.
4000	1.8434	1.7492	1.6598	i=20

Table 1. Capacitance Ratio

Acknowledgment

This work has been supported by the NSF under the following grants: MIP-9211407, NSF D CDR 8803012, and NSF EEC 94-02384.

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