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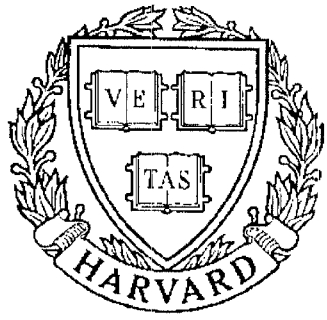

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Fault-Driven Testing of LSI Analog Circuits

by C-Y. Chao, H-J Lin and L. Milor

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FAULT-DRIVEN TESTING OF LSI ANALOG CIRCUITS

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Abstract

Analog circuits are usually tested by checking if their specifications are satisfied. This methodology is very costly. We attempt to reduce production testing time by presenting a fault-driven methodology to handle LSI analog circuits in this paper. A fault-driven methodology has to be able to detect both parametric and catastrophic faults. For statistical performance simulation to detect parametric faults, we propose a two level approach because of the high cost of simulating LSI analog circuits statistically, where a set of primary statistical variables are first mapped to block performances by empirical models, derived by statistical regression techniques and then mapped to system performances using a behavioral simulator. For catastrophic fault simulation, open and short circuits are mapped to distortions in block performances by simulation and then mapped to system performances using a behavioral simulator. Using our statistical simulation technique for parametric variations and our fault simulation technique for catastrophic faults, we will minimize testing time using the algorithm in [1] by eliminating unnecessary specification tests and optimizing the order of tests. The effectiveness and fault coverage of block level testing are also investigated.

1. Introduction

Analog testing is a difficult task without a clear-cut methodology. Even for small analog circuits, testing all specifications to screen out faulty circuits is too time consuming. Given the high cost of testing all specifications, it has been proposed that the specification testing time for analog circuits can be reduced by selecting a subset of specification tests based on their detection of possible faults. This fault driven approach has been proved to be good at detecting both catastrophic and parametric faults, while drastically reducing test sets for some small circuits in [2]. Existing algorithms can not be applied directly to large scale integrated(LSI) circuits because of the high computational cost of statistical simulation. Nevertheless, for LSI analog circuits, the fault-driven methodology is still promising but we need a hierarchical approach.

In this paper, an LSI analog circuit(system) is decomposed into several sub-circuits(blocks) and a behavioral model is used to build the bridge between performances of the system and of the blocks. Analog circuits generally require large numbers of independent variables to model mismatch, requiring a computationally intensive screening experiment to find a smaller subset explaining most of the variations in the processes. If a circuit has n primary process or device parameters, modeling process fluctuations, and m transistors, a novel approach, which only needs to consider $O(mn)$ process or device parameters, including mismatch effects, when undergoing a screening experiment, is proposed to find a smaller subset of process or device parameters. The statistical regression technique is adopted to establish the relation between the reduced set and blocks. Defect simulations using VLASIC [3] are used to gather a set of possible open and short nodes and then this set is mapping to block parameters through the circuit simulator SPICE. Finally, a subset of the specification test set, detecting all faults, and an optimal order of the test set are found by applying the algorithms developed in [2] at the system level to minimize test time and attain a desired fault coverage.

Two different methodologies for block testing are investigated in this paper. One approach starts by finding uncorrelated block parameters which form the basis of the acceptability region in block parameters. The nonlinear relation between the acceptability region at the system level and the acceptability region at block level make this approach difficult to implement. Therefore, an alternate approach to loosely define the acceptability region at the block level is proposed and it is compared with testing at the system level.

We begin this paper with the formulation and solution of problem of fault-driven testing. The detailed methodology to model parametric and catastrophic faults is presented in next section. Finally, we conclude by applying our methodology to a cyclic A/D converter [4].

2. Formulation and Solution of the Problem

2.1. System Level Testing

At the circuit level, it is easiest to categorize faults as being catastrophic or parametric. Catastrophic faults characterized by open nodes, short between nodes, and topological changes in a circuit, almost always result from local defects, mainly coming from contamination by particles in masking, oxidation and doping processes. Parametric faults mostly come from global defects which affect all devices on a chip and are induced by uncertainty in the process environment, such as instability of materials, temperature gradients, and other process disturbances, but they can also come from local defects in some structures like capacitors. In addition, on rare occasions global defects can also result in catastrophic faults. Both local and global defects are generated from different mechanisms and it is reasonable to assume they are statistically independent and possible to approximate their probability density functions.

Since faults are identified by system specifications, the definition of the acceptability region, which is a function of process and device parameters, needs to be related to the system specifications. Let S be the index set of all system specifications and A_i be the set of process and device parameters satisfying i^{th} system specification. The acceptability region, defined in terms of device or process parameters, is

$$A_s = \bigcap_{i \in S} A_i$$

and the yield is defined as

$$Y = \int_{A_s} f(g,l) dg dl$$

where g and l are parameters relating to global and local defect distributions respectively, and $f(g,l)$ is the joint probability density function of global and local defects.

It is difficult to calculate yield directly from local and global defect distributions. Instead it is easier to work with the probability density function of catastrophic and parametric faults at a higher level of abstraction. Since the probability density function of catastrophic faults is essentially independent of sources of global parametric variations, we will separate this component and we can say that the yield can be expressed as a function of the probability density function of catastrophic faults, $f_c(c)$, and the conditional probability density function of parametric faults $f_p(p|c)$:

$$Y = \int_{R^n} f_c(c) [\int_{A_{s(c)}} f_p(p|c) dp] dc$$

where p and c are parameters relating to parametric and catastrophic fault distributions respectively. $A_{s(c)}$ is the acceptability region for a particular catastrophic faults, c.

Note that the catastrophic probability density function is usually treated as a discrete distribution, and moreover, for most catastrophic faults

$$\int_{A_{s(c)}} f_p(p|c) dp = 0$$

If this were the case for all catastrophic faults then yield is computed as follows:

$$Y = (\int_{c=0} f_c(c) dc)(\int_{A_{s(0)}} f_p(p) dp)$$

where $c = 0$ denotes the situation when the circuit contains no catastrophic fault.

This is, however, not usually the case. Our methodology, therefore, is to evaluate $\int_{A_s} f_p(p|c) dp$ for the good circuits and for those faulty circuits for which it is not obvious that this integral is zero. These quantities are then used to calculate yield. To compute the probability within a region A_i, the indicator functions $Z_i(p|c)$ is defined for a parametric distribution, given a catastrophic fault or a good circuit, as

$$Z_i(p|c) = \begin{cases} 1 & \text{if system response at } p \text{ satisfies} \\ & \text{the } i_{th} \text{ system specification} \\ 0 & \text{otherwise} \end{cases}$$

Therefore, the probability of a parametric fault within a region A_i is com-

puted by

$$P_p(c) = \int_{A_{s(c)}} f_p(p|c)dp = \int_{R^n} Z_i(p|c) f_p(p|c)dp$$

The integral $\int_{R^n} Z_i(p|c) f_p(p|c)dp$ is approximated by Monte Carlo Analysis, where p is generated according to $f(p|c)$ and $P_p(c)$ is approximated by $\hat{P}_p(c)$:

$$\hat{P}_p(c) = \frac{1}{N}\sum_{i=1}^{N} Z_i(p_i|c)$$

N is the number of p_i that are generated.

An intuitive method to determine $Z_i(p_i|c)$ is by circuit simulation of the system for each p_i to check whether or not the system response at p_i satisfies the i_{th} specification. Since this methodology needs too many circuit simulations, an alternative method is a two level approach to formulate system performance ϕ_i as a function of p_i. The relation among device and process parameters, p_i , block parameters, b_i, and system performances, ϕ_i ,can be expressed as

$$\phi_i = h(b_i) = h(w(x_i))$$

The implementation of the mapping function $w(\cdot)$ from device level to block level is formulated using a statistical regression model, while the mapping function $h(\cdot)$ from block level to system level is formed by a behavioral model. Therefore, the determination of whether or not p_i is in the acceptability region can be easily achieved through $w(\cdot)$ and $h(\cdot)$.

Yield is computed by

$$Y = \int_{R^n} P_p(c) f_c(c)dc$$

where $P_p(c)$ indicates the probability that a circuit with a catastrophic fault, c, passes the i^{th} specification test. The probability density function, $f_c(c)$, is determined using defect simulator VLASIC to place defects, whose density in each layer of the processes depends on the class of clean room and assumes a negative binomial distribution. If a total of N_t samples are generated, and the yield is approximated by

$$\hat{Y} = \frac{1}{N_t}\sum_{i=1}^{N_t} \hat{P}_p(c_i)$$

Note that $\hat{P}_p(c_i)$ does not have to be computed for every single local defect. Most local defects do not have any significant impact on a circuit. They can therefore be grouped together with the good circuit and $\hat{P}_p(c_i)$ will be calculated once for the entire set and is the probability corresponding to the fault-free circuit. Also many other local defects affect the same geometry, and they too can be grouped together to use the same value of $\hat{P}_p(c_i)$.

The algorithm for determining the optimal test set not only requires the computation of yield for all specifications, but also yield for subsets of specifications. Consider a test set $T \subset S$ which is a subset of specifications, S. The corresponding acceptability region is A_T:

$$A_T = \bigcap_{i \in T} A_i$$

Specifically computing the optimal test set will require calculations of fault coverage, F_T, and test yield, Y_j, after the j^{th} test has been added to test set T. They are defined as follows:

$$F_T = \frac{1 - \int_{A_T} f(p,c)dpdc}{1 - \int_{A_S} f(p,c)dpdc}$$

$$Y_j = \frac{\int_{A_j \cap A_T} f(p,c)dpdc}{\int_{A_T} f(p,c)dpdc}$$

The algorithm developed in [1] can be applied here to find an optimal test set with minimum test time at the system level. This is summarized in the Appendix A.

2.2. Block Level Testing

Since the faulty circuits are defined as failing to meet system specifications, to go for fault-driven testing at the block level means that one needs to find the corresponding block specification, given the system specifications. Let $\phi = [\phi_1, \ldots, \phi_m]$ be the vector of m system parameters and $b = [b_1, \ldots, b_n]$ be the vector of n block parameters. Given a vector of system constraints $\phi^l \le \phi \le \phi^u$, the problem is to find the bounds, b^l and b^u such that $b^l \le b \le b^u$ is equivalent to $\phi^l \le \phi \le \phi^u$.

Due to the correlation among block parameters, the principle component method [5] is applied to the correlation matrix of normalized block parameters to find a smaller set of independent parameters which are linear combinations of normalized block parameters. The procedure is formatted as

$$b' = (V^{\frac{1}{2}})^{-1}(b - E(b))$$

where V is diagonal matrix of $\sigma_i's$, the standard deviation of the $b_i's$, and $\rho = cov(b')$, a correlation matrix for b'. Two matrices $\Lambda = diag(\lambda_i)$ and $U = [e_1, \ldots, e_n]$ are built based on the corresponding eigenvalues λ_i and eigenvectors e_i of the matrix ρ. Then the vector of principle components, C, is computed using

$$C = \Lambda^{\frac{-1}{2}} U^{-1} b'$$

The new problem becomes finding the bounds, C^l and C^u such that $C^l \le C \le C^u$ is equivalent to $\phi^l \le \phi \le \phi^u$. This transformation forms a set of hyperplane constraints for block parameters and is a difficult task due to the possible nonlinear relations between some system parameters and the principle components.

Since the determination of nonlinear relations are often too time consuming and it is difficult to find highly accurate solutions, an alternative approach to finding the constraints for block parameters is to use the designer's knowledge of the system. This approach is to start with a *sensitivity analysis* of system performances to the original block parameters, even though they are correlated, discarding some unimportant parameters to find a subset of the original block parameters. The constraints for each block parameter in the subset are determined by approximating the relation between the system performances and each block parameter, one at a time, deriving specification bounds accordingly. Since the accuracy of this approach depends heavily on the knowledge of the system, in order to substitute testing at the system level with block level tests derived by this methodology, the accuracy of the block tests must be carefully checked by comparing the fault coverage of this method with the fault coverage of system tests. Furthermore, in order for block testing to work, faults between blocks must be much less significant than faults within blocks.

3. Parametric Variation Modeling

Parametric variation can be categorized as wafer to wafer, interdie and intradie variations [6] and also is generally assumed to be normally distributed since most global process variations come from many independent steps in the process. If we neglect wafer to wafer variations, this is a two-level model, shown in Figure 1, and the i^{th} parameter of the k^{th} devices in an arbitrary die is modeled as

$$P_{ik} = u_i + \xi_i \sigma_i + \eta_{ik}\sigma_{ik}$$

where $i = 1, \ldots, n$ are the indices of the n process or device parameters, $k = 1, \ldots, m$ are the indices of the m devices in the circuit, σ_i is interdie standard deviation for the i^{th} parameter, σ_{ik} is the intradie standard deviation for i^{th} parameter of k^{th} device, and ξ_i and η_{ik} are random numbers ($\in N(0,1)$).

Since interdie variables are the same on a chip, the mismatch between the i^{th} parameter of devices k and m is modeled simply by

$$M_{ikm} = \eta_{ik}\sigma_{ik} - \eta_{im}\sigma_{im}$$

Note that while there are $\binom{m}{2}$ possible mismatches, M_{ikm}, for the i^{th} parameter, mismatch is completely modeled by only m random variables, η_{ik}.

This model can incorporate the observed dependence of mismatch on device area [7] by including an area dependence in the constants, σ_{ik}. It can not include the effect of spacing on mismatch that has been observed in [8]. In order to include a spacing dependence, the model for the i^{th} parameter needs to be modeled by $m-1$ more random variables, η_{ij}, $j = m+2, \ldots, 2m$, as follows [9]

$$P_{ik} = u_i + \xi_i\sigma_i + \eta_{ik}\sigma_{ik} + \sum_{j=m+2}^{m+k} \eta_{ij}\sigma_{ijk}$$

where σ_{ijk} are constants modeling the dependence of mismatch on device spacing and ξ_i, η_{ik}, η_{ij} are all random numbers ($\in N(0,1)$). Consequently the variance of P_{ik} is

$$\sigma_i^2 + \sigma_{ik}^2 + \sum_{j=m+2}^{m+k} \sigma_{ijk}^2$$

where σ_{ik}^2 and $\sum_{j=m+2}^{m+k}\sigma_{ijk}^2$ model the area dependence and the spacing dependence of mismatch respectively for the k^{th} transistor.

In order to perform statistical system simulation, we build regression relations between the block parameters ,b_i, and the primary independent statistical variables, ξ_i and η_{ik}. Note that some independent variables are included in more than one block , namely ξ_i and η_{ij}, $j = m+2, \ldots, 2m$, and others are unique to each block, namely η_{ik}, $j = 1, \ldots, m$. In fact, η_{ij}, $j = m+2, \ldots, 2m$, model the impact of block parameter on yield. Furthermore all the parameters η_{ij} model mismatch between blocks, and in general the same regression equation can not be used to model identical blocks because the constants, σ_{ijk}, will be different for different blocks. However if blocks are defined so that mismatch between devices in different blocks is of minimal importance, then the same regression equations can be uesd for identical blocks.

Finally, it needs to be pointed out that the parametric model itself

will come from both the global defect model and some local defects, those not causing topological changes in the circuit. If a local defect impacts a parameter in the global defect model, the statistical description of these parameters can be merged, incorporating the effect of the local defect in the $\eta_{ik}\sigma_{ik}$ term in the model.

4. Catastrophic fault modeling

Unlike the parametric faults, catastrophic faults are primary due to local defects introduced in the IC manufacturing process. These defects when located in a sensitive area will result in a change to circuit topology and most likely cause a circuit to fail specification tests. Since sensitive areas, also called critical areas, are closely related to defect size as well as the physical layout, a promising methodology is to mimic the distribution of local defects using a Monte Carlo algorithm that generates defects in the layout. In this paper, VLASIC, a Monte Carlo defect simulator, was used to generate a variety of possible faults in a circuits.

The physical defects in VLASIC are implemented as missing or extra material in a given layer of a layout. The average defect density($\frac{1}{cm^3}$) is intended to be as close to realistic process conditions as possible. Typical values on the order of 10^{-1} to 1 can be found in [10]. at such a low defect density, multiple faults are unlikely to happen and a large number of samples are needed to cover the full spectrum of possible malfunctions. We deliberately increased the average density level to the order of 10 to 10^2 in order to reduce the sample size while still keeping reasonably low occurrences of multiple faults. The defect density we selected is not too far from the data revealed in [11].

The statistical data that is also needed are the size and spatial distributions of local defects. In VLASIC, the number of defects per chip is drawn from a composite negative binomial distribution and then placed uniformly within the chip. This assumption, a uniform distribution within a chip, may not be valid if the die area is so large that the phenomenon of defect clustering can not be applied within this chip. To generate a fault list for a large layout can be very computationally and memory intensive. A good way to alleviate this problem is to hierarchically decompose the system into several smaller blocks and simulate faults within each block. There can of course be defects that short together wires in different blocks. Therefore, in addition to just simulating the blocks, interface cells have to be simulated as well.

VLASIC transforms random local defects into possible shorts, opens, new devices or changes in the size of existing devices, ignoring defects that result in no topological change to the circuit. Such defects, if they have an impact on the circuit, should be included in the parametric model. Furthermore, since defects are grouped into catastrophic faults, the probability of each catastrophic faults is computed. The probability of catastrophic faults is defined as the ratio of the occurrences for each type of possible short, open, or size change, to the total number of samples(dies) processed. In the case of a gate oxide short, we use a lumped element model developed in [12] and an associated probability is also assigned to this kind of fault.

5. Experimental Results

A cyclic A/D converter [4], shown in Figure 2, is used to illustrate our fault-driven approach to analog testing. This A/D converter is divided into 4 blocks, SH1, SH2, 2X and CMP. All four blocks, contributing to a total of 37 block parameters, model several switching capacitors and an operational amplifier(op amp). A behavioral model based on these 37 parameters was built to relate system responses to block parameters. For simplicity, the same op amp, shown in Figure 3, is used in each block. The block parameters, associating with each op amp, contribute a total 24 block parameters, which are input offset, gain, transconductance, output resistance, input capacitance and output capacitance for each op amp in each block.

For this op amp, the interdie and intradie variations of 13 process and device parameters, which are W, L, N_{sub}, X_j, L_d and V_{to} for each n-channel and p-channel device plus a common T_{ox} for both n-channel and p-channel devices, are assumed to dominate the variations of the op amp outputs. This model was first proposed in [13], where each of these parameter are assumed to be independent. Our model has supplemented the original model with mismatch parameters, but for the sake of simplicity we have ignored placement dependent mismatch parameters in this study. In our investigations of this example, we have found intradie variations of $\frac{W}{L}$ and V_{to} to be dominant effects for the performances of this circuit and we incorporate them into a single variable for each device. Three different screening experiments, standard sensitivity analysis, Level III Fractional Factorial analysis and Level IV Fractional Factorial analysis, were compared and no apparent difference can be observed in the results of the three different screening experiments. For example, The screening results of *input offset* is shown in Figure 4.

$w(\,)$, the mapping functions from device and process level variables to the block level, are then built using the variables obtained from the screening experiment through the technique of regression analysis, and the regression equation for *input offset* of the op amp is shown below as an example.

$$\begin{aligned} Y_{offset} = \; & -0.000912 + 0.00706S_{10} - 0.0062S_{12} - 0.00604S_{14} \\ & +0.005967247S_9 + 0.00374926S_2 - 0.001494S_1 \end{aligned}$$

where S_i denote the normalized intradie variation resulting from V_{to} and $\frac{W}{L}$ for the i_{th} device.

The **ANOVA** table for *Input offset* is :

Source	SS	df	MS	F_{test}	F_{cri}
Model	$6.038e^{-4}$	6	$1.0064e^{-4}$	163.085	3.87
Error	$4.32e^{-6}$	7	$6.1709e^{-7}$		
Lack of Fit	$1.18e^{-7}$	3	$3.93e^{-7}$	0.501	6.26
Pure Error	$3.14e^{-6}$	4	$7.87e^{-7}$		
R^2				0.9929	0.9

If the size of transistors are scaled down, the assumption, that only two important sources of intradie variations dominate mismatch, may not be true. We need to faithfully follow our theory by screening all intradie parameters. For the catastrophic faults, it's difficult to apply the defect simulator to the whole system. Instead, the defect simulator is applied at the block level, where the result and frequence of occurrences for 10000 samples in the SH1 block is shown in the Table 1.

After information on parametric faults and catastrophic faults are obtained, the optimal test ordering algorithm is applied. The specifications for the A/D converter are offset error, gain error, maximum differential nonlinearity, maximum integral nonlinearity, full scale error and the highest noise peak. Differential non-linearity of k^{th} digit is defined as $DNL(k) = X(k) - 1LSB$, where $X(k)$ is the actual step width of k^{th} digital code. Integral non-linearity of k^{th} code is defined as $INL(k) = \sum_{i=1}^{k-1} DNL(i)$. The definitions of the remaining four specifications are shown in Figure 5.

For these specifications, an optimal test set at the system level and the corresponding fault coverages are shown in Table 2. The approach of principle component analysis at the block level was also applied and the resulting vector of principle component consists of 11 principle components $C = [C_1, C_2, \ldots, C_{11}]^T$, where each C_i is a linear combinations of the $b_i's$, $i = 1, \ldots, 37$. Through the use of stepwise regression, the constraints at the system level were transformed to block level constraints. For example, the constraint on gain error, gain error ≤ 0.4 , was transformed to a block level constraints as

$$\begin{aligned} 0.4 \geq \; & 0.1565 + 0.03482C_8 + 0.1325C_1C_2 + 0.03547C_2C_4 \\ & -0.01776C_3C_8 - 0.009136C_6^2 \end{aligned}$$

Even though the transformations can be achieved, the measurement of 37 block parameters is still too time consuming to implement. It appears to be beneficial to apply block level testing using this approach only when the number of block parameters are small or the optimized test set at the system level is too time consuming.

The obtained fault coverage of the alternative approach for block level testing to get loose specifications for block parameters is shown in Table 3. The fault coverage of principle component analysis applied at the block level is shown in Table 4.

6. Conclusion

This paper gives a thorough investigation of applying fault-driven testing for both parametric and catastrophic faults. Besides this, a novel approach to handling statistical simulation of large-scale analog circuits is presented. For the A/D converter used to illustrate the methodology, the fault-driven approach at the system level achieve significant reductions in testing time, since it was not necessary to test integral and differential nonlinearity by measuring all of the transitions. As a consequence, block testing was unable to improve this result. This may not be true for every system, and the investigation of block level testing is still very important.

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Appendix A

Let

$$A_j = \bigcap_{i \subset S-j} A_i$$

The algorithm for eliminating redundant specifications is listed below.

INPUT S (ckt specs.) and F^*(desired fault coverage)
T=0,
For each $j \in S$ {
Compute $P_j = \int_{A_j} f(p,c)dpdc$
}
While $F_j < F^*$ {
Find $argmax_j$ P_j and add it to T
Compute F_j and Y_j
}
Output T (the test set)

The algorithm for optimizing the order of tests is somewhat more complicated. See [1] , [2] for details.

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Freq.	Shorted Nodes	Group	Comment
93	(Vdd,2)(8,13)/m5 (13,8)(11,0)(0,13) (Vss,10 13,10)(7,8) (Vss,1)(vdd,2 7,8) (12,sub)(2,14)(0,10) (11,sub)(13,sub)(2,0) (10,sub)(Vdd,2 2,3) (2,12 Vss,9)(Vss,10) (Vdd,2 2,12)(6,8,9) (Vdd,2 11,12)(8,9)	Vo fixed	system outputs unaffected by parametric variation
161	(Vss,13)(2,12 13,10) (10,8)(2,12)(13,10) (3,4)(55,6)(Vss,2) (2,3,4 m2,m5)(11,12) (4,7) (6,8) (12,10) (2,11 12,10)/m9 (3,4)	Gain $\leq$ 10	system outputs unaffected by parametric variation
3	(3,55)/m1 (9,15)(0,2)	Gain $\leq$ 300 Vos $\geq$ 200 mv	large Distortion in output
8	(11,2) (11,10)	Gain $\geq$ 4500 Vos $\geq$ 20 mv	
6	(2,3)(2,3)/m5 (7,10)	Gain $\geq$ 7000 Vos $\leq$ 8 mv	
22	short bet. two polys.	Cs=0	Outputs always
24	short bet. two polys.	Cp=0	Fail spec.

Table 1. Catastrophic Faults for SH1 Block

Specifications in order of importance	Fault coverage of test combined with tests above
full scale error $\leq$ 0.5 LSB	0.928
offset error $\leq$ 1 LSB	0.990
gain error $\leq$ 0.4	1.000
peak of the highest noise $\geq$ -50dB	1.000
maximum DNL $\leq$ 1 LSB	1.000
maximum INL $\leq$ 1LSB	1.000

Table 2. System Test Set for A/D converter

Specification in order of importance	Fault coverage of test combined with tests above
input offset for each op amp $\leq \frac{1}{2}LSB$	0.709
gain for each op amp $\geq$ 1536	0.749
abs(2-abs($\frac{C_a}{C_b}$)) $\leq$ 0.0027	0.781

Table 3. Test Set for Loose Block Test

Specification in order of importance	Fault coverage of test combined with tests above
full-scale constraint	0.823
offset error constraint	0.920
gain error constraint	0.948
peak of highest noise constraint	0.948
maximum DNL constraint	0.948
maximum INL constraint	0.948

Table 4. Test Set for P.C. Method at Block Level

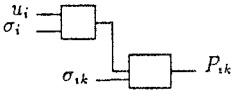

Figure 1: Two level parametric model

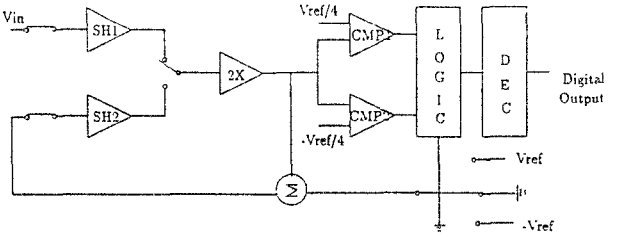

Figure 2: 1 Bit/Cycle Algorithmic A/D converter

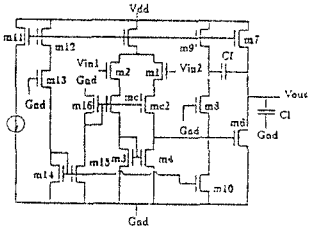

Figure 3: Two stage OP amp

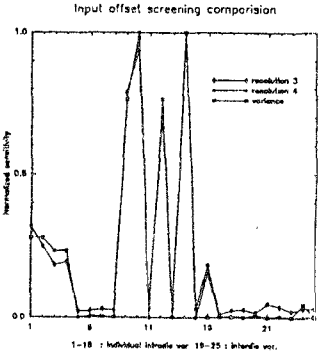

Figure 4: Screening result of input offset voltage

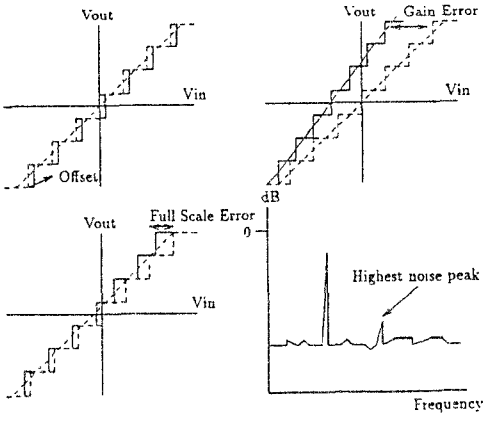

Figure 5: Specification definition