

ABSTRACT

Title of Document: AN ULTRA-LOW POWER VOLTAGE
REGULATOR SYSTEM FOR WIRELESS
SENSOR NETWORKS POWERED BY
ENERGY HARVESTING

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A DC-DC converter is an important power management module as it converts one DC voltage level to another suitable for powering a desired electronic system. It also stabilizes the output voltage when fluctuations appear in the power supplies. For those wireless sensor networks (WSNs) powered by energy harvesting, the DC-DC converter is usually a linear regulator and it resides at the last stage of the whole energy harvesting system just before the empowering sensor node. Due to the low power densities of energy sources, one may have to limit the quiescent current of the linear regulator in the sub- μA regime. This severe restriction on quiescent current could greatly compromise other performance aspects, especially the transient response.

This dissertation reports a voltage regulator system topology which utilizes the sensor node state information to achieve ultra-low power consumption. The regulator system is composed of two regulators with different current driving abilities and quiescent

current consumptions. The key idea is to switch between the two regulators depending on the sensor state. Since the “right” regulator is used at the “right” time, the average quiescent current of the regulator system is minimized, and the trade-off between low quiescent current and fast transient response has been eliminated. In order to minimize the average quiescent current of the system, nano-ampere reference current design is studied, and the proposed reference current circuit is shown (theoretically and experimentally) to reduce the supply voltage dependence by 5X.

The regulator system has been fabricated and tested using an ON Semiconductor 0.5 μm process. It has been verified through experiments that the proposed system reduces the quiescent current by 3X over the state-of-the-art in the literature; and, more importantly, it achieves low quiescent current, low dropout voltage, and fast transient response with small output voltage variation all at the same time. The thesis further presents data on the application of energy harvesting system deriving energies from various RF signals to power a commercial off-shelf wireless sensor node.

AN ULTRA-LOW POWER VOLTAGE REGULATOR SYSTEM FOR WIRELESS
SENSOR NETWORKS POWERED BY ENERGY HARVESTING

By

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This dissertation is dedicated to my family who always supports me.

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Chapter 1: Introduction

1.1 Motivation

Wireless sensor networks (WSNs) are widely used in factories, industrial complexes and urban areas to monitor environmental conditions such as structural health, traffic and temperature [1][2]. Sensor nodes of WSNs can be powered by batteries, but batteries exhibit the downsides of limited lifetime and require periodic replacement [3]. Alternatively, one can capture the energies from the environment and convert them to electrical energy to power the sensor nodes [4]. Major energy sources include solar energy [5][6], motion energy [7] and radio frequency (RF) energy [8].

An energy harvesting system is typically composed of energy capturing, energy storing and energy conditioning blocks [9]. The energy capturing block like the antenna in the RF energy harvesting system is able to capture the RF energy. Energy storing block could temporarily store the harvested energy and is often able to smooth fluctuations appeared at the energy sources. Energy conditioning block is needed in the system as it ensures proper voltage and current levels are provided for safety and efficiency considerations.

A typical RF energy harvesting system is shown as in Fig. 1 [10]. The wideband rectenna is a hybrid antenna/rectifying diode assembly which captures RF energy and converts the AC voltage into DC. The charge pump sometimes is needed as the output voltage of the rectenna is not high enough to charge the energy storage device such as a battery. The charge pump can be used to boost the voltage to a

suitable level to charge the storage device. An energy storage device (e.g., a thin film battery [11]) can temporarily store the energy when the RF power density is high and release the energy later when the RF power density is low. A DC-DC converter is often at the last stage of the whole energy harvesting system just before the empowered load, and it converts a DC voltage level to another and regulates the output voltage to be stable when fluctuations appear in the power supplies.

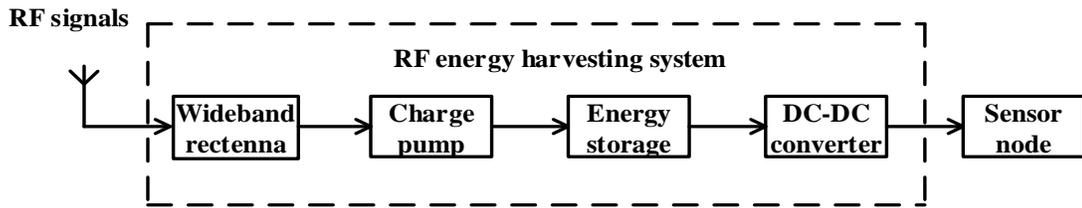


Fig. 1.1 A RF energy harvesting system block diagram [10]

Designing a DC-DC converter in an energy harvesting system is challenging because: (a) the incoming RF power density is very low. Based on the studies of [12][13][14][15], the RF power density at various locations in the world generally is within the range of a few $\mu\text{W}/\text{cm}^2$. Therefore, the power consumption of the DC-DC converter should be as low as possible that there is enough energy left for the sensor node (alternatively speaking, the power efficiency of the DC-DC converter should be as high as possible). The input voltage and output voltage of a DC-DC converter are predetermined by the system (the input voltage is determined by the battery voltage, and the output voltage is determined by the application), besides, the load current is also predetermined by the application. As a result, the only parameter one can play with to increase the DC-DC converter power efficiency is its quiescent current consumption. Considering the low power density level of the RF signals, one needs to limit the quiescent current of a DC-DC converter in the sub- μA range; and (b) a

sensor node often switches among different working modes (e.g., high power mode and low power mode) to optimize its power consumption. In those different modes, the load resistance and current are quite different (the current level may range over several orders of magnitude), and they change frequently and rapidly when the sensor node switches from one mode to another. Thus, it requires the DC-DC converter to respond fast enough with small output voltage overshoot/undershoot over an enormous current range. The circuit response is greatly affected by the quiescent current of the DC-DC converter. Therefore, low quiescent current requirement in (a) could result in a slow response speed and large output voltage variation when the load current changes.

As a result, power management issues need to be addressed carefully to make optimal usage of the harvested energy, and special attention should be taken to design an ultra-low power DC-DC converter.

1.2 An Overview of DC-DC Converters

The supply voltage might not be at the level the load expects (e.g., the supply voltage is 3 V and the load demands 1.8 V). Also, the supply voltage may not be constant and it can fluctuate. For example, when a battery discharges to power the load, its voltage gradually drops as shown in Fig. 1.2. However, the load may expect a constant stable supply voltage in order to function properly. A DC-DC converter is an important module as it produces a DC output voltage at a different voltage level than the input. Besides, a DC-DC converter can regulate the output voltage when the supply voltage fluctuates.

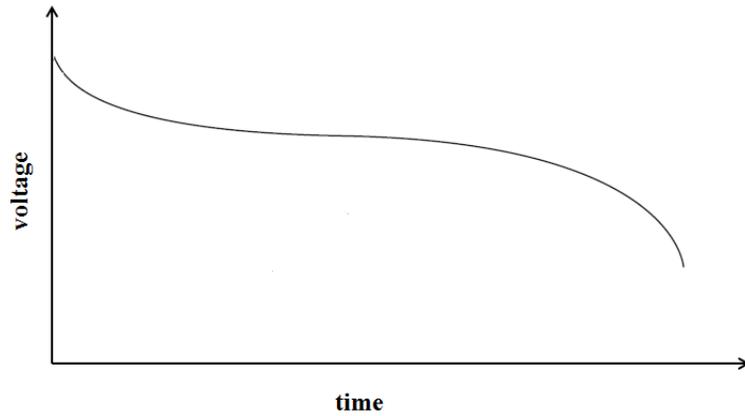


Fig. 1.2 Battery discharging profile

Typically, we can classify DC-DC converters into four categories: Zener diode regulators, linear regulators, charge pumps (switched capacitor DC-DC converters) and inductor based DC-DC switching converters.

1.2.1 Zener Diodes

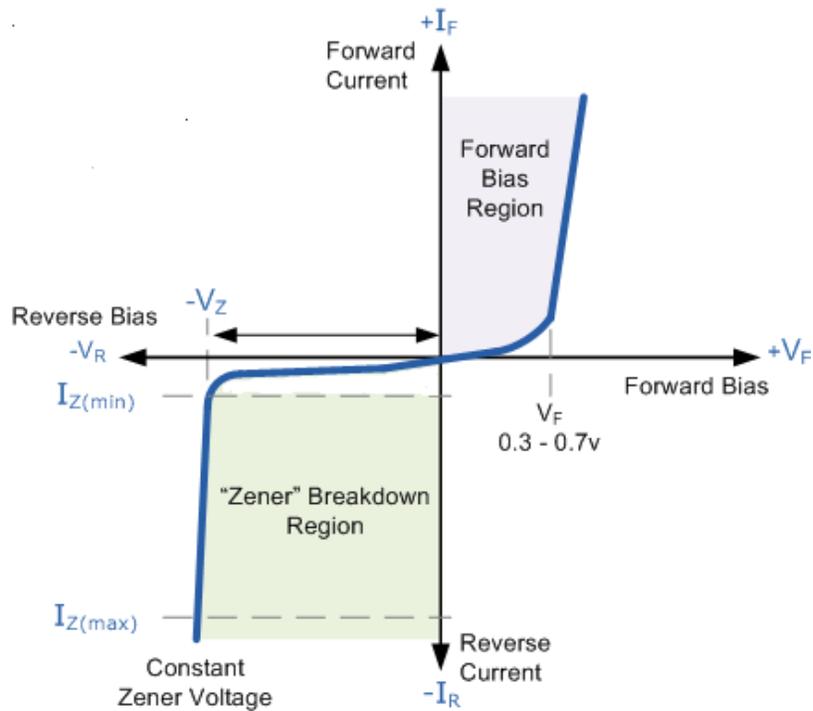


Fig. 1.3 Zener diode I-V characteristic. Adapted from [16]

For a general purpose diode, when it is forward biased, it allows the current to flow, and the current is an exponential function of the bias voltage. As we increase the magnitude of the reverse biased voltage to a certain value, the diode enters the breakdown region, and there can be large current flow in the Zener diode when it is in the breakdown region. The I-V characteristic of a Zener diode is shown as in Fig. 1.3 [16].

As shown in the I-V characteristic, when the Zener diode is in breakdown region, the reverse biased voltage across the Zener diode can stay very stable regardless that the current can change over a wide range. This property can be utilized to construct a Zener diode regulator. The Zener diode regulator is shown as in Fig. 1.4, where the Zener diode is connected in parallel with the load R_L , and the series resistor R_S is used for current limitation whose resistance selection is critical when using the Zener diode regulator. The output voltage is equal to the Zener voltage which usually has a 5% tolerance [17].

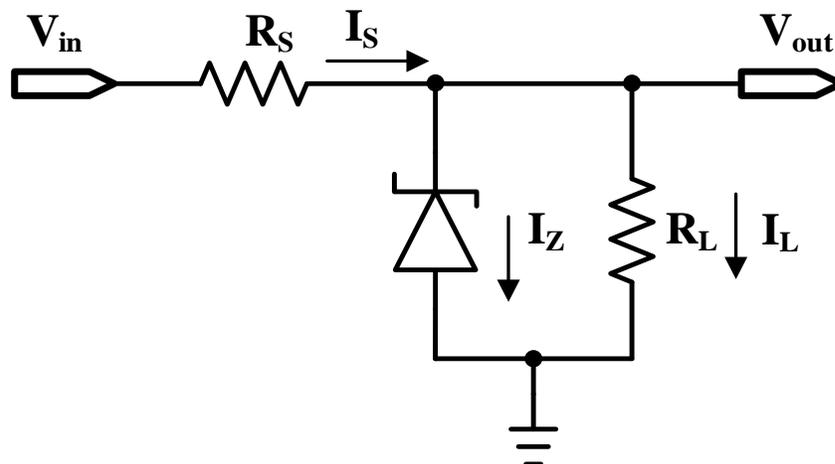


Fig. 1.4 Zener diode regulator

From the I-V characteristic, the current flowing through the Zener diode needs to stay above $I_{Z,min}$ in order to make the zener diode work in breakdown region, and this minimal current requirement dictates the maximal value of R_S allowed:

$$I_{Z,min} \leq I_Z = \frac{V_{in} - V_{out}}{R_S} - \frac{V_{out}}{R_L} \quad (1-1)$$

From equation (1-1), the maximal value of R_S is:

$$R_{S,max} \leq \frac{V_{in} - V_{out}}{I_{Z,min} + \frac{V_{out}}{R_L}} \leq \frac{V_{in} - V_{out}}{I_{Z,min}} \quad (1-2)$$

If the current flowing through the Zener diode is too large, a lot of power is dissipated and the Zener diode can get damaged due to overheat. Therefore, the value of the resistor R_S should be set to a value that the current through the Zener diode does not exceed the maximal current allowed:

$$I_Z = \frac{V_{in} - V_{out}}{R_S} - I_L \leq I_{Z,max} \quad (1-3)$$

From equation (1-3), the minimal value of R_S is:

$$R_{S,min} \geq \frac{V_{in} - V_{out}}{I_{Z,max}} \quad (1-4)$$

Therefore, the resistance value of R_S should be within the two extreme values specified above.

The Zener diode regulator is simple and easy to use. Also, it can react fast to the changes appearing at either the input voltage or the load.

Usually Zener diodes are fabricated with breakdown voltages in the range of a few volts to a few hundred volts [18], Zener diodes with very low breakdown voltages are rarely seen. For example, the lowest breakdown voltage of the Zener

diode from the electronic component distributors Digi-key and Mouser Electronics is 1.8 V [19][20]. Therefore, the uneasy access to low breakdown voltage Zener diode can sometimes limit the usage of the Zener diode regulator in a low power system.

Another problem is that the output voltage is equal to the Zener breakdown voltage and therefore cannot be easily changed and is fixed at only one of the available voltage levels.

The main problem with a Zener diode regulator is its low efficiency: at high load impedance or no load, all the current flowing through the resistor R_S also flows through the zener diode. As a result, the quiescent current at high load impedance could be very large, which is a big problem in low power systems. For example, if a Zener diode regulator is required to output a maximal current of 100 mA, then the quiescent current (i.e., the Zener diode current I_Z) at high load impedance is also 100 mA, meaning the Zener diode regulator is extremely inefficient as compared to the other three DC-DC converters. Besides, since the resistor R_S is in series, therefore, a lot of power is wasted on this resistor at high load current (i.e., light load impedance).

1.2.2 Linear Regulators

The linear regulator is like a resistive voltage divider network as shown in Fig. 1.5 [21]. The principle is to vary the regulator resistance in accordance with the load to produce a stable output voltage. The output voltage V_{out} can be expressed as

$$V_{out} = V_{in} \frac{R_L}{R_L + R_p} \quad (1-5)$$

where V_{in} and V_{out} are the input and output voltages, and R_p and R_L are the regulator resistance and load resistance. The role of the control circuitry is to sense the output

voltage change and adjust the regulator resistance correspondingly to establish a regulated output voltage.

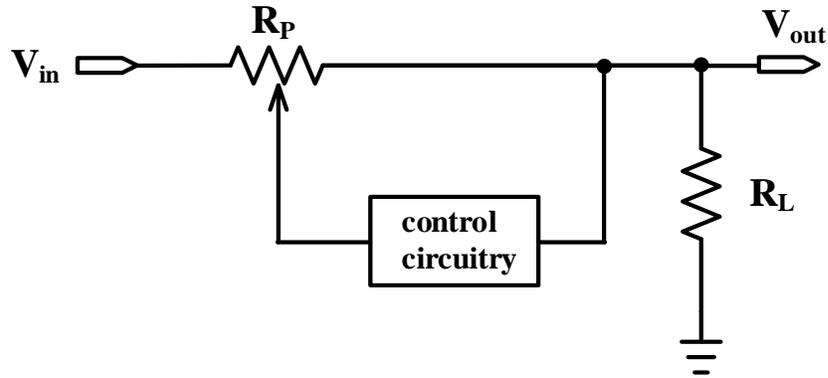


Fig. 1.5 Linear regulator operating principle [21]

The control circuitry can be implemented using a negative feedback network which compares the output voltage against the reference voltage and generates an error term. A transistor (usually called the pass element) can operate as the R_p whose resistance is controlled by the error term generated by the control circuitry. When output voltage is higher or lower than the regulated value, the feedback network senses the difference and changes the resistance of R_p to make the output voltage equal to the regulated value.

A typical linear regulator using a PMOS transistor as the pass element is shown as in Fig. 1.6. The error amplifier compares the reference voltage with a fraction of the output voltage (i.e., $\frac{R_2}{R_1+R_2}V_{out}$) and amplifies the error. The amplified error drives the gate of the pass element. If the error amplifier has an infinite gain, the output voltage is determined by the reference voltage and the ratio of the two feedback resistors R_1 and R_2 :

$$V_{out} = \frac{R_1 + R_2}{R_2} V_{ref} \quad (1-6)$$

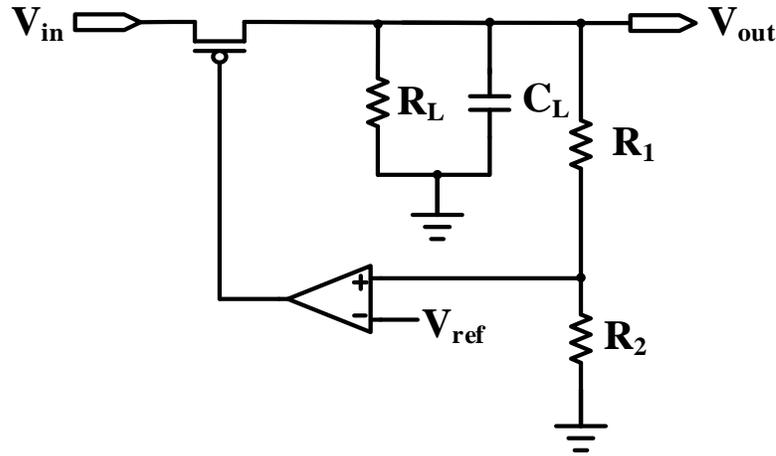


Fig. 1.6 Linear regulator structure

When the load resistance R_L changes or input voltage V_{in} varies (e.g. the voltage of the battery supply drops), the linear regulator cannot respond instantaneously to the change and a finite amount of time is needed for the regulator to achieve a regulated value again. An output capacitor is important in this transient response. For example, when the load current suddenly increases, the current from the pass element cannot change instantaneously, so the output capacitor discharges to provide the increased amount of current to the load. Similarly, when the load current suddenly decreases, the output capacitor absorbs the extra amount of current from the pass element. Therefore, the output capacitor plays an important role in resisting any output voltage change.

The power efficiency of a linear regulator is given by

$$\eta = \frac{V_{out} I_{out}}{V_{in} I_{in}} \times 100\% \quad (1-7)$$

where I_{out} is the current provided to the load and I_{in} is the current drawn from the power supply. The current drawn from the power supply is the sum of the load current and the current consumed by the linear regulator itself (i.e. the quiescent current). At high load current conditions, the load current is much larger than the quiescent current. Therefore, I_{in} is close to I_{out} and the above equation can be approximated as

$$\eta_{\max} = \frac{V_{out}}{V_{in}} \times 100\% \quad (1-8)$$

For a linear regulator, V_{out} is always smaller than V_{in} . Since the pass element is in series with the output load, the power efficiency usually is not high [22]. To improve the power efficiency, we want V_{out} to be as close as possible to V_{in} . When the input voltage is much larger than the output voltage, lots of power is wasted on the pass element.

For a battery powered system, a main goal is to improve the operation time of the battery. Consequently, current efficiency is also important in those systems. For a linear regulator, as stated before, the load current could be much larger than the quiescent current, especially at high load current conditions. Therefore, the current efficiency of a linear regulator can be very high and this makes linear regulators very attractive in those battery powered systems. Also, a linear regulator does not require any inductor, which is bulky and expensive [23]. Besides, linear regulators usually have smaller noises and better power supply rejection, this property makes them widely used in sensitive RF blocks [24].

1.2.3 Charge Pump DC-DC Converters

Charge pump DC-DC converters (also called switched capacitor converters) use capacitors to store energy temporarily and then release energy to the output [25]. There exist several different charge pump topologies [26][27]: such as Doubler, Dickson charge pump, Cockcroft-Walton charge pump, etc.

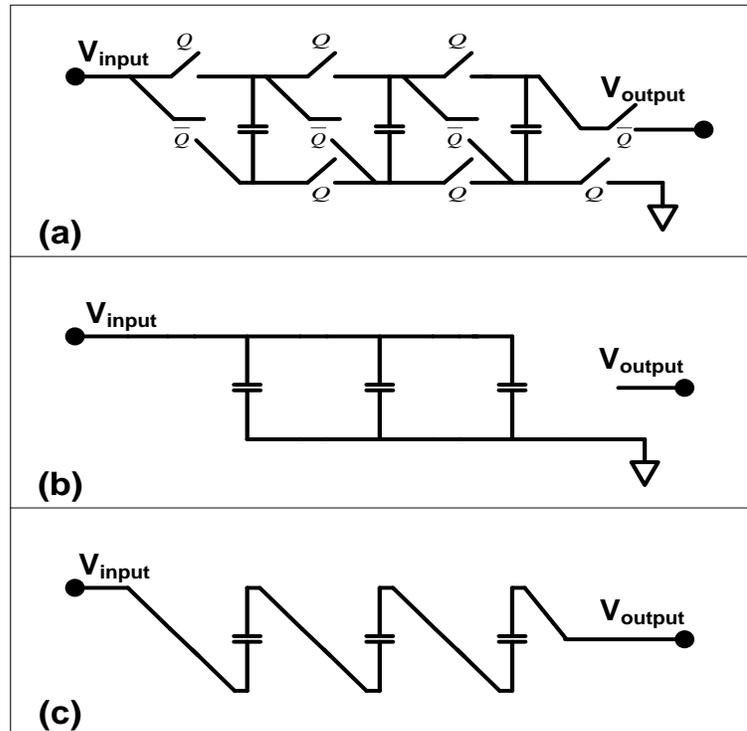


Fig. 1.7 Operation of a charge pump DC-DC converter. Adapted from [10]

Taking the Cockcroft-Walton charge pump of [10] as an example, the operating principle can be explained using the circuit shown in Fig. 1.7. As shown in Fig. 1.7 (a), this charge pump circuit is mainly composed of capacitors and two groups of switches controlled by two complementary signals Q and \bar{Q} (the output capacitor is not shown). In the first phase as shown in Fig. 1.7 (b), $Q=1$ and $\bar{Q}=0$, so the top plates of all the capacitors are connected to the input, and the bottom plates

are connected to ground. Therefore all the capacitors are being charged to the same voltage. In the second phase as shown in Fig. 1.7 (c), $Q=0$ and $\bar{Q}=1$, the capacitors now are connected in series so that the output voltage is boosted a higher level than the input.

For the charge pump discussed above, it is able to convert a DC voltage level to another, but the output voltage is a multiple of the input (i.e. output changes as input voltage changes). To make a charge pump regulating the output voltage, one needs to use feedback control. Generally, we can classify the control schemes into two categories [28]: constant frequency regulation and variable frequency regulation.

There are mainly three control schemes in the constant frequency regulation category [28]: voltage mode control, current mode control and pulse width modulation. For the voltage mode control, a sense amplifier compares the output voltage with the reference, and the error signal is amplified to control the on-resistance of a single or multiple switches. For the current mode control, in contrast, the error signal controls the current flowing through the switch. Different from the voltage mode control and current mode control, in which the duty cycles of the frequency signals are fixed at 50%, the pulse width modulation method dynamically adjusts the duty cycle to control the energy delivered to the load.

For the variable frequency control, one can either do pulse skip regulation or linear skip control [29]. In pulse skip regulation, the output voltage is regulated by skipping unuseful pulses [28]. For example, if the output is smaller than the regulated value, the charge pump works and charges the output capacitor. Otherwise, the charge pump stops operation. In linear skip regulation, there are three phases: charge phase,

transfer phase and wait phase. In the wait phase, all the switches are open and the output capacitor discharges to the load. When the load current is high, the charge pump works in linear mode and the current transferred per cycle is regulated. When the load current is low, the charge pump works in skip mode and the wait phase is regulated while the current is fixed [28].

The charge pump with unregulated output voltage can have high efficiency, but when the output needs to be regulated, the efficiency drops. Charge pump DC-DC converters mainly use transistors and capacitors, so they are economically more efficient than the inductor based DC-DC switching converters and allow easier integration [30]. As compared to linear regulators, due to the pulsing feature, charge pump DC-DC converters tend to be more noisy.

1.2.4 Inductor Based Switching Converters

Similar to charge pump DC-DC converters, an inductor based switching converter is also a switched mode converter, but it incorporates inductor. An inductor based DC-DC switching converter works by periodically storing energy in the inductor and then releasing it to the load. It can step up the voltage (i.e., boost converter), step down the voltage (i.e., buck converter) or step down/step up the voltage (i.e., buck-boost converter).

A buck converter topology is shown as in Fig. 1.8 [31], where M_P and M_N are PMOS and NMOS switches which are controlled by the switch signal S . Inductor L and capacitor C form the filter network and R is the load. When S is at low voltage, M_P turns ON and M_N is OFF, the power source delivers energy to the load through the inductor. The inductor stores energy and its current rises linearly. When S is at

high voltage, M_P is open and M_N closes, now the inductor, capacitor and the load form a loop. The inductor releases its stored energy to the load and its current drops. Depending on whether the inductor current can reach zero or not, a buck converter can work in three modes: continuous current mode (CCM), discontinuous current mode (DCM), and pseudo continuous current mode (PCCM) [32].

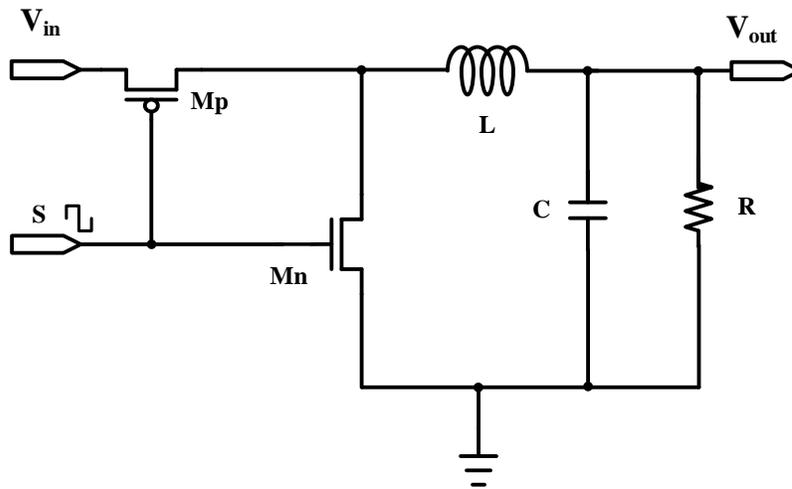


Fig. 1.8 A buck converter topology

Fig. 1.9 shows the inductor current waveforms in CCM and DCM. In CCM, the inductor current always stays above zero. In DCM, the current goes to zero in part of the cycle. PCCM is an operation between CCM and DCM.

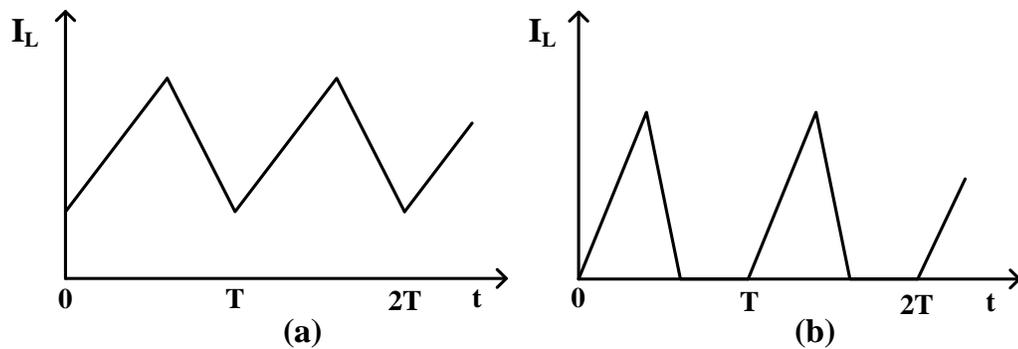


Fig. 1.9 Inductor current waveforms of a buck converter in (a) CCM (b) DCM

If one defines duty cycle D as the ON time of switch M_p over the period, the output voltage of a buck converter working in CCM can be expressed as [33]:

$$V_{out} = DV_{in} \quad (1-9)$$

The circuit shown in Fig. 1.7 only shows the power stage, to achieve a stable output voltage, one still needs feedback control. A voltage mode circuit adopting pulse width modulation (PWM) control is shown in Fig. 1.10. The error amplifier compares the sensed output with the reference voltage and generates an error voltage. The PWM comparator compares the error voltage with the sawtooth signal to generate a pulse signal with a fixed frequency but modulated width.

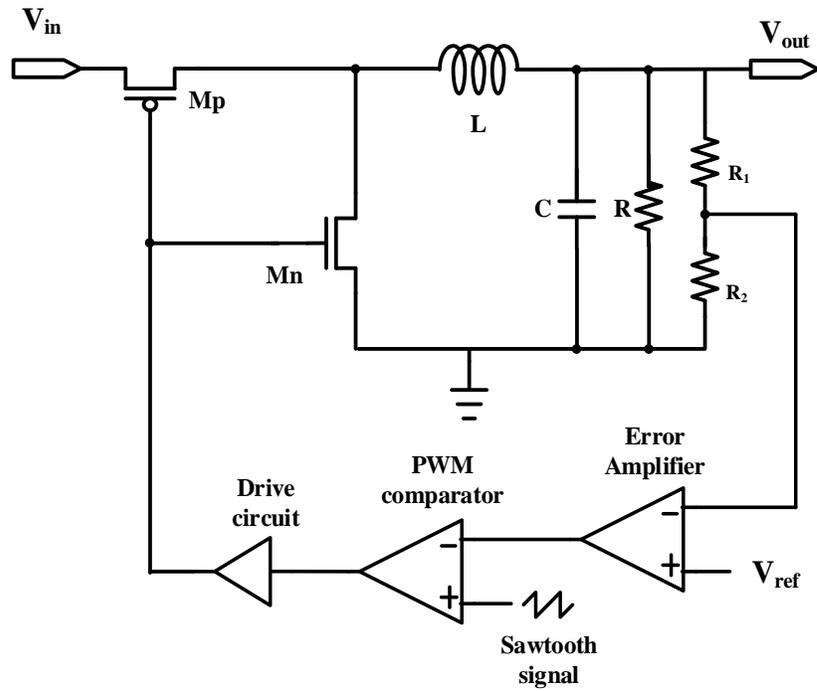


Fig. 1.10 A voltage mode buck converter with PWM control

The capacitor voltage at the beginning of each cycle is equal to its voltage at the end of the cycle, same is true for the inductor current. Therefore, the capacitor and inductor dissipate no energy if ignoring the parasitics. The main power losses of an

inductor based switching converter include switching loss, conduction loss, shoot through loss (dead-time loss), etc [34].

When the switches are switched ON and OFF when an inductor based switching converter works, there is switching loss because power is dissipated to charge the capacitances. The switching power loss $P_{sw} \propto CV^2f_{sw}$. The switches are non-ideal and they have ON resistances. Also, the inductor and capacitor have parasitic resistors. Therefore, power is dissipated on those resistors when current flows. Hence, the converter has conduction loss. Ideally, the two switches work out of phase, i.e., when one is ON, the other is OFF. However, the two switches may not be perfectly synchronized, and there is a chance that the two switches can be ON simultaneously. When the two switches are both ON, they “short” the power supply to ground, which results in shoot through loss [35].

Generally, the efficiency of an inductor based switching converter is a function of the load current, and one of the power losses can dominate the others. Fig. 1.11 shows an example of the efficiency as a function of the load current [35]. At high load currents, the main power loss is the conduction power loss. At light load current conditions, a main component of the power losses is shoot through loss. At very light load current, the switching loss becomes dominant. Even though there exist various different kinds of power losses, an inductor based switching converter can still achieve high power efficiency [36].

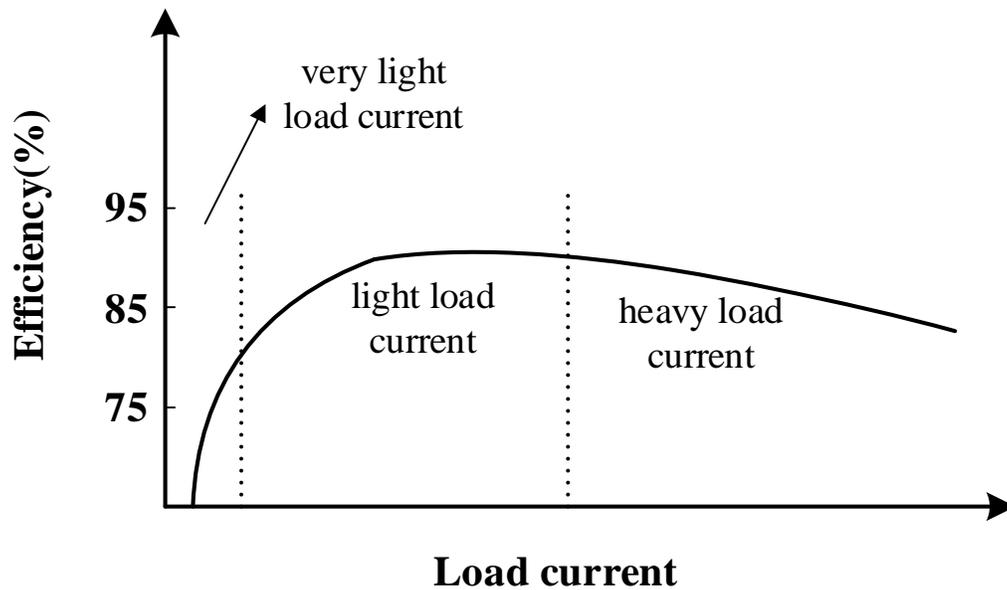


Fig. 1.11 Power efficiencies as a function of load current [35]

One of the main problems with an inductor based switching converter is that circuit is bulky and has high cost since an inductor needs to be involved. Besides, the circuit also has high noise due to the switching behavior of the circuit.

1.2.5 Comparison of the DC-DC Converters

We have discussed the structures and operating principles of four different DC-DC Converters. Advantages and disadvantages of them are summarized in Table 1.1. In summary, a Zener diode regulator is very simple but very inefficient. Linear regulator has low noise and good PSRR performance, therefore it is a good choice to regulate the voltage at sensitive conditions, even though it is not the most efficient. Inductor based switching converter is the most efficient, but it is bulky and noisy. Charge pump has average performance in almost all the aspects.

Table 1.1 A comparison of the four DC-DC converters

Zener diode	Linear regulator	Charge pump	Inductor based
very simple (+)	low noise (+)	relatively simple (+)	high efficiency (+)
easy to use (+)	large PSRR (+)	not very efficient(-)	bulky (-)
fast (+)	not very efficient(-)	noisy (-)	high cost (-)
very inefficient (-)			high noise (-)

1.3 Contributions of This Work

A DC-DC converter often resides at the last stage of the whole energy harvesting system just before the empowering load, and it provides a stable output voltage to the load despite the change in the input voltage or load resistance. This work focuses on designing a voltage regulator for wireless sensor nodes powered by harvesting energies from the environment. Since the power levels of the energy sources are low, one needs to minimize the power consumption of the linear regulator.

A summarization of the contributions of this work is listed as follows,

1. Reviewed and analysed various DC-DC converter structures (Zener diode regulator, linear regulator, charge pump and inductor based switching converter) and operating principles, compared the strengths and weaknesses of each structure. Justified the reason why linear regulators are chosen to regulate the supply voltage to the sensor node. Provided a detailed tutorial on the performance metrics of a linear regulator.

2. Researched the challenges of designing a linear regulator in an energy harvesting system powering the wireless sensor node. Proposed and established an ultra-low power voltage regulator system topology which utilizes the sensor node state information to help us to achieve both ultra-low quiescent current and fast transient response with small output voltage variation. Discussed and explained the system control methodology. Examined the potential implementation problems and proposed solutions to those problems. Discussed and analysed the power consumption benefit of the proposed system.
3. Designed and implemented the composing linear regulators and switches of the voltage regulator system. Proposed the buffer structure used for the linear regulator which reduces the dropout voltage by 500 mV. Studied and analysed system stability and frequency compensation techniques. Performed system stability simulations.
4. Fully studied and improved the self-biasing current reference circuits. Discovered the existence of an oscillation problem associated with the commonly used reference circuit and identified the problem in real circuits. Improved the pure CMOS nano-ampere reference circuit and proposed a supply insensitive nano-ampere reference current generator which reduces the supply sensitivity by 5X.
5. Designed the regulator system and performed simulations in Cadence Virtuoso. Fabricated and taped out the system using an ON Semiconductor 0.5 μm process. Measured system quiescent current, dropout voltage, line

transient response, load transient response, etc. Verified the system is capable of achieving low quiescent current (3X smaller than state-of-the-art), low dropout voltage, good transient response all at the same time.

6. Tested the rectenna harvesting energy from various RF signals in the environment. Configured and integrated the RF energy harvesting system. Performed experiments with the whole energy harvesting system and demonstrated that the system is capable of powering a commercial wireless sensor node product.

1.4 Summary

DC-DC converters serve important roles as power management modules. In those energy harvesting systems, one needs to pay special attention to make the best use of the power. This chapter briefly reviewed various kinds of DC-DC converters and their advantages and disadvantages are also discussed.

Due to its low noise and high power supply rejection ratio, linear regulators excel other DC-DC converters when regulating voltages for sensor nodes which have sensitive RF blocks. In the following chapters, this work is going to focus on linear regulators. More specifically, Chapter 2 is going to discuss the challenges facing a linear regulator design; and Chapter 3 presents our voltage regulator system topology and discusses control methodology; Chapter 4 shows the circuit designs and implementations; Chapter 5 presents the experimental results of the proposed voltage regulator system; Chapter 6 presents results of an RF energy harvesting system. Chapter 7 concludes the work.

Chapter 2: Linear Regulator Performance Metrics and Design Challenges

2.1 Introduction to Linear Regulator Design

A linear regulator is mainly composed of the following blocks: an error amplifier, a pass element and a feedback network. A classical linear regulator structure is shown as in Fig. 2.1 [37].

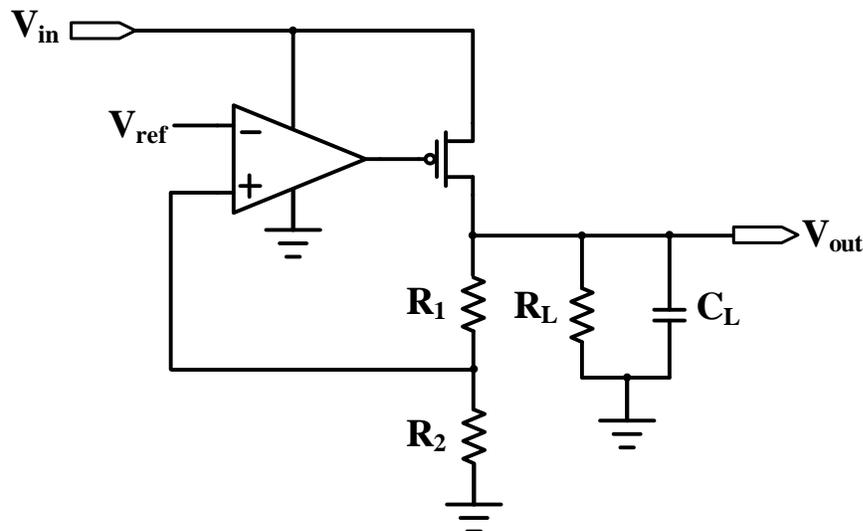


Fig. 2.1 Classical linear regulator structure [37]

When the output voltage changes due to the change in the input voltage or the load current, the error amplifier senses any change at the output and generates an error signal. This error signal adjusts the gate voltage of the pass element so that a stable output voltage can be retained.

For this linear regulator circuit, usually it has at least two poles: one located at the output of the circuit, and the other at the output of the error amplifier. These two poles might lead the whole circuit to be unstable. Therefore, besides the error

amplifier, pass element and feedback network blocks, the circuit often has some frequency compensation network to insure system stability.

In addition to those main blocks, a linear regulator also requires reference generator, startup circuit, etc. In some applications, due to safety considerations, some linear regulators also include over current protection and thermal shut down to avoid thermal damage [38].

2.2 Performance Metrics

There are several important parameters associated with a linear regulator when speaking about its performance. Some of the main parameters include dropout voltage, quiescent current, line regulation, load regulation, transient response, power supply rejection, etc [39].

2.2.1 Quiescent Current

The current flows in a linear regulator are shown as in Fig. 2.2 [40]. The quiescent current I_q is the difference between the input current I_{in} and the output current I_{out} . This current denotes the current drawn from the power supply when there is no load.

One can define the current efficiency as

$$\text{Current Efficiency} = \frac{I_{out}}{I_{out} + I_q} * 100\% \quad (2-1)$$

The quiescent current is composed of the reference current, the tail current of the error amplifier and the current flowing through the feedback resistors, etc. At large load current conditions, the quiescent current is much smaller than the output current, so the regulator has a high current efficiency. But at small load currents, the

quiescent current might become a large portion of the total input current, and therefore the current efficiency in this condition is low. A special case is when there is no load (i.e., $R_L = \infty$), the current efficiency is zero and the input current is equal to the quiescent current.

For those battery powered systems, it is important to maximize the current efficiency. As a result, one needs to reduce the quiescent current of the linear regulator. But there is a tradeoff with the quiescent current and other performance parameters, which would be discussed later in this chapter.

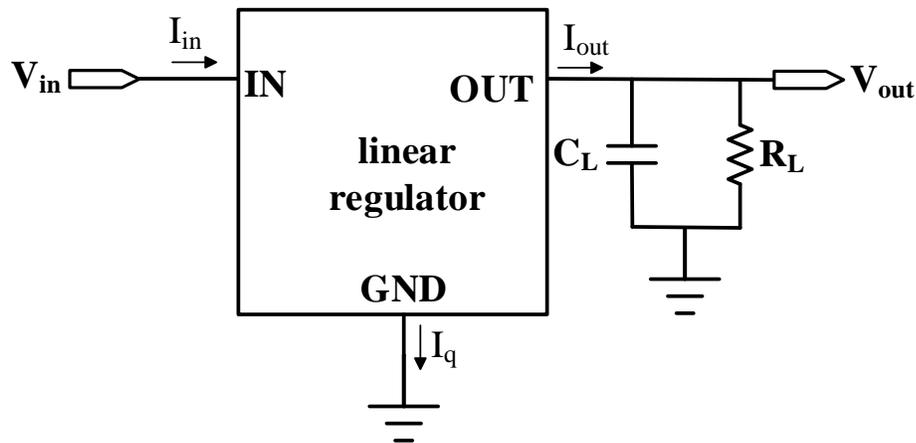


Fig. 2.2 Current flows in a linear regulator

2.2.2 Dropout Voltage

For a regulator, it can only regulate the output voltage for a specific working region. The dropout voltage is defined as the difference between the input voltage and output voltage when the regulator starts to fail regulating [40].

Fig. 2.3 shows the operation regions of a linear regulator [40]. As the input voltage decreases and approaches the output voltage, there exists a critical point where the linear regulator leaves the regulation region and starts to fail to regulate the

output. The voltage difference between the input and output at this critical point is called the dropout voltage. Below this point (i.e., the input voltage continues decreasing), a stable output voltage cannot be maintained anymore and the output voltage drops as the input voltage decreases. This region is called the dropout region. If the input voltage continues decreasing, finally the linear regulator enters the off region and the output voltage drops to zero. Apparently, a small dropout voltage is desirable.

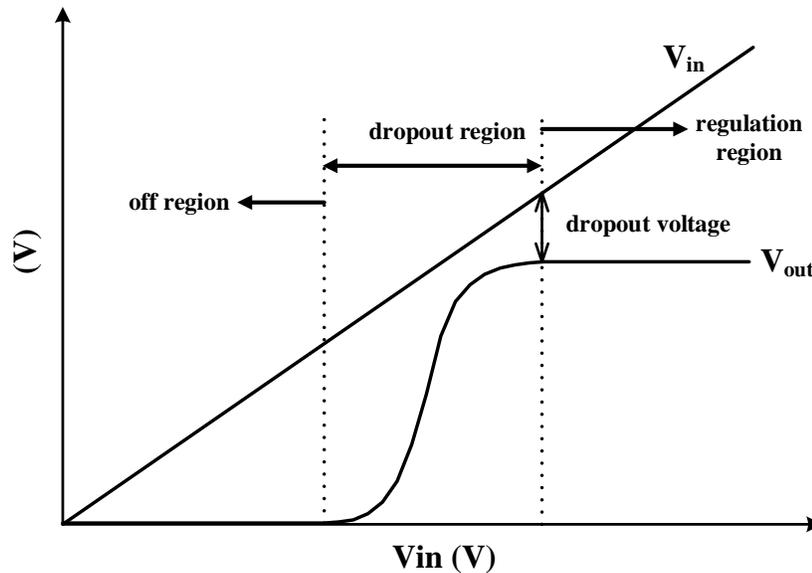


Fig. 2.3 Operation regions of a linear regulator

The main reason why a linear regulator leaves the regulation region and enters the dropout region as the input voltage decreases is because the pass element changes from saturation region into triode region [39]. This can be better explained by studying the I-V characteristic of the pass element.

Both PMOS and NMOS could be used as the pass element, and each one has its advantages and disadvantages, which are going to be discussed later. Here we

choose NMOS as the pass element due to the simplicity of explaining the working of a liner regulator. The I-V characteristic of an NMOS is shown as in Fig. 2.4.

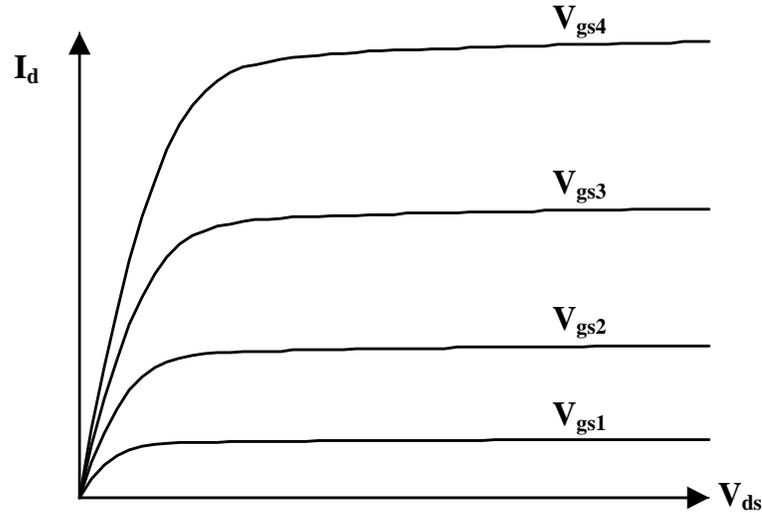


Fig. 2.4 NMOS I-V characteristic

When the drain source voltage of an NMOS is larger than its gate source voltage, i.e., $V_{ds} > V_{gs} - V_{th}$, it operates in saturation region and its drain current I_d is controlled by the gate source voltage. If ignoring the channel length modulation effect, the current is given by $I_d = \frac{1}{2}\mu_n C_{ox}(V_{gs} - V_{th})^2$, where μ_n and C_{ox} are the electron mobility and oxide capacitance. This drain current flows to the load. When the input supply voltage changes (e.g. the battery discharges), since the load current is independent on the drain source voltage as long as the NMOS is in saturation, so the load current does not change when the battery discharges, and the output voltage stays being regulated. When the battery discharges to a point where the drain source voltage of the pass element is smaller than its gate source voltage, i.e., $V_{ds} < V_{gs} - V_{th}$, the pass element works in triode region and its current is given by $I_d =$

$\mu_n C_{ox} [(V_{gs} - V_{th})V_{ds} - \frac{1}{2}V_{ds}^2]$. The drain source voltage could be expressed as $V_{ds} = V_{battery} - V_{out}$ where $V_{battery}$ and V_{out} are the battery supply voltage and the regulator output voltage. Since now the load current depends on the difference of the battery voltage and the output voltage, the output current and output voltage cannot be kept stable as the battery keeps discharging. Hence, regulator enters the so called dropout region.

Dropout voltage V_{DO} is an important performance characteristic of a linear regulator, and it denotes the amount of voltage that the input needs to be higher than the regulated output; therefore, a small dropout voltage is always desired. Besides, the maximal power efficiency of a linear regulator is also a function of the dropout voltage. The power efficiency can be expressed as [41]

$$\eta = \frac{V_{out} I_{out}}{V_{in} I_{in}} = \frac{V_{out} I_{out}}{V_{in} (I_{out} + I_q)} \quad (2-2)$$

Usually the quiescent current is small and the maximal power efficiency can be achieved is approximated as

$$\eta_{max} = \frac{V_{out} I_{out}}{V_{in} I_{out}} = \frac{V_{out}}{V_{in}} \leq \frac{V_{out}}{V_{out} + V_{DO}} \quad (2-3)$$

Thus, specifying the regulated output voltage and the dropout voltage requirements, one can estimate the maximal power efficiency the linear regulator can achieve. Therefore, reducing the dropout voltage also improves the regulator power efficiency.

2.2.3 Load Regulation

Ideally, the output voltage is independent on the load current. In reality, because of the finite gain of the error amplifier, the output voltages at different load currents are different, even though the difference is subtle. Load regulation denotes the output voltage change at a given load current change, and it can be expressed as

$$\text{Load Regulation} = \frac{V_{out1} - V_{out2}}{I_{out1} - I_{out2}} \quad (2-4)$$

where V_{out1} is the output voltage at load current I_{out1} , and V_{out2} is the output voltage at load current I_{out2} . Sometimes the load regulation in equation (2-4) is normalized by the regulated output voltage $V_{out,norm}$ and we have the normalized load regulation:

$$\text{Normalized Load Regulation} = \frac{V_{out1} - V_{out2}}{I_{out1} - I_{out2}} \times \frac{1}{V_{out,norm}} \times 100\% \quad (2-5)$$

Load regulation is an important measure of how “well” the regulator could maintain its constant output voltage when the load changes. Load regulation is a steady state parameter and increasing circuit open loop gain improves load regulation [39].

2.2.4 Line Regulation

Line regulation measures the output change with the input change, and it denotes the capability of a regulator to maintain a constant output when the input varies. Line regulation can be given by the following equation

$$\text{Line Regulation} = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} \quad (2-6)$$

where V_{out1} is the output voltage at load current V_{in1} , and V_{out2} is the output voltage at load current V_{in2} . Sometimes line regulation in equation (2-6) is normalized by the regulated output voltage $V_{out,norm}$ and the normalized line regulation is

$$\text{Normalized Line Regulation} = \frac{V_{out1} - V_{out2}}{V_{in1} - V_{in2}} \times \frac{1}{V_{out,norm}} \times 100\% \quad (2-7)$$

The normalized line regulation defined in equation (2-7) measures the percentage change of the output voltage at a given input change.

2.2.5 Power Supply Rejection Ratio

Quiescent current, dropout voltage, line regulation and load regulation are all DC parameters, and they measure a linear regulator's steady state performance. Power supply rejection ratio (PSRR) measures how well a linear regulator rejects ripples (i.e., small AC signals) from the power supply and is an AC parameter. It denotes a regulator's ability to provide a stable output voltage when the input voltage varies. PSRR is defined over all frequencies and can be expressed in the following equation with units of dB [40]:

$$PSRR = 20 \log \frac{V_{out,ripple}}{V_{in,ripple}} \text{ at all frequencies} \quad (2-8)$$

The small signal model of the output voltage variation due to the supply ripple is shown as in Fig. 2.5. The output ripple can be expressed as a function of the input ripple [42]:

$$v_{out} = \left[\frac{1 - A_p}{A\beta} + \frac{1}{g_{mp} R_{pass}} \cdot \frac{1}{A\beta} \right] v_{in} \quad (2-9)$$

where v_{out} is the output ripple due to the supply ripple v_{in} , A_p is the pass element gain of its gate voltage to its source voltage, i.e., $A_p = \frac{v_p}{v_{in}}$, A is the open loop gain of the error amplifier, β is the feedback ratio, i.e., $\beta = \frac{R_2}{R_1+R_2}$, g_{mp} and R_{pass} are the transconductance and resistance of the pass element, respectively.

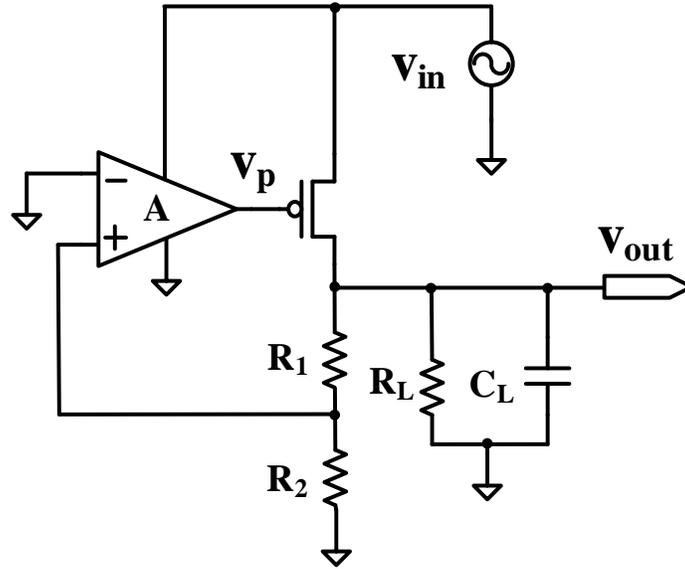


Fig. 2.5 Small signal of PSRR analysis

Having the output ripple expressed in input ripple, the PSRR can be written as

$$PSRR = 20 \log \left[\frac{1 - A_p}{A\beta} + \frac{1}{g_{mp} r_{pass}} \cdot \frac{1}{A\beta} \right] \quad (2-10)$$

The PSRR can be measured using the summing node methods [43]. One basic way to measure PSRR is to generate a DC voltage and an AC voltage, then sum them up together, and then apply them to the input of the linear regulator. The setup is shown as in Fig. 2.6, where the inductor L blocks the AC component of the power supply but allows its DC component to pass. The capacitor C blocks the DC component of the signal generator but allows its AC component to pass. As a result,

the DC component of the power supply and the AC component of the signal generator are summed up and applied to the input of the linear regulator.

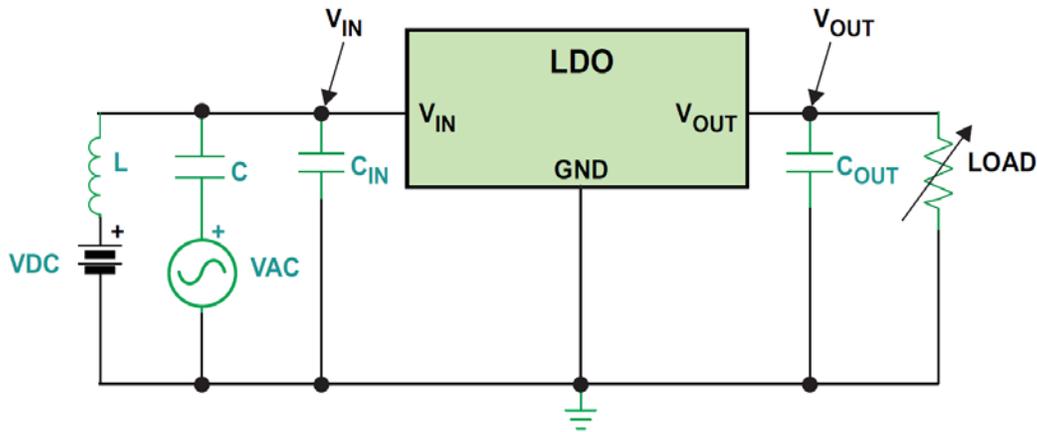


Fig. 2.6 One basic way to measure the PSRR. Adapted from [43]

One main problem of this method is that the LC circuit creates a high pass filter. Therefore, very low frequency signal from the signal generator would be filtered out, which can impose a limit on which the lowest frequency can be [43]. It is recommended that one use an amplifier as the summing node as shown in Fig. 2.7. At high frequencies, the response of the amplifier start to affect the measurement as its gain drops. Therefore, the magnitude of the input AC signals to the input of the linear regulator drops, even though the AC signal from the signal generator stays the same. As a result, a high bandwidth amplifier is desirable.

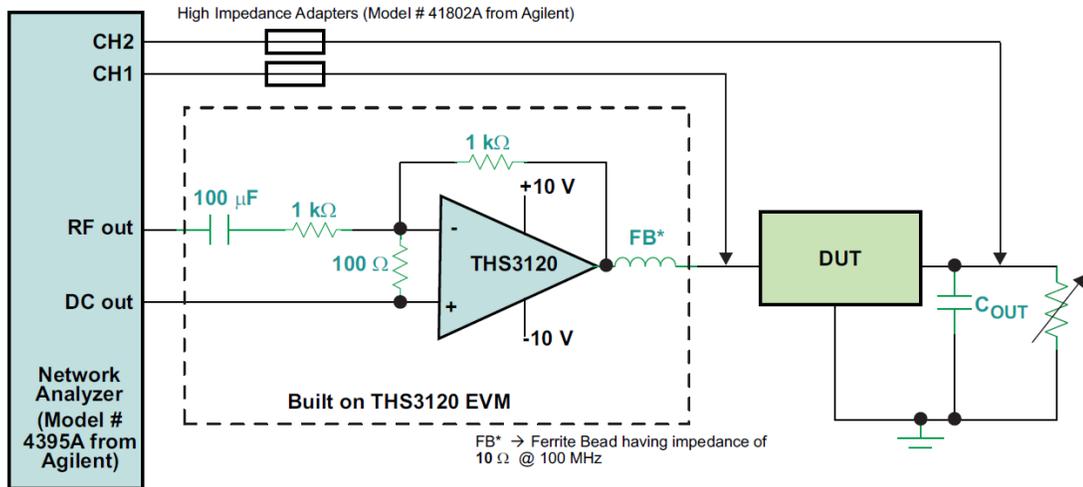


Fig. 2.7 An improvement on the way of measuring the PSRR. Adapted from [43]

2.2.6 Transient Response

For an application where the load current changes frequently, minimizing the output voltage change is very important. As for the WSNs, a sensor node usually switches among several different working modes. For example, in the high power mode, the sensor node needs to collect data from the surrounding environment or communicate with other sensor nodes within the network; in the low power mode, it could go to sleep to save power. The load current changes when the sensor node switches from one mode to another, and the linear regulator is expected to produce a stable output voltage with small variation and minimize voltage undershoot/overshoot during the transition.

The output capacitor plays an important role in improving the transient response and reducing the voltage undershoot/overshoot. When the load current suddenly drops, the drain current of the pass element cannot be adjusted instantaneously. Before the drain current of the pass element accommodates the load current, the output capacitor absorbs some of the current from the pass element and

the capacitor voltage increases. The error amplifier senses this output voltage change and adjusts the gate voltage of the pass element to decrease its drain current to establish a steady state again. The output capacitor helps to avoid a sharp increase in the output voltage as it absorbs the transient current when the load current suddenly drops. Similarly, when the load current suddenly increases, the output capacitor discharges and helps to reduce the output voltage undershoot.

The output capacitor is also important when the supply voltage changes. For example, when the supply voltage suddenly increases, the gate voltage of the pass element cannot be adjusted instantaneously. The output capacitor absorbs the transient current from the pass element and helps to reduce the overshoot.

2.2.7 Miscellaneous: Line Regulation, PSRR and Line Transient Response

Line regulation, PSRR and line transient response all measure how a linear regulator reacts to an input voltage change, but they are measurements of different aspects of a linear regulator.

Line regulation is a steady state parameter without any frequency components, and it measures how much the output voltage changes with an input voltage change in a DC sense. Therefore, it is a DC parameter. PSRR measures how well the linear regulator rejects small AC signals of the input at each frequency value of interest. Therefore, it is an AC parameter. The primary interest of analyzing the line transient response is to study the output voltage when applying to a step signal to the input. From the Fourier transform theory, a step signal can be converted to a bunch of frequencies signals as shown in Fig. 2.8. Therefore, PSRR and line transient response

are strongly related. But these two parameters are not the same, as PSRR is based on small signal analysis and line transient response is based on large signal analysis.

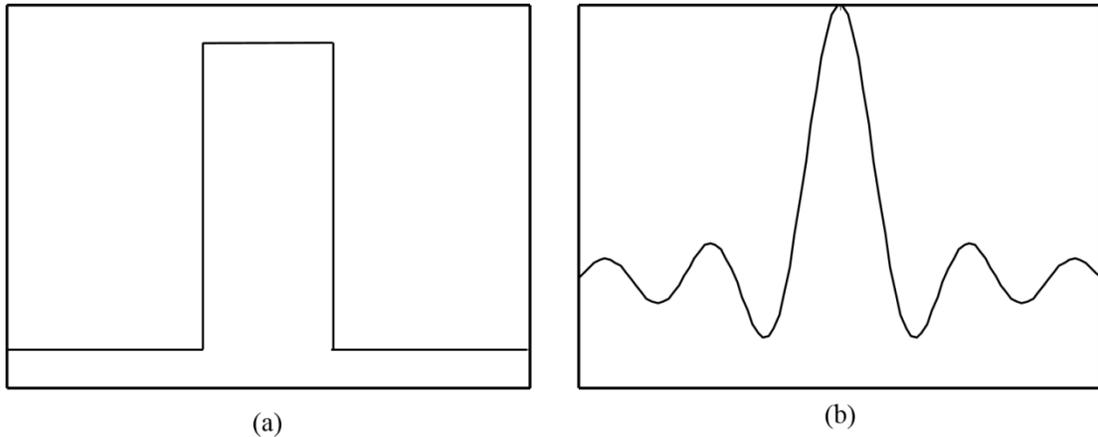


Fig. 2.8 (a) A pulse signal (b) Fourier transform of the pulse signal

2.3 Challenges of Linear Regulator Design in Energy Harvesting Systems

Designing a linear regulator is non-trivial as the performance parameters specified in the last section are not independent, and improving one usually compromises one or several of the rest.

For example, when the load current changes over a large range in a short time, the output voltage can experience a large variation. The output capacitor plays an important role in improving the load transient response as it suppresses the output voltage overshoot/undershoot when the load current changes. However, a large output capacitor also creates a low frequency pole at the regulator output, which could limit the system bandwidth.

For those systems powered by harvesting energies from the environment, the power efficiency is critical. As discussed in subsection 2.2.2, the maximal power

efficiency achievable is determined the dropout voltage and quiescent current. Therefore, to have power efficiency, one needs to reduce the dropout voltage. Besides, a low dropout is always desired because a lower dropout voltage means the output voltage stays regulated at a lower battery voltage. The dropout voltage is mainly determined by the pass element size and the maximal output current requirement. As stated in the subsection 2.2.2, as the battery discharges, when the pass element changes into linear region, the output voltage cannot stay regulated and it starts to drop as the battery continues discharging. Therefore, the dropout voltage can be studied by the following equation

$$I_{out,max} = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} V_{ds}^2 = \frac{1}{2} \mu_0 C_{ox} \frac{W}{L} V_{dropout}^2 \quad (2-11)$$

Rearranging the above equation and the dropout voltage can be written as

$$V_{dropout} = \sqrt{\frac{2I_{out,max}}{\mu_0 C_{ox} \frac{W}{L}}} \quad (2-12)$$

Therefore, given the maximal output current requirement, to reduce the dropout voltage, one can increase the $\frac{W}{L}$ of the pass element, which implies a larger device occupying more chip area. Besides, increasing the size of the pass element also increases its gate capacitance, which means the transient response could be slower as it takes longer time to charge or discharge this gate capacitance during transition.

To improve power efficiency and allow enough energy is left for the load in an energy harvesting system, the quiescent current consumption of the linear regulator should be kept in sub- μ A range. This severe restriction on quiescent current

could greatly compromise other performance aspects, especially the transient response. This is because the tail current of the error amplifier often determines the speed of charging and discharging the large gate capacitance of the pass element. A small tail current limits the slew rate. Therefore, when the load current changes over a wide range in a short time, the circuit takes long time to settle down, and the output voltage variation can be so large that proper operation of the load cannot be maintained.

Researchers have been investigating different methods of reducing the quiescent current of an LDO regulator while at the same time ensuring the quality of other performance aspects. In [44], common gate differential amplifiers and a current summation circuit have been used to eliminate the tradeoff between the quiescent current and the slew rate, and it achieves a fast transient response at a quiescent current of $1.2 \mu\text{A}$. In [45], the authors proposed an ultra-low quiescent current LDO consuming $0.9 \mu\text{A}$ quiescent current at no load. When the load current increases, the regulator transforms itself from a 2-stage structure into a 3-stage structure with an increased quiescent current of $82.4 \mu\text{A}$ at full load condition. In [37], a voltage buffer has been inserted between the amplifier and the pass element, with the bias current of the buffer changing based on the load current to improve the transient response. Similarly in [46], a buffer has also been adopted with varying bias current in response to the changing load, but this bias current returns to a low value at steady state.

Those commercial ultra-low power linear regulator products available in the market also tend to fail to meet the quiescent current limit without greatly hurting the transient response. For example, MCP1700 [47] of Microchip Technology consumes

1.6 μA quiescent current at no load, and the quiescent current increases to above 30 μA at full load current; TPS79718 [48], an ultra-low power regulator of Texas Instruments, consumes 1.2 μA quiescent current, but it takes about 1 ms for the circuit to stabilize again when the load current changes; Even though TPS78330 [49] achieves 0.5 μA quiescent current, the load transient response is sacrificed a lot as the recovery time is more than 10 ms at load transient response.

In conclusion, when designing a linear regulator, one usually needs to explore the design spaces and do a tradeoff among those performance parameters. In those energy harvesting systems, the low incoming power density limits the design spaces and makes the design of low dropout voltage, low quiescent current linear regulator with great transient response very challenging.

Chapter 3: Proposed Voltage Regulator System for Energy Harvesting Systems Powering Wireless Sensor Nodes

3.1 Wireless Sensor Nodes Power Modes

A wireless sensor network is composed of a large number of distributed sensor nodes that work collaboratively to detect and report an object, monitor environmental conditions, etc [50]. Each sensor node is capable of sampling and processing the data, and communicating with other nodes. A sensor node is often composed of at least the following function components as shown in Fig. 3.1: sensors, microcontroller, radio transceiver, energy source and power conditioning, etc. Sensors are capable of measuring the change of physical parameters (e.g., temperature and moisture) or detecting certain objects (e.g., light and smoke). Those sensed analog signals from sensors would be digitized by an A/D converter and the digital signals then are processed by a microcontroller. The microcontroller also controls the other function components and allows them to work as a whole completing the goal. A radio transceiver allows a sensor node to communicate with other sensor nodes within the network. The sensor, microcontroller, transceiver block often demands some specific operating voltage and current ranges, and the power conditioning block is able to provide power to those other function blocks with appropriate voltage and current levels. A more detailed architecture overview of the sensor node developed in [51] is shown as in Fig. 3.2.

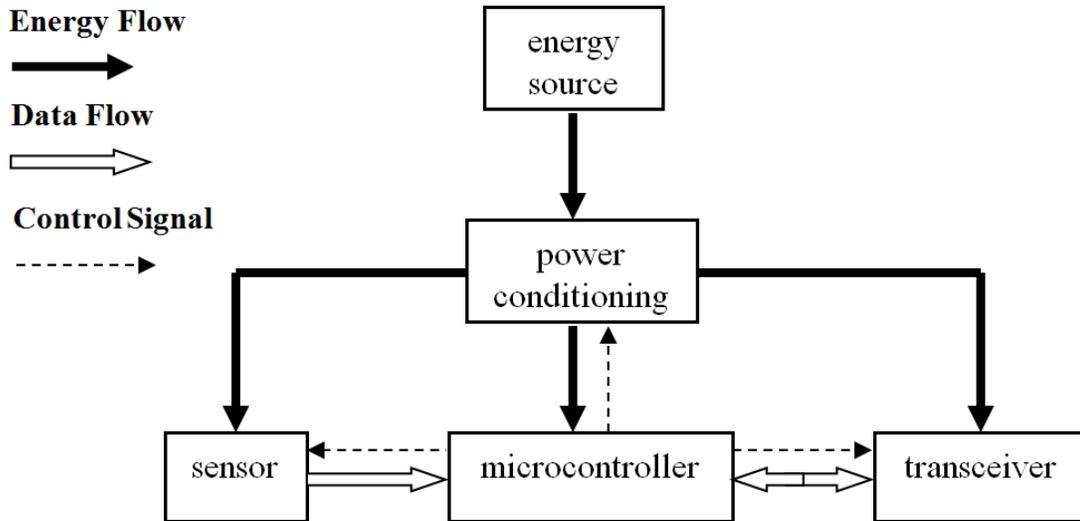


Fig. 3.1 Block diagram of a sensor node

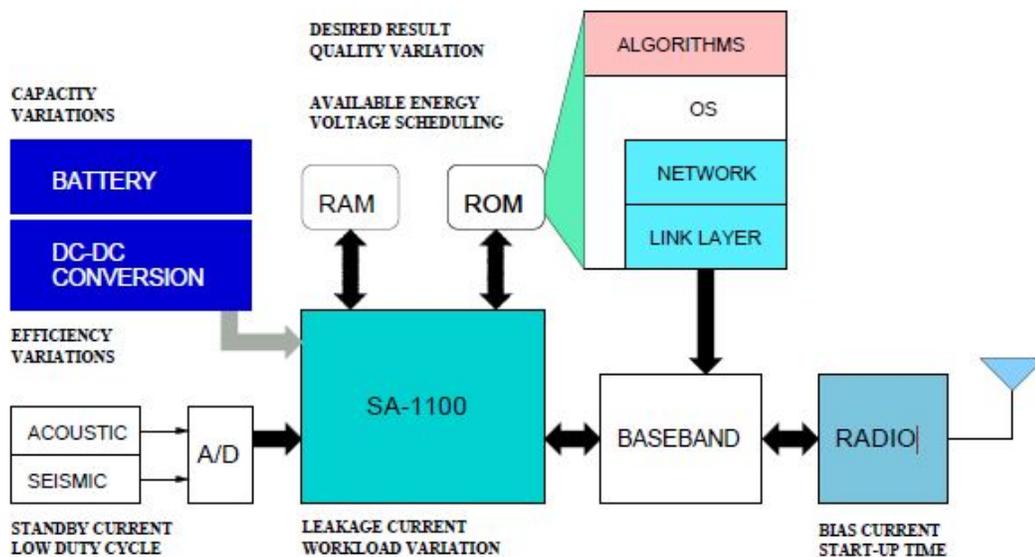


Fig. 3.2 Architecture overview of the sensor node developed in [51]

To save the power consumption, function components of sensor nodes can be turned off when necessary. For example, one can turn off the radio of a sensor node most of the time, and set a timer to allow the sensor node to wake up periodically to see if any other node within the network is trying to communicate with it [50] [52].

Also, the microcontroller can be set into sleep when it is not needed to process signals. Therefore, a sensor node usually has several power modes (states) to optimize its power consumption. An example of the power modes of a sensor node is shown as in Table 3.1 [53], where the sensor node has 5 power modes. Generally speaking, a sensor node usually has at least two power modes with different power demands. In the high power mode, i.e., active mode, a sensor node demands relatively large current. In the low power mode, i.e., standby mode, the sensor node only demands a small current.

Table 3.1 Power modes of a sensor node [53]

Power mode	Processor	Memory	Sensor & A/D	Transceiver
S_0	Active	Active	ON	Tx, Rx [*]
S_1	Idle	Sleep	ON	Rx
S_2	Sleep	Sleep	ON	Rx
S_3	Sleep	Sleep	ON	OFF
S_4	Sleep	Sleep	OFF	OFF

* Tx: transmit, Rx: receive

The current a sensor node consumes changes over an enormous range when it switches among those power modes. For example, in Table 3.1, in power mode S_0 , all the function components are active and therefore the sensor node consumes a large current in this mode. In contrast, in power mode S_4 , since some components are turned OFF and the rest are in sleep, so the sensor node only consumes a small current. A closer look at the current levels at different power modes is given in [54]. Although the actual current value of each function block in each power mode of

sensor nodes in [53] and [54] may not be the same, the breakdown of the current in Table 3.2 gives us an idea about the enormous current change when the sensor node changes from one power mode to another. Usually, when the sensor node is in active mode, it consumes dozens of mA current, and when it is in standby mode, it consumes only μA or even sub- μA range current, which means the current can change by more than 6 orders of magnitude. When the load current fast changes over an enormous range, the voltage overshoot/undershoot can be very large if the linear regulator is not well designed.

Table 3.2 Current consumptions of a sensor node under different power modes [54]

Component	Active (mA)	Idle (mA)	Inactive (μA)
MCU core (AT90S8535)	5	2	1
MCU pins	1.5	–	–
LED	4.6 each	–	–
Photocell	0.3	–	–
Radio (RFM TR1000)	1.2 Tx	–	5
Radio (RFM TR1000)	4.5 Rx	–	5
Temp (AD7416)	1	0.6	1.5
Co-proc (AT90LS2343)	2.4	0.5	1
EEPROM (24LC256)	3	–	1

3.2 Proposed Regulator System Operating Principle

Since power levels of the ambient energies harvested from the environment are so low, so to ensure that there is adequate energy to power a sensor node, one needs to limit the power consumption and quiescent current of the linear regulator to be minimal. As stated before, when the load current changes fast over an enormous range, the output capacitor discharges before the error amplifier goes back to linear region. However, the low quiescent current requirement can limit the slew rate of the error amplifier, which results in a long settling time, so the output voltage overshoot/undershoot can be large and affects the proper function of components of a sensor. Therefore, there always exists a tradeoff between small quiescent current and good transient response in a classical linear regulator design.

We observe that sensor nodes of WSNs often employ duty cycling behaviors: for the majority of time in each time period, sensor nodes are in standby mode demanding little current, and sensor nodes only burst for a short duration in each cycle to transmit/receive the data. This duty cycling behavior motivates us to design a regulator system which utilizes this sensor mode information. The regulator system is composed of two LDOs with different maximal output currents and quiescent current consumptions. The key idea is to switch between the two regulators depending on the sensor mode. Since the “right” regulator is used at the “right” time, the average quiescent current of the regulator system is minimized, and the tradeoff between low quiescent current and fast transient response has been eliminated.

The operating principle of the proposed regulator system can be better explained using the block diagram shown in Fig. 3.3 [55][56], where V_{in} and V_{out} are

the input and output voltages, regulator I and regulator II are regulators with different maximal current driving abilities, SW and \overline{SW} are complementary switches that control which regulator is to be used, and R_L and C_L are the load resistance and output capacitance.

When the sensor node is in active mode, it consumes moderate power and needs moderate current (e.g. mA range). In this case, switch SW is closed and regulator I is activated to deliver current to the sensor while consuming a few μA of quiescent current. When the sensor node changes into standby mode, only a small current (e.g. μA range or even sub- μA range) is needed to keep the sensor node in this mode, so SW is open and \overline{SW} is closed so that regulator II is activated to deliver the standby mode current to the sensor node. Regulator II only consumes sub- μA range quiescent current.

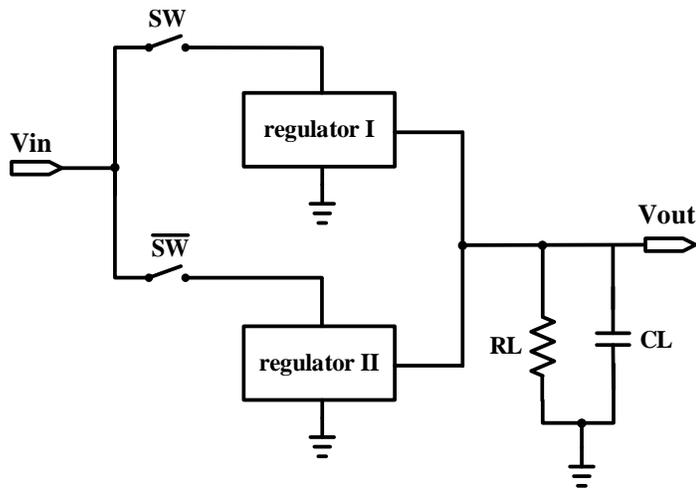


Fig. 3.3 Proposed regulator system block diagram

Usually a sensor node periodically bursts for only a very short duration in each cycle, and for the majority of time the sensor node stays in standby mode, so

regulator I is used for only a small fraction of time, therefore the average quiescent current is mainly determined by regulator II.

The average quiescent current of the regulator system can be studied in the following way: let I_{q1} and I_{q2} denote the quiescent currents of regulator I and regulator II respectively, and t_{active} and $t_{standby}$ denote the time a sensor node spends in active mode and standby mode. Since when the sensor node is in active mode, regulator I is activated and regulator II is off; and when the sensor node is in standby mode, regulator II is activated and regulator I is off, the average quiescent current of the regulator system can be expressed as

$$I_{q,avg} = \frac{I_{q1}t_{active} + I_{q2}t_{standby}}{t_{active} + t_{standby}} \quad (3-1)$$

where $I_{q,avg}$ is the average quiescent current of the regulator system.

We define the duty cycle D to be the fraction of time a sensor node spends in active mode

$$D = \frac{t_{active}}{t_{active} + t_{standby}} \quad (3-2)$$

Then equation (3-1) can be written as

$$I_{q,avg} = I_{q1}D + I_{q2}(1-D) \quad (3-3)$$

Usually a sensor node periodically bursts for a very short duration, so D is small and equation (3-3) can be approximated as

$$I_{q,avg} = I_{q2} \quad (3-4)$$

Since the average quiescent current is mainly determined by the quiescent current of regulator II and I_{q2} lies in sub- μA range, $I_{q,avg}$ is also small and lies in sub- μA range.

3.3 Proposed Regulator System Structure

The block diagram of Fig. 3.3 is used to better explain the operating principle of the proposed regulator system. In fact, switch \overline{SW} can be removed to simplify design. If \overline{SW} is removed, regulator II is continuously ON. When the sensor node is at standby mode, the system still behaves in the way we have described before. When the sensor node is in active mode, both regulators I and II work in this phase. The mA range load current mainly comes from regulator I. Now the average quiescent current of the system is $I_{q1}D + I_{q2}$, which is still approximately I_{q2} . Therefore, eliminating switch \overline{SW} does not affect the function or the performance of the regulator system, and it simplifies the design and control.

The two regulators of the regulator system are implemented using two linear regulators which have a structure similar to the one shown in Fig. 2.1. For regulator I, since it needs to be capable to deliver mA range maximal output current, the pass element has a large width and there is a large gate capacitance associated with it. This large gate capacitance, together with the high output resistance of the error amplifier, generates a low frequency pole. The circuit has another low frequency pole which is located at the output of the regulator due to the large output capacitor. These two low frequency poles could limit the bandwidth or even make the system unstable. To move the pole associated with the gate of the pass element to a higher frequency, one could insert a buffer between the error amplifier and the pass element [23] [57]. For

regulator II, since it only needs to provide the standby current to the sensor node, its width is small. Thus, no buffer is needed. Besides, eliminating this buffer reduces the quiescent current of regulator II, which is helpful in reducing the average quiescent current of the whole system.

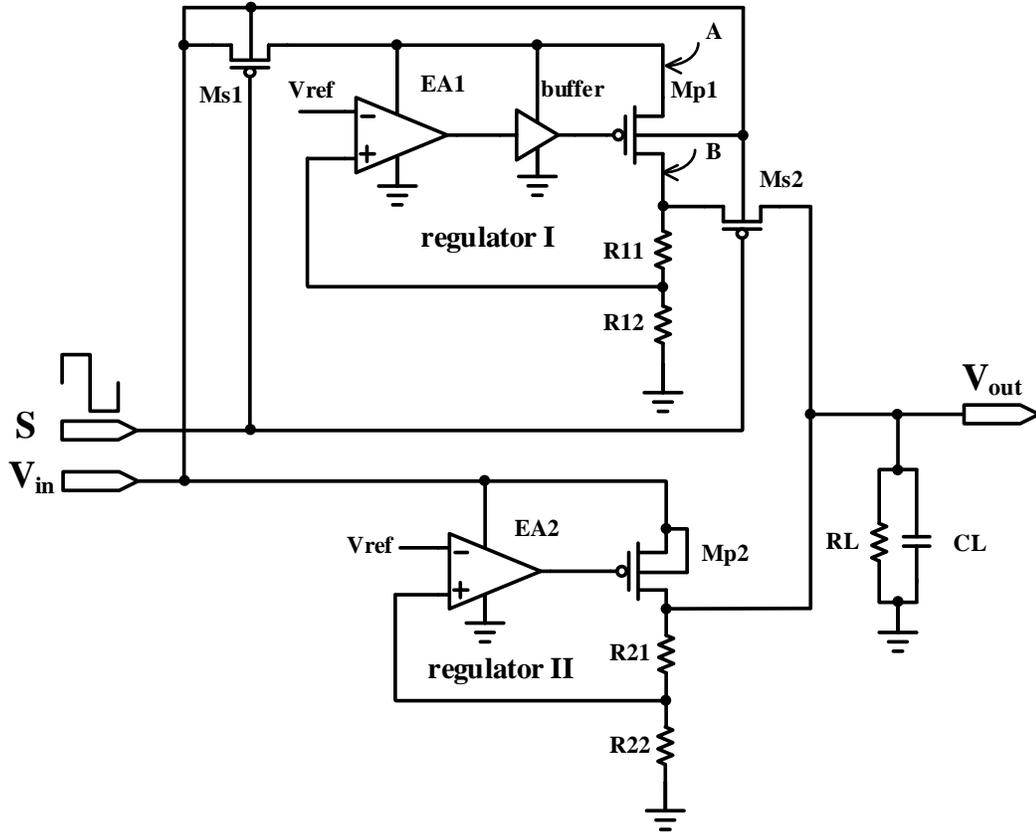


Fig. 3.4 Proposed regulator structure

The structure of the whole regulator system is shown as in Fig. 3.4. Amplifier EA_1 , buffer, pass element M_{p1} and resistors R_{11} and R_{12} form regulator I. Amplifier EA_2 , pass element M_{p2} and feedback resistors R_{21} and R_{22} form regulator II. R_L and C_L are the load and output capacitor. S is a switch signal related to the sensor node state information. M_{s1} is a PMOS transistor corresponding to the switch SW in Fig.

3.2. M_{s2} is a switch used to cut off the reverse current path. The reason why such a switch is necessary would be discussed in more detail later.

The switches of the regulator system are implemented using PMOS transistors. The reason why we have used PMOS transistors instead of NMOS transistors is that NMOS is poor at passing a high voltage because it introduces a threshold voltage drop, whereas PMOS is good at passing a high voltage with negligible voltage drop. This could be more easily understood by studying properties of NMOS and PMOS.

As shown in Fig. 3.5, when an NMOS is passing a high voltage V_{dd} from its drain node to source node, its gate voltage should be higher than the source voltage by at least a threshold voltage in order to conduct current, i.e., $V_{gs} > V_{tn}$, where V_{tn} is the threshold voltage of an NMOS. Therefore, the source voltage V_s is at most $V_{dd} - V_{tn}$, meaning that there is at least a threshold voltage drop between the drain node and the source node. In contrast, when a PMOS is passing a high voltage V_{dd} from its source node to the drain, its drain voltage could be close to V_{dd} , because $|V_{gs}| > |V_{tp}|$ is already satisfied. Considering those switching characteristics, the PMOS transistors are chosen to implement the switches.

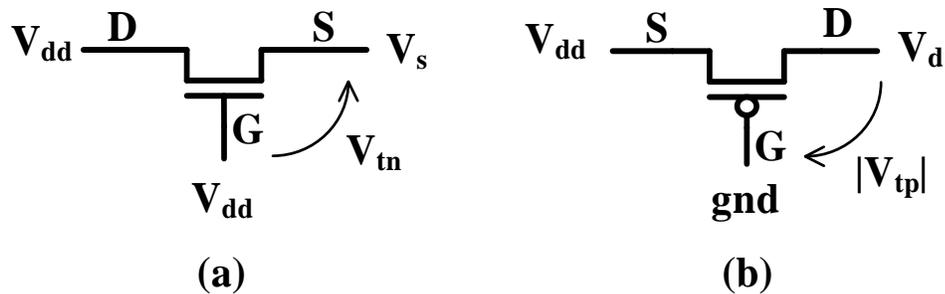


Fig. 3.5 Transistors used as switches passing high voltages (a) NMOS passing a high voltage (b) PMOS pass a high voltage

Without switch M_{s2} , when the sensor node changes from active mode into standby mode, M_{s1} is turned OFF and voltages of nodes within the circuit of regulator I start to drop. A MOSFET is a symmetric device, meaning that its source and drain are interchangeable. As the gate voltage and source (i.e., node A) voltage of M_{p1} keep dropping, the source and drain change their roles when the drain (i.e., node B) voltage becomes higher than the source voltage. When this happens, there is a current flowing through M_{p1} to circuit of regulator I (e.g., EA_1 and buffer). Depending on the current driving ability of regulator II, this reverse current comes from either the output capacitor discharge current or the current provided by regulator II. If regulator II does not have enough current delivering ability to provide the reverse current, the output capacitor discharges itself to provide this current and the output voltage drops. If regulator II has enough current delivering ability, the reverse current is provided by the drain current of M_{p2} , which is drawn from the power supply. In either case, this reverse current flow should be avoided.

For a PMOS transistor, the source voltage generally is higher than the drain voltage, so it is common to connect the body of a PMOS to its source and the PN junction in this case is kept reverse biased. In our regulator system, however, when the source and drain of M_{p1} change their roles, the junction becomes forward biased. The reverse current is μA range, and the pass element M_{p1} is large, so the drain voltage and source voltage difference of M_{p1} is small, so the PN junction is only weakly forward biased. However, for safety reasons, it is still a better approach to make the body node connected to the highest voltage (i.e., V_{in}).

To cut off the reverse current flow, we have added a switch M_{s2} to the system as shown in Fig. 3.3. When the sensor node is at standby mode, switch signal S is at a high voltage and both M_{s1} and M_{s2} are turned OFF. When M_{s2} is OFF, it makes the output node V_{out} disconnected from node B , cutting off the reverse current path. When the sensor node is in active mode, switch signal S is at a low voltage and both M_{s1} and M_{s2} are turned ON, making the whole circuit still function as we have described before. Similarly, the body node of M_{s2} is also connected to the input voltage V_{in} to avoid PN junction becoming forward biased.

For all other PMOS transistors except M_{p1} and M_{s2} , their body nodes can be connected to the source nodes to avoid the body effects. And for all the NMOS transistors, their body nodes are connected to ground if one is using an n-well process.

Chapter 4: Circuit Design and Implementation of the Regulator System

4.1 Pass Element Consideration

In a standard CMOS technology, the pass element can be implemented using either an NMOS or a PMOS, and the corresponding linear regulator structures with the two different pass elements are shown as in Fig. 4.1. The selection of the pass element can greatly affect the regulator performance.

Due to the lower mobility of holes as compared to electrons (e.g., in an ON Semiconductor 0.5 μm process, the motilities of electrons and holes are about 470 cm^2/Vs and 150 cm^2/Vs , respectively [58]), to have equal maximal output currents, the size of a PMOS transistor is usually larger than that of the NMOS. Therefore, the chip area of a linear regulator using a PMOS as the pass element is larger than its counterpart. Besides, a larger size transistor comes together with a larger gate capacitance; therefore, the pole associated with the gate of the pass element is located at a lower frequency, which might limit the system bandwidth.

If we ignore the channel length modulation effect of the pass elements (i.e., $\lambda=\infty$), for the linear regulator with NMOS pass element, the output voltage will not be affected by any disturbance at the input (as long as the linear regulator is still in regulator region, i.e., the pass element is in saturation region). However, the linear regulator with PMOS pass element will not have such an advantage. Therefore, a linear regulator with NMOS pass element has better PSRR performance.

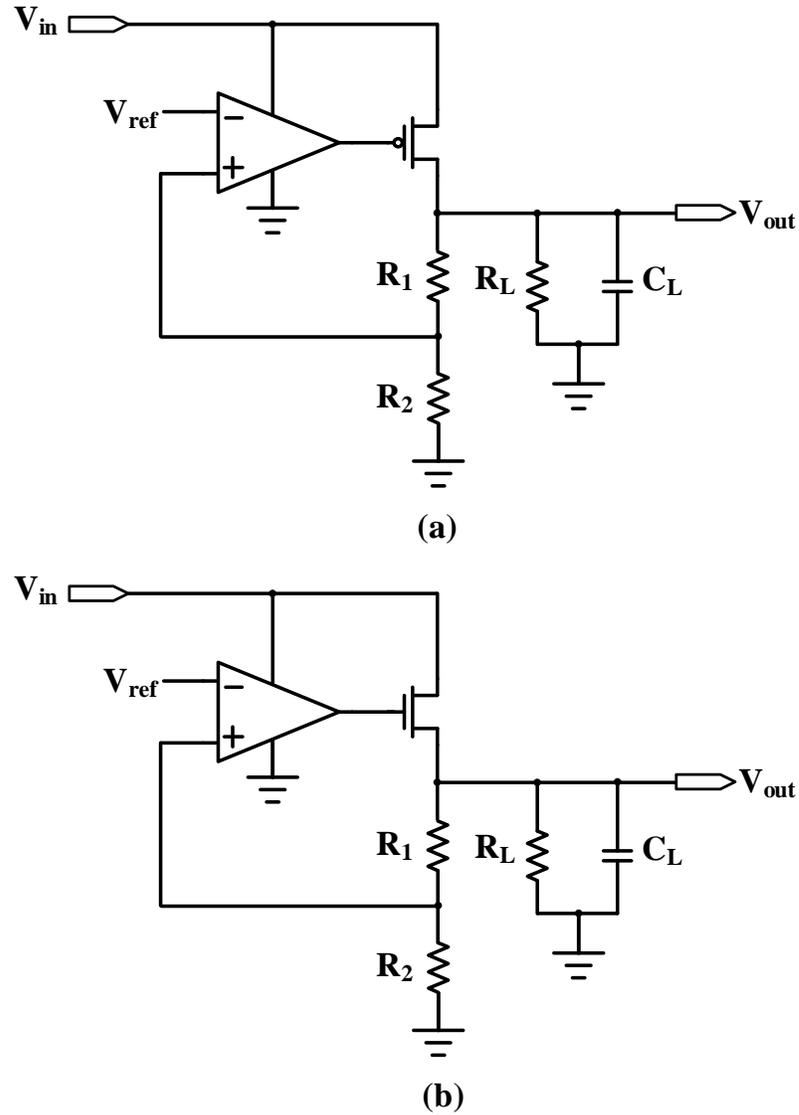


Fig. 4.1 Linear regulators with (a) PMOS pass element (b) NMOS pass element

One of the main disadvantages of using a NMOS as the pass element is the dropout voltage. As shown in Fig. 4.1 (a), the PMOS is connected as a common source structure. Since the linear regulator enters dropout region when the PMOS is at the edge of the saturation region, so the dropout voltage is equal to the overdrive voltage of the pass element (i.e., $V_{ov,p}$). In contrast, in Fig. 4.1 (b), the NMOS is connected as a source follower structure. The highest voltage achievable at the gate of

the pass element is equal to the input voltage V_{in} , and its source voltage (i.e., the regulator output voltage V_{out}) is limited by its gate voltage. To make the NMOS pass element in saturation region, its source voltage is at most $V_{in} - V_{tn} - V_{ov,n}$. Therefore, the dropout voltage is equal to $V_{tn} + V_{ov,n}$, which is a lot larger than the dropout voltage of a linear regulator with a PMOS pass element.

As stated before, a smaller dropout voltage is always desirable as it allows the battery to operate at a lower supply voltage. Besides, the maximum power efficiency achievable is directly related to the dropout voltage. Therefore, considering the low power requirement, the linear regulator with PMOS pass element better meets the requirement in an energy harvesting system. Table 4.1 summarizes the comparisons discussed so far.

Table 4.1 Comparison of PMOS pass element and NMOS pass element

Performance Metric	PMOS pass element	NMOS pass element
Chip Area	–	+
PSRR	–	+
Line Regulation	–	+
Bandwidth	–	+
Dropout Voltage	+	–
Maxim Power Efficiency	+	–

Since the load current comes from the drain current of the pass element, the size of the pass element can be determined by the dropout voltage and maximal output current requirements, and it is given by

$$\frac{W}{L} = \frac{2I_{out,max}}{\mu_p C_{ox} V_{dropout}^2} \quad (4-1)$$

where μ_p and C_{ox} are the hole mobility and oxide capacitance, $I_{out,max}$ and $V_{dropout}$ are the maximal output current and dropout voltage. Equation (4-1) gives the $\frac{W}{L}$ ratio of the pass element. To minimize the chip area, usually the minimal length L is chosen.

4.2 Regulator I Design

Regulator I circuit schematic is shown as in Fig. 4.1, where V_{in} and V_{out} are the input and output voltages, M_{a1} - M_{a8} form the error amplifier, M_{p1} is the pass element, M_{a9} - M_{a13} form the buffer between the error amplifier and the pass element, and R_{a1} and R_{a2} are two feedback resistors. As discussed in the last section, a linear regulator with a PMOS pass element has a smaller dropout voltage, which is beneficial in low power systems. Therefore, the pass element used here is a PMOS transistor.

The error amplifier serves as the main gain stage of the linear regulator and it compares the reference voltage V_{ref} with a fraction of the output voltage and generates an error voltage. Apparently a higher gain implies better output voltage accuracy, line regulation, PSRR, etc. The error amplifier of Fig. 4.2 is a folded cascode structure with PMOS transistors as input devices.

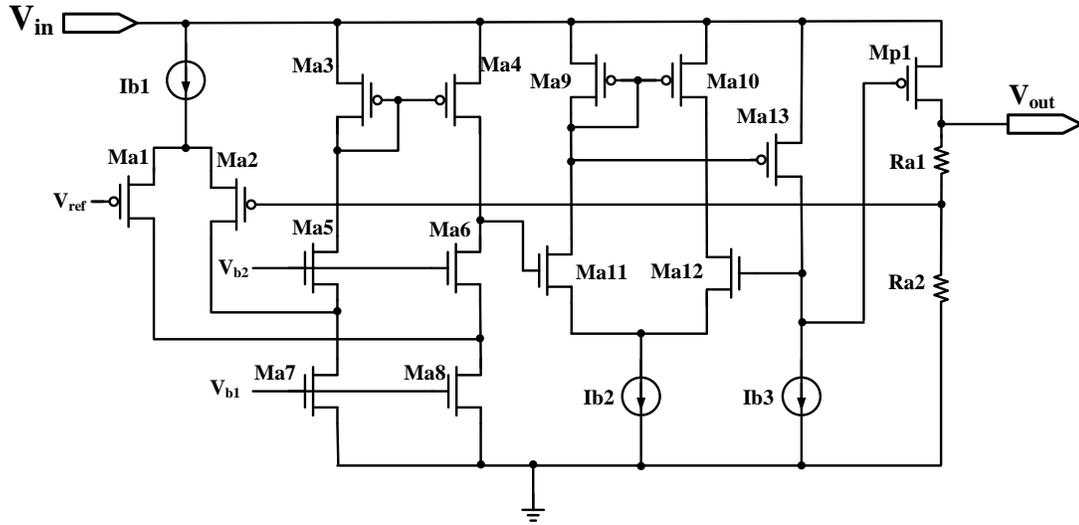


Fig. 4.2 Regulator I circuit schematic

Usually a cascode amplifier also has a cascode structure as its load so as to have a high gain. However, we use a simple current source load, which gives us a smaller output resistance as compared to the cascode amplifier with a cascode load. A smaller output resistance reduces the gain, but at the same time this makes the pole associated with the error amplifier output node locate at a higher frequency.

The gain of this error amplifier can be estimated as

$$A = g_{ma1} r_{oa4} \quad (4-2)$$

where A is the gain of the error amplifier, g_{ma1} is the transconductance of the input PMOS devices (i.e., M_{a1} and M_{a2}), and r_{oa4} is the output resistance of M_{a4} .

The pole associated with the gate of the pass element is located at

$$p = r_{oa4} C_{total} \quad (4-3)$$

where C_{total} is the total resistance seen from the error amplifier output to ground.

The pass element has a large size, so C_{total} is very large. This large capacitance, together with the high output resistance of the error amplifier, generates

a low frequency pole. Due to the large output capacitor, the pole at the regulator output is also located at a low frequency. These two low frequency poles can limit the system bandwidth or even make the system unstable.

To improve the system frequency response, a voltage buffer formed by M_{a9} - M_{a13} has been designed and inserted between the error amplifier and the pass element. This voltage buffer has a much smaller output resistance as compared to the output resistance of the error amplifier, so the pole at the gate of the pass element is pushed to a much higher frequency.

This buffer can be modeled as the circuit shown in Fig. 4.3, where error amplifier A_b is composed of transistors M_{a9} - M_{a12} . The error amplifier of the buffer forces the input voltage and output voltage of the buffer to be equal, so this voltage buffer has a unity gain. Besides, this unity gain voltage buffer employs negative feedback, which helps to reduce to the output resistance of this unity gain buffer to be

$$r_{buffer} = \frac{1}{g_{ma13}A_b} \parallel r_{oa13} \approx \frac{1}{g_{ma13}A_b} \quad (4-4)$$

where A_b is the gain of the amplifier, g_{ma13} and r_{oa13} are the transconductance and output resistance of transistor M_{a13} .

The output resistance of the folded cascode amplifier is about r_{oa4} , so without the unity gain buffer, the frequency of the pole at the gate of the pass element is $\frac{1}{r_{oa4}C_{gate}}$, where C_{gate} is the capacitance seen from the gate to ground.

After inserting the buffer, the pole is located at $\frac{A_b g_{ma13}}{C_{gate}}$. Therefore, this buffer helps

to push the pole at the gate of the pass element to a frequency that is $g_{ma13}r_{oa4}A_b$ times higher than the case without this buffer.

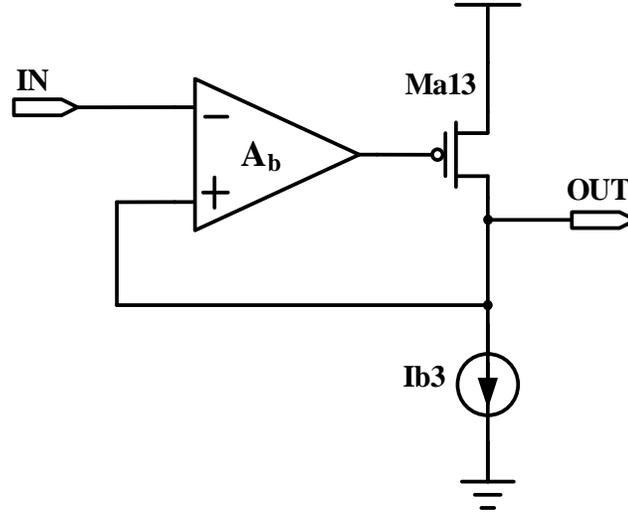


Fig. 4.3 Unity gain buffer model

The unity gain buffer also has a larger output voltage swing as compared to the super source follower buffer used in [23], which results in a smaller dropout voltage. In [23], the minimal output voltage of the buffer, which is also the gate voltage of the pass element, is $2V_{ov,n} + V_{th,p} + V_{ov,p}$, where $V_{ov,n}$ is the overdrive voltage of the NMOS transistors, and $V_{th,p} + V_{ov,p}$ is the gate source voltage of the transistor M_{21} in [23]. For the process we are using, this minimal output voltage is too high to fully turn ON the pass element at full load current, resulting in a high drop-out voltage. The dropout voltage usually arises because the pass element goes into triode region. Here, however, the pass element of [23] is still in saturation region, but the gate voltage is not high enough to fully turn ON the pass element, so the regulator fails to regulate the output before the pass element enters triode region. Therefore, we have a larger dropout voltage. In contrast, in our circuit shown in Fig. 4.2, the

minimal output voltage of the buffer is only $2V_{ov,n} + V_{th,n}$. Thus, the pass element can be easily turned ON at full load current. The threshold voltages of PMOS and NMOS transistors of the process we are using are about 0.9 V and 0.65 V, respectively. The dropout voltage of the regulator is about 700 mV if one is using a super source follower as the buffer [23]. In contrast, with an equal size pass element, the dropout voltage is below 200 mV using the proposed buffer.

4.2 Regulator II Design

Regulator II circuit schematic is shown as in Fig. 4.4, where M_{b1} - M_{b4} form the error amplifier, M_{p2} is the pass element, and R_{b1} and R_{b2} are the two feedback resistors. The error amplifier is a simple differential amplifier with a singled ended output.

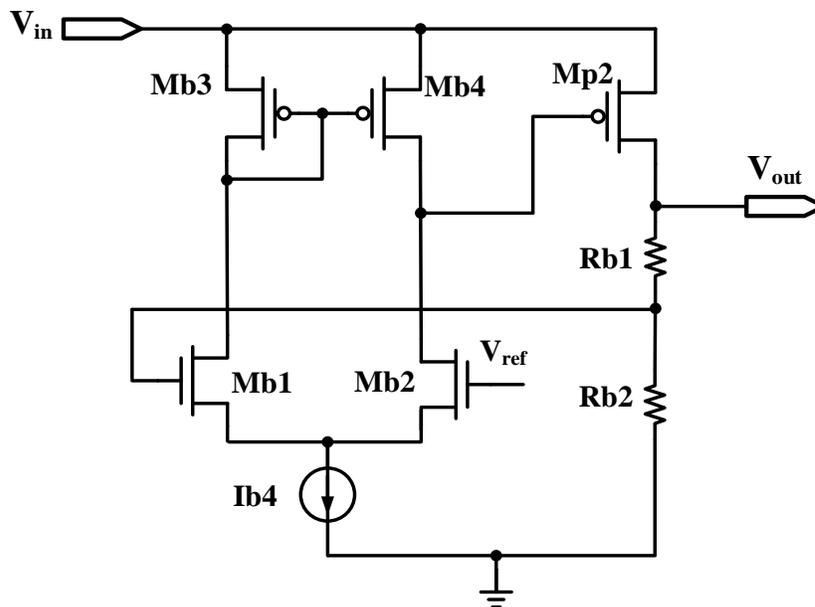


Fig. 4.4 Regulator II circuit schematic

Because the standby mode current of the sensor node is small, the size of pass element M_{p2} could also be small. Therefore, even without inserting a buffer between the error amplifier and the pass element, the pole associated with the gate of the pass element is already located at relatively high frequency. Besides, the output capacitor is large, and the equivalent resistance seen from the output node to ground is also large, so the pole at the regulator output is located at very low frequency. Indeed, there is only one pole within the unity gain frequency (UGF) of the system, so the system is already stable, and no buffer is needed to push the pole associated with the gate of the pass element to a higher frequency.

As stated before, the average quiescent current of the whole voltage regulator system is determined by the quiescent current of regulator II, so one needs to minimize the quiescent current of this regulator. As compared to the error amplifier of regulator I, the error amplifier of regulator II works in sub-threshold region in order to minimize its tail current.

4.3 Reference Design

The regulator system needs reference currents in lots of ways, e.g. the tail currents of error amplifiers, etc. Self biasing (bootstrap) circuits are usually used to generate supply insensitive reference circuits [59][60]. A circuit describing the self biasing idea is shown as in Fig. 4.5.

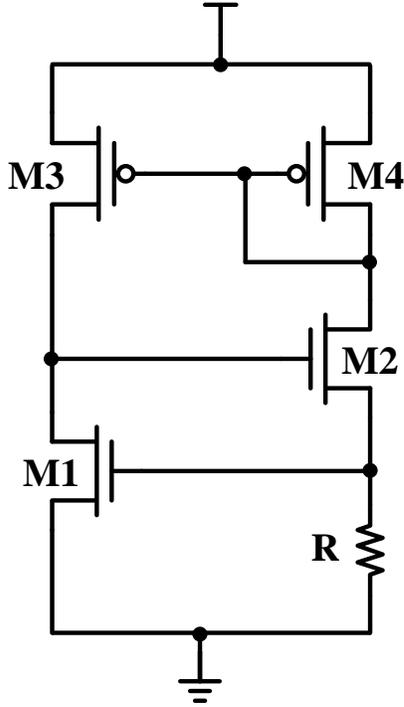


Fig. 4.5 A self biasing circuit [59]

The drain current of M_1 (I_{ds}) is a quadratic function of its gate source voltage, and the current flowing through resistor R (I_R) is a linear function of its voltage drop. If we plot the two currents as a function of the voltage, we get the figure as shown in Fig. 4.6. Since transistors M_3 and M_4 have equal sizes, they force I_{ds} to be equal to I_R . Therefore, operating point of the circuit is at the intersection of two curves.

The reference current can be solved by combining the following two equations

$$I_{ds} = \frac{1}{2} \mu_n C_{ox} \frac{W}{L} V^2 \quad (4-5)$$

$$I_R = \frac{V}{R} \quad (4-6)$$

Combing the equations (4-4) and (4-5), the reference can be expressed as

$$I_{ref} = \frac{2}{R^2 \mu_n C_{ox} \frac{W}{L}} \quad (4-7)$$

As shown in equation (4-7), the reference is not a function of the supply voltage. As a result, ideally, the supply sensitivity is very small.

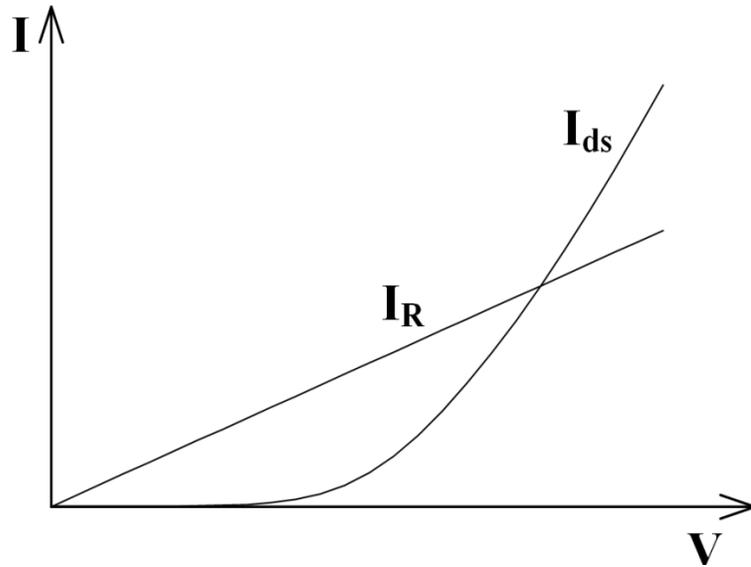


Fig. 4.6 Operating point of the self biasing circuit

A main problem with this self biasing circuit is that the reference current depends on the absolute value of the resistor R , which could have a relatively large variation. Besides, the transistor parameters cannot be well controlled considering the process variation.

Another problem is that the resistor R is in mega ohms range and cannot be integrated on chip. Using an off chip resistor introduces parasitic capacitance and inductance (one main source of the parasitic is from the wire bonding) which can greatly affect the proper operation of the reference current circuit of Fig. 4.5 operating in nano-ampere range current.

Taking the DIP 40 packaging of MOSIS as an example, the parasitic of each of the 40 pins is shown as in Table 4.2 [61].

Table 4.2 MOSIS DIP40 packaging wire bonding parasitic

Pin	R (Ω)	L (nH)	C (pF)
1, 20, 21, 40	0.217	8.18	5.32
2, 19, 22, 39	0.177	7.92	4.39
3, 18, 23, 38	0.154	7.34	3.37
4, 17, 24, 37	0.110	6.48	2.34
5, 16, 25, 36	0.103	5.69	2.16
6, 15, 26, 35	0.0661	4.37	1.43
7, 14, 27, 34	0.0646	4.54	1.48
8, 13, 28, 33	0.0498	3.69	1.05
9, 12, 29, 32	0.0378	3.54	0.863
10, 11, 30, 31	0.0247	3.15	0.660

Those parasitic elements can affect the function of the nano-ampere reference circuit shown in Fig. 4.5. For example, in the circuit simulations, after simply adding a 20 pF capacitor in parallel with the resistor R , the circuit exhibits oscillation as shown in Fig. 4.7.

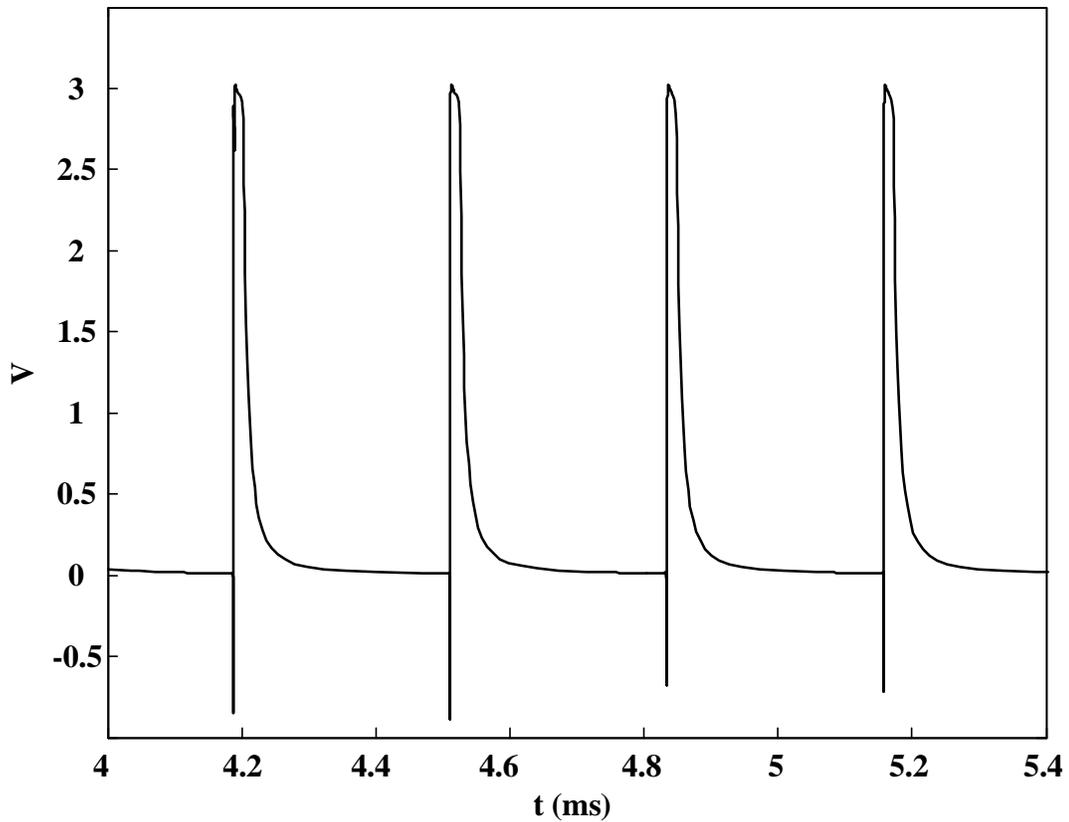


Fig. 4.7 Simulation result of the reference circuit of Fig. 4.5 after adding a 20pF parasitic capacitor

The possibility of oscillation has also been observed in our test of the fabricated chip. The reference current circuit has been fabricated using an ON Semiconductor 0.5 μm process, and the circuit needs a large off-chip resistor. As a result, the bonding wires introduce parasitic capacitance, inductance and so on. Also, the circuit board could also introduce parasitic. The measured result of the reference circuit with an off-chip resistor is shown as in Fig. 4.8 [55], which clearly demonstrates the circuit is oscillating. Since the reference circuit is oscillating, it cannot be used to generate the reference current for our voltage regulator system.

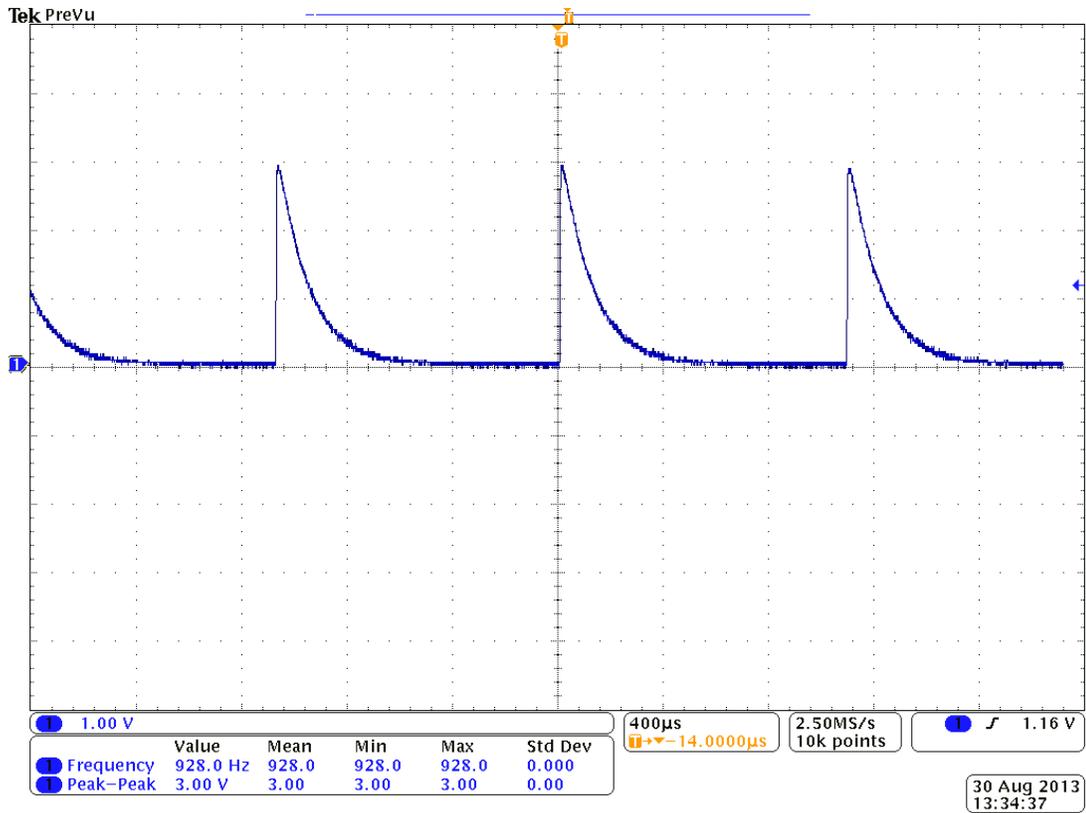


Fig. 4.8 Measured behavior of the reference circuit showing oscillation

Another nano-ampere current reference generator circuit using the self biasing idea is shown as in Fig. 4.9 [62]. This circuit only uses transistors and no off-chip component is needed. Therefore, the circuit can be implemented fully on chip to minimize parasitic. For the circuit shown in Fig. 4.9, transistors M_1 and M_2 both work in sub-threshold. M_3 and M_4 both work in above-threshold (i.e., strong inversion) but at different regions: M_4 is in saturation and it generates the gate voltage of M_3 ; M_3 is in triode region and it operates as a resistor. Speaking in another way, the triode region transistor has been used to serve the role of the resistor. M_5 - M_7 are current mirrors with equal sizes.

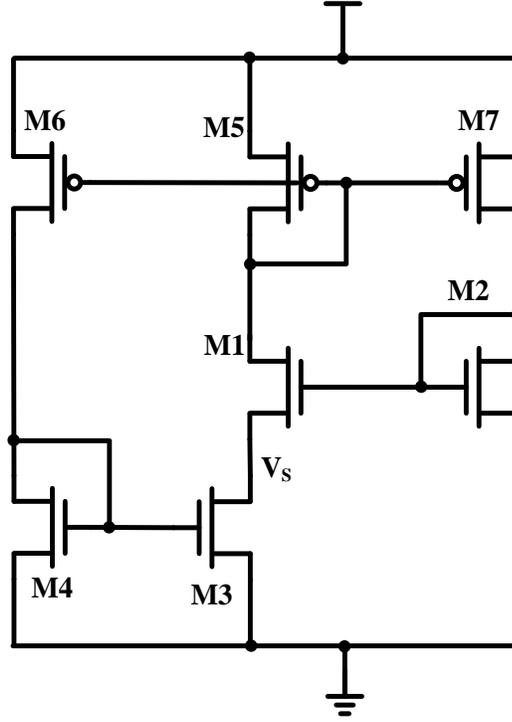


Fig. 4.9 A nano-ampere reference current generator [62]

We define $\beta_i = \mu_n C_{ox} \left(\frac{W}{L}\right)_i$. One can get the source voltage of M_1 (i.e., V_s) by equating the two sub-threshold drain currents of M_1 and M_2 . This V_s is also the drain source voltage of M_3 (i.e., $V_{ds3} = V_s$). V_s is a function of the thermal voltage V_T and the aspect ratio of transistors M_1 and M_2 :

$$V_s = V_T \ln \frac{\beta_1}{\beta_2} \quad (4-8)$$

The drain currents of M_3 and M_4 can be expressed as:

$$I_3 = \beta_3 \left[(V_{gs3} - V_m) V_{ds3} - \frac{1}{2} V_{ds3}^2 \right] \quad (4-9)$$

$$I_4 = \frac{1}{2} \beta_4 (V_{gs4} - V_m)^2 \quad (4-10)$$

Knowing that $V_{gs3}=V_{gs4}$, $I_3=I_4=I_{ref}$, we combine equations (4-8), (4-9) and (4-10) to solve for the reference current [62]:

$$I_{ref} = \beta_4 V_T^2 K_{eff} \quad (4-11)$$

where

$$K_{eff} = \left[\frac{\beta_4}{\beta_3} - 0.5 + \sqrt{\frac{\beta_4}{\beta_3} \left(\frac{\beta_4}{\beta_3} - 1 \right)} \right] \ln^2 \left(\frac{\beta_1}{\beta_2} \right) \quad (4-12)$$

K_{eff} in equation (4-11) is only a function of the aspect ratios of the transistors. The reference current in equation (4-11) is independent on the supply voltage, i.e. supply sensitivity is zero, meaning that ideally the reference does not change with the supply voltage.

In the above analysis, we have neglected the channel length modulation effect. In reality, the supply dependence is usually non-zero. A closer study of supply dependence of nano-ampere current can be carried out by doing a small signal analysis as shown in Fig. 4.10.

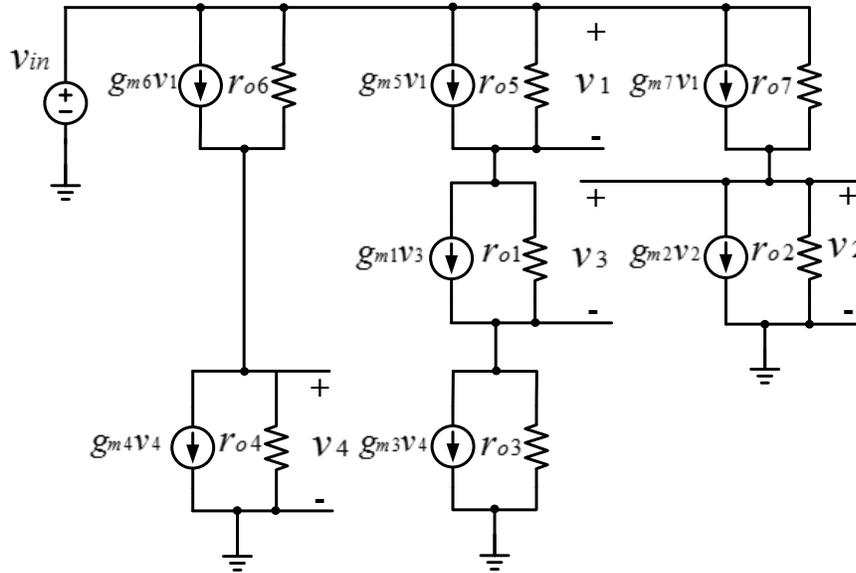


Fig. 4.10 Small signal model of the nano-ampere reference current generator

Using the small signal model, we can get the following equations using KVL and KCL

$$g_{m6}v_1 + \frac{v_{in} - v_4}{r_{o6}} = g_{m4}v_4 + \frac{v_4}{r_{o4}} \quad (4-13)$$

$$g_{m5}v_1 + \frac{v_1}{r_{o5}} = g_{m1}v_3 + \frac{v_3}{r_{o1}} = g_{m3}v_4 + \frac{v_{in} - v_1 - v_3}{r_{o3}} \quad (4-14)$$

$$g_{m7}v_1 + \frac{(v_{in} - v_2)}{r_{o7}} = g_{m2}v_2 + \frac{v_2}{r_{o2}} \quad (4-15)$$

By combining equations (4-13)-(4-15), we can solve for the small signal reference current as a function of the supply voltage,

$$\frac{i_{ref}}{v_{in}} = \frac{g_{m5}v_1 + (v_{in} - v_1)/r_{o5}}{v_{in}} = \frac{1}{(1 - \frac{g_{m3}}{g_{m4}} + \frac{1}{g_{m2}r_{o3}} - \frac{1}{g_{m1}r_{o3}})r_{o1}} \quad (4-16)$$

The commonly used nano-ampere current reference generator circuit is compact as it only uses transistors without using any large resistors or capacitors. Besides, the circuit is economic as it is a pure CMOS technology. The main problem with this circuit is that it has relatively large supply dependence: the reference current changes by 25% when the supply voltage changes by 1 V.

To mitigate the supply dependence of the reference current, we adopt the same idea of supply compensation as in [63] and designed a nano-ampere reference current generator as shown in Fig. 4.11 [56].

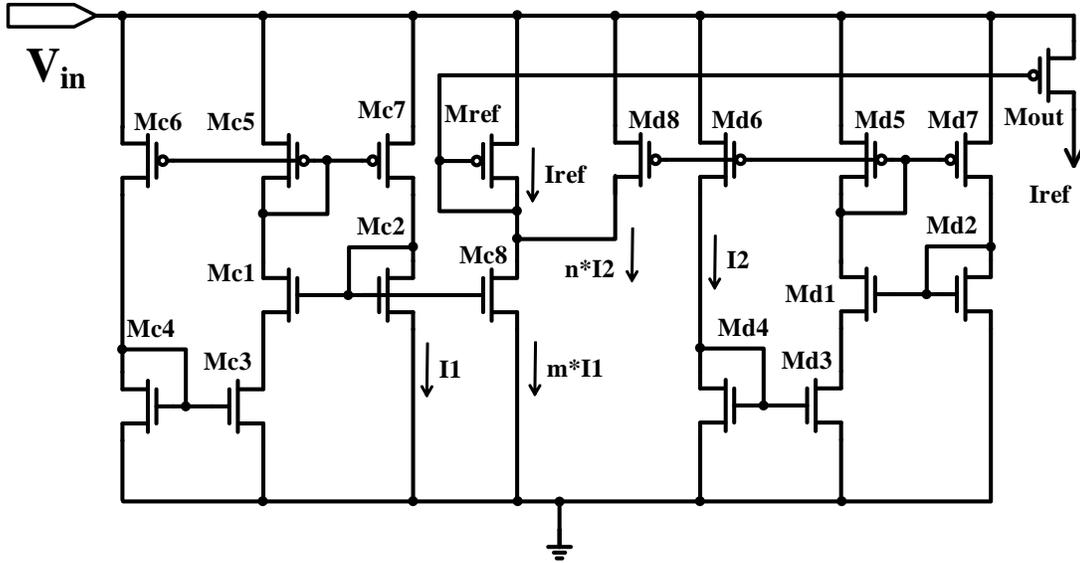


Fig. 4.11 Proposed supply voltage independent nano-ampere reference current generator circuit

The idea of the proposed nano-ampere reference circuit is to generate two reference currents and make them satisfy the two conditions [64]: (1) the two currents are not equal; (2) they have equal supply dependences. If one subtracts one reference current from the other, one can get a non-zero reference current with minimal supply voltage dependence. In Fig. 4.9, $M_{c1}-M_{c7}$ generates current I_1 and the drain current of M_{c8} is a multiple of I_1 (i.e., $m \cdot I_1$). $M_{d1}-M_{d7}$ generates current I_2 and the drain current of M_{d8} is a multiple of I_2 (i.e., $n \cdot I_2$). The reference current (i.e., the drain current of M_{ref}) therefore is

$$i_{ref} = m \cdot I_1 - n \cdot I_2 \quad (4-17)$$

By changing the scaling factors m and n , one can minimize the supply voltage dependence of the reference current.

4.4 System Stability Analysis

4.4.1 Load Impedance to Regulators

The whole regulator system has two regulators, so we need to study how one changes the load impedance of the other. When the sensor node is in standby mode, switch M_{s2} is OFF, therefore, regulator I does not load regulator II, and the load impedance seen by regulator II is just R_L in parallel with C_L . When the sensor node is in active mode, because the two feedback resistors R_{b1} and R_{b2} and the output resistance of M_{p2} (i.e., r_{o2}) are much larger than R_L , as a result, the load impedance seen by regulator I is also R_L in parallel with C_L . Therefore, no matter at what state the sensor node is, the load to each regulator is R_L and C_L , which greatly simplifies the stability analysis and frequency compensation designs.

4.4.2 Stability of Regulator I

Without any frequency compensation of regulator I, the system exhibits mainly three poles: one associated with the regulator output due to the large output capacitor needed to minimize voltage spikes when load current changes, another associated with the error amplifier output due to the high output resistance of amplifier, and another associated with the gate of the pass element. The pole at the regulator output and the pole at the error amplifier output are two low frequency poles. These two low frequency poles greatly limit the system bandwidth and introduce stability problems.

A more detailed analysis on the frequency response of the system can be carried out using the small signal block diagram as shown in Fig. 4.12. g_{mEA1} is the

transconductance of the error amplifier. R_{EA1} and C_{EA1} are the resistance and capacitance seen at the output of the amplifier, respectively. R_{buffer} and C_{buffer} are the output resistance and capacitance seen at the unity gain buffer output, respectively. g_{mp1} is the transconductance of the pass element M_{p1} . R_{fo} is the parallel resistance of the pass element and two feedback resistors, i.e., $R_{fo1} = (R_{a1} + R_{a2})//r_{o1}$, where r_{o1} is the small signal output resistance of M_{p1} . R_{MS2} is the equivalent resistance of the switch M_{s2} .

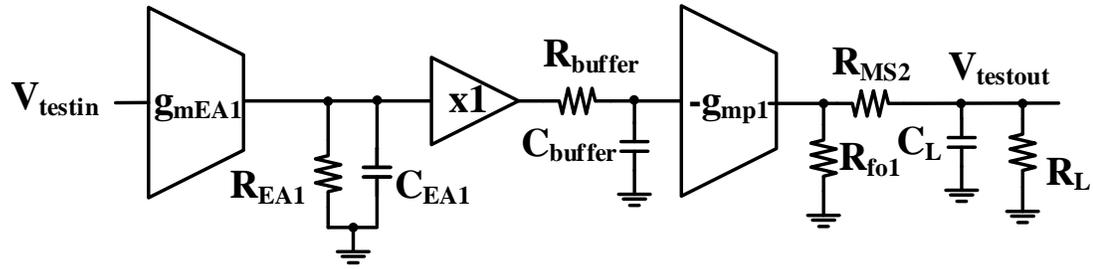


Fig. 4.12 Small signal block diagram for stability analysis of regulator I without compensation

The transfer function of the uncompensated system can be written as

$$T(s) = \frac{V_{testout}(s)}{V_{testin}(s)} = T_0 \frac{1}{1 + \frac{(R_{fo1} + R_{MS2})sR_L C_L}{R_{fo1} + R_{MS2} + R_L}} \frac{1}{1 + sR_{EA1}C_{EA1}} \frac{1}{1 + sR_{buffer}C_{buffer}} \quad (4-18)$$

where $T_0 = T(s=0) = \frac{-g_{mEA1}R_{EA1}g_{mp1}R_{fo1}R_L}{R_{fo1} + R_{MS2} + R_L}$ is the DC gain of the system.

The transfer function shows that the circuit has three poles and they are located at

$$p_1 = \frac{R_{fo1} + R_{MS2} + R_L}{(R_{fo1} + R_{MS2})R_L C_L} \quad (4-19)$$

$$p_2 = \frac{1}{R_{EA1} C_{EA1}} \quad (4-20)$$

$$p_3 = \frac{1}{R_{buffer} C_{buffer}} \quad (4-21)$$

The equivalent resistance of the switch M_{S2} is very small as compared to other resistances in equation (4-18), i.e., $R_{MS2} \ll R_L, R_{fo1}$. So the three poles can be approximated to be

$$p_1 = \frac{R_{fo1} + R_L}{R_{fo1} R_L C_L} = \frac{1}{(R_{fo1} // R_L) C_L} \quad (4-22)$$

$$p_2 = \frac{1}{R_{EA1} C_{EA1}} \quad (4-23)$$

$$p_3 = \frac{1}{R_{buffer} C_{buffer}} \quad (4-24)$$

The dominant pole p_1 in equation (4-22) shows that the output resistance seen at regulator output is equal to $R_{fo1} // R_L$, which is also equal to $R_{fo1} // (R_{a1} + R_{a2}) // R_L$. This is also intuitively correct, because when the switch M_{S2} is ideal without any resistance, the output resistance indeed is a parallel of the load resistor, two feedback resistors, and the output resistor of the pass element.

Since the system has three poles, one needs to do frequency compensation to the system to guarantee stability. There are many different ways to compensate a linear regulator. In [65], cascode-Miller compensation splits the two poles to achieve stability. In [66], a resistor is added in series with the output capacitor to generate a zero (ESR compensation) to make the loop stable. Another way to introduce a zero is to place a bypass capacitor in parallel with one of the feedback resistors (i.e., R_{a1}).

This compensation method generates both a zero and a pole, but the zero comes before the pole so still enough phase margin can be achieved. Some other compensation techniques have also been investigated to achieve stability even without output capacitors. In [67], people utilized the Miller compensation scheme to achieve stability without using external off-chip capacitors. Besides, the circuit uses a differentiator to improve the transient response. In [68], the researchers investigated the damping factor (ξ) control frequency compensation scheme (DFCFC) which substantially increases the bandwidth as compared to the Nested Miller compensation [69]; Some other capacitor-less LDO compensation schemes can be found in [70]-[71].

Here, we use ESR compensation due to its simplicity. The small signal block diagram of the compensated system is shown as in Fig. 4.13, where R_{ESR} is the equivalent series resistor for compensation.

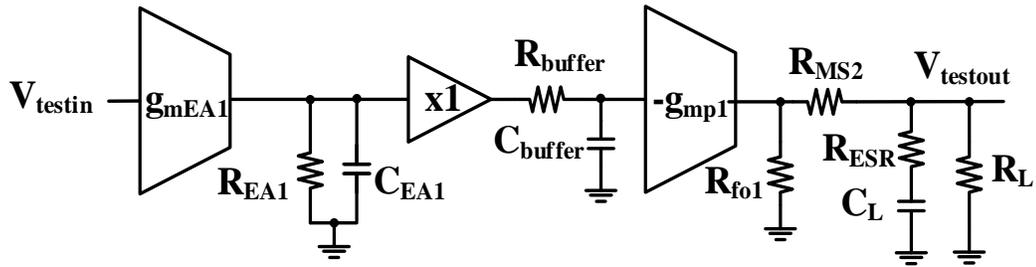


Fig. 4.13 Small signal block diagram for stability analysis of regulator I with compensation

The transfer function of the compensated system can be written as

$$T(s) = \frac{V_{testout}(s)}{V_{testin}(s)} = \frac{-g_{mp1}g_{mEA1}R_{EA1}}{(1+sR_{buffer}C_{buffer})(1+sR_{EA1}C_{EA1})} \frac{R_{fo1}X}{R_{fo1}+R_{MS2}+X} \quad (4-25)$$

with

$$X = \frac{(R_{ESR} + \frac{1}{sC_L})R_L}{R_{ESR} + \frac{1}{sC_L} + R_L} \quad (4-26)$$

When a sensor node is in active mode, it consumes large current. So we only consider the stability of the transfer function when the regulator is delivering large current to the load. Under this condition, the regulator exhibits the following properties:

- (1) The switch equivalent resistance is much smaller than the resistance of the the load, i.e., $R_L \gg R_{MS2}, R_{ESR}$.
- (2) The resistances of two feedback resistors are much larger than the small signal output resistance of the pass element, i.e., $(R_{a1} + R_{a2}) \gg r_{o1}$.

Based on the above two properties, the transfer function in equation (4-25) can be simplified as

$$T(s) = \frac{V_{testout}(s)}{V_{testin}(s)} = \frac{-g_{mp1}g_{mEA1}R_{EA1}}{(1 + sR_{buffer}C_{buffer})(1 + sR_{EA1}C_{EA1})} \frac{r_{o1}R_L(R_{ESR} + \frac{1}{sC_L})}{r_{o1}R_L + \frac{r_{o1} + R_L}{sC_L}} \quad (4-27)$$

If we define $R_{eq1} = r_{o1}/R_L$, then the transfer function can be reorganized as

$$T(s) = \frac{V_{testout}(s)}{V_{testin}(s)} = \frac{-g_{mEA1}R_{EA1}g_{mp1}R_{eq1}(1 + sR_{ESR}C_L)}{(1 + sR_{EA1}C_{EA1})(1 + sR_{buffer}C_{buffer})(1 + sR_{eq1}C_L)} \quad (4-28)$$

The transfer function shown in equation (4-28) exhibits three poles and one zero and they are located at

$$p_1 = \frac{1}{R_{eq1}C_L} \quad (4-29)$$

$$p_2 = \frac{1}{R_{EA1} C_{EA1}} \quad (4-30)$$

$$p_3 = \frac{1}{R_{buffer} C_{buffer}} \quad (4-31)$$

$$z = \frac{1}{R_{ESR} C_L} \quad (4-32)$$

Among those three poles, p_1 is the dominant pole. When load current changes, both the load resistance R_L and the small signal output resistance of the pass element change, as a result, the location of p_1 changes as the load current changes. As stated before, due to the unity gain buffer, the pole p_3 is pushed to a sufficiently high frequency. By making p_2 zero cancelling, the dominant pole p_1 becomes the only pole within the unity gain frequency (UGF) and the system is stable. The bandwidth of the system is estimated as

$$BW = A_{v0} p_1 = \frac{g_{mEA1} R_{EA1} g_{mp1}}{C_L} \quad (4-33)$$

The stability simulation setup is shown as in Fig. 4.14, where V_{testin} is the input signal with its DC component equal to the reference voltage V_{ref} . $V_{testout}$ is the measured output. The inductor L_{big} is very large, so any AC component of the output is blocked and the DC component of the output is allowed to pass. The capacitor C_{big} is large, so the DC component of V_{testin} is blocked and its AC component is allowed to pass. As a result, at the non-inverting terminal of the error amplifier, the DC component is $\frac{R_2}{R_1+R_2} V_{testin}$, and the AC component is equal to the AC component of V_{testin} . By varying the AC signal frequency of V_{testin} , one can measure the system frequency response.

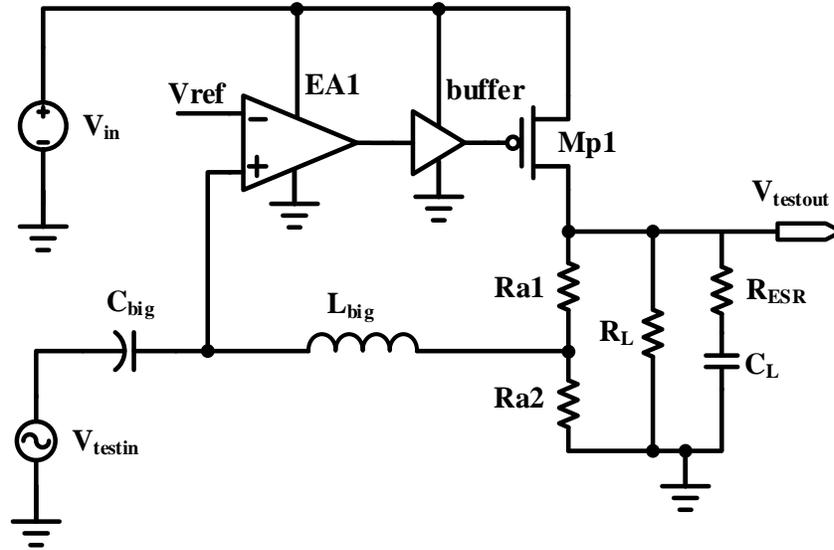


Fig. 4.14 Regulator I stability simulation setup

The simulation is taken with an output capacitor of $4.7 \mu\text{F}$ and a series resistor of 0.1 ohm . The supply voltage is DC with a value of 2.5 V . The load current is 100 mA (i.e., $R_L=18 \text{ ohms}$).

The stability simulation result is shown as in Fig. 4.15. A phase margin of about 70° degrees is achieved, and the system is stable.

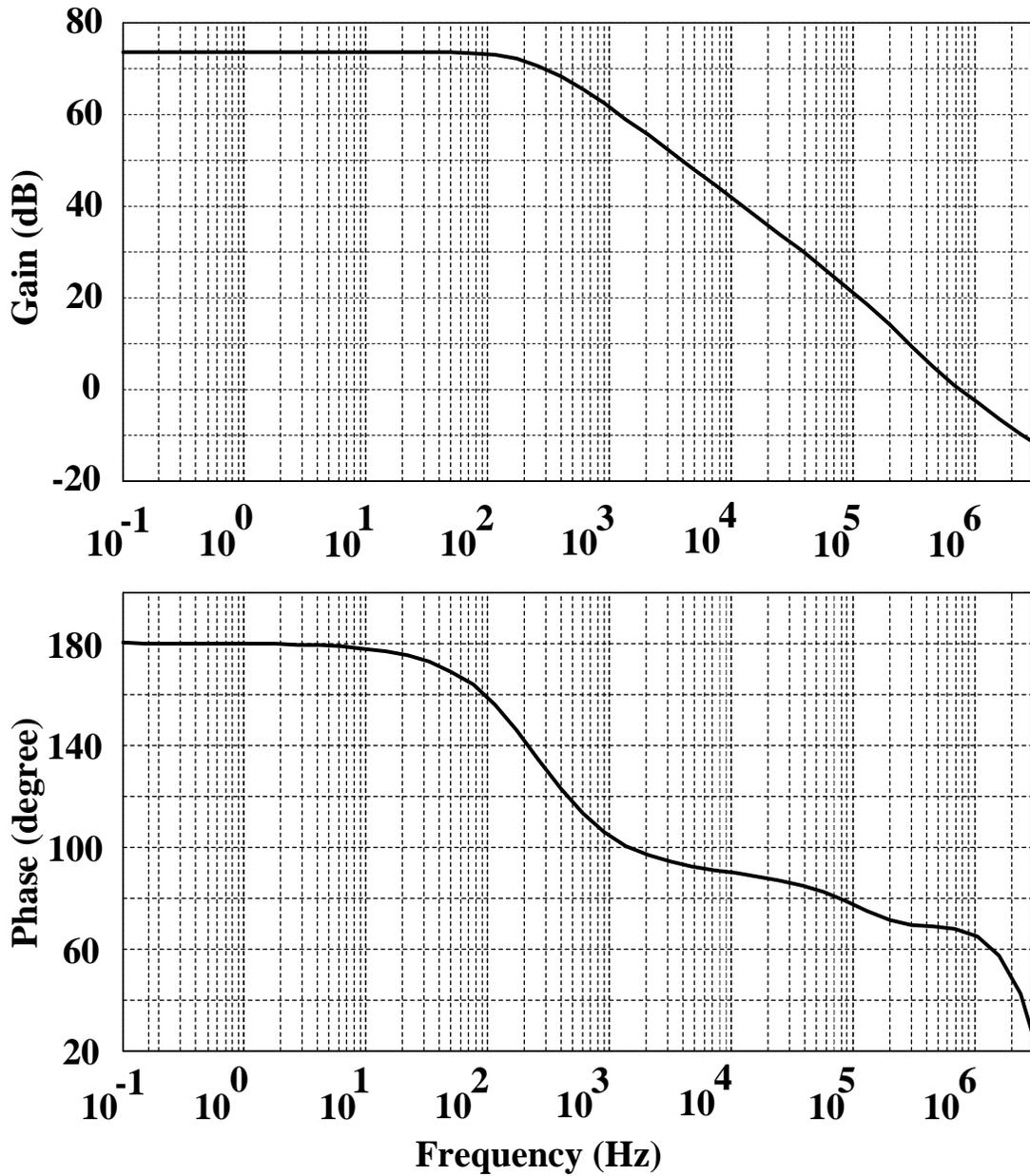


Fig. 4.15 Simulated frequency response of regulator I with $C_L=4.7$ uF, ESR=0.1 ohm,

$$V_{in}=2.5V, I_L=100mA$$

4.4.3 Stability of Regulator II

The small signal block diagram of regulator II is shown in Fig. 4.16, where g_{mEA2} is the transconductance of the error amplifier EA2. R_{EA2} and C_{EA2} are the resistance and capacitance seen at the output of the amplifier, respectively. g_{mp2} is

the transconductance of M_{p2} . R_{eq2} is defined as the resistance seen at the output, i.e.,

$R_{eq2} = (R_1 + R_2) // r_{o2} // R_L$, where r_{o2} is the small signal output resistance of M_{p2} .

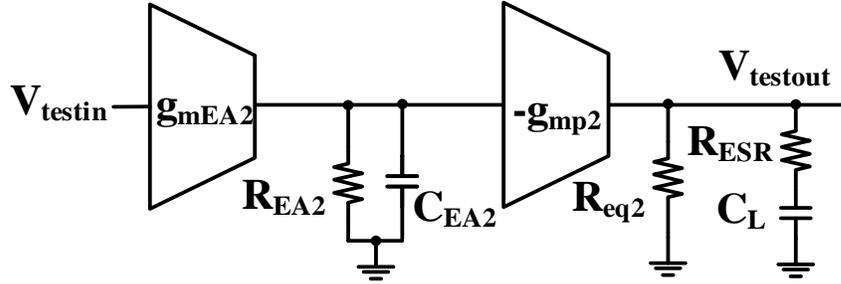


Fig. 4.16 Small signal block diagram of regulator II

The transfer function can be written as

$$T(s) = \frac{V_{testout}(s)}{V_{testin}(s)} = \frac{-g_{mEA2}R_{EA2}g_{mp2}R_{eq2}\left(R_{ESR} + \frac{1}{sC_L}\right)}{(1 + sR_{EA2}C_{EA2})(R_{eq2} + R_{ESR} + \frac{1}{sC_L})} \quad (4-34)$$

Since R_{ESR} is much smaller than R_{eq2} , we have

$$T(s) = \frac{V_{testout}(s)}{V_{testin}(s)} = \frac{-g_{mEA2}R_{EA2}g_{mp2}R_{eq2}(1 + sR_{ESR}C_L)}{(1 + sR_{EA2}C_{EA2})(1 + sR_{eq}C_L)} \quad (4-35)$$

The system has two poles and one zero

$$p_1 = \frac{1}{R_{eq2}C_L} \quad (4-36)$$

$$p_2 = \frac{1}{R_{EA2}C_{EA2}} \quad (4-37)$$

$$z = \frac{1}{R_{ESR}C_L} \quad (4-38)$$

The output capacitor used in the system is $4.7 \mu\text{F}$, and the resistance seen from the output node ground (i.e., R_{eq2}) is at mega ohms range, so p_1 is located at

such a low frequency that the gain is already far below unity before any non-dominant pole or zero can take effect. Therefore, the system is already stable.

The simulation setup is similar to the one used for regulator I. Simulation result is shown as in Fig. 4.17 at a DC supply voltage of 2.5 V and a load current of $0.1 \mu\text{A}$. The phase margin is about 90° degrees.

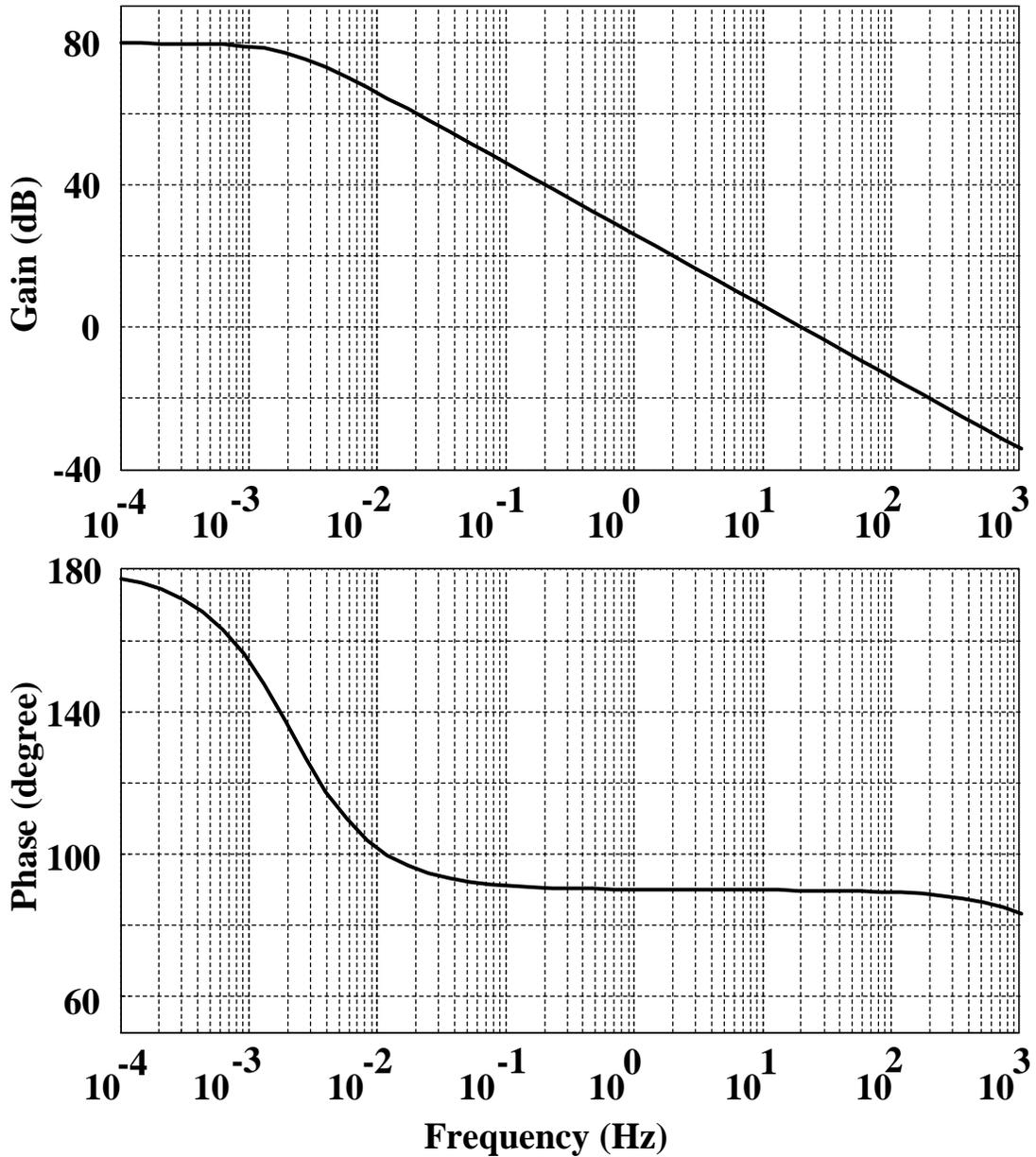


Fig. 4.17 Simulated frequency response of regulator II

Chapter 5: Regulator System Experimental Results and Discussions

The regulator system has been implemented and fabricated using an ON Semiconductor $0.5\ \mu\text{m}$ process. This process is an N-well process and it has 3 metal layers and 2 poly layers. The chip micrograph of regulator I and II (without switches) is shown as in Fig. 5.1.

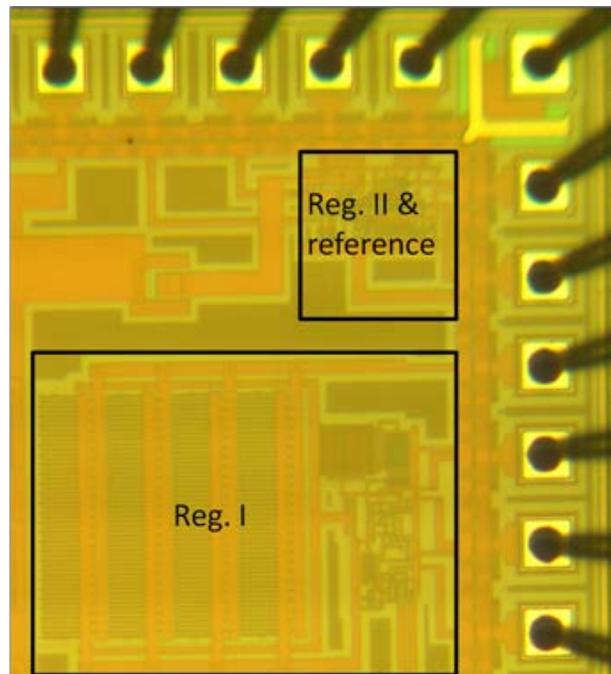


Fig. 5.1 Chip micrograph of regulator I and II

The sensor node we are testing requires a regulated supply of 1.8 V. The sensor node has two working modes: standby mode and active mode. The current profile of the sensor node is as follows: in standby mode, the sensor node demands $0.1\ \mu\text{A}$ current; when the sensor node changes from standby mode to active mode, its current changes from $0.1\ \mu\text{A}$ to 42 mA; in active mode, the current the sensor node

consumes changes from 42 mA to 104 mA and then back to 42 mA; then the sensor goes back to standby mode with a current of 0.1 μ A.

The output voltage is designed to be 1.8 V. To achieve stability, a 4.7 μ F output capacitor with a 0.1 ohm ESR has been used.

5.1 Reference Current

The measured result of the proposed nano-ampere reference current as a function of the input voltage is shown in Fig. 5.2, where the input voltage sweeps from 0 to 4.0 V. As Fig. 5.2 shows, when the input voltage is above 1.5 V, the reference current I_{ref} is a weak function of the input voltage and stays relatively stable. When the input voltage is below 1.5 V, transistors leave the desired operating regions and the reference current changes fast. As the input voltage drops from 4.0 V to 1.8 V, the reference current changes by only 4.4%/V. In contrast, for the current reference circuit without supply compensation, the change is about 25%/V. Therefore, the proposed reference current generator reduces the supply dependence by more than 5 as compared to the nano-ampere reference current generator without supply compensation.

The simulation result of the temperature dependence of the reference current is shown as in Fig. 5.3. The supply voltage is 3 V. When the temperature changes from -40°C to 70°C, the reference current only changes by about 0.76 nA, meaning the temperature coefficient is about 230 ppm/°C.

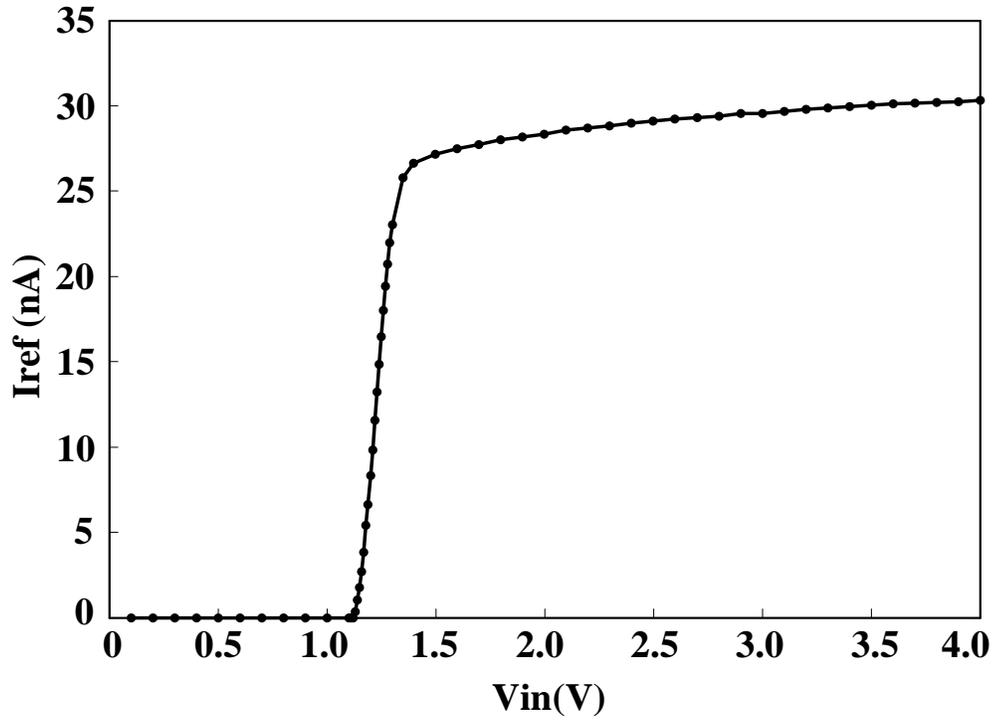


Fig. 5.2 Nano-ampere reference current as a function of input voltage

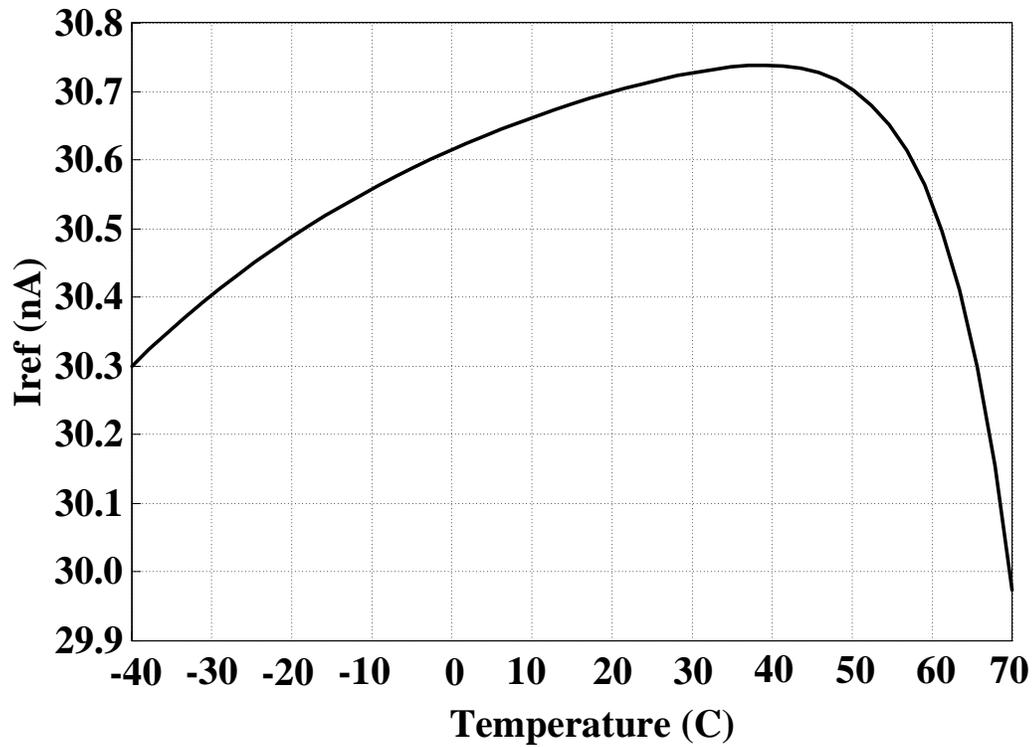


Fig. 5.3 Nano-ampere reference current as a function of temperature

5.2 Quiescent Current

The quiescent current I_q is the difference between the current drawn from the power supply (i.e., I_{in}) and the current delivered to the output load (i.e., I_{out}). It is measured as the current drawn from the power supply when there is no load (i.e., $R_L = \infty$). The quiescent current of regulator I is $18 \mu\text{A}$, and the quiescent current of regulator II is 270 nA .

5.3 Dropout Voltage

As discussed in Chapter 2, as the input voltage decreases and approaches the output voltage, the linear regulator would gradually leave the regulation region and starts to fail to regulate the output. The dropout voltage is defined as the difference between the input and output when the regulator starts to fail regulating. As for “when” the regulator “starts” to fail regulating, several different definitions and criteria exist. Here, we adopt the definition given by Texas Instruments, which says, “dropout voltage is defined as the differential voltage between V_{OUT} and V_{IN} when V_{OUT} drops 100 mV below the value measured with $V_{IN} = V_{OUT} + 1 \text{ V}$ ” [72].

At a load current of 104 mA , the out voltage of regulator I as a function of input voltage is shown as in Fig. 5.4, where the input voltage sweeps from 3 V down to 1.8 V . From Fig 5.4, the dropout voltage is calculated to be 190 mV .

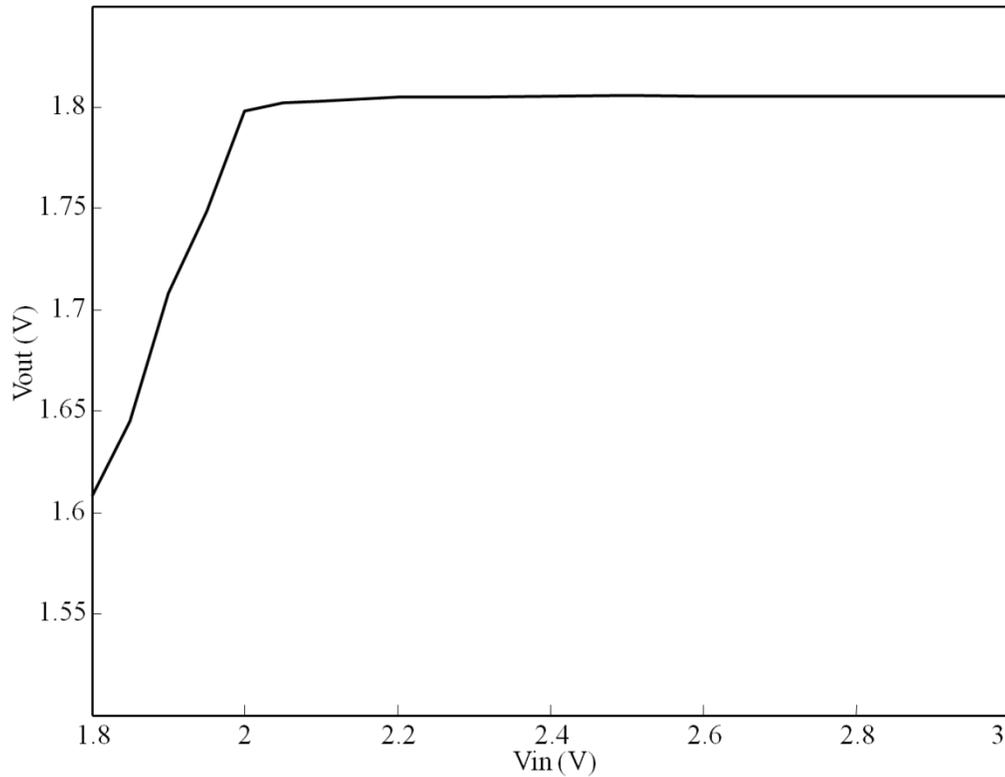


Fig. 5.4 Measured regulator I output voltage as a function of input voltage

The output voltage of regulator II as a function of the input voltage is shown as in Fig. 5.5. According to the dropout voltage definition given above, we need to measure the input voltage and output voltage difference when the output voltage is 1.7 V. However, even when we reduce the input voltage to 1.8 V, which is equal to the regulated output voltage, the output voltage is still above 1.7 V. Therefore, the dropout voltage definition does not apply to regulator II.

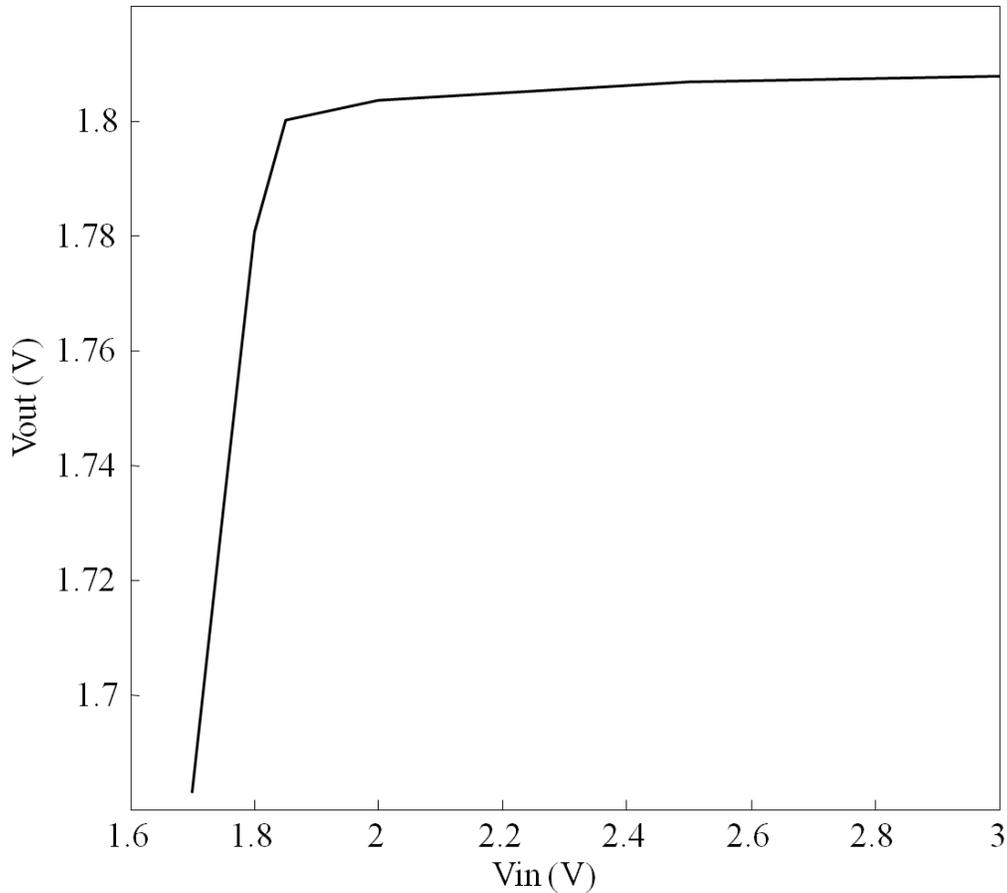


Fig. 5.5 Measured regulator II output voltage as a function of input voltage

5.4 Power Supply Rejection Ratio

Power supply rejection ratio (PSRR) measures how well a linear regulator rejects ripples from the power supply. One applies a small signal AC voltage at the input of the linear regulator which can be generated by a function generator, and then measures the magnitude of the output signal at all frequencies of interest. The PSRR can be calculated from the measured input AC signal and output AC signal. The PSRR at full load current (i.e., 104 mA) is shown as in Fig. 5.6. The PSRR in the whole frequency range of interest is larger than -10dB.

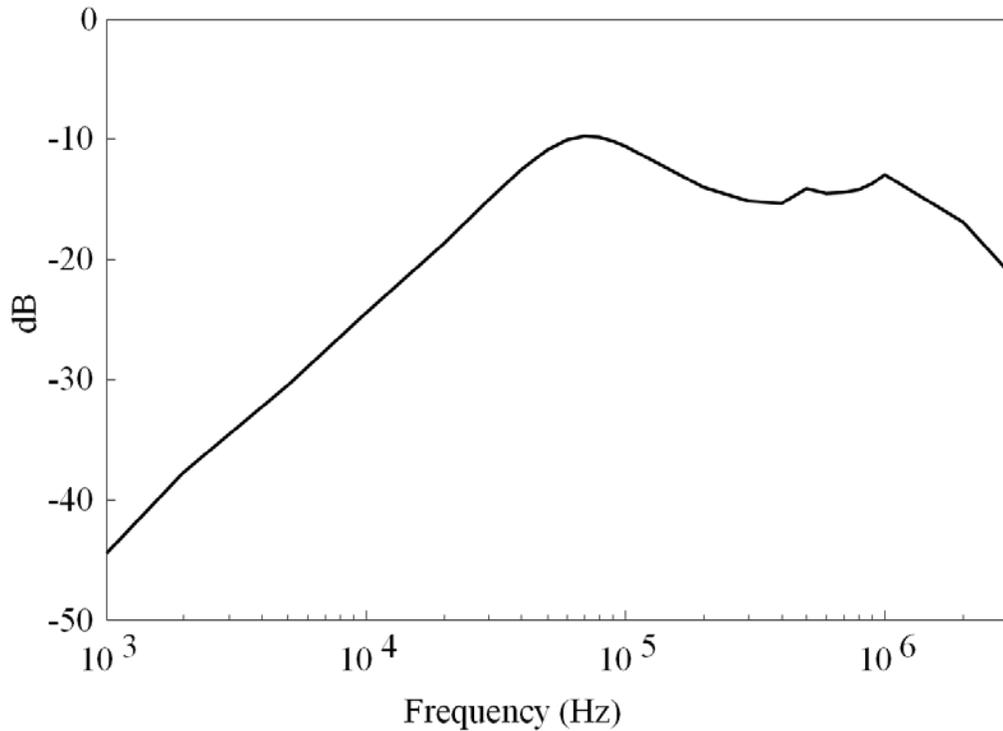


Fig. 5.6 PSRR at full load current

5.4 Line Transient Response

The line transient response measures how the output changes when a sudden change appears at the linear regulator input node. The line transient response measurement setup of a general linear regulator is shown as in Fig. 5.7, where the square pulse signal (step signal) is generated by a function generator. This pulse signal is then applied to the input of the regulator. To improve the current driving ability, sometimes a voltage buffer is needed between the function generator and the regulator. One of the probes of the oscilloscope is used to measure the input signal, and another probe is used to monitor the output node.

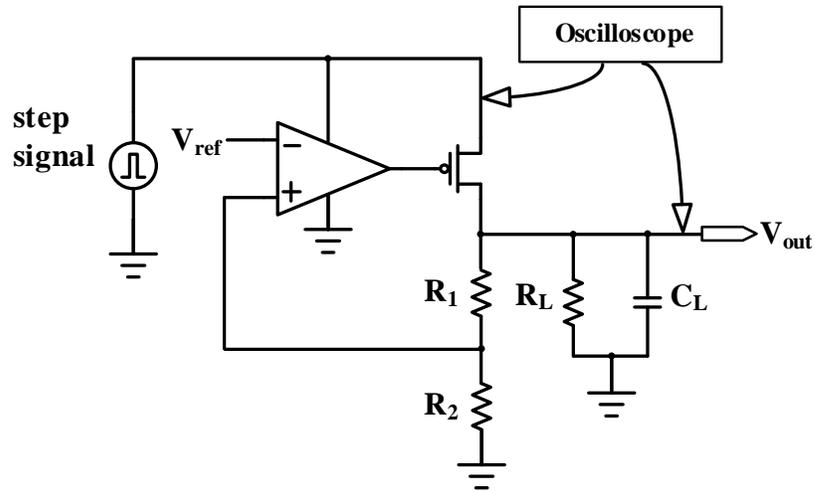


Fig. 5.7 Line transient response measurement setup

At a load current of 104 mA, the line transient response of regulator I is shown as in Fig. 5.8. The input voltage changes between 2.5 V to 3 V in 1 μ s and the output voltage spikes are within 30 mV when the supply voltage changes.

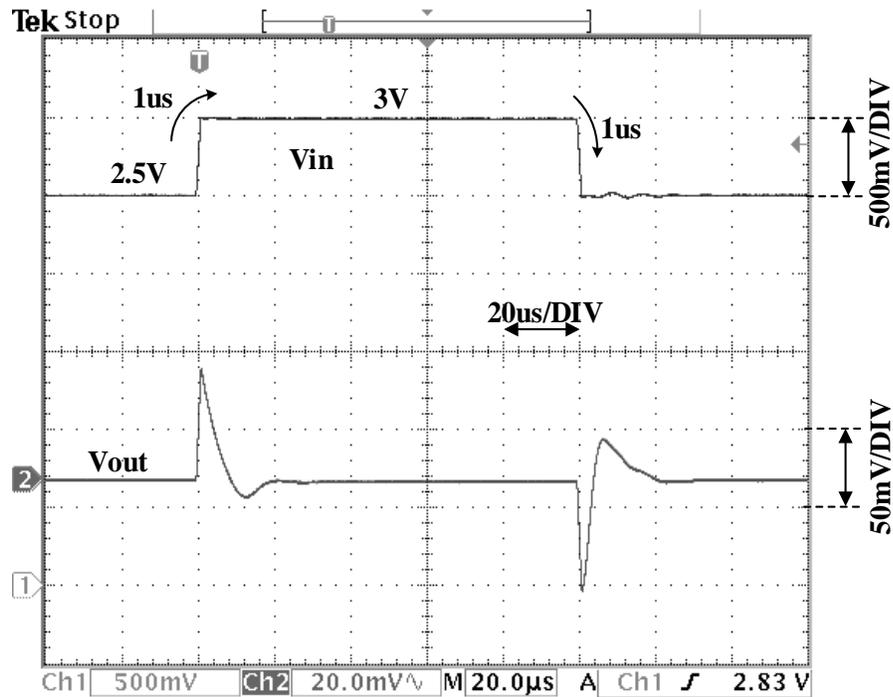


Fig. 5.8 Regulator I line transient response measurement result when the input voltage changes between 2.5V and 3V in 1 μ s at $I_L=104$ mA

Regulator II line transient response is shown as in Fig. 5.9, where the input voltage changes between 2.5 V to 3 V with an edge time of 1 μ s and the load current is 0.1 μ A. When the input voltage changes, the output voltage barely changes. The reason is because the load current is small and the 4.7 μ F large output capacitor can stabilize the output voltage even when a sudden change appears at the input. This undetectable output variation in the line transient response test can also be observed in the simulation result as shown in Fig. 5.10, where the input voltage changes between 2 V and 3 V in 1 μ s, but the output voltage change is within 0.5 mV, which is beyond the resolution of our oscilloscope.

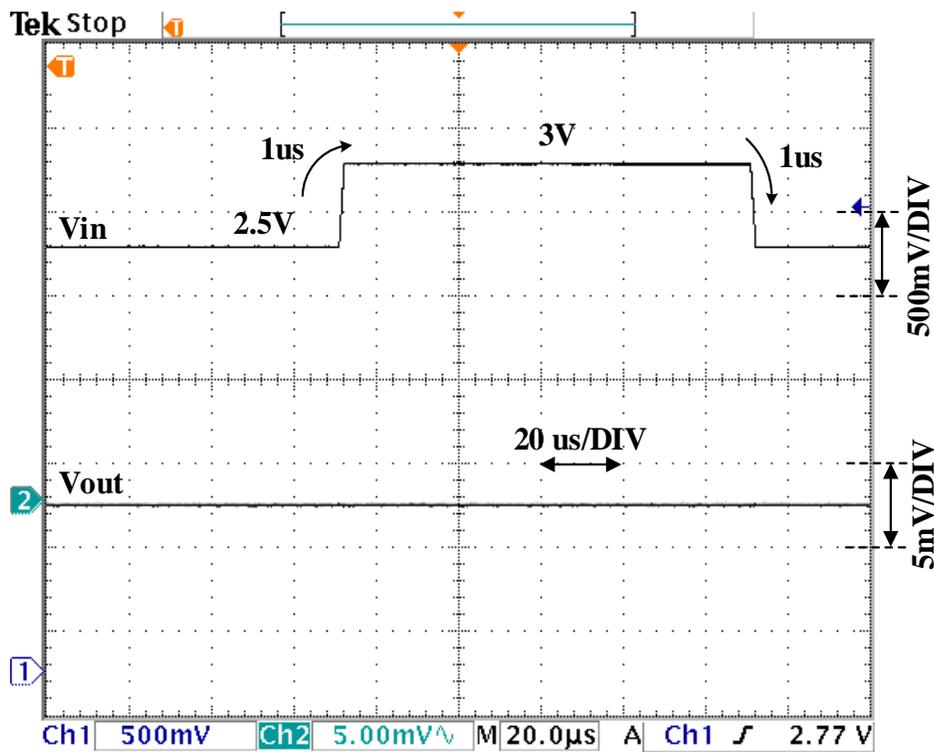


Fig. 5.9 Regulator II line transient response measurement result when the input voltage changes between 2.5V and 3V in 1 μ s at $I_L=0.1\mu$ A

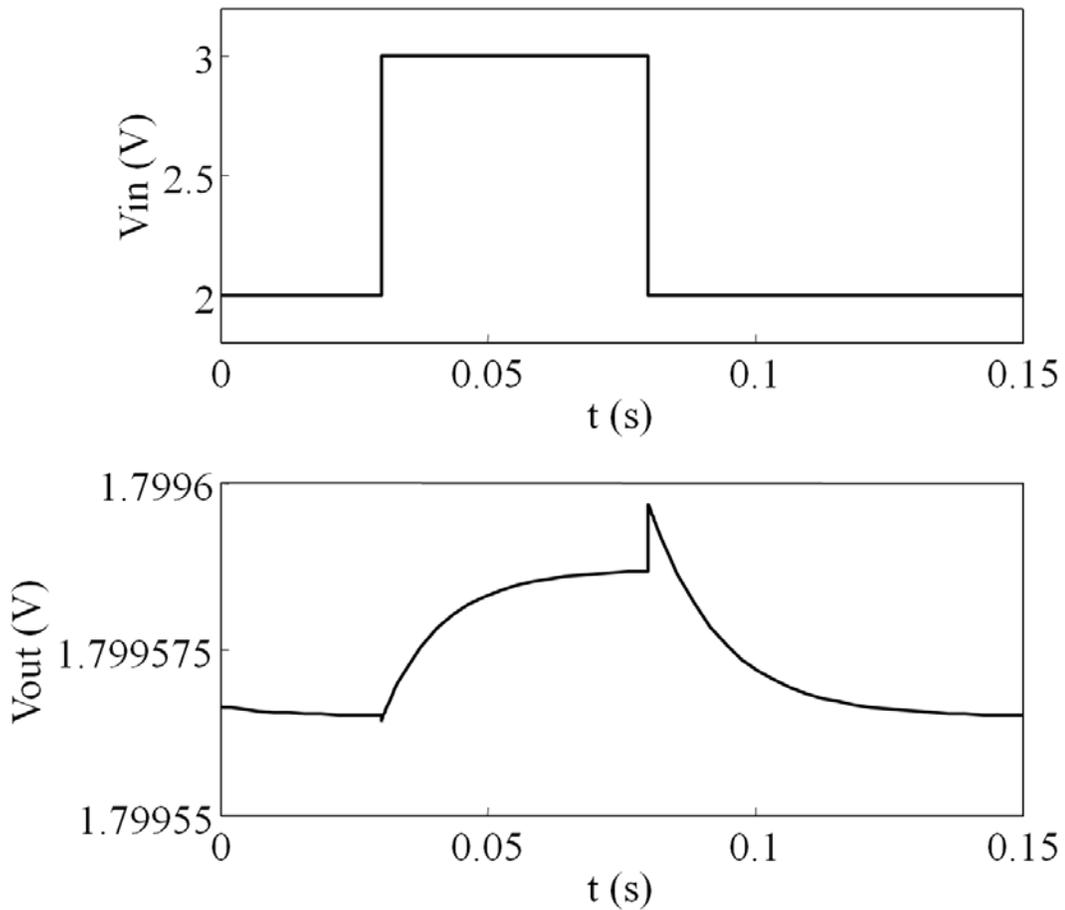


Fig. 5.10 Regulator II line transient response simulation result

5.5 Load Transient Response

Load transient response measures how the system reacts when there is a sudden change with the load current. In circuit simulations, this can be done by using a current source with pulsed signal waveform. In real chip measurements, the measurement can be taken by using switches to control the circuit to model the current change [73].

When the sensor node is in active mode, its current changes from 42 mA to 104 mA, and then the current goes back to 42 mA. So we need to measure how regulator I responds to these changes. The load transient response measurement setup is shown

as in Fig. 5.11. By turning ON and OFF of the control switch, we can control the load resistance to the regulator. The switch can be implemented using either an NMOS transistor or a PMOS transistor. We used a PMOS transistor in our experiment. When the control signal is at a high voltage, the switch is open and the load resistance seen by the regulator is R_{Load} ; when the control signal is at a low voltage, the switch is closed and the load resistance seen by the regulator is $R_{load} // R_{load}'$. Therefore, the load current pulse signal can be modeled by the voltage pulse signal $V_{control}$ from the function generator.

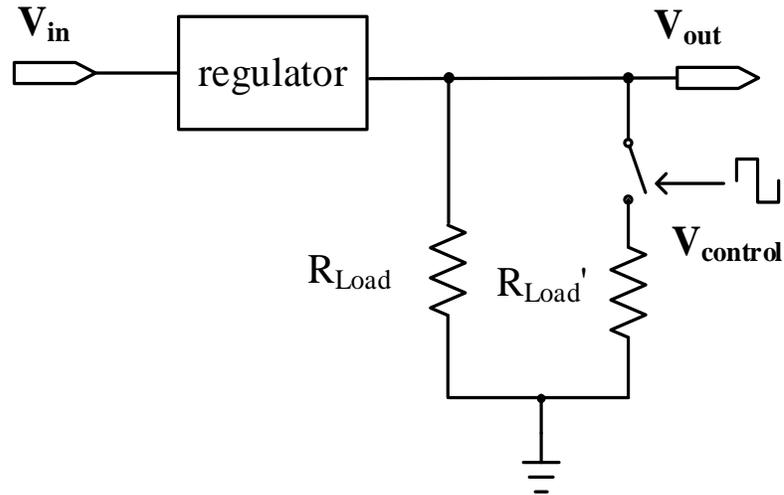


Fig. 5.11 Active mode load transient response measurement setup

The active mode load current transient response is shown as in Fig. 5.12. Since we are using a PMOS switch, therefore, when the control signal $V_{control}$ is at a low voltage, the equivalent load current is 104 mA; when the control signal $V_{control}$ is at a high voltage, the load current is 42 mA. Channel 1 is the load current waveform with an edge time of $1 \mu s$. Channel 2 is the measured output, which shows that the output voltage change is within 15 mV.

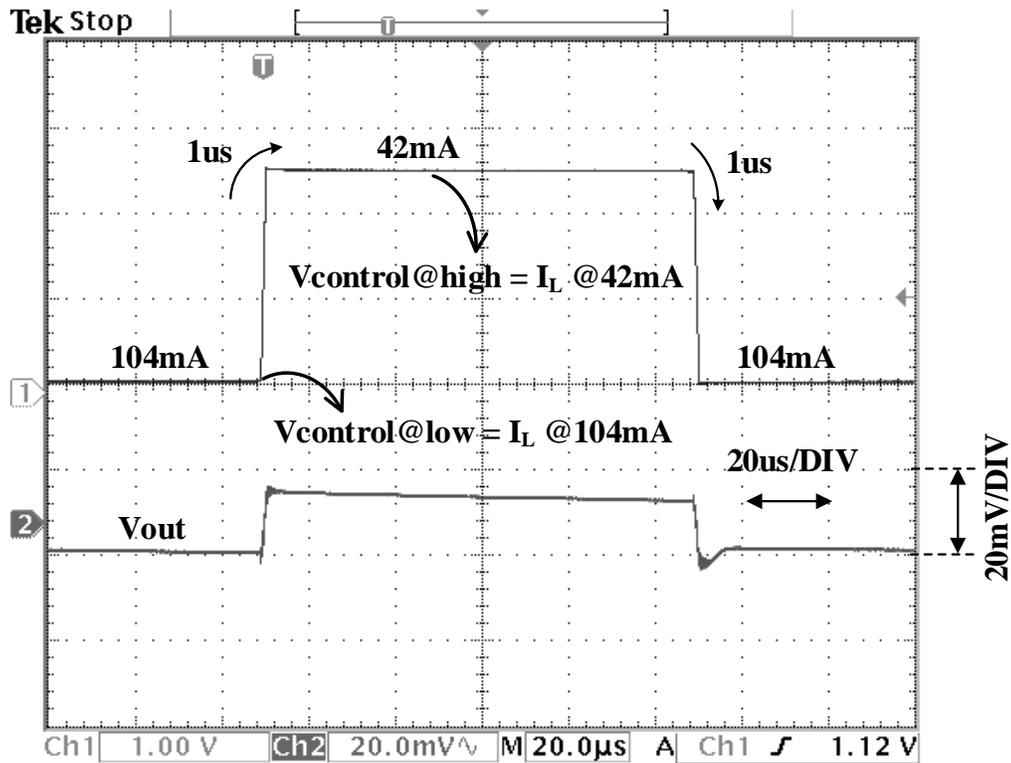


Fig. 5.12 Measured active mode load transient response when the load current switches between 42 mA and 104 mA with an edge time of 1us at 2.5V supply

In order to see how the system reacts when the sensor node changes between standby mode and active mode, we measured voltages at several different circuit nodes of the system. The measurement setup is shown as in Fig. 5.13. There are two groups of switches involved: switches M_{s1} and M_{s2} are part of the regulator system controlling the switching between standby mode and active mode, and switch S_L is used to model the load current change as we did in Fig. 5.11. These two groups of PMOS switches work in phase, i.e., they are all open or closed at the same time. Voltage V_1 is the measured actual supply voltage to regulator I during mode transition; voltage V_2 is the output voltage of regulator I; and V_{out} is the regulator system output voltage.

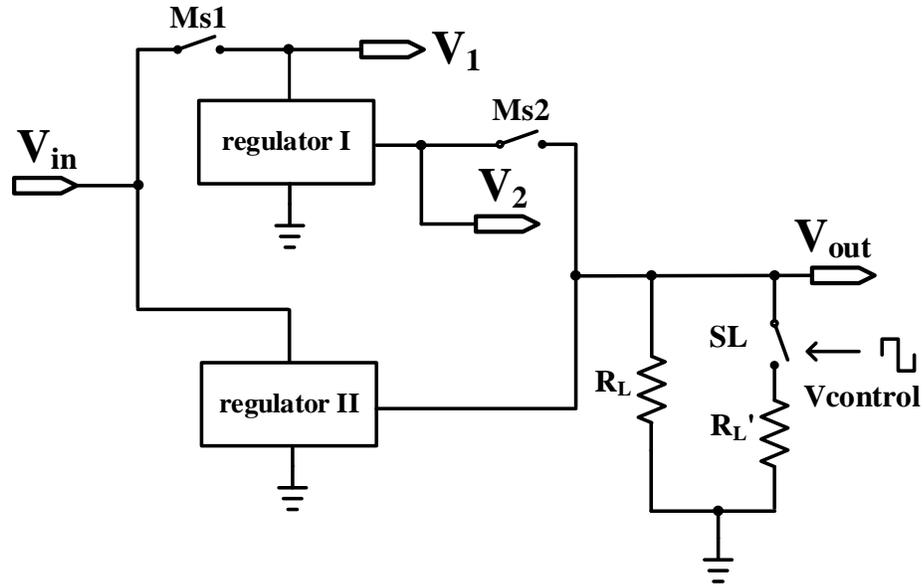
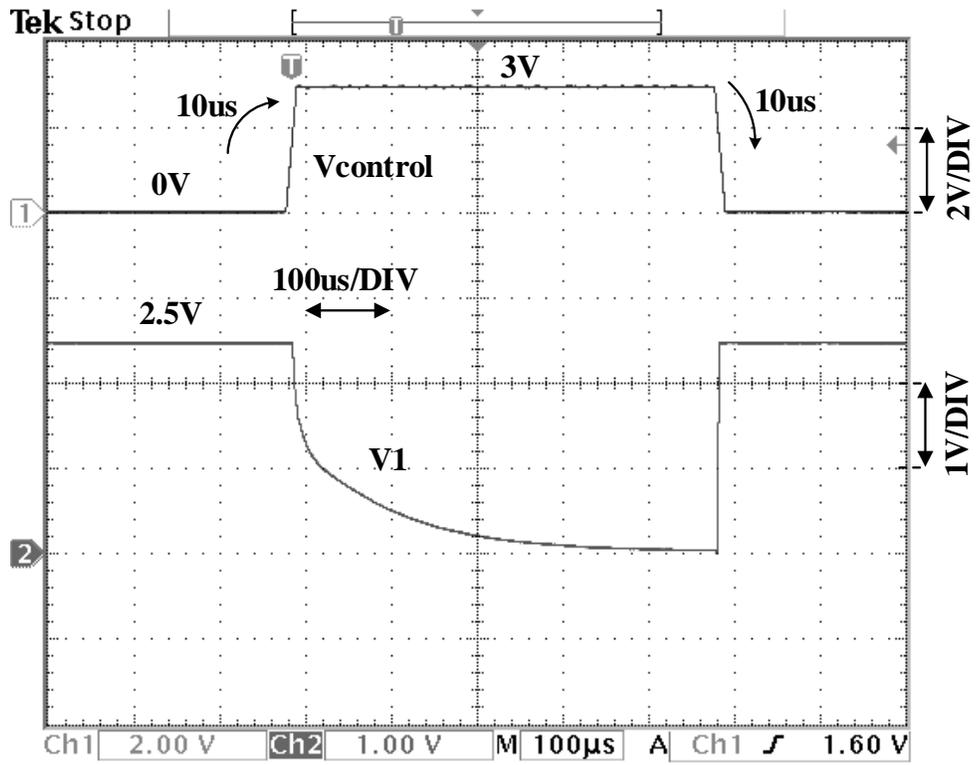


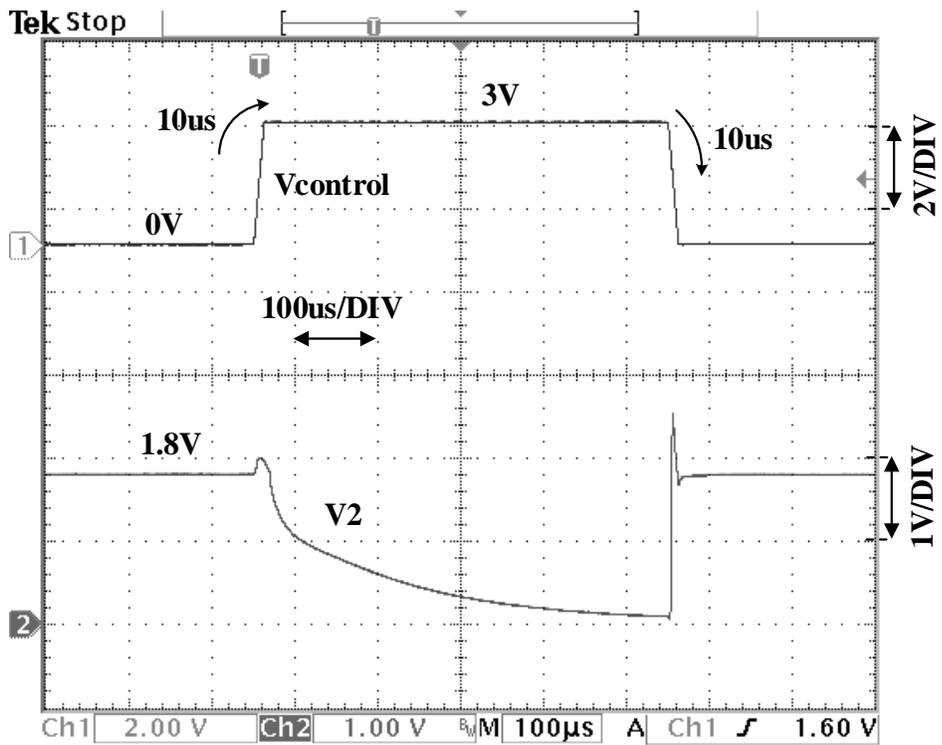
Fig. 5.13 Regulator measurement setup for the load switching between standby mode and active mode

The measured results of the voltages of the regulator system when the load current switches between sleep mode (i.e., $0.1 \mu\text{A}$) and active mode (i.e., 42 mA) are shown as in Fig. 5.14, where channel 1 of each graph is the voltage control signal $V_{control}$, and channel 2 of (a), (b) and (c) are the measured actual supply voltage to regulator I (i.e., V_1), the regulator I output voltage (i.e., V_2) and the regulator system output voltage (i.e., V_{out}), respectively. The regulator system input voltage is kept constant at 2.5 V .

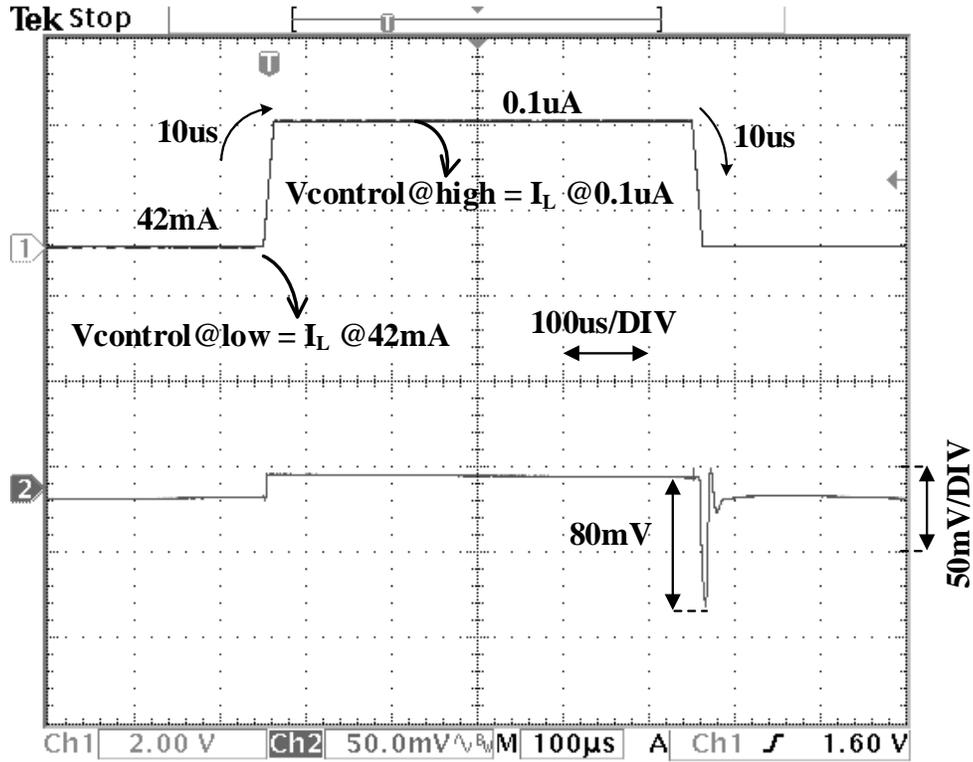
Similarly, since we are using PMOS switches, a high voltage control signal means all the switches are open, implying a small load current (i.e., the load is in standby mode); a low voltage control signal indicates a large load current (i.e., the load is in active mode).



(a)



(b)



(c)

Fig. 5.14 Measured load transient response when the load current switches between 0.1 μA and 42 mA in 10 μs with $V_{in}=2.5V$ (a) supply voltage V_1 to regulator I (b) regulator I output voltage V_2 (c) regulator system output voltage V_{out} to load

As shown in Fig. 5.14 (a), when the load current changes from 0.1 μA to 42 mA (the control signal $V_{control}$ changes from 0 V to 3 V), switch M_{s1} is turned ON, so regulator I is activated and the input voltage to regulator I V_1 increases to the level of the system supply voltage (i.e., 2.5 V). When the load current drops from 42 mA to 0.1 μA , switch M_{s1} is OFF and V_1 gradually drops. Fig. 5.14 (b) shows the output voltage of regulator I V_2 during the switching behavior. When the load current changes from 0.1 μA to 42 mA, regulator I is activated and this voltage increases to the targeted 1.8 V. When the load current changes from 42 mA to 0.1 μA , switch M_{s2}

turns OFF and regulator I is deactivated, so V_2 gradually drops. Fig. 5.14 (c) shows the system output voltage V_{out} to the load. When the load current changes between $0.1 \mu\text{A}$ and 42 mA , the output voltage variation is within 80 mV and the recovery time is within $35 \mu\text{s}$.

Therefore, the proposed regulator system successfully powered the sensor node with $0.27 \mu\text{A}$ quiescent current. When the sensor node switches between standby mode and active mode (the current switches between $0.1 \mu\text{A}$ and 42 mA), the recovery time is only $35 \mu\text{s}$.

The proposed regulator system which is composed of two linear regulators has been verified to achieve low quiescent current and good transient response. Simply using a single linear regulator with sub- μA range quiescent current to power the load might not be a good idea, as the transient response can be very terrible due to the tradeoff between quiescent current and transient response as discussed before. For example, as shown in Fig. 5.15, we designed a linear regulator consumes only about $0.2 \mu\text{A}$ quiescent current. But when the load current changes from $0.1 \mu\text{A}$ to 42 mA , the output voltage changes by more than 1 V , which definitely is unsuitable. The TPS78330 of Texas Instruments consumes $0.5 \mu\text{A}$ quiescent current, and when the load current switches between 0 and 10 mA , the output voltage change is about 100 mV , but the recovery time is more than 10 ms as shown in Fig. 5.16 [49], which is too slow.

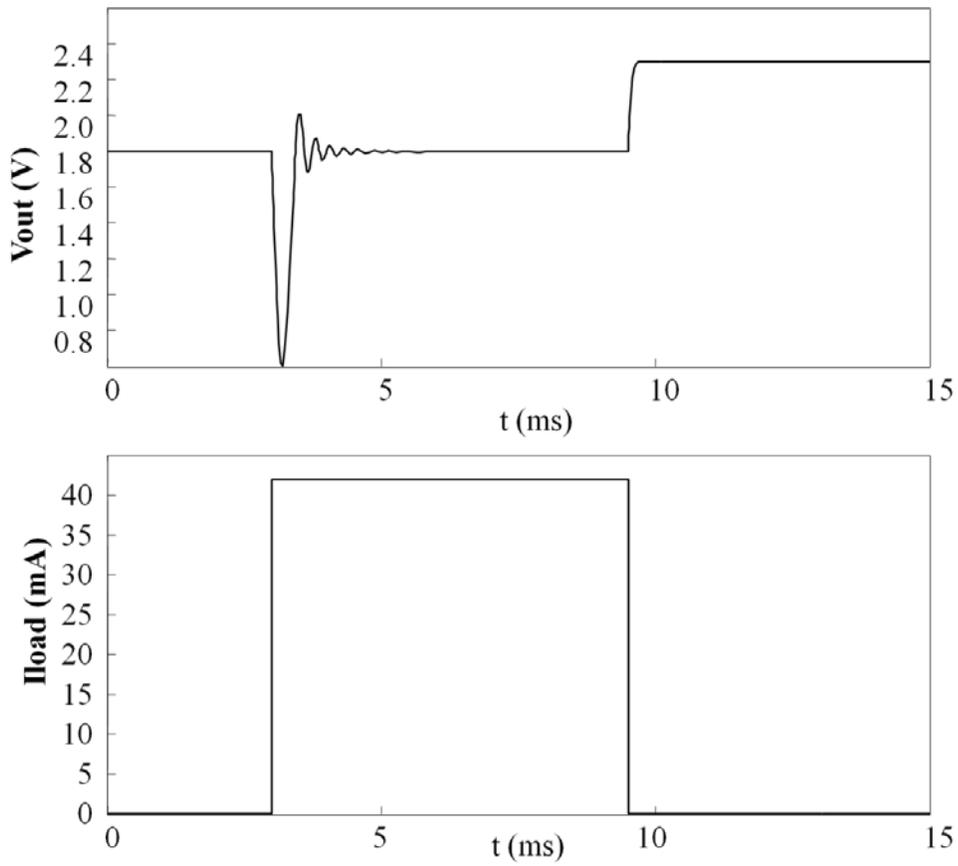


Fig. 5.15 Load transient response of a linear regulator with 0.2 uA quiescent current

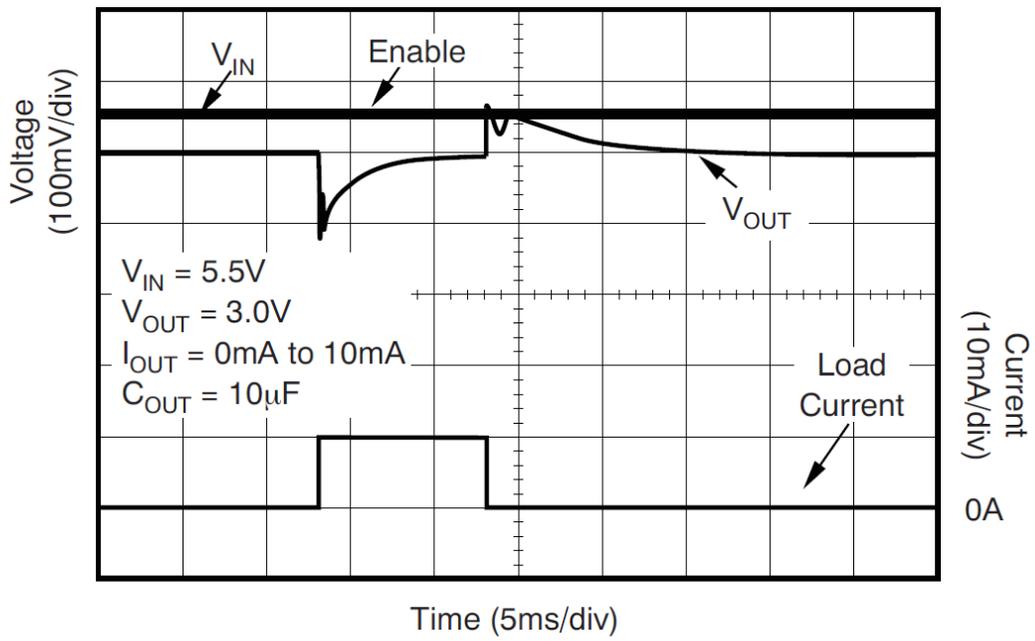


Fig. 5.16 TPS78330 load transient response test result

5.6 Performance Comparison

In an energy harvesting system, due to the low incoming power level, the quiescent current of the linear regulator should be kept extremely low. However, there is always a tradeoff between the quiescent current and transient response. By switching between the two composing LDO regulators based on the sensor node working mode information, the proposed system topology described here eliminates the tradeoff between low quiescent current and fast transient response. A comparison between the proposed regulator system and previous designs is shown as in Table 5.1. Compared to those designs in Table 5.1, even though we did not use an advanced fabrication process, our proposed regulator system has much lower quiescent current and comparable transient response. Due to its ultra-low quiescent current, this regulator system is well suited to those wireless sensor networks powered by energy harvesting.

Table 5.1 A comparison of the performance of the linear regulators

Parameter	[44]	[45]	[46]	[74]	This work
Technology(um)	0.35	0.065	0.35	0.09	0.5
V _{out} (V)	0.9	1	1.8	0.9	1.8
V _{do} (mV)	100	200	200	100	190
I _{L,max} (mA)	50	100	100	50	104
I _q (uA)	1.2	0.9-82.4	4	9.3	0.27
ΔV _{out} (mV)	about 400	68.8	55	about 10	80*

* Load current changes between 0.1uA and 42mA (not full load current). For other works in Table 5.1, load currents change between zero and full load currents

5.7 Conclusion and Discussion

In this Chapter, we performed various tests with the proposed voltage regulator system including quiescent current, dropout voltage, PSRR, line transient response, load transient response, etc. The voltage regulator system is proven to be extremely low quiescent. Combining the low dropout voltage, this voltage regulator system can give us high power efficiency and well suits the energy harvesting system. More importantly, the proposed voltage regulator system eliminates the tradeoff between quiescent current and transient response. Therefore, great transient response performance has also been achieved. When the load current changes by more than 5 orders of magnitude, the settling time is only 35 μs , and the output voltage variation is within 80 mV.

In those line transient response and load transient response tests, we are considering the extremely worst cases. For example, in the load transient response, the load current switches between 42 mA and 0.1 μA in 10 μs , and between 104 mA and 42 mA in 1 μs . In reality, the sensor node usually will not switch over such an enormous current range in such a short time. If the sensor node is consuming sub- μA range current, it means the sensor node is in extremely low power mode with almost all the functional blocks OFF (e.g., the transceiver, the microcontroller, etc.). If the sensor node is consuming dozens of mA current, it dictates that the sensor node is in high power mode and possibly transmitting/receiving signals. In this case, microcontroller and the transceiver are ON. For the microcontroller and the transceiver to switch from OFF to ON, it often takes a relatively time, and usually a few μs is not enough. For example, the CC2500 of Texas Instruments (which is going

to be used in following experiments) takes about $240 \mu\text{s}$ to change from sleep mode into receiving or transmitting mode. In the line transient response experiments, the input voltages change by 1 V in $1 \mu\text{s}$. Also, this kind of change hardly appears in the real situation.

All in all, the proposed voltage regulator system has been proven to successfully function in the worst case considerations. The proposed system achieves low quiescent current, low dropout voltage, and fast transient response with small output voltage variation at the same time.

Chapter 6: Experiments of the RF Energy Harvesting System

The various ambient energies available in the environment powering the small-scale electronics and systems are as shown in Fig. 6.1 [75]. Those ambient energies can be classified into 5 categories: Optical, kinetic, thermal, electromagnetic, and biochemical. Optical energy sources include solar energy from the sun and artificial lights. Kinetic energies result from the moving and vibrations of objects, etc. Thermal energies result from the heat. Electromagnetic energies result from electromagnetic waves. Biochemical energies come from the electrochemical reactions. Those energy forms cannot be directly used to power the small electronics and systems, so energy transducers are needed to convert them into electrical energies [76].

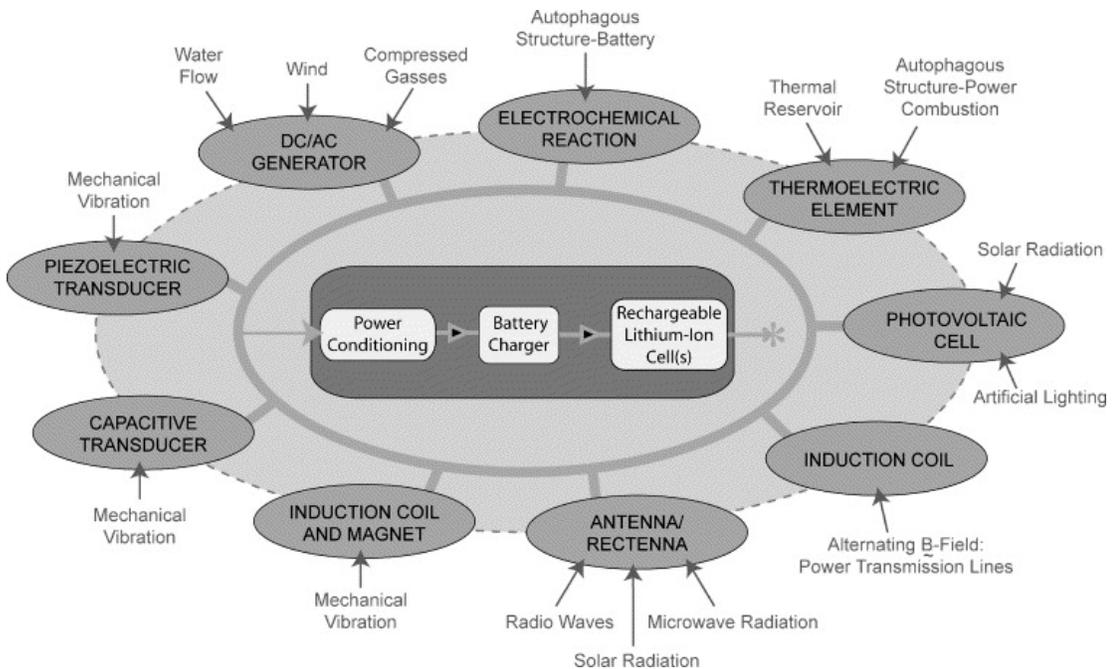


Fig. 6.1 Various ambient energies available in the environment for powering small-scale electronics and systems. Adapted from [75]

The optical energy (i.e., solar energy) power densities in outdoors and indoors can be quite different. Optical energies outdoors mainly come from the sun, and the power densities depends on the weather conditions (i.e., sunny or cloudy), latitude, the time (i.e., summer or winter, and noon or afternoon), etc. It is claimed that at a sunny noon, the solar energy power density can be about 100 mW/cm^2 [75]. The indoor optical energy power density depends on the strength of the source, and distance to the source, etc. It is studied that with a distance of 15 inches from a 60 W bulb, the power density in door is about $567 \mu\text{W/cm}^2$ [77]. And generally the power density indoor is a few $\mu\text{W/cm}^2$ (e.g., $6 \mu\text{W/cm}^2$ [78]).

Kinetic energy harvesting system can convert the kinetic energy into electrical energy by using piezoelectric and electromagnetic components [79]. Depending on the objects and strengths of vibrations, the power density of kinetic energies can differ. For example, the power density from piezoelectronic conversion and electrostatic conversion are about $250 \mu\text{W/cm}^2$ and $50 \mu\text{W/cm}^2$, respectively [78]. Researchers also tried to harvest energies from the shoes when people walk [80], it shown that the power density is about $330 \mu\text{W/cm}^2$.

Thermal energies can also be utilized by thermoelectric transducers to power small electronics. An electrical output voltage can be obtained by connecting several PN junctions with thermal gradients. In [81], it is shown that the power density is $60 \mu\text{W/cm}^2$ for a 5°C temperature difference.

Biochemical energies can be harvested by using fuel cells where the fuel is fed to the anode and the oxidant is fed to the cathode [76]. The fuel can be enzymes, glucose, microbes [76]. It is reported that a power density of $2 \mu\text{W/cm}^2$ has been

achieved for glucose fuel cells [82], and the implanted bio-fuel cell in a living snail is $30 \mu\text{W}/\text{cm}^2$ [83].

The radio waves from various transmitters including the base stations, cell phones and handheld devices can be captured to power electronics. Considering the increasing number of transmitters, RF energies are becoming more and more ubiquitous. Besides, the performance is not affected by weather or time of the day. One main problem with energy harvesting is the low power density. For example, the available power from a 3W transmitter is only a few mW within a few feet, and it goes to tens of μW at around 40 feet [84]. It is found that the RF power densities outdoor and indoor are a few $\mu\text{W}/\text{cm}^2$ [85].

In the following sections, we are focusing on the RF energy harvesting system. The major components and their structures would be discussed, also experiments are carried out on the components and the whole system.

6.1 Rectenna Design and Experiments

To harvest the RF energies in the environment, an antenna is needed to convert the radio waves into electric power for usage. Since we are aiming at harvesting a wide frequency range RF signals in the environment, a wideband antenna is desirable. According to [86], the antenna performance is independent of the frequency if its shape is specified entirely by its angles.

Besides the antenna, a rectifier is also desirable because RF signals are AC which cannot be directly used by the following electronic components. A rectifier is capable of converting an AC voltage into DC. A rectifier can be implemented using a

Schottky diode because of its low turn on voltage and fast transit time as compared to PN junction diodes [76].

A rectenna is an antenna/rectifier assembly which is able to capture RF signals and generate a DC voltage [87]. A rectenna array has been fabricated is characterized over a frequency range of 2-18 GHz [10], and its photograph is shown as in Fig. 6.2. This array has 16 left-handed and right-handed circularly polarized spiral elements. Each element is connected to a Schottky rectification diode. As a result, after rectification, the DC currents and voltages would sum up together to power the load. The shape of each antenna element is shown as in Fig. 6.3 [9].



Fig. 6.2 A broad band rectenna array [10]

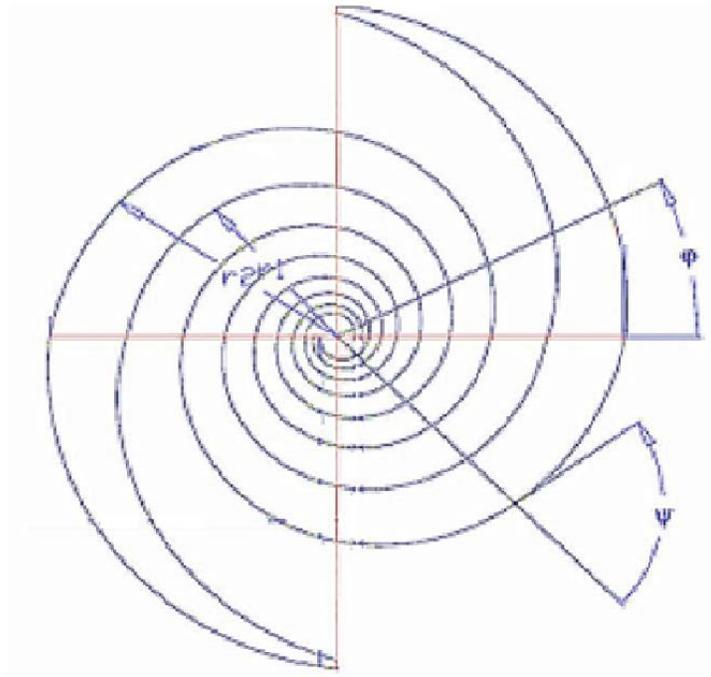


Fig. 6.3 Antenna shape [9]

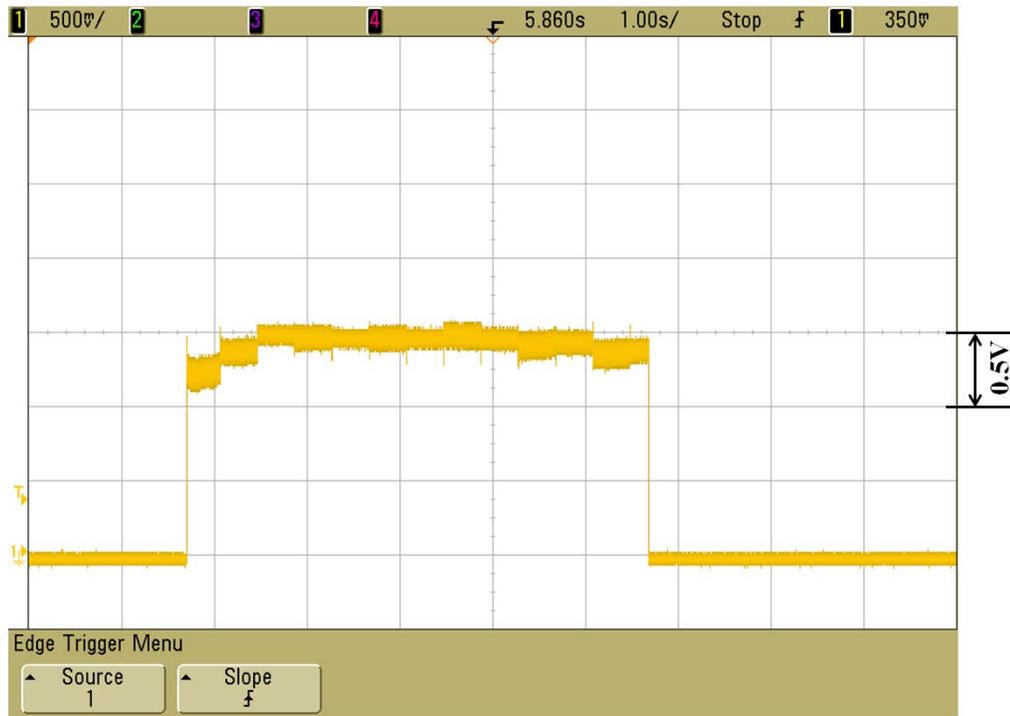


Fig. 6.4 Test result of the rectenna harvesting 900MHz RF signal of a walkie talkie

The rectenna has been tested using a TriSquare TSX300 eXRS walkie talkie [88] as the energy source. This walkie talkie operates in the 900 MHz frequency range with. The walkie talkie is placed 0.5 meters away from the rectenna array. From the measured result shown as in Fig. 6.4, the rectenna is capable of capturing the 900 MHz signal and output a voltage of about 1.5 V.

We have also tested the operation of the rectenna using a cell phone (model: HTC One X) as the power source working in different conditions: sending out Bluetooth signal, sending a text message, making a phone call. The measured results are shown as in Fig. 6.5, Fig. 6.6 and Fig. 6.7, respectively.

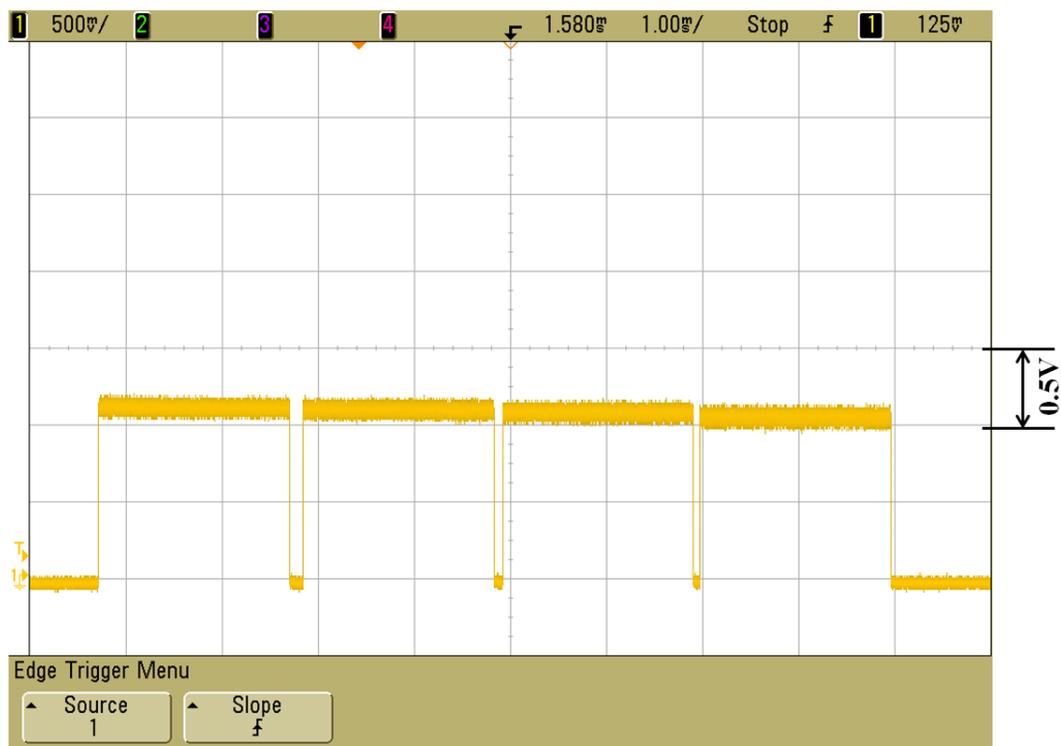


Fig. 6.5 Test result of the rectenna harvesting RF energy of a cell phone sending Bluetooth signal

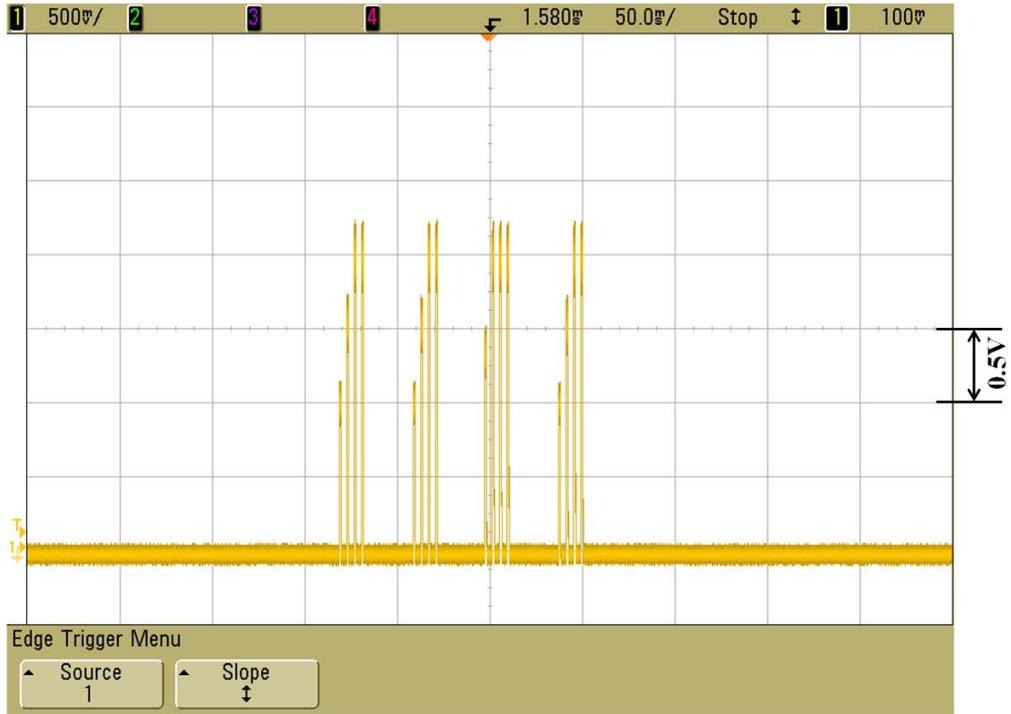


Fig. 6.6 Result of the rectenna harvesting energy of a cell phone sending a message

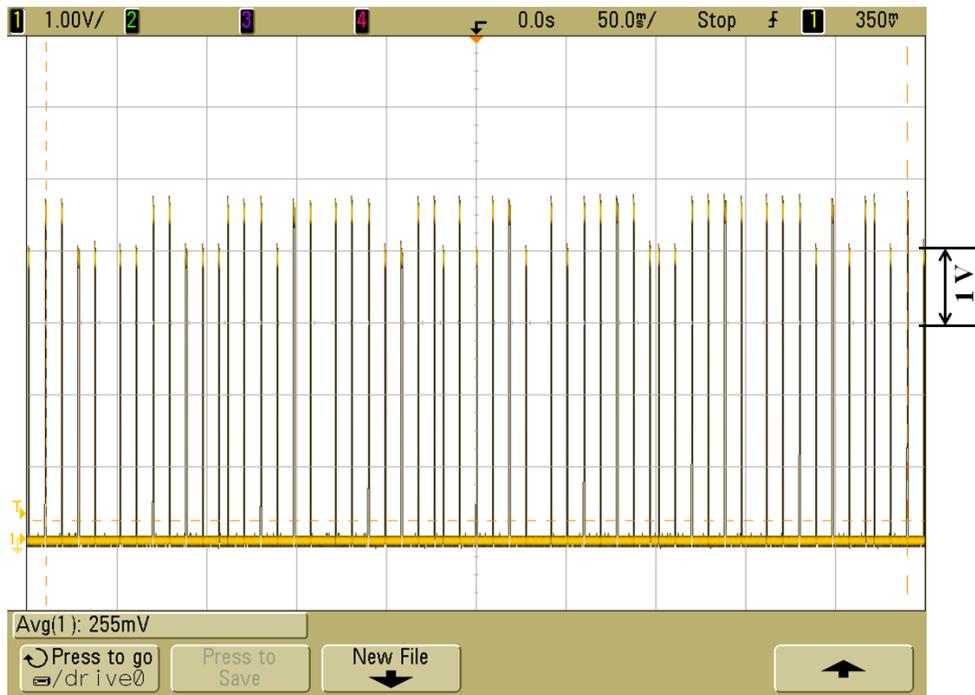


Fig. 6.7 Test result of the rectenna harvesting RF energy of a cell phone making a phone call

In conclusion, we have performed experiments with fabricated rectenna using the walkie talkie and the cell phone as the energy sources. Those experimental results clearly demonstrate that the fabricated rectenna is capable of harvesting RF energies from various signal sources in the environment and converting them into DC voltages.

6.2 Flexible Battery Fabrication and Tests

Because the power levels of the RF signals fluctuate, an energy storage device is therefore needed to store the energy when the RF power density is high and release the energy later when the RF power density is low. Besides, an energy storage device can also help to smooth the voltage.

A Li-ion battery usually requires a charging voltage above 4 V, in contrast, the cell of FlexEl can be charged at a voltage below 1.2 V, which makes them very attractive in an energy harvesting system. Besides, the cell has a capacity as high as 84.4 mAh/cm² [89].

An ultra-high capacity semi-fuel cell operating with sea water has recently been developed by FlexEl, LLC. The cell uses hydrated ruthenium oxide (RuO₂•nH₂O) as part of the cathode, and the metallic materials like zinc and magnesium as the anode. The hydrated ruthenium oxide is a nano-powder with large surface area up to 340m²/g, it acts as a catalyst to break apart sea water into hydrogen and oxygen (the “fuel” of the cell). The relatively expensive hydrated ruthenium oxide is compounded with and “diluted” with the inexpensive activated carbon. As a result, the cathode becomes cheaper due to the “dilution”, besides, the ohmic resistance of the compound drops by a more than 6 orders of magnitude as compared to pure hydrated ruthenium oxide [11].

The semi-fuel cell is shown as in Fig. 6.8. Structures of the galvanic cell, semi-fuel cell and fuel-cell are also shown in Fig. 6.8 for a comparison.

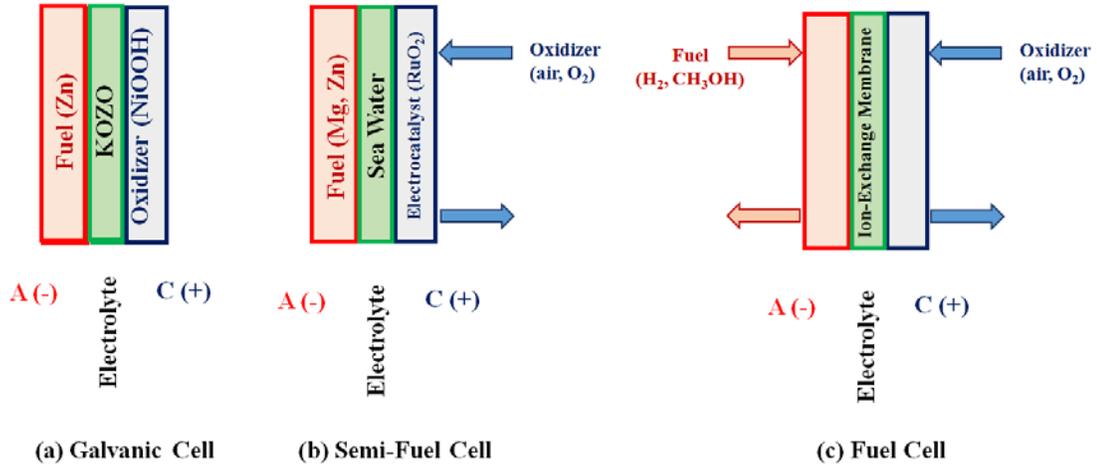
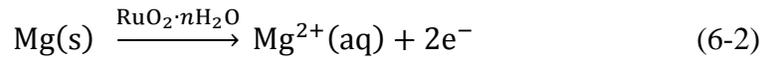
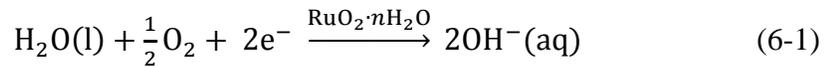


Fig. 6.8 (a) galvanic cell (b) semi-fuel cell (c) fuel cell. Courtesy of Dr. Daniel Lowy

The chemical reaction of the cathode of the semi-fuel cell is described as in equation (6-1). Using the metallic magnesium as the anode, the chemical reaction of the anode is shown as in equation (6-2). The steps of manufacturing the hydrated ruthenium oxide are shown as in Fig. 6.9.



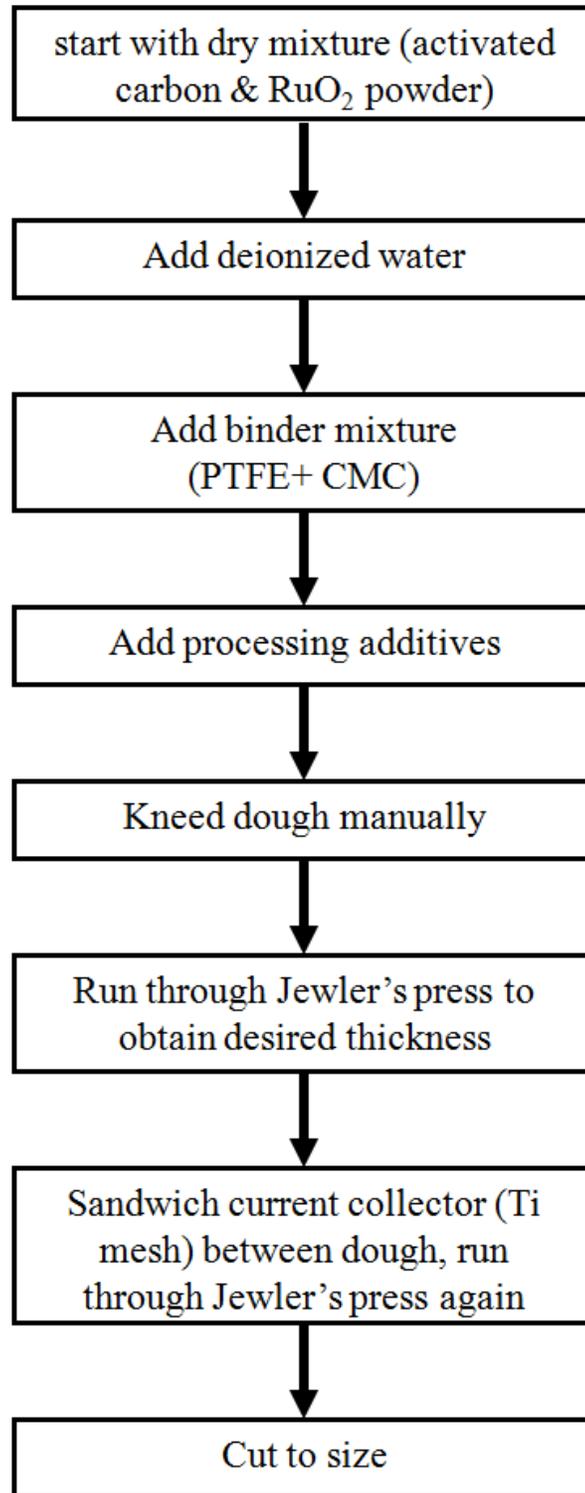


Fig. 6.9 Manufacturing processes of the hydrated ruthenium oxide. Courtesy of

FlexEl, LLC

To study the sea water battery performance, we applied the load to the battery and carried out the load testing. The protocol is: the sea water battery is first discharged at 30 mA for 3 ms, and then is discharged at 100 μ A for 5 minutes. We repeat this procedure until the battery fails. The measurement says that the battery sustained in this protocol for 12 hours. The measured result of the battery output voltage in the first few hours is shown as in Fig. 6.10.

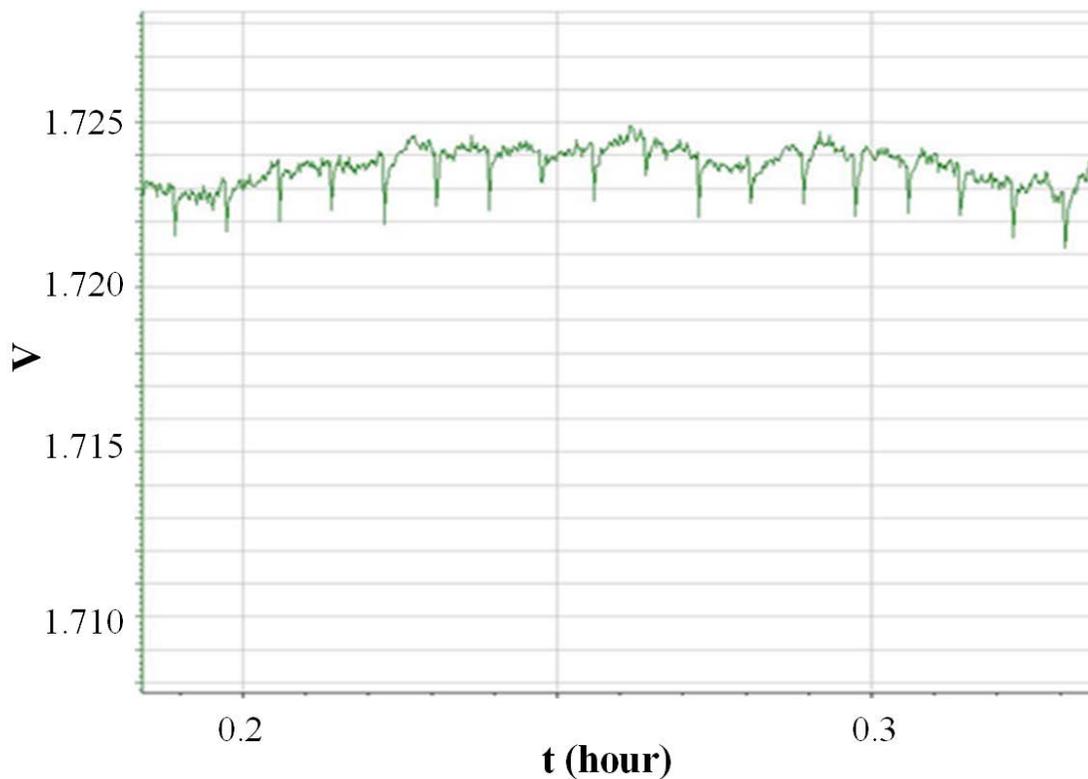


Fig. 6.10 Load testing result of the sea water battery. Courtesy of Dr. Daniel Lowy

6.3 Wireless Sensor Node

The eZ430-RF2500 is a complete wireless development tool incorporates all the necessary hardware and software tools to evaluate the MSP430F2274 microcontroller and CC2500 2.4 GHz transceiver [90]. The MSP430F2274 is a 16-bit RISC processor and 200-ksps 10-bit SAR ADC. It has five low power modes, and it

consumes only 270 μA current in active mode and 0.7 μA in the lowest power mode. CC2500 is a 2.4 GHz RF transceiver with temperature sensors which consumes about 14.5 mA-19.6 mA current in receiving mode, 11.1 mA-21.5 mA in transmitting mode, and 0.4 μA in lowest power down mode. The photographs of the eZ430-RF2500 are shown as in Fig. 6.11.

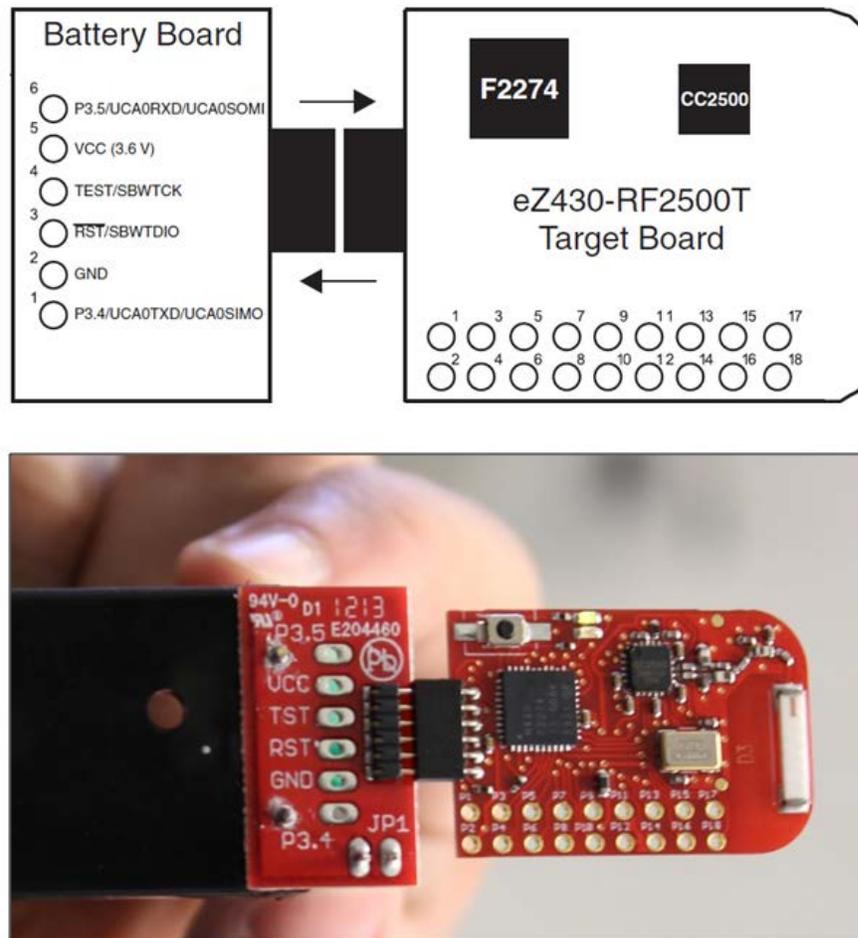


Fig. 6.11 eZ430-RF2500 photograph

The temperature sensors of the CC2500 are capable of sensing the environmental temperatures. The sampled data can be transmitted through the built-in transceiver of CC2500. The eZ430-RF2500 is preloaded with a wireless sensor network firmware. It has an access point so that it can measure its own temperature

and at the same time it can receive temperature measurement results from other end devices. The measured temperature results would be transmitted to the PC for data visualization.

6.4 System Test Results and Discussions

Because the output voltage level of the FlexEl battery is below the operating input voltage range of the sensor node, a boost converter (LT1615-1 of Linear Technology [91]) has been used to boost the voltage to power the sensor node. This boost converter can be operated at a supply voltage down to 1 V with an adjustable output voltage up to 36 V. Its quiescent current is only 20 μA at no load.

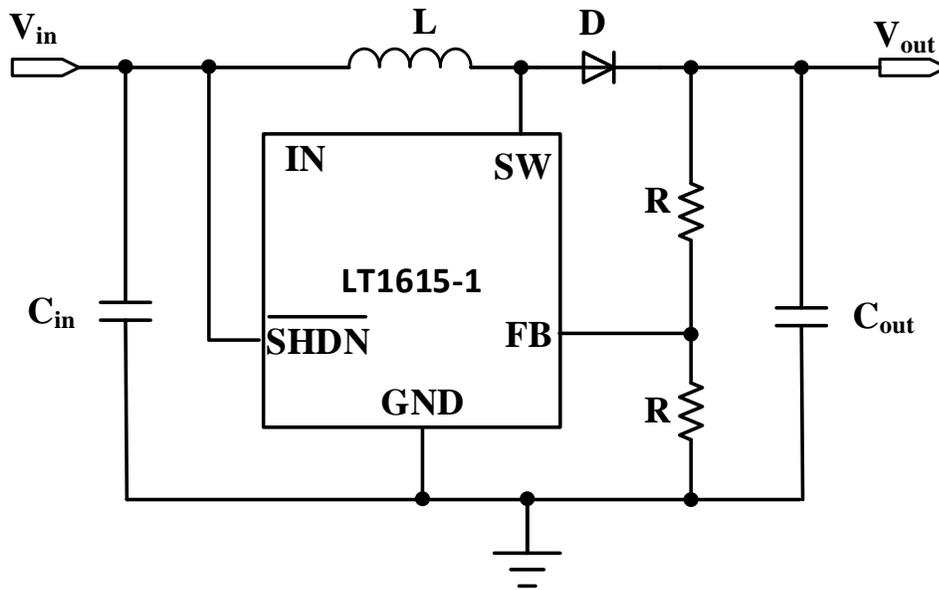


Fig. 6.12 The usage diagram of LT1615-1

The usage of the LT1615-1 is shown as in Fig. 6.12, where V_{in} connects to the battery output, and V_{out} is the output voltage to the sensor node. C_{in} is the input filtering capacitor, C_{out} is the output capacitor, L is the inductor, D is the diode, and two resistors form the feedback network. All of them are external components to the

chip LT1615-1. The voltage at the feedback pin of LT1615-1 is fixed about 1.23 V, so by changing the two feedback resistors, one can set the output voltage.

The energy harvesting system including the FlexEl sea water battery and eZ430-RF2500 sensor node has been tested. The sea water battery contains about 200 mL of the sea water, and the total weight of the anode/cathode is 34 g mass, the dimension is 9.0 cm x 6.0 cm x 0.85 cm dimension. The open circuit voltage of the battery is 1.9 V, and it can provide a maximal burst current up to 2.2 A. The sea water battery used in our experiment is shown as in Fig. 6.13.

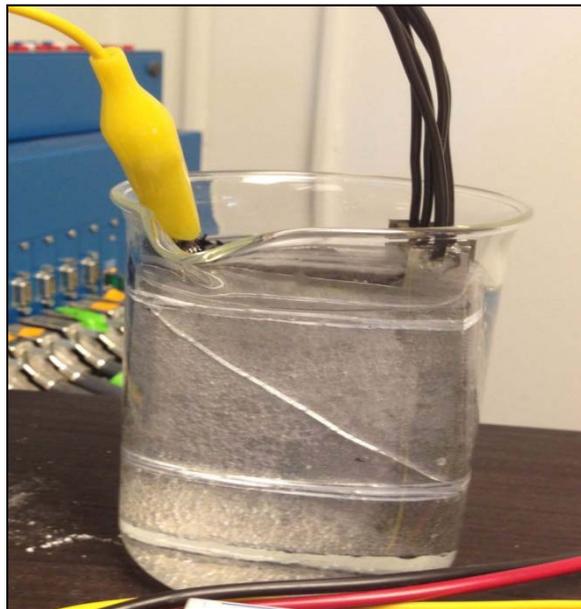


Fig. 6.13 Sea water battery of our energy harvesting system. Courtesy of FlexEl, LLC

The battery output voltage and the supply voltage to the sensor node in the experiment are shown as in Fig. 6.14 and Fig. 6.15, respectively. The sampling period of the voltages is once per 20 seconds, i.e., the measurement tool automatically measures the output voltage and the supply voltage to the sensor node once every 20 seconds.

As shown in Fig. 6.14, the battery output voltage gradually drops as it discharges to power the load, and the battery successfully powered the load for about 145 hours. After that, the battery voltage drops below 1 V, which is not high enough to power the boost converter, as a result, the system stops.

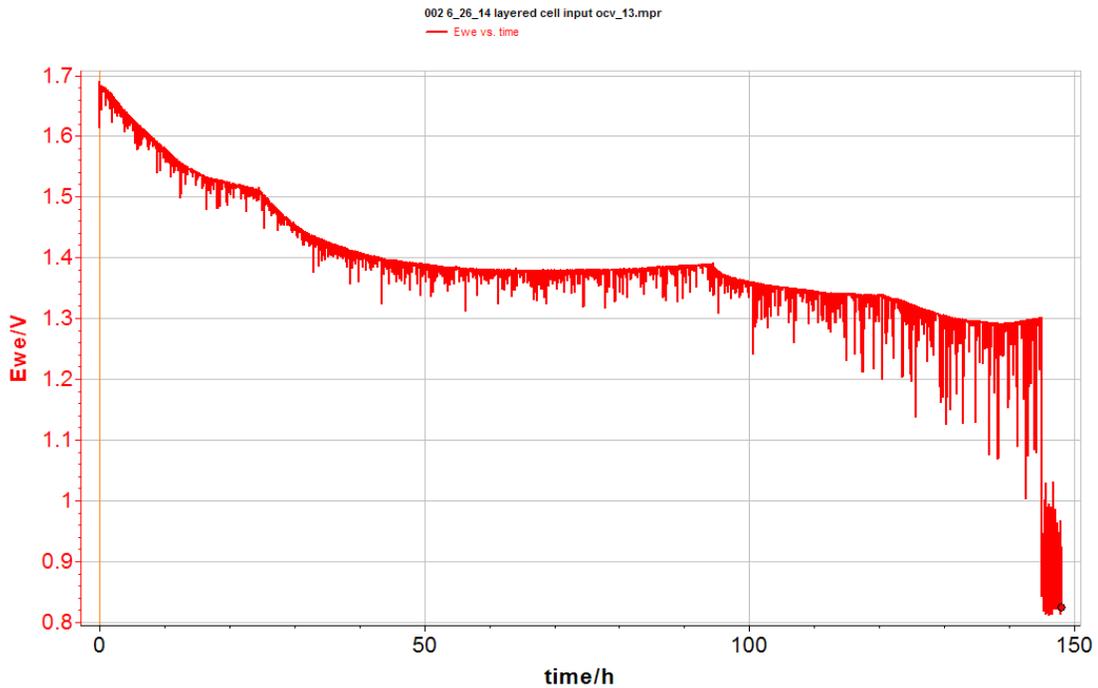


Fig. 6.14 Measured result of the battery output voltage when powering the wireless sensor node eZ430-RF2500

The supply voltage to the sensor node is set by the boost converter. The voltage at the feedback pin of LT1615-1 is fixed at about 1.23 V, and the two feedback resistors have equal values, therefore, the output voltage of the boost converter is set to 2.46 V. This output voltage is also the input voltage to the sensor node. As shown in Fig. 6.15, the supply voltage to the sensor node generally is at around 2.46 V.

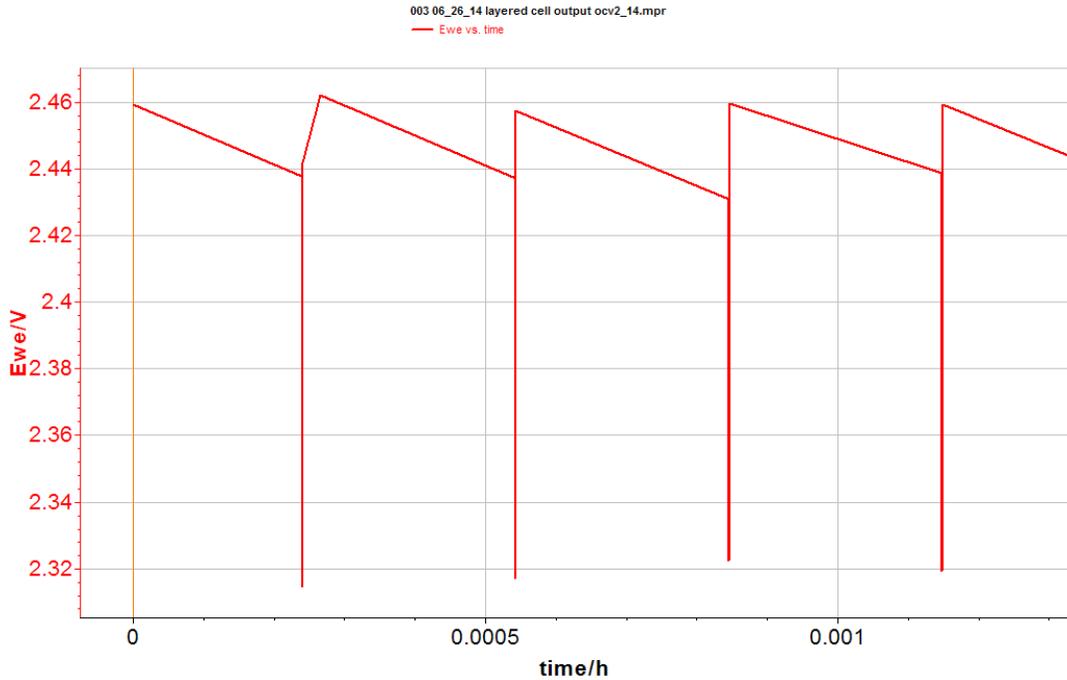


Fig. 6.15 Measured result of the supply voltage to the wireless sensor node eZ430-RF2500 (also the output voltage of the boost converter)

The environmental temperature is sampled by the sensor node and then the data are transmitted to the access point. The measured data are visually displaced on the computer screen as shown in Fig. 6.16. The big bubble shows the temperature of the environment where the sensor node resides (i.e., 73.5°F). Besides, it also displays the supply voltage to this sensor node (i.e., 2.5 V). The small bubble is displaying the temperature of the access point (i.e., 87.9°F).

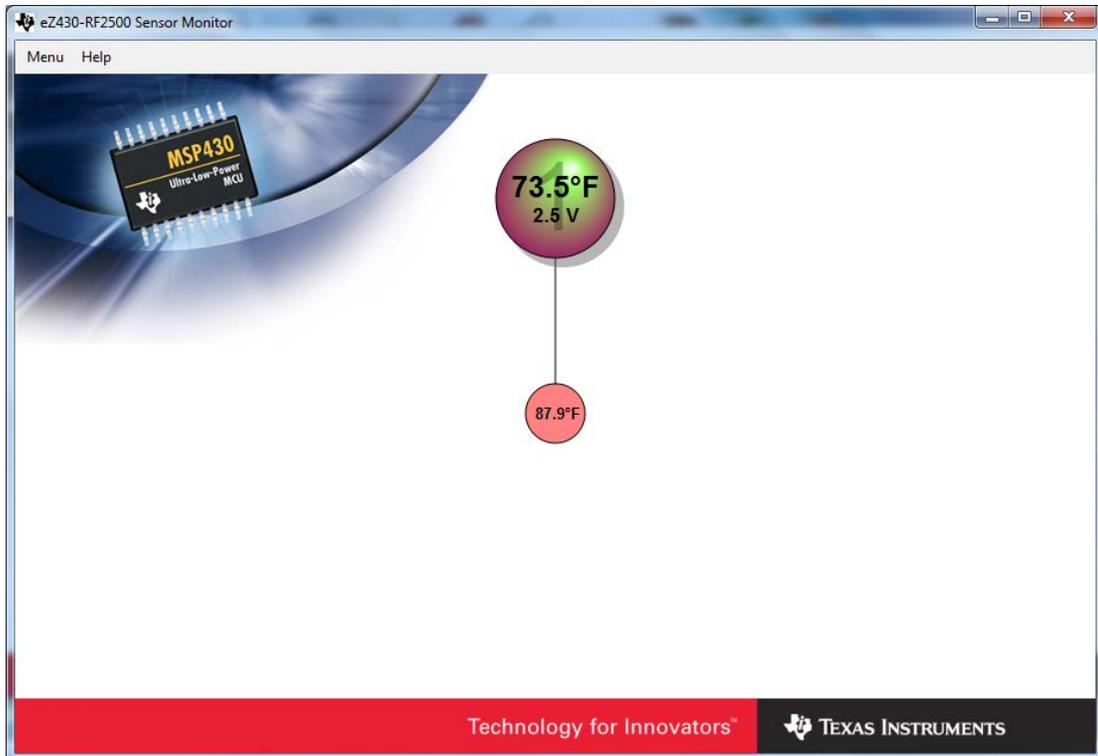


Fig. 6.16 The sampled environmental temperature and supply voltage to the sensor node displaying on a computer screen

Fig 6.17 displays the data streaming in this experiment, where \$HUB0 denotes the access point, and \$N (N=1, 2, 3...) denotes the identifier of the end device. Since we are only using one sensor node, the identifier is \$0001. The data streaming also says the temperatures of the end device and the access point are 73.5°F and 87.9°F, respectively. Besides, the supply voltage to the end device is 2.5 V, while the supply voltage to the access point is 3.6 V.

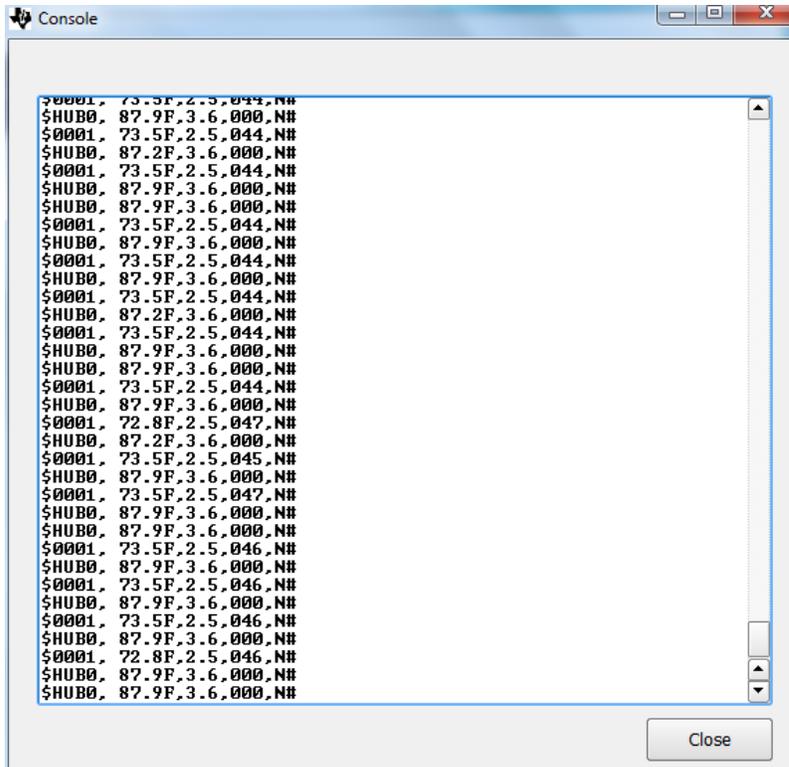


Fig. 6.17 Data streaming of the measured results

In the experiments, we are only using a single wireless sensor node. If multiple wireless sensor nodes have been used, they form a wireless sensor network capable of sensing the environmental temperature over a large area. All the sampled data would be transferred to the access point, and then be displaced on the computer screen.

The measured results of the battery output voltage, the supply voltage to the sensor node and the visual display of sampled temperature data together demonstrate that the system is capable of powering the off-shelf commercial wireless sensor node. Besides, we have demonstrated that the rectenna is capable of harvesting RF energies from various signal sources. In conclusion, the energy harvesting system has been proved to successfully harvesting the RF energy to power the sensor node. Our

voltage regulator system is not used here because the eZ430-RF2500 already has on-chip linear regulators invisible to the end user [92]. If we had been able to incorporate our proposed voltage regulator into the energy harvesting system, the whole system would have been working more efficiently.

Chapter 7: Conclusions and Future Work

WSNs are broadly used to monitor environmental conditions such as structural health, traffic, smoke and temperature. However, the cost of replacing all the batteries powering the sensor nodes can be extremely high (e.g., OnWorld estimates the total cost to replace the batteries could be more than \$1 Billion [93]). Harvesting ambient energies from the environment allows the system to run without batteries. But the low power density requires us to minimize the power consumption of the system. Linear regulators are important modules of the energy harvesting system which are power hungry; therefore, the power consumption of the linear regulators should be minimized without degrading the performance.

By studying the duty cycling behavior of the sensor nodes, we realized that the sensor node state information can be utilized to control the function of the linear regulators and reduce their power consumptions. This dissertation proposed a regulator system topology with ultra-low power consumption. The proposed system mitigates the tradeoff between low quiescent current and fast transient response. The system has been designed and implemented using a $0.5\ \mu\text{m}$ process. The experiment results show that: (1) compared to the state-of-the-art in the literature, the designed system reduces the quiescent current by 3X while at the same time achieving comparable dropout voltage and transient response; (2) compared to the commercial off-shelf products, the designed system reduces the quiescent current by 2X while at the same time improving the transient response settling time by about 300X.

This dissertation also studies an RF energy harvesting system. The system has been designed and tested, showing that the system is capable of capturing various RF signals in the environment and powering commercial off-shelf wireless sensor node.

We think there are two more things to do in the future to improve the RF energy harvesting powering the wireless sensor node: improve the voltage regulator system, and improve the whole energy harvesting system.

For the voltage regulator system, one future endeavors can be devoted reduce the quiescent current of regulator II as it determines the average quiescent current of the voltage regulator system. This can be achieved by designing a current reference circuit with lower current consumptions (we recently succeeded in reducing this current by 4X in simulation, but it needs to be verified through experiments with fabricated chips). The two PMOS switches used in our regulator system are connected in series with regulator I and all the load currents need to flow across those two switches. These two switches have large sizes as to reduce voltage drops across them. The improvement is to use just one NMOS transistor to control the tail currents of the amplifier and buffer (both of the two large PMOS switches can be eliminated). One example of the improved circuit is shown as in Fig. 7.1.

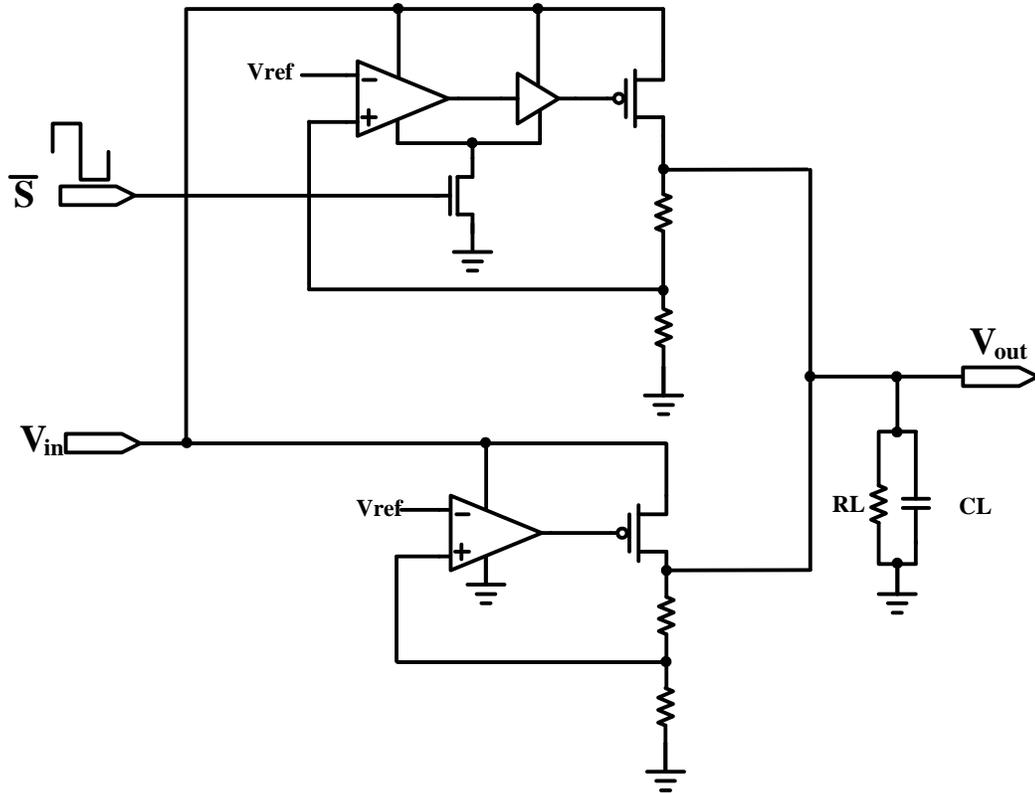


Fig. 7.1 An improved circuit

For the whole energy harvesting system, one limitation in our experiments is that the sea water battery we used is not secondary battery and therefore is not suitable in the energy harvesting system. The output voltage of FlexEl secondary batteries used by our former lab colleagues is not as high as the sea water battery. Therefore, in the future, we need to investigate how to make high output voltage secondary sea water batteries. Besides, finding out how to incorporate the proposed voltage regulator into the whole energy harvesting system would be beneficial.

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