ABSTRACT

Title of Dissertation:	An Integrated Single-phase On-board Charger
	Jiangheng Lu, Doctor of Philosophy, 2019
Dissertation directed by:	Associate Professor, Alireza Khaligh, Electrical and Computer Engineering Department

With the growing demand for transportation electrification, plug-in electric vehicles (PEVs), and plug-in hybrid electric vehicles (PHEVs), cumulatively called electric vehicles (EVs) are drawing more and more attention. The on-board charger (OBC), which is the power electronics interface between the power grid and the high voltage traction battery, is an important part for charging EVs. Besides the OBC, every EV is equipped with another separate power unit called the auxiliary power module (APM) to charge the low voltage (LV) auxiliary battery, which supplies all the electronics on car including audio, air conditioner, lights and controllers. The main target of this work is a novel way to integrate both units together to achieve a charger design that is not only capable of bi-directional operation with high efficiency, but also higher gravimetric and volumetric power density, as compared with those of the existing OBCs and APMs combined.

To achieve this target, following contributions are made: (i) a three-port integrated DC/DC converter, which combines OBC and APM together through an innovative integration method; (ii) an innovative zero-crossing current spike compensation for interleaved totem pole power factor correction (PFC) and (iii) a new phase-shift based control strategy to achieve a regulated power flow management with minimum circulating losses.

AN INTEGRATED SINGLE-PHASE ON-BOARD CHARGER

by

Jiangheng Lu

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List of Abbreviations

ω	----------	Angular frequency
ω_o	----------	Primary side resonant angular frequency
ω_o'	----------	Secondary side resonant angular frequency
m	----------	Resonant inductance ratio
Q	----------	Quality factor
$f_{r1,G2V}$	----------	First resonant frequency in G2V operation
$f_{r2,G2V}$	----------	Second resonant frequency in G2V operation
$f_{r1,V2G}$	----------	First resonant frequency in V2G operation
$f_{r2,V2G}$	----------	Second resonant frequency in V2G operation
p	----------	Resonant capacitance ratio
$R'_{e,HV}$	----------	Effective AC resistance for HV battery
$R'_{e,in}$	----------	Effective AC resistance for DC link
e_1	----------	Input of PI controller 1
e_2	----------	Input of PI controller 2
$V_{hv_{ref}}$	----------	HV voltage reference
V_{HV}	----------	HV Battery voltage
$V_{DC_{ref}}$	----------	DC link voltage reference
V_{DC}	----------	DC link voltage
V_{DC0}	----------	Feedforward term
k_{p1}	----------	P value for PI controller 1
k_{i1}	----------	I value for PI controller 1
k_{p2}	----------	P value for PI controller 2

k_{i2}	----------	I value for PI controller 2
$< V_{in} >_{rms}$	----------	RMS input voltage
G	----------	CLLLC stage gain
V_{LV}	----------	LV battery voltage
P_{12}	----------	Active Power flow from DC link to HV battery
P_{23}	----------	Active Power flow from HV battery to LV battery
P_{13}	----------	Active Power flow from DC link to LV battery
P_1	----------	Active Power at DC link
P_2	----------	Active Power at HV battery
P_3	----------	Active Power at LV battery
Q_{12}	----------	Reactive Power flow from DC link to HV battery
Q_{23}	----------	Reactive Power flow from HV battery to LV battery
Q_{13}	----------	Reactive Power flow from DC link to LV battery
Q_1	----------	Reactive Power at DC link
Q_2	----------	Reactive Power at HV battery
Q_3	----------	Reactive Power at LV battery
V_1	----------	Primary side bridge voltage
V_2	----------	Secondary side bridge voltage referred to the primary side
V_3	----------	Tertiary side bridge voltage referred to the primary side
I_1	----------	Transformer primary winding RMS current
I_3	----------	Transformer tertiary winding RMS current
I_{pri}	----------	Transformer primary winding current
I_{sec}	----------	Transformer secondary winding current
I_{ter}	----------	Transformer tertiary winding current
L_1	----------	Leakage inductance of primary transformer winding

L_2	----------	Leakage inductance of secondary transformer winding
L_3	----------	Leakage inductance of tertiary transformer winding
L_{12}	----------	Equivalent line inductance for power flow P_{12}
L_{23}	----------	Equivalent line inductance for power flow P_{23}
L_{13}	----------	Equivalent line inductance for power flow P_{13}
φ_2	----------	Phase angle between V_1 and V_2
φ_3	----------	Phase angle between V_1 and V_3
δ_1	----------	Half zero duration of V_1
δ_2	----------	Half zero duration of V_2
δ_3	----------	Half zero duration of V_3
f_s	----------	Switching frequency
ω_s	----------	Switching angular frequency
SOCL	----------	State of charge for LV battery
SOCH	----------	State of charge for HV battery
SOCT1	----------	Arbitrary state of charge threshold 1
SOCT2	----------	Arbitrary state of charge threshold 2
SOCT3	----------	Arbitrary state of charge threshold 3
i_L	----------	Inductor current
t_{d0}	----------	Time delay between leg 2 and leg 1
t_{d1}	----------	Time delay between leg 2 and leg 1
t_{d2}	----------	Time delay between leg 3 and leg 1
t_{d3}	----------	Time delay between leg 4 and leg 1
t_{d4}	----------	Time delay between leg 5 and leg 1
t_{d5}	----------	Time delay between leg 6 and leg 1
P_L	----------	Power loss

R_{th}	----------	Thermal resistance
$R_{th.jc}$	----------	Thermal resistance from junction to case
$R_{th.tim}$	----------	Thermal resistance of thermal interface material
$R_{th.hsa}$	----------	Thermal resistance from heatsink to ambient
T_r	----------	Temperature rise
t_r	----------	Rise time
t_f	----------	Fall time
P_{cod}	----------	Conduction loss of device
P_{sw}	----------	Switching loss of device
I_d	----------	Device RMS current
V_{ds}	----------	Device drain-to-source voltage
Δi_L	----------	Inductor current ripple
D	----------	Duty ratio
f_{line}	----------	Line frequency
H	----------	Magnetic field
H_{max}	----------	Maximum magnetic field
H_{min}	----------	Minimum magnetic field
B	----------	Flux density
B_{max}	----------	Maximum flux density
B_{min}	----------	Minimum flux density
ΔB	----------	Flux density ripple
P_{Core}	----------	Core loss
l_e	----------	Effective length of core
A_e	----------	Effective area of core
C_{oss}	----------	Output capacitance of MOSFET

V_g	----------	Gate voltage
Q_g	----------	Gate charge
P_{Cap}	----------	Capacitor ESR loss
ESR	----------	Effective series resistance
$\emptyset_1$	----------	Flux density of core left leg
$\emptyset_2$	----------	Flux density of core middle leg
$\emptyset_3$	----------	Flux density of core right leg
I_p	----------	Transformer primary winding current
I_s	----------	Transformer secondary winding current
I_t	----------	Transformer tertiary winding current
R_{g1}	----------	Magnetic reluctance of core left core
R_{g2}	----------	Magnetic reluctance of core middle core
R_{g3}	----------	Magnetic reluctance of core right core
N_{p1}	----------	Number of primary winding turns on core left leg
N_{p2}	----------	Number of primary winding turns on core right leg
N_{s1}	----------	Number of secondary winding turns on core left leg
N_{s2}	----------	Number of secondary winding turns on core right leg
$\mathrm{N_t}$	----------	Number of tertiary winding turns
L_m	----------	Magnetizing inductance
L_{lk}	----------	Leakage inductance
A_1	----------	Cross section area of core left leg
A_2	----------	Cross section area of core middle leg
A_3	----------	Cross section area of core right leg
l_{g1}	----------	Gap length of core left leg

l_{g2}	----------	Gap length of core middle leg
l_{g3}	----------	Gap length of core right leg
G_1	----------	Distance between top board and middle board
G_2	----------	Distance between middle board and bottom board

*** Variables with symbol ‘′’ means it is referred to the primary side of a transformer**

Chapter 1. Introduction

1.1. Background and objectives

According to the report from the International Energy Agency, electrical vehicles' (EVs) share of car stock has kept growing in the last consecutive eight years (2010-2018) and an unprecedented 1.1 million global sales were witnessed during the year 2017. Moreover, the projected share of the car stock globally is expected to be at least 14% by 2030 [1].

EV technology is attractive from the sustainability standpoint; however, limited range and higher refueling times are two of the main barriers for mainstream adoption. To improve these two aspects and to increase the driving experience of EVs, one effective approach is to design low-weight and highly compact components and possibly to integrate various traction electrical components onboard the vehicle. On-board chargers and auxiliary power modules are two such components. The smaller volume and lighter weight of the electrical powertrain components allows more battery installation to increase the driving range.

The charger and battery pack are key parts of the energy storage system for EVs. Compared to conventional gasoline-powered cars, which get traction from the internal combustion engine, EVs get propelling power from an electric motor driven by an on-board high-voltage (HV) battery pack. This HV battery has a typical terminal voltage of 400V, and a relatively high power charger is needed to charge this battery at relatively fast speed. In the bigger picture, the HV battery chargers can be categorized as on-board chargers (OBCs) and off-board chargers, depending on where the chargers are installed. Off –board chargers are mainly three-phase chargers. The OBCs are mostly used for convenient charging at home and work, and, in North America, they are commonly single-phase chargers.

A schematic diagram of the onboard power electronic interfaces (PEI) on an EV powertrain is presented in Fig. 1.1 [2]-[3]. As shown in Fig. 1.1, apart from the aforementioned HV battery pack, there is another 12V battery called the auxiliary battery,

which supplies the electrical loads like the air conditioner, wipers, lights, radio, etc. Due to the low capacity of this low voltage (LV) battery, a high step-down DC/DC converter is installed between the two batteries to provide galvanic isolation and prevent the LV battery from depleting due to the heavy electronic loads. This DC/DC converter serves as the auxiliary battery charger, therefore it is called the auxiliary power module (APM). APM and OBC together form the on-board charging system in EVs.

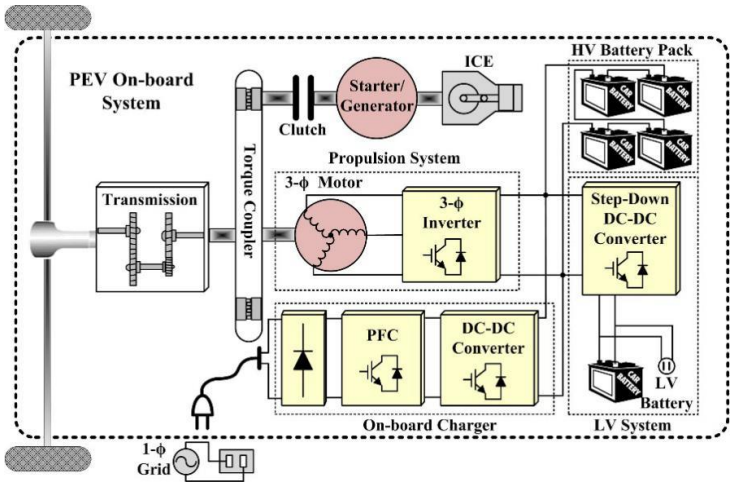


Fig. 1.1. Typical schematic diagram of the onboard PEIs in an EV powertrain.

As mentioned, OBC is the EVs' on-board charging component. The typical structure of a single-phase OBC is a front-end power factor correction (PFC) followed by an isolated DC-DC, as shown in Fig. 1.2.

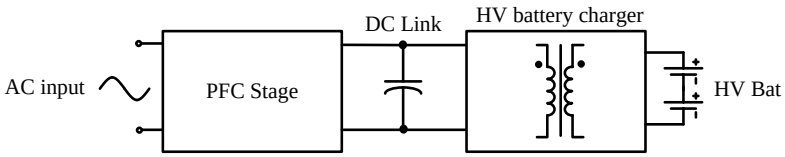


Fig. 1.2. Typical structure for a single-phase EV's OBC

The front-end PFC circuit is used to achieve a unity power factor (PF) on the grid side while regulating the output DC voltage to a desired value. There has been a comprehensive amount of research to improve the performance of this stage by different topologies and control techniques. Topology-wise, the most widely accepted PFC family in single-phase OBCs is boost-derived PFC circuits due to their continuous input current and better EMI performance, as compared to buck-derived PFC topologies whose EMI filters are typically less efficient and bulky due to the discontinuous input current. From the control perspective, critical conduction mode (CRM) is often used in the high frequency range (~MHz) [4]-[6] due to the soft-switching capability. Continuous conduction mode (CCM) operation is widely used in medium frequency range (~100kHz) [7]-[8] because of the low current stress for switching devices. Discontinuous conduction mode (DCM) is more prominent in low power applications [9]- [11] because the control loop design is easier and cheaper and the high current stress is not as punishing as it is in the medium-to-high power applications. Therefore, a single-phase boost-derived CCM PFC circuit is adopted in this work. A detailed review of the boost family PFC topologies will be discussed in Chapter 3.

As for the isolated DC-DC stage, the two most popular types of converters are: 1) the Pulse Width Modulation (PWM) based converter, including phase-shifted full bridge converters (PSFB) and dual-active full bridge converters (DAB); 2) the Pulse frequency modulation (PFM) based converter including different types of resonant converters like LLC, CLLC, LCC, etc. While these two families have unique features, they share several common characteristics. Firstly, they are both decent candidates for wide gain design, which makes them widely accepted in charger applications. Secondly, the zero voltage switching (ZVS) for MOSFETs is achieved by the same mechanism; creating the inductive energy (current with a phase lag with respect to the bridge voltage) and using it to charge/discharge the junction capacitance of the MOSFET during dead-time. Finally, both of them have the potential to achieve bi-directional operation. This is an important factor for a topology to find a niche

among current trends of OBC research because bi-directional capability is seen as one of the most important future directions. For example, PWM based solutions for bi-directional operations were proposed by G. Xu et al. and Y. W. Cho et al. [12]-[13], and their topologies are summarized in Fig. 1.3. Meanwhile, B. K. Lee et al. and Li et al. [14]-[15] presented a good insight on how a bi-directional system can be built based on resonant converters; the system configurations proposed in these two papers are summarized in Fig. 1.4. Moreover, another good example of achieving bi-directional capability based on resonant converters was displayed in the work of J. Shin et al. [16] and the DC-link electrolytic capacitors were avoided due to their unique circuit structure and harmonic compensation.

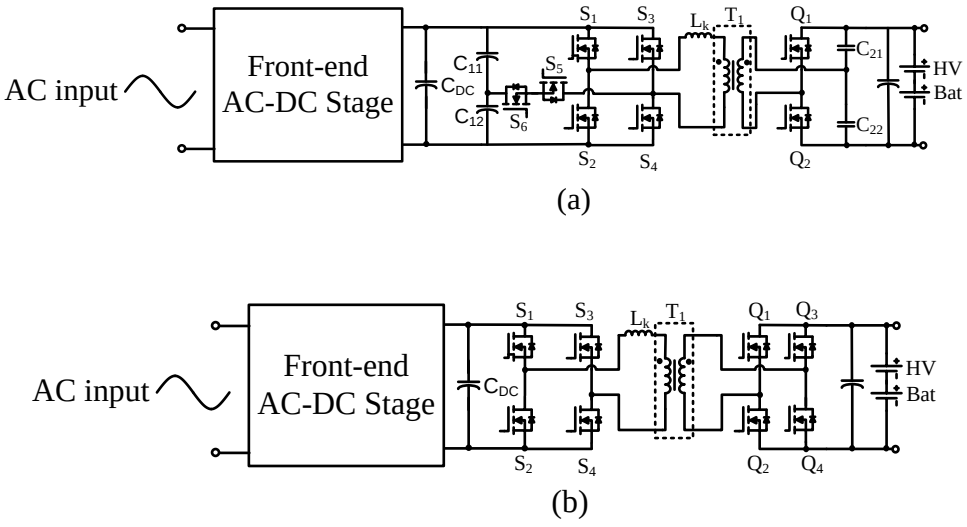
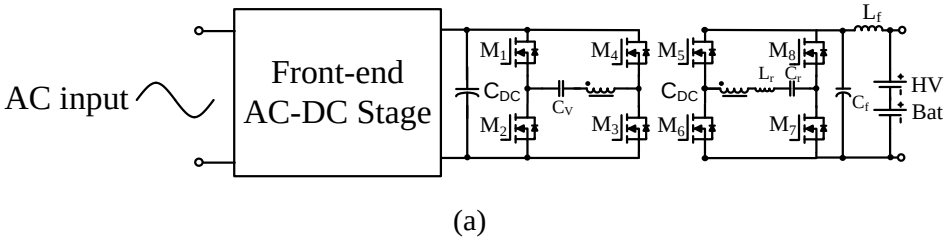
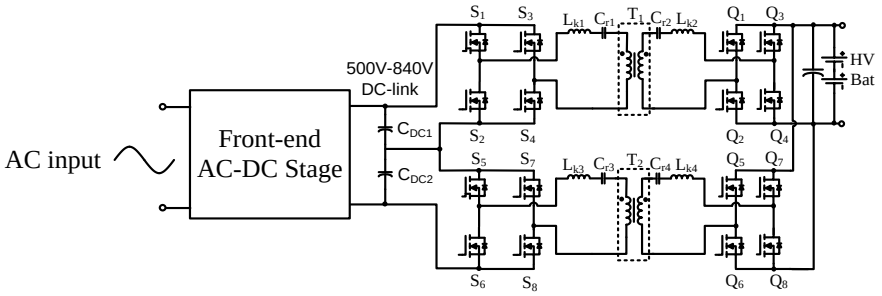


Fig. 1.3. PWM based bi-directional solutions: (a) Hybrid-Bridge-Based DAB Converter [12] (b) Bi-directional DAB inverter [13]



(a)



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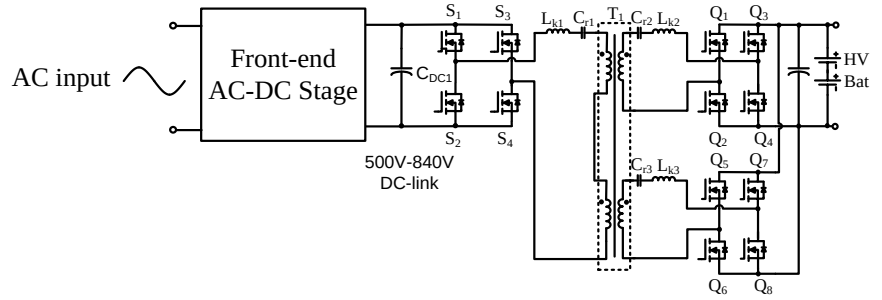
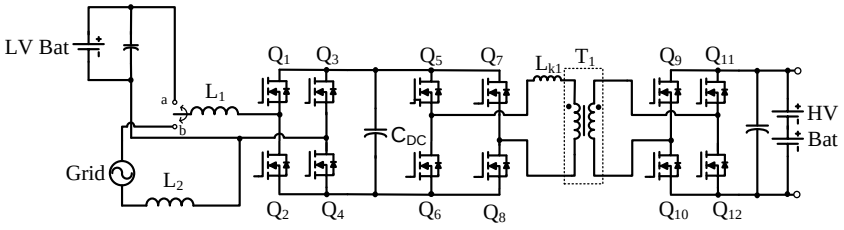


(c)

Fig. 1.4. Resonant converter (PFM) based bi-directional solutions: (a) Bidirectional PWM Resonant Converter [14] (b) Bi-directional CLLC resonant converter with split capacitors [15] (c) Bi-directional CLLC resonant converter with matrix transformer [15].

As mentioned, it is desirable to reduce the volume and weight of the charging system as much as possible because a charging system with higher gravimetric and volumetric power density allows more battery installation and increases the driving range of EVs. Therefore, researchers have been putting their efforts into achieving weight and volume reductions by integration of power electronics on EVs [17]-[25]. Firstly, there is research that focuses on the integration of OBC and a DC-DC bidirectional converter, which is installed between the HV battery pack and the propulsion inverter [17]-[21]. However, such topologies require more transistors and diodes, and integrating a high-power DC-DC converter with a low-power onboard charger might reduce the charging efficiency. In addition, some EVs might

not be equipped with a bidirectional converter between the HV battery pack and the propulsion inverter. Meanwhile, other researchers have tried to integrate bi-directional OBC and APM units [22]-[25]. A configuration consisting of three H-bridges and a selective switch was proposed to realize the integration in the work by S. Kim, et al. [22]. The main issue with this solution is that the efficiency of the LV charging operation is compromised due to three cascaded H-bridges. With two bi-directional switches (either relays or back-to-back MOSFET pairs), the configuration proposed by J. G. Pinto et al. [23] achieves the integration with fewer numbers of semi-conductor devices at the cost of losing isolation in the grid-to-vehicle (G2V) and vehicle-to-grid (V2G) operations. While the two aforementioned works integrated the APM into OBC at the grid side, the following two proposed solutions tried to achieve the integration at the DC-DC stage. The research work by R. Hou et al. [24] proposed a configuration that integrates the APM through the HV DC-link. However this topology does not take full advantage of the integration as the component number is not reduced. The work by X. Lu et al. [25] presents a solution that integrates an interleaved buck-boost converter as APM through the secondary side H-bridge of DC-DC converter. However the HV and LV batteries share the same ground, which may not be an implementable solution due to safety regulations. All the topologies mentioned above are summarized in Fig. 1.5.



(a)

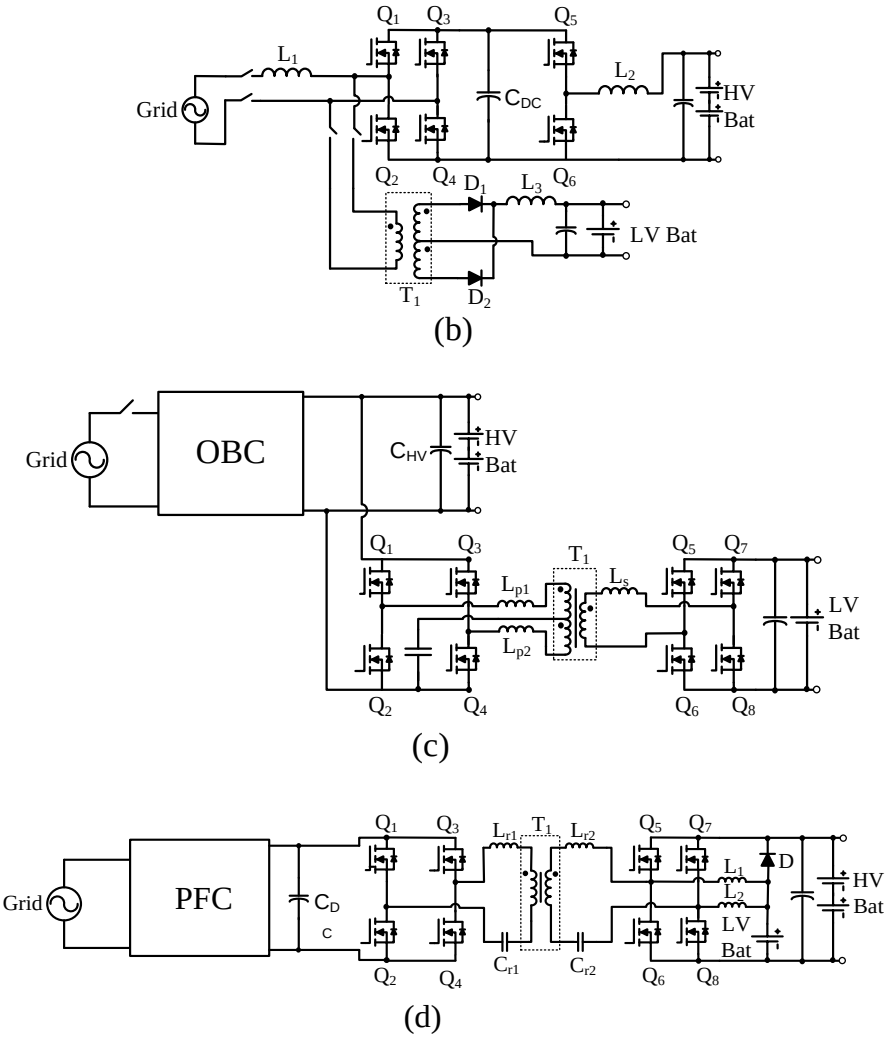


Fig. 1.5. Integrated solutions: (a) Integration of a center-tapped rectifier and LLC resonant converter at grid side [22] (b) Integration of center-tapped rectifier and half bridge rectifier at grid side [23] (c) Integration of full bridge active filter as APM and OBC at DC side [24] (d) Integration of OBC and bi-direction buck-boost converter at the DC side [25]

In addition to the integration, researchers have also been looking recently into the bi-directional OBC solutions that not only can charge the HV battery from the grid, but also can transfer the power from the battery back to the grid [12]-[18] and [25]-[27]. This feature

allows OBC to be a temporary power source to power up the electrical devices during blackouts and potentially become an important piece of the future micro grid to enhance power quality.

Inspired by those two trends, an innovative single phase bi-directional integrated charger that integrates OBC and APM into one circuit topology is proposed in this work.

1.2. Synopsis of the dissertation

In this work, the primary novelty is an innovative approach to achieve an integrated OBC architecture that achieves a highly compact, highly efficient design with the capability of bi-directional operation. More specifically, my contributions are: (i) a three-port integrated DC/DC converter, which combines OBC and APM together through an innovative integration method; (ii) an innovative zero-crossing current spike compensation for interleaved totem PFC; and (iii) a new phase-shift based control strategy to achieve a regulated power flow management with minimum circulating loss. Therefore, this dissertation is organized as follows.

A three-port DC-DC converter is proposed to integrate the OBC and the APM through intertwining a bi-directional CLLC and an LLC resonant converter using a three-winding integrated transformer. The topology and hardware development of the proposed DC/DC converter are presented in detail in Chapter 2.

In Chapter 3, a thorough review of boost-derived PFC circuits is presented first, to justify the selection of interleaved totem pole PFC. This topology suffers from a zero-crossing current spike which degrades the input current quality and threatens the safety of the switching devices. We have conducted detailed analyses for the generation of this current

spike. Then a novel control diagram, which compensates for the zero-crossing current spike is proposed and verified by experimental results.

With the selected interleaved totem pole PFC rectifier and the proposed DC/DC converter, a proof-of-concept of a single-phase bi-directional, dual output charger is designed and developed. It is shown that the gravimetric and volumetric power density of the charger can be improved by a considerable margin as compared to a conventional OBC plus an APM combined.

Moreover, a control method, called "variable DC-link control" is developed to enhance efficiency. This control strategy is most suitable for the two-stage charger structure comprising the front-end PFC rectifier followed by a resonant DC-DC converter (either LLC or CLLC). With this control, DC-link voltage is altered based on the desired HV battery voltage so that the resonant DC-DC converter can always be operated at the resonant frequency to achieve the optimum efficiency. This work proposes a novel approach to analyze and synthesize the voltage loop for the variable DC-link control. The details of voltage loop analyses and design are introduced in Chapter 4. Details about this work can also be found in my publications [28]-[29].

In Chapter 5, in order to achieve the functionality of simultaneously charging both HV and LV batteries, a triple active bridge (TAB) converter is selected and a new phase-shift based control scheme is developed and validated to manage the power flow comprehensively. Moreover, to further improve the power density of the design, novel loss modeling for both PFC and DC/DC stages is developed and validated for more accurate thermal analysis and a low-profile planar integrated transformer is designed. All the aforementioned innovations are verified through experimental results.

Lastly, Chapter 6 puts forward the conclusion and general discussion of potential future work.

For the convenience of the readers, the primary contributions are summarized as follows:

- Integrated OBC based on CLLLC resonant converter
  - New control: Zero-crossing current spike management for interleaved totem pole PFC
  - New model: real-time approach for power loss estimation for boost-derived PFC
  - New topology: CLLLC resonant converter and three-winding integrated transformer
- Integrated OBC based on TAB converter
  - New control: Phase shift based control scheme for the power flow management and the capability of simultaneously charging both HV and LV batteries (G2B mode)
  - Low profile integrated planar transformer for power density enhancement

Chapter 2. Three-Port Integrated Resonant DC-DC Converter

2.1. Introduction

The first and the most critical step of integrating OBC and APM together is to create an isolated three-port DC/DC conversion circuit topology which is capable of charging HV and LV batteries depending on the operational mode. Moreover, the created topology should have less component counts in order to improve the power density of the design compared with the conventional separate OBC and APM structure. Conversion efficiency of this circuit should be at least comparable, if not superior, to the conventional approach.

Prior efforts have studied the integration of non-isolated multi-port circuits. Multi-input and multi-output DC-DC converters were investigated for hybrid energy storage systems [30]-[32]; however, these converters are not able to provide isolation between HV DC-link, HV traction battery and LV DC loads, and do not comply with the IEC 61851-1 Standard [33]. In addition, many of these topologies require more components and have lower efficiency in comparison to stand-alone converters. Three-port isolated resonant and non-resonant DC-DC converters were investigated for potential isolated onboard charging in EVs [34]-[36]. However, they are not suitable for V2G application due to their unidirectional operation. Moreover, some of these topologies are not able to provide high voltage gain between the HV traction battery and LV DC loads. Bi-directional three-port phase-shift active-bridge converters were developed for potential G2V and V2G operation in EVs [37]-[40], but the circulating current significantly increases when the input and output voltages have large differences. Furthermore, the soft-switching range of such converters is narrow at light load [41]. Researchers have studied bidirectional CLLC resonant converters for onboard battery charging with wide voltage ranges; however, such studies have only focused on stand-alone chargers [42]-[43]. Moreover, all of these isolated topologies include a discrete

inductor as the resonant inductor in series with the transformer, which increases the size and weight of magnetic components.

To address the aforementioned concerns, a highly integrated dual-output isolated topology capable of G2V, V2G and high voltage to low voltage (H2L) charging is proposed and developed. This chapter focuses on design and development of the bidirectional isolated resonant DC-DC stage. In comparison to two stand-alone DC-DC converters and other integrated converters, the proposed integrated topology has a fewer number of components, higher power density, wide input/output voltage range, and high efficiency.

2.2. Proposed three-port integrated resonant DC-DC converter

2.2.1. Topological integration

Fig. 2.1 demonstrates the topology of the isolated stage of a typical onboard charger and an individual DC-DC converter. A unidirectional LLC resonant converter is used as the isolated stage of onboard charger to regulate the voltage/current of the HV traction battery. Another LLC resonant converter is used to deliver power from the HV traction battery pack to the LV battery.

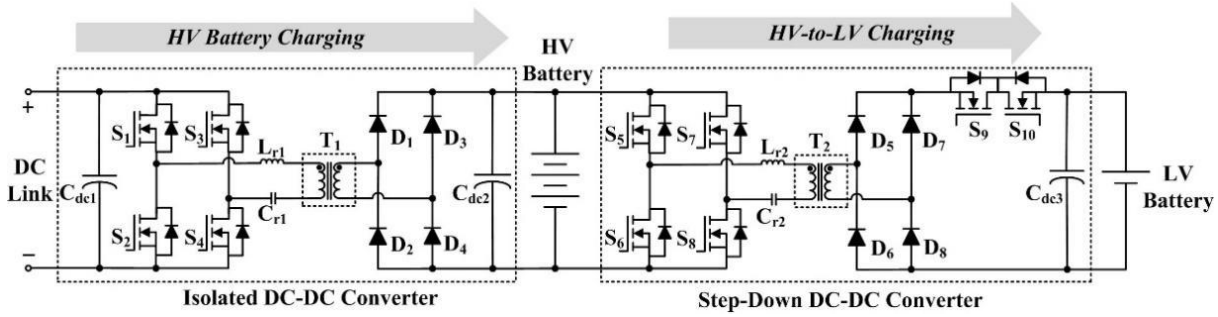


Fig. 2.1. The isolated stage of a typical stand-alone onboard charger and the step-down DC-DC converter on an EV.

The proposed integrated topology, illustrated in Fig. 2.2, not only uses less number of components but also enables multiple operation modes. A bidirectional dual-output CLLLC resonant converter is used for integration of a CLLC converter intertwined with an LLC

resonant converter through an electromagnetics integrated transformer (EMIT). First, in comparison to other isolated DC/DC converters, such as phase-shifted full bridge converter, the CLLC resonant converter can achieve ZVS of primary side MOSFETs at light load condition. Second, CLLC resonant converter enables the bidirectional operation due to its symmetrical structure, taking advantages of the leakage inductance and magnetizing inductance at both primary side and secondary side of integrated transformer without a need for additional individual resonant inductors. Third, the proposed integrated structure enables intertwining an LLC resonant converter with the CLLC converter by using the tertiary winding of the integrated transformer when the charger works in H2L mode. This integrated topology increases the utilization of the transformer, resonant capacitors and switching bridges. Moreover, in comparison to the conventional half-bridge LLC converter, the proposed converter splits the resonant capacitor into two with center point connecting to transformer in order to (i) reduce the current stress of the resonant capacitor; (ii) lower the differential mode conduction noise; and (iii) minimize the flux-doubling effect during the first few switching cycles in the start-up procedure [44].

Fig. 2.3 shows different switching modes and the current path for each mode. The arrows represent the direction of the current. The branch with current alternating its direction during the switching mode is labeled with arrows at both ends. As indicated by Fig. 2.3, the split resonant capacitors carry half of the resonant tank current, therefore the current stress of each capacitor is reduced to half. Meanwhile, the voltage across the capacitor is the sum of resonant capacitor voltage and half of the DC voltage level, i.e. $\frac{V_{in}}{2}$ and $\frac{V_o}{2}$ for primary and secondary side resonant capacitors, respectively.

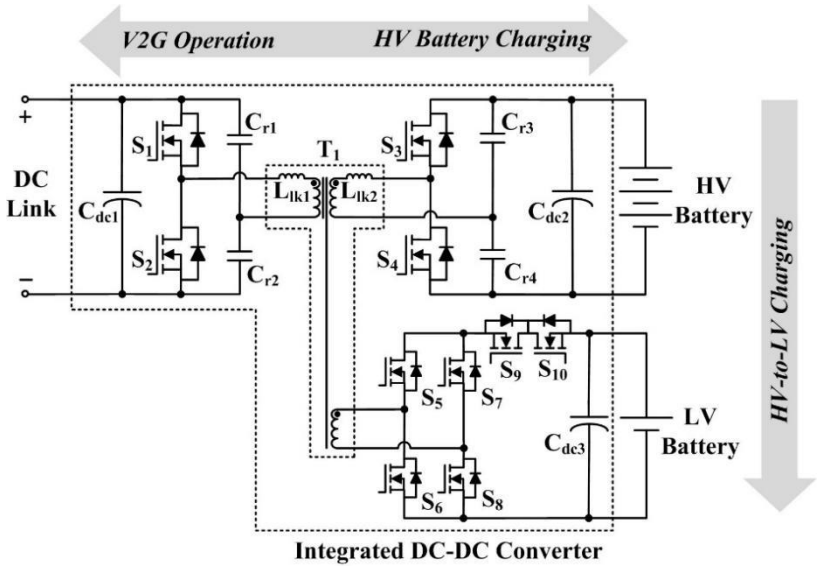
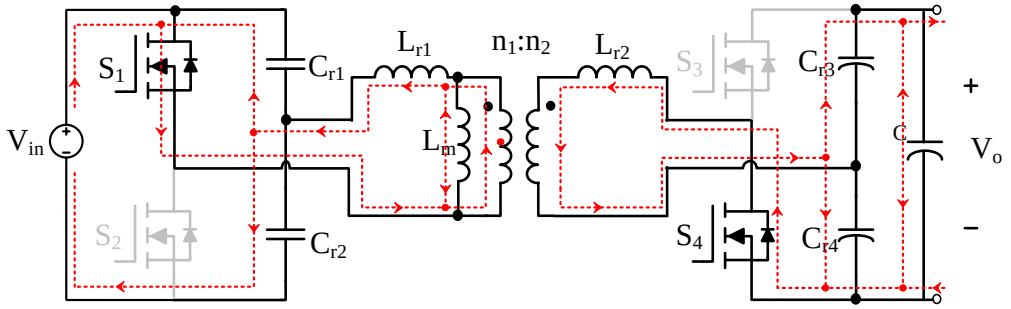
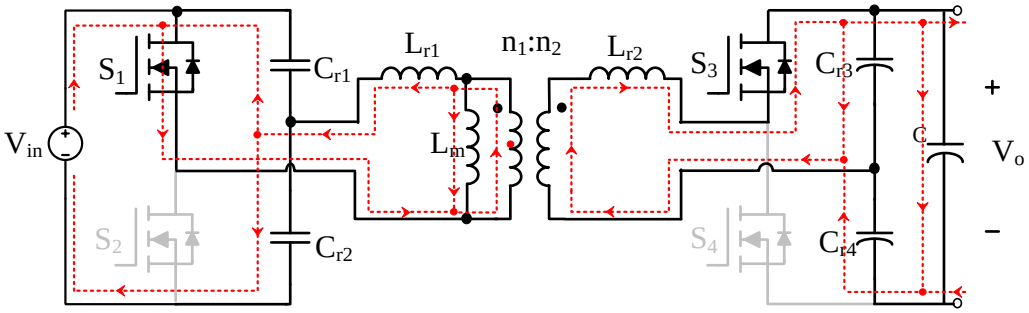


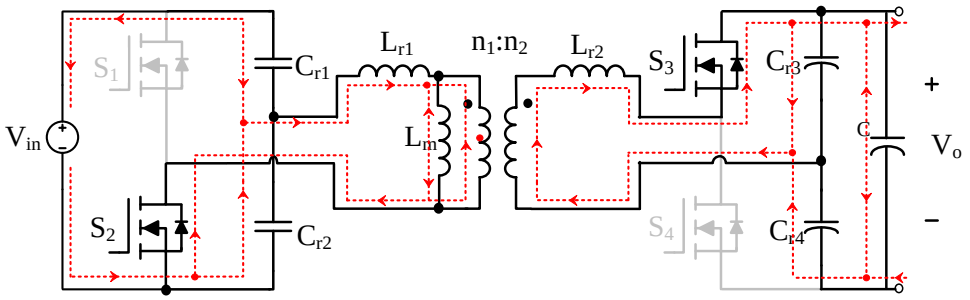
Fig. 2.2. The proposed isolated dual output converter topology.



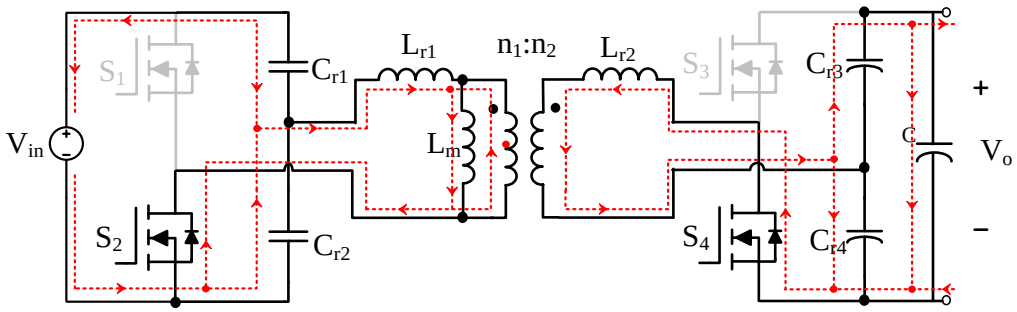
(a)



(b)



(c)



(d)

Fig. 2.3. Switching modes for CLLC resonant converter: (a) S_1, S_4 ON, S_2, S_3 OFF; (b) S_1, S_3 ON, S_2, S_4 OFF; (c) S_2, S_3 ON, S_1, S_4 OFF; (d) S_2, S_4 ON, S_1, S_3 OFF

The CLLLC converter utilizes the leakage inductances (L_{lk1} and L_{lk2}) of the three-winding EMIT (T_1) as the resonant inductors. In order to achieve V2G and H2L charging, the resonant capacitors are placed at both primary (C_{r1} and C_{r2}) and secondary (C_{r3} and C_{r4}) sides of the transformer. Therefore, C_{r1}, C_{r2} and L_{lk1} form a resonant network during G2V operation while C_{r3}, C_{r4} and L_{lk2} form a resonant network during V2G and H2L operations. Thus, the integrated topology utilizes the active bridge leg (S_3 and S_4) at secondary side during both V2G and H2L operations without a need for an additional DC-AC bridge.

At charger part, i.e. primary and secondary sides of the transformer, two half-bridge topologies are used to reduce the number of components. At low-voltage side, i.e. tertiary winding, a full-bridge rectifier is used to reduce the circulating current. In addition, SR (S_5 ~

S_8) is adopted to minimize the turn-on resistance and conduction losses. A back-to-back switch module (S_9 and S_{10}) is used with purpose of (a) disconnecting LV loads when necessary; and (b) reverse polarity protection.

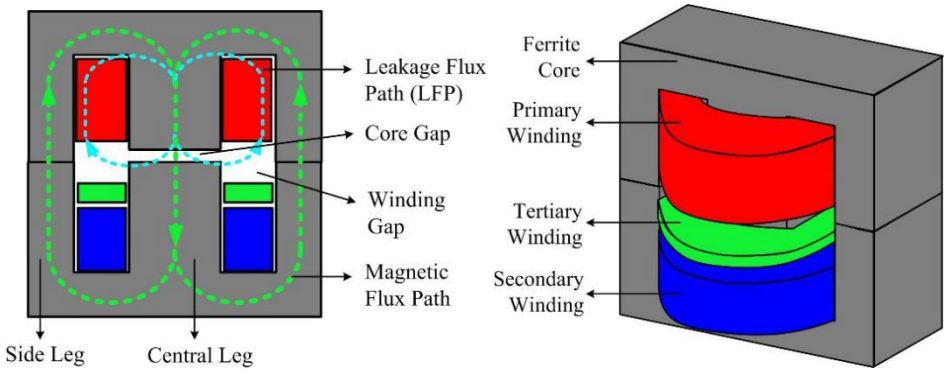
A higher power charging such as 6.6kW or even >10kW can be implemented by paralleling two or more such 3.3kW modules. The H2L operation can still be managed by using the tertiary winding of a transformer in either module, since the power rating of the 12V battery charger is relatively low.

The idea of intertwining H2H (G2V and V2G operation modes) and H2L circuits by using integrated three-winding transformer can be applied to the case of other resonant or non-resonant converter topologies such as three-port series resonant converters [45] or three-port active bridge converters [46].

2.2.2. Electromagnetic integration

In LLC converters with wide output voltage ranges, the required large resonant inductance of the LLC stage is typically realized using an additional external inductor [47]. However, using an EMIT with high leakage inductance can (*i*) remove the external inductor; (*ii*) reduce the converter size; (*iii*) reduce magnetic component losses and (*iv*) prevent saturation during start-up of the converter by flux-doubling effect. Modifications of magnetic-core shapes and winding structures have been studied to develop EMITs [48]-[50]. However, this work is the first effort towards integration of two large leakage inductances in a three-winding transformer. The integration is achieved by novel winding arrangements inside a three-winding transformer. The equivalent resonant and magnetizing inductances of two intertwined resonant converters can be acquired through a primary winding, a secondary winding, a tertiary winding, gaps between windings and transformer's cores as shown in Fig. 2.4.

There are different shapes that are commonly used in power electronics design. The compact shapes, like PQ and pot, have good EMI performance because the winding can be well shielded by the core. However, because of the compact size and relatively small window area, thermal performance of these cores is not as good. Moreover, the limited window area constrains the maximum number of turns that can be deployed inside the core. Because of this, the core may not be able to satisfy the turns ratio design while keep core loss low. On the other hand, UI core is a good candidate for high power application in tight spaces. Its long leg is beneficial for low leakage inductance design and high voltage insulation. However, for the same core volume, the effective cross section area of UI core is almost half of EE shape, which leads to significantly higher core loss. For high power application, the core loss can be invisible as it almost does not scale with power. However, this core loss will degrade the conversion efficiency with a considerable margin in medium-to-low power application, like this work. Compared to aforementioned core shapes, EE shape is selected for its balanced performance over all cylinders. Moreover, EE cores also have good flexibility to shape leakage flux path (LFP) [48]-[51].



(a) (b)

Fig. 2.4. The winding arrangements inside the gapped E cores to design EMIT. (a) 2-dimensional view including flux paths, (b) three-dimensional view with indication of EMIT's elements.

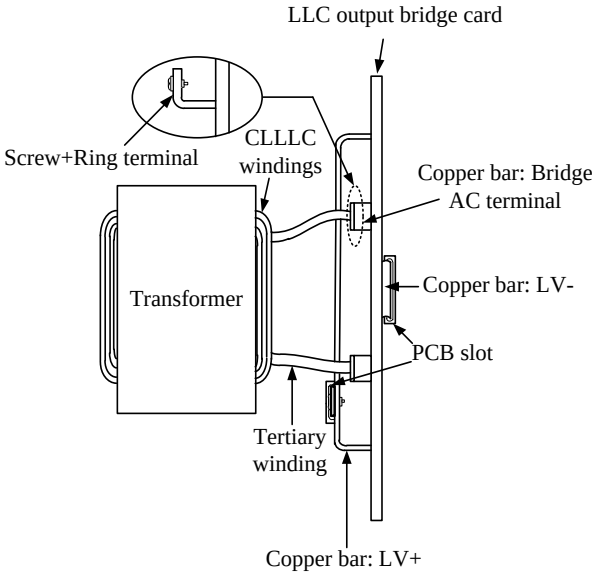


Fig. 2.5. The winding implementation and the bus bar solution

In this work, the primary winding is located on one side of the EE core while the secondary winding is placed on the other side. The tertiary winding is placed in the middle gap of two windings (see Fig. 2.4). The purpose to wind the tertiary winding in the middle of transformer is to generate a tertiary side by sharing the same ferrite core of primary side and secondary side while taking advantage of the window area. When the airgap between primary winding and secondary winding is set to ensure appropriate leakage inductance for the resonant tank, allocating the tertiary winding in the rest of space enables an easy-to-implement solution toward integrated transformer. The parameters of CLLC resonant converter are first achieved by setting the distance between the primary winding and the secondary winding. Then, the parameters of the intertwined LLC converter are dependent on the resonant tank at the secondary side and can be determined by properly selecting the turns ratio of the transformer. The regulation for H2L operation can be easily achieved by PFM without losing the soft-switching operation for the MOSFETs. As seen in Fig. 2.4(a), the LFP is perpendicular to the axis of the windings, passing through the gap between separated windings. This trajectory of LFP substantially contributes to the leakage inductance. In fact,

the air gap between the central legs of two E cores and the gaps among three windings can be adjusted to precisely set the leakage and magnetizing inductances. Therefore, large leakage and magnetizing inductances can be achieved, although the variation of gap between two E cores has less influence on the leakage inductance in comparison to the gaps among three windings. The air gap between E cores significantly reduces the risk of saturation. Furthermore, the gap among three windings helps to increase the voltage isolation.

Table 2.1 demonstrates the design parameters of the three-winding EMIT for the proposed integrated converter. The transformer core size is determined based on switching frequency, voltage and power level of the converter. The 3F3 from Ferroxcube Corporation with low loss (up to 700kHz) is selected as the ferrite E core. The Litz wire size is determined considering the current rating and skin effect. Since core loss constitutes to the majority of loss in the transformer, winding turns are increased to reduce core loss through increasing the magnetic flux density. Moreover, to optimize the efficiency of the converter, the turns ratio between primary and secondary windings is selected to ensure that the converter is operated at the resonant frequency at the nominal input and output voltage level. In addition, the conduction loss dominates the winding loss in LV side due to the high current, therefore the turns of tertiary winding is selected to be 1 to minimize the conduction resistance of the winding. Also, the window area is another factor to limit the turns number of LV side to be 1 as thick wire (AWG8) has to be used for the high current capacity. Therefore, with considerations of window area, core saturation, and current capacity, the turn ratio of the three windings is selected as 30:20:1. The illustration of implemented bus bar configuration for LV side is shown in Fig. 2.5.

Table 2.1. Design parameters of the three-winding EMIT.

Parameters	**Number**

Power rating (kW)	3.3
Nominal input voltage (V)	540
Nominal HV voltage (V)	360
Nominal LV voltage (V)	12
Primary winding turns	30
Secondary winding turns	20
Tertiary winding turns	1
Core shape	E65/32/27
Core material	3F3
Primary wire size (AWG)	14 (1050 × #44AWG)
Secondary wire size (AWG)	14 (1050 × #44AWG)
Tertiary wire size (AWG)	8 (3 × 4200 × #44AWG)
Gap between cores (mm)	0.6
Equivalent primary leakage inductance (μH)	80
Magnetizing inductance (μH)	370

2.3. Operational principles and gain analysis

The dual-output CLLLC resonant converter is the integration of a half-bridge CLLC resonant converter intertwined with a half-bridge LLC converter. The half-bridge CLLC resonant converter consists of the primary leakage inductance (L_{lk1}), secondary leakage inductance (L_{lk2}) and magnetizing inductance (L_m) of transformer (T_1), two bridge legs (S_1 ~ S_4), and four split resonant capacitors (C_{r1} ~ C_{r4}). On the other hand, the half-bridge LLC resonant converter consists of the secondary leakage inductance (L_{lk2}) and magnetizing inductance (L_m) of transformer (T_1), one bridge leg (S_3 and S_4), two split resonant capacitors (C_{r3} and C_{r4}), and a full-bridge synchronous rectifier (S_5 ~ S_8).

2.3.1. G2V Operation

Fig. 2.6 illustrates the circuit topology of the half-bridge CLLC resonant converter during charging HV traction battery. The SR at tertiary side is disabled and the series-connected back-to-back switches (S_9 and S_{10}) are turned off to disconnect the LV DC loads.

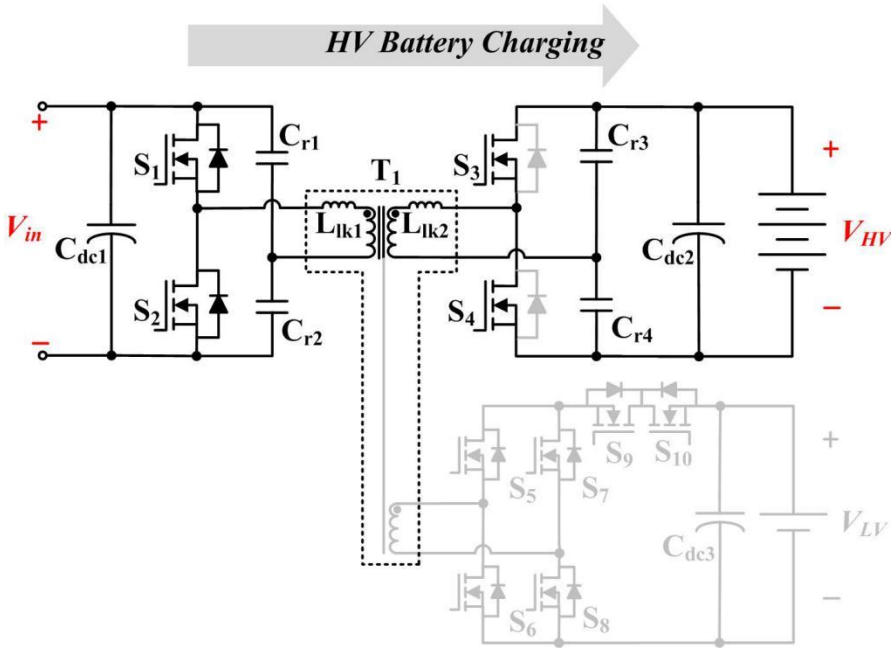
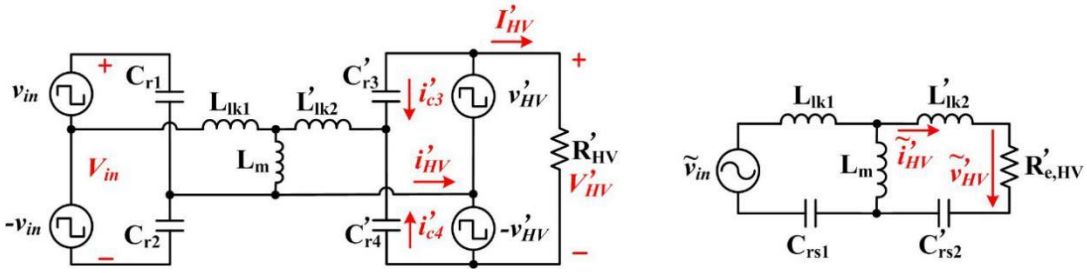


Fig. 2.6. Circuit topology of the half-bridge CLLC resonant converter during G2V charging.

First harmonic approximation (FHA), which is commonly used in the resonant converter analysis, can be utilized to analyze CLLC resonant converter. In resonant converters, the resonant tank performs as a low-pass filter. When the converter is operating at resonant frequency, only fundamental component of the input power can be delivered to the output port, i.e. the resonant current is sinusoidal. Therefore, this method gives the most accurate results when switching frequency is in the proximity of the resonant frequency of the tank. Basic concepts of FHA used in the following derivation were introduced in a well-established literature [52]-[54]. The nonlinear non-sinusoidal equivalent circuit model referred to the

primary side is presented in Fig. 2.7 (a) and the FHA equivalent impedance network is shown in Fig. 2.7(b). In the figure, $R'_{e,HV} = \frac{2n^2}{\pi^2} R_{HV}$ is the equivalent AC load and R_{HV} is the equivalent load resistance for the high voltage battery.



(a) (b)

Fig. 2.7. (a) Nonlinear non-sinusoidal circuit model; and (b) linear sinusoidal circuit model for G2V operation.

As a result of FHA assumption, the transfer function of the resonant converter can be derived from the impedance network as shown in Fig. 2.7(b).

$$M_{G2V}(j\omega) = \left| \frac{j\left(\frac{\omega}{\omega_o}\right)\left(\frac{\omega}{\omega'_o}\right)^2 (m-1)}{\left\{\left[\left(\frac{\omega}{\omega_o}\right)^2 + \left(\frac{\omega}{\omega'_o}\right)^2\right] m - \left(\frac{\omega}{\omega_o}\right)^2 \left(\frac{\omega}{\omega'_o}\right)^2 (2m-1) - 1\right\} Q + j\left(\frac{\omega}{\omega_o}\right)\left(\frac{\omega}{\omega'_o}\right)^2 m - \left(\frac{\omega}{\omega'_o}\right)\left(\frac{\omega_o}{\omega'_o}\right)} \right| \qquad (2.1)$$

where, the primary total inductance is $L_p = L_m + L_{lk1}$, the ratio of primary total inductance to primary leakage inductance is $m = \frac{L_p}{L_{lk1}}$, the quality factor is $Q = \frac{\sqrt{\frac{L_{lk1}}{C_{rs1}}}}{R'_{e,HV}}$, the angular resonant frequency of resonant network at primary side is $\omega_o = \frac{1}{\sqrt{L_{lk1} C_{rs1}}}$, and the angular resonant frequency of resonant network at secondary side is $\omega'_o = \frac{1}{\sqrt{L'_{lk2} C'_{rs2}}}$.

There are two resonant frequencies, $f_0 = \omega_0 / 2\pi$, the resonant frequency of resonant network at primary side, and $f'_0 = \omega'_0 / 2\pi$, the resonant frequency of resonant network at secondary side, respectively. In addition to the two aforementioned resonant frequencies, two series

resonant frequencies, $f_{r1,G2V}$ and $f_{r2,G2V}$, can be determined, in which the voltage gain in Eq. (2.1) becomes independent of load condition,

$$f_{r1,G2V} = \frac{1}{2\pi\sqrt{L_{lk1}C_{rs1}}}\sqrt{\frac{(p^2+1)m+\sqrt{(p^2+1)^2m^2-4p^2(2m-1)}}{2p^2(2m-1)}} \tag{2.2}$$

$$f_{r2,G2V} = \frac{1}{2\pi\sqrt{L_{lk1}C_{rs1}}}\sqrt{\frac{(p^2+1)m-\sqrt{(p^2+1)^2m^2-4p^2(2m-1)}}{2p^2(2m-1)}} \tag{2.3}$$

$$p = \frac{f_o}{f_o'} = \sqrt{\frac{C_{rs2}'}{C_{rs1}}} \tag{2.4}$$

where, p is the resonant frequency ratio, which is the ratio of the resonant frequency of primary network to the resonant frequency of secondary network.

To ensure the converter operating in the inductive region for ZVS, the switching frequency needs to be close to $f_{r1,G2V}$.

2.3.2. V2G operation

During V2G operation, the full-bridge rectifier at tertiary side is still disabled by turning off S_9 and S_{10}. The half-bridge CLLC resonant converter operates in a reversed direction, as shown in Fig. 2.8. V_{HV} at secondary side is considered as the input while V_{in} at primary side is the output. S_3 and S_4 operate as a bridge leg while S_1 and S_2 serve for SR. The half-bridge topology uses the same CLLC resonant network; however, the network impedance, voltage gain and resonant frequency are different from those during G2V operation. The nonlinear non-sinusoidal equivalent circuit model referred to the secondary side is presented in Fig. 2.9 (a) and the FHA equivalent impedance network is shown in Fig. 2.9(b). In the figure, $R_{e,in}' = \frac{2}{n^2\pi^2}R_{in}$ is the equivalent AC load resistance referred to secondary side. R_{in} is the equivalent load resistance in V2G mode.

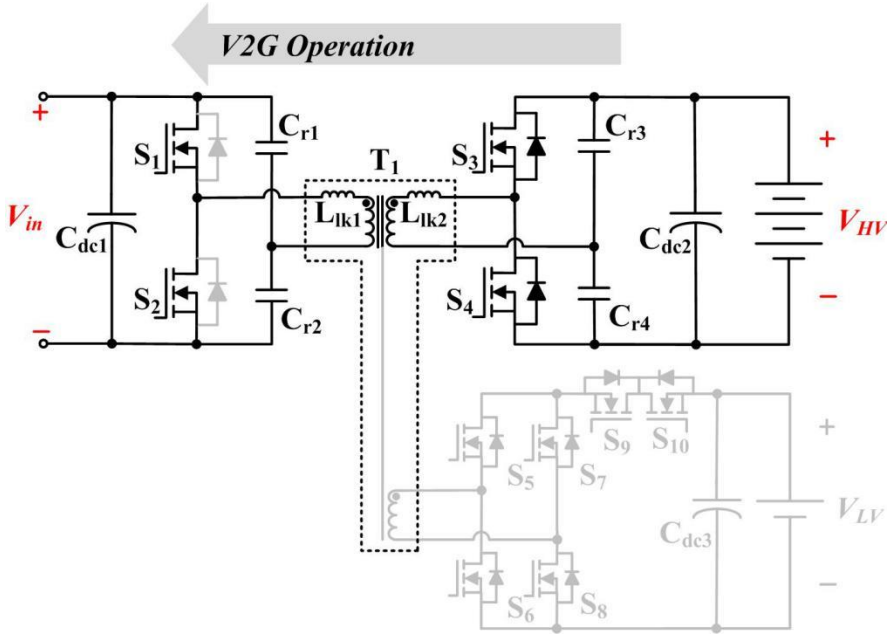
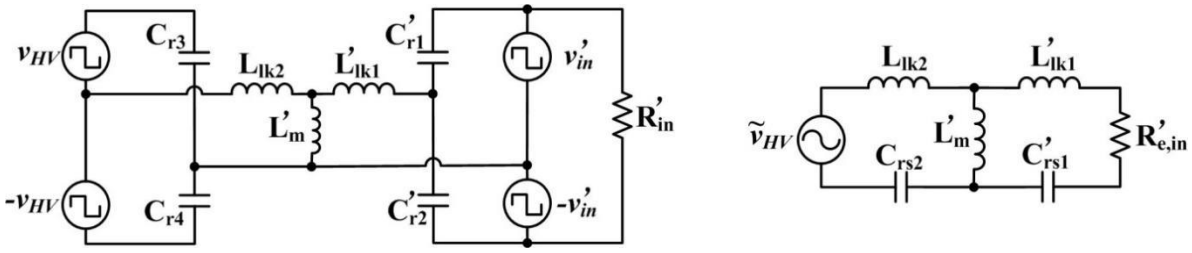


Fig. 2.8. Circuit topology of the half-bridge CLLC resonant converter for V2G operation.



(a) (b)

Fig. 2.9. (a) Nonlinear non-sinusoidal circuit model; and (b) linear sinusoidal circuit model for V2G operation.

From FHA analysis, the voltage gain, $M_{V2G}(j\omega)$, for V2G operation can be represented as

$$M_{V2G}(j\omega) = \left| \frac{j\left(\frac{\omega}{\omega_o}\right)\left(\frac{\omega}{\omega_o'}\right)^2 (m'-1)}{\left\{\left[\left(\frac{\omega}{\omega_o}\right)^2+\left(\frac{\omega}{\omega_o'}\right)^2\right]m'-\left(\frac{\omega}{\omega_o}\right)^2\left(\frac{\omega}{\omega_o'}\right)^2(2m'-1)-1\right\}Q'+j\left(\frac{\omega}{\omega_o}\right)\left(\frac{\omega}{\omega_o'}\right)^2 m'-\left(\frac{\omega}{\omega_o'}\right)\left(\frac{\omega_o}{\omega_o'}\right)} \right| \quad (2.5)$$

where, the secondary total inductance is $L_s = L_m{}' + L_{lk2}$, the ratio of secondary total inductance to secondary leakage inductance is $m' = \frac{L_s}{L_{lk2}}$, the quality factor is $Q' = \frac{\sqrt{\frac{L_{lk2}}{C_{rs2}}}}{R_{e,in}{}'}$, the angular resonant frequency of resonant network at secondary side is $\omega_o = \frac{1}{\sqrt{L_{lk2}C_{rs2}}}$, and the angular resonant frequency of resonant network at primary side is $\omega_o' = \frac{1}{\sqrt{L_{lk1}'C_{rs1}'}}$

Similar as in G2V mode, there are two resonant frequencies where the gain is independent of the load which are expressed as Eq. (2.6) and Eq. (2.7)

$$f_{r1,V2G} = \frac{1}{2\pi\sqrt{L_{lk2}C_{rs2}}}\sqrt{\frac{(p^2+1)m\prime+\sqrt{(p^2+1)^2m\prime^2-4p^2(2m\prime-1)}}{2(2m\prime-1)}} \quad (2.6)$$

$$f_{r2,V2G} = \frac{1}{2\pi\sqrt{L_{lk2}C_{rs2}}}\sqrt{\frac{(p^2+1)m'-\sqrt{(p^2+1)^2m\prime^2-4p^2(2m\prime-1)}}{2(2m\prime-1)}} \quad (2.7)$$

Similarly, to ensure the converter operating in the inductive region for ZVS, the switching frequency needs to be close to $f_{r1,V2G}$.

2.3.3. H2L Operation

During the driving cycle, H2L operation mode will be engaged to charge the LV battery. In this mode, the grid is disconnected. MOSFETs of the half-bridge converter at primary side (S_1 and S_2) are turned off. The body diodes of S_1 and S_2 will also be turned off as soon as the DC link voltage (V_{in}) reaches its maximum value (in this case, 600V). The series-connected back-to-back switches (S_9 and S_{10}) are turned on to enable the full-bridge rectifier at tertiary side. The full-bridge SR (S_5 ~ S_8) is used to reduce the conduction losses. Hence, a half-bridge LLC (L_{lk2}, L_m, C_{r3}, C_{r4}) resonant converter delivers the power from HV battery pack to LV loads, as depicted in Fig. 2.10.

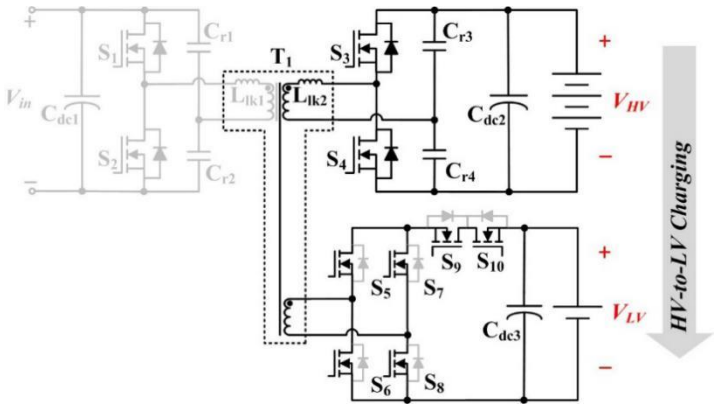
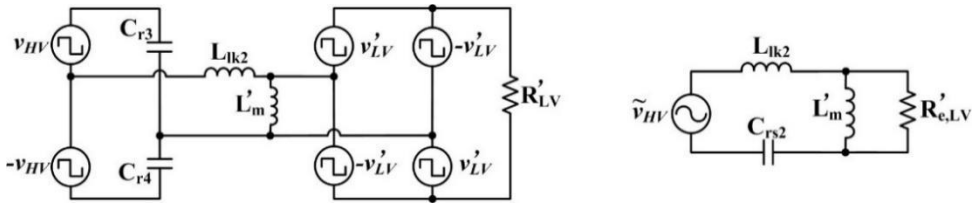


Fig. 2.10. Circuit topology of the half-bridge LLC resonant converter for H2L operation.



(a) (b)

Fig. 2.11. (a) Nonlinear non-sinusoidal circuit model; and (b) linear sinusoidal circuit model for H2L operation.

The nonlinear non-sinusoidal equivalent circuit model referred to the secondary side is presented in Fig. 2.11 (a) and the FHA equivalent impedance network is shown in Fig. 2.11(b). Since the topology operates as a half-bridge LLC converter during H2L operation, the transfer function, gain characteristics and the expression of resonant frequency can be referred to a well-established literature [47].

2.4. Experimental verification

A 3.3-kW prototype of the proposed dual-output DC-DC resonant converter, depicted in Fig. 2.12, is designed and developed to validate the operation of the topology. The HV battery voltage output can be variable from 250V to 420V, and the LV load output can be

variable from 8V to 14V. In the testbed, an SL Series power supply from Magna-Power is used as the DC source and Model 8526 from BK precision is used as the electronic load. Voltage probe P5200A and current probe TCP0030A from Tektronix are used to measure the voltage, current and efficiency.

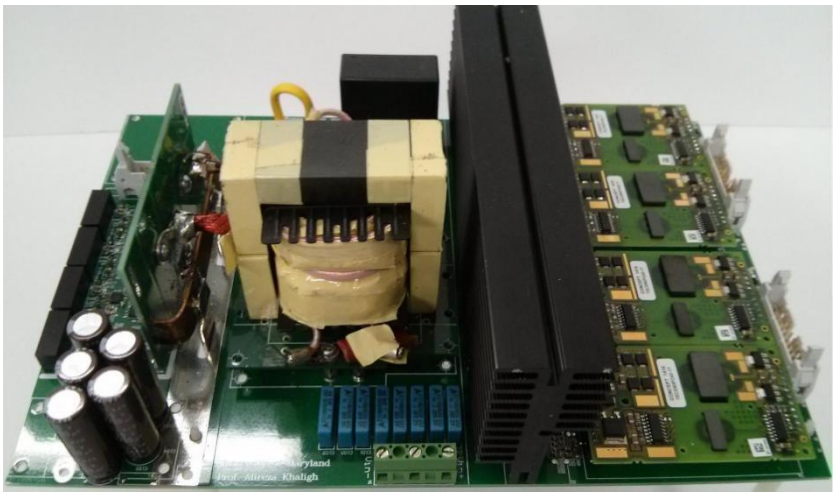


Fig. 2.12. The image of designed 3.3kW bidirectional isolated dual-output DC-DC resonant converter.

2.4.1. Hardware design considerations

The DC-link voltage, which is the input voltage of the DC-DC resonant stage, could be regulated from 400V to 600V, to ensure operation in the vicinity of the resonant frequency. Considering the trade-offs between component sizes and power losses, 190kHz series resonant frequencies ($f_{r1,G2V}$ and $f_{r1,V2G}$) are chosen. In experiments, the operating frequency is in the range from 180 kHz to 200kHz.

A customized designed EMIT is placed in the center of board. According to the nominal voltage of DC-link, HV battery and LV loads, the turns-ratio of the primary to secondary winding is set to 1.5:1. The turns-ratio of secondary to tertiary winding is set to 20:1. The magnitude of primary current that charges output capacitors of MOSFETs depends on the

magnetizing inductance (L_m), the dead-time duration (t_{dead}) and the switching frequency (f_s) [55]. To ensure ZVS operation, the magnetizing inductance can be determined as

$$L_m \leq \frac{t_{dead}}{16 C_{oss} f_s} \tag{2.8}$$

Hence, a magnetizing inductance of 370μH is selected based on a dead-time of 125nsec and a MOSFET output capacitor of 100nF. In order to reduce the circulating current, a relatively high ratio of total primary inductance to primary leakage inductance (m) is preferred. A 5.6 ratio (m=5.6) is acquired by adjusting the transformer air-gaps, yielding a primary leakage inductance of 80μH.

$$l_{lk1} = \frac{L_m}{m-1} \tag{2.9}$$

The air-gap between the central legs of EE cores is set to 0.6mm, and the air-gap between the primary winding and the secondary winding is set to 3mm. With this configuration of windings, 370μH magnetizing inductance, 80μH primary leakage inductance and 36μH secondary leakage inductance can be acquired.

At primary side, according to the resonant frequency and leakage inductance, the capacitance of both C_{r1} and C_{r2} can be determined as

$$C_{r1} = C_{r2} = \frac{1}{2 L_{lk1} (2\pi f_o)^2} \tag{2.10}$$

which equals to 4nF. Four parallel film capacitors, with the rating of 1nF/2kV, from TDK are used to reduce the equivalent series resistance. At secondary side, the capacitance of C_{r3} and C_{r4} equals to 10nF, consisting of three parallel film capacitors, with the rating of 3.3nF/1kV.

To ensure low conduction losses, 1200V CREE silicon carbide (SiC) MOSFETs with low turn-on resistances are selected at both primary and secondary sides. To increase the efficiency of SR at tertiary side, 60V/300A Infineon Si MOSFETs with very low turn-on resistances are connected in parallel and share one gating signal. The full-bridge SR at tertiary side is controlled by TI-UCC24610, a high-performance controller and driver for N-

channel MOSFETs. Large copper bars are used for external connection to further reduce the conduction losses. The circuit components are listed in Table 2.2.

Table 2.2 Component list of a 3.3-kW prototype of the proposed converter.

Components	Value	Part#
T_1	N/A	Customized
L_{lk1}	80μH	N/A
L_{lk2}	36μH	N/A
L_m	370μH	N/A
$N_1 : N_2 : N_3$	30:20:1	N/A
C_{r1}, C_{r2}	4nF	B32672L8102J
C_{r3}, C_{r4}	10nF	B32671L332J
$S_1 \sim S_4$	SiC FET 1200V/36A	Cree C2M0160120D
$S_5 \sim S_{10}$	Si FET 60V/300A	Infineon IPT007N06N

When the converter switching frequency is higher than $f_{r1,G2V}$, hard switching may occur at the load-side half-bridge and therefore the efficiency might decrease. When the converter switching frequency is lower than $f_{r1,G2V}$, circulating current of the transformer will increase and reduce the efficiency. Hence, high efficiency operation can be acquired with a switching frequency at the vicinity of $f_{r1,G2V}$.

2.4.2. Converter performance in G2V mode

As aforementioned, during G2V, the LV side (tertiary side) is disabled. To ensure the converter operation in inductive region and acquire high efficiency, the switching frequency is set slightly higher than $f_{r1,G2V}$. Experiments show that the secondary side rectification using body diodes of MOSFETs significantly reduces the efficiency due to the relatively high conduction voltage drop of SiC MOSFETs body diodes. Therefore, SR is used to turn on

MOSFETs at secondary side for efficient rectification. During HV battery charging, the switches S_1 and S_2 serve as a high-frequency inverter while S_3 and S_4 serve as a rectifier bridge. Fig. 2.13 illustrates the measured current and voltage waveforms of the converter during G2V operation at maximum power (3.3kW). Moreover, Fig. 2.14 shows the measured efficiency curves in G2V mode under different battery voltages and load conditions.

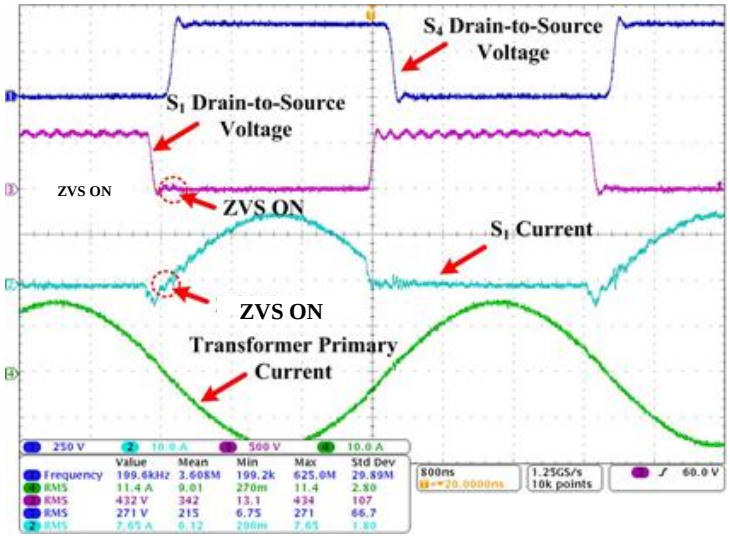


Fig. 2.13. The drain-to-source voltage of S_4, drain-to-source voltage of S_1, switch current of S_1, and primary side resonant current.

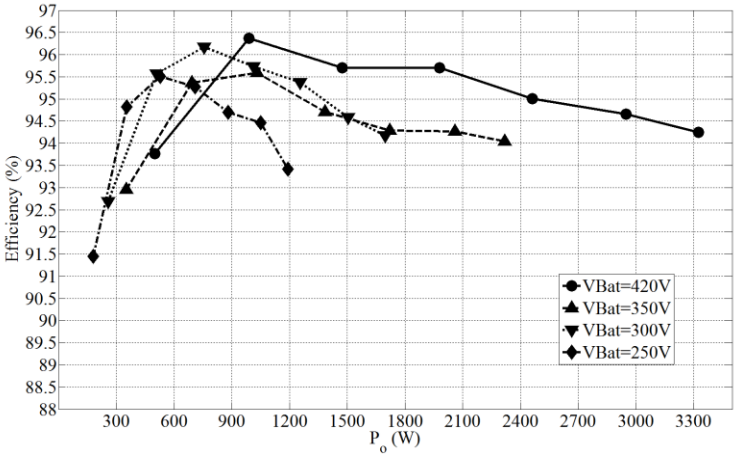


Fig. 2.14. Efficiency of the dual-output DC-DC converter during G2V operation under different load conditions.

2.4.3. Converter performance in V2G mode

In V2G operation, the switches S_3 and S_4 serve as a high-frequency inverter while S_1 and S_2 serve as a rectifier bridge. Fig. 2.15 demonstrates the measured current and voltage waveforms of the converter during V2G operation at 2kW.

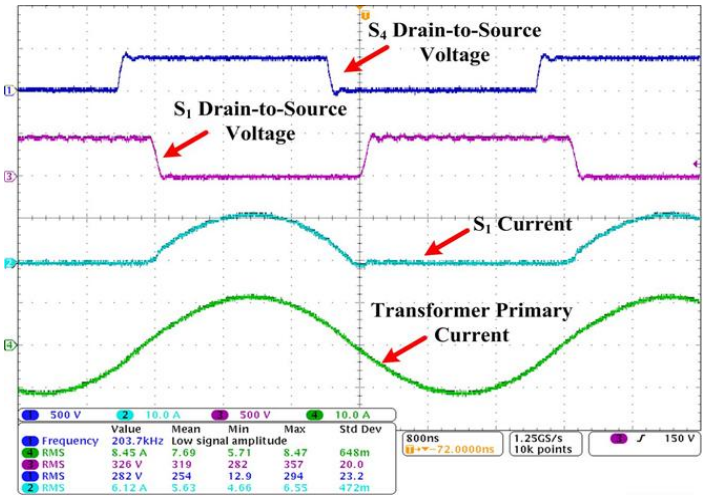


Fig. 2.15. The gate-to-source voltage of S_4, drain-to-source voltage of S_1, switch current of S_1, and primary side resonant current.

Fig. 2.16 shows the CLLC resonant stage efficiency during V2G operation under different load conditions. At an arbitrary input voltage (battery voltage), the efficiency for V2G operation decreases as the output current (DC-link current) increases. At an arbitrary DC link current, the efficiency for V2G increases as the input voltage (battery voltage) increases. Moreover, the maximum efficiency at 1.1kW reaches to 96%.

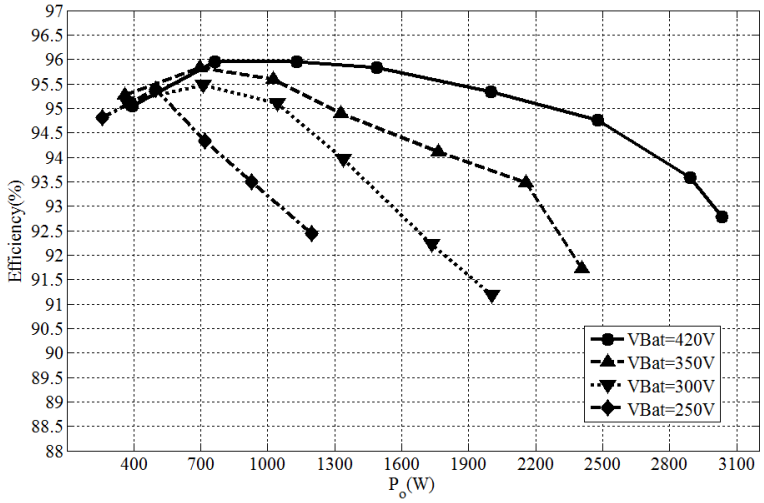


Fig. 2.16. Efficiency of the dual-output DC-DC converter during V2G operation under different load conditions.

2.4.4. Converter performance in H2L mode

During H2L, the primary side of the dual-output DC-DC converter is disabled. The switches S_3 and S_4 serve as a high-frequency inverter while S_5 ~ S_8 serve as a synchronous rectifier. The converter uses the LLC resonant network at secondary side consisting of C_{r3}, C_{r4}, L_{lk2} and L'_m. 1μs deadbands are set in gating signals to ensure that a MOSFET is turned on after its body diode conducts and MOSFET is turned off before its body diode turns off. Large copper bars are used for external connection to reduce the conduction losses. The measured current and voltage waveforms of the converter during H2L operation at 1kW are depicted in Fig. 2.17.

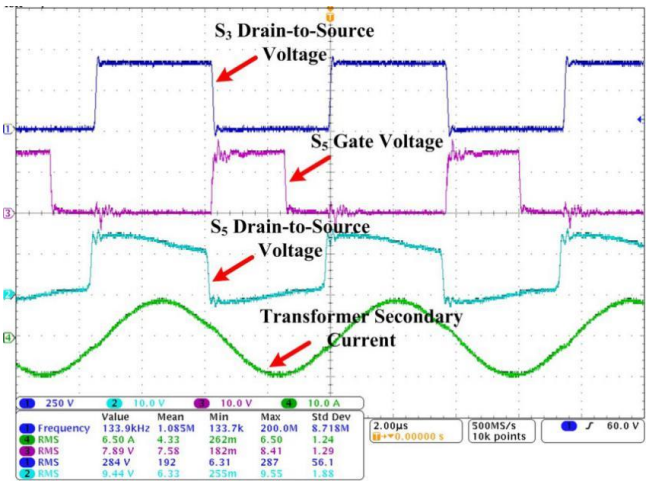


Fig. 2.17. The drain-to-source voltage of S_3, gain-to-source voltage of S_5, drain-to-source voltage of S_5, and secondary side resonant current.

The LLC resonant stage efficiency during H2L operation under different load conditions is plotted in Fig. 2.18. At an arbitrary input voltage (battery voltage), the efficiency for H2L increases as the output current (LV current) increases at low power (<300W). At high power (>300W), the efficiency for H2L decreases as the output current increases. At an arbitrary output current (LV current), the efficiency for H2L increases as the input voltage (battery voltage) increases. The maximum efficiency can be acquired at 500W. The peak second stage efficiency reaches 93.3%.

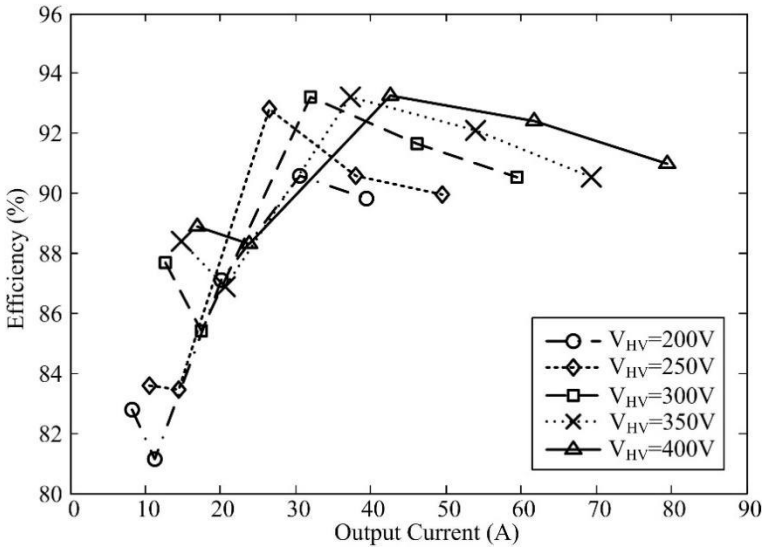


Fig. 2.18. Efficiency of the dual-output DC-DC converter during H2L operation under different load conditions.

2.5. Summary

This chapter outlines an innovative dual-output integrated and isolated converter topology for charging a HV traction battery, LV DC loads and V2G operation in EVs. The proposed topology presents the integration that a half-bridge CLLC converter is intertwined with a half-bridge LLC converter with a minimum number of passive and active components. The magnetic components are integrated into a single three-winding electromagnetically integrated transformer, which leads to an ultra-compact design with improved power density of the converter, improved efficiency and higher voltage isolation. Moreover, an integrated transformer eliminates the risk of saturation due to the flux-doubling effect during start-up of the converter. The half-bridge CLLC converter operates during G2V and V2G operations while the half-bridge LLC converter operates during the H2L operation. In comparison to conventional stand-alone converters, the integrated topology with a fewer number of components improves the gravimetric and volumetric power density of EV's OBC. Modeling, analyses and design guidelines are presented to develop a 3.3-kW prototype. Experimental results are carried out for validation of the operation modes. The maximum efficiency reaches up to 96.5% during G2V and V2G operations, and the peak efficiency during the H2L operation reaches 93.3%.

Chapter 3. Interleaved Totem Pole Power Factor Correction

3.1. Introduction

A PFC circuit is required as the front-end AC/DC stage in OBCs. PFC rectifiers can provide unity power factor and low total harmonic distortion (THD) of the grid current to prevent the power electronics from polluting the power grid by drawing or injecting reactive power and unnecessary harmonics. In this work, a CCM interleaved totem pole PFC is selected as the front-end PFC topology. This selection will be justified with a topological review of boost PFC family in the next section. Despite the fact that this topology has many advantages over others, it suffers from zero-crossing current spike. This current spike not only degrades the input current quality, more specifically THD, but it also can cause failures for the MOSFETs in the PFC circuit. To overcome this problem, the mechanism of current spike generation is investigated. Based on the investigation, an innovative compensation approach is proposed and verified in this chapter. There is well-established literature on the operation and working principle of bridgeless totem-pole PFC [56]-[62], therefore the operation principle of this topology is not included in this dissertation.

3.2. Comparison study of boost PFC topologies

The simplest way to topologically categorized boost PFC circuits is based on the existence of the front-end diode bridge. Based on this, boost PFC circuits can be divided into two major categories: conventional boost PFC circuits and bridgeless boost PFC circuits.

A conventional boost PFC circuit consists of a front-end diode bridge and a regular boost converter as shown in Fig. 3.1(a). Then this converter can be configured into interleaved structure where two boost chokes are in parallel and operating out of phase as shown in Fig. 3.1(b). In such a way, the input current ripple can be reduced by current ripple cancellation effect, thus total inductor volume and the output capacitance can be reduced and the EMI

performance is better. Moreover, two interleaved inductors can be coupled either inversely or reversely [63] as shown in Fig. 3.1 (c) and (d), respectively.

The major issues with conventional boost PFC circuits are (i) high conduction loss in front-end diode bridge, which brings thermal problem and degrades the efficiency; (ii) Reverse recovery loss in output diode which requires the use of a fast diode/schotkky diode.

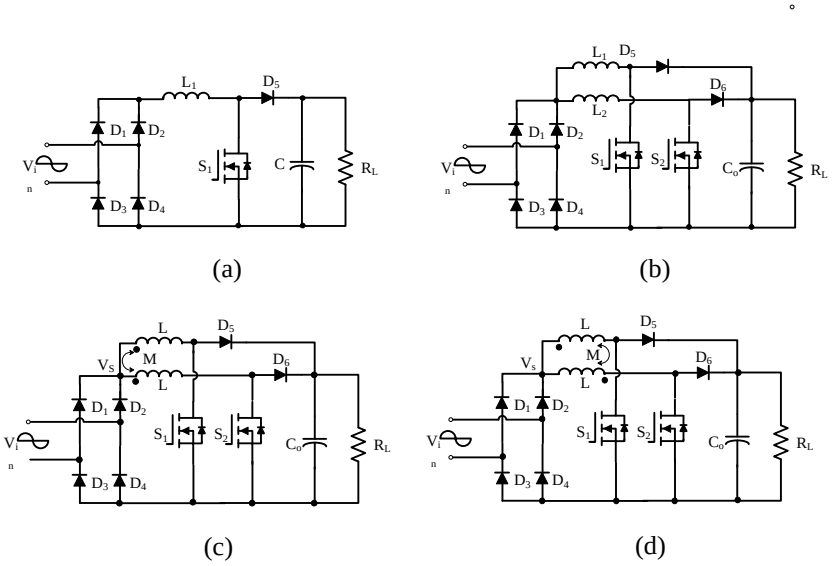


Fig. 3.1. Conventional boost PFC topologies: (a) boost PFC, (b) interleaved boost PFC, (c) directly interleaved boost PFC, (d) inversely coupled interleaved boost PFC.

Topologies of bridgeless PFC circuits are summarized in Fig. 3.2. In those topologies, the diode bridge no longer exists and the efficiency is enhanced as a result, especially under light load and low line conditions.

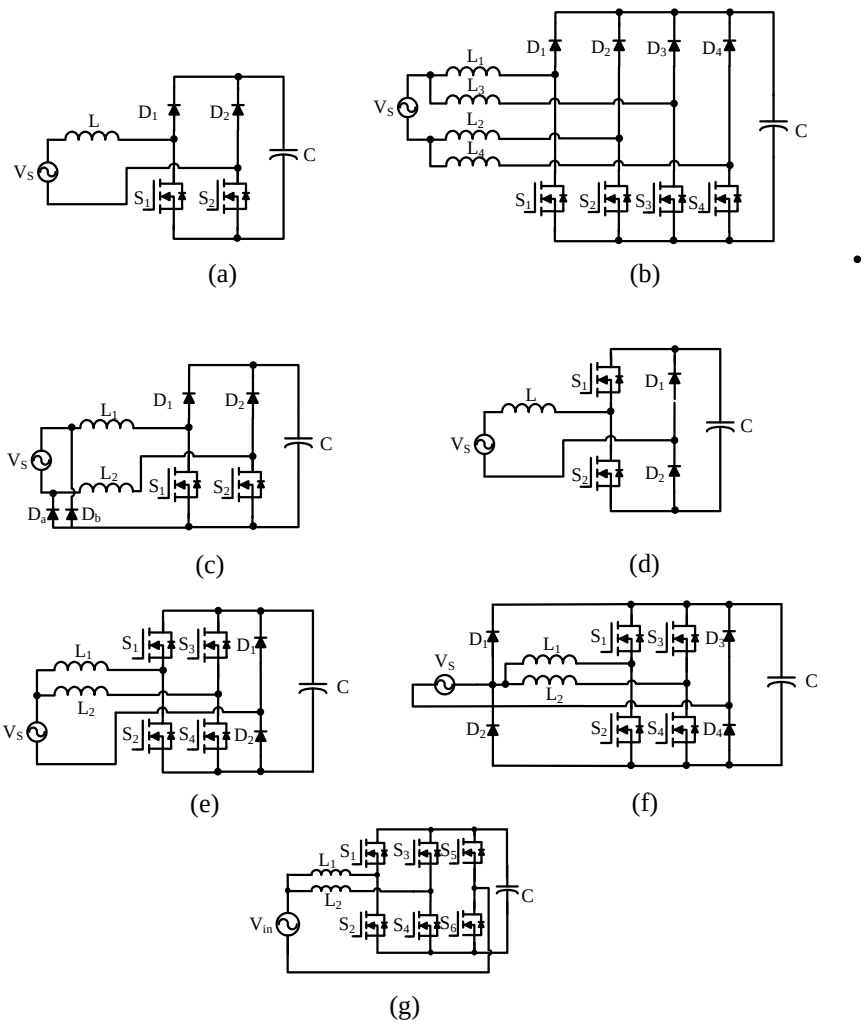


Fig. 3.2. (a) bridgeless boost PFC; (b) Interleaved bridgeless boost PFC; (c) semi-bridgeless boost PFC; (d) totem pole PFC; (e) interleaved totem pole PFC; (f) interleaved resonant boost PFC; (g) proposed bidirectional interleaved totem pole PFC

The conventional bridgeless boost PFC, as shown in Fig. 3.2(a), has the issue of pulsating ground at the load side with respect to the neutral point of the grid. This leads to an extra burden for EMI filter and extra circuit complexity due to input voltage and current sensing solutions [64]. To mitigate the EMI issues, the topology shown in Fig. 3.2(b) was proposed in [65]. In this topology, the EMI performance is improved by interleaved structure where the input current ripple can be greatly reduced. The topology shown in Fig. 3.2(c) is called semi-

bridgeless boost PFC [66]. In this topology, the high frequency pulsation of the floating ground is turned into line-frequency pulsation by two extra free-wheel diodes D_a and D_b. Another brilliant way to improve the EMI performance by slowing down the floating ground pulsation is called totem pole PFC as shown in Fig. 3.2(d). By simply interchanging the position of active switches and slow diodes, the EMI performance is improved without any additional component. In addition, compared to the other bridgeless topologies, the reverse recovery loss for diodes in totem pole PFC is less because those diodes are operating in line frequency despite the reverse recovery loss from the body diode of fast MOSFETs remains the same. So far, the topologies presented above are trying to mitigate the EMI issue by either slowing down the pulsation or current ripple cancellation. A further improvement can be achieved by combining these two together as shown in Fig. 3.2(e). This topology is called interleaved totem pole PFC which has two totem pole PFC circuits in parallel and interleaved [67]. Great EMI performance can be theoretically obtained even though the CM (common mode) noise generated from zero-crossing current spikes has a negative impact on it [68]. The topology in Fig. 3.2(f) is called interleaved resonant boost PFC which is first introduced in [69] by Infineon Technologies and is aimed to be used in level II onboard charger. Compared with the topology in Fig. 3.2(b), it uses four slow diodes to replace the four fast diodes $D_{1\text{-}4}$. Therefore, the efficiency is improved due to the reduction of the reverse recovery loss. Moreover, the efficiency is further improved due to the ZVS of the MOSFETs achieved by CRM operation. The main disadvantages of this topology are (i) high circuit complexity due to the high side drivers, multiple sets of current sensors and additional snubbers; (ii) complicated digital control [65].

In this work, due to the requirement of bi-directional operation, the front-end PFC stage has to work in inverter mode as well. Therefore, bi-directional interleaved totem pole PFC as shown in Fig. 3.2(f) is selected. By replacing two line-frequency diodes with MOSFETs, the PFC rectifier is capable of bi-directional operation while maintaining all the good features of

interleaved totem-pole PFC, i.e. (i) good efficiency, especially in light load and low line voltage conditions; (ii) good EMI performance.

For the convenience of readers, Table 3.1 summarizes a brief comparison among all the aforementioned topologies in terms of applicable power level, magnetics size, efficiency, EMI performance and bi-directional operation capability.

Table 3.1 Brief comparisons among different boost PFCs

Topology	Recommended power rating	Efficiency	Magnetic size	EMI	Bi-directional?
Fig. 3.1(a)	Low	Low	Big	Good	No
Fig. 3.1(b-d)	Medium	Low	Medium	Great	No
Fig. 3.2(a)	Medium	Medium	Big	Bad	No
Fig. 3.2(b)	High	Medium	Small	Good	No
Fig. 3.2(c)	Medium	Medium	Big	Good	No
Fig. 3.2(d)	Medium	Good	Big	Good	No
Fig. 3.2(e)	Medium - High	Good	Medium	Great	No
Fig. 3.2(f)	High	Good	Medium	Good	No
Fig. 3.2(g)	**Medium - High**	**Good**	**Medium**	**Great**	**Yes**

3.3. Zero-crossing current spike of Interleaved Totem Pole PFC

Zero-crossing current spike is a major challenge in an interleaved totem pole PFC. The current spike can come from different mechanism and contains both positive and negative components [70]. Fortunately, by carefully analyzing different mechanism, zero-crossing current spike can be resolved. To simplify the analysis, only one fast-switching leg and slow-switching leg will be addressed in the following study.

The first mechanism of zero-crossing current spike is the reverse recovery from the body diodes of slow MOSFETs. As shown in Fig. 3.3, when line voltage is transitioning from negative half cycle to positive half cycle, the duty ratio of Q_3 jumps from 1 to 0 while the duty ratio for Q_4 abruptly changes from 0 to 1. Meanwhile, the slow switch Q_2 is trying to turn on and Q_1 is trying to block the DC-link voltage. However, due to the reverse recovery from the body diode of Q_1, combined with the junction capacitance of Q_2, the voltage across Q_2 is still remaining V_{DC} at the instance when Q_4 turns on. Meanwhile, line voltage is almost zero at the moment so the AC source can be removed from the equivalent circuit. Therefore, the PFC inductor sees a voltage of V_{DC} and a positive spike is generated. In the same fashion, a negative current spike will be generated when line voltage is transitioning from positive to negative.

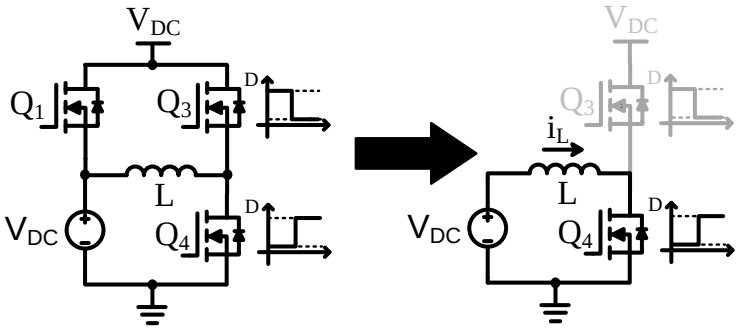


Fig. 3.3. Equivalent circuit when line voltage is transitioning from NEG to POS.

The second mechanism of zero-crossing current spike happens right after the first one. At the moment, Q_2 is on and Q_1 is off. The line voltage is close to zero that the AC source can be removed in the equivalent circuit again. Under this condition as shown in Fig. 3.4, the inductor sees a negative V_{DC} when Q_3 is on, and a negative current spike is generated. With the same fashion, a positive current spike will be generated after line voltage turns into negative half cycle.

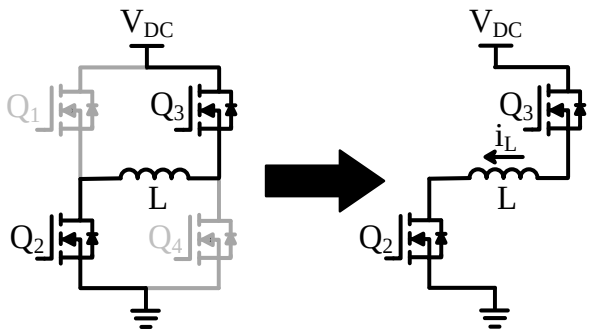


Fig. 3.4. Equivalent circuit when line voltage is positive and Q_2 already turned on.

The third mechanism happens only if the turn-on of Q_2 is even later than the moment when Q_1 has already fully recovered and started to block the DC voltage. At this instance, the line voltage and voltage across Q_2 are both nearly zero. As shown in Fig. 3.5, before Q2 is on, Q3 and Q4 has already started to switch in a complement fashion. When Q_3 is on, the inductor voltage is $-V_{DC}$ and a negative inductor current is building up. With this inductor current, the body diode of Q_2 is reversely biased and the junction capacitance is charged up to a high voltage (close to V_{DC}). Then, Q_3 turns off and Q_4 turns on, the inductor voltage is the V_{ds} of Q_2 and the inductor current is changing in the positive direction. With this process, the inductor current shows a high magnitude swing while maintaining balanced at a small positive average value. However, the operation suddenly changes after the instance when Q_2 turns on. After Q_2 is on, the voltage across it suddenly becomes zero and the volt-second balance of the PFC inductor is temporally lost. A negative inductor current will still be built up with Q_3 turns on, but the small voltage drop of V_g (nearly zero) when Q_4 is on cannot build up enough positive change on inductor current to balance out the previous negative change. Therefore, a negative current spike is formed until the controller tracks the current back to proper sinusoidal. In the same fashion, a positive current spike will be formed in negative half cycle while Q_1 turns on too late. This scenario can take place when the delays from both

digital controller and sensors are significant enough that a misalignment between PWM signal and the inductor current zero-crossing point cannot be negligible anymore.

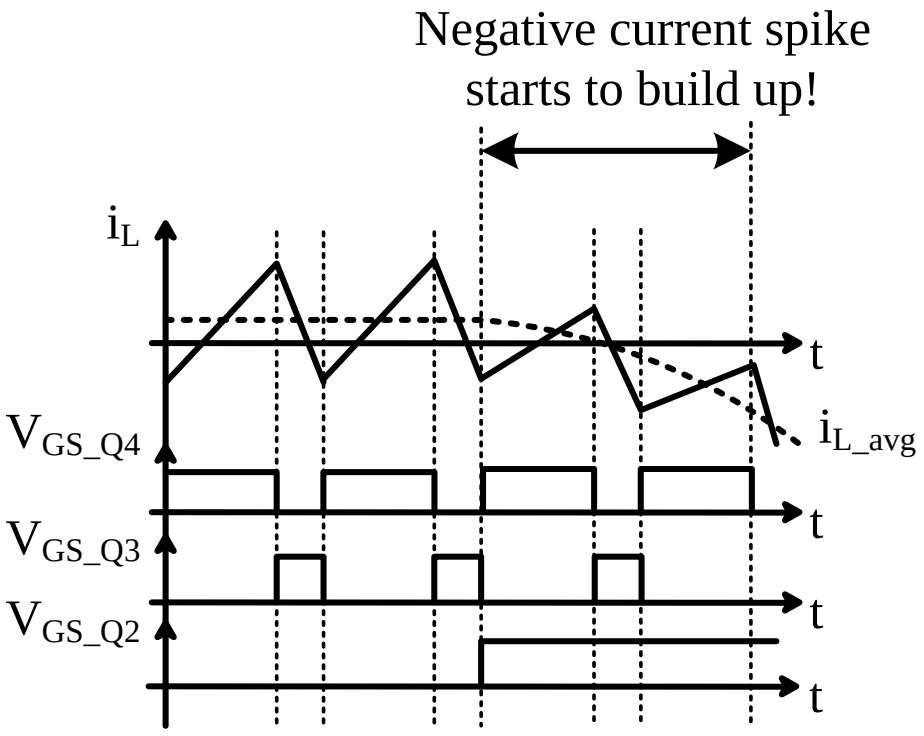


Fig. 3.5. Switching scheme and inductor current if Q_2 turns on too late

Based on the previous analyses, the zero-crossing current spike in interleaved totem pole PFC circuit is a combined result of the reverse recovery current from the body diode of slow MOSFETs, the junction capacitances, abrupt duty ratio change for fast MOSFETS, digital delays and sensor delays. An innovative approach is postposed to compensate the current spike by fixing those factors. First of all, the SiC MOSFETs are used in this work. Compared to regular silicon switches, the reverse recovery of the body diode is low for SiC switches. Moreover, a soft-transition technique is used to reduce the current spike where the duty ratio for fast MOSFETs is changing in small steps (0.1~0.2 per step) instead of jumping between 0 and 1 abruptly. Finally, the digital and sensing delay is eliminated by compensation network

and digital filters. Proposed control diagram for interleaved totem pole PFC circuit is shown in Fig. 3.6.

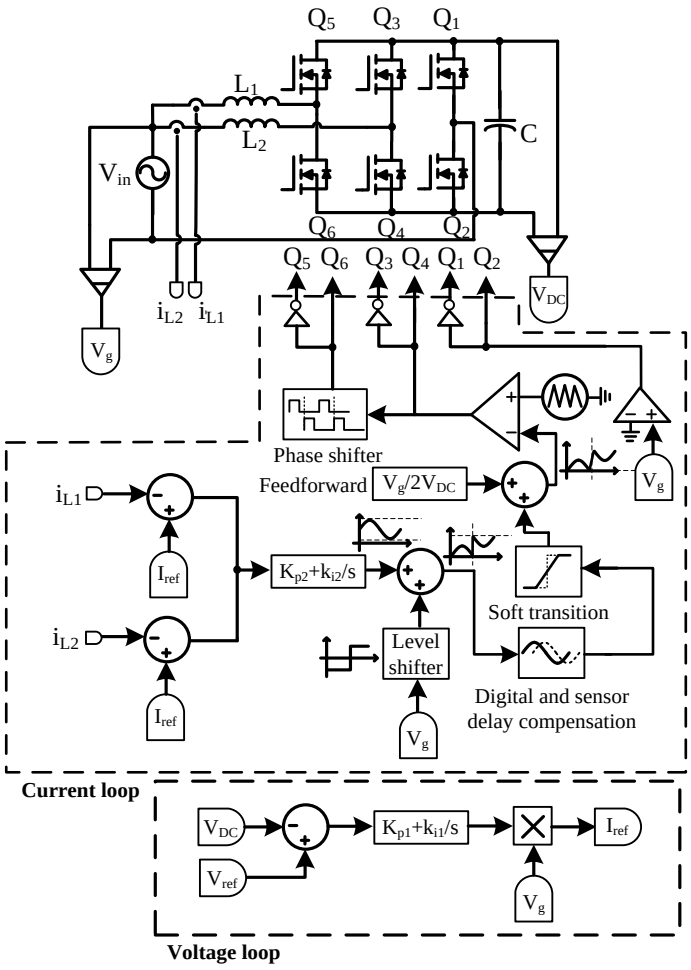
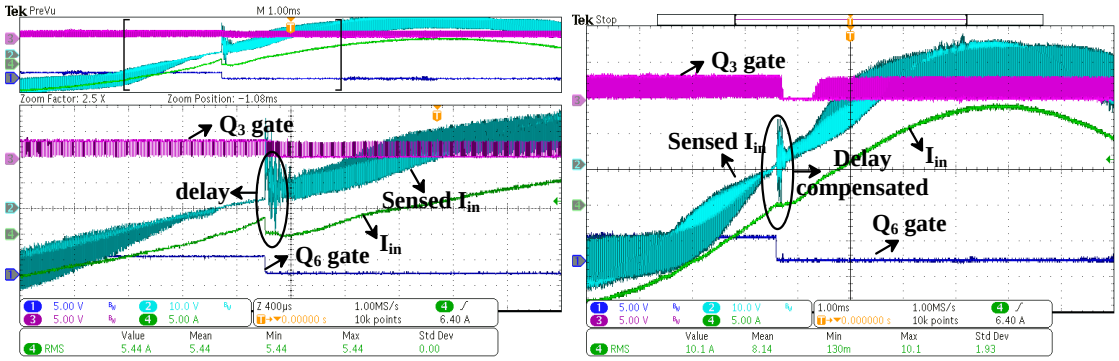


Fig. 3.6. Control diagram for interleaved totem pole PFC

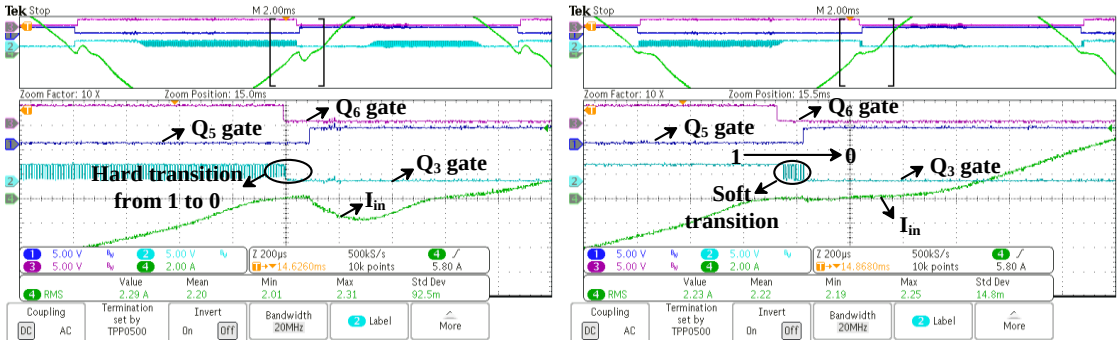
The experimental results shown in Fig. 3.7 - Fig. 3.9 validate the effectiveness of the design. Fig. 3.7(a) shows the how the current spikes generated from the sensing and digital delays and Fig. 3.7(b) shows the input current waveform when delay is properly compensated. Fig. 3.8(a) shows the current spike can be generated by the abrupt change in duty ratio of the fast MOSFETs and Fig. 3.8(b) presents the current waveform when soft

transition block is added to the controller. Finally, Fig. 3.9(a) shows the zero-crossing current spikes in the steady state operation of interleaved totem pole PFC and Fig. 3.9(b) validates the effectiveness of the proposed controller. With this proposed compensation, THD of input current is less than 5%.



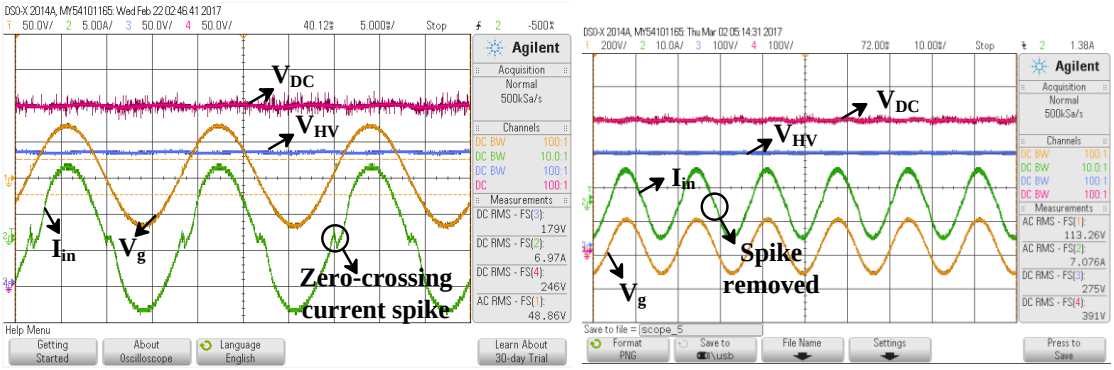
(a) (b)

Fig. 3.7. (a) Current spike from sensing and digital delays. (b) Current waveform with delays compensated



(a) (b)

Fig. 3.8. (a) Current spike from hard duty ratio transition. (b) Current waveform with soft transition.



(a) (b)

Fig. 3.9. (a) Current spike with standard current loop. (b) Current spike removed with proposed control diagram in Fig. 3.6.

3.4. Summary

This chapter starts with a comprehensive review of boost-derived PFC topologies to justify the topology selection for the PFC stage of the proposed integrated charger. Each topology has its own advantages and disadvantages. The topology selection is essentially the balance between different trade-offs. In different applications, efficiency, EMI performance, power density and other factors have different priorities.

Moreover, zero-crossing current spike is investigated. Different mechanisms are analyzed and presented in detail. Based on the analyses, an innovative control diagram to eliminate the zero-crossing current spike is proposed and validated. The experimental results verify the effectiveness of the proposed control and the zero-crossing current spike is properly eliminated. With this proposed compensation, THD of input current is less than 5%.

Chapter 4. Variable DC-link Voltage Control

4.1. Introduction

The typical structure for EV's OBC is a two-stage cascaded system comprised of a PFC circuit followed by an isolated DC/DC converter. For these cascaded converter topologies, the stability and regulation become more critical, which enriches the significance of synthesizing a control loop structure, capable of maintaining the expected regulation. This chapter focuses on analyzing and resolving several issues of variable DC-link control pertaining to the lack of regulation, low frequency oscillation and power quality degradation.

A number of research works [71]-[78] is carried out on AC-DC and DC-DC converters for different applications, aiming at enhancing the net efficiencies. The research work in [71] proposed a single-phase SEPIC PFC followed by a full-bridge LLC converter, connected to a high-voltage EV battery for charging applications. Instead of using a fixed DC link control, it introduced a variable DC link control approach for efficiency enhancement. Although the net efficiency was enhanced by ~3% for the integrated stage in [71], there was no thorough analysis on deriving the integrated control structure and its potential control issues. Furthermore, a variable DC link approach was implemented on a three-level single-stage PFC converter, which inherently operates in a DCM mode. To eliminate the inherent input current distortion in this converter, a higher intermediate DC link voltage reference can be selected; however, the efficiency drops with a rise in the DC link voltage, creating a trade-off between efficiency and power quality. [73] presented a SiC based two-stage EV charger with variable DC-link voltage control and showed a good overall efficiency in experiments. In addition, the research work in [76] proposed a method to ensure optimized DC link voltage for minimizing the total losses in a cascade system consisting of a PFC and a phase-shifted full-bridge (PSFB) converter. However, lower DC link voltage at higher power would result in a higher phase shift requirement for the DC/DC stage, causing higher conduction losses.

Furthermore, a variable DC link control method was applied to a regenerative control application of a bi-directional DC/DC converter for a fuel-cell electric vehicle (FCEV) [78]. The DC link acts as an interface between a DC/DC converter (FCEV battery to a DC voltage) and the propulsion inverter. The distorted output current of the voltage source inverter (VSI) with a fixed DC link at higher power / higher motor speed necessitates a variable DC link voltage to reduce the VSI output ripple current. However, there was no thorough analysis performed on the stability and regulation of the proposed control loop in [78].

Several research works [79]-[83] were performed addressing the instability and power quality degradation issues in cascaded converter stages. The work in [79] focused on the improvement of phase and gain margins through manipulating the input impedance of the second stage in a two-stage AC-DC converter by a digital filter implementation in the feedback loop. Although there is an improvement in the gain and phase crossover frequencies, the method overlooks the effects of the output load power variations. Furthermore, studies on the stability of a two-stage cascaded AC-DC converter were performed in [80], which experimentally resolved an issue of power quality degradation with wide variation in input frequencies. In addition, more related studies [81]-[83] were performed in cascaded AC-DC converters, aiming at improving the phase and gain margins of the inner current loop by modifying the average current control strategy. In most of these studies, individual control loops were used to stabilize the PFC and DC/DC stages separately based on the fixed intermediate DC link voltage. Although the utilization of individual control loops enhances the stability of the integrated stages, the fixed DC link limits the conversion efficiency.

Addressing the aforementioned concerns regarding regulation, stability and efficiency improvement, this chapter comprehensively investigates three possible cases for the voltage loop of the variable DC-link voltage control for two-stage AC-DC converter. Insights into potential issues are explored and two different modes resulting in a stable and well-regulated

variable DC link control structure are derived. Moreover, the main advantage of the variable DC-link voltage control is the improvement of the efficiency across the entire output voltage range. In EV battery charging application, the battery terminal voltage can vary from 250V-420V during constant current (CC) mode and this requires a wide range of output voltage regulation. Given this requirement, the optimization of the efficiency with fixed DC-link voltage can be difficult because when output voltage is regulated at its lower end, the pulse frequency modulation (PFM) control will shift the switching frequency of the DC-DC resonant converter to a higher end for a high step-down ratio and both core loss of the transformer and the switching loss of the secondary side MOSFETs are increased. With the variable DC-link control, even though the efficiency for the PFC stage will be degraded at the higher-end of the output voltage, the DC-DC stage is ensured to operate at the resonant frequency with the optimum efficiency. In addition, when output voltage is regulated at the lower-end of the range, with low DC-link voltage value, the efficiency for PFC stage is improved in comparison to the fixed DC-link voltage control. Therefore, the overall performance across the entire output voltage range can be substantially improved, and the main novelty of this chapter is a new approach to analyze, model and solve the potential issues when designing the voltage loop for variable DC-link control. In addition to the aforementioned issues observed during the experiments, previous work on variable DC-link voltage control for two-stage converters may also potentially face the following practical limitations: 1) requirement of intermediate DC link voltage sensor in the variable DC link control, proposed in [84]-[85]; 2) high sensitivity of DC/DC stage gain variation upon any parameter uncertainty. In the variable DC-link control loop, the DC link reference is generated by multiplying the HV battery voltage by theoretically calculated DC/DC converter gain [84]. However, any change in resonant parameters (especially leakage inductance) may result in gain variation and bring a misleading change in DC link voltage reference causing a lack of converter regulation.

This chapter proposes guidelines to configure the loop structure and select the parameters of compensators to address these issues, with a systematic methodology supported by the thorough mathematical analysis in both time and frequency domains.

4.2. Variable DC-link voltage control

A simplified circuit of the cascaded single phase interleaved totem-pole PFC and a half-bridge CLLC DC/DC converter configuration is shown in Fig. 4.1. The detailed operation principle of the single-phase interleaved totem-pole PFC and CLLC stages can be referred to the well-established literature in [86] and [53], respectively.

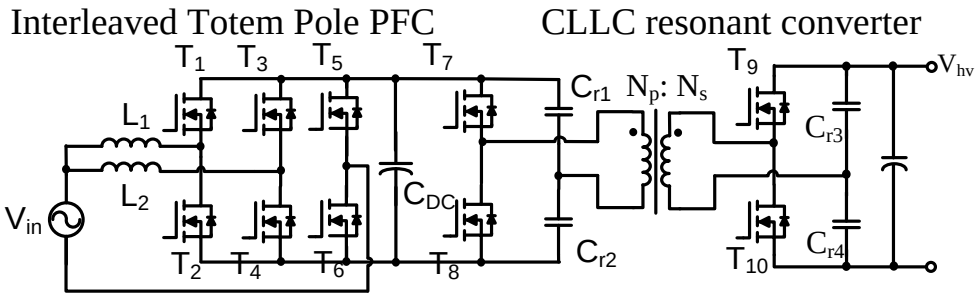
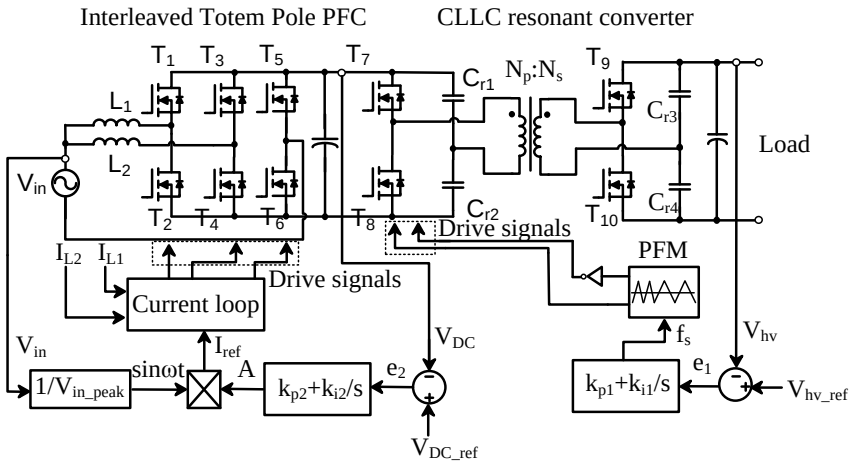


Fig. 4.1. Basic structure of the integrated totem-pole PFC and CLLC DC/DC converter.

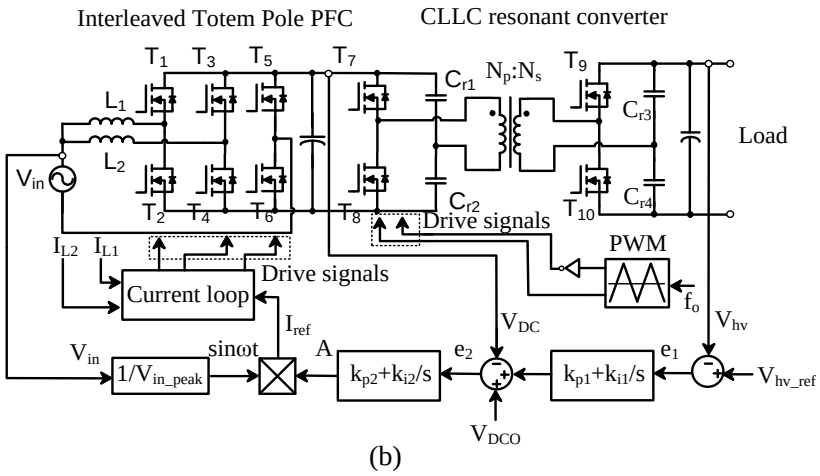
In such a system, the most common practice to achieve the battery voltage regulation is to fix the DC-link voltage and adjusting the gain of DC/DC stage as shown in Fig. 4.2 (a). There are independent controllers for PFC and DC/DC stages. The PFC controller shapes the input current into a sinusoidal waveform, which ensures unity power factor and regulates the output DC-link voltage at a fixed desired value, and the controller of CLLC resonant converter regulates the output voltage by PFM control. However, the maximum efficiency of series resonant converter can only be achieved at the resonant frequency [71]. Therefore, for wide

output voltage range applications like EV charger, variable DC-link control is a better methodology.

The variable DC link control structure is shown in Fig. 4.2(b). As shown in Fig. 4.2(b), the error signal e_1 is processed by a PI compensator. Then the sensed DC-link voltage V_{DC} is subtracted from the output of the compensator. Meanwhile, the feedforward term V_{DC0} is added to improve the performance of the control. The output voltage steady state error can be eliminated by properly configuring this feedforward term, as shown analytically later in this Section. Finally, the computation result is fed to another PI compensator to generate the current reference for the inductor current controller. Meanwhile, the CLLC resonant converter operates in open loop configuration at the resonant frequency to ensure optimum efficiency. While the primary side MOSFETs are operating with the resonant frequency, the secondary side MOSFETs are driven by the SR signals to ensure the best possible efficiency.



(a)



(b)

Fig. 4.2. Control diagram for charging systems: (a) conventional fixed DC-link control (b) proposed variable DC-link control

The proposed variable DC-link control strategy shows a substantial efficiency improvement compared to conventional fixed DC-link control, as verified in later section. The modeling and design considerations of the voltage loop are discussed in the next section.

4.3. Voltage loop modeling and synthetization

As aforementioned, the variable DC-link voltage loop potentially faces several issues: (i) loss of output voltage regulation and (ii) low frequency oscillations in the DC voltages and inductor current. In order to address and analyze these issues, both time-domain and frequency-domain studies of the control loop are performed, which lead to two different voltage loop controller configurations.

During the study of the loop, the control structure shown in the Fig. 4.2(b) will be configured into three different cases which will be discussed later in this section. Before the analyses, several assumptions need to be made to simplify the derivation: 1) The current loop is designed to be ~10-times faster than the outer voltage loop to ensure that the input current of the PFC stage perfectly tracks its reference value; 2) It is assumed that both PFC and

CLLC stages are lossless; 3) The input current distortion is managed by properly selecting the circuit parameters and the control implementations. The control proposed in Chapter 3 is implemented to reduce the zero-crossing current spikes. Therefore, it is a valid assumption that the PFC current loop is working ideally.

From Fig. 4.2 (b), in order to minimize the error between target output voltage and the sensed output voltage, PI compensators are implemented. Based on the loop structure shown in Fig. 4.2(b), the time-domain expression for the active power reference '*A*' can be obtained as follows.

$$e_1 = V_{HV\_ref} - V_{HV} \tag{4.1}$$

$$e_2 = k_{p1}e_1 + k_{i1}\int_0^t e_1 dt + V_{DC0} - V_{DC} \tag{4.2}$$

$$A = k_{p1}k_{p2}e_1 + k_{p2}(V_{DC0} - V_{DC}) + \left(k_{p1}k_{i2} + k_{p2}k_{i1}\right)\int_0^t e_1 dt + k_{i2}\int_0^t (V_{DC0} - V_{DC})dt + k_{i1}k_{i2}\iint_0^t e_1 dt^2 \tag{4.3}$$

Without loss of generality, the following relations hold true.

$$e_1 = E \tag{4.4}$$

$$\int_0^t e_1 dt = E_1 + Et \tag{4.5}$$

$$V_{DC0} - V_{DC} = E_2 \tag{4.6}$$

$$\int_0^t (V_{DC0} - V_{DC})dt = E_2 t \tag{4.7}$$

where, E, E_1 and E_2 are integral constants, k_{p1}, k_{p2}, k_{i1} and k_{i2} are the parameters for PI compensators and V_{DC0} and V_{DC} are the feedforward term and the actual DC-link voltage as shown in Fig. 4.2. By substituting Eq. (4.4) – Eq. (4.7) into Eq. (4.3), the active power reference can be rewritten as:

$$A = k_{p1}k_{p2}E + k_{p2}E_2 + \left(k_{p1}k_{i2} + k_{p2}k_{i1}\right)E_1 + \left[k_{i2}E_2 + \left(k_{p1}k_{i2} + k_{p2}k_{i1}\right)E + k_{i1}k_{i2}E_1\right]t + \frac{1}{2}k_{i1}k_{i2}Et^2 \tag{4.8}$$

The inductor current references are generated by multiplying active power reference '*A*' to the measured input voltage. For stable operation, the time-dependent component in the expression should be zero, as '*A*' should held constant at any load power. This requirement constrains the selection of PI parameters. Thus, the design considerations can be obtained and three different operating modes are available by different control loop configurations (Case I, case II and case II), which will be analyzed as follows.

4.3.1. Case I: Loss of regulation and low frequency oscillations with non-zero k_{i1} and k_{i2}

(1) Time domain analyses

In this case, the steady state error for output voltage is assumed to be zero beforehand to provide a deeper insight to the impacts on regulation from the compensator parameter selection.

$$e_1 = 0 \tag{4.9}$$

$$\int_0^t e_1 dt = E_1 \tag{4.10}$$

$$V_{DC0} - V_{DC} = E_2 \tag{4.11}$$

$$\int_0^t (V_{DC0} - V_{DC}) dt = E_2 t \tag{4.12}$$

Substituting Eq. (4.9) – Eq. (4.12) into Eq. (4.3), the expression for the active power reference, the following expression can be obtained:

$$A = \left(k_{p2}k_{i1} + k_{p1}k_{i2}\right)E_1 + k_{p2}E_2 + (k_{i1}k_{i2}E_1 + k_{i2}E_2)t \tag{4.13}$$

For the stable operation, the time dependent component should not exist. As the assumption for this case, both k_{i1} and k_{i2} are non-zero, the following constraint should be satisfied.

$$k_{i1}E_1 + E_2 = 0 \tag{4.14}$$

Also, '*A*' can be related with the output power:

$$\frac{A<V_{in}>_{rms}}{\sqrt{2}} = \frac{G^2 V_{DC}^2}{2R} \tag{4.15}$$

Combining Eq. (4.13) – Eq. (4.15), the relation among feedforward term V_{DC0}, PI compensator parameters and power stage operating conditions can be obtained.

$$V_{DC0} = V - \frac{\sqrt{2}G^2 V_{DC}^2}{2R<V_{in}>_{rms} k_{p1}} \left(\frac{k_{i1}}{k_{i2}}\right) \tag{4.16}$$

By defining $M = \frac{\sqrt{2}G^2}{2R<V_{in}>_{rms} k_{p1}} \left(\frac{k_{i1}}{k_{i2}}\right)$, Eq. (4.16) can be expressed in the form of a quadratic equation:

$$V_{DC}^2 - \frac{1}{M} V_{DC} + \frac{V_{DC0}}{M} = 0 \tag{4.17}$$

The solution of this equation will be:

$$V_{HV} = GV_{DC} = \begin{cases} Complex\ number & \left(M > \frac{1}{4V_{DC0}}\right) \\ \frac{\frac{G}{M}\left(1-\sqrt{1-4MV_{DC0}}\right)}{2} & \left(M \leq \frac{1}{4V_{DC0}}\right) \end{cases} \tag{4.18}$$

In practice, M is very small and $M \leq \frac{1}{4V_{DC0}}$ holds always true. Based on this fact, Eq. (4.18) can be further simplified into Eq. (4.19).

$$V_{HV} = \frac{G}{2M}\left(1 - \sqrt{1 - 4MV_{DC0}}\right) \tag{4.19}$$

It is clearly indicated by Eq. (4.19) that the output voltage is inherently settled at a particular level, which is governed by the following factors: G (the gain of DC/DC stage), and M (a function of the parameters from both power stage circuit and control loop). None of these factors has any relation with the target output voltage V_{HV_ref}. This indicates the loop loses the regulation on the output voltage.

(2) Frequency domain analysis

The low frequency oscillations around the DC voltage and inductor current are observed under the converter operation in this case. This can be explained using frequency domain analyses of the closed loop integrated converter. In order to prove this phenomenon, the transfer function $\frac{V_{DC\_ref}}{V_{hv\_ref}}$ needs to be analyzed. In order to obtain the DC link voltage variation

across different operating condition, it is required to establish a large signal transfer function between the intermediate DC link voltage and its reference, which is derived as follows.

Assuming the inner current loop to be considerably faster than the outer voltage loop and by setting a proper bandwidth for the current loop compensator, the voltage loop structure can be represented in following way as shown in Fig. 4.3. In the voltage loop plant, V_{avg} denotes the average input voltage over 'N' data points ($N=T/T_s$, where T is the line cycle period and T_s is the switching time period).

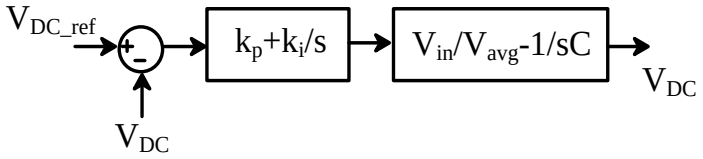


Fig. 4.3. Typical voltage loop configuration in average current mode control.

Therefore, the transfer function between the actual DC link voltage and its reference is given by as follows.

$$\frac{V_{DC}}{V_{DC_{ref}}}(s) = \frac{k_p s + k_i}{s^2 Ck + k_p s + k_i} \tag{4.20}$$

where $K=V_{avg}^2/V_{in}$.

On the other hand, in the control loop structure shown in Fig. 4.2(b), which consists of two different voltage loops, the equivalent DC link for the PFC stage is given as follows.

$$V_{DC\_ref} = \frac{k_{p1}s + k_{i1}}{s}(V_{hv_{ref}} - GV_{DC}) \tag{4.21}$$

where V_{DC_ref} is the sum of output voltage PI controller output and the feedforward term V_{DC0}, and k_{p1} and k_{i1} are the proportional and integral voltage gains of the outer DC voltage loop. Also, assuming k_{p2} and k_{i2} to be the proportional and integral gains for the inner DC voltage (PFC stage) controller, V_{DC} can be replaced in terms of V_{DC_ref} by plugging Eq. (4.20) into Eq.

(4.21). Thus the following relationship between the final DC reference voltage and intermediate DC link voltage reference can be derived.

$$\frac{V_{DC\_ref}}{V_{hv\_ref}} = \frac{(k_{p1}s+k_{i1})[s^3Ck+(k_{p2}s+k_{i2})(s+G(k_{p1}s+k_{i1}))]}{s^4Ck+k_{p2}s^3+k_{i2}s^2} \tag{4.22}$$

Given a constant reference for the output voltage, a constant reference will be generated for the PFC output DC-link. Therefore, a constant magnitude gain with phase closely being zero is expected in the Bode plot of the derived transfer function. However, as seen in the Bode plot, there is a significant amplification in the transfer function magnitude at the low-end frequency range (~10-20 Hz). Physically it means that although the output voltage reference is held constant, the generated PFC DC-link reference has a very low frequency envelope, which also results in a slow-varying envelop of the same frequency in the output voltage waveform. Fundamentally, it implies a power cycling phenomena happening at a very low frequency (even lower than AC grid frequency), which persists across the peaks and valleys of the inductor current waveforms. Aside from the lack of regulation, the oscillations in the DC voltages would potentially result in the degradation of lifetimes of the capacitors. Furthermore, it is notable that the frequency of the power cycling changes with the selection of controller parameters, which is shown in two different Bode plots using different voltage loop controller parameters. The low frequency oscillations in the waveforms of both the DC voltages and inductor currents are verified from the experimental results, presented in the next section.

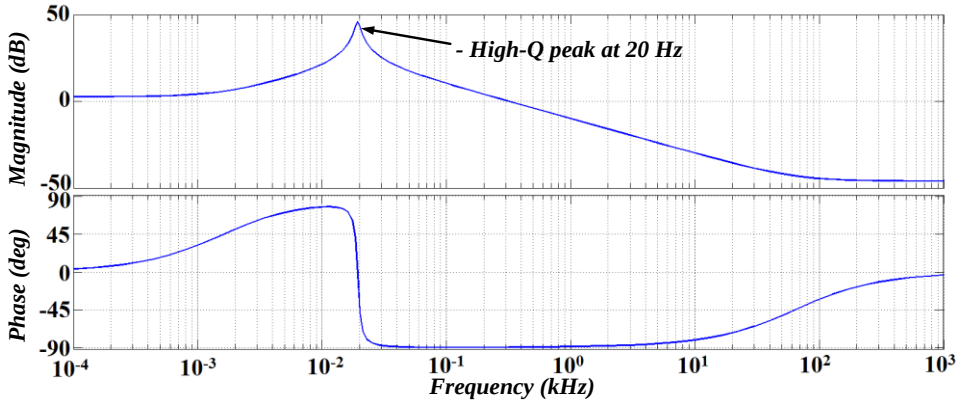


Fig. 4.4. Bode plot of $V_{DC}\_ref(s)/V_{HV}\_ref\ (s)$ using k_{p1}=0.005; k_{p2}=0.01; k_{i1}=20; k_{i2}=0.628;

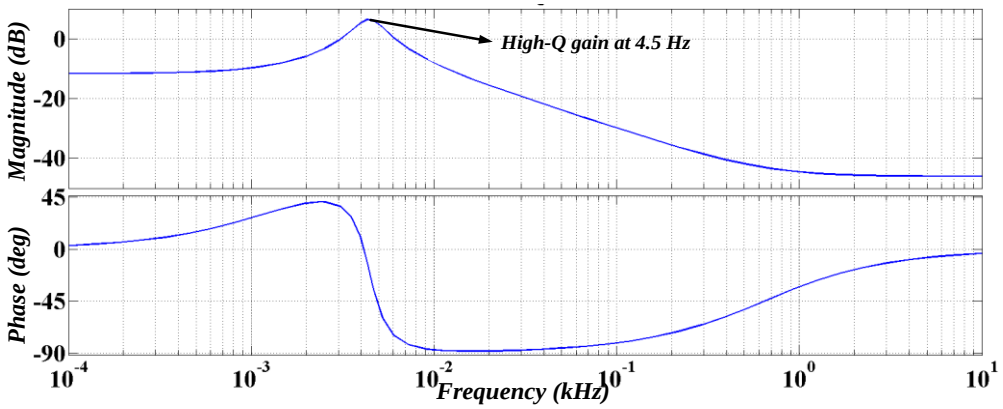


Fig. 4.5. Bode plot of $V_{DC}\_ref(s)/V_{HV}\_ref\ (s)$ using k_{p1}=0.005; k_{p2}=0.01; k_{i1}=10; k_{i2}=0.628;

The ultimate objective is to set a constant ratio between PFC output DC-link voltage reference and CLLC output DC reference. Also, the common gain between V_{DC_ref} and V_{HV_ref} is G, which is fixed by the choice of switching frequency of the DC/DC stage at a fixed load power. One easy way to ensure the constant gain is by setting a common ratio of G between the coefficients of different orders of 's' in numerator and denominator in the expression Eq. (4.22). Comparing the coefficients of s^3, the following is obtained:

$$k_{p1} = \frac{1}{G} \tag{4.23}$$

Comparing the coefficients of s^2, the following is obtained:

$$k_{p1}k_{p2} + kk_{i1}C = \frac{(k_{p2}k_{i1} + Gk_{p1}k_{p2})}{G} \tag{4.24}$$

$$k_{p2} = kCG \text{ or } k_{i1} = 0 \tag{4.25}$$

Comparing the coefficients of s^1, the following is obtained:

$$k_{p1}k_{i2} + k_{p2}k_{i1} = \frac{(k_{i2} + Gk_{p2}k_{i1} + Gk_{p1}k_{i2})}{G} \tag{4.26}$$
$$k_{i2} = 0$$

The coefficients of s^0 inherently have the desired interrelation.

4.3.2. Case II: Reduced to two P compensators with $k_{i1} = k_{i2} = 0$ and feedforward term V_{DC0}

(1) Time-domain analysis

The time-domain analyses in this mode will be conducted using the above-mentioned assumption (*ii*), which can be mathematically formulated using the following relation.

$$P_{in} = \sqrt{2}A < V_{in} >_{rms} = P_o = \frac{V_{hv}^2}{R} = \frac{G^2 V_{DC}^2}{R} \tag{4.27}$$

where, P_{in} and P_o represent the input and output powers, respectively and G is the gain of CLLC resonant converter. Moreover, the time domain expression of the active power reference '*A*' can be written as the following by using Eq. (4.8) and Eq. (4.27) and imposing $k_{i1}=k_{i2}=0$.

$$A = k_{p1}k_{p2}E + k_{p2}E_2 = \frac{\sqrt{2}G^2V_{DC}^2}{2R<V_{in}>_{rms}} \tag{4.28}$$

Rearranging Eq. (4.28), the following expression for the steady state error can be obtained.

$$E = \frac{\sqrt{2}G^2V_{DC}^2}{2R<V_{in}>_{rms}k_{p1}k_{p2}} - \frac{V_{DC0}-V_{DC}}{k_{p1}} \tag{4.29}$$

In this case, the output voltage steady state error is given by Eq. (4.29). To eliminate it, the following design constrain must be satisfied:

$$k_{i1} = k_{i2} = 0,\ V_{DC0} = V_{DC}(1 + \frac{\sqrt{2}G^2V_{DC}}{2R<V_{in}>_{rms}k_{p2}}) \tag{4.30}$$

By implementing this solution, the equivalent loop structure can be obtained as shown in Fig. 4.6.

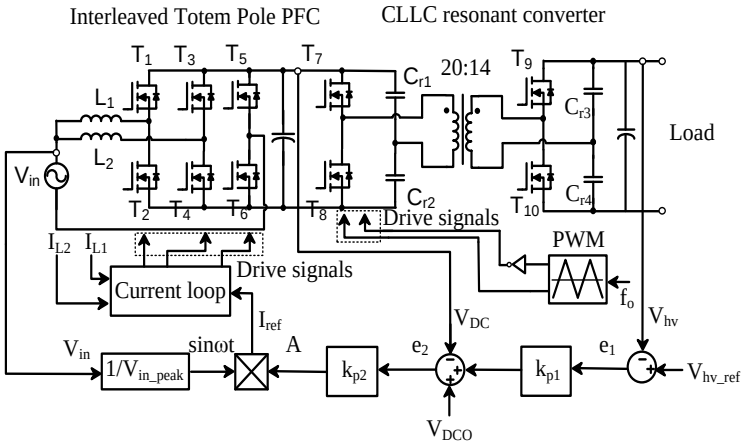


Fig. 4.6. Equivalent loop configuration for case II.

(2) Frequency domain analysis

Using the plant characteristics as $G(s)=V_{HV}/sL$, the equivalent open loop gain of the control structure shown in Fig. 4.6 is demonstrated by a Bode plot, presented in Fig. 4.7. As implied by the plot, the bandwidth and phase margin of the designed loop are 7 kHz and 90 degrees, respectively. As implied by the frequency response, the gain slope is -20 dB/decade which offers a relatively low attenuation to the high frequency components. Presence of high frequency components may lead to degradation in input power quality or loop instability. Even though the high-Q peak does not exist in the closed-loop bode plot as shown in Fig. 4.8, this configuration is still not practically desired mainly due to two reasons: 1) output voltage steady-state error is difficult to eliminate and 2) dynamic performance is not the best.

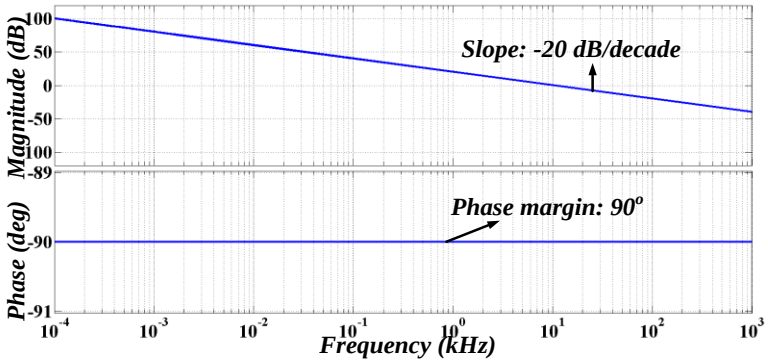


Fig. 4.7. Open loop gain response of the equivalent control structure in case II.

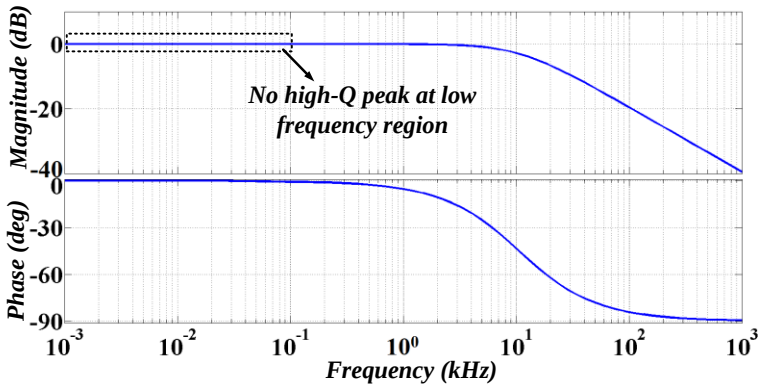


Fig. 4.8. Closed loop Bode plot of case-II controller

4.3.3. Case III (Proposed): Reduced to single PI compensator with $\mathrm{k_p} = \mathrm{k_{p1}} * \mathrm{k_{p2}}$, $\mathrm{k_i} = \mathrm{k_{i2}}$, $\mathrm{V_{DC0}} = \mathrm{V_{DC}}$

(1) Time-domain analysis

By assuming $k_{i1} = 0$, the time-dependent quadratic term will vanish. In addition, the time-dependent linear terms can also be eliminated if Eq. (4.31) holds true.

$$E = -\frac{E_2}{k_{p1}} = \frac{V_{DC} - V_{DC0}}{k_{p1}} \tag{4.31}$$

As Eq. (4.31) indicates, in this case, the steady state error is proportional to the difference between sensed V_{DC} and the feedforward term V_{DC0}. Meanwhile, k_{p1} needs to be small to make the voltage loop at least 10 times slower than the PFC current loop for holding

assumption (*i*) true. Therefore, the steady state error of the output voltage can be amplified with a big margin by any small difference between the sensed DC-link voltage and the feedforward term. The ideal solution is to make the feedforward term equal to the measured DC-link voltage as shown in Eq. (4.32), which equivalently eliminates the inclusion of the measured V_{DC} in the loop shown in Fig. 4.2(b) and the derived control diagram is shown in Fig. 4.9 for readers' convenience.

$$k_{i1} = 0, V_{DC0} = V_{DC} \tag{4.32}$$

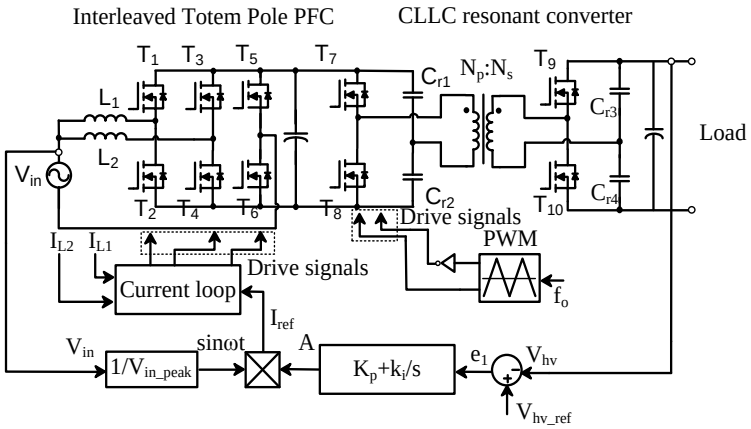


Fig. 4.9. Equivalent loop configuration for case III.

(2) Frequency domain analysis

Similar to case II, using the plant characteristics as $G(s)=V_{HV}/sL$, the equivalent open loop gain of the control structure shown in Fig. 4.9 is demonstrated by a Bode plot, presented in Fig. 4.10. As implied by the plot, the bandwidth and phase margin of the designed loop are 20 kHz and ~67.5 degrees, respectively. The gain response has a slope of -40 dB/decade, which offers a higher attenuation to the high frequency components, in comparison to -20dB/decade slope in case II. Also, the issue of low frequency oscillation in case I controller is eliminated using case III control strategy, which is demonstrated in Fig. 4.11.

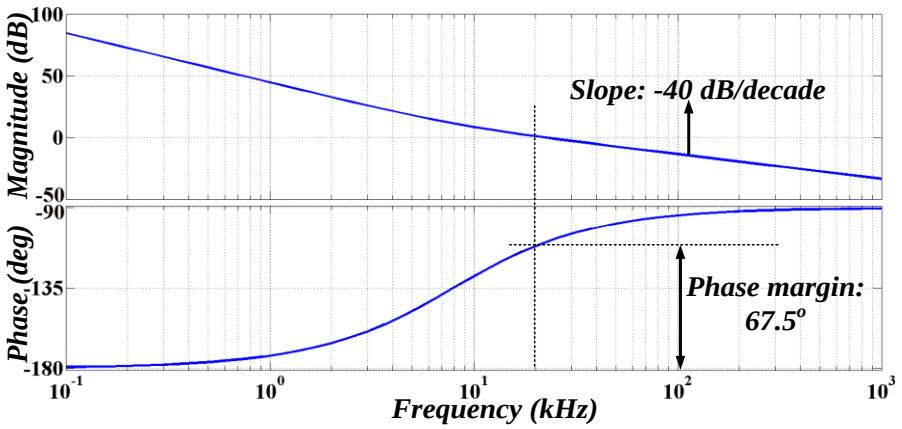


Fig. 4.10. Open loop gain response of the equivalent control structure in case III.

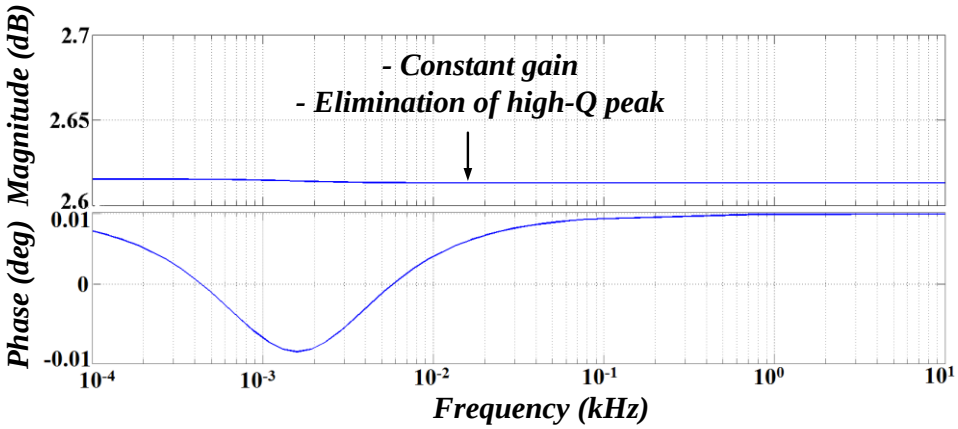


Fig. 4.11. Closed loop Bode plot of case-III controller;

4.4. Experimental verifications

The picture of a 2*kW* hardware prototype is shown in Fig. 4.12.

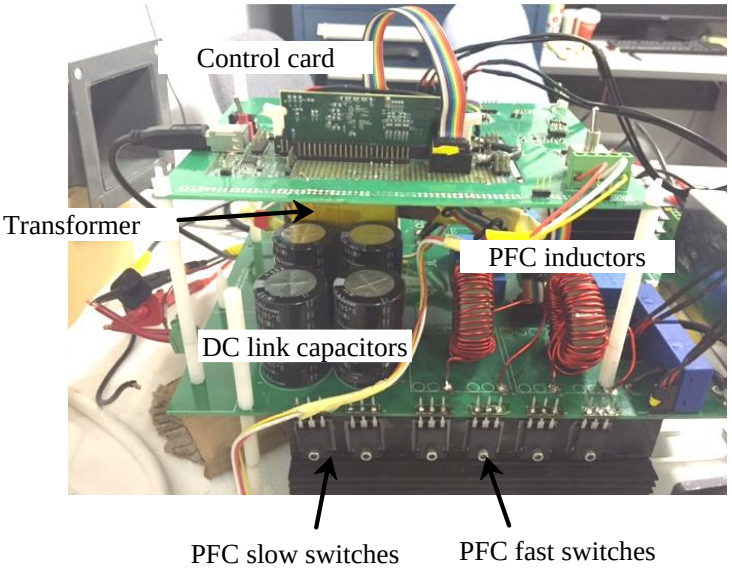


Fig. 4.12. The image of the 2kW prototype.

Fig. 4.13 shows the low frequency oscillation in the inductor current, if the controller is not properly designed. As predicted by the frequency domain analysis, 16*Hz* low frequency oscillation is observed. By proper configuration of loop parameters, as shown in Fig. 4.14 for 1.5*kW* output power, the undesired oscillation is eliminated. An improved power factor of 0.992 and THD <5% are achieved in the steady state.

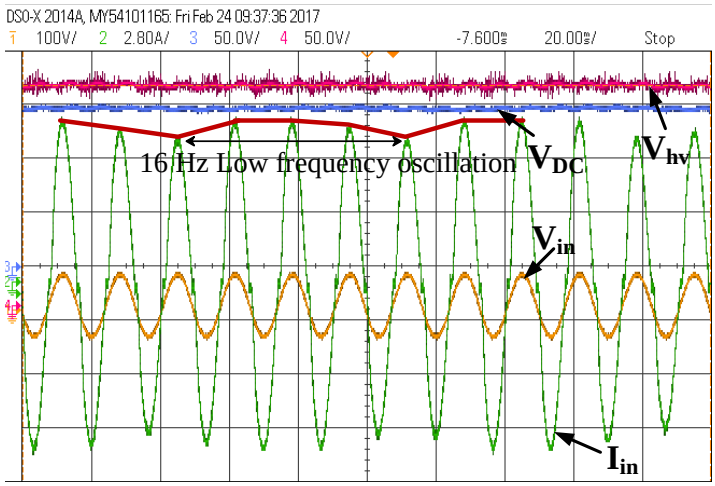


Fig. 4.13. Low frequency oscillation in the inductor current, as predicted by the frequency domain analysis.

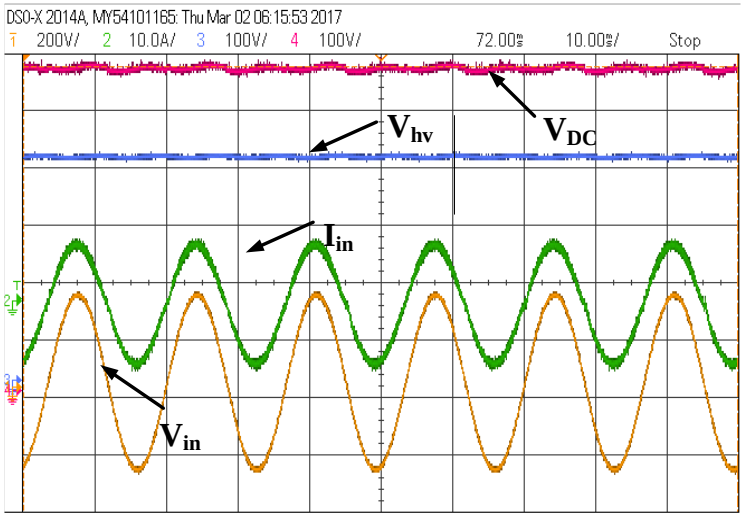


Fig. 4.14. Steady state waveform $P_o = 1.5kW$, $PF = 0.992$, V_{hv} is regulated at ~400V.

In addition, the step-up (1.5kW to 2kW) and step-down (2kW to 1.5kW) load transient waveforms are shown in Fig. 4.15, which illustrates the effectiveness of the proposed control loop, designed in two different methods i.e. Case II and case III. Furthermore, Fig. 4.16 represents the measured efficiencies for both fixed and variable DC link control strategies under different output voltage levels. The experimental measurements substantiate the claim that variable DC-link control can improve the efficiency over the wide output voltage range.

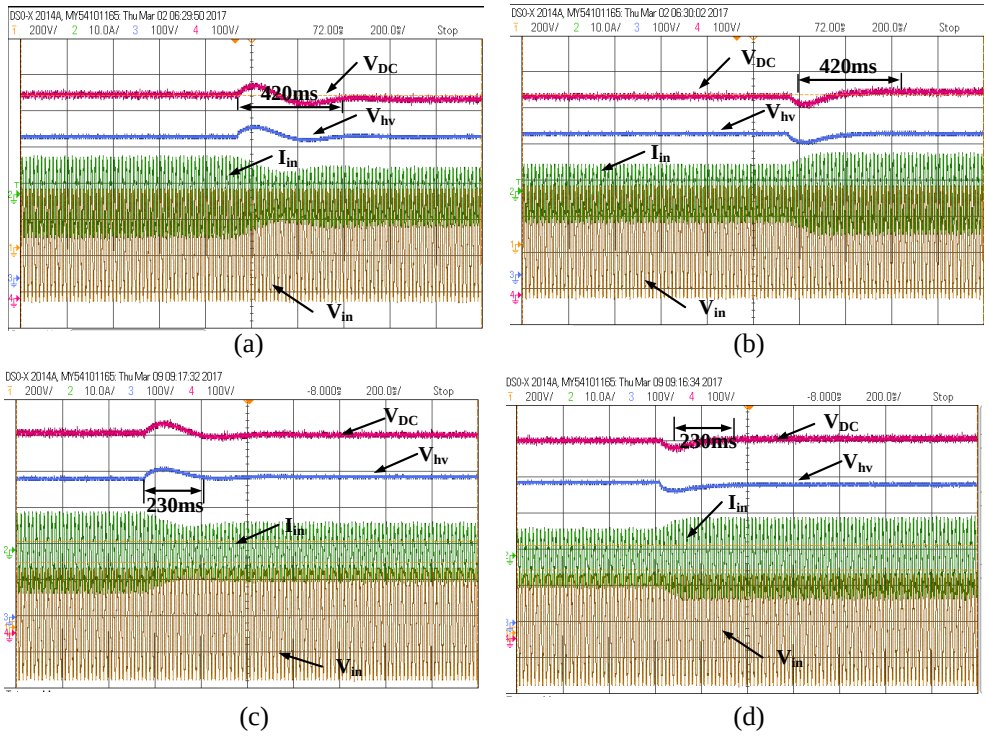


Fig. 4.15. Load step up and step down transients between 2kW and 1.5kW for different cases (a) Case II: load transient from 2kW to 1.5kW (settling time: 420ms); (b) Case II: load transient from 1.5kW to 2kW (settling time: 420ms); (c) Case III: load transient from 2kW to 1.5kW (settling time: 230ms); (d) Case III: load transient from 1.5kW to 2kW (settling time: 230ms).

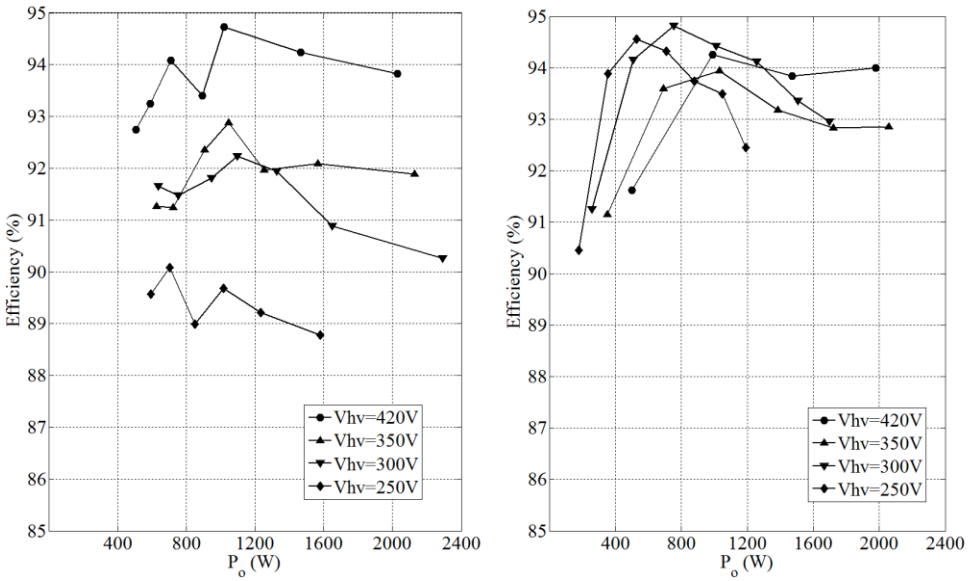


Fig. 4.16. Efficiency curves for a wide output voltage range (a) fixed DC-link strategy (b) variable DC-link strategy.

4.5. Summary

In this chapter, an approach to model and synthesize a variable DC link control structure for an integrated two-stage AC/DC converter is proposed. A proof-of-concept prototype is developed and tested up to 2kW at 220V RMS, 60Hz AC input. The proposed variable DC-link control method is verified to be a more efficient approach than a fixed DC link control method. A peak efficiency of 94% and an overall better efficiency over the entire output voltage range are obtained during the experiments. Moreover, the proposed control structure eliminates the low frequency oscillation around the DC voltages and inductor current. An input power factor of 0.992 and input current THD of <5% are obtained from the steady state experimental results.

Chapter 5. Grid to Both Batteries (G2B) Mode: Simultaneously Charging of both HV and LV Batteries

5.1. Introduction

Before charging the HV battery, the battery pack needs to go under a preconditioning process within which the battery pack and the cabinet are warmed up by the heaters for a better battery performance and prolonged battery life. During the charging process, the LV battery needs to be functional to supply the auxiliary electrical loads from the vehicle controller. Therefore, a charging system capable of simultaneously charging both HV and LV batteries, to prevent the LV battery getting depleted, is required. In a conventional EV charging system, this can be managed as there is an independent APM that can constantly charge the LV battery from the HV battery as shown in Fig. 5.1 (a); although, this could also become challenging, if the HV battery is fully depleted. Therefore, to make the proposed integrated OBC more promising, an additional operation mode is required that can charge both batteries from the grid, i.e. G2B mode. The proposed integrated charger with G2B mode is shown in Fig. 5.1 (b).

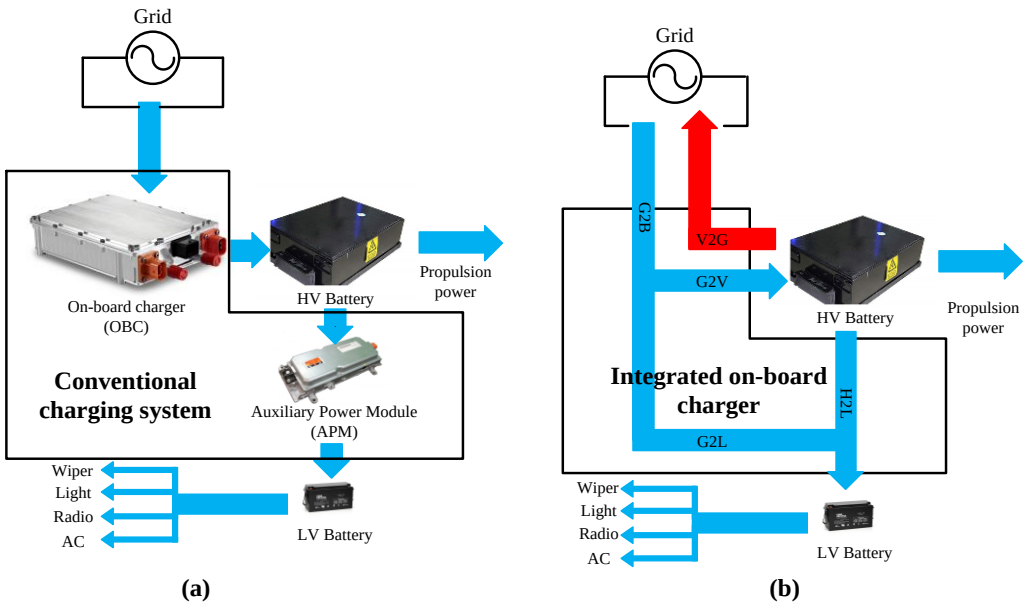


Fig. 5.1. (a) LV battery is independently charged through APM, and (b) Both HV and LV batteries can be charged from the grid (G2B mode) in the proposed integrated OBC

In order to achieve G2B mode operation, a new phase-shift based control scheme is proposed and introduced in this chapter. Moreover, this proposed control scheme can enhance the performance of the system in all the other operation modes, i.e. G2V mode, V2G mode and H2L mode.

Achieving the G2B mode is a challenging task, since the design and proper control of a power flow between different ports of a three-port DC/DC converter with wide range of gains is not trivial. The terminal voltage of the HV battery can range from 200V-450V and LV battery voltage can range from 12V – 14V depending on the state of charge (SOC) of both batteries, as shown in Fig. 5.2. Moreover, designing a converter with both good efficiency performance and wide enough gain range can be overwhelmingly difficult. The variable DC link control strategy proposed in Chapter 4 is a good option for this purpose. However, this strategy works well only with resonant-based topology as it assures the resonant circuit to operate at its resonant frequency with an optimum efficiency. Unfortunately, a resonant-based topology may not be the best candidate to implement the proposed control scheme, which will be explained in a later section.

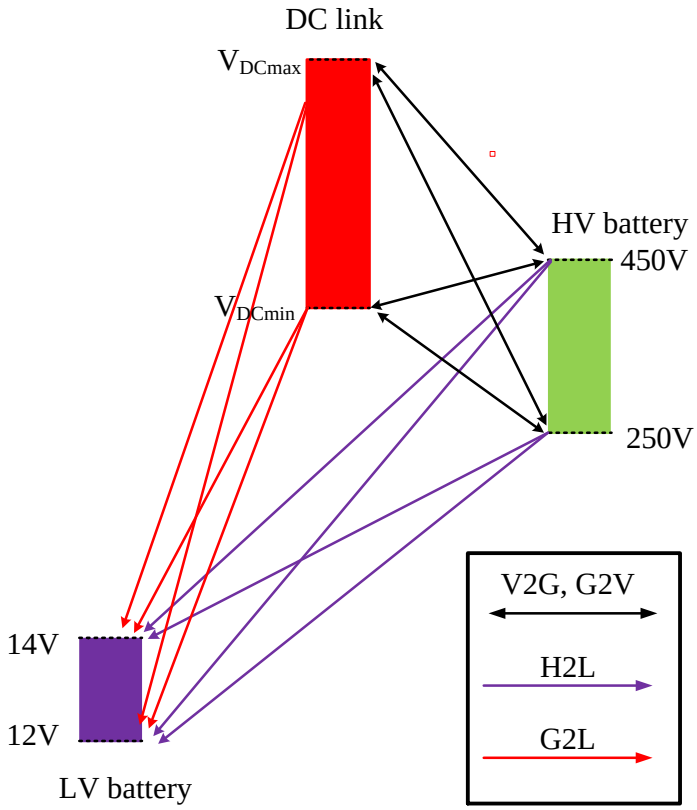


Fig. 5. 2. Gain requirement for the integrated system in G2B operation mode

5.2. Topology evaluation and selection for DC/DC stage

Assuming an interleaved totem pole PFC is used as the PFC Stage, a triple-active full bridge (TAB) converter and a full bridge CLLLC resonant converter can be considered as two viable options to integrate an OBC and an APM, as shown in Fig. 5.3.

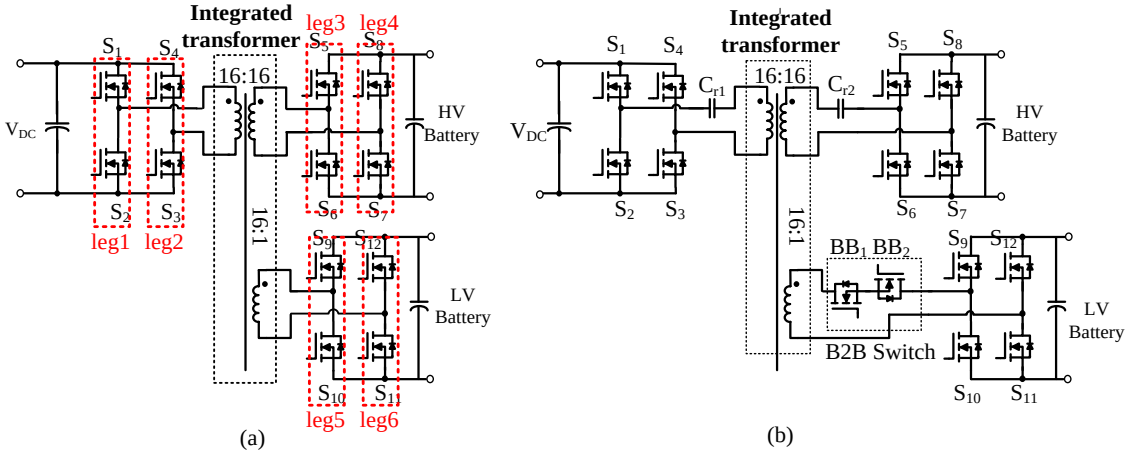


Fig. 5. 3. (a) Triple active full bridge converter with integrated transformer, (b) Full bridge CLLLC resonant converter with integrated transformer

On the one hand, the TAB converter provides enough control flexibility for the proposed control scheme. As shown in Fig. 5.3 (a), this topology consists of 6 switching legs. The upper and lower switch of each leg are complementarily switched with a 50% duty cycle. The required control variables φ_2. φ_3, δ_1, δ_2 and δ_3 can be generated by introducing time delays among these switching legs. t_{d0} is defined as the time delay between leg 1 and leg 2, t_{d1} is the time delay between leg 1 and leg 3, t_{d2} is the time delay between leg 1 and leg 4, t_{d3} is the time delay between leg 1 and leg 5, and t_{d4} is the time delay between leg 1 and leg 6; the relation between time delays and the desired control variables are given as Eq. (5.1)- Eq. (5.5).

$$t_{d0} = \frac{1}{\omega_s}(\pi - 2\delta_1) \tag{5.1}$$

$$t_{d1} = \frac{1}{\omega_s}(\varphi_2 + \delta_2 - \delta_1) \tag{5.2}$$

$$t_{d2} = \frac{1}{\omega_s}(\pi + \varphi_2 - \delta_2 - \delta_1) \tag{5.3}$$

$$t_{d3} = \frac{1}{\omega_s}(\varphi_3 + \delta_3 - \delta_1) \tag{5.4}$$

$$t_{d4} = \frac{1}{\omega_s}(\pi + \varphi_3 - \delta_3 - \delta_1) \tag{5.5}$$

On the other hand, a full bridge CLLLC resonant converter shown in Fig. 5.3 (b) can generate all required control variables in the same fashion. Moreover, switching frequency can be used as another degree of freedom is needed. Furthermore, the same number of switching devices is needed in this topology compared with TAB. However, even though the resonance can help achieve ZVS under the wider range of the load, it also creates higher voltage stress across the resonant capacitors (C_{r1} and C_{r2}). To sustain the voltage stress, multiple film capacitors are required to be placed in series which will result in a design with

larger size, higher cost, and lower reliability. To justify this claim, a simulation verification is conducted with the configuration summarized in Table. 5.1 and the simulation result is shown in Fig. 5.4.

Table 5. 1 Configurations of the simulation verification of full bridge CLLLC resonant converter.

Items	Values
Primary side resonant capacitance	$60nF$
Primary side resonant inductance	$95\mu H$
Secondary side resonant capacitance	$43nF$
Secondary side resonant inductance	$22\mu H$
Switching frequencies	$71kHz$
Load power	P_3=1.5kW (H2L mode)

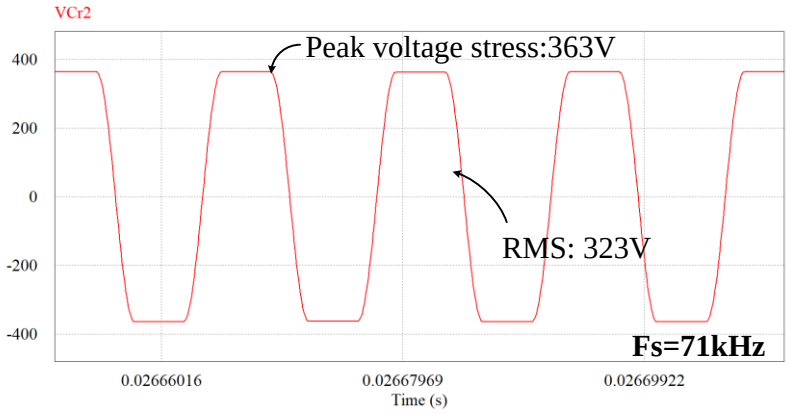


Fig. 5. 4. Simulation results: Voltage waveform across the secondary side resonant capacitor (C_{r2})

Given that the design of the proposed integrated charger should be highly compact and lightly weighted, bulky and expensive film capacitor banks are not desirable. Therefore, a TAB converter is a better option in this design. For readers' convenience, a summary of the comparisons is listed in Table 5.2.

Table 5. 2 Summary of the topology comparison: TAB and full bridge CLLLC

Items	TAB	Full bridge CLLLC
Switch count	12	12
ZVS range	Medium	**Wide**
Control flexibility (Degree of freedom)	5	6
Bulky resonant capacitor bank	**Not needed**	Needed

5.3. Phase-shift based control and charging strategy

In order to achieve G2B mode, the output port for HV and LV batteries should be independently regulated. However, unlike the scenario where one source supplies two resistive loads at the same time, a battery is a power source during the charging process. Therefore, this three-port system should be modeled as a network which consists of three independent power sources, line inductors which are the leakage inductances of the integrated transformer, and the power flows among three ports as shown in Fig. 5.5 (a) where P_1 and V_1 are the power and the voltage of the DC link port (port 1), P_2 and V_2 are the power and voltage of HV port (port 2), P_3 and V3 are the power and voltage of LV port (port3). Because the port voltages are the voltage across the switching nodes of the bridge (can be either full bridge or half bridge depending on the topology selection), the waveform of V_1, V_2 and V_3 are quasi squires. Moreover, these voltages are already referred to the primary side. L_1, L_2

and L_3 are the leakage inductances of the transformer. P_{12}, P_{23} and P_{13} are the power flow between port 1 and port 2, port 2 and port 3, port1 and port 3, respectively. In this equivalent model, the magnetizing inductance of the transformer is ignored due to its relatively large value and the negligible amount of current flowing through this branch.

This equivalent model is in the form of a start connection, which is easily understandable intuitively. However, this form of connection is not friendly for analyzing power flows as all power flows (P_{12}, P_{23} and P_{13}) are coupled with each other. Hence the analysis can be very complicated. Fortunately, by using start-delta transformation, shown as Eq. (5.6) - Eq. (5.8), a new equivalent model can be derived, as shown in Fig. 5.5 (b). Here, power flows can be decoupled from each other, hence much simpler expressions can be written as Eq. (5.9)- Eq. (5.11), where L_2' and L_3' are the leakage inductance referred to the primary side from secondary and tertiary winding

$$L_{12} = L_1 + L_2' + \frac{L_1 L_2'}{L_3'} \tag{5.6}$$

$$L_{23} = L_2' + L_3' + \frac{L_2' L_3'}{L_1} \tag{5.7}$$

$$L_{13} = L_1 + L_3 + \frac{L_1 L_3'}{L_2'} \tag{5.8}$$

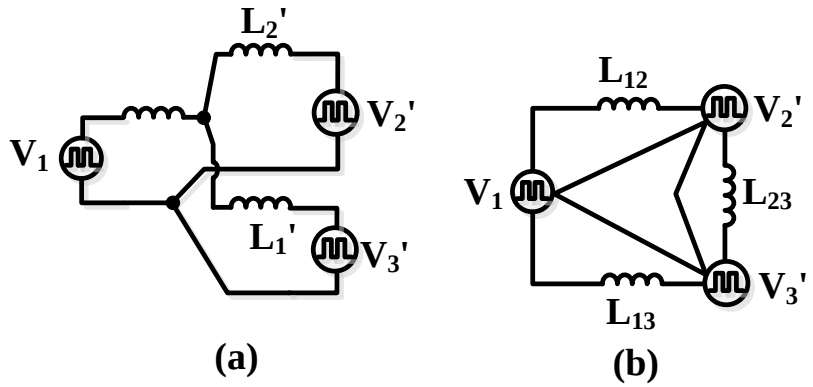


Fig. 5. 5. (a) Three-port equivalent circuit in start connection (b) Three port equivalent circuit in delta connection

$$P_{12} = \frac{8V_{DC}V'_{HV}sin\varphi_2 cos\delta_1 cos\delta_2}{\pi^2 \omega_s L_{12}} \quad (5.9)$$

$$P_{23} = \frac{8V'_{HV}V'_{LV}\sin(\varphi_3 - \varphi_2)cos\delta_2 cos\delta_3}{\pi^2 \omega_s L_{23}} \quad (5.10)$$

$$P_{13} = \frac{8V_{DC}V'_{LV}sin\varphi_3 cos\delta_1 cos\delta_3}{\pi^2 \omega_s L_{13}} \quad (5.11)$$

where $\omega_s = 2\pi f_s$, f_s is the switching frequency of the converter. V_{DC}, V'_{HV} and V'_{LV} are the amplitudes of V_1, V_2 and V_3, respectively.

As indicated by Eq. (5.9) – Eq. (5.11), the power flow can be controlled by the phase angle among V_1, V_2 and V_3 (φ_2 and φ_3) and their own duty cycles (δ_1, δ_2 and δ_3). The definition of these control variables is illustrated in Fig. 5.6.

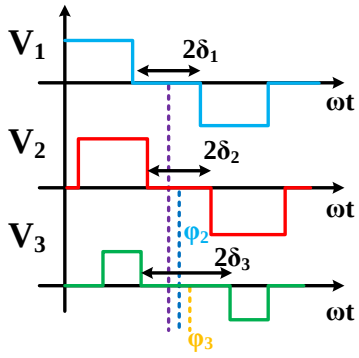


Fig. 5. 6. Definition of control variables in the proposed control scheme

By using superposition, the power delivered to HV and LV batteries can be expressed in terms of the power flow as Eq. (5.12) and Eq. (5.13).

$$P_2 = P_{12} - P_{23} \quad (5.12)$$

$$P_3 = P_{13} + P_{23} \quad (5.13)$$

Moreover, by combining (5.9) to (5.13) together, it is clear that all control variables can have an impact on P_2 and P_3. However, by taking a closer look, it can be noted that the phase shift φ_2 is related to both terms in the right hand side of (5.12) and φ_3 is related to both terms on the right hand side of (5.13). It is quite obvious that the regulation can be most effective if

these two variables are assigned to control P_2 and P_3, respectively. To further justify this option (using φ_2 and φ_3), we can take the case where assigning δ_1 to regulate P_2 as an example. By changing δ_1, P_2 can be adjusted because its component P_{12} is related to this control variable. However, in the scenario where P_{23} is more significant than P_{12}, this change can be negligible, thus the regulation over P_2 is practically lost. On the other hand, if φ_2 is assigned to regulate P_2, the regulation can be effective regardless of the significance of either component.

As φ_2 and φ_3 is assigned to regulate powers, there are three free variables left, i.e. δ_1,δ_2 and δ_3. They can be utilized to fulfill different control targets like reactive power reduction, conduction loss optimization, ZVS realization, etc. Therefore, this discussion can be split into several different cases that utilize these control variables differently.

5.3.1. Case I: Using δ_1 for ZVS realization, δ_2 and δ_3 for circulating power reduction

The circulating power can be split into two parts: circulating active power and circulating reactive power. They can be minimized separately by control variables δ_2 and δ_3.

To minimize the circulating active power, Eq. (5.14) needs to be true.

$$P_{12} + P_{13} + P_{23} = 0 \tag{5.14}$$

Combine with Eq. (5.12) and Eq. (5.13), it can be rearranged into Eq. (5.15)- Eq. (5.17).

$$P_{12} = -\frac{2P_2+P_3}{3} \tag{5.15}$$

$$P_{23} = \frac{P_2-P_3}{3} \tag{5.16}$$

$$P_{13} = -\frac{P_2+2P_3}{3} \tag{5.17}$$

Because P2 and P3 are already regulated, there exists redundancy in requirements Eq. (5.15) - Eq. (5.17). In fact, satisfying either one of them will be enough, thus only one control variable (δ_2) need to be assigned for it.

On the other hand, the reactive power can be expressed in Eq. (5.18)- Eq. (5.23).

$$Q_{12} = \frac{V_{DC}\cos(\delta_1)[V'_{HV}\cos(\delta_2)\cos(\varphi_2) - V_{DC}\cos(\delta_1)]}{2\pi f_s L_{12}} \tag{5.18}$$

$$Q_{21} = \frac{-V'_{HV}\cos(\delta_2)[V_{DC}\cos(\delta_1)\cos(\varphi_2) - V'_{HV}\cos(\delta_2)]}{2\pi f_s L_{12}} \tag{5.19}$$

$$Q_{23} = \frac{V'_{HV}\cos(\delta_2)[V'_{LV}\cos(\delta_3)\cos(\varphi_3) - V'_{HV}\cos(\delta_2)]}{2\pi f_s L_{23}} \tag{5.20}$$

$$Q_{32} = \frac{-V'_{LV}\cos(\delta_3)[V'_{HV}\cos(\delta_2)\cos(\varphi_3) - V'_{HV}\cos(\delta_3)]}{2\pi f_s L_{23}} \tag{5.21}$$

$$Q_{13} = \frac{V_{DC}\cos(\delta_1)[V'_{LV}\cos(\delta_3)\cos(\varphi_3) - V_{DC}\cos(\delta_1)]}{2\pi f_s L_{13}} \tag{5.22}$$

$$Q_{31} = \frac{-V'_{LV}\cos(\delta_3)[V_{DC}\cos(\delta_1)\cos(\varphi_3) - V'_{LV}\cos(\delta_3)]}{2\pi f_s L_{13}} \tag{5.23}$$

As can be seen from the above expressions, for an asymmetric two-port network, the sum of two reactive powers is not equal to zero ($Q_{12} + Q_{21} \neq 0$) if no interdependence constraint is being applied on δ_1 and δ_2. It essentially means that there will inevitably be a phase difference between any bridge voltage and switch current, which unavoidably increases the peak level of the device current. For example, in order to make the net reactive power injection to be zero, the following condition must hold true.

$$\frac{\cos(\delta_1)}{\cos(\delta_2)} = \frac{(M_{12}-1)\cos(\varphi_2) + \sqrt{4M_{12} + (M_{12}-1)^2\cos(\varphi_1)}}{2} \tag{5.24}$$

where M is the normalized gain of the power transfer, defined as $M_{12} = \frac{V'_{HV}}{V_{DC}}$. Therefore, for a given δ_2, the other phase angle δ_1 can be determined. Similarly, in the case of three-port network, satisfying Eq. (5.25) will result into another two quadratic relations between $\cos(\delta_1)$, $\cos(\delta_2)$ and $\cos(\delta_3)$ as shown in Eq. (5.26)- Eq. (5.27).

$$Q_{12} + Q_{21} = Q_{23} + Q_{32} = Q_{13} + Q_{31} = 0 \tag{5.25}$$

$$\frac{\cos(\delta_1)}{\cos(\delta_3)} = \frac{(M_{13}-1)\cos(\varphi_3) + \sqrt{4M_{13} + (M_{13}-1)^2\cos(\varphi_1)}}{2} \tag{5.26}$$

$$\frac{\cos(\delta_2)}{\cos(\delta_3)} = \frac{(M_{23}-1)\cos(\varphi_3) + \sqrt{4M_{23} + (M_{23}-1)^2\cos(\varphi_2)}}{2} \tag{5.27}$$

where $M_{13} = \frac{V_{DC}{}'}{V_{LV}}$, $M_{23} = \frac{V'_{HV}}{V'_{LV}}$. Because δ_2 is already assigned to minimize the circulating active power, there are not enough control variables to satisfy Eq. (5.24), Eq. (5.26) and Eq. (5.27) simultaneously. Fortunately, to minimize the circulating reactive power, the constraint does not need to be as tight as Eq. (5.25). In fact, satisfying Eq. (5.28) is good enough.

$$Q_{12} + Q_{13} + Q_{23} + Q_{21} + Q_{31} + Q_{32} = 0 \tag{5.28}$$

δ_2 needs to be considered as a known value at any given moment as it is assigned for minimizing the circulating active power. For any given δ_1, the sum of Q_{12} and Q_{21} will be a constant value as shown in Eq. (5.29).

$$Q_{12} + Q_{21} = K_{12} \tag{5.29}$$

Given that the rest of the reactive powers (Q_{23}, Q_{32}, Q_{13} and Q_{31}) can be affected by a common variable δ_3, their sum can be expressed as its function.

$$Q_{13} + Q_{31} + Q_{23} + Q_{32} = g(\delta_3) \tag{5.30}$$

To satisfy Eq. (5.28), only δ_3 needs to be assigned to make Eq. (5.29) and Eq. (5.30) equal as shown in Eq. (5.31).

$$g(\delta_3) = -K_{12} \tag{5.31}$$

Furthermore, an additional constraint will arise due to the attempt to ensure soft-switching at all the MOSFETs, which requires a minimum reactive power to be flowing from the input port. Assuming a minimum phase lag angle θ required between the fundamental of primary bridge voltage and primary winding current at a particular load power to ensure ZVS, the minimum reactive power from port-1 is as follows: $Q_1 = Q_{12} + Q_{13} > Q_{1,min} = P_1 \tan(\theta)$, where P_1 denotes the active power input from port 1. θ can be calculated from the condition that instantaneous inductive energy during switching has to be greater than the energy stored in MOSFET output capacitors. Therefore, there exist four equality constraints and one inequality constraint (for soft-switching), based on which four control variables can be explicitly determined, whereas the fifth variable will have a range of solution. The control

system block diagram with constraints on reactive power and soft-switching is shown in Fig. 5.7.

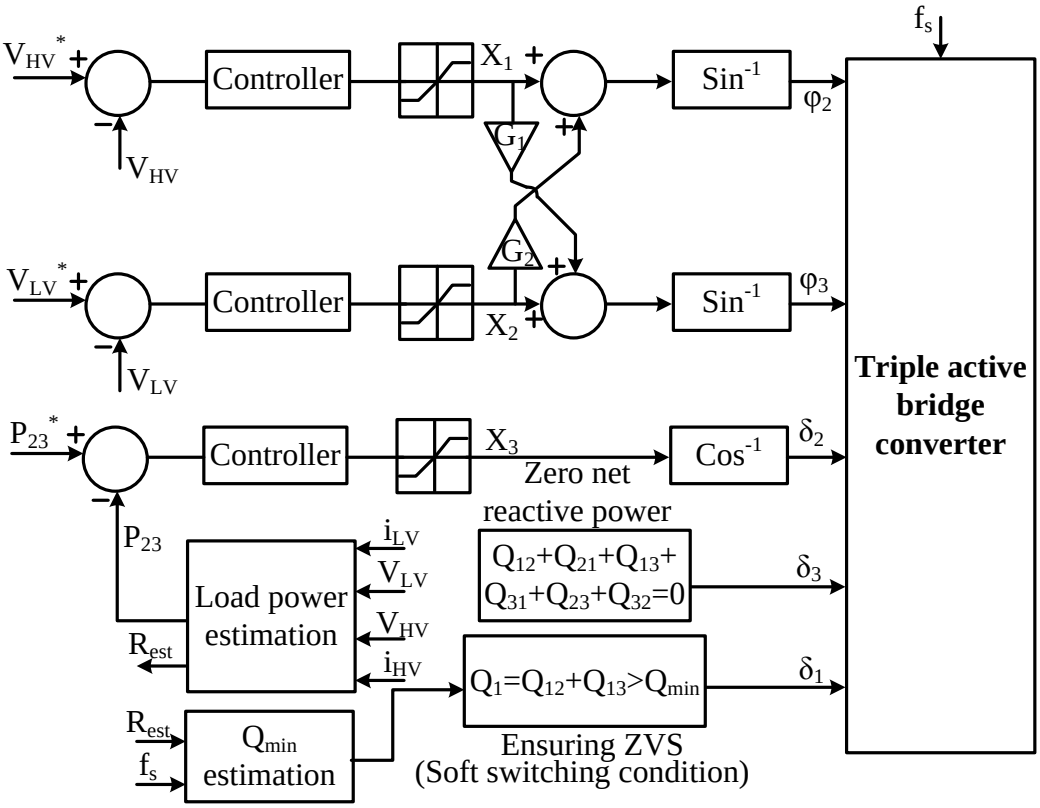


Fig. 5. 7. Proposed control scheme in Case I: using all δ_1, δ_2 and δ_3 for circulating power reduction and soft-switching.

This control scheme exhausts all the freedoms of control variables and is able to achieve both circulating current reduction and soft-switching. On the other hand, it is also mathematically complex and computational resource demanding. Therefore, not only can the implementation of the control scheme be very challenging in practice, but also the high-performance DSP may be required, which may not be desirable in low-cost oriented design.

5.3.2. Case II: Charging strategy without using δ control

The control strategy proposed in the previous section is universal to a three-port network with a large range of voltage and power levels. With the active and reactive circulating power

minimization and the ZVS realization, the efficiency can be optimized under full range of power and voltage. However, it demands highly-complicated mathematical modeling which leads to the requirement for an expensive controller to provide sufficient computation power.

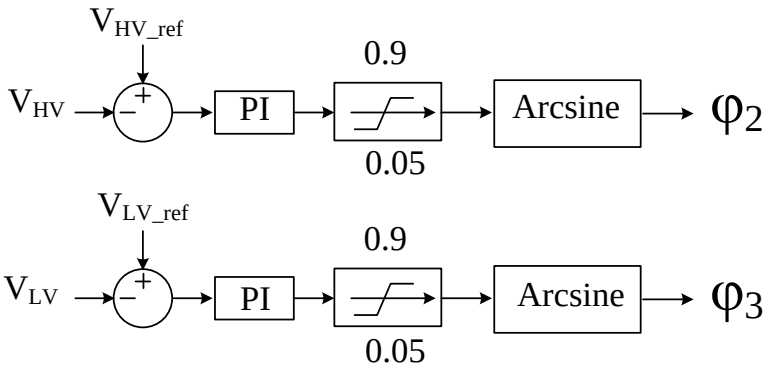


Fig. 5. 8. Proposed control diagram with φ_2 and φ_3

On the other hand, the control diagram shown in Fig. 5.8 includes only two control variables: φ_2 and φ_3, to regulate the HV and LV output powers. Therefore, the implementation of this control structure is significantly simplified and cheaper, as compared with case I. However, this control diagram cannot regulate the circulating power within the network. This leads to a high current ripple for magnetics, output capacitors and MOSFETs under certain circumstances, giving the device a risk of failure.

To address this issue, a comprehensive simulation study has been conducted to measure the current stress in the circuit under different scenarios. It is observed that the worst current stress happens under the following scenarios: (i) either the HV or LV battery demands a low charging current (light load); (ii) both HV and LV battery demand a low charging current. Table 5.3 gives some examples of extremely high current stress on the LV side transformer winding in aforementioned scenarios. In the table, I_1, I_2 and I_3 denote the RMS current on the primary side, HV side and LV side transformer windings.

Table 5. 3 Simulation verification: high current stress under light load conditions

V_{DC}	V_{HV}	V_{LV}	P_2	P_3	I_1	I_2	I_3
400V	400V	12V	3600W	12W	22A	38.8A	**643A**
400V	400V	12V	4000W	12W	22A	31.2A	**516A**
400V	450V	12V	45W	3000W	17A	33.1A	**606A**
400V	450V	12V	45W	3000W	20.8A	19.6A	**462A**

Assuming $I_3 < 500A$ is the standard for acceptable current stress, the G2B operational region can be marked in the (P_2, P_3) plane based on simulation results as shown in Fig. 5.9.

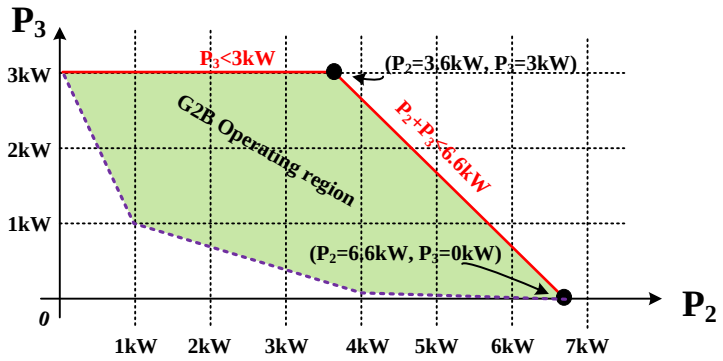


Fig. 5. 9. G2B simulation summary: region of acceptable LV side current stress ($I_3 < 500A$)

According to the commonly used constant current – constant voltage (CC-CV) charging profile, the battery is charged with maximum allowable charging current during CC mode, reaching maximum power when battery voltage increases to a certain level. This charging power will start to drop during CV mode and become minimum when the battery gets fully charged. Therefore, the light load condition normally happens when the battery gets close to 100% SOC. Based on this fact, a charging strategy can be formulated to enable the proposed integrated OBC to operate without facing excessive current stress. The proposed charging strategy includes 4 different scenarios, as summarized in Table 5.4. In this table, SOCL and

SOCH denote SOC of LV battery and SOC of HV battery, respectively. SOCT1 and SOCT2 are two arbitrary thresholds for LV battery, SOCT3 denotes an arbitrary threshold for the HV battery. They can be set by the designer depending on the desired G2B operating region of the integrated OBC. For a better illustration, the proposed strategy is plotted into (SOCH, SOCL) plane as shown in Fig. 5.10.

Table 5. 4 Summary of proposed charging strategy

Scenarios		Charger action
Within G2B operating Region		G2B
Outside of G2B region	SOCL<SOCT1, SOCH>SOCT3	H2L or G2L
	SOCL<SOCT2, SOCH<SOCT3	H2L or G2L
	Rest of the conditions	G2V

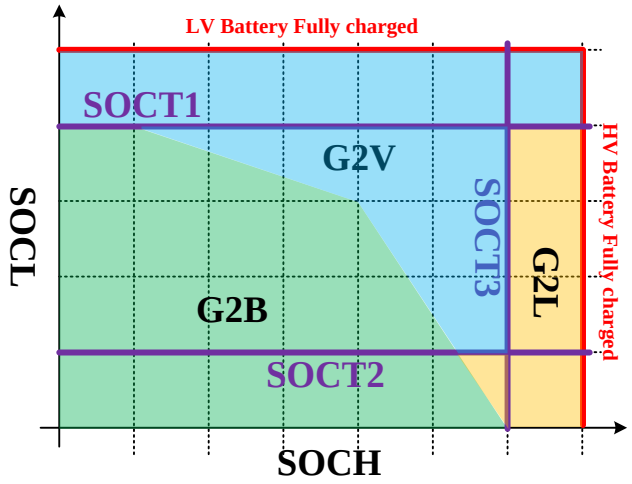


Fig. 5. 10. Proposed charging strategy at a glance.

5.3.3. Case III: Using δ_1, δ_2 and δ_3 for circulating power reduction

The control scheme proposed in case I demands complicated analytical modeling and high computation power to implement, which can be practically difficult to realize. On the other hand, the control strategy in case II provides a practical solution with a basic, simple control with only φ_2 and φ_3 as control variables. However, the limitation of this control strategy is a relatively small operational region for G2B due to the excessive transformer/MOSFET current stress. In this section, an alternative control scheme to reduce the circulating power with less complexity, as compared with case I, is proposed. Therefore, the G2B operation region can be effectively extended from case II with relatively easy implementation.

This control is based on a zero average inductor voltage for a switching period. To illustrate this concept with simplicity, a dual active bridge (DAB) converter with input voltage V_{DC} and output voltage V_{HV} is used as an example. A well-known conclusion of the DAB converter is that the optimum operating condition of the converter is when the gain is exactly equal to the turns ratio of the transformer, i.e. $\frac{N_p}{N_s} = \frac{V_{DC}}{V_{HV}}$, where N_p and N_s are the number of turns for primary and secondary transformer winding. The more the gain of the converter deviates from it, the more a circulating current stress and a narrow ZVS range the converter will possess. The essence of this statement is that the voltage across the inductor in the network should be zero during commutation mode to minimize the circulating current stress. When the gain of the converter deviates from the transformer turns ratio, there has to be a non-zero average inductor voltage during commutation mode as shown in Fig. 5.11.

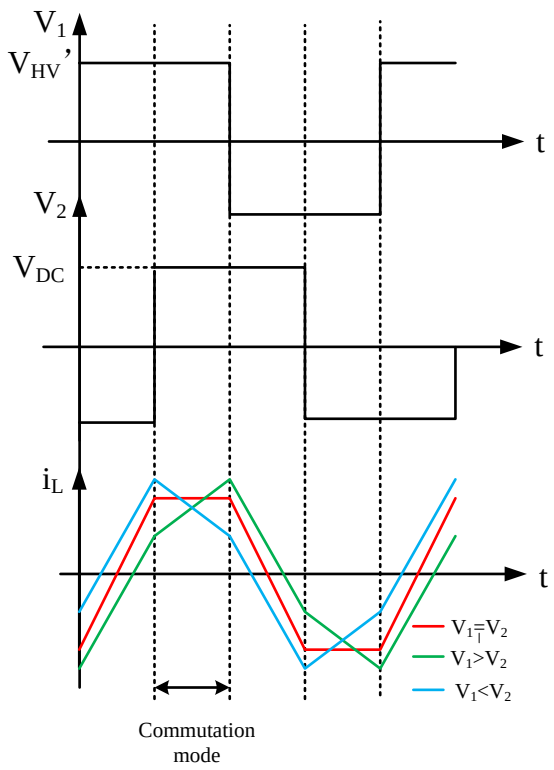


Fig. 5. 11. Example waveform of typical dual active bridge (DAB) converter.

This principle can be also applied to the TAB converter, regardless of the more complicated current shape as duty cycles of all bridges voltage δ_{1-3} are involved. During the commutation modes of the TAB converter, there are two scenarios: (i) the voltage at both sides of the inductor are zero. (ii) the voltage at both side of the inductor are non-zero with the same polarity, (iii) voltage at only one side of the inductor is zero. The first scenario automatically generates zero voltage across the inductor. In the other two scenarios, inequalities among V_{DC}, V'_{HV} and V'_{LV} inevitably produce a high peak of the circulating current with the mechanism described in Fig. 5.12. However, this can be addressed by properly using δ_{1-3} as formulated in Eq. (5.32).

$$V_{1.F} = V_{DC}cos\delta_1 = V_{2.F} = V'_{HV}cos\delta_2 = V_{3.F} = V'_{LV} \tag{5.32}$$

In the above expression, $V_{1.F}$, $V_{2.F}$ and $V_{3.F}$ are the fundamental components of the bridge voltages (referred to the primary side) V_1, V_2 and V_3. $V'_{HV} = \frac{N_p V_{HV}}{N_s}$ and $V'_{LV} = \frac{N_p V_{LV}}{N_t}$ are the

amplitude of the bridge voltages referred to the primary side. N_p, N_s and N_t are the number of turns of primary, secondary and tertiary side windings.

Eq. (5.32) ensures that the average inductor voltage over the commutation mode of the converter is zero, i.e. $V_1 = V_2 = V_3$. Fig. 5.12 gives a graphic illustration of peak current reduction by having zero average inductor voltage during commutation mode. For simplicity, only V_{DC} and V_{HV} are depicted in the figure.

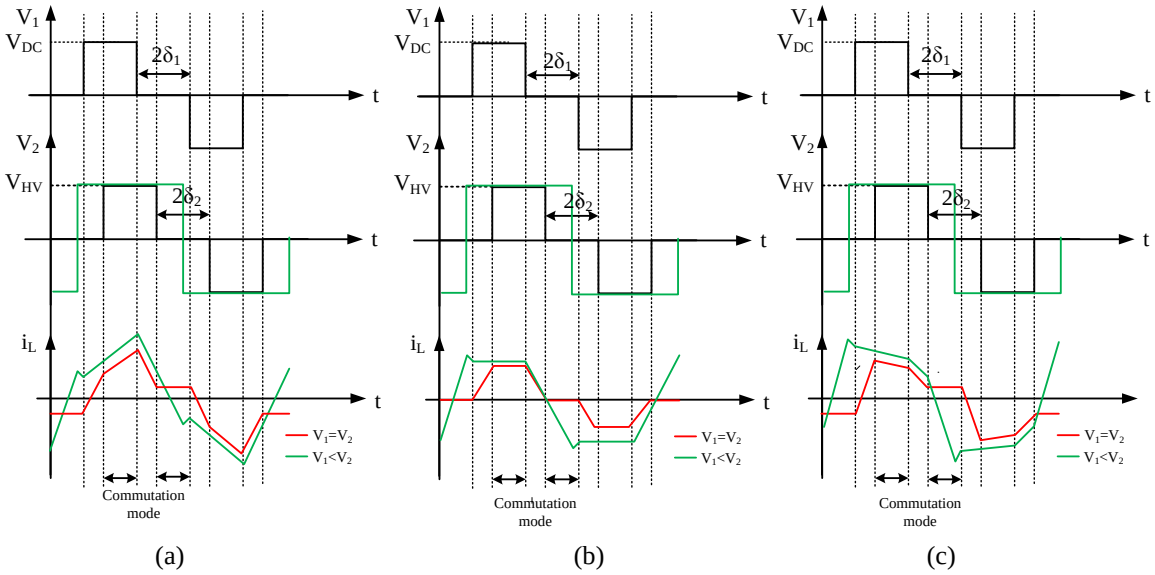


Fig. 5.12. Peak inductor current reduction by having $V_1 = V_2$ with duty cycle control: (a).$V_{DC} > V_{HV}$, (b). $V_{DC} = V_{HV}$(c). $V_{DC} < V_{HV}$

Moreover, this approach will extend the gain range of the converter. With only φ_2 and φ_3 control, the regulation of one output channel may be lost with a significant difference between V_2 and V_3 and a relatively large load mismatch (one light load and one heavy load). In practice, oscillation may be observed in this scenario due to the dynamic cross-coupling between HV and LV power flows. For example, if the control target is $V_{HV} = 200V$ with heavy load, $V_{LV} = 12V$ with light load, HV side voltage will lose regulation and create an

oscillation on both HV and LV powers. This can be solved by implementing $\delta_3 = \arccos(\frac{200N_t}{12*N_s})$. Then both output powers will be regulated as expected.

5.4. Loss estimation with real-time dynamic current waveform estimation

Through the evaluation process, a combination of interleaved totem pole PFC rectifier and TAB converter is selected. Before diving into the hardware design and implementation, it is critical to have a detailed loss analysis. A good loss calculation is critical to component selection and thermal management. Therefore, a novel loss modeling based on linear piece-wise current waveform estimation for both the PFC stage and the DC/DC stage is proposed in this section in order to achieve a better loss estimation. Before introducing the proposed loss estimation model, the relation between loss and component selection, loss and thermal management should be introduced to justify the importance of a good loss estimation. On one hand, a good loss estimation can prevent a catastrophic thermal failure for power devices and ensure the reliability of the design. On the other hand, it can also prevent an overdesign for thermal solutions, thus decreasing the cost, weight, and volume of the resulted solution. There are cases when a design is optimized in operational scheme and control method, but fails to deliver the expected specifications due to overdesign on the mechanical end.

5.4.1. Loss, component selection and thermal management

The most commonly used model for thermal analysis is the first-order thermal model. As shown in Fig.5.13, the loss P_L is the total loss generated from the power devices. This loss will create a temperature difference called temperature rise (T_r) along the dissipation path, which can be calculated as Eq. (5.33). $R_{th} = R_{th.jc} + R_{th.tim} + R_{th.hsa}$ is the total thermal resistance, which is the sum of thermal resistance from junction to case ($R_{th.jc}$), thermal resistance of thermal interface material ($R_{th.tim}$) and thermal resistance from heatsink to ambient environment ($R_{th.hsa}$).

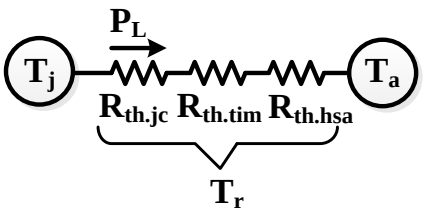


Fig. 5.13. First order thermal modeling: loss, thermal resistance and temperature rise

$$T_r = P_L * R_{th} \tag{5.33}$$

This model is a handy tool to roughly estimate the temperature at the power device junction (T_j), which is critical for a reasonable power device selection. For example, a component selection needs to be made assuming it is known that 40A current will flow through a MOSFET with 400V voltage stress. The decision which is not based on thermal analysis will simply leave a 50% margin for current rating and select the device with a current rating not less than 60A, e.g. IPW60R031CFD7XKSA1 from Infineon Technology. The key specifications of this device along with some commonly used thermal data are summarized in Table 5.5.

Table 5. 5 Key specifications for IPW60R031CFD7XKSA1 and commonly used thermal data

Item	Value
Turn-on resistance (@100℃)	$60m\Omega$
Turn-on time	27ns
Turn-off time	6ns
$R_{th.jc}$	$0.45℃/W$

$R_{th.tim}$	3℃/W (typical number for thermal interface material)[87]
$R_{th.hsa}$	0.04℃/W (typical number for cold plate product)
Ambient temperature (T_a)	70℃
Junction temperature limit	150℃

However, based on the specifications provided by this table, the conduction loss and switching loss of this device can be calculated by Eq. (5.34) and Eq. (5.35). The total loss can be calculated as 102.2W. Then a first order thermal model can be applied to estimate the junction temperature of the MOSFET. According to the information provided in Table 5.5, the calculation result is shockingly 427℃. Therefore, having multiple MOSFETs in parallel is necessary. After several iterations, the component selection based on thermal analysis can be made as shown in Table 5.6.

$$P_{cod} = I_d^2 * R_{ds.on} \tag{5.34}$$

$$P_{sw} = 0.5 V_{ds} I_d (t_r + t_f) f_s \tag{5.35}$$

where I_d is the current flowing through the MOSFET, V_{ds} is drain-to-source voltage, t_r and t_f are the turn-on time and turn-off time of the MOSFET.

Table 5. 6 Component selection based on maximum allowable junction temperature

Item	Thermal analysis based	None thermal analysis based
Component selection	IPW60R031CFD7XKSA1	IPW60R031CFD7XKSA1
# of device in parallel	4	1
Loss per device	12.2W	102.2W
Estimated T_j	112.7℃	427℃

Potential result	**Normal operation**	**Thermal failure**
Total cost	46USD	11.5USD

From the table above, it is clear that wrong decisions can easily be made in component selection if they are not backed up with good loss analyses. Thermal management is a much more complex subject and good component selection is part of it. It is an interactive and iterative process between electrical engineers and mechanical engineers. After component selection and schematic creation, electrical engineers need to plan out the component placement. During this phase, electrical engineers and mechanical engineers need to be on the same page. In general, electrical engineers would like to group components as compactly as possible to achieve higher power density, less parasitic, and conduction loss. On the other hand, mechanical engineers want components to be separated from with each other as much as possible for better heat dissipation. Therefore, for each iteration, the proposed component placement needs to be examined by 3D FEA thermal simulation and the final solution should be agreed by both sides. A good loss estimation is the foundation of an accurate thermal simulation.

From the discussion above, it is crystal clear that an accurate loss analysis is crucial for the success of the hardware design. Therefore, a good loss modeling for both the PFC stage and the DC/DC stage is beneficial.

5.4.2. Real-time dynamic loss modeling for CCM PFC rectifier

A typical loss breakdown for a PFC converter includes inductor core loss, inductor copper loss, switching loss, conduction loss of MOSFETs, and equivalent series resistance (ESR) loss on DC link capacitors. Other loss sources such as PCB traces and parasitic resonance among components and traces are generally negligible if proper design practices are

implemented. To estimate these losses, the high frequency current ripple of input current must be estimated first. However, either assuming an ideally fixed inductance value or fixed amplitude of high frequency current ripple will not be accurate as these dismiss three factors: (1) non-linearity of the inductor as a function of inductor current level and excitation frequency; (2) the high frequency component in the input current; (3) the time-variant nature of the duty cycle. Therefore, the impact of those factors on loss estimation should be investigated and clarified.

a. Non-ideality of inductor and high frequency component of input current as loss factors

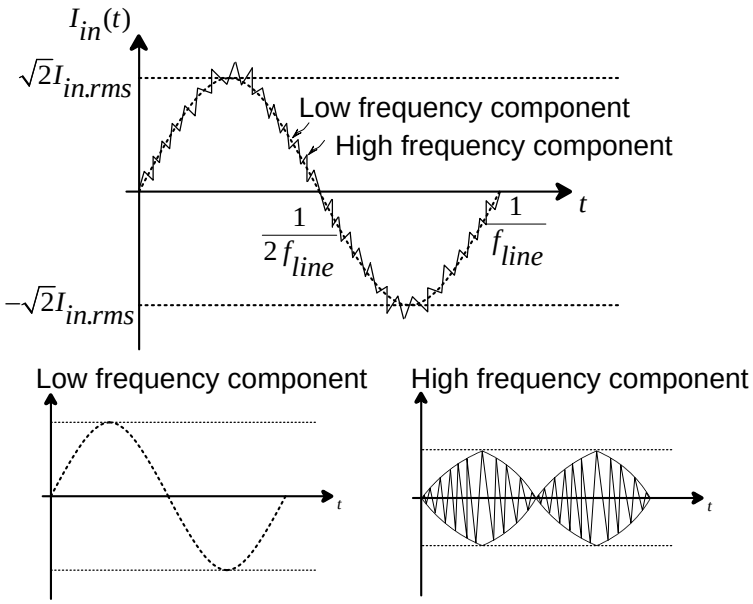


Fig. 5.14. High frequency and low frequency components of input current of CCM PFC

As shown in Fig. 5.14, the input current of a CCM PFC circuits includes two different components: low frequency sinusoidal and high frequency triangular components. As shown in Fig. 5.14, the high frequency component in the current has a time-variant amplitude. This phenomenon is caused mainly for two reasons: the time-variant duty ratio and input line

voltage, as well as non-linearity of the inductor. At any instant, the high frequency inductor current ripple can be calculated by Eq. (5.36).

$$\Delta i_L(t) = \frac{D(t)V_{in}(t)}{Lfs} \tag{5.36}$$

Assuming the input voltage to be an ideal sinusoidal waveform, the duty cycle (*D(t)*) can be expressed in terms of input voltage as:

$$V_{in}(t) = \sqrt{2}V_{in.rms}\sin(2\pi f_{line}t) \tag{5.37}$$

$$D(t) = 1 - \frac{V_{in}(t)}{V_{DC}} = 1 - \frac{\sqrt{2}V_{in.rms}}{V_{DC}}\sin(2\pi f_{line}t) \tag{5.38}$$

Plugging Eq. (5.37) and Eq. (5.38) into Eq. (5.36), the amplitude of high frequency current ripple can be obtained as follows.

$$\Delta i_L(t) = \frac{\sqrt{2}V_{in.rms}\sin(2\pi f_{line}t) - \frac{V_{in.rms}^2}{V_{DC}}(1-\cos(4\pi f_{line}t))}{Lf_s} \tag{5.39}$$

As indicated by Eq. (5.39), the amplitude of the high frequency current ripple includes fundamental and secondary harmonics. Moreover, the permeability of the magnetic material will change according to the current level flowing through the inductor windings. This directly results in a time-variant inductance value over an input line cycle of PFC. Considering this fact, Eq. (5.39) can be further modified into Eq. (5.40).

$$\Delta i_L(t) = \frac{\sqrt{2}V_{in.rms}\sin(2\pi f_{line}t) - \frac{V_{in.rms}^2}{V_{DC}}(1-\cos(4\pi f_{line}t))}{L(t)f_s} \tag{5.40}$$

Therefore, as indicated by Eq. (5.40), estimating the current ripple by simply assuming an ideally fixed inductance or fixed amplitude of current ripple is not accurate. This inaccuracy in current ripple amplitude will further impact the entire loss estimation process and thus results in unreliable prediction of conversion efficiency.

b. Core loss, inductance change and high frequency current ripple

A complete core loss includes hysteresis loss and eddy current loss. In this design, a ferrite core is used for PFC inductor design. Due to the high electrical resistivity of ferrite, the

eddy current can be negligible. Therefore, core loss is only defined by hysteresis loss, which is a function of magnetic field H and switching frequency f. The magnetic field H of a magnetic core in a power converter is calculated using the inductance value at the RMS current level: $H = \frac{NI}{l_e}$, where l_e is the mean flux path length, N is the inductor's number of turns and I is the instantaneous value of the inductor current. Due to the aforementioned dynamic change in inductance with inductor current, the ripple is no longer only the function of duty cycle D over different switching period, which changes the value of H_{max} and H_{min} (maximum and minimum H in a switching cycle) at different switching instants in a single line cycle. Therefore, as a function of H, maximum and minimum flux density in a switching cycle B_{max} *and* B_{min} are also time-varying variables. This time-varying flux density leads to the deviation between the real core loss and the estimation results from existing practical estimation methods[88] - [93], where inductance value is assumed to be constant and the current ripple is represented by its maximum value for a conservative estimation.

Fortunately, fitting curves provided by manufactures is a good approach to depict the non-linearity between magnetic field and flux density as shown in Eq. (5.41). Then the core loss can be calculated using hysteresis core loss equation as shown in Eq. (5.42).

$$B = f(H) \tag{5.41}$$

$$PL = h(\Delta \mathrm{B}, \mathrm{f}) = A(\Delta \mathrm{B})^b (f)^c \tag{5.42}$$

where, PL is the core loss density, ΔB is the AC flux swing, which is given by difference between maximum and minimum flux density levels i.e. (B_{max}-B_{min}) and f is the frequency of the excitation.

Furthermore, since inductance is time-dependent due to the non-linearity between the magnetic field and magnetic flux, the inductance will deviate depending on different values of inductor current. This phenomenon can be accurately depicted by Eq. (5.43)

$$L(t) = \frac{4\pi\mu(t)A_e}{l_e} N^2 = \frac{4\pi A_e N^2}{l_e} g[H(t)] \tag{5.43}$$

where N denotes the number of turns of the inductor. With the aid of Eq. (5.40) – Eq. (5.43), the core loss can be estimated as a sum of low frequency loss and high frequency loss, as shown in Eq. (5.44). The first term of the expression in Eq. (5.44) represents the low frequency loss and the high frequency loss is calculated by taking a time average over the energy loss in a line cycle, represented by the second term. The high frequency energy loss is calculated by integrating the power loss density PL given in Eq. (5.42) over a line cycle i.e. $PL=h((B_{max}-B_{min}), f)$. In Eq. (5.42), the maximum and minimum flux density in a switching cycle i.e. B_{max} and B_{min} are obtained by plugging the maximum and minimum magnetic field intensity within each switching cycle (H_{max} and H_{min}) into Eq. (5.41), respectively. H_{max} and H_{min} are determined by the maximum and minimum current levels in a switching cycle.

$$P_{Core} = A_e l_e \left\{ h\left[f\left(\frac{N\sqrt{2}I_{in.rms}}{l_e} \right), \mathrm{f_{line}} \right] + 2f_{line} \int_{t=0}^{\frac{1}{2f_{line}}} h\left[f\left(H(t) + \frac{D(t)V_{in}(t)l_e}{8\pi A_e f_s N^2 g[h(t)]} \right) - f\left(H(t) - \frac{D(t)V_{in}(t)l_e}{8\pi A_e f_s N^2 g[h(t)]} \right), \mathrm{f_s} \right] dt \right\} \quad (5.44)$$

c. Conduction loss and time dependent duty cycle

In an n-phase boost-derived PFC (e.g. $n = 2$ if PFC is a two-leg interleaved converter), the conduction loss can be evaluated by Eq. (5.45), where $R_{dson.total}$, $R_{wire.total}$, and $V_{f.total}$ are the total channel resistance of MOSFETs, wire resistance of the inductor, and total voltage drop of diodes, respectively.

As Eq. (5.45) indicates, if RMS value of the input current and a constant duty cycle value D_{eff} associated with this RMS input current are used, the time-variant nature of the duty cycle $D(t)$, and input current $I_{in}(t)$ will be completely ignored. This will result in a non-negligible deviation of the calculation from the real situation.

$$P_{Conduction(t)=n[I_{in}(t)^2(D(t)R_{dson.total}+R_{wire.total})+I_{in}(t)(1-D(t))V_{f.total}]} \quad (5.45)$$

d. Switching loss and ESR loss

The inaccuracy of switching loss estimation also originates from the high frequency component of input current. In existing practices[88] - [93], the switching loss can be calculated by Eq. (5.46).

$$P_{Sw} = I_{in.rms} V_{DC} \left(\frac{t_r + t_f}{2}\right) f_s + V_g Q_g f_s + \frac{1}{2} C_{oss} V_{DC}^2 f_s \quad (5.46)$$

where, t_r and t_f are the rise and fall times of selected MOSFET, Q_g is the total gate charge, V_g is the gate voltage and C_{oss} is the output capacitance. However, the RMS current can only represent the low frequency component of the input current, which neglects the high frequency components, introducing significant inaccuracy in measurement as shown in Fig. 5.15.

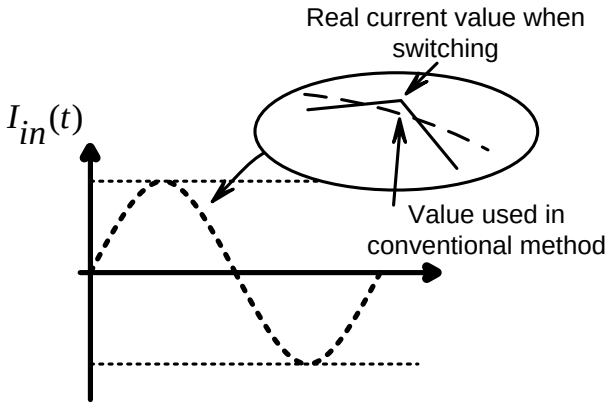


Fig. 5.15. Impact of high frequency ripple on the accuracy of switching loss estimation

Furthermore, completely neglecting the high frequency ripple in the current also affects the estimation of loss due to the ESR of DC link capacitor. The ESR loss can be estimated by calculating the RMS capacitor current within the line cycle. Due to the charge conservation, the charge introduced by the capacitor current should be equal to the charge variance indicated by the DC link voltage ripple:

$$P_{Cap} = (2C\Delta V_{DC} f_{line})^2 ESR \quad (5.47)$$

And the DC link voltage ripple can be calculated by Eq. (5.48):

$$\Delta V_o = \frac{P_o}{2\pi f_{line} V_{DC}} \tag{5.48}$$

As indicated by Eq. (5.47) and Eq. (5.48), this method completely neglects the impact of the high frequency current ripple. More accurate switching and ESR loss expressions are presented in the next section.

e. Proposed real-time dynamic estimation strategy

To estimate the power losses more accurately, the high frequency component of input current should not be neglected and the variation of the inductance over a wide range of inductor currents should also be taken into consideration. Therefore, I propose an innovative method based on input current waveform estimation. By estimating the current real-time value for every switching cycle, this method considers the dynamic of inductance and the high frequency current ripple, thus providing a reasonably higher accuracy.

(a) Prediction of input current and estimation of core loss

Core loss of a PFC inductor includes two parts: a high frequency ripple and a low frequency sinusoidal portion. For the low frequency sinusoidal part, the estimation is the same as existing practices [88] - [93]; however, in the case of the high-frequency switching components of input currents, instead of using a constant current ripple amplitude, the real-time magnetic flux and power loss density considering the impact from inductance variance should be calculated first. To do this, the current waveform containing the information from the high frequency component should be determined by estimating the inductor current variation for each switching cycle, as shown in Eq. (5.49).

$$\Delta I_{in}(t) = \frac{V_{in}(t)D(t)}{L(t)f_S} \tag{5.49}$$

The updated inductor current is obtained by adding the previous cycle value with the change, as shown in the flowchart in Fig. 5.16. Also, the current variation at any two

consecutive cycles is limited to the worst-case ripple (ξ). If not, the duty cycle is manipulated by adding a small perturbation to its previous value, which is equivalent to simulating the feedback loop. This process is repeated iteratively until the check condition satisfies. It is worth mentioning that this iterative loop to track the input current is particularly valid for a CCM operated converter, which is kept as the main focus of this work. Then, using Eq. (5.44), real-time core loss can be calculated for each cycle, and be integrated over the entire line voltage cycle. One of the fundamental variables in core loss calculation is the inductance value, considering instantaneous variation of inductance due to permeability variation over the current level. An empirical relation, established in [90], between permeability and current level is given by Eq. (5.50).

$$\mu = (1 + aI_{in} + bI_{in}^2 + cI_{in}^3 + dI_{in}^4) \tag{5.50}$$

where, the phase current 'I_{in}' is related to the magnetizing field intensity as: $I_{in}=l_eH/N$.

In the existing practical methods [88] - [93], μ is assumed constant at μ_{rms} as expressed in Eq. (5.51), which is the permeability calculated using Eq. (5.50) under the condition of the RMS input current, i.e. $I_{in} = \frac{I}{\sqrt{2}}$, assuming $I_{in}(t) = I\,sin(2\pi f_{line}t)$. Furthermore, the core loss is proportional to the change in magnetic flux density, which is again proportional to the μ_{rms}.

$$\mu_{rms} = 1 + \frac{aI}{\sqrt{2}} + \frac{bI^2}{2} + \frac{cI^3}{2\sqrt{2}} + \frac{dI^4}{4} \tag{5.51}$$

On the other hand, in the proposed method, the magnetic core loss is a function of time-averaged permeability $<\mu>$. Assuming the phase current $I_{in}(t) = Isin(2\pi f_{line}t) + \Delta\mathrm{i(t)}$, which is the superposition of the line-frequency sinusoidal and the high frequency triangular, the time-averaged permeability can be written into the form of Eq. (5.52).

$$<\mu>= \left(1 + a<I_{in}> + b<I_{in}^2> + c<I_{in}^3> + d<I_{in}^4>\right) \tag{5.52}$$

where $<I_{in}>=<Isin(2\pi f_{line}t) + \Delta\mathrm{i(t)}>$,

$<I_{in}^2>=<I^2\sin^2(2\pi f_{line}t) + \Delta\mathrm{i(t)}^2 + 2I\Delta\mathrm{i(t)}sin(2\pi f_{line}t)>$,

$< I_{in}^3 >=<$

$I^3 \sin^3(2\pi f_{line}t) + \Delta i(t)^3 + 3I^2\Delta i(t)sin(2\pi f_{line}t) + 3I\Delta i(t)^2 sin(2\pi f_{line}t) >,$

$< I_{in}^4 >=< I^4 \sin^4(2\pi f_{line}t) + \Delta i(t)^4 + 4I^3\Delta i(t)sin(2\pi f_{line}t) + 4I\Delta i(t)^3 sin(2\pi f_{line}t) + 6I^2\Delta i(t)^2 sin(2\pi f_{line}t) >$

Note that over any line cycle, both $Isin(2\pi f_{line}t)$ and $\Delta i(t)$ are odd functions, then the averages of different exponents of the phase current can be simplified as shown in Eq. (5.53).

Plugging (5.53) into (5.52) and equating it to (5.51), the sufficient and necessary condition for $\mu_{rms} =< \mu >$ is obtained as (5.54).

$$\begin{cases} <I_{in}>=0 \\ <I_{in}^2>=\frac{I^2}{2}+<\Delta i(t)^2>+2I<\Delta i(t)\sin(2\pi f_{line}t)> \\ <I_{in}^3>=0 \\ <I_{in}^4>=\frac{3I^4}{8}+<\Delta i(t)^4>+4<I^3\Delta i(t)\sin(2\pi f_{line}t)+I\Delta i(t)^3\sin(2\pi f_{line}t)>+6I^2<\Delta i(t)^2\sin(2\pi f_{line}t)> \end{cases} \quad (5.53)$$

$$b < \Delta i(t)^2 > +2bI < \Delta i(t)sin(2\pi f_{line}t) > +d < \Delta i(t)^4 > +4d < I^3\Delta i(t)sin(2\pi f_{line}t) + I\Delta i(t)^3 sin(2\pi f_{line}t) > +6dI^2 < \Delta i(t)^2 sin(2\pi f_{line}t) >= \frac{aI}{\sqrt{2}} + \frac{cI^3}{2\sqrt{2}} - \frac{dI^4}{8} \quad (5.54)$$

The coefficients a, b, c and d are the inputs from the core material properties, which in general, can be any value. Therefore, Eq. (5.54) cannot hold true at any given conditions, which means the deviation exists between the estimations of core loss by assuming μ_{rms} and

$< \mu >$, respectively. Moreover, this difference is also verified through experiments and calculation examples in the later sections of the paper.

(b) Capacitor ESR loss

In a PFC converter, the loss on DC-link capacitor is normally considerable. ESR of capacitor can be calculated by the dissipation factor (DF) obtained from datasheet:

$$ESR = \frac{DF}{2\pi f_{test} C} \tag{5.55}$$

where, f_{test} is the testing frequency.

In an n-phase boost-derived PFC (e.g. $n = 2$ if PFC is a two-leg interleaved converter), the average capacitor current over one switching cycle can be calculated by:

$$i_c(t) = nI_{in}(t) - I_o \tag{5.56}$$

where, $I_{in}(t)$ represent the input current per phase.

With the predicted real-time current waveform, capacitor current containing high frequency information can be accurately obtained and, hence, the change of output voltage for each switching cycle can be estimated as well. Then, ESR loss can be determined by:

$$P_{Cap} = [4Cf_{line}(V_{DC.max} - V_{DC.min})]^2 ESR \tag{5.57}$$

(c) Conduction loss and switching loss

With the predicted real-time current waveform, accurate estimation of conduction loss and switching loss is straightforward using Eq. (5.45). Based on all the modeling work, the flow chart of dynamic loss estimation strategy can be summarized as shown in Fig. 5.15. In the figure, ΔD is the change step of the duty cycle to simulate the function of the feed-back control loop in a CCM-PFC. ΔT is the time step of the calculation, which is set to be the PWM switching period. Moreover, there is a trade-off between calculation accuracy and computation time by tuning the value of ξ in Fig. 5.16. An unreasonably small ξ can result in

an undesirably long computation time but ξ must be relatively small to ensure a good accuracy.

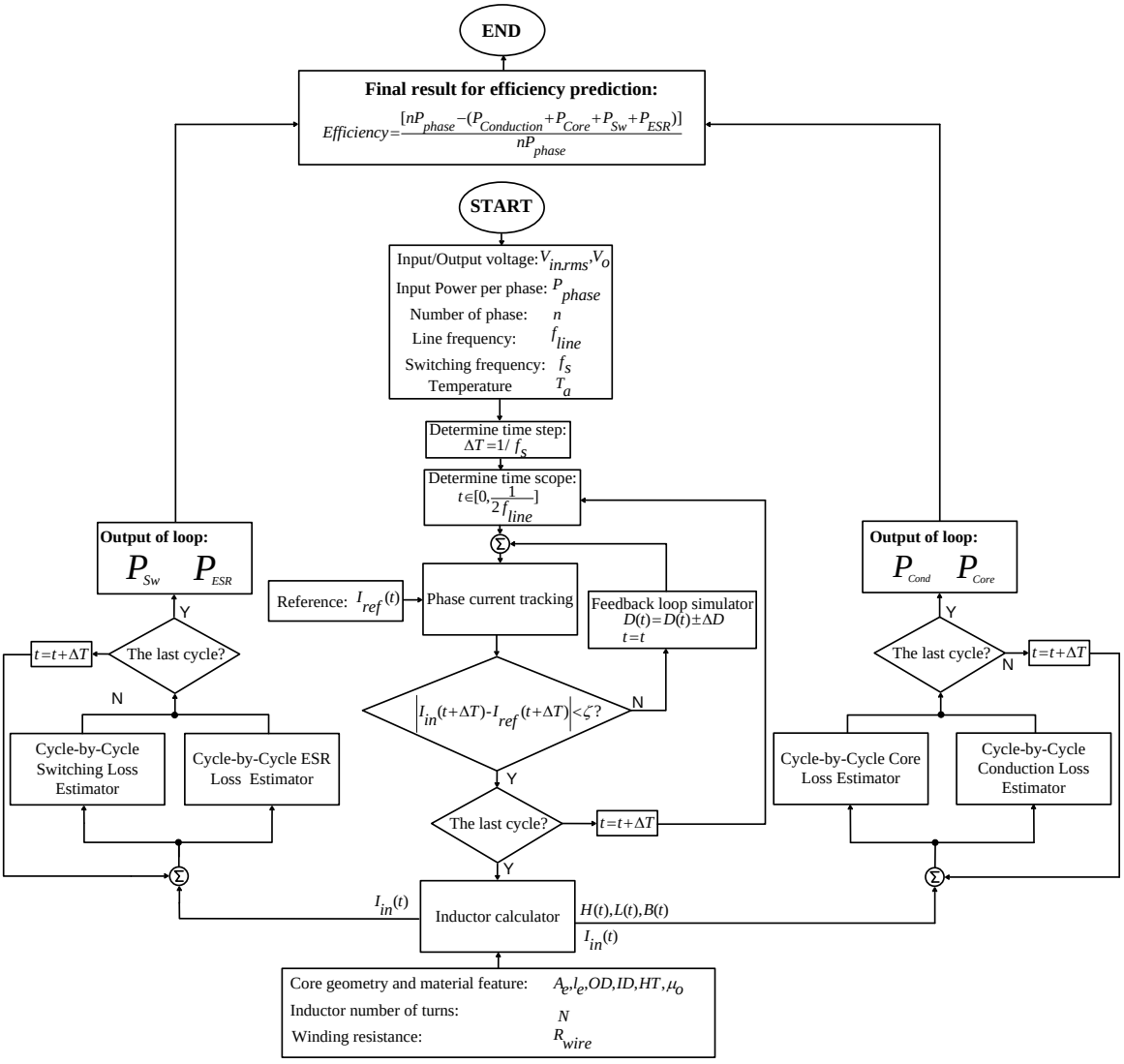


Fig. 5.16. Flow chart of proposed real-time dynamic estimation strategy

f. Estimation results

To illustrate the effectiveness of the proposed estimation model, a calculation example is presented in this section. Specifications used for this calculation are summarized in Table 5.7.

Table 5.7 specification of PFC stages

Item	Value
Topology	Interleaved totem pole PFC
Rated maximum output power	6.6kW
Switching frequency	$70kHz$
Input voltage	85-265V_{ac}
Output voltage	400V_{DC}
Nominal input voltage	220V_{ac}

First, the PFC inductor needs to be designed based on inductor current ripple requirement. Due to the interleaving structure, the inductor ripple will not show in the input current, and a relatively large inductor current ripple is allowed. For this design, the maximum allowable inductor current ripple is selected as 50%. Given this criterion, minimum required inductance at both the nominal line condition and the low line condition can be calculated by Eq. (5.58) and Eq. (5.59). Based on the calculation results, the PFC inductor can be designed as summarized in Table 5.8, and the inductance variance over input power is illustrated as Fig. 5.17.

$$L_{@\text{nominal}} > \frac{0.5V_{in.min}^2}{\%ripple P_{in.phase} f_s} \tag{5.58}$$

$$L_{@low\ line} > \frac{V_{in.min}^2}{\%ripple P_{in.phase} f_s}\left(1 - \frac{\sqrt{2}V_{in.min}}{V_{DC}}\right) \tag{5.59}$$

Table 5.8 Design summary for PFC inductor

Item	Value
Core selection	High flux C058439A2
Wire selection	Magnets wire AWG 14
Number of turns	50
No load inductance	$351\mu H$
Full load inductance	$217\ \mu H$

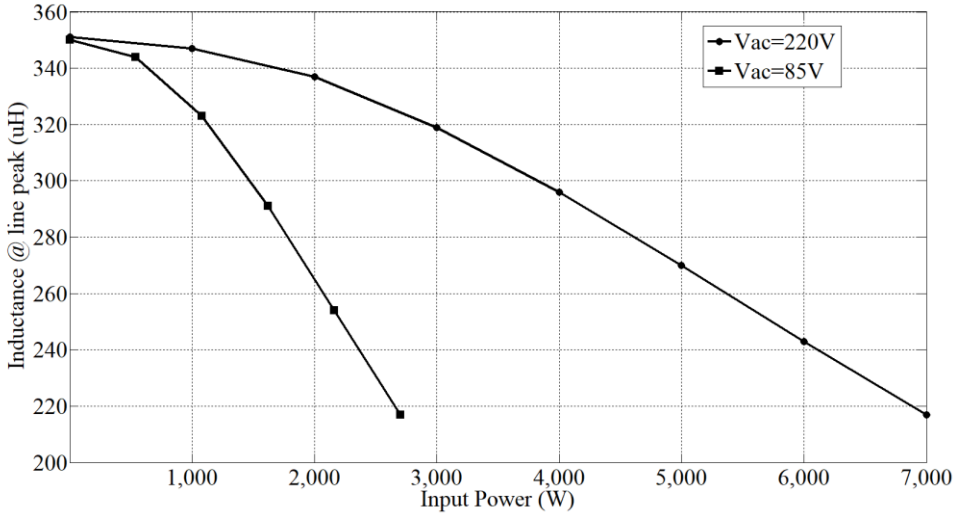


Fig. 5.17. Inductance variation vs. input power under nominal and low line conditions

Then, ripple current of the DC link capacitors can be calculated through the proposed estimation strategy. Therefore, the structure of the DC link capacitors can be determined based on both voltage and current stress per capacitor as shown in Table 5.9.

Table 5.9 Design summary for DC-link capacitors

Item	Value
Component selection	LLS2V102MELC
Ripple current rating	3.6A
Voltage rating	350V
Voltage stress of the DC link	650V (@ H2L mode)
Capacitor bank structure	2 in series, 4 in parallel
Ripple current per capacitor	2.93A
Total capacitance	$2mF$

Moreover, through the proposed estimation method, efficiency under different line conditions and load range can be accurately estimated with different combination of MOSFET selection. Based on the results, the most cost-effective solution can be obtained. In this comparison, four different options are studied as shown in Table 5.10, while the key specs of involved MOSFETs are listed in Table 5.11.

Table 5.10 Candidates of MOSFET selection for PFC stage

Option#	Fast MOSFET	Slow MOSFET
I	IXFH80N65X2	IXFH80N65X2 (2 in parallel)

II	IPW65R048CFDAFKSA1	IPW65R048CFDAFKSA1 (2 in parallel)
III	IPW65R019C7FKSA1	IPW65R019C7FKSA1 (2 in parallel)
IV	IPW65R048CFDAFKSA1	IPW65R019C7FKSA1 (2 in parallel)

Table 5.11 Key specification of candidate MOSFETs

Part#	IXFH80N65X2	IPW65R048CFDAFKSA1	IPW65R019C7FKSA1
$R_{dson.T_j=125℃}$	0.106Ω	0.092 Ω	0.035 Ω
Voltage rating	650V	650V	700V
$I_{d.T_j=125℃}$	40A	34A	58A
Rise time	24ns	10 ns	27 ns
Fall time	11 ns	4 ns	5 ns
Manufacture	IXYS	Infineon	Infineon
RR status	200ns/1.7μC	240ns/1.8 μC	760ns/20 μC
Cost	6USD	8.29USD	12.49USD

Applying these component specifications to the proposed estimation model, efficiencies over various line and load conditions can be plotted as Fig. 5.18. Even though option III shows the best efficiency, it is not the best option due to two constrains: (i) high cost, (ii) high reverse recovery charge which may result in high zero-crossing current distortion and then degrade the THD. On the other hand, option I, II and IV are all viable options from a performance perspective. However, option I is chosen to be the solution because option I has the lowest cost compared with the others.

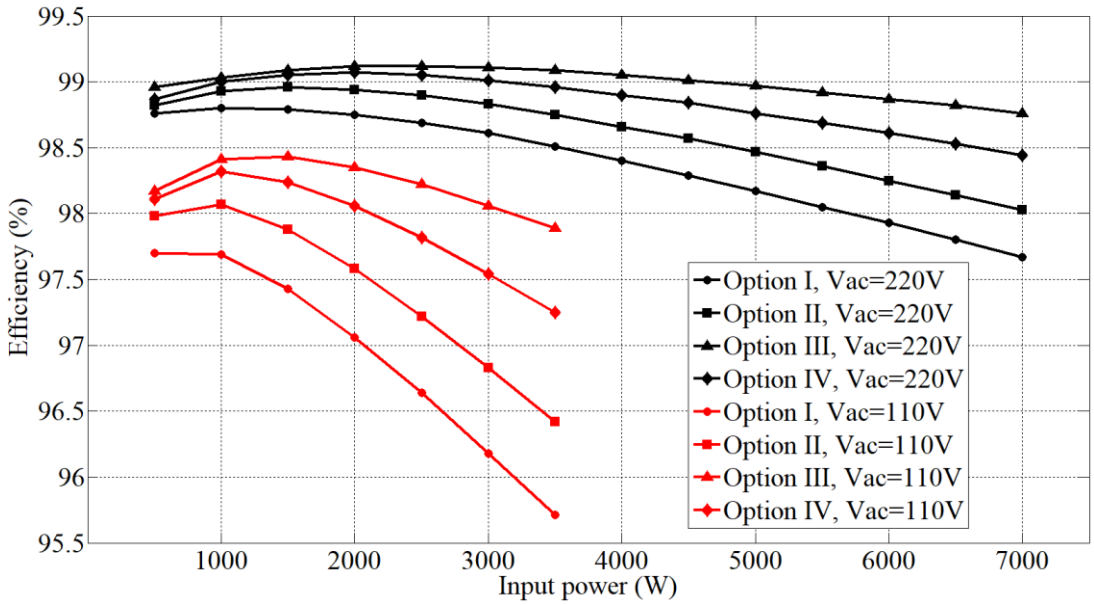


Fig. 5.18. Efficiency estimation for PFC stage under various line and load condition with different MOSFET options

5.4.3. Real-time dynamic loss modeling for TAB converter

After modeling losses for the PFC stage, it is time to analyze the losses from the DC/DC stage. There are two main challenges in order to get an accurate estimation for power device losses: (i) obtaining the shape of transformer currents and (ii) determining the ZVS condition for each MOSFET. This is mainly because, in the TAB converter, three leakage inductances of the transformer are excited by three different voltage levels at each terminal with different phase angles, which is much more complicated than DAB scenarios that can be simplified as one inductor getting excited by two quasi-square voltage sources. Fortunately, by star-delta transformation introduced in section 5.2, the TAB converter can be decoupled and separately modeled as three DAB converters as shown in Fig. 5.19.

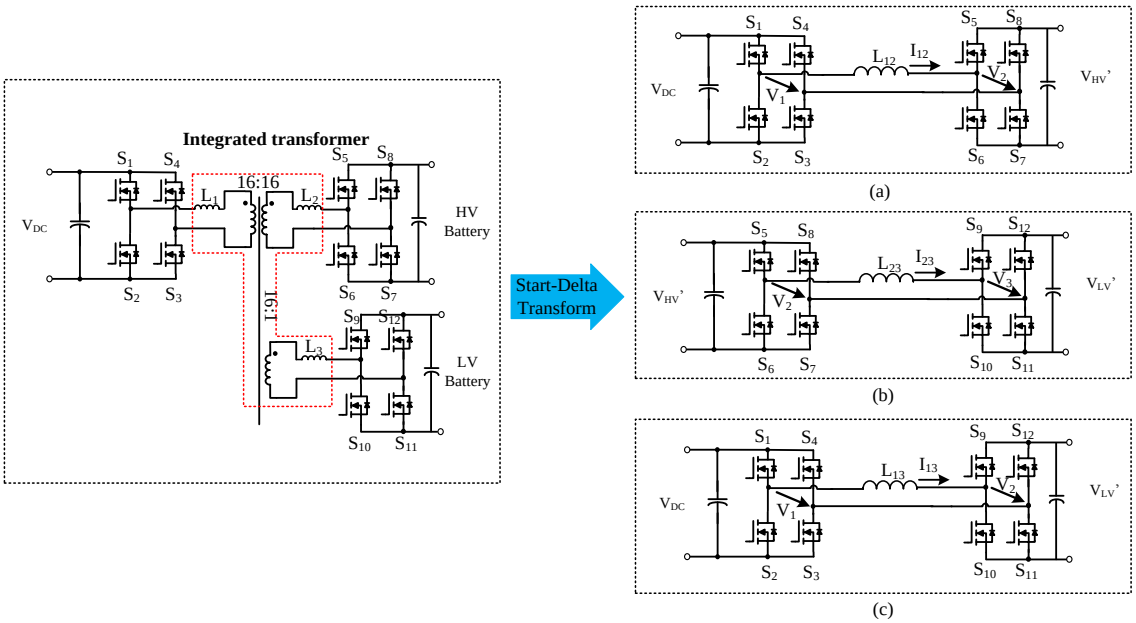


Fig. 5.19. Decoupling TAB converter into three DAB converters by star-delta transformation

For simplicity, taking an equivalent circuit (a) from Fig. 5.19 as an example, the general voltage pattern for two bridges can be summarized in Fig. 5.20, where V_1 is the bridge voltage of the bridge consisting of S_1-S_4, V_2 is the bridge voltage of the bridge consisting of S_5-S_8., φ_2, δ_1, and δ_2 are the control variables described in Fig. 5.4. With different phase angle, the voltage applied across the inductor has different patterns and forms the inductor current waveform accordingly. Therefore, to obtain the current waveform in different scenarios, it is critical to find out the current patterns with different φ_2, δ_1, and δ_2. Although traverse through all the possible combinations of the phase angles seems to be a massive challenge, fortunately there are some tricks that can be used to simplify the process. First, no matter how the phase angles change, the switching timings of the bridge voltage share the same form of expression but different chronological sequence. As shown in Fig. 5.20, they are: 0, δ_1, $\varphi_2 - \delta_2$, $\varphi_2 + \delta_2$, $\pi - \delta_1$, $\varphi_2 - \delta_2 + \pi$ and π. Then, because of the symmetry of the circuit, only half switching cycle ($0 < \omega_s t < \pi$) and one power flow direction ($0 <$

$\varphi_2 < \frac{\pi}{2}$) need to be studied. Given these two considerations, all possible current patterns can be divided into two main categories: A. $\varphi_2 - \delta_2 > 0$ and B. $\varphi_2 - \delta_2 \leq 0$.

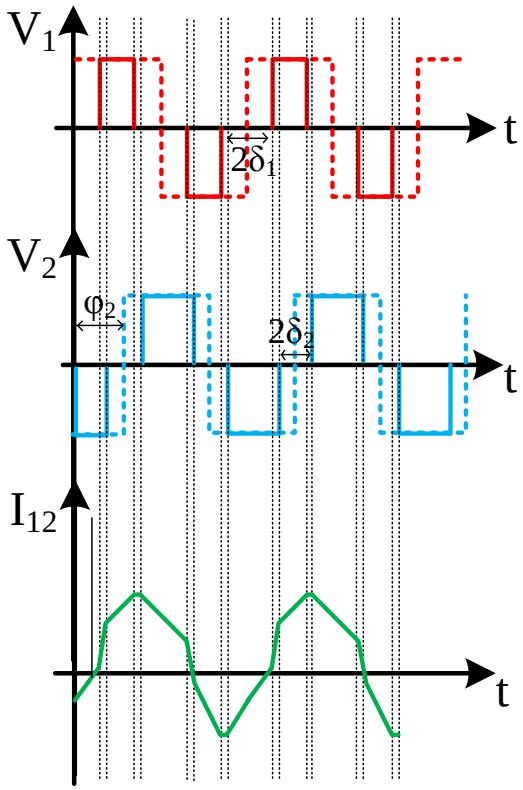


Fig. 5.20. General waveform: inductor voltage and current

A. $\varphi_2 - \delta_2 > 0$

Under this condition, combined with the fact that all control variables are within the range of $[0, \frac{\pi}{2}]$, the following inequalities can be derived as Eq. (5.60) – Eq. (5.62). Applying all constrains, there are five different voltage patterns possible as shown in Table 5.12. The waveforms of inductor current are summarized as Fig. 5.21.

$$\delta_1 < \pi - \delta_1 \tag{5.60}$$

$$\varphi_2 - \delta_2 < \varphi_2 + \delta_2 \tag{5.61}$$

$$\varphi_2 - \delta_2 < \pi - \delta_1 \tag{5.62}$$

Table 5.12 Summary of switching timing sequence under condition A

CASE#	t_0	t_1	t_2	t_3	t_4	t_5
A.1	0	δ_1	$\varphi_2 - \delta_2$	$\varphi_2 + \delta_2$	$\pi - \delta_1$	π
A.2	0	δ_1	$\varphi_2 - \delta_2$	$\pi - \delta_1$	$\varphi_2 + \delta_2$	π
A.3	0	$\varphi_2 - \delta_2$	$\varphi_2 + \frac{\delta_2}{2}$	δ_1	$\pi - \delta_1$	π
A.4	0	$\varphi_2 - \delta_2$	δ_1	$\varphi_2 + \delta_2$	$\pi - \delta_1$	π
A.5	0	$\varphi_2 - \delta_2$	δ_1	$\pi - \delta_1$	$\varphi_2 + \delta_2$	π

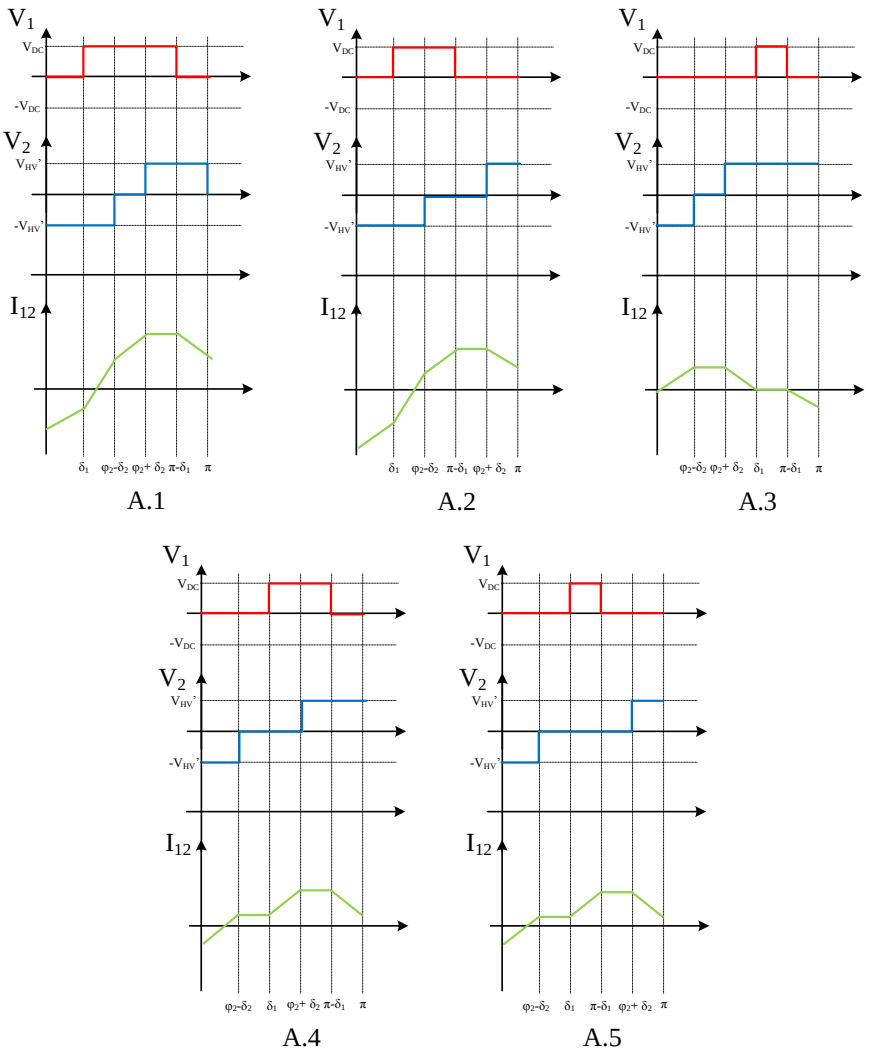


Fig. 5.21. Summary of inductor current waveform under condition A

B. $\varphi_2 - \delta_2 \leq 0$

Similarly, the following inequalities can be derived considering all constrains, shown as Eq. (5.63) – Eq. (5.65).

$$\delta_1 < \pi - \delta_1 \tag{5.63}$$

$$\varphi_2 + \delta_2 < \varphi_2 - \delta_2 + \pi \tag{5.64}$$

$$\varphi_2 - \delta_2 + \pi > \delta_1 \tag{5.65}$$

Then, all the possible current patterns are summarized as Table 5.13. The waveforms of inductor current are summarized as Fig. 5.22.

Table 5.13 Summary of switching timing sequence under condition B

CASE#	t_0	t_1	t_2	t_3	t_4	t_5
B.1	0	$\varphi_2+\delta_2$	δ_1	$\varphi_2-\delta_2+\pi$	$\pi-\delta_1$	π
B.2	0	δ_1	$\varphi_2+\delta_2$	$\varphi_2-\delta_2+\pi$	$\pi-\delta_1$	π
B.3	0	$\varphi_2+\delta_2$	δ_1	$\pi-\delta_1$	$\varphi_2-\delta_2+\pi$	π
B.4	0	δ_1	$\varphi_2+\delta_2$	$\pi-\delta_1$	$\varphi_2-\delta_2+\pi$	π
B.5	0	δ_1	$\pi-\delta_1$	$\varphi_2+\delta_2$	$\varphi_2-\delta_2+\pi$	π

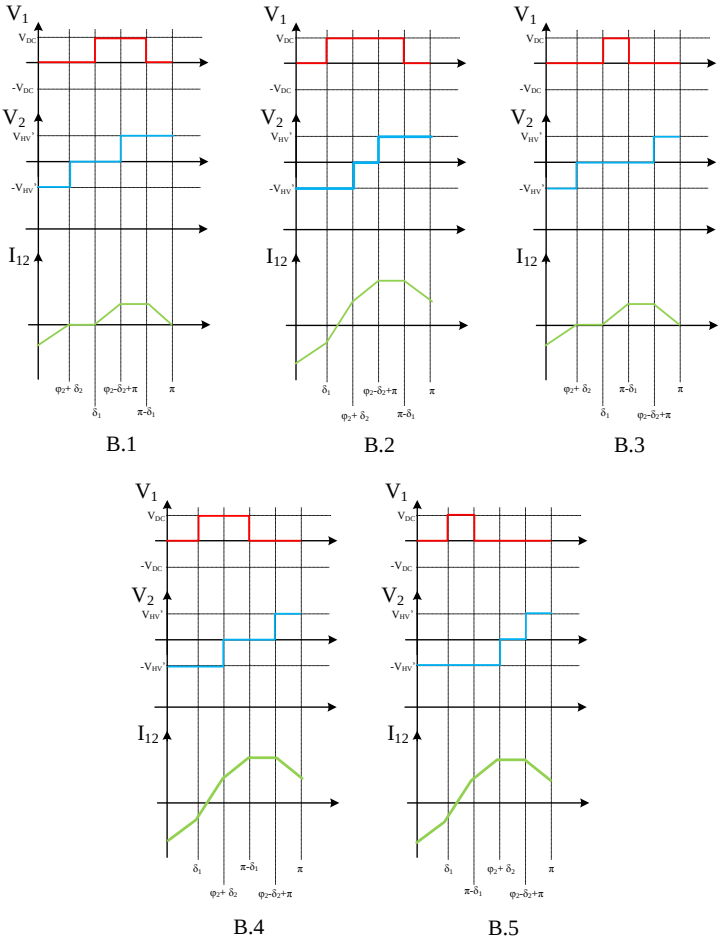


Fig. 5.22. Summary of inductor current waveform under condition B

As the analyses suggest, there are in total ten different inductor current shape patterns in this simplified DAB scenario. It is worth noticing that the current shape obtained in the above analysis is the current waveform in the decoupled DAB equivalent circuit, i.e. I_{12}. To obtain the actual current waveforms in the TAB converter, superposition can be applied, shown as Eq. (5.66) – Eq. (5.68).

$$I_1 = I_{12} + I_{13} \tag{5.66}$$

$$I_2 = I_{23} - I_{12} \tag{5.67}$$

$$I_3 = -I_{23} - I_{13} \tag{5.68}$$

After the TAB inductor currents (also the transformer winding current) are obtained, it is fairly easy to determine if the ZVS condition for each MOSFET is achieved based on he criteria summarized in Table 5.14. Moreover, it is also pretty straightforward to calculate the RMS current, and to get current and voltage instantaneous value when MOSFET switches. Therefore, the total loss for each MOSFET can be calculated accordingly and results are summarized in Table 5.15.

Table 5.14 Criterion of MOSFET soft-switching operation.

Switching instance	MOSFET actions	ZVS conditions	
δ_1	S_4 off, S_3 on	$I_{12} > 0$	Non-ZVS
		$I_{12} < 0$	ZVS
$\pi - \delta_1$	S_1 off, S_2 on	$I_{12} > 0$	ZVS
		$I_{12} < 0$	Non-ZVS
$\varphi_2 - \delta_2$	S_7 off, S_8 on	$I_{12} > 0$	ZVS
		$I_{12} < 0$	Non-ZVS
$\varphi_2 + \delta_2$	S_5 off, S_6 on	$I_{12} > 0$	ZVS

		$I_{12} < 0$	Non-ZVS
$\varphi_2 - \delta_2 + \pi$	S_8 off, S_7 on	$I_{12} > 0$	Non-ZVS
		$I_{12} < 0$	ZVS

Table 5.15 Design summary for TAB MOSFET selection

Item	Primary/Secondary side	Tertiary side
Component selection	IPW65R048CFDAFKSA1	IPT007N06NATMA1
# of devices in parallel	3	4
Loss per device	12W	7.2W
Ambient temperature	70℃	70℃
Estimated junction temperature	**109**℃	**93.04**℃
Junction temperature limit	150℃	175℃
Total cost	158.88USD	43.04USD

5.5. Planar integrated transformer

The concept of the integrated transformer, where the resonant inductor is realized by leakage inductors of the transformer, was introduced in Chapter 2. This concept can be also applied in TAB converter as shown in Fig. 5.23, the transformer leakage inductor is used for the L_1, L_2 and L_3.

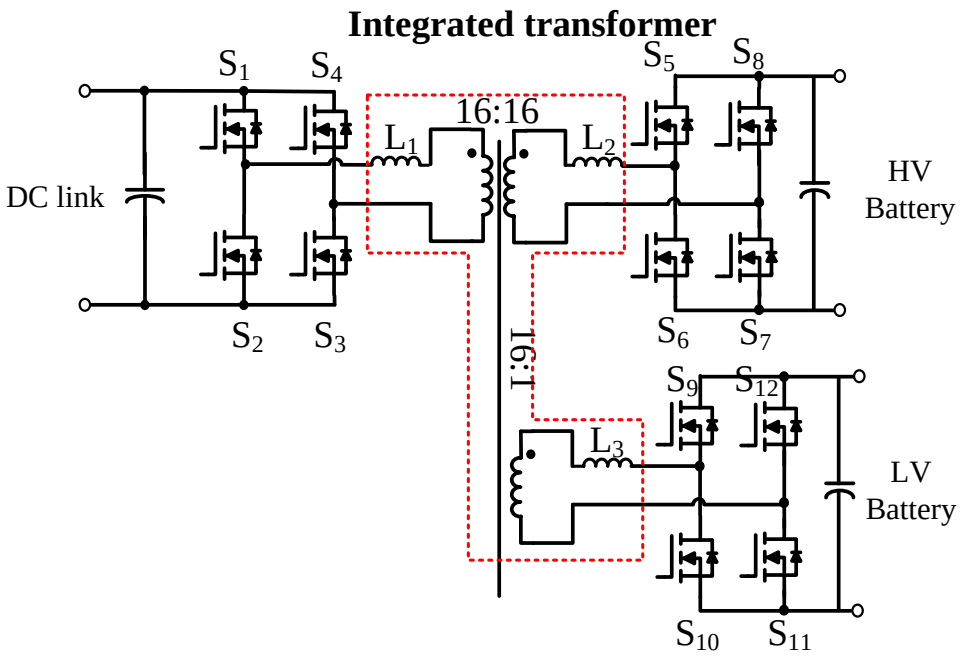


Fig. 5.23. Integrated transformer for TAB converter

However, in order to achieve a compact design, the height of the power component should be carefully designed. If one component has a significantly larger height than the rest, it will waste space and jeopardize the power density. The best component density can be achieved by having all the power components share similar height as shown in Fig. 5.24. Therefore, a flat profile for a transformer is desirable and a planar transformer is the best option for this purpose. However, even though a planar transformer is the best option for a compact design, it has a higher winding loss due to the proximity and skin effect due to the wide PCB windings compared to the regular transformer where Litz wire can be used. High winding loss makes the thermal management challenging, especially for a compact design where not enough surface area is available for heat transfer and dissipation. Therefore, it is critical to find a way to design an integrated planar transformer that can provide a low AC winding resistance while its leakage inductance can be controlled to serve as L_1, L_2 and L_3 in Fig. 5.23.

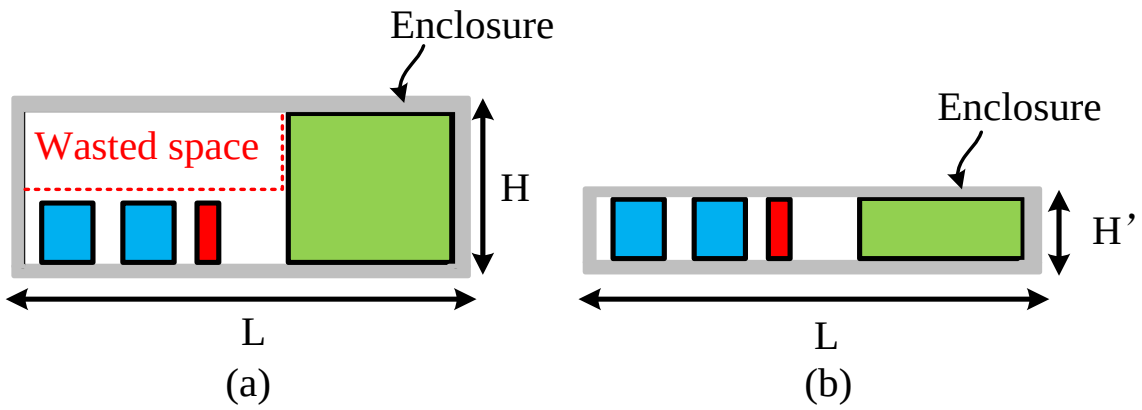


Fig. 5.24. Power density optimization: component height management (a) Components with different height, (b) Components with similar height

5.5.1. Winding resistance reduction, leakage control and economic PCB option

As mentioned in the last section, it is critical to reduce the winding resistance in order to improve the efficiency of the converter and achieve better thermal performance. The most commonly-used method to reduce the winding resistance is to interleave the windings, thus the magneto motive force (MMF) across the windings is as shown in Fig. 5.25.

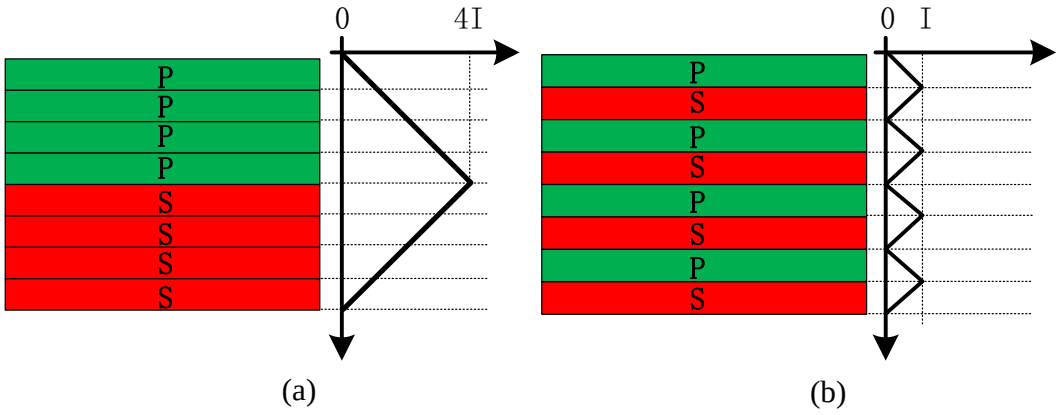


Fig. 5.25. Interleaved winding structure and MMF reduction: (a) Non-interleaving winding, (b) Interleaving winding

However, interleaving winding structure is not good for leakage control because two windings are highly coupled with each other in an interleaving structure. Therefore, in order to achieve both low winding resistance and controllable leakage, an innovative winding structure called asymmetrical interleaving winding is proposed in this section. As shown in Fig. 5.26, the primary and secondary windings of the transformer are distributed on two side legs of the EE core, with N_{p1} and N_{p2} as number of turns for primary windings on the left and right leg, and N_{s1} and N_{s2} as number of turns for secondary winding on the left and right leg, respectively. Meanwhile, for the balance of the magnetic flux, tertiary winding is equally split into two side legs with N_t turns and they will be connected in parallel.

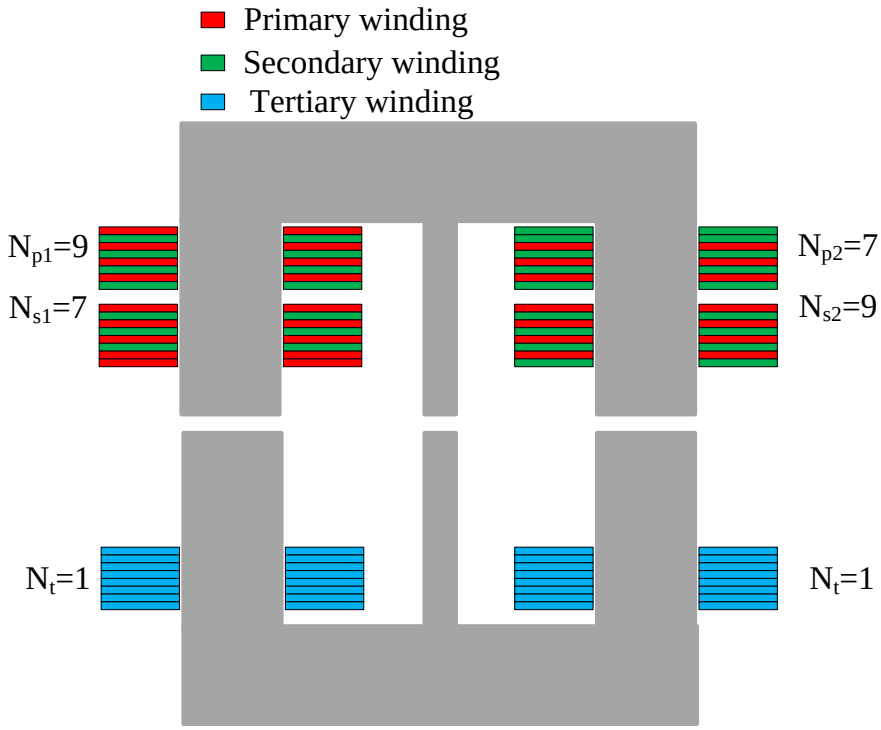


Fig. 5.26. Proposed winding structure of integrated planar transformer:

Asymmetrical interleaving winding

On the other hand, the three-winding transformer can be modeled based on magnetic reluctance and magnetic flux, shown as Fig. 5.27. In this equivalent model, R_{g1}, R_{g2} and R_{g3}

are the magnetic reluctance of the air-gap for each leg, $\emptyset_1$, $\emptyset_2$ and $\emptyset_3$ are the magnetic flux flowing through each leg. These fluxes can be modeled as Eq. (5.69) – Eq. (5.71).

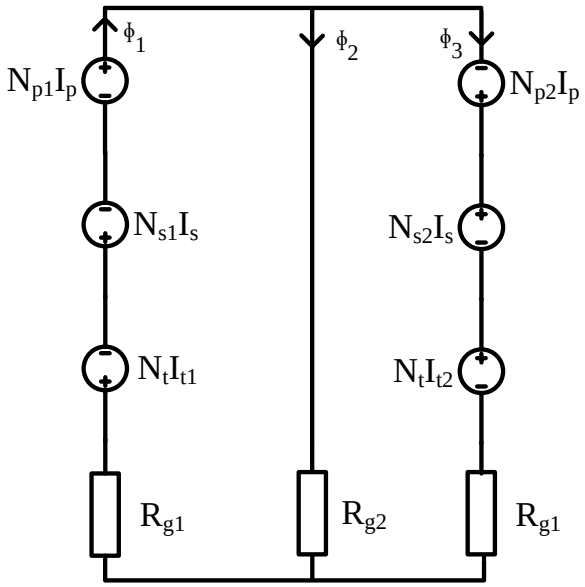


Fig. 5.27. Flux-reluctance based equivalent model for three-winding transformer

$$\emptyset_1 = \frac{I_p\left(N_{p1}R_{g1}+N_{p1}R_{g2}+N_{p2}R_{g2}\right)-I_s\left(N_{s1}R_{g1}+N_{s1}R_{g2}+N_{s2}R_{g2}\right)-I_{t1}\left(N_tR_{g1}+N_tR_{g2}\right)-I_{t2}\left(N_tR_{g2}\right)}{R_{g1}\left(R_{g1}+2R_{g2}\right)} \quad (5.69)$$

$$\emptyset_2 = \frac{I_p\left(N_{p1}-N_{p2}\right)+I_s\left(N_{s2}-N_{s1}\right)-I_{t1}N_t+I_{t2}N_t}{R_{g1}+2R_{g2}} \quad (5.70)$$

$$\emptyset_3 = \frac{I_p\left(N_{p1}R_{g2}+N_{p2}R_{g1}+N_{p2}R_{g2}\right)-I_s\left(N_{s1}R_{g2}+N_{s2}R_{g1}+N_{s2}R_{g2}\right)-I_{t1}\left(N_tR_{g2}\right)-I_{t2}\left(N_tR_{g1}+N_tR_{g2}\right)}{R_{g1}\left(R_{g1}+2R_{g2}\right)} \quad (5.71)$$

Then the magnetizing inductance and leakage inductance of the transformer can be calculated as Eq. (5.72) and Eq. (5.73), respectively [94].

$$L_m = \frac{N_{p1}\emptyset_{1|i_s=i_t=0}+N_{p2}\emptyset_{2|i_s=i_t=0}}{i_p} \quad (5.72)$$

$$L_{lk} = \frac{N_{p1}\emptyset_{1|i_s=i_t=0}+N_{p2}\emptyset_{3|i_s=i_t=0}-N_{s1}\emptyset_{1|i_s=i_t=0}-N_{s2}\emptyset_{3|i_s=i_t=0}}{I_p} \quad (5.73)$$

where reluctance of the air-gap can be expressed as Eq. (5.74) – Eq. (5.76).

$$R_{g1} = \frac{A_1}{\mu_0 l_{g1}} \quad (5.74)$$

$$R_{g2} = \frac{A_2}{\mu_0 l_{g2}} \quad (5.75)$$

$$R_{g3} = \frac{A_3}{\mu_0 l_{g3}} \tag{5.76}$$

where μ_0 is the permeability of the air, l_{g1}, l_{g2}, l_{g3} are the air-gap of left, middle and right leg, A_1, A_2, A_3 are the cross-section area of left, middle and right leg. Eq. (5.72) – Eq. (5.76) together suggest that by controlling the cross-section area of each leg of the core and the air-gap, magnetizing inductance and leakage inductance can be controlled.

Based on the gain requirement shown in Fig. 5.2 and the power rating of the converter, the design specification of the transformer is summarized as Table 5.16.

Table 5.16 Design specification of proposed integrated planar transformer

Item	Value
Turns ratio (Primary : Secondary :Tertiary)	16:16:1
Winding current capacity (Primary/Secondary/Tertiary)	40A/40A/400A
Target Leakage inductance	<15μH
Target Magnetizing inductance	>800 μH
Maximum power capacity	6.6kW

Based on the required specifications and Eq. (5.72) – Eq. (5.76), winding structure (N_{p1}, N_{p2}, N_{s1}, N_{s2} and N_t) and core geometry (A_1, A_2, A_3, lg_1, lg_2, lg_3, etc.) can be determined. Calculation results are summarized in Table 5.17, and core geometry is shown in Fig. 5.28. The design is verified by FEA 3D simulations as shown in Fig. 5.29.

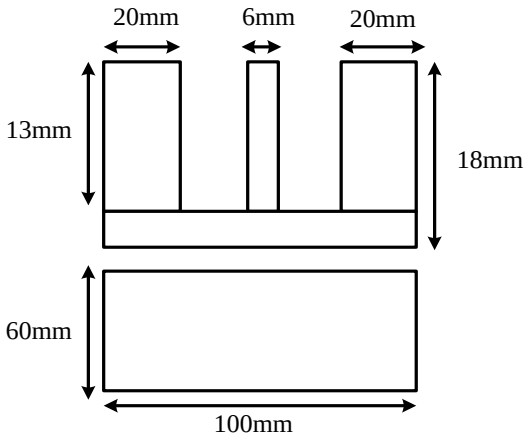


Fig. 5.28. Core geometry for proposed integrated planar transformer

Table 5.17 Design summary of proposed integrated planar transformer

`	Value
Turns ratio (Primary : Secondary :Tertiary)	16:16:1
$N_{p1}/N_{p2}/N_{s1}/N_{s2}/N_t$	9/7/7/9/1
Selected core	Customized core (TDK PC95)
Simulated Leakage inductance	$8\mu H$
Simulated Magnetizing inductance	$1.3mH$
Simulated peak flux density	$200mT$
Estimated core loss	23.2W
Estimated winding loss	73W

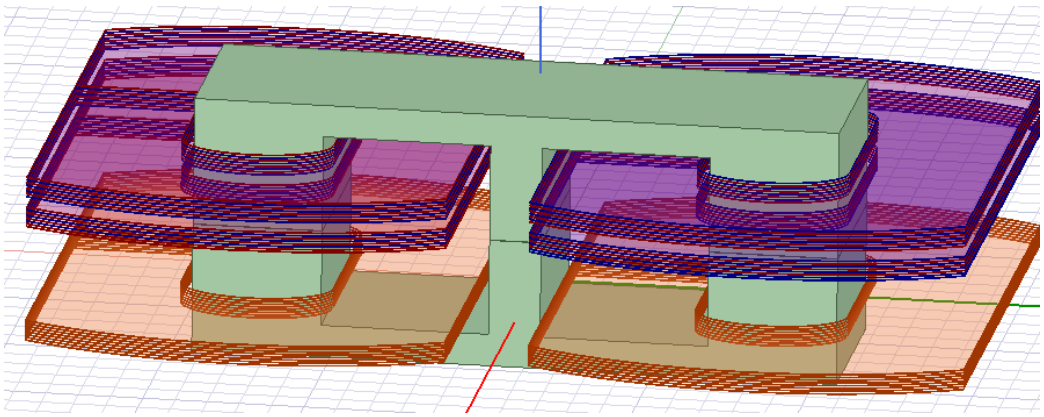


Fig. 5.29. FEA 3D simulation model for proposed winding structure

5.5.2. Hardware implementation

Designing a planar transformer with 16 turns of winding can be costly because the 16-layer boards are expensive. Therefore, it is critical to find a way to reduce the manufacture cost in order to make the design cost-effective. Fortunately, the proposed transformer winding structure can be realized by much cheaper 8 layer boards that are connected in series. As shown in Fig. 5.29, primary windings are labelled as red, secondary windings are labelled as green, tertiary windings are labelled as blue and G_1, G_2 are the gaps among three boards. Inter-board connections are made through copper bars that serve purposes of both electrical connection and mechanical support. As shown in Fig. 5.30, primary and secondary windings in the top two boards are connected in series with short copper bars with a length of G_1. Tertiary windings in the bottom board are connected in parallel. Moreover, long copper bars are used as the connection between winding PCBs and the main power board to make the entire transformer as a through-hole type component to enhance the manufacturability. Furthermore, these copper bars can be designed into press-fit pins to further increase the reliability and manufacturability. The 3D modeling of the design is presented in Fig. 5.31. Verified by the 3D FEA simulation, gap G1 and G2 will not have a noticeable impact on inductance values of the transformer, and the leakage and magnetizing inductance is mainly determined by A_1, A_2, A_3, lg_1, lg_2 and lg_3. After several iterations of design, the values of

these parameters are determined as shown in Fig. 5.28. For readers' convenience, they are also summarized as Table 5. 18. Lastly, PCB design of the proposed transformer windings (top, middle and bottom PCB boards) are shown in Fig. 5.32.

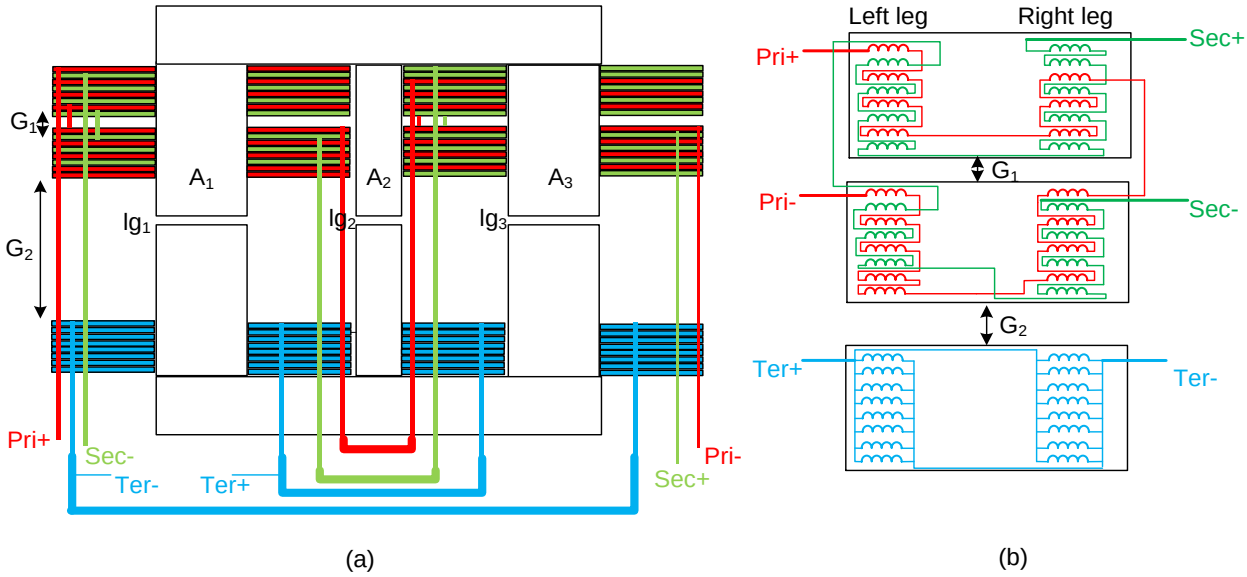


Fig. 5.30. Hardware implementation of proposed transformer windings: (a) Mechanical structure design, (b) Electrical connection of the windings

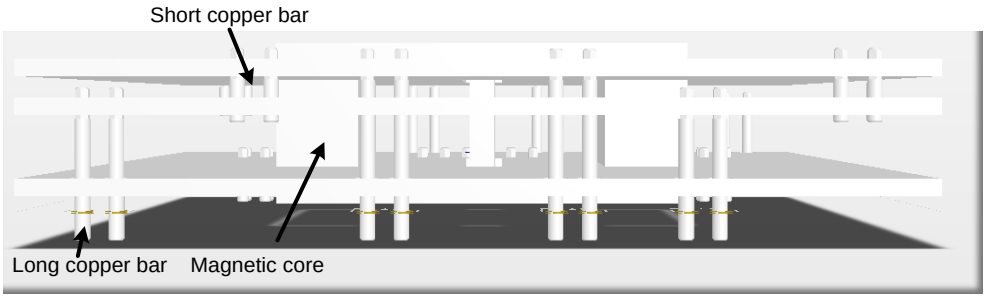


Fig. 5.31. 3D model of the proposed transformer winding structure

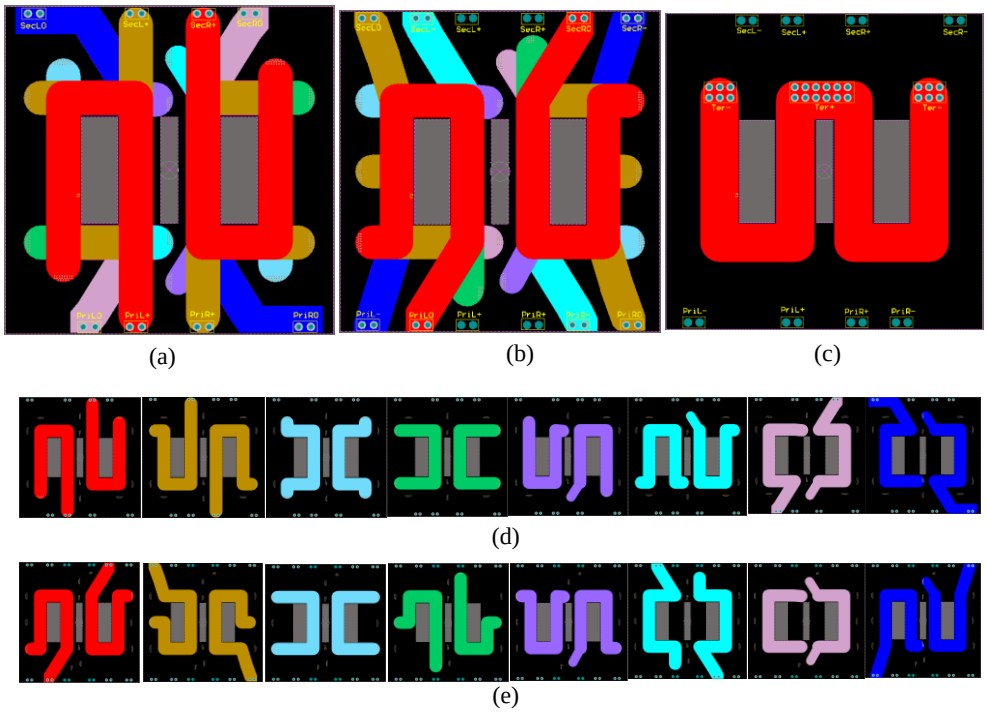


Fig. 5.32. PCB design of the proposed transformer winding: (a) Top board (b) Middle board (c) Bottom board (d) layer-to-layer display of top board (e) layer-to-layer display of middle board

Table 5.18 Design summary of the core geometry and air gaps

Item	Value
A_1	60mm*20mm
A_2	60mm*6mm
A_3	60mm*20mm
lg_1	0.1mm
lg_2	0.1mm
lg_3	0.1mm

5.6. Experimental verifications

To verify the effectiveness of the proposed design, a design set-up was built. Its specifications are summarized as Table 5.19.

Table 5. 19 Summary of experimental set-up design specs

Item	Value
Input voltage	400V
HV side voltage	250-450V_{DC}
LV side voltage	9-14V_{DC}
Maximum HV side output power	450W
Maximum LV output pwer	200W

Moreover, an experimental set-up with the proposed integrated transformer was assembled as shown in Fig. 5.33. The open/short circuit test results of the transformer are recorded in Table 5.20.

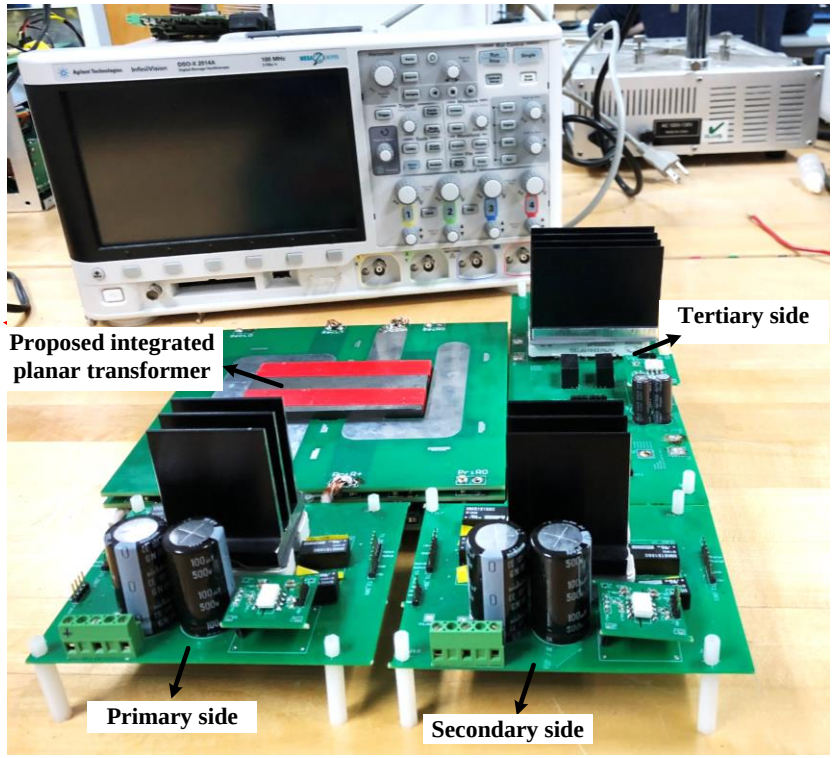


Fig. 5. 33. Assembled experimental set-up for proposed integrated transformer

Table 5. 20 Inductance testing results for the proposed integrated transformer

Item	Value
Primary side open circuit test	1.56mH
Secondary side open circuit test	1.57mH
Tertiary side open circuit test	11µH
Primary side short circuit test	10.56µH
Secondary side short circuit test	11µH
Tertiary side short circuit test	7.6nH
Estimated magnetizing inductance	1.5mH
Estimated leakage inductance (referred to primary side)	7µH

5.6.1. G2V and G2V operation mode

Fig. 5.34 and Fig. 5.35 are steady state waveforms of G2V and V2G operation at 450 output power, respectively. Moreover, to validate the phase-shift based control under this mode, a 50% load step up and step down were performed as shown in Fig .5.36 and Fig. 5.37, respectively. Furthermore, the efficiency performance was thoroughly benchmarked under different HV battery voltage levels and loads as shown in Fig. 38. Here, I_{pri}, I_{sec} and I_{ter} are the transformer winding current on primary, secondary and tertiary side, respectively.

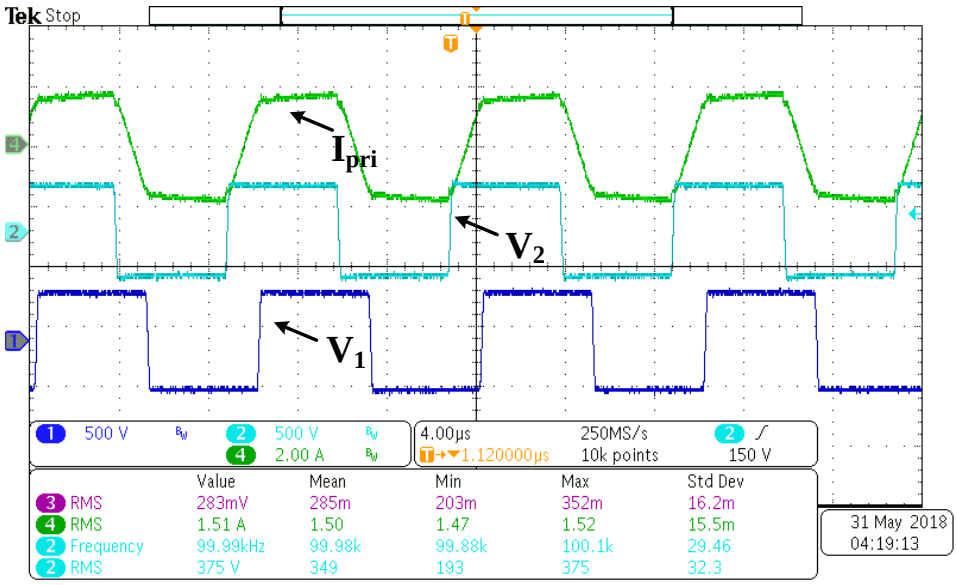


Fig. 5. 34. Steady-state waveform of G2V operation @ $V_{HV} = 400V$, $P_2 = 450W$

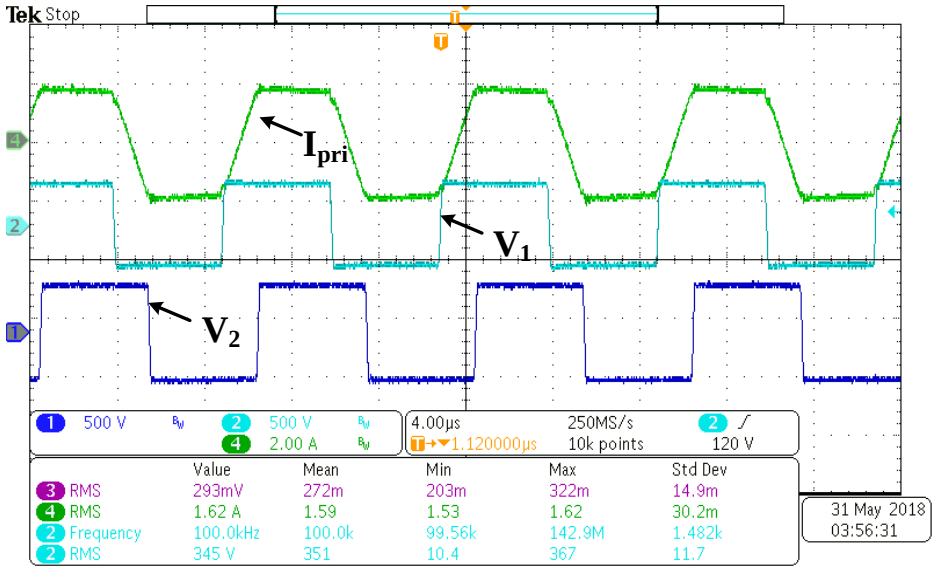


Fig. 5. 35. Steady-state waveform of V2G operation @ $V_{DC} = 400V$, $P_1 = 450W$

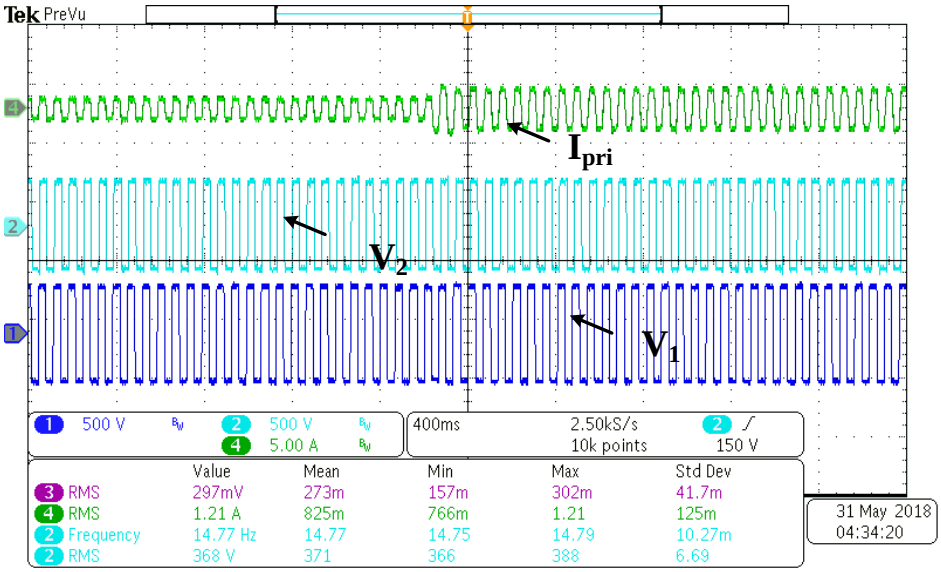


Fig. 5. 36. Load transient waveform: load step up from 260W to 450W

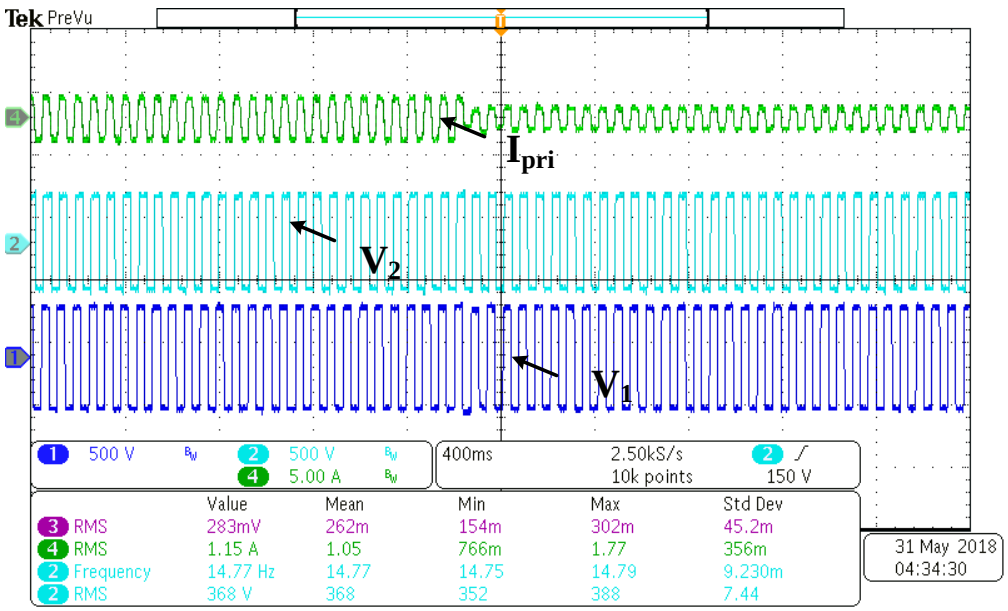
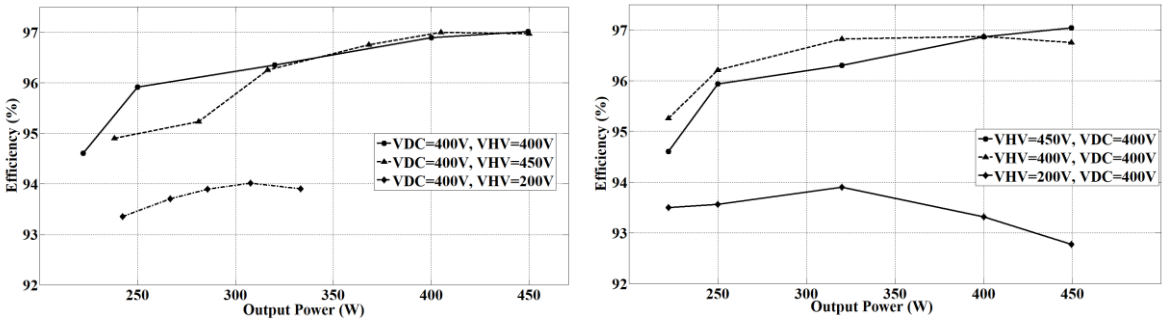


Fig. 5. 37. Load transient waveform: load step up from 450W to 260W



(a) (b)

Fig. 5. 38. Efficiency curves under different HV battery voltage and load power: (a) G2V mode, (b) V2G mode

5.6.2. H2L and G2L mode

The functionality to step down a high voltage of 400V (from HV battery or DC link) to low voltage of ~12V was also tested. The waveform is given as Fig. 5.39 and Fig. 5.40 with different load powers. Similarly, the load steps are performed and shown in Fig. 5.41 to verify the effectiveness of the control.

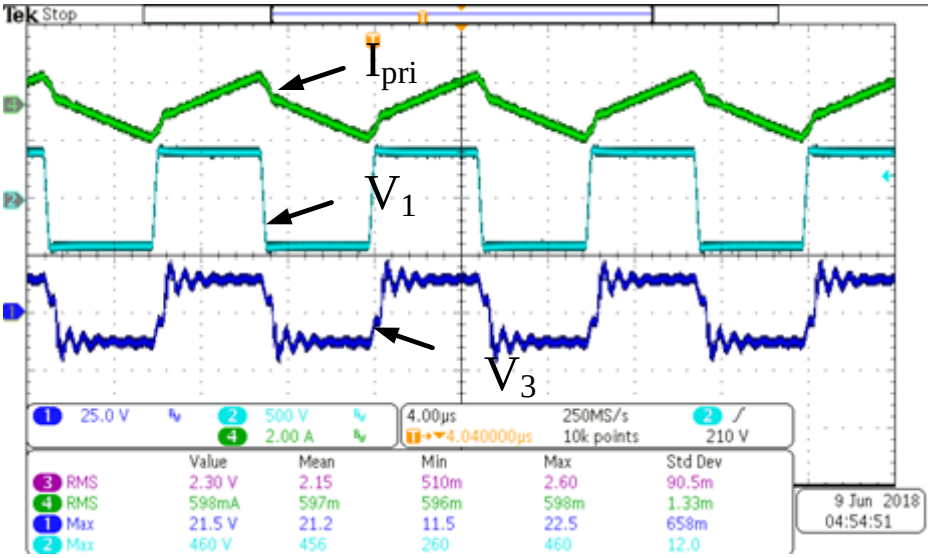


Fig. 5. 39. Steady-state waveform of H2L mode: $V_{LV} = 12V$, $P_3 = 120W$

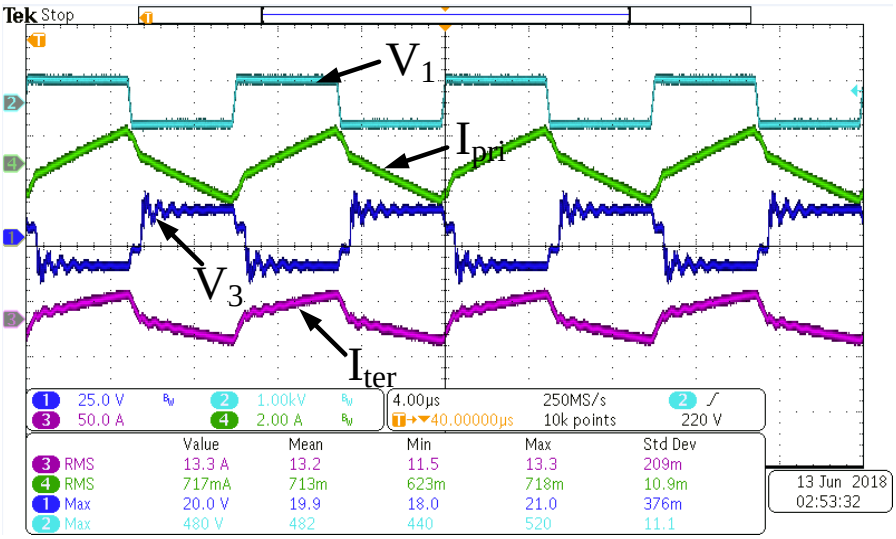
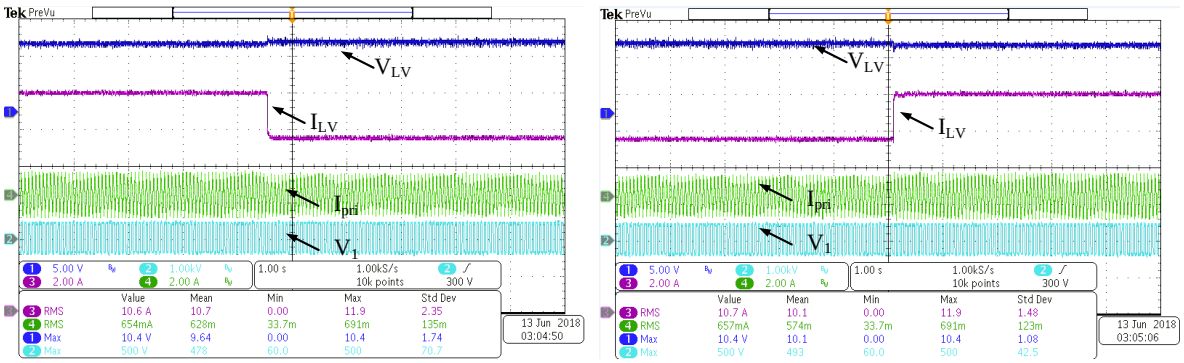


Fig. 5. 40. Steady-state waveform of G2L mode: $V_{LV} = 12V$, $P_3 = 200W$



(a) (b)

Fig. 5. 41. Load transient waveform: (a) Load step down from 200W to 144W, (b) Load step uo from 144W to 200W

5.6.3. G2B mode and mode transitions

Capability of the G2B operation mode is the core feature of the proposed TAB based integrated converter. It was validated through experimental results. Fig. 5.42 is the steady state waveform for the G2B operation mode with $V_{DC} = V_{HV} = 400V$, $V_{LV} = 12V$ under load power of $P_2 = 250W$, $P_1 = 127W$. Fig. 5.43 and Fig. 5.44 are the load step experiment under the G2B operation mode, showing that under the load changes, the proposed controller is able to regulated both HV and LV voltage simultaneously.

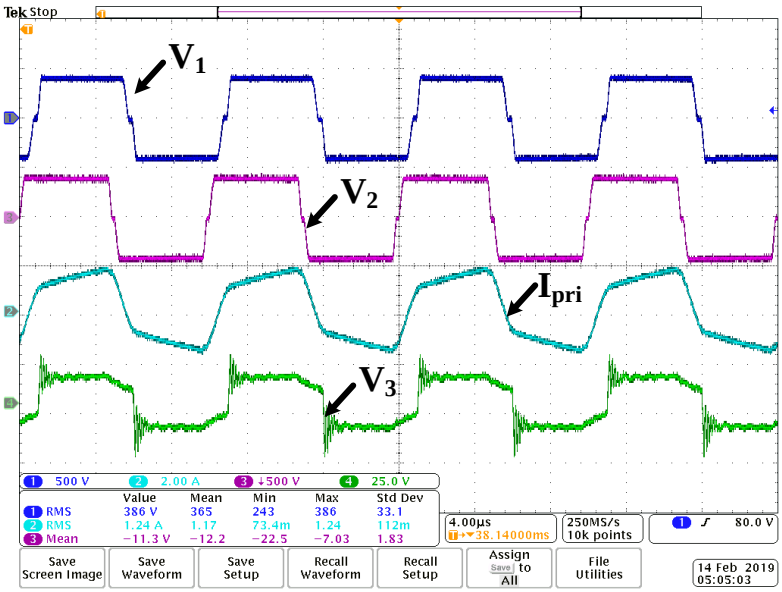


Fig. 5. 42. Steady state waveform of G2B mode: $V_{DC} = V_{HV} = 400V$, $V_{LV} = 12V$, $P_2 = 250W$ and $P_3 = 127W$.

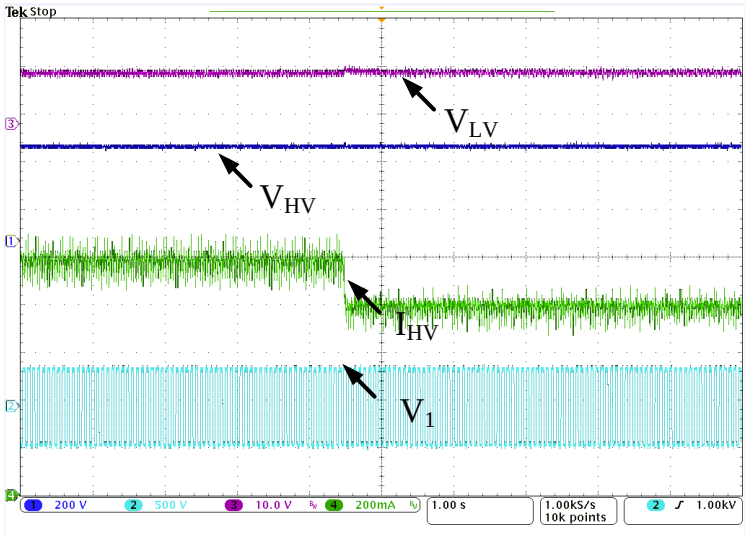


Fig. 5. 43. Load step down at HV side while both HV and LV voltages are tightly regulated

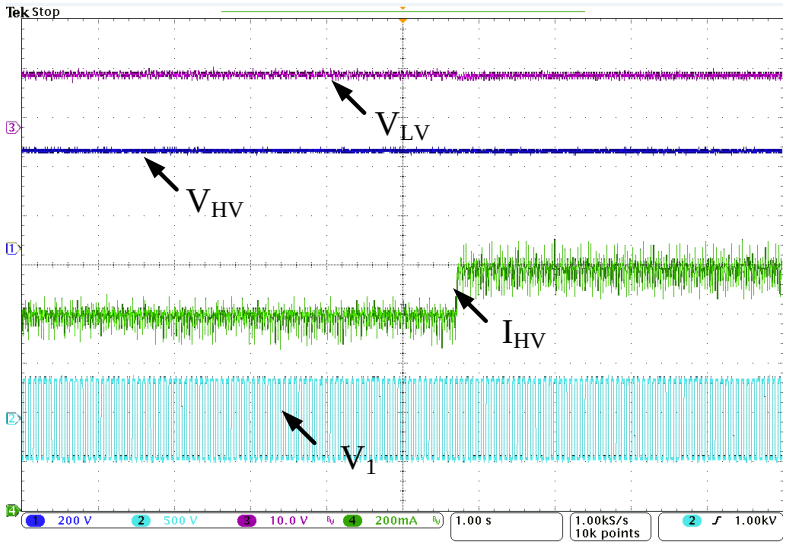


Fig. 5. 44. Load step up at HV side while both HV and LV voltages are tightly regulated

Fig. 5.45 is the measured efficiency for G2B operation mode under different loads for both HV and LV sides. As can be seen from this figure, the peak efficiency is achieved when P_2 and P_3 are not in the light load territory while closed with each other. On the other hand, the efficiency significantly drops whenever there is a big mismatch between P_2 and P_3 or one of the ports demands a light load power. This experimental result vindicates the simulation results and theory craft shown in Fig. 5.7 and shows there is an optimum operation region for G2B mode.

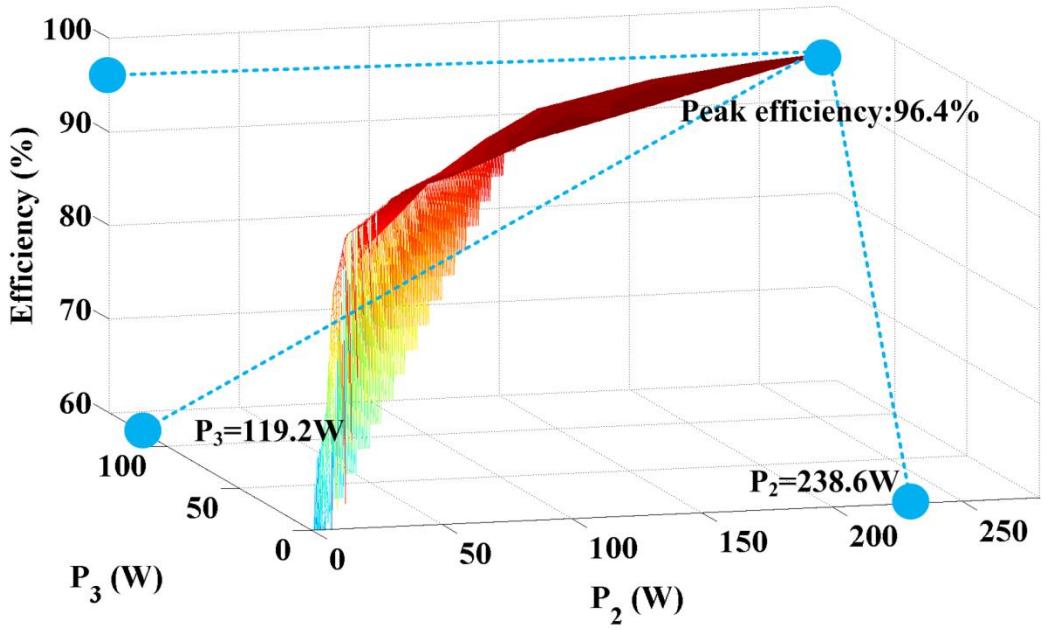


Fig. 5. 45. Efficiency map for G2B operation

Moreover, it is also crucial to validate that the proposed converter is able to switch between two different operation modes. Fig. 5.46 and Fig. 5.47 present the experimental waveforms of transition between G2B and G2V modes, while Fig. 5.48 and Fig. 5.49 are the experimental waveforms of transition between G2B and G2L modes.

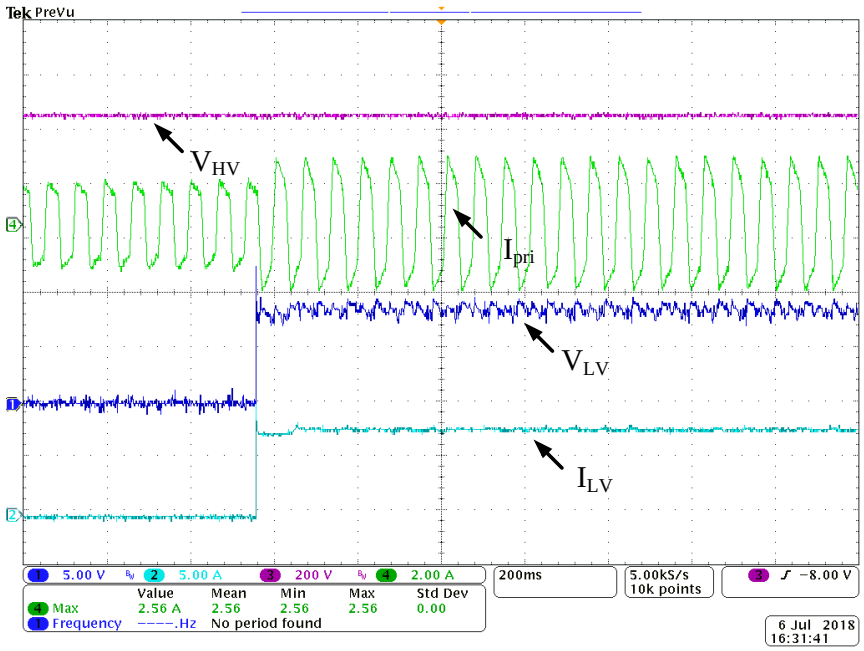


Fig. 5. 46.Mode transition waveform: transition from G2V to G2B mode

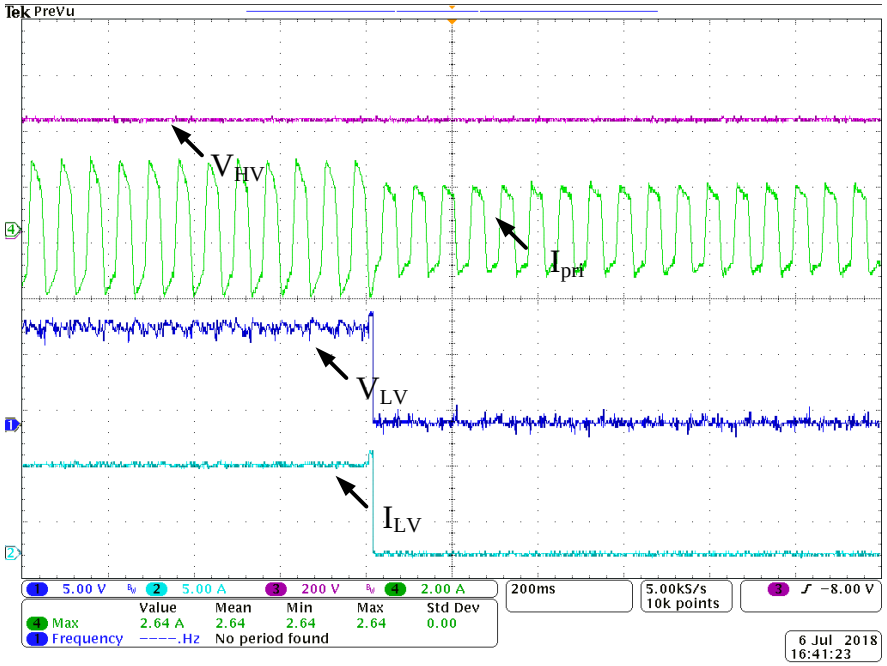


Fig. 5. 47. Mode transition waveform: transition from G2B to G2V mode

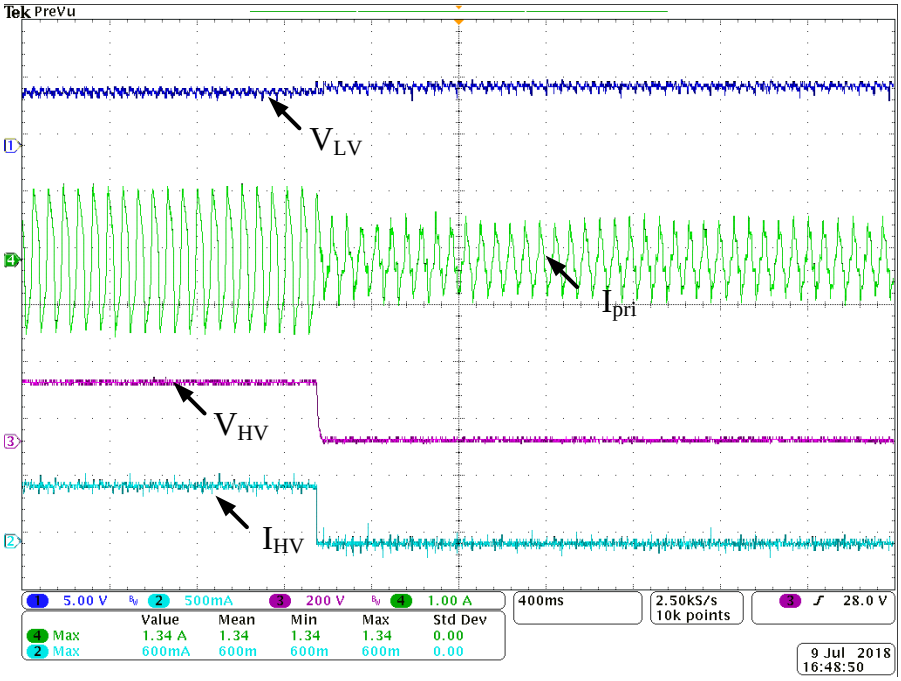


Fig. 5. 48. Mode transition waveform: transition from G2B to G2L mode

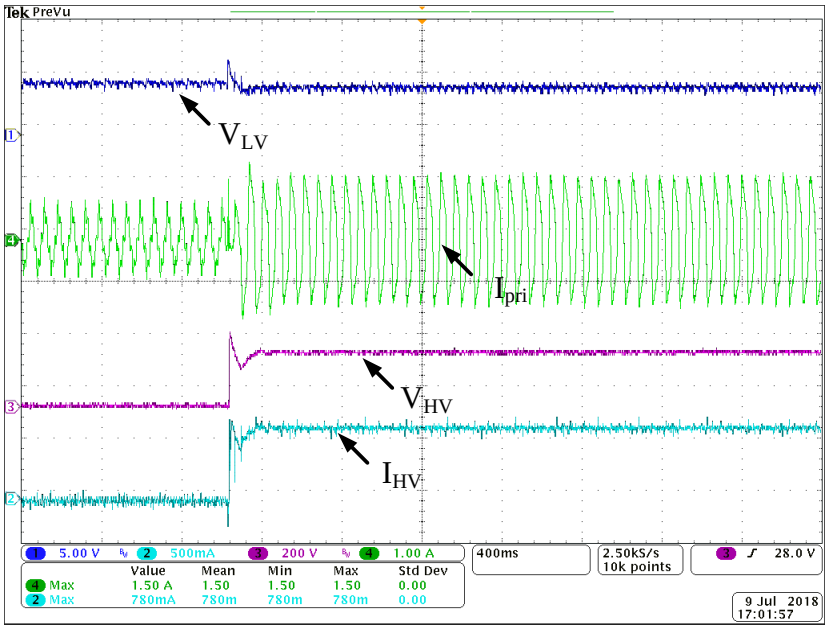


Fig. 5. 49. Mode transition waveform: transition from G2L to G2B mode

Fig. 5.50 validates the effectiveness of the proposed control scheme in terms of the reactive power optimization. The data was acquired under the same output voltage level and load power; the red dot (optimum point) is the output of the proposed control organically. Other points were performed in open loop set up where the phase shift φ_2 is forced to deviate from the optimum point and the same level of output voltage and load power are maintained by adjusting the duty ratio δ_1, δ_2 and/or δ_3. Moreover, a straight efficiency comparison between only phase-shift control and the control scheme with engaging delta control is presented as Fig. 5.51. This comparison shows up to 2% of efficiency improvement with the engagement of the proposed delta control.

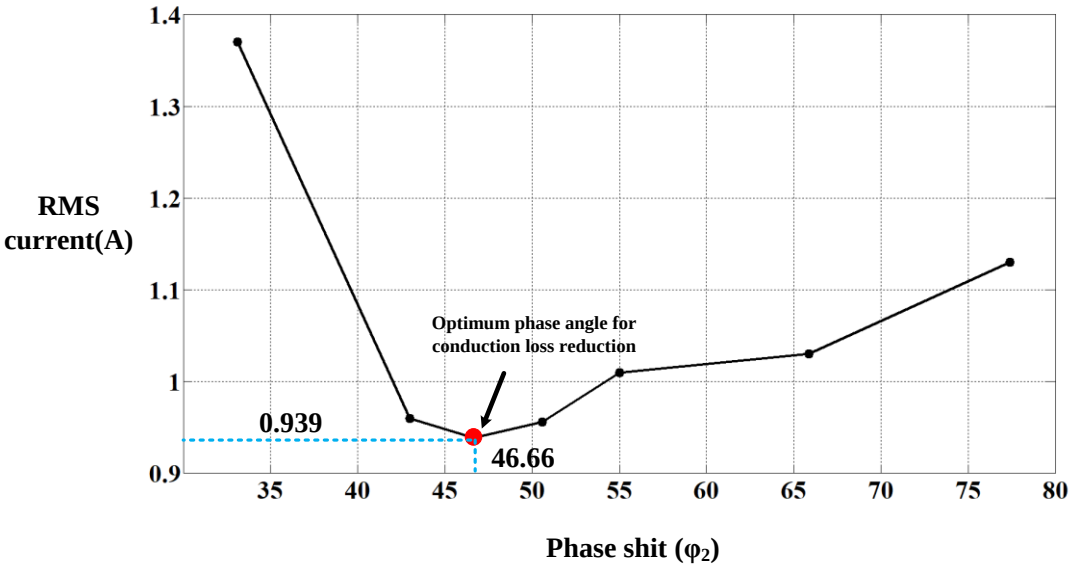


Fig. 5. 50. Comparison of RMS winding current with different control variables (phase shifts) under the same output voltage and load power ($V_{HV} = 400V$, $P_2 = 350W$)

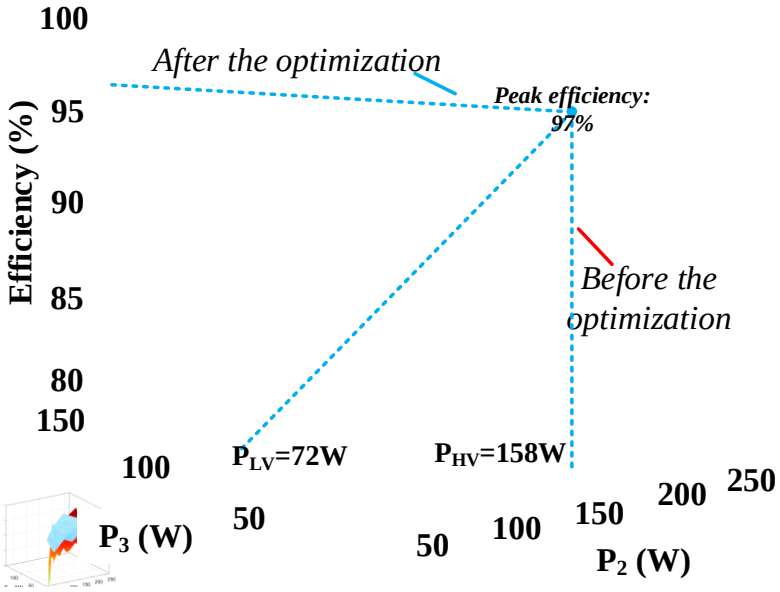


Fig. 5. 51. Comparison between efficiency maps with/without optimization from delta control

5.7. Summary

In this chapter, a new design for integrated OBC is proposed in order to achieve G2B operation mode while being highly compact and cost-effective. A topology consisting of an interleaved totem-pole PFC stage and TAB DC/DC converter is proposed with an innovative phase-shift based control scheme and charging strategy to achieve a complete power-flow management while maintaining good efficiency. Loss analysis is conducted based on an innovative real-time dynamic modeling for better accuracy of loss estimation. Moreover, a planar transformer design is proposed for a three-winding integrated transformer to improve the power density and efficiency of the design. The proposed design is verified through various experiments on an experimental setup and tested up to 600W.

According to the experimental measurements, the proposed control scheme is effective in all operation modes (G2V, V2G, H2L, G2L and G2B). Moreover, the peak efficiency of the TAB converter with the proposed control scheme is 97.6%, which shows ~2% improvement over the peak efficiency without the proposed control scheme.

Chapter 6. Conclusion and future work

6.1. Conclusion

This dissertation work proposed an innovative integrated OBC to enhance the volumetric and gravimetric power density of the conventional EV charging systems by integrating an OBC and an APM together through a three-winding integrated transformer and a novel control strategy.

For the front-end PFC stage, the zero-crossing current spike is resolved by a well-designed control strategy specifically targeting the main mechanism for the spike: reverse recovery of the body diode of the MOSFETs and the hardware delay from sensing circuitry and digital controller. To counter the effect from the reverse recovery of the body diode of the MOSFETs, the soft-transition mechanism is implemented during the input current zero-crossing. Instead of changing the duty ratio abruptly between 0 and 1, the proposed control changes the duty cycle in small steps. Therefore, a much smoother transition can be achieved and current spike can be reduced. Moreover, a phase-lock feedback loop consisting of a notch and a low pass filter is deployed to compensate delays from both digital controller and sensing circuitry by adjusting the central frequency of the loop. As the result of implementing the proposed control method, the zero-crossing current spike is well-mitigated, the power factor is greater than 0.99 for most of the operation condition and the THD remains below 5%.

For the DC/DC stage of the proposed integrated OBC, there are two options: 1) Three-port CLLLC resonant converter; and 2) TAB converter. The CLLLC resonant converter is a combination of a CLLC resonant converter for G2V and V2G operations and a LLC resonant converter for H2L operation. However, due to the limitation of available control variables in this circuit topology, G2B mode is not feasible. It makes the proposed CLLLC resonant converter not suitable for scenario where both HV and LV batteries need to be charged, such

as the preconditioning of the HV battery at the start of the charging process, radio and air conditioner are on during the charging process, etc. One of the biggest benefits of CLLLC resonant converter is the ZVS operation can be easily achieved for MOSFETs under almost all load conditions. With the wide range of ZVS operations for all the MOSFETs, peak efficiency of 96% for G2V and V2G mode and 93.3% for H2L mode is achieved respectively. In G2V and V2G modes, the losses primarily come from the transformer, including both the core loss (~15%) and the winding loss (~40%). On the other hand, in H2L mode, the conduction loss for both transformer winding and MOSFETs is the dominant factor (~50%). Moreover, a low-frequency oscillation was observed during the experiment when both PFC stage and DC/DC stage were cascaded together and controlled by using a cascaded structure consisting of two independent PI controllers. This oscillation can lead to an unstable circuit operation and the failure of the devices. With the analytical modeling of the control-loop for both PFC and DC/DC stages, the low-frequency power oscillation phenomenon is analyzed and explained. In the analyses, three different configurations of feedback loops are studied and trade-offs among them are discussed. From this analysis, it can be concluded that a unified PI controller configuration following several parameter selection guidelines is necessary to remove the aforementioned low-frequency oscillation while maintaining a nice regulation for the output power.

In addition, a novel phase-shift based control scheme is proposed and verified based on the TAB converter. With this newly proposed control scheme, the converter is able to simultaneously charge both HV and LV batteries with optimized conduction loss. Furthermore, the novel loss model for both PFC and DC/DC stages result in accurate loss estimation. The input current waveform of a PFC rectifier circuit is a combination of a line-frequency sinusoidal component and a high-frequency triangular component, the permeability of the PFC inductor core material varies with them. The proposed loss estimation model for PFC stage considers this fact and applies the time-varying inductance to the loss calculation,

whereas conventional calculation methods treat the inductance as a constant value for simplification of the analyses. Moreover, transformer current waveforms for TAB converter are studied and categorized into ten different patterns based on the control variables. As a result, the current waveform can be calculated at any given operating condition of the converter. With the accurate time-domain information of the current waveform, the losses from MOSFETs and the transformer, which are two main loss sources in a TAB converter, can be obtained.

The last but not the least, the three-winding integrated transformer is the core of this proposed integrated charger as the OBC and APM are integrated through magnetic integration. A low-profile planar integrated transformer with innovative winding configuration is proposed. To minimize the winding loss, the AC resistance of the transformer windings is minimized by interleaving primary and secondary windings. On top of that, an asymmetrical winding structure and a new core shape are proposed to generate sufficient leakage inductance to serve as the line inductors in a TAB converter. As a result, no extra inductors and bulky heatsinks are required in a TAB converter with the proposed transformer. Therefore, the proposed low-profile planar integrated transformer further enhances the power density of the design. Through the experimental validation, peak efficiency of 97.6% for the DC/DC stage is obtained from the proof-of-concept laboratory testing setup.

6.2. Future work

One of the main challenges that can be investigated further is parasitic capacitance, and intra/inter winding capacitances in the design and development of the planar transformer technology. More research/work can be done to further improve the transformer design by minimizing the parasitic through new winding configurations and implementation techniques.

Furthermore, this work can be extended into two directions. The first is to increase the switching frequency into MHz territory by utilizing Gallium Nitride (GaN) devices. Secondly, the design can be extended to be scalable to increase the power rating.

6.2.1. GaN based high frequency design

GaN power MOSFETs open up new territory for power electronics solutions for a variety of applications because GaN devices are suitable for working with high frequency operations due to its superior attributes on switching time, reverse recovery, etc. This allows the power electronics to be designed for MHz switching frequency and still maintain the switching loss at an acceptable range.

Therefore, applying GaN technology to this integrated OBC design can potentially be a good path to further enhance the power density of the design. At the current status of the automotive industry, GaN technology is not as mainstream as Si or SiC due to the high production cost, lack of high voltage rating (>650V) devices and less reliability. However, thanks to the massive research effort, the manufacturing process has been slowly but surely improving over time and will finally catch up to where Si and SiC technology are currently at.

6.2.2. Scalability for higher power

Another possible future direction for this work is to increase the power rating of OBC to be 11kW and possibly 22kW. On the other hand, due to the advancement of vehicle entertainment system, the power demand from auxiliary power loads might require the power rating of APM to increase up to 5kW. Moreover, in the foreseeable future, this trend will continue and the power rating for both OBC and APM will continue to increase. Therefore, a

future direction of this work would be to design a scalable integrated OBC as shown in Fig. 6.1.

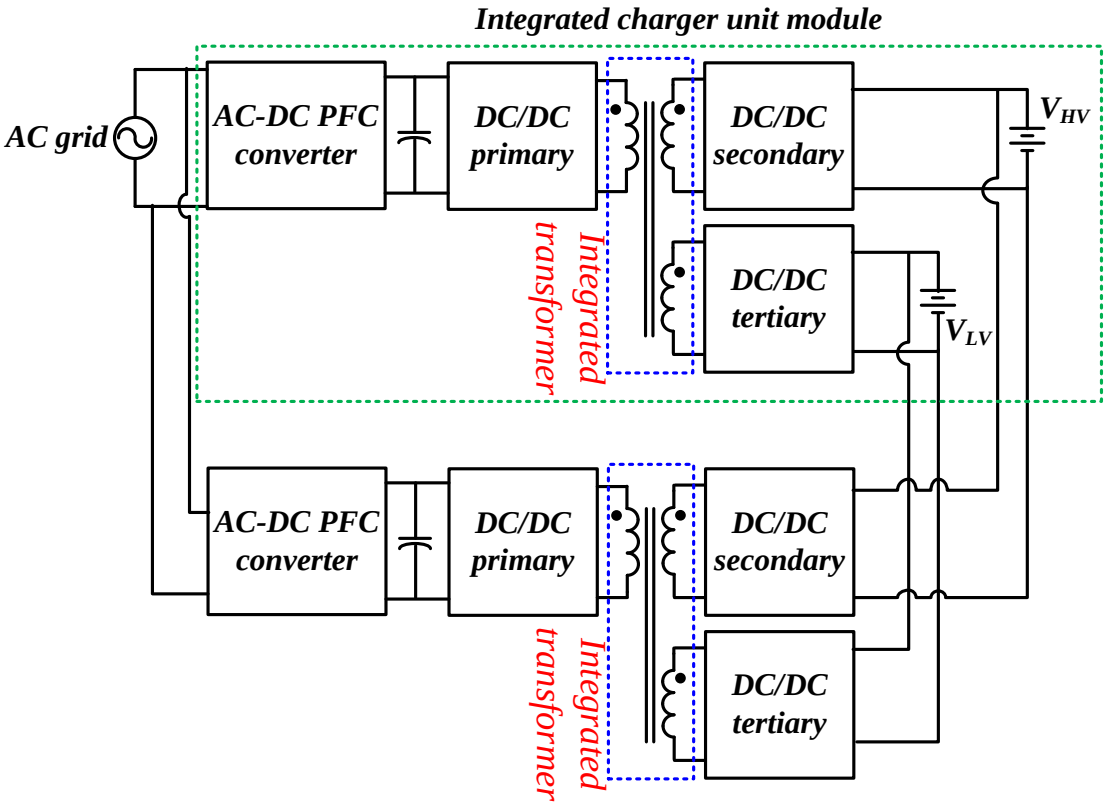


Fig. 6.1. Scalability of the proposed integrated OBC by modular design.

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