#### **ABSTRACT**

Title of Thesis: FABRICATION AND PACKAGING OPTIMIZATION FOR

POLYMER-BASED MICROFLUIDICS

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Packaging microelectromechanical systems (MEMS) often accounts for 80 percent of both the cost and the failures of the devices. For biological MEMS with microfluidic channels, packaging requires reliable fluid and electrical connections. This work describes various strategies for optimizing the fabrication of microfluidic circuits and the design of leak-tight, re-usable, multi-functional packaging systems. Various materials are surveyed to determine the appropriate microfluidic chip substrate for an all-polymer device. Three unique test site designs allow combinatorial experiments and improve the functionality of three proven leak-tight packaging fixtures. Finally, the successful deposition of chitosan, a polysaccharide biopolymer that can act as the interface layer between inorganic electrodes and biological components such as proteins and nucleic acids, is shown in a packaged microfluidic environment for the first time. This study lays the groundwork for future applications in miniaturized bio-reactors and chemical and biological sensors.

# FABRICATION AND PACKAGING OPTIMIZATION FOR POLYMER-BASED MICROFLUIDICS

by

Theresa Michelle Valentine

Thesis submitted to the Faculty of the Graduate School of the University of Maryland, College Park in partial fulfillment of the requirements for the degree of Master of Science 2004

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Professor Gary W. Rubloff, Chair Professor Reza Ghodssi Professor William Bentley ©Copyright by

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2004

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## **Chapter I: Introduction and Motivation**

Motivating this work is the desire to realize the critical "missing link" between proven experimental results and a foreseeable and groundbreaking application. Previously proven in the laboratory (and discussed below) is the beaker-level synthesis of templated biopolymers that allows for future adhesion of proteins, DNA, and cells. The future application is a revolutionary software-controlled fixture for analyzing reactions on disposable microchips (such as for chemical and biological agent detection). What both the literature and in-house laboratories lack is a robust and reliable technique for fabricating and packaging microfluidic systems that would allow reactions to be controlled at a micro-scale. The success of suitable fabrication and packaging techniques and its implication for future research is the subject of the pages that follow.

## BioMEMS: Tiny Sensors and Actuators

Microfluidic systems but subset of bioMEMS (biological are a MicroElectroMechanical Systems), a field swept along by the scientific community's drive to miniaturize systems while imitating the complex elegance of biological function. BioMEMS systems often involve a sensor that emits a signal in response to a stimulus and an actuator that responds by changing or moving the system in some way [1]. One example of this behavior in nature, as McGuire notes, is the iris of the eye. Two sets of muscles lie radially and in a circle around the pupil; they constrict in response to dim or bright light, respectively, to expand or contract the pupil [1]. Chemical sensing cantilevers, whose deflection can be monitored by laser interferometry as molecules are adsorbed, are an example of man-made bioMEMS devices [1]. BioMEMS pumps for microfluidic systems are also under development.

## Packaging Microfluidic Networks

Despite a flurry of research in bioMEMS and specifically microfluidics, few researchers are working to develop reliable packaging systems that are re-usable, multitasked (i.e., all fluid reservoirs and electrical connections are addressed with a single clamping action), and multi-funtional. Packaging systems allow the microfluidic "chip" with micro-scale channels, reservoirs, and electrodes to connect to fluid and electrical sources at the macro-scale. One recent article mentioned that the lack of packaging technologies is the biggest stumbling block to the commercial success of MEMS; packaging generally takes 80 percent of the cost of a MEMS device, and 80 percent of breakdowns are caused by packaging [2]. A review of the current literature shows three major types of packaging systems: single-use, hand-prepared techniques; single-function, single-test-site, re-usable fixtures; and two examples of a multi-tasked, re-usable fixture.

Single-use, hand-prepared techniques often require painstaking connection of fittings and tubing directly to a microfluidic chip by hand. At worst, no fittings at all are used, and all "microfluidics" is forced by dropping solution from a syringe. This approach does not allow for any flow rate control and depends heavily on the hydrophilic properties of the channels to draw fluid to the appropriate areas of the chip. Even hand-fastened fittings are a step above this technique. One procedure used at the University of Maryland requires that tiny 400-micron capillary needles be placed into etched holes on a silicon chip, then surrounded by an O-ring and epoxy for sealing [3]. The needles then connect to tubing for a macro-scale interface. A similar but slightly more complex procedure uses a silicon and plastic press-fitting coupler to connect capillaries to holes

etched in silicon with deep reactive ion etching (DRIE) [4]. Another design for implantable microfluidic devices inserts part of a polyimide chip with microchannels directly into flexible tubing and seals the connection with glue [5].\*

Small re-usable fixtures that contain one test site and generally have one function (such as electrical powering or fluid flow) are also seen in the literature. A microfluidic circuit board offers fairly sophisticated fluid interconnection: small-diameter tubing attaches directly to micromachined hexagonal ports on a silicon breadboard, and a microfluidic component made of silicon anodically bonded to glass joins to the breadboard with either an interlocking fin structure or a hole-and-cylinder structure [6]. This circuit board, however, has been proven only with very simple channels on a small scale (the entire fixture is a few centimeters wide) without any electrical connections. Another small fixture uses a postage-stamp sized chip with thin film heaters and microfluidic channels defined in polydimethyl siloxane (PDMS), packaged in a fixture with high voltage electrodes and a circuit board interface for data acquisition [7]. This approach does not seem to have an easy method for fluid input or for connecting the electrodes to the chip.

One research group has developed a larger, multi-tasked, re-usable fixture made of polycarbonate with fluid connections sealed by O-rings and electrical connections made with spring-loaded probes; an optical window is even added to allow access to a dye laser on the chip [8]. This packaging system, though sophisticated, is set up for one small chip with one test site consisting of a micromixer and dye laser – not for

<sup>\*</sup> 

<sup>\*</sup> ScienceDirect, the searchable database of Elsevier journals, shows 74 hits for "microfluidics AND glue" in articles' full text for 1994 to 2004. For "microfluidics AND packaging" there are 127 hits in articles' full text, but only 8 in the abstract, title, or keywords.

performing multiple experiments on various test sites on the same packaged chip. Finally, an advanced packaging scheme has been shown by a group in Japan, in which an 11x11x0.9 mm chip drops into a socket fitted with 28 electrical connections\*, silicone tubes that self-seal to the chip to provide fluid connections, and screw valves at each fluid connection† [9]. A one-touch closure mechanism seals the entire device. This packaging fixture has a few weaknesses, however: the microchannels cannot be observed in a microscope because of the configuration of the package and the distance of the channels from the package surface, the electrical leads are on the backside of the chip (meaning that electrodes could not be placed in the flow channels), and the wafers had to be drilled with through holes using an ultrasonic technique since the researchers could not pattern electrodes on a plastic substrate [9]. Not only does the work described in this thesis have similar re-usable, multi-tasked results, but also it removes all three of these weaknesses.

## Biofunctionalizing Patterned Substrates

The unique application of the current work is to provide a microfluidic platform for the biofunctionalization of patterned substrates. In the author's research group, many recent publications have dealt with depositing chitosan on patterned (templated) substrates. Chitosan is an amino-polysaccharide derived from chitin (a component of crab shells, among other materials) that acts as a soluble, cationic polyelectrolyte when exposed to solutions of low pH (less than 6) [10]. When the pH of a solution is raised, the amine groups are deprotonated and the chitosan becomes insoluble [10]. For the present work, applied voltage causes a high pH at the negative electrode (cathode) of an electrolytic cell and thereby a pH gradient in the solution around the electrode.

<sup>\*</sup> A standard IC testing socket modified to add fluid connections, etc.

<sup>†</sup> Tightening the screw closes off the tubing.

Therefore, chitosan deposits on this negative electrode to a thickness and structure determined by the applied current density and the properties of the pH gradient. This film remains stable even when the voltage is removed [10].

The deposition mechanism, as it is currently understood, is visualized in Figure 1. Without any chitosan deposition (top diagram), electrons emitted from the cathode combine with hydrogen ions in solution to form molecular hydrogen (1), creating a pH gradient near the cathode where hydrogen is consumed (2), and water dissociation balances the consumed hydrogen ions in the bulk of the solution (3) [11]. The shape of the pH gradient depends on the current density in the solution. When chitosan is added to the solution (bottom diagram), the positively charged chitosan molecules are attracted to the negative cathode surface (1) where they become insoluble at a pH below 6.3, as caused by the hydrogen evolution reaction (2) [11].

This deposition process was shown first using two silicon wafers with patterned chromium and gold electrodes, one to act as the working electrode and one as the reference electrode; in this experiment, chitosan was found to deposit on the negative electrode [12]. A second set of experiments used two sets of patterned electrodes on the same wafer, which was subsequently immersed in chitosan solution – chitosan deposited only on the negatively biased working electrodes, not on the counter electrodes or bare substrate [10]. The most recent experiments on patterned electrodes showed that deposited chitosan could be activated with glutaraldehyde (an amine-reactive cross-linking agent); nucleic acids and proteins could then be conjugated to the activated chitosan surface, resulting in a patterned array of these biological materials [13].

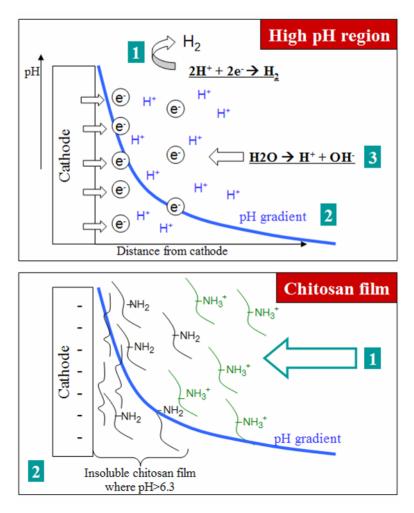


Figure 1. Chitosan deposition driven by pH gradients in solution caused by negative bias on the cathode of an electrolytic cell (based on original figure drawn by Jung Jin Park, 6 April 2004).

As mentioned above, the work described in this thesis serves as a link between experimental results (mainly with chitosan deposition) and future applications for which reliable, packaged microfluidics are necessary. Microfluidic chip and packaging fabrication schemes without the weaknesses of those found in the literature (such as lack of re-usability, multi-functionality, or ability to be characterized under a microscope), combined with a successful display of chitosan deposition in microfluidic channels, are the basic needs explored by this work. Finding the appropriate materials, as described in the next chapter, is the first step toward achieving these goals.

## **Chapter II: Material Selection**

Fabricating and packaging polymer-based microfluidic devices depends on careful material selection to match mechanical, electrical, and other properties to functionality. Proper materials must be chosen for the device substrate, the electrode layer, the fluid flow layer, any necessary gasket or sealing material, and the packaging (in all its components). Some basic criteria consistent for all of these subsystems are that they be:

- Easy and fast (~1 day or less) to fabricate or machine,
- "Known" that is, fabrication procedures are available in-house or from public resources,
- Inexpensive and readily available,
- Non-toxic or (even better) bio-compatible,
- Rigid (for the substrate, packaging, and possibly flow layer) or flexible (for the gasket) as necessary, and
- Reproducibly patterned

Other material selection criteria, of course, exist specific to each subsystem. In most cases, the simplest routes have been taken where more complicated materials might be more suitable in the long term. All materials considered for each subsystem, however, will be discussed below.

#### Device Substrate Material

The most important constraints for device substrate materials at present are that they be temperature-resistant, smooth enough, rigid enough, and of the right size to be used with available microfabrication tools, most importantly spin-coating machines and mask aligners. Temperature resistance comes first, since the polymeric materials to be deposited on the substrate must be cured at temperatures up to 95°C. Obviously, the substrate cannot distort, soften, or melt when in contact with the hotplate or furnace. The second two criteria are vague necessarily, since spin-coating machines especially are generally used with highly polished, rigid silicon wafers and not with the more imperfect materials suitable for bioMEMS. Substrate wafers must be smooth enough for the spincoating machine to create the vacuum necessary to keep the wafer on the chuck. While an exact surface roughness is not known, the unpolished side of a bare silicon wafer is smooth enough, while a wafer covered with Scotch tape is not. "Rigid enough" cannot be quantified other than to state that spin-coating machines are generally used with silicon wafers and support the wafer either only in the central half-inch to three inches. If the edges of the wafer droop noticeably, the coating may not be uniform. Finally, device substrates, for ease of alignment, should be sized to work with available mask aligners – 4 inches in diameter, preferably with a "flat" as on silicon wafers, and 500 microns thick (so that "separation" and "contact" distances for exposure need not be changed).

Substrate materials can be classified as traditional, transparent traditional, and transparent experimental. To date, materials from the first two of these categories have been successfully used, while the third category is still being explored (but holds the most promise for the future).

#### **Traditional Substrate Materials**

The most traditional substrate material possible for bioMEMS is that on which the semiconductor community was built: silicon. However, the advantages of silicon that made it so critical to microelectronics (such as its ability to be doped to a more metallic

or nonmetallic state) are, at least in the current bioMEMS configuration, completely unused. For the initial experiments described in this work, silicon is simply a temperature-resistant, rigid, relatively smooth circle of the right diameter and thickness that can be had for approximately five dollars per wafer\*. Silicon, however, has a few disadvantages, including its brittleness and opacity. A wafer will break if it is clamped too hard in its packaging or it is dropped, and the lack of transparency means that flow cannot be observed from the underside (or as easily from above). Some material properties of silicon are summarized in Table 1; of particular importance for later applications are the modulus of elasticity and the coefficient of thermal expansion.

Table 1. Material properties of silicon substrates [1].

Silicon Material Property	Value
Atomic Density	4.96×10 <sup>22</sup> atoms/cm <sup>3</sup>
Density	2.328 g/cm <sup>3</sup>
Dielectric Constant	11.7 (±0.2)
Energy Gap	1.115 (±0.008) eV
Melting Point	1417(±4) °C
Refractive Index	3.420
Thermal Conductivity	157 W/cm/°C
Thermal Expansion, Linear	2.69(±0.3)×10 <sup>-6</sup> /°C
Lattice Constant	5.4307 Å
Hardness	7.0 Moh
Intrinsic Carrier Concentration $(n_i)$	$1.5 \times 10^{10} / \text{cm}^3$
Poisson's Ratio	0.42
Young's Modulus	130 GPa [15]

<sup>\*</sup> Mechanical grade N and P doped 4" silicon wafers, (100) orientation, were available for \$4.90 a wafer from UniversityWafer.Com as of January 28, 2004. Note that these are mechanical grade wafers, not semiconductor grade – the wafers' semiconducting properties are relatively unimportant.

Silicon is not the only traditional substrate material available, but rather the first to be used. For applications in which electrodes will be patterned on the substrate surface, it is important to have an insulating layer on the substrate to avoid short-circuiting the chip. One of the simplest substrates to provide this functionality is a silicon wafer with a thin layer of insulating silicon dioxide. Such wafers can be purchased pre-processed\* or oxidized in-house. Silicon dioxide has a dielectric constant of 3.9, as opposed to the 11.7 of silicon, and a thermal expansion coefficient of  $0.56 \times 10^{-6}$  /°C [1]. Other traditional substrates such as gallium arsenide could be used, but the additional expense in using these materials cannot be justified since their cheaper silicon and silicon dioxide counterparts already meet the requirements of temperature-resistance, rigidity, smoothness, size, and insulation. Improvements can be made, however, by transitioning to transparent (yet readily available) materials.

#### **Transparent Traditional Substrate Materials**

To solve one of the major limitations of silicon substrates, the opacity that prevents back-side flow monitoring and imaging, transparent substrates can be explored. One of the most widely available transparent substrates is Pyrex, a glass that can be safely taken to high temperatures. Although they cost nearly six times as much as cheap silicon wafers<sup>†</sup>, Pyrex wafers are transparent and less brittle than silicon. However, properties such as thermal expansion are similar to those of silicon, allowing it to be an

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<sup>\*</sup> Pre-processed SiO<sub>2</sub> wafers are also available cheaply from UniversityWafer.com. As of January 28, 2004, a special advertised 4" P/Boron (100) wafers with 10,000 angstrom of oxide for \$19.75 each.

<sup>†</sup> Purchased from UniversityWafer.com, Pyrex 7740 substrates were readily available as of January 28, 2004, in 500 micron (\$28) and 700 micron (\$22.95) thicknesses, both double-side-polished and 4 inches in diameter.

acceptable substitute. Additionally, the dielectric constant of Pyrex is fairly low, much closer to that of silicon dioxide than to that of silicon, so electrodes can be pattered directly onto Pyrex. Table 2 lists some of the same material properties as were listed for silicon. Pyrex also shares a major disadvantage with silicon in that it is difficult to machine. For example, if holes need to be drilled into a substrate to meet packaging needs, Pyrex is not a suitable material. Holes can be drilled with a diamond bit, but the thinness of the material causes cracking that will spread throughout the wafer when it is further processed.

Table 2. Material properties of Pyrex substrates [16], [17].

Pyrex 7740 Material Property	Value
Density	2.23 g/cm <sup>3</sup>
Dielectric Constant	4.6
Softening Point	821°C
Refractive Index	1.473 (at 589.3 nm)
Thermal Expansion, Linear	3.25×10 <sup>-6</sup> /°C
Poisson's Ratio	0.20
Modulus of Elasticity	62.75 GPa

More expensive\* transparent substrates, such as fused silica, fused quartz, 7070 glass, and quartz, can be purchased easily. However, all of these "glassy" substrates have the same machinability problem as Pyrex. The added expense would only be justified if even better optical transmission were necessary (such as for backside microscope interrogation of flow and deposition in microfluidic channels). Otherwise, Pyrex is the

<sup>\*</sup> As an example, double-side polished 4-inch quartz wafers cost \$75 each for small quantities (as of January 28, 2004, on UniversityWafer.com).

best traditional substrate solution. To achieve both machinability and transparency, more creativity is necessary in the material choice.

## **Transparent Experimental Substrate Materials**

The ideal substrate is smooth, relatively rigid, transparent, and easily machinable (into the right dimensions and to achieve desired patterning). Based on these criteria, the obvious choice seems to be a plastic wafer of some sort. However, plastic wafers are not readily available from the same companies that supply traditional substrates. Suppliers of bulk materials, as well as specialty plastic producers, are possible sources of acceptable plastic films. To yield wafers, discs must generally be cut out by hand using a computer-drawn template; any necessary holes in the wafers can be punched with a ¼" hole punch. Several varieties of plastic substrates have been tested to date. Their properties, advantages, and disadvantages are described below.

#### **Polycarbonate**

Thin plastic sheets can be purchased from the McMaster-Carr Supply Company, a supplier of raw materials and diverse mechanical and industrial components. Among these materials is polycarbonate, said to be a material with "excellent clarity and impact strength over a wide temperature range" [18]. Based on this description, polycarbonate seems to meet the requirements of temperature-resistance, transparency, and rigidity; it is, however, a poor electrical insulator. Several material properties of polycarbonate film are given in Table 3. Maximum temperature information was not available specifically for polycarbonate film, but bulk polycarbonate has a maximum temperature of 115°C, a value significantly higher than all anticipated processing temperatures described below.

Additionally, its thermal expansion coefficient will be important to the discussion of fluid flow layer materials in subsequent sections.

Table 3. Material properties of polycarbonate film (<0.3" thick) [19].

Polycarbonate Film Material Property	Value
Dielectric Strength	380 V/mil
Maximum Temperature (bulk)	115°C
Thermal Expansion, Linear	$6.75 \times 10^{-5} / ^{\circ}\text{C}$
Tensile Strength	62.1 MPa
Hardness (Rockwell R)	118

Polycarbonate film is quite easy to work with. Sheets are shipped flat\* with a protective film on one side of the polycarbonate, and discs can be cut and customized with holes as described above. However, the weakness of polycarbonate is its lack of chemical resistance. McMaster-Carr warns: "Use with low concentration acids and alcohols and mild detergents. Do not use with solvents, aromatic hydrocarbons, esters, and ketones." [19] Indeed, traditional wafer cleaning with acetone, methanol, and isopropanol results in a streaked white discoloration of the polycarbonate wafer. Therefore, polycarbonate must not be cleaned in this manner, but only with water and then sufficiently dehydrated.

Additionally, the combination of unexposed SU-8 (a photosensitive epoxy used for the fluid flow layer, described in later sections) and its developing solution on a polycarbonate wafer results in a white, slightly powdery solid being formed on the wafer. If the entire wafer was covered with unexposed SU-8, the wafer is ruined due to cracking and curling; small channels that should have been developed away merely become tinted

<sup>\*</sup> A 24.25"x24.5" sheet of 0.015" thick polycarbonate film from McMaster-Carr cost \$4.41, as of February 25, 2004. Thicknesses from 0.005" to 0.04" were available as films.

white. Figure 2 shows a polycarbonate wafer after developing unexposed SU-8, 24 hours after processing. The curled plastic film at left was peeled from the backside of the polycarbonate wafer (and is not the protective film provided by the manufacturer, which had been removed previously). The white circle with curled edges is what remains of the polycarbonate wafer after reaction with the SU-8 and developer; note the large crack in the middle and the distortion of the wafer. As yet, the details of this reaction are unknown.



Figure 2. Polycarbonate wafer after reaction with SU-8 and developer. At left is plastic film separated from backside of wafer; at right is the remains of the wafer with white reaction product.

Although the transparency, machinability, temperature resistance, and low cost of polycarbonate film are all attractive properties, the unexplained reaction with SU-8 developer and its incompatibility with traditional wafer-cleaning techniques significantly limit its usefulness as a substrate for SU-8 structures. If other materials (described below) are used for microfluidic channels, polycarbonate can again be a wafer candidate. *Cellulose* 

Similarly to polycarbonate, cellulose (acetate) film can be purchased easily from McMaster-Carr\* and cut and customized to a desired wafer configuration.\* McMaster-

<sup>\*</sup> A 42"x50" sheet of acetate film, 0.01" thick, cost \$11.64 from McMaster-Carr as of February 25, 2004. Film thicknesses of 0.005", 0.01", and 0.02" were available.

Carr notes cellulose's good optical clarity and impact resistance, but that it is a poor electrical insulator [18]. Table 4 lists some material properties of acetate film, most of which are comparable to those for polycarbonate film. The thermal expansion coefficient of acetate is higher than that of polycarbonate, and its maximum temperature is also slightly higher.

Table 4. Material properties of acetate film [20].

<b>Acetate Film Material Property</b>	Value
Dielectric Strength	250-600 V/mil
Maximum Temperature	123°C
Thermal Expansion, Linear	10-15×10 <sup>-5</sup> /°C
Tensile Strength	31.0-55.2 MPa
Hardness (Rockwell R)	85-120

Chemical resistance problems also exist for acetate film. McMaster-Carr states that strong acids and alkalis will cause the material to decompose, but that it can be used with weak acids and alkalis [20]. A simple wafer cleaning with acetone, methanol, and isopropanol, however, results in unacceptable degradation of the wafer, as seen in Figure 3. Therefore, as with polycarbonate, acetate must not be cleaned in this manner, but only with water and then sufficiently dehydrated. Acetate film does not seem to be substantially degraded by SU-8 developer, but its texture changes slightly, which may lead to a degradation of optical properties and unsuitability as a substrate.

<sup>\*</sup> If the film is sold as a roll (as from McMaster), significant curling of the film will occur. Back-rolling the film for a day or more should remove enough curl to produce adequately flat wafers.



Figure 3. Acetate wafers before (left) and after (right) cleaning with acetone, methanol, and isopropanol. Such cleaning results in major discoloration and degradation of the wafer.

Kapton

Kapton®, a high-performance polyimide film produced by DuPont, can be used over a wide range of temperatures, is a good insulator, and has high strength and chemical resistance. Some material properties of Kapton® 500 HN (127 micron thick) film are summarized in Table 5. Its tensile strength and dielectric strength are much higher than those for polycarbonate and acetate films, while its thermal expansion coefficient is slightly lower. Notably, Kapton can be used at temperatures up to 400°C, much higher than necessary for SU-8 or PDMS polymeric materials described below, but conceivable for other fluid flow layer material candidates not yet explored.

Table 5. Material properties of DuPont Kapton® 500 HN film [21], [22].

Kapton® 500 HN Material Property	Value
Density	$1.42 \text{ g/cm}^3$
Dielectric Strength	3900 V/mil
Dielectric Constant	3.5
Volume Resistivity	$1.0\times10^{17}\Omega$ -cm
Maximum Field Use Temperature	400°C
Thermal Expansion, Linear (25 micron thickness)	2×10 <sup>-5</sup> /°C
Elastic Modulus (25 micron thickness)	2.5 GPa

Tensile Strength	165 MPa
% Elongation	50

As was true for polycarbonate and acrylic, Kapton can be easily cut and otherwise customized to create a desired wafer configuration. Kapton's cost is also approximate to that of polycarbonate and acrylic.\* Kapton films, however, are not transparent, but rather a translucent brown color with approximately 0% transmission in the ultraviolet [23]. This property makes them suitable as a substrate for microfluidic channels but not for applications in which transparency is critical (for example, performing ultraviolet (UV) exposure through a transparent wafer to achieve bonding of two wafers coated with photoresist). Except for the transparency issue, Kapton's electrical, mechanical, and thermal properties make it an extremely attractive candidate for microfluidic substrates.

## Other Options

Other options not yet explored exist for plastic substrates. DuPont Teflon® film has similar excellent electrical, mechanical, and chemical properties to Kapton and is also transparent. However, Teflon's hallmark inertness makes it currently unacceptable as a microfluidic substrate, because materials spun onto it do not wet the surface as films but rather bead up, as shown in Figure 4.



Figure 4. Teflon® substrate showing non-wetting of SU-8 on inert Teflon® surface.

<sup>\*</sup> DuPont prices Kapton® 500 HN film at \$2.96 per square foot on rolls of a maximum width of 52 inches and a standard length of 1000 feet. Smaller quantities are also available from American Durafilm (Jay or Mike, 800-234-8885).

Other possible candidates for plastic substrates are available from Promerus Electronic Materials. Their line of performance films includes Appear<sup>TM</sup> 3000, Arylite<sup>TM</sup> A100, and Sumilite<sup>TM</sup>. Although these materials have not yet been tried, they seem to have appropriate optical clarity, electrical insulation, and thermal resistance, examples of which are given in Table 6. In addition, Sumilite<sup>TM</sup> resists common chemicals (such as methanol, acetone, hydrogen peroxide, hydrochloric acid, and sodium hydroxide) and is available with an indium tin oxide (ITO) conductive coating [24].

Table 6. Material properties of Promerus performance films [24].

Material Property		Appear <sup>TM</sup> 3000 (100μm thick)	Arylite <sup>TM</sup>	Sumilite <sup>TM</sup>
Density		1.15 g/cm <sup>3</sup>		
Dielectric Constant (1 MHz)		4.14		
Volume Resistivity		$3.2 \times 10^{16} \Omega$ -cm		
Refractive Index	589 nm	1.5282		1.65
	633 nm	1.5222-1.5237		
	830 nm	1.5170-1.5187		
Optical Transmission	n (400-700 nm)	90%	>90%	>88%
Glass Transition Temperature		320°C	325°C	223°C
Thermal Expansion, Linear		7.5×10 <sup>-5</sup> /°C		$5.4 \times 10^{-5}$ /°C
Young's Modulus		1.93 GPa	2.9 GPa	
Tensile Strength		48 MPa	100 MPa	
% Elongation		10%	17%	

## Electrode Layer Materials

Because chitosan should be deposited in microfluidic channels as a template for later biofunctionalization, an electrode layer must pass under the channels to drive the chitosan electrochemical reaction. This electrode material must have a known and

consistent conductance (to enable reproducibility of reactions), should be relatively simple to pattern, and must not interfere with the solution in the microchannels. Several options are feasible: chromium-gold, indium-tin oxide, and conducting polymers.

#### Chromium-Gold

Electrodes made of chromium (a thin adhesion layer) and gold (the bulk of the electrode) are the easiest to deposit and pattern on available substrates. The exact procedure will be described later, but both materials can be evaporated onto the substrate surface and patterned using positive photoresist and the appropriate etch solutions. Some material properties of bulk chromium and gold are shown in Table 7.

Table 7. Material properties of bulk chromium and gold [25].

Material Property	Value – Cr	Value – Au
Density	$7.14 \text{ g/cm}^3$	19.3 g/cm <sup>3</sup>
Electrical Resistivity	12.7 μΩ-ст	2.2 μΩ-cm
Melting Point	1907°C	1064.18°C
Thermal Expansion, Linear	$4.9 \times 10^{-6} / ^{\circ}\text{C}$	$14.2 \times 10^{-6} / ^{\circ}\text{C}$
Poisson's Ratio	0.21	0.44
Modulus of Elasticity	279	78 GPa

Lithographically patterned thin films of gold and chromium have been found to have electrical properties within the range of the bulk materials. Sheet resistance measurements of 2000Å gold over 90Å chromium on a silicon dioxide substrate resulted in a calculated resistivity of 8.16  $\mu\Omega$ -cm [26]. On Kapton® substrates, patterned films of 2000Å gold over 90Å chromium resulted in an average calculated resistivity of 5.85  $\mu\Omega$ -cm. Both values are higher than would be expected for pure bulk gold, possibly attributable to residual photoresist or other processing uncertainties, but are lower than

the resistivity of bulk chromium and therefore can be corrected for in the electrodeposition process.

The disadvantages of using chromium-gold electrodes are twofold. First, if a totally transparent device is desired, so that reactions and depositions can be observed most easily, these opaque metallic electrodes are not suitable. Second, the desired trend is toward an all-polymer device from substrate to channels – a paradigm into which metallic electrodes certainly do not fit. These disadvantages can be removed by pursuing the more complex options described below.

#### **Indium-Tin Oxide**

Indium-tin oxide (ITO) is an alternative electrode material developed primarily for touch-screen electronics, wear-resistant glass, energy-conserving windows, and other applications for which transparent electrodes are important [27]. The material can be electron-beam evaporated or sputtered onto glass and plastic substrates [27]. Conductivity and optical transmission are competing properties in ITO and depend on the processing parameters. For example, ITO on standard microscope slides can have a sheet resistance of 8-12  $\Omega$ /square at 83% transmittance and 120-160 nm thickness, but sheet resistance increases to 70-100  $\Omega$ /square at greater than 88% transmittance and 15-30 nm thickness [28]. Because of its use in commercial applications, ITO can be purchased predeposited on glass and plastic substrates, increasing its feasibility as a possible electrode material for bioMEMS.\* While ITO would work well with polymer substrates, it is not a polymer itself and therefore suffers the same limitation as chromium-gold in the

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<sup>\*</sup> A quick internet search reveals ITO available on float glass, fused quartz, and 0.2 mm thick polyester film from SPI Supplies (http://www.2spi.com/); on 125 and 175 micron thick polyester film from Sheldahl (http://www.sheldahl.com/); and on Sumilite, a polyethersulfone based polymer, from Promerus (http://www.promerus.com/).

transition to all-polymer devices. Its transmission and availability, however, make it a material that should be explored in the future.

#### **Conducting Polymers**

The most non-traditional electrode materials – but those that may be the most important in a future of all-polymer devices – are conducting polymers. These materials have not been explored for the current work. They are, however, the source of much research in the scientific community and the subject of the Nobel Prize in Chemistry for 2000. The Nobel Prize work involved polyacetylene doped with halogens, resulting in a polymer film with conductivity only three orders of magnitude less than copper [29]. Conducting polymers are generally conjugated, meaning that the polymer backbone has alternating single and double bonds with a weaker "pi" bond [29]. Doping injects holes (locations with missing electrons) into the material, allowing charge to flow, much as in semiconductors [29]. Many conducting polymers have been developed for various applications, including polyaniline for electromagnetic shielding of electronic circuits, polythiophene derivatives for field effect transistors, and polypyrrole\* as the active layer of sensors [29]. In the trend toward an all-polymer microfluidic device, conducting polymers should soon be explored.

### Fluid Flow Layer Materials

Choosing a substrate and electrode material, despite the many options, is fairly straightforward because a wide range of properties (electrical, optical, etc.) is acceptable. For the fluid flow layer of a microfluidic device, however, material selection is critical.

<sup>\*</sup> Work on polypyrrole and other conjugated polymers continues at the University of Maryland in the Department of Mechanical Engineering under Dr. Elisabeth Smela – see http://www.wam.umd.edu/~smela/.

The properties of the fluid flow layer material determine the precision to which it can be patterned, the possible channel dimensions, its reactivity with solutions to be pumped through the microchannels, the appropriate packaging strategy, and other factors.

Although microfluidic networks in the literature are formed from many materials – glass, silicon, and various plastics – only two materials have been pursued seriously in this effort. These materials, SU-8 and polydimethyl siloxane (PDMS) can act both as the fluid flow layer and the sealing material in a microfluidic device. In both cases, the materials have been selected for their availability and ease of deposition and patterning.

#### **SU-8**

SU-8 is an epoxy-based negative photoresist developed and patented by IBM and licensed for sale by MicroChem, Inc. [30]. Using spin-coating techniques, SU-8 can be deposited to thicknesses from less than 1 micron to more than 200 microns and patterned with extremely high aspect ratios and straight sidewalls using near UV (350-400 nm) and electron beam imaging (i-line, 365 nm, is recommended) [31]. SU-8 also has high optical transparency and good chemical and thermal resistance [31]. Basic material properties of SU-8 are listed in Table 8.

Table 8. Material properties of SU-8 photo-patternable epoxy [30].

Material Property	Value
Refractive Index	1.8
Glass Transition Temperature	~50°C before exposure, >200 °C fully cross-linked
Thermal Expansion, Linear	5.2×10 <sup>-5</sup> /°C
Young's Modulus	4.02 GPa
Poisson's Ratio	0.22
Tensile Strength	34 MPa

In the current work, SU-8 is desirable because it forms a rigid and sharply defined structural material for microfluidic networks, can be deposited and patterned using standard lithographic techniques, and requires relatively low-temperature (less than 100°C) processing. It can also be used as a self-sealing material to create sealed microchannels, as will be described in a later section on SU-8 bonding. The major disadvantages of SU-8 are the time required to create a patterned SU-8 wafer (approximately 6 hours for a 130-micron-thick film), its sensitivity to thermal expansion mismatch with its substrate, and the difficulty of removing cross-linked SU-8 from its substrate.

Because SU-8 is a negative photoresist, it is patterned using a mask that blocks light in locations that should have SU-8 removed (such as microchannels). Where SU-8 is exposed to UV light, strong acid is formed during the exposure process [31]. Acid-initiated, thermally driven cross-linking of the SU-8 occurs during a post-exposure baking step [31]. After the post-exposure bake, the SU-8-coated wafer is placed in SU-8 developer (also from MicroChem, Inc.) to remove any unexposed SU-8.

#### **Polydimethyl Siloxane (PDMS)**

Polydimethyl siloxane (PDMS), a silicone elastomer\*, is an alternative material for fluid flow layers. Although it is also transparent, PDMS is quite different from SU-8: it is flexible, not rigid, and patterned by molding rather than with lithographic techniques. Some basic material properties of PDMS are given in Table 9.

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<sup>\*</sup> Sold as Sylgard® 184 by Dow Corning. See http://www.dowcorning.com/applications/product\_finder/pf\_details.asp?11=009&pg=00000029&prod=010 64291&type=PROD for product details, as of 12 April 2004.

Table 9. Material properties of polydimethyl siloxane (PDMS) [32].

Material Property	Value
Density	$0.97 \text{ kg/m}^3$
Resistivity	$4\times10^{11}\Omega$ -cm
Refractive Index	1.4
Young's Modulus	360-870 kPa
Poisson's Ratio	0.5
Tensile Strength	2.24 MPa

The flexibility of PDMS allows it to be used not only as a structural material for fluid flow, but also as the flexible complement to SU-8 for sealing purposes. Because PDMS is patterned with a mold-and-release process (see later section for procedure), patterned PDMS layers can be stacked to create a multi-layer microfluidic network. PDMS layers, as molded, create a reversible water-tight seal to most smooth surfaces (such as SU-8, glass, or plastic). They can be peeled off to allow re-use of the substrate.\* PDMS can also be treated in oxygen plasma before sealing to a smooth surface to produce a permanent seal.

PDMS, however, has a few major disadvantages that have caused SU-8 to be the primary fluid flow material in the current work. First, PDMS is strongly hydrophobic, as Figure 5 illustrates. Therefore, the flow of aqueous solutions through PDMS-defined channels is hindered rather than assisted by capillary action. The high pressures necessary to force fluid into a PDMS fluid flow layer can cause the PDMS to delaminate from the substrate, ruining the device. Second, PDMS is known to have high gas permeability, which may become a disadvantage if gases (such as from cellular

<sup>\*</sup> This property is especially important when great time and expense has been required to obtain (for example) a Pyrex substrate with patterned gold and chromium electrodes. If SU-8 is used for the fluid flow layer and something goes wrong, the SU-8 cannot be removed and the whole wafer is wasted.

metabolism) should be collected in a microchannel for sampling and characterization. Finally, the stress of the demolding process leaves PDMS fluid flow layers much less sharply defined than SU-8 fluid flow layers. Corners become rounded, and cracks show near the edges of molded features, as Figure 6 depicts.

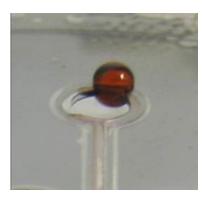


Figure 5. PDMS gasket over SU-8 fluid flow layer, with non-wetting water droplet (red) showing extreme hydrophobicity of PDMS.

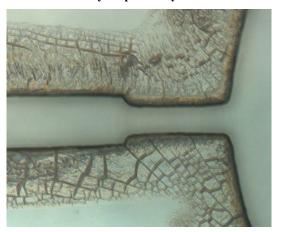


Figure 6. Microchannel defined by PDMS structure, showing stress in PDMS from demolding process. Microchannel is 100 microns wide at left and 60 microns wide at right.

In the future, it may be necessary to explore other material options for fluid flow layers beyond SU-8 and PDMS as property requirements change. Currently, however, SU-8 is the primary candidate for fluid flow layers, with PDMS used in some special cases.

# Packaging Materials

Material choice for microfluidic packaging fixtures is much less critical than for the actual microfluidic device. When choosing a packaging material, the main requirements to balance are rigidity, machinability, transparency, and cost. The packaging fixture must clamp the microfluidic wafer and hold all electrical and fluid fittings that connect the wafer to the outside world. Therefore, it must be rigid enough to hold the wafer steady, allow for many clamping "cycles," and have threads tapped into it. Machinability limits the material choices to those that can easily be cut to size and have holes tapped. Transparency is necessary to visualize fluid flow and reactions in the microchannels. If the packaging material itself is not transparent, it must be cut in such a way that the active areas of the device are visible. Finally, cost considerations require that machining the desired design into the chosen material take as little time as possible and that the bulk material itself be the least expensive option that is rigid, machinable, and transparent.

Many sturdy plastic materials are available that meet most of the requirements for packaging materials. Acrylic is transparent and readily available, but it tends to crack at threaded locations and can bow when clamped. For early packaging fixtures, acrylic was an acceptable solution. Polycarbonate is even less expensive than acrylic\* and has excellent optical clarity and rigidity; it is the best choice for transparent structural packaging materials. Recommended for its ease of machining and strength, Delrin (an acetal material) was selected for a later ring-shaped packaging fixture (so the white color did not matter).

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<sup>\*</sup> For a 12"x12"x½" sheet from McMaster-Carr, as of April 5, 2004, polycarbonate was \$19.51 and acrylic was \$33.80.

Fittings added to the packaging do not generally allow for much material choice. For example, the most readily available fluid fittings are either brass or polyvinyl chloride (PVC) plastic. The pump used requires a particular type of tubing\* for which material choices are limited to mainly silicone, Viton, and Tygon – of which silicone is the cheapest. Commercially available spring-loaded electrical fittings (pogo pins) are gold-plated nickel/silver. In the future, it may be necessary to acquire or fabricate specialty fittings (such as all Teflon and gold) to increase performance and reduce reaction of the flowing solution with the fittings. At present, however, the available fitting materials work quite well.

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<sup>\*</sup> Cole-Parmer MasterFlex L/S tubing

# **Chapter III: Microfluidic Chip Design**

Several different designs for a "chip" involving microfluidic channels and reservoirs, as well as electrodes, were fabricated to test various elements of microfluidic flow and packaging. Surprisingly, the first chip design was the most complex, a network of microfluidic pathways that tested flow combinatorially. A second design featured less complex channels, but a more complex fabrication strategy, to test the integrity of the packaging. A third design used the simplest channels that could be combined with the best-functioning packaging fixture to allow biofunctionalization of electrode surfaces.

# Combinatorial Microfluidics

The combinatorial microfluidics chip was designed with a twofold purpose. First, it has multiple test sites so that independent reactions can be carried out simultaneously or in sequence. Second, these test sites differ in subtle ways: some channels are choked (with a constriction where channel and reservoir meet), some are scaled to various widths, and some are the same size but with different electrode placement. This variation in channel design allows for a single pass of tests to determine the ideal conditions for flow, reaction, and deposition. For example, the chitosan biopolymer might only deposit in channels with widths greater than a certain value or only when the counter electrode was placed under the output reservoir. Previously unsolved questions of appropriate flow rates and electrode placement, therefore, could be answered quickly by using combinatorial techniques.

The layout of the combinatorial microfluidics wafer is shown in Figure 7.\* Red lines and circles represent fluid flow channels and reservoirs. Eight independent fluid

<sup>\*</sup> This design was created during a group brainstorming session with the bioMEMS team and formalized with the L-Edit mask design program by Michael Carrier.

test sites are pictured, each with four channels. Flow is directed from the inlet reservoirs (inner ring of eight red circles), through all four channels at once, to the outlet reservoirs shared by adjacent test sites (outer square of four red and purple circles). The letters near the outlet reservoirs indicate the configuration of the adjacent channels. "N" represents "normal," 100-micron-wide channels; "S" represents channels scaled from 10 to 200 microns in width; and "C" represents 100-micron-wide channels with a choking constriction at the outlet from 10 to 100 microns in width. The inlet and outlet reservoirs are 5 mm in diameter.

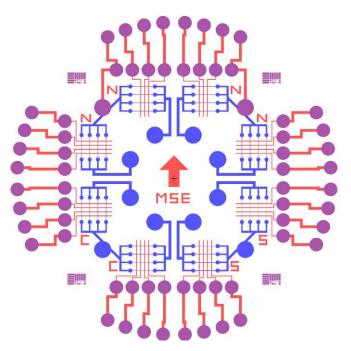


Figure 7. Combinatorial microfluidics wafer layout, showing fluid channels and reservoirs (red), electrodes (blue), and overlap of reservoirs and electrodes (purple).

Blue lines represent electrodes, four for each test site, passing under all four channels. The test sites marked "N" also have an electrode under their outlet reservoirs so that a counter electrode may be biased either in the channel or further downstream. Connections to external electrical wiring may be made either to the inner 32 purple

circles (designed to be contacted through the packaging) or to the outer 32 purple circles (designed to be contacted with alligator clips). Finally, the four purple rectangles in the corners are simply complex alignment marks to ensure proper alignment of the fluid layer to the electrodes.

This wafer design requires two masks, one to pattern the electrodes and one to pattern the fluid control layer. Masks were photo-plotted onto 0.007" high-resolution polyester film by J.D. Photo-Tools, Ltd.\* The fabrication procedure for this device is described in the following chapter.

## Micro-Knife-Edge Channels

A second major chip design was developed to account for weaknesses in the "X" and "Square" packaging fixtures described below. This design implemented the novel feature of micro-knife-edges to cause localized sealing pressure in the packaging and allow fluid to flow in the microchannels without leaking.

#### **Test Concept**

The basic concept of micro-knife-edges is shown in Figure 8. SU-8 is patterned on a substrate in two distinct layers (see double-layer SU-8 fabrication procedure below) to create a bottom layer that defines the microfluidic channels and a top layer that defines small protrusions (rectangular in cross-section) surrounding every channel-reservoir test site. A PDMS gasket is placed on top of the SU-8 wafer, creating a combination that is ready to package.

<sup>\*</sup> J.D. Photo-Tools, on the web at http://www.jdphoto.co.uk/, is a British company specializing in both film and glass masks. They provide a 2-4 day turnaround and shipping from 1-5 days. As of January 30, 2004, a 10"x12" film mask printed from a file in Gerber format (an L-Edit software option) cost \$122.40 to fabricate and \$20.40 to ship at 3-5 day speed.

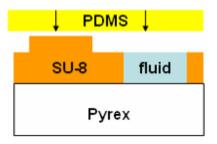


Figure 8. Conceptual drawing of the micro-knife-edge technique for sealing microfluidic channels. "Micro-knife-edge" is the rectangular protrusion of SU-8 on the side of the channel.

The micro-knife-edge technique allows a microfluidic system (channels, reservoirs, and electrodes on a patterned substrate) to be clamped in a leak-tight, waferlevel "packaging" with fluid inlets and outlets and electrical connections. Without knifeedges surrounding each channel-reservoir unit, the flexible gasket and clamping devices do not provide adequate sealing force to allow flow through the channel from inlet to The addition of micro-knife-edges to the wafer design, however, provides outlet. localized force on the gasket material close to the fluid flow path and creates a much better seal. A similar "knife-edge" seal is used at a macro-scale in vacuum systems, where a metal gasket is compressed by sharp edges on a flange to seal a vacuum chamber. The scope of the technique is for sealing of microfluidic devices when waferlevel packaging (i.e., allowing a wafer to be dropped into a packaging device immediately after processing with all fluid and electrical connections pre-set) is desired. Because of the small size of the microchannels, non-uniformities and bowing in the packaging can easily lead to leakage. However, the additional force applied to the gasket by the micro-knife-edge allows the channels to seal adequately for fluid flow to occur.

## Wafer Layout

Four different wafer layouts were designed to test the micro-knife-edge sealing technique. All of these designs were much simpler than the combinatorial microfluidics

design, since the goal was simply to achieve sealing around the microfluidic channels. These four designs were: (1) initial proof-of-concept, (2) varied channel geometry, (3) varied channel size, and (4) varied edge size.

### Initial Proof-of-Concept

The initial proof-of-concept design for the micro-knife-edge chip has the simplest channel and micro-knife-edge dimensions. Five channels are included on a 4-inch wafer with length and orientation matched to the fluid inlet and outlet fittings on the "X" and "Square" packaging fixtures described below. In this design, all channels are 500 microns wide and all micro-knife-edges are 500 microns wide and positioned 500 microns from the channel edges. Reservoir diameters are 6 mm. The two mask designs necessary for this chip are shown in Figure 9.

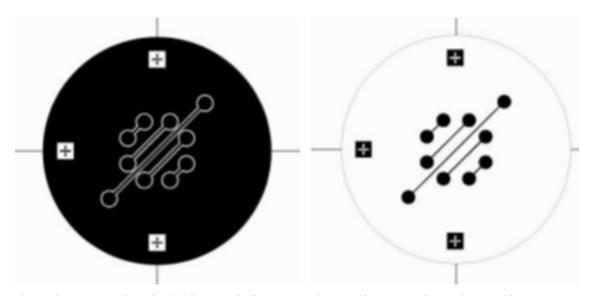


Figure 9. Mask designs for initial proof-of-concept micro-knife-edge wafer. Micro-knife-edge mask is at left, and channel mask is at right. All channels are 500 microns wide, and all knife-edges are 500 microns wide and 500 microns from channel edges.

### Varied Channel Geometry

Test chips with varied geometries and sizes were designed after the initial concept was proven with the first micro-knife-edge chip. The varied channel geometry chip also

has 6 mm reservoirs and 500-micron-wide channels with 500-micron-wide micro-knife-edges positioned 500 microns from the channel edge. Unlike the proof-of-concept chip, however, the channels are not all straight, as Figure 10 shows. The chip contains five individual test sites designed to explore flow in:

- 1. a straight channel
- 2. a T-shaped channel
- 3. a serpentine channel
- 4. a channel with a  $\sim 150^{\circ}$  bend
- 5. a channel with a 90° bend

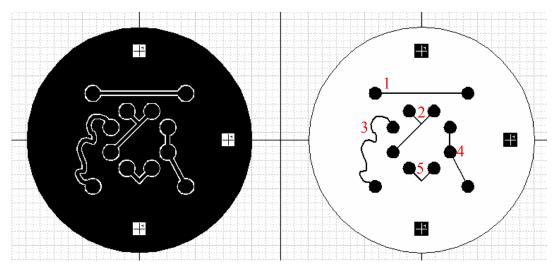


Figure 10. Mask designs for varied channel geometry chip, with micro-knife-edge mask at left and channel mask at right. Channels and micro-knife-edges are 500 microns wide.

#### Varied Channel Size

The varied channel size chip design contains five straight channels with 6 mm reservoirs and 500-micron-wide micro-knife-edges positioned 500 microns from the channel edges. Channel widths, however, are 750, 500, 300, 100, 50, and 30 microns rather than uniformly 500 microns. The mask designs for this chip are given in Figure 11.

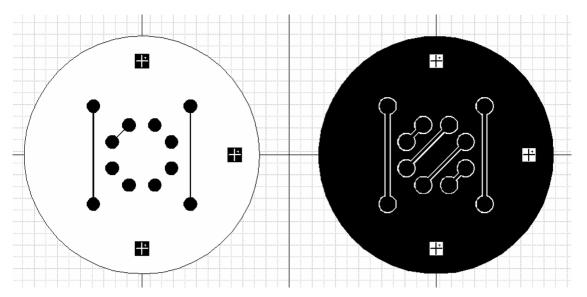


Figure 11. Mask designs for varied channel size chip, with micro-knife-edge mask at left and channel mask at right. Micro-knife-edges are 500 microns wide and 500 microns from channel edge.

Channels are scaled from 30 to 750 microns wide (30-100 micron channels not visible).

### Varied Edge Size

The varied edge size chip design was created to explore the effects of various micro-knife-edge widths and positions. In this design, each channel is 500 microns wide and each reservoir is 6 mm wide. The micro-knife-edges, however, have the following configurations:

- 1. 100 microns from channel edge, 500 microns wide
- 2. 500 microns from channel edge, 500 microns wide
- 3. 100 microns from channel edge, 100 microns wide
- 4. 500 microns from channel edge, 100 microns wide
- 5. 100 microns from channel edge, 50 microns wide
- 6. 50 microns from channel edge, 50 microns wide

The masks required for this chip design are shown in Figure 12.

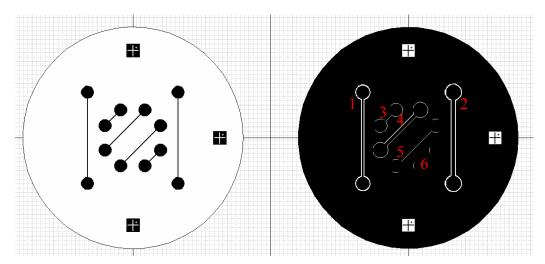


Figure 12. Mask designs for varied edge size chip, with micro-knife-edge mask at left and channel mask at right. Channels are 500 microns wide, and micro-knife-edges vary from 50 to 500 microns in width and in placement from channel edge. (Thinner micro-knife-edges not clearly visible.)

Gasket Mold Wafer

One final wafer design was necessary to complete the micro-knife-edge devices: a mold wafer to be fabricated in SU-8 on which PDMS gaskets could be patterned. In this mask design, the shrinkage of the PDMS layer on curing (approximately 1.5%) was accounted for. For each dimension (hole diameters and radial positions), the desired dimension was divided by 0.985 to yield a designed value. Desired hole diameters are 5 mm, and hole positions are at  $(\pm 20.9, \pm 20.9)$ ,  $(\pm 5.6, \pm 12.8)$ , and  $(\pm 12.8, \pm 5.6)$  millimeters from the center of the wafer. The mask design for the gasket mold is shown in Figure 13.

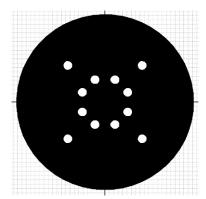


Figure 13. Mask design for gasket mold. Hole diameters and radial positions are designed to compensate for 1.5% shrinkage of PDMS on curing (e.g., hole design diameter is 5.076 mm for desired diameter of 5 mm).

# Six-Fold Symmetric Microchannels

To use with the "Ring" packaging described below, the simplest possible chip design that would allow for multiple test sites was conceived. Figure 14 shows these six identical test sites – fluid channels are shown in red, electrodes are blue, and holes for clamping in the packaging are black. Table 10 gives the dimensions of the various features on the wafer. In each channel, there are two independent electrode paths that can be used as counter and working electrodes for electrodeposition within the channels. Depending on external pump and valve configurations, a given test site can be selected and flow directed either clockwise or counter-clockwise. This chip design requires two masks, one to define the electrodes and one to define the channels.

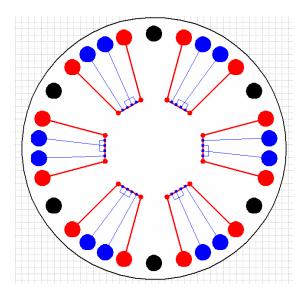


Figure 14. Wafer concept for six-fold symmetric chip design. Fluid channels are red, electrodes are blue, and packaging screw holes are black.

Table 10. Feature dimensions for six-fold symmetric chip design.

Feature	Dimension
Channel (  _  )Width	500 microns
Channel Leg (  ) Length	25 mm
Channel Base ( _ ) length	10 mm

Fluid Inlet/Outlet Reservoir Diameter	6.35
Fluid Corner Reservoir Diameter	2 mm
Large Electrode Pad Diameter	6.35 mm
Electrode Size	1 mm x 1 mm
Actual In-Channel Electrode Size	0.5 mm x 1 mm
Electrode Wire Width	100 microns

Each of the chip designs described above serves a unique purpose and is associated with a particular type of packaging fixture. The most complex, the combinatorial microfluidics chip, could not be used within the time constraints of this work but will certainly be revisited in the future to explore the effects of fluid velocity and other parameters on biofunctionalization of surfaces. The micro-knife-edge and sixfold symmetric chips allowed for successful flow in each generation of packaging fixture, as following sections will describe. Designs with greater complexity will be needed eventually to serve specific needs that arise.

# **Chapter IV: Microfluidic Chip Fabrication**

No matter the wafer design, the same procedures are generally used to fabricate microfluidic chips. The wafer must be prepared, electrodes patterned (if necessary), and a fluidic layer deposited (either of SU-8 or PDMS). Basic procedures for these steps are outlined in detail below. It is important to note, however, that film thicknesses can be changed easily by adjusting processing parameters (such as spin speed or evaporation time).

## Wafer Preparation

In general, wafers should be prepared before depositing electrode materials, patterning electrode materials, or depositing a fluidic layer, using the following process. Some plastic wafers, however, cannot withstand the acetone/methanol/isopropanol cleaning procedure and must be cleaned with pure water.

- 1. Wash the wafer in acetone over the proper waste bottle.
- 2. Wash the wafer in methanol over the proper waste bottle.
- 3. Wash the wafer in isopropyl alcohol over the proper waste bottle.
- 4. Rinse the wafer in de-ionized water.
- 5. Dry the wafer with nitrogen.
- 6. Dehydrate the wafer for 10-15 minutes on a 100°C hotplate.

## Electrode Patterning Procedure

To pattern electrodes on a wafer prior to defining microfluidic networks, the following procedure should be used.

 Deposit metal (e-beam evaporation of 90Å Cr and 2000Å Au in ECE clean room).

- 2. Clean wafer with acetone, methanol, and isopropanol; dehydrate for 10 minutes on hotplate at 100°C.
- 3. Cover wafer with HMDS primer while on spinner, wait exactly 1 minute, and spin HMDS at 5000 rpm for 30 seconds.
- 4. Apply Shipley 1813 photoresist to approximately 1/3 of the wafer and spin at 5000 rpm for 30 seconds.
- 5. Soft bake for 1 minute at 100°C on hotplate.
- 6. Expose at a dose of 150-200 mJ/cm<sup>2</sup> with i-line UV light.
- 7. Develop for 30 seconds in Shipley 352 developer and wash immediately.
- 8. Hard bake at 120°C for approximately 5 minutes.
- 9. Etch Au in Transene TFA etchant, 28Å/s (1 min 40 s works well for 2000Å).
- 10. Etch Cr in Transene 1020 etchant, 40Å/s (20 s works well for 90Å)
- 11. Remove residual photoresist by rinsing in acetone for approximately 1 minute.

### SU-8 Fabrication Procedure

SU-8 fabrication techniques form the "backbone" of microfluidic network fabrication, whether the SU-8 becomes the fluid flow layer material or the mold for a gasket or other component. For various wafer configurations, different SU-8 processing is necessary. Simple microfluidic channels or molds require single-layer SU-8; channels with micro-knife-edges demand double-layer SU-8; and sealed SU-8 microchannels necessitate SU-8 bonding. Procedures for these various techniques are outlined below.

### Single-Layer SU-8

A single layer of SU-8 is deposited and patterned using the following basic procedure:

- 1. Clean wafer with acetone/methanol/IPA if not fresh from box.
- 2. Dehydrate wafer for 10 minutes on hotplate at 100°C.
- 3. Cover the backside of any holes in the wafer with adhesive labels to prevent through-wafer leakage of SU-8. Labels will float off during development.
- 4. Cover 2/3 of wafer with SU-8 (from bottle) while wafer is on spinner.
- 5. Spin SU-8 using appropriate recipe.
- 6. Pre-bake SU-8 for appropriate time on hotplate at 95°C using a ramp of 300°C/hour; let wafer cool on hotplate for 30 min after baking.
- 7. Expose to UV light with appropriate dose.
- 8. Post-bake SU-8 for appropriate time on hotplate at 95°C using a ramp of 300°C/hour; let wafer cool on hotplate for 30 min after baking.
- 9. Develop for appropriate time in SU-8 developer, rinse wafer in fresh SU-8 developer, and let dry.

Appropriate recipes for various SU-8 thicknesses are given in Table 11.

Table 11. Recipes for SU-8 coating and patterning for three approximate thicknesses.\*

Thickness (µm)	130	~100	80
Resist Grade	SU-8 50	SU-8 50	SU-8 50
<b>Spin-Coating Recipe</b>	500/10 +	500/10 +	500/10 +
(RPM/sec.)	1000/20	1200/20	2160/20
Pre-Bake (min. at 95°C,	120	100	45
ramp 300°C/hr.)			
Exposure Dose (mJ/cm <sup>2</sup> )	1000	900	600
Post-Bake (min. at 95°C,	30	30	10
ramp 300°C/hr.)			
<b>Developing Time (min.)</b>	25	22	12

<sup>\*</sup> Based on work of Sheng Li, MEMS Sensors and Actuators Lab, UMCP; thicknesses are different from those he measured.

### **Double-Layer SU-8**

Double-layer SU-8, necessary to fabricate devices with micro-knife-edges, requires only a slight deviation from the single-layer SU-8 procedure. First, the bottom layer of SU-8 is spun on, pre-baked, and exposed following steps 1-7 in the single-layer SU-8 procedure given above. Before post-baking the bottom layer of SU-8, spin on the top layer of SU-8 using steps 4-5. Steps 6-8 are then carried out using the parameters appropriate for the top layer of SU-8. (Thus, the post-bake step of the bottom layer is performed at the same time as the pre-bake step of the top layer.) Finally, the entire wafer is developed (step 9) for a time equivalent to the sum of the times necessary to develop the bottom and top layers. Figure 15 shows a schematic of this double-layer SU-8 process.

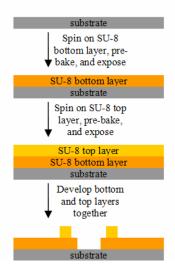


Figure 15. Processing schematic for double-layer SU-8 deposition and patterning. Pre-bake of top layer doubles as post-bake of bottom layer.

The procedure for double-layer SU-8 adds a constraint to the mask design – the top layer of SU-8 can be cross-linked only above locations on the bottom layer of SU-8 that were also already cross-linked. This constraint is caused by the UV exposure depth,

which does not cut off sharply at a depth defined by the dose but rather decays exponentially. Therefore, a bit of the bottom layer that was not previously cross-linked would be exposed to the dose from the top layer and the device dimensions would change. For example, a structure like that defined by Figure 9 is acceptable because the top layer (the micro-knife-edge mask) allows light through only in locations that already were exposed on the bottom layer (the channel mask). Figure 16 further illustrates this principle. In contrast, a solid SU-8 cover cannot be formed over unexposed channels using this procedure.

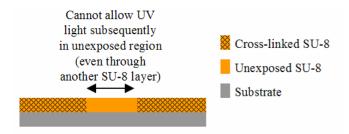


Figure 16. Illustration of double-layer SU-8 limitation because of exponential decay of UV light (rather than a sharp 100-micron exposure depth, for example).

#### **SU-8 Bonding**

A different SU-8 fabrication procedure, SU-8 bonding, allows for microchannels sealed with a layer of SU-8 (the capability that double-layer SU-8 cannot provide). This procedure was developed by Li *et al.* at the University of Maryland [3]. To perform SU-8 bonding, one wafer is first taken through a complete SU-8 process (i.e., the SU-8 is spun on, exposed, and developed to create the desired pattern). Next, SU-8 is spun on a second wafer and pre-baked. The two wafers are sandwiched together with the SU-8 sides together and joined with a bonding step that requires applied force and elevated temperature. The SU-8 on the second wafer is then exposed to UV light through the

wafer on which it was deposited, post-baked, and developed. Resulting is a sealed sandwich of SU-8 with wafers on either side, as Figure 17 shows.

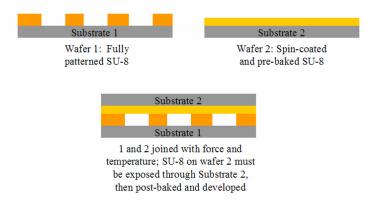


Figure 17. Schematic of SU-8 bonding process to create a "sandwich" of patterned wafer 1 and unexposed wafer 2.

The SU-8 bonding process has the advantage of sealing pre-fabricated microchannels (on wafer 1 in Figure 17) at the wafer level without applying extra gaskets and force at the packaging level. However, there are several requirements implicit in this process that may not be acceptable in the future. First, this procedure requires that the second substrate be transparent to UV light, since the second SU-8 layer is exposed through its substrate. For such purposes, Kapton and silicon are unacceptable substrates. Pyrex, acetate, and polycarbonate all allow UV transmission for SU-8 bonding but may not meet other needs of the system. Second, the SU-8 bonding process seals the two wafers irreversibly, so this technique is not suitable if the microchannels must be exposed later for characterization. Finally, it is difficult to remove air bubbles from between the sandwiched SU-8 layers, even with the assistance of air escape paths built into the first patterned SU-8 wafer. For channels located wholly within a small area of the wafer, the entire channel may be adequately sealed; however, a channel that traverses an entire wafer probably intersects several air bubbles along its path. With an appropriate UV-

transparent substrate and a reliable technique for removing air bubbles, SU-8 bonding can become a reliable procedure for sealing microchannels at the wafer level.

#### **Potential Problems and Solutions**

Two major problems can occur in SU-8 processing: thermal expansion cracking and poor adhesion. Thermal expansion cracking results from a mismatch in the thermal expansion coefficients of the SU-8 and the substrate on which it lies. High-temperature steps in the patterning procedure (pre-bake and post-bake) cause the two materials to expand to different degrees, and the stress that results causes cracking in the SU-8, especially at feature corners, if the substrate is rigid. If the substrate is flexible, the wafer will simply bend to accommodate the stresses. Figure 18 gives an example of extreme cracking with fissures approximately 50 microns long (and of unknown depth). When SU-8 is used purely as a structural material (as for microchannels or a mold master for PDMS), the cracks are small enough not to affect the performance of the material in a noticeable way. However, these cracks scatter light and could have a dramatic effect on future work on integrated SU-8 waveguides.

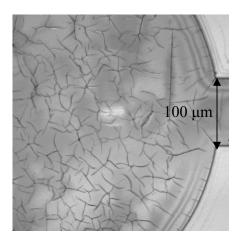


Figure 18. SU-8 structure showing extreme cracking due to thermal expansion mismatch.

Thermal expansion cracking can be minimized by ramping the temperature on processing steps as slowly as possible (300°C per hour in the current procedure), avoiding thermal shock (such as rinsing a warm wafer in cold water), and selecting a substrate with as closely matched a thermal expansion coefficient as possible. Thermal expansion coefficients for substrates (from previous tables) are compared with that of SU-8 in Table 12. Obviously, silicon and Pyrex, with thermal expansion coefficients more than an order of magnitude less than that of SU-8, are not ideal substrate materials. No current substrate material is perfectly matched, but all of the plastic substrates are much better than traditional substrates. Figure 19 shows a microchannel patterned from SU-8 on a Kapton substrate with no evidence of cracking (although the wafer did curl slightly).

Table 12. Thermal expansion coefficient comparison for SU-8 and various substrate materials.

Material	Thermal Expansion Coefficient (x10 <sup>-5</sup> /°C)
SU-8	5.2
Silicon	0.269
Pyrex	0.325
Polycarbonate	6.75
Acetate	10-15
Kapton	2

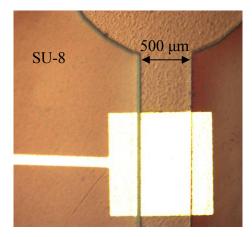


Figure 19. SU-8 channel patterned on Kapton substrate (with gold electrode under SU-8) showing no evidence of cracking.

The other potential problem with SU-8, poor wetting and adhesion, can generally be avoided with appropriate surface treatment. SU-8 adheres well to bare silicon and Pyrex substrates that have been cleaned and dehydrated. In past experiments, SU-8 also adheres well to fresh plastic substrates even without cleaning. However, fingerprints on the surface of a plastic substrate will cause SU-8 not to wet the substrate surface near the fingerprint. On silicon dioxide surfaces, SU-8 will not adhere well normally, but dehydrating the substrate for approximately an hour will improve the SU-8's adhesion. Surfaces designed to be non-wetting, such as Teflon®, will not allow SU-8 to wet the surface (although surface treatments may make wetting possible in the future). When plastic substrates curl slightly because of thermal expansion mismatch between SU-8 and substrate, the SU-8 has a tendency to peel up at the edges if the wafer is forced flat. More extended dehydration of the plastic substrate before spin-coating SU-8 should improve adhesion. Care should also be taken when flattening curled substrates to avoid as much peeling as possible.

### **PDMS** Fabrication Procedure

Fabricating a free-standing PDMS layer requires three steps: patterning a mold master from SU-8, casting PDMS on the mold master, and removing the PDMS from the mold. After the PDMS layer is removed, the SU-8 master can be re-used for subsequent PDMS layers. Therefore, only one iteration of the time-consuming SU-8 process is necessary per mold, and fabricating each PDMS layer requires only a few minutes of labor and two hours of baking.

#### SU-8 Master

The SU-8 mold master for PDMS layer fabrication uses exactly the same procedure described previously for single-layer SU-8. A silicon substrate is generally used for its rigidity and low cost. It is important to remember that the mold master mask design is the negative of a mask designed to fabricate the same features in plain SU-8 – "hills" in the SU-8 are needed to create "valleys" in the molded PDMS.

### **PDMS Molding**

To create a gasket or fluid flow layer in PDMS, the polymer is spun onto a preprepared mold and cured in a box furnace in the following steps.

- 1. Mix PDMS (Sylgard 184) in a plastic cup with curing agent in 10:1 weight ratio.
- Cover mold wafer with PDMS while wafer is on the spinner and spin PDMS
  to a height less than the mold feature height (so that holes will go through the
  layer for approximately 100 microns, spin at 200 rpm for 20 seconds,
  followed by 850 rpm for 60 seconds).
- 3. Bake wafer in box furnace for 2 hours at 70°C.
- 4. Remove wafer from box furnace, turn off furnace, and let wafer cool.

### **Demolding and Stacking**

Demolding of PDMS layers is a fairly delicate process because of the thinness of the layer and its tendency to fold over on itself when exposed to air. Keeping the mold wafer and any wafer to which the PDMS will be applied wet with methanol allows the PDMS to stay flat and manageable. To demold a PDMS wafer and stack it onto its destination wafer, this procedure is used:

- Loosen PDMS edges with a razor blade, submerge entire wafer in a dish of methanol, and pull one side of PDMS gently from wafer with tweezers until the entire layer is free. Carefully remove the mold wafer from the dish, leaving the PDMS layer floating in the methanol.
- 2. Keep PDMS layer under methanol while aligning to the destination wafer (slip wafer underneath floating PDMS layer).
- 3. Remove wafer with PDMS from methanol and check alignment under microscope (use extra methanol squirted on wafer to allow fine alignment).
- 4. Use a roller to drive excess fluid and air bubbles from the interface between the PDMS and the layer underneath. Dry wafer gently with a wiper or let dry in air.

### **Temporary and Permanent Sealing**

The demolding and stacking procedure described above results in a temporary seal between the PDMS layer and the destination wafer below, caused by van der Waals forces between the two layers. PDMS layers can be removed and repositioned if stacked in this manner (especially with the assistance of methanol). Permanent sealing of PDMS has not been attempted in the current work, but such a seal is possible by treating PDMS in oxygen plasma before attaching it to the destination wafer (for one example, see [33]).

### **Potential Problems and Solutions**

PDMS processing is desirable because of the speed with which multiple layers can be made while re-using the same mold master and because of the sealing properties of PDMS. As with SU-8, however, there are a few problems with PDMS layers, two of which can be overcome fairly easily. The first of these is the difficulty of demolding

PDMS from its master. The demolding process is not complicated and can be performed quickly after sufficient practice, but it is fairly delicate and could not be automated without a fair amount of modification. Loosening the PDMS from the master with a razor blade also results in rough edges on the released layer, which might be a problem in the future. For current small-scale operations, however, the demolding process is appropriate.

The second problem with PDMS can be referred to as the "crinkle factor," in which the ready temporary sealing of PDMS becomes a disadvantage. When exposed to air, PDMS will stick to itself if two parts come in contact. The thinner the PDMS layer, the more severe the crinkling becomes and the harder it is to untangle a balled layer without tearing it. If wafer-size (4-inch) PDMS layers must be used, the layer thickness should be at least 100 microns to reduce the likelihood of tearing the PDMS. Thinner PDMS layers should be smaller to make them easier to use.

The third and most important problem with PDMS is the extreme hydrophobicity already mentioned. When PDMS is used simply as a gasket (as with the micro-knife-edge chip design), its hydrophobic properties do not interfere strongly with fluid flow. However, an all-PDMS device could be severely limited by the hydrophobic nature of the PDMS. In the current work, no attempt has been made to increase the hydrophilicity of PDMS; the literature, however, reveals some approaches. One group found that the contact angle of water on a PDMS surface could be reduced significantly by treating the surface with hydrochloric acid (1:1 with water) for 10 minutes at room temperature [34]. This procedure, however, may contaminate microchannels for future processes. The same oxygen-plasma treatment that causes permanent sealing in PDMS can also be used

to make the surface hydrophilic, reducing the contact angle from 108° to 30° after 1 minute of oxidation in one study [35]. PDMS remains hydrophilic for only a short time (minutes to hours) after oxidation, however, unless it is submerged in water – then it remains hydrophilic for weeks [36]. Although some experiments may be compatible with this limitation, the current work is largely not, so the oxidation technique has not been pursued. In the future, it is possible that atomic layer deposition of a material on the PDMS surface may be sufficient to make it hydrophilic while maintaining its other physical properties.

#### Fabrication Results

For each of the microfluidic chip designs, wafers were fabricated using a combination of the processes described above. The following sections specify which processes were necessary to realize the designs and show images of the completed wafers.

#### **Combinatorial Microfluidics**

To fabricate chips based on the combinatorial microfluidics design, a three-step process was undertaken: (1) depositing and patterning chromium-gold electrodes, (2) fabricating an SU-8 master on a second wafer, and (3) molding a PDMS fluidic layer from the SU-8 master and applying it to the electrode wafer. Figure 20 shows the patterned electrodes on a 4-inch diameter, 500 micron thick Pyrex wafer. The SU-8 master from which PDMS fluidic layers were molded is pictured in Figure 21. The small, sharply defined features achievable in patterned SU-8 are reflected in Figure 22, which shows the SU-8 master for a channel choked to 20 microns in width at the intersection of channel and reservoir. Finally, Figure 23 shows a PDMS fluidic layer

after removal from the SU-8 master and alignment on the electrode wafer; the channel pictured is choked to 30 microns in width.

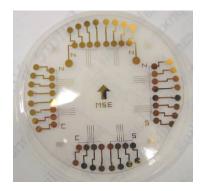


Figure 20. Au/Cr electrodes patterned on 4-inch diameter, 500 micron thick Pyrex wafer.

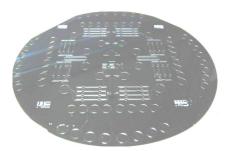


Figure 21. SU-8 fluidic layer master patterned on a 4-inch diameter, 500 micron thick silicon wafer



Figure 22. 20-micron choked channel master in SU-8 (taken with Zeiss LSM310 laser-scanning microscope). Scale bar is 500 microns.



Figure 23. 30-micron choked channel in molded PDMS over (bright) patterned gold electrode (taken with Zeiss LSM310 laser-scanning microscope). Scale bar is 500 microns.

These images reveal that the initial fabrication attempts to realize the combinatorial microfluidics chip were extremely successful. Features are well-defined and of the desired sizes. Some distortion of the PDMS fluidic layer is seen at the edges of the channels and reservoirs, caused by stress on delamination from the SU-8 master, but these cosmetic features do not interfere with the integrity of the fluid flow paths. Also, it was possible to remove a full wafer-size patterned PDMS sheet from the PDMS master and apply it intact to a prepared electrode wafer. Combinatorial microfluidics chips were also fabricated with SU-8 as the fluidic layer material; these results are not shown because of their similarity to those in the following section.

### **Micro-Knife-Edge Channels**

To fabricate chips with micro-knife-edge channels, the double-layer SU-8 process was carried out on a silicon substrate for each of the four mask designs. Figure 24 gives an example of the results, a varied-geometry chip fabricated in SU-8 on a silicon substrate. It is covered by a PDMS gasket fabricated separately on an SU-8 mold master, then demolded and stacked. The micro-knife-edges were able to surround even the most complex channels.

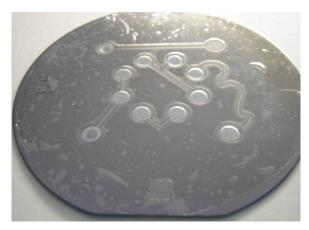


Figure 24. Varied-geometry micro-knife-edge wafer fabricated in SU-8 on a silicon substrate with a PDMS gasket on top.

To fully characterize the fabrication process, the thickness of the two SU-8 layers was determined using a Veeco optical profiling tool, model WYCO NT1100, which measures feature heights on a surface using interferometry of reflected light. A reflective surface was obtained by coating one of the micro-knife-edge chips with 100Å of chromium and 400Å of gold. The chip was designed to have 500-micron-wide micro-knife-edges positioned 500 microns outside each 500-micron-wide channel. The profile revealed that the channel and micro-knife-edge layers, processed with two different recipes, had thicknesses of approximately 130 and 80 microns, respectively. Figure 25 shows the three-dimensional profile obtained of the channel and micro-knife-edge, and Figure 26 shows a line scan from the profile in which the layer heights are visible.

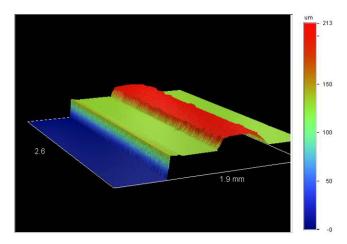
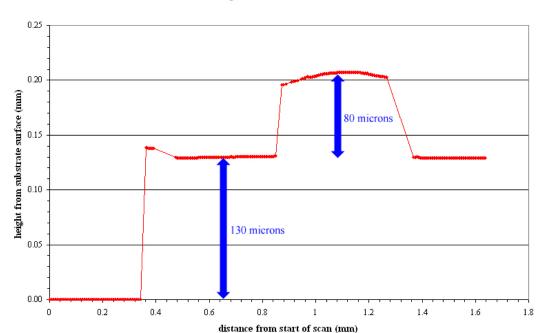


Figure 25. Veeco optical profile of channel and micro-knife-edge fabricated in SU-8.



Knife-Edge and Channel Dimensions

Figure 26. Line scan from Veeco optical profile of channel and micro-knife-edge fabricated in SU-8, showing 130-micron channel depth and 80-micron micro-knife-edge height.

The fabrication process revealed a problem inherent in the chip designs. Because of the thickness of the SU-8 layers compared to typical photoresist (100 microns versus just a few), wafers usually stick to the mask in the mask aligner (even in "separation" position) and must be aligned by hand. This limitation reduces the accuracy with which features can be aligned. Unless extreme care is taken, micro-knife-edges cannot be

designed and fabricated successfully closer than 100 microns from the edge of a channel. Figure 27 shows the varied-edge-size chip fabricated in double-layer SU-8 on a silicon substrate, revealing that the micro-knife-edges spaced only 50 microns from the channel edge were too misaligned to survive development.



Figure 27. Varied-edge-size chip with micro-knife-edges fabricated in SU-8 on a silicon substrate. Micro-knife-edges positioned 50 microns from the channel edge were too misaligned to survive the development process.

#### **Six-Fold Symmetric Channels**

To fabricate chips based on the six-fold symmetric channel design, a three-step process was undertaken: (1) depositing and patterning chromium-gold electrodes on a Kapton plastic substrate, (2) punching ¼" holes in the Kapton substrate through which the packaging screws would pass and covering the backsides with adhesive labels, and (3) depositing and patterning an SU-8 flow control layer on top of the electrodes. Appendix A shows the full procedure (with figures) for fabricating these devices. Although slight curling of the wafers was observed, the fabrication process resulted in extremely well-defined channels and electrodes. One microscope picture of these SU-8-defined channels and gold electrodes on a Kapton substrate has already been shown in Figure 19. Figure 28 shows the entire six-fold symmetric wafer – the channels are

difficult to visualize in the transparent SU-8, but they can be detected near each of the large reservoirs near the edge of the wafer.

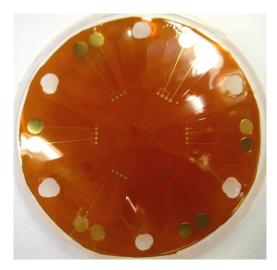


Figure 28. Six-fold symmetric channels patterned in SU-8 over chromium-gold electrodes on a Kapton plastic substrate. Holes in substrate are for packaging screws.

# **Chapter V: Microfluidic Packaging Design**

This body of work's most novel aspects lie in the design and execution of various packaging strategies to allow fluid and electrical (and eventually optical and others) connection from the macro-scale outside world to a micro-scale microfluidic chip. As was discussed in the introduction to this work, many researchers currently focus on labor-intensive, one-time strategies for connecting to microfluidic chips, such as gluing tiny tubes and o-rings to on-chip reservoirs. The packaging strategies described below, by design, are re-usable, multi-tasked (i.e., all fluid reservoirs and electrical connections are addressed with a single clamping action), and simple in design and manufacture. Each of the three packaging fixtures offers unique advantages in its design. Although designs will certainly evolve further in the future, the trend through the three basic designs has been toward greater simplicity and functionality. Common to all three designs is the external macro-scale equipment such as pumps and valves that will be described in the next section.

### External Fluid Control

In the future, ideal microfluidics chips will have valves and pumps on-chip — features that require advancements far beyond the work described here. For the packaging fixtures described in this chapter, all pumping and valve control is assumed to come from macro-scale equipment off-chip. Fluid is pumped through a single tube out of a supply container, into a valve-controlled manifold to select the correct inlet tubing, and into the packaging. Another valve-controlled manifold sends fluid from the outlet tubing back to the pump and waste container. Table 13 lists the external parts necessary for all three packaging fixtures.

Table 13. External parts list for all packaging fixtures.

Part	Supplier	Part Number*	Price <sup>†</sup>	Description
Minimatic fitting	Clippard	11752-2-PKG	\$3.45	10-32 flat bottom x 1/16" ID hose barb, 10-pack (to connect tubing to packaging)
urethane hose	Clippard	3814-7-CL-RL	\$9.15	1/16" ID clear urethane hose, no clamps needed, 50 feet (from manifold to packaging)
12-port manifold	Clippard	MAN-12	\$4.65	12 10-32 outlet ports, 1/8" pipe connection, 13/64" mounting hole, solid brass hex stock
shut-off valve (F-F)	U.S. Plastics	22121	\$6.11	1/8" NPT FxF PVC ball valve, Buna-N seal
shut-off valve (M-F)	McMaster- Carr	4757K13	\$8.58	1/8" NPT MxF easy-grip PVC mini ball valve
10-32 brass nipple	Clippard	11999-PKG	\$3.25	male-male 10-32 brass nipple, 10-pack (to connect manifold to valve)
UNF to NPT adapter	Clippard	15006-1-PKG	\$3.55	10-32 female to 1/8" NPT male adapter, 10-pack (to connect manifold to valve)
plug	Clippard	11755-PKG	\$1.60	screw plug for 10-32 holes, 10-pack (to close unused holes in manifold)
1/8" NPT to 1/16" ID adapter	Cole- Parmer	EW-06365-41	\$7.50	1/16" ID hose barb to 1/8" MNPT adapter, 25-pack (to connect manifold valves to packaging tubes)
silicone tubing	Cole- Parmer	EW-96400-13	\$23.00	L/S 13 tubing, 0.03" ID, accepts 1/16" hose barb, 25 ft. <i>(from fluid supply through pump to manifold)</i>
digital pump drive	Cole- Parmer	EW-07524-50	\$915.00	peristaltic pump, 0.1 to 6 mL/min flow rate
easy-load pump head	Cole- Parmer	EW-07518-00	\$135.00	pump head for L/S 13 or larger tubing

<sup>\*</sup> As of June 2003. † As of June 2003.

### "X" Packaging

The first packaging fixture designed – the "X" packaging – is shown in Figure 29. View A gives the top view: 12 hexagons mark the locations of the Clippard Minimatic fluid fittings (designed to match the inlet and outlet reservoir positions on the combinatorial microfluidics chip), 32 small circles mark the locations of spring-loaded electrical contacts (designed to match the positions of the inner set of electrode pads on the combinatorial microfluidics chip), and 4 large circles mark the locations of clearance holes for ½-20 screws to tighten the packaging plates. View B shows the bottom plate: 4 large circles mark the threaded holes for the clamping ½-20 screws, and a sunken hole allows wafers to align easily to the fittings in the top plate. View C gives a side view of the two plates together. Figure 30 shows the completed packaging with fittings, cut from 1-inch-thick acrylic sheet.

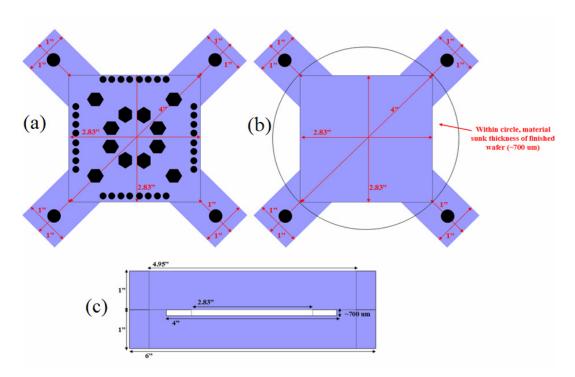


Figure 29. "X" packaging fixture design: (a) top plate with fluid (hexagonal) and electrical (small round) fittings and screws (large round), (b) bottom plate with sunken circle for wafer seating and threaded screw holes, and (c) side view.



Figure 30. Completed "X" packaging with fluid fittings and spring-loaded electrical contacts.

This first packaging attempt has, in addition to the re-usability and multi-tasking common to all packaging fixtures, a unique feature: redundancy in electrical contacts. Because of the "X" shape, the edges of the wafer are exposed, providing access by alligator clip to the outer ring of electrode pads on the combinatorial microfluidics chip. In addition, the 32 handmade spring-loaded electrical contacts integrated into the packaging fixture allow access to the inner ring of electrode pads on the chip. If one electrode pad or contact method associated with a test site becomes damaged, a second option exists to allow work on that test site to continue. Although commercially manufactured spring-loaded contacts were later found, these first contacts were designed and made in-house using the materials listed in Table 14. The Nanoport nut screws into the packaging with wire threaded through it and soldered to the Molex pin (which has a flat-sanded solder bead on its tip to provide good electrical contact). A spring between the nut and Molex pin provides the force to hold the Molex pin against the on-chip contact. Figure 31 gives a schematic diagram of the assembled spring-loaded contact.

Table 14. Parts list for handmade spring-loaded electrical contact.

Part	Supplier	Part Number*	Price <sup>†</sup>	Description
wire	McMaster- Carr	7587K56	\$5.50	26 AWG insulated stranded wire, 0.051" OD, 100 ft.
Nanoport nut	Upchurch Scientific	F-126Hx	\$51.10	6-32 coned nut, holds 1/32" OD tubing, 10-pack
spring	McMaster- Carr	9434K14	\$7.92	0.12" OD, 0.016" wire, <sup>3</sup> / <sub>4</sub> " length, 0.3" solid length, closed and ground, 5-pack
Molex pin	Digi-Key	WM1003-ND	\$5.52	0.062" family, 24-30 AWG, Molex #MO-02006-1132, 100-pack

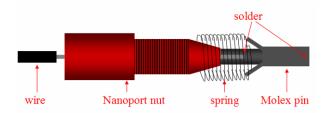


Figure 31. Schematic diagram of handmade spring-loaded electrical contact.

Results of testing this packaging fixture are discussed in the next chapter. The design alone, however, reveals some weaknesses. Because they are hand-made, the electrical contacts are not all alike, so the electrical performance of each would be slightly different. The inch-thick acrylic plates are too thick to allow interrogation of the test sites under a microscope.<sup>‡</sup> Finally, the clamping screws at each corner of the packaging are far from the active areas of the wafer, meaning that bowing of the plates might occur in the center of the packaging. These weaknesses are addressed in the second-phase "Square" packaging.

<sup>\*</sup> As of June 2003.

<sup>†</sup> As of June 2003.

<sup>&</sup>lt;sup>‡</sup> Long working-distance objectives offer working distances up to an inch or so at low magnification, which would not work well when an inch is the closest distance possible to a sample through a material not designed for optical clarity.

## Square Packaging

To allow troubleshooting of flow problems described in the next chapter, the "Square" packaging simplifies the design of the "X" packaging. The fluid fittings are in the same location, but the electrical fittings are removed for simplicity. Plate thickness is reduced to ½-inch rather than 1 inch. Instead of an "X" shape, the acrylic plates are cut simply to 5-inch squares with a ring of eight ¼-20 clamping screws just outside the wafer edge. Figure 32 shows this simplified packaging fixture.

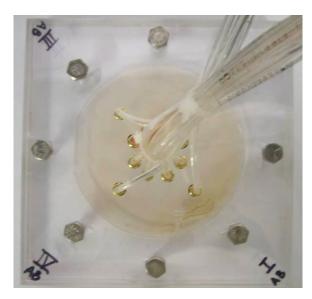


Figure 32. Completed square packaging with fluid fittings and tubing and eight clamping screws on 5" square, 1/2" thick acrylic plates.

The square packaging provides multi-tasked fluid control, but no electrical control, since its purpose is to troubleshoot flow on the combinatorial and micro-knife-edge microfluidic chips. It has the additional advantage of thinner clamping plates, allowing the entire packaging fixture to be placed under a microscope.

## Ring Packaging

Multi-tasked fluid and electrical control in a re-usable packaging are re-united in a totally redesigned third packaging phase – the ring packaging. This packaging fixture is

designed to work with the six-fold symmetric channel chip design and has four unique features not seen in previous packaging designs:

- A ring-shaped top plate that allows clear wafer access (for microscopy and other analysis) to the central three inches of the wafer,
- Dependence on package-level sealing only at the inlet and outlet reservoirs at the edge of the chip (wafer-level sealing seals all of the microchannels),
- Commercially manufactured spring-loaded electrical contacts<sup>\*</sup> for greater reliability, and
- Reliance on plastic substrates to allow packaging screws to pass through the wafer.

Figure 33 shows the overall packaging concept for the ring packaging. A ring-shaped plate on top and a circular plate on the bottom clamp a plastic wafer patterned with microchannels and electrodes. The plastic wafer must be designed with holes through which the bolts that hold the packaging together can pass. A Neoprene gasket, cut to match the holes in the top ring, lies between the top ring and the wafer to seal the fluid reservoirs at the edge of the six-fold symmetric microfluidic chip.

The drawing in Figure 33 assumes that the wafer-level sealing strategy employed is SU-8 bonding (described in the previous chapter). However, the microchannels on the plastic wafer can also be sealed by other means, including various widely available clear plastic tapes. If SU-8 bonding is not used to achieve wafer-level sealing, the sealed

<sup>\*</sup> Also known as pogo pins, these gold-plated nickel-silver contacts are a two-part assembly of probe and spring-containing receptacle. Those used were part numbers S-3-F-4-G and R-3-SC, respectively, from IDI Interconnects.

Wafer 1 is simply clamped between the two plates of the packaging fixture without Wafer 2.

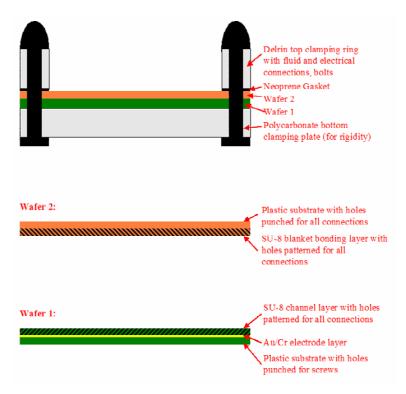


Figure 33. Packaging concept for the ring packaging showing side view of packaging fixture with wafer clamped. Wafers 1 and 2 refer to those in an SU-8 bonding process (one method of wafer-level sealing).

More detail of the top and bottom plates for the ring packaging is given in Figure 34. The top plate, a 4-inch outer-diameter and 3-inch inner-diameter ring of Delrin (a white acetal plastic), has:

• Twelve 0.096"-diameter holes\* into which the spring-loaded electrical contacts press-fit;

<sup>\* #41</sup> drill, as specified by IDI Interconnects. The receptacle end of the contact is placed in the hole, then tapped in with a soft-headed hammer to achieve a tight fit. The probe end is then inserted into the receptacle from the other side of the packaging ring.

- Twelve L-shaped holes that allow fluid to flow horizontally from 10-32 threaded fittings in the side of the packaging, then vertically to the fluid reservoirs on-chip; and
- Six clearance holes for the ¼-20 bolts that clamp the packaging together.

The bottom plate, a 4-inch circle of clear polycarbonate, simply has six clearance holes for the packaging bolts.

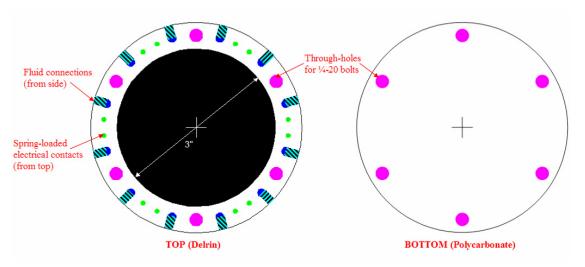


Figure 34. Schematic views of the top ring and bottom plate for the ring packaging fixture.

#### **Fabrication**

The Physics Machine Shop at the University of Maryland performed the basic cutting, drilling, and tapping steps necessary to fabricate the plates for each of the three packaging fixtures. Appropriate fittings and bolts were added later by hand.

### **Chapter VI: Iterative Results of Packaged Flow**

Because of the originality of packaging a full 4-inch wafer in a simple, re-usable, and multi-tasked fixture, the appropriate strategy for ensuring leak-tightness was not clear at the outset of the work. Therefore, the design improvements detailed in the previous chapter, as well as other configuration changes, were necessary in an iterative improvement process. Each time a leak appeared on the packaged microfluidics chip, a systematic approach ensured that the appropriate improvements were made.

# "X" Packaging

Initial experiments used the "X" packaging and the combinatorial microfluidics chip. A chip with a molded PDMS fluid flow layer was tested, followed by a chip with a patterned SU-8 fluid flow layer covered by a molded PDMS gasket (a 4-inch circle with holes located at each of the fluid reservoirs and electrode pads). Figure 35 shows the experimental setup (with pump and valve manifolds) for testing these wafers in the "X" packaging.

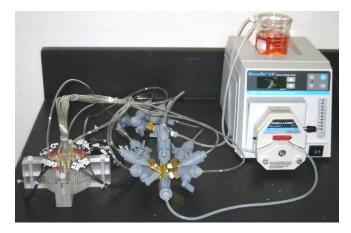


Figure 35. Experimental setup for testing combinatorial microfluidics chip in "X" packaging.

Testing with the "X" packaging showed that the external flow elements were leak-tight, but the wafer-level packaging was not. No fluid leaked as it flowed from the

supply container through the pump and valve manifold to the threaded hole in the acrylic packaging plate. Where the inlet hole in the packaging plate met the on-chip reservoir, however, fluid leaked immediately, flowing between the PDMS layer and the packaging rather than within the SU-8 or PDMS channel. Possible causes for this leakage were the chamfered holes on the underside of the top packaging plate (which may have directed flow to the sides instead of straight down to the on-chip reservoir) and a lack of localized pressure near the active channels (because of bowing of the packaging plates). At this point, the "X" packaging was temporarily abandoned in favor of the simpler square packaging.

#### Square Packaging with Gasket

The first experiments with the square packaging addressed three major problems with the "X" packaging: eight screws near the wafer were used instead of four screws on the legs of the "X," the holes in the packaging plate were not chamfered, and the gasket used was designed for the first time to accommodate the 1.5% shrinkage of the PDMS during curing. These changes, however, did not yield leak-tight flow through the channels of the combinatorial microfluidics chip. To improve the localized pressure near the active channels, the micro-knife-edge chip design was adopted.

# Square Packaging with Micro-Knife-Edges and Clamps

Once again, the micro-knife-edge microfluidic chips (fabricated in double-layer SU-8 on a silicon substrate with a PDMS gasket) did not immediately allow flow without leakage in the square packaging. However, once C-clamps were added at the center of the packaging to account for slight bowing of the packaging plates, the localized pressure was adequate to allow flow into the inlet reservoir, all the way through the channel, and

out to a waste container.\* This testing setup is shown in Figure 36. If either the clamps or the micro-knife-edges was removed, sealing could not be achieved; therefore, both elements were critical to a leak-tight packaging design.



Figure 36. Setup for testing micro-knife-edge microfluidic chips in the square packaging with C-clamps.

Figure 37 illustrates successful flow of liquid<sup>†</sup> from the inlet (left) to the outlet (right) of a 500-micron-wide, 130-micron-deep microchannel with a 500-micron-wide micro-knife-edge positioned 500 microns from the edge of the channel. The microchannels are fabricated in double-layer SU-8 on a Pyrex substrate. A similar test site on a silicon substrate is shown in Figure 38 after removal from the packaging – the residual red color in the microchannel shows that flow did proceed through the channel.

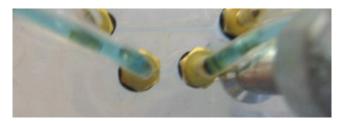


Figure 37. Successful flow from inlet to outlet (left to right) of a micro-knife-edge microchannel made of double-layer SU-8 on a Pyrex substrate. Packaging used is the square packaging with C-clamps to add force.

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<sup>\*</sup> Sealing was strongly affected by gravitational forces. For example, if the outlet tubing was directed straight up from the packaging or fluid had to travel upward to reach the waste container, the pressure required to pump the liquid upward was too great – the fluid would instead "fall back" and leak out onto the wafer. As long as vertical travel of the fluid was minimized, however, flow would continue.

<sup>†</sup> In this case, water with blue food coloring.



Figure 38. Micro-knife-edge microchannel in SU-8 on silicon substrate, covered with PDMS gasket. Residual red color in channel shows that fluid flowed through the entire channel.

After approximately ten minutes of flow (and a change in water color), some leakage was observed into the other microchannels and fittings on the wafer, as shown in Figure 39. This leakage was not (as it had been in past cases) catastrophic, and flow could continue through the channel and out of the system despite small leakage losses. For cases in which contamination of other areas of the chip is not important, and only flow through the channel in question matters, the sealing mechanism of micro-knife-edges and a well-clamped packaging is quite successful.

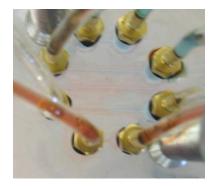


Figure 39. Continued flow from inlet to outlet (left to right) of a micro-knife-edge microchannel after fluid color is changed from blue to red. Some leakage of fluid into other microchannels and fittings is evident, but flow continues.

# "X" Packaging with Micro-Knife-Edges and Clamps

With the combination of micro-knife-edge microchannels to provide localized pressure at each channel and C-clamps to prevent bowing of the packaging fixture, successful through-channel flow was also realized in the "X" packaging. Figure 40

reveals this successful flow from the inlet tubing (far left, filled with red-colored water) to the outlet tubing (far right, partially filled with red-colored water).

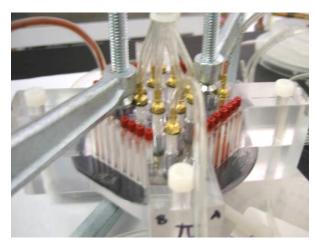


Figure 40. Successful through-channel flow of red-colored water using the "X" packaging, micro-knife-edges, and C-clamps. Inlet fitting is at far left of wafer; outlet fitting is at far right.

## Ring Packaging

Although the "X" and square packaging fixtures worked successfully once micro-knife-edges and C-clamps were added, the desire for a much simpler fixture and wafer fabrication technique, as well as for a reduction of problems caused by vertical fluid flow, drove the project toward the ring packaging. Initial efforts to achieve SU-8 bonding resulted in wafers that either did not fully bond (Figure 41) or showed significant degradation of the transparent plastic substrate caused by the SU-8 developer.



Figure 41. Six-fold symmetric microchannel wafer fabricated on two polycarbonate 4-inch substrates. Note that incomplete SU-8 bonding caused red-colored water to leak from one reservoir across the wafer.

Rather than pursuing a lengthy optimization process for SU-8 bonding with various transparent substrates, the decision was made to use other methods of wafer-level channel sealing to quickly prove the effectiveness of the ring packaging. These sealing mechanisms are short-term, but potentially very effective, solutions. Three transparent methods of wafer-level sealing were attempted: Scotch® Magic tape\*, transparent shelf paper†, and Scotch® Storage tape‡.

Scotch® Magic tape, applied to individual test sites on the six-fold symmetric microchannel chip, provides a leak-tight seal when combined with the ring packaging. However, the tape is not wide enough to cover a whole test site, so two pieces of tape must be used, and leakage occurs eventually at this interface as exposure to liquid weakens the adhesive. One test site worked without leaking for several test runs (including one under the microscope – see Figure 43), but leaked at the tape interface when re-tested approximately 30 hours later. Figure 43 also reveals the other disadvantage of Scotch® Magic tape: its matte surface reduces the quality of the microscope image viewed through it.

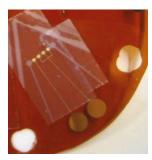


Figure 42. Microfluidic test site (single-layer SU-8 over chromium-gold electrodes on a Kapton substrate) sealed with Scotch® Magic tape.

<sup>\*</sup> A 3M product with a matte surface and a pressure-sensitive adhesive backing. Tape is 1" wide. Detailed information is available at http://www.3m.com/about3m/student/scotchbrand/scotchbrand\_index.jhtml, as of 7 April 2004.

<sup>†</sup> Also known as contact paper.

<sup>&</sup>lt;sup>‡</sup> A 3M product with a shiny surface, long-lasting adhesive, and temperature resistance. Tape is 1.88" wide.

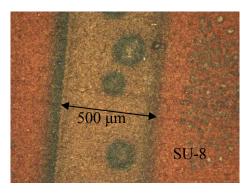


Figure 43. Bubbles visible in fluid flowing through a 500-micron-wide, 130-micron-deep microchannel in SU-8 on a Kapton substrate, sealed with Scotch® Magic tape.

Transparent shelf paper has the advantage of a large sheet size that can be cut to fit a 4" wafer and punched with holes to match reservoirs and electrode pads. (See Figure 44 for an example of a wafer with shelf-paper-covered channels.) However, the shelf paper tends to buckle at the inner edge of the packaging ring, pulling up from the SU-8 surface and creating a path for leakage. Also, the matte finish causes the same fuzzy images as the Scotch® Magic tape.



Figure 44. Microfluidic test site (single-layer SU-8 over chromium-gold electrodes on a Kapton substrate) sealed with transparent shelf paper.

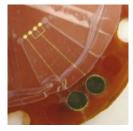


Figure 45. Buckling of shelf paper at inner edge of packaging ring creates a leakage path.

The best candidate to date for sealing the microchannels on the six-fold symmetric chip is Scotch® Storage tape. At 1.88 inches wide, the tape can seal three test sites at once and can be punched for access to reservoirs and electrode pads. In addition, the slightly glossy finish looks quite similar to the SU-8 surface and does not interfere with microscopy. When access holes are punched in the tape (rather than simply cutting the tape just inside the ring of reservoirs and electrode pads), no buckling is seen and leak-tight pumping can be achieved. No leakage was observed at either the package or wafer sealing level in 3 different test channels over 6 runs of approximately 40 minutes each (at pumping speeds ranging from 0.1 to 1 mL/min). The experimental setup for testing these channels is shown in Figure 46.

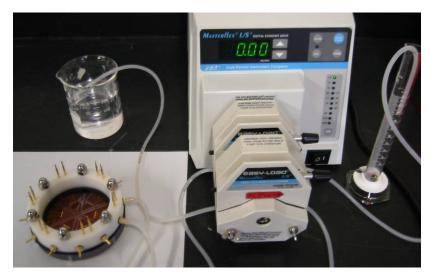


Figure 46. Experimental setup for testing six-fold symmetric microfluidics chip sealed with Scotch® Storage tape in the ring packaging fixture (bottom left).

Given that all three packaging fixtures successfully connected outside fluid and electrical sources to the micro-scale wafer level (when coupled with appropriate sealing mechanisms), it is important to characterize the flow of liquid and electricity within the on-chip channels. The following two chapters deal with these efforts at a basic level.

### **Chapter VII: Flow Characterization**

Fluid velocities and pressures in microfluidic systems control many important factors. Velocity and residence time are related to the ability of species to deposit on or react at a particular site in a microfluidic channel (i.e., whether they have enough time to react before they are pushed along by the fluid flow). Pressure may also relate to deposition and reaction and certainly controls many aspects of sealing at both the package and wafer level. So far, the microfluidic chip designs do not include flow and pressure sensors, so flow characterization depends on macro-scale control and measurement combined with simulation.

#### Macro-Scale Flow Control and Measurement

The peristaltic tubing pump employed to drive fluid into the packaging and microfluidic networks allows for macro-scale control of fluid flow rates. Rather than flow rate specifically, the user actually controls the rotational speed of the rollers that L/S periodically press the tubing, forcing fluid along. These rotational speeds are calibrated to various tubing diameters to achieve certain flow rates, and those flow rates are shown on the pump display. The pump currently in use can rotate at 1.6 to 100 rpm, resulting in the flow rates shown in Table 15. L/S 13 tubing is presently used for all experiments, so flow rates can be set from 0.1 to 6 mL/min.

Table 15. Masterflex L/S tubing sizes and possible flow rates at 1.6 to 100 rpm [37].

Tubing	<b>Tubing Inner</b>	Possible Flow	
Name	Diameter (in.)	Rates (mL/min)	
L/S 13	0.03	0.1 to 6	
L/S 14	0.06	0.4 to 21	
L/S 16	0.12	1.4 to 80	

L/S 25	0.19	3 to 170
L/S 17	0.25	5 to 280
L/S 18	0.31	6 to 380

The actual flow rate produced by the pump is not constant; rather, it pulses because of the separation of the pump rollers. Cole Parmer suggests several ways to reduce pulsation, including using a pulse dampener, using dual heads with offset rollers, and running smaller tubing at higher speeds [37]. These techniques have not yet been applied, but may become necessary in the future.

To verify that the flow rate set by the pump is correct at the macro-scale, water exiting the outlet of a packaged microfluidic chip\* was collected and measured at a pump speed of 1.0 mL/min. Excluding the first two minutes of flow, the average flow rate was exactly 1.0 mL/min. Including the first two minutes of flow, the average flow rate over six minutes was slightly higher – 1.07 and 1.1 mL/min for two different channels. Therefore, one can assume that the set flow rate is equal to the actual flow rate after a few minutes of pumping has removed any initial irregularity.

#### Flow Simulation

Fluid velocities and residence times on-chip can be calculated from the set flow rate using computer simulation. VisSim<sup>TM</sup>, by Visual Solutions Incorporated, is a simple package that allows the user to build simulations from graphical blocks rather than by writing code. Flow rate (constant throughout the system) can be converted to fluid velocity simply by dividing by the cross-sectional area of the feature through which fluid flows, since:

<sup>\*</sup> A varied-geometry micro-knife-edge chip, for both the serpentine and 90°-bend channels.

flow rate  $[cm^3/s] = cross\text{-sectional area } [cm^2] * velocity [cm/s]$ 

Cross-sectional areas are known for all features of the packaging and chip.\*

Similarly, the residence time over a particular feature (such as an electrode or an entire channel) can be calculated using the length of that feature, as in:

residence time [s] = feature length [cm] / velocity [cm/s]

Figure 47 shows the architecture of the VisSim simulation, as well as its results (fluid velocity, residence times) for a given set of parameters related to the six-fold symmetric microchannel chip. Even at the lowest flow rate possible, the speed of fluid in a small channel over a small electrode is extremely fast — only about 40 microseconds. This velocity can be tuned by changing the flow rate, as well as the dimensions of the microchannel and its features. For biofunctionalization of surfaces, as will be described later, even this lowest flow rate may therefore be too fast. In future studies, on-chip pressure and flow sensors will be critical for characterizing the actual environment in microfluidic channels.

<sup>\*</sup> For a microchannel, the appropriate cross-sectional area is the channel width times the channel depth (500 microns times 130 microns for most channels in the present work). For tubing, the inner diameter is known, so the cross-sectional area is easily calculated. For the packaging, the inner diameter of the fittings and the size of the packaging holes is known. Because this model is mainly important inside the channels and the total-circuit residence time is dominated by the inlet and outlet tubing, many features are simplified (for example, reservoirs are ignored).

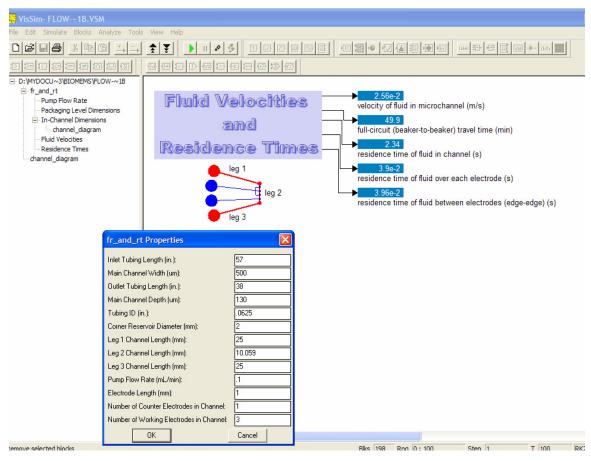


Figure 47. Architecture of VisSim simulation to determine fluid velocities and residence times, with variable values and results shown.

### **Chapter VIII: Electrical Characterization**

Electrodeposition experiments depend critically on selecting the correct current and voltage parameters. To choose the right values, it is important to know the electrical properties of the contacts and electrodes used. For patterned chromium-gold electrodes, four-point probe measurements allow determination of the sheet resistance (and thereby resistivity) of the thin film electrodes. Four-point probe measurements were taken on three different Kapton wafers, all of which had 90Å of chromium and 2000Å of gold deposited with e-beam evaporation.\* One wafer was unpatterned, and two wafers had been patterned with the six-fold symmetric electrode mask using the procedure described previously.† Voltage and current outputs from the four-point probe can be converted to sheet resistance using the equation for thin films and wafers. [38]:

$$R_s = \rho/t = 4.53 \ V/I$$

In this equation,  $R_s$  is the sheet resistance,  $\rho$  represents the bulk resistivity of the film, t is the thickness of the film, and V and I are the voltage and current, respectively. Figure 48 shows the resistivity calculated from current and voltage data taken at various points on the three wafers. Wafers 1 and 2 (the patterned wafers) show higher resistivity values than Wafer 3 (the unpatterned wafer), probably because of residual photoresist from the patterning process. The average values for both sets of data (5.8  $\mu\Omega$ -cm for patterned wafers and 3.6  $\mu\Omega$ -cm for unpatterned wafers) are higher than the pure gold resistivity of 2.2  $\mu\Omega$ -cm. Both values, however, are between the pure values for

<sup>\*</sup> Wafer structure: Kapton 500HN film (127 microns thick), then chromium, then gold on top.

<sup>†</sup> Patterned wafers may have residual photoresist despite acetone cleaning, which would increase the resistivity of the film.

<sup>&</sup>lt;sup>‡</sup> Where the film thickness is less than 5 times the probe spacing – certainly true for these thin films and typical probe spacings of 25-60 mils (6 to 15 *million* angstroms). Derivation for this equation is available in [38] as well.

chromium and gold (as discussed in Chapter II). Since the values are known, the higher resistivity of the patterned electrodes can be accounted for during electrodeposition experiments.

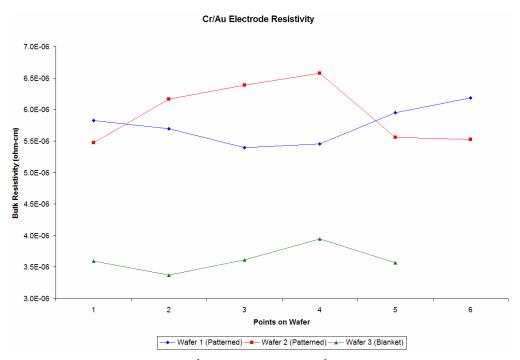


Figure 48. Calculated resistivity of 90Å chromium and 2000Å gold electrodes on Kapton substrates, based on four-point-probe measurements of current and voltage at several positions on the wafers.

Two wafers are patterned (with possible residual photoresist) and one is not.

# Packaged Electrode Properties

The total resistance of the packaging and on-chip electrode can also be measured easily with a multimeter by placing one probe at the top of a spring-loaded electrical contact<sup>\*</sup> and the other probe on a connected electrode within an unsealed microchannel. This experiment also shows that the spring-loaded contacts provide electrical continuity between the packaging and the chip. Over eight electrodes in two different test sites<sup>†</sup>, an average resistance of 43.1  $\Omega$  (with a standard deviation of 2.63  $\Omega$ ) was found. A slight

\* Here, the commercially available contacts on the ring packaging are used.

<sup>†</sup> Six-fold symmetric microfluidic chip with Kapton substrate, electrodes patterned from 90Å of chromium and 2000Å of gold, and fluid control layer patterned in 130-micron thick SU-8.

variation in resistance is to be expected, since not all electrodes have the same on-chip wire length (see Figure 14). Once fluid is introduced into the channel to complete the circuit between counter and working electrodes, the total circuit resistance will be dominated by the solution resistance; the resistances of the contacts and electrodes, however, are still important to know.

### **Chapter IX: Surface Biofunctionalization**

Though painstakingly executed, the many stages of design and testing described in the previous four chapters are but the groundwork for the exciting experiments that can be performed in leak-tight packaged microfluidic systems. Many experiments remain, but the platform on which they can be executed – the electrodeposition of chitosan to biofunctionalize a surface (described in Chapter I) – has been demonstrated in initial tests. Several experiments were performed to optimize on-chip conditions and allow deposition to occur.

## Chitosan Deposition Procedure

Once the combination of the ring packaging and a six-fold symmetric microfluidic chip sealed with Scotch® Storage tape proved leak-tight, experimentation could begin. All of the results described below, therefore, were achieved in test sites with the dimensions listed in Table 10: 500-micron-wide microchannels patterned in 130-micron-thick SU-8 on a Kapton substrate patterned with 90Å Cr / 2000Å Au electrodes. Each channel is associated with four 1.0 by 1.0 mm electrodes (one counter and three working), each with a 0.5\* by 1.0 mm area exposed to the fluid.

The chitosan solution contained 1% chitosan labeled with NHS-fluorescein and had a pH of 5.<sup>†</sup> NHS-fluorescein is a fluorescent tag that can be attached to chitosan and glows green under UV light, with an excitation wavelength of 490-495 nm and an emission wavelength of 520-525 nm (see Figure 49 for its structure) [39]. The preparation of this solution is described in [10].

<sup>\*</sup> The channel width determines the 0.5 mm.

<sup>†</sup> Solution provided by Li-Qun (Cynthia) Wu, University of Maryland Biotechnology Institute.

Figure 49. Chemical structure of NHS-fluorescein [39].

Five different experimental procedures were followed, varying parameters until successful deposition resulted with the fifth procedure. Each procedure requires that the chitosan solution flow slowly (0.1 mL/min) from the solution container, through the inlet fitting, into the channel, and out to the outlet tubing before deposition is attempted. After deposition, the inlet tubing is moved from the chitosan solution to de-ionized (DI) water to flush the channel (also at 0.1 mL/min).\* After sufficient DI water has been drawn into the inlet tubing, the end of the tubing is exposed to air so that all of the liquid can be pumped out of the channel once it is flushed. The experiment ends when the channel is as dry as possible. The full experiment takes nearly an hour because of the long residence time of the solution in the inlet tubing and fittings (as demonstrated in Figure 47).†

Table 16 lists the parameters for each of the five procedures. Procedure 5 is the most complicated. First, the channel is filled with solution, flow is stopped, and the electrodes are powered for 2 minutes. Then, the power is turned off and fluid is pumped

<sup>\*</sup> If the channel were not flushed, the entire channel would glow green in the fluorescence microscope from the fluorescently labeled chitosan solution. Removing all of the water is not as critical (fluorescence can even be more visible in wet conditions [40]), and is actually quite difficult.

<sup>†</sup> Faster flow rates may well be suitable and would reduce the total experiment time greatly. For these initial experiments, care was more important than time.

through the channel at 0.1 mL/min for 10 seconds. This power-and-flow cycle is repeated three times for a total power-on time of 6 minutes.

Table 16. Experimental procedures for chitosan deposition in six-fold microfluidic channel. Inchannel working electrode area is 1.5x10<sup>-6</sup> m<sup>2</sup>.

#	Current Density (A/m²)	Current (µA)	Flow Rate (mL/min)	Power-On Time (min)	Deposited Film?
1	2	3	0.1	2	Maybe
2	2	3	0.1	10	No
3	6	9	0.1	10	No
4	4	6	0	5	No
5	4	6	0.1 (for 10 s	2 x 3 (flow	Yes
			while not	between each 2	
			depositing)	min deposition)	

After each experiment, the chip (still packaged) was examined in a fluorescence stereomicroscope (MZ FLIII, Leica) with GFP1\* and GFP2† filters. The results of these experiments are described in the next section.

# Deposition Results

Few experiments work correctly the first time. Procedure 1 yielded the possibility of chitosan film growth, a slight difference in fluorescence was seen between the counter and working electrodes (especially the working closest to the counter electrode), as shown in Figure 50. This image was encouraging enough to try the longer deposition time of Procedure 2; if film had really been deposited, a longer deposition time should make the fluorescence more noticeable. Procedures 2 and 3 (even higher current density, which should have increased deposition), however, resulted in no noticeable difference between the counter and working electrodes. The lack of success with these procedures, all of which included flowing solution during deposition, suggested that the 40-

<sup>\*</sup> Excitation filter at 425 nm, bandwidth of 60 nm, emission barrier filter at 480 nm.

<sup>†</sup> Excitation filter at 480 nm, bandwidth of 40 nm, emission barrier filter at 510 nm.

microsecond residence time over each electrode might not be enough for the chitosan to sense the pH gradient, become insoluble, and deposit on the electrode.

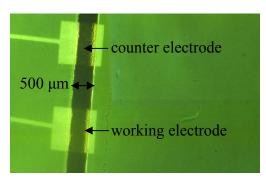


Figure 50. Fluorescence microscope image (GFP1 filter) of six-fold symmetric microfluidic chip after Procedure 1 experiment. Working electrode has slightly different color from counter electrode (chitosan should glow bright green). SU-8 is green because of intrinsic fluorescence.

To avoid residence time problems, Procedure 4 was developed to deposit chitosan in a static channel with no flow during deposition. This experiment was performed with the packaging fixture placed under the 5x objective of a standard optical microscope. During deposition, a bubble formed on the working electrode, eventually growing to cover the entire electrode, as shown in Figure 51. This bubble could have indicated chitosan deposition (since hydrogen is evolved as chitosan becomes insoluble in high pH regions), but no glow from fluorescently labeled chitosan was visible on the working electrode in a fluorescence microscope. Although it certainly removed any residence time problems with static conditions, this procedure may have gone to the other extreme, depleting the electrode region of chitosan before a noticeable film could deposit.

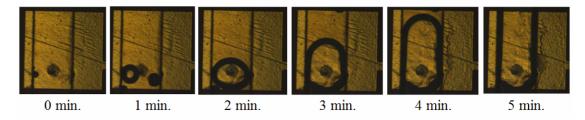


Figure 51. Bubble formation on working electrode of a six-fold symmetric microfluidic chip test site, tested using Procedure 4. Electrode is 1x1 mm, and channel is 0.5 mm wide. Flow is from bottom to top.

Procedure 5 struck a compromise between Procedures 3 and 4 with its power-and-flow cycle. Ideally, the cycle would allow a long residence time over the working electrodes during deposition in static conditions, as well as fresh solution every two minutes because of the short flow period. This experiment was also performed under an optical microscope, and Figure 52 shows the progression of optical images. As in the previous experiment, bubbles form and grow throughout deposition. In addition, areas that look slightly raised are visible after one cycle at the bottom of the electrode (closest to the counter electrode) and around the dumbbell-shaped imperfection seen in the predeposition image on the working electrode. These raised areas also grow throughout the deposition procedure.

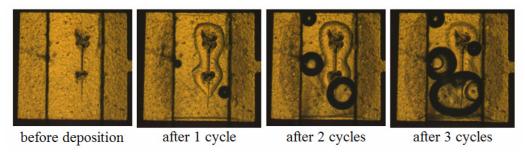


Figure 52. Chitosan deposition on one working electrode (that nearest the counter electrode) of a six-fold symmetric microfluidic chip test site, tested using Procedure 5. Electrode is 1x1 mm, and channel is 0.5 mm wide. Flow direction is from bottom to top.

The indication of deposition given by the raised areas was confirmed with fluorescence microscopy. Dramatically different fluorescence can be seen in Figure 53 between the counter and working electrodes, indicating that chitosan film deposited. The images are taken at three different magnification levels: 0.8x, 4x, and 5x.\*

<sup>\*</sup> Fluorescence is generally more noticeable at higher magnifications [40].

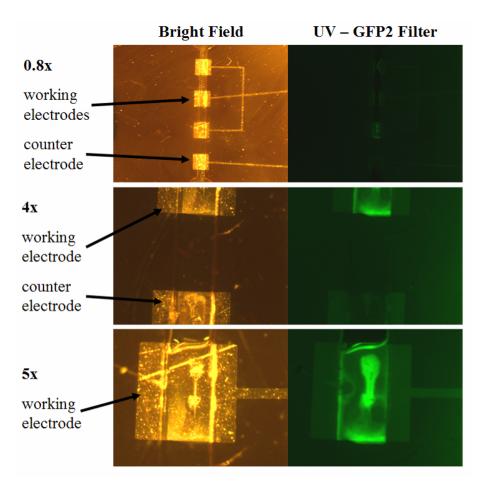


Figure 53. Images of the same six-fold symmetric microfluidic chip test site at different magnifications after chitosan deposition with Procedure 5. Electrodes are 1x1 mm, and channel is 0.5 mm wide. Flow direction was from bottom to top.

In the 0.8x image, noticeable fluorescence is visible only on the working electrode nearest the counter electrode – luckily, this is the same electrode that was monitored during deposition. It is likely that the separation between the working and counter electrodes affects the electric field, which affects the pH gradient at the working electrode, which in turn affects chitosan deposition. If the electrode separation were decreased further, deposition would likely be greater.

Another feature of note is that the brightest fluorescence is visible in the same locations that appeared raised in Figure 52. This pattern may indicate two factors that encourage film growth: (1) imperfections on the surface of the electrode (the dumbbell

shape) that may serve as nucleation sites for growth and (2) proximity to the counter electrode.

These chitosan deposition experiments are the first to join pre-established chitosan deposition techniques with packaged microfluidic chips. Success with Procedure 5 is extremely encouraging; much future work, however, is necessary to improve film quality and learn more about the deposited film.

#### **Chapter XI: Future Work**

With the groundwork of successfully packaged microfluidic chips and deposited biopolymer films, it is simple to delineate some areas of future work that would quickly add value to the project. These major areas include *in-situ* monitoring of both flow and deposition, optimization of the deposition process, characterization of the deposited films, and further biofunctionalization of the chitosan surface.

### In-Situ Monitoring

Many methods, simple and complex, can monitor solution flow *in situ* in microchannels. One of the simplest techniques is to flow water that contains microspheres of polystyrene\* or another material. Under a microscope, the microspheres move noticeably through the channel. A video of their motion can be analyzed to determine the velocity of the fluid (possibly even velocity differences between the nearwall areas and the center of the channel). On the more complex side, sensors can integrate into microfluidic chips to monitor fluid flow rates and pressures at precise on-chip locations. Research is ongoing to determine the best strategies for this integration.

Deposition of chitosan and other species in microchannels can be monitored *in situ* as well. The chitosan deposition experiments described above were performed under a standard optical microscope. If they had been performed under a fluorescence microscope, the growth of the fluorescent chitosan film would have been even easier to monitor. Additionally, integrated optics such as waveguides and sensors are being researched to allow excitation and detection of fluorescence to occur at specific on-chip

<sup>\*</sup> Polystyrene microspheres can be manufactured with a very narrow size distribution, so they are ideal for this purpose. One supplier, PolySciences, Inc., provides microspheres both in suspension and dry from 0.05 to 600 microns in size. 5mL of 10 micron spheres in a 2.5% suspension cost \$75.50 as of 9 April 2004. See catalog at http://www.polysciences.com/shop/viewCatalog.asp?dept\_id=4035.

locations rather than at the macro-scale with a fluorescence microscope. Finally, other members of the research group are currently pursuing a laser reflectivity technique that correlates the reflectivity of the electrode surface with deposited film thickness by comparing incident and reflected laser beam intensities. These techniques will allow future researchers to characterize deposition during an experiment and change parameters as necessary to improve quality without having to run an experiment and later take the chip to another laboratory for characterization.

## Process Optimization

Process optimization will be critical in the near future to improve film quality and uniformity. Although the results presented in the previous chapter showed that chitosan did deposit on the working electrode in a microchannel, the long process and film non-uniformity left much to be desired. Experiments are necessary to determine the dependence of fluid velocity on film deposition and thickness\*, channel geometry on fluid flow, and current density and other parameters on film quality. Also, the wafer fabrication process should be further optimized to make SU-8 bonding a viable option to replace the various sealing adhesive tapes.

#### Film Characterization

Just as chitosan films deposited in a two-electrode system in a beaker have been, the films deposited in microchannels must be fully characterized with standard materials-analysis techniques. Atomic force microscopy can help examine the film surface. Also, x-ray photoelectron spectroscopy and secondary ion mass spectrometry give composition data (relating to the quality of the film). The procedure for performing these analyses on

<sup>\*</sup> There must be some dependence, since constant-flowing and static experiments failed, but the experiment "in the middle" succeeded.

beaker-deposited films is already set with collaborators at the ITC-irst center for science and technological research in Italy – it need only be expanded to include microchannel-deposited films.

# Further Biofunctionalization

The most exciting bioMEMS research lies not in the optimization and characterization of chitosan films, but rather in their further biofunctionalization for actual applications. In the near future, other species will be added to the chitosan films: DNA strands, enzymes, and even cells for cell adhesion studies. The enzyme work, specifically, is interesting because particular sequences of enzymatic reactions can yield substances useful for chemical and biological sensing. Work in these areas is just beginning.

### **Chapter XII: Conclusion**

The accomplishments detailed in this work can be organized into three main categories: microfluidic chip design and fabrication, packaging design and testing, and surface functionalization. In microfluidic chip design and fabrication, the major accomplishments are:

- Three unique test site designs to allow combinatorial experiments and improve the functionality of three different packaging fixtures;
- An optimized PDMS fabrication procedure that allows for full-wafer mold release and stacked layers while accounting for material shrinkage;
- A survey of materials to determine the best substrate currently Kapton® plastic film for its electrical, thermal, chemical, and mechanical properties;
   and
- Documentation of reliable fabrication procedures not readily available previously.

For packaging design and testing, the most important achievements are:

- Three packaging fixtures, the most recent of which is re-usable, has multitasked addressing of multiple fluid and electrical connections directly to microchannels, allows for multiple test sites on a single microfluidic chip, and provides optical access to the wafer for analysis under a microscope\*;
- Leak-tight sealing in all three packaging fixtures, even for multiple experiments of approximately an hour each;

<sup>\*</sup> Packaging fixtures in the literature all have some combination of these features, but none found has all four.

- Characterization of flow rates, fluid residence times, and electrical properties of packaged electrodes; and
- A microfluidic "toolbox" of fluid and electrical fittings appropriate for a wide range of uses.

Finally, for surface functionalization, the major achievement is the successful deposition of chitosan on working electrodes within a microfluidic channel. Although much more work is necessary to improve the uniformity and repeatability of this deposition, this accomplishment links past experimental work (chitosan deposition on electrodes in beakers) to the packaging efforts and future applications in bioMEMS and chemical and biological sensing.

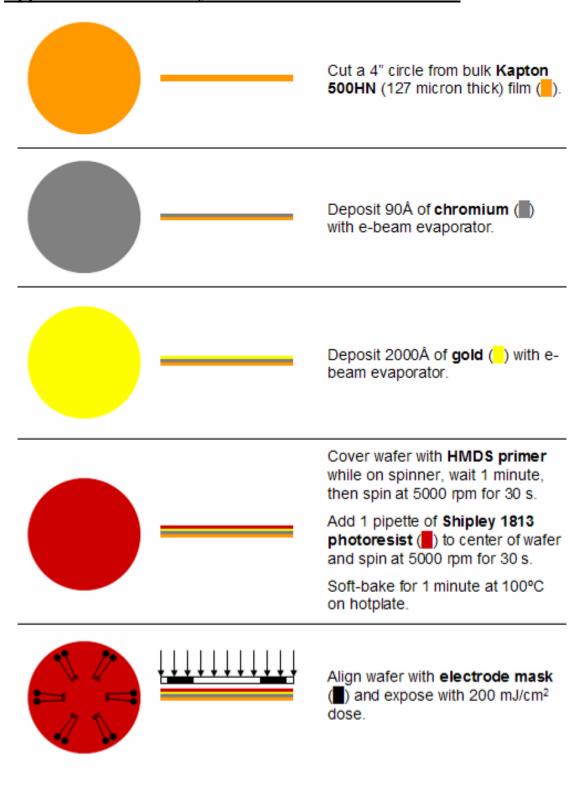
#### Intellectual Merit

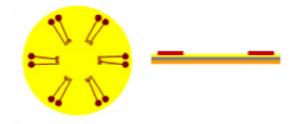
Because of the lack of attention in microfluidics research to packaging (as with microelectronics, taking packaging as an afterthought once a device is designed [2]), there is significant intellectual merit to a close study of optimizing fabrication and packaging techniques for microfluidics. In the trend toward all-polymer devices for cost reduction and disposability, the material survey undertaken here to find the best substrate for microfluidic devices (ideally polymer-based) is also quite important. Finally, the proof-of-concept of chitosan deposition in microfluidic channels provides the background knowledge necessary to design future experiments with more complicated enzyme-, protein-, and cell-based reactions.

## **Broader Impacts**

The broader impacts of this work's successes should be to provide ideas for reusable, multi-tasked packaging fixtures for bioMEMS – thus removing one of the major sources of cost and failure of MEMS devices. Additionally, the concept of biofunctionalizing the surface of a microfluidic channel will be extremely important to future studies of microfluidics (with their interesting high surface-to-volume ratio) and development of chemical and biological sensors. As has been stated previously, the efforts described here lay the groundwork for many future studies employing polymer-based microfluidics.

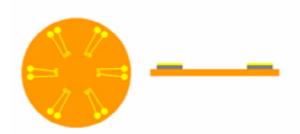
# **Appendix A: Six-Fold Symmetric Fabrication Procedure**





Develop wafer in **Shipley 352** developer for 30 s, then rinse immediately.

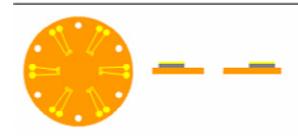
Hard-bake for several minutes at 120°C on hotplate.



Etch gold in **Transene TFA** etchant for 100 s.

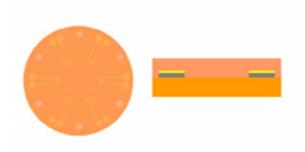
Etch chromium in Transene TFA etchant for 30 s.

Remove photoresist from gold by rinsing in **acetone** for 30 s.



Punch ¼" holes in Kapton at appropriate locations for packaging screw clearance.

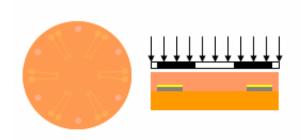
Place adhesive label over back side of each hole to prevent leakage.



Cover 2/3 of wafer with **SU-8 50** (III) that has been at room temperature for at least 2 hours.

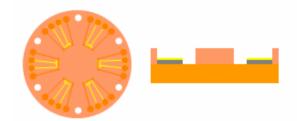
For ~130 micron thickness, spin SU-8 at 500 rpm for 10 s, then 1000 rpm for 20 s.

Place wafer on hotplate, set temperature to 95°C, and bake for 120 minutes once temperature has reached setpoint. Allow wafer to cool for 30 minutes before continuing.



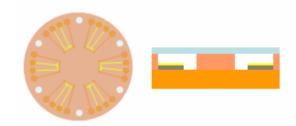
Align wafer with **channel mask**(a) and expose with 1000 mJ/cm<sup>2</sup>
dose.

Place wafer on hotplate, set temperature to 95°C, and postbake for 30 minutes once temperature has reached setpoint. Allow wafer to cool for 30 minutes before continuing.

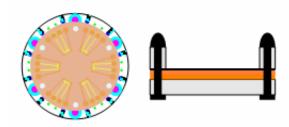


Develop wafer in **SU-8 developer** for 25 minutes on a rocking table.

Rinse in fresh SU-8 developer and allow to dry.



Apply transparent adhesive sealing film ( ) to wafer or individual test site, leaving input holes clear.



Clamp wafer in packaging, aligning to screw clearance holes, and tighten packaging bolts.

Flow fluorescently labeled chitosan solution through tubing, into channel, and back out to a collection container.

Apply appropriate current/voltage settings to deposit chitosan.

Flush with deionized water, then remove wafer from packaging for characterization.

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