ABSTRACT

Title of Document: HIGH POWER MICROWAVE INTERFERENCE EFFECTS ON ANALOG AND DIGITAL CIRCUITS IN IC'S.

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Microwave or electromagnetic interference (EMI) can couple into electronic circuits and systems intentionally from high power microwave (HPM) sources or unintentionally due to the proximity to general electromagnetic (EM) environments, and cause "soft" reversible upsets and "hard" irreversible failures. As scaling-down of device feature size and bias voltage progresses, the circuits and systems become more susceptible to the interference. Thus, even low power interference can disrupt the operation of the circuits and systems. Furthermore, it is reported that even electronic systems under high level of shielding can be upset by intentional electromagnetic interference (IEMI), which has been drawing a great deal of concern from both the civil and military communities, but little has been done in terms of systematic study and investigation of these effects on IC circuits and devices.

We have investigated the effects of high power microwave interference on three levels, (a) on fundamental single MOSFET devices, (b) on basic CMOS IC inverters

and cascaded inverters, and (c) on a representative large IC timer circuit for automotive applications. We have studied and identified the most vulnerable static and dynamic parameters of operation related to device upsets. Fundamental upset mechanisms in MOSFETs and CMOS inverters and their relation to the characteristics of microwave interference (power, frequency, width, and period) and the device properties such as size, mobility, dopant concentration, and contact resistances, were investigated. Critical upsets in n-channel MOSFET devices resulting in loss of amplifier characteristics, were identified for the power levels above 10dBm in the frequency range between 1 and 20 GHz. We have found that microwave interference induced excess charges are responsible for the upsets. Upsets in the static operation of CMOS inverters such as noise margins, output voltages, power dissipation, and bit-flip errors were identified using a load-line characteristic analysis. We developed a parameter extraction method that can predict the dynamic operation of inverters under microwave interference from DC load-line characteristics. Using the method, the effects of microwave interference on propagation delays, output voltage swings, and output currents as well as their relation to device scaling, were investigated. Two new critical hard error sources in MOSFETs and CMOS inverters regarding power dissipation and power budget disruption were found. EMI hardened design for digital circuits has been proposed to mitigate the stress on the devices, the contacts, and the interconnects. We found important new bit-flip and latch-up errors under pulsed microwave interference, which demonstrated that the excess charge effects are due to electron-hole pair generation under microwave interference. We proposed a theory of excess charge effects and obtained good

agreement of our excess charge model with our experimental results. Further work is proposed to improve the vulnerabilities of integrated circuits.

# HIGH POWER MICROWAVE INTERFERENCE EFFECTS ON ANALOG AND DIGITAL CIRCUITS IN IC'S

By

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Dissertation submitted to the Faculty of the Graduate School of the
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# Dedication

To my wife Ellie, my son Joseph, and my family for their love and support during the course of my studies.

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# Table of Contents

# List of Tables

# List of Figures

# Contributions

The followings are the contributions in this dissertation.

(A) Developed measurement technique for load-line characteristics of CMOS inverters under microwave interference.

(B) First to do systematic study of high power microwave interference on operational parameters of MOSFETs and identify vulnerabilities.

(C) Proposed new excess charge based theory for explaining the effects of the interference on MOSFETs.

(D) Identified fundamental upset mechanisms in MOSFETs and CMOS inverters.

(E) Developed a new parameter extraction method to predict the dynamic behavior of inverters under microwave interference from the DC load-line characteristics.

(F) Correlated upsets and vulnerabilities of the devices with pulsed microwave interference parameters.

(G) Showed two critical hard error sources in MOSFETs and CMOS inverters: power dissipation and power budget disruption.

(H) Showed increased susceptibilities of MOSFETs and CMOS inverters with device scaling down.

(I) Proposed EMI hardened design for digital circuits.

# Publications

## Journals

1. K. Kim and A. A. Iliadis, “Critical Upsets of CMOS Inverters in Static Operation due to High Power Microwave Interference”, IEEE Trans EMC, Vol. 49, No. 4, pp. 876-885, Nov. 2007.

2. K. Kim and A. A. Iliadis, “Impact of Microwave Interference on Dynamic Operation and Power Dissipation of CMOS Inverters”, IEEE Trans EMC, Vol. 49, Issue 2, pp. 329-338, May 2007.

3. K. Kim, A. A. Iliadis, and V. Granatstein, “Effects of microwave interference on the operational parameters of n-channel enhancement mode MOSFET devices in CMOS integrated circuits”, Solid State Electronics, 48 (10-11), pp. 1795-1799 (2004).

4. K. Kim and A. A. Iliadis, “Operational Upsets and Critical New Bit Errors in CMOS Digital Inverters due to High Power Pulsed Electromagnetic Interference”, IEEE Trans EMC, submitted, Dec. 2007.

5. K. Kim and A. A. Iliadis, “Latch-Up Effects in CMOS Inverters due to High Power Pulsed Electromagnetic Interference”, IEEE Trans EMC, submitted, Dec. 2007.

## Conferences

1. K. Kim and A. A. Iliadis, “Characterization of Latch-Up in CMOS Inverters in Pulsed Electromagnetic Interference Environments”, 2007 Int’l Semiconductor Device Research Symposium, accepted, Sept. 2007.

2. K. Kim and A. A. Iliadis, “Critical Bit Errors in CMOS Digital Inverters due to Pulsed Electromagnetic Interference”, 2007 Proc. Int’l Conf. on Electromagnetics in Advanced Applications, Torino Italy, pp. 217-220, Sept. 2007.

3. K. Kim, Y. Bayram, P. C. Chang, J. L. Volakis, and A. A. Iliadis, “High Power EMI on Digital Circuits within Automotive Structure” Proc. IEEE Int. Symp. on EMC, Vol II, pp 507-512, Aug. 2006.

4. K. Kim and A. A. Iliadis, “Degradation of Characteristics and Critical Bit-Flip Errors in Cascaded 3-Stage CMOS Inverters due to RF Interference”, Proc. 2005 International Semiconductor Device Research Symposium, Washington D.C., pp. 5-6, Dec, 2005.

5. A. Iliadis, K. Kim, and V. Granatstein, “Study of the effects of microwave interference on MOSFET devices in CMOS integrated circuits.” Proc. URSI-EMTs, Pisa, Italy, Vol II, pp. 819-821, May 2004.

6. K. Kim, A. A. Iliadis, and V. Granatstein, “Effects of microwave interference in CMOS integrated circuits.” Proc. International Semiconductor Devices Research Symposium, pp 530-531, Dec. 2003.

7. A. A. Iliadis, K. Kim, and V. Granatstein, “Effects of Microwave Interference on MOSFET Devices in Integrated Circuits”, Proc. Sixth Annual Directed Energy Symposium, Albuquerque, NM, pp. 932, Aug. 2003.

# Chapter 1: Introduction

## *1. 1 Motivation*

### Integrated circuits (IC's) are vulnerable to microwave interference.

Integrated circuits (IC's) are vulnerable to microwave interference and are expected to be more vulnerable with device scaling down [1]. Microwave interference can couple into integrated circuits and systems intentionally from high power microwave (HPM) sources or unintentionally due to the proximity to general microwave environments, and cause "soft errors" which are reversible upsets disrupting device operation without permanent damage, and "hard errors" which result in permanent damage [2]. In this dissertation we will use "microwave (MW) interference" and "electromagnetic (EM) interference" interchangeably.

### System upsets due to unintentional and intentional microwave interference have been reported.

Critical upsets in electronic systems due to unintentional and intentional microwave interference have been reported. System upsets due to unintentional interference were known to cause discharge of munitions, failure of antilock braking systems, and shut-down of defibrillators [3]. It has been also reported that portable intentional HPM sources can cause serious upsets in commercially available electronic systems from a maximum distance of 500m, and hand-held HPM units located in suitcases can cause upsets from a distance of 50m, and permanent damage at a distance of 15m [3][4]. Furthermore, a recent study have shown that such HPM sources can be built easily with microwave ovens and horn antennas [5] and be used

for criminal and terrorist purposes, which is a serious concern for both the military and civilian communities.

## Can protection prevent such upsets?

Protection in the form of shielding [6] have been considered for reducing this hazard but for high power interference, even systems under shielding effectiveness of 30dB can be upset [5] due to connecting wires, micro-slits in packaged chips, and the input/output leads of chips, as well as actual antennas for mobile communication units. It is known that 30dB shielding effectiveness corresponds to the level of shielding for the avionics in aircrafts.

## Why do systems fail under microwave interference?

Most of electronic systems now contain IC chips that consist of fundamental device units such as MOSFETs and CMOS inverters. System stability depends on the robust operation of the fundamental devices. Therefore, the reason electronic systems fail under microwave interference is that interference disrupts the operation of systems by affecting fundamental devices in IC chips. For this reason, a study of microwave interference effects on the active devices of IC's is of outmost importance to understand system level upsets.

## What are the important parameters related to microwave interference effects on active devices in IC's ?

Microwave interference induced operational upsets in the active devices in IC's may depend on the operational and physical parameters of devices. The operational parameters include currents, voltages, transconductance, gain, noise margins, operational voltages, delays, and power dissipation, and the physical parameters are

related to device size, geometry, circuit configuration, mobility, dopant concentration, and contact resistance.

### Little is known in HPM interference effects.

Little has been done in terms of systematic study and investigation of HPM interference effects on IC circuits and devices. Our understanding of EMI effects is limited to lower power levels and lower frequency [7]-[33] and thus, HPM interference induced upsets and their relation to interference characteristics are still not understood. In addition, no theory exists to predict the effects. Thus, it is of outmost interest to clarify the effects first at the device level, and then at the circuit and system levels.

## *1. 2 Objective and Approach*

### To understand the effects of high power microwave interference on the fundamental operational parameters and the physics of the basic devices in IC's.

This work focuses on the effects of high power microwave interference on the basic devices in IC's. The targeted elements are MOSFETs, CMOS inverters, cascaded inverters, and timer circuits. We concentrate on identifying the most vulnerable static and dynamic parameters of operation related to device upsets under the interference. The relation between the upsets, the characteristics of microwave interference (power, frequency, width, and period), and the device properties such as size, mobility, dopant concentration, and contact resistances are investigated based on experimental studies and theoretical analyses.

**To develop the theoretical models explaining the behavior of devices under HPM and to propose EMI hardened designs based on experimental results.**

We develop the theoretical models based on experimental results to explain the operation of devices under the interference. The prediction in the dynamic operation of integrated circuits under the interference using the models is validated with experimental results. Based on the analysis on device stress, we also propose design layouts that can mitigate the stress at the device itself, contacts, and interconnects, leading to improved susceptibility to HPM.

**For a systematic work in a controlled environment, high power microwave signals were directly injected.**

The effects of high power microwave interference depend on a number of factors such as the direction, polarization, amplitude, and waveform of radiated fields, the physical layers of IC's, the size and architecture of the chips, the packaging materials, the integrity of the seals at inputs-outputs, the size and operational parameters of the devices, and the interconnections [3]. In addition, under radiated microwave interference it is hard to know how much power is coupled to devices. This makes the prediction and analysis of such effects a complex task. Thus, to make the task simpler and clearer, it is necessary to have well-controlled environments. In this respect, we focus on direct injection of controlled microwave signal into the input and output of targeted devices and circuits, which allows us to monitor the power level of the signal. The input and the output of devices are designed to have a G-S-G (Ground-Signal-Ground) co-planar waveguide for device matching. In addition, the devices and circuits are designed as unpackaged and packaged chips with arrays of individual test

devices of different size and IC's of a high number of interconnected devices (inverters, cascaded inverters, and timer circuits). Once the effects of controlled microwave interference are characterized, the result can provide a standard metric to understand the effects of radiated field by correlating the effects under direct-injection with the ones under radiated field.

## *1. 3 Background*

### 1. 3. 1 High power microwave (HPM)

A high power microwave (HPM) signal is an intense electromagnetic signal in microwave frequency (300MHz – 300GHz) that is strong enough to cause critical upsets at electronic circuits and systems by affecting operational parameters such as current level, gain, transconductance, delays, power dissipation, and so forth. Especially, a substantial current increase induced by the strong field of the HPM signals, can result in permanent physical failures at the device contacts, metal interconnects, and gate oxide. Even less intense interference can temporarily disrupt or shutdown the operation of circuits and systems [1][3].

### A. Narrowband and ultra wideband signals

Depending on the characteristics, HPM signals can be categorized as narrowband (NB) or ultra wideband (UWB) signals. As shown in Figure 1. 1 (a), NB signals have a single frequency with pulse width and period and thus, continuous wave (CW) signals with a single frequency also can be considered as one of NB signals that has a long pulse width.

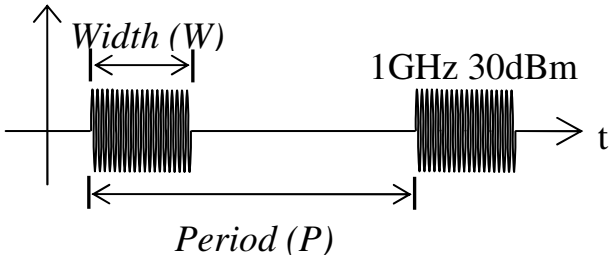



Fig. 1. 1 (a)

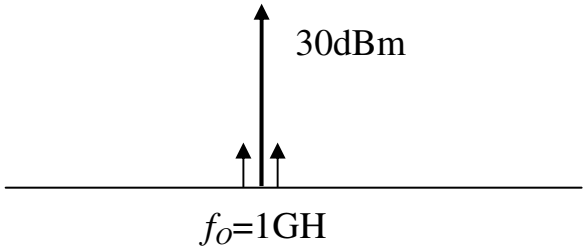



Fig. 1. 1 (b)

Figure 1. 1 (a) Schematic of an arbitrary narrowband (NB) signal with width and period in time domain. The frequency and power of the signal is chosen arbitrarily to be 1GHz and 30dBm, respectively for illustrative purpose. (b) The equivalent NB signal in frequency domain.

UWB signals shown in Figure 1. 2 (a), on the other hand, consist of a broad range of frequencies. NB signals carry all the power in the single frequency, while the power of UWB signal is distributed over wide range of frequencies as shown in Figure 1. 1 (b) and Figure 1. 2 (b), respectively [1][3]. Thus, NB signals are more dangerous one to the electronic circuits and systems because of short duration but high power. Especially, frequencies around 1GHz is known to important for HPM interference from Baum's Law [3]. From experimental viewpoint, NB signals are well defined and

easier to generate and control, allowing us more systematic study. For this reason, our work focuses on the effects of NB signals (CW and pulsed microwave signals) with frequencies around 1GHz on MOSFETs, CMOS inverters, and digital circuits.

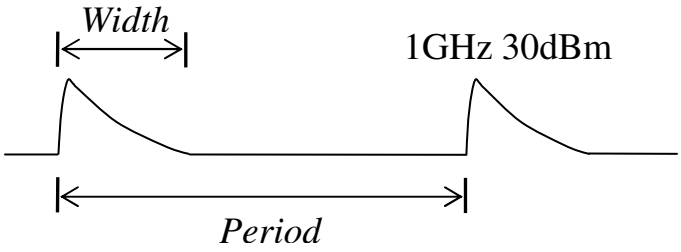



Fig. 1. 2 (a)

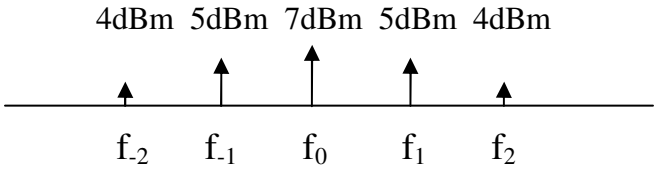



Fig. 1. 2 (b)

Figure 1. 2 (a) Schematic of a arbitrary ultra wideband (UWB) signal in time domain. (b) The equivalent UWB signal in frequency domain. The frequency and power are arbitrarily numbers for illustrative purpose.

## 1. 3. 2 Important parameters of IC's and the fundamental components in IC's

The upsets due to microwave interference fall into two regimes: "soft" reversible errors or "hard" irreversible errors. Soft errors may produce upset events where the IC systems or components return to normal operation after the interference stops or where the systems or components must be reset to return to normal operation. For

hard errors, on the other hand, the systems or components cannot return to the normal operation even after the interference due to the permanent physical failures in the components, their contacts and interconnects, or their physical characteristics [1][2]. In the following section, we further discuss about the contingent effects of the interference and upsets on the important operational and physical parameters of IC's and the fundamental components in IC's to provide background knowledge in our work in both device and system viewpoints.

## A. Important operational and physical parameters of IC's

### Size and voltage scaling

Current integrated circuits (IC's) and systems are built in small size, requiring faster clock frequency and smaller operating voltage. Thus, highly dense layouts are inevitable, which results in closely placed traces and interconnects. Thus, increased cross talk leading to IC's more susceptible to the interference is expected. Miniaturization makes the systems more susceptible to GHz range microwave interference [3]. Faster clock frequency makes the timing and synchronization between clock and data signals very tight. Thus, a little change in propagation delays can result in logic failures. With scaling down of voltage, even low power interference can disrupt system operation.

### Tight noise margins and bit errors

Smaller operating voltage in IC's would result in tight noise margins. Thus, relatively low power interference may be able to produce bit errors or significant noise, making the IC's more susceptible to disturbances.

## Delays and timing errors

Faster and tighter timing of logic signal operation in digital IC's may be another vulnerable area to the interference. Since the devices are well interconnected in IC's, even small changes in device delay under the interference may result in serious logic failure in the IC's. Thus, the investigation in the device delays due to the interference is an important topic to understand upset mechanisms in logic operation.

## Low power dissipation

Highly integrated circuits and systems require a very tight total power budget, resulting in strictly limited power consumption at each circuit unit [34]. Thus, an increase in the current of a device unit in IC's due to the interference may cause a serious disruption in total power budget distribution. Such disruption could deprive other interconnected units in the IC's from power. Therefore, entire IC's would experience logic failure or shutdown. Furthermore, the unit experiencing increased power dissipation may suffer from the increased stress on its device contacts and interconnects.

## Stress on device contacts and interconnects

Device size scaling also introduces increased contact and sheet resistance and thinner gate oxides [34]-[36]. This makes circuits more vulnerable to stress and physical failure. The stress at device contacts and metal interconnects under high power will be examined. This will allow us to establish the level of integrity of the contacts, the interconnects, and the device structure with power level and pulse duration and further provide important guidelines for a better and hardened designs.

## B. Important parameters of fundamental components in IC's

In this section we discuss probable effects of high power interference on MOSFETs and CMOS inverters. This includes the effects on DC operation, small and large signal operation, and high frequency operation, as well as junction temperature, thermal effects, gate oxide, metallization and contact.

### MOSFET devices

In the electrical characteristics of MOSFETs under the interference, current-voltage (I-V) characteristics of the devices will provide the changes in operational parameters such as output currents, transconductance, threshold voltage, output resistance, and gain. For example, interference at the gate of MOSFETs may induce current increase, thus driving the channel into deep inversion. As a result, the devices experience no pinch-off at the channel, resulting in linear relation in I-V characteristics. Furthermore, the linear relation in the I-V characteristics would cause a decrease in transconductance and gain. The reliability issues will deal with the gate oxide integrity. Under the interference, electric field can increase interface trap densities, resulting in progressively larger drift in threshold voltages and reduction in effective channel mobility. Especially, for sub-micron devices even moderate interference can produce high normal fields resulting in increased interface traps in scaled down gate oxide. Higher lateral field associated with the interference at the drain will generate hot-electrons that can be injected to the gate oxide. In addition, shorter channel will cause more impact ionization triggering avalanche breakdown and leading to catastrophic failure. Also high power delivered to the devices can introduce significantly increased channel temperature and thus, results in the decrease

in the effective channel mobility. This information will further enhance our understanding on interference effects on different types of devices. For example, SOI MOSFETs is known to prevent the latch-up effects from excess charges [37][38] due to $SiO_2$ insulator layer below the devices. However, SOI devices also suffer from self-heating due to very poor thermal conductivity resulted from the insulator layers [39]. Thus, interference induced channel temperature increase can cause a significant reduction in the output currents. Long pulses of high power can deliver enough power to raise junction temperature substantially and cause metallization peel-off and arcing. Small signal response under high power microwave including s-parameters will determine interference effects on the important frequency response parameters such as cut-off frequency.

## CMOS inverters

The CMOS inverters are the most fundamental digital circuits where an n and a p channel MOSFETs connected in parallel to provide a load and active device for the gate. Since the devices are well interconnected, the operational integrity of the inverters depends on the quiescent point of each MOSFET, the stability of load-line characteristics, the gain, and response time of each MOSFET. Thus, the introduction of an interference signal at the gate would affect the quiescent point of operation in load-line characteristics and change the voltage and current transfer characteristics, altering static and dynamic response and performance of the inverters. With scaled-down voltage, the degradation in the load-line characteristics can result in compressed noise margins which may leads to loss of noise immunity and thus, loss of signal regenerative properties in cascaded inverters. High power interference will be able to

induce more delays in logic circuits violating timing in dynamic logic operation and thus, producing glitches or bit errors. For hard errors, the study on the stress at device contacts and metal interconnects under high power will establish the level of integrity of the contacts, the interconnects, and the device structure with power level and pulse duration, and further provide important guidelines for a better and hardened designs.

### Integrated circuits

Once the results from the fundamental devices are well established, then the operational parameter changes for the different device structures can be tabulated and be used to model the effects of microwave interference power, pulse characteristics, and frequency. This study can be expanded to more complex IC's containing a higher number of interconnected devices. Thus, this will help us understand better the upset mechanism of failures at IC's.

### Protection

Different design layout may mitigate the microwave interference effects to some extend. Thus, based on the analysis on the device level, we can propose design layouts that can mitigate the stress at the device itself, contacts, and interconnects, leading to improved susceptibility to microwave interference.

## ***1. 4 Prior Work***

In this section, previous work on EMI effects on MOSFETs, CMOS inverters, and electronic circuits and systems, is discussed.

### 1. 4. 1 MOSFET devices

A previous study on RFI effects on MOSFETs only concentrated on the changes in current-voltage characteristics with microwave frequency and power. The study proposed harmonic balance simulation method combined with SPICE model to predict low power interference effects [26]. The upsets in current-voltage characteristics of MOSFETs due to the direct injection of low power RF signals with the power ranging between -5dBm to 10dBm and the frequency between 100MHz and 2GHz, has been reported. The report showed some changes in measured $I_{DS}$-$V_{DS}$ characteristics under RF injection into the gate and drain, resulting in shifting in the quiescent point of operation of the device. A simulation method based on harmonic balance simulation and SPICE model, was proposed to predict the upsets in the $I_{DS}$-$V_{DS}$ characteristics under the interference. SPICE simulation is based on time domain and small signal analysis. Thus, a great amount of time is required to simulate DC quiescent point of operation under RFI because for higher RF frequency the shorter analysis time span is required. As a result, the number of calculation increases substantially and it take to much time to get steady-state DC response. With harmonic balance simulation and SPICE model, however, the calculation can be done in frequency domain. Thus, it saves simulation time significantly for the prediction of the DC quiescent operation. However, it is difficult to apply this method for transient response simulation because numerous frequency components are necessary and thus, simulation time would greatly increase. Most importantly, simulation study cannot explain the physics of the upset mechanisms in the device operation under the interference. Therefore, it is necessary to develop a theoretical model.

### 1. 4. 2 CMOS Inverters

Previous studies on low power and frequency EMI effects on CMOS inverters have concentrated on delays, bit errors, and modeling and simulation. Delays induced by in-band low-level radiated and capacitive coupled RF interference on CMOS inverter chips were reported in [15][16]. Experimental results showed that delays were larger under in-band interference (5MHz), where interference frequency is smaller than the maximum switching frequency of the inverters. In addition, cascaded inverters suffered more from the induced delays than a single inverter did. However, delays were observed to be independent from the phase of the interference as interference frequency increased to 50MHz, which is higher than the maximum switching frequency. An experimental study reported in [14] demonstrated that RF interference (RFI) induced delays could cause critical logic failure in digital circuits.

SPICE simulation results for the prediction on the rise and fall times of logic signal in digital circuits under injected RF interference [13] showed linear dependence of rise time increase and fall time decrease with interference power. It was also found that such changes in the rise and fall times became larger as interference frequency increased from 100MHz and 220MHz. Based on simulation results, possible upset scenario in microprocessor due to RFI induced rise and fall time changes was discussed.

SPICE simulation study on the bit error rate (BER) of CMOS inverters due to RF interference with peak voltage of 2.5V and frequencies of between 100MHz and 5GHz was reported in [40]. The study showed that BER increases as interference

frequency is close to legitimate pulse signal frequency (100MHz). An experimental study on the susceptibility levels of TTL and CMOS inverters to radiated high field microwave signals, was reported in [41]. The susceptibility levels in terms of breakdown threshold (BT) and destruction threshold (DT) ranged from 55 to 108 kV/m, and among 10 different inverter devices, advanced TTL-compatible inverters were the most susceptible to the EMI. Susceptibility levels causing static logic failure in CMOS inverters were investigated in [19] using harmonic-balance simulation and SPICE models, and the critical RF power levels causing upsets were identified. Although this is valuable information, it does not establish a relationship between the operational parameters and the EMI-induced upsets.

An empirical model based on the small signal parameters such as intrinsic and extrinsic capacitance and inverter gate conductance was proposed in [16] to predict delays induced by in-band RFI as shown in Figure 1. 3. From the model, it is found that worst case delays occur when the interference is capacitively coupled.

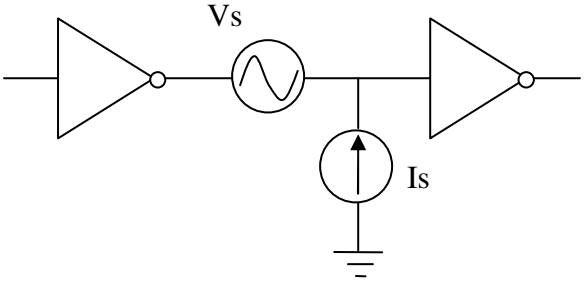



Fig. 1. 3 (a)

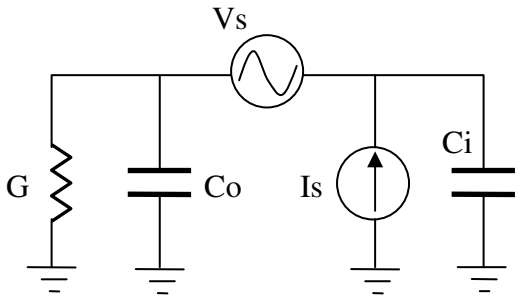



Fig. 1. 3 (b)

Figure 1. 3 (a) Schematic of cascaded CMOS inverters with voltage (Vs) and current (Is) sources from radiated RF interference coupling. (b) Schematic of equivalent

small signal model representing intrinsic and extrinsic capacitance and inverter gate capacitance.

Tront [13] proposed SPICE2 simulator to predict the rise and fall times of logic signal in digital circuits under injected RF interference.

Laurin et al presented a simulation method allowing us to predict effects of radiated RF interference on digital circuits by combining a linear electromagnetic momentum method model for wire structure with non-linear SPICE circuit model for digital gates [19]. The static operation of CMOS inverters under radiated RFI was obtained using the simulation models run on frequency domain harmonic balance simulator (LIBRA), and the dynamic operation under radiated RFI was obtained using time domain SPICE simulator. Because of the limitation in the maximum number of harmonic frequencies (10), the harmonic balance simulation cannot be applied for the IC's with high number of gates. In addition, increased number of harmonic frequencies will result in significantly increased simulation time. SPICE simulator used for simulation in dynamic operation is not suitable for high power interference because SPICE is based on small signal analysis. For high frequency interference, SPICE simulator will also suffer from substantial amount of simulation time. Therefore, the simulation tool can be used for limited case such as low power and low frequency interference effects, which makes it not suitable for simulating high power interference effects.

Bayram et al presented a novel simulation method consisting hybrid s-parameter matrix and HSPICE allowing us both time domain and harmonic balance analysis. Especially, hybrid s-parameter matrix allows us to model coupling of plane wave to

circuit board ports. However, it was observed that the method did not provide accurate prediction for high power interference, and it is believed to be due to HSPICE could not provide accurate prediction for high power interference (35dBm) [42].

### 1. 4. 3 Other Digital Circuits

State changes at digital counter clock network circuit under pulsed RF interference was reported in [43][44]. An experimental study on the susceptibility levels of modern electronic equipments such as TTL logic gates, CMOS logic gates, microcontroller, and PC network devices under radiated high power microwave interference, has been reported [41]. Such studies, however, did not provide a fundamental understanding of how the upsets occurred and thus, strongly expressed the need for in-depth investigation to understand the upset mechanism in the system.

## *1. 5 Detailed Experimental Approach*

### 1. 5. 1 Device design and measurement setups

For our work, MOSFETs, CMOS inverters, and digital timer circuits are designed and fabricated as packaged and unpackaged chips based on micron and sub-micron technologies. Inverter units are also designed as individual units and cascaded two or three inverters. For on-chip measurements at a coplanar probe station, the input and output of each unit is designed to have a G-S-G (Ground-Signal-Ground) configuration with 150μm pitch [45]. Unpackaged and packaged chips have arrays of individual devices in different size for measurement under microwave interference.

### 1. 5. 2 MOSFETs

For MOSFETs, we study the effects of CW microwave signal at the gate and drain and evaluate the changes in the operational parameters such as current-voltage characteristics ($I_{DS}$-$V_{DS}$ and $I_{DS}$-$V_{GS}$), transconductance, s-parameters, and small signal capacitances with microwave power and frequency. Upsets due to the loss of saturation, current increase, gain decrease, gate oxide breakdown, avalanche breakdown, and device burn out are investigated based on the experiments and theoretical analyses. The study also includes microwave frequency effects on MOSFETs with s-parameter measurements and small signal capacitance analysis. Based on the observation and results, an excess charge model is developed. The model accounts for physics of charge creation and transportation under microwave interference.

### 1. 5. 3 CMOS inverters

For CMOS inverters, the operational upsets and bit errors due to CW and pulsed microwave interference are studied. The study focus on identifying the upsets in the static and dynamic operational parameters such as output voltage, static and dynamic power dissipations, noise margins, load-line characteristics, gain, and propagation delays. We also investigate bit-flip errors, thermal and charge effects, and stress on device contacts and interconnects with pulsed microwave interference.

### A. Upsets in static operation

For the effects on the static operation, we measured the voltage and current transfer characteristics, the input/output voltages, the noise margins, the static power dissipation of individual and cascaded inverters. Load-line characteristics with respect

to input voltage were measured to identify upset mechanisms in the static operation due to degradation in the quiescent point of operation.

## B. Upsets in dynamic operation

For the upsets in dynamic operation, we develop a parameter extraction method allowing us to predict the output currents and voltages of inverters when legitimate input pulse is subjected to CW microwave interference. Using parameter extraction method, we investigate CW microwave effects on dynamic operation of the inverters such as output voltage swings, switching output currents, delays, and dynamic power dissipation. By comparing the dynamic operational parameters of 0.5μm inverters with the ones of 1.5μm inverters, relation between the susceptibility of the inverters to microwave interference and device scaling are studied. Using parameter extraction method and SPICE simulation, upsets in timer circuits due to CW interference injected into the clock port of the circuits are predicted and the predicted results are compared with measured results.

## C. Pulsed microwave interference effects on CMOS inverters

With pulsed microwave interference, we focus on the upsets in the inverters that are different from the ones under CW interference, and how such upsets are related to the characteristics of the pulsed interference such as the peak and average powers, the width, and the period. We measure voltage and current characteristics with single inverters in different size and cascaded inverters. Based on experiment results under CW and pulsed microwave interference and calculated effective mobility, the relative importance and contribution of thermal and charge effects to the upsets is discussed. Stress on the device contacts and metal interconnects are evaluated using voltage

current measurements under microwave interference. A microwave interference hardened design is proposed and evaluated by examining stress on the contacts. In cascaded inverters, latch-up effects [46] turning on parasitic p-n-p-n structures in CMOS devices due to pulsed microwave, is investigated.

## *1. 6 Organization*

This work is organized as follows. Chapter 2 describes the experimental study of CW microwave interference on micron and sub-micron n-channel enhancement mode MOSFETs. We investigate device upsets by examining current characteristics, tansconductances, threshold voltages, s-parameters, and small signal capacitances. We discuss microwave power effects and their relation to microwave frequency and small signal capacitances.

Chapter 3 discusses upsets in the static operation of 1.5μm and 0.5μm CMOS inverters under CW microwave interference. We first measured the voltage and current transfer characteristics of the inverters under the interference and identified a significant degradation in the output voltages and currents, leading to severe noise margin compression and static power dissipation increase. Using a simple model, we discuss imbalanced current driving capabilities of MOS devices in the inverters under the interference. The fundamental upset mechanisms are explained based on measured load-line characteristics.

Chapter 4 presents the impact of CW microwave interference on the dynamic operation of 1.5μm and 0.5μm CMOS inverters. We develop an analytical parameter extraction method allowing us to predict dynamic operation of the inverters under the

interference from experimentally measured load-line characteristics. Based on the method, the dynamic operational parameters of the inverters such as output voltage, output short circuit currents, propagation delays, and dynamic power dissipation are extracted, and we evaluate the impact of the interference on the parameters and investigate their relation to device scaling.

Chapter 5 discusses the effects of pulsed microwave interference on 1.5μm and 0.5μm CMOS inverters. We identified bit-flip errors from output logic high ($V_{OH}$) to low ($V_{OL}$) under pulsed microwave interference, and the relation between bit-flip error rates, the characteristics of pulsed microwave signals, peak power, and device size is studied. Relative importance of thermal and charge effects at the output currents of the inverters are investigated using measured current characteristics and calculated effective channel mobility of MOSFETs in the inverters. We discuss the effects of peak power of pulsed microwave signals when the average power is the same by investigating the output voltages and currents. An EMI hardened inverter design is proposed. The effectiveness of the design is evaluated by comparing the stress on the device contacts and interconnects under the interference with the stress of other inverter design. Latch-up effects in the inverters under pulsed microwave interference is also presented.

Chapter 6 deals with the development of the theory and model to predict the operation of the devices under the interference. We develop the theory based on an excess charge transport model and correlate it with experimental results and observations, allowing a better understanding of the upset mechanisms in MOSFETs and CMOS inverters.

Chapter 7 provides the conclusions that can be drawn from this work. The understanding of upsets in MOSFETs and CMOS inverters under microwave interference signals is discussed.

And in Chapter 8 the future work is discussed.

# Chapter 2: Effects of High Power Continuous Wave (CW) Interference on n-Channel Enhancement Mode MOSFET Devices

In this chapter, the effects of CW microwave interference on the operational parameters of individual micron and sub-micron n-channel MOSFET devices, is studied. In order to investigate the effects, we measure and extract the operational parameters characterizing MOSFETs as an analog circuit such as current-voltage characteristics ($I_{DS}$-$V_{DS}$ and $I_{DS}$-$V_{GS}$), transconductance ($g_m$), output resistance ($r_O$), s-parameters, and small signal capacitances with and without the interference, and identify most important device operational parameters and microwave signal properties responsible for device upsets.

The work focuses here on measuring the current-voltage characteristics ($I_{DS}$-$V_{DS}$ and $I_{DS}$-$V_{GS}$), the transconductance ($g_m$), the threshold voltage ($V_{TH}$), the output resistance ($r_O$), and the gain. Furthermore, the cut-off frequency ($f_T$) which defined as the frequency where ac current gain is unity, the S-parameters, and the small signal intrinsic capacitances. In order to provide a background knowledge regarding these parameters, the physical structure and device operation are introduced briefly. A typical n-channel enhancement mode MOSFET has a heavily doped n-type source and drain and a p-type substrate (Figure 2. 1). A thin silicon dioxide ($SiO_2$) layer is grown over the substrate between the source and drain and a conductive polysilicon gate covers the silicon dioxide layer. MOSFETs have three operational modes: cut-off, triode, and saturation. When the voltage between the gate and source ($V_{GS}$) is 0V and the source and body is tided together, the source and drain are separated by back-to-

back pn junction resulting in about $10^{12}\,\Omega$. As $V_{GS}$ increases, positive charges at the channel under the gate oxide ($SiO_2$) are repelled, leaving negative acceptor atoms behind. This is a depletion layer. Further increase in $V_{GS}$ starts to draw electrons from the heavily doped n-type source and drain, and when the surface potential reaches twice the Fermi potential ($\phi_f$), a thin layer of electrons called inversion layer is formed in the depletion layer directly under the oxide.

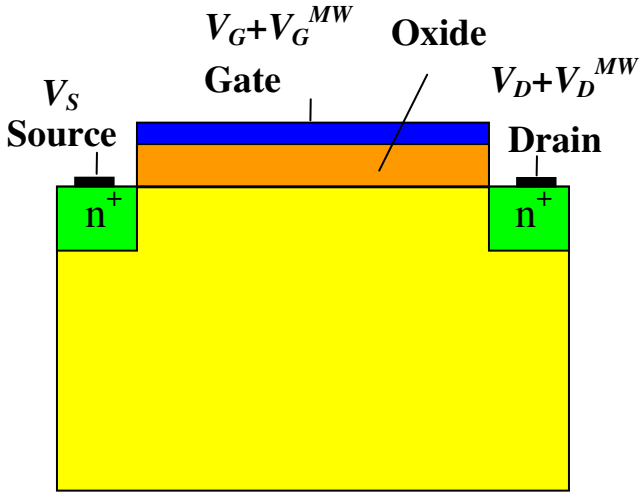



Figure 2. 1 Schematic of n channel enhancement mode MOSFETs.

When $V_{GS} > V_{THn}$, inversion occurs and conducting channel exists. The channel conductivity depends on the vertical electrical field, thus $V_{GS}-V_{THn}$. The horizontal electric field by $V_{DS}$ causes the current from the drain to the source to flow as given in Equation 2. 1. This is called triode.

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left[2(V_{GS} - V_{THn})V_{DS} - {V_{DS}}^2\right] \qquad V_{DS} < V_{GS} - V_{THn} \quad (2.\ 1)$$

where, $I_{DS}$ is the drain current, $V_{GS}$ is the gate-source voltage, $V_{DS}$ is the drain-source voltage, $C_{ox}$ is the gate oxide capacitance ($C_{ox}= \varepsilon_{ox}/t_{ox}$), $\mu_n$ is the electron mobility, $V_{THn}$ is the threshold voltage, W is the width of the device, L is the length of the device, $\varepsilon_{ox}$ is the dielectric constant of oxide, and $t_{ox}$ is the thickness of the oxide. $V_{DS}$ appears as a voltage drop across the channel, from 0V at the source to $V_{DS}$ at the drain. As $V_{DS}$ increases, the induced channel narrows at the drain edge, and eventually the channel at the drain edge no longer exists when $V_{DS} > V_{GS}-V_{THn}$. This is pinch-off. When pinch-off occurs, the drain current only depends on $V_{GS}$. However, in practice as $V_{DS}$ increases, the effective channel length decreases due to the increased depletion layer at the drain edge. This channel length modulation results in a current increase with drain voltage as given in Equation 2. 2. This is saturation.

$$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}\left(V_{GS} - V_{THn}\right)^2\left[1 + \lambda\left(V_{DS} - V_{GS} + V_{THn}\right)\right] \qquad V_{DS} \geq V_{GS} - V_{THn} \tag{2. 2}$$

where, $\lambda$ is the channel length modulation parameter. There are three important parameters characterizing small signal operation: transconductance ($g_m$), output resistance ($r_O$), and cut-off frequency ($f_T$).

The transconductance and output resistance of MOSFETs are given in Equation 2. 3 and 2. 4, respectively. These parameters are related to the gain of MOSFET amplifiers as shown in Equation 2. 5.

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_{V_{DS}} \quad (2.\ 3)$$

$$r_O = \left.\frac{\Delta V_{DS}}{\Delta I_{DS}}\right|_{V_{GS}} \quad (2.\ 4)$$

$$gain = g_m r_O \quad (2.\ 5)$$

The cut-off frequency ($f_T$) defined as the frequency where the magnitude of ac current gain falls to unity is given in Equation (2. 6).

$$f_T = \frac{g_m}{2\pi\left(C_{gs} + C_{gb} + C_{gd}\right)} \quad (2.\ 6)$$

## ***2. 1 Experimental Details***

In order to monitor the effects systematically, individual MOSFET devices with gate lengths between 2 and 20μm on p-type Si wafers, were examined first. The chips that contained individual devices with varying gate lengths, were packaged (Figure 2. 2) and placed on a specially designed PC board for measurements. A controlled microwave signal was amplified and injected first into the gate through a bias-T, and then into the drain and the output characteristics such as $I_{DS}$-$V_{DS}$, $I_{DS}$-$V_{GS}$, and transconductance ($g_m$) were measured using a HP 4145B semiconductor device parameter analyzer as shown in Figure 2. 3. Input microwave power and frequency were ranged from 0 to 30 dBm and 1 to 20 GHz respectively. Sub-micron (0.5μm) gate n-channel enhancement mode MOSFETs (Figure 2. 4.) were also examined in

this work. The input and output of each device were designed to have a ground-signal-ground (G-S-G) pads with a 150µm pitch [45] for on-chip measurements on a probe station. The schematic of the experimental set-up is shown in Figure 2. 5. The microwave signal, generated from the internal microwave source of a *HP8510C* network analyzer (*NA*), was injected into the gate and the drain through a bias-T using ACP40-GSG150 Microtech coplanar probes and the output characteristics and s-parameters were measured. The power and frequency of the microwave signal were ranged from 0 to 20dBm and 1GHz to 20GHz, respectively.

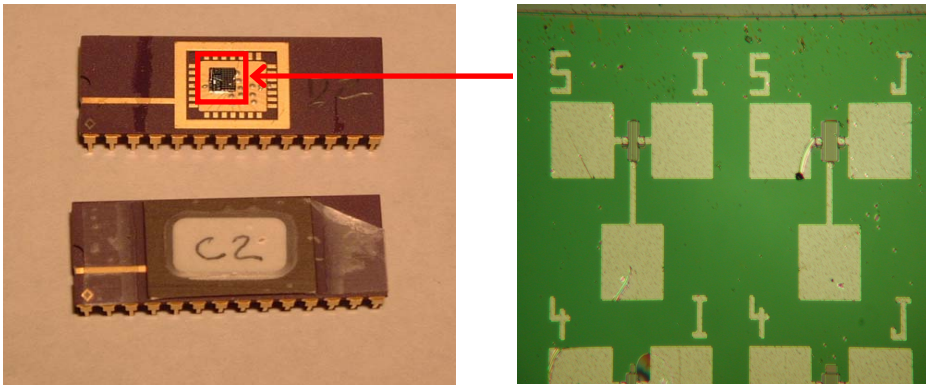



Figure 2. 2 MOSFET devices with gate length between 2 and 20µm on p-type Si wafer (right) and packaged chips (left).

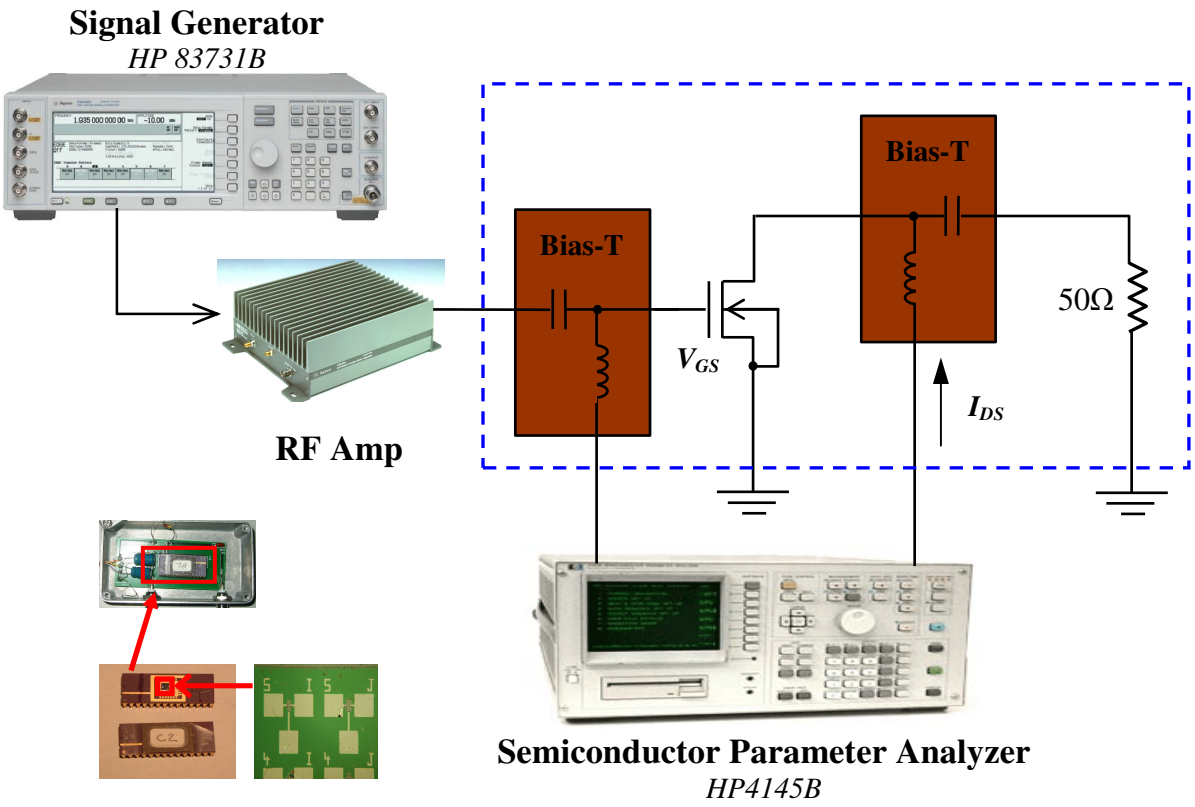



Figure 2. 3 Schematic of measurement setup for MOSFET devices.

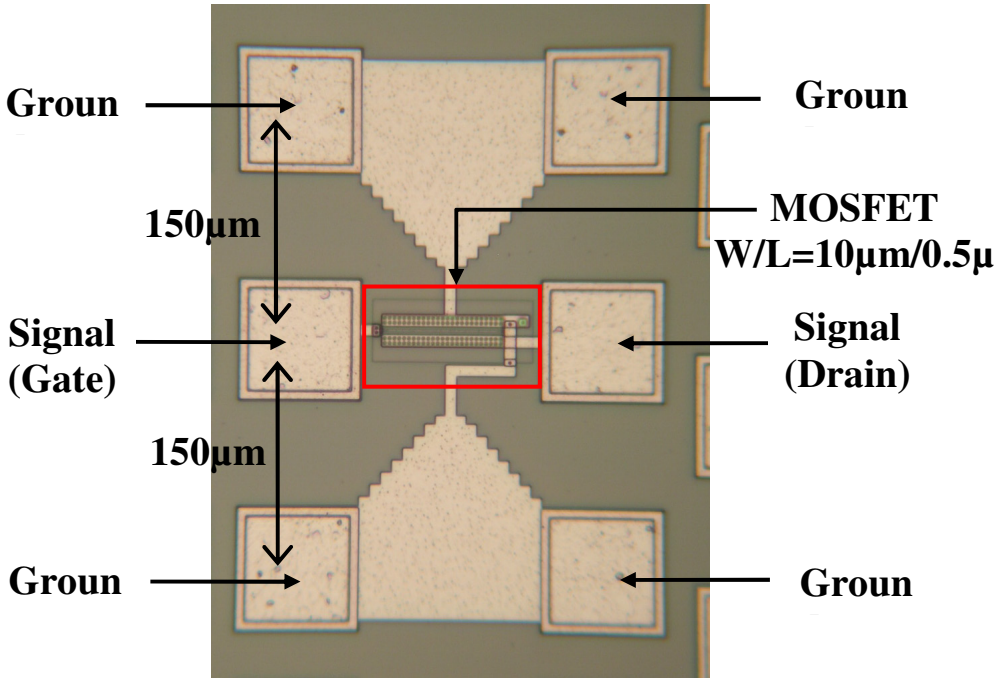
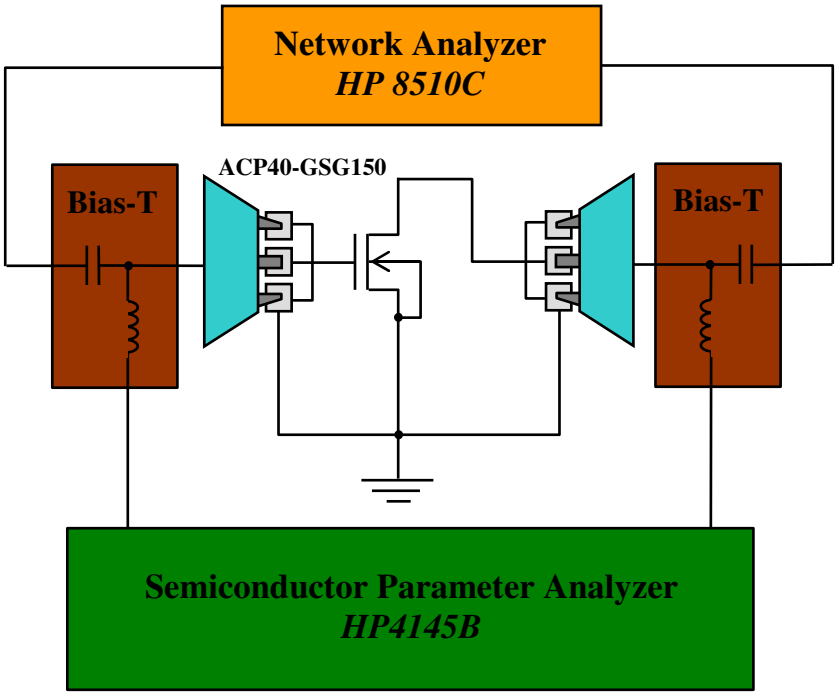


Figure 2. 4 Photograph of unpackaged sub-micron MOSFET device with G-S-G (Ground-Signal-Ground) pads at the input and output for on-chip measurement using Microtech probes on a probe station. The dimension of the device is W/L = 10μm/0.5μm.



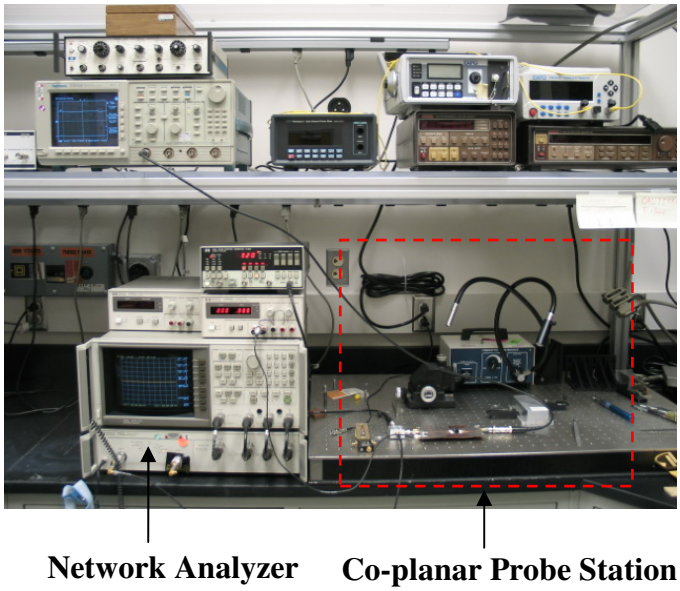



Figure 2. 5 Schematic of on-chip measurement setup for unpackaged sub-micron MOSFETs.

## *2. 2 Experimental Results and Discussion*

### 2. 2. 1 Microwave Interference Effects on Micron MOSFETs: Injection into Gate

Microwave injection at the gate of the device had a profound effect on the output $I_{DS}$-$V_{DS}$ characteristics for power levels above 10dBm, and made the devices inoperable at 30dBm as shown in Figures 2. 6 and 2. 7. The device characteristics show a gradual increase in output drain current with injected power levels, a gradual loss of saturation, and a positive offset current at zero drain bias, suggesting that the induced microwave field at the gate drives the channel into deep inversion to an approximately uniform channel that reaches no pinch-off at the drain for saturation to occur. The collapse of the characteristic allows no effective channel modulation by the gate, and the substantially increased current levels, render the device well outside the set operational limits for the circuit. In addition at higher frequencies (> 5 GHz) the microwave power effects were found to be strongly suppressed by the increased frequency, as shown in Figure 2. 8. A plot of the difference of drain current, $\Delta I_D$, measured from the $I_{DS}$-$V_{DS}$ characteristics with and without microwave injection at the gate is shown in Figure 2. 9. The plot shows significant increase in current with microwave at frequencies up to 4 GHz and power levels above 10 dBm, and no effects at higher frequencies. After the microwave event the devices were measured again in order to identify permanent changes in their operational characteristics, but no discernible changes were observed. Hence these effects are categorized as “soft”

error effects where the device may return to operation without permanent damage evident.

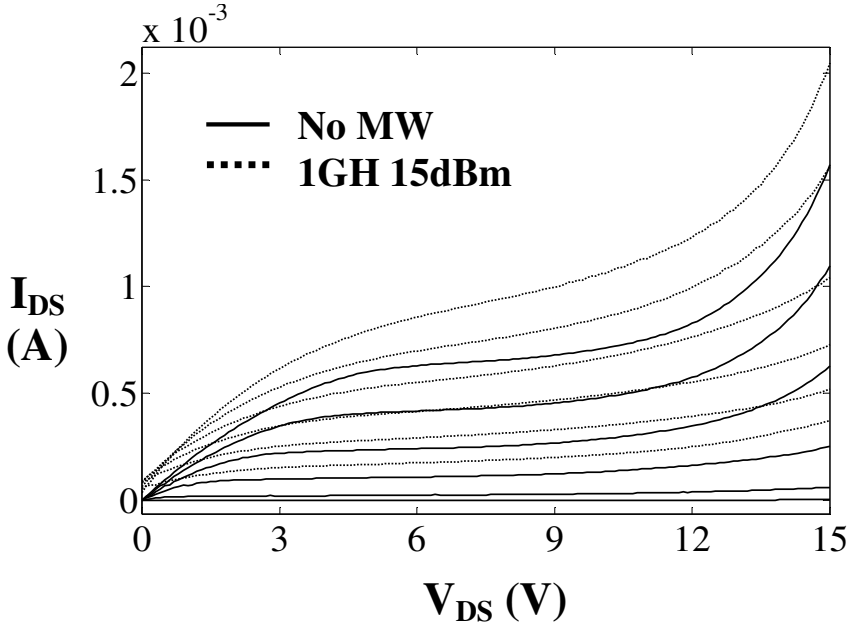



Figure 2. 6 Output current $I_{DS}$ versus input bias $V_{DS}$ with and without microwave injection to the gate. Output current increase and positive offset current at zero drain bias are observed at power 15dBm, 1GHz.

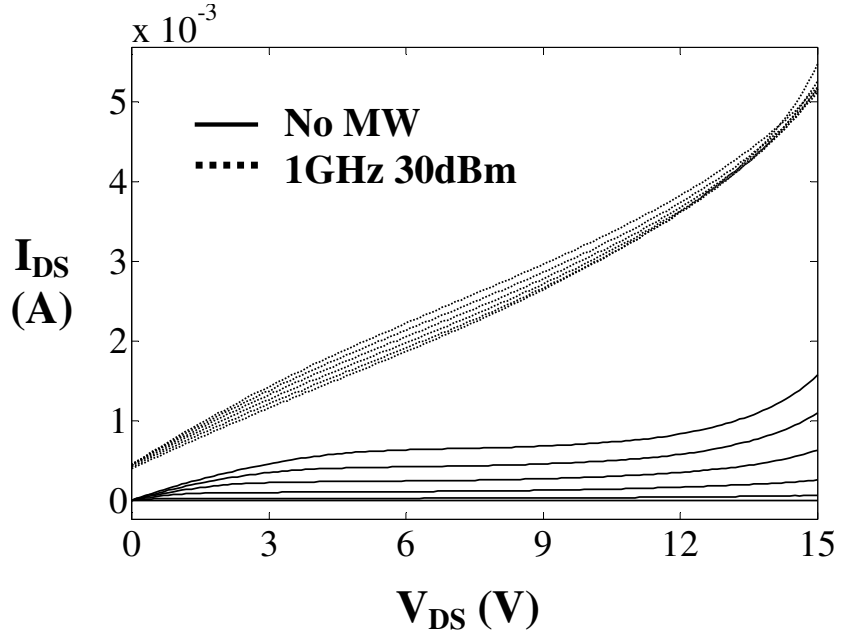


Figure 2. 7 Output current $I_{DS}$ versus input bias $V_{DS}$ with and without microwave injection to the gate. Induced microwave field, power 30dBm, 1GHz, drives the channel into deep inversion to an approximately uniform channel that reaches no pinch-off at the drain for saturation to occur.

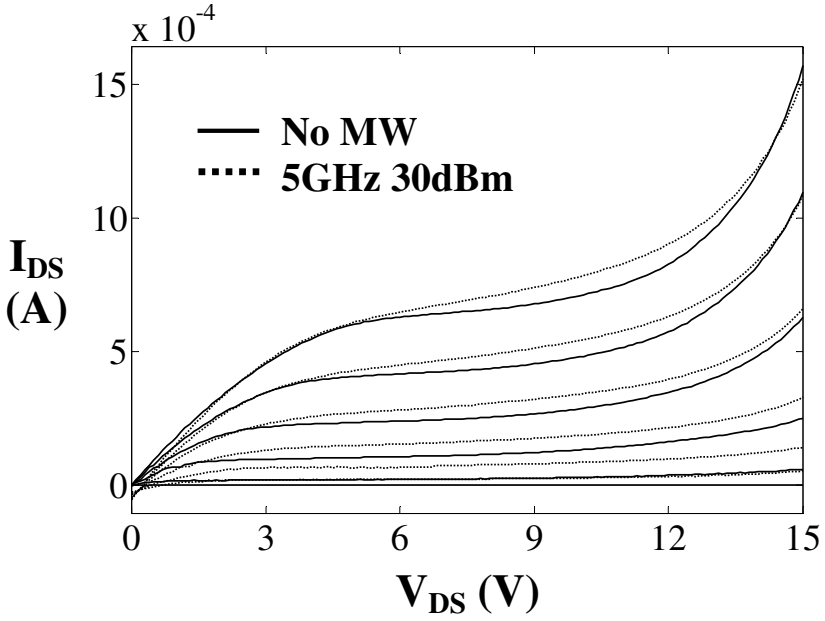



Figure 2. 8 Output current $I_{DS}$ versus input bias $V_{DS}$ with and without microwave injection to the gate. Power effect is strongly suppressed by frequency: power 30dBm, 5GHz.

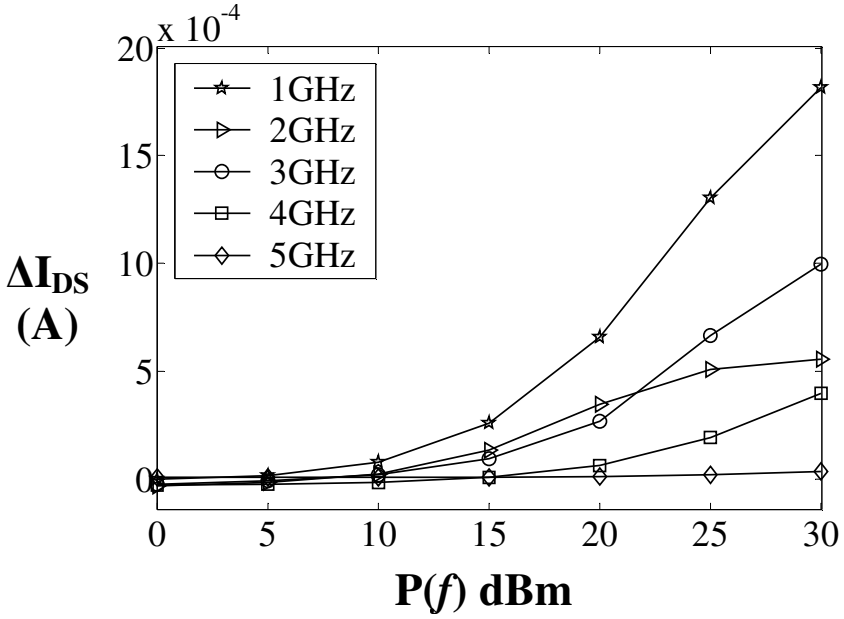


Figure 2. 9 Plot of drain current difference $\Delta I_{DS}$ with and without microwave injection to the gate, versus injected power and frequency.

## 2. 2. 2 Microwave Interference Effects on Micron MOSFETs: Injection into Drain

Microwave power injection to the drain electrode resulted in a decrease in drain current as shown in Figure 2. 10 (i.e. negative $\Delta I_D$) for power levels up to 15 dBm, and then an increase (positive $\Delta I_D$) at higher power levels, with the characteristics loosing saturation, and showing a significant reduction in break-down voltage as shown in Figure 2. 11. A negative current offset at zero drain bias is evident, indicating the device starts operating at accumulation, before going into inversion at a drain bias around 0.5V (Figure 2. 10). Again, at higher frequencies the power effect is strongly suppressed as in the case of gate injection.

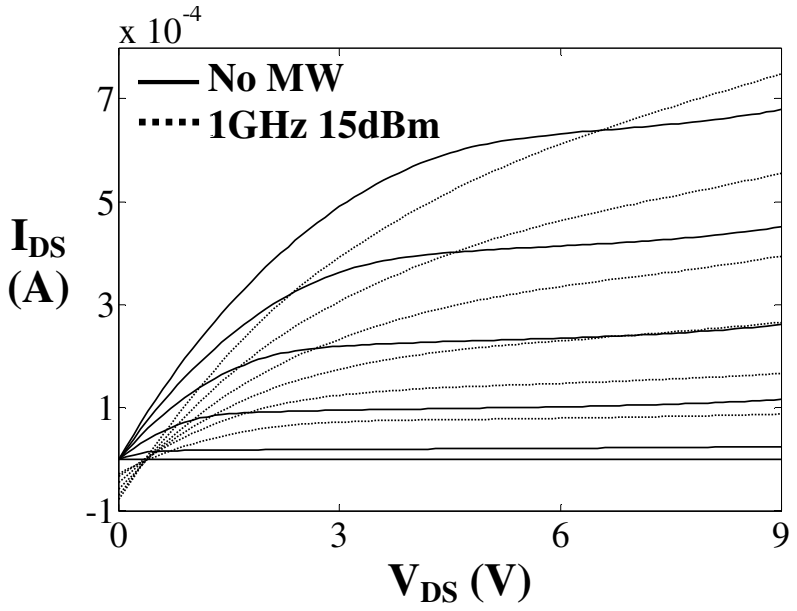



Figure 2. 10 Plot of drain current $I_D$ versus input bias $V_{DS}$ with and without microwave injection to drain. Drain current decrease and negative offset current at zero drain bias are observed at power 15dBm, 1GHz.

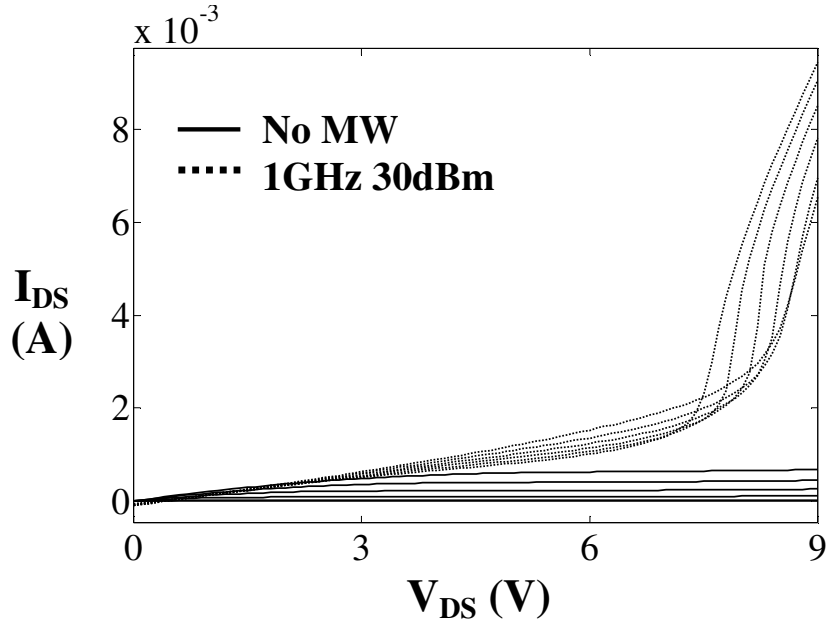



Figure 2. 11 Plot of drain current $I_D$ versus input bias $V_{DS}$ with and without microwave injection to drain. Significant reduction in break-down voltage and output current increase are observed at power 30dBm, 1GHz.

Figure 2. 12 shows the drain current plotted versus gate bias with and without microwave injection at the gate. Under no microwave injection the characteristics show good convergence and a threshold voltage ($V_{th}$) of 1 V is measured. Under the microwave injection however, lack of convergence of the characteristics is evident, indicating a fully-on channel with a high concentration of electrons where a threshold voltage cannot be defined. This demonstrates the inability of the channel to be effectively modulated by the gate bias, which results in significant reduction in transconductance ($g_m$) as shown in Figure 2. 13. Significant decrease in $g_m$ is observed at 1GHz at 30dBm for injection to the gate. However, at higher frequencies (5GHz) the effect of power (30 dBm) is strongly suppressed and the transconductance

value is restored. Injection to the drain gave similar results showing no convergence of the family of curves to define the threshold voltage, and a reduced transconductance for drain biases lower than 5 V. However, unlike the injection to the gate, an increase in transconductance is observed at drain biases close to the breakdown point (7 V), as shown in Figure 2. 14. Higher frequency (5GHz) again strongly suppresses the effect of power as observed under gate injection also.

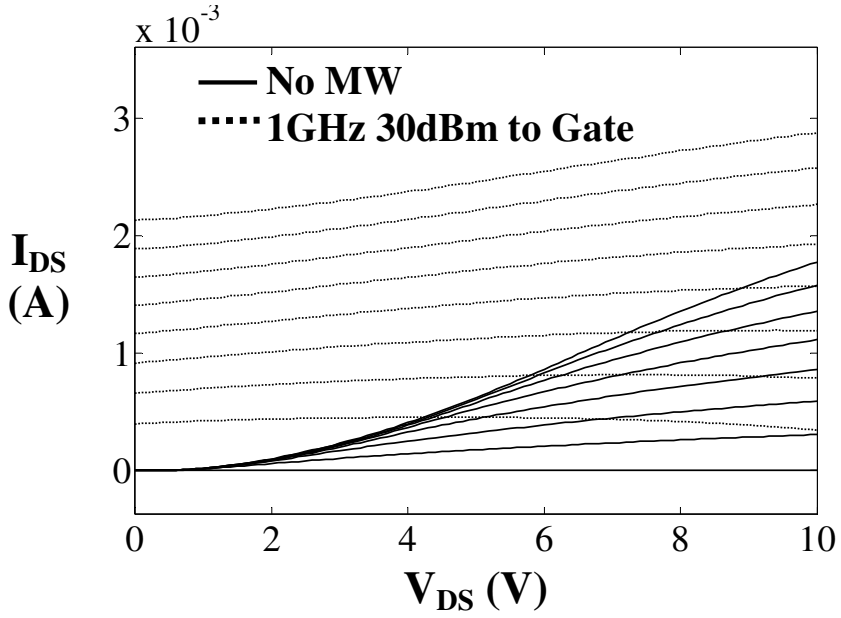



Figure 2. 12 Output current $I_{DS}$ versus input bias $V_{GS}$ with and without microwave injection to the gate: $V_{TH}$ =1V with the interference. With interference $V_{TH}$ cannot be defined.

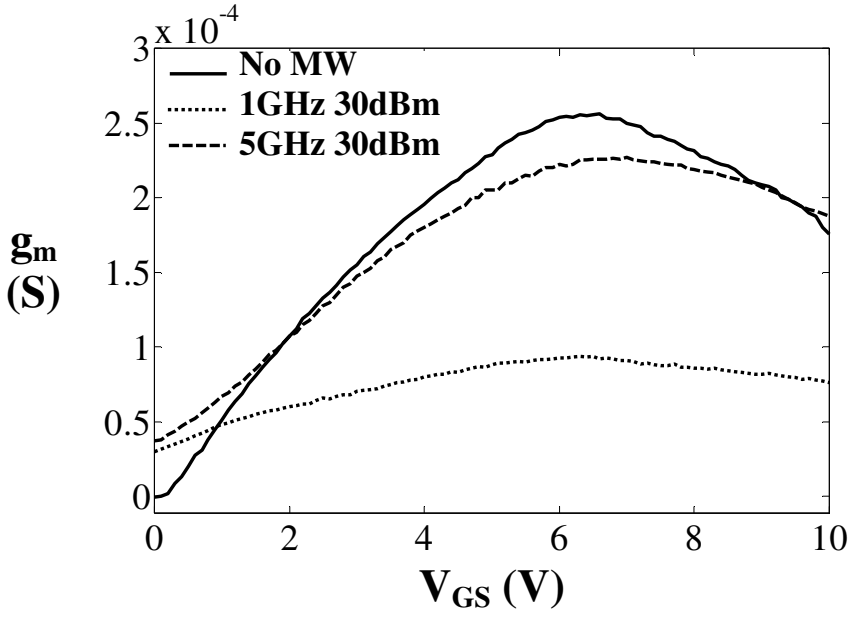



Figure 2. 13 Transconductance versus input bias $V_{GS}$ with and without microwave injection to the gate. Transconductance is observed to decrease significantly. At higher frequencies (5GHz) power effects are suppressed and transconductance is restored.

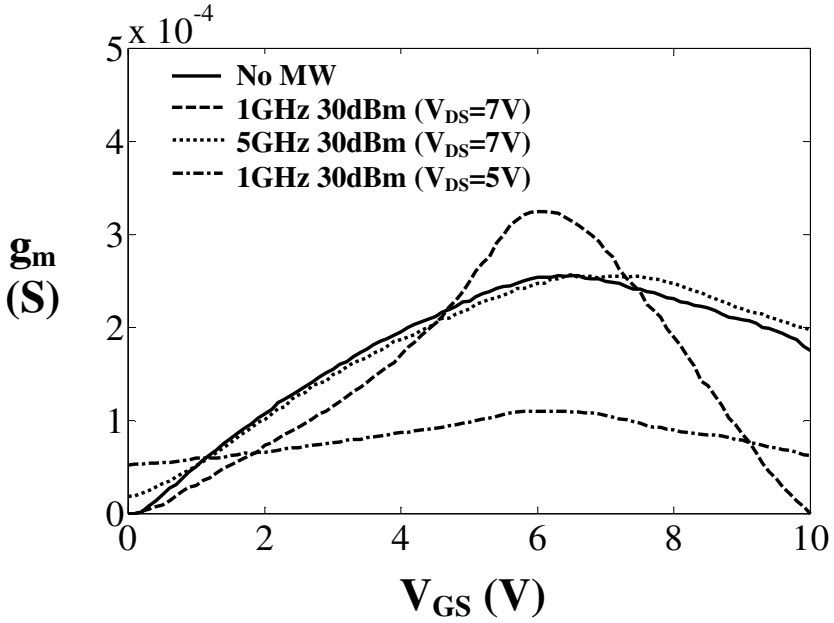


Figure 2. 14 Transconductance versus input bias $V_{GS}$ with and without microwave injection to the drain. Transconductance decreases significantly at drain bias $V_{DS}$ = 5V. At drain bias close to breakdown (7.0V), transconductance increases. At higher frequencies (5GHz) power effects are suppressed and transconductance is restored.

## 2. 2. 3 Interference Effects on Gain, Output Resistance, and Cut-off frequency

The degradation of gain, output resistance ($r_o$), and cut-off frequency ($f_T$) under gate and drain injection is examined and given in Table 1. 1. Bias condition is $V_{GS}$=5V and $V_{DS}$=7V or 5V. With 1GHz 30dBm gate injection, the transconductance and the output resistance show a decrease from $2.19\times10^{-4}$ (without microwave) to $0.9\times10^{-4}$ and from $49.2\times10^{3}$ (without microwave) to $4.08\times10^{3}$, respectively, resulting in a gain reduction to 0.37 from 10.8. In addition, the cut-off frequency is also decreased from 1.74GHz to 716MHz, indicting severe degradation in the small signal operational parameters. Thus, the device cannot operate properly as an amplifier circuit. With 1GHz 30dBm drain injection, the transconductance is observed to be the same as the one without interference for $V_{DS}$=7V, which is due to the avalanche breakdown at this bias condition. But for $V_{DS}$=5V the device again shows a decrease from $2.3\times10^{-4}$ to $0.98\times10^{-4}$. It is also observed that the output resistance decreases to $2.67\times10^{3}$ from $63.251\times10^{3}$ to and thus, resulting in a decrease in the gain to 0.66 for $V_{DS}$=7V and to 0.26 for $V_{DS}$=5V from 14.6 (without microwave). A little increase in the cut-off frequency is observed for $V_{DS}$=7V but for $V_{DS}$=5V it shows a reduction to 780MHz. At higher frequency (5GHz), however, the effects of power (30dBm) are observed to be strongly suppressed and the operational parameters are restored.

Therefore, it can be concluded that microwave power severely degrades the operational parameters such as the transconductance, the output resistance, gain, and cut-off frequency. As the frequency increases, the power effects are to be strongly suppressed.

| | | No Microwave | 1GHz 30dBm | 5GHz 30dBm |
|---|---|---|---|---|
| Gate injection | $g_m(S)$ | $2.19\times10^{-4}$ | $0.9\times10^{-4}$ | $2.1\times10^{-4}$ |
| | $r_O(\Omega)$ | $49.2\times10^{3}$ | $4.08\times10^{3}$ | $29.8\times10^{3}$ |
| | *Gain* | 10.8 | 0.37 | 6.3 |
| | $f_T$ | 1.74GHz | 716MHz | 1.74GHz |
| Drain injection | $g_m(S)$ | $2.3\times10^{-4}$ | $2.47\times10^{-4}$ [$0.98\times10^{-4}$ ($V_{DS}$=5V)] | $2.2\times10^{-4}$ |
| | $r_O(\Omega)$ | $63.251\times10^{3}$ | $2.67\times10^{3}$ | $48.78\times10^{3}$ |
| | *Gain* | 14.6 | 0.66 [0.26 ($V_{DS}$=5V)] | 10.7 |
| | $f_T$ | 1.83 GHz | 1.99GHz [780MHz ($V_{DS}$=5V)] | 1.75GHz |

Table 2. 1 The transconductance ($g_m$), output resistance ($r_O$), gain, and cut-off frequency of micron MOSFETs with microwave injection to the gate and the drain. Bias condition is $V_{GS}$=5V and $V_{DS}$=7V, or $V_{DS}$=5V.

## 2. 2. 4 Microwave Effects on Sub-micron MOSFETs

The sub-micron MOSFETs showed also the same trends in their operational parameters although the effects were not as pronounced due to lower power levels used to avoid burn-out and the difficulty to dissipate the injected power due to the by-pass capacitive effect at the gate and drain terminals. These devices were observed to

be more vulnerable to the injection of microwave power to the drain, due to gate oxide catastrophic failure at power levels above 18 dBm. S-parameter measurements of these devices are shown in Figure 2. 15 where the $S_{11,}$ $S_{12}$, $S_{21,}$ and $S_{22}$ parameters are measured.

Measured S-parameters show a large reflection in $S_{11}$ and $S_{22}$ (87-90%) due to the absence of matching units at the input and output of the device. This specific measurement is used, therefore, only to observe the trend of S-parameter variations with frequency. Reflection parameters ($S_{11,}$ $S_{22}$) of the injected microwave power are observed to decrease with increasing frequency indicating that injected power must be dissipated (or transmitted) in the device. However, transmission parameters ($S_{12}$, $S_{21}$) remain constant and below one, indicating that the device has no gain and no significant power is transmitted. If we examine the small signal intrinsic capacitances of the devices, the capacitance values calculated for each mode of operation (saturation, triode, cut-off) show that the gate to ground capacitance and the drain to ground capacitances are the largest in value (Table 1. 2) and therefore, as the frequency is increased these capacitors will be the first to become the by-pass capacitors providing a path for the microwave injected signal to ground.

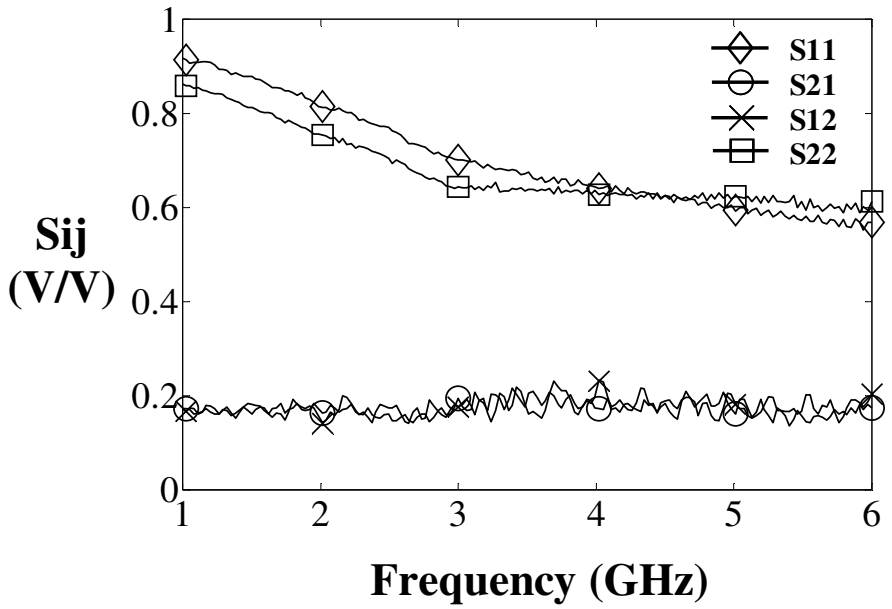



Figure 2. 15 Linear magnitude of s-parameters for sub-micron devices.

| | Off | Triode | Saturation |
|---|---|---|---|
| $C_{gs}$ | 2.33fF | 6.08fF | 8.11fF |
| $C_{gb}$ | 7.98fF | 0.5fF | 0.5fF |
| $C_{gd}$ | 2.33fF | 6.08fF | 2.33fF |
| $C_{db}$ | 6.46fF | 6.46fF | 6.46fF |

Table 2. 2 Calculated small signal intrinsic capacitances of sub-micron devices for each mode of operation (saturation, triode, cut-off), showing that the gate to ground capacitance and the drain to ground capacitances are the largest in value.

## ***2. 3 Summary***

In summary, our study showed that injected microwave power significantly affects output current, transconductance, output conductance, and breakdown voltage for power levels above 10dBm in the frequency range between 1 and 20 GHz. The effects result in loss of switching-off capability, loss of saturation and linearity in the

amplification region, development of DC offset currents at zero drain bias, and substantial reduction in breakdown voltages. Most importantly the power effects were observed to be suppressed at frequencies above 4 GHz for these devices indicating the possibility of ineffective microwave power coupling to devices of this size at the higher frequency range.

# Chapter 3: Critical Upsets in CMOS Inverters in Static Operation due to Microwave Interference

Inverters in static circuits have two main differences as compared with those in dynamic circuits. In static circuits, voltages and currents at each node depend on the resistive path between $V_{DD}$ and ground, while in dynamic circuits the values at each node are determined by charge transport to capacitors associated with each node. Furthermore, static circuits do not require periodic clock signals synchronized with data signals [34]. Due to the nature of digital operation, CMOS inverters are known to be robust to noise or EMI, allowing stable static operation. However, with current IC technology developing smaller feature sizes, higher clock frequencies, and lower operating voltage levels, digital circuits become more vulnerable to EMI [43]. Thus, noise immunity and operational robustness may be seriously compromised.

In this regards, we study the effects of high power CW microwave interference on the static operational parameters of CMOS inverters such as gain, output voltage and current, noise margins, regenerative signal properties, static power dissipation, load-line characteristics, and bit-errors. Especially, upset mechanisms and device scaling effects will be investigated using a simple device model.

## *3. 1 Experimental Details*

For the on-chip direct microwave measurements we used Agilent ADS (Advanced Design System) to design the devices with on-chip waveguides at the inputs and outputs (Figure 3. 1), matched inputs and outputs resulted in input power transmission

better than 97%. The $S_{11}$ and $S_{21}$ were monitored prior to every measurement to maintain a well controlled experimental procedure and make sure that the reflected component ($S_{11}$) was less than 3%. Five different size individual inverters, and a cascaded CMOS inverter, were designed and fabricated for this work. The five individual inverters are designated inverters 1 to 5. Inverters 1 to 3 were 1.5µm technology, while inverters 4 and 5 were 0.5µm technology, and multiple chips containing several inverters of each size, were fabricated. Table 3. 1 shows the specific dimensions of the inverters, while a photograph of an individual inverter is shown in Figure 3. 1. The cascaded inverters were the same size as inverter 1. Measurements were performed using on-chip microwave probes on a microwave probe station. The input and output of each inverter unit were designed to have coplanar waveguides in a ground-signal-ground (GSG) configuration with a 150µm pitch [45], suitable for on-chip microwave probes. A schematic of the experimental set-up is shown in Figure 3. 2.

| | | | W/L |
|---|---|---|---|
| 1.5µm Technology | Inverter 1 | p-MOS | 9.6µm/1.6µm |
| | | n-MOS | 3.2µm/1.6µm |
| | Inverter 2 | p-MOS | 24µm/1.6µm |
| | | n-MOS | 8µm/1.6µm |
| | Inverter 3 | p-MOS | 120µm/1.6µm |
| | | n-MOS | 40µm/1.6µm |
| 0.5µm Technology | Inverter 4 | p-MOS | 3.6µm/0.6µm |
| | | n-MOS | 1.2µm/0.6µm |
| | Inverter 5 | p-MOS | 18µm/0.6µm |
| | | n-MOS | 6µm/0.6µm |

Table 3. 1 The dimensions (W/L) of the five CMOS inverters used in this study, are shown.

The microwave signal ($V_{MW}$), generated from the internal microwave source (*port1*) of a *HP8753C* network analyzer (*NA*), was coupled to the DC input voltage from the source monitor unit (*SMU1*) of a *HP4145B* semiconductor parameter analyzer through a bias-T, and directly injected into the input of the inverter ($V_{IN}$) using the on-chip ACP40-GSG150 Microtech coplanar probes. The power and frequency of the microwave signal was between 0dBm (1mW) and 24dBm (251.2mW) and 0.8 and 3GHz, respectively. We have focused on the 0.8 to 3GHz range because our previous study [2] showed that the effects were most prominent around 1GHz as it was also reported in [3]. Furthermore, to avoid frequent burn-out of the devices we did not exceed 24dbm of power. At each frequency and power level, the DC bias voltage was swept from 0V to 5V with 0.1V step using *SMU1*, and the output voltage ($V_O$) and current ($I_O$) were measured through the voltage monitor unit (*Vm1*) and *SMU2* of the *HP4145B*. The bias voltage ($V_{DD}$) was set to 5V using *SMU2*. From the measurements, the static operational parameters, such as voltage and current transfer characteristics, load-line characteristics, gain, noise margins, output currents, static power dissipation, and input/output voltage ranges, were obtained with and without microwave interference.

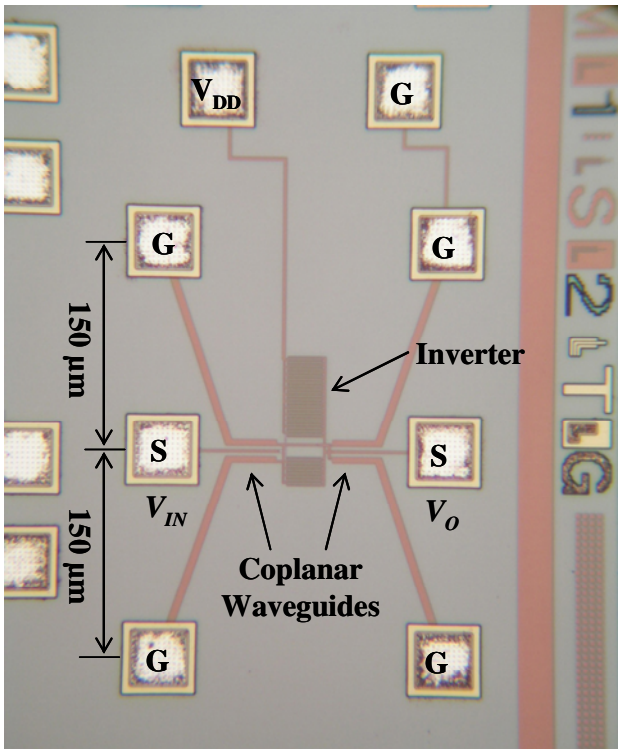



Figure 3. 1 The photograph of a single CMOS inverter showing on-chip measurement G-S-G pads for Microtech coplanar probes.

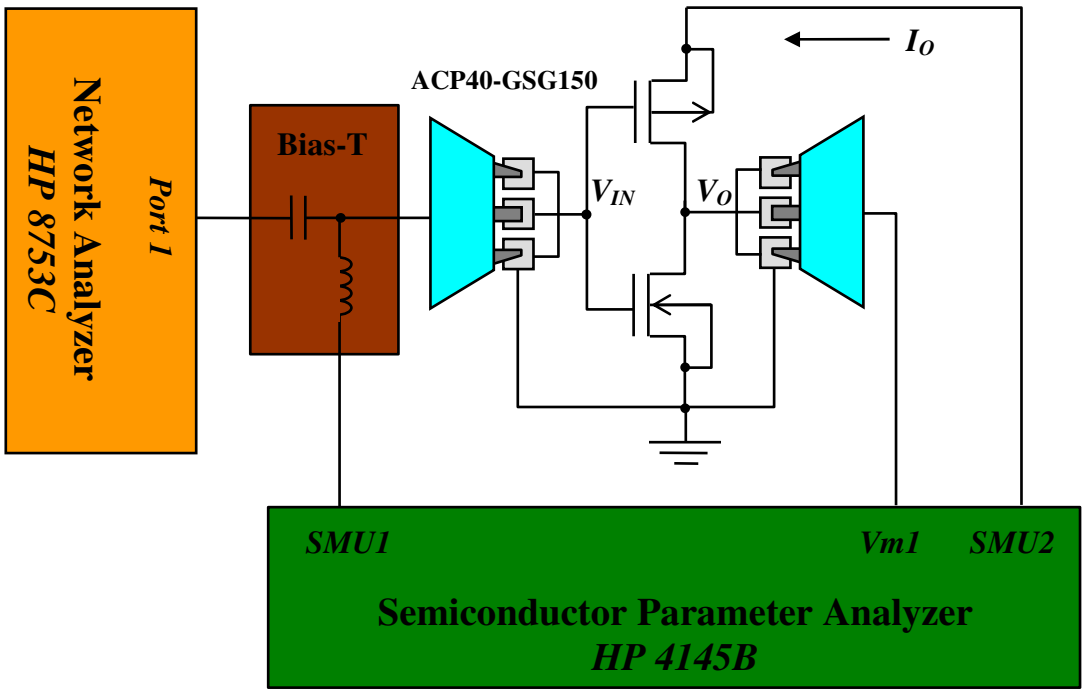



Figure 3. 2 The schematic of the measurement set-up for the CMOS inverters.

## *3. 2 Voltage Transfer Characteristics and Gain*

The voltage transfer characteristics (VTCs) represent the output voltage ($V_O$) with respect to the input voltage ($V_{IN}$) at steady-state. A typical VTC (solid line) schematic of an inverter is shown in Figure 3. 3.

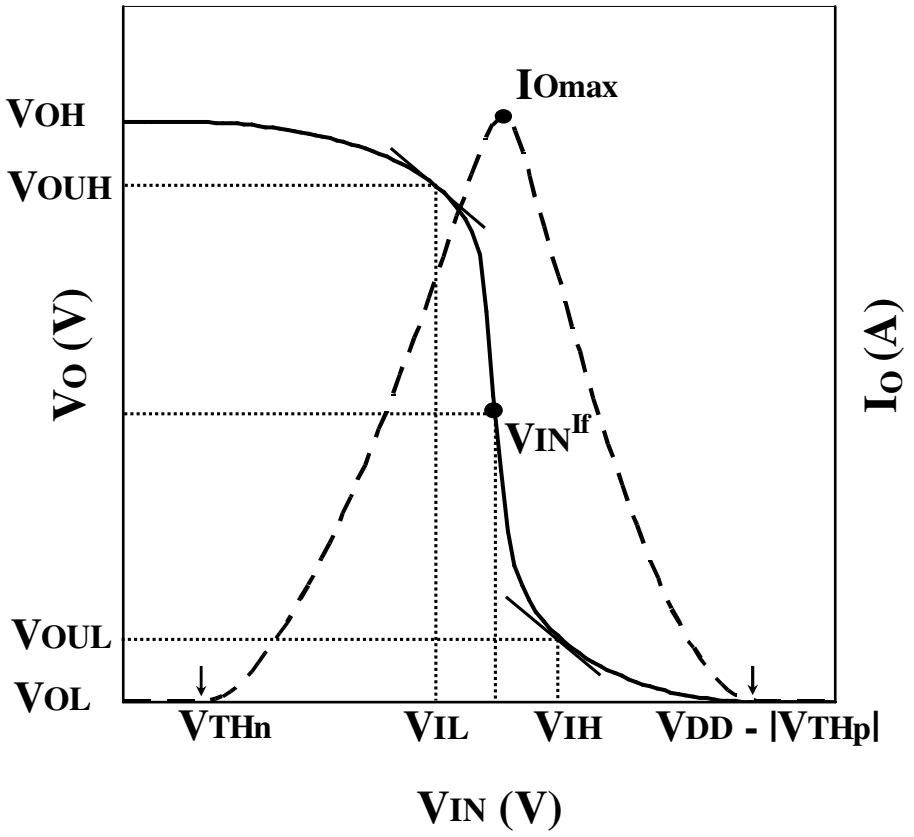



Figure 3. 3 Typical schematic of voltage transfer characteristics (VTCs, solid line) and current transfer characteristics (CTCs, dashed line), of a single hypothetical inverter. Points of interest are the threshold voltages for n-MOS and p-MOS devices in inverters: $V_{THn}$ and $V_{THp}$.

The VTC can be divided into three regions. In the first region the output voltage ($V_O$) stays within $V_{OH}$ and $V_{OUH}$ until the input voltage ($V_{IN}$) reaches $V_{IL}$. Ideally this is a zero gain region before the inverter switches. The second region is the

gain region where switching of the inverter from logic high to logic low occurs for input voltages between $V_{IL}$ and $V_{IH}$. The higher the gain in that region the more effective the switching is. As implied by Equation 3. 1, the slope of the region provides the gain of the inverter in the VTC. The points where the slope equals –1, are defined as the high and low switching points of the inverter and designated as $V_{OUH}$ and $V_{OUL}$ respectively. The third region begins at the low switching point where $V_O$ stays within $V_{OL}$ and $V_{OUL}$ as long as $V_{IN}$ exceeds $V_{IH}$. The inflection point ($V_{IN}^{IF}$) is defined as the input voltage where the output voltage is $V_{DD}/2$. The gain region between $V_{IL}$ and $V_{IH}$, and the corresponding output voltages $V_{OUH}$ and $V_{OUL}$, is critical to maintain the switching capability and complementary characteristics of the inverter.

$$gain = \left.\frac{\partial V_O}{\partial V_{IN}}\right|_{V_{IN}=V_{INO}} \tag{3. 1}$$

For the extreme case, for example, where the gain in that region is reduced to zero, then the two states of the inverter, high and low, cannot be distinguished and no switching action can be observed. Thus, degradation of the gain region in CMOS inverters is critical to their performance.

### 3. 2. 1 Voltage Transfer Characteristics

Figure 3. 4 shows the VTC of inverter 1, measured with and without a 1GHz continuous wave (CW) microwave interference signal injected into the input of the device. The family of characteristics shows a gradual decrease in gain with the power

of the microwave interference at the gain region, as evidenced by the change in the slope of the characteristic at the inflection point $V_{IN}^{IF}$. A substantial gain reduction from 13.5V/V to 2.1V/V at 24dBm (Table 3. 2), corresponding to an 84% decrease, is observed, and the gain region ($V_{IH}$–$V_{IL}$) is extended substantially by 88.9%, suggesting significant degradation in the complementary operation of the inverter. The characteristic also shows changes in the output voltage levels from 5V ($V_{OH}$) to 4.8V and from 0V ($V_{OL}$) to 0.3V, respectively at 1GHz, 24dBm. Therefore, it is clear that the inverter cannot be turned ON (when $V_O$ is logic high) and OFF (when $V_O$ is logic low) properly. This degradation in the inverter characteristics can be better understood by analyzing the load-line characteristics of the n and p-MOS devices of the inverter.

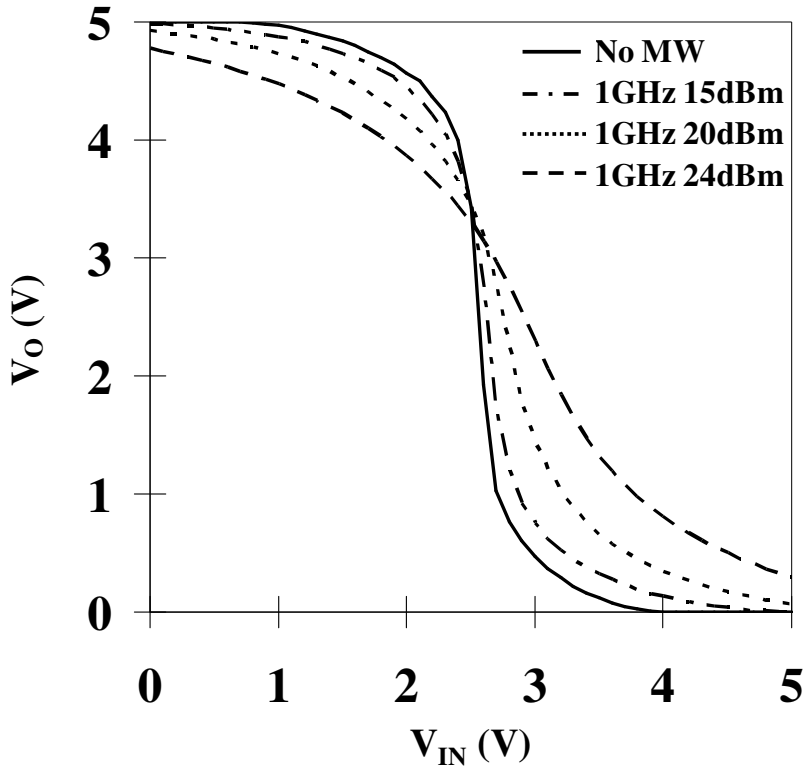


Figure 3. 4 Experimentally measured voltage transfer characteristics (VTCs) of inverter 1 under microwave interference at 1GHz and varying power levels.

| | $V_{IH} - V_{IL}$ | Gain at $V_{IN}^{If}$ | $V_{OH}$ | $V_{OL}$ |
|---|---|---|---|---|
| No MW | 0.9 V | 13.5 V/V | 5 V | 0 V |
| 1GHz 5dBm | 1 V | 11.6 V/V | 5 V | 0 V |
| 1GHz 15dBm | 1.1 V | 8.5 V/V | 4.9 V | 0 V |
| 1GHz 20dBm | 1.41 V | 4.8 V/V | 4.9 V | 0.1 V |
| 1GHz 24dBm | 1.7 V | 2.1 V/V | 4.8 V | 0.3 V |

Table 3. 2 The degradation in the high gain region ($V_{IH}$–$V_{IL}$), the gain at $V_{IN}^{If}$, the output voltage high ($V_{OH}$), and the output voltage low ($V_{OL}$), are summarized, for inverter 1 under 1GHz microwave interference.

## 3. 2. 2 Load-Line Characteristics and Quiescent Point of Operation

Figure 3. 5 shows the measured VTC (inset 6), and CTC (inset 5) of inverter 1, with (solid line) and without (dashed line) 1GHz, 24dBm microwave interference. For better clarity, the load-line characteristics of the inverter at each boundary point ($V_{OH}$, $V_{OL}$, $I_{O(ON)}$, $I_{O(OFF)}$) are shown as insets 1 ($V_{OH}$ and $I_{O(ON)}$), and *3* ($V_{OL}$ and $I_{O(OFF)}$), without interference, and 2 ($V_{OH}^{MW}$ and $I_{O(ON)}^{MW}$), and 4 ($V_{OL}^{MW}$ and $I_{O(OFF)}^{MW}$), with interference. This load-line characteristic measurement is a new measurement technique allowing a better understanding on the changes in the quiescent point of operation, the currents, and the output voltages under microwave interference.

For $V_{IN}$=0V, inset 2 shows a significant increase in the drain current of the n-MOS ($I_{DSN}$) at 1GHz 24dBm, as compared with inset 1. Thus, the quiescent (Q) point of operation shifts from A to B under interference, resulting in an increase in output

current ($I_{O(ON)}$) from 12.6nA to 0.11mA, and a corresponding decrease in output voltage ($V_{OH}$) from 5V to 4.8V, as indicated by the arrows in the figure. This means that the effective ON resistance (active load) of the n-MOS device decreases substantially with microwave interference, providing a current path to the ground. As a result, the output current increases and the output voltage decreases. Similarly, for $V_{IN}$=5V, the $I_{O(OFF)}$ increases from 17.4nA to 88.7μA and $V_{OL}$ increases from 0V to 0.3V due to the transition of the Q point from C (without interference) to D (with interference), as shown in inset 3 and 4. Thus, the degradation in the characteristics can be attributed to the substantial increase in the drain current of each MOSFET of the inverter that shifts the Q point of operation.

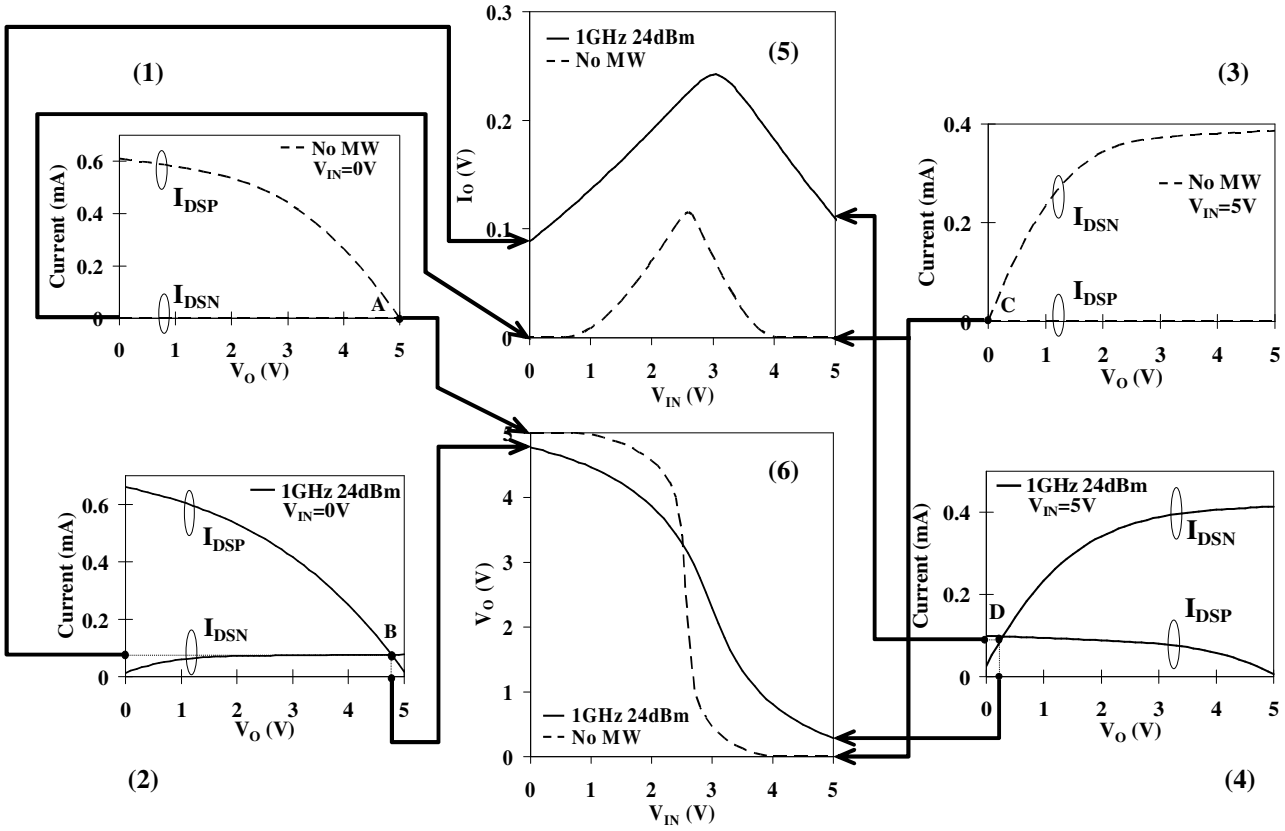


Figure 3. 5 Experimentally measured load-line characteristics, VTC (inset 6), and CTC (inset 5) of inverter 1 with (solid line) and without (dashed line) 1GHz 24dBm microwave interference. The load-line characteristics of the inverter at each boundary point ($V_{OH}$, $V_{OL}$, $I_{O(ON)}$, $I_{O(OFF)}$) are shown as insets 1 ($V_{OH}$ and $I_{O(ON)}$), and *3* ($V_{OL}$ and $I_{O(OFF)}$), without interference, and 2 ($V_{OH}^{MW}$ and $I_{O(ON)}^{MW}$), and 4 ($V_{OL}^{MW}$ and $I_{O(OFF)}^{MW}$), with interference. The quiescent point of operation (Q), and the corresponding currents and voltages are indicated at the VTC and CTC by the arrows.

### 3. 2. 3 Gain at the Inflection Voltage

The gain of the five different inverters measured at the inflection point ($V_{IN}^{If}$) versus microwave power is plotted in Figure 3. 6. For the 1.5µm inverters, the graph shows decrease in gain from 13.5V/V (without interference), to 1.4V/V to 2.2V/V at 24dBm, a decrease by a factor of 6 to 10. For the 0.5µm inverters the gain decreases by a factor of 18 to 24 in the given power range, showing significantly higher susceptibility to the interference.

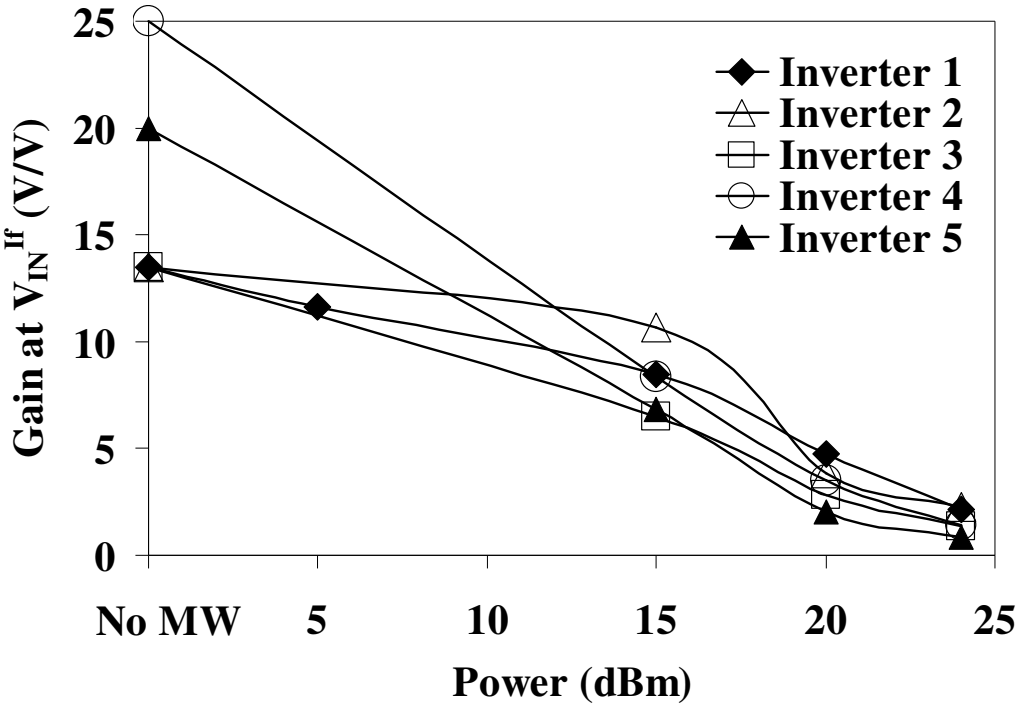


Figure 3. 6 Measured inverter gain at inflection point for five different inverters under 1GHz microwave interference. Inverters 1, 2, and 3, are 1.5μm, while inverters 4, and 5 are 0.5μm technology. Substantial gain reduction is observed after 15dBm.

This reduction in gain is related to the transconductance ($g_m$) of the MOSFETs. In order to analyze the effect of interference on the $g_m$, it is necessary to model the drain current of the MOSFETs under interference. As indicated in our previous results [2], drain current increase under interference is related to the increase in the charge at the channel, the decrease in the threshold voltage, and the increase in the channel length modulation factor $\lambda$. These changes can be modeled in the following equations for ${I_{DSN(sat)}}^{MW}$ and ${I_{DSP(sat)}}^{MW}$:

$$I_{DSN(sat)}{}^{MW} = \frac{C_{ox}\mu_n}{2}\left(\frac{W_n}{L_n}\right)\left(V_{IN} + \Delta V_n{}^{MW} - V_{THn}{}^{MW}\right)^2 \times\left(1+\lambda_n{}^{MW}V_o\right) \tag{3. 2}$$

$$I_{DSP(sat)}{}^{MW} = \frac{C_{ox}\mu_p}{2}\left(\frac{W_p}{L_p}\right)\left(V_{DD} - V_{IN} + \Delta V_p{}^{MW} - \left|V_{THp}{}^{MW}\right|\right)^2 \times\left[1+\lambda_p{}^{MW}\left(V_{DD}-V_o\right)\right] \tag{3. 3}$$

Where, ${I_{DSN(sat)}}^{MW}$ and ${I_{DSP(sat)}}^{MW}$ are the drain currents of the n and p-MOS devices in saturation under microwave interference, respectively. $C_{ox}$, $\mu$, $W$, $L$, $V_{IN}$, $V_{TH}$, $\lambda$, $V_{DD}$, and $V_o$ are the gate oxide capacitance, the mobility, the width, the length, the input voltage, the threshold voltage, the channel length modulation factor, the bias voltage,

and the output voltage. The subscripts n and p represent the n-MOS and p-MOS devices, respectively. The "MW" superscript represents microwave interference. Since $Q=CV$, the increase of charge at the channels can be modeled as an equivalent voltage source ($\Delta V_n^{MW}$ and $\Delta V_p^{MW}$) at the gates of the n and p-MOS devices.

As the power of microwave interference increases, $\Delta V^{MW}$ and $\lambda^{MW}$ increase, while $V_{TH}^{MW}$ decreases [2], thus affecting $I_{DN(sat)}^{MW}$ and $I_{DP(sat)}^{MW}$. Based on the definition of the transconductance ($g_m$) given below,

$$g_m^{MW} = \left.\frac{\partial I_{DS}^{MW}}{\partial V_{GS}}\right|_{V_{DS}} \tag{3. 4}$$

the incremental change of $I_{DN(sat)}^{MW}$ and $I_{DP(sat)}^{MW}$ with respect to the incremental change in the input voltage ($V_{IN}$) or equivalently $V_{GS}$ , becomes smaller, resulting in reduced $g_m^{MW}$, and hence, reduced gain.

### 3. 2. 4 The Output Voltage High and Low ($V_{OH}$ and $V_{OL}$)

The measured $V_{OH}$ and $V_{OL}$ also showed substantial changes with microwave power. As shown in Figure 3. 7 (a), the decrease in $V_{OH}$ ranged between 4.73V and 4.45V at 1GHz, 24dBm. In this case, the larger width device (inverter 5) gives larger decrease than the smaller width (inverter 4), with the same trend being observed in inverters 1-3. Figure 3. 7 (b) showing $V_{OL}$ follows the opposite trend. Here it is observed that $V_{OL}$ increases between 0.1V and 1.24V at 24dBm. In this case, the

smaller width device shows the higher increase. This trend can be attributed to the changing current driving capabilities of the n and p-MOS devices under interference.

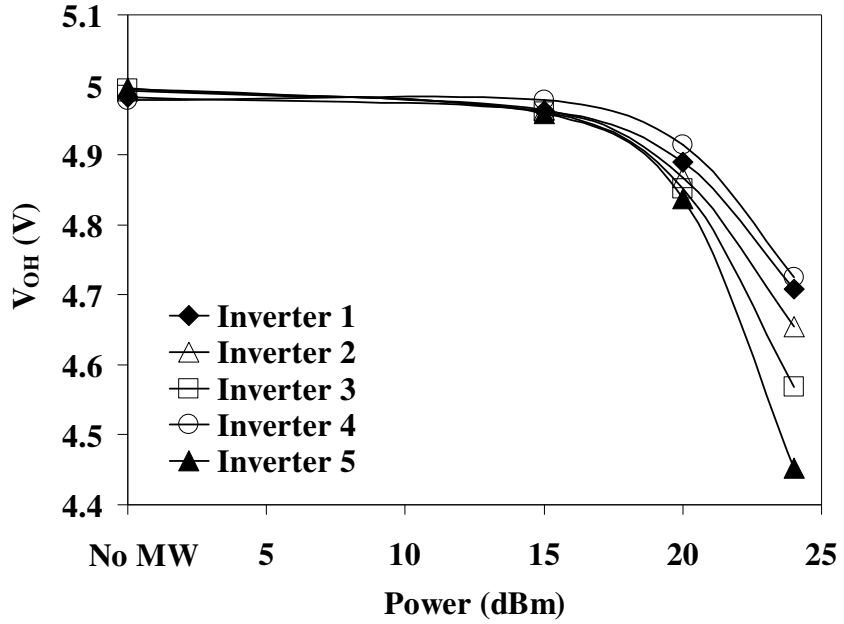



Figure 3. 7 (a).

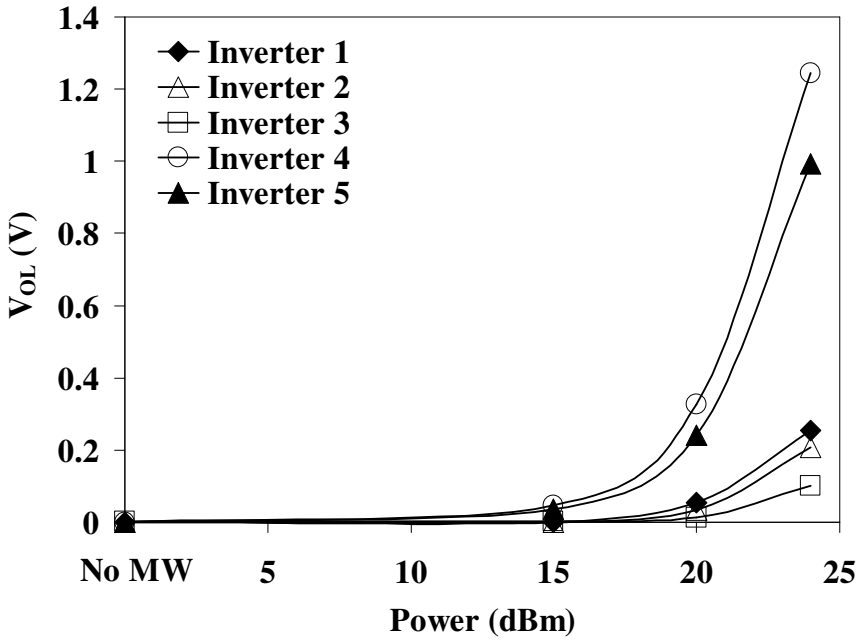



Figure 3. 7 (b).

Figure 3. 7 (a) Measured output voltage high ($V_{OH}$) of the five inverters showing significant decrease after 15dBm microwave interference at 1GHz. (b) Measured

output voltage low ($V_{OL}$) of the five inverters showing significant increase after 15dBm, 1GHz microwave interference.

The inverters operate in two different modes depending on input conditions (a) pull up and (b) pull down modes. For instance, as the input voltage changes from input logic high to low, the n-MOS devices will be OFF, and the p-MOS devices will be ON. This will pull up the output voltage from logic low to logic high, and vice versa, as the input changes from input logic low to input logic high, the p-MOS will be OFF and the n-MOS will be ON. Hence, the output voltage will be pulled down to output logic low. The speed of the pull up/pull down operation primarily depends on the relative current driving capabilities of the n and p-MOS devices. Since each of the MOS devices operates in the saturation region, the current driving capabilities of each device can be evaluated at the inflection point ($V_{IN}^{If}$), as follows:

$$I_{DSN(sat)} = I_{DSP(sat)} \tag{3. 5}$$

where, $I_{DSN(sat)}$ and $I_{DSP(sat)}$ are the drain currents of the n and p-MOS at the saturation region, respectively.

$$\begin{aligned} \frac{C_{ox}\mu_n}{2}\left(\frac{W_n}{L_n}\right)\left(V_{IN}-V_{THn}\right)^2\left(1+\lambda_n V_o\right) &= \frac{C_{ox}\mu_p}{2}\left(\frac{W_p}{L_p}\right) \\ &\times\left(V_{DD}-V_{IN}-\left|V_{THp}\right|\right)^2\left[1+\lambda_p\left(V_{DD}-V_o\right)\right] \end{aligned} \tag{3. 6}$$

Since $V_o = \frac{V_{DD}}{2}$ at the inflection voltage ($V_{IN}$=$V_{IN}^{If}$) when $L_n$=$L_p$, Equation 3. 6 becomes Equation 3. 7, where $V_{IN}^{If}$ is given by Equation 3. 8.

$$\left(\frac{\mu_n W_n}{\mu_p W_p}\right)\left(\frac{1+\frac{\lambda_n V_{DD}}{2}}{1+\frac{\lambda_p V_{DD}}{2}}\right)\left(V_{IN}^{\ If} - V_{THn}\right)^2 = \left(V_{DD} - V_{IN}^{\ If} - \left|V_{THp}\right|\right)^2 \tag{3. 7}$$

$$V_{IN}^{\ If} = \frac{V_{DD} - \left|V_{THp}\right| + \alpha V_{THn}}{1+\alpha} \tag{3. 8}$$

where

$$\alpha = \sqrt{\frac{\mu_n W_n\left(1+\frac{\lambda_n V_{DD}}{2}\right)}{\mu_p W_p\left(1+\frac{\lambda_p V_{DD}}{2}\right)}} \tag{3. 9}$$

If $V_{THn}$=$|V_{THp}|$, then $V_{IN}^{If}$ will be $V_{DD}$/2 for $\alpha$=1. This specific case shows symmetric transfer characteristics indicating that the n and p-MOS have the same current driving capabilities at each input condition. The current driving capabilities are determined exclusively by $\alpha$ and thus, by $\mu$, $W$, and $\lambda$. If we increase $\alpha$, $V_{IN}^{IF}$ decreases, and vice versa. This is mainly because one of the current driving capabilities of the MOS devices is greater than that of the other. For instance, if $\alpha > 1$, the numerator of $\alpha$ is greater than the denominator indicating that the n-MOS device drives more current

during the pull down operation than the p-MOS devices does during the pull up operation. Therefore, the output will reach $V_{DD}/2$ at a $V_{IN}$ less than $V_{DD}/2$.

The same analysis holds when microwave interference is on. For $I_{DSN(sat)}{}^{MW} = I_{DSP(sat)}{}^{MW}$, using the models given in Equation 3. 2 and 3. 3, $V_{IN}{}^{If\,MW}$ can be given by Equation 3. 10.

$$V_{IN}{}^{If\ MW} = \frac{V_{DD} + \left(\Delta V_p{}^{MW} - \left|V_{THp}{}^{MW}\right|\right) - \beta\left(\Delta V_n{}^{MW} - V_{THn}{}^{MW}\right)}{1+\beta} \tag{3. 10}$$

where $V_o = \frac{V_{DD}}{2}$ at $V_{IN}=V_{IN}{}^{If\,MW}$ when $L_n = L_p$, and

$$\beta = \sqrt{\frac{\mu_n W_n\left(1+\frac{\lambda_n{}^{MW} V_{DD}}{2}\right)}{\mu_p W_p\left(1+\frac{\lambda_p{}^{MW} V_{DD}}{2}\right)}} \tag{3. 11}$$

Now, the inflection voltage depends on $\beta$, $\Delta V^{MW}$, and $V_{TH}{}^{MW}$. Thus $V_{IN}{}^{If\,MW}$ measured at 1GHz 24dBm for the 1.5µm inverters, gave a value of 2.95V, 2.56V, and 2.1V for inverters 1, 2 and 3, respectively. This result indicates that the p-MOS device of inverter 1 drives relatively more current than the n-MOS device, while the p-MOS device of inverter 3 drives relatively less current than the n-MOS device. Therefore, $V_{OL}$ of inverter 1 is larger than that of inverter 3, while $V_{OH}$ of inverter 1 is less than that of inverter 3. The 0.5µm inverters also show the same trend.

Comparing the 0.5µm with the 1.5µm inverters, we observe that the 0.5µm are more vulnerable to interference, because of larger relative changes in gain, $V_{OH}$ and $V_{OL}$, as shown in Figure 3. 5, and Figure 3. 7 (a),(b), for the gain, and voltages,

respectively. The graph also shows that most significant changes in $V_{OH}$ and $V_{OL}$ occur above 15dBm.

## *3. 3 Noise Margins and Regenerative Signal Properties*

### 3. 3. 1 Noise Margins

The reduction in gain and changes in steady state output voltages ($V_{OH}$ and $V_{OL}$) observed under microwave interference, lead to degradation in noise immunity of the inverters. The level of noise immunity is related to the static noise margins. Static noise margins indicate the maximum noise allowed without causing a state change in the inverter. The static noise margins are given in Equations 3. 12 and 3. 13 [34].

$$\mathrm{SNM_H} = V_{OH} - V_{IH} \tag{3. 12}$$

$$\mathrm{SNM_L} = V_{IL} - V_{OL} \tag{3. 13}$$

The static noise margins of the inverters measured with 1GHz microwave interference into the input gate of the inverters, are shown in Figure 3. 8 (a) and (b). Static noise margin high ($\mathrm{SNM_H}$) is observed to be compressed severely for all inverters in particular when the interference power exceeds 15dBm, as shown in Figure 3. 8 (a). The highest compression is observed for inverter 4 where the $\mathrm{SNM_H}$ was compressed from 1.74V without interference to –0.14V with 1GHz 24dBm interference. Static noise margin low ($\mathrm{SNM_L}$) is shown in Figure 3. 8 (b), where it is observed to also be compressed but to a lesser extend. $\mathrm{SNM_H}$ and $\mathrm{SNM_L}$ for inverter 5 could not be obtained at 1GHz 24dBm because the gain decreased below 1 and $V_{IH}$

and $V_{IL}$ could not be defined. The substantial noise margin compression observed under microwave interference, can cause serious logic errors in interconnected units and make digital systems vulnerable to bit errors.

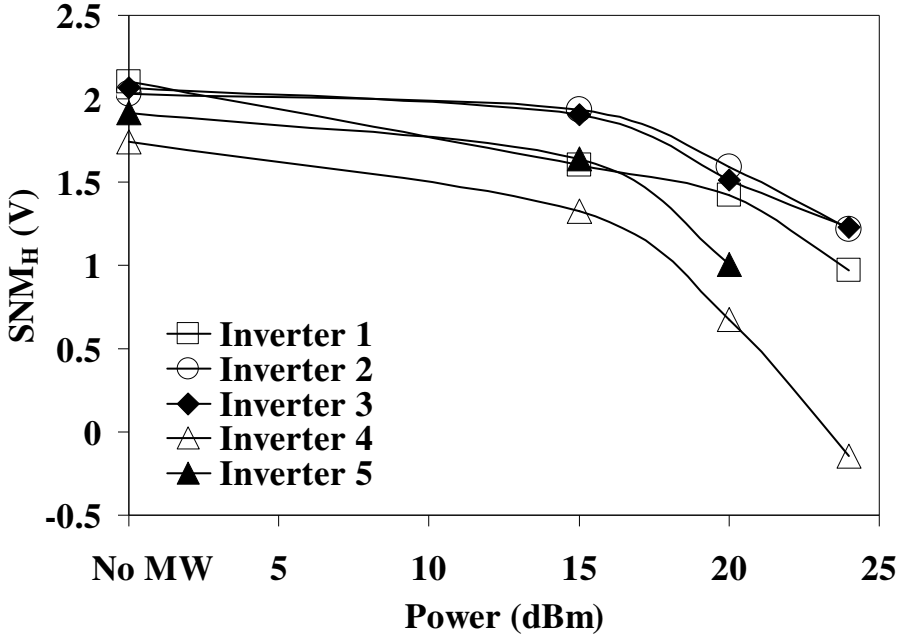



Figure 3. 8 (a).

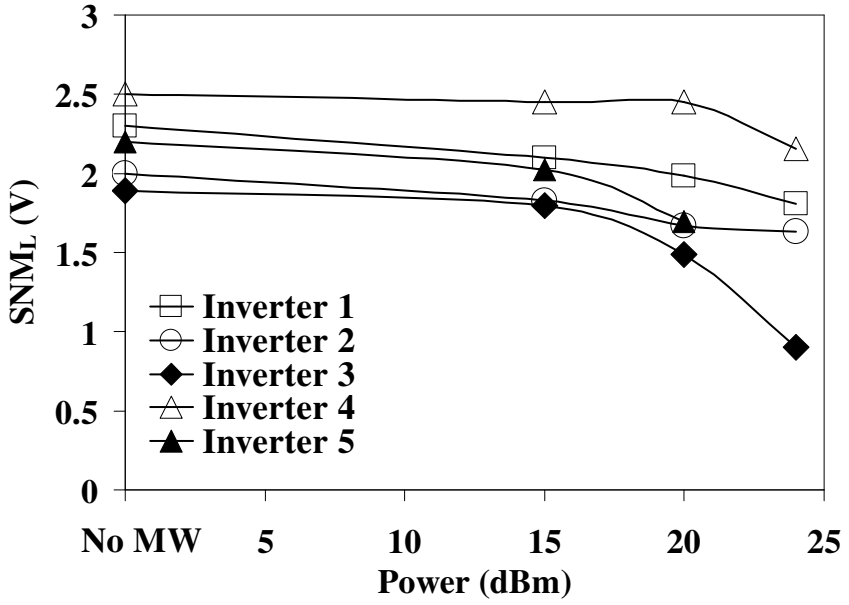



Figure 3. 8 (b).

Figure 3. 8 (a) Measured static noise margin high ($SNM_H$) of the five inverters under 1GHz microwave interference. Significant compression of noise margin after 15dBm is observed. (b) Measured static noise margin low ($SNM_L$) of the five inverters under 1GHz microwave interference. Significant compression is also observed.

### 3. 3. 2 Regenerative Signal Properties

The integrity of the noise margins is the most critical aspect to maintain the ability to reject noise and retain the regenerative signal property of inverters in digital systems. The regenerative signal property can be explained using the schematic of input and output voltage ranges shown in Figure 3. 9. From the schematic, the input signal residing in the input voltage range for logic 1 (between $V_{DD}$ and $V_{IH}$) will map into the output voltage range (between $V_{OUL}$ and $V_{OL}$) for logic 0, and vice-versa. Region X represents the region where a bit cannot be determined. Under normal conditions, the input voltage ranges are larger than the output voltage ranges. As long as fluctuations of input signals (see illustration in Figure 3. 9) due to noise remain within the input voltage range (between $V_{DD}$ and $V_{IH}$) for logic 1 where the gain is low, the output will also remain within the output voltage range (between $V_{OUL}$ and $V_{OL}$) for logic 0. As a result, the next few inverters would attenuate the noise even further and be immune to the noise. However, if the output voltage ranges were comparable to or larger than the input, a small fluctuation in the input would produce a bit error as the signal propagates through subsequent inverters [34]. As shown in Figure 3. 10 (a), the input voltage range of inverter 1 measured without microwave interference, is observed to be larger than the output voltage range, which is in good agreement with the regenerative principle. However, Figure 3. 10 (b) shows that the

device suffers from significantly reduced input voltage range and increased output voltage range for logic 1 with 1GHz, 24dBm microwave interference. Especially, the input voltage range for logic 1 (1.2V) is now comparable to the output voltage range for logic 0 (0.7V), indicating the loss of noise immunity and the signal regenerative property. This degradation in the regenerative signal property would result in bit errors even under small signal fluctuations in the input, as will be discussed further in section V for cascaded inverter clusters. Furthermore, when CMOS technology is scaled down, bias voltages ($V_{DD}$) and noise margins are scaled down as well, resulting in smaller noise margins under normal operating conditions. Therefore, microwave interference will affect the devices more severely, and upsets will be caused even at lower power levels.

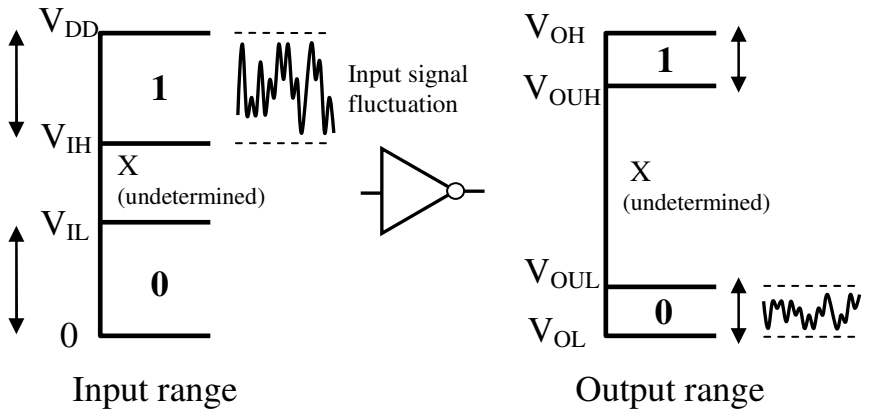



Figure 3. 9 Typical schematic representation of input and output voltage ranges for an inverter circuit.

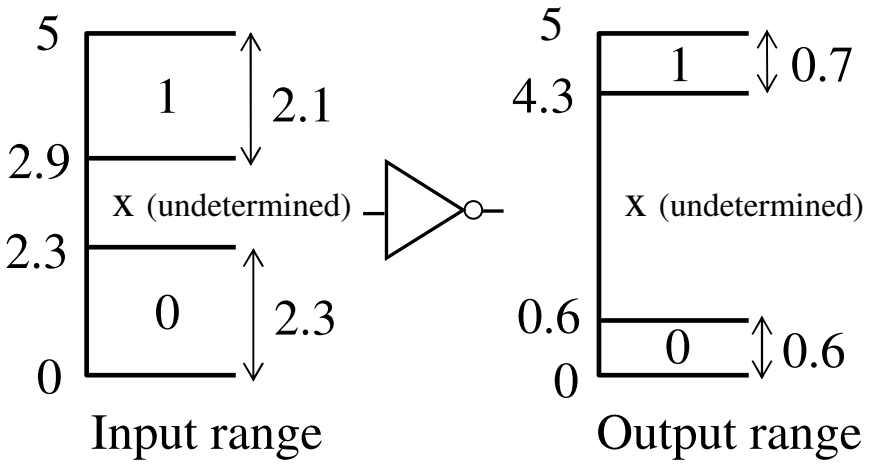



Figure 3. 10 (a)

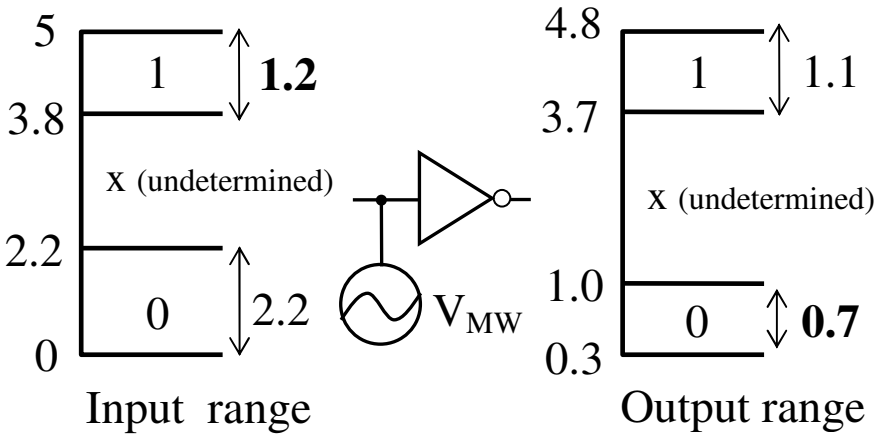



Figure 3. 10 (b)

Figure 3. 10 (a) Schematic representation of input and output voltage ranges of inverter 1 without microwave interference, using measured values. The input voltage ranges are larger than the output voltage ranges showing a good regenerative property. (b) Schematic representation of input and output voltage ranges of inverter 1 with 1GHz microwave interference, using measured values. Significantly reduced input voltage range (from 2.1 to 1.2) and increased output voltage range for logic 1, indicating the loss of noise immunity and the signal regenerative property.

## *3. 4 Current Transfer Characteristics and Static Power Dissipation*

### 3. 4. 1 Current Transfer Characteristics

In this section the current transfer characteristics (CTCs), and the load-line characteristics are measured with and without microwave interference, in order to evaluate the static power dissipation in the inverters. The CTCs of individual inverters are shown in Figure 2 (dashed line). Depending on the state (ON or OFF) at the output, one of the MOSFETs in the inverter is ON and thus, acts as an active load while the other is OFF. This makes the output current ($I_O$) from $V_{DD}$ to ground to be very small and results in low power dissipation. Figure 3. 11 shows the measured CTCs of inverter 1 with a 1GHz microwave signal. The graph shows a gradual increase in the output current and a shift in the maximum current point ($I_{Omax}$) toward higher $V_{IN}$ voltages (i.e. from 2.56V to 3V) as the microwave power increases. It is also evident that the n-MOS and p-MOS devices in the inverter cannot be turned ON and/or OFF, allowing significant current to flow at the logic 1 and/or 0 states. This is due to the changes in the Q point of operation resulting from substantial increase in the currents of the n and p-MOS devices as we observed in Figure 3. 5. Measured output currents at the ON state were 88.7μA with 1GHz, 24dBm microwave interference and 17.4nA without interference while output currents at the OFF state were 0.11mA with 1GHz, 24dBm microwave interference and 12.6nA without interference, showing 3 to 4 orders of magnitude increase in the output currents at ON and OFF states. Hence, the device suffers from elevated static power dissipation at

the stand-by (ON or OFF) states, defined as follows:

$$P_{ON} = V_{DD} I_{O(ON)} \tag{3. 14}$$

$$P_{OFF} = V_{DD} I_{O(OFF)} \tag{3. 15}$$

where, $P_{ON}$ and $P_{OFF}$ are the static power dissipation at the ON and OFF states, respectively, and $V_{DD}$, $I_{O(ON)}$, and $I_{O(OFF)}$ are the bias voltages, output currents at the ON state, and output currents at the OFF state, respectively.

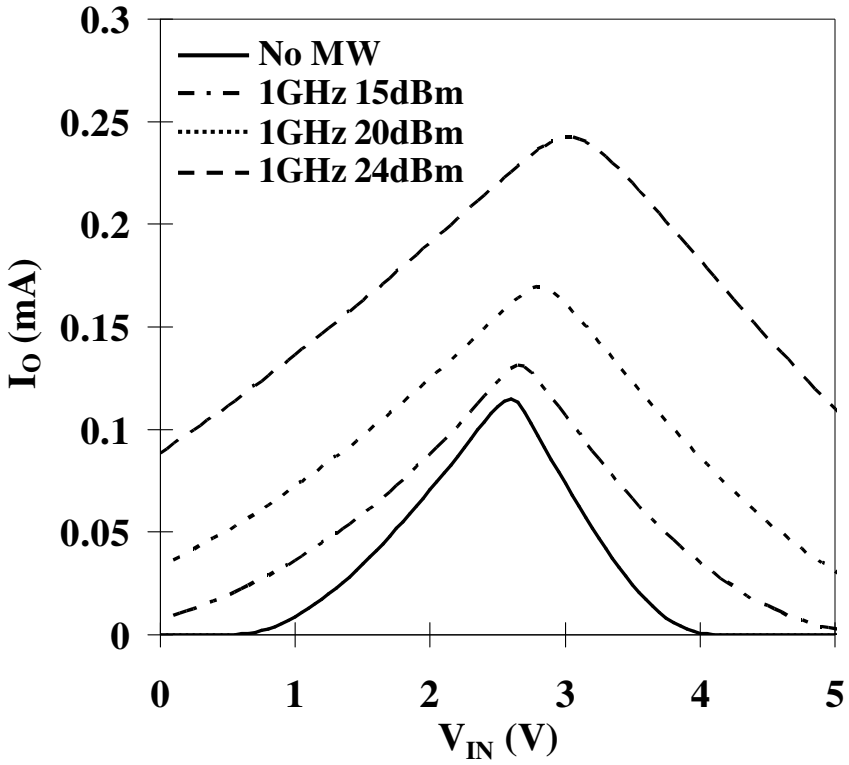



Figure 3. 11 Measured current transfer characteristics (CTCs) of inverter 1 with 1GHz microwave interference.

### 3. 4. 2 Static Power Dissipation

The static power dissipation of the five inverters, measured at stand-by states with a 1GHz microwave signal, is shown in Figure 3. 12 (a) and (b). The graphs show gradual increase in static power dissipation and more substantial increases above 15dBm of microwave power. This results in a 1 to 4 orders of magnitude increase for the ON state and a 3 to 6 orders of magnitude increase for the OFF state. From the graph, inverter 3 and 5 showed the most substantial increase in static power dissipation. Although the absolute $P_{ON}$ value of Inverter 3 is larger than the one of Inverter 5 (Figure 3. 12 (a)), the relative $P_{ON}$ increase of Inverter 5 shows 2 orders of magnitude larger than the one of Inverter 4, indicating that the smaller devices are more vulnerable to the interference.

This demonstrates a significant vulnerability in the power budget of the devices due to microwave interference. As the scaling down of CMOS technology progresses, minimizing overall power consumption becomes one of the most important design goals, further restricting the power budget for the IC design. Thus, the amount of power assigned from the total budget, needs to be precisely determined for each device, reducing the tolerance levels for power variation. Therefore, a 3 to 6 orders of magnitude increase in the static power dissipation at stand-by states makes the device draw excess current continuously from the power rails, depriving other devices of power and increasing the load on interconnects and contacts, not rated for such levels of continuous power. This can cause elevated temperatures at the metallizations, which eventually results in catastrophic failure. Therefore, the entire system experience a significant disturbance of power budget distribution from the

power rails to each individual device, resulting in local soft and/or hard errors at first, and then in entire system failure.

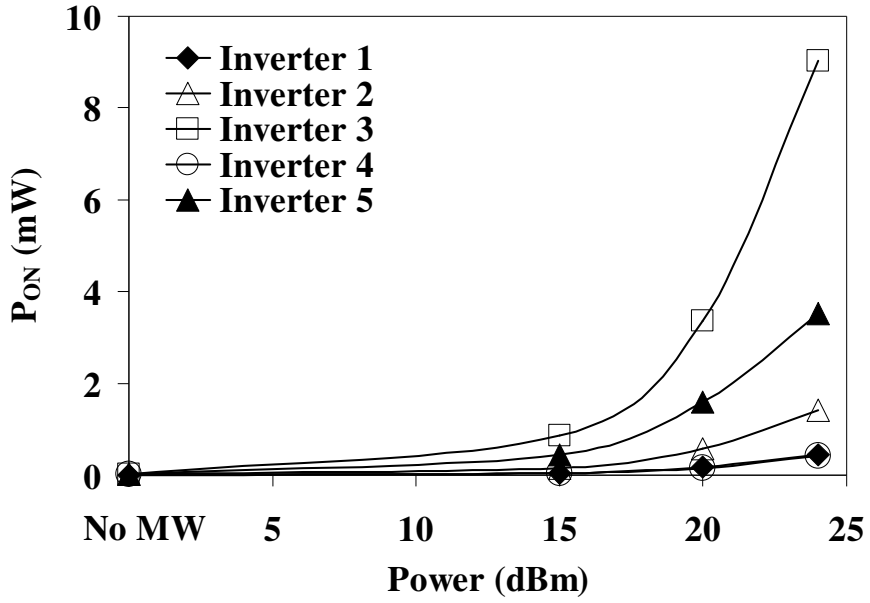



Figure 3. 12 (a).

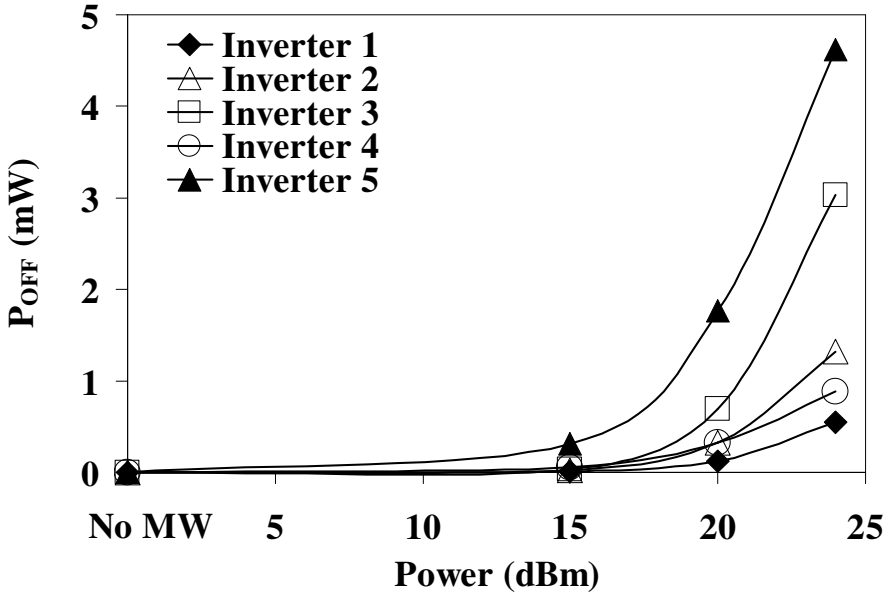



Figure 3. 12 (b)

Figure 3. 12 (a) Measured static power dissipation of the five inverters at the "ON" output state under 1GHz microwave interference. Significantly increased power dissipation is observed after 10dBm. Inverter 5 shows a relatively larger increase in the power dissipation than Inverter 3 does, indicating that the smaller devices are more vulnerable to the interference. (b) Measured static power dissipation of the five inverters at the "OFF" output state under 1GHz microwave interference, showing also a substantial increase after 10dBm.

## ***3. 5 Frequency Effects***

The current transfer characteristics of inverter 1 are measured when a 24dBm microwave interference with frequency varying between 0.8 and 3GHz, is applied at the input. As shown in Figure 3. 13, most pronounced changes are observed in the frequency range between 0.8 and 1GHz, while at 3GHz the effects are suppressed, in good agreement with our previous experiments on single MOSFETs [2].

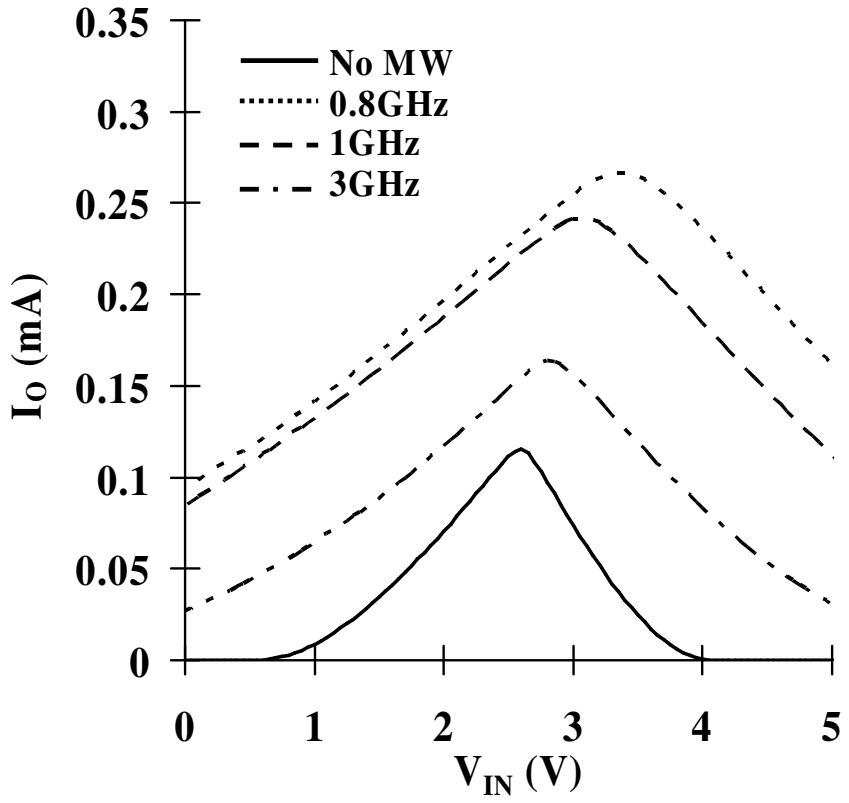



Figure 3. 13 Measured current transfer characteristics (CTCs) under 24dBm microwave interference. Frequency varies from 0.8GHz to 3GHz.

Since the inverter is composed of the bias dependent non-linear small signal capacitances, the characteristics of the device strongly depend on the frequency and input voltage conditions. Among all small signal capacitances, gate to drain overlap capacitances ($C_{oln}$, $C_{olp}$), gate to ground capacitances ($C_{gs}$, $C_{gd}$), and drain to ground capacitance ($C_{dbn}$,$C_{dbp}$), are known to be the dominant capacitances [34],[2]. As a result, these capacitances provide a by-pass path to ground for the interference at the higher frequency range, resulting in the suppression of the interference effects.

## *3. 6 Effects of Microwave Interference on Cascaded Inverters*

In order to evaluate the effects of microwave interference on the noise immunity of cascaded inverters, the voltage transfer characteristics, static noise margins, and input/output voltage ranges of cascaded inverters, were studied. The cascaded inverters consist of three individual inverters. The voltage transfer characteristics and input/output voltage ranges of the cascaded inverters are measured under a 1GHz microwave interference of varying power applied first into the input of the first stage inverter, then into the input of the second, and then into the third stage inverter, as shown in Figure 3. 14.

Figure 3. 15 shows the VTC of the whole cluster. Most pronounced effect in the VTC of the cluster, was obtained (dashed line) when the interference was applied into the third stage inverter. With 1GHz 24dBm, the voltage transfer characteristic ($V_{IN}$-$V_{O3}$) shows substantial increase in $V_{OL}$ from 0 to 3.54V, where $V_{IN}^{If\ MW}$ can not be defined. Gain at the high gain region decreased by a factor of 60.

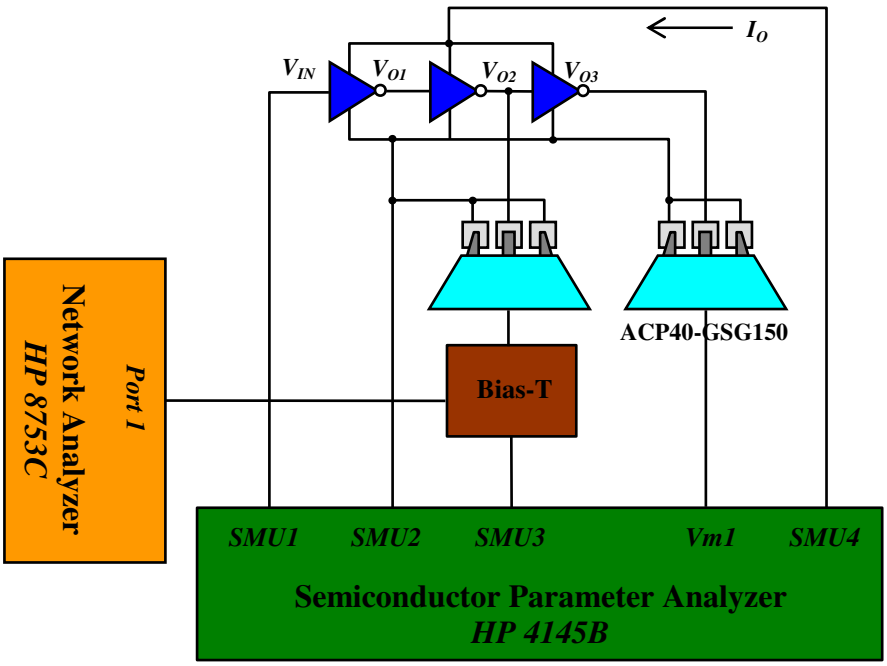



Figure 3. 14 Measurement set up schematic for cascaded inverter clusters. Each inverter is the same as inverter 1.

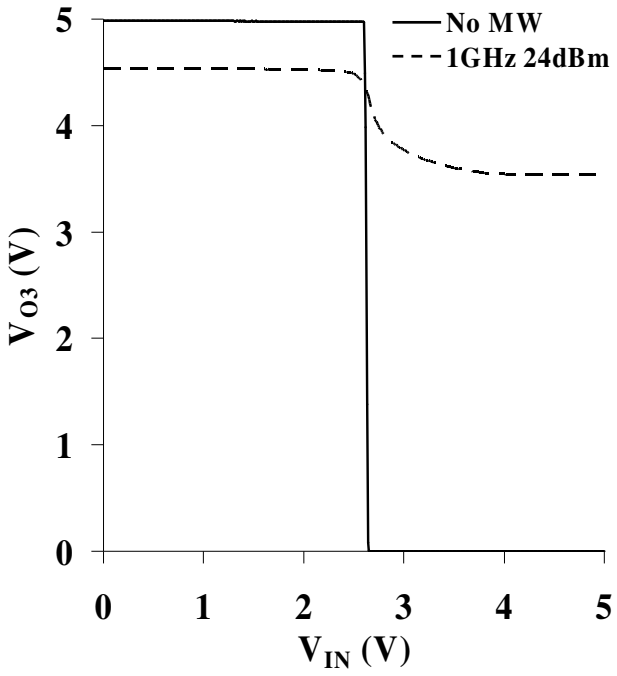



Figure 3. 15 Measured voltage transfer characteristics ($V_{IN}$-$V_{O3}$) with a 1GHz, 24dBm microwave interference signal.

Without interference, $SNM_H$ and $SNM_L$ were measured to be 2.33V and 2.6V, respectively, demonstrating excellent noise immunity. However, at 1GHz 24dBm, $SNM_H$ and $SNM_L$ decreased to 1.64V, and –0.98, respectively, compressing noise margins severely.

Without interference, as the input signal ($V_{IN}$) propagates through the inverters, the undetermined range (X), and the output voltage ranges get smaller, while the input voltage ranges get larger as shown in Figure 3. 16 (a). The input voltage ranges for logic 1 and 0 are 2.35V and 2.6V, respectively, and the output voltage ranges for logic 1 and 0 are 0.01V and 0V, which results in high gain (99.4V/V), and a very small undetermined region (0.05V), appropriate for high noise immunity and good signal regenerative properties. However, with interference, the output voltage ranges are severely compressed due to the degradation of $V_{OH}$ and $V_{OL}$, as shown in Figure 3. 16 (b), where the output voltage ranges of the cluster are now between 4.53V and 3.54V regardless of the input logic voltage ($V_{IN}$). Therefore, the cascaded inverter cluster produces bit-errors at the output, as shown in Figure 17, which propagate to the next stage to result in full bit-flip errors. This demonstrates critical vulnerability issues in digital systems under interference, due to static noise margins, and input/output voltage range compression.

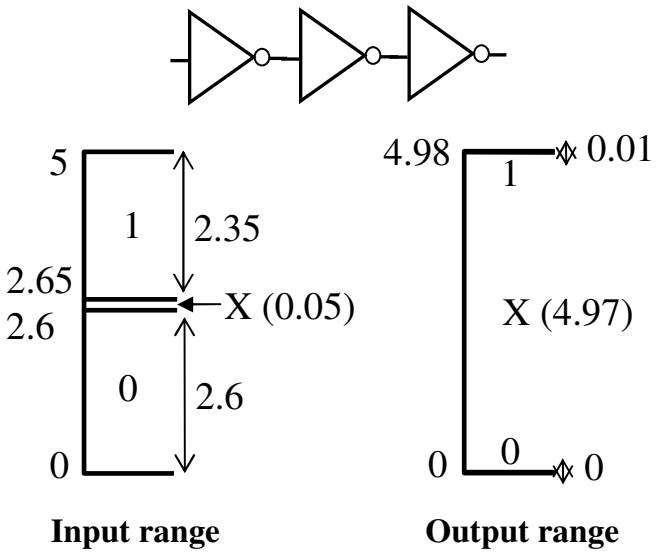



Figure 3. 16. (a)

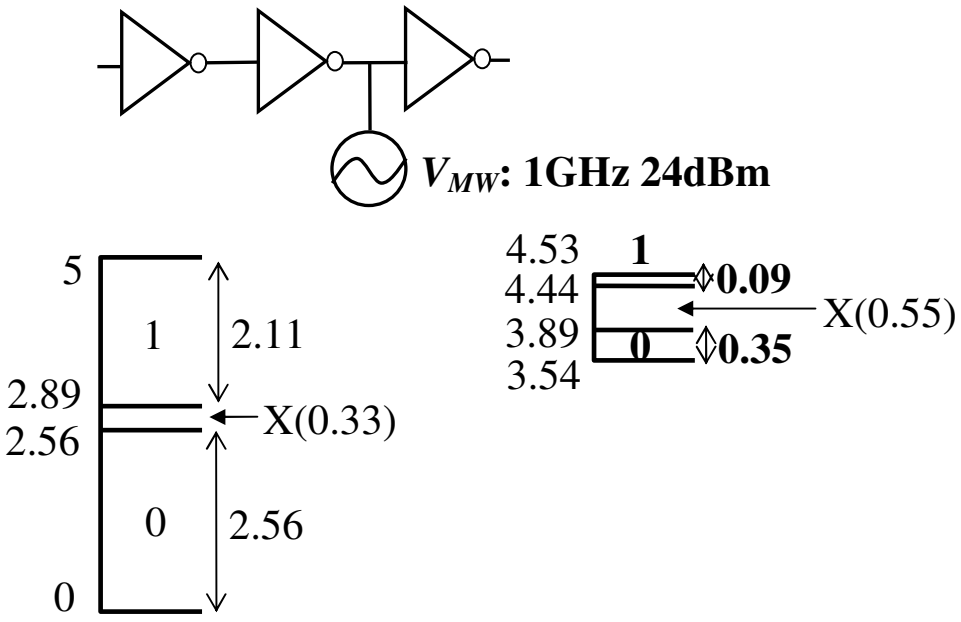



Figure 3. 16 (b)

Figure 3. 16 (a) Measured input and output voltage ranges of cascaded inverter clusters without microwave interference. These near ideal inverters will have a large input range for high and low with a very small undetermined region resulting in a sharply defined output high (0.01V) and low (0V) states and a large undetermined region (4.97V). Figure 3. 16 (b). Measured input and output voltage ranges of

cascaded inverter clusters under 1GHz 24dBm interference, showing severe compression of the output ranges leading to errors.

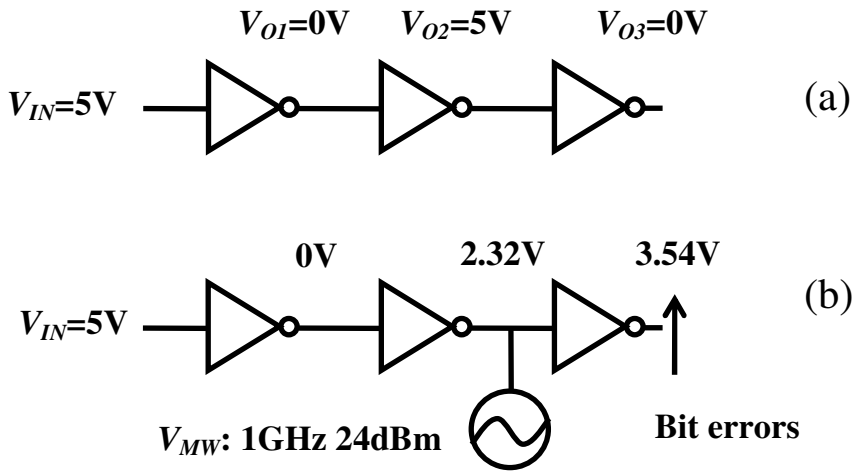



Figure 3. 17 (a) Measured responses of cascaded inverter clusters when $V_{IN}$=5V without microwave interference. No error is observed. (b). Measured responses of cascaded inverter clusters when $V_{IN}$=5V under 1GHz 24dBm microwave interference. Bit error from 0V to 3.54V is observed at the output of the third inverter.

## *3. 7 Summary*

Microwave interference on CMOS inverters revealed significant operational vulnerabilities due to significant changes in the static characteristics of the devices, the gain, the noise margins, the static power dissipation, the input/output voltage ranges, and the load-line characteristics. The upsets under interference can be mainly attributed to the shift of the Q point of operation in the voltage transfer characteristics and load-line characteristics. This shift results from the asymmetric substantial increase in the current driving capabilities of the n and p-MOS devices of the

inverters, changing the inflection voltage ($V_{IN}^{If}$), and output voltages ($V_{OH}$, and $V_{OL}$). Furthermore, significant reduction in the transconductance ($g_m$) is observed, resulting in gain reduction by a factor of 6 to 24. Compressed static noise margins, severely degraded noise immunity and, hence, invalidated the regenerative signal properties of the digital system, introducing bit errors in cascade inverter clusters. Due to the substantial increase in the output current, the static power dissipation at the ON and OFF states showed several orders of magnitude increase, which can lead to catastrophic failures due to elevated current and temperature stress at the device contacts and interconnects, that are not designed for such current levels.

# Chapter 4: Dynamic Operation and Power Dissipation of CMOS Inverters under Microwave Interference

In the present chapter, we introduce a new analytical parameter extraction method that can be used to obtain the dynamic characteristics of the inverters under high power microwave interference. Using the method, we focus on characterizing and identifying the effects of microwave interference on the dynamic characteristics of CMOS inverters such as output voltages and currents, propagation delays, and dynamic power dissipation. Using the method and SPICE model, we predicted the upsets in timer circuits under CW microwave interference and the predicted result was validated by comparing with measured result.

## *4. 1 Experimental Details*

The CMOS inverters in this work were designed and fabricated as individual inverter units. Each inverter unit has a width to length ratio (W/L) of 3.2μm/1.6μm for the n-MOS and 9.6μm/1.6μm for the p-MOS device. In order to investigate the relation between device size and vulnerability to microwave interference, inverters with 1.2μm/0.6μm (n-MOS) and 3.6μm/0.6μm (p-MOS), were also fabricated. Measurements with and without microwave interference were performed on-chip at the input and output of the devices, using microwave probes with a coplanar waveguide and a ground-signal-ground (G-S-G) probe pattern having 150μm pitch, on a coplanar probe station. The current-voltage, and load line characteristics were measured using the HP4145B semiconductor parameter analyzer when a controlled

microwave signal and a $V_{IN}$ input varying between 0V and 5V (or 0V and 3.3V in the scaled down inverter units) in increments of 0.1V, was applied at the input of the devices through a bias-T, as shown in Figure 4. 1 (a). The power and frequency of the microwave signal were varied between 0 and 24dBm, and 800MHz and 3GHz, respectively.

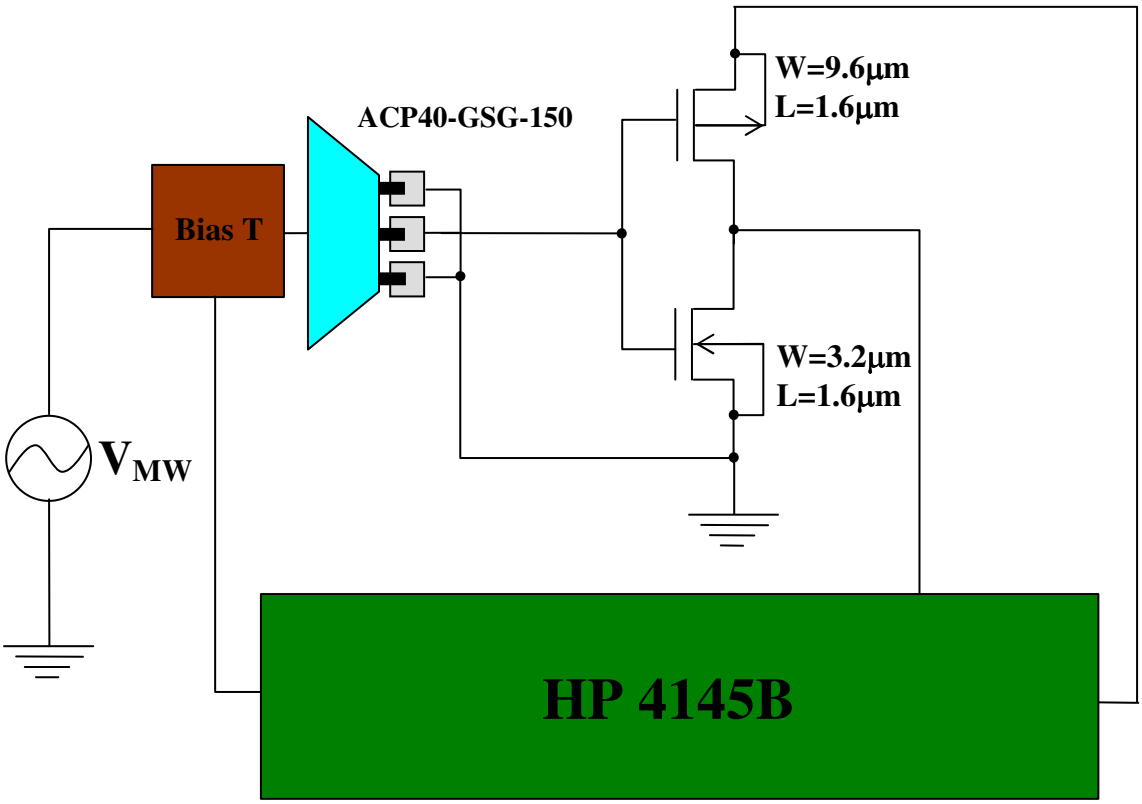



Figure 4. 1 (a)

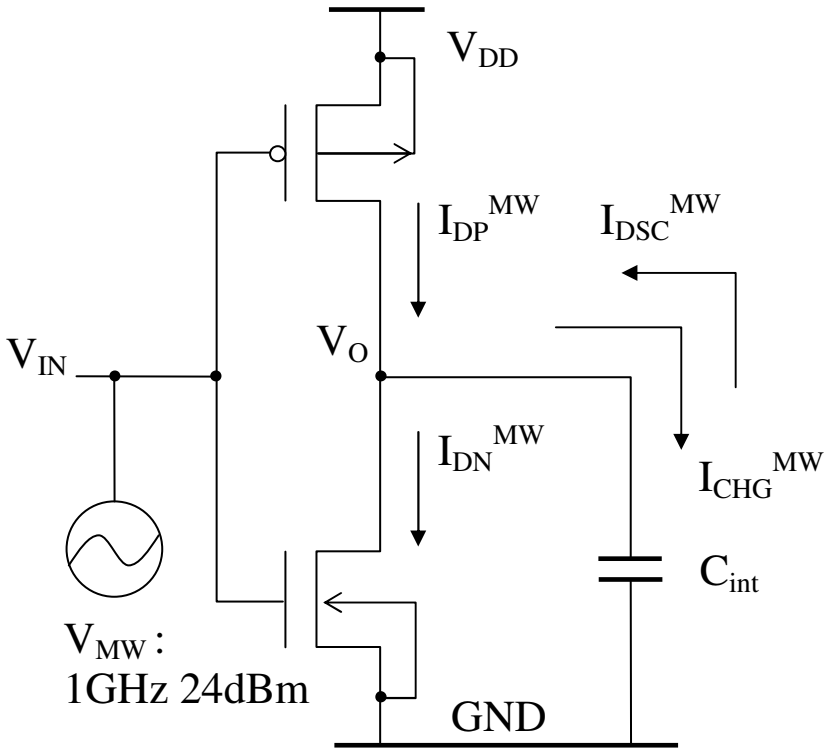



Figure 4. 1 (b)

Figure 4. 1 (a) Schematic of the measurement set-up for microwave interference effects on unpackaged CMOS inverters. (b) Schematic of a CMOS inverter. The intrinsic capacitance ($C_{\text{int}}$) is modeled as an equivalent load capacitance at the output. Note that $C_{\text{int}} = C_{dbn} + 2C_{o\ln} + C_{dbp} + 2C_{olp}$.

## ***4. 2 Dynamic Operation of CMOS Inverters under Microwave Interference***

Microwave interference may affect the intrinsic propagation delay, through changes in the switching capability of the inverter, which will in turn affect dynamic power dissipation. This is an important metric for dynamic logic circuits where the

data signals need to be synchronized with the periodic clock signals. Although analytical models proposed previously [47-49] allow us to predict the dynamic parameters of operation in inverters under normal operating conditions, they cannot be safely applied under microwave interference due to the unpredictable and severe changes induced in the characteristics of the devices [2], making operational parameter extraction impractical. Therefore, it is necessary to develop a method to predict and evaluate the effects of microwave interference on the dynamic operation of the inverters. In the following chapters we propose the analytical parameter extraction method, which allows us to calculate the propagation delays, the changes in output voltages and currents, and the dynamic power dissipation due to microwave interference, from experimentally measured load-line characteristics.

### 4. 2. 1 Intrinsic and Fan-Out Capacitances of CMOS Inverters

The dynamic operation of CMOS inverters depends on output currents $i_{DN}$, $i_{DP}$, $i_{CHG}$, and $i_{DSC}$, output voltage ($V_O$), and load capacitance. The load capacitance consists of intrinsic and fan-out capacitances. For the case that the output of the inverter is connected to other gates, the fan-out capacitances are defined as the sum of the equivalent capacitances of those gates. Since a single inverter is considered in our study, the intrinsic capacitance will also be the load capacitance. The n and p-MOS transistors in the inverter are always ON or OFF in a complementary fashion. Thus, the gate-to-drain overlap capacitances ($C_{oln}$, $C_{olp}$) and the drain-to-substrate junction capacitances ($C_{dbn}$, $C_{dbp}$) will be dominant. These are the ones to be considered as contributing to the intrinsic capacitance ($C_{\text{int}}$) of the inverter (Equation 4. 1).

Therefore, the inverter can be expressed as an equivalent circuit model having the intrinsic capacitance ($C_{\text{int}}$) at the output (Fig. 4. 1. (b)). The charging and discharging current relation are given in Figure 4. 1. (b). Since the gate-to-drain overlap capacitances ($C_{oln,}$ $C_{olp}$) experience a voltage swing of $2V_{DD}$ ($V_{IN}$: $0 \rightarrow V_{DD}$, $V_O$: $V_{DD} \rightarrow 0$), the capacitances are expressed at the output as $2C_{oln}$ and $2C_{olp}$ due to the Miller effect [34]:

$$C_{\text{int}} = C_{dbn} + 2C_{o\ln} + C_{dbp} + 2C_{olp} \tag{4. 1}$$

where the *n* and *p* in the subscript *dbn, oln, dbp,* and *olp* represent n and p-MOS devices. The gate-to-drain overlap capacitance is expressed in Equation 4. 2 [50] as:

$$C_{ol} = \frac{\varepsilon_{ox}}{t_{ox}} L_d W \tag{4. 2}$$

where $\varepsilon_{ox}$ =3.97×8.854 aF/μm is the dielectric constant of the gate oxide, $t_{ox}$ is the thickness of the oxide, $L_d$ is the depletion width of the drain junction under the gate, and $W$ is the width of the inverter. The drain-to-substrate junction capacitance is composed of the periphery part $C_{jsw}$ and the depletion capacitance $C_j$ between the diffused junction and substrate under the drain. The drain-to-substrate capacitance ($C_{db}$) is given by:

$$C_{db} = \frac{C_{jsw} + C_j}{\sqrt{1 + V_{DB} / \phi_B}} \tag{4. 3}$$

$$C_{jsw} = C_{jswo}(W + 2Y) \tag{4. 4}$$

$$C_j = C_{jo} WY \tag{4. 5}$$

where $V_{DB}$ is the reverse bias on the drain-substrate junction, $\phi_B$ is the built-in potential, $C_{jswo}$ is the drain periphery capacitance at zero bias, $C_{jo}$ is the drain substrate junction capacitance at zero bias, $W$ is the width of the device, and $Y$ is the length of the drain and source regions ($2Y$) [51]. The calculated capacitance values of the CMOS inverters used in this work, are given in Table 4. 1. These are the values used in evaluating the dynamic operation of the inverters.

| | $C_{int}$ | $C_{dbn}$ | $C_{oln}$ | $C_{dbp}$ | $C_{olp}$ |
|---|---|---|---|---|---|
| 1.6μm ($V_{DD}$=5V) | 8.52fF | 0.92fF | 0.55fF | 2.54fF | 1.98fF |
| 0.6μm ($V_{DD}$=5V) | 4.1 fF | 0.41fF | 0.25fF | 1.15fF | 1.02fF |
| 0.6μm ($V_{DD}$=3.3V) | 4.38fF | 0.48fF | 0.25fF | 1.36fF | 1.02fF |

Table 4. 1 Calculated intrinsic, gate-to-drain overlap, and drain-to-substrate capacitances of 1.6μm and 0.6μm CMOS inverters with bias voltages of 3.3V and/or 5V.

## 4. 2. 2 Analytical Parameter Extraction Method and Prediction of Dynamic Operation with a Step Input

In this section, we focus on investigating the change in currents and voltages at the output of the inverter due to microwave interference when the input to the inverters is an ideal step input. This analysis combined with the analysis presented in the following section using a ramp input provides a more realistic input signal consisting of three sections, namely, a rising ramp, a steady state (step), and a falling

ramp signal. The dynamic operation of the inverter at the output, as the step input changes its state from logic low ($V_{IL}$) to logic high ($V_{IH}$), can be expressed as follows:

$$-i_{DSC}(t) = C_{\text{int}} \frac{dV_O}{dt} \tag{4. 6}$$

where $i_{DSC}(t) = i_{DN}(t) - i_{DP}(t)$ by Kirchhoff's current law (KCL). $i_{DSC}(t)$, $i_{DN}(t)$, $i_{DP}(t)$, and $V_O$ represent the discharging current, the drain current of the n-MOS, the drain current of the p-MOS, and the output voltage, respectively. Similarly, when the step input changes from logic high to low, the expression is given in Equation (4. 7):

$$i_{CHG}(t) = C_{\text{int}} \frac{dV_O}{dt} \tag{4. 7}$$

where $i_{CHG}(t) = i_{DP}(t) - i_{DN}(t)$ is the charging current. For the former case, let us consider that the step input transits from $V_{IL}$ to $V_{IH}$ in $t = t_1$. As the input state changes to $V_{IH}$, the output voltage ($V_O$) starts to decrease gradually from $V_{OH}$ due to the discharging at the intrinsic capacitance, and this can be quantified by measuring the static load-line characteristics of the inverter, and following the trajectories of the currents. The measured load-line characteristic of the 1.6μm inverter, is shown in Figure 4. 2.

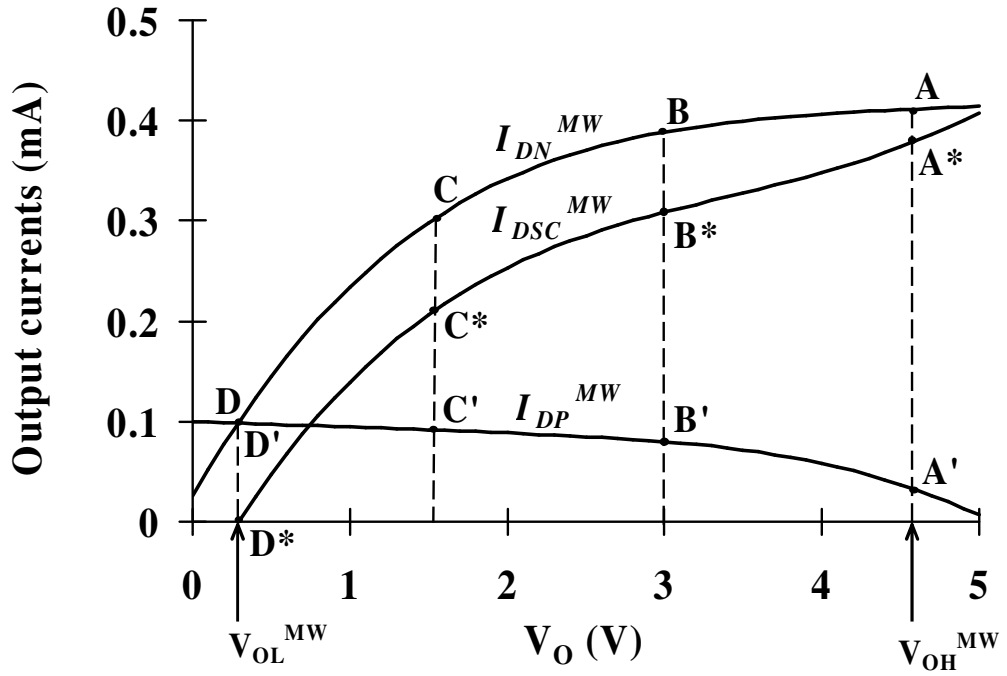



Figure 4. 2 Measured load line characteristics of the 1.6μm inverter, showing output currents under 1GHz, 24dBm microwave interference. The transition of the output currents and voltages ($I_{DN}^{MW}$, $I_{DP}^{MW}$, $I_{DSC}^{MW}$, $V_{OH}^{MW}$, and $V_{OL}^{MW}$) are displayed when $V_{IN}$ changes from $V_{IL}$ to $V_{IH}$.

Due to substantial increase in $I_{DP}^{MW}$ and $I_{DN}^{MW}$ under the interference, the quiescent operating voltage point increased from 0V without interference to $V_{OL}^{MW}$ with 1GHz 24dBm interference. As shown in the figure, the trajectories of currents ($I_{DN}^{MW}$, $I_{DP}^{MW}$, and $I_{DSC}^{MW}$) during discharging are along the path A-B-C-D, A'-B'-C'-D', and A*-B*-C*-D* respectively as the input voltage changes from 0V to 5V, and the relation between the currents is given by Equation 4. 8:

$$I_{DSC}^{MW} = I_{DN}^{MW} - I_{DP}^{MW} \tag{4. 8}$$

The currents are given in capital letters to indicate that the data obtained from the load-line characteristics represent time independent static information. In order to investigate the dynamic characteristics of the inverter, it is necessary to solve Equation 4. 6 as follows:

$$-\int_{t1}^{t2} i_{DSC}(t)dt = C_{\text{int}} \int_{V_1}^{V_2} dV_O \tag{4. 9}$$

For a sufficiently small time increment, the change in output voltage ($V_O$) can also be considered sufficiently small that the discharging current can be represented with a linear function of time, as given in Equation 4. 10 below:

$$i_{DSC}(t) = at + b \tag{10}$$

where $i_{DSC}(t) = i_{DN}(t) - i_{DP}(t)$ in lower case letters to indicate time varying components. Time ($t$) is then set as shown in Equation 4. 11, with the assumption that the time interval between two adjacent times is sufficiently small.

$$t = t_1, t_2, t_3, \ldots\ldots, t_n \tag{4. 11}$$

where $t_1$ is taken to be a known initial value and the others are unknown. The corresponding output voltage ($V_O$) values for each time are given in Equation 4. 12, and can be generalized in Equation 4. 13:

$$V_O = V_1, V_2, V_3, \ldots\ldots, V_n \tag{4. 12}$$

$$V_m = V_{m-1} - V_a \quad (m = 2, 3, \ldots\ldots, n) \tag{4. 13}$$

where, $V_1 = V_{OH}$ and $V_n = V_{OL}$ (output high and output low: known values), and $V_a$ is sufficiently small that the linearity condition in Equation 4. 10 is satisfied. Since each time set ($t_1, t_2, t_3, \ldots\ldots, t_n$) is mapped to the static output voltage set ($V_1, V_2, V_3, \ldots\ldots, V_n$), the corresponding discharging current set ($i_{DSC}(t_1), i_{DSC}(t_2), i_{DSC}(t_3), \ldots\ldots,$

$i_{DSC}(t_n)$) can be obtained from the measured load-line characteristics by examining $I_{DSC}$ at each output voltage ($V_1$, $V_2$, $V_3$, …… , $V_n$). Consider the case of $t_1 \le t \le t_2$, then $V_2$ associated with $t_2$ is set to be $V_1 - V_a$, and the unknown $t_2$ is guessed and labeled as $t_{2(1)}$. Based on $i_{DSC}(t_1)$, $i_{DSC}(t_2)$, $t_1$, and the guessed $t_{2(1)}$, the $i_{DSC}(t)$ is obtained from Equation 4. 10, and Equation 4. 9 is solved with respect to $t_2$ as follows:

$$-\left(\frac{at^2}{2}+bt\right)\Bigg|_{t1}^{t2} = C_{\text{int}}(V_2 - V_1) \tag{4. 14}$$

$$\frac{at_2{}^2}{2}+bt_2-\left(\frac{at_1{}^2}{2}+bt_1\right)+C_{\text{int}}\left(V_2-V_1\right)=0 \tag{4. 15}$$

Set $\quad \frac{a}{2}\equiv X, \quad b\equiv Y, \quad -\left(\frac{at_1{}^2}{2}+bt_1\right)+C_{\text{int}}\left(V_2-V_1\right)\equiv Z$

$$Xt_2{}^2+Yt_2+Z=0 \tag{4. 16}$$

$$t_{2(2)}=\frac{-Y\pm\sqrt{Y^2-4XZ}}{2X} \tag{4. 17}$$

where the solution of the quadratic equation is labeled as $t_{2(2)}$ in Equation 4. 17 in order to distinguish it from the guessed value $t_{2(1)}$. If these two values are different, meaning the initial guess is wrong, then a new discharging current $i_{DSC}(t)$ has to be calculated based on the $t_{2(2)}$ value (now $t_{2(2)}$ is set as the second guess value), and the previous procedure is to be repeated. The iteration continues until the solution of the quadratic equation converges to the previous guessed value ($t_{2(n)} = t_{2(n-1)}$). This converged value represents the time required for the output voltage and the discharging current to change from $V_1$ to $V_2$ and $i_{DSC}(t_1)$ to $i_{DSC}(t_2)$, respectively. For

the next time period ($t_2 \leq t \leq t_3$), the previous processes can be applied where the converged solution from the previous time period is now the initial condition. This process is repeated until a converged solution for the final condition ($V_O$=$V_{OL}$) is obtained. By considering Equation 4. 7 and the initial conditions, the transition of the ideal step signal from high to low ($V_{IH}$ to $V_{IL}$) can be analyzed in the same fashion.

When microwave interference is applied to the input of the inverter, the procedure to investigate the dynamic operation of the device follows exactly the same process except for the initial and final conditions in the output voltage set. From the voltage transfer characteristics measured under microwave interference, the output voltages between $V_{OH}^{MW}$ and $V_{OL}^{MW}$ can be extracted, and the output voltage set ($V_O^{MW}$=$V_1^{MW}$, $V_2^{MW}$, …… , $V_n^{MW}$), generalized as $V_{OH}^{MW}$, $V_{OH}^{MW} - V_a^{MW}$, …… , $V_{OH}^{MW} - (n-1)V_a^{MW}$ , can be obtained. $V_a^{MW}$ is again a sufficiently small value that satisfies the linearity condition of Equation 4. 10.

## 4. 2. 3 Analytical Parameter Extraction Method and Prediction on Dynamic Operation with a Ramp Input

In this section, a ramp signal is considered as the input of the inverter for investigating the dynamic operation of the device. For simplicity, the ramp signal is considered as an ideal ramp signal having $t_r$ (rise) or $t_f$ (fall) transient periods. During the transient period, the input voltage ($V_{IN}$) increases or decreases linearly from $V_{IL}$ to $V_{IH}$ or $V_{IH}$ to $V_{IL}$ respectively. Therefore, the ramp has a gradient of $(V_{IH} - V_{IL})/t_r$ or $(V_{IL} - V_{IH})/t_f$ in the transient period. For a small increase in input voltage ($V_{IN}$), and a short time increment, $i_{DN}$, $i_{DP}$, $i_{DSC}$, and $i_{CHG}$ can be considered to be linear functions

with time. Hence, we can apply the expression used in Equation 4. 6 and 4. 7. Now the input voltage ($V_{IN}$) and time ($t$) are well defined during the period. Thus, in order to analyze the dynamic operation of the device, it is necessary to find the unknown output voltage ($V_O$) at each time set ($t$) from Equation 4. 6 and 4. 7. For $0 \leq t \leq t_r$, set time (t) as follows:

$$t = t_1,\ t_2,\ \ldots\ldots,\ t_n \tag{4. 18}$$

where, the relation can be generalized as $t_m = t_{m-1} + t_a$, ($m = 2, \ldots\ldots, n$). It is noted that $t_a$ is taken to be a small value so that the linearity condition of Equation 4. 10 is again satisfied. Due to the gradient of the ramp signal at the transient period, the corresponding input voltage ($V_{IN}$) at each time is designated as $V_{IN} = V_{IN1}, V_{IN2}, \ldots\ldots, V_{INn}$. Hence, the input voltage can be expressed as follows:

$$V_{IN} = \frac{V_{IH} - V_{IL}}{t_r} t_1\ ,\quad \frac{V_{IH} - V_{IL}}{t_r} t_2\ ,\ \ldots\ldots\ ,\ \frac{V_{IH} - V_{IL}}{t_r} t_n \tag{4. 19}$$

Now consider $t_1 \leq t \leq t_2$, the initial condition of the output voltage will be $V_O = V_{OH}$ ($V_1$) at $t = t_1$. Since the output voltage ($V_2$) at $t = t_2$ is unknown, $i_{DSC}(t_2)$ cannot be defined from the load-line characteristics. However, with a small increase of the input voltage within a short time period, we can assume that the decrease of the output voltage is also small. From this assumption, we can guess the output voltage ($V_{2(1)}$) at $V_{IN} = V_{IN2}$ (where subscript $_{(1)}$ represents a first guess value), and the corresponding discharging current ($I_{DSC}$) is obtained from the measured load-line characteristics at $V_{IN} = V_{IN2}$ in accordance with $V_O = V_{2(1)}$ and assigned as $i_{DSC}(t_2)$. Now from the data extracted from the measurement, $i_{DSC}(t)$ can be obtained by solving Equation 4. 10. The solution of Equation 6 can be found as follows:

$$-\int_{t1}^{t2} i_{DSC}(t)dt = C_{\text{int}} \int_{V_1}^{V_2} dV_O \tag{4. 20}$$

where $V_1$ and $V_2$ is the output voltage at $t_1$ and $t_2$, respectively. $V_1$, $t_1$, and $t_2$ are known and $V_2$ is unknown.

$$-\left(\frac{at^2}{2} + bt\right)\Bigg|_{t1}^{t2} = C_{\text{int}}(V_2 - V_1) \tag{4. 21}$$

$$V_{2(2)} = V_1 - \frac{1}{C_{\text{int}}}\left(\frac{at_2{}^2}{2} + bt_2 - \frac{at_1{}^2}{2} - bt_1\right) \tag{4. 22}$$

In order to evaluate the solution ($V_2$) in Equation 4. 22 and distinguish it from the initial guess value $V_{2(1)}$, we label the solution as $V_{2(2)}$. If the two values are different, then we consider $V_{2(2)}$ as the second guess value, and obtain a new discharging current using $I_{DSC}$ (=$i_{DSC}(t_2)$) extracted from the load-line characteristics ($V_{IN}$ = $V_{IN2}$ and $V_O$=$V_{2(2)}$). Based on this current, $V_{2(3)}$ is obtained and compared to $V_{2(2)}$ for convergence. The iteration is performed until the solution converges to the previous guessed value ($V_{2(n)}$= $V_{2(n-1)}$). Once a converged value of $V_2$ is obtained, $V_3$ for the next time interval ($t_2 \le t \le t_3$) can be found by the same iterative procedure. With this method the entire transition profile of the dynamic operation of the device can be obtained and the converged solution for the final condition ($V_{IN}$=$V_{INn}$) will be $V_O$=$V_n$. As the ramp reaches the final condition ($V_{INn}$= $V_{IH}$), the ramp signal starts to provide steady state voltage ($V_{IH}$). For the analysis of the operation in this steady state, we need first to define the initial condition of this steady state. Since the final condition ($t$ = $t_n$) of the transient period is the initial condition of the steady state, the corresponding converged solution ($V_O$ = $V_n$) and currents ($i_{DSC}(t_n)$) of the final

condition can be adopted as the initial conditions for the steady state. Thus, for the steady state $V_{OH(steady)} = V_n$. The analysis of the dynamic operation of the inverter for the steady state period can be done exactly in the same fashion as that of the ideal step input, with the only difference being the initial condition. Likewise, the analysis for the transition of the ramp signal from high to low ($V_{IH}$ to $V_{IL}$) can be performed in the same way as that of the transition from low to high described earlier, using as initial condition the final condition obtained from the steady-state. In the same fashion, we can extract the data ($V_O{}^{MW}$, $i_{DSC}{}^{MW}$, and $i_{CHG}{}^{MW}$) from the measured static characteristics under microwave interference, and the method can be successfully applied to describe the dynamic operation of the inverter with microwave interference.

The propagation delay with a ramp input is given in Equations 4. 23 and 4. 24 below:

$$t_{PHL(ramp)} = t_r + t_{PHL(steady)} \tag{4. 23}$$

where $t_{PHL(ramp)}$ is the total propagation delay as the ramp signal transits from $V_{OH}$ to $V_{OL}$. $t_r$ is the rise transient time of the ramp signal, and $t_{PHL(steady)}$ is the propagation delay during $V_O$ transitioning from $V_{OH(steady)}$ to $V_{OL}$.

$$t_{PLH}{}^{MW}{}_{(ramp)} = t_f + t_{PLH}{}^{MW}{}_{(steady)} \tag{4. 24}$$

where $t_{PLH(ramp)}{}^{MW}$ is the total propagation delay as the ramp signal transits from $V_{OL}{}^{MW}$ to $V_{OH}{}^{MW}$. $t_f$ is the fall transient time of the ramp signal, and $t_{PLH(steady)}$ is the propagation delay during $V_O{}^{MW}$ transitioning from $V_{OL(steady)}{}^{MW}$ to $V_{OH}{}^{MW}$.

## *4. 3 Dynamic Power Dissipation of CMOS Inverter with a Ramp Input*

The dynamic power dissipation of the CMOS inverter with a ramp input signal depends on currents and voltages at the output and the average clock frequency of the inverter $f_{avg}$, and consists of three parts: (1) the charging and discharging output currents on the intrinsic output capacitance during the switching. In addition to these currents we have (2) the output short-circuit currents during the rise and fall times of the ramp input when one device is in the triode region and the other in saturation, and (3) the output short-circuit currents during steady state. A ramp input is composed of three periods, the rise and fall times and the steady-state period. The dynamic power dissipation during the rise ($t_r$) and fall ($t_f$) times can be obtained by:

$$P_{SC}{}^{MW}{}_{(Rise/Fall)} = \left(t_r I_{PSC}{}^{MW}{}_{(Rise)} + t_f I_{NSC}{}^{MW}{}_{(Fall)}\right) V_{DD} f_{avg} \qquad (4.\ 25)$$

where $t_r$ is the rise time of the ramp input, $t_f$ is the fall time, $I_{PSC}{}^{MW}{}_{(Rise)}$ is the average short-circuit current of the p-MOS during the $t_r$ period, and $I_{NSC}{}^{MW}{}_{(Fall)}$ is the average short-circuit current of the n-MOS during the $t_f$ period, and $f_{avg}$ is the average clock frequency of the inverter in the dynamic logic gate. The dynamic power dissipation due to the short-circuit current during steady state will be:

$$P_{SC}{}^{MW}{}_{(steady)}$$

$$= \left(t_{PHL}{}^{MW}{}_{(steady)} I_{PSC}{}^{MW}{}_{(steady)} + t_{PLH}{}^{MW}{}_{(steady)} I_{NSC}{}^{MW}{}_{(steady)}\right) V_{DD} f_{avg} \qquad (4.\ 26)$$

where $t_{PHL}{}^{MW}{}_{(steady)}$ is the time the $V_O$ transits from $V_{OH}{}^{MW}{}_{(steady)}$ to $V_{OL}{}^{MW}$, $t_{PLH}{}^{MW}{}_{(steady)}$ is the time that the $V_O$ transits from $V_{OL}{}^{MW}{}_{(steady)}$ to $V_{OH}{}^{MW}$, $I_{PSC}{}^{MW}{}_{(steady)}$ is the average

short-circuit current of the p-MOS during the $t_{PHL}^{MW}{}_{(steady)}$ period, and $I_{NSC}^{MW}{}_{(steady)}$ is the average short-circuit current of the n-MOS during the $t_{PLH}^{MW}{}_{(steady)}$ period. The power dissipation due to the charging and discharging (switching) of the intrinsic output capacitance ($C_{int}$) will remain unchanged and it is given again as:

$$P_{SW}^{MW}{}_{(ramp)} = C_{\text{int}}\left(V_{OH}^{MW} - V_{OL}^{MW}\right)V_{DD} f_{avg} \qquad (4.\ 27)$$

Therefore, the total dynamic power dissipation ($P_{Dyn}^{MW}{}_{(ramp)}$) with a ramp input, is given by:

$$P_{Dyn}^{MW}{}_{(ramp)} = P_{SW}^{MW}{}_{(ramp)} + P_{SC}^{MW}{}_{(Rise/Fall)} + P_{SC}^{MW}{}_{(steady)} \qquad (4.\ 28)$$

## *4. 4 Validation of Anaytical Parameter Extreaction Method*

Due to the absence of models predicting dynamic operation of CMOS inverters under large signal high power microwave interference, it is not possible to compare our analytical parameter extraction method with such models. However, there are models that predict dynamic operation of inverters under normal operating conditions without the interference, such as the α-power law [47], and SPICE models. Therefore, it is worth comparing our analytical parameter extraction method with these models when interference is not present, to allow us to evaluate the effectiveness of the method. The output voltages of 1.6μm inverters were obtained using those two models and the parameter extraction method, and then compared each other for the evaluation. The SPICE model used for the simulation was extracted from the layout of the actual inverter circuit. An ideal ramp signal having 100ps transient period was considered as the input. As shown in Figure 4. 3, the output

voltage obtained from the SPICE simulation showed good agreement with that from the parameter extraction method. With the α value of 1.31, the output voltage of the α-power law model also showed a good match with that of the method up to 176ps as shown in Figure 4. 3. However, for t ≥ 176ps the output voltage from the α-power law model showed much slower decrease with respect to time than that from the extraction method, resulting in a longer propagation delay of 392ps. This is believed to be due to the inaccuracy of the α-power law model at the region near and below the threshold voltage. From these results, it can be concluded that the parameter extraction method is as accurate as the SPICE model, providing a better prediction than the α-power law model, under normal operating conditions without interference.

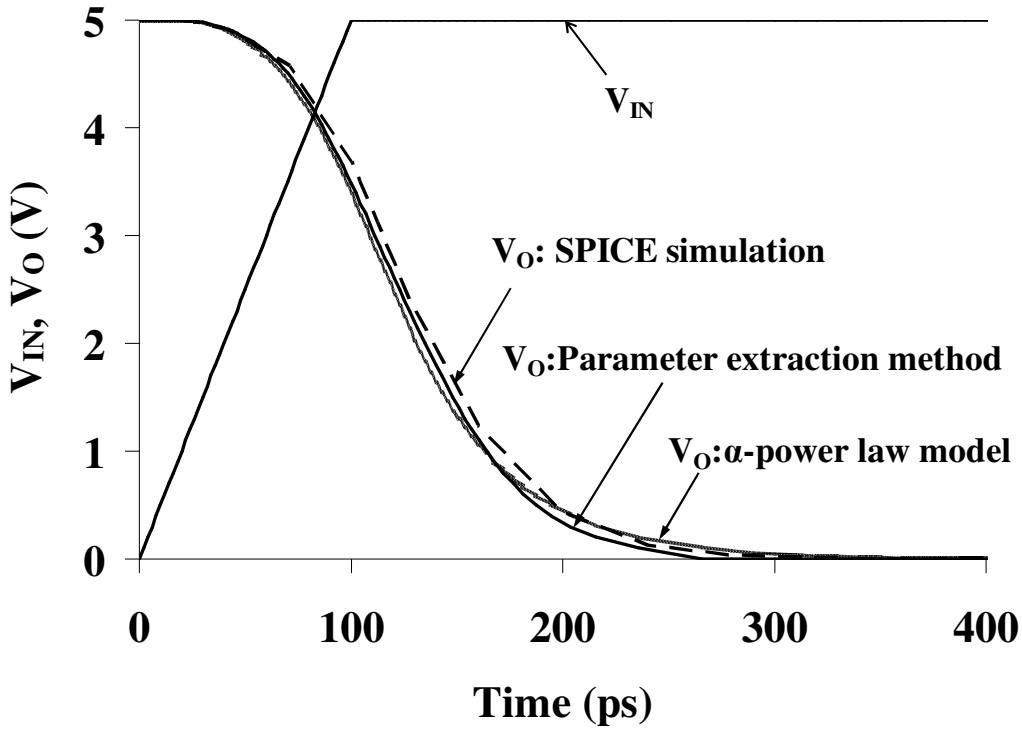



Figure 4. 3 Comparison between α-power law model, SPICE model, and the parameter extraction method under normal operating conditions without interference

for a 1.6μm inverter. The comparison shows that the parameter extraction method is as accurate as SPICE model.

The method allows us to predict the impact of high power microwave interference on the dynamic operation of the inverters without developing nonlinear models. Analysis based on this method can reveal upset mechanisms by identifying the most critical operational parameters. Furthermore, the dynamic operation of digital circuits depends on charge transport at each node with respect to input signals and bias conditions and this charge transport follows Kirchhoff's current and voltage laws. Therefore, this method can be generalized and applied to obtain the dynamic operational parameters of any digital circuit, once the load-line characteristics at each node are measured, and the corresponding equivalent capacitances are obtained.

## *4. 5 Results and Discussion: 0.6μm Devices*

In this section, the effects of microwave interference on the dynamic operation of the inverters are investigated by examining the output voltages, propagation delays, output currents, and dynamic power dissipation with and without the interference using the parameter extraction method. Both 1.6 and 0.6μm devices gave similar effects under interference, although the effects were more pronounced in the 0.6μm devices. Thus, the results from the 0.6μm devices are presented and discussed here to avoid repetitiveness. The input considered in this section is an ideal ramp signal that has a 100ps transient period.

### 4. 5. 1 The Effects of Microwave Interference on Dynamic Operation with a Ramp Input

The ramp signal used in this section has transient periods at $0 \leq t \leq 100$ps and $2\text{ns} \leq t \leq 2.1\text{ns}$, and gradients of ±0.05V/ps as shown in Figure 4. 4. During the transient period, the input voltage ($V_{IN}$) increases or decreases linearly from $V_{IL}$ (0V) to $V_{IH}$ (5V) or $V_{IH}$ to $V_{IL}$, respectively. In this specific case, the $t_a$ satisfying the linearity condition of Equation 10 was set at 2ps. Therefore, for $0 \leq t \leq 100$ps, time ($t$) is given as follows:

$$t = 0, 2\text{ps}, 4\text{ps}, \ldots\ldots, 100\text{ps} \tag{4. 29}$$

and it is labeled as $t_1, t_2, \ldots\ldots, t_{51}$. The corresponding input voltage ($V_{IN}$) at each time ($t$) is designated as $V_{IN}$ = 0V, 0.1V, 0.2V, ……, 5V. Hence, the input voltage is expressed as follows:

$$V_{IN} = 0V\ (t = t_1),\quad 0.1V\ (t = t_2),\quad 0.2V\ (t = t_3),\quad \ldots\ldots,\quad 5V\ (t = t_{51}) \tag{4. 30}$$

The measured load-line characteristics of the inverter showed that the initial output voltage ($V_O$=$V_1$) at $t$=$t_1$ is 5V without interference, and 4.7V with a 1GHz, 24dBm interference. The $t_a^{MW}$ was also set at 2ps. Based on these conditions, the output voltages at each time ($t$) were obtained by applying the analytical parameter extraction method described in section 4. 2. 3 for a ramp input. The results showed that the final value of the output voltage at $t$=$t_{51}$ (100ps) is 2.9V without microwave interference, and 3.3V with the 1GHz, 24dBm interference. Note that these final output voltages are equivalent to the initial output voltages for the steady state

analysis. Thus, the initial output voltage at 100ps is given as 2.9V without interference, and 3.3V with the 1GHz, 24dBm interference, for the steady state region, where the input voltage remains at 5V for 100ps ≤ t ≤ 2ns. $V_a$ and $V_a^{MW}$ for this region, is taken to be 0.1V. Therefore, the output voltages $V_1$, $V_2$, $V_3$, ……, $V_n$ can be assigned as 2.9V, 2.8V, 2.7V,……. , 0V and $V_1^{MW}$, $V_2^{MW}$, ……, $V_n^{MW}$ as 3.3V, 3.2V, ……. , 1.7V, respectively. With these conditions, the output voltage for this region is obtained by the analytical parameter extraction method in the section 4. 2. 2 for a step input. For t ≥ 2ns, the output voltages and currents were obtained in the same fashion, the only difference being in the initial conditions.

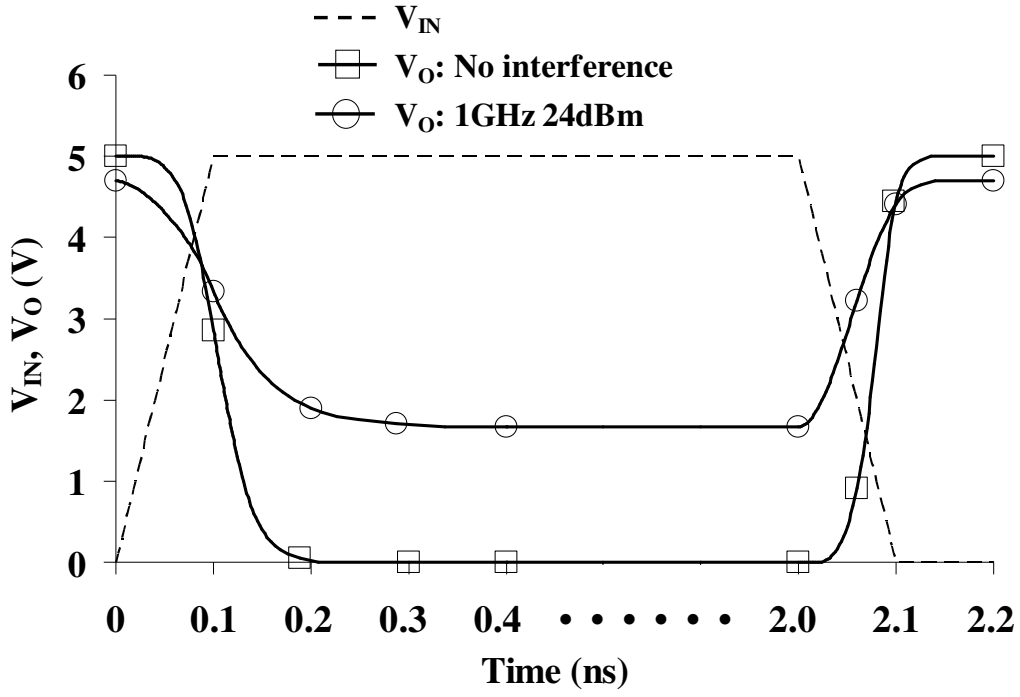



Figure 4. 4 Input and output voltages of a 0.6μm inverter at $V_{DD}$=5V, obtained by the parameter extraction method, with and without 1GHz, 24dBm interference. Reduced dynamic range swing in the output voltage and increased propagation delays are shown, resulting in the loss of digital inverter characteristics.

The input and output voltages with and without interference obtained based on this analysis are given in Figure 4. 4. Under a 1GHz, 24dBm microwave interference, the output voltage showed a reduced dynamic range swing from $V_{OH}^{MW}$(4.7V) to $V_{OL}^{MW}$(1.7V), instead of $V_{OH}$ (5V) and $V_{OL}$ (0V). This means that the device cannot switch ON or OFF completely at the output. Especially, $V_{OL}^{MW}$ resides in the region where a bit cannot be defined (undetermined bit region), and thus, bit errors are obtained. This effect can be attributed to the severe change of the quiescent operating point in the load-line characteristics of the inverter due to the interference as shown in Figure 4. 2. The intrinsic propagation delays, defined as the time for the output ($V_O$) to switch from $V_{OH}$ to $V_{OL}$ ($t_{PHL}$, discharging) or $V_{OL}$ to $V_{OH}$ ($t_{PLH}$, charging), showed an increase of 3.6 to 120% under the 1GHz, 24dBm microwave interference as shown in Table 4. 2. The most prominent increases were observed when the input voltage changes from $V_{IL}$ to $V_{IH}$. In this region, $t_{PHL}^{MW}{}_{(steady)}$ and $t_{PHL}^{MW}{}_{(ramp)}$ showed 120% and 65% increase, respectively. These propagation delays depend on (1) the output voltage difference of $V_{OH}$ and $V_{OL}$, and (2) the charging and discharging currents [34]. Therefore, the substantial increase in the delay time ($t_{PHL}^{MW}$) is believed to be due to the significantly reduced discharging current (–59.5%, Table 4. 3), resulting from the reduced voltage swing at the output.

A high frequency SPICE (HSPICE) was also proposed as a technique to simulate the high power EMI effects [42]. However, it was shown in the report [42] that the technique severely underestimated the effects, while our parameter extraction technique (PEM) provides an accurate representation of the effects observed in the

experiment. Furthermore, if PSPICE is employed to simulate the effects of high power EMI the results do not match the experimental results at all.

| | | | | |
|---|---|---|---|---|
| No interference | $t_{PHL(steady)}$ | $t_{PHL(ramp)}$ | $t_{PLH(steady)}$ | $t_{PLH(ramp)}$ |
| | 107.9ps | 207.9ps | 35.4ps | 135.4ps |
| 1GHz 24dBm (% change) | $t_{PHL}^{MW}{}_{(steady)}$ | $t_{PHL}^{MW}{}_{(ramp)}$ | $t_{PLH}^{MW}{}_{(steady)}$ | $t_{PLH}^{MW}{}_{(ramp)}$ |
| | 236.9ps (120%) | 336.9ps (62%) | 40.3ps (14%) | 140.3ps (3.6%) |

Table 4. 2 Intrinsic propagation delays of a 0.6μm inverter at $V_{DD}$=5V with and without 1GHz, 24dBm interference. Ramp input signal has 100ps of rise and fall transient period. A large increase in the propagation delays are observed under the interference.

This is shown in Figure 4. 5. (a) and (b) where the output currents with and without the microwave interference are plotted with the input voltage. As seen in Figure 4. 5. (b), the discharge current is significantly smaller with interference as compared with that in Figure 4. 5. (a) without interference. In contrast, the average short-circuit currents ($I_{PSC(Rise)}$, $I_{PSC(steady)}$, $I_{NSC(Fall)}$, and $I_{NSC(steady)}$) showed one to four orders of magnitude increase under interference, as shown in Table 4. 3. Among those currents, $I_{PSC(steady)}$ showed the highest increase. This increase of the short-circuit currents makes the device draw excess current continuously, resulting in significant increase in power dissipation at the metal contacts and the interconnects from the power rails, not designed to deliver that amount of current continuously. This results in operation at elevated current densities and temperatures, resulting in high stress at

interconnects and contacts, and eventually leading to catastrophic failure by interconnect peel-off, and contact degradation.

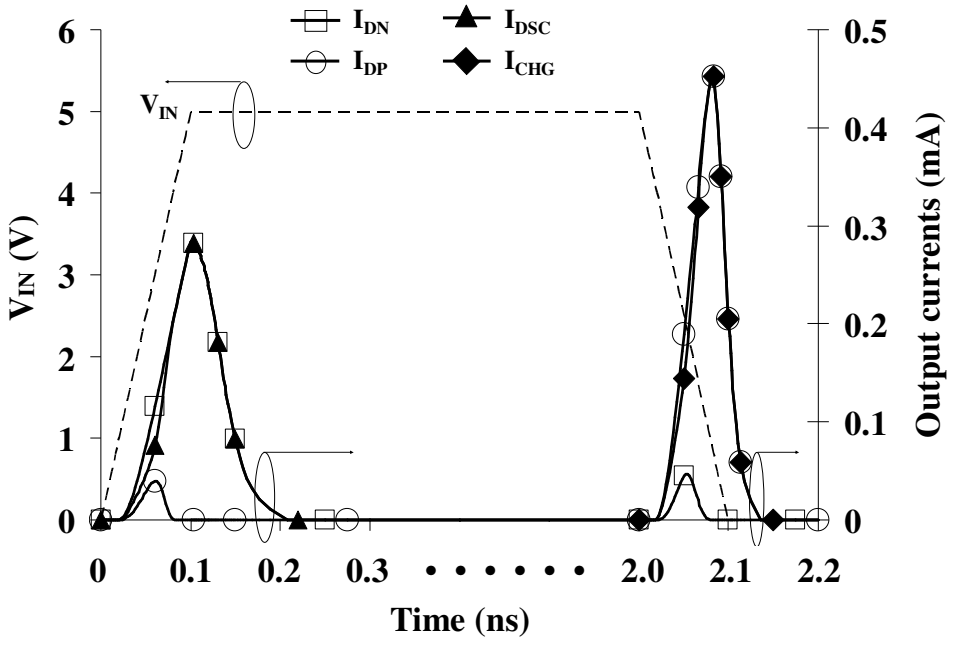



Figure 4. 5 (a)

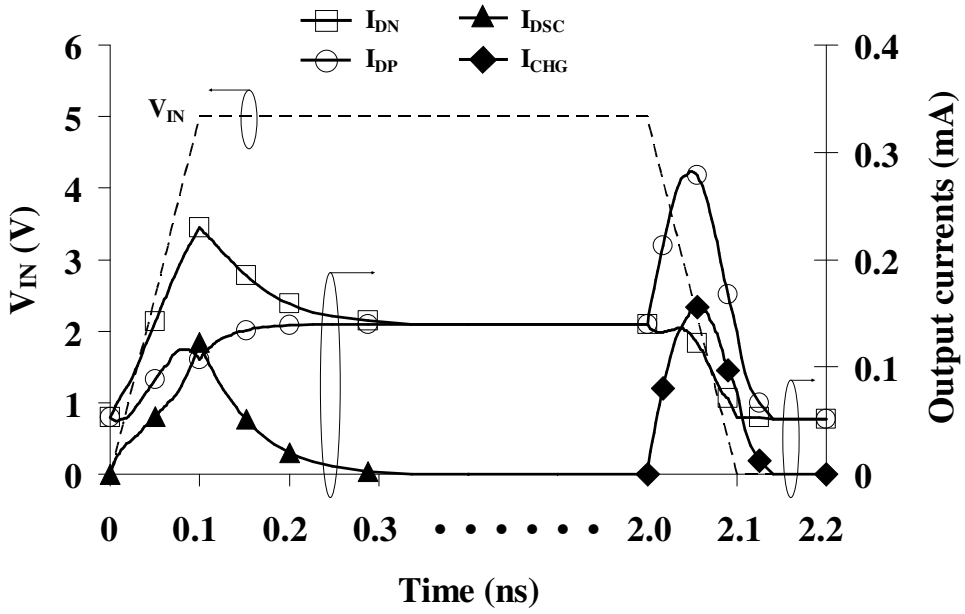



Figure 4. 5 (b)

Figure 4. 5 Input voltage and output currents of a 0.6μm inverter at $V_{DD}$=5V. (a) Output currents without microwave interference. (b) Output currents with 1GHz, 24dBm microwave interference. Note that $I_{DSC}^{MW} = I_{DN}^{MW} - I_{DP}^{MW}$ and $I_{CHG}^{MW} = I_{DP}^{MW} - I_{DN}^{MW}$. The figures show a substantial increase in the average short-circuit currents leading to significant increase in power dissipation.

| No interference | $I_{PSC(Rise)}$ | $I_{PSC(steady)}$ | $I_{NSC(Fall)}$ | $I_{NSC(steady)}$ | $I_{DSC}$ | $I_{CHG}$ |
|---|---|---|---|---|---|---|
| | 10.8μA | 3.65nA | 12μA | 0.12μA | 145μA | 165μA |
| 1GHz 24dBm (% change) | $I_{PSC}^{MW}{}_{(Rise)}$ | $I_{PSC}^{MW}{}_{(steady)}$ | $I_{NSC}^{MW}{}_{(Fall)}$ | $I_{NSC}^{MW}{}_{(steady)}$ | $I_{DSC}^{MW}$ | $I_{CHG}^{MW}$ |
| | 85.4μA (691%) | 128μA (3506700%) | 113μA (842%) | 53μA (44067%) | 58.7μA (–59.5%) | 102μA (–38.2%) |

Table 4. 3 Calculated short-circuit, discharging, and charging currents of a 0.6μm inverter at $V_{DD}$=5V with and without 1GHz, 24dBm interference. 1 to 4 orders of magnitude increase in the short-circuit currents is observed, leading to substantial increase in power dissipation and stress on the device contacts and interconnects.

## 4. 5. 2 The Effects of Microwave Interference on Dynamic Power Dissipation with a Ramp Input

The effects on dynamic power dissipation are investigated using the propagation delays, currents, and output voltages obtained from the previous section. The transient periods of the input ramp signal are chosen to be 100ps. Thus, $t_f$ and $t_r$ are both 100ps. Using Table 4. 2 and 4. 3, and assuming the average clock frequency $f_{avg}$ =250MHz, the dynamic power dissipation with ramp input is calculated by Equation 25–28 and given in Table 4. 4. The intrinsic propagation delays from high-to-low ($t_{PHL}^{MW}{}_{(ramp)}$) are observed to have 62% increase with a 1GHz, 24dBm

interference, while low-to-high ($t_{PLH}{}^{MW}{}_{(ramp)}$) show a moderate 3.6% increase (Table 2). This asymmetric increase in the delays is partly due to the difference in the decrease of the average discharging ($I_{DSC}{}^{MW}$: 59.5%) and charging ($I_{CHG}{}^{MW}$: 38.2%) currents, as we observe in Table 4. 3, and partly to the asymmetry of the n and p MOS devices. $P_{SW}{}^{MW}{}_{(ramp)}$ showed a decrease of 39% mainly due to the reduced dynamic range of the output voltage swing, while $P_{SC}{}^{MW}{}_{(Rise/Fall)}$ at rise and fall, and $P_{SC}{}^{MW}{}_{(steady)}$ at steady-state increased substantially, resulting in an overall increase of 184% in the dynamic power dissipation under the 1GHz, 24dBm interference. This increase in the dynamic power dissipation is predominantly due to the dissipation from the short circuit current from $V_{DD}$ to ground during the transient period (24.8μW, one order of magnitude increase) and steady state (40.6μW, four orders of magnitude increase).

| | | | | |
|---|---|---|---|---|
| No interference | $P_{SW(ramp)}$ | $P_{SC(Rise/Fall)}$ | $P_{SC(steady)}$ | $P_{Dyn(ramp)}$ |
| | 25.6μW | 2.85μW | 5.8nW | 28.5μW |
| 1GHz 24dBm (% change) | $P_{SW}{}^{MW}{}_{(ramp)}$ | $P_{SC}{}^{MW}{}_{(Rise/Fall)}$ | $P_{SC}{}^{MW}{}_{(steady)}$ | $P_{Dyn}{}^{MW}{}_{(ramp)}$ |
| | 15.5μW (–39%) | 24.8μW (770%) | 40.6μW (699900%) | 80.9μW (184%) |

Table 4. 4 Calculated dynamic power dissipation of a 0.6μm inverter with and without 1GHz, 24dBm interference. $f_{avg}$ is set at 250MHz. 2.84 times increase in the dynamic power dissipation is observed under the interference.

As discussed in section 4. 5. 1, the increase in power consumption at the inverter unit would not only introduce serious stress at the device and circuit level by substantially

increasing current density through device contacts and interconnects rated by design to handle much lower current densities, but it would also disrupt the overall operational power requirements which are strictly regulated by the power supply, thus shutting down other units in the system by depriving them from power.

## *4. 6 Results and Discussion: Device Bias and Size Scaling Effects*

In this section, the vulnerability of CMOS inverters to microwave interference with respect to bias voltages and device size is discussed. First, the relation between the interference and bias voltage is investigated by comparing the dynamic operation of the 0.6μm inverters operating at $V_{DD}$=3.3V, with the dynamic operation at $V_{DD}$=5V. The ramp signal applied to the input port changed from 0V to 3.3V at $0 \leq t \leq 100$ps with a slope of 0.033V/ps and from 3.3V to 0V at $2\text{ns} \leq t \leq 2.1\text{ns}$ with –0.033V/ps. The device size and its relation to the interference are also studied by examining the dynamic operation of the 1.6μm inverters. The inverter is biased with 5V and the condition of the ramp signal remains the same as that adopted in section 4. 5. 1. Based on these conditions and the measured load-line characteristics, the output voltages and currents, propagation delays, and dynamic power dissipation of the 0.6μm and 1.6μm inverters, are obtained by exactly the same analytical parameter extraction method as before. These results are then compared with those obtained from section 4. 5.

### 4. 6. 1 Device Bias Scaling

The output voltage of 0.6μm inverters biased at 3.3V, showed a severely compressed voltage swing from 2.92V to 1.42V under a 1GHz, 24dBm microwave interference as shown in Figure 4. 6. This degradation in the output voltage drives $V_{OL}^{MW}$ nearly into the inflection voltage point (1.87V) where the actual switching of the inverter output occurs, revealing that the device will suffer a critical bit error at the output. Furthermore, the propagation delays showed a 7.8 to 22% decrease as shown in Table 4. 5. We learned that propagation delays proportional to output voltage swing and inversely proportional to charging and discharging currents [34]. Therefore, the decrease in the delays (Table 4. 5) is attributed to the fact that the severely compressed voltage swing (Figure 4. 6) overshadows the decrease in the charging (–58.8%) and discharging (–46.6%) currents (Table 4. 6). This degradation in the output voltage and propagation delays (increase or decrease) would result in critical bit errors in digital circuits by invalidating the edge triggers in clock signals as we reported in [52].

The short-circuit currents showed two to four orders of increase (Table 4. 6) under the 1GHz, 24dBm interference, which is comparable to the increase of the short-circuit currents at $V_{DD}$=5V. Again, most prominent increase was observed in $I_{PSC}^{MW}{}_{(steady)}$ (98.3μA, four orders of magnitude increase). Table 4. 7 shows a substantial reduction in $P_{SW}^{MW}{}_{(ramp)}$ by 54% under interference, which results from the severely reduced dynamic range swing of the output voltage. On the other hand, the power dissipation during the transient ($P_{SC(Rise/Fall)}$), and steady state ($P_{SC(steady)}$) periods, showed two to three orders of increase, thus, resulting in a 175% increase in

the over all power dissipation ($P_{Dyn}{}^{MW}{}_{(ramp)}$). This is a substantial increase in short-circuit current, and hence, power. It introduces increased vulnerability and serious reliability issues in the units, such as reduced device lifetime due to increased current densities, interconnect failure due to current densities substantially exceeding design ratings, and power supply rail regulation degradation in the integrated circuit. From Table 4. 4 and 4. 7 it is evident that the increase in the power dissipation with a $V_{DD}$=3.3V follows a similar trend with that of $V_{DD}$=5V. Therefore, those results demonstrate that as the bias voltage is scaled down from 5V to 3.3V, the CMOS inverter suffers more from severely compressed output voltage and hence, larger changes in propagation delays under interference, while the substantial increase in the dynamic power dissipation still remains at a critical level causing soft and hard errors in the device.

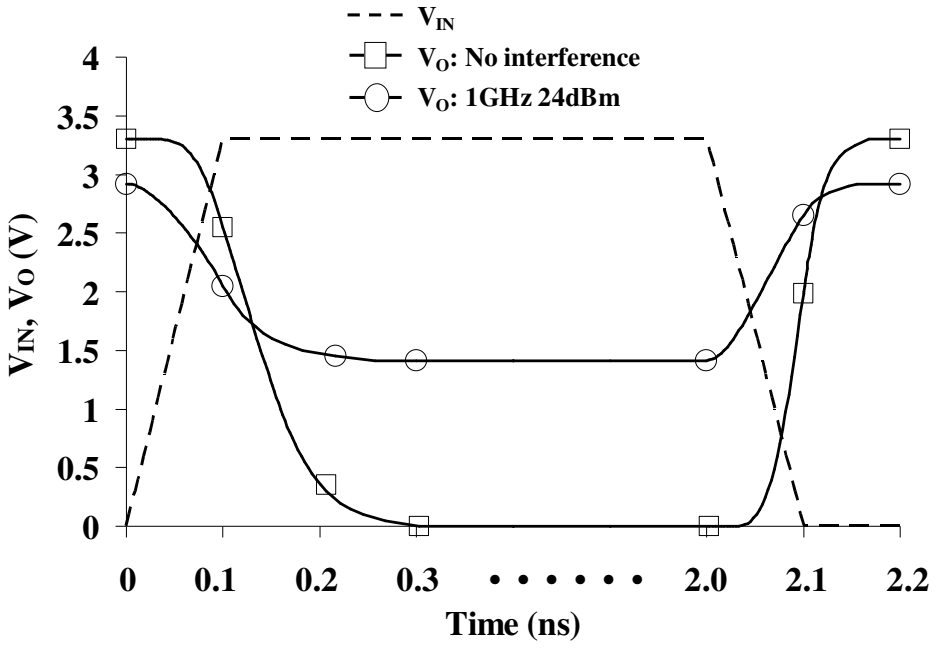



Figure 4. 6 Input and output voltages with and without 1GHz, 24dBm interference. Output voltages of a 0.6μm inverter at $V_{DD}$=3.3V, showing the device bias scaling

effects. The smaller devices (0.6μm) shows more compressed output voltage swing than the larger devices (1.6μm), indicating that the smaller devices are more susceptible to the interference.

| | | $t_{PHL(steady)}$ | $t_{PHL(ramp)}$ | $t_{PLH(steady)}$ | $t_{PLH(ramp)}$ |
|---|---|---|---|---|---|
| No interference | 0.6μm inverter $V_{DD}$=3.3V | 202.5ps | 302.5ps | 68.2ps | 168.2ps |
| | 1.6μm Inverter $V_{DD}$=5V | 165.9ps | 265.9ps | 134.8ps | 234.8ps |
| | | $t_{PHL}^{MW}{}_{(steady)}$ | $t_{PHL}^{MW}{}_{(ramp)}$ | $t_{PLH}^{MW}{}_{(steady)}$ | $t_{PLH}^{MW}{}_{(ramp)}$ |
| 1GHz 24dBm (% change) | 0.6μm inverter $V_{DD}$=3.3V | 157.4ps (–22 %) | 257.4ps (–15%) | 55ps (–19%) | 155ps (–7.8%) |
| | 1.6μm inverter $V_{DD}$=5V | 187.7ps (13.1%) | 287.7ps (8.2%) | 157.4ps (16.8%) | 257.4ps (9.6%) |

Table 4. 5 *Intrinsic propagation delays* of 0.6μm and 1.6μm inverters with and without 1GHz, 24dBm interference. Bias voltage is 3.3V or 5V. The comparison shows that the smaller devices suffer more from the larger changes in the propagation delays than the larger devices do.

| | | $I_{PSC(Rise)}$ | $I_{PSC(steady)}$ | $I_{NSC(Fall)}$ | $I_{NSC(steady)}$ | $I_{DSC}$ | $I_{CHG}$ |
|---|---|---|---|---|---|---|---|
| No interference | 0.6μm inverter $V_{DD}$=3.3V | 0.82μA | 3.94nA | 0.97μA | 100nA | 67μA | 116μA |
| | 1.6μm inverter $V_{DD}$=5V | 8.17μA | 2.65nA | 10.43μA | 77.3nA | 189μA | 229μA |
| | | $I_{PSC}^{MW}{}_{(Rise)}$ | $I_{PSC}^{MW}{}_{(steady)}$ | $I_{NSC}^{MW}{}_{(Fall)}$ | $I_{NSC}^{MW}{}_{(steady)}$ | $I_{DSC}^{MW}$ | $I_{CHG}^{MW}$ |
| 1GHz 24dBm (% change) | 0.6μm inverter $V_{DD}$=3.3V | 67.7μA (8156%) | 98.3μA (2494800%) | 88.2μA (8993%) | 47μA (46900%) | 35.8μA (–46.6%) | 47.8μA (–58.8) |
| | 1.6μm inverter $V_{DD}$=5V | 88.97μA (988%) | 89.8μA (3389000%) | 108μA (935%) | 75μA (96925%) | 158μA (–16.4%) | 202μA (–11.8%) |

Table 4. 6 *Calculated short-circuit, discharging, and charging currents* of 0.6μm and 1.6μm inverters with and without 1GHz, 24dBm interference. Both of the larger and smaller devices are suffered from the significant increases of short circuit currents. This results in increased power dissipation and higher stress on the device contacts and interconnects.

| | | $P_{SW(ramp)}$ | $P_{SC(Rise/Fall)}$ | $P_{SC(steady)}$ | $P_{Dyn(ramp)}$ |
|---|---|---|---|---|---|
| No interference | 0.6μm inverter $V_{DD}$=3.3V | 11.9μW | 0.15μW | 6.3nW | 12.1μW |
| | 1.6μm inverter $V_{DD}$=5V | 53.25μW | 2.33μW | 13.58nW | 55.59μW |
| | | $P_{SW}^{MW}{}_{(ramp)}$ | $P_{SC}^{MW}{}_{(Rise/Fall)}$ | $P_{SC}^{MW}{}_{(steady)}$ | $P_{Dyn}^{MW}{}_{(ramp)}$ |
| 1GHz 24dBm (% change) | 0.6μm inverter $V_{DD}$=3.3V | 5.44μW (–54%) | 12.9μW (8500%) | 14.9μW (236410%) | 33.24μW (175%) |
| | 1.6μm inverter $V_{DD}$=5V | 47.93μW ( –10%) | 24.62μW (956%) | 35.83μW (263744%) | 108.38μW (95%) |

Table 4. 7 *Calculated dynamic power dissipation* of 0.6μm and 1.6μm inverters with and without 1GHz, 24dBm interference. $f_{avg}$ is set at 250MHz. The substantial increase in the short-circuit currents observed in Table 4. 6, results in large increase in the dynamic power dissipation.

## 4. 6. 2 Dynamic Effects and Device Size Scaling

The output voltage of the 1.6μm inverter with $V_{DD}$=5V, showed a small reduction in the voltage swing ($V_{OH}^{MW}$: 4.8V and $V_{OL}^{MW}$: 0.3V) under a 1GHz, 24dBm interference, as shown in Figure 4. 7. The propagation delays also showed a moderate increase of 8 to 16 % with interference, which is believed to be due to the mild decrease in the discharging and charging currents (–16.4% and –11.8%), as

shown in Table 6. Under interference, one to four orders of magnitude increase in the short-circuit currents was observed, and the power dissipation due to these currents are the primary elements contributing to a 95% increase in the overall dynamic power dissipation, as shown in Table 4. 7. Due to the small change in the output voltage swing, $P_{SW}^{MW}{}_{(ramp)}$ showed only a 10% decrease. When we compared those results with the results from the 0.6μm inverter, it is apparent that the 0.6μm inverter suffers more from compressed output voltage swing, significantly increased propagation delays, and substantial increases in dynamic power dissipation, than the 1.6μm inverter does. Therefore, it is concluded that the device becomes more vulnerable to the microwave interference with the scaling down of the devices.

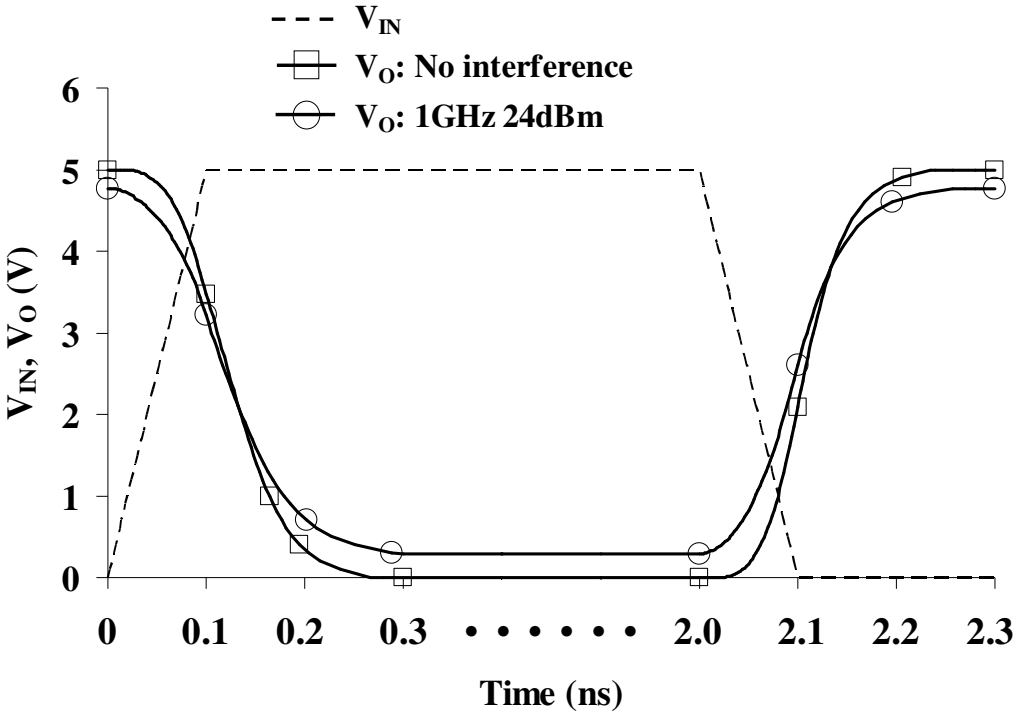



Figure 4. 7 Input and output voltages with and without 1GHz, 24dBm interference. Output voltages of a 1.6μm inverter at $V_{DD}$=5V, showing the device size scaling effects. The interference effects are less pronounced for the 1.6μm inverter, indicating that larger devices are less susceptible to the interference.

## *4. 7 Predicting Interference Upsets using The PEM on Timer IC's*

The previous section showed that microwave interference severely disrupts inverter operations and induce upsets. The primary goal of this section is to investigate how such upsets can affect the operation of integrated circuits (IC's) when the inverter subjected to microwave interference is interconnected to the IC's by identifying the most important electronic design parameters and interference characteristics related to the upsets. Furthermore, we study upset mechanisms in the IC's by comparing measured results with predicted results using the Parameter Extraction Method proposed in the previous section. For this study, we examined high power microwave interference effects on a Philips 74HC4017 Johnson decade counter (Timer) mounted on a RT/Duroid 5880 printed circuit board (PCB).

### 4. 7. 1 Experimental Details

The measurement setup is shown in Figure 4. 8. (a). In order to investigate the impact of disrupted clock port (which is a CMOS inverter) of the timer circuit, microwave interference is injected into the clock port with the clock signal using a hybrid power combiner. The timer has 11 decoded outputs ($O_0$ – $O_9$, and $\overline{O}_{5-9}$), active clock inputs ($\overline{CP}_1$, $CP_0$), and a master reset input ($MR$). It is designed to advance with positive or negative edge trigger depending on the pin connections of the clock and master reset inputs. For our experiments, MR and $CP_0$ were set to logic low and high respectively to provide negative edge clock trigger at the $\overline{CP}_1$ clock input. An HP8116A 50MHz pulse function generator was used to generate the clock pulse signal. Microwave interference signal was obtained using an HP 8753C 300kHz

- 6GHz network analyzer set. To investigate interference effects on the timer, the clock pulse and microwave signal were connected to the $\overline{CP}_1$ clock input port through the power combiner and the decoded outputs were then measured using Tektronics 450 digital oscilloscope. The oscilloscope was connected to a computer controlled by Labview program to obtain experimental data. The counter was biased with 2V or 3.3V DC and the power and frequency of the interference signal ranged from 0 to 24dBm, and 1 to 3GHz, respectively.

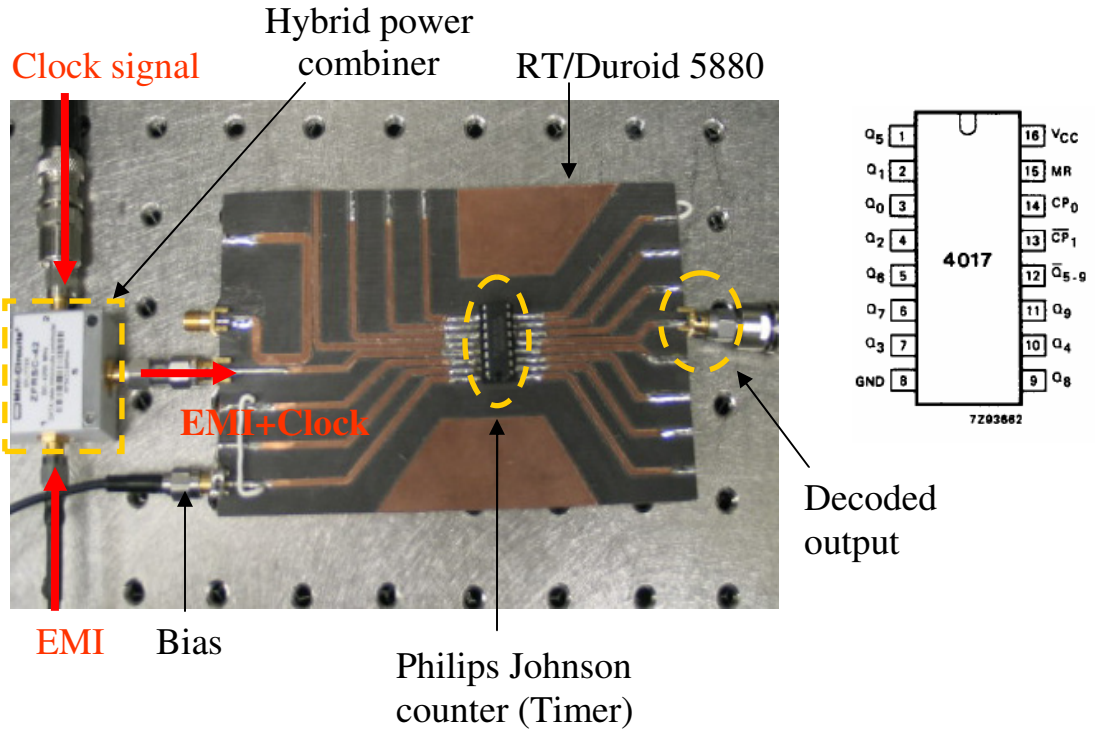



Figure 4. 8 (a)

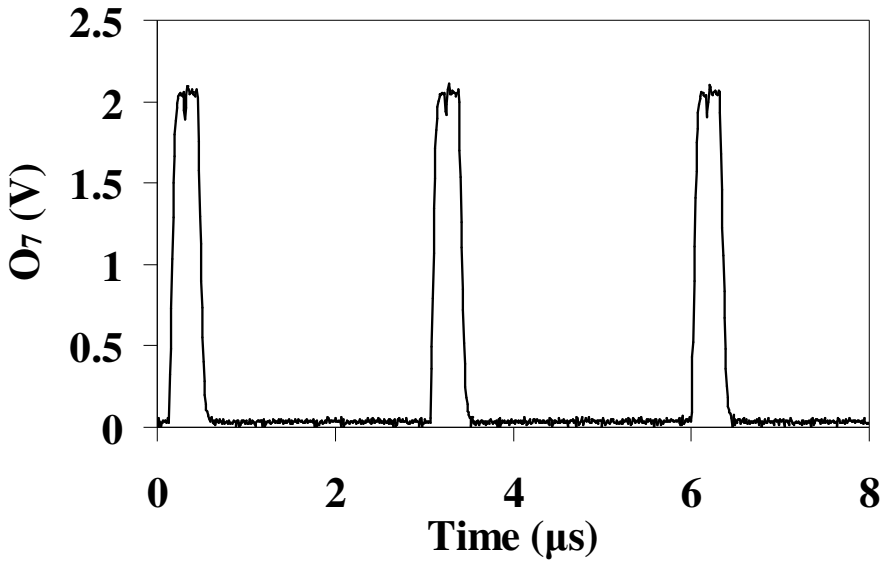



Figure 4. 8 (b)

Figure 4. 8 (a) Measurement setup for microwave interference effects on a Philips 74HC4017 Johnson Decade Counter (Timer circuit). (b) Measured output of Johnson Timer at port $O_7$ without the interference.

## 4. 7. 2 Experimental Results and Discussion

The decoded output ($O_7$) without microwave interference is shown in Figure 4. 8. (b) for 2V DC bias and 3.4MHz clock pulse having 50% duty cycle applied to the $V_{DD}$ and $\overline{CP}_1$ port respectively. As shown in the figure, the output had 320ns width and 2.936μs period indicating that the counter is at normal operation with 26ns propagation delay. The timer showed no significant changes until the power level of 23dBm. At 1GHz 23dBm, a saturation of output voltage level to $V_{DD}$ is observed as shown in Figure 4. 9. (a), indicating that the device can not turn off the output ($O_7$) (critical device error). This demonstrates that the interference power severely degrades the device performance by invalidating the negative edge trigger of the

clock signal at the port. When the interference was at 3GHz, the timer showed a gradual degradation at the output voltage as the power increased, but overall effects was less pronounced that the one under 1GHz interference. At 3GHz 22dBm, the output voltage showed a decrease to 0.85V sufficient to cause malfunction (Figure 4. 9. (b)) and a saturation to $V_{CC}$ at 24dBm (Figure 4. 9. (c)). After the interference was terminated, the device returned to normal operation implying no permanent failure. Thus, this indicates that the upsets were soft errors.

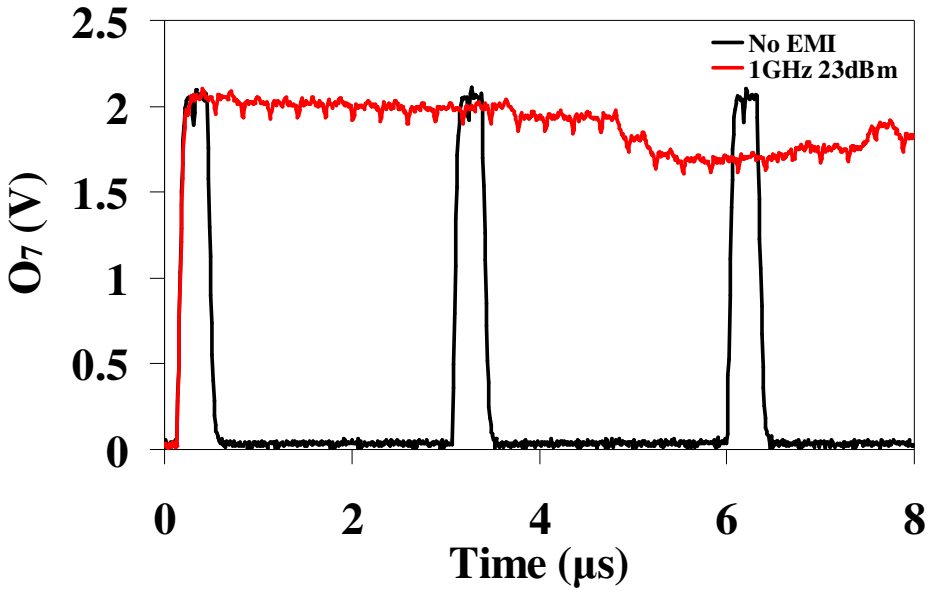



Figure 4. 9 (a)

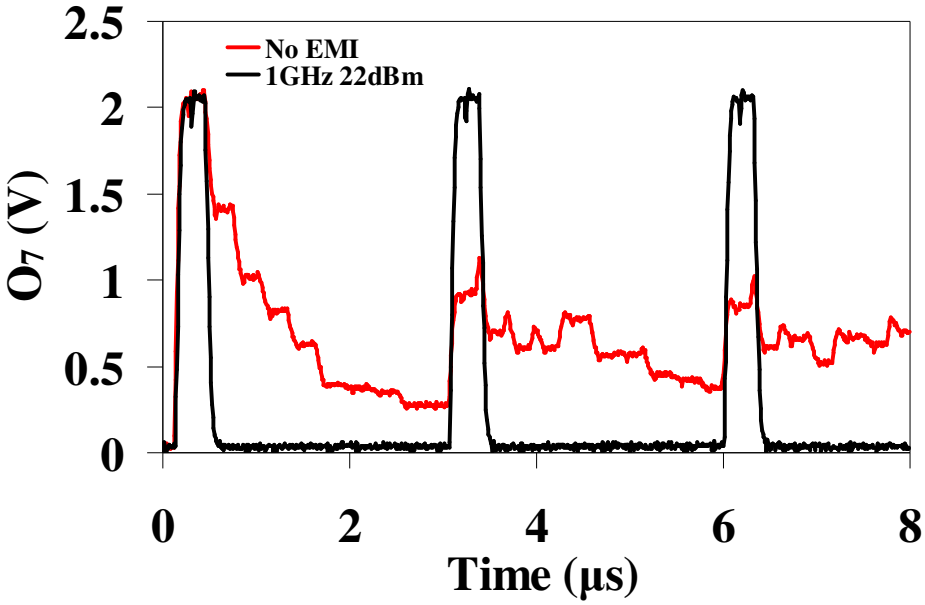



Figure 4. 9 (b)

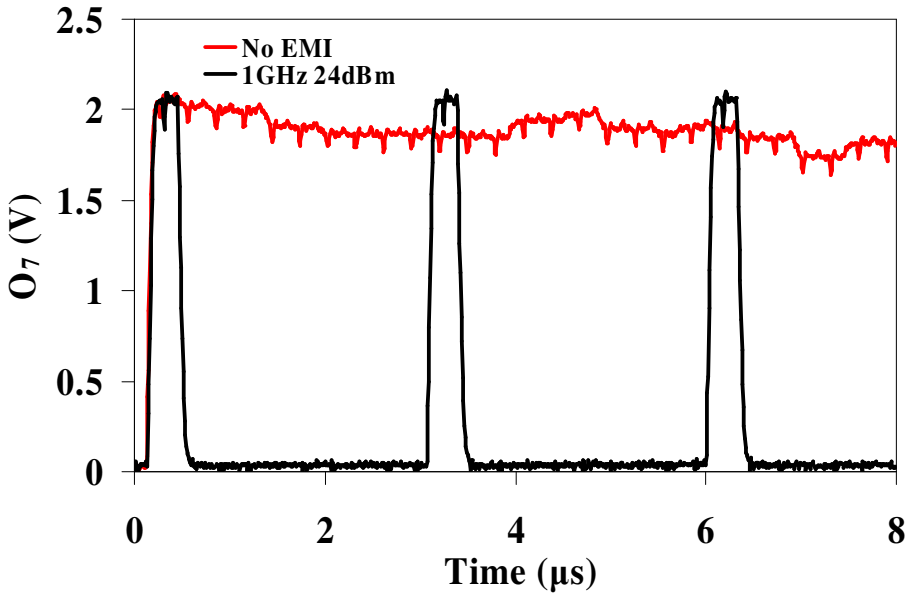



Figure 4. 9 (c)

Figure 4. 9 (a) Output of Johnson Timer at Port $O_7$ under 1GHz 23dBm interference. The output voltage shows a saturation to 2V ($V_{DD}$), indicating a logic failure. (b) Output ($O_7$) under 3GHz 22dBm interference, showing bit errors. (c) Output ($O_7$) under 3GHz 24dBm. The output also shows a saturation to 2V ($V_{DD}$).

When bias voltage ($V_{DD}$) was increased to 3.3V while other inputs remained the same as before, the output voltage showed no changes with respect to the power and frequency of interference signal. As we decreased the clock frequency from 3.4MHz to 1MHz, no significant changes were observed except for a delay of 0.032μs under 1GHz 24dBm corresponding to 2.7% of delay. Therefore, we conclude that the device becomes more susceptible to interference as the bias voltage decreases and clock frequency increases.

### 4. 7. 3 Prediction on Timer Circuit using the Parameter Extraction Method

The experimentally observed upsets on the timer circuit are predicted in this section based on SPICE simulation combined with the model derived from the parameter extraction method. This allowed us to identify upset mechanisms responsible for the failure of the timer operation due to microwave interference.

From the device data sheet, it is found that the clock port is a CMOS inverter where microwave interference was injected, as indicated with a dashed circle in the diagram of the Johnson Timer (Figure 4. 10. (a)). For simulation, we created a SPICE schematic based on 0.5μm technology as shown in Figure 4. 10. (b). The reason we chose 0.5μm technology arbitrarily is that the actual size and dimensions of the timer were not provided in the data sheet. In order to account for the effects of microwave interference on the timer input port which is a CMOS inverter, the response of the input port under microwave interference is modeled using the parameter extraction

method and the model is combined with SPICE code to simulate the operation of the timer circuits under microwave interference as shown in Figure 4. 10. (b). In this simulation, we chose $V_{DD}$ as 3.3V and the clock pulse as 3.4MHz, and the power and frequency of the interference signal were set as 24dBm and 1GHz respectively. The dimension of the inverter consisting of the clock port is the same as the one in section 4. 5.

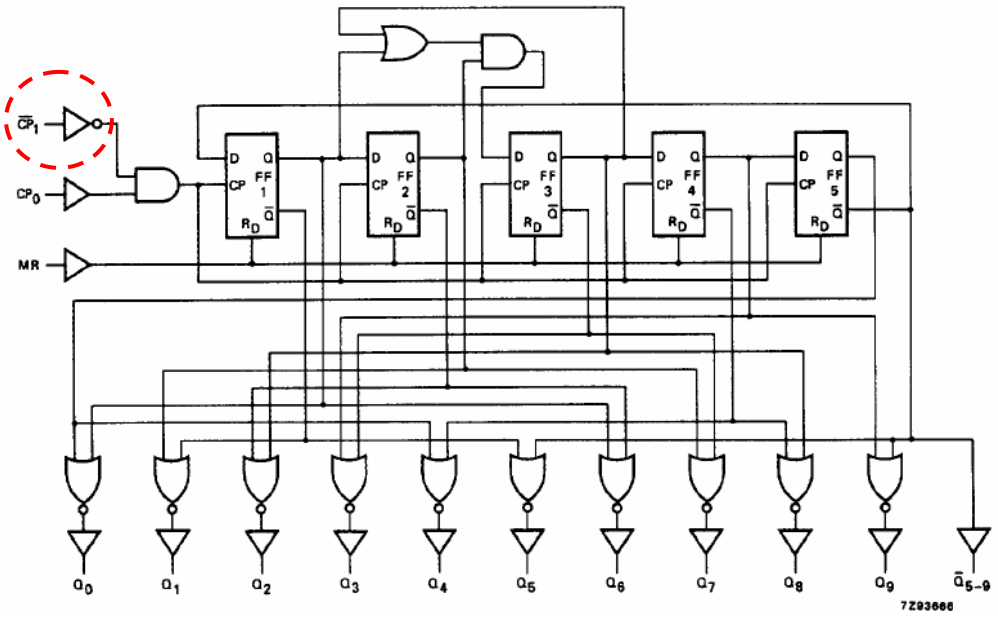



Figure 4. 10 (a)

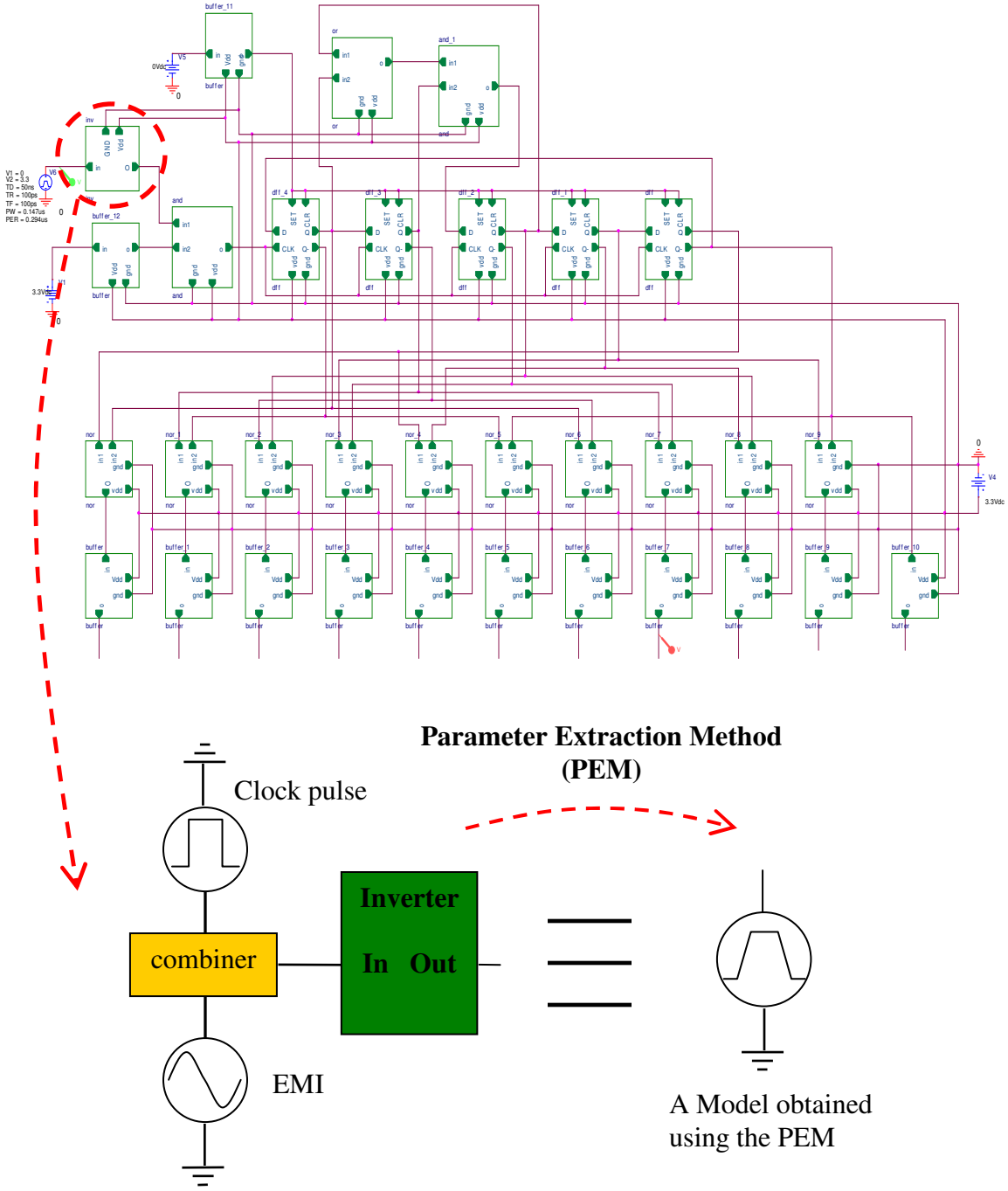



Figure 4. 10 (b)

Figure 4. 10 (a) Schematic of the timer circuit (from data sheet). (b) SPICE Schematic of timer circuits. Effects of microwave interference on clock input port (a CMOS inverter) is modeled using the parameter extraction method. These schematics show the way we combine the SPICE code with the model using the PEM to simulate timer circuit operation under the interference.

At 1GHz 24dBm interference, the output voltage of the model of the inverter clock port obtained using the parameter extraction method is shown in Figure 4. 11. (a) along with the output voltage of the inverter clock port without microwave interference. The graph shows a decrease in the voltage level from 3.3V without the interference to 2.92V with the interference and from 0V without the interference to 1.42V with the interference, indicating a loss of clock signal integrity. Also propagation delays increased to 155ps ($t_{PLH}$) and 257ps ($t_{PHL}$). The result from SPICE simulation shows a good timer operation without the interference. However, at 1GHz 24dBm the saturation of timer output voltage ($O_7$) to $V_{DD}$ (3.3V) is observed as shown in Figure 4. 11. (b), which agrees with measured results shown in Figure 4. 9. (a). Therefore, the upsets in the timer can be attributed to the severe compression in the output voltage of inverter clock port and the increased propagation delays in CMOS inverters [10].

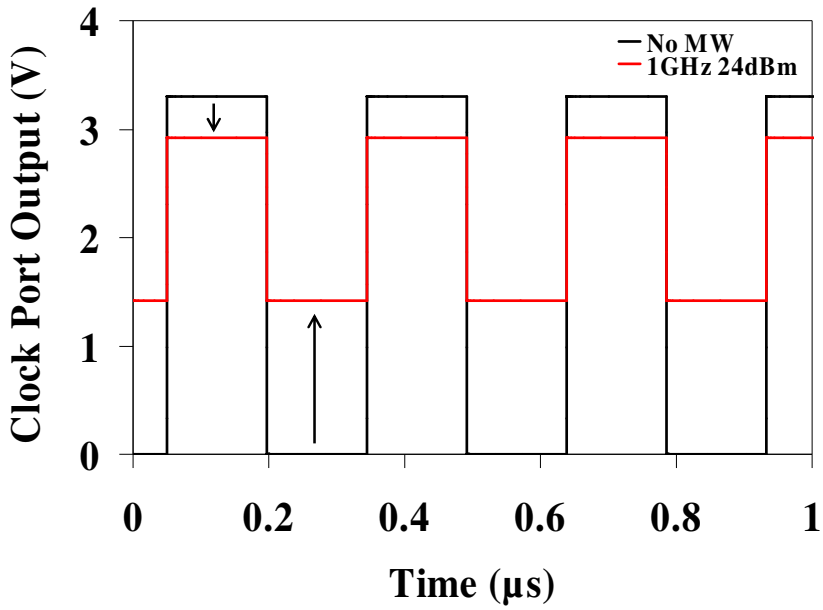



Figure 4. 11 (a)

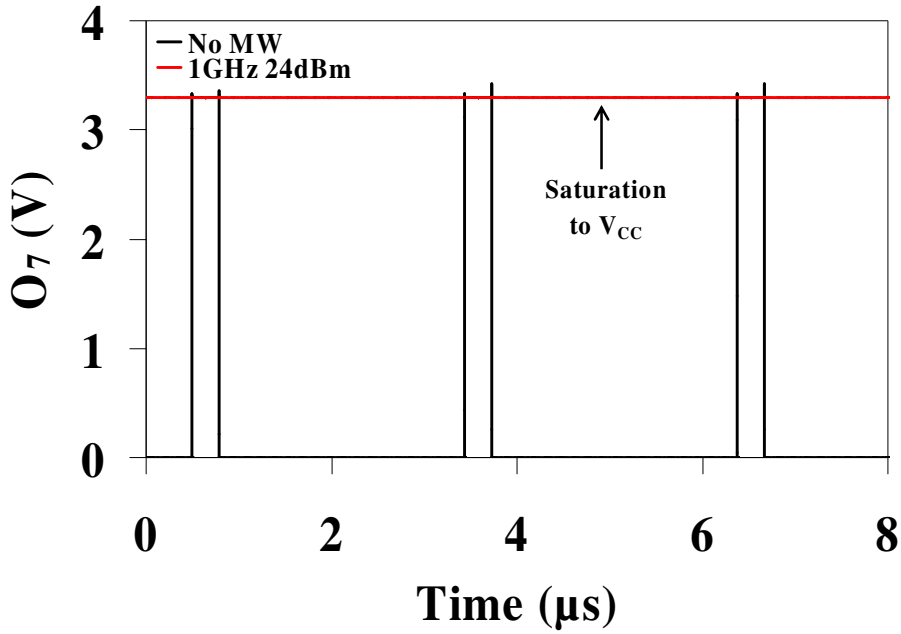



Figure 4. 11 (b)

Figure 4. 11 (a) Output voltage of clock port (a CMOS inverter) with and without 1GHz 24dBm interference, obtained using the parameter extraction method. The output voltage shows a significant change in the output voltage level, leading to a logic error. (b) Simulation results for the timer IC's: output ($O_7$) of timer circuits with and without 1GHz 24dBm interference shows a saturation to $V_{DD}$, demonstrating a good match between measured data (Figure 4. 9. (a)) and simulation result (Figure 4. 11. (b)).

## ***4. 8 Summary***

Microwave interference on CMOS inverter units, revealed severely compressed output voltage swings, and significantly changed propagation delays, as well as a large increase in dynamic power dissipation. A novel parameter extraction method proposed in this work, effectively provided a way of predicting the effects of microwave interference on the dynamic operation of CMOS inverters. The substantial

changes in the quiescent operating point under microwave interference were observed to be responsible for the severe compression in the output voltage swing. Such severe compression is expected to result in critical bit errors. This degradation in the output voltage together with the decrease in the charging and discharging currents, resulted in the changes in the propagation delays. Due to the substantial increase in the short-circuit currents the dynamic power dissipation showed a 95 to 184 % of increase, resulting in elevated current and temperature stress at the device contact and interconnect level. As metallizations are rated for substantially lower current densities by design, catastrophic device failure is expected. In addition, such increase in the power dissipation would introduce a system upset by disrupting all power budget distribution, depriving operating currents from other units. Most prominent increase among the short-circuit currents is observed in the $I_{PSC}{}^{MW}{}_{(steady)}$. Most importantly, the effects of microwave interference were observed to be severe, as the bias voltage and device size were scaled down. Upsets in the timer circuit due to microwave interference on a CMOS inverter clock port were predicted using a model obtained from the parameter extraction method and SPICE simulation and the comparison between simulation result (Figure 4. 11 (b)) and measured result (Figure 4. 9. (a)) showed good agreement.

# Chapter 5: Operational Upsets and Critical Bit Errors in CMOS Digital Inverters due to Pulsed Interference

In this chapter, we study pulsed electromagnetic interference effects on CMOS inverters. When microwave interference is pulsed, the pulsed interference can induce different types of upsets that need to be studied and better understood. Such upsets may depend on pulse properties the characteristics of pulse, as well as device properties such as size, dopant concentration, mobility, and contact resistance. The previous study in [2] only focused on the susceptibility levels of TTL and CMOS inverters to pulsed high power microwave and ultra wide band (UWB) sources, and it is still not clear the relationship between device upsets, pulse properties, and device characteristics.

We identified upsets in CMOS inverters due to pulsed interference and investigated their relation to the characteristics of the pulsed interference as well as device properties. Based on experimental results and calculated channel mobility, relative importance of thermal and charge effects to the current transport of the inverters under CW and pulsed interference was evaluated. The stress on the device contacts and metal interconnects under the interference was also analyzed, and an EMI hardened design scheme mitigating the stress was proposed.

The average power and peak power of CW and pulsed microwave signal is discussed here. Let us define a sinusoidal signal (CW voltage signal) as follows:

$$v(t) = v_{peak} \sin(\omega t + \varphi) \tag{5. 1}$$

Where $v(t)$ is the CW voltage signal, $v_{peak}$ is the peak voltage, $\omega$ is the angular frequency ($=2\pi f$), and $\varphi$ is the phase. For the simplicity we put $\varphi=0$. Then,

$$P^{CW}(t) = \frac{v^2(t)}{R_L} \tag{5. 2}$$

$$= \frac{v^2{}_{peak} \sin^2(\omega t + \varphi)}{R_L} \tag{5. 3}$$

The instantaneous power of the CW signal can be expressed as

$$P_{inst}^{CW} = P^{CW}(t)\Big|_{t=to} \tag{5. 4}$$

$$= v(t_O) i(t_O) \tag{5. 5}$$

$$= \frac{v^2(t_O)}{R_L} \tag{5. 6}$$

Where $P_{inst}^{CW}$ is the instantaneous power, $i(t)$ is the current signal, $R_L$ is the load resistance. The average power of CW signal is defined in Equation 5. 7.

$$P_{avg}^{CW} = \frac{1}{T}\int_0^T P(t)dt \tag{5. 7}$$

$$= \frac{1}{T}\int_0^T \frac{v^2(t)}{R_L}dt \tag{5. 8}$$

$$= \frac{v_{peak}^2}{2R_L} \tag{5. 9}$$

$$= \frac{v_{rms}^2}{R_L} \tag{5. 10}$$

Where, $P_{avg}^{CW}$ is the average power of the CW signal, T is the period, and $v_{rms}$ is $v_{rms} = \frac{v_{peak}}{\sqrt{2}}$. Thus, the peak voltage is given as follows:

$$v_{peak} = \sqrt{2} v_{rms} = \sqrt{2 P_{avg}^{CW} R_L} \tag{5. 11}$$

And the peak power of the CW signal will be

$$P_{peak}^{CW} = \frac{v_{peak}^2}{R_L} = 2 P_{avg}^{CW} \tag{5. 12}$$

$P^{CW}(t)$ and $P_{avg}^{CW}(t)$ are shown in Figure 5. 1 (a) and (b), respectively. The graphs show the relation between the two powers. Mathematically, the two powers are equivalent.

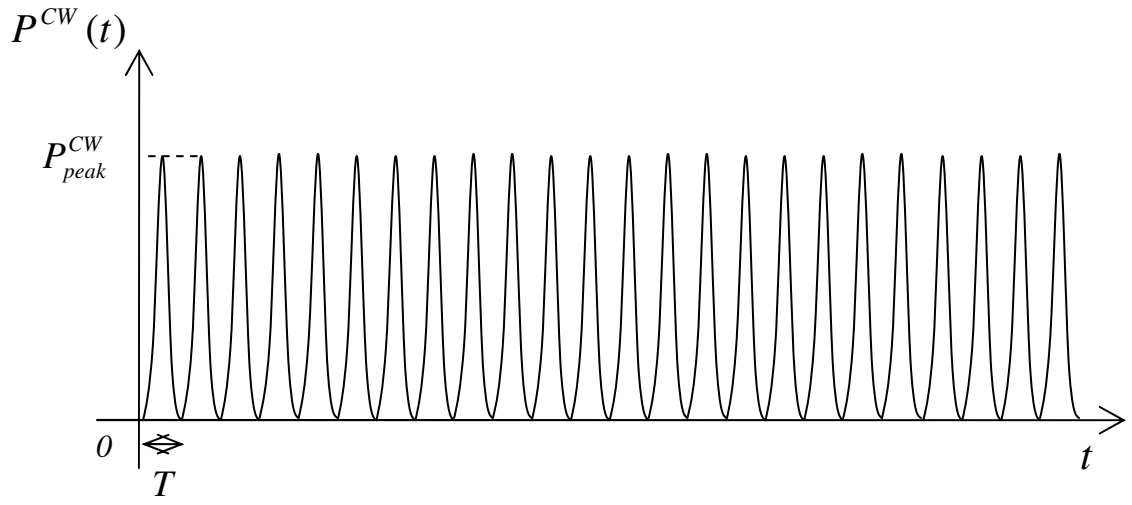



Figure 5. 1 (a)

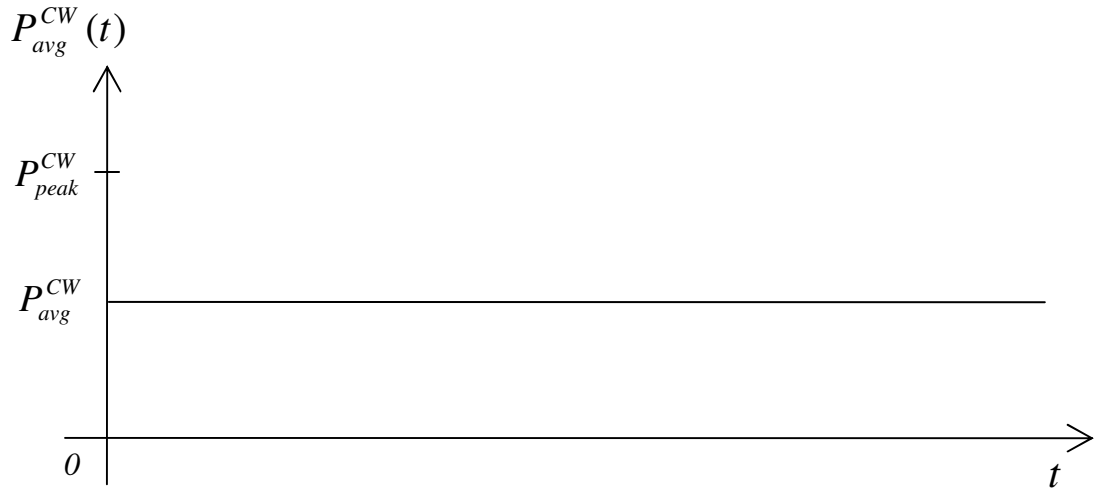



Figure 5. 1 (b)

Figure 5. 1 (a) $P^{CW}(t)$, power of the CW sinusoidal signal. (b) $P_{avg}^{CW}(t)$, average power of the CW sinusoidal signal. The two powers are mathematically equivalent.

For our measurements, a pulsed microwave signal is generated by making a CW microwave signal (a sinusoidal signal) a pulsed signal as shown in Figure 5. 2. (a). The pulse signal has the pulse width of W and the pulse period of P. As shown in the figure, the a CW microwave signal is present when pulse is ON and for this region, the peak power of the pulsed signal is the same as that of the CW signal and 2 times of the average power of CW signal as shown in Figure 5. 2. (b) and Equation 5. 13 (b).

$$P_{peak}^{pulse} = P_{peak}^{CW} = 2P_{avg}^{CW} \tag{5. 13}$$

The average power of the pulsed signal ( $P_{avg}^{pulse}$ ) is expressed in Equation 5. 14 and 5. 15 and shown in Figure 5. 13 (c).

$$P_{avg}^{pulse} = \frac{W}{P} P_{avg}^{CW} \tag{5. 14}$$

$$= \frac{W}{P} \frac{P_{peak}^{CW}}{2} \tag{5. 15}$$

Therefore, the pulse peak power turns out to be equal to the CW peak power. We will see in the next chapter that the peak power of the pulsed signal is important to the vulnerabilities of the devices.

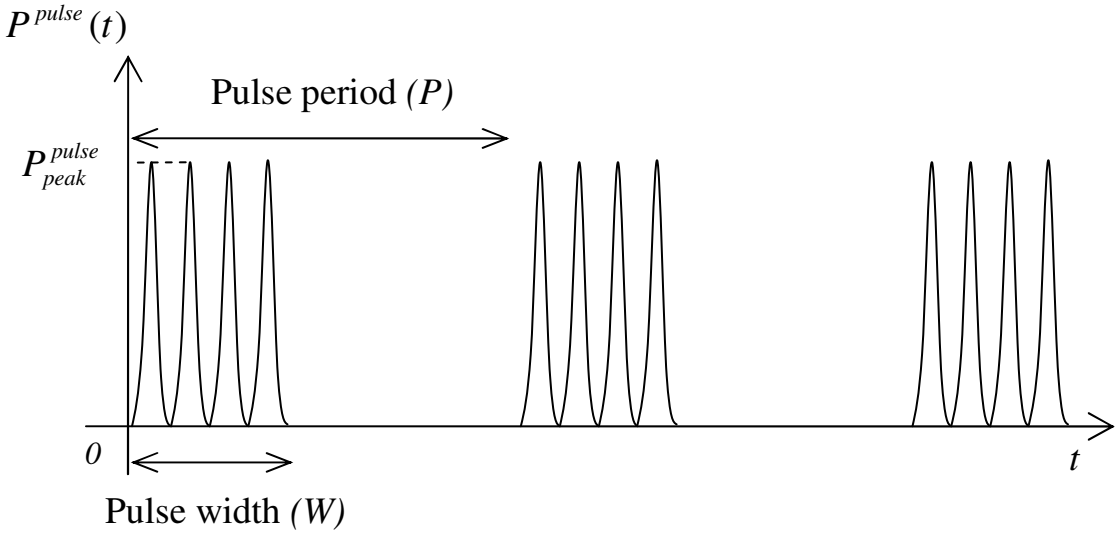



Figure 5. 2 (a)

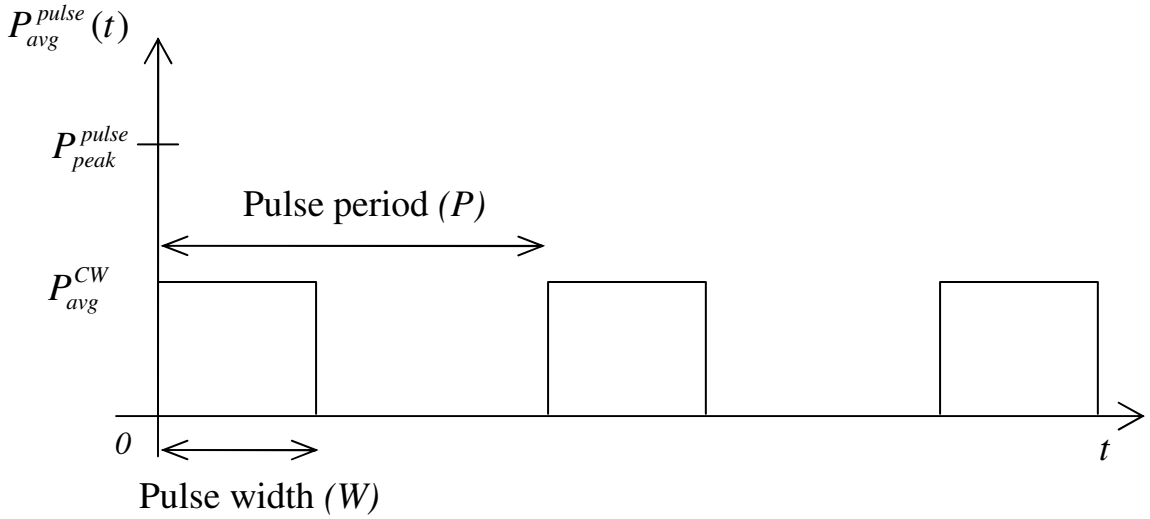



Figure 5. 2 (b)


Figure 5. 2 (c)

Figure 5. 2. (a) $P^{pulse}(t)$, power of the pulsed signal. (b) Average power of the pulsed signal in terms of $P_{avg}^{CW}$. (c) Average power of the pulsed signal based on duty cycle. These three representations are mathematically equivalent.

The average power of network analyzers has dBm unit. The average power in watts can be converted into dBm using Equation 5. 15 and vice versa using Equation 5. 16.

$$dBm = 10\log_{10}\left(\frac{P_{avg}}{1mW}\right) \tag{5. 16}$$

$$P_{avg} = (1mW)10^{\frac{dBm}{10}} \tag{5. 17}$$

## 5. 1 Experimental Details

Three different size CMOS inverters were designed and fabricated based on 1.5µm and 0.5µm technology and designated as inverter 1, 2, and 3. The dimensions of the inverters are given in Table 5. 1. For on-chip measurement at a co-planar probe station, the input and output of each inverter were designed to have a ground-signal-ground (G-S-G) configuration with a 150µm pitch. The current and voltage transfer characteristics of the inverters were measured using a HP 4145B semiconductor parameter analyzer (dashed line) when DC voltage and pulsed microwave signal were applied into the input through a bias-T as shown in Figure. 5. 3. The DC voltage was increased with steps. For the pulsed interference signal, a continuous wave (CW) microwave signal was generated using a HP8753C network analyzer and pulsed by providing an external trigger using a HP8116A pulse function generator. The frequency of the CW microwave signal was 1GHz or 3GHz. The width and period of the pulsed interference signals are given in Table 5. 2. The width and period of the pulsed signals are defined as shown in the inset of Figure 5. 3.

In order to investigate peak power effects on device upsets, the output voltage and current of inverter 3 under pulsed interference were measured in time domain using a HP 4145B and a Tektronix TDS 540 digital oscilloscope as indicated with dotted line in Figure 5. 3. For inverter 3, the average power was fixed at 12.6mW, while the peak power was chosen to be 502mW (27dBm) or 50.2mW (17dBm).

| | | W/L |
|---|---|---|
| Inverter 1 (1.5µm Technology) | p-MOS | 120µm/1.6µm |
| | n-MOS | 40µm/1.6µm |
| Inverter 2 (0.5µm Technology) | p-MOS | 3.6µm/0.6µm |
| | n-MOS | 1.2µm/0.6µm |
| Inverter 3 (0.5µm Technology) | p-MOS | 24µm/0.6µm |
| | n-MOS | 8.1µm/0.6µm |

Table 5. 1 The dimensions (W/L) of CMOS inverter 1, 2, and 3.

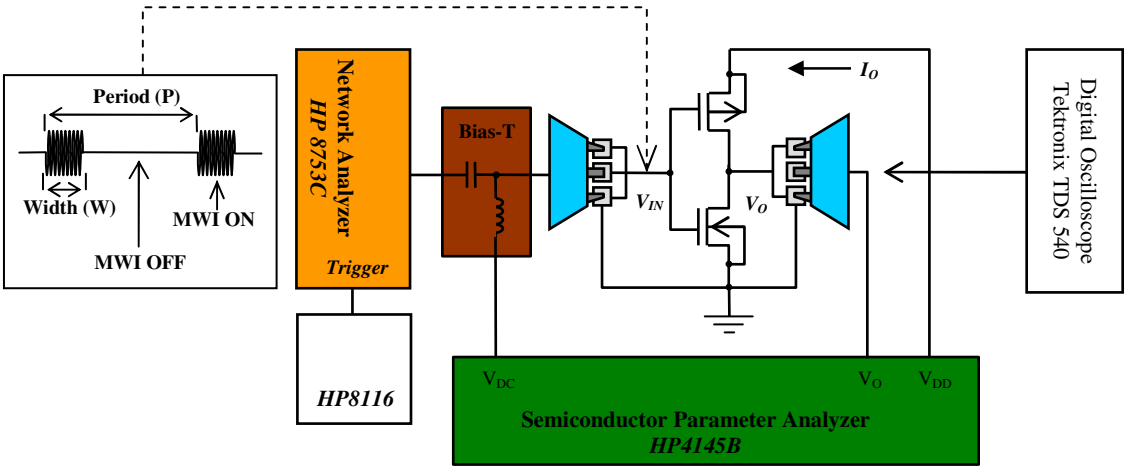



Figure 5. 3 Schematic of on-chip measurement set-up. The output voltage ($V_O$) and current ($I_O$) of the inverters under pulsed microwave interference were measured using a semiconductor parameter analyzer and a digital oscilloscope. Schematic

representation of the pulsed microwave interference (PMWI) signal showing width and period is given in the inset.

| | Width | Period | Peak Power ( $P_{peak}^{pulse}$ ) | Average Power ( $P_{avg}^{pulse}$ ) |
|---|---|---|---|---|
| A | 1ms | 2s | 502mW (27dBm) | 0.126mW |
| B | 1ms | 500ms | | 0.5mW |
| C | 1ms | 200ms | | 1.26mW |
| D | 100ms | 200ms | | 125.5mW |
| E | 100ms | 2s | | 12.6mW |
| F | 200ms | 2s | | 25.1mW |

Table 5. 2 Pulse conditions of interference signals. The width, the period, the peak power, and the average power of the interference signals are given.

## *5. 2 Experimental Results and Discussion*

### 5. 2. 1 Upsets due to Pulsed Microwave Interference

### A. Bit-flip Errors

In this section, we investigate the effects of pulsed microwave interference on the voltage transfer characteristics of the inverter 1, 2, and 3. The voltage and current transfer characteristics of inverter 1 with and without 1GHz pulsed interference were measured and plotted together in Figure 5. 4. The width and period of the pulsed signal were 1ms and 500ms for (a) and 1ms and 200ms for (b) and (c), respectively.

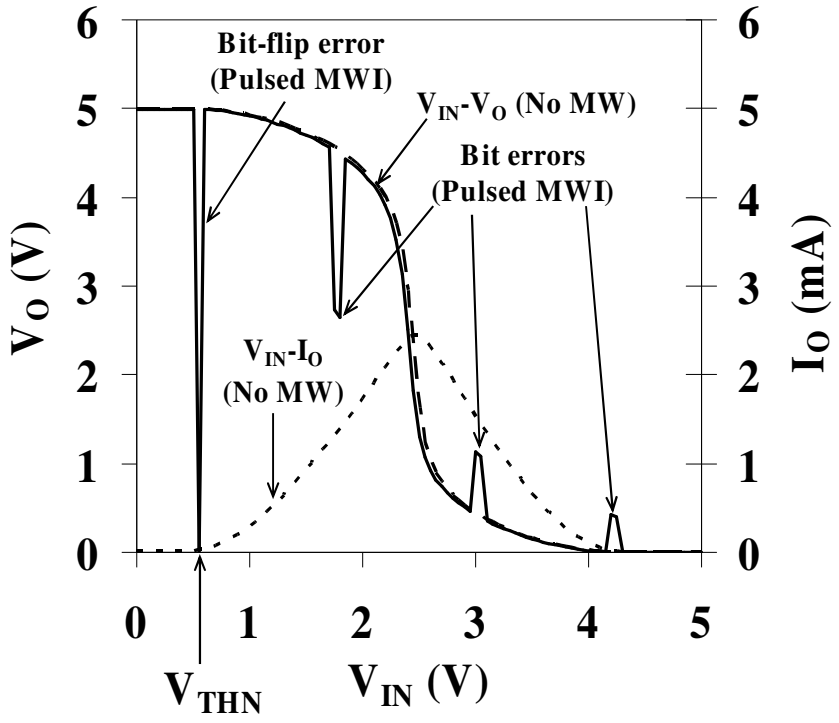



Figure 5. 4 (a)

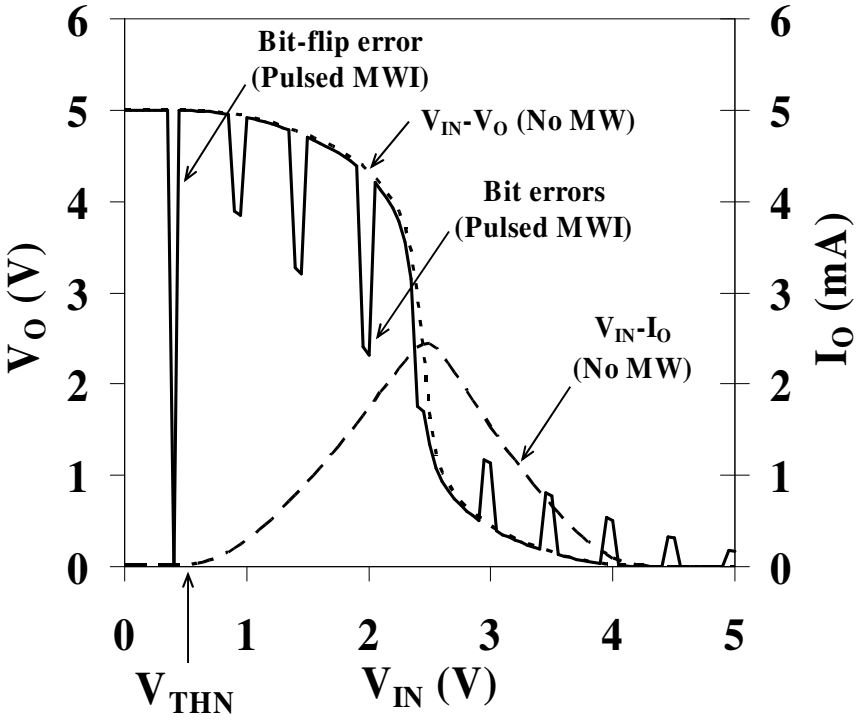



Figure 5. 4 (b)

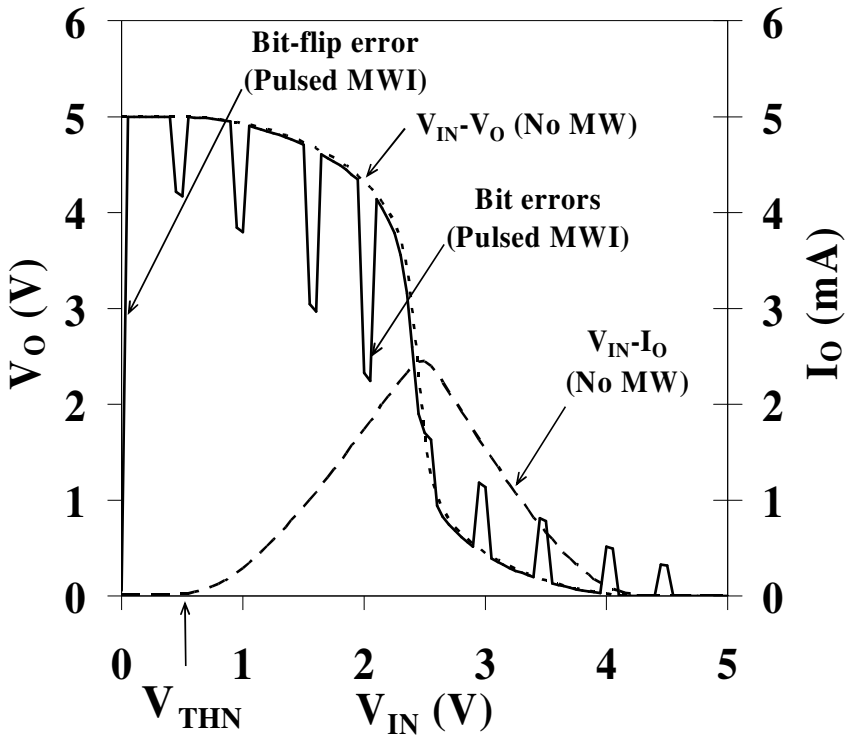



Figure 5. 4 (c)

Figure 5. 4 (a) Voltage and current transfer characteristic of Inverter 1 with and without 1GHz pulsed microwave interference. The width and period of the pulsed signal were 1ms and 500ms (pulse condition B), respectively. A bit-flip error from $V_{OH}$ (5V) to $V_{OL}$ (0V) is observed when the pulsed signal occurs at the threshold voltage ($V_{THN}$=0.55V) of the n MOSFET in the inverter. (b) Voltage and current transfer characteristics of Inverter 1 with pulse condition C, showing bit-flip errors and bit-errors. (c) Voltage and current transfer characteristics of Inverter 1 with pulse condition C, showing a bit-flip error at $V_{IN}$=0V.

As shown in the Figure 5. 4 (a), the output voltage ($V_O$) shows a bit-flip error from $V_{OH}$ (5V) to $V_{OL}$ (0V) as the pulsed signal occurs at the threshold voltage ($V_{THN}$=0.55V) of the n MOSFET in the inverter. After the pulse is OFF, the output voltage returns to $V_{OH}$ (5V) and is observed to be the same as the one without the interference, until the next pulse is ON. When the next pulse is ON at $V_{IN}$=1.75V, 3V,

and 4.2V, the output voltage shows bit errors from 4.44V, 0.49V, and 0.42V to 2.64V, 1.13V, and 0.42V, respectively. With pulse condition C, the output voltage shows bit-flip errors at the threshold (Figure 5. 4. (b)) and at $V_{IN}$=0V (Figure 5. 4. (c)). Thus, it is evident that the inverter is more susceptible to the pulsed interference at the threshold voltage where the channel of the MOSFET is being formed. Such bit-flip errors in the inverters can result in critical system upsets due to logic failure when the inverter unit under the interference is interconnected to other units in the systems.

## B. Other Errors and Noise due to Interference

In Figure 5. 4, we also observe additional spikes in the voltage transfer characteristics. These errors propagate to the next stage and they may or may not result in altering the state of the device. These spikes propagate to the next stage either as noise if the magnitude of the spike is less or equal to the noise margin or as bit errors if the spike exceeds the noise margin, and cause a bit flip-error in the subsequent stage (Figure 5. 5 (b)). Measured noise margin low ($SNM_L$) and high ($SNM_H$) of Inverter 1 are 2V and 2.1V, respectively. We obtained the voltage transfer characteristics of three cascaded inverters when the first inverter is subjected to pulsed interference. We developed the Matlab code to simulate the propagation of errors, using measured transfer characteristics of each inverter. As shown in Figure 5. 5. (a) voltage transfer characteristics of three cascaded inverters (Inverter 1) under pulse condition B shows that the bit-flip error at the threshold voltage propagates to the next inverters, causing logic failure at the third inverter stage. The bit error at $V_{IN}$=1.75V is observed to be eliminated at the next inverters stages due to the regenerative signal properties of the inverters. With pulse condition C, the voltage transfer characteristics showed more

severe bit errors. Among the two bit errors at $V_{IN}$=1.6V and 2V, the larger one (at $V_{IN}$=2V) results in a complete bit-flip error at the third inverter, while the smaller one (at $V_{IN}$=1.6V) is eliminated by regenerative properties. The results show that not only bit-flip errors but also bit errors can cause serious upset problems in logic IC's where individual logic units are interconnected.

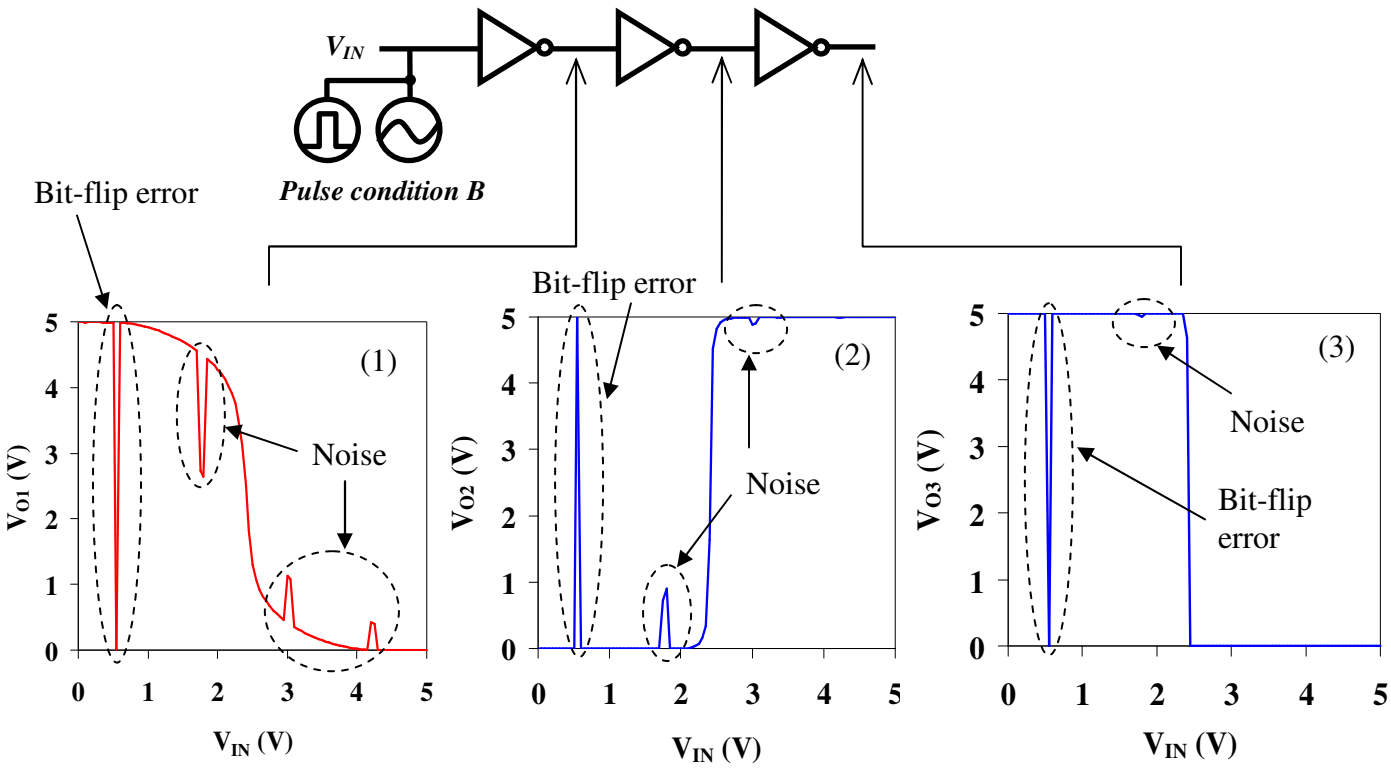



Figure 5. 5 (a)

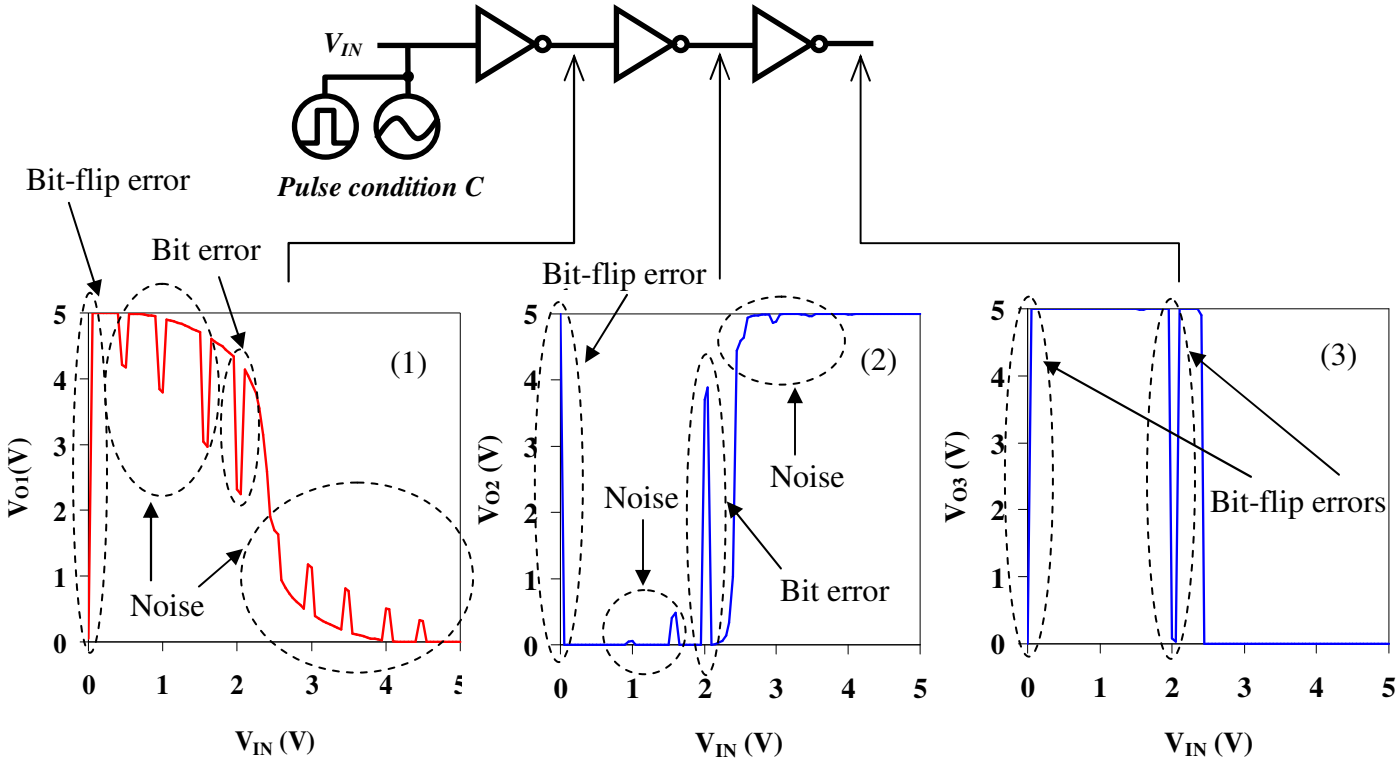



Figure 5. 5 (b)

Figure 5. 5 We developed the Matlab code to simulate the propagation of errors. (a) Voltage transfer characteristics of three cascaded inverters (Inverter 1) under pulse condition B, showing that the bit-flip error at the threshold voltage propagates to the next inverters. The bit error at $V_{IN}$=1.75V is observed to be removed at the next inverters due to the signal regenerative properties of the inverters. Voltage spikes that are smaller or equal to the noise margin become noise. (b) Voltage transfer characteristics of three cascaded inverters (Inverter 1) under pulse condition C, among the two bit errors at $V_{IN}$=1.6V and 2V, the larger one (at $V_{IN}$=2V) results in a complete bit-flip error at the third inverter (Figure 5. 6 (b) inset (3)), while the smaller one (at $V_{IN}$=1.6V) is eliminated by the regenerative properties of the inverters.

## 5. 2. 2 Peak Power Effects on the Inverters

In this section, we investigated peak power effects on inverter 3. For pulsed microwave interference, two peak power levels (27dBm and 17dBm) and three pulse conditions (E, G, and H) are chosen to have the same average power level (11dBm) as given in Table 5. 3.

| | Width | Period | Average Power ( $P_{avg}^{pulse}$ ) | Peak Power ( $P_{peak}^{pulse}$ ) |
|---|---|---|---|---|
| E | 100ms | 2s | 11dBm (12.6mW) | 502mW (27dBm) |
| G | 100ms | 200ms | | 50.2mW (17dBm) |
| H | 500ms | 1s | | 50.2mW (17dBm) |

Table 5. 3 Pulse conditions for inverter 3. Two peak power levels (27dBm and 17dBm) and three pulse conditions (E, G, and H) are chosen to have the same average power level (11dBm).

Measured output voltages ($V_O$) of inverter 3 with $V_{IN}$=0V under pulse condition E, G, and H are given in Figure 5. 6. (a), (b), (c), and (d). As compared in Figure 5. 6, the output voltage ($V_O$) under pulse condition E shows a decrease from 5V to 4.5V as the pulse occurs between 100ms and 200ms, while the $V_O$ under pulsed condition G and H show a decrease from 5V to 4.9V as the pulse occurs (indicated with arrows), showing more degradation in the output voltage level under pulse condition E. The same trend was observed when $V_{IN}$=5V, where the inverter showed more degradation in the output voltage level for pulse condition E (voltage increased from 0V to 0.66V) than for pulse condition G and H (voltage increased from 0V to 0.1V). This indicates that the inverter is more susceptible to the higher peak power of the interference when average power is the same.

Under pulse condition E, the inverter also showed bit-flip errors from 5V to 0V as shown in Figure 5. 6. (d), resulting in 10% of bit-flip error rate. No bit-flip error was observed under pulse condition G and H. Thus, this result also indicates that the pulsed interference with higher peak power cause more bit-flip errors in the inverters.

In order to examine the effects of the peak power on the output current, we measured the output current at the ON ($V_{IN}$=0V), Switching ($V_{IN}$=2.6V), and OFF ($V_{IN}$=5V) states under pulse condition A, C, and E and showed in Figure 5. 7. Under pulse condition G and H where the peak power is 50.2mW (17dBm), the output currents show 4 orders of magnitude increase at the ON and OFF regions but no significant increase at the Switching region as compared with the current without the interference. Under pulse condition E where the peak power is 502mW (27dBm), the currents at the ON and OFF regions show 5 orders of magnitude increase from the current under No MWI, which is 11 to 21 times greater than the currents under pulse condition G and H, respectively. At the Switching region, only 1.2 times increase is observed in the output current under pulse condition E. The higher peak power of the interference results in a larger increase in the output currents when average power is the same. Thus, the results show that the peak power is the most important parameter related to the device upsets.

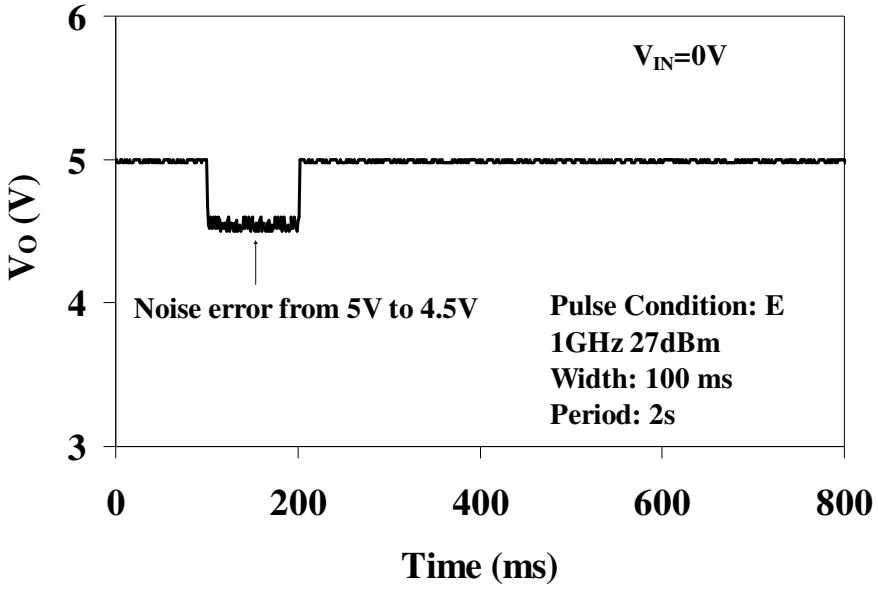



Figure 5. 6 (a)

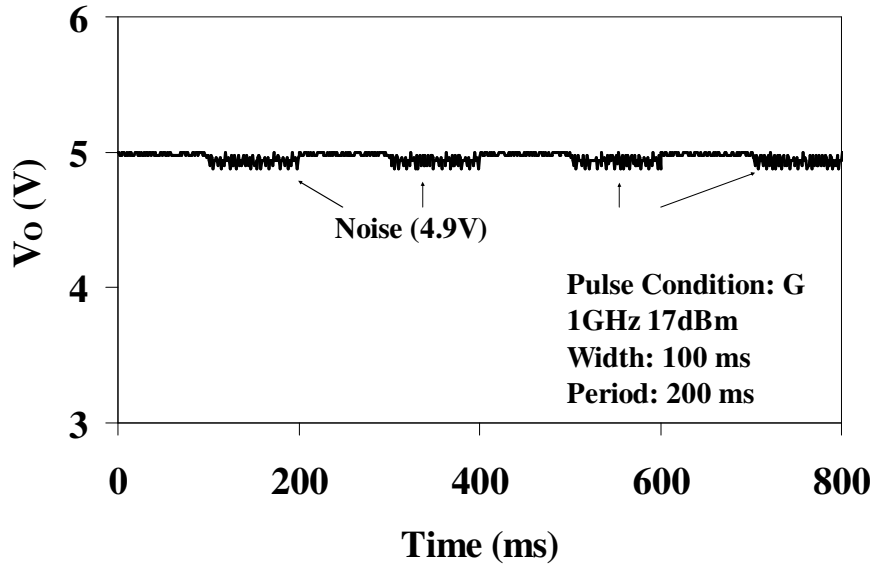



Figure 5. 6 (b).

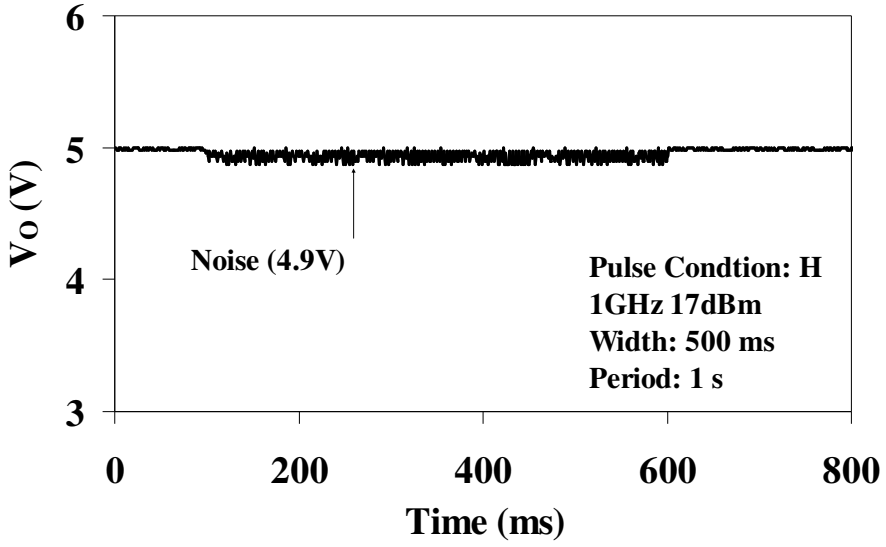



Figure 5. 6 (c).

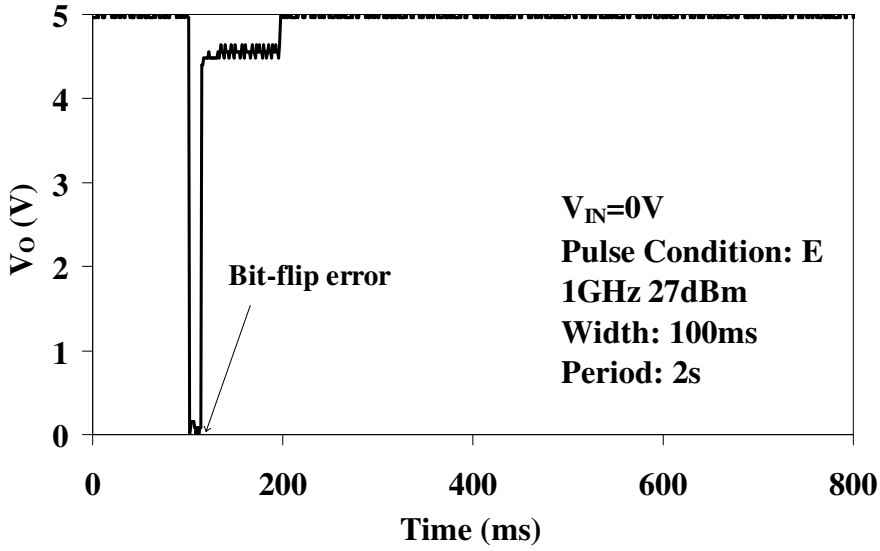



Figure 5. 6 (d).

Figure 5. 6 Output voltages ($V_O$) of inverter 3 with $V_{IN}$=0V. (a) The output voltage shows noise error from 5V to 4.5V with the higher peak power (27dBm (502mW), pulse condition E). (b) $V_O$ shows a little change in the output voltage with the smaller instantaneous power (14dBm, under pulse condition G). (c) $V_O$ shows a little change under pulse condition H. (d) $V_O$ shows a bit-flip error from 5V to 0V under pulse

condition E. The results show that the peak power is the most important parameter related to the device upsets.

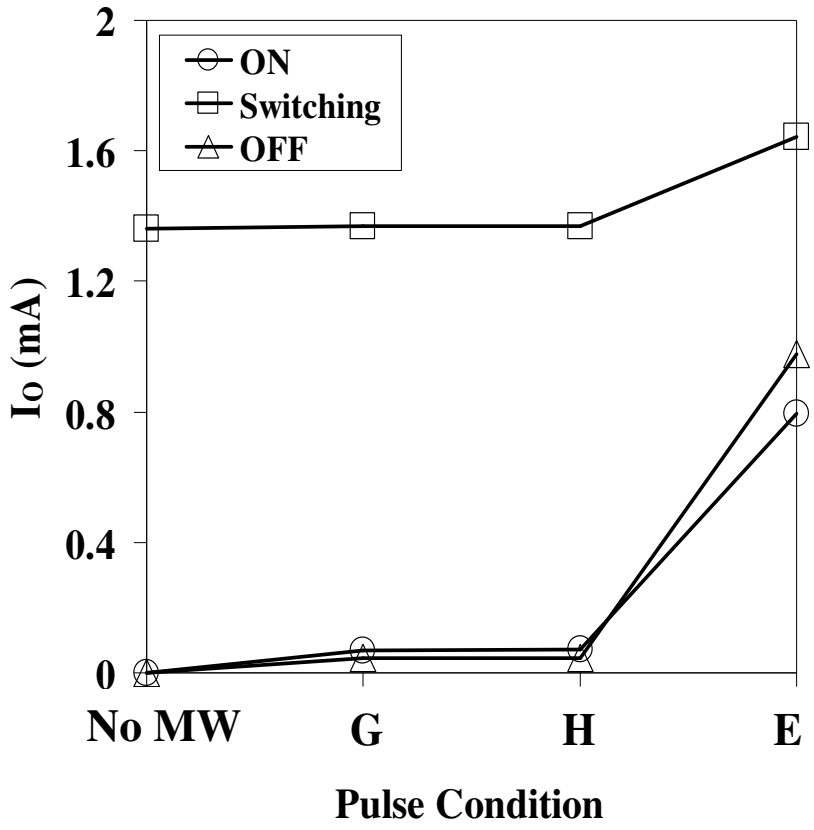



Figure 5. 7 Output current of inverter 3 at the ON, Switching, and OFF regions under pulse condition E, G, and H. The result shows higher current increase with higher peak power.

## 5. 2. 3 Relative Importance of Charge and Thermal Effects

In this section, we investigate relative importance of thermal versus charge effects by comparing the current transfer characteristics under CW and pulsed interference and analyzing calculated channel mobility.

## A. Thermal Effects on Carrier Concentration, Mobility, and Conductivity

**Carrier Concentration:**

The carrier concentration is determined by dopant concentration and intrinsic carrier concentration. For example, the electron concentration ($n_o$) is given as the intrinsic carrier concentration $n_i(T)$ and dopant concentration ($N_d$) as shown Equation 5. 18. Both of the intrinsic carrier and dopant concentrations are temperature dependent functions. The semiconductors used in modern electronic devices are designed to have shallow donors and acceptors resulting in small ionization energies. Thus, at room temperature, all of the dopant carriers (acceptors and donors) can be ionized and thus, the ionized donor and acceptor ions become equal to the dopant concentrations as given in Equation 5. 19 and 5. 20. On the other hand, no significant ionization of the intrinsic carriers occurs until very high temperature [52]. For inverter 1 and 2, the carrier concentrations of the p and n MOSFETs in the inverters are calculated using Equation 5. 8 and shown in Figure 5. 8. As shown in the figure, the carrier concentrations show no significant increase until 600K.

$$n_o(T) = N_d + n_i(300K)\left(\frac{T}{300}\right)^{3/2} \exp\left\{-\left[E_g\left(\frac{1}{2kT} - \frac{1}{600k}\right)\right]\right\} \qquad (5.\ 18)$$

where $N_d$ is the donor concentration ($1.12\times10^{15}$ atoms/cm$^3$), $n_o(T)$ is the electron concentration, $T$ is temperature in Kelvin, $E_g$ is energy band gap (1.124eV), and $k$ is Boltzmann's constant ($8.62\times10^{-5}$eVK$^{-1}$).

$$N_d^+ \approx N_d \tag{5. 19}$$

$$N_a^- \approx N_a \tag{5. 20}$$

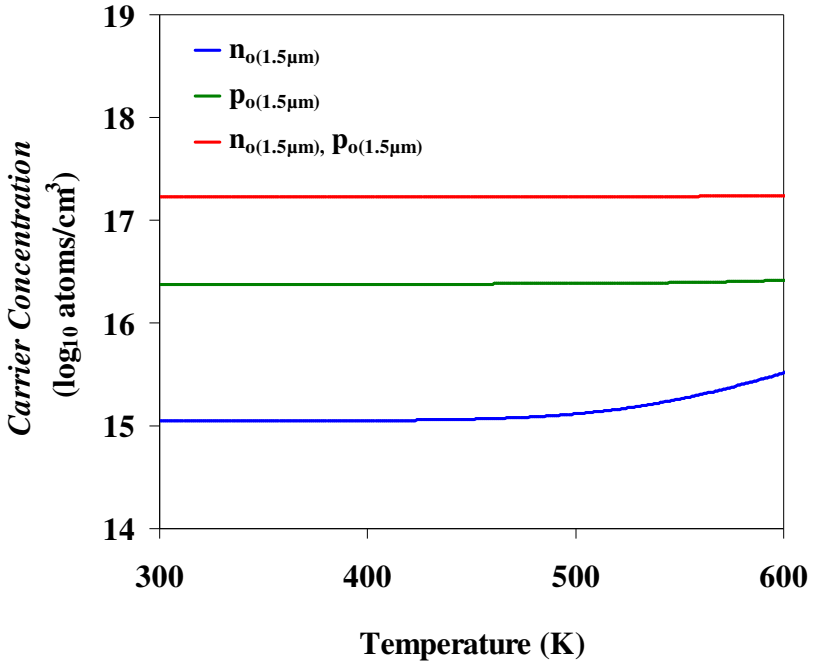



Figure 5. 8 Carrier concentration ($\log_{10}$ atoms/cm$^3$) of n and p MOSFETs in inverter 1 and 2 with respect to temperature. $n_o$ and $p_o$ represent the electron can hole concentration, respectively. 1.5µm and 0.5µm represent inverter 1 and inverter 2, respectively. No significant increase in the carrier concentration is observed until 600K.

**Mobility:**

The mobility of silicon is known to decrease with temperature due to phonon scattering process [52-53]. Temperature dependent channel mobility models of n and p MOSFETs are given in Equation 5. 21 and 5. 22 [53].

$$\mu_n = 88T_n^{-0.57} + \frac{1250T_n^{-2.33}}{1+\left[N_n/(1.26\times10^{17}T_n^{2.4})\right]0.88T_n^{-0.146}} \quad (5.\ 21)$$

$$\mu_p = 54.3T_n^{-0.57} + \frac{407T_n^{-2.23}}{1+\left[N_p/(2.35\times10^{17}T_n^{2.4})\right]0.88T_n^{-0.146}} \quad (5.\ 22)$$

where, $T_n$=$T$/300 with $T$ measured in Kelvin (K), and $N_n$ and $N_p$ represent the total dopant density in n and p MOSFETs. The dopant density of n MOSFET is $1.12\times10^{15}$ atoms/cm$^3$ and that of p MOSFET is $2.4\times10^{16}$ atoms/cm$^3$ for inverter 1. The dopant densities for both of n and p MOSFETs in inverter 2 and 3 are known to be $1.7\times10^{17}$ atoms/cm$^3$. Using the models, the effective channel mobility of n and p MOSFETs ($\mu_n$ and $\mu_p$) for 1.5μm and 0.5μm devices is obtained and plotted in Figure 5. 9. The mobility shows a large decrease in the temperature between 300K and 500K and a moderate decrease above 500K. The slop of the mobility for the n and p MOSFETs ranges from –8.83 cm$^2$V$^{-1}$S$^{-1}$/K to –1.51 cm$^2$V$^{-1}$S$^{-1}$/K, respectively between 300K and 500K, resulting in 2 – 3.4 times more sensitive n-channel mobility ($\mu_n$) to temperature than p-channel mobility ($\mu_p$). It is also observed that the slop of mobility for the larger devices (1.5μm devices) is 1.7 – 2.9 times greater than that for the smaller devices (0.5μm devices), indicating that the mobility of the smaller devices are less sensitive to temperature.

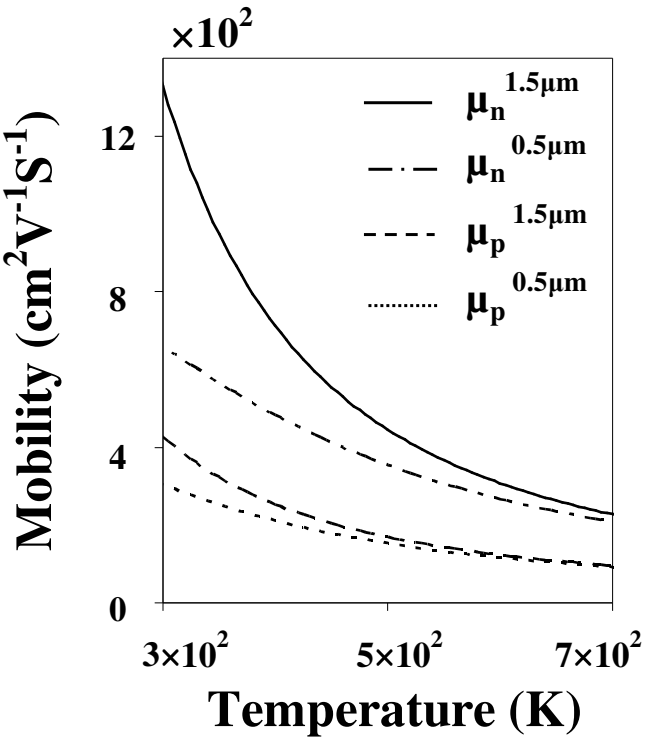



Figure 5. 9 Calculated effective channel mobility of n and p MOSFETs for 1.5μm and 0.5μm devices with temperature (K). Effective channel mobility is inversely proportional to temperature. The mobility of smaller devices is less sensitive to temperature.

**Conductivity:**

The conductivity involves both carrier concentration and mobility. Thus, it is a temperature dependent function. At the temperature ranging between 300K and 600K, the carrier concentration is largely temperature independent as shown in Figure 5. 8. Therefore, the conductivity will decrease along with mobility as the temperature increases as also observed in SOI MOSFET devices due to self-heating [39][54]. Therefore, current decrease implies thermal effects.

## C. Excess Charge Effects

Excess charge effects, on the other hand, increase the output current. High power can increase charges in the device. These excess charges are primarily responsible for the observed operational upsets in the devices.

## D. Experimental Results

As the thermal effects due to mobility degradation decrease and the charge effects increase, output current increases with the microwave interference. The relative importance of the thermal and charge effects can be determined from the current transfer characteristics under CW and pulsed microwave interference.

**Current Transfer Characteristics and Channel Mobility:**

Measured current transfer characteristics ($V_{IN}$–$I_O$) of inverter 1 with and without 1GHz, 24dBm pulsed and CW microwave signal, are shown in Figure 5. 10. The width and period of the pulse were 1ms and 500ms (pulse condition B), respectively.

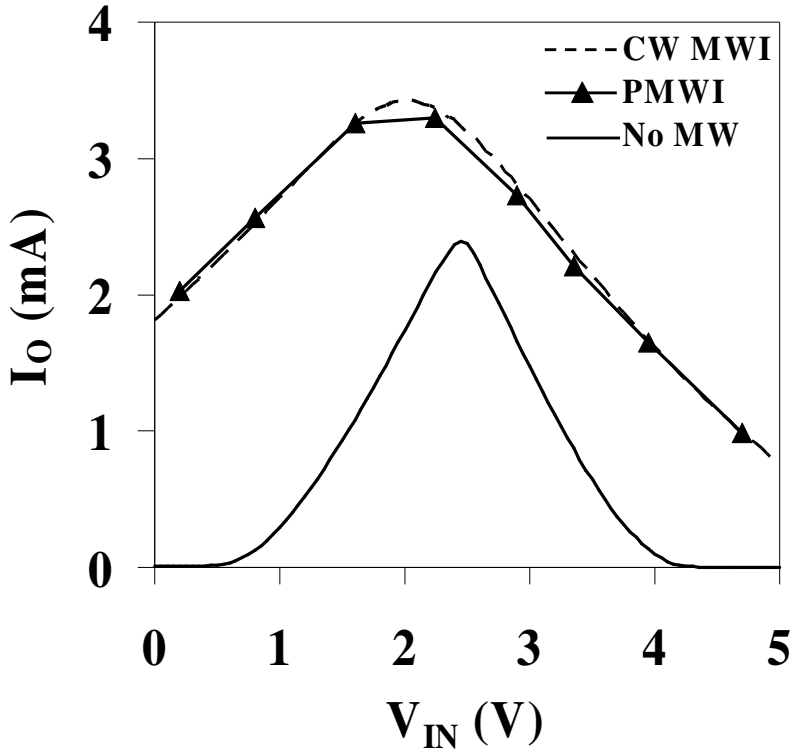



Figure 5. 10 Measured current transfer characteristics of inverter 1 with 1GHz, 24dBm pulsed and CW microwave signal. Solid line represents the output current of inverter 1 without microwave signal. The width and period of the pulsed signal (condition B) is 1ms and 500ms, respectively. The graph shows the changes in the currents under CW and pulsed interference.

As shown in Figure 5. 10, the output current shows up to 3 orders of magnitude increase at the ON, OFF, and switching regions under both pulsed and CW interference. At the ON region, the output current under pulsed interference is observed to be larger than the one with CW interference, and visa-versa at the switching region. At the OFF region, the output currents with pulsed and CW interference are observed to be comparable each other. In order to examine in more detail the observed results and their relationship to pulse characteristics, $\Delta I_O$ under

pulse condition A, B, C, and F was measured as shown in Figure 5. 11. $\Delta I_O$ is defined in Equation 2.

$$\Delta I_O = I_O^{PEMI} - I_O^{CW} \quad (5.\ 23)$$

where, $I_O^{PMWI}$ is the output current of the inverter under pulsed interference and $I_O^{CW}$ is the output current under CW interference.

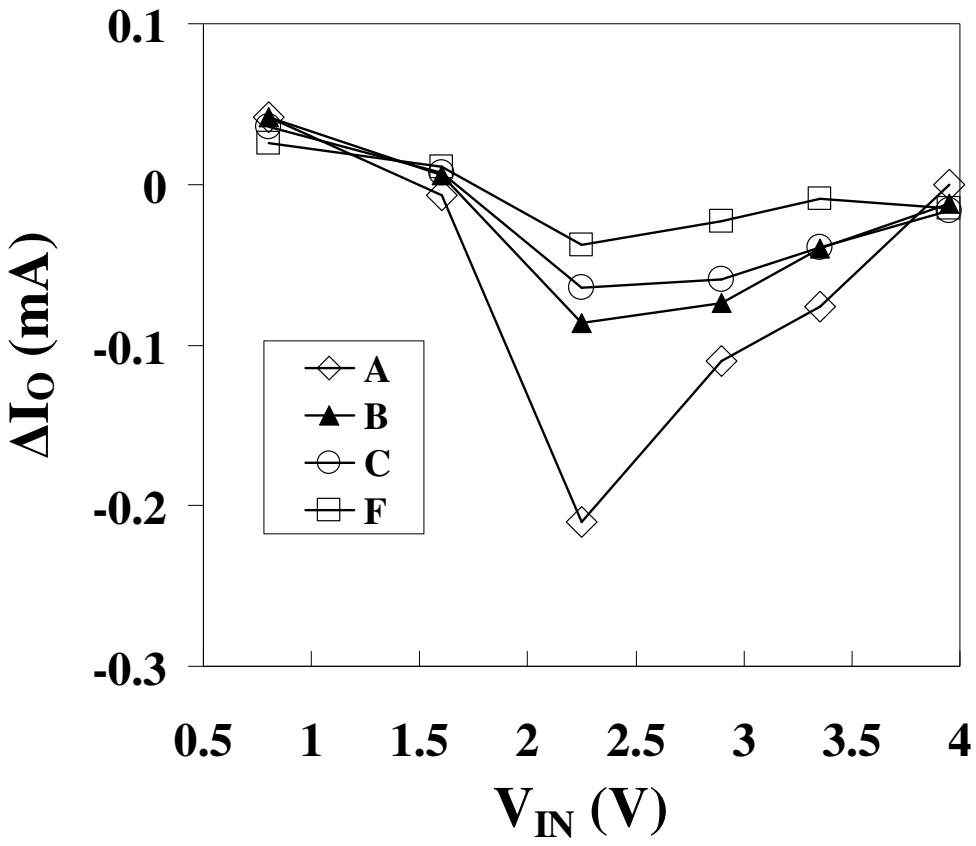



Figure 5. 11 $\Delta I_O$ versus $V_{IN}$ for inverter 1 under pulse condition A, B, C, and F. $\Delta I_O = I_O^{PMWI} - I_O^{CW}$. The figure shows a little thermal effects at the ON states but no thermal effects at the switching and OFF states where charge effects are dominant.

Figure 5. 11 shows positive $\Delta I_O$ when $V_{IN}$ is between 0V and 1.7V, which corresponds to the ON region for inverter 1. In this region, $\Delta I_O$ shows a little but

gradual decrease from pulse condition A to F where the average power increases from 0.126mW to 25.1mW. In the switching region where $V_{IN}$ is between 1.7V and 3.7V, on the other hand, $\Delta I_O$ shows negative values. Here, $\Delta I_O$ is observed to increase with increasing average power as shown in the changes of $\Delta I_O$ from –0.21mA under pulse condition A (average power: 0.126mW) to –0.037mA under pulse condition F (average power: 25.1mW) at $V_{IN}$=2.25V. When $V_{IN}$ is between 3.7V and 4V corresponding to the OFF region, $\Delta I_O$ is observed to be close to zero.

The fundamental reason for this graph is to identify the relative importance of the thermal effects due to mobility degradation with respect to the excess charge effects [2] in the channel of the MOSFETs. Thermal effects result in a reduction in the output current due to the reduction in the effective mobility of the channel from phonon scattering [52-53]. Given that the CW interference delivers significantly higher power (251mW) than the pulsed interference, it is expected that the thermal effects due to mobility degradation would be more pronounced. If this is the case then on the basis of the calculated channel mobility, this will result in a decrease in the output current due to the reduction in the effective mobility, thus giving an inversely proportional character to the output current under interference. Excess charge effects, on the other hand, that increase the charge in the channel substantially, show an output current increase with increasing interference power [2]. Thus, thermal and charge effects compete with each other in contributing to the output current under microwave interference. Therefore, a positive $\Delta I_O$ where $I_O^{CW}$ is lower than $I_O^{PMWI}$, indicates that the thermal effects compete with the excess charge effects to give an $I_O^{CW}$ value lower than expected, and vice-versa, when the thermal effects that reduce

the output current are absent where the $I_O^{CW}$ due to the CW higher power should be higher than $I_O^{PMWI}$, resulting in negative $\Delta I_O$.

Therefore, a positive $\Delta I_O$ at the ON region in Figure 5. 11 indicates that a weak component of thermal effects is compensating the current increase resulted from the charge effects. At the switching region, $\Delta I_O$ shows negative, indicating that the effects of interference are predominantly due to excess charge effects. The thermal effects are observed to be very small at the OFF region, where $\Delta I_O$ is close to zero. The variation in $\Delta I_O$ suggests that the increase in the output current of the inverters under the interference is mainly due to excess charge effects rather than thermal effects which appear to have a weak presence at the ON region. This also suggests that bit-flip errors at $V_{THN}$ are excess charge related.

**Thermal and Charge Effects for Smaller Devices :**

The thermal and charge effects on smaller devices are also studied by examining $\Delta I_O$ of inverter 2 under pulse condition A, C, and E as shown in Figure 5. 12. As we predicted in the channel mobility analysis, $\Delta I_O$ shows negative values due to less sensitive channel mobility to temperature as shown in Figure 5. 9, demonstrating that the current increase in inverter 2 under interference is excess charge related.

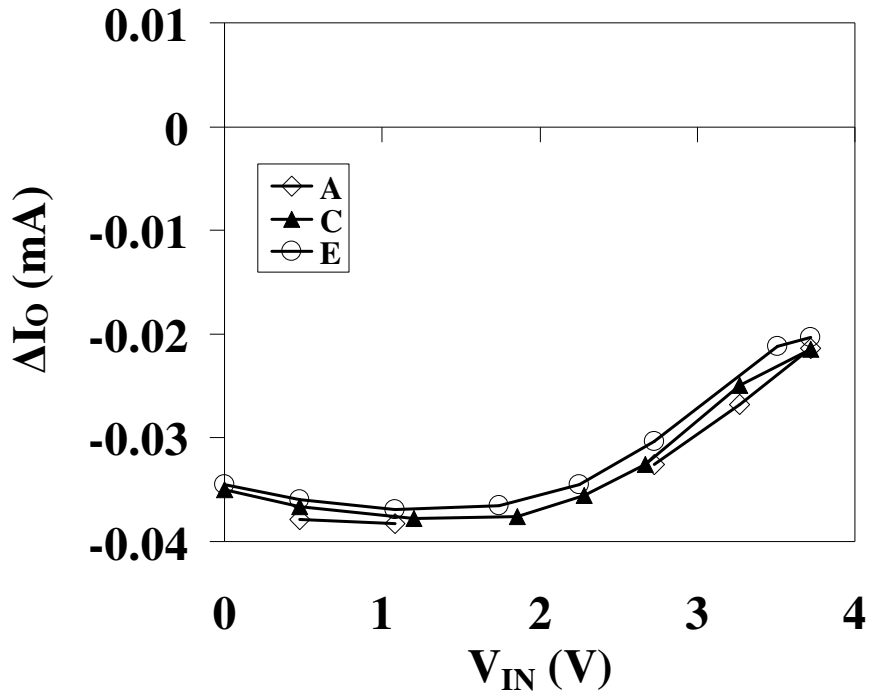



Figure 5. 12 $\Delta I_O$ versus $V_{IN}$ for inverter 2 (0.5μm) under pulse condition A, C, and E, showing that excess charge effects are dominant for the smaller devices due to a less sensitive mobility to temperature.

## 5. 2. 4 Stress on Device Contacts and Interconnects and EMI Hardened Design

### A. Stress on Contacts and Metal Interconnects

In this section stress on device contacts and metal interconnects due to pulsed interference is studied. Based on the calculated power dissipation on the contacts and interconnects of inverters under the interference, we evaluate the stress and propose an EMI hardened design mitigating such stress using interdigitated finger design at the gates of MOSFETs in inverters. From measured current transfer characteristics of

inverter 1 and 2 under pulse condition C (Table 5. 2), we found that the output currents of inverter 1 and 2 at $V_{IN}$=0V show 2 and 3 orders of magnitude increase, respectively. Such increase in the output currents will result in severe stress on the contacts and interconnects due to significantly increased power dissipation, eventually leading to catastrophic failure. Four contact resistance values of inverter 1 and 2 are given in Table 5. 4. As given in Table 5. 4, the resistance values of n+ active and p+ active contacts are the highest ones among others resulting in the highest increase in power dissipation. As the size of the devices decreases, the resistance values increase. Therefore, it is expected that n+ active and p+ active contacts are the most susceptible areas to the interference for a catastrophic failure, and the devices become more vulnerable from the stress as the size of the devices decrease.

| Contacts | Contact Resistance (Ω) | |
|---|---|---|
| | Inverter 1 (1.5µm Technology) | Inverter 2 (0.5µm Technology) |
| Metal (mc) | 0.05 | 0.97 |
| n+ active (n+c) | 45.7 | 64.9 |
| p+ active (p+c) | 39.5 | 149.7 |
| Poly (pc) | 25.4 | 28.2 |

Table 5. 4 Contact resistance values for inverter 1 and inverter 2 indicating that contact resistance values of n+ active and p+ active contacts are the highest among those of others. Thus, n+ active and p+ contacts are expected to be most susceptible areas to EMI for catastrophic physical failures.

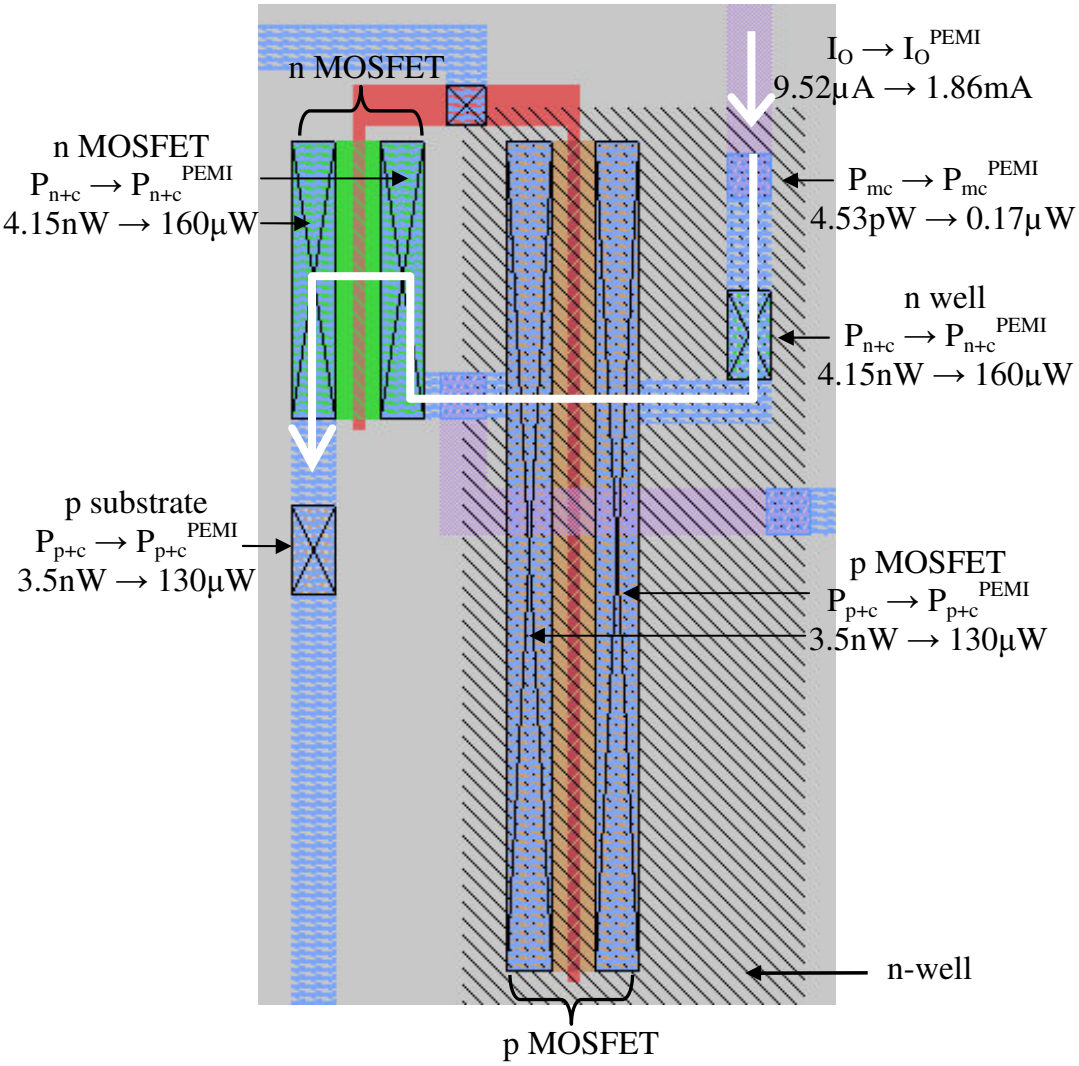
Metal interconnects will also experience substantial increase in the current, resulting in metal electromigration. It is known that metal electromigration results from a large current flow in the metal interconnects and leads to physical failure [50]. The

threshold current level that the metal interconnects are not designed to exceed. For a 2μm device, this is 1–2mA per width (W) in μm. For our case, minimum width (W) of the metal interconnects by design rules is 2.4μm for the 1.5μm inverters. Thus, the threshold current of the metal interconnect having 2.4μm width is 2.4–4.8mA. From measured current characteristics, the output current of inverter 1 under pulse condition C showed 3.4mA at $V_{IN}$=2V which exceeds the threshold current, and this demonstrates that the pulsed interference can cause severe stress on the metal interconnects.

## B. EMI Hardened Design: Interdigitated Finger Gates

In order to develop a design scheme mitigating such stress, we proposed interdigitated gate design fabricated two inverters (one single and one interdigitated gate) based on 1.5μm technology. We then evaluated and compared the power dissipation at the contacts in each device as shown in Figure 5. 13 (a) and (b), respectively. We designate the layouts shown in Figure 5. 13 (a) as inverter A and (b) as inverter B. Inverter A has W/L ratio of 120μm/1.6μm for p MOSFETs and 40μm/1.6μm for n MOSFETs. Inverter B has four interdigitated fingers for p MOSFETs, and each finger has W/L ratio of 29.6μm/1.6μm. For n MOSFETs, three interdigitated fingers are used, and each finger has W/L ratio of 12.8μm/1.6μm. Thus, the inverter has overall W/L ratio of 118.4μm/1.6μm for p MOSFETs and 38.4μm/1.6μm for n MOSFETs. With these inverters, the output currents under pulse condition C are measured when $V_{IN}$=0V. The output current showed an increase from 9.52μA to 1.86mA (195 times increase) for inverter A and from 5.13μA to 1.63mA

(317 times increase) for inverter B, indicating 2 orders of magnitude increase for both inverters. The contact resistance values are given in Table 5. 4 (1.5μm technology). Based on measured currents, we calculated the power dissipation at each contact as indicated with the arrows in Figure 5. 13 (a) and (b). The results from Figure 5. 13 (a) and (b) are summarized in Table 5. 5. The table shows the power dissipation under the interference at each contact and the amount of reduction in the power dissipation with inverter B over inverter A. The table indicates that the power dissipation at n+ active and p+ active contacts of n wells, p MOSFETs, n MOSFETs, and p substrates can be reduced by 79.8–91.5% with inverter B. Overall power dissipation under the PMWI at the contacts with inverter A was 870μW, while inverter B showed 302.1μW of power dissipation, resulting in 65.3% reduction. Therefore, we can conclude that interdigitated finger design can significantly reduce power dissipation at each contact by increasing current flowing paths and contact points, leading to substantially reduced stress on the device contacts. It is also suggested (1) to broaden metal interconnects with lower sheet resistance and (2) to increase the number of contacts at each contact point. These will (1) increase the maximum current that the metal can hold (2) and reduce effective contact resistance at each contact point by placing the contacts in parallel.


n MOSFET
$I_O \rightarrow I_O^{PEMI}$
9.52µA → 1.86mA
n MOSFET
$P_{n+c} \rightarrow P_{n+c}^{PEMI}$
4.15nW → 160µW
$P_{mc} \rightarrow P_{mc}^{PEMI}$
4.53pW → 0.17µW
n well
$P_{n+c} \rightarrow P_{n+c}^{PEMI}$
4.15nW → 160µW
p substrate
$P_{p+c} \rightarrow P_{p+c}^{PEMI}$
3.5nW → 130µW
p MOSFET
$P_{p+c} \rightarrow P_{p+c}^{PEMI}$
3.5nW → 130µW
n-well
p MOSFET

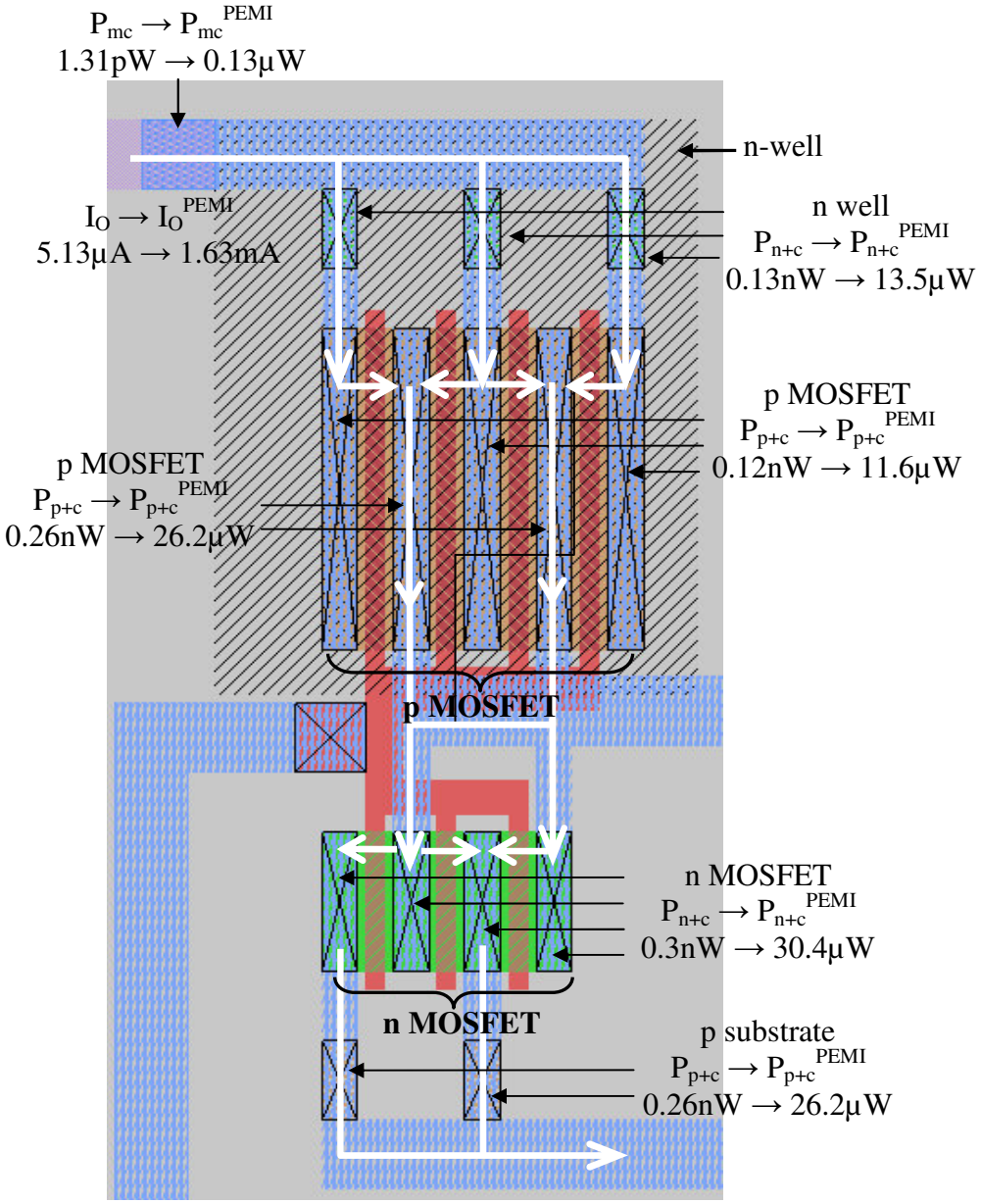



Figure 5. 13 (a) Layout of inverter A having MOSFETs with single finger gate. Dotted line represents current path. Power dissipation at each contact is calculated using measured currents and indicated with arrows. (b) Layout of inverter B having MOSFETs with interdigitated finger gates. Current path is also represented with dotted lines. The figures show that interdigitated finger gates can substantially mitigate the stress on the device contacts and metal interconnects by reducing maximum of 91.5% in power dissipation.

| Power Dissipation | Design A | Design B | Reduction at Each Contact |
|---|---|---|---|
| $P_{n+c\ (n\ well)}$ | 160 μW | 13.5 μW | 91.5 % |
| $P_{p+c\ (p\ MOSFET)}$ | 130 μW | 11.6–26.3 μW | 91.1–79.8 % |
| $P_{n+c\ (n\ MOSFET)}$ | 160 μW | 30.4 μW | 81 % |
| $P_{p+c\ (p\ substrate)}$ | 130 μW | 26.2 μW | 79.8 % |

Table 5. 5 The results from Figure 5. 14 (a) and (b) are summarized here. Power dissipation under pulse condition C at each contact in the inverters of design A and B, respectively. Maximum of 91.5% reduction in power dissipation is achieved with interdigitated finger devices, resulting in EMI hardened design.

## *5. 3 Latch-up Effects in CMOS Inverters due to Pulsed Microwave Interference*

### 5. 3. 1 Experimental Details

Latch-up effects of CMOS inverters due to pulsed electromagnetic interference, is studied in this section. The inverters were designed and fabricated as cascaded inverters in packaged chips and placed on a PC board for measurements. The cascaded inverters consisted of two identical inverters with a width to length ratio (W/L) of 3.2μm/1.6μm for n MOSFETs and 9.6μm/1.6μm for p MOSFETs. The output voltage ($V_{O1}$) of the cascaded inverters were measured using a Tektronix TDS 540C oscilloscope when pulsed microwave signal was injected into the input of the inverters through a bias-T as shown in Figure 5. 14. The microwave signal was generated using a HP E4438C signal generator, amplified by an Ophir RF amplifier, and pulsed using a Standford Research System pulse generator. The peak power of

pulsed microwave signal is between from 3dBm to 33dBm and the frequency ranged between 1.23GHz and 4GHz. The width and period of the pulse signal were 800ns and 10ms, respectively.

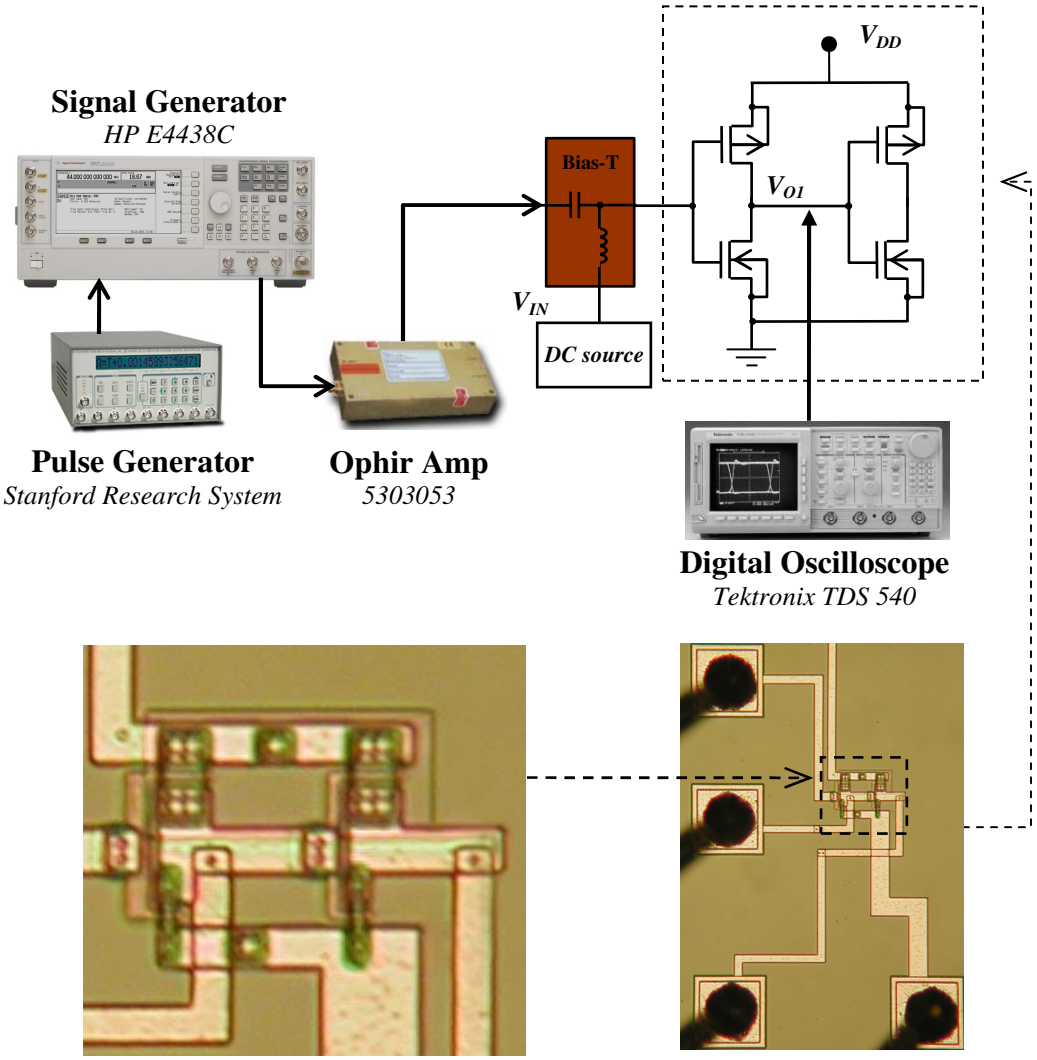



Figure 5. 14 Schematic of the measurement set-up for pulsed microwave interference for cascaded inverters. Pulsed microwave signal is injected into the input of the inverters through a bias-T, and the output of the first inverter is measured using an oscilloscope.

### 5. 3. 2 Latch-Up in CMOS Inverters due to Pulsed Interference

With 1.23GHz pulsed microwave injection and input logic low ($V_{IN}$=0V), the output voltage of the first inverter ($V_{O1}$) of the cascaded inverters showed a gradual decrease from logic high ($V_{OH}$=5V) as the power of microwave signal increased (Figure 5. 15). As seen by the envelope of the pulsed interference in Figure 5. 15 inset 4, the pulsed signal occurs between 2.5μs to 3.3μs showing 800ns of pulse width. Note that the time scale at the X axis in each inset is not absolute time. The peak power of the pulsed signal is indicated and the corresponding average power is given in Table 5. 6. At 23dBm (peak power), the output ($V_{O1}$) showed a bit error that retuned to normal operation after the pulsed signal was OFF indicating a soft error. At 25.5dB, the output ($V_{O1}$) showed gradual decrease with repeated pulsed signal (Figure 5. 16 inset 2), and then a latch-up of the output to 1.23V (Figure 5. 15 inset 3) at 3 seconds of measurement time as schematically shown in Figure 5. 15 inset 1. After the latch-up of the output, the inverters refused to respond to the input stimuli, and the output stayed at 1.24V even when the pulsed interference was OFF. The inverters needed to be reset to obtain normal logic operation again. With input logic high ($V_{IN}$=5V), the cascaded inverters also suffered from a soft error due to a gradual increase in $V_{O1}$ from 0V as the power of microwave signal increased (Figure 5. 16 inset 1), and the output showed a latch-up to 1.24V at 26.3dBm (Figure 5. 16 inset 2).

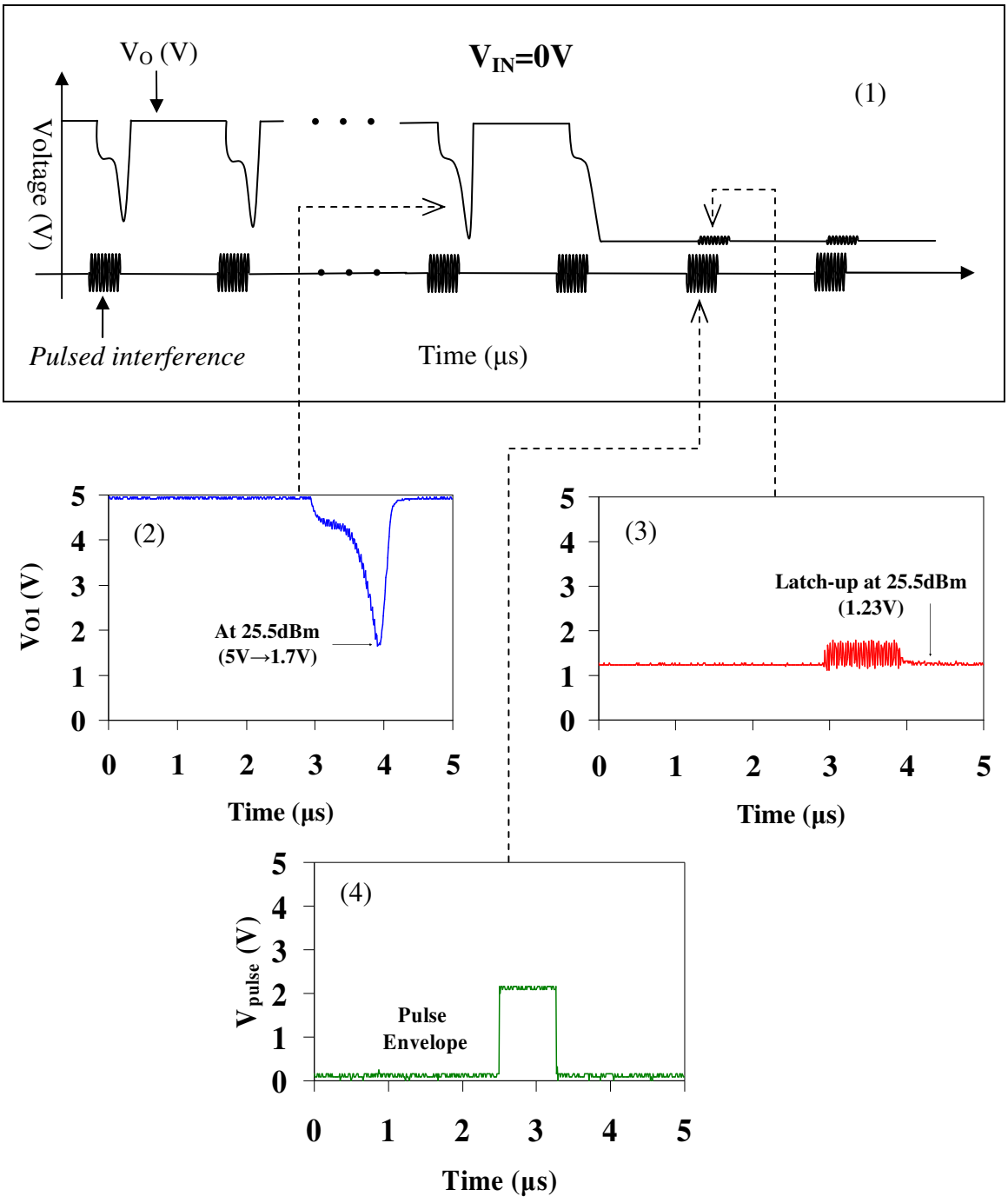



Figure 5. 15 Measured output voltage ($V_{O1}$) of the first inverter for input logic low ($V_{IN}$=0V) with 1.23GHz pulsed microwave signal. The width and period of the pulse were 800ns and 10ms, respectively. (1) Schematic representation of the output voltage and the interference signal. (2) Measured output voltage showing a bit-flip

error from 5V to 1.7V at 25.5dBm. (3) Measured output voltage showing a latch-up to 1.24V at 25.5dBm with repeated pulse. Device failed to respond even after the interference and gained normal operation after resetting the power ($V_{DD}$). (4) The envelope of pulse signal.

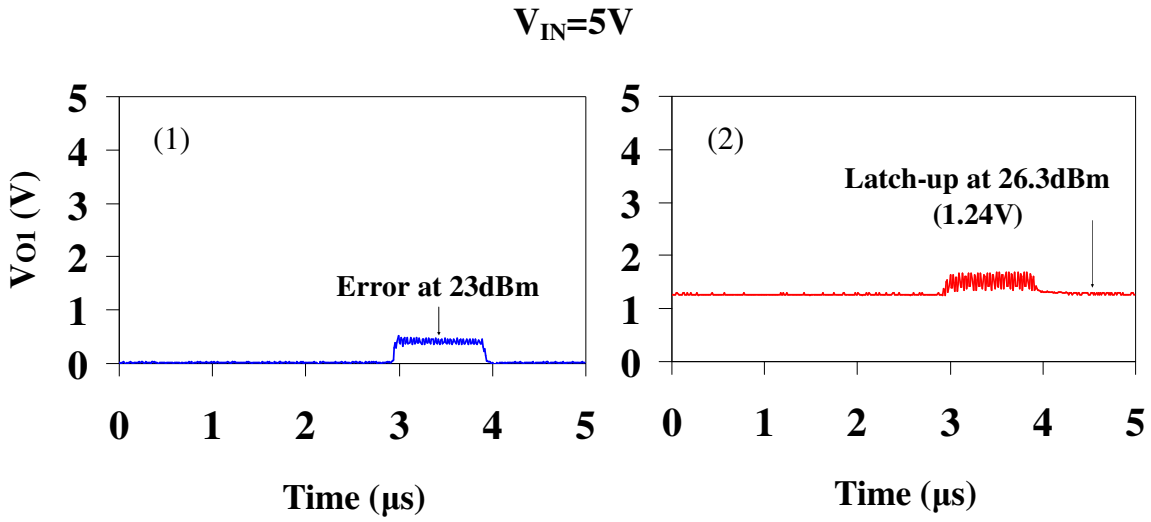



Figure 5. 16 Measured output voltage ($V_{O1}$) of the first inverter for input logic high ($V_{IN}$=5V) with 1.23GHz pulsed microwave signal. (1) The output voltage shows an increase at 23dBm. (2) The output shows latch-up to 1.24V at 26.3dBm, indicating that the inverters with input logic low are more susceptible to the pulsed microwave interference.

With 4GHz pulsed microwave injection, the inverters showed a latch-up of the output to 1.24V at 29.1dBm for input logic low and 31.9dBm for input logic high as given in Figure 5. 17. Thus, the results indicate that the power level causing the latch-ups at the output increases as the frequency of the microwave signal increases, suggesting suppressed power effects at higher microwave frequency. The figure also indicates that the latch-ups for the inverters with input logic low occur at lower power

level, indicating that the inverters with input logic low are more susceptible to the pulsed microwave interference.

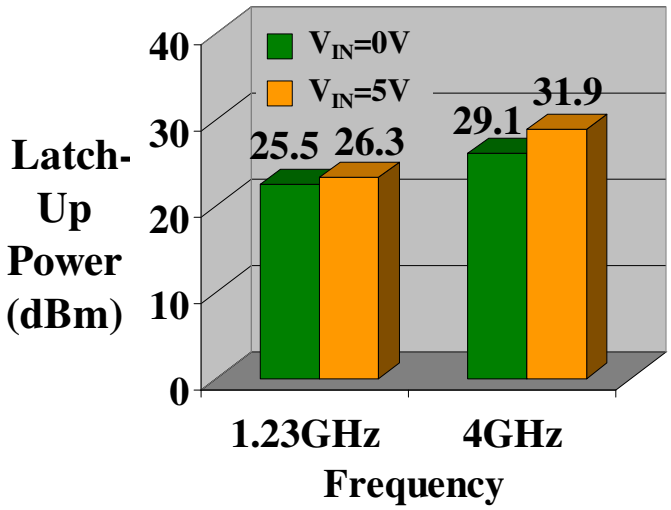



Figure 5. 17 The power of pulsed microwave interference that causes the latch-ups at the output ($V_O$) of the first inverter. The width and period of the pulsed microwave are 800ns and 10ms, respectively. The figure shows that inverters with input logic low ($V_{IN}$=0V) are more susceptible to the pulsed interference.

| Width | Period | Peak Power ( $P_{peak}^{pulse}$ ) | Average Power ( $P_{avg}^{pulse}$ ) |
|---|---|---|---|
| 800ms | 10ms | 200mW (23dBm) | 16mW |
| | | 355.7mW (25.5dBm) | 28.5mW |
| | | 427.6mW (26.3dBm) | 34.2mW |
| | | 814.8mW (29.1dBm) | 65.2mW |
| | | 1552.5mW (31.9dBm) | 124.2mW |

Table 5. 6 Peak power and average power of the pulsed microwave signal with the width of 800ns and the period of 10ms.

### 5. 3. 3 Latch-Up Mechanism and Modeling

Latch-up effects are due to the p-n-p-n parasitic bipolar transistor (Figure 5. 18) action in the CMOS devices [46] [55] through the voltage drops at the parasitic resistances (R1 or R2) by p-substrate and n-well currents. When the body or well currents are large enough to have a voltage drop of 0.7V at either parasitic resistance R1 or R2, they turn on either parasitic transistor Q1 or Q2. For example, when p-substrate current is large enough to have voltage drop of 0.7V at R1, it turns on Q1. Once Q1 turns on, it provides a large current to parasitic resistance R2 and thus, causes another voltage drop of 0.7V, turning on transistor Q2 as well. This results in more p-substrate current and thus, drives Q1 harder and provides more n-well current to R2, and Q2 is driven harder too. This mechanism eventually results in significant current flow from $V_{DD}$ to ground through the parasitic bipolar transistor loop, and that causes the devices to have latch-up, where all conduction goes via the parasitic bipolar transistors rather than the MOSFET channels. This excess current can damage the devices permanently if the current from $V_{DD}$ is not regulated properly to limit the current from the power supply. The latch-up effects observed in our work clearly show that pulsed EMI triggers the parasitic bipolar transistor action in the inverters under repeated pulse conditions, indicating that the EMI induces excess mobile charges in the devices that provide the p-substrate and n-well currents triggering the parasitic bipolar transistor action (excess majority holes in the p-substrate and electrons in the n-well). This is another important high power EMI induced charge effects along with the excess charge effects discussed in section 5. 2. 3, that resulted in the increase in the channel currents due to excess minority carriers (electrons in n

MOSFETs). Thus, high power EM interference induces excess electrons and holes in CMOS devices, contributing to both channel and body (p-substrate and n-well) currents. We modeled the pulsed interference induced excess carriers as electron and hole pairs in CMOS inverters (Figure 5. 19). Most of the excess minority carriers (electrons in p-substrate and holes in n-well) will be drawn to the channels by the strong field of the interference at the input (MOSFET gate) and contribute to the channel currents. Some of the carriers will be drawn to the p-substrate and n-well junction by the relatively weaker junction field (E). Due to the reverse bias between n-well ($V_{DD}$) and p-substrate (GND), no diffusion of the majority carriers (holes in p-substrate and electrons in n-well) happens at the p-substrate and n-well junction. Thus, excess majority carriers will flow to p-substrate and n-well contacts (excess holes to p-substrate and excess electrons to n-well). These body currents are given as follows:

$$i_h^{excess} = qA_h p_N^{'} \gamma_h \tag{5. 24}$$

$$i_e^{excess} = qA_e n_P^{'} \gamma_e \tag{5. 25}$$

where $i_h^{excess}$ is the current due to excess holes at the P-substrate, $i_e^{excess}$ is the current due to excess electrons at the N-well, $q$ is the electron charge ($1.6\times10^{-19}$ C), $A_h$ and $A_e$ are the area cross-sections where $i_h^{excess}$ and $i_e^{excess}$ flow, respectively, $p_N^{'}$ and $n_P^{'}$ are the excess holes and excess electrons, respectively, $\gamma_h$ and $\gamma_e$ are coefficients related to the current transport process. The currents can turn on either transistor Q1 or Q2 by the voltage drop at the parasitic resistances R1 and R2. Once one of the parasitic bipolar transistors turns ON, it provides a large current to the other transistor, causing that transistor to be turned on as well by another voltage drop. This mechanism will result in significant current flow from $V_{DD}$ to ground through the

parasitic bipolar transistor loop, and that causes the devices to have latch-up, where all conduction goes via the parasitic bipolar transistors rather than the MOSFET channels. This excess current can damage the devices permanently if the current from $V_{DD}$ is not regulated properly to limit the current.

Latch-up in CMOS devices can be caused by other effects also. For example, latch-up due to overshoot and undershoot voltage spikes at inputs and outputs, avalanche break-down at the N-well junction, punch through between N-well and n+ contact, punch through between P-substrate and p+ contact, have been reported [46]. However, latch-up due to electromagnetic interference is reported here for the first time.

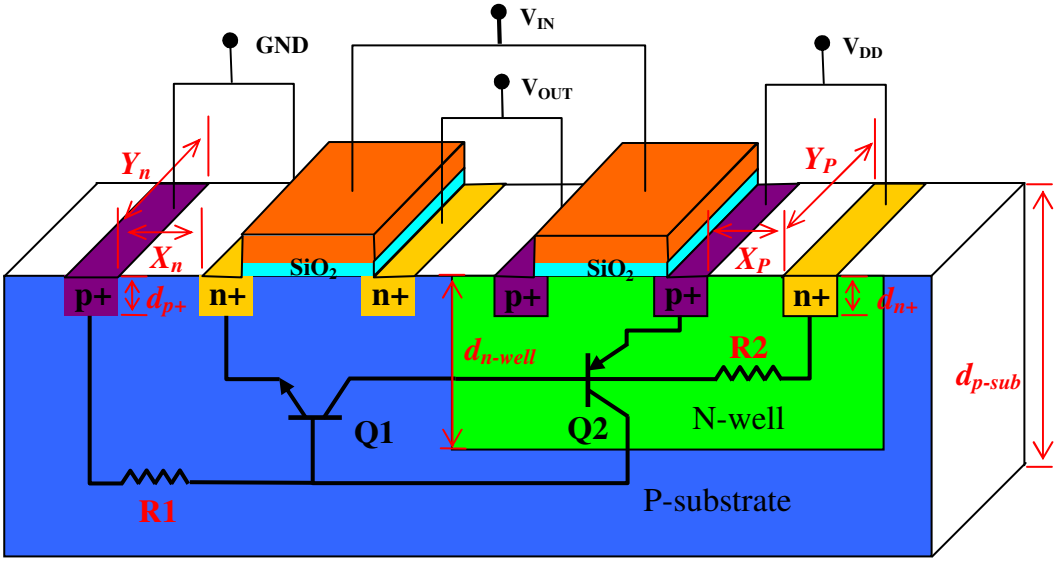



Figure 5. 18 Schematic of CMOS inverter showing the p-n-p-n parasitic bipolar transistor responsible for latch-up under MWI.

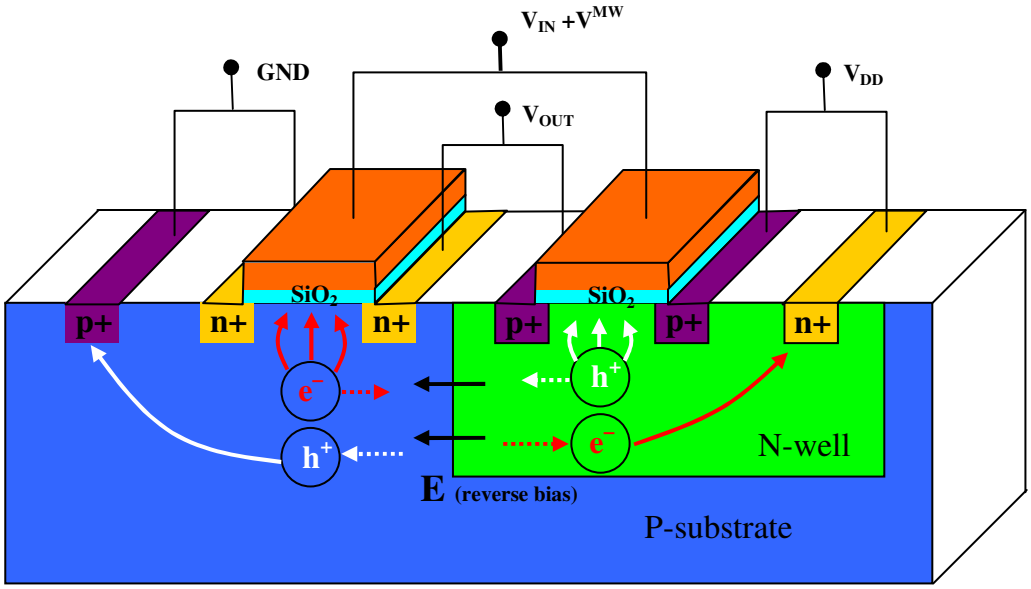



Figure 5. 19 Schematic of CMOS inverters showing excess electron-hole pairs. This is a non-equilibrium high level injection case. Minority excess carriers (electrons in P-substrate and holes in N-well) are drawn to the channels due to high field at the inputs and to the P-substrate and N-well junction (indicated with dotted arrows) due to the junction field (E). Due to reverse bias, no diffusion of majority carriers exists between P-substrate and N-well junction. Thus, majority excess carriers diffuse to P-substrate contact (GND) and N-well contact ($V_{DD}$).

Figure 5. 20 shows the layout and the photograph of the two cascaded CMOS inverters. The substrate and well parasitic resistances R1 and R2 can be calculated using Equation 5. 26 and 5. 27.

$$R_1 = \frac{\rho_{p-sub} X_n}{d_{p-sub} Y_n} = R_{\square(p\text{-}sub)} \frac{X_n}{Y_n} \tag{5. 26}$$

$$R_2 = \frac{\rho_{n-well} X_p}{d_{n-well} Y_p} = R_{\square(n\text{-}well)} \frac{X_p}{Y_p} \tag{5. 27}$$

where, $\rho_{p\text{-}sub}$ and $\rho_{n\text{-}well}$ are the resistivity of P-substrate and N-well, respectively, $d_{p\text{-}sub}$ and $d_{n\text{-}well}$ are the depth of P-substrate and N-well, respectively, $R_{\square(p\text{-}sub)}$ and $R_{\square(n\text{-}well)}$ are the sheet resistance of P-substrate and N-well, respectively, and $X$ and $Y$ are the length and width of parasitic resistance, respectively. The subscript n and p represent n and p MOSFETs, respectively. The sheet resistance of p-substrate and n-well for our devices are 2291.9 Ω/□ and 1582Ω/□, respectively. The design shows that $X_n$=12µm, $Y_n$=6.4µm, $X_p$=11.2µm, and $Y_p$=6.4µm. Thus, R1 and R2 are 4.3KΩ and 2.8KΩ, respectively. These values show that $i_h^{excess}$ is 0.163mA at 1.23GHz, 25.5dBm microwave interference that turns on the parasitic bipolar transistor Q1 through 0.7V voltage drop at the resistance R1. This in turn triggers the latch-up.

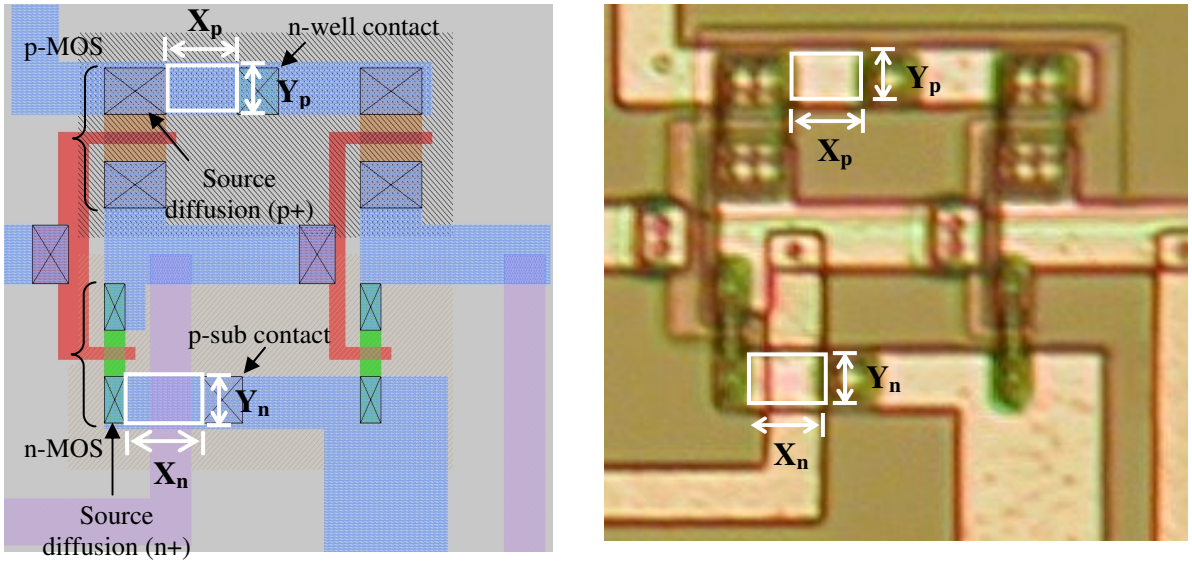



Figure 5. 20 (a) Layout of the two cascaded CMOS inverters showing the length and width of the parasitic resistances R1 and R2. (b) Photograph of the fabricated actual cascaded inverters. The resistances R1 and R2 are 4.8KΩ and 2.8KΩ, respectively.

Latch-up effects due to pulsed microwave interference can be mitigated by reducing substrate and well resistances by using highly doped substrate and well. By regulating and limiting the current from $V_{DD}$, the "burn-out" due to latch-up can be avoided. Trench isolation [46],[56-57] can also reduce latch-up effects when it is used in some CMOS technologies, but full isolation is difficult to achieve except for silicon-on-insulator (SOI) technology.

## *5. 4. Summary*

The effects of pulsed microwave interference on 1.5μm and 0.5μm CMOS inverters showed severe degradation in the voltage and current transfer characteristics. The voltage transfer characteristics showed bit-flip errors from 5V to 0V when pulsed MWI occurred at or below the threshold voltage of n MOSFETs of the inverters. For above threshold voltage, errors are observed to propagate to next stage as noise or bit-errors that may eventually cause bit-flip errors to subsequent stages. Bit-flip error rate is observed to increase with higher peak power and smaller devices. The current characteristics also showed that 2–3 orders of magnitude increase under pulsed interference resulting in 4 orders of magnitude increase in the power dissipation at the device contacts. Measured current characteristics and calculated effective channel mobility suggested that the increase in the output current of the inverters were predominantly due to excess charge effects. The excess charge effects were observed to be more pronounced at the 0.5μm inverters due to less sensitive channel mobility to temperature. Most significant increases in the stress on the device contacts and metal interconnect under the interference were found to be n+ active and p+ active

contacts and the stress are to be severer for the smaller inverters (0.5μm inverters) due to higher contact resistance values. Thus, those areas are the most vulnerable areas to the interference. Proposed inverters with interdigitated finger gates showed maximum of 91.5 % decrease in the power dissipation at the device contacts by increasing current flow paths and contact points, suggesting that the design can significantly reduce vulnerability by reducing stress on the contacts.

Latch-up events in CMOS inverters due to interference are observed and studied. Excess majority carriers from EHP generate the currents to P-substrate and N-well and these currents eventually turn on the p-n-p-n parasitic bipolar transistors by the voltage drop at the parasitic resistances R1 and R2 and trigger the latch-ups. Highly doped substrates and wells that decrease parasitic resistance values are suggested to prevent latch-up effects.

# Chapter 6: Device Excess Charge Based Theory for MWI

## *6. 1 Introduction*

In this chapter, the theory of the effects of high power microwave interference on n channel enhancement mode MOSFETs is proposed based on the fundamental understanding of device operation and the observed experimental results. The conventional approach in dealing with microwave interference effects on current-voltage characteristics in devices such as diodes and BJTs has focused on the nonlinear characteristics of the devices resulting from p-n junctions. However, for MOSFETs the nonlinearity is not just because of the p-n junctions but rather because of the nonlinear nature of device operation related to the bias conditions at each port (gate, drain, source, and body), which controls the transport of charges i.e. currents. Depending on the bias conditions, such nonlinear nature gives three unique operational modes such as the cut-off, the triode (linear), and the saturation regions. Our experimental observations indicate that under interference excess charge effects rather than thermal effects are predominantly responsible for the upsets and errors. We concluded in Chapter 2 and Chapter 5, that the increase in the current of MOSFETs and latch-up effects in CMOS inverters under microwave interference are due to excess charges in the devices, and in this Chapter we develop the theoretical framework for these effects.

## *6. 2 Excess Charge Model*

### 6. 2. 1 Excess charges

If excess charges are the cause, the theoretical treatment is based on the non-linear continuity equation under steady-state. The continuity equation is given by:

$$\frac{dn}{dt} = \frac{dp}{dt} = G - R \tag{6. 1}$$

where G is the generation rate and R is the recombination rate. $R=npr$.

$$\frac{dn}{dt} = \frac{dp}{dt} = G - npr \tag{6. 2}$$

In thermal equilibrium, $n=n_o$, $p=p_o$, and $dn/dt=dp/dt=0$. Thus, $G_o=n_o p_o r$. When there is EHP generation due to microwave interference, additional generation term g(t) needs to be added.

$$G = G_o + g(t) \tag{6. 3}$$

so Equation 6. 1 becomes as follows:

$$\frac{dn}{dt} = \frac{dp}{dt} = G_o + g(t) - npr \tag{6. 4}$$

$$\frac{dn}{dt} = \frac{dp}{dt} = g(t) - (np - n_o p_o)r \tag{6. 5}$$

Let us define excess holes and electrons as follows:

$$n' = n - n_o \tag{6. 6a}$$

$$p' = p - p_o \tag{6. 6b}$$

Thus,

$$n = n_o + n' \tag{6. 7a}$$

$$p = p_o + p' \tag{6. 7b}$$

Since excess carriers are created by EHP generation, excess holes and electrons exist in pairs. Thus,

$$n' = p' \tag{6. 8}$$

Since in thermal equilibrium $dn_o/dt = dp_o/dt = 0$,

$$\frac{dn}{dt} = \frac{dn'}{dt} \text{ and } \frac{dn}{dt} = \frac{dp'}{dt} \tag{6. 9}$$

Using this relation Equation 6. 5 is given as

$$\frac{dn'}{dt} = g(t) - [(n_o + n')(p_o + n') - n_o p_o]r \tag{6. 10}$$

$$\frac{dn'}{dt} = g(t) - n'(p_o + n_o + n')r \tag{6. 11}$$

$$\frac{dn'}{dt} = g(t) - \frac{n'}{\tau_{\min}} - \frac{(n')^2}{(p_o + n_o)\tau_{\min}} \tag{6. 12}$$

where, $\tau_{\min} = \dfrac{1}{(p_o + n_o)r}$. For slowly varying microwave interference, $g(t) \approx G^{MW}$ (G = generation of carriers at the steady state due to microwave signal). The time derivative of the excess population is zero in the steady state and the excess population at steady state $n_{ss}^{'}$ is:

$$\frac{(n_{ss}^{'})^2}{(p_o + n_o)\tau_{\min}} + \frac{n_{ss}^{'}}{\tau_{\min}} - G^{MW} = 0 \tag{6. 13}$$

Quadratic solve and get:

$$n_{ss}^{'} = \frac{(p_o + n_o)}{2}\left[\sqrt{1 + \frac{4G^{MW}\tau_{\min}}{(p_o + n_o)}} - 1\right] \tag{6. 14}$$

If $G^{MW}\tau_{\min} >> (p_o + n_o)$, then

$$\sqrt{1 + \frac{4G^{MW}\tau_{\min}}{(p_o + n_o)}} - 1 \approx \sqrt{\frac{4G^{MW}\tau_{\min}}{(p_o + n_o)}} \tag{6. 15}$$

Thus,

$$n_{ss}^{'} \approx \sqrt{G^{MW}\tau_{\min}(p_o + n_o)} \tag{6. 16}$$

Similarly, excess hole will be

$$p_{ss}^{'} \approx \sqrt{G^{MW}\tau_{\min}(p_o + n_o)} \tag{6. 17}$$

The excess carriers given in Equations 6. 16 and 6. 17 contribute to the increase in drain current. The excess electrons ($n_{ss}^{'}$) are drawn to the channel due to the high field at the input. On the other hand, the excess holes ($p_{ss}^{'}$) flow to the body.

## 6. 2. 2 Excess charges at the channel of MOSFETs

The electrons ($Q_{adj}$) from the adjacent highly doped source and drain regions and the excess electrons ($\delta n_{ss}^{'}$) drawn to the channel can be modeled as an equivalent voltage source at the gate using Equation 6. 18.

$$Q^{MW} = \delta n_{ss}^{'} + Q_{adj} = C_{OX}\Delta V^{MW} \tag{6. 18}$$

Thus, the increase in the drain current due to the equivalent voltage can be expressed as follows:

$$\Delta I_{DS}^{MW} = g_m \Delta V^{MW} \tag{6. 19}$$

The corresponding circuit model is given in Figure 6. 1.

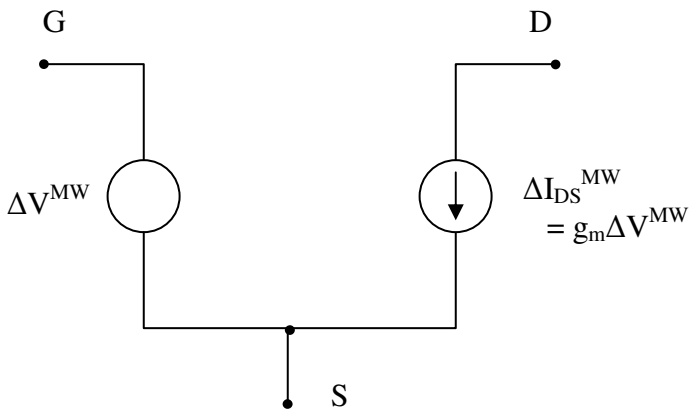



Figure 6. 1 Schematic of a circuit model for the current increase in MOSFETs due to microwave interference. Excess charges are modeled as equivalent voltage and expressed in a small signal model.

The relation between microwave interference and the equivalent voltage representing excess charges can be obtained using Taylor series expansion as given in Equation 6. 20 - 6. 23. Let us define the effective microwave signal at the gate as a sinusoidal signal $V_m sin(\omega t)$.

Taylor series expansion is given as follows:

$$f(a+b) = f(a) + \frac{f'(a)}{1!}b + \frac{f''(a)}{2!}b^2 + \cdots\cdots \tag{6. 20}$$

The current increase due to equivalent voltage can be given as

$$\overline{I_{DS}(V_{GSO}+V_m\sin(\omega t))} = I_{DS}(V_{GSO}) + \frac{\partial I_{DS}(V_{GSO})}{\partial V_{GS}}\overline{V_m\sin(\omega t)} + \frac{1}{2!}\left(\frac{\partial^2 I_{DS}(V_{GSO})}{\partial {V_{GS}}^2}\right)\overline{{V_m}^2\sin^2(\omega t)} + \cdots\cdots \quad (6.\ 21)$$

$$\overline{I_{DS}(V_{GSO}+V_m\sin(\omega t))} = I_{DS}(V_{GSO}) + \frac{{V_m}^2}{4}\frac{\partial g_m(V_{GSO})}{\partial V_{GS}} = I_{DS}(V_{GSO}) + \Delta I_{DS}^{MW} \quad (6.\ 22)$$

$$\Delta V^{MW} = \frac{{V_m}^2}{4}\frac{\partial g_m(V_{GSO})}{\partial V_{GS}}\frac{1}{g_m} \quad (6.\ 23)$$

Where $V_m = \sqrt{2R_o P^{MW}}$ , the $V_m$ is the peak voltage of the effective microwave interference signal. Under 50Ω matching termination, $R_o$ is 50 and $P^{MW}$ is the effective power of microwave interference in watts (W).

Thus, the excess charge for the source is given in Equation 6. 24.

$$Q^{MW} = C_{OX}\frac{{V_m}^2}{4}\frac{\partial g_m(V_{GSO})}{\partial V_{GS}}\frac{1}{g_m} \quad (6.\ 24)$$

The equation shows that excess charge is proportional to the square of the peak voltage and inversely proportional to transconductance ($g_m$). This model has limitation because in Triode region $\frac{\partial g_m(V_{GSO})}{\partial V_{GS}}$ is zero and furthermore $\frac{1}{g_m}$

cannot be defined at $V_{GSO}$=0V. Therefore, we cannot directly use this model but we have an idea how excess charges are related to the power and device parameters. We modified Equation 6. 24 and propose Equation 6. 25. and 6. 27.

$$Q^{MW} = C_{OX} V_{eq}^2 \frac{1}{V_{GS}^{eq}} \tag{6. 25}$$

where $V_{eq}$ is the equivalent voltage of microwave interference contributing to the excess charges, $V_{GS}^{eq}$ is the equivalent gate voltage contributing to the excess charges.

$$\Delta V^{MW} = \frac{Q^{MW}}{C_{OX}} \tag{6. 26}$$

## 6. 2. 3 MOSFET Model

Based on the model, we derived current-voltage characteristics ($I_{DS}$-$V_{DS}$) for the off, the triode, and the saturation regions. At the off region, the drain current is given as the excess holes ( $p_{ss}^{'}$ ) flowing to the body. This current is given as follows:

$$I_{DS(off)}{}^{MW} = I_{p-sub}^{MW} = qAp_{ss}^{'}\gamma \tag{6. 27}$$

where, $q$ is the electron charge ($1.6\times10^{-19}$ C), $I_{p-sub}^{MW}$ is the current flowing to the body, $A$ is the cross-section areas where $I_{p-sub}^{MW}$ flows, $p_{ss}^{'}$ is the excess holes, γ is a coefficient related to the current transport process.

For the triode region, we consider both the body current and the current due to excess charges at the channel (Equation 6. 28). The effective mobility of MOSFETs can decrease due to the fact that high field attracts the carriers in the channel closer to the surface of the silicon, where surface imperfection impedes their movement from the source to the drain. We introduce α to account for this effect in the model.

$$I_{DS(Triode)}{}^{MW} = \frac{C_{ox}\mu_n}{2}\left(\frac{W}{L}\right) \times \left[2(V_{GSO} - V_{TH} + \Delta V^{MW})V_{DS} - V_{DS}^{\alpha}\right] + I_{p-sub}^{MW} \quad (6.\ 28)$$

For the saturation region, the device cannot fully pinch off the channel due to excess charges at the channel, resulting in increased channel length modulation factor (Equation 6. 29). The channel length modulation factor becomes a microwave power dependent function.

$$I_{DS(sat)}{}^{MW} = \frac{C_{ox}\mu_n}{2}\left(\frac{W}{L}\right)\left(V_{GS} - V_{TH} + \Delta V^{MW}\right)^{\alpha} \times \left(1 + \lambda^{MW} V_{DS}\right) + I_{p-sub}^{MW} \quad (6.\ 29)$$

Using the equations, $\Delta V^{MW}$–Power with respect to $V_{GSO}$ ranging from 0V to 5V is given in Figure 6. 2. showing inversely proportional characteristics to gate bias. α versus Power relation is shown in Figure 6. 3. α shows a decrease from 1.945 to 1.7 as the power increases from 5dBm to 30dBm. $I_{p\text{-}sub}{}^{MW}$–Power relation shows the

substrate current due to excess holes at the substrate (Figure 6. 4). Most significant increase is observed at the power level greater than 15dBm. $\lambda^{MW}$–Power with respect to $V_{GSO}$ is shown in Figure 6. 5. $\lambda^{MW}$ represents the increase in the channel length modulation factor due to no pinch off at the drain junction under microwave interference.

Figure 6. 6 shows $I_{DS}$-$V_{DS}$ based on the Shockley's model without accounting for microwave interference. The figure shows a little mismatch because of the simplicity of the model. $I_{DS}$-$V_{DS}$ based on the excess charge model for 1GHz, 15dBm CW microwave interference at the gate and for 1GHz, 30dBm interference are shown in Figure 6. 7 and 6. 8, respectively. The result shows a good match with measured results.

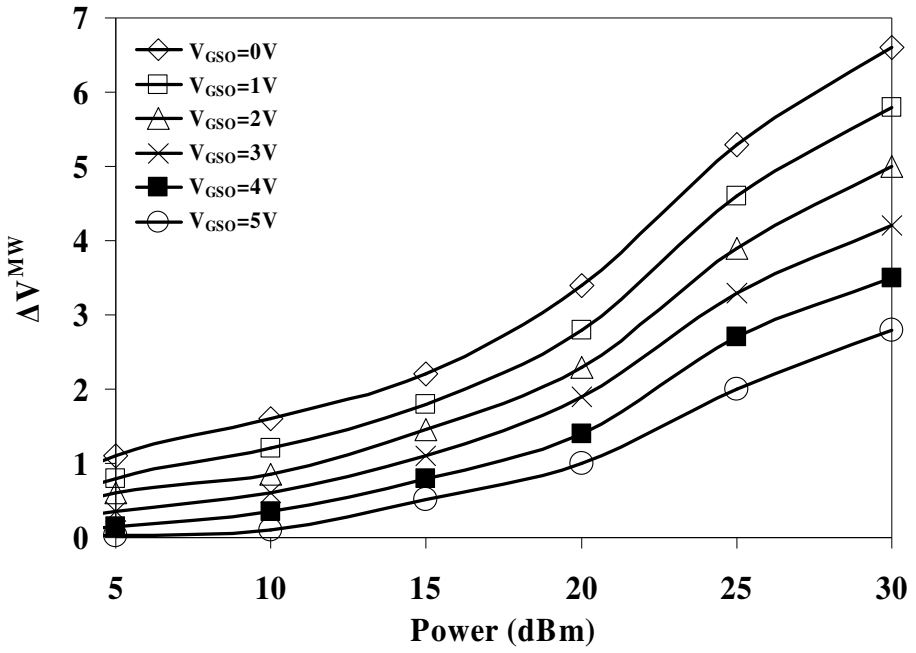


Figure 6. 2 $\Delta V^{MW}$ versus Power with respect to $V_{GSO}$ ranging from 0V to 5V with 1V step. $\Delta V^{MW}$ is the equivalent voltage representing the excess charges at the channel.

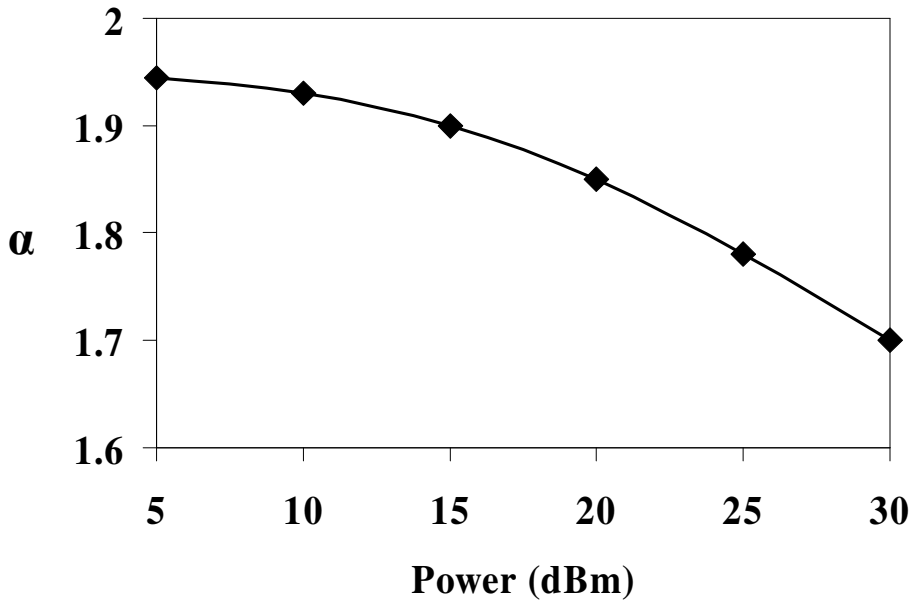



Figure 6. 3 α versus Power showing a decrease from 1.945 to 1.7 as the power increases from 5dBm to 30dBm. α accounts for the decrease in the effective mobility due to the high field at the gate.

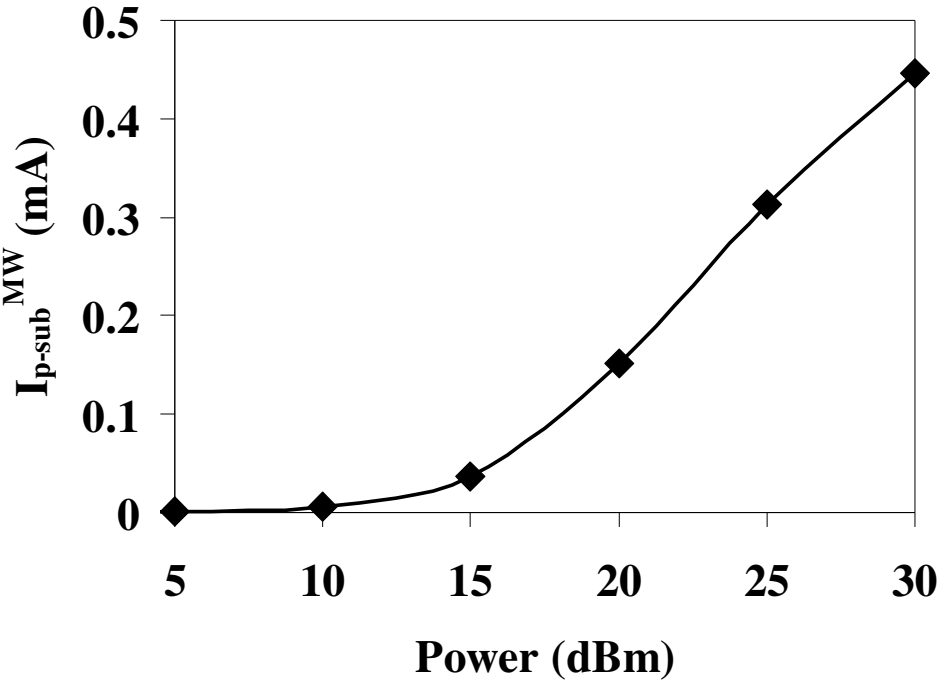


Figure 6. 4 $I_{p\text{-}sub}{}^{MW}$ versus Power showing the substrate current due to excess holes at the substrate.

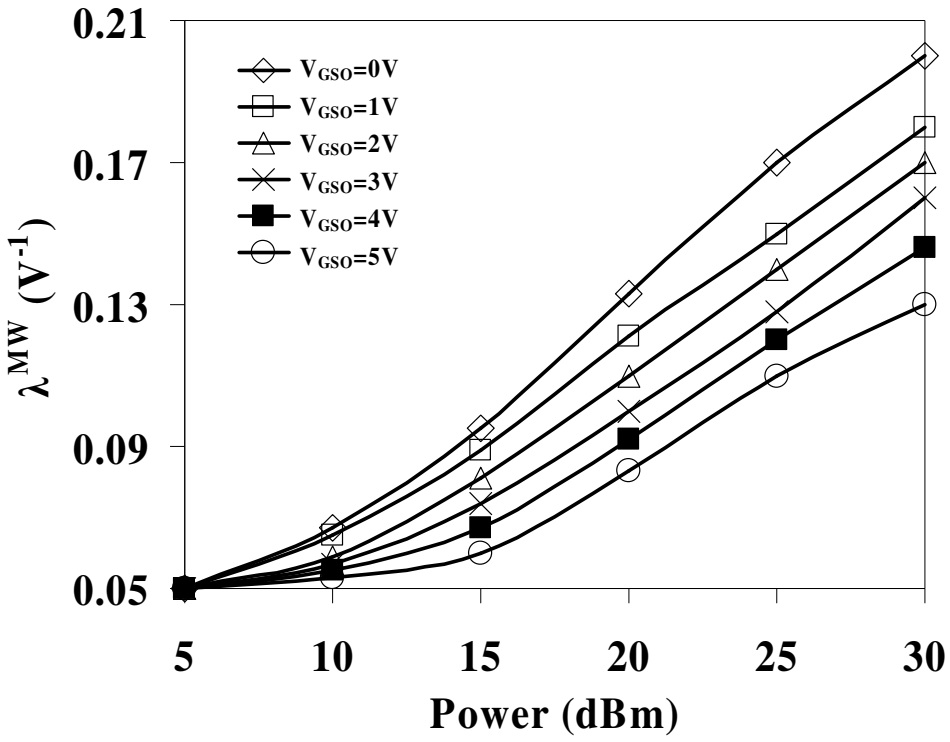



Figure 6. 5 $\lambda^{MW}$ versus Power with respect to $V_{GSO}$. $\lambda^{MW}$ represents the increase in the channel length modulation factor due to no pinch off at the drain junction under microwave interference.

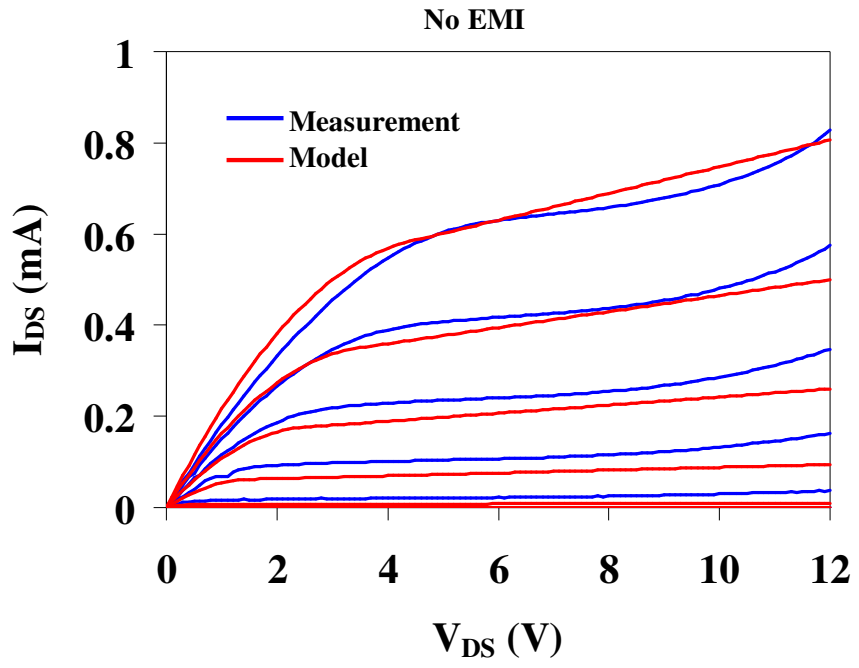



Figure 6. 6 $I_{DS}$-$V_{DS}$ based on the Shockley's model without microwave interference, showing little mismatch because of the simplicity of the model.

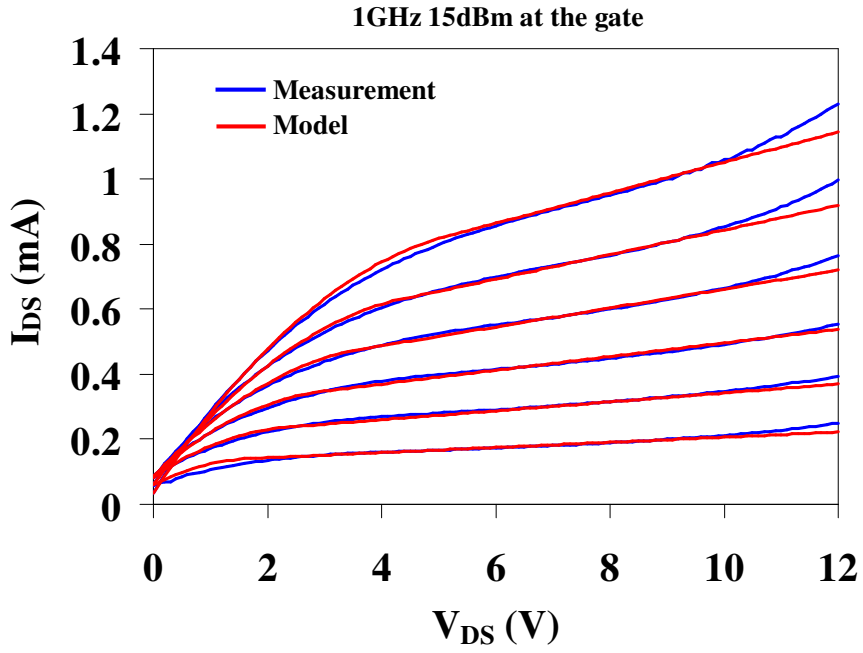



Figure 6. 7 $I_{DS}$-$V_{DS}$ based on the excess charge model for 1GHz, 15dBm CW microwave interference at the gate. The result shows a good match with measured results.

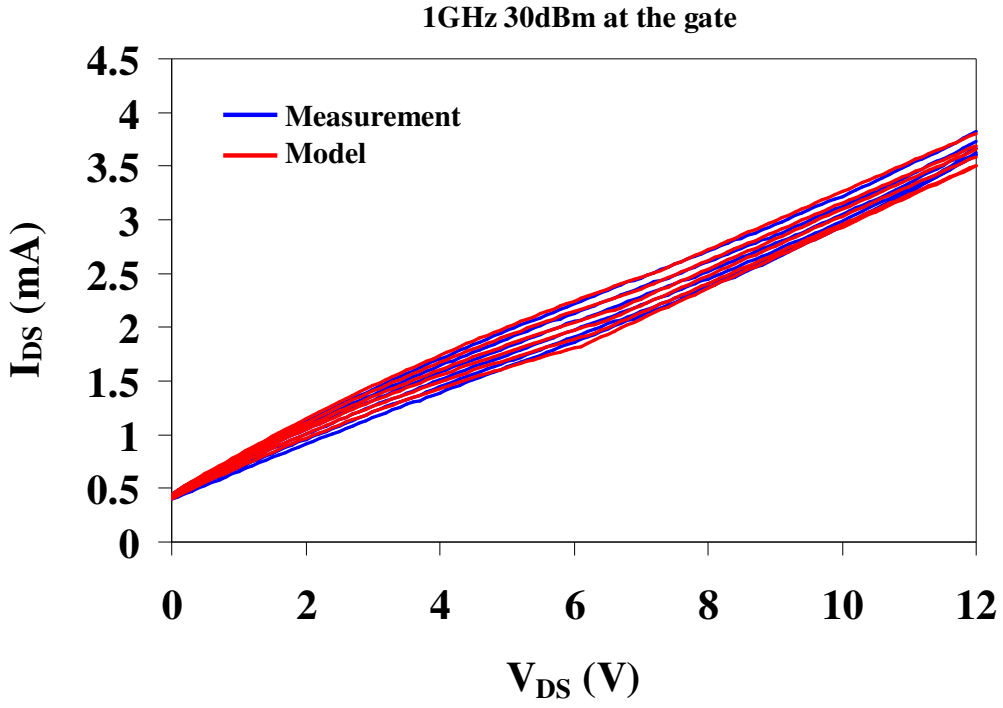



Figure 6. 8 $I_{DS}$-$V_{DS}$ using the excess charge model for 1GHz, 30dBm CW microwave interference at the gate.

## *6. 3 Summary*

An excess charge theory for the operation of n-channel MOSFETs under microwave interference is proposed. The model based on the theory provided an accurate prediction of $I_{DS}$-$V_{DS}$ characteristics of MOSFETs at the cut-off, triode, and saturation regions. In the model, the excess electrons are modeled as the charges in the channel, while the excess holes are modeled in the substrate current. The excess charges in the channel are expressed as the equivalent voltage at the gate. At the cut-off region, the drain current is modeled as the substrate current due to the excess holes flowing to the body. We modeled the degradation of the channel mobility due to the high field at the gate as the α value, which decreases with microwave power. We introduced the microwave power dependent channel length modulation factor to account for no

pinch-off at the channel due to the excess charges. Based on the theoretical model, $I_{DS}$-$V_{DS}$ characteristics with no microwave interference, 1GHz 15dBm, and 1GHz 30dBm microwave interference are obtained. The results show excellent match with measured results indicating the effectiveness of the excess charge theory.

# Chapter 7: Conclusions

Our study has focused on investigating the upset mechanisms of MOSFETs, CMOS inverters, and digital timer circuits under high power microwave interference by identifying the most vulnerable static and dynamic parameters of operation related to device upsets. We proposed a theoretical model based on experimental results to explain the operation of devices under the interference. We also developed a parameter extraction method from static load-line characteristics allowing the prediction of the dynamic operation of CMOS inverters under microwave interference.

We identified critical upsets in n-channel MOSFET devices for power levels above 10dBm in the frequency range between 1 and 20 GHz, which resulted in loss of switch-off capability, loss of saturation in the amplification region, development of DC offset currents at zero drain bias, and substantial reduction in breakdown voltages. In smaller devices, the drain area was observed to be more vulnerable to catastrophic physical failures. Such effects were suppressed at frequencies above 4GHz due to capacitive coupling through intrinsic device capacitance to ground.

The static operation of CMOS inverters under interference showed significant reduction in the gain, the noise margins, increase in the static power dissipation, changes of the input/output voltage ranges, and loss of the regenerative signal properties of digital inverters. Such upsets were mainly attributed to the shift of the quiescent (Q) point of operation of the devices. This shift resulted in changes of the inflection voltage ($V_{IN}^{If}$), and output voltages ($V_{OH}$, and $V_{OL}$). Furthermore, static noise margins were compressed significantly, resulting in severe degradation of noise

immunity and thus, loss of the regenerative signal properties, introducing bit errors in cascade inverter clusters. Substantial increase in the output currents caused several orders of magnitude of increase in the static power dissipation, which in turn upsets the power budget distribution and leads to catastrophic failures at the device contacts and interconnects.

For the dynamic operation of CMOS inverters, we developed a parameter extraction method that can predict the dynamic operation under microwave interference from experimentally measured static load-line characteristics. The method allowed the evaluation of the dynamic operation of the inverters and revealed severely compressed output voltage swings and decrease in the charging and discharging currents due to the substantial changes in the quiescent (Q) point of operation. This also resulted in changes in propagation delays and bit errors in cascaded inverters. Due to the substantial increase in the short-circuit currents the dynamic power dissipation showed 95 to 184 % of increase, which again resulted in the stress at the metal contacts and interconnects. As the bias voltage and device size were scaled down, the effects of microwave interference were observed to be more severe. We predicted logic errors in the timer circuits due to microwave interference using SPICE and the model obtained from the parameter extraction method. Comparison between simulation results and measured results showed good agreement.

The effects of pulsed microwave interference on 1.5μm and 0.5μm CMOS inverters showed new bit-flip errors at or below the threshold voltage of the devices and other errors propagating as noise or bit-flip errors in the subsequent stages. Bit-flip error rate was observed to increase with higher peak power and smaller devices.

Measured current characteristics and calculated effective channel mobility suggested that the increase in the output current of the inverters is predominantly due to excess charge effects, which were observed to be more pronounced at the smaller devices due to a less sensitive channel mobility to temperature. Interdigitated finger gate structures are proposed for EMI hardened inverters that shows maximum of 91.5 % decrease in the power dissipation at the device contacts. Latch-up effects in the CMOS inverters due to high power pulsed microwave interference supported the fact that microwave interference induced output current increase was due to excess charges under microwave interference. We concluded that the currents due to excess carriers flowing to P-substrate and N-well were the main source triggering latch-ups. Highly doped substrates and wells that decrease parasitic resistance values are suggested to prevent latch-up effects under the interference.

A theory based on excess charges predicting the operation of n-channel MOSFETs under high power microwave interference was proposed. The theoretical model included the excess electrons and holes created under the interference. The excess electrons contribute to the channel current, while excess holes to the substrate current. We introduced new terminology in the output current where the power dependence of $V_{DS}$ is given by parameter $\alpha$ and a channel length modulation factor $\lambda$ dependent on microwave power to model the degradation of the channel mobility due to high field at the gate and no pinch-off at the channel due to the excess charges, respectively. The $I_{DS}$-$V_{DS}$ characteristics based on the model showed a good match with the measured characteristics indicating that the excess charge theory is valid.

# Chapter 8: Future Work

The prediction of microwave interference induced upsets in digital IC's is a challenging problem. SPICE and harmonic balance simulation have been used to solve this problem but they could not provide an accurate prediction for high power and frequency interference due to their limitation in simulation time and number of harmonics that can be used.

We demonstrated that the parameter extraction method could predict the dynamic operation of CMOS inverters under the interference from static load-line characteristics. The method was based on solving charge transport mechanism at the output capacitance. As we observed the charge transport mechanisms in integrated circuits (CMOS inverters) depend on the operation of each units (each MOSFETs), which can be obtained using the MOSFET model proposed in this dissertation. Thus, by combining the MOSFET model with the parameter extraction method, we can generalize the parameter extraction method to predict the operation of any digital logic units. As we demonstrated with the timer circuit, this generalized extraction method can be correlated with SPICE model to simulate the operation of integrated circuits containing digital units subjected to the interference.

Another area of investigation is the protection and shielding from microwave interference at the chip level. Conventional protection methods such as metallic enclosures fail to completely shield the chips inside. Thus, on-chip protection and shielding is an important area of research. The development of CMOS processes compatible on-chip coating material having shielding effectiveness will provide lightweight and cost effective shielding method. For input and output port of IC's, we

can adopt EMI sensing units that cut off entry port from inner core IC's when EMI is present.

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