ABSTRACT

Title of dissertation: INTEGRATION OF CMOS TECHNOLOGY INTO

LAB-ON-CHIP SYSTEMS APPLIED TO THE DEVELOPMENT OF A BIOELECTRONIC NOSE

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This work addresses the development of a lab-on-a-chip (LOC) system for olfactory sensing. The method of sensing employed is cell-based, utilizing living cells to sense stimuli that are otherwise not easily sensed using conventional transduction techniques. Cells have evolved over millions of years to be exquisitely sensitive to their environment, with certain types of cells producing electrical signals in response to stimuli. The core device that is introduced here is comprised of living olfactory sensory neurons (OSNs) on top of a complementary metal-oxide-semiconductor (CMOS) integrated circuit (IC). This hybrid bioelectronic approach to sensing leverages the sensitivity of OSNs with the electronic signal processing capability of modern ICs.

Intimately combining electronics with biology presents a number of unique challenges to integration that arise from the disparate requirements of the two separate domains. Fundamentally the obstacles arise from the facts that electronic devices are designed to work in dry environments while biology requires not only a wet environment, but also one that is precisely controlled and non-toxic. Design and modeling of such heterogeneously integrated systems is complicated by the lack of tools that can address the multiple domains and techniques required for integration, namely IC design, fluidics, packaging, and microfabrication, and cell culture. There also arises the issue of how to handle the vast amount of data that can be generated by such systems, and specifically how to efficiently identify signals of interest and communicate them off-chip.

The primary contributions of this work are the development of a new packaging scheme for integration of CMOS ICs into fluidic LOC systems, a methodology for cross-coupled multi-domain iterative modeling of heterogeneously integrated systems, demonstration of a proof-of-concept bioelectronic olfactory sensor, and a novel event-based technique to minimize the bandwidth required to communicate the information contained in bio-potential signals produced by dense arrays of electrically active cells.

INTEGRATION OF CMOS TECHNOLOGY INTO LAB-ON-CHIP SYSTEMS APPLIED TO THE DEVELOPMENT OF A BIOELECTRONIC NOSE

By

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Preface

The work described herein will address the development of an olfactory sensor. Amongst the five basic senses, olfaction and taste remain the least understood because unlike the three others, they are based upon chemoreception. The domains of sight, sound, and touch can be described as signals that are fundamentally conveyed by energy transfer. Vision is achieved by transducing optical energy from photons. Hearing relies on detecting perturbations caused by sound waves. Physical feeling is based on mechanical force. Artificial sensors that operate in these three domains rely on well understood mechanisms for transducing such signals; this is not the case for olfaction or taste. As such, the field of artificial olfaction lags far behind other types of electronic sensing.

Though numerous methods have been suggested for developing artificial olfactory sensors, this body of work takes the approach of creating a system comprised of both electronics and biology. The underlying intent being to leverage the chemoreceptive capabilities of natural systems and to combine them with state of the art modern electronic technology to create a hybrid bioelectronic sensor. The methods and technologies described herein represent multidisciplinary work that utilizes techniques from the fields of biology, electrical engineering, lab-on-a-chip technology, materials science, and micro-electromechanical systems.

I have already touched upon the reason for using a biological approach to olfactory sensing. Though additional justification will be provided later, it is important to mention that biological transduction of odor involves electrical signaling, which is why it is appropriate to combine biology with electronics.

Early on in my education as an electrical engineer, I found myself interested in microelectronics; in particular I found the field of mixed-signal integrated circuit design to be fascinating. This was coupled with a strong interest in neuromorphic systems, first, natural and artificial neural networks, and later on, biomimetic systems. I also found myself in the privileged position of being a member of two laboratories that collaborated to develop sensors and actuators that primarily relied on electronics and microelectromechanical systems. As a graduate student, the greatest boon is when one is given the opportunity to work on a project that one finds to be truly exciting. I was fortunate to be in such a position, and was able to work on a sensing platform that combines my two greatest interests.

Though combining biology with electronics held the promise of delivering new types of sensors, it turned out that building a physical system that brought the two together required a great deal of process and technology development. At its core this work describes the development of a system that falls within an emerging class of lab-on-a-chip devices, those that integrate CMOS electronics to create systems that

are freed from being confined to a physical laboratory because of the need to be tethered to benchtop equipment for readout. System integration and assembly was performed by applying materials and microfabrication techniques initially developed within the field of micro-electromechanical systems.

The integrated circuit prototypes employed in this work were fabricated through the MOSIS service. Microfabrication was performed at the Maryland Nanocenter Fablab. All of the rest of the work was conducted in the Araneda Lab (Department of Biology), the Integrated Biomorphic Information Systems lab (Department of Electrical and Computer Engineering), the Laboratory for Microtechnologies (Department of Mechanical Engineering), and the laboratory of the White Research Group (Department of Bioengineering).

This dissertation features material from a number of multi-authored publications and manuscripts. My personal contributions to each of these works are highlighted in the preface of each of the chapters that borrow from them.

Dedication

I dedicate this work to my family. To my mother Monica Das Gupta who raised me, to my father Mrinal Kanti Datta-Chaudhuri who taught me how to conduct myself and instilled in me a sense of curiosity about the arts and human nature, to my stepfather Peter Miovic who is a never-ending source of guidance and calming energy, and to my brother Mihir Datta-Chaudhuri who somehow managed to survive having someone like me as an elder brother.

Acknowledgements

The work presented here would not have been possible without the contributions of numerous individuals. First, I would like to thank Professors Pamela Abshire and Elisabeth Smela for their help and guidance over the course of my graduate education. Importantly I would also like to express my deep gratitude to Professor Ricardo Araneda, without whom much of the biological results in this work would not have been possible. I would also like to specifically thank Professor Robert Newcomb, who not only generously offered to serve on my committee but can also claim responsibility for being the first to introduce me to the field of neural circuits. Additionally, I thank all of the members of my committee in its entirety; every one of them has been extremely generous with their time and also with resources.

Many of my lab mates have helped me with not only experimental work but also by providing advice and guidance, they are: Jeff Burke, Mark Kujawski, Tsung-Hsueh Lee, Nicole McFarlane, Babak Nouri, Disha Pant, Somashekar Prakash, David Sander, Anshu Sarje, and Bathiya Senevirathna.

There are also a few special individuals that I met during my time at UMD who have become close and lifelong friends, these are the people who have helped me the most, and they are: Eduardo Arvelo, Marc Dandin, Sowmya Subramanian, and Filiz Yesilkoy. I couldn't have done it without you guys.

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Chapter. 1

Introduction

The work described herein serves as a foundation for the development of complementary metal—oxide—semiconductor (CMOS) based hybrid bioelectronic sensors. This class of sensors is best described as a subset of lab-on-a-chip (LOC) or micro total analysis systems (µTAS). The underlying motivation behind the development of LOC systems is to integrate the functionality of laboratory equipment into a miniature platform, enabling sampling, detection, and signal processing on a device that can be measured on the scale of centimeters. LOC systems have applications in a variety of different types of sensors, screening assays, implantable systems, and basic scientific research. Though there are a broad range of applications for LOC systems, the common aspects of all LOC devices are that they aim to provide the same functionality as large-scale laboratory equipment in a small form factor while using minimal quantities of samples and reagents.

An important goal of LOC systems that remains largely unrealized is the ability to perform laboratory functions outside of a laboratory environment. The key enabling technology for LOC has been microfluidics, which has led to significant developments in the field. However, many LOC systems remain primarily microfluidic devices, capable of intricate manipulation of minute sample quantities, yet requiring complex and often large bench-top equipment for sensing, detection, and readout. An emerging technology in the field of LOC is CMOS integrated circuits (ICs); the technology found at the heart of nearly all modern electronic

devices, CMOS ICs are capable of dramatically increasing the functionality of existing LOC systems. The operation of CMOS ICs is not limited to traditional electronic computation and signal processing. CMOS devices can themselves be used to directly sense many physical phenomena, thus freeing LOC systems from the confines of a laboratory setting and allowing truly portable self-contained systems.

In recent years there has been significant interest in developing cell-based LOC biosensor systems using living cells as the sensor front-end. Biological cells have evolved over millions of years to be able to sense trace quantities of particles. Man-made sensors cannot easily approach the sensitivity or scope of biological systems. Integrating cell-based sensing into LOC devices is another powerful method for increasing the sensing modalities available to LOC systems. Hybrid bioelectronic systems that combine traditional LOC systems with CMOS ICs and cell-based sensing are miniaturized systems capable of detection with the sensitivity of biological systems found in nature, while also exhibiting signal transduction and information processing capacity that parallels advanced laboratory equipment.

1.1 Technical Contributions

This work will describe the development of a hybrid bioelectronic LOC olfactory sensor. The core concept was to develop a system that leverages the unique properties of both biology and CMOS into a single integrated LOC system. The primary contributions of this work include the development of a generalized cell-based sensing platform that integrates CMOS IC technology into a traditional LOC framework, a methodology for cross-domain iterative modeling and design of heterogeneously integrated systems, the demonstration of the a hybrid

bioelectronic olfactory sensor that incorporates CMOS technology with living sensory neuron, and the introduction of a new paradigm for readout of bio-potential signals. The fundamental technical contributions of this work are highlighted in the bullets below:

• Packaging CMOS for fluidic interface

 A new packaging method for integration of CMOS ICs into fluidic LOC systems is introduced.

• System design and modeling for heterogeneous integration

 A methodology is described which covers the front-to-back design and integration process for systems that intimately combine CMOS ICs with biology.

• A hybrid bioelectronic olfactory sensor

 A proof-of-concept bioelectronic olfactory sensor that utilizes living olfactory sensory neurons as sensing elements is demonstrated.

• A novel readout paradigm for bio-potential signals

An event-based readout method is applied to bio-potential signals, this
new paradigm is highly scalable and will enable future systems to
interrogate large populations of cells while minimizing bandwidth
requirements.

The remainder of this chapter will provide background material to establish context for the contributions of this work. Chapter. 2 will introduce the packaging method for integrating CMOS ICs into fluidic LOC systems. Chapter. 3 will discuss the development of the cell-based sensing platform and introduce a decision making process and methods for approaching the

complex design and fabrication of such heterogeneously integrated systems. Chapter. 4 will describe the development of, and present the results from, a proof-of-concept hybrid bioelectronic olfactory sensor. Chapter. 5 will introduce the new paradigm for efficient readout of bio-potential signals. Finally, Chapter. 6 will conclude by clearly summarizing the original contributions presented in this work and discussing the future of the technology introduced here.

1.2 Integration of CMOS into LOC

One of the primary contributions of this work is the introduction of a new method for packaging commercial CMOS ICs so that they can be integrated with fluidics to form a robust platform for LOC system development. The motivation behind the development of this method was to be able to perform complicated sensing using ICs in direct contact with sensory cells and fluidics. Integration proved to be quite challenging because of the disparate requirements of electronics and biology. This section will briefly introduce some of the key concepts relevant to the development of a CMOS based fluidic LOC platform.

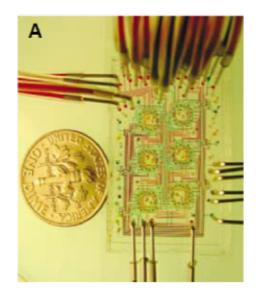
1.2.1 Lab on a Chip technology

LOC technology has blossomed since its inception. Some of the first LOC devices included a gas chromatography (GC) device fabricated in silicon (Si) [1], and a miniaturized total chemical analysis system [2]. These early devices incorporated the basic components required for micro total analysis systems (μ TAS), namely, sample collection and handling, sample treatment, signal transduction and readout. Today LOC systems are in everyday use for

research and medical tasks such as on-chip polymerase chain reaction (PCR) [3], antigen screening [4], trapping of circulating tumor cells [5], as well as point of care devices [6]. The ubiquitous nature of LOC devices becomes apparent when considering the glucose test strips used by millions of individuals every day, this technology started out with the development of glucose oxidase electrodes [7], and has now been adapted and developed so that it provides critical healthcare data and is easily operated by the end user.

1.2.1.a Microfluidics

Much of the recent advancements in LOC technology have come from the advent of microfluidic systems. Microfluidics uses technology that can manipulate small volumes of fluids (as low as 10⁻¹⁸ liters [8]), using devices that contain channels with dimensions much smaller than a millimeter. Microfluidic technology offers the ability to use extremely small quantities of reagents, while performing manipulation of the fluid to perform tasks such as separation and mixing, and allowing the development of devices that offer high resolution and sensitivity, while offering the promise of mass production and low cost [9, 10]. The realm of microfluidics has also evolved from using traditional materials such as silicon, glass, and polymers [8] to novel materials such as paper based devices [11, 12]. New methods and techniques for developing microfluidic devices continue to arise, and in a sense the technology still remains in its infancy [10] with a great number of future potential applications.



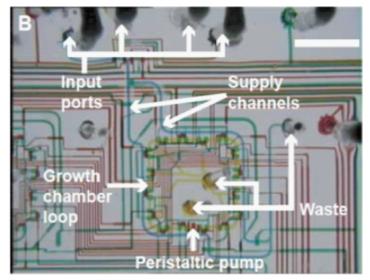


Fig. 1. Example of a modern microfluidics device. The device is a bioreactor for long-term culture and monitoring of small populations of bacteria. A) Shows the scale and macro structure of the device. B) Shows the complex multi-layered set of internal channels. Figure taken directly from [13].

The appeal and promise of microfluidics arise from the capability, cost, scalability and potential for adoption of microfluidic based systems. The analytical capabilities of microfluidic devices show great promise for applications in both industry and academia [10]. The simple materials, such as polydimethylsiloxane (PDMS), and processes used to create microfluidic structures, allow nearly anyone to create devices capable of complex analytical functions. At the same time, the low material cost and the ability to produce intricate structures using easily applied techniques such as soft lithography [8], mean that the mass production of cheap microfluidic devices will remain a possibility for the foreseeable future. An example of a modern microfluidic device designed for long term culture of bacteria is shown in Fig. 1.

Though microfluidic technology was not present in the earliest LOC devices, today the two terms have become nearly synonymous. An unfortunate side effect of the rapid proliferation of readily fabricated microfluidic structures is that most LOC devices are primarily microfluidic

chips, and the early established goal of total analysis capability on a miniaturized platform has not been realized for most modern LOC devices.

1.2.2 Motivation to Integrate CMOS into LOC

CMOS ICs provide the core computational and processing infrastructure for nearly all modern electronic devices. The term CMOS generally brings to mind images of microchips on computer motherboards that are performing billions of operations per second. However, CMOS chips are not simply relegated to the world of computation, CMOS technology can also be used to directly sense the physical world, a common example is the CMOS camera found in most mobile phones, and in this manner they can contribute significantly to the development of truly portable, autonomous, and compact LOC devices that can be used outside of the laboratory environment. Thus, for LOC systems, CMOS devices can be used to not only provide information readout and signal processing but can also be used to transduce signals of interest into the electronic domain.

The concept of fully functional LOC devices that do not require external equipment for readout is not recent; in fact one of the early LOC devices included silicon photodetectors in addition to on-chip heaters, temperature sensors, and microfluidics (Fig. 2). The device shown in Fig. 2 is a DNA analysis system capable of measuring and mixing reagents, amplifying and digesting DNA, and separating and detecting products from reactions, without the need for external lenses, or heaters or pumps [14].

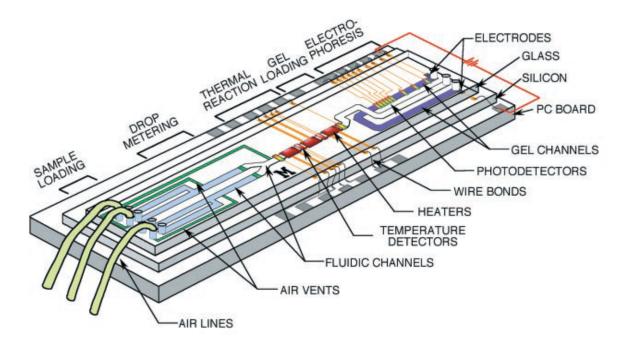


Fig. 2. An early example of an integrated LOC system that included photodetectors for readout, microfluidics for sample handling, as well as on-chip heaters for temperature control. Figure taken directly from [14].

Over the last decade there has been a trend towards monolithic integration of CMOS into LOC devices. These systems have used not only electrical sensing but also optical [15], electrochemical [16], capacitance [17], and magnetic [18]. In many cases these devices have been built using traditional CMOS packaging techniques developed by industry, which is a feasible option when there is no need for direct contact between the CMOS IC and fluidics. However, when integration involves fluidics, and in particular fluid that must come in contact with the CMOS surface, the issue of packaging becomes far more complex.

1.2.3 Technical Challenges for Physical Integration

Fundamentally, the obstacles to packaging CMOS for integration with fluidics arise from the simple fact that electronics are not designed to work in the presence of conductive fluids. The matter is further complicated when biological elements are used as part of the system, in that case not only must the electronics be protected from the fluids, but the biological entities must be provided an environment in which they can survive, meaning protection from electrical effects as well as exposure to only nontoxic materials. A lot of different packaging approaches have been demonstrated for integrating CMOS with fluidics, a review of the most prominent techniques will be provided in Chapter. 2.

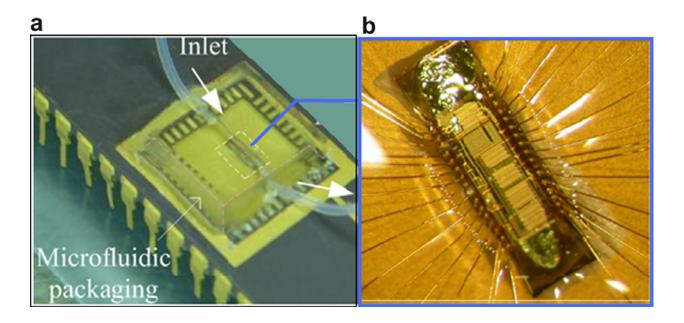


Fig. 3. An example of an industrial ceramic package that has been modified to allow basic fluidic integration. a) Shows a macro view of the chip in the package, the entire chip surface and wire bonds are insulated using a polymer and the fluidic path is formed by an intentionally formed vacancy over the IC itself. b) Shows an overhead view of the IC, in this case it can be seen that the IC was specifically designed to accommodate a longitudinal fluidic path since the bond pads are only on the lateral sides of the chip. Figure taken directly from [19].

The two basic approaches for integration are to either modify an existing industrial package, or to fabricate a new package based on the design requirements of a particular system. The first approach may be simpler, but may require modification of the CMOS chip to accommodate the fluidics. In particular the design of the CMOS IC may have to be altered so that the fluidic structures will not interfere with the electrical connections. In many cases this will result in wasted silicon real estate, which is a costly design choice. An example of a device

that integrates CMOS with fluidics in a traditional package is shown in Fig. 3 [19]. An impressive aspect of this device is that electronic interface can be done in a completely standard manner since a regular industrial package is used. This particular device was fabricated by casting a polymer over a soluble thread. The polymer serves to encapsulate the wire bonds that provide electrical connections between the chip and the package.

The second approach of fabricating a custom package requires more consideration about materials and assembly, but can allow more flexibility for the specifications and capabilities of the CMOS chip and the integrated system. An example of the second method is shown in Fig. 4 [20]. This device is an example of intimate integration of CMOS electronics with fluidics. The CMOS IC is a potentiostat designed to perform electrochemical measurements. Integration was achieved by embedding the IC into a carrier substrate, thus providing the necessary area for building microfluidic structures. Electrical connections to the chip are provided by means of patterned metal traces, and the microfluidic structure is formed by using glass and the photopatternable SU-8 polymer.

Though the particular method used to fabricate the device in Fig. 4 requires a tailor-made hole within the handle substrate and careful consideration for leveling the IC with the substrate surface, it does address one of the major challenges for integration of CMOS with fluidics, namely that there exists a size disparity between the real estate provided by the surface of the CMOS chip, and that required to build microfluidic structures. CMOS ICs used in research settings are generally millimeter scale, with the area primarily being limited by prohibitive fabrication costs. Microfluidic devices are typically centimeter scale, because although they take

advantage of fluid dynamics which occur at the micro-scale, the infrastructure required to assemble a device is generally much larger than the active portion of the device itself.

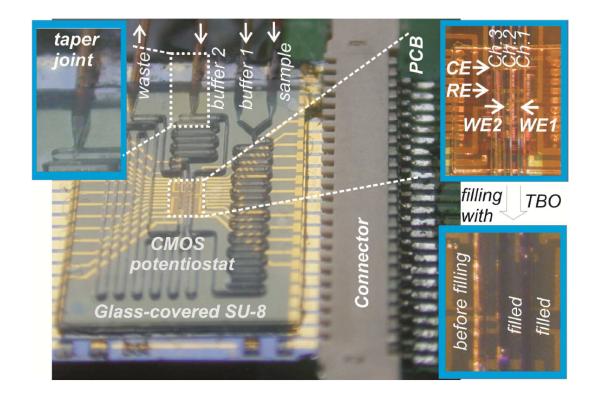


Fig. 4. An example of a CMOS IC monolithically integrated with fluidics to form an LOC electrochemical sensor. The IC has been embedded into a substrate, glass covered SU-8 polymer is used to form the microfluidic channels that run directly over the IC. This type of package can become significantly more complex than adapting an existing package; however it also allows greater flexibility for system integration. The inset figures show taper joints for fluidic connections (top left), the electrochemical cell and the microfluidic channels (top right), and the channels before and after filling with fluid. Figure taken directly from [20].

This section introduced some of the key technical challenges that arise when integrating CMOS with fluidics and biology. For the electronics, proper operation requires passivation from the fluid to prevent undesired conduction. Biology on CMOS requires careful selection of materials and the ability to maintain an environment conducive to life. Integrating fluidics requires larger area than that which is typically available on the surface of a CMOS chip. Ideally, a packaging method that addresses all of these requirements should be cheap and easily reproducible while accommodating any naturally occurring differences in chip size.

1.2.4 Modeling and System Design

Beyond the technical challenges of physical implementation, there also arise challenges in the design and modeling of systems that integrate CMOS ICs with fluidics and biology. These challenges once again stem from the heterogeneous integration of multiple domains into a single system. From the perspective of IC design, the main challenges are: continuous operation at temperatures higher than room temperature, the possibility for signal coupling through fluids, considerations of heat generation due to power consumption, and the necessity to rethink floor planning and area resources when taking into account the integration of additional components. Similarly packaging must take into account the materials and processes used, and whether they will satisfy requirements while not damaging sensitive electronic circuits during processing or possibly leaving behind toxic residue that will affect cell culture on the surface of the chip. Biology on the chip has to, amongst other things, account for new conditions and surfaces on which cell culture is to be performed.

Thus the three domains become inseparably interrelated, and system design must account for how each domain will affect the others. Unfortunately, no single CAD tool exists that can perform the necessary cross-domain simulations that are required. In light of this, Chapter. 3 introduces an iterative cross-coupled multi-domain simulation methodology, and provides a rubric for designing heterogeneously integrated systems, another primary contribution of this work.

1.3 Olfaction

Olfaction is a fundamental sense that has many functions in the natural world. Animals use it to communicate and sense the world around them. In humans the sense of olfaction is strongly tied to memory, emotion, and taste. Artificial or machine olfaction has yet to be realized in a form that can parallel the natural capabilities of biology. Although significant work has been done in this area there are only a few commercial electronic noses, and all of them have a limited library of odorants that can be sensed. Because of this, the long standing gold standard for olfactory sensing remains highly trained dogs.

Detection of odorants has many different applications, including explosives and illegal drug detection, search and rescue, medical diagnosis, industrial quality control, commercial product authentication, food spoilage monitoring, detection of toxins, and pollution monitoring. Development of a true electronic nose is an ongoing challenge and has the potential for disruptive change in medicine, biometrics, and homeland security.

1.3.1 What is an Odor?

The definition of a "simple odor" is a small polar molecule that when airborne can enter the nasal cavity and be sensed by the biological olfactory system [21]. Chemically, there are many different functional groups that make up odorous compounds. Interestingly, studies on the relationship between the chemical structure of an odor and the elicited sensory activity that it stimulates find that is essentially impossible to predict what an odor will smell like based on its chemical composition. Also, compounds from different functional groups can have similar smells [22]. For humans, like other animals, the detection threshold, the point at which an odor

is just barely detectable, of various simple odorant molecules can vary significantly. It has been shown that the detection threshold for ether is 1780 ppm (parts per million), and that the detection threshold for musk xylene is as low as 573 ppt (parts per trillion), a variation of 7 orders of magnitude [23].

A "complex odor" is defined as the combination of two or more different volatile compounds that can elicit a response from the biological olfactory system. The number of contributing compounds can vary from just two, to several thousand, each with different concentrations and detection thresholds [21]. The issue becomes even more complicated when taking into account that the detection thresholds for the compounds within a complex odor can vary from their own detection threshold when they are considered as simple odors. So, although the relationship between structure and response is easy to model for simple odors, the relationship for complex odors is highly non-linear. All of these issues contribute to the complexity of developing an electronic analog to the biological olfactory system.

1.3.2 What is an Electronic Nose?

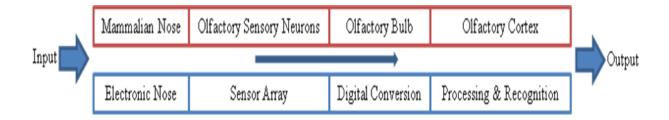


Fig. 5. Schematic representation of biological olfactory system and its electronic analog.

Although the term "electronic nose" has been used by scientists for many decades, the following definition was first published in 1994 [24]:

"An electronic nose is an instrument which comprises an array of electronic chemical sensors with partial sensitivity and an appropriate pattern recognition system capable of recognizing simple or complex odors."

A schematic comparing the structure of an electronic nose to the biological olfactory system is shown in Fig. 5.

1.3.3 Biological Olfaction

The biochemical processes and machinery involved in olfactory sensing are complex and not yet fully understood. In this section a simple overview is provided of the current understanding of mammalian olfaction. The basic processes involved in human olfaction are the following, inhalation of an odorant into the nasal cavity, transport of the odorant across an aqueous mucous layer, interaction of the odorant with OSNs, the generation of electrical signals by the sensory neurons, the communication of the electrical signals from the olfactory neurons to the olfactory bulb, processing of the signals in the olfactory bulb, and finally transport of signals to the olfactory cortex from where the information is projected to other sensory centers of the brain [25].

1.3.3.a The Nasal Cavity

The process of olfaction begins with the transport of volatile odorant compounds into the nasal cavity during the process of inhalation. The incoming air and its contents are filtered,

warmed, and humidified during the inhalation process. [23]. Most of the air and the odorants it may contain are then transported to the lungs during the respiratory process. A small amount of air containing a few odorant particles comes into contact with the olfactory epithelium which contains the OSNs; this is because the olfactory epithelium is located in the posterior of the nasal cavity and is not directly in the path of the incoming air.

1.3.3.b The Olfactory Epithelium

OSNs are located in the olfactory epithelium, an area of tissue about 6 cm² in humans. Because the tissue is covered with a mucous layer the interaction between odorants and OSNs occurs in an aqueous environment. The odorant must first cross this aqueous layer to interact with the OSNs. Different processes, referred to as perireceptor events [26], determine the length of time an odorant molecule spends in the mucous and in the vicinity of the odorant receptors. These include the transport of often hydrophobic molecules across the mucous, along with the chemical transformation of molecules by enzymes while within the mucous [27]. In the insect olfactory system the transport of hydrophobic odorant molecules is aided by odorant binding proteins (OBPs), which enhance the aqueous solubility of the odorants [28].

The olfactory epithelium is primarily composed of three different types of cells. The OSNs, basal cells, and supporting cells. Interestingly, OSNs, having a half-life of 4 to 8 weeks are one of the few types of neurons which regenerate in the adult brain, and it is the basal cells which facilitate this regeneration [29]. The OSNs themselves are bipolar neurons, long and thin with the dendrite and axon extending out from opposite ends. The dendrites project up into the mucous layer covering the epithelium where they terminate with multiple cilia per neuron. These cilia move with the mucous acting to increase the area where odorant binding can occur.

This termination site is also where the receptors that bind to odorants exist, these odorant receptors are from a family of G protein-coupled receptors (GPCRs), which are used in signal transduction across cell membranes.

1.3.3.c Odorant Transduction

In the mammalian olfactory system each OSN expresses exactly one of the approximately 1000 types of odorant receptors [30]. The odorant receptor proteins exist both inside and outside the OSNs, spanning the cell membrane. Thus the binding of an odorant is communicated from outside the cell to within the cell membrane. The receptor binding is transduced by a G-protein system that triggers the generation of secondary messengers within the cells [31]. The binding of one molecule to a receptor leads to the generation of secondary carriers, and thus can be thought of as an in-cell amplification step. It should be noted that instead of binding to a specific odorant molecule, each receptor displays varying affinity for a range of odorants, and that a single odorant may also bind to different types of receptors [32].

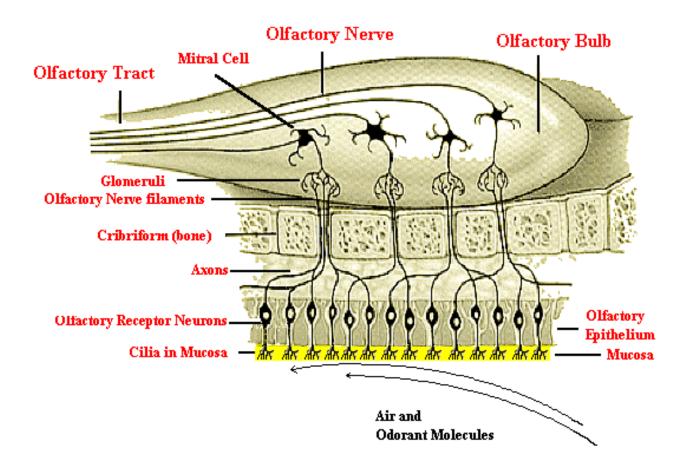


Fig. 6. Diagram of human olfactory system. The cilia of the OSNs protrude into the mucosa, while the cell bodies remain in the olfactory epithelium. The axons of the OSNs pass through the cribriform plate and meet at glomeruli in the olfactory bulb. Figure taken directly from [33].

1.3.3.d The Olfactory Bulb

Each olfactory neuron in the olfactory epithelium projects a single axon to the olfactory bulb, shown in Fig. 6. These axons converge into a bundle known as the olfactory nerve and pass through an aperture in the cribriform plate to reach the olfactory bulb. OSNs expressing a particular receptor may be randomly distributed in the olfactory epithelium, but they all project their respective axons to one or a few closely spaced networks of axons, dendrites, and synapses (neurophil known as glomeruli) in the olfactory bulb [34, 35]. Here the axons from single OSNs form synaptic connections with many other OSNs expressing the same type of receptor. Thus

the binding of a particular odorant molecule at the olfactory epithelium results in the conglomeration of activity at certain glomeruli in the olfactory bulb. The organization of the glomeruli can be thought of as a map, and particular topographical activity patterns are associated with specific odorants [23]. The fact that many OSNs expressing the same odorant receptors meet at a single glomerulus which goes on to stimulate a group of approximately 25 mitral cells has two very important effects on the transduction and recognition of odors. First, the fact that multiple cells expressing the same receptor meet at the same point means that the sensitivity of being able to detect a particular odorant increases. Secondly, since OSNs regenerate, at any given time OSNs with a large range in age produce activity at a single glomeruli, this is thought to help with output drift and sensitivity decrease which may occur to an OSN over the course of its lifetime [23]. The mitral cells which receive excitatory inputs from the OSNs at the glomeruli also receive inhibitory inputs from their lateral synaptic connections to granular cells, which adds another layer of signal processing to the interpretation of odors [36].

1.3.4 Machine Olfaction

There have been many different approaches to machine olfaction. Nearly all of the methods rely on some type of chemical interaction. Odorants bind to some chemically sensitive layer that produces a response that is transduced to a readable signal. Sensors of this type include: metal-oxide, conducting polymer, acoustic wave, field effect, electrochemical, pellistor based, chromatograph, and fiber optic. Much work has been done in this field and has been reviewed in [24, 37-39]. There has also been significant interest in using olfactory sensors to detect explosives, which has led to the development and commercialization of different types of sensors

including luminescent and fluorescent polymers, and quartz crystal microbalances, as reviewed in [21].

The approach of using OSNs as the sensing front-end has also been shown in the past. OSNs have been used to detect explosives [40], as well as other odorants [41-47], however, in all of these cases the recordings from the neurons were either invasive if in-vitro or in-vivo, or of local field potentials from intact epithelium. None of these examples of sensors have demonstrated the ability to record activity from individual OSNs in a non-invasive manner.

1.4 Cell-Based Olfactory Sensors

A primary contribution of this work is the demonstration of a proof-of-concept hybrid bioelectronic olfactory sensor. The sensor will be introduced in Chapter. 4, this section will serve to provide context for this contribution. First the concept of cell-based sensing will be discussed, followed by a brief review of prominent cell-based olfactory sensors, and then a summary of the methods and basic circuits used in the development of the olfactory sensor introduced in this work.

1.4.1 Cell-Based Sensing

Cell-based sensing refers to any case where living cells are used to determine information about the surrounding environment or a particular stimulus. Cell-based sensing leverages the high specificity and sensitivity of biological cells to perform sensing in ways that may not be possible with other types of sensors [48]. Many different types of cells can be employed for cell-based sensing, ranging from naturally occurring sensory cells such as OSNs, to genetically modified cells created for a specific sensing task.

Using cells as technology is actually quite commonplace. The biotechnology industry has long used cells for synthesis of bio-products such as proteins and vaccines. Cell-based sensing is similar, except that the cells are used to transduce information from one domain to another. Such sensors can be used for numerous purposes including detection of minute quantities of chemicals, toxicology assays, and testing of new drugs before they come to market.

Readout of information from cells is a key aspect of developing cell-based sensors. With the cells acting as the sensing front-end, an integrated system must be able to interpret the responses from the cells. Typically, this is performed in one of four ways, chemical sensors that are designed to sense the chemical signaling naturally exhibited by cells [49], electrical sensors that can pick up the voltage signals produced by electrogenic cells [50], fluorescence sensors that can detect bio-luminescence produced by the cells [49], and finally sensors that can detect the morphology of cells [51].

1.4.2 Existing Cell-Based Olfactory Sensors

There exist in the literature a number of cell-based olfactory sensors. All use biological odorant receptors as the primary transduction elements. After the odor is transduced by the cell (or other biological structure), different methods are used to readout the information. The methods discussed here are based on either fluorescence or detection of electrical signals.

1.4.2.a Living Animals as Olfactory Sensors

One approach to creating an olfactory sensor is to use not only the sensory cells to transduce the signal but the entire animal itself as a sensor. This method has the added advantage of allowing the OSNs to stay within their natural environment. Thus, the cells are maintained as they normally would be, and the responses of the cells to odors should most closely recreate those that would occur naturally.

1.4.2.a.i An in vivo Sensor using a Rat

This method has been employed with mammals, such a system is presented in [42], where a microelectrode array is placed in the olfactory bulb of a rat. An overall schematic of the system is shown in Fig. 7. The animal is exposed to odors and neural activity in the olfactory bulb is analyzed to identify unique firing patterns corresponding to individual odors.

The recordings of bio-potential signals were from multiple neurons, simultaneously. This method was successfully used to discriminate between 6 different odors. Results showed that high quality recordings could be achieved for a period of three weeks.

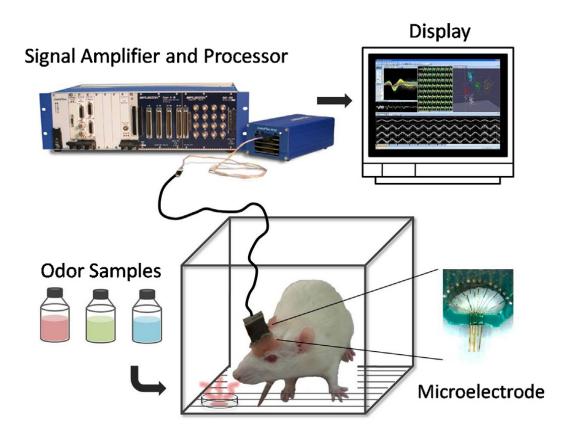


Fig. 7. An in vivo biosensing system. Microelectrodes and an external amplifier are used to record neural signals from the olfactory bulb of a rat. The animal is presented with odors, and the resulting recording is analyzed to determine unique patterns corresponding to individual odors. Figure taken directly from [42].

1.4.2.a.ii Recordings from Salamander Epithelium

Unlike the previous case where recordings were taken from the olfactory bulb of the rat, early work presented in [52] shows that olfactory sensing can be performed by directly recording from the olfactory epithelium of live salamanders. Though this work was primarily done to characterize the electrophysiological response of salamander OSNs to odors, it represents a viable method for creating an olfactory sensor. The basic schematic of the sensor is shown in Fig. 8.

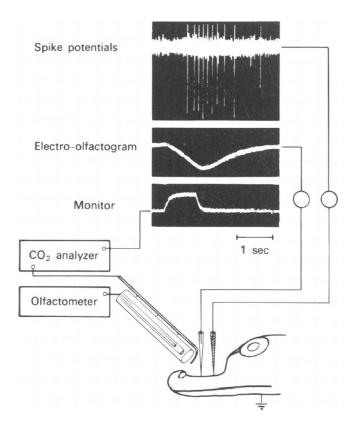


Fig. 8. Recording from the intact olfactory epithelium of a live salamander. Recording electrodes are placed in the epithelium and the response to controlled odor pulses is characterized. Figure taken directly from [52].

Recording electrodes were placed in the olfactory epithelium of a live salamander. The animal was exposed to controlled pulses of odors, the durations of which were recorded by a

CO₂ analyzer (the odors were mixed into a gas mixture of 95% O₂ and 5% CO₂). This method allowed basic characterization of the behavior of in vivo OSNs. This work served as the foundation for future works in which the response of salamander OSNs to longer time duration odorant presentation was characterized [52, 53]. Some of the relevant results from the later work are shown in Fig. 9. These early works help to establish context for much of the methods and results discussed in Chapter. 4.

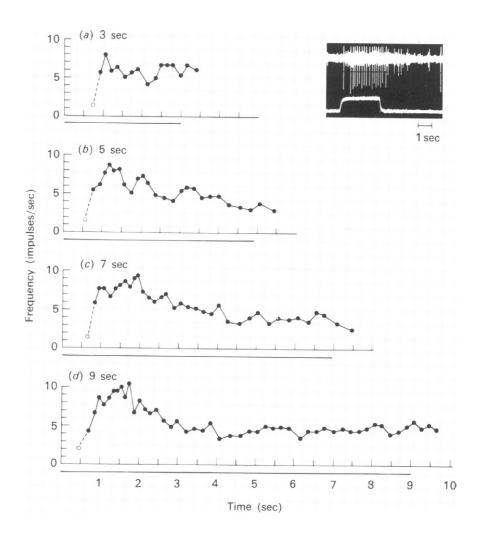


Fig. 9. Recorded firing rates of OSNs to the presentation of longer duration odorant stimuli. Plot a) shows the response to 3 seconds of stimulus, plot b), c), and d) show the responses to 5,7,and 9 seconds (respectively). These plots show that the onset of spiking occurs quickly after odor presentation and that though they exhibit adaptation; the neurons continue firing during and post odor presentation. Figure taken directly from [54].

1.4.2.a.iii Insect Electroantennography

Though the olfactory system in insects is different than that of either mammals or amphibians, the same methods can be applied to detect electrical signals generated in response to odors. In the case of insects, the odorant receptors exist on the antennae, and the method of electroantennography (EAG) can be used to detect overall changes in electrical potential between the tip of the antenna and the base of the antenna, representing a summation of elicited responses of the antenna to its environment. Developed in 1957 [55] the basic schematic for the technique is shown in Fig. 10e, in which the potential difference between the tip and base of the antenna are measured.

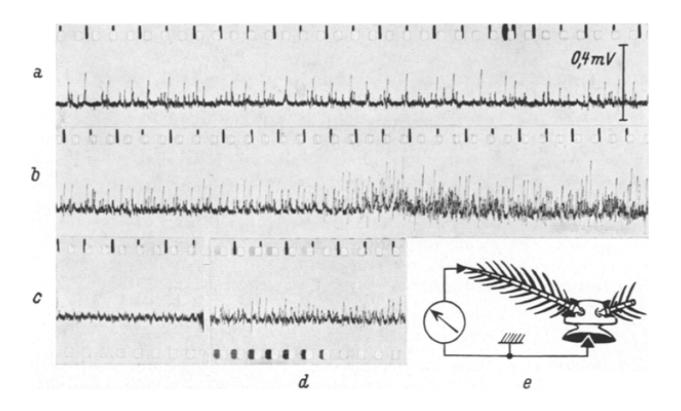


Fig. 10. The technique of EAG and resultant recordings. Insets a)-d) show recordings produced using the EAG method. Inset e) shows a schematic of the technique, where the electrical potential difference between the tip and the base of the antenna are measured. Figure taken directly from [55].

The technique of EAG continues to be used, not only to characterize the response of insect antennae to odors [56-58], but also to create sensors [59, 60]. This method has been extended to robotics, using an EAG based sensor to provide navigational input to locate a hidden odor source [61], images of the device and experimental setup used for this example application are shown in Fig. 11.

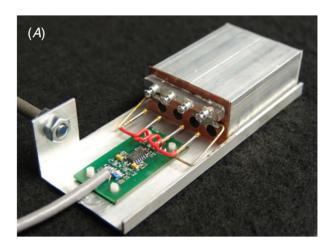




Fig. 11. An EAG based sensor used for robotic navigation. A) Shows the device, which includes 4 EAG amplifiers as well as the chamber for housing the insects. B) Shows the experimental setup in which the sensor (foreground) was used to provide navigational data to locate an odor source (tripod in the background). Figure taken directly from [61].

1.4.2.b Fluorescence Based Olfactory Sensing

Though the response of OSNs to odor stimulus is ultimately measurable as a voltage signal, the generation of an action potential requires the dynamic opening and closing of a number of different ion channels in the cell membrane. One method of capturing the dynamics of ion flow across cell membranes is to use fluorescence. In the case of calcium channels, specially developed fluorophores exhibit increased fluorescence upon binding to Ca²⁺ ions. Thus fluorescence can be used to interrogate the response of OSNs to olfactory stimuli.

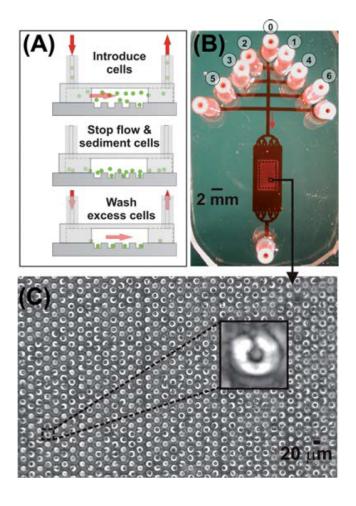


Fig. 12. The microfluidic device used in [62] to interrogate the response of OSNs to chemical stimuli using fluorescence. A) Cell loading. B) An overhead view of the entire device. C) A close up view showing cells trapped in well. Figure taken directly from [62].

This was demonstrated in [62], where fluorescence was used to characterize the response of an array of OSNs to various odorants. A microfluidic device was used to trap a large number of dissociated cells from the olfactory epithelium of a mouse. The cells were loaded with the fluorophore and then exposed to chemical stimuli. First the cells were exposed to a high potassium solution to determine which cells were actually OSNs. Then the cells were exposed to a series of odorants and the spatial pattern of the fluorescence response was characterized.

1.4.2.c Multi-electrode arrays

One way to record the electrical activity of OSNs is to use multi-electrode arrays in combination with external amplifiers. This can be performed in vivo as shown in Section 1.3.2.a, or it can be done in vitro using either individual cells or tissue. The basic technique is to harvest tissue of interest (olfactory epithelium) from an animal and then to either dissociate the cells into individual cells before recording, or to record from the whole tissue itself. The cells or the tissue are placed on the surface of a multi-electrode array and then exposed to chemical stimuli, resulting electrical activity is recorded and analyzed on an external computer to determine firing patterns that are unique to specific odors.

Whole epithelium recordings have been shown in [47], the basic schematic for the setup is shown in Fig. 13. The epithelium was exposed to a number of different stimulants, and the resulting electrical activity was recorded and analyzed.

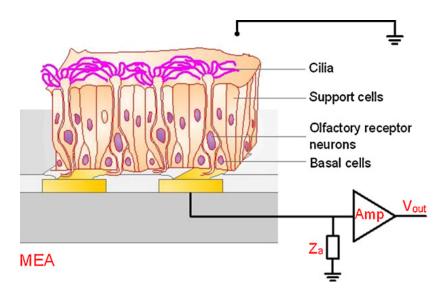


Fig. 13. The schematic for an olfactory sensor based on whole epithelium plated on a micro-electrode array. Figure taken directly from [46].

When individual cells are used, the methods are slightly different. The harvested tissue is subjected to a digestion process, either enzymatic, or in some cases mechanical, to yield individual dissociated cells. The cells are then plated on the surface of a micro electrode array and similar experiments are performed to determine the response of the cells to odorants.

Odorants can be introduced in an aqueous phase or as a gas. The latter more closely mimics the biological system, though it lacks the mucous and proteins that help transport odorants to the OSNs. This method was demonstrated in [63], where a commercially purchased micro-electrode array was used to culture dissociated rat OSNs. A gas delivery system was employed to deliver odorants to the cells. Though the response of the system was slow (on the order of 100 seconds), the method was able to record activity from multiple sites (60) simultaneously and analyze the information to determine specificity towards odorants.

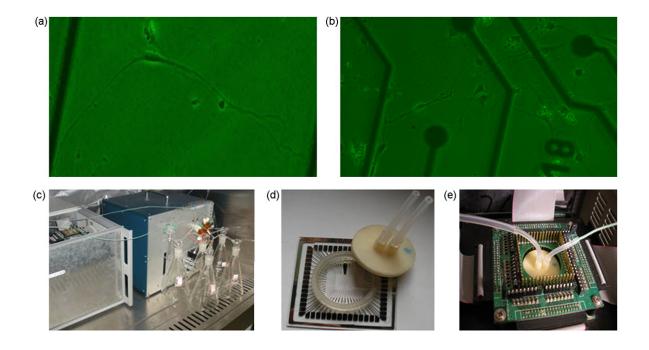


Fig. 14. A gas phase cell-based olfactory sensor. A) Shows an individual OSN. B) Shows a number of different OSNs. C) Shows the gas delivery system. D) Shows the commercial multi-electrode array on which the cells were cultured. E) Shows the custom setup used to connect to the array and amplify the signals. Figure taken directly from [63].

1.4.2.d Light Addressable Potentiometric Sensors

A disadvantage of using micro-electrode arrays is that precise placement of OSNs relative to the recording sites is difficult to achieve. In most cases the cells are plated from a solution in which they are suspended, yielding essentially zero control over where on the array the individual cells will eventually settle. Thus, in some cases it may be impossible to pick up electrical signals from cells that are too far away from the recording electrodes.

A solution to this issue is to use light addressable potentiometric sensing (LAPS). LAPS technology allows the conductivity of a semiconductor substrate to be modulated by application of light. In effect the semiconductor substrate acts as a photoconductor. The properties of the photoconductor change when the applied bias is changed. In the case of LAPS a mean DC bias is applied to the cell medium, but local changes in potential are generated by electrical activity of OSNs, thus it becomes possible to locally measure the surface potential of the semiconductor substrate by shining a laser on its surface. This method has been used to measure local field potentials generated by both intact olfactory epithelium [45] as well as dissociated OSNs [44]. A schematic for the whole epithelium based sensor is shown in Fig. 15.

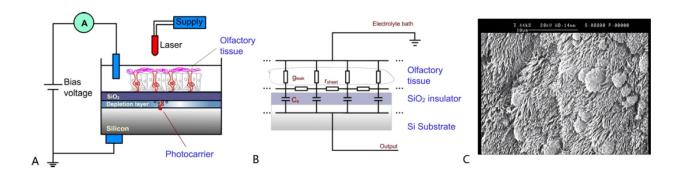


Fig. 15. LAPS based whole epithelium olfactory sensor. A) Shows the schematic diagram of the LAPS setup. B) Shows the equivalent circuit model. C) Shows a close up image of olfactory epithelium. Figure taken directly from [45].

1.4.3 Cell-Based Olfactory Sensing on CMOS

Artificial olfactory sensors that rely on a chemical binding event have the limitation that a-priori knowledge is required of the analyte to be sensed. Biological olfaction overcomes this through the use of many distinct types of olfactory sensory neurons (OSNs), each expressing unique receptors. The combination of firing patterns amongst the thousands of neurons in response to an odor distinctly classifies the odor. Simply put, a biological olfactory system can be trained to recognize new odors which it has not previously been exposed to, something which cannot be said for other olfactory sensors. The approach taken by this body of work is to combine the biological mammalian olfactory system with CMOS ICs to create a hybrid bioelectronic nose on a chip. This is a multi-disciplinary approach borrowing from and contributing to the fields of electrical engineering, microelectromechanical systems, materials science, and biology.

Cell-based sensing lends itself well to the development of artificial olfactory sensors.

Olfaction and taste are the only two basic senses that cannot easily be described as information transfer using energy. The other three senses are readily addressed by electronic sensors. Sight can be performed by transduction of optical energy into electrical energy. Hearing relies on physical perturbations caused by sound waves. The sense of touch is mechanical force that can be transduced to electrical energy using well known mechanisms. Olfaction and taste are chemoreceptive senses, and as such the development of artificial sensors that can recreate these two basic senses lags far behind the rest. This leads to the motivation to use OSNs as the transduction element in an artificial olfactory sensor, which is primarily, why attempt to create an artificial transducer when nature has already provided an exquisitely sensitive structure?

There has been a lot of effort over the years to create artificial olfactory sensors, yet they remain severely limited in their applications. On the other hand, cells have evolved to have a response profile that's naturally matched to a stimulus profile for which no other good sensors exist.

The advantages of using OSNs as the sensing front-end are many. Apart from the ability to sense an essentially limitless number of odorants, the cells contain the machinery to maintain their odorant receptors over time so that sensor degradation does not occur. The OSNs produce action potentials which are electrical signals that can directly be sensed by electronic systems. Finally, the cells have high sensitivity due to internal amplification within the cells such that a small number of binding events can lead to an easily detectable action potential.

By culturing OSNs directly on the surface of CMOS chips, the advantages of both systems can be combined to create a standalone bioelectronic olfactory sensor. The biological front-end provides the sensitivity and selectivity while the integrated circuit back-end provides signal conditioning, pattern recognition, training capability, and any required communication or control.

1.4.4 Measuring Electrophysiological Signals

There are three fundamentally different ways to perform electrophysiological measurements of the ionic currents and resultant voltage spikes from electrogenic cells. The first group of methods is based on intra-cellular recordings; methods such as patch clamping are used to either penetrate or attach to the cell membrane with an apparatus capable of sourcing and measuring current and voltage. The second group of methods is based on extracellular recording, where external electrodes are used to record the voltage generated by the flow of ionic currents

in and out of the cell membrane. There are many variations of the extracellular recording method, ranging from small electrodes that record from single neurons, to field potential recording and amperometry, which measure changes in ionic concentration over a larger area. The intracellular techniques are invasive in nature, and do not easily allow for high throughput because individual cells have to be "patched", although, recently a new method coined the "planar patch clamp [64]" has been developed which creates an array of patch clamping sites on a planar substrate. The third method is to use voltage sensitive fluorescent dyes, which change their optical properties based on changes in voltage. The response of voltage sensitive dyes is fast enough to detect single action potentials, but phototoxicity and delivery challenges have discouraged their widespread use [65].

1.4.5 CMOS Active Arrays

Extracellular recordings are performed either by implanting a sensing array into living tissue or by culturing cells on the surface of electrodes. In both cases the ionic currents from the electrical activity of the cells result in a measurable electric potential at the recording electrode. There are two types of electrode arrays, passive arrays and active arrays. Passive arrays are simply electrodes on a surface that must be connected electrically to an external amplifier and other electronic circuits for signal conditioning and readout. Active arrays incorporate the amplification and signal processing in the substrate on which the electrodes exist. The advantage of using active arrays is that the signals which are weak in nature don't have to travel very far before they are amplified. An additional benefit of this is that the shorter path length also leads to lower likelihood that noise will be incorporated into the signal [66, 67], leading to a higher signal to noise ratio (SNR). One way of fabricating active electrode arrays is to use CMOS technology.

Amplifiers and other electronic circuits can be fabricated within the bulk of the semiconducting material, while electrodes can be fabricated on the top surface.

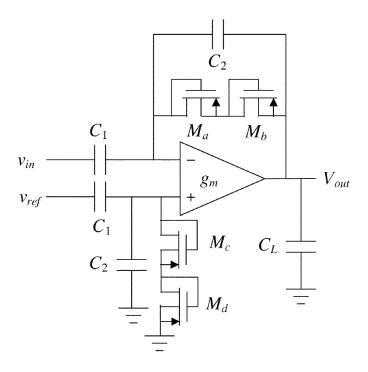


Fig. 16. Schematic of neural amplifier circuit. An operational transconductance amplifier with gain set by capacitive feedback. Figure taken directly from [50] \odot 2003 IEEE.

CMOS neural amplifiers capable of amplifying and recording the action potentials from electrically active cells have already been demonstrated [68-73]. The basic circuit used for the bioamplifiers in this work is based on [50], the overall schematic for a single bioamplifier is shown in Fig. 16. This circuit is an operational transconductance amplifier (OTA) with its gain set by capacitive feedback. The circuit internal to the OTA as originally proposed in [50] is shown in Fig. 17, minor adjustments were made to this circuit, most notable of which is the addition of a cascode to the current mirror formed by transistors M₉ and M₁₀, this was done to increase the common-mode rejection capability of the structure.

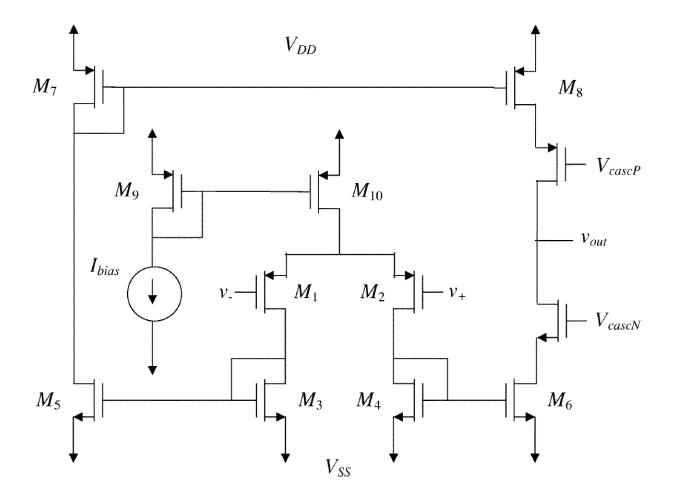


Fig. 17. Internal transistor-level schematic of the OTA. Minor adjustments were made to this circuit for this work, but its core operation remains the same. Figure taken directly from [50] © 2003 IEEE.

The integrated circuits used in this work have been fabricated in a commercially available $0.35~\mu m$ CMOS process using the MOSIS service. An example CAD layout of a 3 mm x 3 mm bioamplifier chip that includes 32 individual amplifiers is shown in Fig. 18. The bond pads on the periphery of the chip provide electrical connections to the outside world, while the square electrodes inside the chip boundary serve as recording sites. The large rectangular electrode in the center acts either to set the electrical potential of the cell medium, or to allow its measurement.

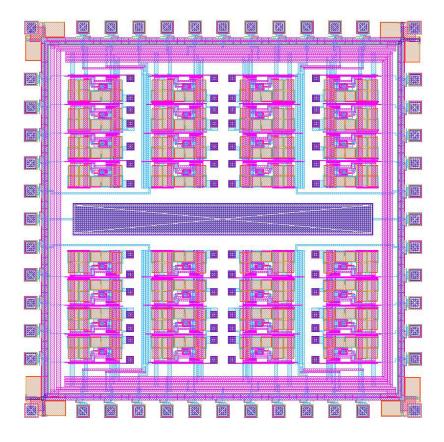


Fig. 18. CAD drawing of a Bioamplifier designed in 0.35 μm process, including 32 neural amplifiers.

The bioamplifier serves as the IC for all of the integrated systems presented in this work. Though the IC has gone through multiple iterations, the core design of the bioamplifier remains the circuit shown in Fig. 16. The only real change to the system has been the addition of unity gain buffer stages after the amplifiers. The buffer stages proved necessary when considering the large capacitive load presented by the data acquisition hardware used in this work.

1.5 Spike Information Acquisition

Typically, action potential spiking data is taken off-chip in an analog fashion. A commercial data acquisition system connected to a computer is used to record high resolution data from multiple channels simultaneously at high speed, and the signals are then stored on a computer. Recording signals at high speed and high resolution results in large data files are unwieldy to view and manipulate.

The information of concern contained in these data streams is the occurrence of action potentials. And, most of time, the cells are not spiking so the data that is recorded is essentially a flat line, leading to wasted storage space and unnecessary use of bandwidth. Furthermore, given the all-or-nothing nature of action potentials, the temporal dynamics of single spikes are generally exactly the same and in most applications carry no additional information.

Because of these reasons it is advantageous to represent the information in a different manner, one which will use far less file space and data bandwidth, while still conveying the necessary information. One such protocol that is readily applicable to neural data is address event representation (AER) [74], an asynchronous method in which what is transmitted is the occurrence of events rather than the events themselves.

1.5.1 On-Chip Spike Detection

Using AER significantly decreases the cost associated with data collection and processing since it will turn analog signals into digital events. However, to be able to use AER, the detection of an event must be done on-chip, so that its occurrence can be transmitted off-chip.

So, spike detection must be performed at the individual amplifier level (so called "in-pixel"), or using some sort of multiplexed-bus scheme. To perform in-pixel spike detection and not significantly decrease amplifier density per chip, the detection circuits should be smaller in area than the amplifiers themselves. There have been many different approaches to spike detection, some of the more common methods include adaptive thresholding [75], non-linear energy operator (NEO) [76], and derivative computation [77]. Other, more computationally intensive methods have also been used, such as matched filters and wavelet transforms [77]. Recently, very promising results have been shown using a modified version of the NEO algorithm [78].

1.5.2 Scalability of Future Cell-Based Sensors

As the density of microelectrode arrays increase, so will the required signal readout bandwidth. Correspondingly the file sizes for data storage will increase, as well as the computational effort required to process the data. Because of these reasons it is desirable to develop a system that is capable of outputting only the signals of interest in an effort to minimize bandwidth and storage requirements.

One of the primary technical contributions of this work (Chapter. 5) is the evaluation of some of the different methods for on-chip spike detection, and implementation of an AER-based active micro-electrode array with on-chip spike detection. To date this method represents the most bandwidth efficient manner for readout of spiking bio-potential signals.

Chapter. 2

Packaging

2.1 Preface

This chapter is a reproduction of [79], an article with multiple authors. My own contributions to this work include the development of the packaging method (with guidance from Dr. Elisabeth Smela), all of the experimental work, and much of the writing.

2.2 Abstract

Combining integrated circuitry with microfluidics enables lab-on-a-chip (LOC) devices to perform sensing, freeing them from benchtop equipment. However, this integration is challenging with small chips, as is briefly reviewed with reference to key metrics for package comparison. In this paper we present a simple packaging method for including mm-sized, foundry-fabricated dies containing complementary metal oxide semiconductor (CMOS) circuits within LOCs. The chip is embedded in an epoxy handle wafer to yield a level, large-area surface, allowing subsequent photolithographic post-processing and microfluidic integration. Electrical connection off-chip is provided by thin film metal traces passivated with Parylene-C. The Parylene is patterned to selectively expose the active sensing area of the chip, allowing direct interaction with a fluidic environment. The method accommodates any die size and automatically levels the die and handle wafer surfaces. Functionality was demonstrated by packaging two different types of CMOS sensor ICs, a bioamplifier chip with an array of surface

electrodes connected to internal amplifiers for recording extracellular electrical signals and a capacitance sensor chip for monitoring cell adhesion and viability. Cells were cultured on the surface of both types of chips, and data were acquired using a PC. Long term culture (weeks) showed the packaging materials to be biocompatible. Package lifetime was demonstrated by exposure to fluids over a longer duration (months), and the package was robust enough to allow repeated sterilization and re-use. The ease of fabrication and good performance of this packaging method should allow wide adoption, thereby spurring advances in miniaturized sensing systems.

2.3 Introduction

Lab-on-a-chip (LOC) devices, or micro total analysis systems (microTAS) [80], have the potential to replace large-scale laboratory equipment for chemical and biological analyses. The concept of a miniaturized platform for sampling, performing reactions, and detection was exemplified early on in [1, 2, 14]. Microfluidics has been the key enabling technology, allowing development of devices for applications ranging from basic scientific research to point-of-care diagnostics. Most LOCs, however, are still chips in labs, requiring benchtop instrumentation for sensing. To address this issue, LOC devices can incorporate complementary metal oxide semiconductor (CMOS) circuitry, the technology used in the chips found in computers, cell phones, and other electronic devices. It is well known that CMOS integrated circuits (ICs) can perform computational tasks such as signal processing [66] (e.g. amplification, filtration, classification, mathematical manipulation, logic), control of actuators [81] and other system components, and information readout [82, 83]. Less well-known is that CMOS can also been used for directly sensing various types of stimuli, not just electrical, but also thermal [84],

electrochemical [85], magnetic [86-88], and optical [89]. Combining microfluidics with computation and sensing capabilities enables microsystems to become actual labs on a chip. Advances in CMOS-based microsystems have been reviewed in [82, 84, 90-93].

The utility of CMOS ICs in LOC devices can be further increased by the addition of surface micromachined structures [66, 82-84, 92, 94]. Features such as microfluidic channels [87, 88], wells or vials [95], coatings [96], and optical filters [97, 98] can be added to the surface of the die. Devices such as micromechanical actuators and 3D electrodes [99] can be electrically connected to the internal circuitry through vias in the surface passivation layer.

CMOS chips are particularly well suited for sensing weak electrical signals from biological sources such as electrogenic cells. High signal to noise ratios (SNRs) can be achieved by placing on-chip amplifiers directly under the sensing electrodes to reduce the path length from the signal source [66, 67]. The benefits of shorter distances also apply to other sensing modalities. For example, in fluorescence measurements the SNR can be improved by placing the photodetector close to the light source [100].

Researchers have two main sources for custom CMOS chips: research clean rooms for relatively simple devices and commercial foundries for high density circuits featuring very large scale integration (VLSI) of millions of transistors. As CMOS feature sizes shrink, following Moore's Law, semiconductor fabrication facilities become outdated for industrial production, but they remain active and available for less demanding applications and research use [92, 93, 101]. Universities and small companies have access to the somewhat older, larger-feature technologies through aggregation onto multi-project wafers (MPWs), such as the IC prototyping offered through the MOSIS service, in which multiple customers share space on a wafer. At US

institutions, student projects are often allocated free space in units of so-called "tiny chips", which have an area of 1.5 x 1.5 mm²; larger chips, for research use, can also be obtained, with cost proportional to silicon area. Chips produced in a research lab lack this size constraint and can be made as large as desired. The focus of this paper is on the small commercial chips, delivered diced and unpackaged. (They can also be ordered wire-bonded into standard chip carriers.)

Unfortunately, inclusion of CMOS in applications that require direct contact of electrodes or sensors with a fluid medium complicates packaging and system integration [92], which is one of the reasons that it still remains an emerging technology in the LOC community. For one thing, the small size of the dies poses clear problems in handling and microfabrication.

Additionally, fluidics typically have lateral dimensions measured in cm, an order of magnitude greater than the chip, necessitating a package that manages this size disparity [85]. Furthermore, with the commercially fabricated chips the industry-standard packaging methods enclose the die within a carrier and provide electrical connectivity to the outside world via bond pads at the periphery of the top surface of the chip [102], limiting flexibility for system integration.

In this paper we describe a new method for packaging foundry-fabricated CMOS dies in a way that allows photolithographic post-processing on the surface and microfluidic integration, with the fluid making direct contact with the chip active area. These packages are robust enough for cleaning between experiments and long term exposure to cell medium at 37 °C (nearly 4 months without failure). The method is insensitive to variations in die size and shape (variations in lateral dimensions can be hundreds of μ m and variations in thickness, tens of μ m). The chip is embedded in an epoxy carrier, or handle wafer, to produce a flat, large-area surface. Thin film

metal interconnects are made to the bond pads, and the I/O region is passivated with Parylene. We demonstrate the utility of the method by showing proper electrical functionality of two different types of packaged CMOS ICs. The first, a bioamplifier chip designed for amplification of extracellular action potentials and the second a capacitance sensor chip; both functioned correctly in the new package.

2.4 Fabrication

The process flow used for the bioamplifier IC is shown in Fig. 19. In summary (details are given below), the chip is placed face-down into the center of a glass petri dish coated with PDMS (Fig. 19a); the dish acts a mold while the PDMS serves a dual purpose: first as a surface to which the chip is temporarily adhered and second as a release agent for the epoxy. Epoxy is poured around the chip and cured (Fig. 19b), thereby forming a handle wafer for processing and microfluidic integration as well as a substrate for electric connections and fan-out[85]. After curing, the epoxy wafer is removed from the petri dish, leaving the chip face-up. Cr/Au is sputter-deposited onto the surface and patterned to provide connectivity to the chip's I/O region and to cover the Al electrodes from the CMOS process with a biocompatible and electrochemically inert metal in the active region (Fig. 19c). Poly(3,4-ethylenedioxythiophene) doped with poly(styrenesulfonate), PEDOT:PSS, is electrodeposited on the Au electrodes in the center of the chip to decrease interfacial impedance with the solution. A conformal coating of Parylene is deposited and patterned to expose the active area of the chip and cover the I/O region (Fig. 19d,e). A packaged die is shown in Fig. 20.

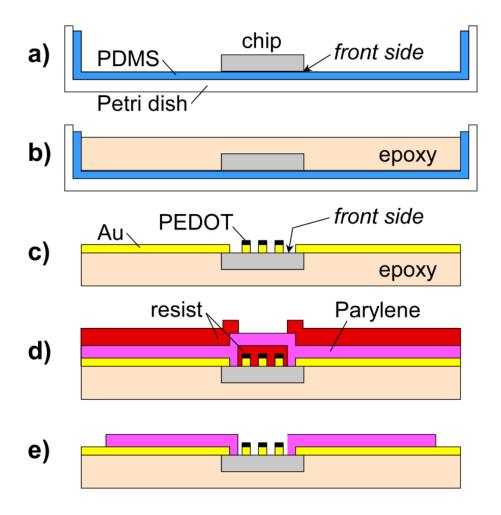


Fig. 19. Cross-sectional view of the packaging process sequence. Fabrication steps are described in the text.

The process sequence for packaging alone (as used for the capacitance chip), excluding post-processing (e.g. PEDOT deposition), requires three steps: formation of the epoxy handle wafer, deposition and patterning of the metal interconnects, and deposition and patterning of the Parylene passivation layer. Three masks are required, one for patterning the metal and two for patterning the Parylene, which is done using a two-step process of dry etching and liftoff (explained below). (One additional mask was used to pattern the PEDOT for the bioamplifier chip.)

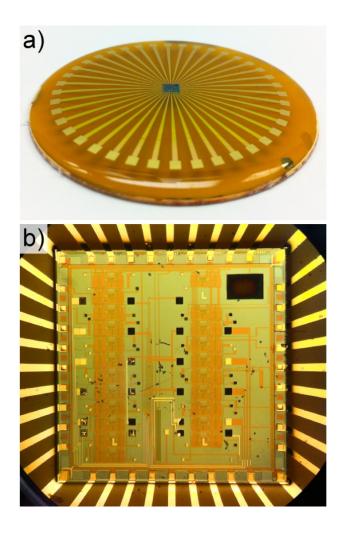


Fig. 20. a) A packaged bioamplifier die. Patterned thin-film Au connections fan out from the chip to the edge of the 5 cm handle wafer. b) Close-up view around the die.

2.4.1 Mold Preparation

The handle wafer was created within a 50 mm Pyrex petri dish. The dish was lined with PDMS by manually mixing a 10:1 ratio of elastomer base to curing agent (Sylgard® 184) for 4 minutes (until it appeared visually to be homogenous). The mixture was placed into a vacuum desiccator for 20 minutes to remove bubbles. The PDMS precursor (5 g) was poured into the dish, and the dish was rotated manually to coat the sidewalls. The PDMS was again placed into

the desiccator for a further 20 minutes and rotated on its edge to thicken the coating on the sidewalls. The dish was placed on a level hotplate and the temperature was ramped from room temperature to 120 °C over a period of 10 hours. Curing the PDMS this slowly facilitated the release of absorbed gas. (This was critical. Gas released from the PDMS during subsequent epoxy curing results in bubbles within the epoxy.) The dish was covered to decrease thermal gradients. The PDMS was held at 120 °C until the epoxy was added.

2.4.2 Die Encapsulation with Epoxy

The dies were unpackaged as supplied from the foundry. Surface cleanliness is essential to achieving high yield, so just before packaging the dies were rinsed in acetone, methanol, isopropanol, and deionized water followed by a dehydration bake (150 °C, 15 minutes). When the die is placed onto the PDMS, it is critical that it adhere well to prevent epoxy from creeping under the die. This can be ensured by applying force to the center and corners of the back of the die by gently pressing with tweezers.

Several characteristics of the epoxy are essential for successful packaging. A high resistivity is required to isolate the electrical traces. The wafer experiences temperatures between -20 ° and +150 °C during processing, so a coefficient of thermal expansion (CTE) similar to that of Si reduces interfacial stress. The epoxy should also be able to withstand exposure to photoresist (AZ9260), developer (AZ400K), and Cr and Au etchants (Transene TFE and TFA, respectively) during microfabrication, as well as the ethanol and UV light to which it is exposed during cell culture. The viscosity of the precursor should be low to permit complete filling of the mold and easy removal of air bubbles inadvertently trapped during mixing. A high

thermal conductivity minimizes temperature gradients during processing so that photoresists bake evenly.

Several products were tested for suitability as handle wafers, including Loctite 3340 (a photocurable polymer), MasterBond EP30AO, Cotronics Duralco 128 ceramic-filled epoxy, Duralco 4525, Duralco 4461, and EPO-TEK OJ2116 (formerly 88-116). Only one epoxy, Cotronics Dura-Pot 863, proved to have the required combination of properties (resistivity = $10^{14} \Omega$ -cm, CTE = $34*10^{-6}$ /°C, as compared to $2.6*10^{-6}$ for Si, viscosity = 2000 CPS at room temperature, and thermal conductivity = 9 BTU/(hr*ft*°C)).

A mixture was created with a 10:7 ratio by mass of resin to hardener, as recommended by the manufacturer. The epoxy was mixed by hand using wooden mixing dowels for a few minutes until visually homogenous. The epoxy mixture (5 g) was poured into the mold over the die.

A bubble in the epoxy under a metal trace may result in an open circuit and a nonfunctioning chip. During curing, bubbles can form in the epoxy at the edges of the chip or at the
PDMS surface from air introduced either during mixing the epoxy or while pouring it over the
chip. Bubbles tend to appear on the PDMS surface if the PDMS has been touched or scratched,
for example when the chip is placed onto it. At room temperature the epoxy is opaque,
preventing observation of bubble formation. A heat gun was therefore used to increase the
temperature of the epoxy so that it became transparent. Heat was applied at 30 second intervals
for 2-3 minutes. After each 30 second interval the mold was swirled to mix the epoxy to a
uniform temperature. Non-uniform heating results in improper curing, causing the epoxy to
deform as one area cures faster than others. Once the epoxy was transparent, the mold was

placed onto a 120 °C hotplate and leveled. A 20 minute period of observation was required to eliminate bubbles that formed while the epoxy mixture remained liquid. Bubbles were removed with either a needle or a wooden mixing rod, taking care not to disturb the PDMS surface. After 20 minutes the epoxy was no longer liquid and the Petri dish was moved to a 140 °C oven.

After 10 minutes in the oven, the edges of the epoxy wafer curled away from the PDMS mold. At this stage the epoxy handle wafer was removed from the mold and flipped over so that the chip surface faced up. It remained in the oven for 6 hours, following the manufacturer's instructions, to aid in curing the epoxy and to minimize degassing during later high vacuum processing; this is important during later metal deposition because a lower base pressure results in higher quality thin film characteristics. (For optimal degassing the instructions note that the temperature can be increased to 175 °C for an additional 16 hours.) The resulting cured structure is slightly curved at the edges, leading to a domed effect: the center (4 cm diameter) is essentially flat (see the Supporting Information for a profilometer scan of the center area), but the outer 0.5 cm at the rim has a high curvature. The repercussions of this are discussed below.

2.4.3 Metal Deposition

The metals (50 Å Cr and 3000 Å Au) were deposited onto the surface of the handle wafer by magnetron sputtering (AJA, 200 W DC, Ar pressure 5 mTorr). Sputter deposition is preferred over other methods because it ensures trace continuity: it conformally coats the small stress cracks, of 500 nm to 1 µm depth (see the profile in the Supporting Information), that may form in the epoxy at the edge of the chip due to differences in the coefficients of thermal expansion between the epoxy and the Si. (These cracks appear when the epoxy is cured at high temperature, as shown in Fig. 21b; when it is cured at room temperature for a period of days,

they do not form.) If non-conformal deposition methods such as thermal evaporation are used, there can be discontinuities and thus package failures. Trace continuity is shown visually in Fig. 21a. Electrical continuity between the fan-out pad and the CMOS bond pad was verified using a probe station, and sputter deposited samples never exhibited failures.

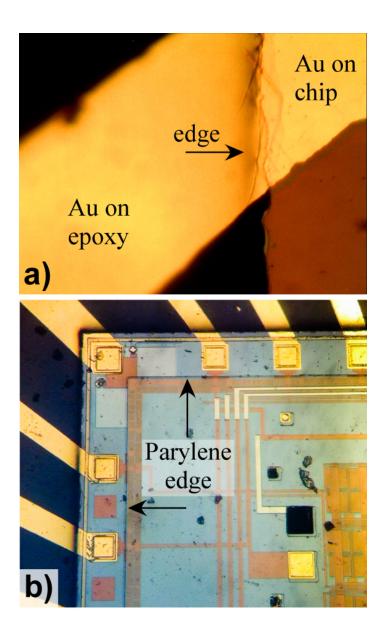


Fig. 21. a) Close-up showing continuity of the metal traces across the edge of the chip and onto the epoxy. Tiny cracks at the edge of the chip are conformally coated with metal. b) The patterened edge of the Parylene. The passivation layer lies outside the IC active area

2.4.4 Metal Patterning

The metal was patterned using contact photolithography (Karl Suss MJB-3). A high viscosity resist (AZ 9260) was applied to the surface (2000 rpm, 40 seconds) and soft-baked (90 °C, 12 minutes) on a hotplate. The resist was allowed to rehydrate for 30 minutes at room temperature at a relative humidity of 60% before exposure (400 mJ/cm²) using a printed mask (25,400 dpi, Fine Line Imaging). Since the pitch of the bond pads was 250 μm, to facilitate alignment the mask features were made to be 25 μm larger than the 75 μm bond pad width. The resist was developed (1:4 mixture of AZ 400K developer to water, 3 minutes) with continuous mild agitation. The developed resist had a height of 10 μm as determined by mechanical profilometry (Tencor P-20). This resist was consistently conformal, unlike thinner resists such as Shipley 1813. The resist was hard-baked at 145 °C for 5 minutes to enhance adhesion, following the manufacturer's instructions (since this is above the softening temperature of the resist (110 °C [103]), there is some loss in lithographic resolution). The metal was wet-etched (Transene TFE for Cr, Transene TFA for Au). The resist was removed by rinsing sequentially in acetone, methanol, isopropanol, and deionized water.

2.4.5 Passivation using Parylene

The metal traces were passivated with a 2 µm conformal coating of Parylene C (2 g of dimer, SCS Labcoter). The Parylene was patterned by oxygen plasma etching (20 minutes, 50 W, 5 mTorr, Jupiter March RIE). For a 1 µm thick film of Parylene, the initial 90% of the film etched at a constant rate, but the remaining 10% etched more slowly and often left behind a rough "grass-like" layer (not seen by optical microscopy but evident with mechanical

profilometry) that was difficult to remove, as noted previously in [104-106]. To overcome this issue a "sacrificial layer" of photoresist (10 µm, AZ9260) was patterned over the active area of the IC before Parylene coating. This allowed for a lift-off of the residual Parylene remaining after the plasma etching process, leaving behind a clean surface.

Depending on the tool and plasma conditions, the Parylene etched 1-3x faster than Shipley 1813. Thicker resists, such as AZ4620 and AZ9260 showed similar selectivity and could be used as mask layers if they were thicker than the Parylene.

The Parylene passivation layer provides a nearly flat surface onto which PDMS-based microfluidics can be bonded using plasma-based techniques [107] or, as shown below, uncured PDMS "glue". It is important to note that some CMOS chips and other devices, such as ISFETs, are sensitive to electrostatic discharge (ESD) and susceptible to damage during plasma etching [108]. Both of the ICs discussed in this work included ESD protection on their input pads, and thus did not suffer damage during etching. A bioamplifier IC that has been selectively passivated with Parylene is shown in Fig. 21b.

2.4.6 Microfluidic Integration

A PDMS microfluidic structure was bonded to the surface of a packaged chip to demonstrate microfluidic integration capability. The mold was fabricated in SU-8 on an oxidized Si wafer, giving 100 µm high features. PDMS (10:1 ratio of precursor to curing agent) was poured over the mold and placed into a vacuum desiccator for 20 minutes to remove trapped air bubbles. The mold was placed into a 50 °C oven for 2 hours to cure the PDMS.

PDMS has been reported not to bond to Parylene simply by activation of both surfaces using an oxygen plasma [107]. Therefore, following [107], uncured PDMS pre-polymer was used as a "glue" to form a moderate-strength bond. The pre-polymer was spun onto a glass slide (4000 rpm) to create a thin layer for micro-contact printing. The cured PDMS microfluidic structure was removed from the mold, pressed onto the coated glass slide to cover the bottom surface with the pre-polymer, and placed onto the packaged chip. The assembly was cured on a hotplate at (100 °C, 15 minutes). This was expected to form a bond sufficient for filling the microchannels but not the application of high pressure. It has been reported that the bond strength between PDMS and Parylene can be enhanced using plasma treatment of the assembly after bonding[107].

The channels were filled with water using a syringe, under pressure. Fig. 22 shows a close-up at one edge of the chip. The fluid filled the channels, with no leakage at any points. The self-leveling of the epoxy around the die produced negligible step heights, enabling this satisfactory bonding.

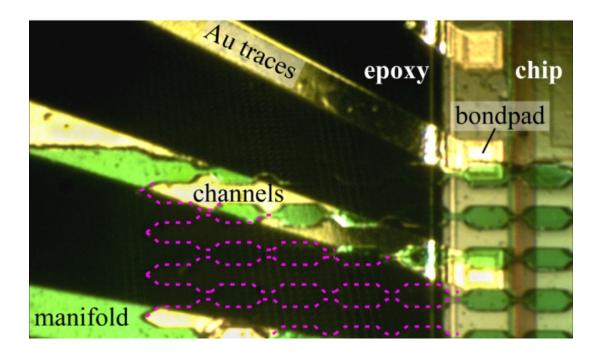


Fig. 22. A microfluidic structure bonded to the surface of a packaged chip. Green dye has been used to visualize the fluid. A manifold on the left sub-divides into parallel crenellated channels that run horizontally across the figure to the right (indicated by dashed lines in the dark region). The internal channel dimensions vary periodically from 2 μ m to 50 μ m.

During curing, the epoxy curls away from the edges of the PDMS mold, resulting in a handle wafer that is rounded at the edges, as can be observed in Fig. 20a. As noted above, the wafer is flat enough in the center for post-processing, and vacuum chucks in the spinner and mask aligner hold the handle wafer without a problem. PDMS bonding is also unaffected. However, the shape does prevent high resolution photolithography at the edges of the handle wafer: the chip at the center comes into contact with the mask, but the edges remain slightly away, decreasing the resolution. This is not an issue for fan-out, as shown in this paper, but it could pose a problem if multiple chips were packaged in the same wafer, out to the edge.

The bond strength of PDMS to Parylene is weak compared to the bonding of PDMS to glass. For higher pressure microfluidics it would be advantageous to employ an oxy-nitride stack as the passivation layer: the Si₃N₄ would meet the passivation requirements while the top layer of SiO₂ would bond strongly to the PDMS. The oxy-nitride stack can be deposited conformally on the epoxy handle wafer using low temperature (200 °C) plasma-enhanced chemical vapor deposition (PECVD). (The epoxy can withstand a temperature of 340 °C [109]). One disadvantage of using oxy-nitride, however, is that it would require additional steps for patterning because the etch procedure would also attack the passivation layer used in the CMOS process.

The packaging method presented here results in a yield of 100% if the die has been properly encapsulated by the epoxy. Errors made in later processing steps can be remedied by removing the material and redoing the step.

2.5 Packaging Results

The general utility of the packaging method was demonstrated by showing proper electrical functionality of two different CMOS sensor ICs. The ICs were fabricated using the same commercial 0.35 µm CMOS process through MOSIS. Both were designed using a 40 bond pad configuration with redundant dual power supply connections. (This connection is critical to chip function; without a backup, a discontinuous trace to a power supply pad would be fatal.) The die area for both ICs was 3 mm x 3 mm. The fan-out masks for both chips were the same and they shared similar instrumentation for data acquisition and connection to a PC.

2.5.1 Instrumentation

A PCB was designed to form connections between the handle wafer and a data acquisition card. (A photograph is shown in the Supporting Information.) The PCB had two parts: a daughter board that contacted the package using vertical spring-loaded Au-coated pins and a motherboard with headers for connection to the data acquisition system. The daughter board was mounted on a clamp to simultaneously contact all of the pads on the handle wafer. The PCB included two 1.5 V batteries as a low-noise power supply and two shunt capacitors to compensate for transients in power draw.

A National Instruments high-speed USB DAQ was used with a PC running MATLAB code for data acquisition. Sampling rates ranged from 10 kHz to 40 kHz.

2.5.2 Electrical Recordings from Cardiomyocytes

To test the functionality of the package, we utilized a large clump of cardiomyocytes cultured on a chip that detected spatial differences in potentials. Such clumps visibly beat, so the occurrence of signals and their timing was known and could be correlated with data obtained from the chip. In addition to the generation of electrical signals and beating, viability of the cells was confirmed by their continuous spreading over the surface (images are included in the Supporting Information).

2.5.3 Bioamplifier IC

The bioamplifier is an integrated circuit for amplification of extracellular potentials. A total of 22 differential amplifiers and a large reference electrode were included in the IC. The design was based on [50], in which a capacitor ratio was used to set the gain and bandpass of the amplifiers. This configuration was chosen because of its inherent low noise and DC rejection capabilities. Small PEDOT-coated recording electrodes (Fig. 20b, Fig. 23a) provided the differential inputs to the amplifiers. The electrode area under the glass cuts was 40 µm x 40 µm.

2.5.4 PEDOT Deposition

It has been shown that films of the conjugated polymer PEDOT:PSS decrease interfacial impedance at 1 kHz by over an order of magnitude compared with other common electrode coatings like Ir [110]. Conjugated polymers are both electrically and ionically conducting. Our own impedance spectroscopy showed that it decreased the impedance by nearly 2 orders of magnitude when compared to uncoated Au electrodes (see the Supporting Information for details).

PEDOT was selectively deposited by masking areas of the IC with photoresist. After the Cr/Au sputter coating step (section 2.4.3), Shipley 1813 resist was applied (3000 rpm, 30 seconds) and soft-baked (60 seconds, 90 °C). The resist was exposed (8 mW/cm² dose, 15 seconds) and developed (Shipley 352, 30 seconds), opening the areas to be coated. The polymer was electrodeposited galvanostatically (2 mA/cm²) onto the exposed electrodes on the IC surface from an aqueous solution of 0.01 M EDOT (Sigma 483028) and 2.5 mg/mL PSS (Sigma 243051). After PEDOT deposition the resist layer was stripped (acetone). Impedance

measurements of PEDOT immediately following deposition and after further processing showed no significant change in conductivity.

2.5.5 Fluid Well

A well to contain fluid for cell culture was added to the surface of the packaged chip. The well was formed from a 15 mL centrifuge tube cut 15 mm from the top opening to preserve the screw threads on the cylinder so that the original cap could be used to close the well. The well was glued to the surface of the chip using a biocompatible quick-setting silicone elastomer (Kwik-Cast Sealant, World Precision Instruments). The well could hold over 500 μ L of fluid, but normally media volumes ranged between 200 μ L and 300 μ L.

2.5.6 Cell Culture and Plating

Human induced pluripotent stem cell (IPSC) derived cardiomyocytes and supporting cells, consisting of clumps of approximately 10,000 cells (ReproCell) were plated onto the surface of the IC. The cells were shipped at slightly below room temperature. The plating procedure, provided by the supplier, consisted of centrifuging the cell clusters to collect them at the bottom of the tube, removing the supernatant, re-suspending the clusters in plating medium (ReproCardio Culture Medium, ReproCell), and transferring the cell clumps by pipette to the plating surface. Such clumps of cells generate large signals and are easily positioned manually. (For sparse cultures it is possible to increase the SNR by positioning the cells over the sensing sites, for example using dielectrophoresis, as demonstrated in [111].)

Experiments were performed using a packaged chip that had previously been used for long term cell culture and had been exposed to cells in media continuously for a period of 15 weeks. Prior to plating the cardiomyocytes, the packaged IC was cleaned, sterilized, and incubated overnight in cell medium (Roswell Park Memorial Institute (RPMI), Gibco 21875034) with 10% B27 supplement (Gibco 17504-044). On the day of plating, the RPMI/B27 solution was removed and replaced with 200 μL of an adhesion promoter (ReproCoat, ReproCell) and incubated for 2 hours in standard cell culture conditions (37 °C, 5% CO₂ air mixture, 100% humidity). The adhesion promoter solution was removed by aspiration, and a clump of cells was plated on top of the active portion of the IC. The clumps were beating before and after plating. To the well, 200 uL ReproCardio medium was added, and the packaged IC was incubated overnight in standard conditions.

2.5.7 Cell Recordings

The cells were allowed to settle for 24 hours, at which time they were visually observed to be still beating. An image of the cell clump (dark mass) after 24 hours is shown in Fig. 23a, where a light-field microscope image is overlaid onto the CAD schematic of the layout of the bioamplifier IC.

Electrical recordings are shown in Fig. 23b-d. Recordings were simultaneously collected from all 22 channels of the bioamplifier IC; a collection of representative traces is shown in Fig. 23b. Each trace is the output signal from one of five amplifiers, each connected to a separate pair of recording electrodes on the surface of the bioamplifier IC. The action potentials coincided with the "heartbeats" of the clump (a video in the Supporting Information shows the beating). No spikes were recorded in the absence of cells. The data show that the chip is

electrically functional after packaging, post-processing, and long-term exposure to the fluid medium. Fig. 23b shows that the signal amplitude decreased with sensing electrode distance from the clump, as it should. Fig. 23c shows a trace from a single channel recorded at higher temporal and voltage resolution than Fig. 23b. Fig. 23d shows the longer duration spike train from which Fig. 23c was taken. (These are unfiltered, raw data, showing the DC rejection capability of the chip.)

Recordings were made over a period of two days, with the packaged IC and cells being kept in the incubator between recordings. The cell clumps remained active for over 21 days; the lateral dimensions of the primary cell clump increased, and networks of interconnected cells formed around its periphery (see the Supporting Information). Testing of various packaged devices showed that they were fully functional with no degradation in performance after a period of 15 weeks in the incubator with cell medium on the surface. Since using a large well meant that the saline solution covered the entire surface of the chip, these tests of the passivation integrity were more stringent than if microfluidics had been used to expose localized areas. Similarly packaged bioamplifier chips have also been used to collect data from cortical neurons, and those have been cleaned and re-used multiple times.

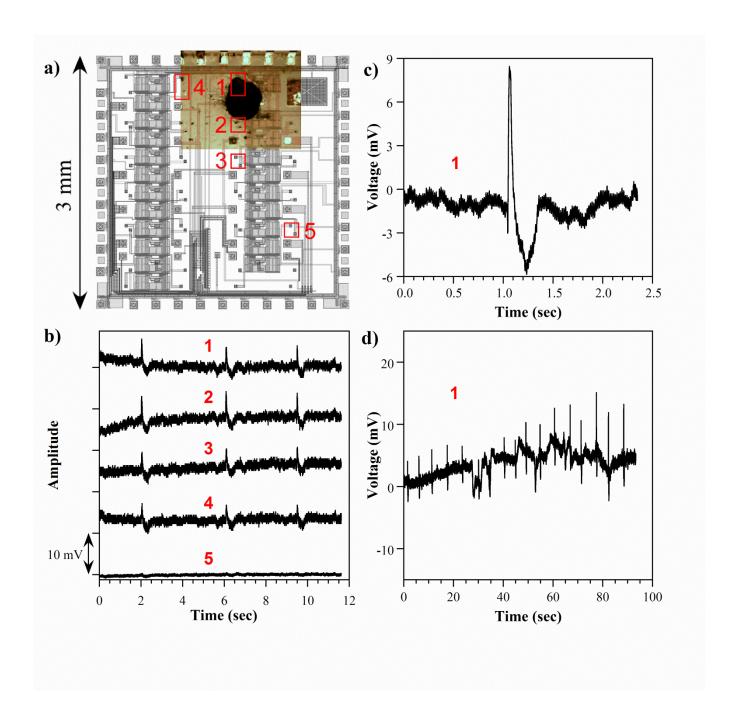


Fig. 23. a) An image of the cell clump overlaid on the layout of the IC. Some of the differential electrode pairs are outlined with red rectangles. b) Recordings from the six electrodes labeled in (a) over a period of 12 seconds. c) A single action potential from the cell clump at electrode 1, recorded with high resolution. d) Longer duration recording showing discernible spiking activity.

2.5.8 Cell Adhesion Monitoring using a Capacitance Sensor

Package functionality was also demonstrated with a CMOS capacitance sensor IC, designed to measure capacitance changes on the chip surface. This type of chip has previously been used to characterize cell health and adhesion [112]. Unlike the bioamplifier chip, this chip had digital addressing (allowing multiplexing of the many sensors to a smaller number of output channels) and a higher slew rate (> 0.1 V/μsec). One question about the package, which could be answered with this experiment, was whether it would burden the limited driving capability of a low-power chip. Measurements were made with just cell media and after cells were plated, which leads to a change in capacitance.

2.5.8.a Capacitance Sensor IC

The IC, described in [112], consisted of an 8x16 array of differential capacitance sensors. Each of the 8 columns shared a single evaluation structure, and row readout was selected using a digital addressing scheme. The sensing electrodes were interdigitated with reference electrodes. The IC measured capacitance by integrating current onto the sensing electrodes for a fixed period of time and reading out the resultant voltage; changes in the effective dielectric constant between the electrodes, due to cells or media, resulted in changes in the capacitance.

2.5.8.b Chip Packaging and Preparation

Two capacitance chips were packaged using the same method as described for the bioamplifier chip but omitting the PEDOT deposition and patterning. A well was attached to the surface of the packaged IC as described in section 2.5.5, and 500 μ L of cell medium was added to the well. The chip was incubated overnight in standard cell culture conditions.

2.5.8.c Cell Culture and Measurements

Epithelial kidney cells from *Cercopithecus aethiops* were purchased in frozen form (ATCC CCL-26). Following the supplier's instructions, the cells were thawed, centrifuged, and re-suspended in cell media; they were then plated onto the surface of the capacitance chip. The first set of measurements were taken before the cells were introduced, and the second after they had been allowed to settle for one day (approximately 60% confluency). The output voltage from three capacitance sensing sites is shown in Fig. 24.

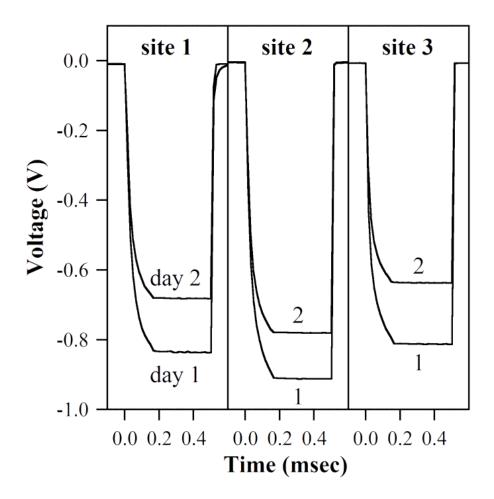


Fig. 24. Raw data from the capacitance sensing chip. Measurements were taken before cells were plated (day 1) and after cells adhered to the chip surface (day 2). The sensor starts out in a reset state ($V \approx 0$). At t = 0, a known current is fed onto the interdigitated electrodes for a fixed period of time, after which the resulting voltage is held and sampled. The output voltage at each site is proportional to the effective capacitance.

Both of the capacitance chips were found to function as expected electrically: the voltage increased at each site after the cells adhered, corresponding to an increase in the sensed capacitance. These data were compared to data collected from chips supplied from the foundry in dual in-line packages (DIP). The output slew rate was comparable, indicating that the package did not present a significant capacitive load to the circuits on the chip.

2.5.9 Discussion: CMOS Packaging

Packaging of mm-sized CMOS dies in LOCs has been challenging, and the lack of good solutions has hindered progress in system miniaturization. A number of methods for packaging CMOS dies for LOC systems have been presented in the literature. Fig. 25 illustrates the range of methods, including the most prominent ones and some unique approaches, but the figure is not exhaustive. These approaches vary substantially, raising the question of how they can be evaluated and compared. In Table. 1 the prior work is contrasted utilizing some metrics that have previously been proposed and also a few new ones introduced here that can be almost universally applied. The metrics comprise two dimensions and a ratio, as illustrated in Fig. 26, as well as a fabrication metric – yield – and a performance metric – lifetime. (Since yield is rarely reported, in Table. 1 it is assessed indirectly through the number of fabrication steps.)

Regardless of the approach, the first step in processing tiny foundry-produced dies to create CMOS-based microsystems is fixing them to a carrier so that they can be handled. That can be a wafer (silicon or another material), a standard chip package, a printed circuit board, or a flexible substrate.

When discussing the packaging requirements for an integrated CMOS LOC system, it is convenient to define two separate regions of the chip: the first is the "active" area, which must interface with the liquid environment to perform sensing, and the second is the input/output (I/O) region of the chip, which must be passivated to isolate it from the fluid [91, 113]. (The circuits within the chip are protected by an insulating layer on the surface, typically oxide, nitride, or a polymer. Connections between the sensors and the I/O pads are made internally, by metal routing layers.) The passivation material must therefore be patternable in some way to

selectively expose the active area(s) of the die. For full integration, the packaging should permit later surface micromachining and addition of microfluidics.

On CMOS dies with large area C (Fig. 26) it is easier to separate the active and I/O regions [113], as discussed below. However, given that the price of a CMOS chip scales with its area and that it may be the most expensive component of the integrated LOC system [85], it is advantageous to use smaller dies. (For small-volume orders, a modern 5-metal, 2-poly CMOS process costs \$60-\$300 per mm², with average prices of \$1000 each for 5 mm x 5mm die and a minimum lot size of 40, which is prohibitive for research applications. Prices for chips are low (pennies) only for mass production.) On the other hand, as previously mentioned, small die present difficulties in handling and processing. For example, they are too small for standard microfabrication equipment such as resist spinners and mask aligners, and photoresist edge beads can cover the entire chip [114-116].

The chip area *C* determines how far the I/O regions can be separated from the active region, i.e. the barrier distance *B*. If *B* can be made large, isolation becomes simple: glue a well onto the surface for containing the fluid and use wire bonding to the bond pads that lie outside of that to connect the IC to either a printed circuit board (PCB) or a chip carrier (Fig. 25a)[86]. With that popular approach, the adhesive occupies considerable area. A conceptually similar method employed a glass slide with microfluidic channels bonded to the chip surface between the bond wires (Fig. 25b)[14].

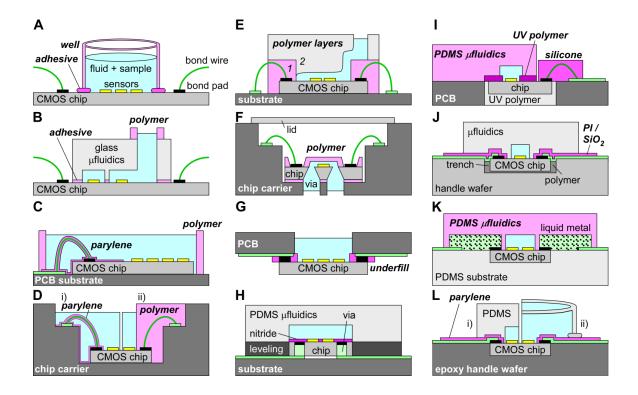


Fig. 25. Predominant and recent packaging techniques for CMOS LOC systems. The critical fluid barriers are indicated in pink; the materials for which vary by system. The protected external electrical connections are shown in green. A) A large die with a well to contain fluid glued between the active and I/O regions [86]. B) A large chip bonded between two I/O regions to a glass cap with etched microfluidic channels [14]. C) A die wire-bonded to a PCB and selectively passivated with Parylene surrounded by a well [108]. D) A small die wire bonded to a standard chip carrier i) selectively passivated with Parylene, the chip carrier acting as a well [114] or ii) with a polymer forming both the passivation layer and well [66, 113, 117]. E) Wire bonds encapsulated in a first layer of polymer, surmounted by a second layer of polymer having a microfluidic channel formed using a sacrificial ink [17] or plastic thread [89]. F) A die with fluid vias etched through it surmounted by a polymer fluidic layer, mounted to a chip carrier also having fluid vias; a lid protects he wire bonds [118] G). A flip-chip packaged die with the printed circuit board serving as the well and a polymer underfill protecting the electrical connections [94, 119]. TAB packaging is similar [120]. H) This approach is still conceptual for LOC applications. A die with metal-plated through-holes connecting to the I/O metal of the chip from the back, surrounded by a leveling layer; the I/O pads are not exposed to the fluid by a glass cut but remain under the chip passivation layer, allowing the entire chip surface to be immersed. I) A "chip in hole" approach. A chip inside a hole formed within a PCB, made level with the top surface using a UV-curable polymer. Additional UV polymer is patterned on the front surface as a fluid barrier and bonded to PDMS microfluidics. The wirebonds are further encapsulated with PDMS [121]. J) A second "chip in hole" approach. A die adhered to the bottom of a cavity in a handle wafer, the gap between the chip and the handle wafer filled with a polymer, and thin film metal I/O leads patterned onto the surface and passivated with polyimide and silicon dioxide. Microfluidics are fabricated on the surface using either PDMS or SU8 [85, 102]. K) A die encapsulated within a PDMS substrate surmounted by a second PDMS slab with microchannels for containing fluid. Electrical connections to the bond pads are made using a liquid metal alloy contained within additional microfluidic channels [88]. L) This work. A chip encapsulated within an epoxy substrate with thin film metal I/O leads patterned onto the surface and passivated with Parylene. Fluid can be contained within either i) microfluidic channels or ii) a well.

Table 1. Evaluation of the packaging methods that have been used for integrating CMOS chips with microfluidics. Each of the packaging methods in Fig. 25 is represented except for those not done using active chips or that remain theoretical. Entries were inferred or estimated (indicated by *) whenever possible from the available information if they were not given explicitly in the paper. Codes: --= not reported, *= estimated, †= not estimated, BP = before packaging, BW/C = bond wire / chip height, F = flip-chip, H = high, L = low, NA = not applicable, TAB = tape automated bonding, TF = thin film, W = wire-bonded.

Reference	Type (Fig. 25)	Chip Size (mm)	Bonding Method	Sensor	Fluid Barrier Material	Area Efficiency*, η	Lifetime (days)	Barrier Distance (μm) *	Number of Steps	Vertical Step Height, <i>h</i> (μm)	Post- Processing Possible?	Microfluidics Integrated
[86]	A	large**	W	magnetic	PDMS/plastic	L	<u>≥</u> 10	<u>< 400</u>	<u>></u> 4*	Н	N	N
[14]***	В	5 x 47	W	optical	SiO ₂	Н		<u>≥</u> 500	<u>></u> 9	NA	BP	Y
[108]	С	NR	W	ISFET	Parylene	Н	H*	< 100	4*	300*	N	N
[66]	D	4.4 x 4.4	W	electrical	epoxy & PDMS	L	<u>≥</u> 28	> 1000	<u>≥</u> 6*	Н	BP	N
[67]	D	6.5 x 6.5	W	electrical	epoxy & PDMS	L	≥ 56	> 1000	≥ 6*	Н	BP	N
[114]	D	3 x 3	W	electrochemical	Parylene	Н	H*		≥ 6*	BW/C	N	N
[113]	D	3.2 x 3.2	W	electrical	Silastic 9161 RTV	Н	<u>≥</u> 14	≥ 200	<u>≥</u> 8*	Н	BP	Y
[113]	D	3.2 x 3.2	W	electrical	Hysol CB064	Н	<u>≥</u> 14	≥ 200	> 8*	Н	BP	Y
[122]	D	5.2 x 6.5	W	electrical	epoxy	L	<u>≥</u> 1	≥ 1000	<u>></u> 4*	Н	BP	N
[87]	Е	2 x 5	W	magnetic & temperature	SU-8	L		> 1000	<u>≥</u> 6*	low*	Y	Y
[89]	Е	1 x 2.4	W	optical	epoxy & PDMS	Н	L*	<u>≥</u> 400	<u>></u> 4*	BW/C	N	Y
[17]	Е	1 x 2*	W	capacitive	epoxy	L		NA	≥ 5 *	BW/C	N	Y
[81]	Е	1 x 4	W	magnetic	polyimide	L		≥ 1000	<u>></u> 7	BW/C	N	Y
[81]	Е	2 x 5	W	magnetic	SU-8	L		≥ 1000	<u>≥</u> 6	BW/C	N	Y
[94]	G	8 x 8	F	electrical	NR	25% [†]		<u>≤</u> 2000	<u>≥</u> 3	Н	N	N
[119]	G	NR	F	magnetic (Hall effect)	epoxy	L		≥ 500	<u>≥</u> 5*	120	N	Y
[89]	G	1 x 2.4	F	optical	glass	Н	H*	NA	≥ 5*	75	N	Y
[120]	G	1.3 x 2.2	TAB	ISFET	polyimide	L		< 150	≥ 5*	<u>≥</u> 50	N	N
[121]	I	3 x 3	W	ISFET	Ebecryl 600	L		<u>≥</u> 800	<u>≥</u> 6	L	Y	Y
[85]	J	2 x 2.3	TF	electrochemical	polyimide/SiO ₂	Н		< 200	<u>≥</u> 8*	2	Y	Y
[102]	J	1.6 x 1.8	TF	electrochemical	oxide & nitride	Н		NA	<u>≥</u> 7	<u>≤</u> 3	Y	Y
[88]	K	1.5 x 1.5	Galinstan	magnetic	PDMS	Н		<u><</u> 200	≥ 5*	L	N	Y
this work	L	3 x 3	TF	electrical	Parylene	84%	> 90	25	3	<u>≤</u> 1	Y	Y

^{**} Chip was diced larger than CMOS area. *** Not CMOS.

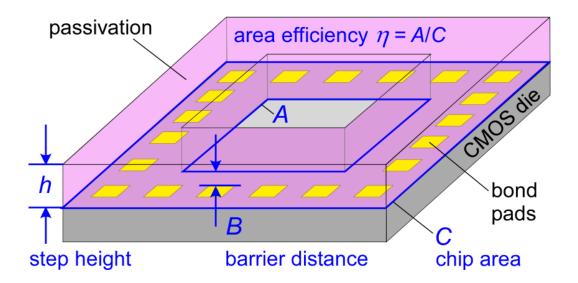


Fig. 26. Generalized features of a package for a CMOS die illustrating key dimensional metrics. Bond pads (yellow) and the electrical connections from there to the substrate or carrier (not shown) at the chip periphery are covered by a barrier layer (pink) to prevent contact with the fluid (not shown) over the center area.

Alternatively, for large *B* flip-chip packaging is also possible [94, 119], if the equipment is available. The chip is bump-bonded to metal traces on a substrate having a window for fluid containment, and the area between the bonds is filled with a waterproof adhesive for passivation (Fig. 25g). A large *B* is required if the passivation material is applied manually or if it wicks into the active area. Tape automated bonding (TAB) is similar to flip-chip packaging. In the TAB process, the bond pads of the CMOS die are bonded with solder balls to patterned conductive traces on a polymer tape that "fan out" the connections to other circuits or external connections. TAB was briefly used in packaging chemical and ion-sensitive field effect

transistor (CHEMFET and ISFET) chips [120], but it was abandoned because encapsulation failed during long term exposure to ionic fluids [123].

Because chip area is expensive it should be utilized efficiently, as characterized by η , the ratio of the active area to the total area. A large B reduces η . The width that must be passivated at the edge of the chip is more or less constant, since bond pads range from 60 µm to 100 µm on a side. Therefore, a high η can be achieved (at commensurate expense) with a large chip having a large active area A, which renders the I/O region relatively narrow in comparison. With small chips, however, high area efficiency must be achieved by minimizing the barrier distance B through the use of a precisely patternable passivation material. For wire-bonded chips, passivation has been done with Parylene (Fig. 25c,d) [108, 114], which can be patterned directly by laser ablation or photolithographically by defining a mask and dry etching in oxygen plasma. Other advantages of using Parylene to coat the bond wires and pads are that it applies no mechanical stress, is pinhole-free and conformal, and has negligible water absorption [124]. Another approach to minimizing B is to form a well in a thick polymer (Fig. 25dii), which can be done in a couple of ways. After bonding, the chip carrier can be filled to the top with a photocurable precursor, exposed photolithographically, and developed [117]. With the right material, this method can give the required high-aspect-ratio structure with excellent alignment. However, swelling of the photocurable polymer by cell medium or by ethanol is an issue, and leads to bond wire delamination [117]. Alternatively, a physical post can be placed over the active area and a polymer cured around it, followed by removing the post [113, 114]. This permits a wider range

of passivation material choices, including epoxies that have minimal shrinkage and water absorption, but aligning and fixing the post in place (without damaging the surface but still preventing seepage underneath) are challenging. A variation of this method involves an SU-8 "dam" in the form of a ring between the active and I/O regions, which can prevent a low-swelling epoxy applied over the wire bonds from encroaching into the active area [125]. This is tricky because the surface energies and viscosity must be just right, and bond wire failures remain a problem [117].

The step height *h* between the die surface and the top of the package impacts the ability to post-process the die – to fabricate structures and devices on the surface or add microfluidics, for example by bonding molded polydimethylsiloxane (PDMS) to the chip. Non-planarity is greatest when industry-standard wire bonding is employed since the wires rise hundreds of µm above the surface of the die. If *h* is large, then post-processing must be done before or during the packaging process. For example, in Fig. 25e [17] the wire bonds were protected by a first layer of epoxy, a sacrificial layer was drawn by 3D printing over that and down to the sensors, a second layer of epoxy was added, and the sacrificial layer was removed to form microfluidic channels. In another case (Fig. 25f), microfluidics were added to a wire-bonded chip by laminating a free-standing plastic film containing micro-channels and a cut-out to the front, and wire bonding through the cut-outs. Fluidic connections were made from the back of the chip by means of etched vias. Fluid vias consume significant chip area, thus sacrificing computing performance and device density.

Only those packages in which chips are embedded within a handle wafer (Fig. 25i-l) have a small enough vertical step h to allow photolithography, and thus the integration of more than microfluidics, after packaging. Electrical connections can be made using patterned thin metal films if the surface is sufficiently flat for electrical continuity (Fig. 25j [85, 102] and Fig. 25*l* (this work)). This requires that trench and step formation around the IC be minimized. (Steps and gaps hinder uniform application of photoresist, which can result in discontinuities in thin film electrical traces used for I/O connections.) For example, in "chip in hole" processes [85, 102, 117], in which the IC is placed into a pre-formed hole within a handle substrate, mismatch between sizes of the IC and cavity can lead to uneven surface topography, so particular care must be taken to fill the gaps and level the chip [102]. Alternatively, electrical connections can be made using liquid-metal-filled microchannels (Fig. 25k) [88], which have less stringent flatness requirements. This package is quite similar to the one presented in this work, but uses a PDMS handle wafer. It thereby offers the advantage of mechanical flexibility, but has the drawback of presenting challenges during microfabrication due to swelling upon solvent absorption [126]. One could in principle also use metal-filled vias from the back of the chip (Fig. 25h), such as used in packaging optical CMOS sensors [127]. In the latter package, there is no significant increase in chip area because no holes are required through the interior circuit layers, just down from the bond pads at the periphery.

Post-processing is limited by the temperatures that the packaged chip can withstand. The CMOS chip itself has a limit of approximately 450 °C [128, 129], but the polymers employed in

the package may lower that considerably: Parylene has a melting temperature T_m of 290 °C [130, 131], and PDMS should be kept below 343 °C [132] and SU8 below 200 °C [133]. The epoxy used in this work has a T_m of 340 °C [109].

Fabrication through shared run services can yield as few as 5 dies, and the time lag between submitting the design and receiving the chips is usually 3 months. Because the IC is precious and cannot easily be replaced, high packaging yield is critical. The yield depends on the number of processing steps n since every step introduces additional opportunities for failure [134]: yield $\sim f^n$ where f is the yield for each step (assumed identical for all steps for purposes of this discussion). The yield is not usually reported, but n can serve as an indirect metric that can be obtained from a description of the fabrication process. A more complex fabrication process may, however, still provide a net benefit by permitting the design to incorporate elements that increase package durability. Illustrating this trade-off, two packages in Table. 1 that required 6 or more fabrication steps demonstrated long lifetimes [66, 67]. In this work, two masks were required for packaging.

The ability to package several dies at once would lead to material and time savings, but this has not yet been demonstrated. Packages that employ wire or bump-bonding (Fig. 25a-h) inherently handle one chip at a time, although this can be automated. Those that embed the chip in a carrier (Fig. 25i-l) are more amenable to handling multiple dies for processing together using standard microfabrication equipment. The carrier could later be cut to individuate the

devices. One obstacle to this approach is that CMOS die vary in size: although the circuit real estate remains the same, there are variations in both chip thickness and total diced area. These variations can present significant issues for the chip-in-hole processes (also known as micromachined redistribution padframes, MRP [117]), in which the cavity size must match the size of the die. In [102], wax filled the gaps between the chip and carrier walls, and wax reflow was performed to reduce the vertical offset between the top surfaces. Fluid leakage at the trench around the chip was circumvented using open SU-8 channels and a glass cap. With the chip-in-hole approach, one can heterogeneously integrate various chips into an active substrate. Methods in which the carrier wafer is formed around the die (Fig. 25k,l) are insensitive to chip size variations, but precise positioning of multiple dies within the carrier followed by later photolithography using a single mask could be problematic; separate alignment of each die with an individual mask may be needed. Although polymeric carriers are inactive, heterogeneous integration could be achieved by incorporating other dies adjacent to the CMOS die.

Extending package lifetime is of critical importance because it increases the number and duration of experiments that can be performed, thereby conserving the limited number of chips and lowering the cost of each experiment. It also allows long-term observations and permits replicate experimental runs as well as runs under different conditions. Regrettably, lifetime often goes unreported. The barrier material plays a key role in package durability [91, 135]: it must be able to withstand extended exposure to aqueous mediums with negligible absorption and expansion, and if the LOC is to be reused it may need to survive exposure to surfactants,

solvents, bleach, autoclaving, or UV light. Materials such as PDMS, photocurable Loctite polymers, and various epoxies absorb water and swell, resulting in package failure [117]; worst of all, the failure time is unpredictable, occurring in some cases after a couple of weeks but in other cases within the first hour. One of the two long-lived packages (28 days) mentioned above used epoxy to encapsulate the bond wires and PDMS to keep the water away from the epoxy [66], and the second (56 days) encapsulated the bond wires with a water-resistant medical epoxy (EPOTEK 302-3M)[67]; the chips in both cases were somewhat large (4.4 and 6.5 mm/side, respectively). Materials such as Parylene and nitride provide good resistance to solvents and saline solutions, and they adhere strongly to Si, oxides, and epoxy.

For chips on which cells are cultivated in an incubator, another consideration, separate from the packaging method, is the next layer of electronics and the connections to it. Cables and connectors to the package must be able to go into the incubator, and so must be sterilizable and impervious to high humidity. Likewise, if the chip is mounted directly to a PCB, the PCB must be designed for use in that atmosphere.

We conclude by evaluating the packaging method presented here by the above metrics. The approach was developed for CMOS tiny chips, but would work with any size chip. The area efficiency is high (η = 83.8%) because the passivation layer falls entirely outside the IC guard rings. The choice of Parylene (or a nitride-oxide stack) as the passivation material and the ability to pattern the passivation layer photolithographically allows a barrier distance of just 25 μ m,

which could possibly be made even smaller. The vertical step is less than 1 μ m, amongst the lowest values reported, while the lifetime is one of the longest reported. Moreover, this method requires very few microfabrication steps (3). This approach therefore has significant advantages.

2.5.10 Conclusions

The CMOS tiny chip packaging method reported here allows post-processing by conventional surface micromachining, contact with liquid samples, and integration with PDMS microfluidics. It is relatively simple, requiring only two masks, resulting in high yield, good lifetime, and excellent robustness. The key to this approach was utilizing an epoxy with the right characteristics to form an encapsulating wafer around the die that is impervious to solvents, etchants, and other solutions and to which materials such as Al, Cr, and Parylene adhere strongly. The wafers are therefore microfabrication-compatible, a key advantage. Most importantly, the epoxy forms a flat surface around the chip with a minimal trench at the chip edge, allowing electrical continuity of metal traces and later straightforward bonding to PDMS microchannels. Because the wafer is formed around the die, dies of any size or type can be packaged: the process is vertically self-aligning and insensitive to variations in dimensions. This method also opens the possibility of integrating multiple chips in one handle wafer or integration of passive components such as resistors, capacitors, and inductors, which typically occupy large areas of valuable silicon real estate.

The utility of the packaging method was demonstrated with a bioamplifier chip and a capacitance sensor chip. Exposing the packaged chips to saline solution at 37 °C for a period of nearly 4 months produced no detrimental effects on electrical performance. The packaged chips were exposed to cleaning and sterilizing agents without harm (acetone, methanol, isopropanol, ethanol, bleach, commercial enzymatic cleaning solution, and UV light). Because the chips could be cleaned and reused, each one supported repeated experiments.

2.5.11 Supporting Information

The supporting information includes images of long term cell culture on the surface of the chip, a profilometer scan showing the step between the Si and epoxy after curing, details of the fabrication procedure, the PCB used for data acquisition, different types of cells plated on both the bioamplifier IC and the capacitance sensor IC, a plot showing impedance spectroscopy of PEDOT-coated electrodes, and detail regarding the metrics used in Table. 1. Also included is a video of the heart cell clump beating on the surface of the chip.

2.5.12 Acknowledgments

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Chapter. 3

Considerations for Heterogeneous

Integration

3.1 Preface

This chapter is a reproduction of a manuscript that has been submitted to IEEE Transactions on Biomedical Circuits and Systems, an article with multiple authors. My own contributions to this work include the development of the multi-step iterative cross-domain simulation method, all of the simulations, and most of the writing.

3.2 Abstract

CMOS chips are increasingly used for direct sensing and interfacing with fluidic and biological systems. While many biosensing systems have successfully combined CMOS chips for readout and signal processing with passive sensing arrays, systems that co-locate sensing with active circuits offer significant advantages in size and performance while increasing the complexity of multi-domain design and heterogeneous integration. This emerging class of biointegrated circuits (bio-ICs) poses distinct and vexing technical challenges that arise from the

disparate requirements of biosensors and integrated circuits. Modeling these systems has to address not only circuit design but also physical structures on the surface of the IC and the behavior of biological components. Existing tools do not support the cross-domain simulation of heterogeneous bio-IC systems, and we recommend a two-step modeling approach to overcome the lack of multi-domain modeling tools: using SPICE simulation to inform physics-based FEM simulation, and vice versa, in an iterative fashion to satisfy design requirements. We review the primary implementation challenges for bio-ICs and discuss practical approaches to overcome them. These effects include new versions of many classical challenges in system-on-chip integration, such as thermal effects, floor-planning, and signal coupling, as well as new challenges that are specifically attributable to biological and fluidic domains, such as electrochemical effects and packaging. We describe these effects as they arise in bio-ICs and discuss solutions that have been experimentally demonstrated.

3.3 Introduction

Incorporating CMOS chips for direct sensing and interfacing in fluidic or biological systems introduces a number of constraints and associated technical challenges spanning the fields of integrated circuits, microelectromechanical systems (MEMS), and biosensors. While some, such as interference and coupling between different signals, power limitations, mixed-signal processing, communications interfaces, and floor-planning, are familiar in system-on-chip design, a number of unique challenges arise from the fluidic and biological domains. In this

paper we discuss the front to back process of designing such a system and review some of the solutions that have been presented in the literature as well as our own experiences. First we discuss the design from the perspective of the circuits. Next we discuss packaging the CMOS integrated circuit (IC) for use in a fluidic environment. Finally we review considerations for successful cell culture on the chip surface. The three distinct areas are inseparably interrelated in this application.

3.4 System Design and Modeling

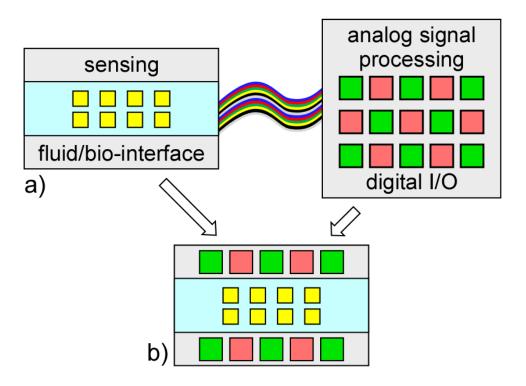


Fig. 27.) A two chip remote computation solution. The CMOS IC is connected to a second chip that has the sensing sites and interfaces with the fluid/biology. b) A single chip solution, a CMOS IC with integrated sensing sites, designed and packaged to operate with a direct fluidic interface.

3.4.1 Local versus Remote Computation

"Bio-IC" systems fall into two broad categories, as indicated schematically in Fig. 27. These categories are distinguished by whether the sensing and the signal processing are colocated or separate, a decision that occurs early in the design. In the first, an interface chip (not necessarily CMOS) accommodating the sensors is the only part that touches the fluid or biological system. It is connected to one or more ICs that perform signal processing and computation. In the second category are CMOS chips that include both the sensors and the circuitry. There are distinct advantages to both approaches.

3.4.2 Remote Computation, a Multi-Chip Solution

Multi-chip solutions are generally easier to implement and less costly than single chip solutions (Fig. 28). This approach allows the use of widely available sensing and packaging technologies as well as commercially available components, resulting in designs that are more modular in nature.

There are many examples of successful 2-chip systems. For example many neural amplifiers are implemented using a 2-chip configuration [50, 72, 73]. In a 2-chip system an IC designer can rely on well-known design and validation methods, and the biological interface chip can be realized independently, with an agreement between designers on the number of wires

needed to connect the two chips. In addition, the electronics can be readily and rapidly tested with other biological interfaces, either custom-made or commercially available.

The size of the IC is defined by the necessary circuits, and there are no inherent limits on the size and shape of the passive chip. This allows the cost of the IC to be minimized. Using a second non-CMOS chip also permits passive electrical components to be placed off of the expensive CMOS chip, for example using an integrated passive device (IPD) process, allowing higher circuit density, but at the cost of adding input/output (I/O) pads. The passive chip can be as large as needed to accommodate fluidics (as discussed in 3.5.4. At the same time, the size, form factor, and material of the second chip can be optimized for the biological application. For example, neural probes must be long, thin, and flexible. The most important advantage to using more than one chip is reduced system complexity: there are a lot of demands on a single chip solution, as will be discussed.

One disadvantage of placing active circuits away from the sensors (2-chip systems) is that sensing density is limited by the availability of input-output connections. Sensing sites are typically connected to off-chip active circuits using wires, leading to a 1:1 mapping between sensing sites and dedicated CMOS bond-pads in the case of completely passive sensors. Another disadvantage is the opportunity for noise to enter the measurements. Clearly, unshielded wires between the sensors and electronics can result in strong interference from ambient electromagnetic (EM) radiation (e.g. power supplies [50]). Even with shielded wires, the wire

length should be minimized. For a single-chip approach, noise can be reduced by actively buffering weak signals.

3.4.3 Heterogeneous Integration, a 1-Chip Approach

There are also numerous examples of successful integrated systems designed for direct interaction with biology or fluidic systems, such as neural amplifiers [67, 94, 122], magnetic sensors [86, 88], and optical sensors [14, 89]. The main reasons for combining CMOS with MEMS surface structures and fluidics are: weak signals, sensing that requires active circuits, small size/footprint, applications where wires are not possible, additional functionality, and increased density of sensing sites.

A significant motivation for creating an integrated system is the minimization of electrical noise and parasitics. Most single-chip solutions for neural amplifiers exhibit exceptional signal clarity with high SNR. Sensing modalities that utilize inherently passive devices, such as optical sensors or magnetic sensors, produce weak signals that suffer from interference or attenuation due to parasitic loading if connected by wire to a remote chip. These types of sensors benefit from close integration with signal conditioning and readout electronics, and perhaps computation.

Some sensing mechanisms inherently require close integration with active circuits.

Examples includes active pixel sensors [136] and charge-based capacitance measurement

approaches [137]. In other cases the quality of sensing can be enhanced through close integration of sensors and circuits. One method for improving the detection of very weak light, such as bioluminescence [138], is to minimize optical loss and maximize geometrical collection efficiency by placing the sample volume and optical detectors as close as possible to each other [98].

Some applications, such as micro-robotics and implantable devices, are highly sensitive to size and power requirements associated with sensing. In applications that operate under extreme resource constraints, it is necessary to integrate sensing together with circuitry in order to minimize the footprint associated with sensing. Two chips take more space than one. In a similar vein, we anticipate the development of future applications in which it is simply not possible to establish connections from the sensing region to the outside world using wires. In such applications, sensors can be integrated closely with circuitry in order to provide power transfer and establish communications in order to enable functionality in the absence of wiring.

CMOS circuits from the foundry can be modified using post-processing to add sensing domains. Intermediate structures, between the IC and the sample, can transduce physical phenomenon beyond those sensed by CMOS alone, such as pressure or mass. Micromachined channels and structures offer additional capability. An impressive early example was an implantable active probe [139] that was developed into to a high density neural interface with microfluidic drug-delivery capability [140].

Sensing density in passive arrays is limited by wiring. Active circuitry can utilize addressing to support a high density of sites. In a binary switching scheme, the number of wires required scales logarithmically with the number of sensing sites, rather than linearly.

There are many obstacles to implementing a single-chip configuration. System design and modeling have completely new sets of constraints that may be unfamiliar to a circuit designer (discussed in the remainder of this section). The tools for designing such systems have not reached a level of sophistication and reliability comparable with that of IC design software. Furthermore, heterogeneous integration of electronics and fluidics requires packaging, which cannot rely on industry-standard wire bonding or flip chip mounting (Section 3.6). Finally, using a CMOS chip as a platform for successful cell culture and biological experiments requires modification of existing biological protocols (Section 3.7).

3.4.4 Comparison of Signal Quality With The two Approaches

Notwithstanding the technical challenges, in many design scenarios the most important considerations are resolution and accuracy. Ideally, one would like to be able to quantitatively compare the signal quality of the one and two chip approaches to aid in the decision process.

Unfortunately, differences between individual systems and a lack of testing data make this difficult. Typically, circuit designers report the electrical specifications of their circuits alone (no sensors), and in some cases the circuits are tested with sensors attached. It is uncommon to find a

characterization of the system performance before and after the front-end sensors have been added.

A good example of a two-chip system is a neural amplifier chip connected to passive, remote electrodes. Significant design effort has been invested in the development of low power amplifiers (for example for implantation or portable use) that exhibit low input-referred noise. The input-referred noise amplitude must be lower than the neural signals, which are as low as 10s of μV . Typically the neural amplifiers are characterized before they are connected to the electrodes, and the noise characteristics of the system are usually not specified.

The electrodes for neural amplifiers contribute both thermal noise and 1/f noise [139], as well as less-understood interfacial noise. The contributions of each of these is unknown. Two groups have characterized their systems with added electrodes, providing ballpark values that would be expected to be similar for other systems. Najafi et al. [139] found that the noise (at 1 kHz) in their system increased tenfold, from under $10 \text{ nV}/\sqrt{Hz}$ for the preamplifier alone to $100 \text{ nV}/\sqrt{Hz}$, upon the addition of electrodes (of 5.8 M Ω). A band-limited integration under the noise curve provided in [139] shows that the rms noise value increases by a factor of 2 as the electrode impedance is increased to 12.9 M Ω . Mohseni et al. [141] found that the input-referred noise increased, from 7.8 to 10 µV rms, when an electrode (177 µm²) grounded in saline solution was attached. (Surprisingly, the addition of an unusually large (3000 µm²) electrode decreased the input-referred noise below that of the amplifier alone, from 7.8 µV rms to 7 µV rms.)

System noise has been estimated by post-processing the amplified neural signal. The identified spikes were removed by filtering, and the background noise was estimated from the remainder. This method was utilized in [142], showing that the input-referred noise increased from 3.5 μ V rms to 10 μ V rms when considering the added effects of the electrodes and test setup. The electrodes again brought the noise floor of the system to 10 μ V rms.

There are no reports of noise in 1-chip systems. Since the electrodes are close to the active devices, presumably the only noise would be front-end noise introduced by the sensing electrodes. For further information about noise contribution mechanisms from electrodes, we point the reader to the insightful discussion about electroencephalogram (EEG) electrodes in [143].

3.4.5 1-Chip or 2-Chip Approach

Single chip systems are significantly more complicated to implement. In fact, the focus of many papers has been solely on the development of packaging and integration schemes for single chip systems because most CMOS sensors continue to be developed independently. The design process for bio-ICs should consider from the outset not only the sensor operation but also all of the integration and application constraints.

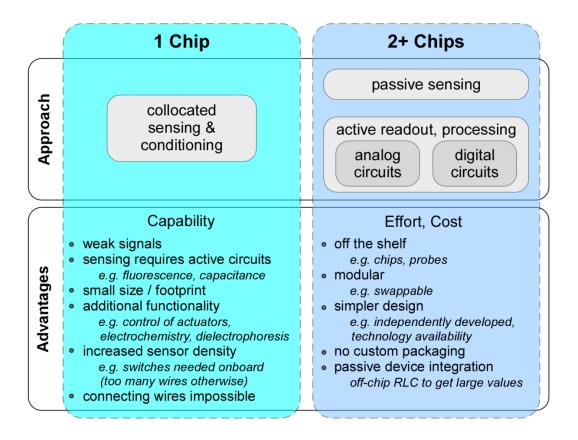


Fig. 28. Advantages of 1-chip versus multi-chip approaches.

The design flow begins with the decision to make either a 1-chip or 2-chip system (Fig. 28). Given the packaging challenges of a single chip system, the decision to pursue this approach must be sufficiently justified. Since a 2-chip system includes one passive chip the decision process must revolve around the ability of the passive chip to perform the required sensing, and the feasibility of communicating high quality information from the passive chip to the active CMOS IC. Because the 2nd chip is passive it cannot contain any active sensing sites, switches, or signal buffers. Accordingly, the first criteria becomes whether the sensing can be performed with

purely passive structures, for example a simple photodiode could be placed on a passive chip whereas an active pixel sensor could not. Similarly if the signal source is weak and the signal path is subject to noise comparable with the signal power, then it requires active amplification and a single chip solution would be required. Lastly, even if the sensing can be performed by passive devices, communicating the information between the passive chip and active chip can present issues with the number of electrical connections required, the possibility of creating the connections given the application, and the opportunity for noise to be coupled into the signal traces. Certain applications cannot accommodate a large number of connections, for example in implantable systems the percutaneous wiring density is limited by the surgical site and the expected lifetime is a function of the anticipated motion. Since each sensing site must be connected by a wire to the active IC, these wires will effectively act as antennas for noise from electromagnetic radiation. Therefore a single chip solution is necessitated when either the required number of wires cannot be implemented, or if the signals are too weak and would be subject to excessive interference from noise.

3.4.6 Modeling of Heterogeneous Systems

The materials and components (including the biological ones) in a heterogeneous system often have wide ranges of parameters (such as dielectric constants and layer thicknesses) and batch-to-batch inconsistencies. Some CAD tools partially address the modeling of heterogeneous

systems, e.g. finite element simulation of MEMS structures and SPICE-like simulation of biological components, but widespread adoption and standardization are not on par with IC CAD tools. As these tools develop to incorporate cross-domain simulation and modeling, they are expected to play an increasingly important role in the design and optimization of future heterogeneous systems.

3.4.7 MEMS Modeling and Simulation

There was a push in the early 1990s to develop standardized goal-oriented CAD tools for MEMS [144], with lumped-parameter models for various mechanical components that could be subsequently integrated into an electrical simulator to model their interaction with circuits. This effort and others have led to the development of modern MEMS simulators that are capable of aiding the entire MEMS design process from mask design to fabrication. Software can model the results of sequential deposition and etching steps and provide a 3D model of the resulting physical structures. However, MEMS processing is susceptible to variations, especially within a university research environment. A few CAD platforms are capable of modeling process uncertainty and error propagation using Monte Carlo methods (eg. MEMS Pro). However, even these advanced CAD tools are incapable of modeling the interactions of MEMS with CMOS and biology.

The main MEMS CAD software packages are listed in Table 1. Some of these tools, such as MEMS Pro, are built as modular extensions to existing circuit design software. Other

tools, such as those offered by ConventorWare and IntelliSense, are more complete packages that include multi-physics capabilities and MEMS process simulation, and they can be used to create parametric behavioral models for circuit simulators.

TABLE I SOFTWARE PACKAGES FOR SIMULATION

Circuits	Heat	MEMS	Fluidics
Cadence	COMSOL HeatWave* SYMMIC ANSYS FloTHERM	COMSOL	COMSOL
Mentor Graphics		IntelliSense	Fluent
Tanner Tools		CoventorWare	FLOW-3D
Synopsys		MEMS Pro**	CFD-ACE+

^{*} A plug-in for circuit simulators. ** Works with Tanner Tools.

3.4.8 Two-Step System Level Modeling

CAD tools for each domain can be used to simulate particular aspects of an integrated system. Unfortunately, no tool adequately addresses all of these issues in one platform. The fundamental obstacle to modeling an entire system with heterogeneous integration of CMOS, MEMS, and biology is that each one of the domains is sufficiently complex that modeling interactions between them presents a significant challenge. A preliminary approach to integrated modeling may be to use domain-specific modeling systems to develop macro-level behavioral models that can be subsequently imported into a simulator to provide a limited level of cross-

domain simulation capability. Even then, model validation for bio-IC components will not be trivial: MEMS devices can vary significantly, and biological processes are notoriously stochastic.

Once the decision to pursue a 1-chip system has been made, a coupled iterative simulation process is required, such as the one introduced in [145] for electro-thermal circuit simulation. Fig. 29 illustrates the two-step design and simulation methodology for the multiple domains in which a bio-IC must operate. The core idea is that the results from simulation in one domain are used to inform the others.

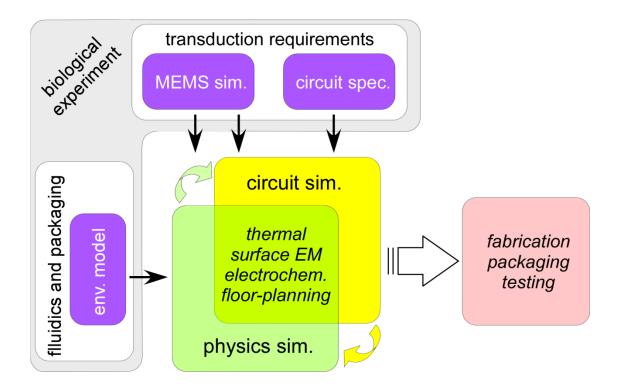


Fig. 29. Design flow for a 1-chip bio-IC system. The biological experiment determines the transduction requirements (top) as well as the fluidics integration and system packaging (left). These requirements set the specifications (purple) for the circuits and MEMS devices as well as the environmental model for physics simulation. Results from circuit simulations (yellow) are used to provide input to physics simulations (green) and vice versa, iteratively. The process may need to cover multiple physical domains. Lastly, the devices are fabricated and packaged.

The process begins with the biological question to be answered. This sets the requirements for the transduction as well as the packaging and fluidic integration. The MEMS and circuit schematics are simulated in SPICE, while the multi-physics models are built around the chip's environment. The models for the MEMS structures are developed on their own and then used as parametric inputs to both the circuit and multi-physics models. Then, the circuit simulations and multi-physics simulations are performed iteratively.

3.5 CMOS IC Design

The rest of the paper pertains to 1-chip bio-IC systems: fully integrated systems with CMOS, post-fabricated MEMS structures, and cells cultured on the surface of the chip. IC design for such an integrated system needs to take into account thermal effects, changes in electrical characteristics, electrochemistry, and additional floor planning constraints.

3.5.1 Thermal Effects

3.5.1.a Circuit Design and Simulation

In most cases bio-ICs will operate in a 37 °C environment. Circuit simulators can account for this, i.e. via the ".Temp" statement in SPICE. The temperature dependence of MOS transistors has been well characterized; the threshold voltage varies with temperature [146], as does the carrier mobility [147]. Some advanced simulation packages can even compensate for Joule heating and heat transfer (eg: the Heatwave module for Cadence), but if they do not, the onus is on the designer to take these electro-thermal effects into account [148] using a secondary simulation platform. The option also exists to build temperature compensation into the circuits [149] using feedback from on-chip temperature sensors [150-153].

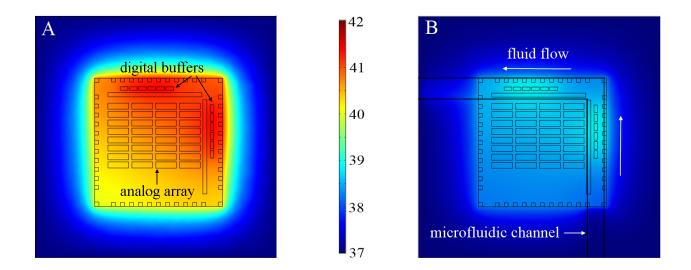


Fig. 30. Results of a COMSOL electro-thermal simulation showing the effects of Joule heating for an IC containing both digital and analog components encapsulated in epoxy and with fluid on the top surface. High power digital buffers are on the top and right edges of the layout. The analog circuits are arrayed in the center. A) The temperature profile shows the equilibrium reached after continuously running within a 37 °C environment. B) Shows the same IC with active cooling provided by a microfluidic channel.

3.5.1.b Modeling Temperature Variations

Ceramic dual inline packages (CerDIPs) are designed to act as heat sinks [151], but bio-IC packages present new thermal boundary conditions. Typical thermal analysis of IC operation assumes a boundary condition of room temperature, but bio-ICs must operate at temperatures that are suitable for cell culture. A secondary or modular plug-in simulation platform can be used to model Joule heating effects as well as heat conduction by the package. This two-step iterative modeling approach requires an initial SPICE simulation to find the power dissipation of the circuit blocks. Power dissipated over the circuit layout areas is used to model thermal heating effects (Fig. 30) using a finite element simulator [151] such as COMSOL, adding information

on materials and the environment. Then, the results of the thermal simulation can then be fed back into the SPICE simulation to specify the operating temperature of the circuits for determination of changes in operation and power consumption.

3.5.1.c Biological Consideration of Thermal Effects

Cell culture requires strict temperature control: for mammalian cells, the surface should be at 37 + 2 °C [154]), a condition that is typically maintained by an incubator. However, when the IC is continuously operated, power dissipation raises the chip surface temperature. Fig. 30 shows the surface temperature predicted by an electro-thermal simulation of a mixed signal IC within an epoxy package at a boundary condition of 37 °C. The IC was designed to amplify biopotential signals and used an asynchronous readout scheme to output the spatial location of spiking events as they were identified in real-time. The analog array included amplifiers with inpixel spike detection circuits, and the digital portion of the IC included address event representation circuitry and high powered buffers to enable the chip to directly drive external hardware. Fig. 30A shows the temperature of the chip when a well is used to contain the cell medium, the surface temperature is indicated by the color. It is evident from the figure that high power dissipation in the digital circuits results in not only temperatures that are too high over the entire surface, but also a temperature gradient across the chip, despite the high thermal conductivity of silicon and conduction of heat by direct contact with water. This issue could be partially resolved by changing the thermal boundary condition: specifically, by lowering the

incubator temperature by an amount corresponding to the local heat generated by the bio-IC. Alternatively, the results of the electro-thermal simulation can be used to inform the design of microfluidics to actively cool the bio-IC. Fig. 30B shows the resulting temperature profile when a fluidic channel is used to transport heat away from the IC. Although the temperature of the fluid at the inlet is 37 °C, the active flow reduces the surface temperature of the IC to a level that is within the tolerance for cell culture.

For use of the bio-IC outside an incubator, on-chip heaters can be employed advantageously to warm the cell medium [151], at the expense of significant power draw. However, many biological experiments require fluid flow over the cells. In such cases, it is necessary to preheat the fluid because on-chip heaters cannot warm the fluid sufficiently without operating at much higher temperatures than cells can tolerate. Without flow, and if the system is well insulated, on-chip heaters may be sufficient, but they should be uniformly spatially distributed throughout the layout to minimize thermal gradients. It has been observed that relatively small variations in temperature play a large role in cell viability across the chip [151]. Power dissipation causes a similar concern for in-vivo implantation, for which there are varying reports of the maximum acceptable power density. Some of the reported values range from 40 mW/cm2 [155] to 80 mW/cm2 [156]; the numbers vary based on the type of tissue and heat dissipation from blood flow around the implantation site.

3.5.2 Fluidic Effects on Communication and Computation

Communication traces are needed for coupling signals and controls in and out of the system and for internal signal routing for processing or computation. By changing the medium that surrounds the chip from air to water, the effective dielectric constant between areas of the chip is increased (since the dielectric constant of water is approximately 80 times that of air), making the IC more susceptible to coupling of interfering signals. This can be illustrated by examining pad-to-pad capacitance. In a typical CMOS IC, the pad-to-pad impedance is large and well characterized, but in the presence of an aqueous solution such as cell medium, the capacitance between pads increases. Using a finite element model we show (Fig. 31) that this increase can be over an order of magnitude. (The relative permittivity of saline solution varies with salt concentration, but for the levels of solutes used in biological media the relative permittivity remains close to that of water [157]). The larger capacitance will increase pad-to-pad signal coupling, which is a problem when one pad has a digital signal and the other an analog signal from a high impedance source.

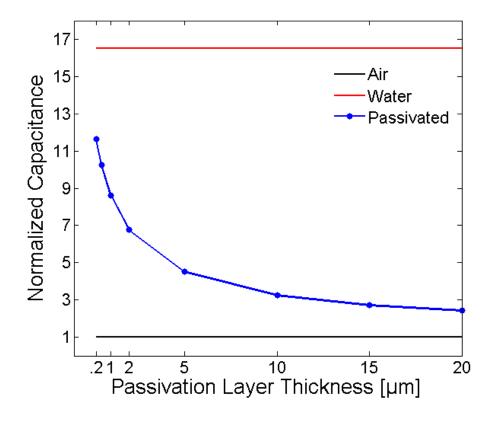


Fig. 31. Results of a FEM simulation showing the change in pad-to-pad capacitance when water $(\epsilon_r \approx 80)$ replaces air $(\epsilon_r \approx 1)$ on the chip surface. Also shown is the effect of varying the thickness of an intermediate passivation layer $(\epsilon_r = 3)$. Values have been normalized to the capacitance in the presence of air.

Due to the increased likelihood of signal coupling, it may be necessary to use standard techniques such as driven guards for immunity to interference [158] and differential processing for immunity to correlated noise sources, or to introduce additional microfabrication processing steps and structures in order to mitigate the noise, such as the introduction of an electrical shielding layer between the surface and the underlying circuits [158].

The results of FEM simulation can again be used in a two-step modeling process: the effect of coupling through the fluid can be taken into account during the circuit simulation by altering model parameters. Unfortunately, the parameters will differ among CMOS fabrication processes, which utilize different materials and layer thicknesses. It would likely require collaboration with the CMOS foundry for accurate modeling.

Increasing inter-pad spacing at the cost of silicon (Si) real estate is not an optimal way to alleviate the issue of signal coupling. An approach that we have employed for an optical imager has been to post-process the IC to coat the surface with a transparent conductor (indium tin oxide). However this is not an option for chips that are designed to measure electrical signals from the fluidic environment. For such systems, FEM simulation can be used to determine the packaging materials and appropriate layer thicknesses to mitigate the increased signal coupling. For the results shown in Fig. 31 a three dimensional model of an IC was used for electrostatic simulation. An initial simulation was performed to determine the difference in capacitance when air was replaced with fluid. Further simulations were then performed to determine the necessary thickness of passivation material (Parylene) to minimize the effects of signal coupling through the fluid.

3.5.3 Electrochemical Effects

Microfluidic and cell culture environments are inherently electrochemical, and CMOS chips are inherently electrical. This difference imposes new challenges, such as unknown

electrode potentials that vary substantially over time due to electrochemical effects and unintentional activation of electrostatic discharge protection structures due to DC differences between the electrochemical "ground" and on-chip electrical potentials.

Electrochemical potentials may generate large DC offsets, which saturate the inputs of electrical circuits. One possible way to reject such offsets would be to use an auto-zeroing amplifier, such as the one proposed by Hasler et al. [159], which is capable of rejecting DC offsets in the input signal by using an adaptive floating-gate circuit. For neural amplifiers, another approach to this issue has been the use of differential amplifiers with large coupling capacitors at the inputs [50]. These amplifiers work well but use a large amount of space, decreasing the density of active microelectrode arrays. This is a case where a 2-chip solution may be advantageous (section 3.4.2.)

Another problem occurs when electrical circuits are used to drive electrochemical reactions. Electrochemical reference electrodes provide a well-defined potential in electrochemical space, but thin-film versions are short-lived. Without the use of a true reference electrode, the potential of the CMOS circuits relative to the electrochemical potentials in the fluid is not known exactly. Thus, the redox potentials may appear to be scaled and shifted. This places dynamic range constraints on the circuits, in some cases requiring them to provide driving signals that are below the supply ground. In such cases, the circuits must be designed to have

positive and negative supplies with a reference ground (connected to the fluid) at the middle of the supply rails [160].

The design of on-chip potentiostats for electrochemistry requires consideration of not only the materials and environment, but also informed design of the CMOS circuits that drive the reactions. We point the reader to reference [161] for a thorough discussion of the various circuit configurations and readout techniques, including temperature compensation for precise current measurement.

3.5.4 Floor Planning and Area Resources

Limited Si area always poses a challenge to designing CMOS systems. The integrated nature of the bio-IC complicates floor planning further because portions of the chip need to be utilized for reference electrodes, fluidic integration, cell culture, and MEMS structures.

3.5.4.a Surface Topography

Topographical variations in the CMOS surface can be problematic for post-processing. The thickness of structures fabricated on top of the chip may be less than the height variations of unplanarized layers, distorting the structures as well as creating difficulties in employing sacrificial layer release. Patterning fine features may also be a problem due to inconsistent focus during photolithography. The occurrence of topographical artifacts varies between CMOS processes; in some technologies, the internal layers are planarized, but the surface is not. If the

topmost metal layer introduces unacceptable surface topography, it cannot be utilized, reducing design flexibility and possibly system capability.

3.5.4.b Surface Structures

The physical layout of overlying electrical or capacitive structures will affect the placement of underlying electronics. At least the top layer of CMOS metal will be required for interfacing, and will thus not be available for signal routing.

The top CMOS metal layer cannot connect to the fluid directly unless it is electrochemically inert (section 3.7.3). Ideally, the top electrode should be covered with an inert metal such as gold (Au) or platinum (Pt). Furthermore, aluminum (Al) (which is commonly used for on-chip routing) is susceptible to etching by both wet and dry processes used during post-fabrication. To mitigate accidental etching of the CMOS top metal layer, it is advisable to use a metal stack with arrayed vias (tungsten (W), a common material for vias, is impervious to many etchants that attack Al), to ensure connectivity with underlying metal layers.

3.5.4.c Fluidic Integration

One of the major hurdles in integrating microfluidics arises from the mismatch in sizes between microfluidic systems and CMOS ICs [102]. Though microfluidics take advantage of fluid dynamics at the micro-scale, the material surrounding the fluid path and the inlets and

outlets are relatively large. Typical ICs are millimeter scale, while microfluidic systems are centimeter scale.

If wire-bonding is used for packaging, the fluid path must avoid the bondpads entirely. One approach has been to remove bondpads from two sides of the IC to make room for a fluid path down the center of the chip [162]. Other packages avoid wirebonds entirely and use patterned thin-film metal traces to provide I/O [79, 102]. Systems that employ flat interconnects significantly ease the issue of adding complex fluidics. If the surface is flat enough to employ microfabrication techniques to create I/O paths, then other post-processing, such as the addition of MEMS structures and microfluidics, is also possible.

3.5.4.d Placement Considerations for Biology

It is known that electric fields influence cell morphology, particularly nerve cells [163]. For cell culture or device implantation, it may be necessary to use one metal layer to shield the biology from the underlying electronics, again using up one of the metal layers in the CMOS process.

Although some of the effects of EM radiation from the IC itself can be modeled, the interaction of the IC with the environment cannot. Basic EM radiation modeling can be performed in COMSOL with parameters such as locations of potential sources and RF signal generation sites. However, the effect that the EM radiation will have on the cells and the medium cannot be modeled fully because in many cases these effects remain unknown. Certain well-

understood effects could be predicted, for example dielectrophoresis, but modeling other effects, such as electrochemical interface effects and ionic gradients, is likely to be too complicated for a general FEM solver.

3.6 Packaging and Integration constraints

CMOS chips exposed to fluidic environments have packaging requirements not satisfied by standard methods developed for ICs. Packaging that integrates electronics with fluidics remains an ongoing area of research with many different approaches demonstrated in the literature [17, 67, 86, 88, 89, 102, 121, 164].

Unlike traditional electronic packaging using CerDIP or similar methods, fluidic packaging has not been standardized by industry. Few commercial products exist that incorporate CMOS with fluidics. One notable exception is the BioCAM system offered by 3Brain, which allows neural cell cultures to be plated on the surface of a CMOS sensing array. Although the packaging for the commercial product is proprietary, some related early work by Berdondini et al. [165] indicates that the CMOS chips were wire-bonded to a PCB and then passivated using epoxy. Another example of an industrial solution that has been successfully adapted for fluidic integration can be found in ceramic packages based on the commonly used low temperature co-fired ceramic (LTCC) package. CMOS chips were bump-bonded to ceramic carriers, and passivation material was applied to the bonds to isolate them from fluid, allowing cell culture on the surface of the IC [94]. LTCC packages themselves can be designed to

incorporate microfluidic channels (in addition to the electrical traces) within the stacked layers that form the ceramic substrate [166].

In the absence of standardized fluidic packaging, there are two options to accommodate bio-IC requirements: adapt a pre-existing standard package or develop a custom package. The primary requirement for any fluidic integration is that the IC surface must be *selectively* passivated, allowing isolated electrical connections from the I/O region to the outside world while exposing the "active" areas of the chip to the fluid to enable sensing. Inadequate passivation results in system failure and undesired electrochemical effects, as shown in Fig. 32.

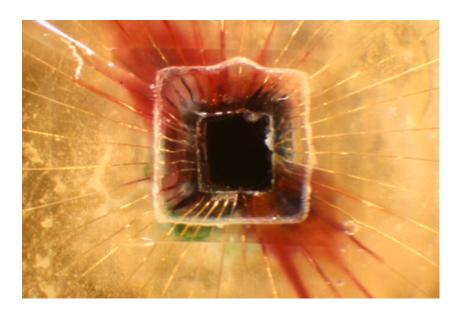


Fig. 32. Discoloration due to electrochemical reactions occurring at improperly passivated bondwires. This chip was developed and packaged for surface cell culture. Over a period of one week operating in the culture environment, the neutral red stain from the cell culture medium was transported along several of the bond wires (red traces), and corrosive electrochemical effects were observed on other bond wires (green).

The issue of separating the I/O from fluid is easily solved for large CMOS chips, where physical separation between the sensing region and the I/O allows the use of structures such as glued-on wells to meet the selective passivation requirement. On the other hand, if the chips are mm scale, other techniques must be used for integrating the fluidics. A review of some common methods can be found in [79].

If wirebonds are used to provide I/O, isolation is challenging because of their topography. Wirebond passivation can be done with a conformal material such as Parylene (which can be selectively patterned) or epoxy (which can be selectively applied) to expose the sensing region of the chip. In a standard chip carrier (Fig. 33), the entire cavity can be treated as a well for fluid. Alternatively, if the passivation material can be patterned during deposition (for example by using a UV-curable polymer or sacrificial material (see section 3.6.6), it can be used to define the fluidic path. Similarly, if the IC is wire-bonded to a PCB, a patternable passivation material can be used to protect the wirebonds after which additional fluidic structures can be added around the chip. However, patterning the passivation material photolithographically is difficult because of the large step height between the chip and the carrier.

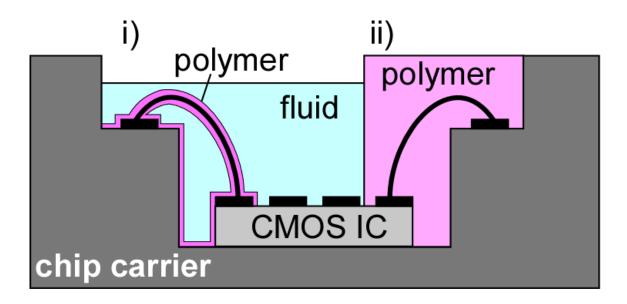


Fig. 33. A standard IC package adapted for fluidic interface. i) Wirebonds (to the I/O region) passivated using Parylene. ii) A photopatternable polymer used to simultaneously passivate the wirebonds and define the fluid well for the sensing region.

The second category of packages, those that use a custom "chip-in-hole" type carrier, allow significantly more freedom for integrating not only fluidics but also additional structures. The defining characteristic of such packages is that the chip surface is level with the carrier. Post-processing is straightforward when the IC is embedded in a "handle" substrate (Fig. 34) [79, 102, 121]. This allows microfabrication techniques to be used not only for passivation but also for constructing the I/O as well as fluidic structures.

MEMS-based post-processing can also be used to increase system functionality in embedded chip packages by adding structures such as actuators for sample manipulation or optical filters. Handle wafers also allow placement of off-the-shelf components away from the CMOS real estate. Using a semiconductor-based handle substrate opens the possibility of

integrating large-area components (resistors, capacitors, and inductors) and even diodes and transistors.

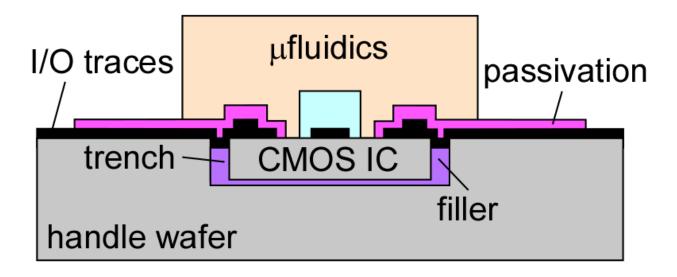


Fig. 34. Schematic of an example custom chip-in-hole package. The IC is embedded in a handle wafer and leveled using a filler material. Patterned metal traces provide electrical I/O, and a passivation material isolates them from the μfluidics.

One issue with creating chip-in-hole carriers is that the size of the chip from the foundry is not always consistent. There can be a substantial gap between the edge of the IC and the handle wafer, which inhibits conformal application of photoresist and results in discontinuity of the metal traces used for I/O connections. An elegant solution is to create a custom hole for the IC using the chip itself to define the lateral dimensions of the cavity (self-aligned masking) [167]. Other approaches to the gap issue have been to create holes that are larger than the chip and use material such as spin-on-glass (SOG) or polymers to bridge the gap and also bring the chip flush and level with the surface of the carrier [102]. The issues caused by non-uniformly

sized chips is mitigated if, instead of a hole being created within the carrier, the carrier is formed around the chip. This can be achieved by using a polymeric carrier [79]. This method has the additional benefit of enabling integration of multiple chips and passive components into a single carrier wafer. An epoxy yields a rigid substrate that can be treated like a wafer. An interesting alternative is the use of an elastomer such as PDMS [88], which allows for flexible substrates. This method shows great promise for implantable and wearable electronics.

Given that generalized bio-IC design should consider not only lab-on-chip systems but also medical devices and environmental sensors, it would be beneficial if there were greater collaboration between academia and industry in developing standardized packages for fluidic interfaces.

3.6.1 Surface Materials

Information about the materials on the surface of the integrated circuit is needed for subsequent processing. For example, whether the uppermost layer is nitride, oxide, or polymer determines its resistance to etchants. Commercial CMOS chips come with a fixed, proprietary set of materials, and different foundries are known to utilize different materials for the metal stacks and final passivation layers. Since the materials and thicknesses are unknown to the end-user, it may be necessary to identify materials using elemental analysis.

Biocompatibility poses additional constraints (see Section 3.7.3). Depending on the material placement, it may be necessary to have compatibility with cells growing directly on the material surface or just with cells growing nearby. (Some materials contain toxic additives that can leach into the sample volume.)

Lab-on-chip diagnostic systems require surface functionalization with biological molecules, such as nucleic acids, proteins, or antibodies. In this case the chip surface must be amenable to the attachment chemistry, e.g. silanization, thiol bond formation, micro-printing, or electrodeposition.

3.6.2 Resist Edge Beads

Microfabrication requires that photoresist can be applied uniformly and defined photolithographically. Resist is applied by spin-coating to yield a particular thickness. Surface tension results in an unwanted thicker "edge bead" around the perimeter of the substrate [168]. For wafer-level processing, the edge bead is removed so that the photo-mask can make contact with the resist surface, since a gap degrades resolution. In our own work we have measured (Tencor P-20 profilometer) edge beads as thick as 25 μm for a resist with a nominal thickness of 1.8 μm (Shipley 1813, 2000 rpm, 3x6 mm die). The problem of edge beading is exacerbated on mm-scale ICs, on which the bead can occupy most of the die area. Lin et al. measured resist uniformity under similar conditions (3000 rpm, 3x3 mm die), and it was limited to 50% of the

chip surface [169]. Embedded chip packaging techniques circumvent this issue by shifting the edge bead to the perimeter of the handle wafer.

Another approach to mitigating the edge bead is to increase the centrifugal force on the resist by temporarily adhering the chip to the outer edge of a large wafer, thereby increasing the spin radius and correspondingly the centrifugal force. This technique has been applied at typical resist spin speeds [169], and it was found that larger dies exhibited less edge beading and greater uniformity. In our own work at higher spin speeds (8000 rpm) the edge bead was reduced in width and height but the resist thickness in the center decreased.

3.6.3 Low Temperature Processing

Many standard processes used during MEMS fabrication, such as annealing polysilicon structures to relieve stress, occur at temperatures above the point at which underlying circuits are damaged [170]. The thermal budget for an integrated system with heterogeneous materials is limited by the material with the lowest thermal tolerance. Si-based CMOS chips with Al interconnects can handle temperatures as high as 450 °C [129]. Polymers have lower limits: Parylene melts at 290 °C [130], polydimethylsiloxane (PDMS) deteriorates at 340 °C [132], and the limit for SU-8 (an epoxy based negative resist often used for permanent structures) is 200 °C [133]. The limits for individual materials do not account for interfacial stress arising from thermal expansion mismatch between different materials. For example, Si expands 3 ppm/°C, while SU-8 2000 expands 52 ppm/°C. This difference of over an order of magnitude can result in

delamination of SU-8 structures from the Si substrate at temperatures below the destruction limit for SU-8.

3.6.4 Damage to Circuits during Post-Processing

IC design rules include considerations to mitigate damage to gate oxides by antenna effects (charging during plasma-based processing) [171, 172]. Post-processing steps that employ plasma can cause similar damage, which can be avoided by first depositing a metal layer to electrically short all the exposed CMOS connections on the chip surface. This metal layer can later be removed after the post-processing has been completed.

3.6.5 Interfacial Impedance

An electrode-electrolyte interface presents a large interfacial impedance due to the transition between electronic and ionic conduction. One method to reduce the impedance is to use electrodes having larger area; however this limits sensing array density. Another traditional method is to use specialized electrode materials such as platinum black or iridium to reduce the interfacial impedance [173]. Conjugated polymers, applied as a coating over a metal electrode, are another class of materials that have recently been employed for recording [174] and electrical stimulation of cells [175]. They decrease interfacial impedance and increase the charge capacity of the electrode. One example is poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS), which increased the SNR for in-vivo implanted electrodes [176]. We found that

PEDOT:PSS deposited on Au electrodes using the methods outlined in [175] resulted in a decrease in impedance of nearly two orders of magnitude [79].

3.6.6 Fluidics Integration

Cell culture requires a medium that maintains isotonicity and pH, as well as provides nutrients and growth factors. Microfluidics can be used not only to provide the required environment for cell culture, but can also be used to provide chemical stimulation to the cells. For fluidics that are open to the atmosphere, evaporation changes the osmolality. Evaporation is exacerbated when working with smaller volumes of fluids [177]. Sealing the system is likely to be required unless the fluid is continually replenished.

The microfluidic structures can be fabricated on their own and then bonded to the chip surface (e.g. PDMS bonded using oxygen plasma), or a material such as SU-8 that can be patterned directly on the surface of the IC using photolithography [87]. Hybrid systems have also been demonstrated in which the microfluidic channels are patterned in a material such as acrylic, plastic, or glass and the fluid manifold is sealed to the surface of the IC using an intermediate gasket material such as PDMS [167]. Alternatively, microchannels can be fabricated within the encapsulation material itself by using a soluble patternable material around which the encapsulation material is allowed to cure [19].

Surface hydrophilicity is essential for both adherent cell culture and proper wetting of the surface by the fluid medium. An inadequately wetted surface inhibits cell adhesion. CMOS ICs are often passivated at the foundry with a natively hydrophobic material like silicon nitride (Si₃N₄). Fortunately nitride is readily modified by using oxygen plasma to create an intermediate layer of oxide that is hydrophilic [178].

3.6.7 Package Sterility

The risk of exposing cells to microbial pathogens or mold increases every time the bio-IC is removed from the incubator. One approach to keeping cultures healthy is to keep them in sealed chambers enclosing the sensing sites [179]. Microfluidics structures can also be employed to isolate the cells from the environment and have successfully been used for cell culture outside of an incubator [151]. Fluid flow within microfluidic channels can, however, apply large shear forces to cells. Stress due to shear has been shown to lead to abnormal morphology, induce changes in biomolecular processes [180], and cause apoptosis [181].

The bio-IC should be sterilized initially and between subsequent experiments.

Autoclaving (120-190 °C) may be incompatible with heterogeneously integrated systems.

Rinsing with alcohol or exposure to ultraviolet light (UV) are other common sterilization methods, but material compatibility should be known beforehand. Parylene and Si3N4, commonly used for surface passivation, are compatible with alcohol and bleach, allowing use of liquid disinfectants followed by UV light exposure.

It is also important to consider bio-fouling for chips that are to be reused. Cell culture on the surface of the chip will inevitably result in the formation of a film of cells and proteinaceous debris on the surface of the chip. This film degrades signal strength and can prevent proper cell attachment when the chip is reused. We have observed that these films must be removed as quickly as possible and not allowed to dry out, since this makes removal difficult. Rinsing with alcohol is not an effective method for cleaning chip surfaces because it can result in "fixation" of cellular debris on the chip surface [182]. Use of a cleaning agent that combines detergents with protease enzymes (such as Alconox Tergazyme) is recommended by manufacturers of multi-electrode arrays. We have achieved effective cleaning of active microelectrode array chips by soaking in a 1% solution of Tergazyme and applying gentle agitation over the course of two hours, followed by rinsing and sterilization.

3.6.8 Robustness

Materials in the system must remain robust and stable over time, but when they are exposed to the aqueous saline environment for cell culture, many corrode or chemically react (Fig. 32). One pernicious way in which systems fail is if materials absorb water. If a polymer is used to encapsulate wirebonds, swelling leads to electrochemistry (Fig. 32) and bond wire detachment.

3.7 Biology on CMOS

The third set of constraints on the fluidic CMOS system comes from incorporation of living biological components, such as sensory cells, since the cells must be provided an environment that closely mimics physiological conditions.

3.7.1 Cell Plating

The culture of adherent cells is facilitated by adhesion promoter. While some cells, e.g. muscle cells, do not require coatings for surface attachment, others, such as neurons, do. Natural adhesion promoters such as collagen, laminin, and fibronectin simulate the extracellular matrix found in most types of tissue. Cationic polymers such as polylysines and polyethylenimine create a positively charged surface, which facilitates attachment of negatively charged cell membranes [183]. Unbound synthetic polymer molecules can be toxic, so surface treatment with these requires thorough rinsing after coating [184].

Promoting intimate contact between cells and the underlying material has the added benefit of increasing the SNR for electrical sensing [185]. However, most adhesion promoters are insulating, so coatings must be kept thin to minimize interfacial impedance. Biology protocols do not consider the minimum thickness of adhesion promoter required for cell attachment, and the tradeoff between adhesion promoter concentration and signal strength has

not yet been characterized. It may be necessary to experimentally determine the minimum amount of adhesion promoter required to successfully plate cells on the surface of the bio-IC.

3.7.2 Cell Culture Outside of an Incubator

Outside of an incubator, successful cell culture requires special consideration regarding maintenance of media pH and temperature. The bicarbonate buffering system (using carbon dioxide (CO2)) is used for acid-base homeostasis by many animals and has been adopted for mammalian cell culture [186]. Bicarbonate buffered media require non-atmospheric levels of CO2 to maintain physiological pH. Although CO2-independent media do exist, bicarbonate remains essential for certain types of cell culture [187]. Agents such as HEPES do not require CO2 but can be toxic to cells when exposed to light [188]. The Hibernate medium (Life Sciences)[189] can sustain mammalian neural cell culture at 2-8 °C and atmospheric CO2 levels for up to 30 days, allowing experiments, and even culture, outside an incubator.

Amphibian cells have less strict requirements (nutrients, temperature, and pH) than mammalian cells and can survive hypoxic conditions. Primary amphibian neurons remain viable (determined by cilia movement and Trypan blue exclusion) for at least 7 days at 2-8 °C when stored in a standard amphibian Ringer's solution containing glucose, salts, and HEPES.

When traditional CMOS packaging is used (e.g. CerDIP), a potential approach to maintaining temperature for cell culture may be to place a heating element on the package itself

and use an on-chip temperature sensor to implement feedback control. Ceramic packages have high thermal conductivity as well as substantial thermal mass, allowing them to act as stable heat sources for the fluidics.

3.7.3 Biocompatibility of Intrinsic and Added Materials

Materials such as Au, Si, silicon dioxide (SiO₂), Si₃N₄, and SU-8 have been shown to not inhibit cell culture and proliferation for durations of at least a week [190-192]. However, many of the materials commonly used in microfabrication have not been tested for compatibility with cell culture.

Al is reactive and subject to electrochemistry when in contact with cell media. Unfortunately, Al is commonly used for signal routing layers in CMOS, and active electrode arrays generally use the top metal from the CMOS process as the recording electrode. Therefore, Al electrodes must be covered with an electrochemically inert metal such as Au. Chromium (Cr) is commonly used as an adhesion layer for Au, but it is also electrochemically active and reacts with oxygen. Thus, it may be necessary to isolate the sidewalls of a patterned Cr/Au layer from cell medium, e.g. with a dielectric film [66]. Alternatively, titanium (Ti) can be used instead of Cr as an adhesion material. Ti is well established as a biocompatible material, with a long history of use in implants. However, wet etchants for patterning Ti generally contain hydrofluoric acid, which would also attack any SiO2 that may be on the IC surface.

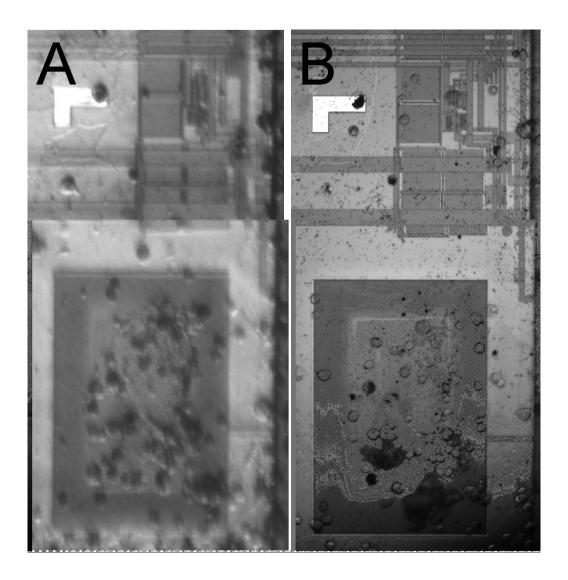


Fig. 35. Photomicrographs of salamander olfactory sensory neurons cultured on the surface of a neural amplifier IC. A) Image taken using a standard upright microscope. The focus is the best possible given the optical path. B) The same region taken with an immersion lens. The focus is better and more uniform across the image.

3.7.4 Imaging Cells on Opaque Substrates

It is often desirable to optically image cells plated on top of a CMOS substrate, for example, to correlate signals from an electrode array with cell locations or to perform calcium

imaging. Imaging techniques that rely on an optical path through the substrate, such as differential interference contrast (DIC) or phase contrast microscopy, are not usable with opaque samples. Reflected light imaging techniques, such as confocal microscopy or reflected DIC, are necessitated.

An optical path through an air-liquid interface renders non-immersion microscopy inadequate for producing high-quality images, with only a small portion of the image in focus and the rest subject to distortion (Fig. 35). High quality images through PDMS layers are also difficult to acquire. Capping the microfluidics with a glass coverslip confines the fluid under a material with better optical properties than PDMS and also eliminates the meniscus, reducing distortion but not eliminating it. The best images are obtained with an immersion lens, which the experimental configuration needs to accommodate, for instance with large-diameter shallow wells or removable wells.

Alternatively, determining cell location and detecting bioluminescence or fluorescence can be achieved with lensless imaging, using the bio-IC itself as a contact imager [193-195]. Contact imagers forgo the large and often expensive optics required for traditional imaging and can be used in compact lab-on-chip systems.

3.8 Conclusion

We have reviewed many of the challenges associated with designing, packaging, and using a heterogeneously integrated system that interfaces CMOS with biology and fluidics. Splitting the sensing and signal processing functions onto separate chips alleviates many of the issues. There are, however, advantages to combining these functions in a single chip that make facing the integration issues worthwhile, including improved signal quality, increased sensing density, and added functionality.

During chip design, heat must be critically examined: power dissipation by circuits can easily be high enough to compromise cell viability, and operation in a 37 °C environment will need to be considered during simulation. Exposure to fluidics raises two other issues. The high dielectric constant of water directly over the circuits and routing traces increases signal coupling. Electrochemical potentials on the electrodes may saturate the inputs to amplifiers and impose dynamic range constraints. Unfortunately, system design and modeling remains a significant challenge because of the lack of tools that can address multi-domain integration, necessitating an iterative approach using both FEM and SPICE simulations. Additionally, floor planning must account for surface topography, connections to sensors and actuators produced by post-processing, and any necessary electrical shielding.

Packaging CMOS chips for fluidic interfacing keeps the I/O regions dry, but allows cell culture in the center of the chip. Fortunately this is an area that has seen much recent progress,

especially from the lab-on-chip community, for whom integrating sensing, computation, and microfluidics enables not only miniaturization for portability but also massively parallel experiments and increased capability. The most versatile packages are those that embed the chip in a handle wafer, flush with the surface. The flat surface readily permits microfabrication procedures, such as the deposition of coatings to reduce interfacial impedance, and the addition of microfluidics; it also opens the possibility to move components off the chip and onto the handle.

Fundamentally, cell culture on CMOS has the same requirements as traditional cell culture, which means that the packaged chip may need to be coated with biomolecules and sterilized, and materials in the presence of cells must be nontoxic and nonreactive. Optical imaging of cells on the chip surface requires some consideration because the chip is opaque. One of the most important motivations for lab-on-a-chip systems is freedom from benchtop equipment, including incubators. Advancements in culture media have made it possible to keep some cell types alive without a CO₂ environment, meaning that culture is possible if sterility and a temperature of 37 °C can be maintained. The former can be achieved with sealed wells or channels, and the latter with heaters for the chip and any fluid streams flowing over the cells.

Chapter. 4

A Hybrid Bioelectronic CMOS Olfactory

Sensor

4.1 Introduction

Cell-based olfactory sensors offer the promises of homeostasis, high sensitivity, and adaptive sensing. Cells contain the necessary machinery to maintain themselves, eliminating the need for de-fouling mechanisms. Olfactory sensory neurons (OSNs) have high internal gain, producing easily detectable voltage signals, action potentials (APs), clearly indicating odorant binding events in a binary manner. They can also exhibit adaptation, allowing cell-based sensors to not only demonstrate variable dynamic range, but also to reach equilibrium with the ambient environment and respond to changes in stimulus concentration [196].

The idea that living material can be used as technology has existed since the 19th century [197]. The techniques of cell culture, controlling elements of life outside of the natural body have advanced significantly since they were originally conceptualized. Today, biotechnology and in particular, cell culture based technologies are the basis of a huge industry, used for production of proteins and vaccines, as assays for screening new chemicals and drugs, and numerous other

applications [198]. Cell culture has three basic requirements, delivery of sustenance, removal of waste, and maintenance of the environment. Microfluidic technology can address the first two requirements by flowing media over the cells. Regulating the environment primarily involves pH and temperature control, the former can be done chemically, either with synthetic or natural buffering systems, and the latter can be addressed with simple heaters and insulating materials. Methods and devices have been developed that allow cell culture without incubators, within labon-a-chip devices, in so-called "harsh" environments. Indeed, scientific experiments [199] using cells have been carried out in autonomous culture devices in the zero gravity environment of space [200].

Cell-based olfactory sensor development has relied on the existing technology and techniques that have been developed to study electrically active cells. Fluorescence imaging has been used to interrogate the response of a large array of cells trapped in microfluidic wells [62]. Light-addressable potentiometric sensors (LAPS) have been used to record the responses of both whole olfactory epithelium [47] and dissociated cells [44]. Similarly, "passive" microelectrode arrays have also been used to record from whole epithelium [46], as well as dissociated cells [63].

CMOS technology has been used to develop compact "active" microelectrode arrays, leading to high density systems with 4096 sensing sites within an area less than 2 mm² [201]. Lab-on-a-chip devices that combine CMOS sensing arrays with fluidics allow miniaturization

without the need for laboratory equipment [79]. Such devices closely integrate sensing with computation, and using CMOS allows on-chip signal processing and interpretation of data. One of the remarkable aspects of the natural olfactory system is that OSNs along with other simple cells combine to create a massively parallel dynamic computational system that is capable of distinguishing a great number of different odors, using just a few 100 different OSN types (more in certain animals). Using OSNs as a front-end, with CMOS circuits that can emulate this type of back-end processing will allow the development of truly bio-mimetic olfactory sensors.

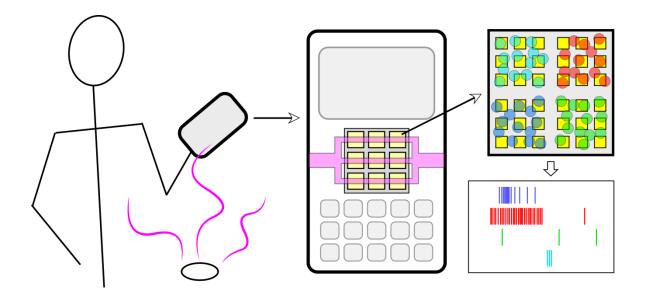


Fig. 36. Future vision for a handheld olfactory sensor. Figure credit: Dr. Elisabeth Smela

Fig. 36 shows the future vision for cell-based olfactory sensors. Currently OSNs can be used within a laboratory environment to sense stimuli as they are delivered. This technology can be extended to handheld portable systems. Microfluidics can be used to deliver odorants to

highly dense arrays of bio-engineered cells. CMOS chips can be used to sense and interpret the response of the cells to various odorants.

This work presents a hybrid-bioelectronic olfactory sensor that utilizes OSNs cultured on the surface of a CMOS integrated circuit (IC) designed to amplify the extracellular voltages produced by the cells. The resultant signals were recorded onto a computer and the response of the system to different odorant solutions was characterized. This work was done using primary cells harvested from salamanders. Amphibian cells were found to be far more robust than mammalian cells, having been shown to be electrically active for 19 days after harvesting [202], compared to typical durations of 4 [203]to 7 [204, 205] days for mammalian cells. Though, recently, mammalian (rat/mouse) OSNs have been cultured for periods of up to 2 weeks [206](the cells were not completely dissociated and large pieces of tissue remained intact). The culture requirements for amphibian cells are less strict, allowing the use of CO₂ –free media and storage in a fridge. Salamander OSNs are also significantly larger than murine cells, allowing easier identification and handling.

4.2 Materials and Methods

4.2.1 Experimental Setup

The recording setup included a CMOS IC, a printed circuit board (PCB), a commercial data acquisition system (DAQ), a computer running MATLAB software, and two syringe pumps. The IC was designed to amplify biological electrical signals, and was packaged to allow direct interface with fluidics and cells. Electrical connections between the packaged IC and the DAQ were provided by a two-tiered PCB, which was designed specifically to accommodate the packaged IC. Signals from the PCB were converted to digital format and logged by the computer using MATLAB. The syringe pumps were used to perform perfusion of chemical stimulants and cell medium to the cells cultured on the surface of the IC.

4.2.2 CMOS Device and Packaging

The CMOS amplifier circuits were based on a design originally presented in [50], which employs an operation transconductance amplifier (OTA) with the gain set by capacitive feedback. This design was chosen because it presented a good balance between system noise and total power usage. A two stage amplification scheme was used, with a total gain of 1200 (100 for the first stage, and 12 for the second stage). An operational amplifier with unity gain was used as a third stage to buffer the signals, this was necessary because of the low power nature of the amplifiers and the relatively high capacitive load presented by the DAQ (100 pF per channel).

The packaging procedure has been described in detail previously in [79]. A polymer handle wafer was formed around the CMOS IC. Electrical connections to the bondpads on the perimeter of the IC were provided by patterned thin film metal traces (Ti/Au). The sensing electrodes (normally formed at the IC foundry using a reactive material such as Al) were also covered with the Ti/Au layer to present an inert surface to the cells. The chip surface was selectively passivated with Parylene C to expose the sensing electrodes while protecting the bondpads and input output traces from the cell culture medium. An image of the packaged chip is shown in Fig. 37.

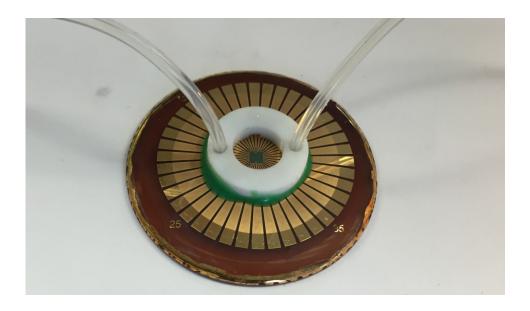


Fig. 37. The packaged chip with a perfusion chamber on its surface, the CMOS IC is at the center, metal traces are used fan out the electrical connections. Passivation was achieved using patterned Parylene.

4.2.3 PCB and DAQ

A two-level PCB was designed to interface with the packaged CMOS chip. The PCB consisted of a pair of two-layer boards used in a motherboard/daughterboard configuration with the packaged chip clamped between the two boards, as shown in Fig. 38. The on-board power source of 2 AA batteries was chosen to minimize power line noise in the system, and was contained on the lower level. The lower level also contained the potentiometers for setting bias voltages for the IC, and the headers for connecting the cables from the DAQ system. The upper level of the PCB included a decoupling capacitor and spring loaded contact pins that provided the electrical connections to the packaged chip. Electrical connections between the two tiers of the PCB were achieved by using a flat ribbon cable. An access port was milled into the top PCB to allow access to the packaged chip, the port was used to pass through the hoses for stimulant delivery, and also to allow optical assessment of the chip surface.

The DAQ system was purchased from National Instruments (NI USB-6259), and is capable of data conversion at 16 bits of resolution at a total sampling rate of 1.25 MS/s, because of the nature of the internal multiplexing scheme used within the DAQ, the maximum effective sampling rate is determined by the number of channels sampled.

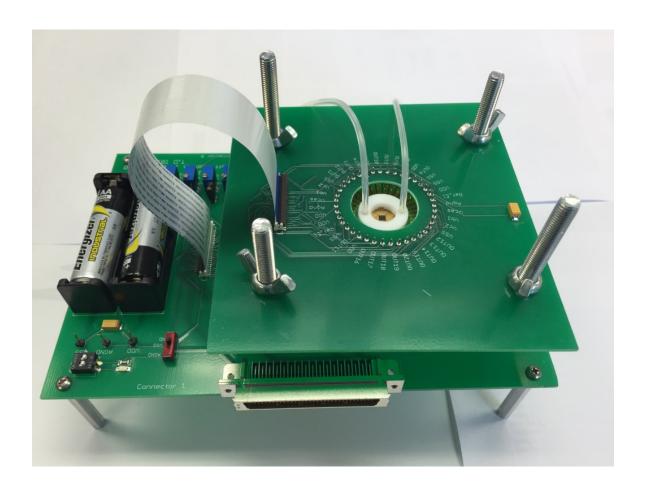


Fig. 38. An image of the two-tiered PCB used in this work. The packaged chip can be seen through the access port at the center of the top PCB.

4.2.1 Perfusion Chamber

Perfusion of odorants was performed using syringe pumps and a specially designed perfusion chamber. The perfusion paths were machined into the PTFE cell culture chamber, the total chamber dimensions were designed to limit the fluid volume to 200 μ L and to permit optical assessment using an immersion lens. During experiments the volume in the chamber was

reduced to $100~\mu L$ to enable faster clearing of the chamber contents. Three syringe pumps were used (NE-1000 New Era Pump Systems), two for infusion and one for withdrawal. 5 mL syringes were placed into the pumps and perfusion was performed at rates varying between 200- $1000~\mu L/min$. 18 gauge needles were used to connect the syringes to silicone tubing, the tubing was primed before use and plugged into ports on the perfusion chamber. Using two separate pumps for infusion allowed for quick exchange of the perfusion solution, with the second perfusion line primed and ready to be plugged into the port once the first pump finished. The design of the perfusion chamber was informed by a COMSOL simulation of fluid flow. The chamber was designed to accommodate a 1 cm internal well with 5 inlets and a single outlet. An image of the simulated fluid flow is shown in Fig. 39

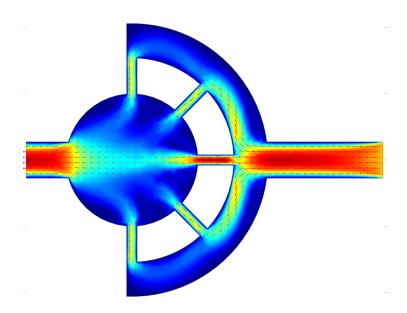


Fig. 39. A COMSOL simulation of the fluid flow in the perfusion chamber. The inlet is on the right and the outlet is on the left. Arrows indicate flow direction, and color indicates velocity, dark blue represents the lowest velocity while dark red represents the highest velocity.

4.2.2 Perfusion Solutions

Odorant solutions were prepared by mixing stock solutions of odorants into the culture media. Three stock odorant mixtures were created, each containing three odorants, and each odorant was mixed at a concentration of 20 mM in dimethyl sulfoxide (DMSO). Thus, stock solutions of odorant mixtures contained 60 mM total odorants, comprised of 20 mM of each of three odorants. Stock solutions of individual odorants were also prepared in a similar manner, 20 mM stock in DMSO. Before use, the odorant mixtures were diluted in the cell culture medium by a factor of 100, yielding 200 μM odorants in a 1% DMSO solution. Due to the volatile nature of the odorant compounds, new solutions were prepared every two days. Odorant mixture one contained: α-pinene (Sigma, 147524), geraniol (Sigma, 163333), and amyl acetate (Sigma, W504009). Odorant mixture two contained: eucalyptol (Sigma, C80601), acetophenone (Sigma, A10701), and isopentyl acetate (Sigma, 79857). Odorant mixture three contained: 2-isobutyl-3-methoxypyrazine (Sigma, 297666), linalool (Sigma, L2602), and l-carvone (Sigma, W224901).

4.2.3 Odorant Perfusion

Perfusion during each experiment followed the same basic protocol. The chamber was initially flushed with medium containing 1% DMSO (15 seconds at 1000 μ L/min with 5 additional seconds to allow for switching the solution lines, for a total time of 20 seconds). Then each odorant mixture solution was perfused (60 seconds at 200 μ L/min, with an additional 5 seconds for switching), with a 15 second flushing step in between odorant solutions. Lastly a

modified medium containing 50 mM KCl was perfused for 60 seconds after the final flushing step. If a specific cell plating was found to respond to a particular odorant mixture, the next experiment would include perfusion of only the constituent odorants of that mixture to determine which odorant had elicited the response. After experiments were performed, the cells were flushed with standard medium and the total volume was brought back to 200 µL for storage. If multiple experiments were performed on the same day, the cells were stored at 4 °C for a period of two hours between experiments.

4.2.4 Euthanasia

Animal procedures were carried out using an institutionally approved protocol. Care was taken to minimize distress to animals during handling and sacrifice. The euthanasia procedure employed is approved by both the National Research Council on Pain and Distress in Laboratory Animals, and by the American Veterinary Medicine Association. Adult tiger salamanders (Ambystoma tigrinum) were anesthetized by percutaneous application of benzocaine. A 0.02% solution of benzocaine was prepared using 990 ml aged water (tap water that was allowed to sit for 48 hours to minimize the amount of dissolved gasses and water treatment chemicals) mixed with a solution containing 10 ml of ethanol and 200 mg of benzocaine (Sigma E1501). The salamanders were placed into a shallow bath (high enough to immerse the ventral side) of the benzocaine solution and observed till anesthesia was induced (generally varying between 20-30 minutes), anesthesia was confirmed by the lack of the righting reflex once animals were turned

on their backs [207]. Following anesthesia, the animals were euthanized by decapitation and pithing.

4.2.5 Olfactory Cell Harvesting

Olfactory epithelium was dissected from the dorsal and ventral walls of the nasal cavities of the tiger salamanders. The tissue was placed into a modified amphibian Ringer's solution and cut into approximately 1.5 mm x 1.5 mm pieces using dissecting scissors. The modified Ringer's solution contained :120 mM NaCl, 2.5 mM KCl, 4 mM CaCl₂, 0.2 mM MgCl₂, 5 mM HEPES, 5 mM glucose, .5 mM EDTA, and was brought to pH 7.6 using NaOH and HCl as needed, then it was passed through a 200 nm filter for sterilization and fortified with antibiotics (100 U/ml Penicillin and 100 μ g/ml Streptomycin). During dissection and mincing, the tissue was repeatedly rinsed with the Ringer's solution to wash away as much mucus and bacteria as possible.

Cells were dissociated using a commercially available enzymatic digestion kit (Papain Dissociation System, Worthington Biochemical Corporation). Some minor adjustments were made to modify the procedure for amphibian cells and CO₂ free culture medium, as well as to minimize bacterial contamination. The minced tissue was placed in Earle's Balanced Salt Solution (EBSS) with papain (20 units/ml) activated with L-cysteine (1 mM) and containing EDTA (0.5 mM) as a metal ion sequestering agent. Prior to mixing with the lyophilized enzyme preparation, the EBSS was brought to physiological pH by bubbling a 95% O₂: 5% CO₂ mixture

through it for 5 minutes, then filtered for sterilization and fortified with 100 U/ml Penicillin and 100 μ g/ml Streptomycin. To aid in dissolving the lyophilized enzyme mixture the solution was gently swirled and placed into a 37 °C water bath for a period of 10 minutes. During this period, the solution was capped in a container in which the air had been displaced by the O_2 : CO_2 gas mixture.

The tissue was incubated in the digestion solution at 30 °C for a period of 55 minutes, with constant agitation. Then the solution was triturated gently 10 times using a standard 10 ml pipette, after which, the remaining large pieces of tissue were allowed to settle to the bottom of the tube and the turbid cell solution was removed. The cell solution was then centrifuged at 300 G for 5 minutes and the supernatant was removed and replaced with 3 ml of the sterilized and fortified EBSS, with additional protease inhibitors, ovomucoid inhibitor (1 mg/ml) and bovine serum albumin (1 mg/ml). The cell pellet was resuspended and incubated at 4 °C for 15 minutes. Though the osmolarity of amphibian medium is generally 60% of that of mammalian medium, the hyperosmolarity of the EBSS solution did not present any noticeable detrimental effects incurred during the digestion process. However, cell viability was maximized when amphibian storage medium (120 mM NaCl, 3 mM KCl, 1 mM CaCl₂, 2 mM MgCl₂, 10 mM HEPES, 5 mM glucose, at pH 7.2, fortified with 50 U/ml Penicillin and 50 µg/ml Streptomycin) was slowly added to the cell suspension (to prevent osmotic shock), bringing the total volume to 10 ml. After this, the solution was once again centrifuged at 300 G for 5 minutes, the supernatant removed, and the cell pellet resuspended in 1 ml of medium. The number of cells and their viability was

then determined by using Trypan blue staining and a hemocytometer. Typical yield was on the order of 10^6 viable cells from a procedure that included harvested olfactory epithelium from two animals.

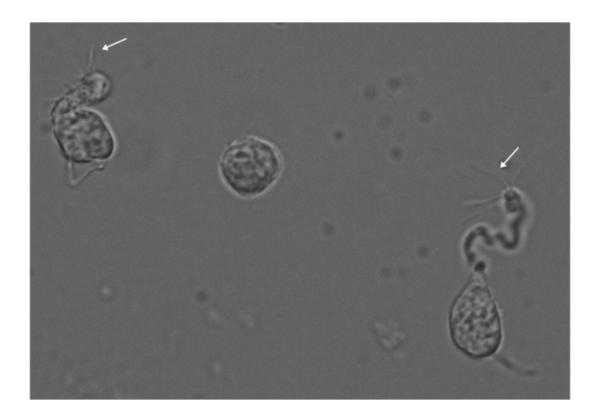


Fig. 40. Dissociated olfactory sensory neurons, the arrows indicate the cilia which house the odorant receptors. Figure credit: Dr. Ricardo Araneda.

4.2.6 Cell Plating

The packaged amplifier chips were first treated with O_2 plasma (30 seconds 100 W, 500 mTorr, 2 SCCM O_2) to render the Parylene and chip surfaces hydrophilic. The cell culture well was created by gluing a chamber made of polytetrafluoroethylene (PTFE) (1 cm diameter) to the

surface of the packaged chip using a bio-compatible silicone adhesive (Kwik-Cast Sealant, World Precision Instruments). The plating area on the chips was then incubated overnight at 4 °C with a polyethylenimine (PEI) solution. The solution was made by diluting a 50% PEI solution ([w/v] in H_2O , Sigma P3143) to a final concentration of .1% in borate buffer (155 mg boric acid Sigma B6768, 237 mg sodium tetra borate Sigma 71997, 50 ml sterile filtered water Sigma W3500, pH adjusted to 8.4 with HCl). After incubation the remaining PEI solution was aspirated and the chip surface was rinsed 4x with sterile water. Lastly the cell plating well was filled with $100~\mu l$ of a solution containing concanavalin A (Sigma L7647) 10 mg/ml in phosphate buffered saline (PBS) (Sigma D8662), the solution was allowed to settle for 1 hour at room temperature after which point the remaining liquid was aspirated. The dissociated cells were then plated at a density of 2000 cells/mm² and the total media volume was brought to 200 μl , the cells were then allowed to settle overnight before any experiments were performed. Except when performing experiments the cells were stored at 4 °C, and half of the medium was replaced every day to compensate for evaporation due to the low relative humidity in the refrigerator.

An image of OSNs and supporting cells plated on the chip surface is shown below in Fig. 41. Two electrodes that serve as differential inputs to an amplifier are seen as large squares. There are multiple cells in the image, two cells that appear to exhibit morphology that is typical of OSNs are highlighted in red. This particular image was composed of two different images taken at different focus levels, this was necessary to clearly define the edges of the cells and the electrodes. The images were taken with an immersion objective at a magnification of 40X. The

images were later combined using software to overlay the relevant portions of each image. The opaque nature of the substrate means that typical cell imaging procedures could not be used.

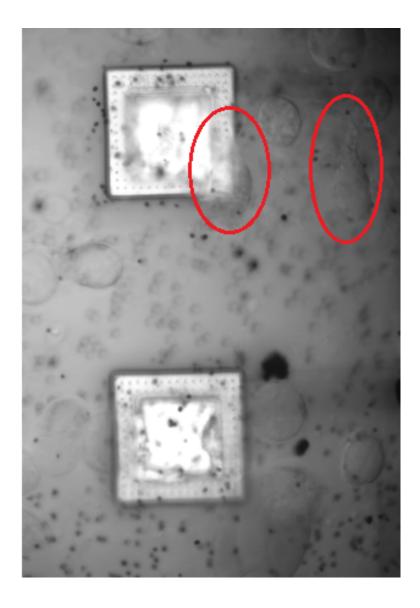


Fig. 41. An image showing OSNs and supporting cells plated on the surface of a bioamplifier chip. The field of view shows two recording electrodes surrounded by cells. The two red circles indicate cells that exhibit morphology that is typical of OSNs. This figure was composed of two different images taken at different focus levels.

4.3 Results

4.3.1 Data Collection and Processing

Voltage signals were recorded from all 20 channels simultaneously at a sampling frequency of 20 kHz and a resolution of 16 bits. In a few cases action potentials were readily identified in the raw data, however, in most cases it was necessary to filter the data to automate detection of spiking events. Significant noise was observed at the 60 Hz power line frequency as well as its harmonics up to 360 Hz. All of the raw signals were filtered using a highpass filter with 80 dB rejection and a cutoff frequency of 400 Hz. Initially, filtering was performed with a bandpass filter (400 Hz – 5 kHz) but it was found that this lead to the exaggeration of certain frequency components, and resulted in distortion of the filtered signal. A peakfinder algorithm (peakfinder.m, © Nathanael Yoder, 2013), was used to identify action potentials by looking at the temporal derivative of the signal as well as relative and absolute thresholds. An example of raw and filtered data is shown below in Fig. 42.

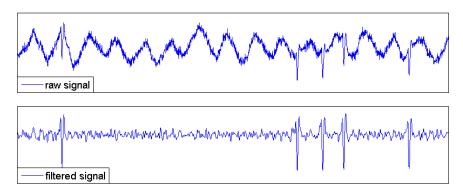


Fig. 42. Filtering of raw signals (upper trace) was necessary to clearly identify spikes (lower trace).

4.3.2 Perfusion Characterization

The perfusion system was characterized by measuring the change in conductivity between two electrodes. The PTFE perfusion chamber was placed on top of a surface on which two gold electrodes had been patterned. The chamber was filled with deionized water and the same perfusion protocol described above was followed using 1 M KCl solution (60 seconds KCl at 200 μL/min, 5 seconds wait, 15 seconds deionized water at 1000 μL/min, 5 seconds wait). This procedure was repeated 3 times. The resulting change in conductivity is shown in Fig. 43, where it can be seen that 90% of maximum concentration is reached after 30 seconds, and that a drop to 10% of the maximum concentration occurs after 5 seconds of initiating flushing.

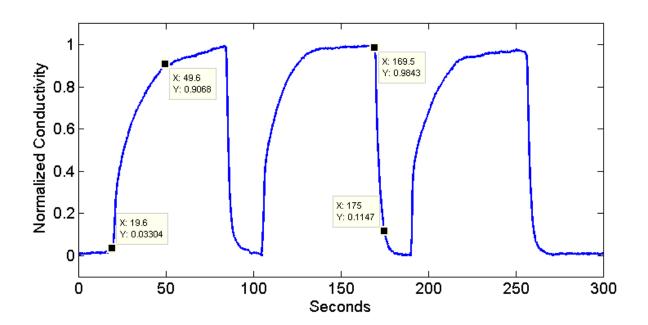


Fig. 43. Perfusion system characterization using conductivity of KCl solution (the data are normalized). The data points indicate that 90% of the maximum concentration is reached after approximately 30 seconds of perfusion, and that during flushing a drop to 10% conductivity occurs within approximately 5 seconds.

4.3.3 Recording Characterization

The recording capability of the system was characterized before experiments with OSNs were performed. Commercially available primary rat cortex neurons were used to characterize device functionality. The chip was coated with PEI solution, and cryopreserved neurons (Invitrogen, A10840-01) were thawed and plated on its surface. The thawing and plating procedure for the neurons was the standard procedure provided by the supplier. Briefly, the vial containing the cells was thawed rapidly in a 37 °C water bath, the cells were transferred to a tube that had been previously rinsed with prepared media, 1 ml of media was added drop by drop to the thawed cells to prevent osmotic shock, an additional 2 ml was then added slowly to bring the total volume to 4 ml. Cell viability was determined using Trypan blue staining, and the cells were plated on the chip surface at density of 100 cells/mm². The cell medium was Neurobasal Medium (Invitrogen 21103-049) supplemented with 2% B-27 serum-free supplement (Invitrogen 17504-044), and .5 mM GlutaMax (Invitrogen 35050-061). Cells were cultured overnight in a 37 °C incubator (5% CO²:95% air).

Recording experiments were performed 24 hours after plating. The low cell plating density was chosen so that spikes from individual neurons could be identified by amplitude. A typical action potential from a cortical neuron is shown in Fig. 44.

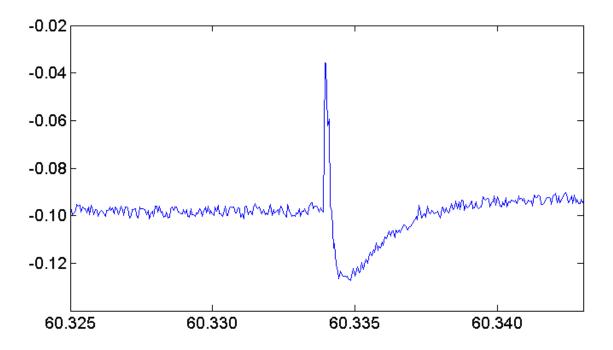


Fig. 44. An action potential from a cortical neuron, the signal is raw and unfiltered. The horizontal axis is time; the vertical axis is the amplified potential. The x-axis is in seconds, the y-axis is in volts.

Given the low plating density, a few electrodes were able to record signals from single neurons, while another electrode was able to record from multiple (3) neurons simultaneously. Signal amplitudes along with estimated distances from the electrodes were used to determine a basic relationship between distance and expected amplitude (Fig. 45). It should be noted however that the data required filtering before spikes could be sorted and analyzed, the filtering resulted in attenuation of part of the signal amplitude, because of this, the plot shown in Fig. 45B should be considered a normalized plot.

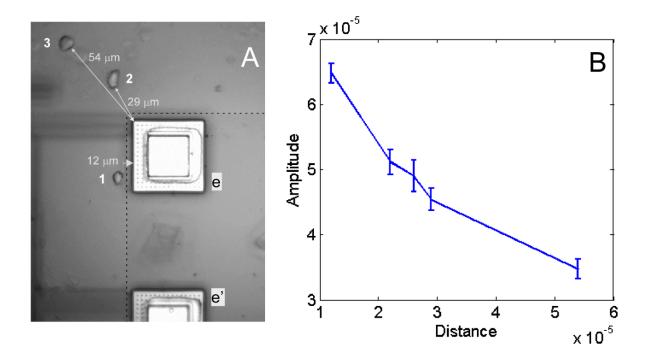


Fig. 45. Determination of the relationship between neuron distance and measured signal amplitude. A) shows 3 neurons next to a recording electrode, the differential inputs to the amplifier are formed by electrodes e and e'. B) Shows the measured signal amplitude and standard deviation as a function of distance. The plot on the right has absolute units of volts and meters. The original images used to compose figure A are part of the experimental work performed by the author, credit for the preparation of the figure is due to Dr. Elisabeth Smela.

4.3.4 Response of OSNs to Stimulation

Recording experiments with OSNs were performed using multiple chips. Exposure to stimulants was performed approximately 24 hours after cell plating. For each chip the following procedure was carried out. On day 1 (24 hours after plating), the cells were sequentially exposed to the three odorant mixtures followed by KCl. If a response to an odorant mixture was observed, then the constituent odorants of that mixture were perfused over the OSNs to determine which odorant elicited the response. On the following days, only the constituent odorants were applied

to the cells, experiments were repeated daily till no response was observed. A summary of all the results is shown in Fig. 46.

Chip	1				2				3				3			
Channel	13				13				14				9			
Mix	1	2	3	KCl	1	2	3	KCI	1	2	3	KCI	1	2	3	KCI
day 1, all																
day 1																
day 2																
day 3																
day 4																
Channel					17				15				13			
day 1, all																
day 1																
day 2																
day 3																
day 4																

Fig. 46. A summary of the results of the experiments performed with OSNs. Three devices were used, chips 1,2, and 3. The first experiment performed was to expose the each chip to all three odorant mixtures. If a response was recorded, then the constituent odorants from the mixture were then applied to the chip. Gray indicates exposure; red indicates response to odorants, yellow indicates response to KCl. Figure credit: Dr. Elisabeth Smela.

The olfactory sensor was capable of distinguishing between different odors. To illustrate this and the experimental procedure that was followed, the data set from the third column of Fig. 46 will be shown below. Fig. 47 and Fig. 48 show recorded signals from two responding channels when all three odorant mixtures were applied to the cells. In each figure the top trace shows the filtered signal and the lower trace shows the histogram data, indicating firing rates in spikes/second (the thin blue line represents the actual histogram data, while the thicker black line is a smoothed version of the same signal. The results from Fig. 47 and Fig. 48 indicate that a neuron at electrode 14 is responding to odorant mixture 3, and that a neuron at electrode 15 is

responding to odorant mixture 2. Using this information the next set of experiments, performed approximately 2 hours later on the same day, exposed the neurons to the constituent components of odorants mixtures 2 and 3 (as indicated by syringe (syr) 1,2,3). Fig. 49 and Fig. 50 show the responses of the same two neurons to the components of odorant mixture 2. In this case it can be seen that the neuron at electrode 14 responds only to the KCl stimulant, and that the neuron on electrode 15 responds to the second component of odorant mixture 2 (acetophenone). Fig. 51 and Fig. 52 show the responses of the neurons to the third experiment performed on day 1, exposure of the neurons to the constituent components of odorant mixture 3. For the third experiment, it is apparent that the neuron on electrode 14 responds to the third component of odorant mixture three (1-carvone), while the neuron on electrode 15 only responds to the KCl stimulant.

Exposure to the constituent components of odorant mixtures 2 and 3 (hereafter referred to as odorant sequences 2 and 3) were repeated on the following days till no responses were observed. Fig. 53 and Fig. 54 show the responses on day 2 to odorant sequence 2. Fig. 55 and Fig. 56 show the responses on day 2 to odorant sequence 3. Fig. 57 and Fig. 58 show the responses on day 3 to odorant sequence 2. Fig. 59 and Fig. 60 show the responses on day 3 to odorant sequence 3. On day 4 it was observed that no signal was recorded from channel 14. Fig. 61 shows the response observed on channel 14 on day 4 to odorant sequence 2. Fig. 62 shows the response observed on channel 14 on day 4 to odorant sequence 3.

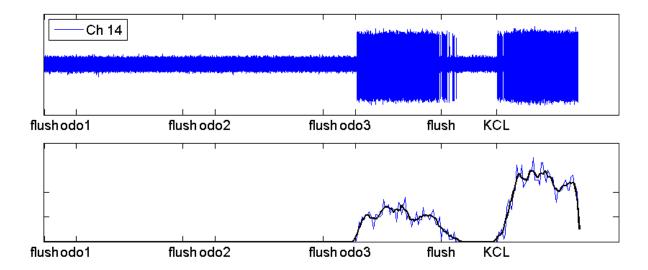


Fig. 47. Results from chip 3, day 1, channel 14. Recordings were taken 24 hours after plating. The cells were exposed to all three odorant mixtures. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. The neuron shows a distinct response to odorant mixture 3 and KCl.

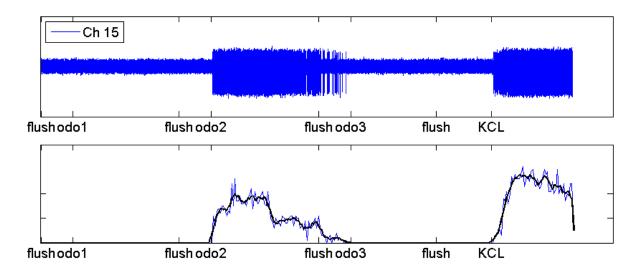


Fig. 48. Results from chip 3, day 1, channel 15. Recordings were taken 24 hours after plating. The cells were exposed to all three odorant mixtures. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. The neuron shows a distinct response to odorant mixture 2 and KCl.

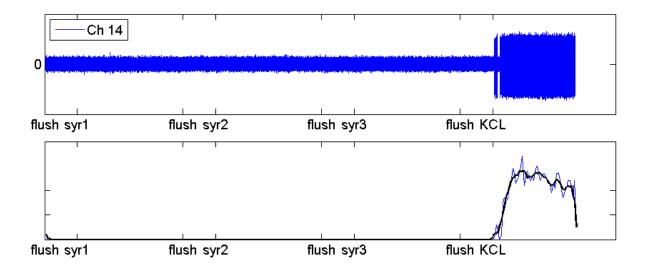


Fig. 49. Results from chip 3, day 1, channel 14. Recordings were taken 24 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

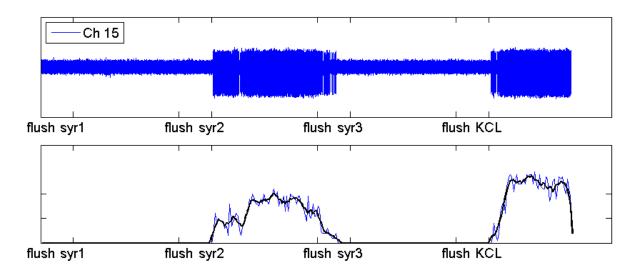


Fig. 50. Results from chip 3, day 1, channel 15. Recordings were taken 24 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the second component of odorant mixture 2 and KCl.

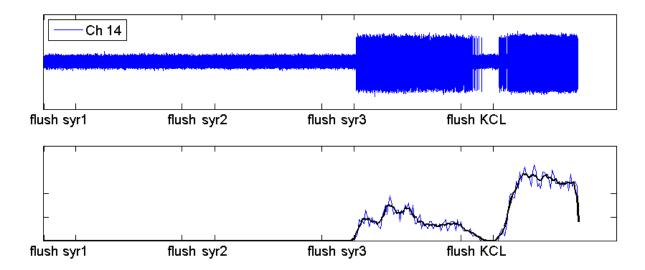


Fig. 51. Results from chip 3, day 1, channel 14. Recordings were taken 24 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the third component of odorant mixture 3 and KCl.

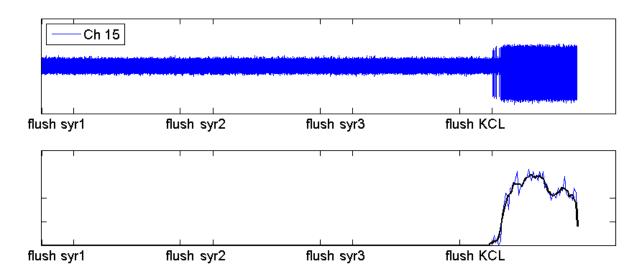


Fig. 52. Results from chip 3, day 1, channel 15. Recordings were taken 24 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

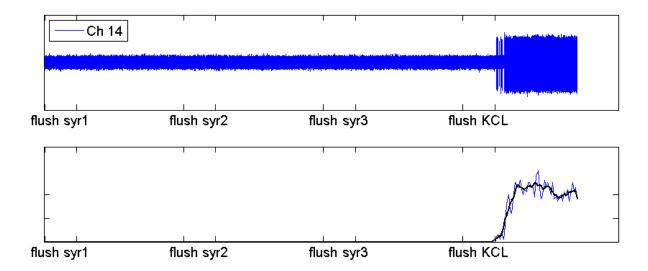


Fig. 53. Results from chip 3, day 2, channel 14. Recordings were taken 48 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

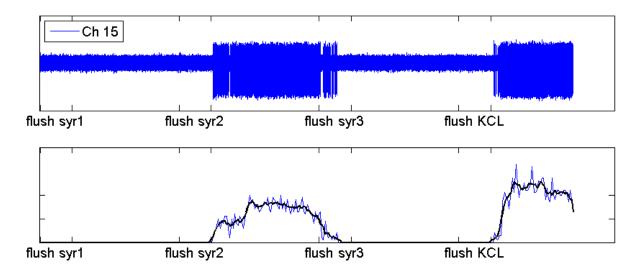


Fig. 54. Results from chip 3, day 2, channel 15. Recordings were taken 48 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the second component of odorant mixture 2 and KCl.

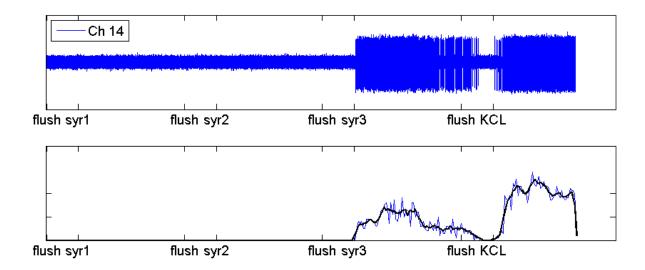


Fig. 55. Results from chip 3, day 2, channel 14. Recordings were taken 48 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the third component of odorant mixture 3 and KCl.

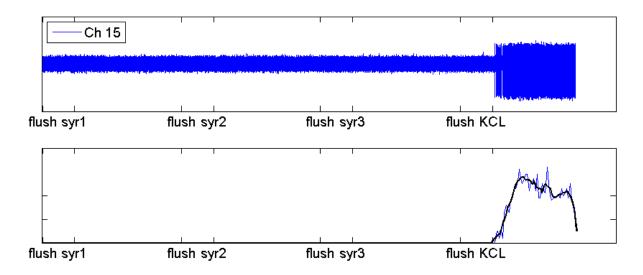


Fig. 56. Results from chip 3, day 2, channel 15. Recordings were taken 48 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

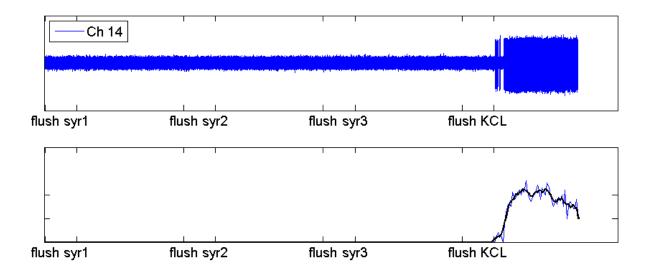


Fig. 57. Results from chip 3, day 3, channel 14. Recordings were taken 72 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

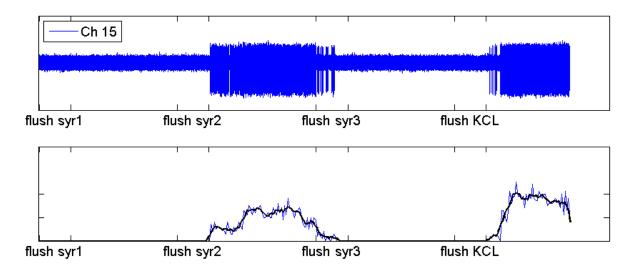


Fig. 58. Results from chip 3, day 3, channel 15. Recordings were taken 72 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the second component of odorant mixture 2 and KCl.

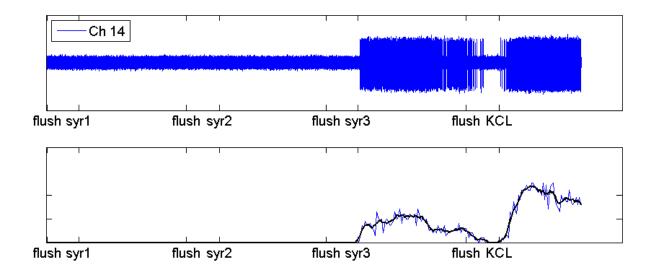


Fig. 59. Results from chip 3, day 3, channel 14. Recordings were taken 72 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the third component of odorant mixture 3 and KCl.

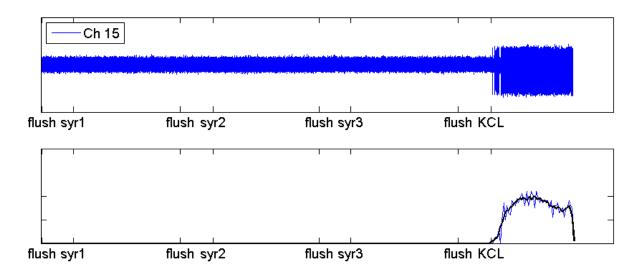


Fig. 60. Results from chip 3, day 3, channel 15. Recordings were taken 72 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 15. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

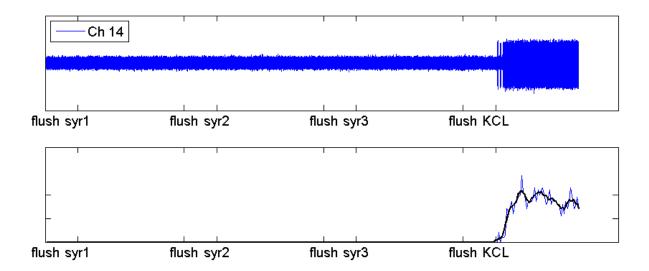


Fig. 61. Results from chip 3, day 4, channel 14. Recordings were taken 96 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 2. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron only shows a response to KCl.

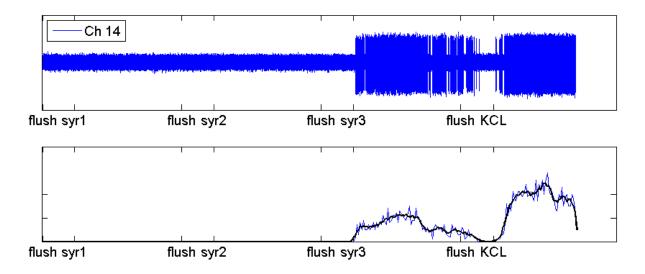


Fig. 62. Results from chip 3, day 4, channel 14. Recordings were taken 96 hours after plating. The cells were exposed to the constituent odorants of odorant mixture 3. The top trace shows the response recorded on channel 14. The bottom trace shows a normalized histogram showing spikes per second, the thin blue trace is the raw histogram, the wider black trace is a smoothed version of the histogram. This neuron shows responses to the third component of odorant mixture 3 and KCl.

The above figures indicate the basic functionality of the device as an odorant sensor. However, more information can be gleaned from the data set. Looking at the various figures it can be seen that as the experiments progress the maximum firing rates of the neurons decrease. This is likely an indicator of the health of the cell. Interestingly, even though the maximum firing rates decreased over time, the shape of the histogram did not change significantly. For example, looking at the histogram of the firing rates observed on channel 14 in response to KCl stimulation it can be seen that on the first day the maximum firing rate exceeded 30 spikes/second, but that on the fourth day the maximum firing rate barely exceeded 20 spikes/second. However, when all of the histograms are synchronized in time and normalized relative to the maximum firing rate they appear to follow the same general profile, as indicated below in Fig. 63. Seemingly indicating that the relative firing rates within a particular experiment are closely tied to the stimulant concentration (as indicated in Fig. 43).

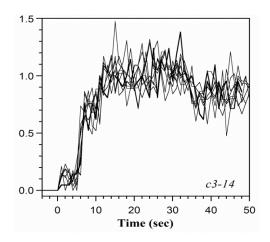


Fig. 63. Normalized histograms over the course of 4 days of the recordings on channel 14. Though the maximum firing rate decreases over time, the profile of the histogram remains the same. Figure credit: Dr. Elisabeth Smela.

Looking at the data it is also possible to extract more information about the response of the system to stimulants. The dynamic of the response can be used to characterize the system as a whole, as well the cells themselves. With regard to the system dynamics, the data can yield response times (time to first spike after stimulant introduction), as well as time course of firing rates (e.g. how long it takes till the neurons reach maximum firing rates). Regarding the individual cells rudimentary analysis of the spiking data can be used to extract the spike signal shape. Although all of these recordings came from single neurons, the analysis of the spike shape can be used in future systems to determine which neuron is firing when multiple neurons are firing on the same channel (multi-unit recording). An example of extracted spike shapes is shown in Fig. 64, in which two characteristics spike shapes are displayed as overlaid signals synchronized in time.

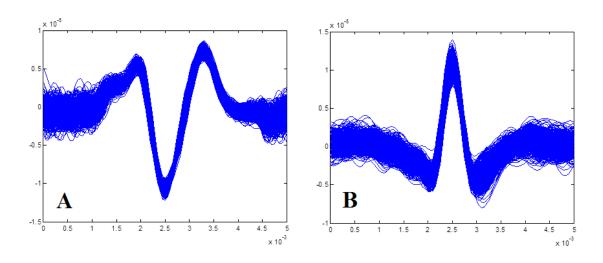


Fig. 64. Two overlays of spikes from individual neurons, each plot consists of approximately 500 spike synchronized in time. The data come from the second set of experiments performed with chip 3. A) is from channel 9, and B) is from channel 13. It is evident from this figure that the dynamics of the spike shape can be used to identify individual neurons.

4.4 Discussion

As shown here, bioelectronic noses can be fabricated without the need for large laboratory equipment. By using CMOS ICs, all electronic sensing and signal processing can be performed at the millimeter scale. Furthermore, integration of custom CMOS ICs with off the shelf microprocessors and memory elements can be used to create a self-contained hand held device. Sample handling and delivery can be performed using microfluidics, and long term maintenance of the front-end sensing infrastructure can be performed by the cells themselves.

Some of the disadvantages of the methods employed here are the following. First, the cells have a limited lifetime, and long-term development of this technology will require immortalized cell lines with known olfactory response profiles. Secondly, using the method of cell dissociation from harvested tissue results in a relatively low yield of actual OSNs, this problem can be alleviated by using cell sorting, but again this is an area where custom bioengineered cell lines could be used solve the problem entirely. The last problem stems from a combination of low OSN yield and lack of high density neural recording sites. Using the particular amplifiers and technology employed in this design, the number of sensing sites on the chip surface is low, and occupies a very small proportion of the total chip surface area. This low-density combined with the fact that there is little to no control of where on the chip surface the cells will end up, means that it is critical to increase the number of OSNs and sensing site density.

Chapter. 5

Active Spike Detection

5.1 Preface

This chapter is a reproduction of [208], a publication with multiple authors. This material also serves as the basis for a future article that is currently under preparation. My own contributions to this work include the conceptualization of the core idea, development of the system architecture, a significant portion of the simulations, integration of the VLSI layout of the IC, and most of the writing.

5.2 Abstract

We present an active micro-electrode array for neural recording with integrated spike detection and an asynchronous readout architecture. Neural amplifier arrays generate voluminous data because of the necessary per-channel sampling rates and number of channels in a dense array. Most of the time, neural cells produce well below 100 spikes per second, with action potential durations generally on the order of 1 ms, and accordingly much of the recorded data from a neural amplifier is not of interest. In the case of dense arrays recording from single units, only the timing of action potentials is relevant and spike sorting is not required. In such a

case, the bandwidth requirement of the neural array can be reduced by employing an event-driven data communication protocol such as address event representation (AER). In our array, these events are generated by the spike detection circuits and then relayed to AER modules that send the address of the spiking neuron off-chip using a digital encoding scheme. Based on simulation data, the system implemented here reduces bandwidth requirements by a factor of 1600 in comparison to traditional synchronous sampling.

Keywords—AER; neural amplifier; bio-potential; spike detection; NEO

5.3 Introduction

Bio-potential recording systems have many potential commercial and research applications ranging from *in-vivo* implantable systems for basic neuroscience research to portable *in-vitro* cell-based sensing platforms [91]. In all cases the goal of such systems is to detect and amplify the extracellular potentials of cells that are communicating with each other and responding to their environment. The action potentials (APs) produced by neurons and muscle cells are inherently sparse and of short duration. The biphasic waveforms have time periods as short as 250 µs [209], necessitating sampling rates on the order of 40k samples per sec. Using a typical 16 bit data acquisition system this sampling rate would result in 80 kB of data per second, so for a 32 channel array this would result in approximately 154 MB of data per minute. Acquiring bio-potentials over periods of time on the order of tens of minutes results in

unwieldy files that are difficult to store and manipulate for data processing after recording. Since the signals of interest are actually sparse, much of this data is not of any use.

The issues of sparsity and bandwidth have led to interest in the development of biopotential recording systems containing readout architectures with lower bandwidth requirements.

One approach has been to use an ASIC for embedded data compression [210], which led to a
factor of 11 reduction in bandwidth. Systems have also been developed that employ
asynchronous delta analog-to-digital conversion that only activates the data converter when the
input signal is changing [211]. Event driven data management schemes that buffer the incoming
neural signal and only transmit a limited portion of the signal upon the detection of an event have
also been introduced [212]. Additionally, multi-chip systems have been designed that perform
AP detection and signal conditioning as well as bandwidth reduction [213], achieving a
bandwidth reduction of 48. The front-end neural recording and on-chip signal conditioning are
critical design features for neural recording arrays [214].

Reference	Spike Detection Method	Feature Size (µm)	Density (channels/mm²)	Power Consumed per Channel (µw)	
[213]	rectification & threshold	0.18	3.85	138	8
[211]	threshold	0.5	1.77	125	960
[215]	biphasic threshold	0.5	NA	NA	8
[210]	biphasic threshold	0.5	1.23	170	11
[71]	threshold	1.5	NA	NA	14
this work	NEO	0.5	1.77	503*	1600

TABLE I. PERFORMANCE COMPARISON

^{*}Obtained from a fabricated chip with test circuits.

To provide greater utility in basic science and portable sensor applications, neural recording arrays could provide high density and integrated signal processing to reduce bandwidth usage when communicating information off-chip. A tradeoff exists between bandwidth reduction and spike feature extraction. Table 1. summarizes several relevant neural recording arrays that offer spike detection and bandwidth reduction. Many of the systems in Table. 1 included some form of feature extraction, such as spike amplitude or even a short sampled spike waveform. Spike detection alone suffices for single unit (single cell) recordings. Multi-unit recording may require additional feature extraction to enable subsequent spike sorting (i.e., the identification of the firing neuron). As the array density increases, the requirements for multi-unit processing will diminish.

In this work we present an active microelectrode array with neural amplification and spike detection integrated in-pixel, with events from the spike detectors fed into an event-driven readout system that outputs digital address bits to an off-chip data acquisition system (DAQ). The system provides a bandwidth reduction factor (BRF) of 1600, which arises from matching an asynchronous signal source to an asynchronous readout scheme.

5.4 System Overview

A system block diagram is shown in Fig. 65. The entire system is integrated as a sensor array within a single ASIC that connects to an external DAQ. Each independent signal processing chain comprises an electrode pair that feeds into a neural amplifier, a nonlinear spike

emphasis circuit, and an asynchronous readout bus. The amplifiers boost the signal power of the extracellular APs. The nonlinear signal processing emphasizes spikes and suppresses noise. The asynchronous readout (labeled as AER) generates "events" in the form of digital pulses in response to detected spikes. The addresses of the detected spikes are then placed on the bus and sent off-chip.

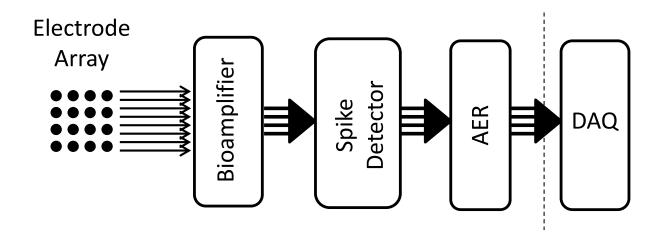


Fig. 65. System block diagram.

The electrode array is formed in the top metal layer of a 0.5 µm 3M2P CMOS technology. Glass cuts in the top passivation layer allow the electrodes to be exposed to cell culture medium. As previously described [79], the electrodes are processed post-fabrication to include gold and conjugated polymer coatings for biocompatibility and decreased interfacial impedance. The gold and polymer coating are suitable for cell culture for durations of 30 days; other materials should be considered for chronic recordings.

5.5 System Components

5.5.1 Bioamplifier

The bioamplifier uses an operational transconductance amplifier with capacitive feedback [50]. The midband gain is designed to be 46 dB by setting input and feedback capacitors to 20 pF and 100 fF, respectively. The high and low frequency roll-offs were measured at 8.1 kHz and 280 mHz. The experimentally measured gain on fabricated chips was found to be only 39 dB, presumably due to parasitic capacitances.

5.5.2 Spike Detection

For high density recording, the detection of spikes on-chip, in real-time, is of practical importance. Even for modest channel density, the communication bandwidth quickly becomes the limiting factor in overall system design [210]. Data transmission requirements increase super-linearly with the number of active input channels since data rates scale with the number of channels, and practical systems must include redundant inputs to compensate for underutilized channels. Power dissipation increases correspondingly with the total number of channels. Detection of neural spikes prior to transmission can reduce data rates and power requirements by suppressing extraneous data and allowing for transmission of only relevant activity in the neural recordings.

Over the past decade, several algorithms have been proposed for neural spike detection, from simple thresholding to energy-based computations. The nonlinear energy operator (NEO) [216] has been used in several applications [69, 217-219] in both analog and digital implementations. The NEO algorithm emphasizes both signal amplitude and high frequency energy content, and it is defined as:

$$\psi_{NEO}(x(t)) = \left(\frac{dx(t)}{dt}\right)^2 - x(t)\left(\frac{d^2x(t)}{dt^2}\right)$$

NEO performance degrades when spike amplitudes are small relative to low-frequency components of the input. To mitigate this, we evaluated two other energy-based algorithms: the frequency-enhanced NEO (fNEO), and the energy-of-derivative (ED) [220], defined as:

$$\psi_{fNEO}(x(t)) = \left(\frac{d^2x(t)}{dt^2}\right)^2 - \frac{dx(t)}{dt}\left(\frac{d^3x(t)}{dt^3}\right)$$

$$\psi_{ED}(x(t)) = \left(\frac{dx(t)}{dt}\right)^2$$

The ED and fNEO modify/remove the NEO term that includes the original signal amplitude; all three methods emphasize the high frequency content of the input signal.

5.5.3 Algorithmic Evaluation

The selection of an efficient and robust algorithm for neural spike detection is important due to the inherently noisy environment encountered during neural recording. In this work the

ED, NEO, and fNEO algorithms were analyzed numerically with real extracellular cortical neuron data previously recorded using commercial electrophysiology hardware at the Neural Systems Lab at the Institute for Systems Research. Fig. 66 shows a 50 ms duration representative sample of the neural data, which had neural spike amplitudes of 6 μ V. The recordings had a corresponding file with manually identified spike times, providing a comparison for the spike detection algorithms.

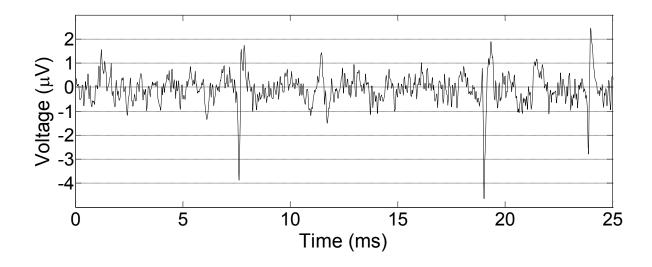


Fig. 66. Raw spike data used for analysis.

Each algorithm was applied to the raw data to provide an output waveform. The outputs were normalized and passed through a threshold detection scheme to designate detected spikes.

Receiver operating characteristics (ROCs) were generated for each algorithm by sweeping the detection threshold level. This compares the true positive rate (TPR) as a function of false positives. Several ROC curves were generated by varying two input parameters: signal

to noise ratio (SNR) and common-mode signal variation. Families of data sets were generated to evaluate the effect of SNR by increasing the power of additive white noise. Similarly families of data sets were generated to evaluate the effect of common-mode variation by increasing the amplitude of an additive low-frequency common-mode signal. The white noise and low frequency signals were added to the raw spike data shown in Fig. 66. The best performing algorithm would ideally increase steeply for a low false positive rate (i.e. follow the y-axis) and thereafter flatten out to a TPR of 1.

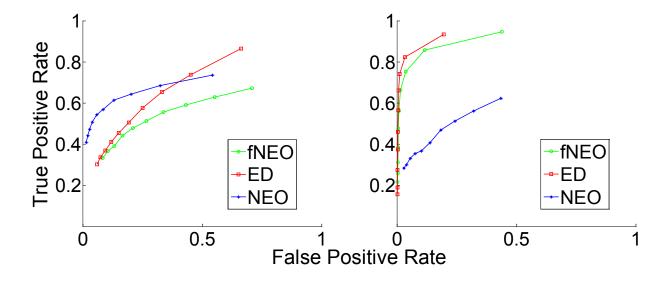


Fig. 67. Left: ROC for signal to SNR of 2.5. Right: ROC for a signal to common mode amplitude ratio of 0.3.

Fig. 67 shows the ROC curves for the three algorithms. The NEO and fNEO algorithms were evaluated using both discrete and continuous time representations; results were similar and the continuous time versions are shown on the ROC plots. As expected, all three performed better with higher SNR (left panel), with the NEO generally performing the best. On the other

hand, for large common-mode signal (right panel) the NEO performed poorly for variations in common-mode voltage, while the EOD and fNEOs performed well.

In this work we expect low SNRs in the experimental neural recording setup to have the greatest impact on the success of spike detection. Common-mode variations are expected to have modest impact on spike detection due to a pre-amplification stage that was designed to reject low-frequency common-mode signals, thus minimizing feed-through to the spike detection stage. As such, the NEO algorithm was chosen for implementing the spike emphasis circuit in this work.

5.5.4 Circuit Implementation

The NEO algorithm requires three fundamental computations: a time-derivative, a multiplication, and a subtraction.

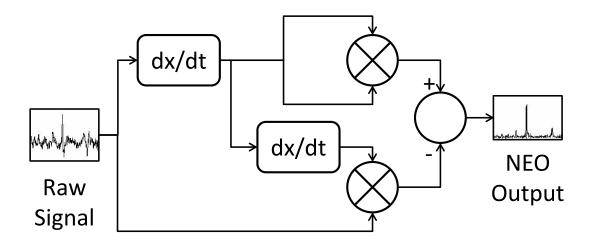


Fig. 68. Block diagram of the NEO circuit.

A derivative circuit based on a digital inverter was used in this design [221]. An input capacitor fed to a high-gain inverting amplifier with negative feedback through a Tobi element that provided high impedance [222]. A translinear four-quadrant multiplier was used in this design [223]. The core component of this circuit consisted of a voltage loop created by six PMOS transistors. Two differential input currents were provided to the circuit, and the final product was a differential current output. A simple current subtractor was used to compute the final result.

Several other circuits were used in the overall spike detection system. These included differential signal generation, voltage-smoothing, digital pulse generation, and signal filtering. The final spike detection circuit consisted of two derivative circuits, three single-ended to differential-ended signal converters, two multipliers, one current subtractor, one comparator, four filters, one peak detector, and corresponding biasing transistors as shown in Fig. 68. Additional inverters were added for digital pulse generation.

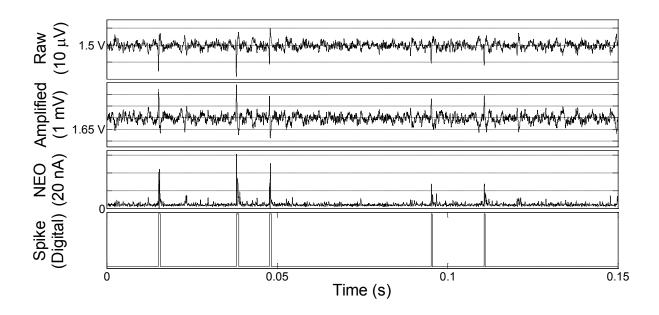


Fig. 69. Simulation results for the NEO. The traces are ordered from top to bottom as follows: the input to the neural amplifier, the output of the amplifier, the current mode output of the NEO circuit, and the pulse output of the event generator. The units in parentheses refer to the grid line spacing.

5.5.5 Simulations

Several simulations were performed to ascertain circuit performance and functionality. These included variations in the raw signal between real and artificial spike data, variations in common-mode voltage and frequencies, the effects of a non-ideal power supply, and fabrication mismatch. Fig. 69 shows the signal chain from input to event-based output. Fig. 70 shows a side-by-side comparison of the NEO output obtained from numerical and transistor level simulations.

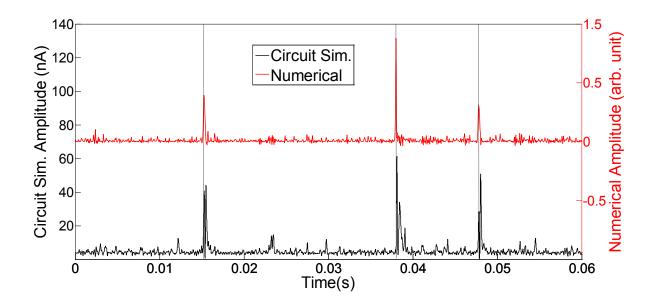


Fig. 70. Comparison of numerical (top) and transistor level (bottom) implementations of NEO algorithm.

5.6 Asynchronous Readout

The address-event representation (AER) interface protocol has been widely used in neuromorphic systems [224], digital circuits [225], and software [226] for inter-chip or multichip communication.

The AER system was adapted from [227]. The amount of time the address bits stayed on the bus was increased to compensate for the settling time of the off-chip DAQ. An edge detector was added at the input of each event generator to shorten the incoming pulse since the input from the NEO shares the millisecond scale duration of an AP. Each amplifier and spike detector block fed into an event generator as shown in Fig. 71. The event generators sent out row and column requests when spikes occurred. The requests were sent to arbiters that determined the temporal

order for the row and column addresses to be sent to the address encoders. The system could run in two modes. The first requiring an external acknowledge signal, and the second was an autonomous mode wherein addresses existed on the bus for a duration specified by an external bias.

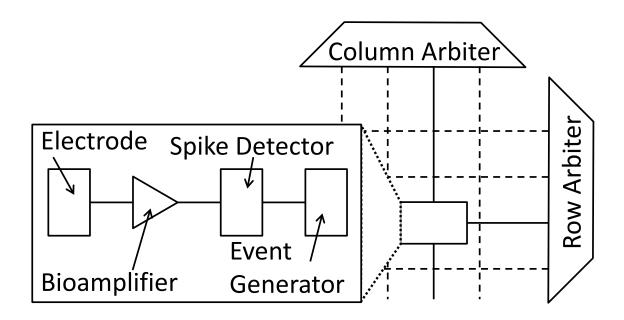


Fig. 71. Block diagram of the AER system showing the sensor interface to the event generator.

For a 16 channel interface the AER system used 8 bits in total for addressing. With a typical firing rate of 50 AP/s, this amounts to a data rate of 50 B/s, reduced from 80 kB/s and yielding a BRF of 1600.

5.7 Conclusion

A neural recording array with integrated spike emphasis and active readout was introduced. The spike detection methodology was discussed and simulation results were shown that used data recorded from the auditory cortex of a ferret. This system is being developed for use in active micro-electrode array platforms for cell-based sensing. The performance of the system is compared to the state-of-the-art in Table I. The most comparable bandwidth reduction factor of 960 [211] was reported using 12 bit data conversion at 80k samples/s for 50 AP/s. If the same conditions had been used to calculate the BRF of this work, the value would increase from 1600 to 2400. It should, however, be noted that the data reduction scheme employed in [211] allows reconstruction of the analog waveform, whereas the method used in this work does not.

5.7.1.a Acknowledgment

The authors would like to acknowledge MOSIS for chip fabrication. We would also like to thank Jonathan Fritz, Ping-Bo Yin, and Diego Elgueda of the Neural Systems Lab in the Institute for Systems Research for providing neural recording data.

Chapter. 6

Conclusion

6.1 Summary

This work has developed a number of different technologies and methods to create devices that intimately combine CMOS ICs with traditional LOC functions like fluidics, cell culture, and signal transduction. CMOS and LOC systems show promise in the future for many applications beyond what has been shown in this work. The foundations introduced here will enable not only integration of CMOS into LOC systems, but will allow new opportunities for CMOS-based sensors beyond the platform of LOC.

The cell-based olfactory sensor introduced here will serve as a proof-of-concept device for the development of more advanced olfactory sensors. The technologies demonstrated here can be combined with existing and future technologies to develop portable handheld olfactory sensors, finally allowing olfactory sensing without the use of highly trained animals.

The interfacing technologies introduced here, namely on-chip spike detection with asynchronous readout opens the doors for truly autonomous and sophisticated brain machine

interface systems. The readout method is highly amenable for future high density interfaces since it scales with the logarithm of the array dimension.

6.2 Technical Contributions

6.2.1 Packaging CMOS for fluidic interface

The packaging method discussed in Chapter. 2 tackled the issues encountered when integrating electronics with fluidics and introduces a number of original contributions. The fundamental contributions of the method are that it allows any size CMOS chip to be packaged in a way that allows standard microfabrication techniques to be applied for further integration of sensing and fluidic structures.

6.2.1.a Robust integration of CMOS with fluidics

There are a myriad of applications that can benefit from direct integration of CMOS and fluidics, in the LOC field as well as other areas. Unfortunately, intimate integration of CMOS with fluidics has proved to be challenging. The literature shows many examples of contributions dedicated entirely to packaging CMOS chips for integration with fluidics. Articles that introduce LOC or LOC-like systems that integrate CMOS generally dedicate a large portion of their discussion to the problem of integration. LOC integration generally requires unpackaged chips, (standard CMOS packages are not amenable to most types of integration). Using the CMOS chips for sensing requires the surface to be exposed and integration of additional structures

requires a flat surface. The packaging method introduced in Chapter. 2 presented a robust solution to this problem. The primary techniques that led to this result were the development of the patternable passivation scheme (Parylene) and embedding of the IC in a handle wafer. This packaging method uses thin-film interconnects instead of traditional bond wires, providing a surface that is flat and allows fluidic integration using standard soft-lithography techniques.

6.2.1.b Size mismatch between CMOS and fluidics

CMOS chips are small. Their size is determined primarily by their cost. The rate of progression of modern CMOS technology means that a lot of electrical functionality can be fit into a very small area. However, though the field of microfluidics deals with manipulation of small volumes of fluids, the actual size of microfluidics structures is typically on the order of cm² because of infrastructure such as fluidic ports and hoses. Thus there exists a size mismatch between ICs and microfluidics structures, which presents an obstacle to integrating microfluidics directly on the surface of a CMOS IC. The epoxy handle wafer used in the packaging process overcomes this issue by adding usable surface area around the IC, thus enabling integration with larger microfluidic structures.

6.2.1.c Accommodate any chip size

A key aspect of the packaging method is that it can accommodate any chip size. As previously mentioned, chip dimensions can vary between batches and even within a batch.

Embedded-chip packaging techniques must accommodate the size of the chip and leave minimal

gap between the chip and the carrier substrate. Typically, the hole for the chip is made using a microfabrication process such as DRIE, which requires an etch mask that matches the chip dimensions. A key issue for many of the chip-in-hole type packages discussed in Chapter. 2 was minimizing the gap between the chip and the handle substrate. A gap prevents continuity of the patterned metal traces, and can inhibit microfabrication by preventing proper application of photoresist. As such, many of the other packaging methods in the literature use complex methods to minimize the gap. By using a polymer to form a handle wafer around the chip, this problem is made a non-issue since the hole in the handle wafer assumes the dimensions of the chip automatically, thus eliminating any gap and allowing the same procedures to be applied to any size IC.

6.2.1.d Enabling microsystem integration

For systems that require added functionality from additional structures or features, microfabrication has been the method of choice for post-processing on the surface of the chip. This is because microfabrication and photolithography are the only techniques that can create features the same size as those on the surface of the CMOS IC.

In general, microfabrication that uses photolithography to define features has three requirements, first that the surface be flat so that photoresist can be applied, second that the photoresist can be applied in a uniform manner, and third that the die be large enough to be used in standard clean room equipment. Though a CMOS die is flat, spinning resist on its surface

leads to significant edge beading, which prohibits proper photolithographic performance. By embedding the chip in a handle wafer, the effective area is increased allowing easy handling and use in standard equipment that was designed for use with wafer. Furthermore, any resist edge bead is moved to the periphery of the handle wafer where it can be removed using standard edge bead removal techniques.

6.2.1.d.i Patterned PEDOT Deposition

As mentioned in Chapter. 2, the deposition of PEDOT on the surface of sensing electrodes greatly reduces their effective impedance. There are two ways by which PEDOT is deposited, the first method is similar to the application of resist where a solution containing PEDOT:PSS is spun onto the surface of the device, the second method is to deposit it using electrodeposition. Electrodeposition results in high quality PEDOT structures, and when done on a masked surface it allows patterned features. However, as a polymer PEDOT is subject to attack by many of the processes used during microfabrication. The technique of protecting the PEDOT with a layer of resist circumvents this issue and allows PEDOT structures deposited at the initial stage of post-processing to survive the entire integration process.

6.2.1.d.ii Co-location of multiple chips

A byproduct of using a polymer handle wafer is that multiple ICs can be co-located into the same integrated system. This allows greater and more complex sensing and processing capabilities. Similarly, passive devices can also be integrated into the handle wafer, thus freeing

up precious silicon real estate for other purposes. Though not directly demonstrated in the work presented here, the polymer handle wafer technique is easily extended to include this feature.

6.2.2 Hardware interface for packaged CMOS LOC systems

Though the intention for future LOC devices is to be completely self-contained, for now systems require additional components. In the case of the work described here the goal was to decrease the number of external devices required for readout and signal processing. This was achieved by using CMOS ICs to perform sensing and on-chip signal processing. However, the devices presented here still required the use of an external data acquisition system and a computer for information storage and data post-processing. Future visions for such LOC devices can include the functions of signal acquisition and storage, and even additional processing by using more complex CMOS ICs, or by integrating additional chips into the same device. Given the limitations of the current system it was necessary to develop hardware that would provide the necessary connections to external equipment.

6.2.2.a Simple two-tiered PCB

The packaged CMOS ICs described in this work redistribute their electrical input/output connection points to the periphery of the handle wafer. This provides the dual benefits of moving the electrical connections away from the fluidics, and increasing their pitch, which makes it easier to form electrical connections using non-microfabricated components. The system

employed here was a two-tiered PCB with spring-loaded contact pins. The pins provide reliable and durable electrical connections. The entire PCB was designed to be placed in either an incubator or refrigerator depending on the requirement of the type of cell culture being performed on the chip surface. See the Appendix for an image of the PCB.

6.2.2.a Accommodates external requirements

Similarly the fluidics on the chip surface needed to be accessible by hoses and other infrastructure. This need was accommodated by a specially located hole in the top PCB allowing not only access for hoses, but also optical assessment of the chip surface.

6.2.3 Heterogeneous Integration

Heterogeneous integration of CMOS ICs with fluidics and biology presents a number of unique challenges. The challenges arise from the different requirements of the different domains. Physical integration including packaging and addition of sensing structures presents challenges, as does the modeling and simulation of the various components of the system

6.2.3.a Decision making process for SOC implementation

The decision to make a single heterogeneously integrated system on chip, requires careful weighing of the benefits in light of the added complexities that arise from integration challenges.

Chapter. 3, provided a detailed explanation of the various considerations, providing examples and comparing performance of systems that use either multi-chip or single-chip implementations.

6.2.3.b Cross-domain iterative modeling

Because no single CAD tool exists that can model the complicated cross-domain problem of heterogeneous integration, a method was proposed to use existing CAD tools to perform iterative cross-coupled multi-domain modeling. Two specific examples were given. The first addresses the challenge of CMOS power dissipation and operation at higher temperatures, while taking into account the fluidic environment, and specifically using fluidics to cool the IC surface. The second looks at the increased coupling of electrical signals through the fluid medium, and informs the design of the packaging process to minimize the likelihood of interference.

6.2.3.c Rubric for complex integrated system design

Once the decision has been made to proceed with a single-chip solution, the process for integration is clearly outlined in Chapter. 3. Challenges to integration are systematically identified and solutions are proposed that have either been implemented in this body of work or in the literature. The topics discussed include the CMOS IC design process, packaging, and integration of fluidics and biology.

6.2.4 Hybrid bioelectronic olfactory sensor

The senses of sight, hearing, and touch have all been brought into the electronic realm, the two remaining senses of smell and taste (of which smell is a major component) remain out of the grasp of modern technology. The few commercial sensors that currently exist cannot even

attempt to parallel the biological nose in terms of sensitivity or scope. Development of a true electronic nose will have far reaching consequences and bring disruptive change to many fields including medicine, security, industrial control, and environmental monitoring.

Chapter. 4 introduces the first example of a hybrid bioelectronic olfactory sensor that uses olfactory sensory neurons as the sensing element and CMOS integrated circuit technology as the back end for signal processing. The sensor is capable of distinguishing between odorants and does so within a compact implementation. Furthermore, since the olfactory system remains to be fully characterized, the system will enable basic science in the study of mammalian olfaction.

6.2.4.a Adapting commercial protocols

For engineering applications it is typical to purchase kits of enzymes and solutions instead of coming up with new processes, especially when doing so may require a more intimate knowledge of the biological processes involved. Thus, robust and easy-to-use methods for integrating biological components like cells into LOC systems are necessary.

The olfactory sensor demonstrated here used amphibian cells. Because the physiology of amphibian cells is different than that of mammalian cells, the commercial products and procedures developed for mammalian cells must be modified for use with amphibian cells. Chapter. 4 explains how to adapt a commercial mammalian cell dissociation kit for use with amphibian cells and tissue.

6.2.4.b Surface treatment for cell adhesion

Surface treatments to increase cell adhesion are common. However, different types of treatments are used for micro-electrode arrays than for methods like patch clamp. This is because any surface treatment used for a microelectrode array must allow electrical signals to be conducted. During the experimental procedures with the amphibian cells it was found that typical microelectrode array treatments did not provide the required adhesion capabilities. A modified protocol was suggested using a combination of surface treatments. This yielded a surface that not only allowed proper adhesion of the cells, but also allowed conduction of electrical signals.

6.2.5 Asynchronous readout of bio-potentials

The area of brain machine interfaces remains an ongoing and exciting field of study.

Electrophysiology is one way to measure the activity of natural neural networks. Unfortunately when looking at large networks the amount of analog data becomes overwhelming when sampling at the necessary speed and resolution to detect the electrical activity of interest.

Bio-potential signals are asynchronous in nature. Furthermore, a signal that is continuously sampled only has useful information when actual spiking events occur. This leads to a tremendous use of bandwidth and storage space for signals with sparse information content. Chapter. 5, introduces a new event-based paradigm for bio-potential signal readout.

6.2.5.a.i Scalable readout paradigm

The address event protocol, originally used in neuromorphic systems to communicate information between artificial neural network ICs was adapted to minimize the bandwidth requirements for bio-potential signal readout. Instead of communicating an analog signal trace, the occurrence of spiking events is communicated. Specifically the address of the spatial location on the chip where the spiking even occurred is communicated off-chip. This method shows the highest currently reported reduction of bandwidth, by a factor of 1600 (compared to 960 [211]). Importantly, the readout paradigm scales well. As an array grows in size the number of elements to be read out using traditional methods would scale with the square of the array dimension, the event-based address readout scheme employs binary addressing and scales proportional to the logarithm (base 2) of the array dimension.

6.2.5.a.ii In-pixel spike detection

A key component of the event-based readout scheme is spike detection. The spikes must be detected before their address can be communicated off-chip. A number of different spike detection algorithms were evaluated in simulation using neural recording data. The highest performing algorithm was implemented on-chip. Each spike detector was placed within a so-called "pixel" containing the detector, and amplifier, and an event generator. The performance of the spike detection was evaluated by testing a fabricated chip and using artificially generated cardiac waveforms.

6.3 Discussion and Perspectives

The olfactory sensing technology shown here is a proof-of-concept that can be applied in the future to a handheld device capable of detecting odors outside of a laboratory environment. The necessary technology development has already started. Custom cells have been developed that express specific odorant receptors, and cell culture outside of an incubator is possible and techniques for doing so were described in Chapter. 3. The application of on-chip signal processing techniques to perform pattern based odorant recognition can employ the methods introduced in Chapter. 5. However, looking forward it is useful to have a discussion regarding future work that must be performed, and the prospects for this technology.

6.3.1 Short-Term Technology Development

Using the existing system, further experiments can be performed to characterize the response of the system to odorants. The first set of experiments that should be performed are those that look at the response of the OSNs to different concentrations of odors, this information will be necessary to determine the sensitivity of the system. Next it will be important to determine the time course of the system's response to odorant delivery, this should include investigation of adaptation behaviors exhibited by the neurons. Finally, the response of the system to mixtures of complex odors should also be characterized, as preliminary data appear to

indicate that the response to mixtures differs from the response to individual odorants, even when looking at the response of a single neuron.

The perfusion system used in this work should be replaced with microfluidic structures. Using microfluidics will allow finer control of odorant and stimulus concentration as well as delivery timing. This can be achieved by using techniques such as hydrodynamic focusing, where sheath streams of fluid are used to steer a central stream, thus enabling nearly instantaneous switching and control of odorant exposure to the cells.

Using the readout methods described here, larger CMOS chips with higher amplifier density can be used to sense from a larger population of cells. This will require the development of new chips, as well as investigation of different amplifier topologies to determine how to increase amplifier density without sacrificing signal quality.

Odorant recognition can be performed using simple feed forward neural networks and training using the data set that has already been collected. This classification method can readily be implemented in software and will prove useful, especially as array densities increase and more complex odorant mixtures are presented to the system.

An area of concern which should be addressed immediately is mitigation of the failure modes for the integrated LOC system. The fundamental failure mode is electrochemical. Though the packaging technique introduced here is more robust than most other methods from the literature, in certain cases the packaged devices fail over time, and the observable symptoms are

dissolved metal traces, gas bubbles in the fluid medium, or a change in pH of the fluid medium. All of these symptoms can be attributed to electrochemical effects. There are only two possible avenues for electrochemistry to occur. The first is if an electrochemically reactive material (such as Al) has not been properly passivated by an inert material, the second is if the polymer passivation layer fails to passivate the underlying metal structures adequately. For the first case, care must be taken during processing to ensure that the electrochemically reactive materials are conformally coated by an inert material, or that additional processing procedures are undertaken to ensure that there are no exposed sidewalls or that there are no pinholes in the inert material. For the second case, the polymer as-deposited should be investigated. The datasheets for Parylene indicate minimal absorption in the presence of fluid (.06% in 24 hours), yet the films have been observed to become soft after exposure to saline for just a few hours. Another manner by which the polymer passivation may fail is by inadequate adhesion to the underlying material, indicating that additional adhesion promotion strategies should be investigated or that a completely new passivation material should be used.

6.3.2 Long-Term Technology Development

Further development of the bioelectronic sensor technology described in this work will require a concerted effort in multiple fields. As a system, the olfactory sensor can be broken down into the following 5 macro-level components: the odorant sampling system, the cell-based sensing front-end, the CMOS sensor, the CMOS signal processing module, and finally the

electronic interface between the CMOS IC and the electronics used in the actual field portable device. The last portion is something that can be handled using existing methods and technology. Specifically, any necessary processing can be performed using either a field programmable gate array (FPGA) or a microprocessor. The other four components will require further technological development to bring the technology to the point where it can be deployed in the field.

6.3.2.a Algorithms and Architectures

Once the spike events have been detected, the question arises of how to interpret the information. One popular approach to this has been principal component analysis [228, 229] (PCA). In fact, PCA has been used to classify the in vivo response of neurons in the olfactory bulb of the rat [42], however, in that particular example it was done using a software on a PC. Efforts have been made to implement PCA on-chip [230], and also for feature extraction using PCA for spike sorting [231].

Another approach is to use a self-organizing map (SOM), where spiking events from OSNs that have an affinity for a particular odorant are grouped together. Indeed such a map would mimic exactly the biological structure found in the olfactory bulb, where OSNs expressing a certain receptor all send their axons to a particular glomeruli [23]. One such SOM from the field of artificial neural networks is the Kohonen feature map [232, 233]. Simulated Kohonen maps have been used for chemotopic mapping of the response of OSNs to odorants, and have been found, as expected, to mimic the structure of the biological system [234]. Kohonen maps

have been implemented in VLSI early on [235, 236], using 2 μ m features a 35 element Kohonen map was implemented in 1 mm². Extrapolation based on area yields that for a more modern process with a 0.5 μ m feature size, the same structures would occupy .0625 mm², scaling to .0018 mm² per map element, far smaller than the current amplifiers and easily implemented inpixel.

Additional circuits will need to be designed and implemented to perform pattern recognition on the output of the SOM. Since the distribution on the surface of the bioamplifier of the OSNs expressing particular receptors will vary with the particular culture, unsupervised learning can be utilized with the SOM to cluster the activity of OSNs that produce electrical activity in response to a particular stimulant. Using this clustered output, the pattern recognition stage will produce an output that is unique to each odorant, thus classifying the odorants.

6.3.2.b Odorant Sampling and Handling

In the proof-of-concept device introduced in this work the odorants are delivered to the OSNs in an aqueous solution. Many odorants are not directly soluble in water, and as such DMSO was used as a solvent to introduce the odorants to the aqueous solution. Though solvents can be found for specific odors, real odors are present in a gaseous state, mixed with air. As mentioned in section 1.2.3.b mucous plays a major role in the delivery of airborne odorants to OSNs. The olfactory epithelium requires an aqueous environment to prevent the cells from drying out, this environment is maintained by mucous secreted by nearby glands. Odorant

binding proteins within the mucous play a role in the transport of hydrophobic odorants to the receptor sites on the surface of the OSNs. Odorant sampling in future devices based on this technology can either use natural mucous secreted by supporting biological elements (co-cultured cells), or will require the development of an artificial mucous that can recreate the functions of the natural system.

6.3.2.c Increasing neuron density

One issue encountered in this work was low neuron density. The dissociation protocols that were used produced a cell population that mirrored the tissue which was used as the starting material (the entire olfactory epithelium). Because of this, there were a large number of supporting cells and the percentage of actual OSNs was quite low, on the order of 10%. Ideally the population of cells should be comprised only of OSNs.

The current vision for future OSN-based olfactory sensors requires arrays of precisely placed OSNs with known olfactory response profiles. Fortunately, there are two approaches that can be used to achieve this goal. The first is cell sorting, a well-established technique by which individual cells are sorted based on assessed features; this can be performed using optics and microfluidics. The other technique, and likely the one which will be most useful for furthering this technology, is the development of custom OSN cell lines. Currently odorant receptors have been expressed in different types of cells including yeast cells [237], dissociated rat neurons [238], and frog oocytes [239], indicating this this technology is within reach.

6.3.2.d Sensor Characterization

To be used as sensors, these hybrid bioelectronic systems should be characterized in a manner that enables them to be compared to traditional sensors. Typical sensor attributes such as SNR, sensitivity, and detection limit will need to be ascertained and optimized. From the perspective of the electronics, the signal to noise ratio is fundamentally determined at the frontend of the biopotential amplifiers. The primary factors that determine the SNR are the inputreferred noise of the amplifier, which sets the minimum level of external signal that can be distinguished from the noise inherent in the circuits, and the noise introduced at the electrode/electrolyte interface. As mentioned in Chapter. 3, the input-referred noise of an amplifier in a given technology node is set by the circuit topology and transistor sizing. Similarly, the noise at the electrode is determined primarily by electrode material and geometry. Both of these factors can be optimized through design and testing. Sensitivity, defined as the magnitude in change of the sensor response for a given change in sensed analyte, will likely vary more than traditional sensors. This is because of the inherent adaptation observed in the sensory neurons and because of the binary nature of the response of the neurons. Because of these reasons, it may be necessary to determine a new method for quantifying sensitivity. The detection limit of such cell-based sensors will need to be determined by basic scientific experiments, as introduced in Chapter. 1, for an intact biological olfactory system the detection limit can vary by 7 orders of magnitude depending on the odorant that is being sensed. Since one of the advantages of the cell-based sensing approach is the broad scope of odorants that can be

sensed, it may be necessary to define the detection limit for specific odors instead of for the device itself.

6.3.3 Looking Forward

General purpose olfactory sensing remains out of the grasp of modern sensor technology. The challenge lies in the chemical nature of olfaction. We still rely on the biological olfactory system when smells have to be detected. Cell-based sensing techniques leverage the sensitivity and scope of olfactory receptors that have evolved over millions of years. The key concept is to take the sensors, which are living cells, out of the body and place them into a portable device that can be used in a manner similar to other traditional sensors such as cameras and microphones. In this work a proof-of-concept sensor was demonstrated which accomplished this by intimately combining CMOS ICs with OSNs. Unlike many of the other cell-based sensing approaches discussed in Chapter. 1, the method employed in this work lends itself to truly portable sensors free from the confinement of a laboratory. The CMOS ICs are capable of sensing and processing the electrical activity from the cells upon detection of odorants, and the cells have the potential for homeostasis, alleviating many of the concerns that arise with other types of biosensor technologies. Advances in biotechnology and engineering will enable future cell-based olfactory sensors to move beyond the proof-of-concept work demonstrated here, and allow the development of portable olfactory sensors that exhibit the sensitivity, selectivity, and adaptability of the biological olfactory system.

6.4 Publication Record

6.4.1 Refereed Journal Articles

- [1] **T. Datta-Chaudhuri**, P. Abshire, and E. Smela, "Packaging commercial CMOS chips for lab on a chip integration," *Lab on a Chip*, 2014, 14(10), pp. 1753-1766.
- [2] **T. Datta-Chaudhuri**, E. Smela, and P. Abshire, "System-on-Chip considerations for heterogeneous integration of CMOS and fluidic biointerfaces," IEEE Trans. on Biomedical Circuits and Systems, (submitted).
- [3] **T. Datta-Chaudhuri**, P. Abshire, and E. Smela,"A Hybrid BioElectronic CMOS Olfactory Sensor," Biosensors and Bioelectronics, (in submission)

6.4.2 Journal Articles in Preparation

[1] **T. Datta-Chaudhuri**, B. Senevirathna, A. Castro, E. Smela, and P. Abshire, "An Active Micro-Electrode Array with On-Chip Spike Detection and Asynchronous Readout for Bandwidth Reduction", IEEE Trans. on Biomedical Circuits and Systems, *(in preparation)*.

6.4.3 Refereed Conference Proceedings and Abstracts

- [1] **T. Datta-Chaudhuri**, and P. Abshire, "Mismatch compensation of CMOS current mirrors using floating-gate transistors," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Taipei, Taiwan, 2009, pp. 1823-1826.
- [2] D. Sander, **T. Datta-Chaudhuri**, and P. Abshire, "Mismatch Compensation of a Subthreshold CMOS Current Normalizer," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Paris, France, 2010, pp. 3409-3412.
- [3] **T. Datta-Chaudhuri**, and P. Abshire, "Towards A Legged Chip," in *IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio de Janeiro, Brazil, 2011, pp. 2501-2504.

- [4] P. Abshire, **T. Datta-Chaudhuri**, et al, "Confession session: Learning from others mistakes," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Rio de Janeiro, Brazil, 2011, pp. 2501-2504.
- [5] **T. Datta-Chaudhuri**, E. Naviasky, and P. Abshire, "Floating-gate Capacitance Sensor Array for Cell Viability Monitoring," *in IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Baltimore, MD, 2013, pp. 65-68.
- [6] **T. Datta-Chaudhuri**, N. Halonen, A. Hassinen, P. Möller, S. Kellokumpu, P. Abshire, A. Lloyd-Spetz, E. Smela, "Integration of CMOS Chips into LOCs for Cell-Based Sensing," Biosensors, Melbourne, Australia, May 27-30, 2014.
- [7] E. Naviasky, **T. Datta-Chaudhuri**, and P. Abshire, "High Resolution Capacitance Sensor Array for Real-Time Monitoring of Cell Viability," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, 2014, pp. 634-637.
- [8] **T. Datta-Chaudhuri**, E. Smela, and P. Abshire, "System-on-Chip considerations for CMOS fluidic and biointerface applications," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Melbourne, Australia, 2014, pp. 2009-2012.
- [9] **T. Datta-Chaudhuri**, "Platform for Nose on a Chip," Nanoparticles and Health Workshop, Oulu, Finland, June 24-25, 2014.
- [10] **T. Datta-Chaudhuri**, B. Senevirathna, A. Castro, E. Smela, and P. Abshire, "An Active Micro-Electrode Array with Spike Detection and Asynchronous Readout," *in IEEE Biomedical Circuits and Systems Conference (BioCAS)*, Lausanne, Switzerland, 2014.
- [11] A. Berkovich, **T. Datta-Chaudhuri**, and P. Abshire, "A Scalable 20x20 Fully Asynchronous SPAD-Based Imaging Sensor with AER Readout," *in IEEE International Symposium on Circuits and Systems (ISCAS)*, Lisbon, Portugal, 2015, (accepted)

Appendix

The material in this appendix is taken directly from the supporting information for the article [79], it has been added here to provide additional details for some of the concepts discussed in Chapter. 2.

Biocompatibility - Although the supplier's instructions indicated that the human IPSC cardiomyocytes would only be viable for 10 days after plating, the cell clumps remained active for over 21 days. These cardiomyocytes did not proliferate because they were terminally differentiated, but the supporting cells continued to grow for the entire duration, indicating biocompatibility of the materials used in the packaging process. Fig. 72a shows the cell clump 24 hours after plating, and Fig. 72b shows the cells after 3 weeks. The lateral dimensions of the primary cell clump increased, and networks of interconnected cells formed around its periphery. The cells did not appear to exhibit a preference for either the Parylene or silicon dioxide surfaces, likely due to the use of the adhesion promoter.

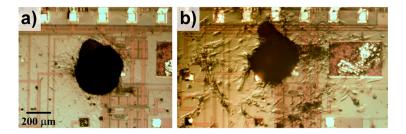


Fig. 72. a) Clump of cardiomyocytes 24 hours after plating onto the bioamplifier chip. b) Proliferation after 3 weeks.

Fabrication – The following figures show the chip surface during different stages of the fabrication process.

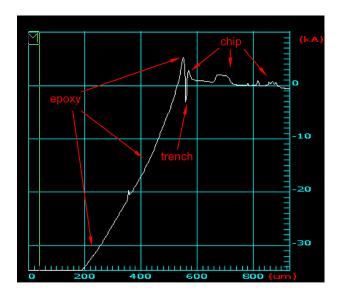


Fig. 73. Profilometry scan (Dektak III) of an edge of a "dummy" 3×3 mm silicon die within an epoxy handle wafer. There is a trench at the edge of the die located at 550 μ m on the x-axis. The depth of the trench is 500 nm with respect to the edge of the die and 900 nm with respect to the epoxy handle wafer over a lateral distance of 25 μ m. Around the chip there is a fall-off of 4 μ m over a distance of 350 μ m, corresponding to a slope 0.65°.

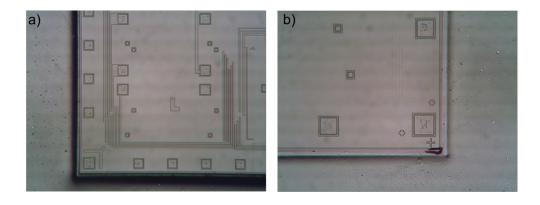


Fig. 74. The surface of a chip embedded in epoxy after metal (Cr/Au) deposition. a) At lower magnification the metal may appear to be discontinuous, but b) further magnification reveals that the metal is indeed continuous across the chip edge and onto the epoxy substrate.

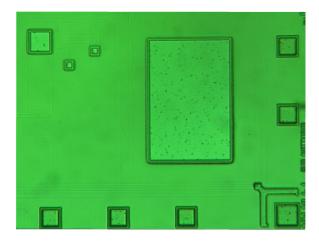


Fig. 75. The chip after it is masked with photoresist to permit selective deposition of PEDOT:PSS onto the recording and reference electrodes. (The green color of the image results from the filter used in the microscope to protect the resist from exposure.)

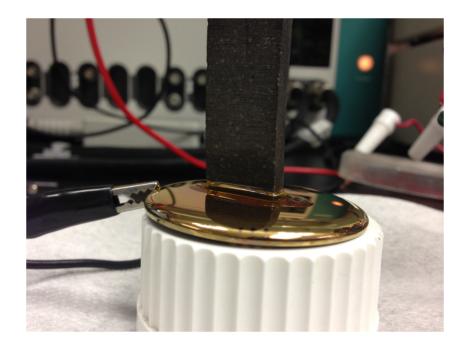
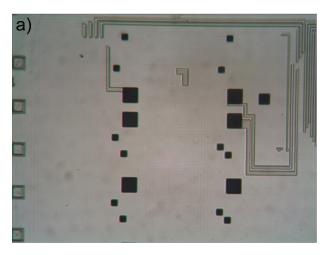


Fig. 76. The electrodeposition setup for PEDOT:PSS, which occurs after the handle wafer containing the chip is covered with Au. The Au, masked with photo resist (Fig. 75), serves as the working electrode for the constant-current electrodeposition and is contacted by the alligator clip on the left hand side. The counter electrode is the carbon bar shown hanging vertically above the chip. The aqueous monomer-containing electrolyte can be seen between the working and counter electrodes.



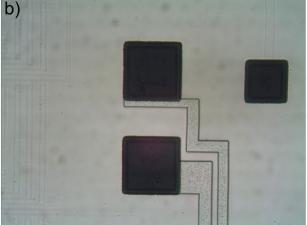


Fig. 77. Close-up of the chip surface after selective PEDOT:PSS deposition.

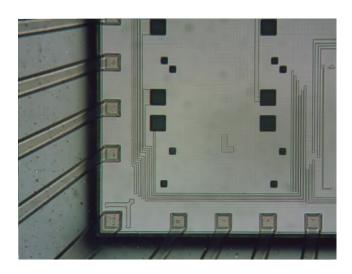


Fig. 78. The edge of a chip after the photolithography step for the metal etching step. Thick resist has been patterned to protect the metal traces that connect to the bond pads. After developing the resist was reflowed to increase adhesion to the underlying materials.

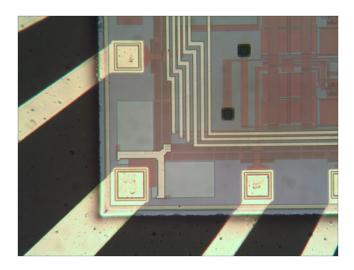


Fig. 79. The corner of a packaged chip after metal etching. Au traces contact the bond pads of the chip. The dark area around the chip is the epoxy handle wafer.

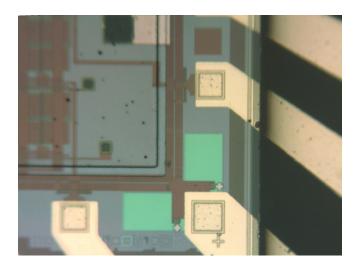


Fig. 80. The edge of a chip after deposition of the Parylene passivation layer over the entire wafer, but before the Parylene has been etched. The active area of the chip was protected before Parylene deposition using a thick layer of resist, which allows the subsequent etch procedure to leave behind a clean surface that was never in contact with Parylene. The metal etch on this particular chip was performed using a revised version of the mask that allowed for greater overlap of the metal traces over the bond pads.

 ${\ensuremath{ {\mbox{PCB}}}}$ – A custom two-tiered PCB architecture was developed to contact the packaged chips.

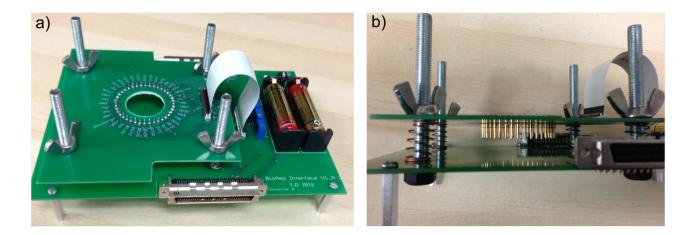


Fig. 81. The PCB that provides connections between the packaged chip and a data acquisition system. The PCB has two layers that are connected by a ribbon cable. The bottom layer provides a power supply and bias voltages, as well as connection headers for two data acquisition cables. The top layer of the PCB has spring-loaded Au contact pins that contact the exposed pads at the edges of the wafer.

Cells on CMOS Surfaces – The following figure is an image of the cells that were

cultured on the surface of various CMOS ICs.

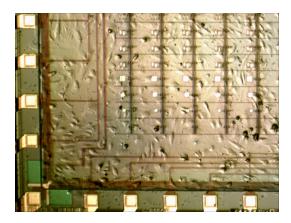


Fig. 82. An image of a capacitance sensor IC packaged using the method described in this work. The electrodes were not exposed to the fluid medium. The cells cultured on its surface are kidney cells from *Cercopithecus aethiops*. No biological adhesion promoter was used. It can be seen from the complete absence of cells on the Parylene that the cells preferred the chip surface.

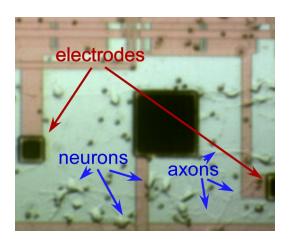


Fig. 83. Rat cortical neurons (Invitrogen Cat. No. A10840-01) cultured on the surface of a packaged bioamplfier IC. This image was taken on the 9th day in vitro (DIV 9). The cells were plated onto the chip after a cell adhesion promoter (poly-D-lysine, SIGMA P6407) was applied following the suppliers instructions. Arrows labeled "neurons" indicate some of the cell bodies, and arrows labeled "axons" indicate projecting processes that are forming an interconnected neural network. Two differential recording electrodes from an amplifier are also shown. The large black square in the center is a reference electrode. The electrodes are coated in PEDOT:PSS.

Electrode Impedance – The effects of different electrode coatings are shown in the following figure.

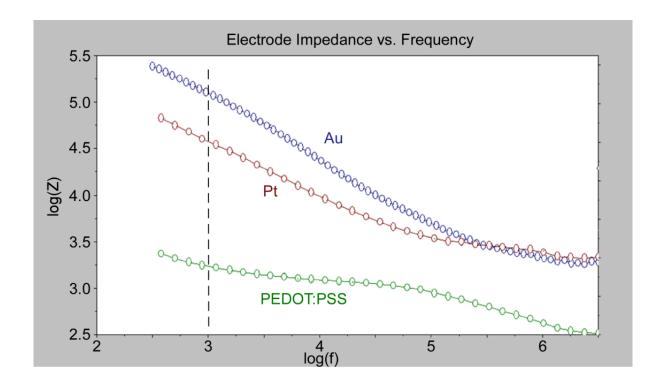


Fig. 84. The effect of Pt and PEDOT:PSS coatings over Au electrodes on the impedance between an electrode and an electrolyte solution (phosphate buffered saline). Electrochemical impedance spectroscopy was performed using a potentiostat/galvanostat (Eco Chemie, Autolab) with a module for frequency response analysis (FRA). The vertical line marks 1 kHz (the frequency of interest for neural recordings) at which the impedance is decreased by nearly two orders of magnitude when the electrodes are coated with PEDOT:PSS compared to bare Au.

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