

ABSTRACT

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JUNCTION TRANSISTORS FOR FLEXIBLE
MICROWAVE APPLICATIONS

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Microwave frequency flexible electronic devices require a high quality semiconducting material and a set of fabrication techniques that are compatible with device integration onto flexible polymer substrates. Over the past ten years, monocrystalline silicon nanomembranes (SiNMs) have been studied as a flexible semiconducting material that is compatible with industrial Si processing. Fabricated from commercial silicon on insulator (SOI) wafers, SiNMs can be transferred to flexible substrates using a variety of techniques. Due to their high carrier mobilities, SiNMs are a promising candidate for flexible microwave frequency devices.

This dissertation presents fabrication techniques for flexible SiNM devices in general, as well as the progress made towards the development of a microwave frequency SiNM bipolar junction transistor (BJT). In order to overcome previous limitations associated with adhesion, novel methods for transfer printing of metal films and SiNMs are presented. These techniques enable transfer printing of a range

of metal films and improve the alignment of small transfer printed SiNM devices. Work towards the development of a microwave frequency BJT on SOI for SiNM devices is also described. Utilizing a self-aligned polysilicon sidewall spacer technique, a BJT with an ultra-narrow base region is fabricated and tested.

Two regimes of operation are identified and characterized under DC conditions. At low base currents, devices exhibited forward current gain as high as $\beta_F = 900$. At higher base current values, a transconductance of 59 mS was observed. Microwave scattering parameters were obtained for the BJTs under both biasing conditions and compared to unbiased measurements. Microwave frequency gain was not observed. Instead, bias-dependent non-reciprocal behavior was observed and examined. Limitations associated with the microwave impedance-matched electrode configuration are presented. High current densities in the narrow electrodes cause localized heating, which leads to electrode material damage and ultimately dopant diffusion in the BJT.

Finally, device design improvements are proposed to address the problem of localized heating and increase device lifetime under testing conditions. High values for DC current gain suggest that future modifications should improve microwave frequency performance and measurement reproducibility.

SILICON ON INSULATOR BIPOLAR JUNCTION TRANSISTORS FOR
FLEXIBLE MICROWAVE APPLICATIONS

By

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Dedication

To my father, Richard Bavier, for always encouraging me to pursue that which is worthy of my effort.

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There are many without whose help I could not be writing this thesis. It's truly a humbling experience to try to account for all of the support I've received from friends, family, and colleagues over my graduate career. While I don't have the space to thank everyone here, I am forever indebted to those who have helped and I aspire to their generosity as I continue my career.

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Finally, thanks to my family. To my wife Heather, for putting up with the late nights and dirty dishes. And for always believing that I would do well, even when I had my doubts. To my mother Mary, for unconditional support and friendship, and for encouraging me to reach out of my comfort zone and pursue bigger things. To my brother and all-time favorite guitar player Andy, for giving someone to look up to as an academic and as a man.

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List of Abbreviations

AC – alternating current

BJT – bipolar junction transistor

BOX – buried oxide layer

CMOS – complementary metal-oxide-semiconductor

CPW – coplanar waveguide

DC – direct current

EDX – energy dispersive x-ray microscopy

FTDS - 1H,1H,2H,2H-perfluorodecyltrichlorosilane

HF – hydrofluoric acid

HFSS – High Frequency Structure Simulator

LPCVD – low-pressure chemical vapor deposition

LPS – Laboratory for Physical Sciences, University of Maryland

MOSFET – metal-oxide-semiconductor field effect transistor

OTS – octadecyltrichlorosilane

PECVD – plasma-enhanced chemical vapor deposition

poly-Si – polycrystalline silicon

RIE – reactive ion etching

SAM – self-assembled monolayer

SFTP – surface functionalized transfer printing

SiNM – silicon nanomembrane

SOI – silicon on insulator

Chapter 1: Introduction and Background

The focus of this project has been to develop techniques and devices for use in the growing field of flexible electronics. Flexible electronics are a class of devices that can conform to non-planar surfaces and operate under bending conditions. Due to their flexibility, they are able to operate in environments previously inaccessible to rigid chip-based electronics. This work will present new techniques for the transfer of high-quality electronic materials to flexible substrates and describe the performance and limitations of a transistor in development for flexible microwave applications.

There are a variety of methods and materials for the fabrication of electronic devices on flexible substrates. In this study we use transfer printing, due to its scalability and the high quality of films that it is capable of producing. Whereas transfer printing of metals had previously been limited to gold films, this work presents a technique that enables transfer printing of a range of metals. A previously unreported technique for transfer of aligned monocrystalline silicon nanomembranes (SiNMs) will also be presented.

The availability of high quality metal and semiconductor films on flexible substrates has led to recent research into microwave frequency flexible electronic devices. The addition of microwave frequency devices to existing flexible technology will enable a

range of new capabilities like fast, low power communication and wireless energy transfer. In this study, we present progress on the development of the first flexible microwave silicon nanomembrane bipolar junction transistor.

The second and third chapters of this thesis provide background that will be useful in the discussion of the progress we've made. The fourth chapter will describe our work in the transfer printing of metals and SiNMs. In the fifth chapter, the design and fabrication of bipolar junction transistors (BJTs) for flexible applications will be presented. This chapter will also describe the primary limitation of this device design, the effects of localized Joule heating. The sixth chapter will describe direct current and microwave electrical characterization. Finally, chapter 7 will provide conclusions based on current work and an outlook on directions for future studies.

1.1 Silicon Nanomembrane Background

In order to achieve microwave frequency performance on flexible substrates, a high quality flexible semiconducting material is required. SiNMs are chosen due to their high carrier mobility, flexibility, and compatibility with established complementary metal-oxide-semiconductor (CMOS) processing techniques. Previous work has demonstrated microwave frequency operation of SiNM devices, indicating that they should be a suitable material for microwave BJTs.

The flexibility of a material is a function of both material properties and geometry. Thick aluminum stock is very difficult to bend and quickly deforms plastically if

bent. aluminum foil, on the other hand, is flexible can be bent easily and many times before failure. Monocrystalline silicon is similarly rigid at thicknesses above 100 μm , and will cleave along crystalline planes when bent. At thicknesses between 1 nm and 1 μm , however, Si is highly flexible. For instance, a SiNM with 7 nm thickness has been shown to have a bending stiffness of $8.86 \text{ MPa} \cdot \mu\text{m}^4$, seven orders of magnitude lower than if it were 1.5 μm thick [1].

Over the past ten years, SiNMs have been studied as the active semiconductor in high-performance flexible devices. They consist of freestanding thin monocrystalline Si films that can be transferred to any properly prepared adhesive substrate. Once transferred, the mechanical properties of the overall device are dominated by the (much thicker) substrate, allowing for flexible monocrystalline Si devices.

SiNMs have a combination of properties that make them uniquely suited to high performance flexible electronics. They can be mechanically and epitaxially strained, which alters their band structure and conductivity. Due to their thinness, they can be patterned at the nanoscale to alter their thermal properties. Finally, their combination of high carrier mobility and flexibility make them well suited to bio-implantable and high frequency flexible devices.

The typical method for creating freestanding nanomembranes utilizes a three-layer configuration wherein a functional layer is separated from the bulk substrate by a sacrificial layer (Figure 1.1). The sacrificial layer is then etched, decoupling the

functional layer from the bulk substrate, leaving a freestanding functional film. This technique requires a selective etch process that will completely remove the sacrificial layer but not damage the functional layer.



Figure 1.1 – Three layer configuration for nanomembrane fabrication [2]

The three-layer configuration of choice for SiNMs has been the silicon-on-insulator (SOI) wafer. In the case of SOI, both the functional layer and bulk substrate are monocrystalline Si and the sacrificial layer is SiO₂. SOI has the advantage that it is already widely used in the semiconductor industry and is commercially available. SiO₂ is also a convenient sacrificial layer, because it can be selectively etched by hydrofluoric acid (HF) solutions, which have a very low etch rate for Si [3].

SOI also has the significant advantage that it can withstand high temperatures and solvent treatment which would otherwise be incompatible with most polymers. After ion-implantation, Si must be annealed to temperatures above 900 °C in order to repair crystalline damage and to move interstitial dopant species into lattice sites. Standard e-beam deposition and lift-off requires the sample to be submerged in acetone for an extended period of time. The ability to perform these processing steps on SOI and

then transfer to a flexible substrate gives SiNMs an advantage over directly-deposited semiconductors.

The basic SiNM transfer process is shown in figure 1.2. The functional top Si layer is partially etched to expose the underlying buried oxide (BOX) layer to the HF solution. It is then submerged in HF, which undercuts the top Si layer and releases it (Figure 1.2b, 1.2c). The weakly coupled SiNM is then brought into contact with an adhesive substrate and is transferred (Figure 1.2d-1.2f).

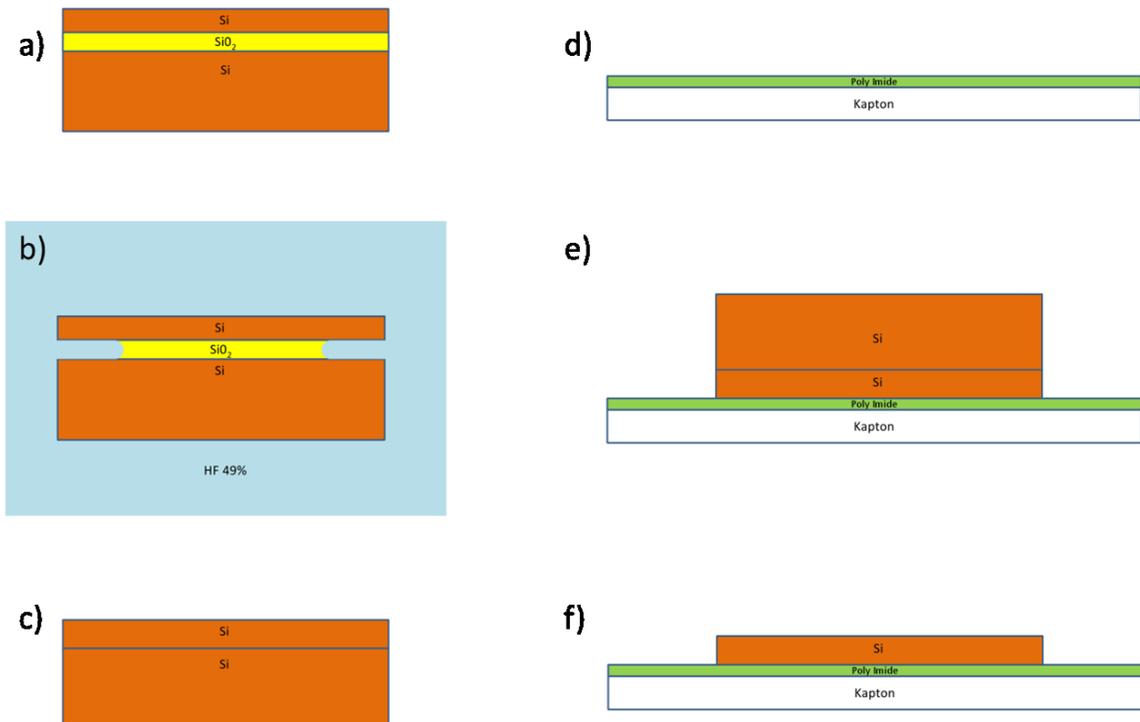


Figure 1.2 – Generic SiNM transfer process

A more specific description of SiNM transfer methods will be given in chapter 2. This section will describe some of the interesting properties of SiNMs as well as their applications in medicine and high frequency flexible electronics.

The first significant outcome of transferring SiNM devices to flexible substrates is the ability to apply strain. Because it is an indirect band-gap semiconductor, the conduction band of Si forms six symmetrical ellipsoids in the reciprocal lattice, two on each axis (Figure 1.3). It is well known that strain on the Si crystal lattice breaks the six-fold symmetry of the conduction band, reducing inter-valley phonon scattering. Furthermore, the shape of the ellipsoids is distorted, lowering the effective mass of electrons in the conduction band in the direction of tensile strain. These two effects combine to increase the mobility of electrons in the conduction band. This increased mobility decreases switching time, and strained Si is widely used in the microprocessor industry [4].

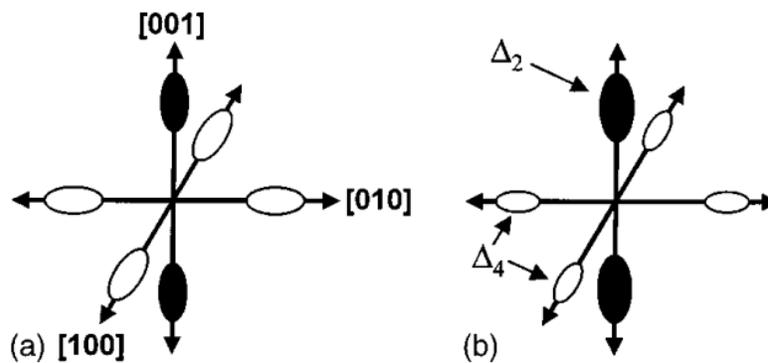


Figure 1.3 - Si conduction band in the reciprocal lattice [5]

A typical method for introducing strain to the Si lattice is to introduce germanium (Ge) to the Si during growth. Ge atoms have the same valence state as Si, but are larger and introduce an isotropic tensile strain to the lattice. This type of strain can be achieved by adding Ge during wafer fabrication, as well as during epitaxy. Using this

method, electron mobility can be enhanced to more than double that of unstrained Si [6].

In the case of SiNMs, however, strain can also be applied mechanically, through the bending or stretching of a flexible substrate. When SiNMs are transferred, the overall mechanical properties of the device are dominated by the new substrate. By bending or straining the substrate, local strain at its surface is transferred to the SiNM, altering its electrical properties.

The effects of strain can be exploited in order to increase device performance. Three layer epitaxial Si/SiGe/Si membranes are, when released, under strain even while elastically relaxed. Before membrane release the SiGe layer is under compressive strain, due to the larger Ge atoms. Once released, the stress due to compression in the SiGe layer introduces tensile strain to the two Si layers, and strain is shared between all three layers (Figure 1.4). Metal-oxide-semiconductor field-effect transistors (MOSFETs) made from this strained heterostructure exhibit significantly higher field-effect mobility than identical devices fabricated from Si alone (Figure 1.5) [7].

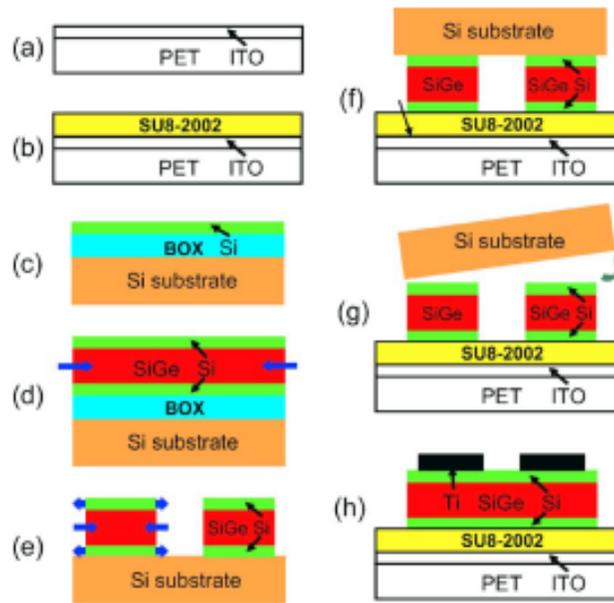


Figure 1.4 - Elastically relaxed strain sharing membrane transfer [7]

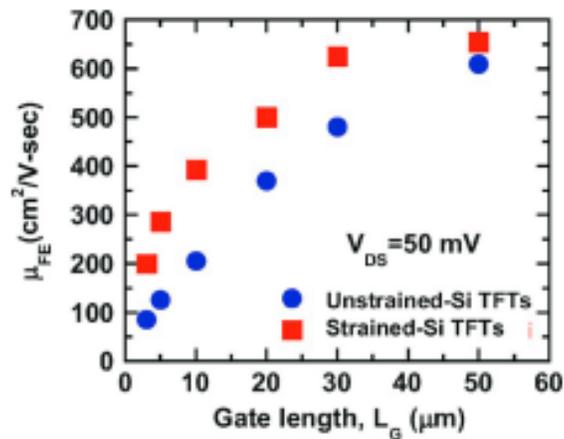


Figure 1.5 - Field effect mobility for strained and unstrained SiNM MOSFETs [7]

The effect of strain on SiNMs has been exploited to create piezoresistive flexible strain sensors (Figure 1.6) [8]. The heterogeneous system including the Si device and flexible substrate was shown to have a gauge factor (ratio of percent change in electrical resistance to mechanical strain) of approximately 43. The devices were

found to be mechanically robust with no appreciable change in operation after 1000 cycles at bending radii as small as 12mm.

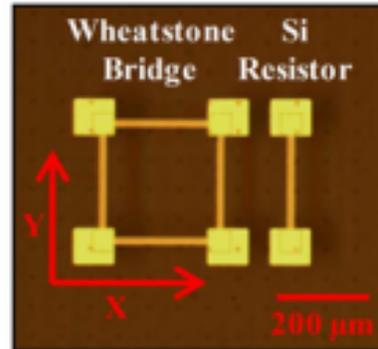


Figure 1.6 - Piezoresistive SiNM strain sensor [8]

In addition to altering the electrical properties of SiNMs using strain, their thermal properties can be altered using advanced nanopatterning techniques. By introducing scattering sites for phonons, the thermal conductivity can be suppressed. This low thermal conductivity (combined with high electrical conductivity due to heavy doping) could lead to the use of Si as a thermoelectric material.

The figure of merit for thermoelectric materials is ZT .

$$ZT = \frac{\sigma S^2 T}{\lambda} \quad \text{Eq. 1.1}$$

It is proportional to electrical conductivity σ and inversely proportional to thermal conductivity λ . Monocrystalline Si can be doped to achieve high electrical

conductivity, but its relatively high thermal conductivity ($1.3 \text{ Wcm}^{-1}\text{C}^{-1}$) has prevented its use as an efficient thermoelectric material.

Using block copolymer lithography, however, holes can be etched into the SiNM at a size and spacing that is on the order of a phonon's mean free path but larger than the mean free path of an electron. This creates preferential phonon scattering, reducing thermal conductivity by a factor of 25 without degrading electrical conductivity [9].

The thermoelectric figure of merit ZT of these “holey” SiNMs was measured to be as high as 0.4 at room temperature (Figure 1.7), better than non-patterned Si by a factor of nearly 50. This ZT value also brings Si within an order of magnitude of the highest performing telluride thermoelectric materials which have a room temperature ZT between 2 and 2.5 [10].

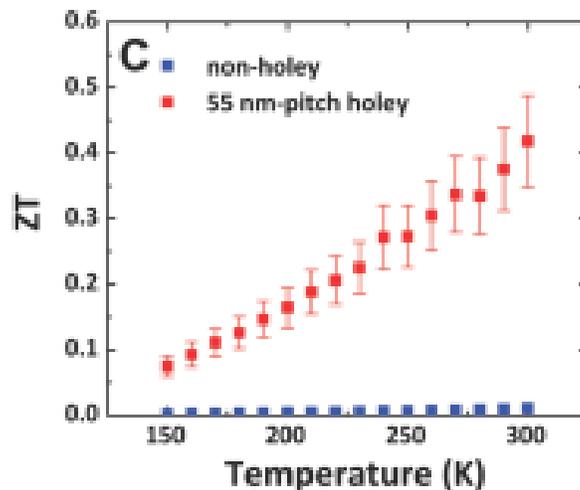


Figure 1.7- ZT for “holey” and “non-holey” SiNMs

Silicon has a significant advantage over Te based thermoelectric materials in that it is naturally abundant and non-toxic. A significant limitation to SiNMs' adoption as a thermoelectric material is also related to their nanoscale thickness. Because they are so thin, the overall power density of a SiNM thermoelectric device is limited. It has been theorized that bulk 3D Si with nanopores of comparable size and pitch could have similar thermoelectric properties to holey SiNMs [11]. The ability to manufacture nanoporous Si on an industrial scale could lead to the use of Si and a thermoelectric material.

Over the past five years, SiNMs have been investigated for possible integration into bio-implantable devices. SiNMs can conform to the surface of skin and organs without inhibiting their electrical performance. They can be patterned into serpentine shapes and applied to pre-strained substrates so that they stretch as well as bend [12]. Si is nontoxic in the quantities present in SiNM devices and will dissolve into the body on the timescale of days. Coatings have been developed that can provide stable device performance for months, with rapid transience thereafter [13].

SiNM-based biological sensors have been demonstrated to be effective in several animal trials, and have begun human medical testing [14]. High resolution SiNM sensor arrays were applied directly to the brains of cats and oscillatory sleep signals were observed at a spatial resolution below that of conventional subdural electrodes [15]. Large area sensors on pigs' hearts were able to detect the propagation of electrical signals as the heart beats, possibly leading to a new way of diagnosing

arrhythmia [16]. High spatial resolution sensors were also used to monitor the temperature of the surrounding tissue during rf and cryo-ablation, which could minimize tissue damage during those procedures in the future. Most recently, a human medical trial was performed where SiNM based devices were placed on the skin to monitor temperature, moisture and other data during the healing of surgical wounds [14].

Flexible implantable devices have shown great promise for minimally invasive monitoring, but previously reported devices all require a physical connection to the outside world for power and communications. These devices would benefit greatly from wireless communication and charging. Microwave frequency transmission between these devices and the outside world could potentially overcome both of these challenges and enable truly non-invasive monitoring and treatment.

Passive and active microwave frequency SiNM devices have been demonstrated. The microwave performance of flexible PIN diodes has been measured under conditions of strain (Figure 1.8) [17]. A 10% reduction in internal parasitic impedance was shown at a strain of 0.4% while in the ON state. Isolation in the OFF state was not shown to degrade under strain conditions.

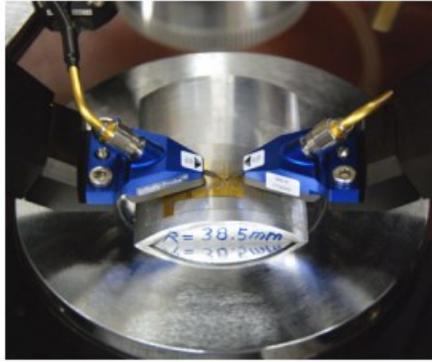


Figure 1.8 – Measurement of strained SiNM PIN diodes

The first active high-frequency SiNM device was a field-effect transistor with a maximum oscillation frequency (f_{MAX}) of 515 MHz [18]. These devices were doped using phosphorous diffusion at high temperature. This design was improved upon by a subsequent study that used ion implantation as the doping method. Ion implantation gives better lateral and vertical spatial resolution to doped regions than diffusion does, and these devices reported a f_{MAX} of 3.1 GHz [19]. Improvements in gate alignment lead to FETs with reported f_{MAX} values of 7.8 GHz [20] and most recently 12 GHz [21] (Figure 1.9).

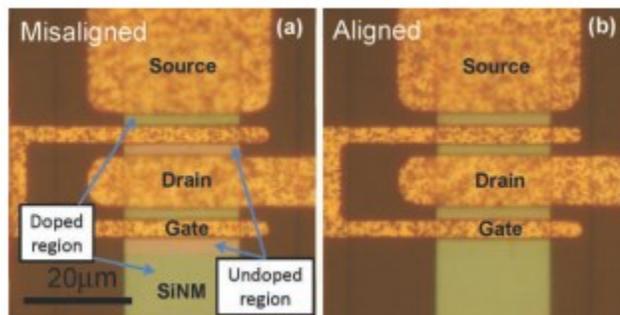


Figure 1.9 – Alignment of microwave frequency SiNM FET [21]

All previously reported active SiNM devices have been FETs. While passive PIN devices have been studied, there have been no reports of the active NPN or PNP BJT configuration at any frequency. While FETs are the most common configuration in use today, BJTs are still preferred for certain applications like high frequency switching and amplification. The addition of BJTs to existing FET based SiNM technology would also pave the way for SiNM based bipolar-CMOS (BiCMOS) technology, which exploits the advantages of both types of transistor in a single device.

In conclusion, SiNM technology has shown promise in a wide range of applications. Previous work has shown that SiNM based devices can exhibit microwave frequency performance. Due to their flexibility, high mobility, and compatibility with standard Si processing techniques SiNMs were chosen as the semiconducting material for this project. In this work, we fabricate SiNMs using an established method as well as demonstrate a previously unreported SiNM transfer technique. We also design, fabricate, and characterize BJTs on SOI for integration into SiNM technology.

1.2 Theoretical Background

1.2.1 Bipolar Junction Transistors

The device chosen for development in this project is the BJT. Previously reported SiNM microwave devices in the MOSFET configuration indicate that it should be possible to fabricate microwave SiNM BJTs. While less common than MOSFETS,

BJTs are preferred for certain applications such as fast switching and signal amplification.

BJTs are an electrical device consisting of three regions of alternating semiconductor type. An NPN BJT consists of two n-type semiconductors separated by a thin p-type semiconductor, and a PNP consists of two p-type semiconductors separated by a narrow n-type region. The interfaces of the semiconductor regions form PN junctions, whose properties determine the operation conditions of the device. Direct current (DC) device performance is described using the Ebers-Moll model and DC output conditions are used to bias the device for alternating current (AC) signal gain.

The fundamental constituent of the BJT is the PN junction (Figure 1.10). When a p-type semiconductor comes into contact with an n-type semiconductor, free electrons diffuse into the p-type material and free holes diffuse into the n-type material. These minority carriers leave behind ionized donor and acceptor atoms and then recombine with carriers of the opposite type. The result is a region on either side of the junction that is depleted of free charge carriers called the depletion region. In this region, the space charge from the ionized donors creates an electric field in the opposite direction of carrier diffusion. In equilibrium the force of this electric field prevents further diffusion of charge carriers. This field also creates a built-in potential across the interface.

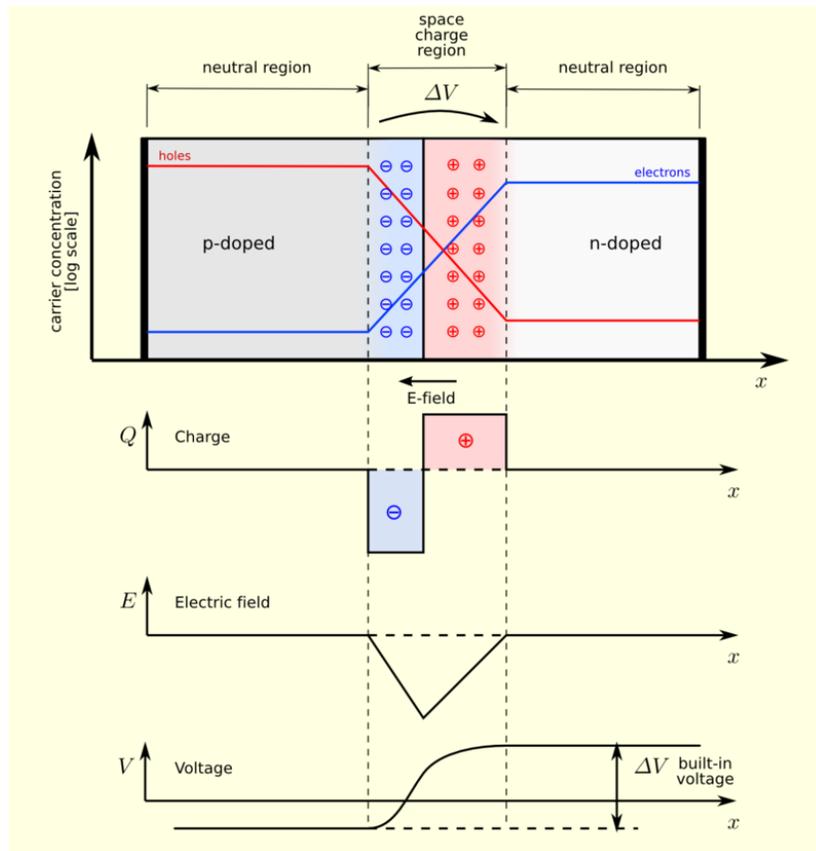


Figure 1.10 – PN junction

When a PN junction is reverse biased, the applied potential adds to the built-in voltage and the depletion region widens. Under reverse bias conditions, only a very small current flows due to thermal diffusion of free carriers into the depletion region. This current is called the reverse saturation current and is roughly independent of the reverse bias.

If the PN junction is forward biased at a value higher than the built-in potential, electrons move freely across the junction and become minority carriers in the p type material. These minority carriers then diffuse some distance before recombining with holes. Simultaneously, holes diffuse into the n type material and recombine with

electrons. The net effect of this diffusion and recombination is forward current flow (Figure 1.11). The average distance a carrier will travel before recombination is called the minority carrier diffusion length.

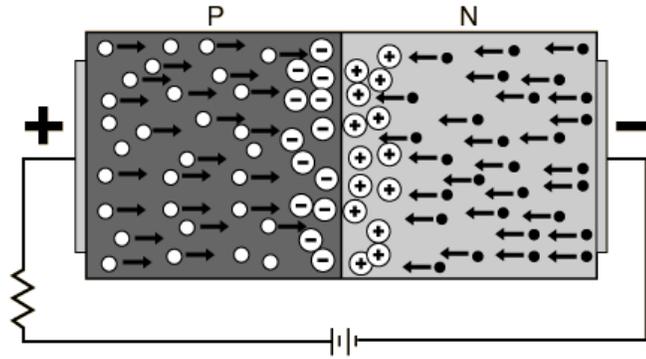


Figure 1.11 – Forward biased PN junction [22]

The flow of current under forward bias but not under reverse is the defining property of a PN junction. The current flowing across a PN junction is given by the Shockley diode equation

$$I = I_S \left(e^{\frac{qV_D}{nkT}} - 1 \right) \quad \text{Eq. 1.2}$$

Where I is the diode current, I_S is the reverse saturation current, q is the charge of the electron, V_D is the applied diode voltage, k is Boltzmann's constant, T is the temperature and n is an ideality factor with $n=1$ being an ideal PN junction. The current-voltage output of an ideal PN junction is shown in Figure 1.12.

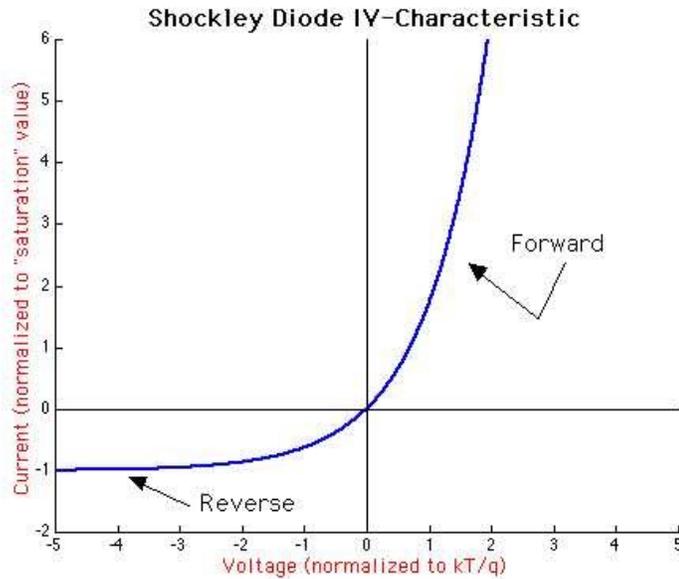


Figure 1.12 – Shockley diode IV characteristic [23]

A BJT is a three terminal device consisting of two PN junctions, with each terminal connecting to one of the three NPN or PNP regions. The configuration chosen for this project is NPN, so further treatment will describe this configuration. The three terminals are called the emitter, base, and collector.

There are four modes of operation depending on the relative biasing of each of the PN junctions: forward active, reverse active, saturation, and cutoff. The biasing of the two junctions in each of these modes is given in Table 1.1. Among these, the highest DC current gain and AC signal gain can be achieved in forward active mode. A schematic of a BJT in forward active mode is given in Figure 1.13.

Base-Emitter Bias	Base-Collector Bias	Mode
Forward	Forward	Saturation
Reverse	Reverse	Cutoff
Reverse	Forward	Reverse active
Forward	Reverse	Forward active

Table 1.1 – BJT modes of operation

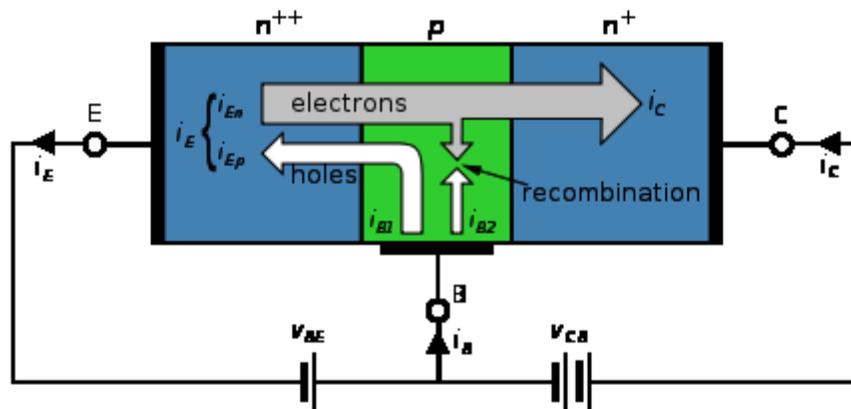


Figure 1.13 – BJT, forward active mode

In forward active mode, the base-emitter junction is forward biased and the base collector junction is reverse biased. A small current going into the base region controls a large current between the emitter and collector.

In the limit of a very wide base region, the presence of a reverse biased base-collector junction would prevent any current from flowing between the collector and emitter. Majority carriers in both the base and collector are not able to cross the base-collector depletion region. This behavior will be observed in chapter 5 when we observe the

effects of Joule heating on devices. Current will only flow if a BJT's base region is narrow compared to the minority carrier diffusion length.

When the base-emitter junction is forward biased and current flows from the base into the emitter, electrons are able to diffuse into the base region as minority carriers. Some then recombine with holes to constitute the base current. Others will diffuse across to the base-collector depletion region and are swept into the collector by the built-in electric field of the base-collector PN junction. This diffusion across the base region is the source of current gain. In order to maximize the number of electrons that diffuse across to the base-collector depletion region, the dopant concentration in the emitter is typically several orders higher than that of the base. The base region is also designed to be very narrow, typically a small fraction of the minority carrier diffusion length.

With the proper geometry and dopant concentrations, it is possible to design a BJT such that the current due to electrons diffusing across the base region is many times larger than the current used to forward bias the base-emitter junction. This ratio is called the forward common emitter current gain, β_F and is an important figure of merit for BJTs.

$$\beta_F = \frac{I_C}{I_B} \tag{Eq. 1.3}$$

For modern Si BJTs β_F has a typical value of 100-300, but can be as high as 1000. The other important figure of merit for this study is transconductance.

Transconductance, g_m is defined as the change in collector current divided by the change in base voltage.

$$g_m = \frac{\partial I_{CE}}{\partial V_{BE}} = \frac{I_{CE}}{V_T} \quad \text{Eq. 1.4}$$

where V_T is the thermal voltage, approximately 26 mV at room temperature. Current gain and transconductance will play an important role when biasing our BJTs for AC signal gain.

The DC output characteristics of a BJT can be described using the Ebers-Moll model. This model extends the Shockley diode equation to include the currents at all three terminals. The full Ebers-Moll model states that

$$i_C = I_S \left(e^{\frac{qV_{BE}}{nkT}} - e^{\frac{qV_{BC}}{nkT}} \right) - \frac{I_S}{\beta_R} \left(e^{\frac{qV_{BC}}{nkT}} - 1 \right) \quad \text{Eq. 1.5}$$

$$i_B = \frac{I_S}{\beta_F} \left(e^{\frac{qV_{BE}}{nkT}} - 1 \right) + \frac{I_S}{\beta_R} \left(e^{\frac{qV_{BC}}{nkT}} - 1 \right) \quad \text{Eq. 1.6}$$

$$i_E = I_S \left(e^{\frac{qV_{BE}}{nkT}} - e^{\frac{qV_{BC}}{nkT}} \right) + \frac{I_S}{\beta_F} \left(e^{\frac{qV_{BE}}{nkT}} - 1 \right) \quad \text{Eq. 1.7}$$

where i_C is the collector current, i_B is the base current, i_E is the emitter current, n is an ideality factor and β_R is the reverse common emitter current gain. In forward active mode, we can use the approximation:

$$V_{BC} < 0, \quad e^{\frac{qV_{BC}}{nkT}} \sim 1 \quad \text{Eq. 1.8}$$

The Ebers-Moll equations then become

$$i_C = I_S \left(e^{\frac{qV_{BE}}{nkT}} - 1 \right) \quad \text{Eq. 1.9}$$

$$i_B = \frac{I_S}{\beta_F} \left(e^{\frac{qV_{BE}}{nkT}} - 1 \right) = \frac{i_C}{\beta_F} \quad \text{Eq. 1.10}$$

$$i_E = I_S \frac{\beta_F + 1}{\beta_F} \left(e^{\frac{qV_{BE}}{nkT}} - 1 \right) = \frac{\beta_F + 1}{\beta_F} i_C \quad \text{Eq. 1.11}$$

Proper biasing for AC signal gain is usually determined from the BJT's current-voltage output characteristics (Figure 1.14). i_C is measured as V_{CE} is swept while i_B is held constant. This process is repeated for different values of i_B . In forward active mode i_C is nearly independent of V_{CE} but strongly dependent on i_B . For this reason, a BJT in forward active operation is considered a current controlled current source.

The biasing conditions for AC signal gain are usually chosen somewhere in the middle of the forward active region, so that small changes in i_B and V_{CE} do not take the device out of forward active mode.

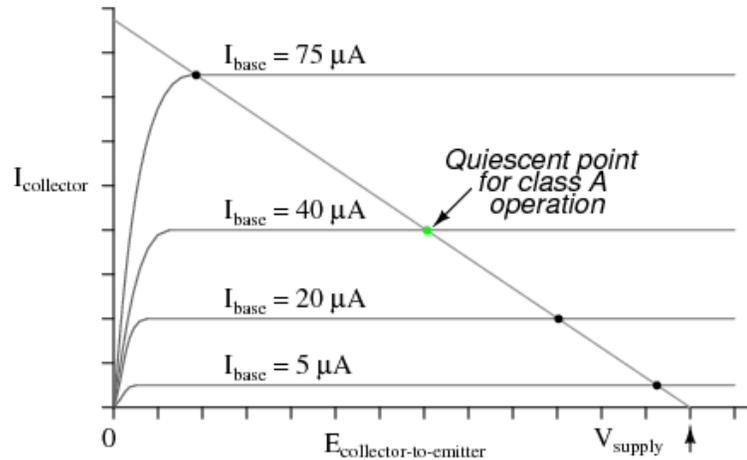


Figure 1.14 – Quiescent point on DC IV curve [24]

The biasing conditions for AC operation are obtained from the quiescent point, which is chosen to be in a biasing region of linear response. The value of V_{CE} during AC operation is equal to the value of V_{CE} at the quiescent point. The value of i_B under AC operation is the i_B value of the curve that intersects the quiescent point. In Figure 1.14, that value is $i_B = 40 \mu\text{A}$. In order to determine the DC bias for V_{BE} given a value for i_B , a current-voltage sweep of the base-emitter junction is taken, and the corresponding V_{BE} is obtained.

In summary, BJTs use the properties of PN junctions along with minority carrier diffusion to create gain. When in forward active mode they operate as a current controlled current source. BJT behavior under DC conditions is described using the Ebers-Moll model. DC current-voltage data can be used to obtain biasing conditions for AC signal gain.

1.2.2 Microwave Frequency Electronics

Existing flexible device technology stands to benefit significantly from microwave frequency technology. Low-power directional microwave communication and wireless inductive energy transfer could have applications from implantable medical devices to space exploration. At microwave frequencies, the standard lumped-element model starts to become invalid and a new set of concepts is necessary to describe microwave networks. In order to develop flexible microwave devices, it is necessary to have an understanding of some basic principles of microwave engineering.

Microwave electronics are used extensively in telecommunications, the military, and increasingly in consumer electronics. Microwave signals can transmit data at high speed using directional, low power antennas. The microwave regime is also the point at which the wavelength of the electromagnetic signal becomes comparable to the size of practical devices. As a consequence, microwave signals behave and must be treated differently than lower frequency AC signals. In this section we will review some relevant microwave frequency concepts that will be used in device analysis.

All electromagnetic signals obey the Maxwell equations. Because it is not feasible in practice to obtain solutions to Maxwell's equations at all points in space and time, electrical models are employed that give approximate solutions for the equations based on key assumptions. For DC and lower frequency AC signals, the lumped element model is used. This model treats components as discrete units, with

properties of resistance, capacitance, and inductance. A key assumption of this model, however, is that the phase of the AC signal is the same at all points in a discrete element. In other words, the unit is much smaller than the signal's wavelength.

As the wavelength of an electromagnetic signal becomes comparable with the size of the device, the phase of the signal will vary appreciably from one end of the device to the other. At this point the assumption of constant phase is no longer valid, and the lumped element model no longer applies.

In order to understand signal propagation through devices and along transmission lines, a set of microwave engineering concepts has been developed. In this section we will establish some new definitions for impedance and signal transmission and reflection, as well as scattering parameters and the Smith chart. In doing so we will follow the formalism used in *Microwave Transistor Amplifiers* by Guillermo González [25].

A sinusoidal signal in both voltage and current can be described as the real part of its complex exponential function

Eq. 1.12

$$v(x, t) = \text{Re}[V(x)e^{-i\omega t}]$$

$$i(x, t) = \text{Re}[I(x)e^{-i\omega t}]$$

Eq. 1.13

In a lossless medium, these two signals satisfy the wave equation

$$\frac{d^2V(x)}{dx^2} - \gamma^2V(x) = 0 \quad \text{Eq. 1.14}$$

$$\frac{d^2I(x)}{dx^2} - \gamma^2I(x) = 0 \quad \text{Eq. 1.15}$$

where $\gamma = \alpha + i\beta$ and α and β are the attenuation and propagation constants. For a lossless transmission line, $\alpha = 0$.

At every point along this line, there is a ratio between the amplitude of the voltage and that of the current. We define this ratio as the point's characteristic impedance.

$$Z(x) = \frac{V(x)}{I(x)} \quad \text{Eq. 1.16}$$

And for uniform transmission, this value is constant.

$$Z(x) = Z_0 \quad \text{Eq. 1.17}$$

We will see the effects of a non-uniform characteristic impedance below. The general solutions to the wave equations then become

$$V(x) = Ae^{-\gamma x} + Be^{\gamma x} \quad \text{Eq. 1.18}$$

$$I(x) = \frac{A}{Z_0} e^{-\gamma x} - \frac{B}{Z_0} e^{\gamma x} \quad \text{Eq. 1.19}$$

In order to understand the effects of a change of characteristic impedance, imagine that an incident wave travelling in the forward direction terminates at an interface. Some fraction will then be transmitted through the interface and the rest will be reflected. We define Γ_0 as the reflection coefficient, which is equal to the ratio of the amplitude of the reflected wave to the amplitude of the transmitted wave.

$$\Gamma_0 = \frac{B}{A} \quad \text{Eq. 1.20}$$

The general solutions at this interface are then

$$V(x) = A(e^{-\gamma x} + \Gamma_0 e^{\gamma x}) \quad \text{Eq. 1.21}$$

$$I(x) = \frac{A}{Z_0} e^{-\gamma x} - \frac{B}{Z_0} e^{\gamma x} \quad \text{Eq. 1.22}$$

We can then define the characteristic impedance at the interface the same way we did at points along the transmission line.

$$Z_L = \frac{V(x)}{I(x)} = Z_0 \frac{e^{-\gamma x} + \Gamma_0 e^{\gamma x}}{e^{-\gamma x} - \Gamma_0 e^{\gamma x}} = Z_0 \frac{1 + \Gamma_0}{1 - \Gamma_0} \quad \text{Eq. 1.23}$$

Or, solving for Γ_0

$$\Gamma_0 = \frac{Z_L - Z_0}{Z_L + Z_0} \quad \text{Eq. 1.24}$$

The reflection at an interface is directly proportional to the difference in characteristic impedance on either side. The reflection coefficient approaches unity (total reflection) as the load impedance approaches infinity. It also approaches negative unity as the load impedance approaches zero. This situation corresponds to a total reflection with a phase shift of 180° .

Maximum transmission of a signal across an interface occurs when the characteristic impedance must be the same on both sides. This corresponds to a reflection coefficient of $\Gamma_0 = 0$ and 100 percent transmission. In microwave electronics, if two components have the same characteristic impedance they are said to be “impedance matched” and no signal is reflected when passing from one to the other. This concept will be used in the design of our coplanar waveguide electrodes.

In microwave electronics, a transistor is modeled as a two-port network (Figure 1.15). A two-port network has an input port (Port 1) and an output port (Port 2). The incident signals on port 1 and 2 are a_1 and a_2 , and the reflected signals at port 1 and 2 are b_1 and b_2 , respectively.

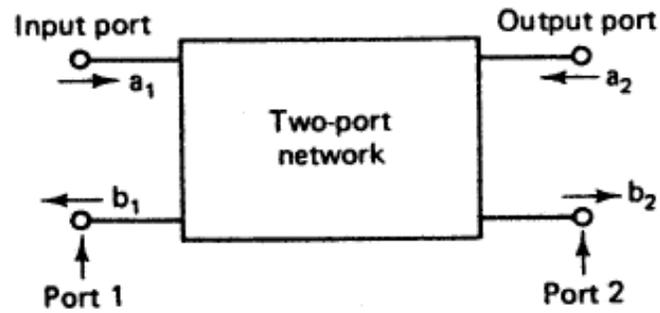


Figure 1.15 – Two-port network [25]

A BJT is a three terminal device, and in order to treat it as a two-port network one terminal must be shared between two ports. The common-emitter configuration was chosen for this project because it generally gives the highest signal gain. In this configuration, the emitter is connected to the ground for both port 1 and port 2.

Two port networks can be characterized by their scattering (S) parameters. These parameters are defined as the ratios between the different incident and reflected signals at the two ports.

$$S_{11} = \left. \frac{b_1}{a_1} \right|_{a_2=0} \quad S_{21} = \left. \frac{b_2}{a_1} \right|_{a_2=0} \quad \text{Eqs. 1.25, 1.26}$$

$$S_{12} = \left. \frac{b_1}{a_2} \right|_{a_1=0} \quad S_{22} = \left. \frac{b_2}{a_2} \right|_{a_1=0} \quad \text{Eqs. 1.27, 1.28}$$

S_{11} is the reflection coefficient (Γ_0) for an incident signal on port 1. S_{22} is the reflection coefficient for an incident signal on port 2. For an impedance matched

network, S_{11} and S_{22} will be small and for a poorly matched network they are close to 1. S_{21} is the forward signal gain of the device and S_{12} is the reverse signal gain. For impedance matched networks, S_{21} and S_{12} are close to 1, for mismatched networks they are low and for active devices with signal gain they are greater than 1.

S-parameters are often displayed visually using a Smith Chart (Figure 1.16) [26].

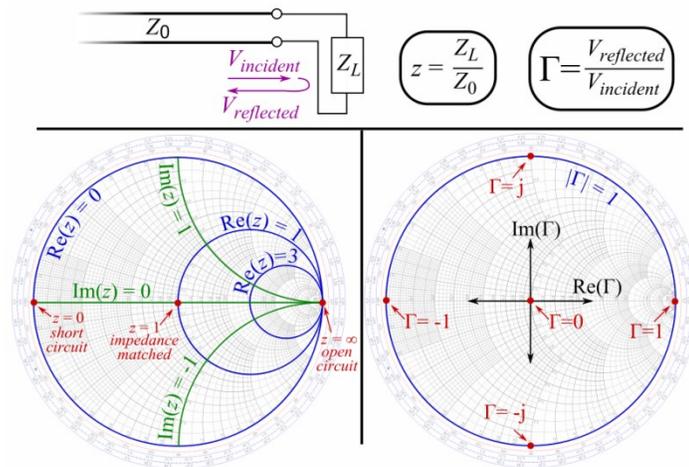


Figure 1.16 – The Smith Chart [27]

The Smith chart can be read quickly to obtain both complex impedance and complex reflection coefficient. Set in a complex plane, the x axis of the Smith chart represents real impedance (resistance). Impedance is scaled so that the origin corresponds to the real impedance of a matched system (for our case 50 Ω). The left end of the real axis corresponds to an impedance of zero and the right end corresponds to an impedance of infinity.

The vertical axis corresponds to imaginary impedance or reactance. The top of the vertical axis represents an infinite inductive load and the bottom represents an infinite

capacitive load. The center of the vertical axis represents zero net imaginary impedance.

Circles of constant normalized real and imaginary impedance are shown in Figure 2. A point's real and imaginary impedance can easily be determined visually by the two circles it intersects.

The real and imaginary components of the complex reflection coefficient are simply the Cartesian coordinates on the Smith chart. The magnitude of the reflection coefficient is its radial distance from the center. Networks with well-matched impedance will appear near the center of the Smith chart and networks with poorly matched impedance will appear toward the edges.

The behavior of microwave networks requires a different set of concepts than is used at lower frequencies. In our characterization of microwave devices, we will use the concepts of characteristic impedance, signal reflection and transmission, and S-parameters. In order to show the real and imaginary components of the S-parameters, it will be useful to view them on a Smith chart. The design of our electrode configuration will be based on the concept of impedance matching, in order to maximize signal transmission and minimize reflection. For our BJT devices, S-parameters will be examined to show transmission and reflection at both biased and unbiased conditions.

1.2.3 Tapered Coplanar Waveguide Electrodes

We saw, in Section 1.2.2, how characteristic impedance affects the transmission of microwave signals across an interface. In order to characterize a device's microwave performance, all components connected to it must be impedance matched, including the on-chip electrodes. At lower frequencies, any geometrical layout with suitably low resistance, capacitance and inductance is suitable to transmit AC signal to a device. At microwave frequencies, however, the characteristic impedance of an electrode depends critically on its geometry.

We require an electrode configuration that is impedance matched to our test equipment, which has a characteristic impedance of 50Ω . Because we are depositing metals onto a flat surface, a planar structure is additionally required. There are a number of planar structures capable of transmitting microwave signals such as microstrips, slotlines, and coplanar strips. The configuration chosen for this project was the coplanar waveguide (CPW). A CPW is compatible with the BJT's three terminal geometry and with the resolution of our photolithography process.

A CPW consists of three metal strips on top of a dielectric substrate (Figure 1.17). The two outer strips constitute the ground plane and in practice are much wider than the center strip. An ideal coplanar waveguide has an infinitely thick substrate and infinitely wide ground planes.

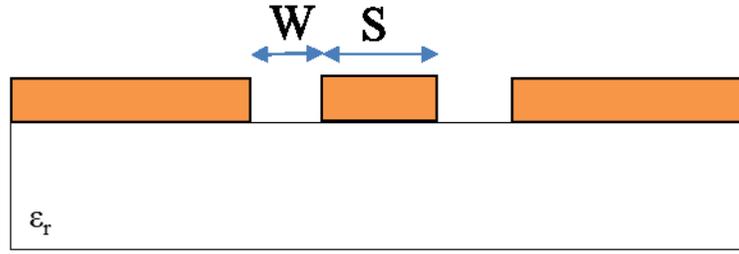


Figure 1.17 – Coplanar waveguide

The characteristic impedance of an ideal CPW is given by the expression [28]

$$Z_0 = \frac{1}{C_{v_{ph}}} = \frac{30\pi K'(S/(S+2W))}{\sqrt{\epsilon_{re}} K(S/(S+2W))} \quad \text{Eq. 1.29}$$

where S is the half-width of the center strip and W is the width of the gap, $K(x)$ is the complete elliptic integral of the first kind and

$$K'(x) = K(\sqrt{1-x^2}) \quad \text{Eq. 1.30}$$

The characteristic impedance of an ideal CPW depends only on the center trace width, gap spacing and dielectric constant of the substrate. In practice, CPWs must have finite dielectric thickness and a constant ground plane width. Additionally, CPWs on SOI have two dielectric layers with different dielectric constants corresponding to the thin buried oxide layer and the thick Si handle wafer. These non-ideal properties of a CPW must be taken into account when designing CPW electrodes.

The first non-ideal characteristic is that the ground planes must have a finite width and the dielectric must have a finite thickness. The characteristic impedance of a CPW with finite width ground planes and a single dielectric layer of finite thickness has been approximated using the conformal mapping method [28]. It is given by

$$Z_0 = \frac{30\pi K'(k_2)}{\sqrt{\epsilon_{re}} K(k_2)} \quad \text{Eq. 1.31}$$

where

$$k_2 = \frac{a}{b} \sqrt{\frac{1 - b^2/c_0^2}{1 - a^2/c_0^2}} \quad \text{Eq. 1.32}$$

$$\epsilon_{re} = 1 + \frac{\epsilon_r - 1}{2} \frac{K(k_3) K'(k_2)}{K'(k_3) K(k_2)} \quad \text{Eq. 1.33}$$

$$k_3 = \frac{\sinh(\frac{\pi a}{2h})}{\sinh(\frac{\pi b}{2h})} \sqrt{\frac{1 - \sinh^2(\frac{\pi a}{2h})/\sinh^2(\frac{\pi c_0}{2h})}{1 - \sinh^2(\frac{\pi b}{2h})/\sinh^2(\frac{\pi c_0}{2h})}} \quad \text{Eq. 1.34}$$

a is equal to half of the center trace width ($S/2$ in Figure 1), b is equal to the distance from the center of the CPW to the ground plane ($S/2+W$ in Figure 1), c_0 is the width of the ground plane, h is the thickness of the substrate and ϵ_r is the relative dielectric constant of the substrate.

This value approaches the ideal approximation as ground plane width and dielectric thickness approach infinity. The method to account for the presence of a two-layer

dielectric has been previously reported for the case of infinite ground planes [29]. In this method, a fill factor is included in the expression for effective relative dielectric constant ($\epsilon_{r\text{eff}}$) to account for the two layers' thicknesses and dielectric constants. This same method can be applied to the above equations to give the impedance of a CPW with finite ground planes and a two-layer finite dielectric thickness. The new expression for $\epsilon_{r\text{eff}}$ is

$$\epsilon_{r\text{eff}} = 1 + \frac{\epsilon_{r1} - \epsilon_{r2}}{2} \frac{K(k_4) K'(k_2)}{K'(k_4) K(k_2)} + \frac{\epsilon_{r2} - 1}{2} \frac{K(k_5) K'(k_2)}{K'(k_5) K(k_2)} \quad \text{Eq. 1.35}$$

where

$$k_4 = \frac{\sinh\left(\frac{\pi a}{2h_1}\right)}{\sinh\left(\frac{\pi b}{2h_1}\right)} \sqrt{\frac{1 - \sinh^2\left(\frac{\pi a}{2h_1}\right)/\sinh^2\left(\frac{\pi c_0}{2h_1}\right)}{1 - \sinh^2\left(\frac{\pi b}{2h_1}\right)/\sinh^2\left(\frac{\pi c_0}{2h_1}\right)}} \quad \text{Eq. 1.36}$$

$$k_5 = \frac{\sinh\left(\frac{\pi a}{2(h_1 + h_2)}\right)}{\sinh\left(\frac{\pi b}{2(h_1 + h_2)}\right)} \sqrt{\frac{1 - \sinh^2\left(\frac{\pi a}{2(h_1 + h_2)}\right)/\sinh^2\left(\frac{\pi c_0}{2(h_1 + h_2)}\right)}{1 - \sinh^2\left(\frac{\pi b}{2(h_1 + h_2)}\right)/\sinh^2\left(\frac{\pi c_0}{2(h_1 + h_2)}\right)}} \quad \text{Eq. 1.36}$$

h_1 and h_2 are the thicknesses of the two dielectric layers and ϵ_{r1} and ϵ_{r2} are their relative dielectric constants.

Using the above expressions along with the known dielectric constants of Si and SiO₂ it is possible to calculate the characteristic impedance of a CPW on SOI of any geometry. Alternatively, the impedance can be set at 50 Ω and a gap spacing (b-a)

can be calculated for a given trace width ($2a$) and ground plane thickness (c_0). Using this method, an impedance matched CPW can be calculated for any arbitrary trace width. Due to the presence of elliptic integrals, the above expressions must be solved numerically.

The final important consideration in the design of the CPW electrode is the size disparity between the microwave probes and the device under test. In order to minimize internal parasitic resistance in our devices, they were designed to be as small as the photolithography tool at LPS could reliably produce. The resulting total device width was $8\ \mu\text{m}$, with contact metal traces separated by approximately $1.5\ \mu\text{m}$. The ground-signal-ground test probes on our probe station have a much larger separation, $150\ \mu\text{m}$ between probes. While smaller probes can be purchased, the smallest commercially available probes have a $50\ \mu\text{m}$ spacing. Even if suitably spaced probes could be obtained, the probe station does not accommodate alignment at the $1.5\ \mu\text{m}$ scale.

Due to these considerations, it is necessary to employ a tapered CPW electrode configuration (Figure 1.18). The probes make contact at the ends where the center trace width is $50\ \mu\text{m}$, well within the alignment capabilities of the probe station. The device is in the center, where the center trace width is $1.7\ \mu\text{m}$. As the center trace narrows, the spacing must also be adjusted in order to maintain a characteristic impedance of $50\ \Omega$.

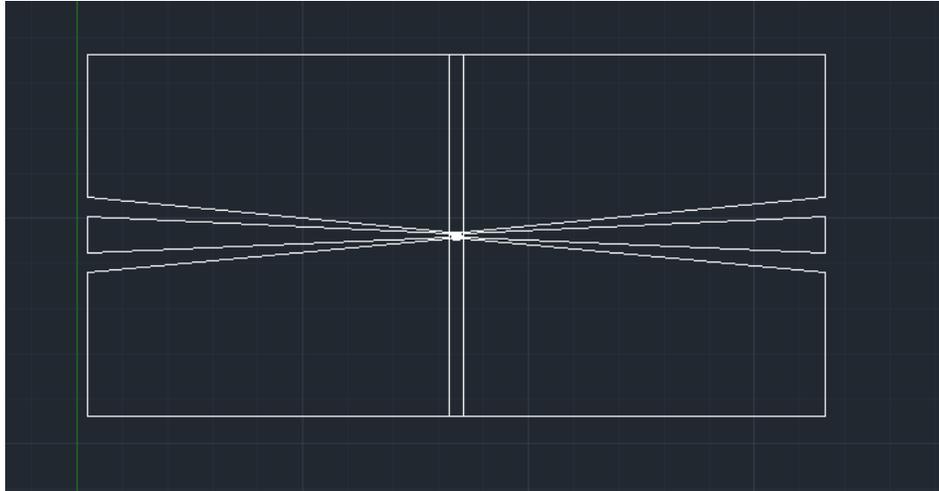


Figure 1.18 – Tapered CPW design

In order to maintain the correct spacing at all points along the waveguide, a Python script was written to calculate the characteristic impedance at every point along the taper. The script uses Newton's method to solve for W given a trace width S , and a characteristic impedance $Z_0 = 50 \Omega$. The output is an Autocad macro that draws the taper with the correct spacing. The resulting Autocad shape was then used in the photomask design file.

In order to use this tapered CPW design with confidence, the electrode configuration is also characterized. The structure used for electrode testing is shorted where the device would otherwise be (Figure 1.19). This allows us to test the CPW itself, independent of the effects of the Si BJT.

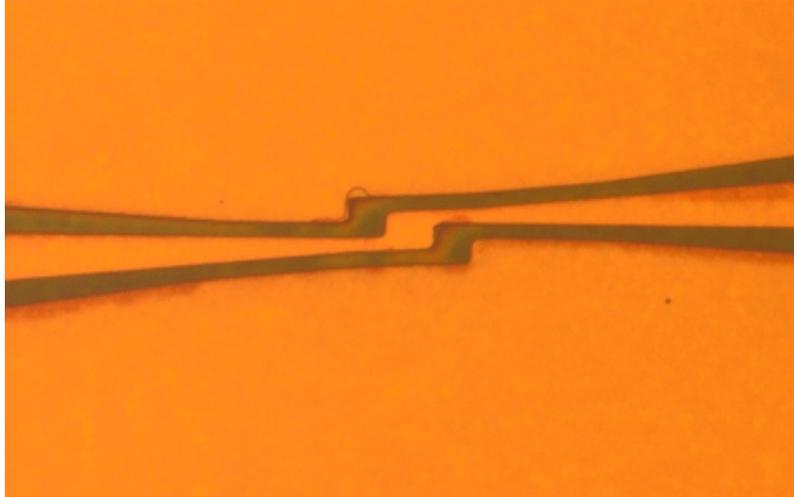


Figure 1.19 – Shorted electrode configuration

This “shorted” configuration was chosen because it better represents the final device than an electrode that passes straight through. The taper coming in from the left will contact a different device region than the one coming in from the right. In the center region, the spacing of the CPW is interrupted, due to the shift associated with making contact to two different terminals of the Si device. This interruption will necessarily cause some impedance mismatch. High frequency modeling and electrode fabrication and testing were performed to determine if the reflection due to this interruption is suitably low.

The structure is imported into the Ansys High Frequency Structure Simulator (HFSS). Port 1 is placed along the left end of the taper, with the signal along the center trace and the outer planes set at ground and Port 2 is placed along the right end. A frequency sweep is performed and S-parameters were obtained from the software.

The simulation result shows very high transmission of the signal through the taper (Figure 1.20). Approximately 96% of the signal is transmitted, and only 2% is reflected. Signal reflection is attributed to a small impedance mismatch at the center of the taper, where the shorted electrodes are located. The remaining 2% signal loss can be attributed to losses in the substrate and the metal itself.

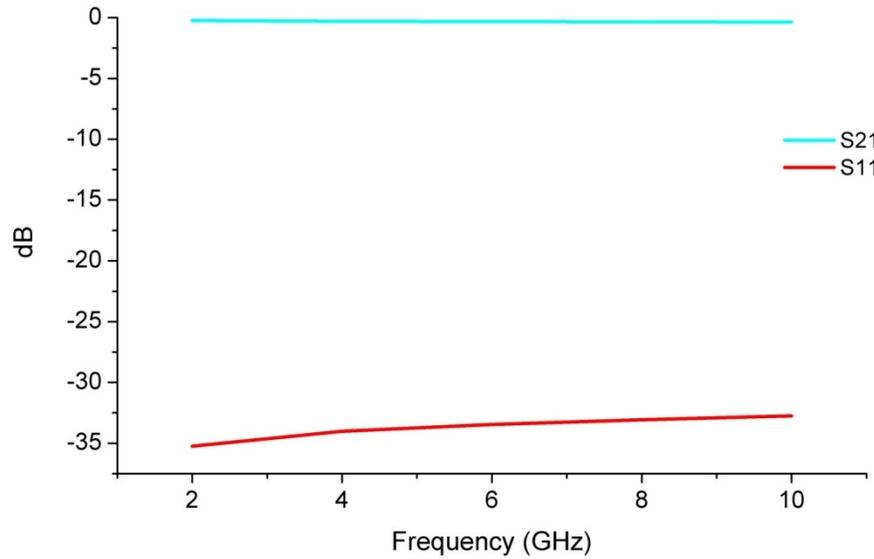


Figure 1.20- HFSS simulation results for signal transmission and reflection

The simulation results are consistent with expectations. Some reflection is present, but it is low enough to be considered acceptable. Based on the results of this simulation, a photomask was ordered and a shorted CPW was fabricated on SOI.

In order to best replicate the conditions of the final devices, test electrodes were fabricated on SOI with the top Si layer completely etched. Standard photolithography is performed to pattern the region of metal deposition. 30 nm of Ti is deposited as an adhesion layer, on top of which 700 nm of Au is deposited. Lift-off is performed in

acetone. S-parameters are measured using an Agilent E5071C network parameter analyzer. The test probes were Picoprobe model 40A-GSG-150-P.

S-parameter measurements show qualitatively similar performance, but less ideal than simulation (Figure 1.21). Approximately 80 percent of the signal is transmitted, and approximately 11 percent reflected.

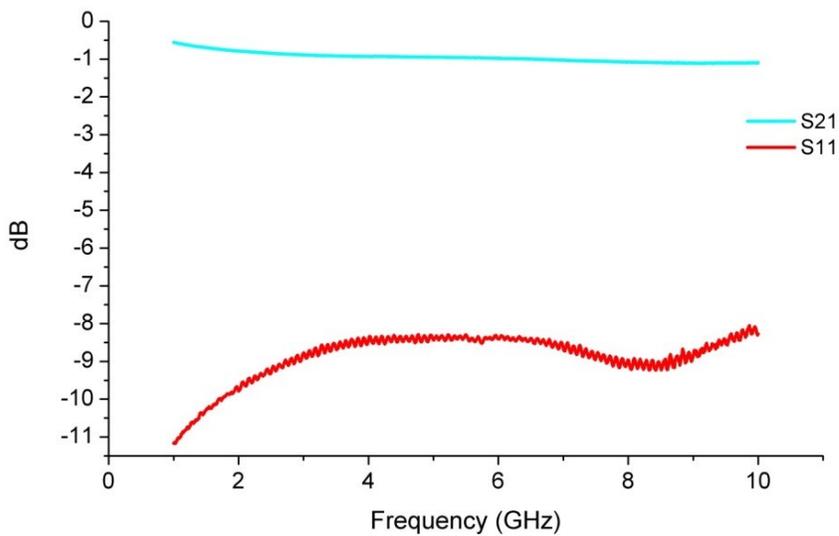


Figure 1.21 - S-parameter measurements for tapered CPW

This higher level of reflection could be due to a number of factors. Whereas the simulation assumes 100 percent transmission into the CPW itself, it's possible that one source of reflection is the interface between the probes and the metal. Factors in the fabrication process like resist shrinkage or overexposure could affect critical spacing and cause an impedance mismatch. Additionally, there could be coupling with other devices on the same chip.

After reviewing the measurement results, it was determined that a loss of -1 dB through the measurement apparatus is sufficient and a signal reflection -8.5 dB is low enough to be acceptable. Enough signal is transmitted through the test structure that we are confident we should see the effects of the BJT. Based on the HFSS model and the shorted electrode test data, we decided to use the tapered CPW electrode structure for BJT devices.

In conclusion, a tapered CPW electrode has been designed to meet the on-chip measurement needs for our Si BJT. Established methods are used to calculate the impedance of a CPW on a two-layer dielectric with a finite ground plane, and a Python script is used to solve for the spacing of the CPW as a function of the trace width. This script was then used to calculate the spacing at all points along a taper going from the widely spaced probe to the small contact regions on a Si BJT.

High frequency modeling shows that the structure is well matched to a 50 Ω transmission line. A test electrode structure was fabricated and measured. While the real-world measurement shows higher signal reflection and loss than the simulation, the high level of signal transmission is sufficient for microwave frequency measurements.

Chapter 2: Transfer Printing

2.1 Transfer Printing of Patterned Metal Films

The integration of flexible devices into complex circuits requires metal interconnects and electrodes. The first project presented in this dissertation is a technique for transfer printing of metal films. This work was carried out in parallel with the development and fabrication of BJTs, with the goal of enabling fully transfer printed microwave devices in the future.

There are several techniques for creating metal interconnects on metal substrates. Ink-jet printing and soft lithography techniques exist, but these often suffer from low resolution and poor film quality. Using transfer printing, high quality films can be fabricated on a Si wafer and then transferred to a flexible substrate.

Earlier work has described successful transfer printing of Au films [30], but transfer printing of other metal films has not been achieved previous to this study. Without surface modification, evaporated metal films adhere too strongly to bare Si substrates and cannot be transferred using conventional methods. In this study, we develop a method for transfer printing of five different metals by pre-coating the deposition substrate with parylene C in order to reduce adhesion and enable the transfer process [31].

Transfer printing is based on the principle of differential adhesion. If a material is weakly bound to one substrate and brought into contact with another, more adhesive substrate, it will transfer to the target substrate when the two are separated. If a substrate can be made adhesive through surface treatments such as adhesive coatings or plasma treatment is a suitable target (post-transfer) substrate material for transfer printing. Conversely any substrate whose adhesion can be made sufficiently low is a candidate for pre-transfer processing.

Adhesion can be caused by chemical bonding, electrostatic forces, mechanical interlocking of materials, diffusion, polar interaction, and dispersive forces (wetting). Among these, polar and dispersive adhesion are the primary forces in evaporated metal films. By controlling polar and dispersive adhesion, we can fabricate substrates that have desirable characteristics for transfer printing. The combination of polar and dispersive contributions to a substrate's adhesion is the substrate's surface energy.

Surface energy is a measure of the energetic disruption of molecular bonds that arises due to the formation of a surface. Liquids and vapor on a surface with high surface energy will more readily wet the surface and adhere more strongly to it. Total surface energy is simply the sum of the polar and dispersive contributions.

Surface energy is typically measured by contact angle measurements with various liquids of known polar and dispersive properties [32]. This technique, described in

detail later, is used in this study as a measure of the polar and dispersive adhesive properties of substrate surface treatments.

A range of metals deposition techniques has been developed to accommodate the needs of flexible electronics. Ink printing has been demonstrated [33] but faces challenges. An ink containing conducting or semiconducting material can be deposited directly onto a target substrate. Typically, this ink must be sintered at high temperature after deposition in order to remove solvents and obtain useful conductivity values. Ink rheology and drying time have a significant effect on film quality as well as adhesion. These challenges have limited the reported resolution of ink-based printing technology to tens of microns [34]. The use of solvents, variable film quality and resolution, and need for high-temperature processing makes ink based material deposition incompatible with many flexible substrates and applications.

Soft lithography transfer methods have been developed for transfer of deposited material from one substrate to another [35]. These typically employ an elastomeric stamp with raised features corresponding to the final patterned film. The stamp is designed to have low adhesion to the deposited film, and when brought into contact with a target substrate, the film transfers over. Soft lithography can be performed as an additive process, producing a minimum of waste material, and once a template has been fabricated, it can be reused many times. Flexible stamps can also be applied to non-planar surfaces. Flexible stamps, however, are susceptible to distortions. Strain

from the printing process can deform the stamp causing pairing and sagging, as well as swelling and shrinking of features [36]. The resolution, while better than ink-based printing is typically no less than one micron [37].

Transfer printing offers advantages over ink and soft-lithography based techniques [38]. Resulting films can consist of high quality materials at very high resolution on a wide range of substrates. Materials are fabricated and patterned on a host substrate of choice, and then transferred via differential adhesion to a target substrate. The host substrate can be chosen such that it is able to withstand harsh processing steps. Some examples include carbon nanotubes that have been grown on SiO₂ substrates at temperatures above 800°C, organic semiconductors deposited onto octadecyltrichlorosilane (OTS) treated SiO₂ substrates, and graphene deposited at temperatures above 900°C [30]. All have been successfully transferred to alternate substrates using surface functionalized transfer printing (SFTP). The only requirement for the transfer of these and other high-quality materials to alternate substrates is the ability to establish differential adhesion between the host and target substrates. In addition to high quality materials, SFTP allows for resolutions limited only by lithography technique. In combination with e-beam lithography, SFTP can achieve resolutions much lower than one micron.

Prior to this study, Au was the metal of choice for transfer printing. Au exhibits relatively low adhesion to Si substrates when deposited via e-beam evaporation. This low adhesion to the host substrate facilitates transfer to a variety of target substrates.

Other metals, however, typically exhibit stronger adhesion to Si substrates, limiting their utility for transfer printing.

One attempt at lowering the adhesion of deposited metal films onto Si substrates has been the formation of self-assembled monolayers (SAMs) on the substrate before metals deposition [39]. Any surface treatment candidate for use in transfer printing must meet three main requirements:

1. The adhesion of the deposited film to the treated substrate must be high enough for the film to survive pre-transfer processing, usually photolithography, metals deposition and liftoff.
2. The same adhesion must not be higher than that of the metal film to the target transfer substrate, which would prevent successful transfer.
3. The surface treatment must survive the entire transfer process without significant damage, which could degrade its adhesion-lowering properties.

1H,1H,2H,2H-perfluorodecyltrichlorosilane (FDTS) has been used as a release layer to lower the adhesion of nanoimprint lithography templates to polymer films [40]. FTDS has been reported to significantly lower the surface energy of Si surfaces. Janssen has reported a surface energy of 16.14 mJ/m² for an FTDS coated Si wafer, as compared to 71.91 mJ/m² for bare Si surfaces. This creates a very low adhesion between the deposited film and deposition substrate. However, metal films with feature sizes less than ~100 μm have not been found to survive photolithographic processing. Typically, deposited films are washed away during lift-off indicating that

the adhesion between the films and substrate is too low and our first requirement is not met [41].

OTS had previously been used to lower the surface energy of SiO₂ substrates in order to improve the crystallinity of organic films [42]. OTS treated Si has a reported surface energy of 25.38 mJ/m² which is higher than FTDS, but still well below that of bare Si. While OTS treated samples do survive pre-transfer processing, films do not release completely during transfer. Previous studies have reported degradation of OTS films beginning around 180 °C [43] which is below the temperatures experienced during the transfer process. The high pressure and elevated temperature of the transfer process, therefore, likely damages the OTS monolayer, which would indicate that OTS treatment does not satisfy our third requirement.

In this study, we develop a surface treatment for transfer printing of metals that satisfies all three requirements. Parylene C is a polymer commonly used as a moisture-proof coating in medicine and electronics. It is compatible with all solvents and developers used in our photolithography process and has a reported dissociation temperature of 290 °C, [44] which is well above the temperature of transfer printing which we set at 175 °C. We use parylene C as a surface treatment that has a suitable surface energy (and corresponding adhesion) and which remains stable throughout the fabrication and transfer process.

In order to determine the surface energy of parylene C, contact angle measurements were performed using a Ramé-Hart contact angle goniometer. A liquid droplet was dispensed onto the surface of a given solid substrate and the angle of the liquid formed at the surface of the solid substrate was measured. This was done using 4 different liquids (water, ethylene glycol, formamide and diiodomethane) with five angle measurements averaged together for each liquid on a given surface. The total, dispersive and polar components of the surface energy of the solid substrate surface can then be calculated using Equations 2.1 and 2.2 [32]:

$$(1+\cos\theta)/2(\gamma_l^T/\gamma_l^D)^{1/2} = (\gamma_s^P)^{1/2} (\gamma_l^P/\gamma_l^D)^{1/2} + (\gamma_s^D)^{1/2} \quad \text{Eq. 2.1}$$

$$\gamma_s^T = \gamma_s^D + \gamma_s^P \quad \text{Eq. 2.2}$$

where θ is the measured contact angle and γ_l^T , γ_l^D , γ_l^P are the known values of the total, dispersive and polar components of the test liquids, respectively.

Liquid	Contact Angle	γ_l^D (mJ/m ²)	γ_l^P (mJ/m ²)
Water	81.04°	21.8	51.0
Formamide	68.12°	34.0	30.0
Ethylene Glycol	58.04°	29.0	19.0
Diiodomethane	36.54°	50.8	0.0

Table 2.1 – Contact angle data for parylene C

A plot of the (known) left hand side of Eq. 1 vs. $(\gamma_l^P/\gamma_l^D)^{1/2}$ is therefore linear, with a slope of $(\gamma_s^P)^{1/2}$ and a y intercept of $(\gamma_s^D)^{1/2}$ (Figure 2.1).

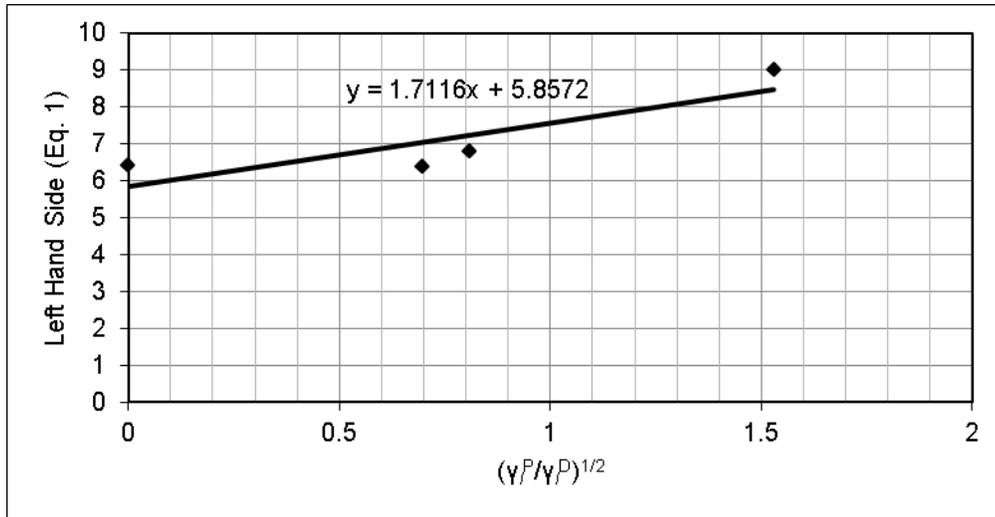


Figure 2.1 - Linear regression to determine γ_s^P and γ_s^D

A linear regression shows the slope to be 1.71 +/- 0.72 and the intercept to be 5.87 +/- 0.68. This corresponds to a γ_s^P value of 2.93 mJ/m² +3.02/-1.96 mJ/m² and a γ_s^D value of 34.31 mJ/m² +8.63/-7.36 mJ/m² for a total surface energy of 37.23 mJ/m² +9.14/-7.61 mJ/m². The measured value of surface energy for parylene C falls in the range between SAM surface treatment (OTS, FTDS) and the surface energy of bare Si. Based on surface energy measurements, it is determined that parylene C has the adhesive properties needed for transfer printing of metal films.

The processing steps for the fabrication of patterned metal films onto parylene C coated Si wafers (Figure 2.2, 1 – 3) and the transfer printing of the patterned metal films onto a plastic substrate (Figure 2.2, 4 & 5) are shown in Figure 2.2.

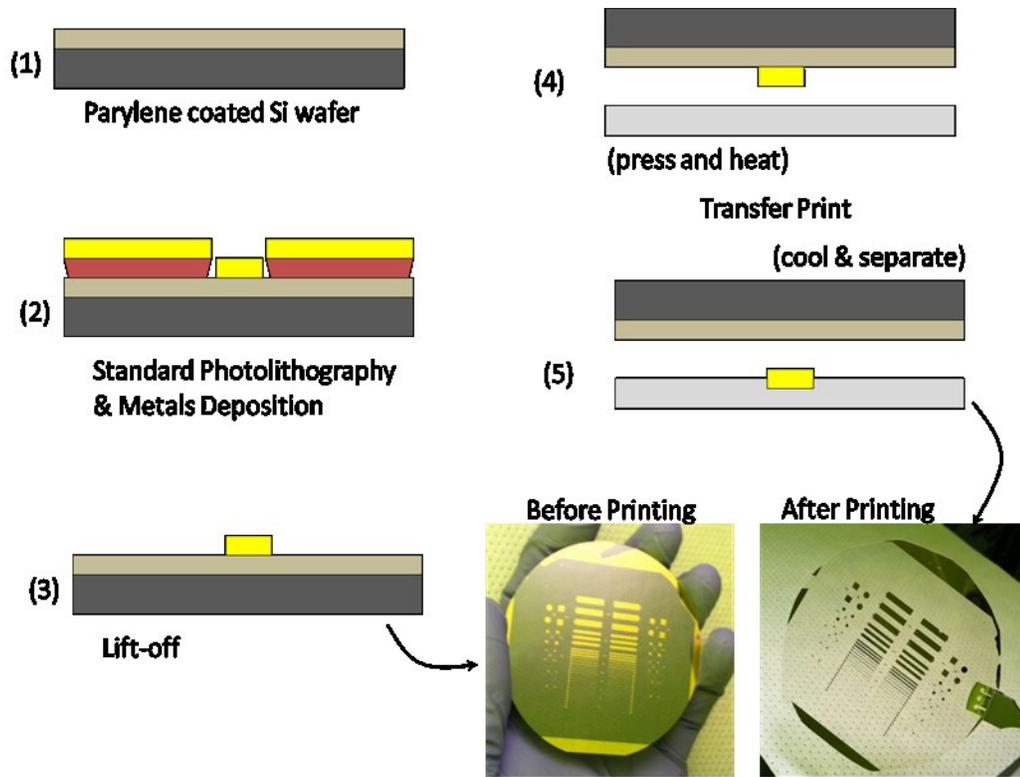


Figure 2.2 – Fabrication and transfer process

Three inch diameter Si wafers were purchased from Silicon Quest International and used as received. The wafers are coated with a 25 μm thick parylene C film by Specialty Coating Systems. Wafers are coated on both sides, with the parylene film continuous over the edge from one side to the other. This two-sided coating prevents delamination of the parylene film during processing. If the wafer is diced, the film will no longer be continuous over the edge, and delamination is likely. Therefore, only full 3" wafers are used in this study. No adhesion promoters are applied to the Si wafer prior to parylene deposition. (Figure 2.2, 1). Standard photolithography, vacuum deposition of metals and lift-off is performed on the surface of the parylene coated wafer (Figure 2.2, 2 & 3) resulting in a patterned metal film as seen in the optical image (left image) in Figure 2.2. An oxygen plasma treatment using a

PlasmaStar Axic system at 100 SCCM and 200 Watts is performed for 1 minute on the surface of a polyethylene naphthalene (PEN) plastic substrate. The plasma treated PEN surface is placed in contact with the patterned metal surface of the parylene coated Si wafer and the two substrates are then placed together in a Nanonex NX2500 imprinter machine for transfer printing. Transfer printing is performed in the NX2500 chamber at approximately 175 °C and 500 psi for 3 minutes (Figure 2.2, 4). The substrates are then removed from the chamber and separated (Figure 2.2, 5). The resulting successfully transfer printed metal films are shown in the optical image (right image) in Fig. 2.2 and in the optical images in Fig. 2.3 for Al, Cu, Ni, Ag and Au (from left to right).

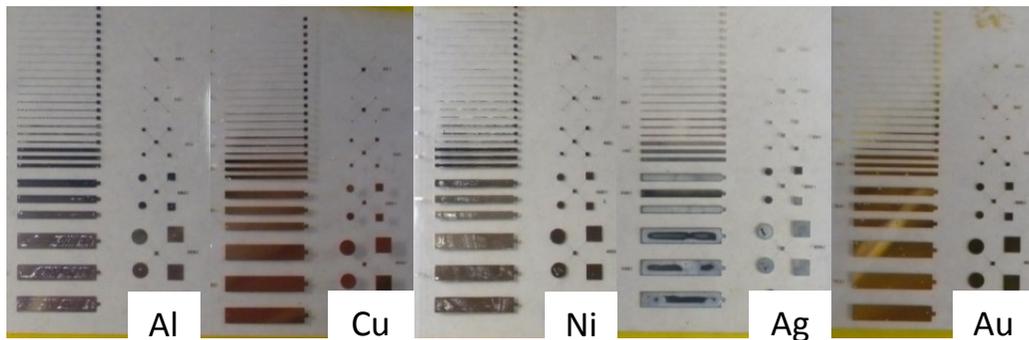


Figure 2.3 – Successfully transferred metal films

Thickness measurements are taken before transfer using a Tencor Alpha-step 200 profilometer. Resistance measurements are taken with a handheld Fluke multimeter at the ends of 1 cm long bars of varying widths (as shown in Fig. 1). Pre- and post-transfer resistivity measurements are shown in Table 2.2.

Metal	Pre-transfer Resistivity	Post-transfer Resistivity
Al	41.7 nΩm	37.5 nΩm
Ag	13.9 nΩm	17.6 nΩm
Cu	15.6 nΩm	15 nΩm
Ni	80.1 nΩm	81.0 nΩm
Au	21.8 nΩm	20.7 nΩm

Table 2.2 – Pre- and post-transfer resistivity measurements

Resistivities are comparable to bulk values for each metal, indicating that the films are of high quality. Additionally, post-transfer resistivity values are not significantly reduced due to the transfer process. This indicates that the films are not damaged during transfer.

In this study, a method was developed for transfer printing deposited metal films onto flexible plastic substrates. In order to overcome previous limitations, a parylene C film is used as a surface treatment before metals deposition. The surface energy of deposited parylene C was measured to be $37.23 \text{ mJ/m}^2 \pm 9.14/-7.61 \text{ mJ/m}^2$, which indicates its desirable adhesion to deposited metal films. Parylene C coated Si wafers show adhesion to metal films high enough to withstand pre-transfer processing but low enough to facilitate film transfer. Resistivity is measured before and after transfer, and was not found to degrade significantly during the transfer process.

2.2 Silicon Nanomembrane Transfer Process

In Chapter 1.1 the basic process of nanomembrane release and transfer was described. A number of variations on this method have been developed to suit the needs of

specific applications. In this study, we reproduce one transfer method from the literature. Additionally, we develop a previously unreported method for transfer of multiple small SiNM structures with good alignment.

The SiNM transfer process relies on selective etching of the sacrificial buried oxide, combined with one of several methods for transferring the decoupled SiNM to an alternate substrate. First, the buried oxide must be exposed by partially etching the top Si layer (Figure 2.4). The remaining Si will constitute the SiNM. If the SiNM feature is large, it can be perforated with small holes in order to reduce etching time (Figure 2.5).

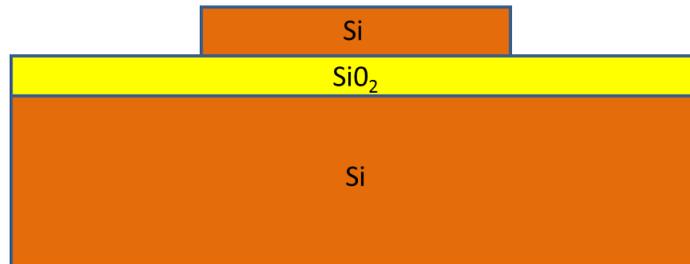


Figure 2.4 – Partially etched top Si layer

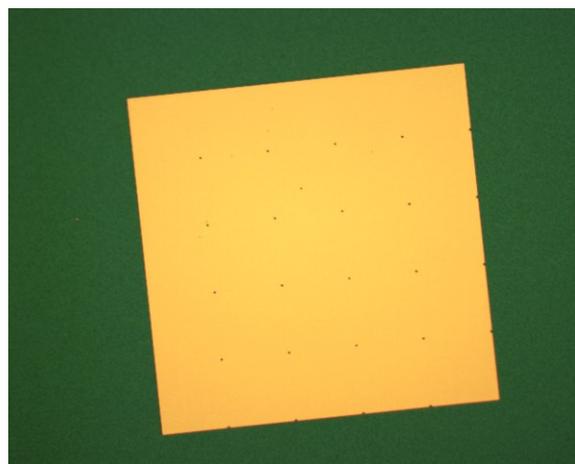


Figure 2.5 – Perforated Si sheet

Once the buried oxide is exposed, the sample is submerged in HF. HF and Buffered HF solutions have been shown to etch SiO_2 over Si with high selectivity [45]. The HF solution etches the buried oxide layer and undercuts the remaining top Si layer (Figure 2.6). The undercut begins at the edge of the Si features and etches inwards in an isotropic and predictable manner. In Figure 2.7 the remaining SiO_2 can be seen through the translucent SiNM at the center of the four large square features. The rate of lateral undercut for SOI with a 200 nm top Si layer and 400 nm buried oxide layer is measured to be 1.2 $\mu\text{m}/\text{minute}$ for 49% HF solution.

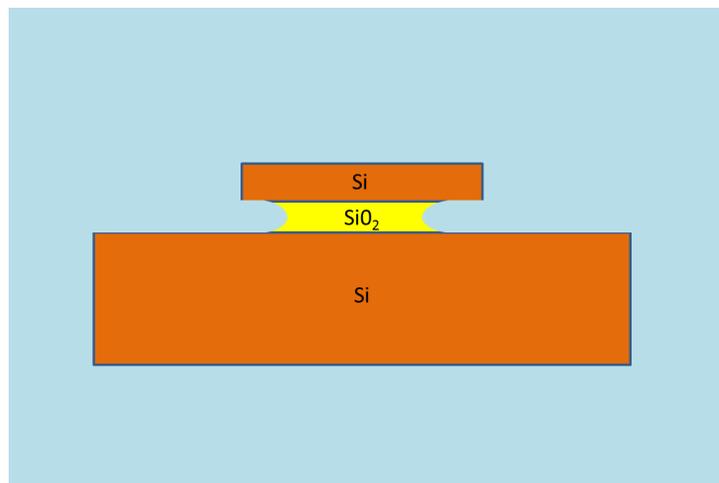


Figure 2.6 – Diagram of HF solution undercut

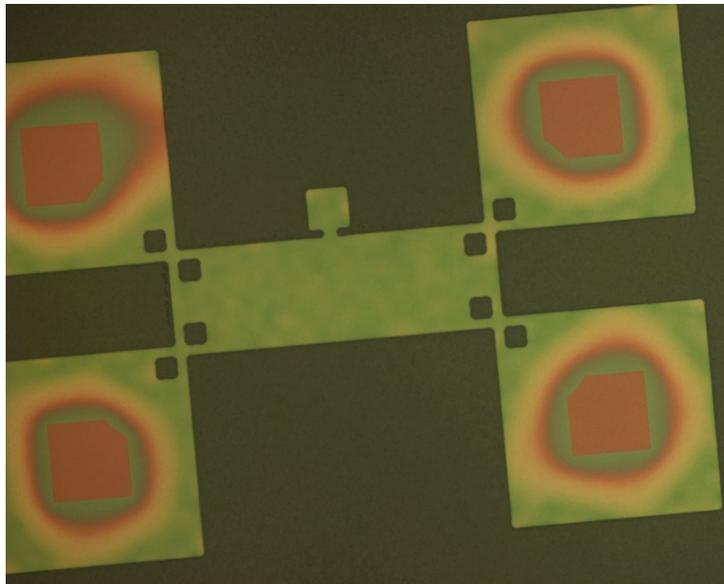


Figure 2.7 – Partially undercut Si feature

If left long enough, the HF solution will completely etch the buried oxide layer, leaving the released SiNM weakly coupled to the Si handle wafer (Figure 2.8).



Figure 2.8 – Completely released SiNM

Upon removal from HF, the surfaces of the SiNM and the Si handle wafer are hydrogen terminated [46]. A combination of Van der Waals forces, hydrogen bonding and hydrophobic interaction couples the membrane to the Si handle wafer. In order to avoid contamination, the sample must then be rinsed in de-ionized water and dried.

The steps of patterning the top Si layer and fully etching in HF solution are common to nearly every reported SiNM transfer method. The main exceptions are the use of HF vapor instead of liquid solution [47] and the etch technique presented in this work where the etch is stopped before the membrane is fully released. Once the buried oxide has been etched, the different transfer techniques diverge.

A wet transfer technique has previously developed in which the membrane is left in H₂O until it loses its hydrophobic properties and floats to the surface. It can then be scooped up with another substrate and heated to bond the SiNM to the new substrate [48]. Another technique uses a sacrificial polymer stamp to pick up the SiNM features and then bond them to a final adhesive polymer substrate (Figure 2.9) [49]. Kinetic control of adhesion has also been demonstrated as a transfer technique [50].

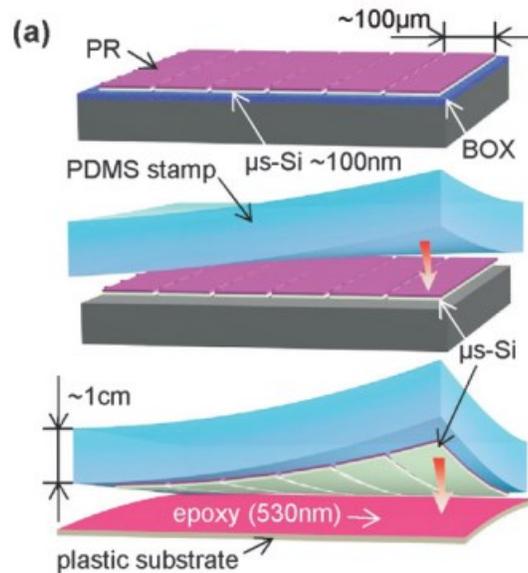


Figure 2.9 Stamp assisted SiNM transfer [49]

The transfer method replicated in this project was the flip-transfer method. The flip-transfer method is reported in many publications due to its simplicity and because it does not require special equipment. It can be performed at room temperature and is compatible with a variety of adhesive substrates. A schematic of the flip-transfer method is shown in Figure 2.10. The membrane is fully released and then brought directly into contact with an adhesive target substrate. Because the SiNM is weakly coupled to the Si handle wafer, it transfers and stays adhered to the target substrate when the two are separated.

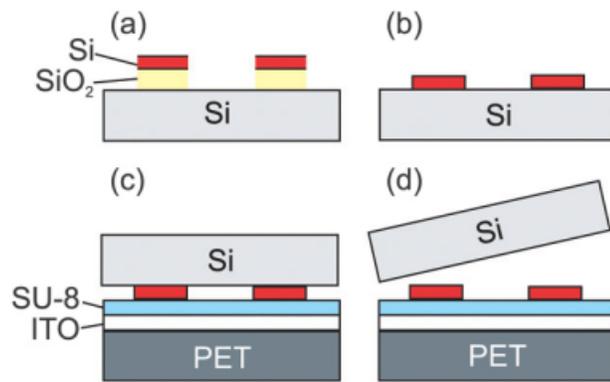


Figure 2.10- The flip-transfer process [7]

As the name implies, the process flips the membrane during transfer. This can be beneficial because it allows for processing on both sides of the SiNM. It can also be problematic, since areas of metal contact need to be heavily doped to achieve ohmic contact. This means that heavily doped areas must be formed on the bottom of the Si layer before transfer.

In our replication of the flip-transfer technique, the SiNMs are fully released and rinsed as described above. DuPont HD-4100 polyimide is spin coated onto a kapton substrate and pre-baked at 120 °C for 3 minutes. The etched SiNM and handle wafer are then brought into contact with the kapton substrate, gently pressed, and the substrates are separated.

Our investigations find that the flip-transfer process works consistently well for large area SiNMs (Figure 2.11). The large contact area between the membrane and the Si substrate gives the released SiNM sufficient coupling from Van der Waals and hydrogen bonding that the membrane stays in place during rinsing and transfer.

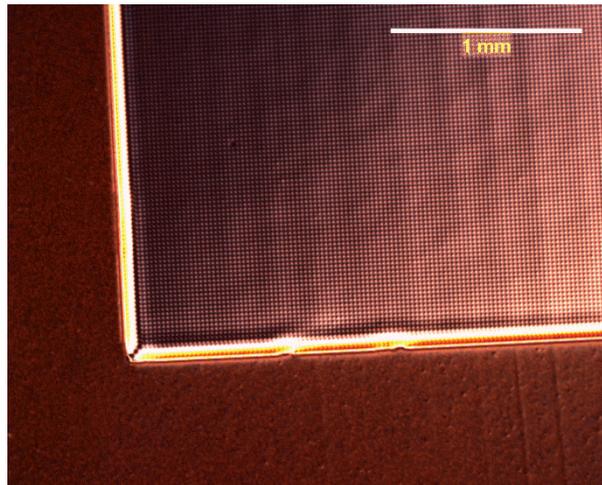


Figure 2.11 – Large area, flip-transferred SiNM

Flip-transfer of smaller devices, however, is less consistent. SiNMs with contact areas less than 0.05 mm² will often move or float away during rinsing and transfer (Figure 2.12). Some transfer attempts were successful (Figure 2.13) but overall yield

was below 25%. Even in successful transfers, there was still some misalignment and out of plane deformation (top left, Figure 2.12).

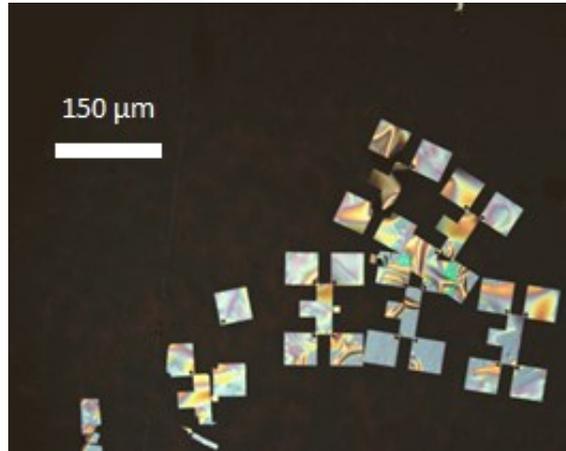


Figure 2.12 – Shifting during flip-transfer

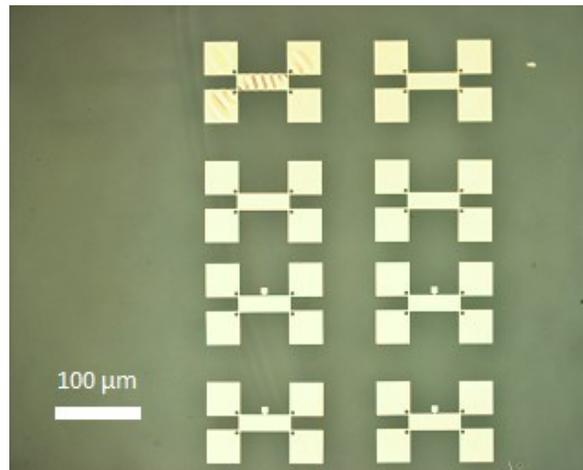


Figure 2.13 – Successful transfer

Our findings show that due to their low contact area, features smaller than 0.05 mm^2 do not have sufficient coupling to the substrate to keep them from moving during rinsing and transfer. These small features require a transfer method that holds SiNMs in place during rinsing and drying. In this work we develop a technique in which the

buried oxide layer is partially but not fully etched, leaving behind oxide “pillars” that anchor the membrane in place until final transfer is achieved.

Since HF undercuts the Si isotropically from the sides, the largest non-perforated features are the last to fully release. Figure 2.14 shows a design with four 100 μm by 100 μm pads that were etched in 49% HF for 40 minutes. At the center of each large pad remains a small pillar of buried oxide, and the membranes retain their alignment during rinsing.

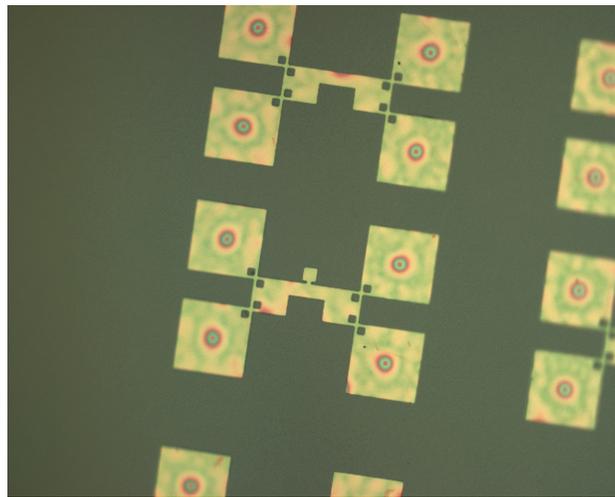


Figure 2.14 – Partially released SiNMs

The target substrate is prepared by spin-coating HD-4100 polyimide onto a kapton substrate and pre-baking for 10 minutes at 120° C. The two substrates are then brought into contact and pressed together at high temperature and pressure until the oxide pillar punches through the membrane, releasing it from the Si handle wafer.

Transfer is carried out in a Nanonex NX 2500 nanoimprint lithography tool. The two substrates are placed in between two polymer sheets and into a holder. The holder is then loaded into the machine where a piston is clamped down around it. Compressed nitrogen is then fed into the piston to provide the necessary pressure for the transfer process. Transfer was carried out at 100° C and 200 psi for 3 minutes. After venting and cooling, the two substrates were separated, and the SiNMs had transferred to the kapton substrate. Figure 2.15 shows transferred SiNMs with holes where the oxide pillars punch through. Alignment is maintained throughout the transfer process.

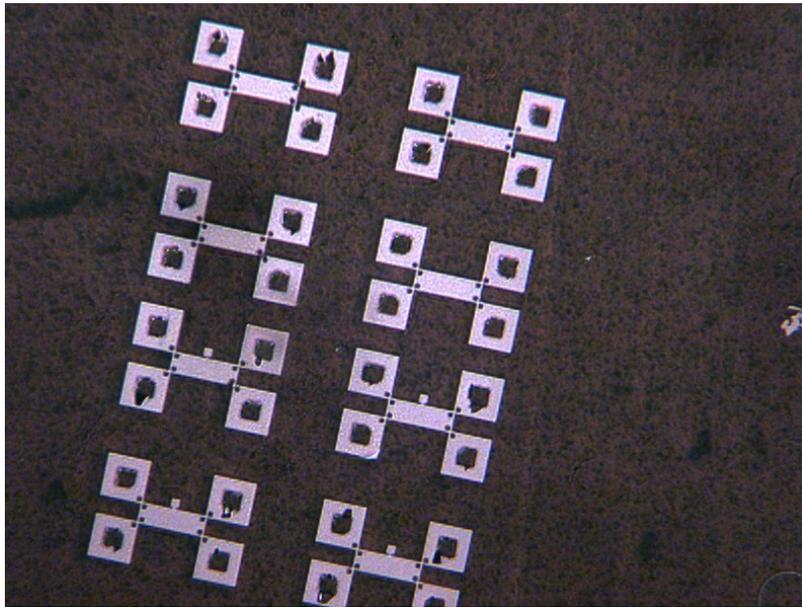


Figure 2.15 – Transferred aligned SiNMs on kapton

The main advantage of this method over methods that fully release the SiNM is the ability to transfer small SiNM features without causing misalignment. Because alignment is maintained, high resolution post-transfer processing is possible. As a

proof of concept, post-transfer metals deposition and lift-off (Figure 2.16) and silicon reactive ion etching (Figure 2.17) were demonstrated on kapton substrates.

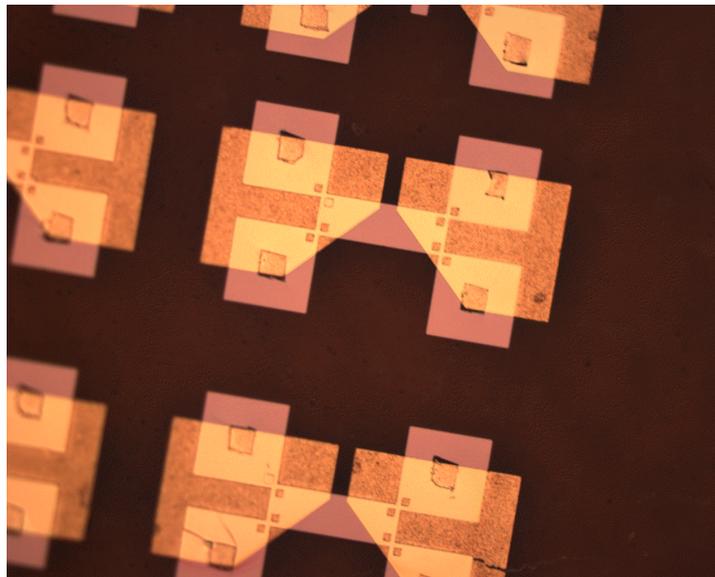


Figure 2.16 – Au electrodes on transferred SiNMs

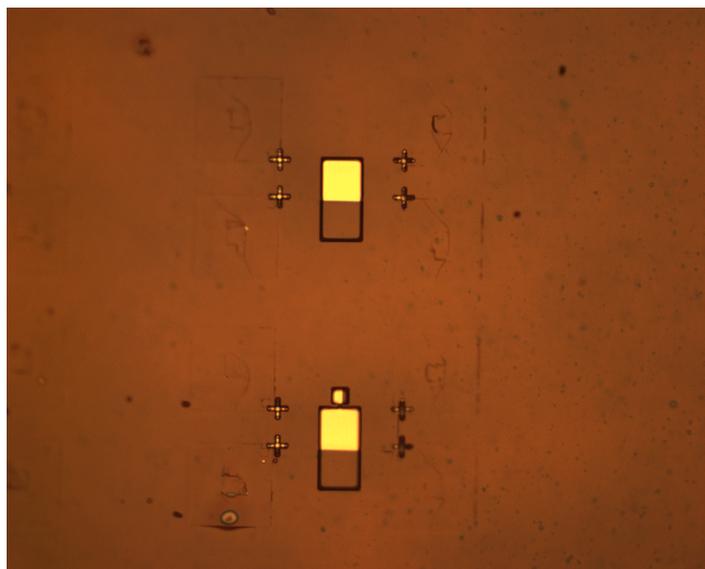


Figure 2.17 – Etched SiNM on kapton

This study reviews the reported SiNM transfer techniques and replicated the flip-transfer method. We find that the flip-transfer method is suitable for large SiNMs, but that small features are often misaligned or washed away due to their weak coupling to the Si substrate. We have developed a technique for SiNM transfer that anchors devices in place throughout the transfer process. The oxide pillar technique developed in this study enables the transfer of small SiNM features without misalignment and enables post-transfer processing of SiNM devices.

Chapter 3: Bipolar Junction Transistor Design and Fabrication

BJT operation was described in Chapter 3. In this section, we describe the design, modeling, and fabrication of BJTs on SOI with the ultimate goal of transferring them to flexible substrates. In designing the devices, we consider two known sources of signal loss and chose a geometry that minimizes their effect. Once a configuration is chosen, ion implant modeling is carried out in order to verify the presence of the n type collector and emitter regions and the p type base region.

The design used in this project calls for a base region that is narrower than the resolution of our lithography. In order to define this region, we use a previously reported self-aligned poly-Si sidewall spacer technique [51]. Sidewall spacer formation is confirmed using cross-sectional SEM. Post-implant annealing is also modeled and performed to ensure that dopant diffusion does not significantly alter the configuration of n-and p-type regions. Pre-metallization fabrication concludes with a protective nitride patch over the side of the device to prevent the base electrode from making contact with the underlying collector region.

3.1 Device Design

The design of transferrable ultrathin BJTs on silicon on insulator (SOI) addresses two known mechanisms for signal loss. They are:

1. Recombination of minority charge carriers in the intrinsic base region
2. Parasitic junction capacitance

When the emitter-base junction is forward biased, electrons flow into the p type base region as minority carriers. They then diffuse thermally into the base region, until one of two things happens. An electron can diffuse across the base region entirely, at which point the electric field of the reverse-biased base-collector junction sweeps it into the collector. Alternately, it can recombine with a majority carrier hole. Electrons that diffuse all the way to the collector are the source of gain in a BJT amplifier, and recombination is a source of signal loss. The concentration of minority carriers that diffuse across the base region to the collector is given by:

$$n' = A e^{-W/L_e} \quad \text{Eq. 3.1}$$

Where W is the width of the base region and L_e is a dopant dependent recombination length, typically on the order of microns in Si [52]. Because of the exponential nature of this expression, small reductions in W/L_e can cause a large increase in electron concentration at the collector which equates to a large increase in signal. It is apparent, then, that devices with an ultra-narrow base region will give the highest signal with the lowest rate of recombination.

The second source of loss, junction capacitance, is addressed through the lateral configuration of the device. Junction capacitance of a rectangular pn junction is given by the expression:

$$C_j = WL \frac{\epsilon_{Si}}{d} = WL \sqrt{\frac{q \epsilon_{Si}}{2(\varphi - V_a)} \frac{N_a N_d}{N_a + N_d}} \quad \text{Eq. 3.2}$$

where φ is the built-in junction potential, q is the charge of an electron, V_a is the applied voltage, N_a and N_d are the dopant concentrations, W is the width and L is the length of the rectangular junction area. A lateral NPN configuration is chosen so that W is the thickness of the top SOI layer (200 nm) and L is defined photolithographically. By defining the smallest junction area allowed by our lithography techniques, parasitic junction capacitance should be minimized.

3.2 Implant Modeling

All ion implantation steps are modeled using two different software packages, Stopping Range of Ions in Matter (SRIM) and ATHENA. The two packages use Monte Carlo collision simulation (SRIM, ATHENA) and empirically verified analytical models (ATHENA).

SRIM is a one-dimensional implant modeling program that simulates screened Coulomb collisions between energetic ions and target materials [53]. It accounts

for ion recoils, surface sputtering, crystalline damage, and cascade phenomena. Given a beam angle, target material implant species and beam energy, it generates dopant distribution as a function of depth as well as straggling, skewness and kurtosis (Figure 3.1).

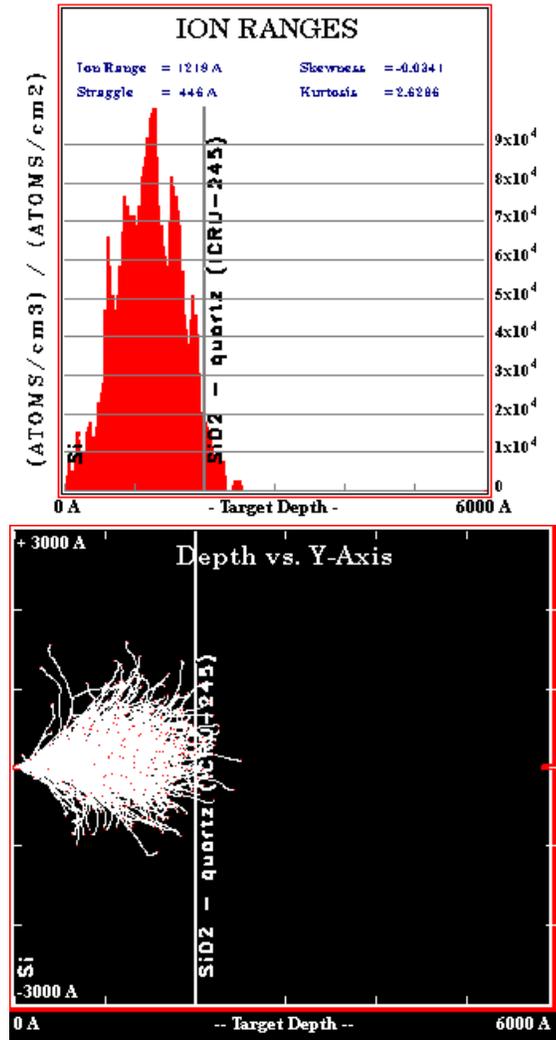


Figure 3.1- Output from SRIM simulation

SRIM is free software and has been used in the semiconductor processing industry for many years. It is well suited to simpler implant processes as well as to verify individual steps in multiple-implant processing. Since the proposed BJT device utilizes multiple implants at different angles as well as deposition and etch processing in between implants, a two-dimensional processing simulation environment is required.

ATHENA from Silvaco is chosen for two-dimensional implant and processing simulation [54]. ATHENA is capable of both Monte Carlo collision simulation (as in SRIM) as well as empirically verified analytical simulation. ATHENA is also capable of simulating material deposition, etch processes (both isotropic and anisotropic) and annealing. Using ATHENA we were able to vary process parameters to ensure all processing steps yielded the desired device configuration.

The analytical model used by ATHENA is the dual Pearson distribution. A Gaussian distribution has a mean (first cumulant) and standard deviation (second cumulant) which are both roughly proportional to ion beam energy. A Pearson distribution also has a skewness (third cumulant) and kurtosis (fourth cumulant). In amorphous materials, a single Pearson distribution accounts for ion backscattering and is a better approximation than a Gaussian.

For crystalline materials, there can also be channeling effects if the ion is travelling along a crystalline plane. In order to account for this, a second Pearson distribution is

added to the first. The dual Pearson model has been compared to secondary ion mass spectroscopy data of ion implanted samples and has shown good agreement with a χ^2 of $\approx 1.5 \cdot 10^{-3}$ [55].

ATHENA simulations are carried out on all processing steps, and the resulting NPN configuration is confirmed. Post-implant annealing is also simulated to verify that diffusion during the annealing process is not sufficient to affect device geometry.

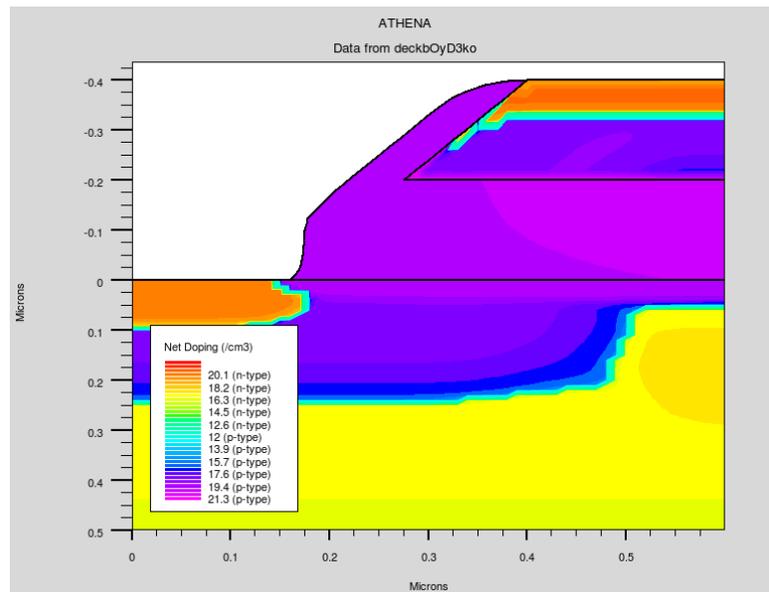


Figure 3.2 - ATHENA two-dimensional doping profile

3.3 Fabrication

Fabrication of on-chip ultrathin BJT samples is carried out using standard CMOS processing techniques. In particular, lithography is limited to photolithography which has a resolution of approximately 600 nm using the stepper at LPS. In order to create

an intrinsic base feature that is smaller than the resolution of photolithography, a self-aligned polysilicon (poly-Si) sidewall spacer technique is employed [51].

Fabrication begins with a silicon-on-insulator wafer from SOITEC. The wafer has a 200nm thick Si device layer and a 400 nm buried oxide layer on top of a Si handle wafer. The initial p type dopant concentration was $7.5 \times 10^{14}/\text{cm}^3$.

The first implant is performed to create the collector region of the device. This region is relatively lightly doped in order to prevent junction breakdown as well as to allow for p-type compensation when the base region is formed. A shallow phosphorous implant is performed at an angle of 7° , an energy of 50 keV and a fluence of 1.6×10^{11} ions/ cm^2 . A deep phosphorous implant is also performed at an angle of 7° , an energy of 140 keV and a fluence of 4×10^{12} . Implant modeling confirms that the resulting n-SOI layer has a dopant concentration ranging from $8 \times 10^{15}/\text{cm}^3$ ($0.6 \Omega \cdot \text{cm}$) at the surface to $1.6 \times 10^{17}/\text{cm}^3$ ($0.6 \Omega \cdot \text{cm}$) at the bottom (Figure 3.3).



Figure 3.3 – N-type SOI

200 nm of poly-Si is then deposited on top of the n-SOI layer. A Tystar low pressure chemical vapor deposition (LPCVD) system is used in the FabLab at the Maryland

Nanocenter. This poly-Si layer forms the extrinsic base contact region and therefore must be heavily doped in order to achieve Ohmic tunneling contact. In order to effectively dope the poly-Si layer but not the underlying n-SOI, BF₂ was chosen as the implant species. The use of a heavier ion creates a thin damaged amorphous layer at the surface and prevents channeling. BF₂ is implanted at an angle of 7°, an energy of 35 keV and a fluence of 8*10¹⁵. Implant modeling as well as inline four point probe resistivity measurements confirm dopant concentration (Figure 3.4).

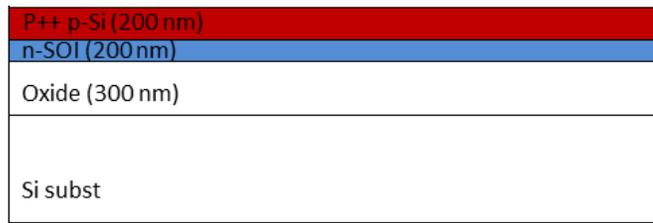


Figure 3.4 - Poly-Si extrinsic base layer

In order to mask the p++ type poly-Si extrinsic base layer from future implants, 300 nm of SiO₂ is deposited using an Oxford PECVD system at LPS (Figure 3.5).

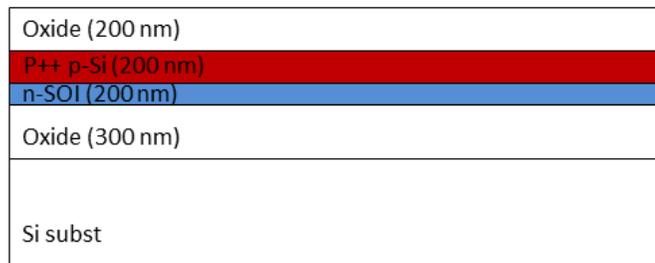


Figure 3.5 – Protective SiO₂ layer

The extrinsic base region is then defined photolithographically using positive photoresist. The resist is used as a mask to anisotropically etch the protective SiO₂ and p⁺⁺ poly-Si to form a step. The etch was performed in a PlasmaTherm 790 reactive ion etch tool at LPS (Figure 3.6). Since there is no selective etch for poly-Si that will not etch crystalline Si, the second etch must be carefully timed to go all the way through the poly-Si but not too far into the underlying SOI. Etch rates and times are determined using a cross-sectional sample in a scanning electron microscope (SEM). The process is shown to give a vertical step edge and that the necessary precision in etch depth is repeatable.

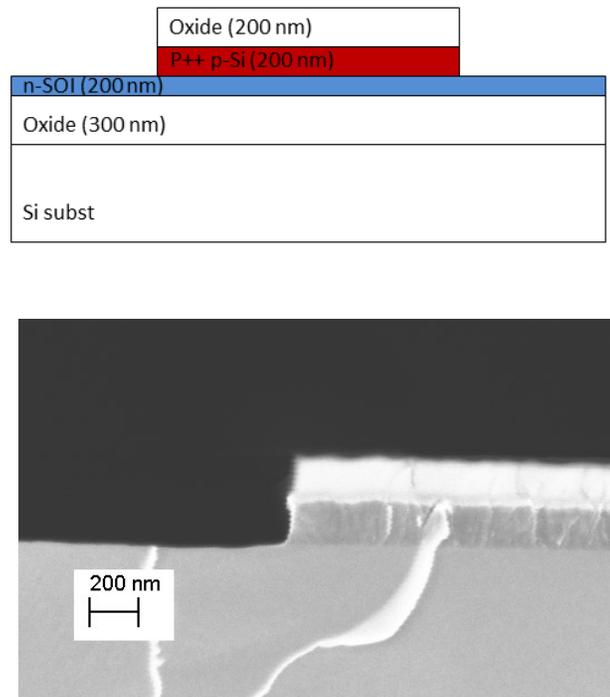


Figure 3.6 – Vertical step etch, diagram and SEM image

Next, the intrinsic base region is defined. Since this region needs to be narrower than the resolution of our lithography method, an angled implant is performed and a self-

aligned poly-Si sidewall spacer is formed. This technique takes advantage of the conformal nature of LPCVD films and the anisotropic, directional nature of reactive ion etching (RIE).

Three boron implants are performed at an angle of 45° which compensate for the n-type doping in the SOI layer and create a p type region that extends slightly underneath the p++ extrinsic base region. The first implant is performed at 5.6 keV at a fluence of 1.2×10^{13} ions/cm² the second at 15 keV and a fluence of 2×10^{13} ions/cm² and the third at 35 keV with a fluence of 7.2×10^{13} ions/cm² (Figure 3.7).

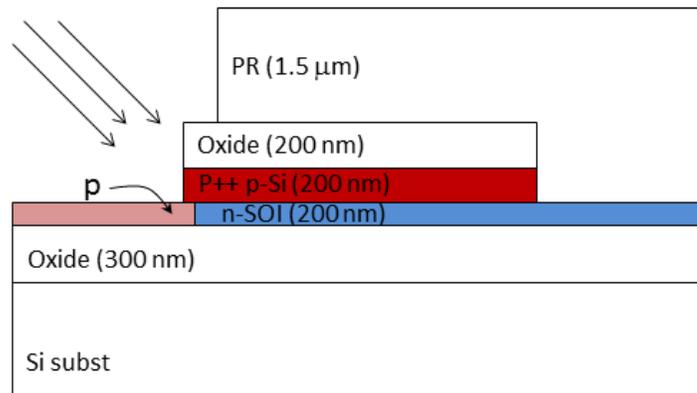


Figure 3.7 – Angled ion implant

Poly-Si is then deposited using the FabLab's LPCVD system. Because deposition occurs at very low pressure and flow rate it is highly conformal. The thickness of the film on the side of the step is nearly the same as that on the top. Conformal deposition is confirmed using cross-sectional SEM (Figure 3.8).

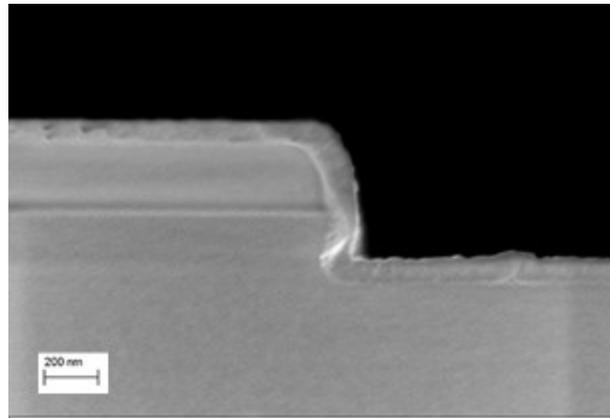
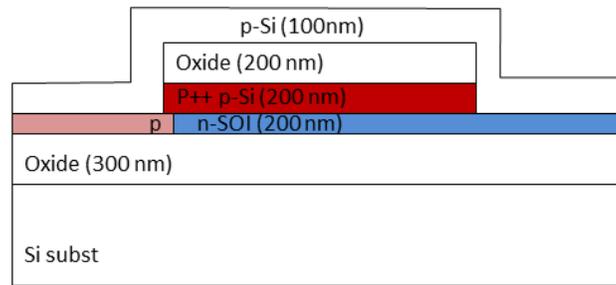


Figure 3.8 – Conformal poly-Si deposition

The poly-Si is then etched using the PlasmaTherm 790 RIE tool. At low pressures, this tool etches anisotropically in the vertical direction. By etching at 1 milli Torr, poly-Si is removed from the top and bottom of the step and a spacer is left on the side (Figure 3.9). Spacer formation is confirmed using cross-sectional SEM.

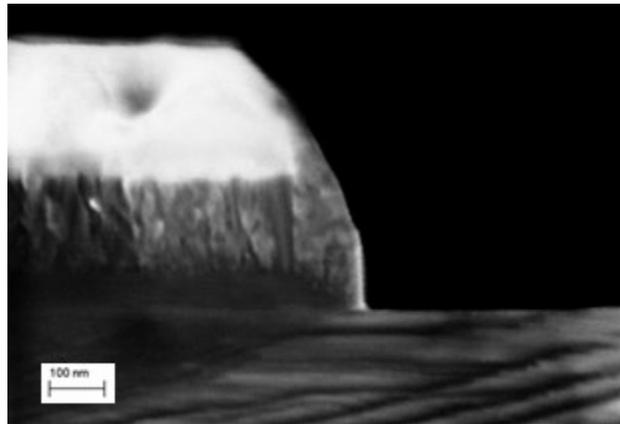
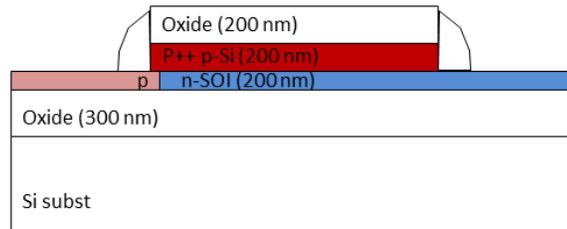


Figure 3.9 – Poly-Si sidewall spacer

This spacer serves as a mask for the final vertical n++ implant, and defines the outer edge of the intrinsic base region. Phosphorous is implanted at an angle of 7° at an energy of 75 keV and a fluence of $4 \cdot 10^{14}$ ions/cm².

A post-implant anneal is performed in order to activate dopants and repair damage to the crystalline structure caused during ion implantation. Simulations show that diffusion due to annealing for one minute at 950° C did not significantly change dopant distribution (Figures 3.10 & 3.11). After annealing, dopant activation is confirmed using an inline four point probe. Resistivity values of $0.04 \Omega \cdot \text{cm}$ for the n++ emitter/collector region and $0.06 \Omega \cdot \text{cm}$ for the p++ extrinsic base region are

measured. These values are consistent with the level of bulk doping predicted by ATHENA and SRIM simulations, about 10^{18} ions/cm³.

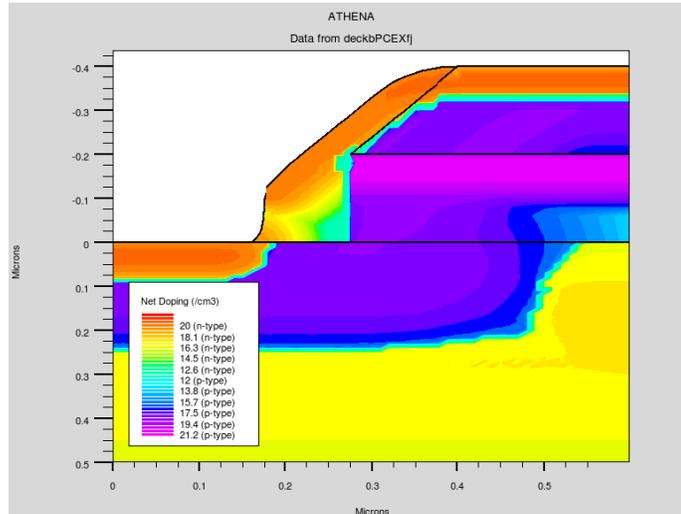


Figure 3.10- Simulated dopant distribution before annealing

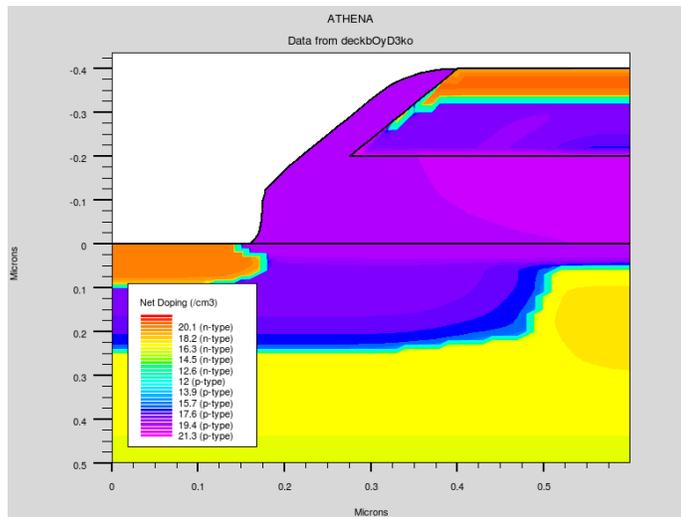


Figure 3.11 – Simulated dopant distribution after annealing

Individual devices are then isolated by masking the device outline with positive photoresist and etching through the remaining Si down to the buried oxide. Etching is performed using the PlasmaTherm 790 at LPS. A diagram of the device as viewed

from the top is shown in Figure 12 with the n++ collector at the top, the p++ base in the middle and the n++ emitter at the bottom.

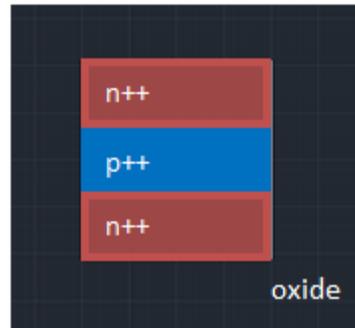


Figure 3.12 – Top view of Si device

The final step before metallization is to prevent the n-type emitter layer underneath the p++ base from contacting the base electrode, which would short the device. The base electrode extends over the base contact region from the left side of figure 3.12. The metal then must cross onto the p++ base region and in doing so will go over a step whose lower layer must be isolated from the base electrode (Figure 3.13).

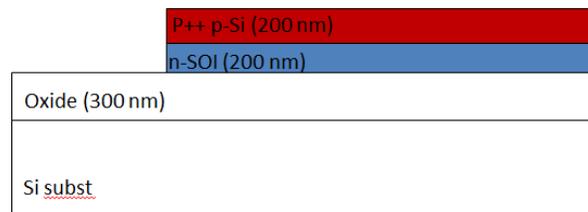


Figure 3.13 – Cross-section of step

In order to isolate the lower n-type layer, a Si_3N_4 patch is deposited and patterned using a nitride lift-off process. A lift-off process is chosen because an etch process

that selectively etches Si_3N_4 but not SiO_2 was not available. Photoresist is spin-coated onto the sample and a window is defined photolithographically to cover the step edge (Figure 3.14).

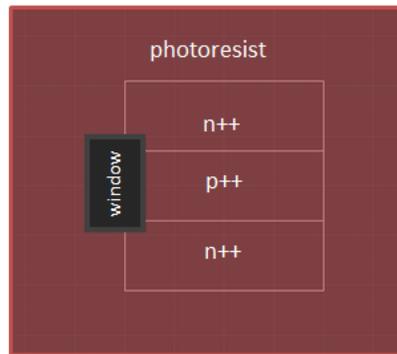


Figure 3.14 – Nitride patch window

100 nm of Si_3N_4 is then deposited using the Oxford PECVD at LPS and the sample is submerged in N-Methyl-2-pyrrolidone (NMP) overnight, lifting off all but the nitride deposited in the photoresist window. A cross-section of the resulting step is shown in Figure 3.15.

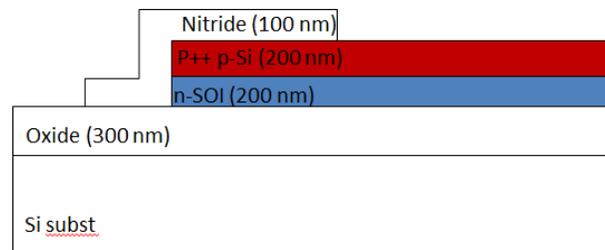


Figure 3.15 – Cross-section of step with protective nitride

With the protective nitride in place, pre-metallization processing is complete. In this section we described the design and fabrication BJT's on SOI for high frequency applications. In order to satisfy our design criteria, an ultrathin base region is created using a previously reported poly-Si sidewall spacer technique combined with angled ion implantation. This technique enables the definition of device features that are smaller than the resolution of our photolithography process. Metals deposition and limitations due to localized Joule heating will be discussed in the next section.

3.4 Metallization and Localized Heating

Complications associated with metallization and localized heating have been a significant limiting factor for BJT device performance in this work. The electrode configuration, chosen for AC impedance reasons, contains narrow ($\sim 1.5 \mu\text{m}$) contacts. When placed under quiescent DC bias these contacts are subjected to extremely high current densities which cause localized Joule heating. This heating causes rapid degradation in device performance due to damaged metal contacts and dopant diffusion in the Si device.

Initial attempts at metallization are carried out using standard electron-beam deposition and lift-off. The tapered CPW configuration discussed in chapter 2 is used because it was shown to be suitably impedance matched to a 50Ω measurement network. Test electrodes are deposited onto a conductive (n++) Si pad in order to

study the effects of high current density. The metal electrode pattern is shown in Figure 3.16.

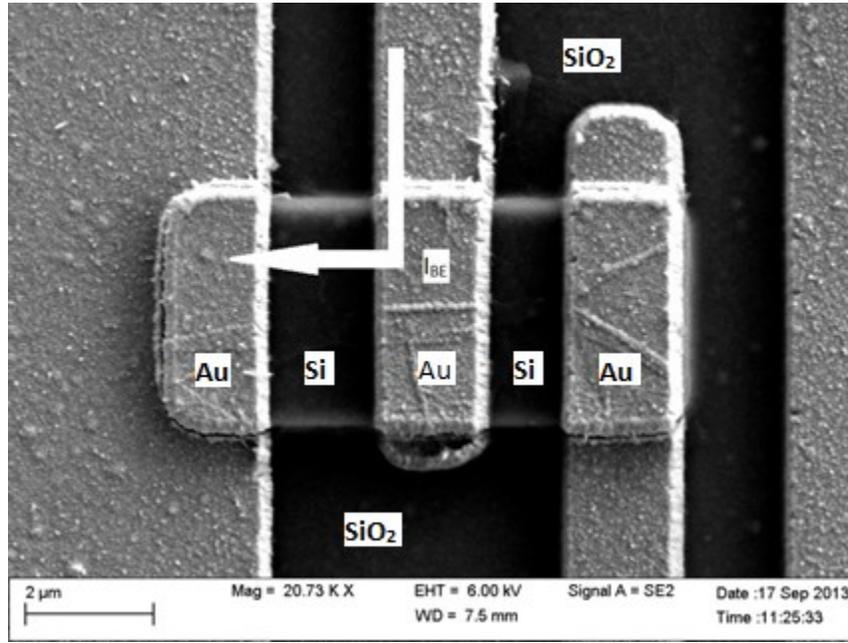


Figure 3.16 – Patterned metal electrodes

The width of these CPW electrodes at their narrowest point is approximately 1.7 μm , with film thicknesses up to 800 nm. For these dimensions, current flows through a cross-sectional area of $1.2 \cdot 10^{-8} \text{ cm}^2$. The observation of important DC and AC effects requires current values up to 3 mA, which corresponds to a current density of 250,000 A/cm^2 . Devices operating under these conditions show performance degradation after measurement times of less than one minute due to the effects of Joule heating. Three different modes of device failure are observed, corresponding to the three different metals chosen as electrode materials.

The first metal structure used was Au with a thin Ti layer to promote substrate adhesion. This is a common configuration since Au has both a high conductivity and high resistance to corrosion. The coplanar waveguide design is patterned using photolithography, and the metals are deposited using a CHA electron beam evaporator at LPS. Lift-off is performed in NMP overnight.

The failure mode observed in Ti/Au is that of a short circuit. The voltage sweep in Figure 3.17 starts at -10 V and sweeps to +10 V. Shorting behavior is observed around $V_{CE} = 9.5$ V.

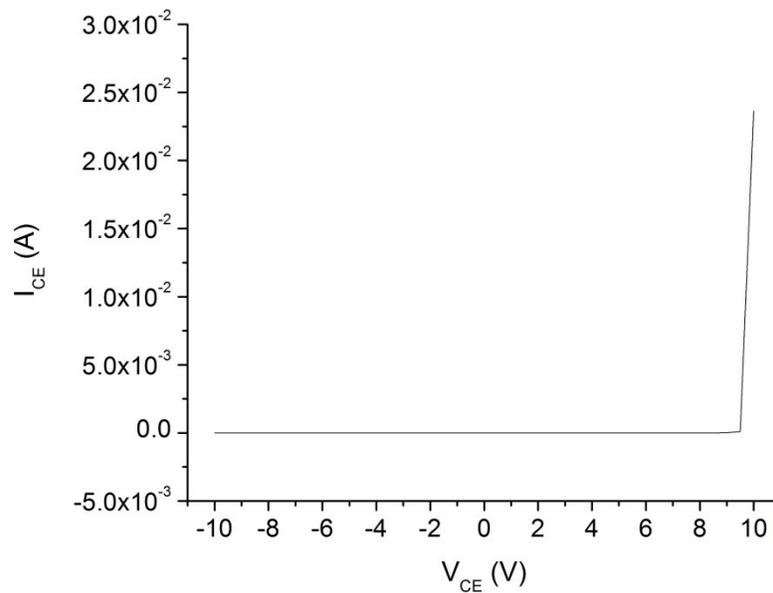


Figure 3.17 – Ti/Au device failure

SEM and Electrical Dispersive X-Ray (EDX) characterization (Fig 18-22) are performed on the Ti/Au devices before and after electrode failure. Examination of the micrographs shows inter-diffusion of Au and Si to be the cause of device shorting.

Figures 3.18 and 3.19 show EDX overlays of Au and Si signals before shorting behavior is observed. In these images, it can be seen that the gold film is completely localized within the electrode pattern and there is very low Si signal in the electrode pattern area.

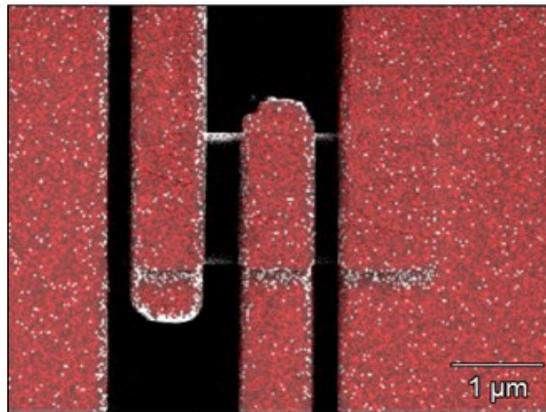


Figure 3.18 – EDX Au overlay before failure

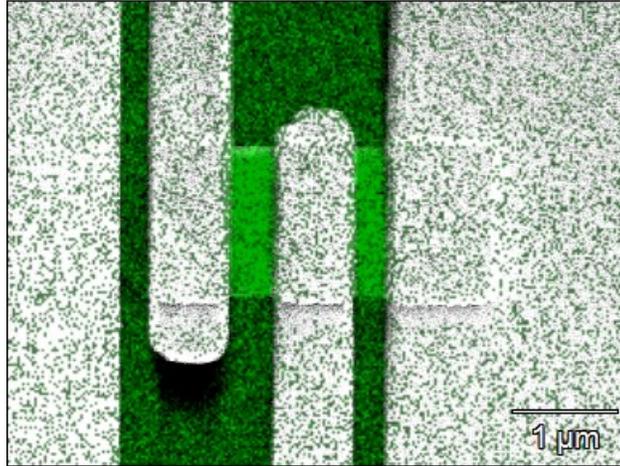


Figure 3.19 – EDX Si overlay before failure

Figures 3.20 and 3.21 show the same device after electrode failure. Au signal can clearly be seen between the original electrode traces. Si signal is also present in the region of the metal film.

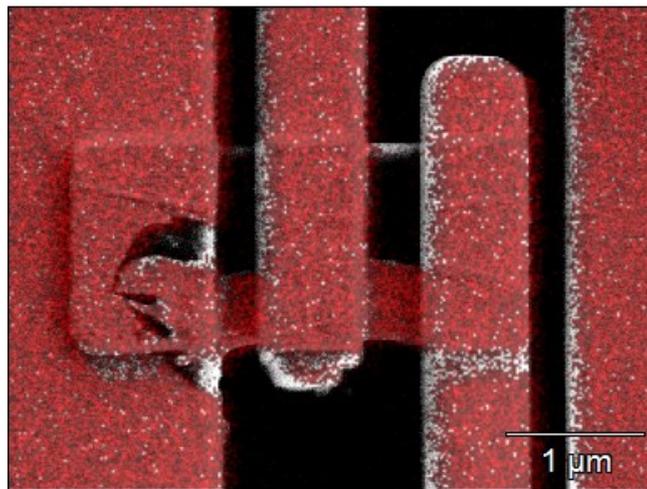


Figure 3.20 – EDX Au overlay after failure

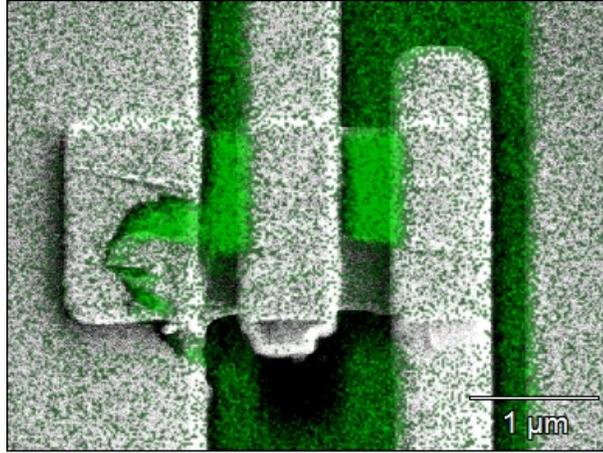


Figure 3.21 – EDX Si overlay after failure

Figure 3.22 shows a tilted SEM image after electrode failure. It can be seen that even after failure, the electrodes have retained their shape. There is still a clear gap between the sections of raised Au film. The Au rich region between the raised sections is roughly level with the Si. The Si rich region in the electrode pattern is level with the raised Au film. This indicates that the Si rich area is not simply exposed Si from damage or removal of the Au film. The fact that the Au film is not deformed and that Si is observed at the surface of the raised film leads us to conclude that diffusion, rather than melting or electromigration, is the cause of failure in Ti/Au electrodes.

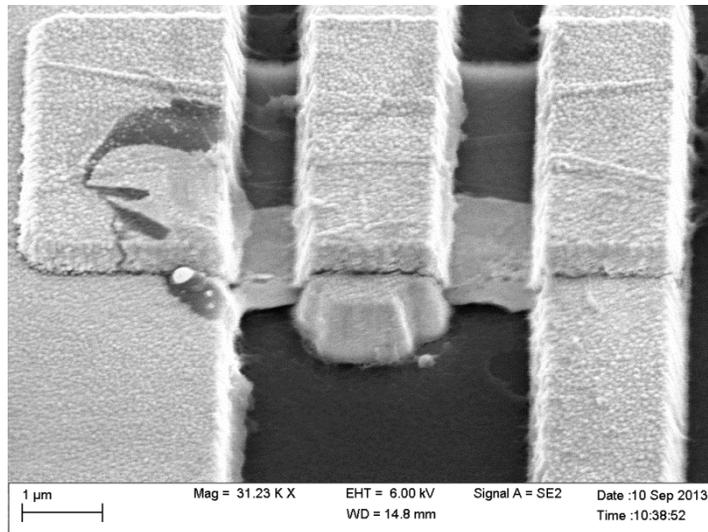


Figure 3.22 – Tilted SEM image of electrodes after failure

It is known that Au and Si form a eutectic system (Figure 3.23). Previous work has examined diffusion at Si/Au interfaces near the eutectic temperature [56]. Simulations have shown that below the eutectic temperature, a zone of enhanced diffusion as wide as 10 μm forms at the interface. This enhanced diffusion is consistent with the images obtained using EDX and SEM. We conclude that Joule heating in the electrodes raise the temperature near the eutectic temperature (350 $^{\circ}\text{C}$), causing rapid diffusion between the Au and Si and shorting the device. This diffusion either passed through the thin Ti layer, or occurred at cracks or discontinuities in the Ti film.

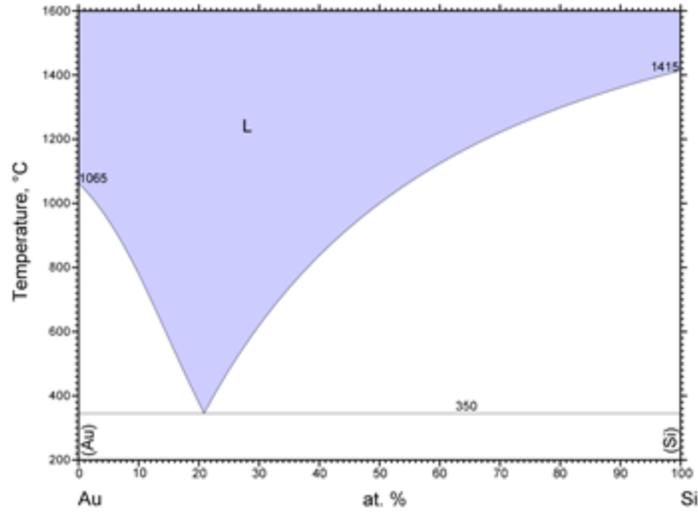


Figure 3.23 – Au-Si binary phase diagram [57]

In order to mitigate the effects of this diffusion, Cu was first chosen as a replacement metal for Au. The Cu-Si binary system differs from the Au-Si system in that it has no liquid phase below 803 C (Figure 3.24). The Cu electrodes therefore should not be susceptible to enhanced diffusion at the temperatures of electrode failure in Au films.

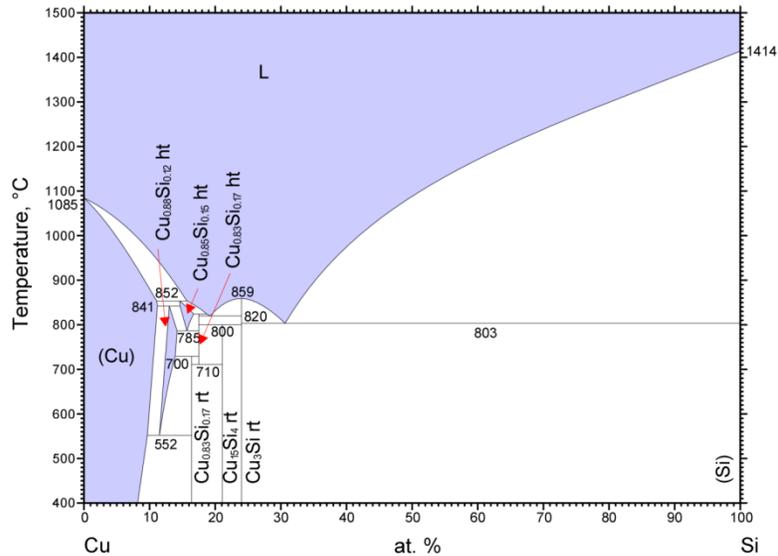


Figure 3.24 – Cu-Si binary phase diagram [58]

Ti/Cu electrodes are fabricated using the same deposition and lift-off technique as Ti/Au. Under electrical testing, Ti/Cu electrodes also fail, but their behavior is different than that of the Au films. At high current densities, Ti/Cu electrodes exhibit irreversible open circuit behavior (Figure 3.25). Again, the voltage sweep is going from negative to positive, and the device fails around $V_{CE} = -4$ V.

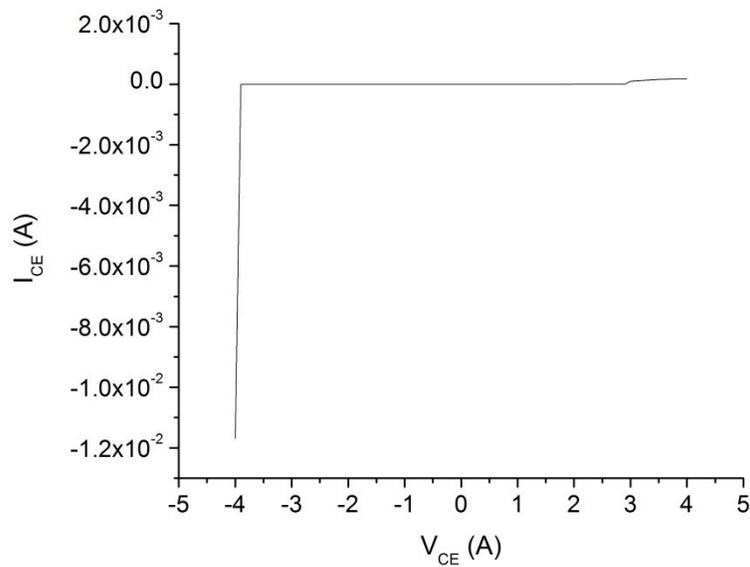


Figure 3.25 – Ti/Cu device failure

This open circuit failure mechanism is consistent with what one would expect for electrode melting or electromigration. SEM imaging was performed on Ti/Cu electrode devices after failure (Figure 3.26). The damaged Cu is observed to be in the shape of droplets that have dewetted from the SOI. This is consistent with previous studies that have studied melting behavior of copper films [59][60].

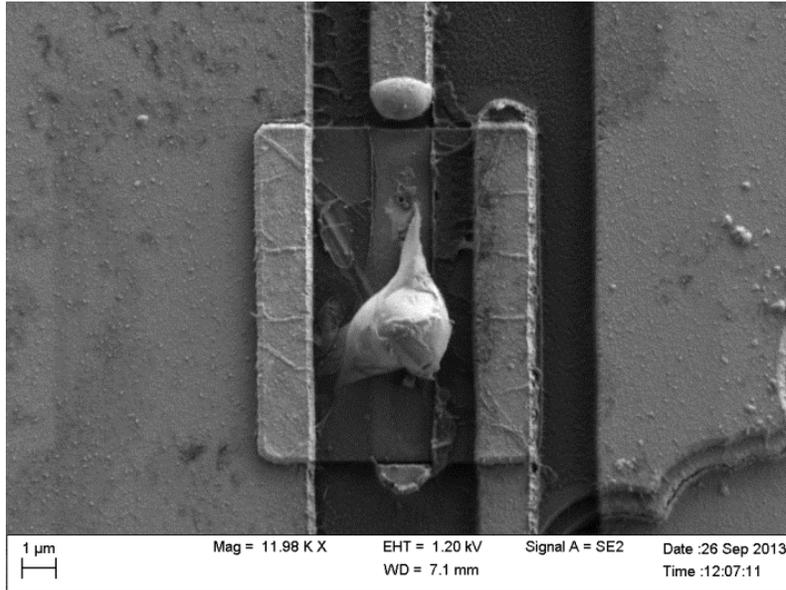


Figure 3.26 – SEM image of melted Ti/Cu electrode

By contrast, electromigration typically manifests as whisker formations (Figure 3.27) or voids (Figure 3.28). Neither of these is consistent with what is observed for copper electrode failure.

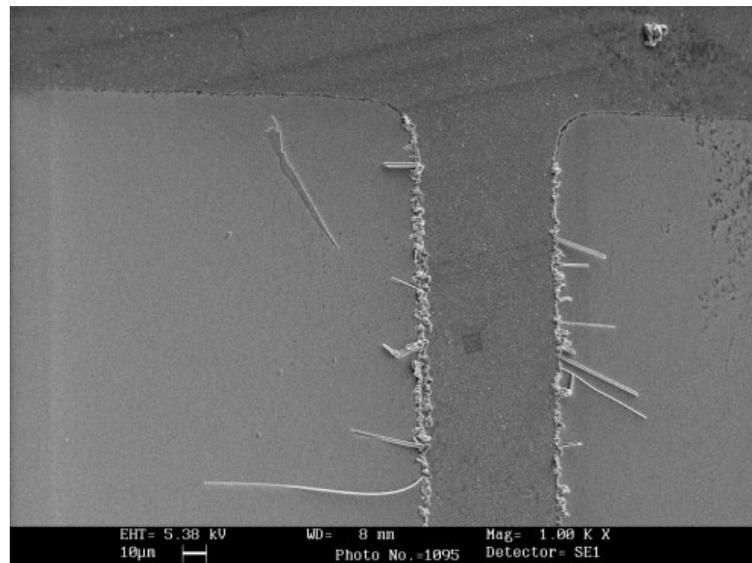


Figure 3.27 – Whisker electromigration pattern [61]

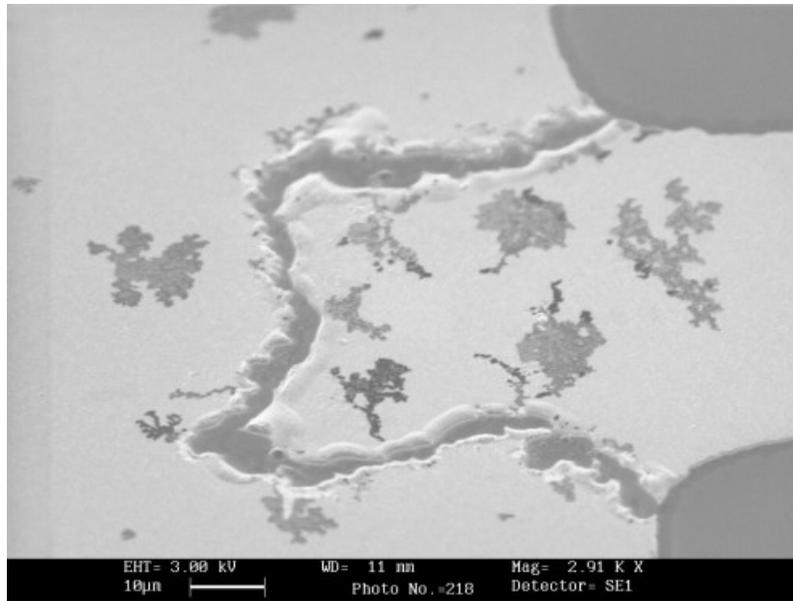


Figure 3.28 – Voids caused by electromigration [61]

Based on SEM images, we conclude that electrode failure, is in fact, due to melting of the Cu metal. This conclusion, along with the fact that the Cu-Si system has no liquid phase below 803 °C indicates that devices under test are being exposed to very high temperatures.

Because a metal was needed that could withstand temperatures above 800 °C, W was chosen as an ultimate replacement metal. W has a melting point of 3,422 °C, which is more than three times that of Au (1,064 °C) and Cu (1,085 °C). W is also resistant to etching in HF, which makes it compatible with membrane release and transfer.

Due to its high melting point, W is not typically deposited in e-beam evaporation systems. W was deposited in the sputtering system in the FabLab at Maryland

Nanocenter. Since the sputtering unit is not compatible with photoresist, a different patterning method is needed.

For definition of W electrodes, conformal W films are first sputtered over the entire sample. Photoresist is then patterned to define the electrode area and is used as a mask for the etch process.

There are two common methods for etching W: dry etching exhibits high anisotropy and poor selectivity, and wet etching gives high selectivity but poor anisotropy. Our electrode design, however, requires both anisotropy and selectivity. Anisotropy is necessary because the width of electrode features is comparable to the thickness of the W film. An isotropic etch would cause undercutting, considerably narrowing electrode features. Selectivity is also necessary, because excessive etching of the underlying Si could damage the device itself.

A dry etch process was developed using the PlasmaTherm 790 at LPS. Etch tests show a highly anisotropic vertical etch profile. Once the W film is etched, however, the underlying Si is etched nearly twice as fast as W. The consequence of this poor selectivity is that once the W layer is etched completely, damage to the underlying Si device is likely.

A highly selective wet etch was also developed using W etchant solution from Sigma Aldrich. This solution has a published selectivity of W to Si of greater than 20:1. In

etch tests, no measurable etching of Si was observed. This etch process, however, is isotropic and shows undercut of the W features after etching through the W film (Figures 3.29, 3.30). Figure 3.29 shows considerable undercutting compared to the width of the resist and Figure 3.30 shows the resulting narrow electrodes (~200nm wide) after resist removal.

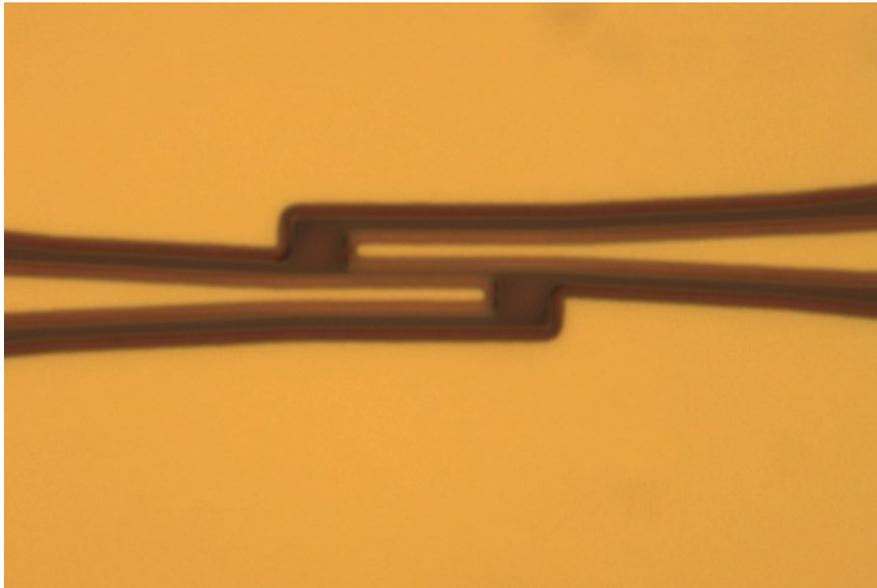


Figure 3.29 – Fully etched W film before resist removal

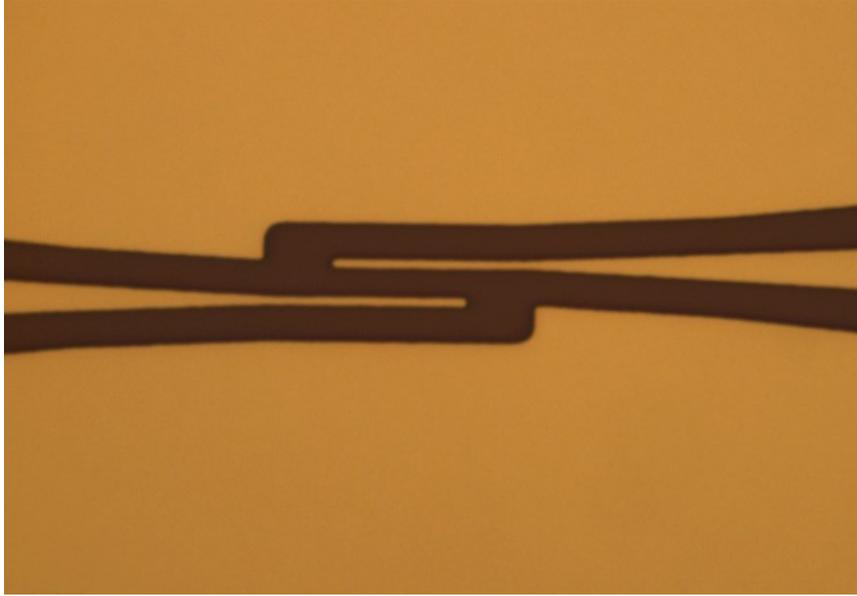


Figure 3.30 – Etched W electrodes using isotropic W etch

In order to avoid this shrinkage of features, a two-step process is used. The dry plasma etch is used to etch through roughly 90 percent of the W film, leaving a small amount left in areas not protected by photoresist. The wet etch is then used to etch the remaining W while preserving the underlying Si device and causing minimal undercutting of the resist.

Sputtered W electrodes do not exhibit the shorting, diffusion behavior of Ti/Au electrodes or the open circuit, melting behavior of Ti/Cu. Device performance does, however, still degrade rapidly under DC biasing conditions. Within minutes of device operation, DC gain falls to a value of 1, signifying that the only current reaching the emitter is from the base current and none is being contributed by electrons crossing the base region.

A likely explanation for this degradation is the diffusion of dopant atoms due to heating of the Si. Since Cu melts at 1085 °C, the device is likely to be operating at temperatures at or above this value. An ATHENA simulation was performed to show the effects on dopant distribution of annealing at 1100 °C. After only 45 seconds, dopants from the p⁺⁺ base contact region diffuse through the entire width of the 200nm collector (Figure 3.31).

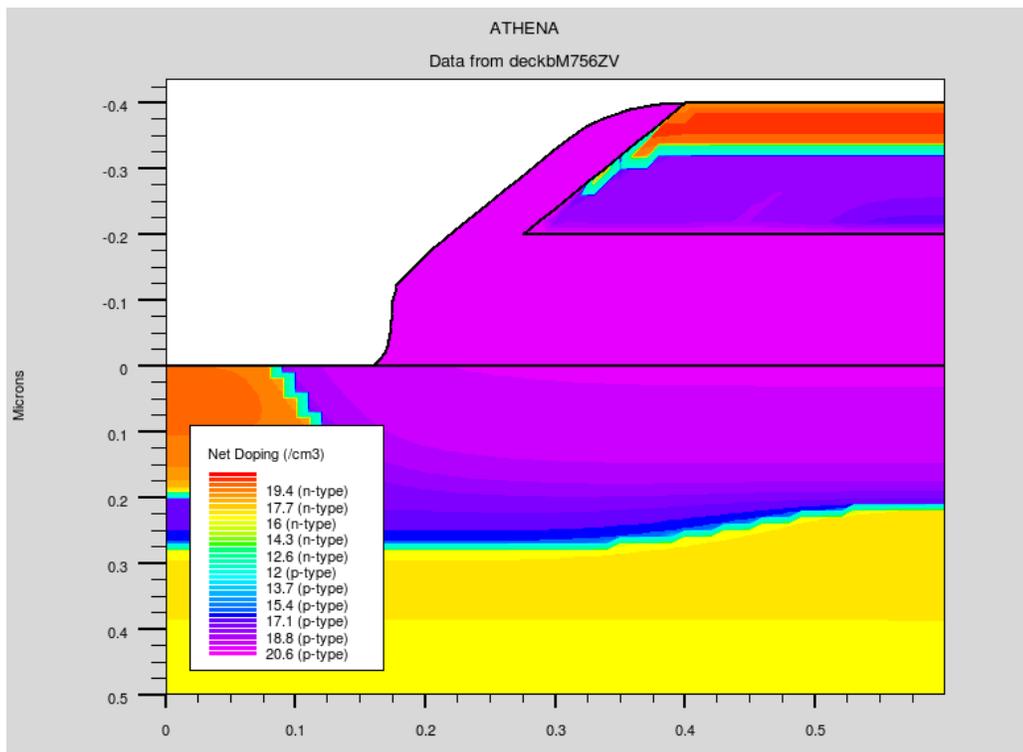


Figure 3.31 – Effect of annealing at 1100°C for 45 seconds

This diffusion effectively widens the base region to the width of the base contact region, 1.7 μm. This means that electrons diffusing across have much farther to go before reaching the base-collector depletion region. The level of doping in the base

region is also increased, which increases the likelihood of recombination. The net effect is that few if any electrons are able to diffuse from the emitter to the collector. In the end, W proved to be the best electrode material for high temperature applications, but the underlying problem is that of Joule heating of the Si itself.

In this section, electrode failure due to Joule heating was observed at DC conditions. Narrow electrode features, chosen for their microwave frequency properties, create a critical problem for device operation under quiescent DC bias conditions. Electrode metal failure was observed using SEM and EDX, and three material configurations were attempted. W is found to perform sufficiently well at device operating conditions, but device performance is still degraded due to dopant diffusion. Ultimately, Joule heating is the limiting factor for device operation.

Chapter 4: Electrical Characterization

4.1 Direct Current Characterization

The primary motivation for DC characterization in this study is to obtain figures of merit for the BJT devices and to obtain proper biasing conditions for AC signal gain. Common emitter forward current gain β_F and transconductance g_m are observed in two different regimes of operation. Based on these measurements, quiescent conditions are obtained for microwave frequency measurements.

Direct current measurements are performed using an Alessi REL-4300 probe station. Voltages and currents are sourced using Keithley 2400 Source meters. Measurements are automated using the graphical programming language Labview.

The base-emitter junction is of critical importance to DC and AC device operation. The biasing of the base-emitter junction determines the base current, which determines the much larger collector current. In order to select the proper bias for a given base current, we use the I-V characteristics of the base-emitter junction, shown in Figure 4.1.

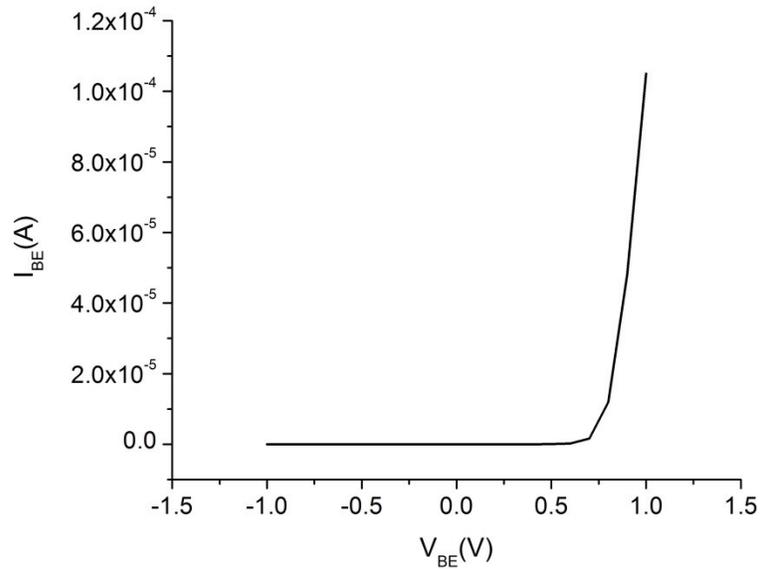


Figure 4.1 – I-V characteristics of the base-emitter junction

This behavior is typical of silicon PN junctions. The built-in potential for Si is approximately 0.7 V. At forward bias above the built-in potential, the diode allows forward current flow. The reverse saturation current was measured to be approximately 100 nA.

Preliminary measurements of the DC I-V characteristics examine base and collector currents up to 3 mA. These measurements yield maximum DC gain values around $\beta_F = 3$, and often lower. This is not particularly high for Si transistors which can exhibit current gains up to 1000 or more. As discussed in the previous section, these current values also lead to very high current density, resulting in device damage within a few minutes of operation. Early DC I-V data is shown in Figure 4.2.

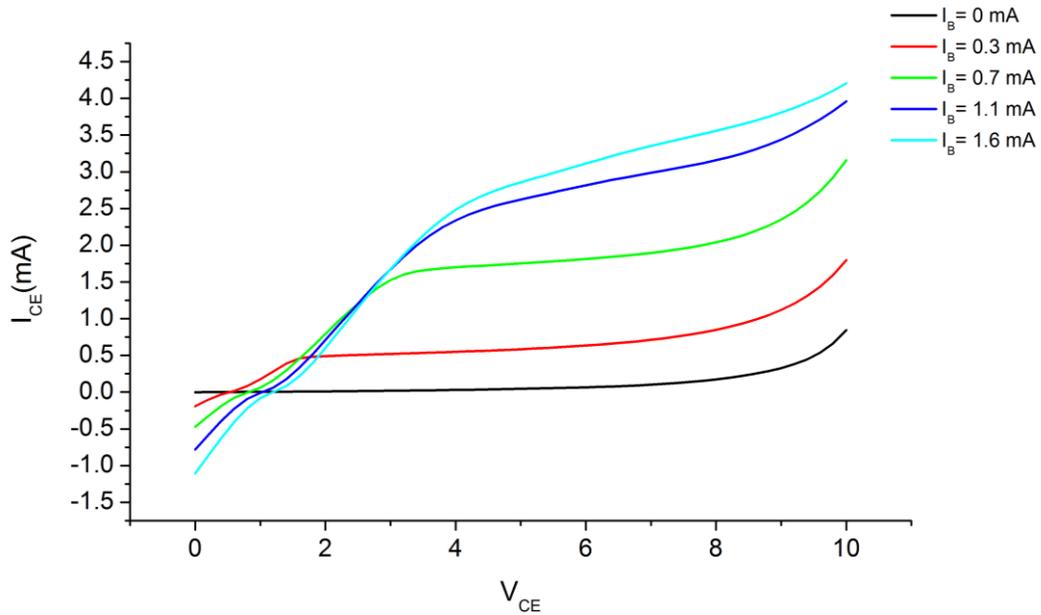


Figure 4.2 – Preliminary I-V data

The transconductance of the BJT is defined as

$$g_m = \frac{I_{CE}}{V_T}$$

where V_T is the thermal voltage, about 26 mV at room temperature. For the above device at the operating conditions where β_F is 2.4, g_m is 59 mS. This value of g_m is higher than most commercially available FETs but lower than many BJTs. This value is typical of the highest g_m observed in the BJTs fabricated in this study.

Subsequent DC measurements probe the regime of very small base current (0-20 nA). It was found that at low base currents, very high current gains are observed. A reasonable explanation for this would be that high base currents inject so many holes into the narrow base region that most of the minority carrier electrons recombine

rather than diffuse across. These results are also more reproducible, due to lower current density and less Joule heating.

A DC I-V curve for low base current is shown in Figure 4.3.

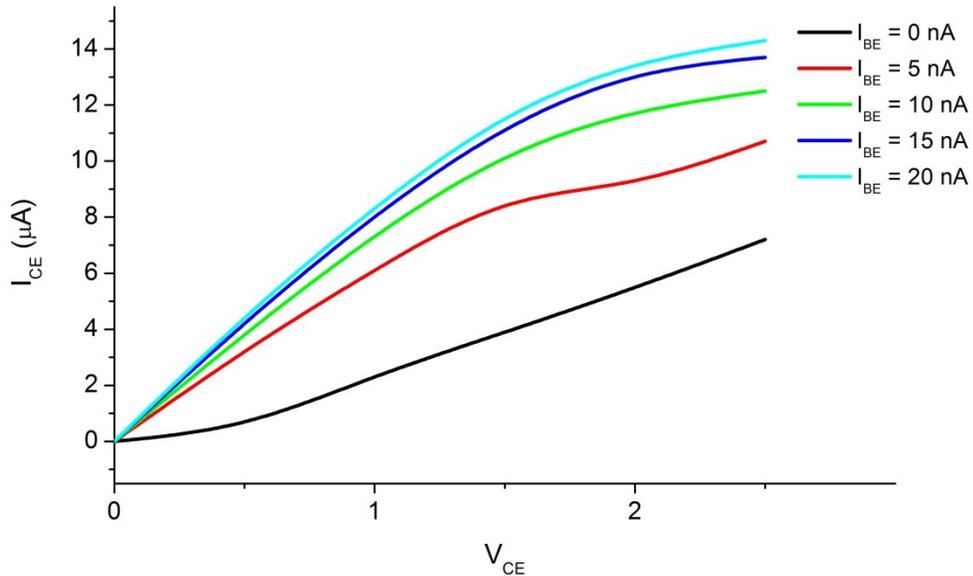


Figure 4.3 – Low base current I-V characteristics

In this biasing regime, we see a finite I_{CE} even at $I_{BE}=0$. This current is roughly ohmic with respect to I_{CE} and is likely due to thermally excited carriers crossing the reverse biased base-collector junction. Because I_{CE} is the sum of this current and the current that exists as a result of I_{BE} , this ohmic behavior needs to be taken into account when discussing current gain.

The current gain of a BJT is defined as

$$\beta_F = \frac{I_{CE}}{I_{BE}}$$

Using this definition, current gain β_F is plotted in Figure 4.4.

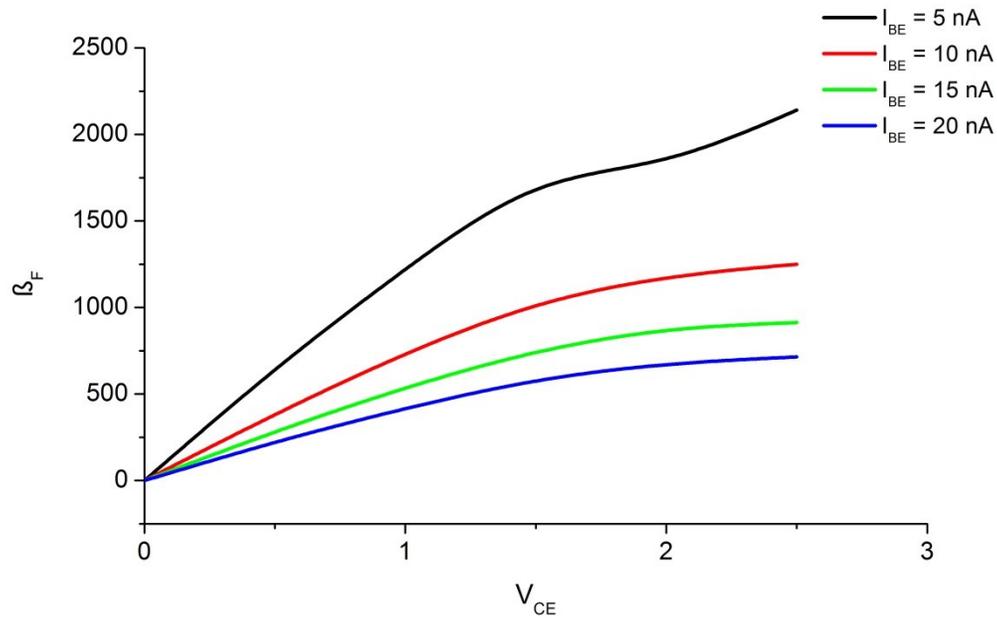


Figure 4.4 - β_F including ohmic current

These values for β_F , however, include the ohmic current observed in Figure 4.3. This parallel current path adds to the value of I_{CE} and inflates the measured value of $\frac{I_{CE}}{I_{BE}}$. A more accurate figure for β_F can be obtained by subtracting out the effects of the ohmic current. The expression for β_F then becomes

$$\beta_F = \frac{I_{CE} - I_{CE0}}{I_{BE}}$$

where I_{CE0} is I_{CE} at $I_{BE} = 0$. Values for β_F obtained this way are plotted in Figure 4.5

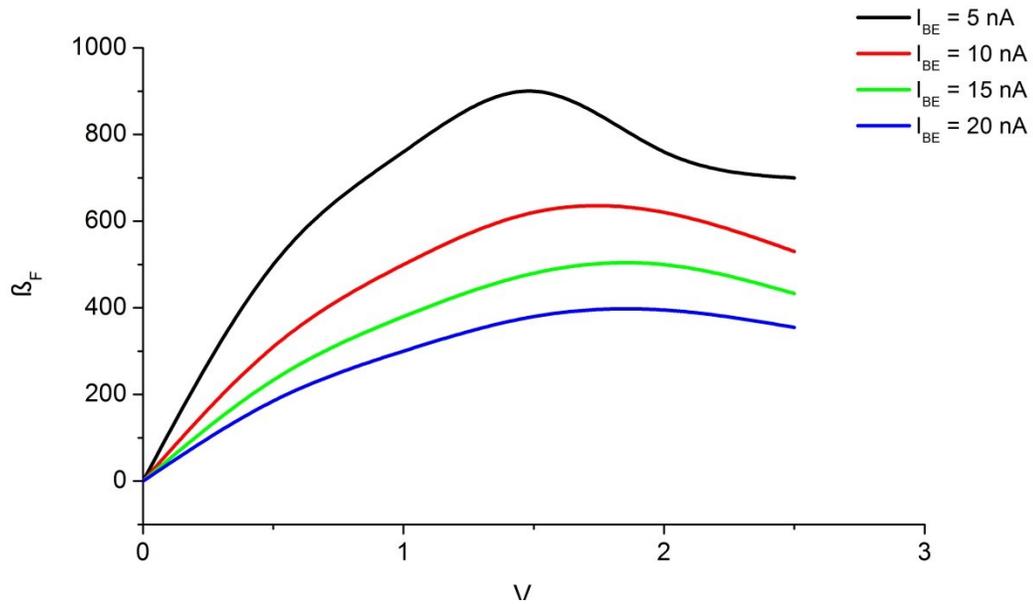


Figure 4.5 – β_F with ohmic current subtracted

Even with ohmic current subtracted, we see that β_F in this regime is quite high. By comparison, commercial Si BJTs typically have a β_F value of 100-200. This behavior, however, is transient. Dopant diffusion caused by Joule heating quickly and irreversibly damages the device and β_F falls to values of less than two. Figure 4.6 shows the same device as in Figure 4.5, after a DC measurement time of approximately two minutes. This effect is attributable to boron diffusion from the p-type external base contact region into the n-type collector, effectively widening the base region and reducing the likelihood of electrons diffusing across.

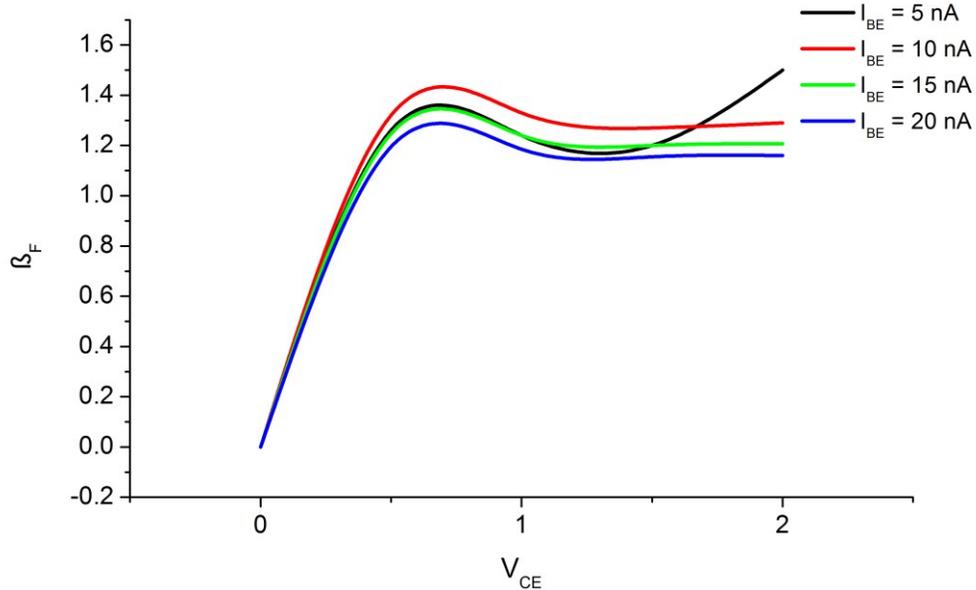


Figure 4.6 - β_F after two minutes under test

At low base currents, there are comparatively few holes being injected into the base region. This minimizes recombination and maximizes the number of electrons that make it across to the collector. Low base currents and an ultra-narrow base region have the effect of very high current gain. Because I_{CE} is on the order of μA , g_m as defined above is quite small in this region, less than 0.5 mS.

Two distinct regimes of BJT operation are observed. At high base currents, low values of β_F are observed but the same regime have relatively high g_m . At low base currents, evidence of very high β_F can be inferred from the data, but low values of I_{CE} correspond to low g_m . Both biasing regimes were subsequently tested at microwave frequencies.

4.2 Microwave Frequency Characterization

Microwave frequency measurements are performed on BJTs under three biasing conditions. “ON - g_m ” measurements are taken with the device biased in the regime of high base current and high transconductance, “ON- β_F ” measurements are taken under low base current and high current gain conditions, and “OFF” measurements are taken with the device unbiased. The three are then compared to determine the effect of biasing on microwave BJT performance.

S-parameter measurements are obtained using an Agilent E5071C ENA series network analyzer. DC biasing is performed using two Keithley 2400 digital source meters connected to two ZX85-12G-S+ bias tees made by Mini-Circuits. High frequency ground-signal-ground probes are model 40A-GSG-150P by Picoprobe. A diagram of the experimental setup is shown in Figure 4.7.

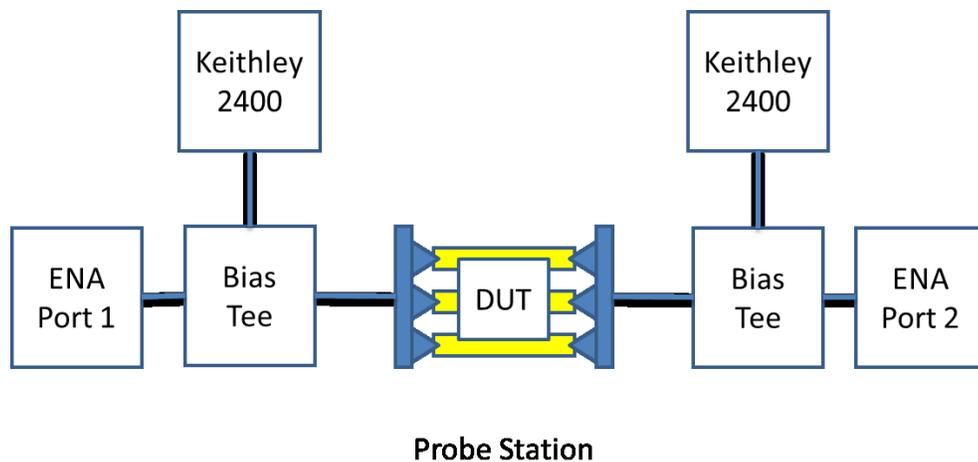


Figure 4.7 – Experimental setup for S-parameter measurements

Measurements are first performed with the device in the “OFF” unbiased state. These measurements are used as a control to ensure that behavior in the biased state is due to the transistor and not to other factors. In an unbiased state, both PN junctions of a BJT should be blocking signal in either direction. Under these conditions, the separated space charge regions of unbiased or reverse biased PN junctions behave like a parallel plate capacitor.

The magnitude of S_{11} and S_{22} for an unbiased BJT are plotted in Figure 4.8.

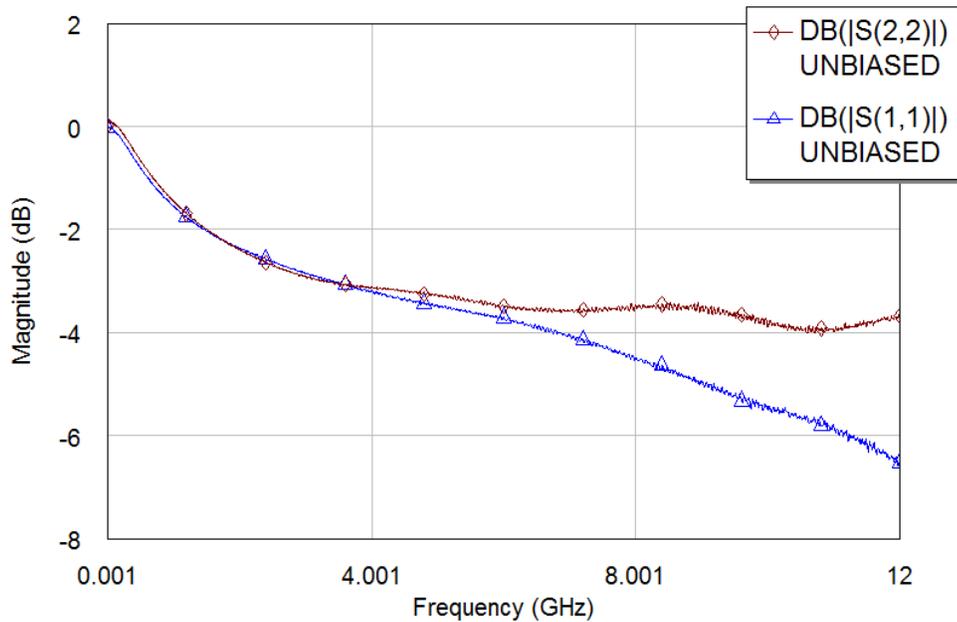


Figure 4.8 – S_{11} and S_{22} for an unbiased BJT

The magnitudes of S_{11} and S_{22} show high levels of reflection as would be expected of an unbiased BJT. An examination of the Smith chart for S_{11} and S_{22} shows their real and imaginary components (Figure 4.9).

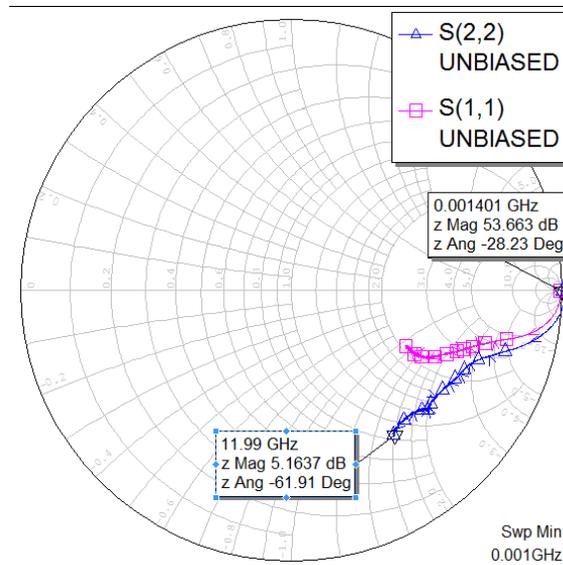


Figure 4.9 - Smith chart of S_{11} and S_{22} for an unbiased BJT

The Smith chart shows that S_{11} and S_{22} have roughly equivalent resistive components, and are both capacitive, which is consistent with unbiased PN junctions. Signal incident on port 2 also sees a larger capacitive load than signal incident on port 1.

The values for S_{21} and S_{12} are low, which is consistent with the measured values of reflection (Figure 4.10). An unbiased BJT will not transmit signal in either direction.

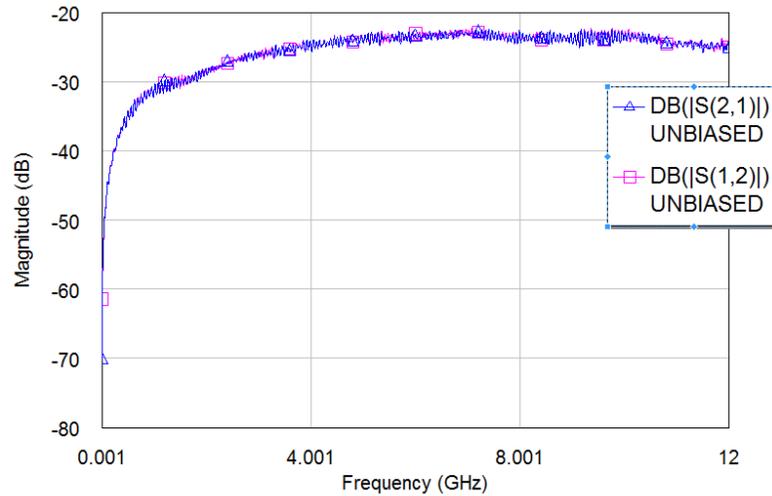


Figure 4.10 – S_{21} and S_{12} of an unbiased BJT

S_{21} and S_{12} are nearly identical and neither reaches -20dB up to 12 GHz.

An unbiased BJT behaves predictably under microwave conditions. Most signal is reflected, and reflections from ports 1 and 2 are both consistent with a capacitive load.

For measurements the “ON - g_m ” state, we biased port 2 (V_{CE}) at 5 V. Port 1 (V_{BE}) was biased at 1.2 V. The corresponding I_{BE} was 180 μ A and I_{CE} was 1.87 mA. This biasing corresponds to a DC condition of high transconductance.

In the biased state, S_{22} is still high. In forward active mode, the collector-base junction is reverse biased, so we expect to see a large S_{22} value as we did in the unbiased case. S_{11} , however, is lower, reaching a minimum at around 8.9 GHz

(Figure 4.11). Lower values of reflection are consistent with a forward biased base-emitter junction and an impedance matched tapered CPW electrode.

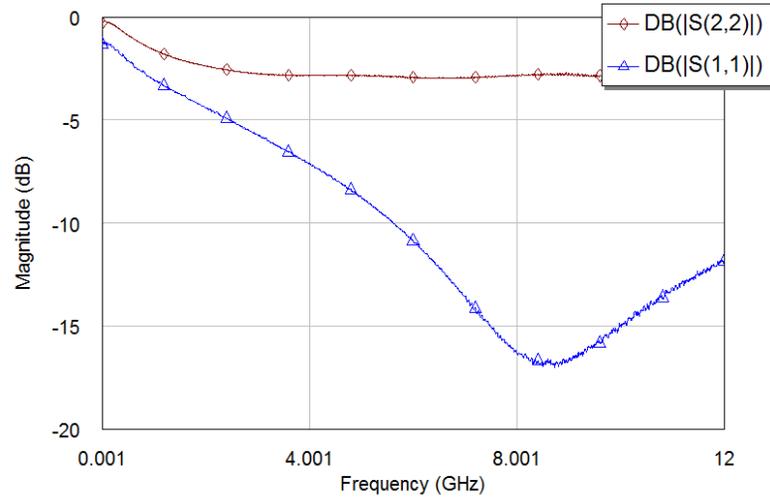


Figure 4.11- S_{11} and S_{22} for an “ON – g_m ” biased BJT

The Smith chart for S_{11} and S_{22} shows that the minimum for S_{11} corresponds to the point that it crosses over from the capacitive (negative) to the inductive (positive) side of the chart (Figure 4.12). S_{22} has a similar resistance and reactance to the transistor in the unbiased state.

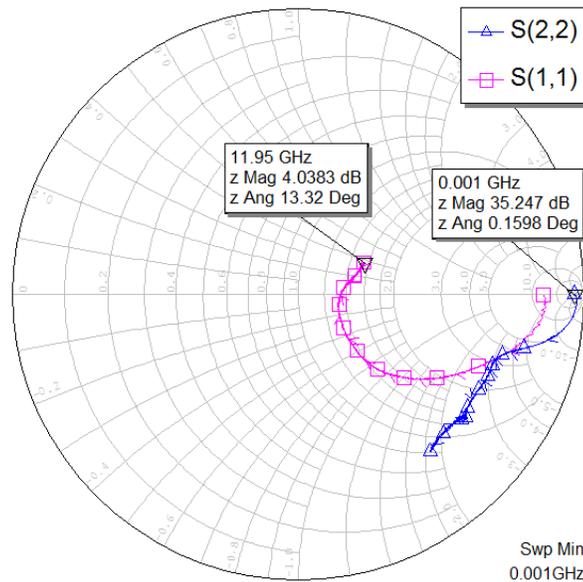


Figure 4.12 – Smith chart of S_{11} and S_{22} for an “ON - g_m ” biased BJT

The most significant outcome of biasing the transistor into the “ON - g_m ” state is higher signal transmission on the forward direction (figure 4.13). At the low end of the frequency spectrum, S_{21} is significantly higher in the “ON - g_m ” state than it was in the unbiased. While microwave frequency gain is not observed, it is observed that biasing the transistor has an effect on the transmission and reflection of microwave signal. S_{12} is even lower than in the unbiased state.

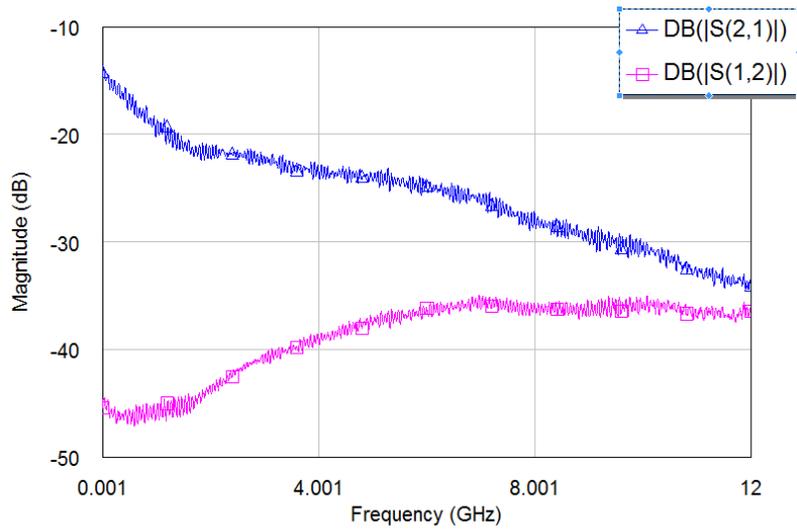


Figure 4.13 – S_{21} and S_{12} for and “ON – g_m ” biased BJT

The microwave performance of an “ON- β_F ” biased device has similarities to each of the other two regimes. For this biasing condition, V_{CE} was set to 2V and V_{BE} was set to 0.72V. The corresponding I_{CE} was 11 μ A and I_{BE} was 10nA.

S_{11} shows a similar minimum to the one observed in the “ON - g_m ” state, this time a little below 8 GHz (Figure 4.14). S_{22} is also lower than in “ON - g_m .”

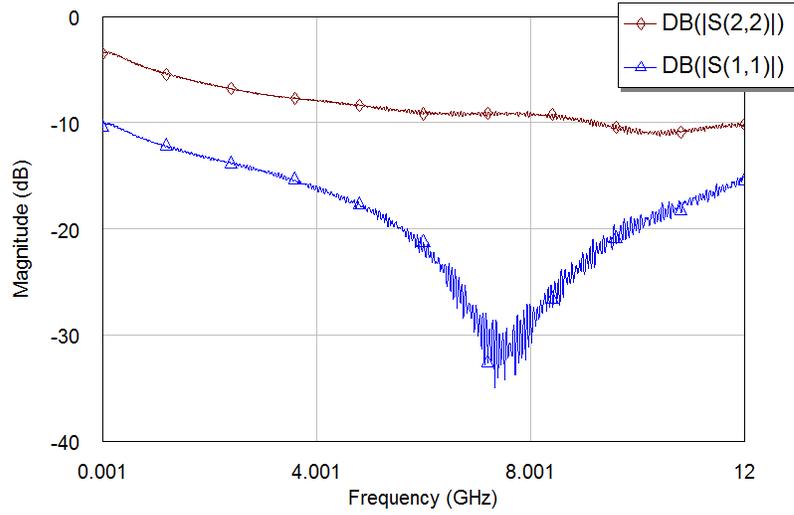


Figure 4.14 - S_{11} and S_{22} for an “ON- β_F ” biased BJT

The Smith chart (Figure 4.15) shows S_{11} near the center, corresponding to low signal reflection at all frequencies. Its minimum just below 8 GHz is again where it crosses over from capacitive to inductive loading.

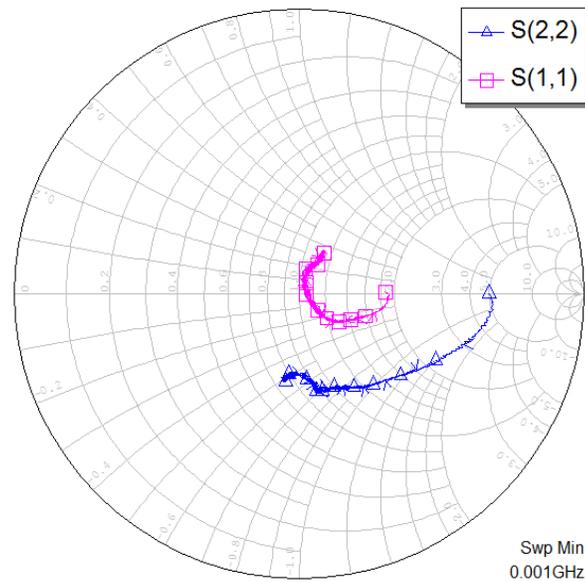


Figure 4.15 - Smith chart for an “ON- β_F ” biased BJT

S_{21} and S_{12} were both higher in under these conditions than they were in the unbiased device, but signal transmission observed in the “ON - g_m ” state was not observed (Figure 4.16). The difference between signal transmission in the forward and reverse directions was less than 3 dB.

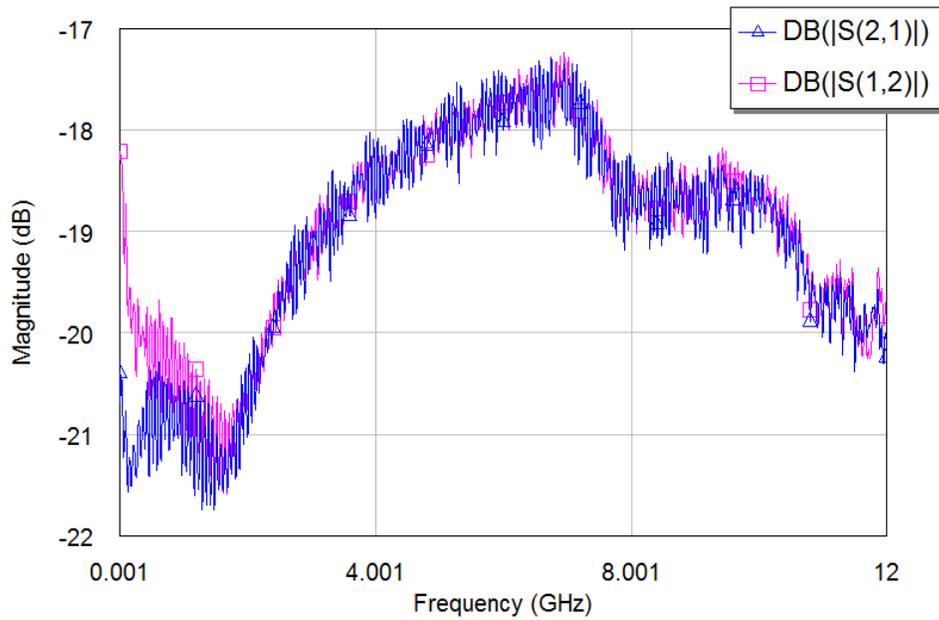


Figure 4.16 - S_{21} and S_{12} for an “ON- β_F ” biased BJT

An important characteristic of a two-port network is its reciprocity. A reciprocal network is one where transmission and reflection are equal regardless of which direction they come from. By definition, for a reciprocal network

$$S_{21} = S_{12}$$

$$S_{22} = S_{11}$$

Networks containing passive, anisotropic materials are always reciprocal. Networks containing active or directional components, however, can be non-reciprocal. Components like amplifiers and isolators are exploited for their non-reciprocal behavior in order to achieve gain and provide directional transmission of signals. The two reciprocity factors are a measure of how non-reciprocal a two-port network is

$$\epsilon_1 = S_{21} - S_{12}$$

and

$$\epsilon_2 = S_{22} - S_{11}$$

For a reciprocal network

$$\epsilon_1 = \epsilon_2 = 0$$

Non-reciprocal devices without gain have values of ϵ_1 and ϵ_2 between 0 and 1. Devices with gain can have values higher than one. While microwave frequency gain was not observed in our devices, they did exhibit non-reciprocal behavior that was dependent on their biasing conditions, clearly indicating active behavior at these frequencies.

Figure 4.17 shows values for ϵ_1 under the three biasing conditions. For the unbiased and “ON- β_F ” “ON- g_m ” states, ϵ_1 is very low. For the state, “ON - g_m ” state, however, measurable ϵ_1 is observed. This is in agreement with the expectation that a transistor,

when biased in forward active mode, should transmit signal in the forward direction but not in the reverse direction. When unbiased, signal is rejected in both directions, consistent with expectations.

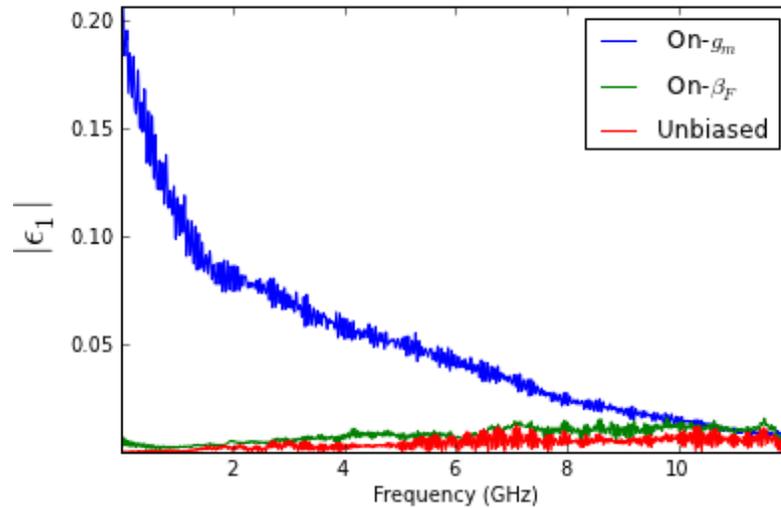


Figure 4.17 - ϵ_1 for the three biasing regimes

Figure 4.18 shows values for ϵ_2 under the three biasing conditions. In the case of reflection, we see non-reciprocal behavior under all three biasing conditions, with an increase in ϵ_2 as bias levels are increased.

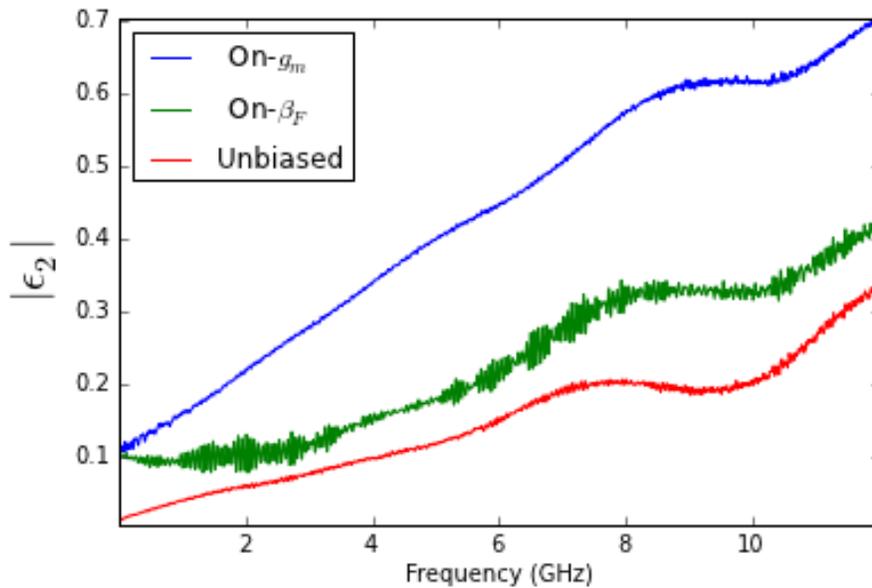


Figure 4.18 - ϵ_2 for the three biasing regimes

The non-reciprocal behavior of these BJTs suggests that, with further improvement, they may be useful in certain microwave applications. The fact that the non-reciprocal behavior can be switched on and off depending on biasing conditions gives this type of device an advantage over passive non-reciprocal components such as PIN diodes. High DC values for transconductance and DC gain suggest that if reflection can be reduced, similar devices might be able to provide high frequency signal gain.

While the goal of microwave signal gain has not yet been achieved in this generation of devices, they do exhibit switchable, non-reciprocal behavior under certain biasing conditions. Three different modes of operation are identified at DC and observed at microwave frequencies. With further design improvements and reduction in signal

reflection, devices of this design may exhibit microwave frequency gain, enabling their use in flexible microwave frequency amplifiers.

Chapter 5: Conclusions and Outlook

In this work, progress is presented toward the development of flexible microwave frequency SiNM bipolar junction transistors. New techniques are presented for the transfer printing of metal films and SiNM devices. An impedance matched tapered coplanar waveguide electrode structure was designed and demonstrated to transmit microwave frequency signals, in good agreement with simulation.

The effects of localized Joule heating due to high current density are observed. Issues with metal electrode failure are addressed by the use of W as an electrode material, but device performance still degrades rapidly under DC bias conditions. A SiNM BJT with ultra-narrow base region was designed, modeled, fabricated and characterized at DC and microwave frequencies. Two modes of DC operation are identified, one with high transconductance and the other with high DC current gain. While gain is not observed at microwave frequencies, the devices exhibit switchable, directional signal transmission.

Prior to this work, transfer printing of deposited metal films had been limited to Au. When deposited on Si wafers, Au has adhesive properties that are suitable for transfer printing and pre-transfer device processing. Other metal films, however, adhere too strongly to Si and will not transfer reliably. In order to lower adhesion, common surface treatments based on SAMs of FTDS and OTS are deposited before metal deposition. FTDS lowers adhesion too much, and metal films are damaged during

pre-transfer processing. OTS is damaged due to the transfer process itself, and films are not cleanly released. Parylene C is shown to have a surface energy between that of Si and the SAM treated surfaces, indicating that it is a suitable pre-deposition surface treatment. Films deposited onto parylene C coated Si wafers survive pre-transfer processing and are successfully transfer printable onto flexible substrates. Resistivity measurements taken before and after transfer printing verify that the films are of high quality and that they are not damaged during the transfer printing process.

SiNM transfer is also examined. The previously reported flip-transfer technique is replicated, and found to be suitable when SiNM features are large. After release, the SiNM is coupled to the Si handle wafer by hydrogen bonding and Van der Waals forces, both of which are proportional to contact area. For small devices, it is found that this coupling is insufficient to hold the membrane in place during post-release rinsing in DI water. In order to facilitate transfer printing of small SiNM devices with good alignment, an oxide “pillar” technique is demonstrated. SiNMs are partially released, with small SiO₂ sections left un-etched. These pillars hold the SiNMs in place during the transfer process, maintaining alignment and preventing the SiNMs from floating off during rinsing. Transfer is performed in a NIL tool where the host wafer is brought into contact with a flexible substrate and high pressure and temperature are applied. The oxide pillars punch through the SiNM, decoupling it from the SOI wafer and completing transfer. Transferred devices are shown to have maintained alignment through the process. Post-transfer metals deposition and lift-off is demonstrated, as well as post-transfer Si etching in RIE. The oxide pillar

technique developed for this project should be compatible with the transfer of SiNMs of arbitrary size.

In order to expand the functionality of SiNM devices, a microwave frequency BJT on SOI is designed. For reasons of scalability, processing is limited to standard CMOS processing techniques including photolithography. An ultra-narrow base region with a width of only ~200 nm is designed using a self-aligned poly-Si sidewall spacer technique combined with angled ion implantation. Spacer formation is demonstrated and characterized using cross-sectional SEM. Two-dimensional ion implant modeling is performed using the ATHENA software package. Post-implant annealing is also simulated to show the effects of dopant diffusion during RTA. A protective nitride patch is deposited to prevent electrical contact between the base electrode and the collector.

In order to deliver microwave frequency signals to the BJTs, an impedance matched electrode configuration is necessary. The CPW configuration was chosen due to its compatibility with our device geometry. Impedance is calculated, and non-ideal characteristics of the CPW are accounted for. Because the size of the devices is smaller than the alignment capability of the probe station, a tapered CPW is needed that can interface with both the widely spaced GSG probes and the narrow device features. A python script calculates the spacing of a CPW given a center trace width, and this script generates a photomask design file. The tapered CPW configuration is simulated using HFSS and shown to be well impedance matched, with the vast

majority of signal being and very little being reflected. A test CPW structure is fabricated and its S-parameters measured. While the test sample shows higher reflection than the HFSS model, the loss is only about 1 dB and signal transmission was deemed sufficient for device characterization.

Due to the small size of the devices, metal traces need to be very narrow in order to make contact. These narrow traces are subjected to high current density during device operation and the effects of localized heating are observed. Au and Si, which form a eutectic system, are shown to diffuse into each other, even in the presence of a Ti barrier layer. This diffusion shorted out devices, making them unusable. Cu electrodes are shown to melt under device operating conditions. Au and Cu have melting points of 1064 °C and 1085 °C, respectively. In order to overcome the damage associated with high operating temperatures, W was chosen as an alternate electrode material due to its high melting point of 3422 °C. A two-step etch technique is used for W in order to achieve vertical, anisotropic features with a high selectivity of W over Si and SiO₂. The use of W as an electrode material solves the problem of electrode failure, but the effects of localized heating still lead to a rapid decrease in device performance, likely due to dopant diffusion.

DC characterization is performed with the primary purpose of identifying the biasing conditions for microwave frequency measurements. Two regimes of DC operation are identified, one with high transconductance and one with high DC current gain. Microwave frequency performance is measured for devices biased in each of the two

regimes, as well as on unbiased devices. Microwave frequency gain is not observed, but in the regime of high transconductance, the attenuation of signal is much lower in the forward direction than in the reverse. If this non-reciprocal behavior can be optimized, these devices could have applications as microwave frequency isolators. Further optimization could lead to microwave signal gain, enabling their use in amplifier circuits.

While the basic design and fabrication processes have been developed, there remains significant opportunity for future work on these SiNM BJTs. Localized Joule heating is still the largest hurdle to be overcome before these devices can be integrated into existing flexible electronic systems. This problem could be addressed by a change in device geometry, with an eye towards reducing current density. The most straightforward way to decrease current density would be to fabricate a device with larger contact areas so that metal traces can be made wider. Contact regions were initially designed to be narrow in order to minimize resistive losses in the current flowing through the Si itself. A wider base contact region would correspond to a longer current path through the emitter, adding to device resistance.

The design of these devices could be modified to reduce this resistance, however. Part of the collector region could be heavily doped before poly-Si is deposited, leaving low doping only in the vicinity of the base region. Doing so would allow for a wider base contact region without much added resistance. Collector and emitter contacts could be widened simply by extending the boundary of the device.

With the problem of heating mitigated, it will be much easier to get reproducible data from these devices. Due to short device lifetimes, AC measurement has focused on microwave characterization because microwave gain was the initial goal of the project. Lower frequency AC characterization, particularly cutoff frequency, would be useful in benchmarking device performance. An increase in device lifetime would enable better AC characterization.

If the heating issue can be solved, the elements of a transfer process for these devices are already in place. Larger metal traces and contact areas would fall within the alignment capabilities afforded by the pillar SiNM transfer method. There is a good probability that the next iteration of Si device design could produce the first microwave frequency SiNM BJT.

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