ABSTRACT

Title of Thesis: THERMOELECTRIC COOLING OF HIGH FLUX ELECTRONICS

Sevket Umut Yuruker, Master of Science, 2017

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On-Chip Thermoelectric cooling is a promising solution for thermal management of next generation integrated circuits. This thesis focuses on three thermoelectric cooling applications for high flux electronics. A micro contact enhanced thin film thermoelectric cooler was designed for remediation of a 5kW/cm^2 hotspot and its integration with manifold microchannel system is numerically demonstrated. In addition, thermoelectric cooling was utilized for thermal de-coupling of electronic chips with different operating temperatures, eliminating the need to over-cool the entire package. Furthermore, effect of

decreasing contact resistances in thin film thermoelectrics was numerically investigated to effectively remove 100W (~280W/cm^2) of heat dissipation from quantum cascade lasers. Finally, a system-level optimization methodology is established with comprehensive mathematical modeling, verified with numerical simulations. Master curves are generated to understand the effect of system-level parasitics on performance and optimal design variables. In conclusion, the advantages of thermoelectric cooling for high flux electronics is demonstrated in this thesis.

THERMOELECTRIC COOLING OF HIGH FLUX ELECTRONICS

by

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Thesis submitted to the Faculty of the Graduate School of the

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Dedication

I dedicate this to my family: Mom, Dad and my little Sister.

Thanks for always supporting me.

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I would like to thank my advisors Professor Bao Yang and Professor Avram Bar-Cohen. Thank you for providing me the opportunity to study on cutting edge research topics and widen my knowledge and experience. Your friendly and supportive demeanor always helped me understand and solve many research problems.

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NOMENCLATURE

TE	Thermoelectric Element
TEC	Thermoelectric cooler
COP	Coefficient of performance
Z	Figure of Merit for TE [1/K]
ZT	Figure of Merit for TE
m*	Effective mass [kg]
n	Carrier concentration [$1/m^3$]
PF	Power Factor [$W/m\text{-}K^2$]
Q	Net heat pumped at the specified junction [W]
T	Temperature [K]
I	Electrical Current [A]
S	Seebeck Coefficient per TE element [V/K]
R_{TE}	Electrical resistance of TE element [ohm]
k	Thermal conductivity of TE element [W/m-K]
K	Conductance of the TE element [W/K]
L	Thickness of the TE element [m]
A	Area [m^2]
R_{source}	Sum of source side structural resistances per TE element [K/W]
R_{sink}	Sum of sink side structural resistances per TE element [K/W]
T_{source}	Source temperature [K]
T_{sink}	Sink(Fluid) temperature [K]
Q_s	Heat flow from the source per TE element [W]
q''	Heat Flux [W/cm^2]
HTC	Heat transfer coefficient [$W/m^2\text{-}K$]
N	Number of elements within the thermoelectric module
$R_{str,areal}$	Area based version of the structural resistance [cm^2K/W]

Greek Symbols

μ	Carrier mobility [$m^2/(V\text{-}s)$]
γ	Ratio of sink side resistance to total structural resistance
Δ	Difference in temperature [K]
ρ	Electrical resistivity of TE element [ohm-m]
ρ_{ECR}	Electrical contact resistivity [$ohm\text{-}m^2$]

Subscripts

c	Denotes cold junction of the TE element
h	Denotes hot junction of the TE element
opt	Denotes the optimum value for the variable
e	Denotes element level
eff	Denotes effective
str	Denotes structural
trace	Denotes electrical resistance of the Cu trace
spr	Denotes spreading
s	Denotes source
ECR	Denotes electrical contact resistance

1 Introduction

1.1 Motivation

Continuous rise in heat dissipation of integrated circuits necessitate advanced thermal solutions to ensure system reliability and efficiency. Power amplifiers, such as IGBTs and HEMTs, are examples of high power devices, which process and dissipate more energy than typical logic chips. In GaN based amplifiers, linear power dissipation in excess of 40W/mm has been demonstrated, however device power dissipation is limited to less than 5W/mm due to reliability concerns [1, 2]. In particular, local hotspots pose a significant challenge on maintaining system reliability due to the significantly increased heat fluxes, which are in the order of kW/cm^2 [3-6].

Therefore, next-generation integrated circuits necessitates superior—and hence more complex—cooling methods. Thermoelectric cooling, especially thin film thermoelectric cooling is a favorable solution for both hotspot mitigation. For applications where the background heat fluxes are within reasonable range (in the order of 10s or 100s of W/cm^2), the TECs can also serve as the sole cooling mechanism for the overall uniform background heat fluxes [7, 8].

This work focuses on developing various packaging schemes and optimization of important system and device level parameters for cooling of high flux electronic devices through numerical end experimental investigations.

1.2 Thermoelectric Phenomena and Figures of Merit

There are three effects in the thermoelectric phenomena; Seebeck effect, Peltier effect and Thomson effect, which are discussed in this section. The energy carried by an

electron (or hole) is material dependent, therefore the carriers flowing through a junction of two different conductors either absorb or release heat. This constitutes the Seebeck and Peltier effects, which are inverse explanation of this physical process. The material property that enables such process is referred to as “Seebeck Coefficient (V/K)”. Thus, the materials that possess larger magnitudes of Seebeck coefficients (generally negatively or positively doped semiconductors) are called thermoelectric materials and larger magnitudes of Seebeck coefficients are desired for improved cooling and power generation.

In the presence of a temperature differential between the hot and cold junctions, an open circuit voltage is created. This is called the Seebeck effect. Conversely, if electrons (or holes) are made to flow through a junction of two dissimilar materials via an externally applied voltage difference, heating or cooling will occur at these junctions. This is referred as the Peltier effect. Lastly, if there is a temperature gradient within a conducting material, a continuous Peltier/Seebeck effect occurs within the material itself, due to the fact that the Seebeck coefficient is temperature dependent and is different along the material. This effect is called the Thomson effect. However it is typically not considered in the thermoelectric equation because the magnitude of this effect is significantly smaller than the other effects [9].

There are two intrinsic parasitic terms in thermoelectric phenomena, joule heating and back conduction. As other semiconductors, thermoelectric materials also have mediocre electrical conductivity. Significant joule heating occurs when electrical current flows through the material, this is the main inherent parasitic that limits the electrical current. The other parasitic term is the back conduction, which occurs due to the conduction

of heat from the hot junction to the cold junction through the thermoelectric material. Thus, to improve the performance of the thermoelectric devices, lower values of electrical resistivity and thermal conductivity are desired.

$$Q_c = ST_cI - \frac{1}{2}I^2R_{TE} - K(T_h - T_c) \tag{1.1}$$

$$Q_h = ST_hI + \frac{1}{2}I^2R_{TE} - K(T_h - T_c) \tag{1.2}$$

$$R_{TE} = \rho\frac{L}{A_{TE}} \tag{1.3}$$

$$K = k\frac{A_{TE}}{L} \tag{1.4}$$

As can be seen from the equation (1.1), the Seebeck cooling term "STI" is linearly related to the temperature of the medium and the electrical current. Thus the net cooling value is increased at larger electrical currents and elevated temperatures. It is important to note that, increasing these parameters also lead to an increase in the heat rejected at the hot junction, indicating that proper heat removal needs to be considered for high flux applications.

To understand a thermoelectric materials ability to perform good cooling/heating or power generation, various figures of merit have been introduced. The most common figure of merit is the Z value [10]; which is defined as;

$$Z = \frac{S^2}{k\rho} \tag{1.5}$$

Since the result is in (1/K), a new t figure of merit, ZT is introduced by multiplying the equation by the temperature of the media during the measurement to obtain a non-dimensional figure of merit [10], and is given as;

$$ZT = \frac{S^2 T}{k\rho} \tag{1.6}$$

Z and ZT serve as generally applicable figures of merits in evaluation of thermoelectric applications. However for high flux cooling applications, the primary goal is to increase the amount of net heat that can be pumped. The electrical resistance is the only parameter that limits the operating current and in turn reduces the achievable net heat flux, and thermal conductivity becomes less important for such applications [15]. Therefore, another figure of merit, power factor, is introduced as;

$$PF = \frac{S^2}{\rho} \tag{1.7}$$

Lastly, thermoelectric cooling is solid state form of refrigeration, and COP can be defined as the net amount of heat pumped by the total energy consumed [10], and is given as;

$$COP = \frac{(S_p - S_n)T_c I - \frac{1}{2} I^2 R_{TE} - K(T_h - T_c)}{I^2 R_{TE} + (S_p - S_n)(T_h - T_c)I} \tag{1.8}$$

1.3 Thermoelectric Materials

Most common thermoelectric materials used in commercial thermoelectric modules are Bismuth Telluride (Bi_2Te_3) and its alloys with other metals such as Sb_2Te_3, Bi_2Se_3, and Bi_4Te_6 [11, 12, 13]. They are semiconductors which are either positively or negatively doped to achieve large magnitudes of Seebeck coefficients. Both P-type and N-type elements are required to build the module since the current flows through a series connection of thermoelectric elements. The most important material property of

thermoelectric materials, the Seebeck value, is related to its dopant concentration. In Bi_2Te_3 based materials, it was found that lower concentration of tellurium results in positive Seebeck values while higher concentration results in negative, as can be seen in Figure 1.

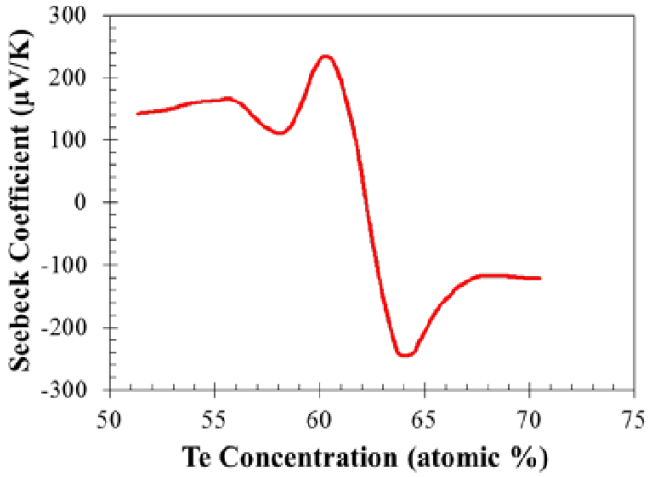


Figure 1: Dependence of Seebeck coefficient on Te concentration for BiTe [14]

However, the figure of merit Z is a combined value of all three material properties, the Seebeck coefficient, electrical and thermal resistivity, which are all affected differently by the dopant concentration. The Figure 2 shows the combined effect of all three material properties on the figure of merit Z.

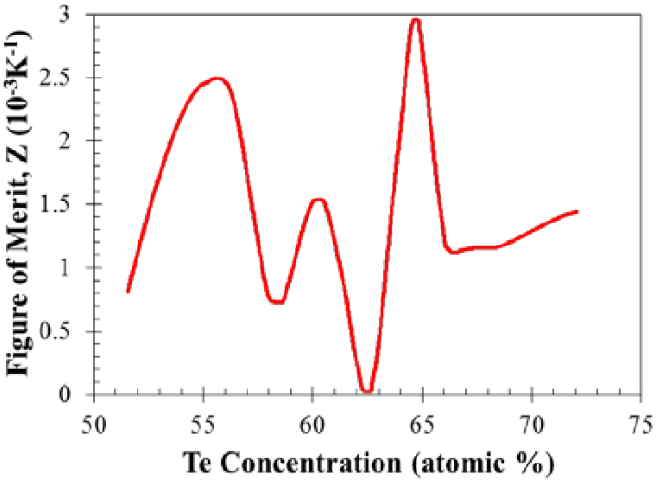


Figure 2: Dependence of figure of merit, Z, on Te concentration for BiTe [13]

In order to enhance thermoelectric performance, researchers have studied ways to decrease the electrical resistivity and thermal conductivity of the materials. However, thermal conductivity and electrical resistivity of a material are linked to each other by Weidemann-Franz law [15]. Therefore it is a challenge to decrease thermal conductivity while increasing electrical conductivity, or at least keeping it constant.

Thermal conduction has two contributing components; the electrical component where the heat is transferred via the energy carrying electrons and the lattice component where the phonons carry the heat as vibrations. Thus, through layer by layer grown structures called super lattices, it is possible to decrease the phonon transport while the electron transport is almost unaffected. The diffuse reflections at interfaces between the layers scatter the phonons and does reduces heat transfer. This significantly decreases the thermal conductivity of the material while the electrical resistance does not change [16-19].

Similar to the tradeoff between electrical and thermal effects, there are trade-offs to consider in the efforts of increasing the Seebeck coefficient of a doped semiconductor. The Seebeck value of a doped semiconductor is given as;

$$S = \frac{8\pi^2 {K_b}^2}{3eh^2} mT \left(\frac{\pi}{3n}\right)^{\frac{2}{3}} \tag{1.9}$$

It is clear from the given expression that Seebeck value increases as the carrier concentration “n” increases. However the theoretical equation of the electrical resistivity also depends on the carrier concentration as follows;

$$\rho = \frac{1}{ne\mu} \tag{1.10}$$

This equation indicates that greater values of carrier concentration to enhance Seebeck coefficient will result in an increase in the electrical resistivity. Therefore the concentration must be optimized to obtain the maximum ZT, as shown in Figure 3.

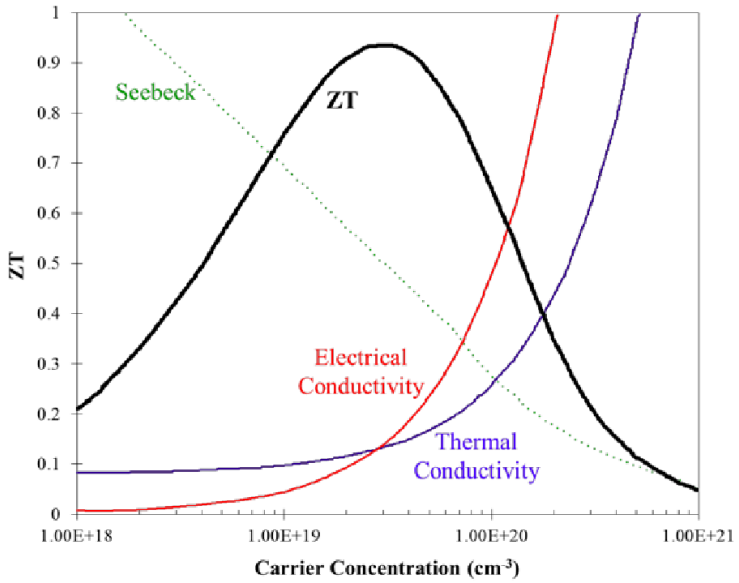


Figure 3: General behavior of Seebeck coefficient, electrical conductivity, and thermal conductivity as a function of carrier concentration for Bi_2Te_3 [15]

1.4 Conventional (Bulk) Thermoelectric Cooling

Thermoelectric modules have multiple couples of P- and N- type elements, which are electrically connected in series and thermally connected in parallel. The electrical connection between the thermoelectric legs is accomplished using traces that are made out of conductive materials, such as copper or aluminum. The thermoelectric elements are bonded to the metal traces with various types of solders, depending on the desired operating temperatures.

Traditional thermoelectric coolers have bulk semiconductor legs in the order of millimeters, achieving very large temperature differentials by means of decreased thermal conductance. However, the thick legs also cause significant intrinsic electrical resistance, which restricts the optimum current. As can discussed before, the Peltier cooling term "STI" is linearly related with the electrical current "I" passing through the elements, therefore the optimum current restriction directly dictates the maximum cooling power of the device.

Other than improving the material properties to enhance the cooling power of traditional thermoelectrics, studies have shown that changing the leg angle can provide larger packing fractions, which in turn increases the achievable maximum cooling flux. [20] As the angle between the thermoelectric legs gets closer to 90 degrees, effective packing fractions more than 1 is obtainable as shown in Figure 4.

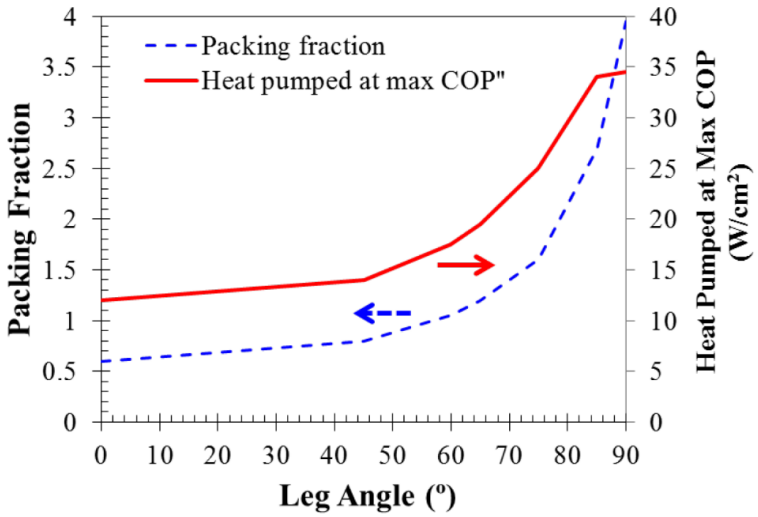


Figure 4: Dependence of packing fraction and cooling flux at maximum COP on element leg angle [20]

It is obvious from Figure 4 that even with the enhancement of the leg angle, the heat flux capacity of the conventional thermoelectrics is considerably low. They are useful for

cooling of heat sources with considerably low heat fluxes, or they are very suitable for temperature controlled applications. However not suitable for thermal management of high flux electronics, where the heat dissipation level is already in the order of 100s of W/cm^2, and expected to exceed kW/cm^2 in the near future.

1.5 Thin Film Thermoelectric Cooling

One of the main obstacles in achieving high cooling flux is the restriction on the optimum operating current due to the intrinsic electrical resistance of the TE elements. There is not a unanimously accepted value of a thickness that separates the Bulk and thin film regimes, however the thickness of most thin film thermoelectric coolers (TFTECs) are in the range of micrometers. The reduction in the TE element thickness allows for higher optimum currents and it can be seen in the equation (1.11) and Figure 5 that, reducing the thickness of the thermoelectric legs by an order of magnitude results in an increase in cooling power of approximately one order of magnitude [21].

$$q_{max} = \frac{1}{l}\left[\frac{S^2 {T_c}^2}{2\rho} - k(T_h - T_c)\right] \tag{1.11}$$

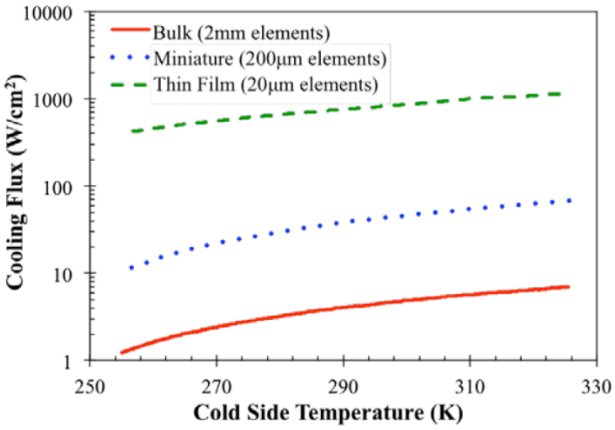


Figure 5: Cooling flux as a function of cold side temperature for three element thicknesses for a BiTe alloy based thermoelectric device [22]

As a side note, for thin film thermoelectrics, the contact resistances dominate the overall electrical resistance of the module because the inherent electrical resistance is reduced significantly, and contact resistances must be addressed for higher cooling performances.

Using approximately 2000 layers with each one having about ~10 Angstroms thickness, Venkatasubramanian et.al. has successfully manufactured superlattice thin film thermoelectric elements with element level cooling flux of 585W/cm^2 and 700W/cm^2 at 353K and 298K respectively [23].

In another study, Harman et al presented their findings with a PbSeTe quantum dot superlattice thin film thermoelectric cooler fabricated using molecular beam epitaxy. Using the configuration shown in Figure 6, a maximum device level ΔT of 43.7K is achieved at I=650mA. To compare the enhancement over bulk TECs, Harman also compared this result with a bulk TE leg with similar dimensions and achieved a ΔT of 30.8K, which shows the improvement via the enhanced material properties of such superlattice structures [24].

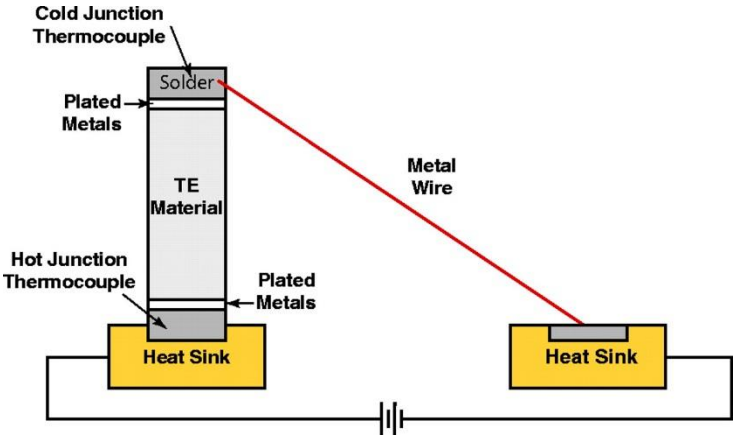
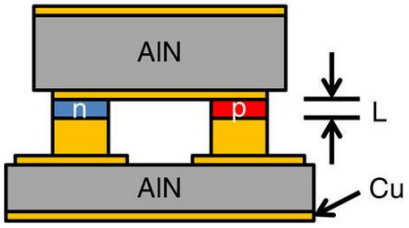
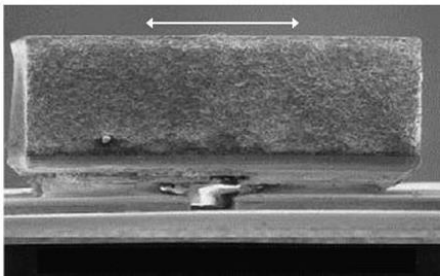


Figure 6: Test structure for single leg TEC [24]

In their previous studies, Bulman et.al has already demonstrated element level heat flux of 715W/cm^2 and a device level cooling of 128W/cm^2 with their Bi_2Te_3 superlattice thermoelectrics. [27] The main reason for the discrepancy between the element level and device level cooling fluxes is the low packing fraction of the module. The packing fraction is defined as the ratio of total thermoelectric elements' footprint by the overall footprint of the TEC module. Due to certain fabrication challenges, packing fraction of TEC modules are typically below 50%, thus large discrepancies between the element level and device level cooling fluxes exist. In a more recent study, Bulman et.al.[25] has successfully manufactured and 8.1 μm thick thermoelectric couple as shown in Figure 7, consisting of a p-type Sb_2Te_3/Bi_2Te_3 superlattice and n-type δ-doped $Bi_2Te_{3-x}Se_x$, both of which are grown heteroepitaxially using metalorganic chemical vapor deposition. Experimental work done on this module demonstrated a much higher device level cooling flux of 258W/cm^2 by the means of the increased packing fraction of 48%[25].



a)



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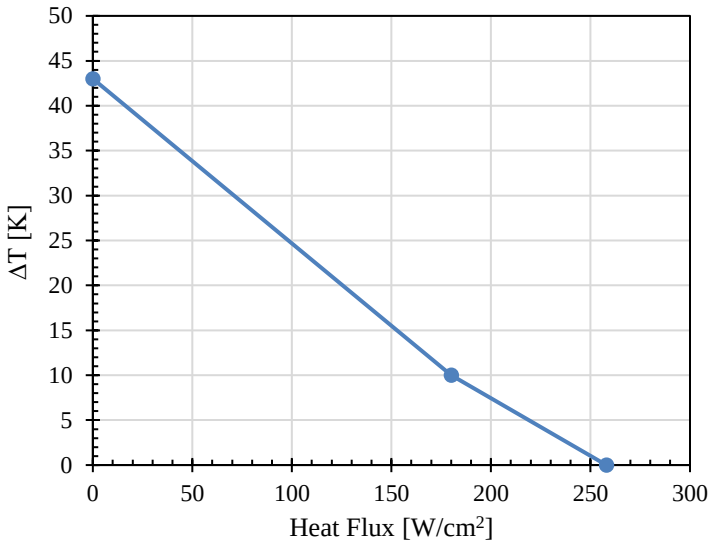


c)

Figure 7: a) Schematic and b) SEM images of the P-N couple used in the study c) The achieved cooling flux curve [25]

The Table 1 below lists a summary of reported TFTEC achievements till today;

Table 1: Reported TFTEC cooling fluxes

Researcher and Year	Classification	Materials	ZT	Max Cooling at ΔT=0 [W/cm^2]	Max ΔT at Q=0 [K]
Venkatasubramanian et al. – 2001 [23]	Superlattice	Bi2Te3/Sb2Te3	2.4 (@ 300K)	700 (@353K) Element level	32 (@ 300K)
Harman et al. – 2002 [24]	Superlattice, Quantum-Dot	PbSeTe/ PbTe (n)	2 (@ 300K)	Not reported	43.7 (@ 300K)
Semenyuk – 2006 [26]	Thinned down Bulk Device	Bi2Te3	1.1 (@ 350K)	132 (@ 350K) Device level	92 (@ 350K)
Bulman et al. – 2006 [27]	Superlattice	Bi2Te3	0.75 (@ 300K)	128 (@ 300K) Device level 715 (@ 300K) Element level	55 (@ 300K)
Goncalves et al. – 2007 [28]	Thin film	Bi2Te3 (n) Sb2Te3 (p)	0.86(n) 0.49 (p)	Not reported	5 (@300K)
Jovanovic et al. – 2009 [29]	Quantum Well Thin Film	Si/SiGe	~7 (@ 350K)	Not reported	Not reported
Bulman et al. – 2016 [25]	Superlattice	Sb2Te3/Bi2Te3	1.4 (p) 1.5 (n)	258	43.5 (@300K)

1.6 Thermoelectric Cooling of Hotspots

Thermoelectric coolers, especially thin film structures, can be made small enough to be integrated into high flux electronics to mitigate local hotspots. The configuration of the initial studies in this field is shown in Figure 8, where a TEC module located right on top of the hotspot and a heat sink was placed on the TEC to remove the rejected heat [30].

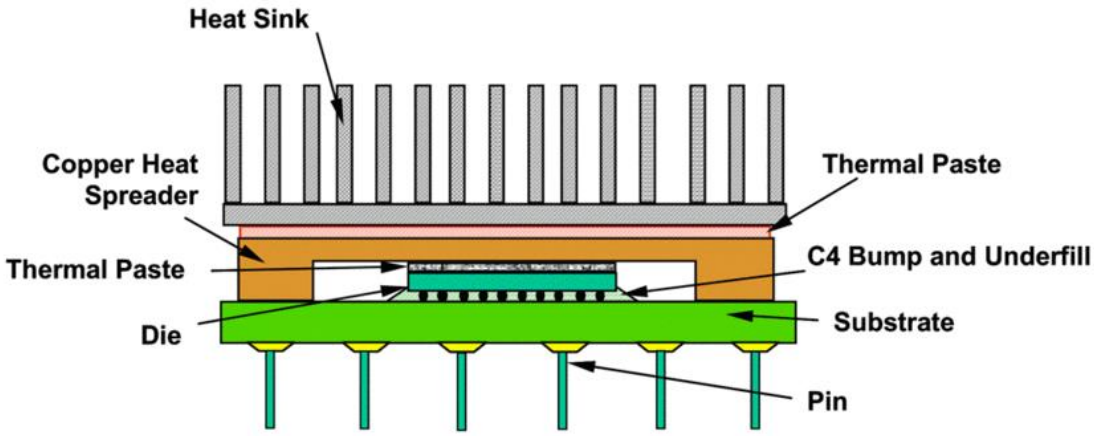


Figure 8: Schematic of a typical thin film thermoelectric hotspot cooling test setup, consisting of a test chip with a hotspot in the center [30]

Chau et.al [30] studied cooling a 400μm x 400μm hotspot located at the center of a silicon chip using a TFTEC with a total thickness of 100μm and footprint of 2.5mm x 2.5mm. The hotspot dissipated 3W of power, resulting in a 1.875 kW/cm^2 heat flux, while the rest of the chip had a background heat flux of 100W/cm^2. Various configurations of the system were evaluated where the location of the TEC differed; the module was embedded in the die, embedded in the Cu heat spreader, or it was located within the TIM layer between the die and Cu spreader. It was found that the placement of the TEC did not cause a significant effect on the hotspot temperature and the TEC was capable of reducing the hotspot

temperature rise by 16K at I=6A supplied to the module. It is important to realize that in each one of these configurations there is thermal back conduction. Embedding the TEC module in a solid material leads to thermal short circuiting between the hot and cold sides of the module. If it could be insulated, the hotspot remediation would be improved.

The Table 2 below summarizes some of the reported achievements in the area of hotspot mitigation with thermoelectric coolers using the conventional approaches similar to the configuration shown in Figure 8.

Table 2: Reported hotspot cooling results in the literature

Researcher and Year	Classification	Hotspot Heat Flux [W/cm^2]	Max Hotspot ΔT [K]	Hotspot Size [μm^2]
Chau et al. – 2006 [30]	Thin Film	1875	16	400x400
Ramanathan et al. – 2006 [31]	Superlattice/ Thin Film	800	17	500x500
Chowdhury et al. – 2009 [21]	Superlattice/ Thin Film	1300	15	400x400
Gupta et al. – 2011 [32]	Superlattice/ Thin Film and Bulk	1250	15	400x400

An improved approach for hotspot cooling is introduced by Wang et al. [7, 8], where a pillar structure called micro-contact (also called mini-contact) is placed between the hotspot and the TEC as shown in Figure 9. The mini-contact's primary benefit is to separate the TEC from the background as much as possible and thus concentrate the cooling power of the module directly on the hotspot.

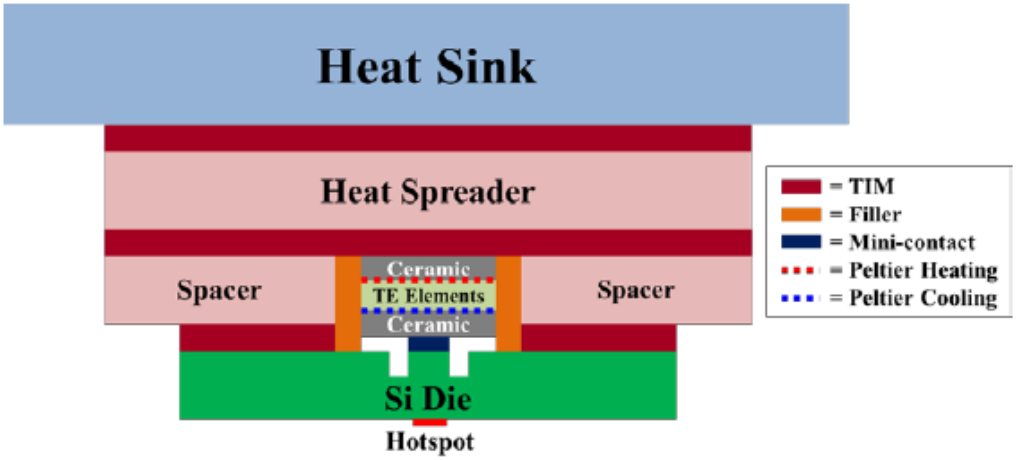


Figure 9: Schematic of the mini-contact enhanced thermoelectric cooling system tested by Yang et al. [8]

In this study, the mini-contact was etched out of the Si chip through making trenches around it, and the thermoelectric device was attached on top of the mini-contact. A Bi_2Te_3 based thermoelectric cooler with a footprint of 3.6mm x 3.6mm was utilized to cool a 400µm x 400µm hotspot with a heat flux of 1250W/cm^2, where the size of the micro contact was optimized to obtain the minimum hotspot temperature rise [8]. His numerical works was experimentally validated by Yang et al. in which the hotspot (613W/cm^2) temperature rise was reduced by ~5.5K using a 500µm x 500µm x 500µm cube of silicon as a mini contact. In 2009, Wang et al. further modified the mini-contact enhanced configuration to include a discrete copper mini-contact, rather than etching the silicon chip as previously discussed [7]. The results shown in Figure 10 shows the improvement in hotspot cooling in the presence of a mini-contact over the case with no mini-contact.

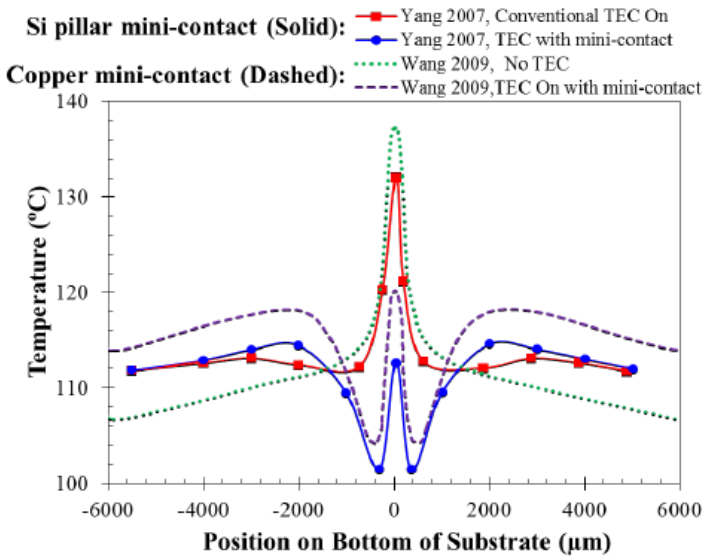
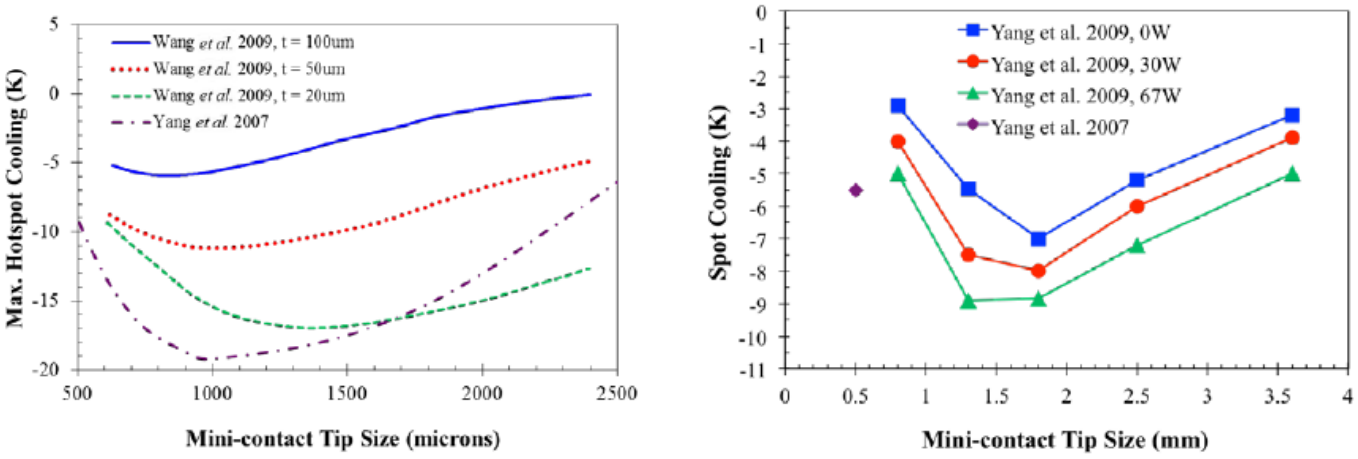


Figure 10: Temperature distribution on the bottom of the silicon substrate in the Yang(2007) and Wang(2009) mini-contact enhanced thermoelectric cooling studies [7,8]

Further numerical studies were conducted to determine the optimum mini-contact size in the given systems, their results are presented in Figure 11-a below;



a) b)

Figure 11: a) Numerically b) Experimentally determined temperature reduction on the backside of the silicon substrate as a function of mini-contact tip size [7, 8]

In order to validate the numerical results, a commercially available thermoelectric device, with a footprint of 1.8mm x 1.8mm, was attached to a silicon test chip. The silicon test chip was heated uniformly with powers of 0, 30, and 67 watts and the maximum temperature reduction achieved with mini-contact enhanced cooling was measured. Figure 86 shows the maximum spot cooling as a function of mini-contact tip size for the three chip powers tested in the Wang et al. study. Larger chip powers resulted in elevated chip temperatures, which increased the amount of Peltier cooling, thus larger temperature reductions were achieved at higher chip powers. When the chip was dissipating a background power of 0W, a maximum spot cooling of approximately 7K was achieved. Alternatively, when the chip was dissipating a background power of 67W, approximately 9K of spot cooling was measured. The maximum spot reduction achieved experimentally was approximately 9K and there was good agreement with the numerical results as seen in Figure 11-b [7, 8].

2 Integration of Micro-Contact Enhanced TFTEC in Microchannel Manifold System

2.1 DARPA-ICECool Fundamentals

The rapid increase in heat dissipation of next-generation integrated circuits necessitates superior—and hence more complex—cooling methods for heat fluxes in the magnitudes of kW/cm^2. Two-phase microchannel cooling, due to its remarkable heat removal capability, is a favorable cooling method. However, challenges can occur when CHF is exceeded at local hotspots. The uniform cooling over the chip surface may leave

the hotspots with ultra-high heat fluxes unmitigated, thus leading to a non-uniform temperature distribution. Thermoelectric coolers, on the other hand, are scalable and perfectly suited for localized cooling. In particular, micro-contact enhanced thermoelectric cooling, which concentrates the cooling flux of the TEC module on a much smaller area, has recently shown promising hotspot cooling results [7, 8]. Combining these two methods into a single system can provide sufficient heat removal over both the larger surface of the electronic chip as well as high-flux hotspots. This would increase system reliability as well as the lifetime and efficiency.

Recent programs, such as DARPA's ICECool Fundamentals [33], have motivated the development of high performance cooling systems by requiring program participants to achieve high heat transfer coefficients, high outlet vapor qualities, and low pressure drop, while maintaining temperature uniformity with a hotspot. Specifically, the program requires the achievement of two simultaneous objectives explained below:

1. Cooling of 1 kW/cm^2 back ground heat flux at less than 30 K base temperature rise above inlet temperature, greater than 90% outlet vapor quality and less than 10% absolute pressure drop. This objective is to be addressed via two-phase manifold-microchannel cooling (MMC) approach.

2. Cooling of a 200 μm x 200 μm, 5kW/cm^2 hotspot in the center of the chip to with 5 K rise with respect to the background temperature. This objective is to be addressed using a micro-contact enhanced thin film thermoelectric cooler.

These two objectives are targeted to be fulfilled simultaneously, meaning that the thermoelectric cooling system and MMC system needs to be integrated. They are designated to work simultaneously, reliably and smoothly with each other.

2.2 Integration Concept

The approach for mitigating the background heat flux of 1 kW/cm^2 is highlighted in other recent works [34-36], where the FEEDS (thin-Film Evaporation and Enhanced fluid Delivery System) approach is presented. The approach utilizes a novel two-phase, manifold-microchannel configuration. A flow dividing manifold lies perpendicular to the micro-grooved surface and provides alternating liquid inlet and vapor outlet channels. Due to the simultaneous reduction of flow rate and flow length, pressure drop is reduced while heat transfer coefficient is increased as a result of operating in the thermally developing flow regime.

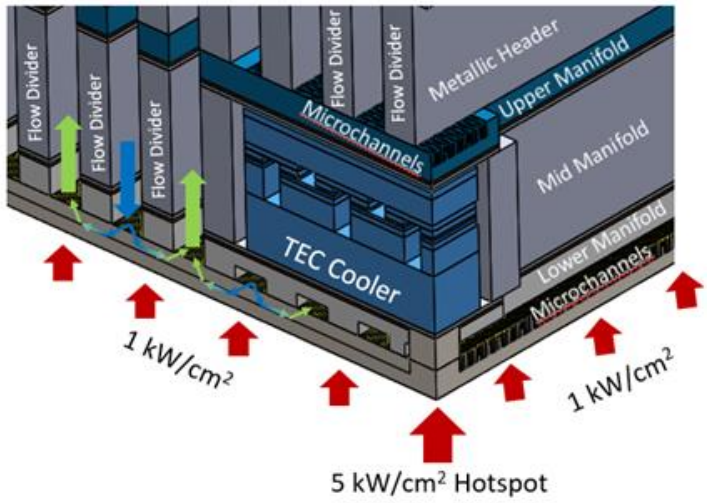


Figure 12: Quarter 3D view of the integrated system

The FEEDS approach shows promise for background cooling, as experimental results showed it is capable of achieving high heat flux (>1 kW/cm^2) and high vapor qualities (~85%) [36-38]. However, this approach alone is unable to meet the desired hotspot cooling. Thus, a thin film thermoelectric cooler will be used to remediate the 5kW/cm^2 hotspot heat flux via help of a mini contact. The use of the mini contact allows separating the TEC module from the background and allows concentrating the cooling

power solely on the hotspot. The heat rejected from the sink side of the device will be also removed with two-phase microchannel cooling on top of the TEC.

Such high heat fluxes are typically found in power electronics, where the operating temperatures are around 150°C. Therefore, water is used as coolant fluid, with its saturation temperature is assumed 110°C in the further analysis. The background is kept within 140C (30K superheat) and the hotspot 145°C (35K superheat).

2.3 Device Level Analysis

As discussed in earlier sections, it is important to determine the contact resistances between the semiconductors and solder layers for accurate analysis and optimization. Therefore, a standard geometry TEC module from RTI/Micross was acquired to extract the contact resistances from the device level performance. The device had a 600 x 600 μm^2 footprint with a single P-N couple, and a thermoelectric material thickness of 6μm. To characterize the device's heat pump curve, an experimental setup is prepared consisting of a laser to provide the heat, a thermal camera to capture the hot and cold side temperatures, and a chiller to maintain the hot side at a constant temperature as seen in Figure 13.

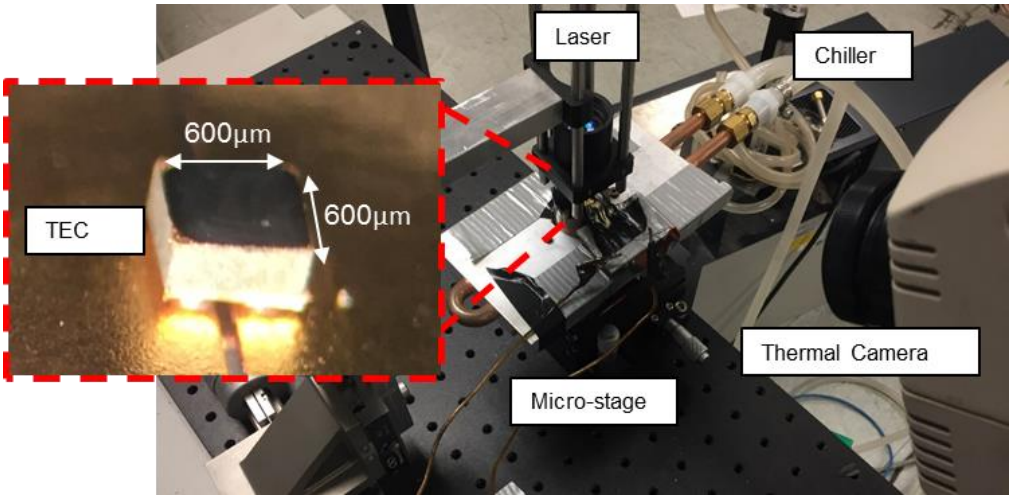


Figure 13: Experimental setup for TEC characterization

Firstly, the optimum current was obtained in the absence of an external heat from the laser, simply by gradually increasing the electrical current to the TEC and observing the change in the generated temperature differential. Once the optimum current was determined as shown in Figure 15-a, the laser was used to gradually heat the source side header of the TEC, and the temperature values were recorded until the source and sink side temperatures were equal, demonstrating the maximum cooling flux capacity of the module, as can be seen in the Figure 15. Once the experimentation was finished, an ANSYS model of the device was built as shown in Figure 14, and the same boundary conditions of the experiment were applied in the model. The electrical and thermal contact resistances were fine-tuned to match the experimental findings. A good agreement was obtained with electrical and thermal contact resistances of 1.5e-10 ohm-m^2 and 1e-7 m^2-K/W, respectively.

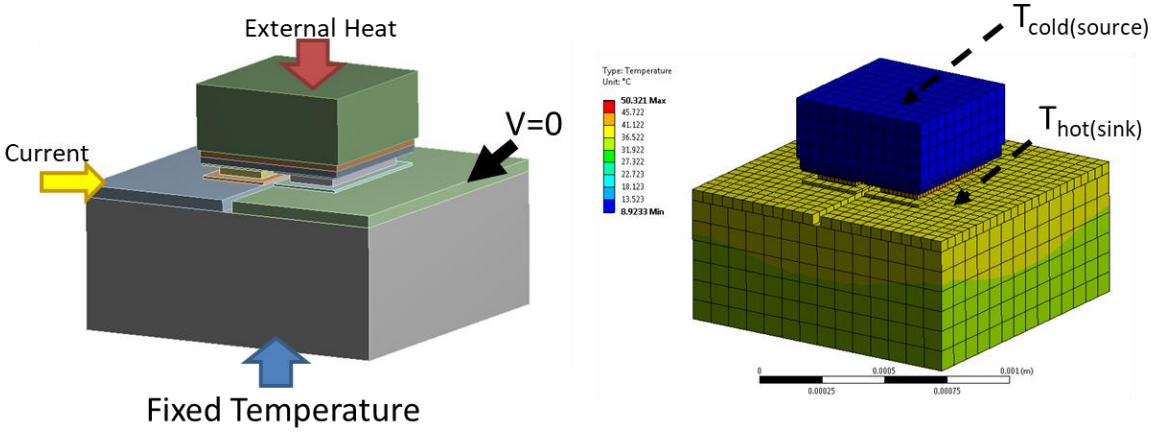
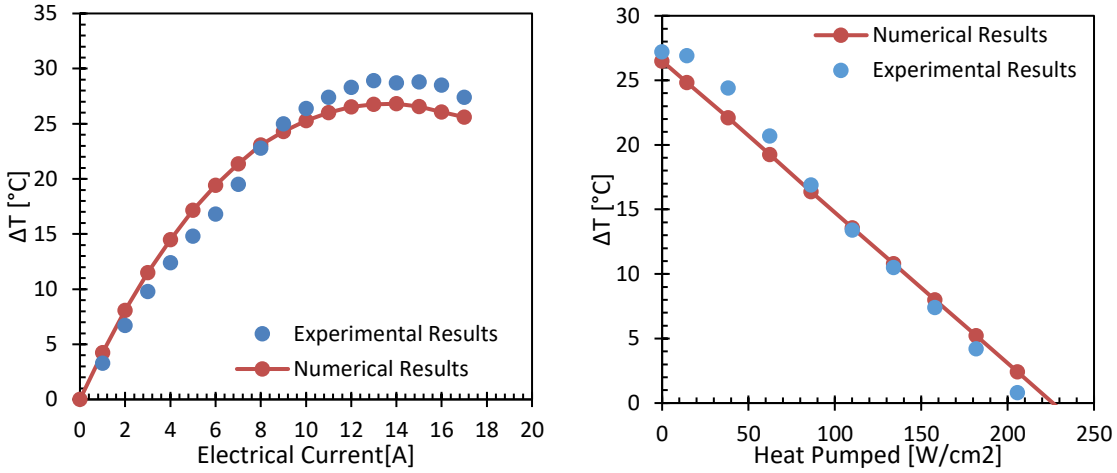


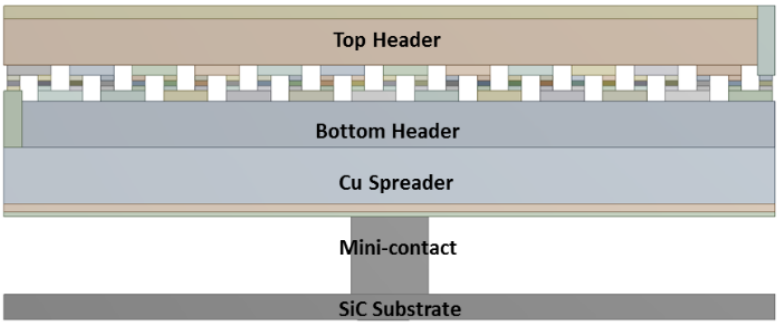
Figure 14: Numerical model of the characterized TEC module



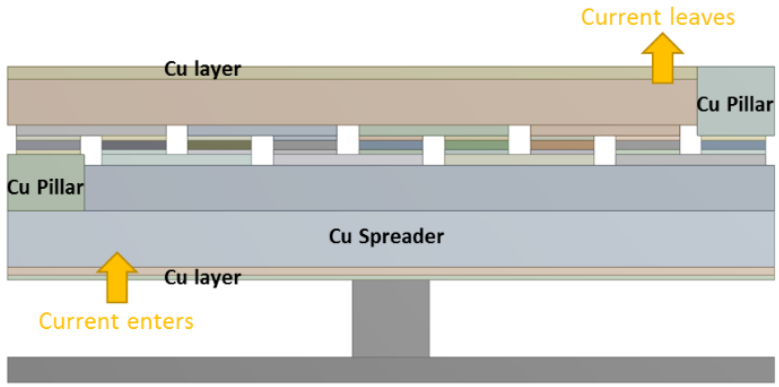
a) b)

Figure 15: Experimental optimum current results and numerical fine tuning

After the contact resistances were determined, the actual Icecool structure was modeled on ANSYS-Workbench as shown in Figure 16. Initial step in the modeling process was to optimize the inner thermoelectric structure, the width, number and thickness of the thermoelectric elements within the module. It can be seen from the model image in Figure 16 that the TEC device was placed on the mini-contact etched from the SiC substrate. The material used in the simulation for the semiconductor elements was Bismuth Telluride with ±220 μV/K Seebeck coefficient. The electrical and thermal contact resistances between the Bismuth Telluride films and the tin solder layers were 1.5e-10 ohm-m^2 and 1e-7 m^2-K/W, respectively. The total footprint of the TEC was restricted to 3 mm x 0.8 mm to minimize flow blockage underneath the TEC. Thus, there was only one row of thermoelectric elements that were 760 μm in length (length direction is into the paper in Figure 16.)



a)



b)

Figure 16: a) Layer by layer explanation of the 25-element structure, b) current path explanation on 9-element structure

The widths of the elements were parametrized from 100 to 250 μm with increments of 50 μm. To make a realistic design, the minimum gap between the semiconductor legs for these different designs was assumed to be 60-80 μm. The number of elements can be fitted, and their corresponding packing fractions can be seen in Figure 17 and in detail in Table 3. In order for the current to enter the module from the bottom surface and leave from the top, two Cu pillars were placed under and on top of the first and last semiconductor legs. This

property of the configuration also dictates that the number of elements must be odd, so that the current can enter/leave from opposite sides.

The lowest hotspot temperature obtained was 250 μm width, and the optimum current for that case was 16.5A, while the 200 μm width yielded almost the same cooling at 13.5A. It was observed in the complete system-level simulations that when the input electrical current exceeded 15 A, the joule heating on the copper wire between the manifold and TEC tremendously increased. This led to elevated temperatures on the copper wires that easily exceeded 150°C. Thus, given that there is not much improvement in hotspot temperature between the 200- and 250-μm designs, 11 x 200 μm width elements with an optimum current of 13.5A were chosen for this application.

It is also important to note that since the minimum gap between semiconductor legs was restricted, the packing fraction inevitably decreases as the number of elements increase. That is the main reason larger elements yield better cooling. If the same packing fraction could be preserved, theoretically they should yield the same performance.

Table 3: Important optimization parameters and the resultant optimum thicknesses

Element Width [μm]	Element Quantity	Packing Fraction [%]	Optimum Thickness [μm]
50	25	42	26
100	17	57	31
150	13	65	35
200	11	73	38
250	9	75	39

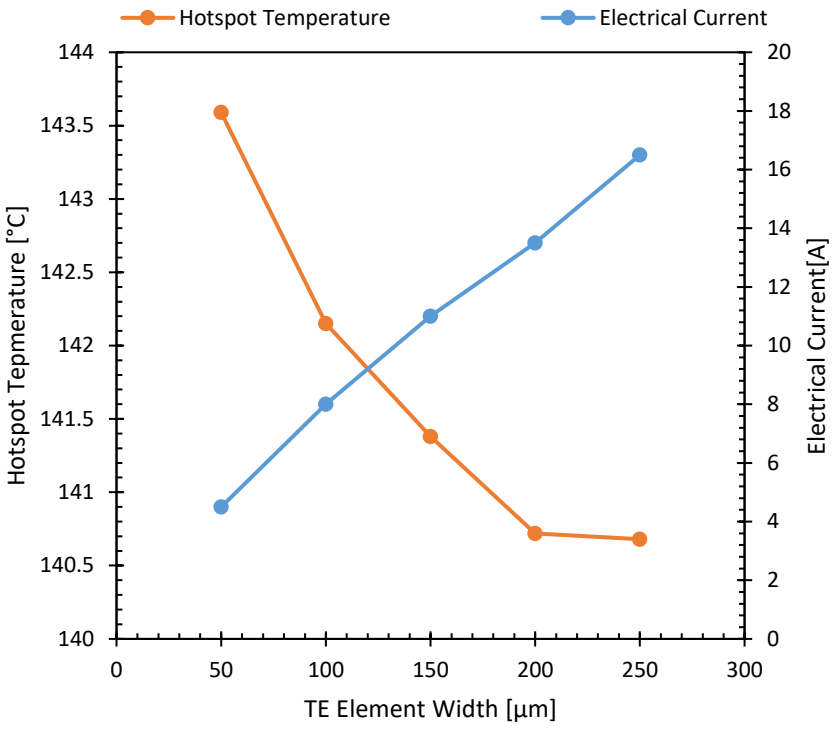


Figure 17: TEC inner structure parameterization results

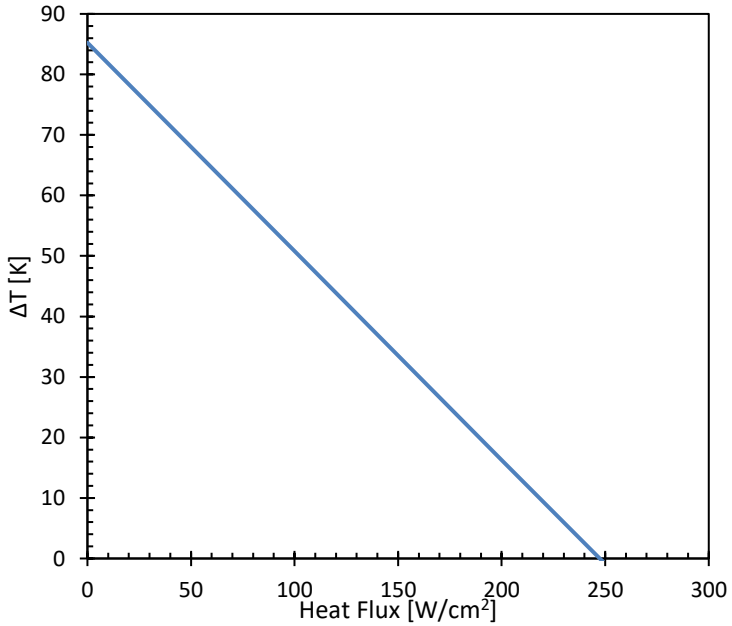


Figure 18: Numerical device level characterization of the final design (370,000W/m^{2}K at 110°C, I=13.5A)

After determining the optimum inner structure for the TEC, the device level performance was characterized as shown in Figure 18. Since the sink side will be subjected to evaporative cooling at 110°C in the actual system, a convection boundary condition was applied on the hot side for the characterization.

The initial simulation results indicated that the module has ~150 W/cm^2 Q_{max} at 25°C, which is expectedly lower than what has been published by RTI (258W/cm^2) [12]. But as discussed before, the maximum cooling flux capacity alone doesn't always imply better performance; the achievable temperature differential is also very important, especially when there are many structural resistances besides the TE element. Thus instead of focusing on the improving the Q_{max}, the main focus of the optimization process was on improving the ΔT at the given heat flux coming from the mini-contact.

It is also very important to realize that the operating temperatures of the integrated system is expected to be approximately T_{sat}=110°C, which is much higher than 25°C and the thermoelectric cooling performance increases with temperature of the operating media. With hot side having a convection boundary of 370,000 W/m^2-K at 110°C, cooling flux capacity improves to 250 W/cm^2 as can be seen in Figure 18.

2.4 System Level Analysis

There are certain system-level parameters to be analyzed to achieve the highest possible performance. One important consideration is the uniformity of the heat reaching the TEC's bottom surface. Especially when utilizing a mini-contact to enhance thermoelectric cooling, this uniformity must be investigated, because the size of the mini-contact will be much smaller than the source-side header. This creates a challenge to spread

the heat coming from the mini-contact as evenly as possible over the TEC footprint to make full use of all semiconductor legs. To make this possible, a copper heat spreader was modeled beneath the TEC as can be seen in Figure 19, and a parameterization study was carried out for the thickness of this layer. Interestingly, it was observed that although there is an optimum thickness at around 400 µm, the improvement from 100 to 400 µm is only about 0.4°C. This means that even if there is no copper spreader, the aluminum nitride headers can spread the heat almost as uniformly.

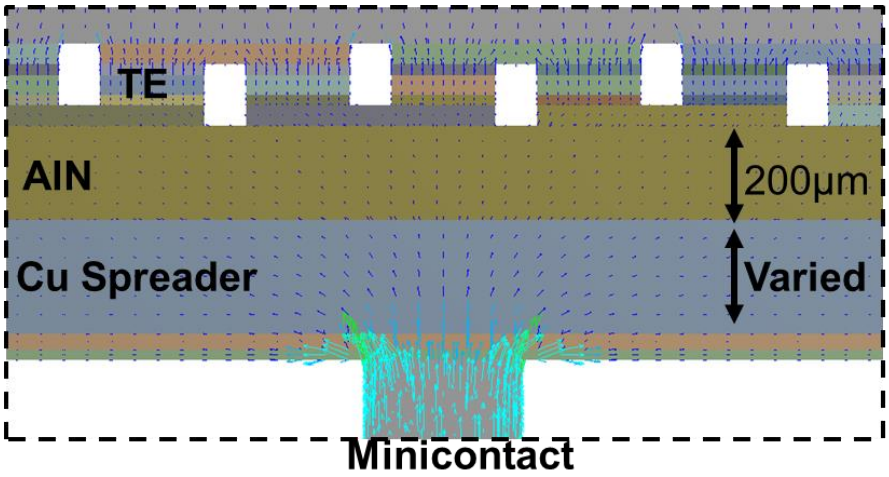


Figure 19: Varied Cu spreader thickness between the TEC module and the mini-contact

SiC is a very conductive material. Therefore, the heat generated at the hotspot easily spreads in the SiC substrate, as can be seen in Figure 20. To cool the hotspot properly, the spreading heat must be fully captured by the mini-contact. This indicates that if the mini-contact size is equal to the hotspot, some of the heat will not travel through the mini-contact, and high hotspot temperatures will be observed. However, it is important to mention that as the mini-contact gets bigger than the hotspot, the surrounding background

heat flux also reaches the mini-contact, and the TEC must deal with more heat than the hotspot alone. Therefore, there must be an optimum size for the mini-contact. To determine that size, the size of the mini-contact has been parameterized. The best results were obtained at the 300-µm edge length, as can be seen in Figure 21.

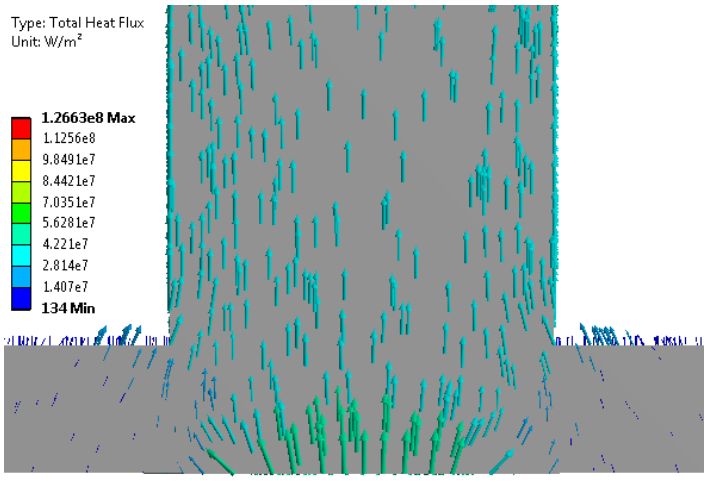


Figure 20: Heat flux vectors show spreading at SiC substrate

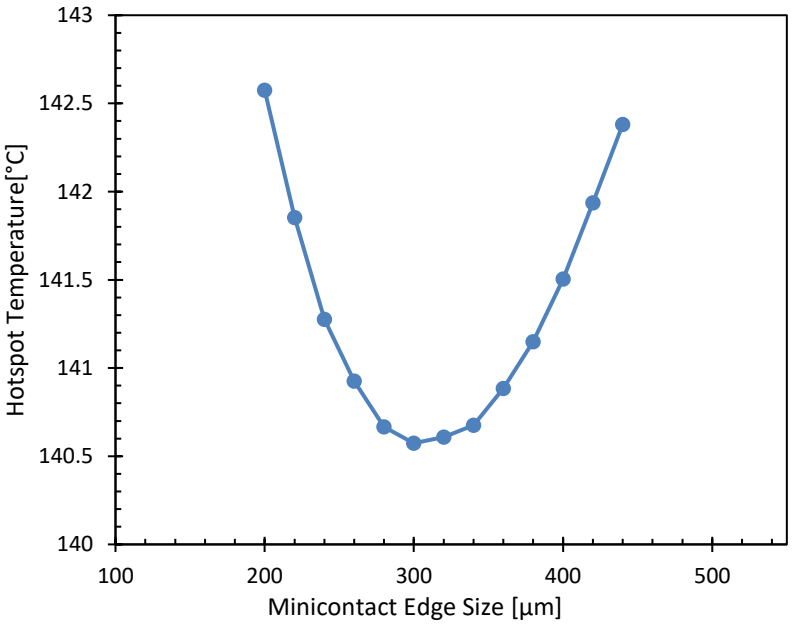
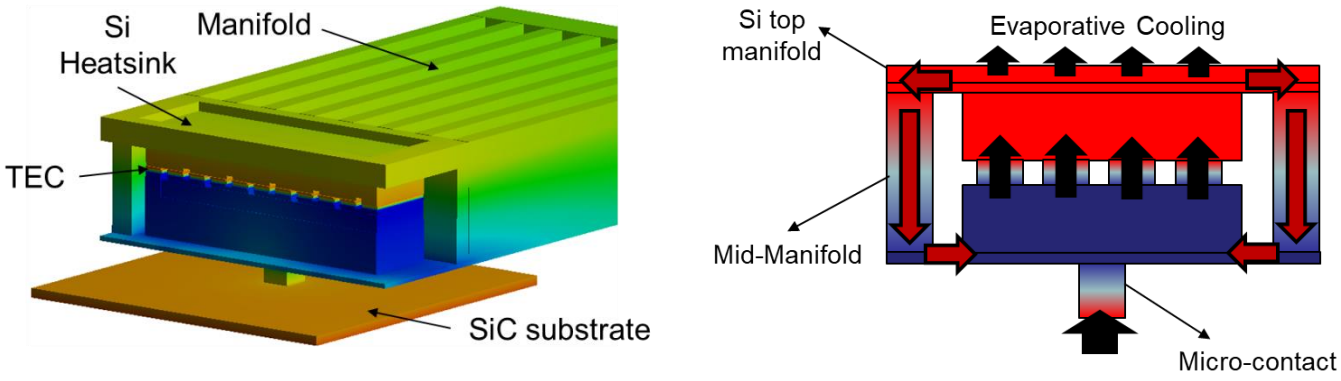


Figure 21: Mini-contact size optimization

Once most of the important components of the system were optimized and modeled, the manifold walls were added to the FEA model to determine the overall performance of the system, as shown in Figure 22.

Initially, the manifold was considered to be made of silicon for ease of manufacturing purposes. However, system-level simulations demonstrated that most of the heat pumped by TEC conducts back through the Si manifold. In other words, the manifold thermally short circuits the system and almost completely undermines the performance.



a) b)

Figure 22: a) The system level model with the manifold, b) schematic explanation of the thermal short-circuiting through manifold walls

Therefore, a parameterization study was performed on the thermal conductivity of the manifold material to determine the maximum allowable thermal conductivity. The results shown in Figure 23 indicate that any material with high thermal conductivity causes significant thermal short circuiting on the system. Thus, as explained in an earlier section, rather than silicon, the mid-manifold was modeled as glass with thermal conductivity of 1 W/m-K.

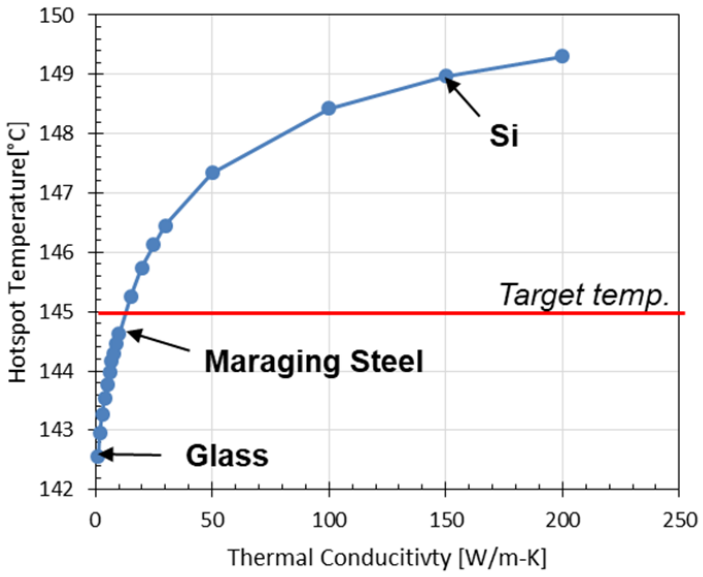


Figure 23: Effect of manifold thermal conductivity on hotspot temperature

Figure 24 shows the overall temperature distribution with the final geometry of our system if operated at the optimum current. In order to show the enhancement on the temperature uniformity over the SiC substrate background, a comparison of the temperature distribution is shown in Figure 25 and Figure 26. By using a thermoelectric cooler, a 14.5°C hotspot temperature remediation is achieved.

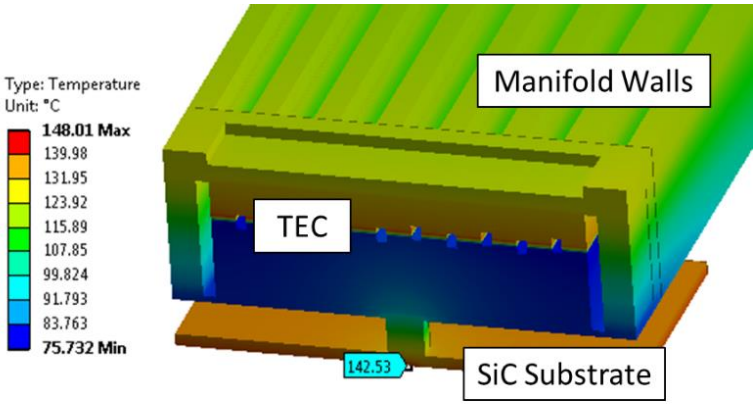


Figure 24: Results for glass manifold (k=1W/m-k) with 300-µm-tall mini-contact (Tmax 148°C occurs on Cu traces far away from the module)

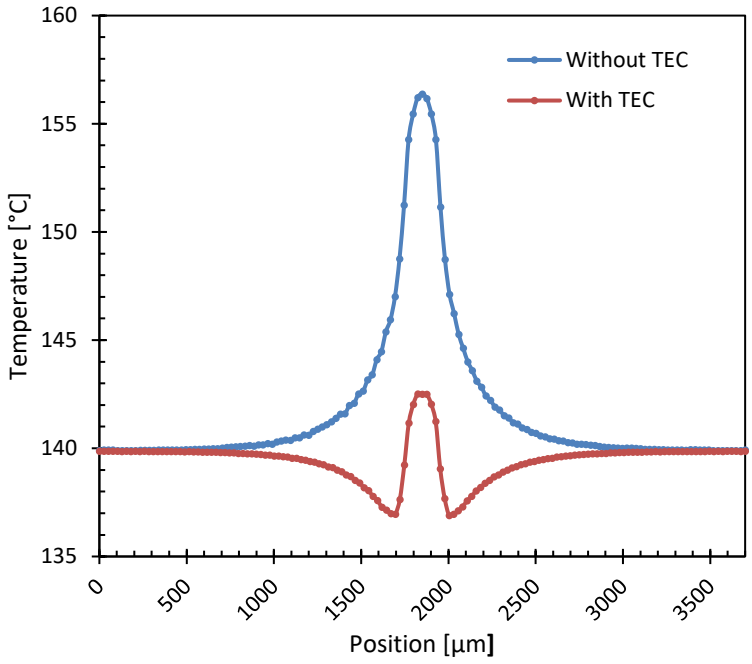


Figure 25: Plotted temperature distribution near the hotspot

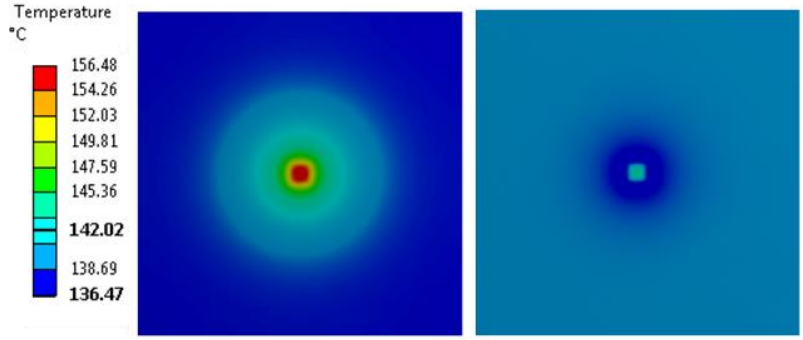


Figure 26: Temperature distribution over the bottom side of the SiC substrate a) without TEC cooling (left) and with TEC cooling (right)

As it was discussed in an earlier section, the optimum electrical current of the TEC module was around 13A, which results in the lowest hotspot temperature. However, it can be seen from the parametric analysis shown in Figure 27 that, in order to reach the project's metric for the hotspot temperature rise, the required current is only 7A. This is important

to know because operating at lower currents has benefits such as higher COP and more reliable TEC structure in terms of electro migration, which is discussed in a following section.

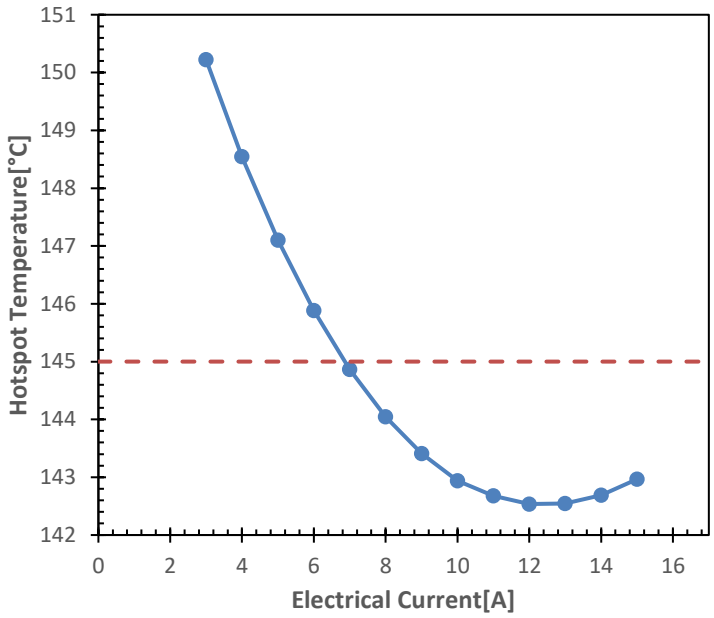


Figure 27: Hotspot temperature as a function of electrical current

The mini-contact height modeled in the simulations so far was 300 μm, mainly due to the layers beneath the TEC (the microchannel fins and a lower manifold), adding up to around 300 μm of height from the substrate. However, the simulation results show that the maximum temperature gradient occurs at the mini-contact. This makes sense because the heat flux in the mini-contact is tremendously high, and even with a very high conductivity material such as SiC, a large temperature drop occurs. Thus, taller mini-contacts make it harder for the TEC to achieve the desired cooling on the heat source. In order to explore the possible outcomes of shorter or taller mini-contacts, the height was parameterized and the hotspot temperature was monitored. The results shown in Figure 28 indicate that if the

mini-contact could be as short as a 200 μm, the hotspot temperature could be lower than as 141°C, meaning that the temperature rise with respect to background temperature (140°C) could be potentially almost completely eliminated.

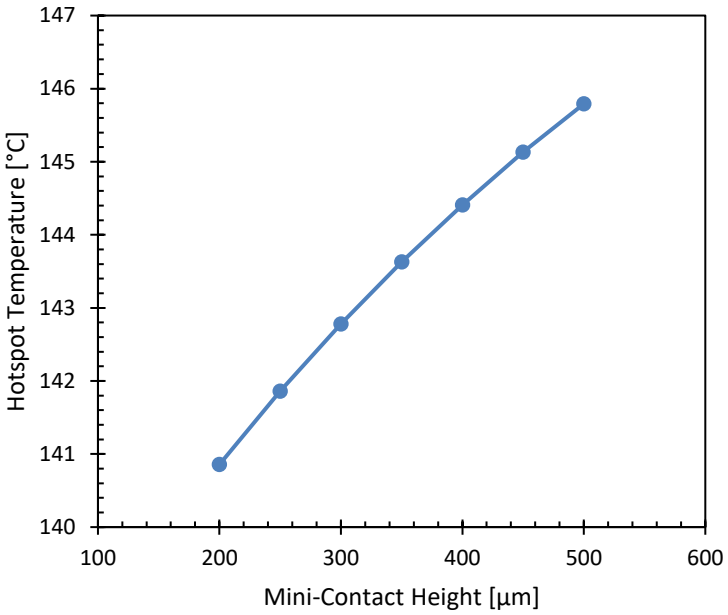
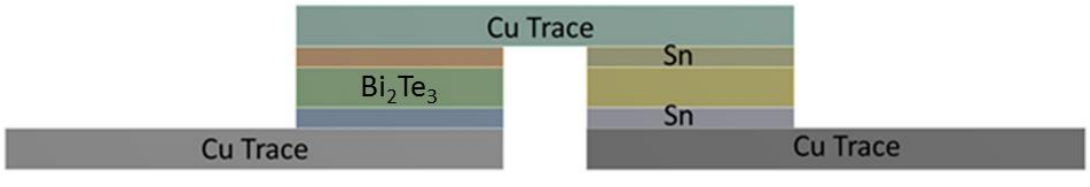


Figure 28: Effect of mini-contact height on hotspot temperature

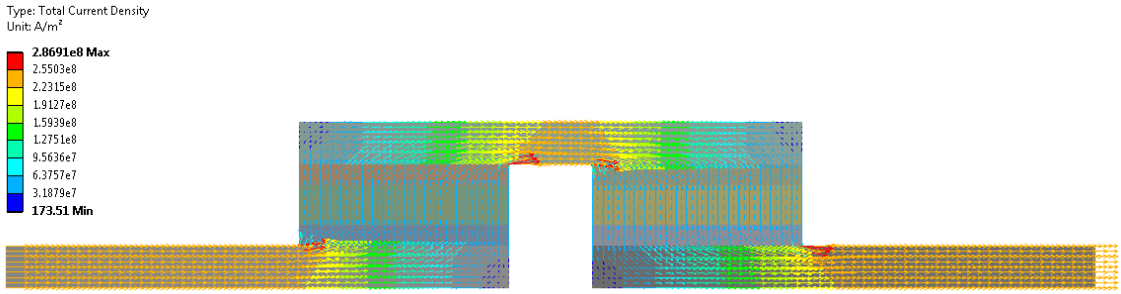
2.5 Electromigration

Material transport can occur in a conductor due to the movement of ions, especially in the presence of high temperature and high current densities, which can lead to voids within the material and eventually complete failure. This phenomenon is called electromigration and must be addressed for high current applications such as thin film thermoelectric cooling. Unfortunately, there is not much work done on investigation of electromigration in thermoelectrics, but there are many studies related to electromigration in thin film solders, which are generally the point of interest, because the solder materials typically have much lower current density thresholds than most of the other conductors [39, 40] To be able to predict whether the ICECool TEC structure will experience

electromigration, the local current densities must be obtained and compared with the existing threshold values in the literature. Therefore, a model was built on ANSYS Workbench shown in Figure 29, which consists of one P-N couple of the full thermoelectric module (including the Cu traces, solder layers and TE elements).



a)



b)

Figure 29: a) Numerical model for current density investigation; b) numerical results for I=7A demonstrating the current crowding effect

As can be seen from Figure 29, the highest current density occurs at the corners where the solder layer meets the Cu traces. This effect is called current crowding and it has been discussed in the literature for similar solder joints [41, 42]. generally the far away regions from the corner doesn't experience high current densities; therefore, the failure starts from the corner and propagates to the other side until complete disconnection. Figure 30 demonstrates the linear increase in maximum observed current density at the corner of the Sn layer as a function of the electrical current input.

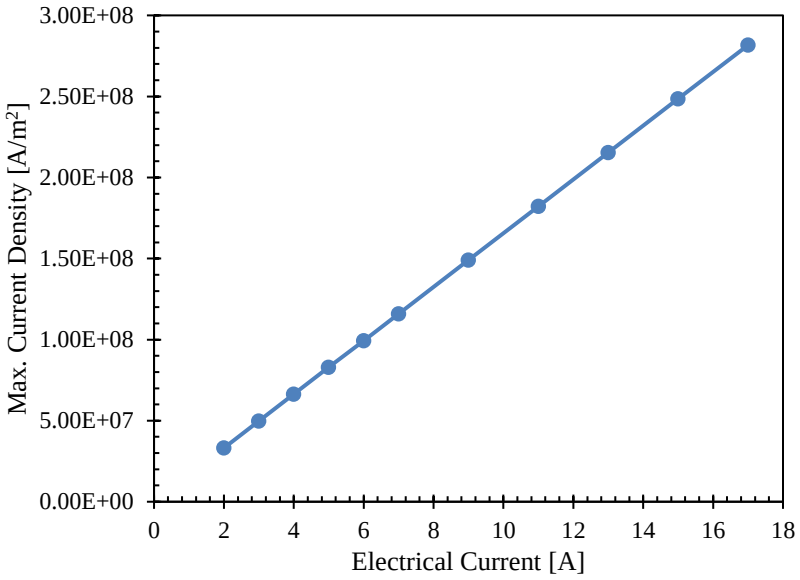
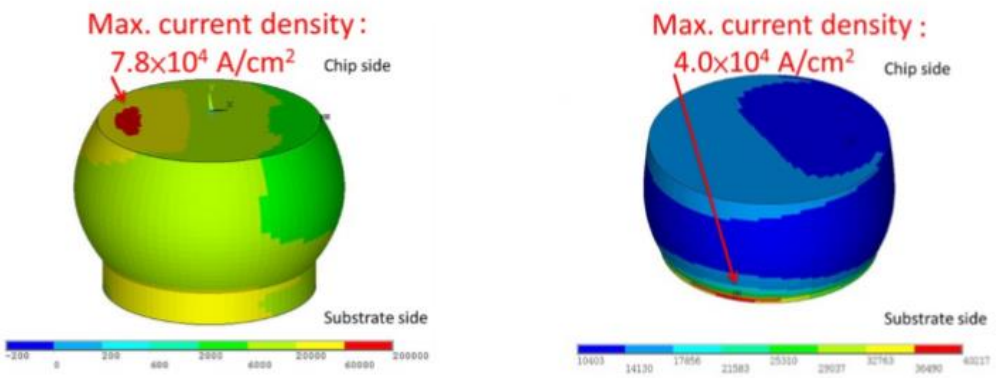


Figure 30: Observed maximum current densities on Sn solder as a function of total electrical current applied to the device

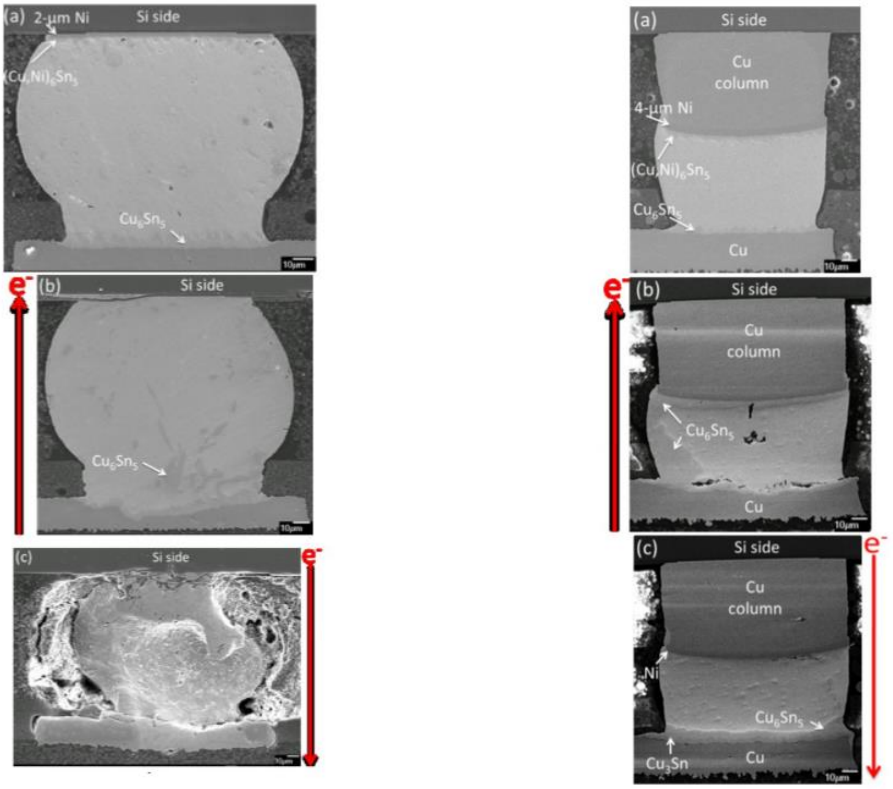
The thresholds for thin-film Sn layers for these discussed operating conditions of ICECOOL design was found to be 7.93×10^7 A/m^2 [39] Thus, given that the current densities are kept below these values anywhere on the solder layer, any possible electromigration issues is circumvented.

The only way to decrease the current crowding effect is through geometrical manipulation of the current path. One practical solution for this is by employing Cu pillar UBMs below the solder layer, so that the turn takes place within the Cu and by the time it reaches the solder joints it is virtually uniform. Liang et al.[42] has demonstrated this methodology both experimentally and numerically and found that by employing Cu pillar UBMs, the current crowding on the solder joint can actually be circumvented, and the lifetime of the device is elongated, as can be seen from Figure 31 and Figure 32 [42].



a) b)

Figure 31: Numerical findings on the current densities for (a) without Cu UBM, b) with Cu UBM [42]



1) 2)

Figure 32: Experimental findings of Liang et.al.[42] 1) SEM images of the solder bump with a 2-μm Ni UBM stressed at 2.16 × 104 A/cm^2 at 150 °C for (a) 0 h, (b) 42.7 h with

upward electron flow and (c) 42.7 h with downward electron flow, 2) SEM images of the solder bump with a Cu column UBM stressed at 2.16 × 104 A/cm^2 at 150 °C for (a) 0 h, (b) 286.5 h with upward electron flow and (c) 286.5 h with downward electron flow [42]

The same approach can be applied to the ICECool structure by adding a pillar-like thickness on the two ends of the Cu traces. This way the current crowding takes place in the Cu, and since Cu has a very high current density threshold, electromigration will be avoided, as can be seen in Figure 33. In order to investigate the current density remediation, the ANSYS model was updated with Cu UBMs, and their thickness was parameterized. According to the simulation results, with a certain thickness of additional Cu UBM, the maximum current density observed at the solder layers can be kept within the threshold values for various electrical current inputs as shown in Figure 34.

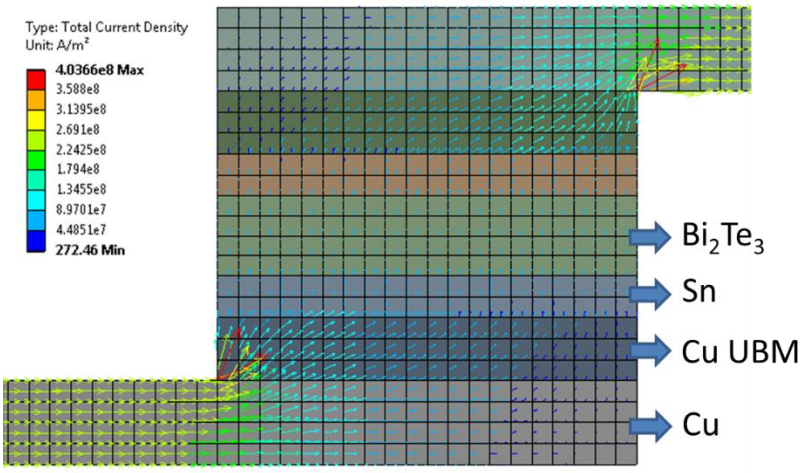


Figure 33: Current density distribution with Cu UBM structure

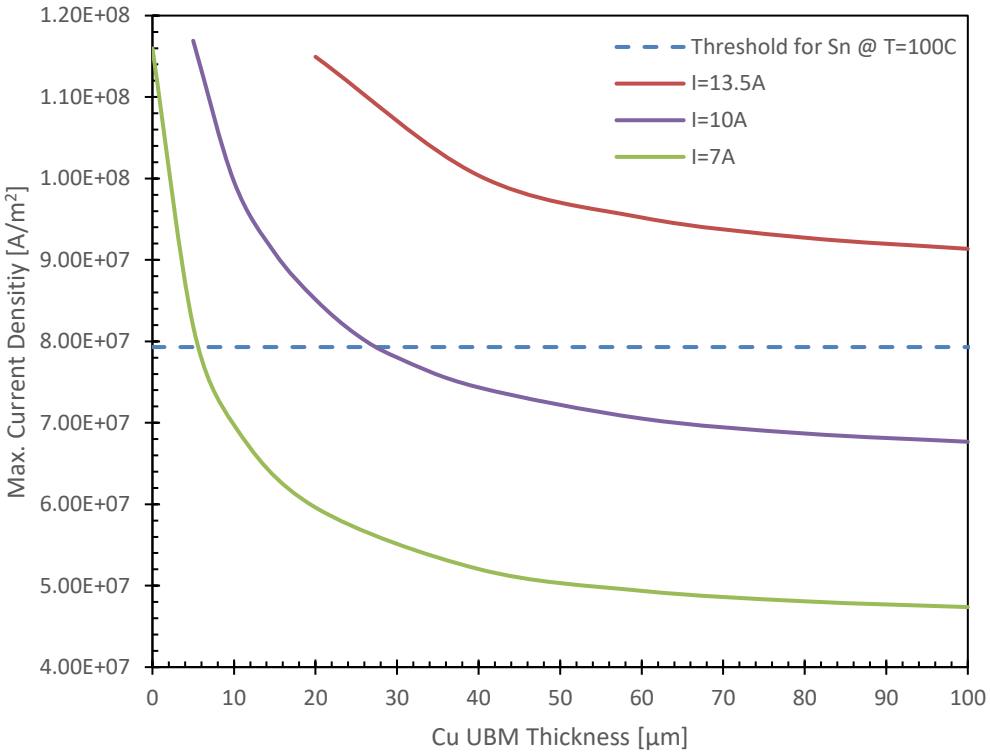


Figure 34: Maximum current densities observed at various electrical current inputs compared with the threshold value for electromigration in thin film Sn

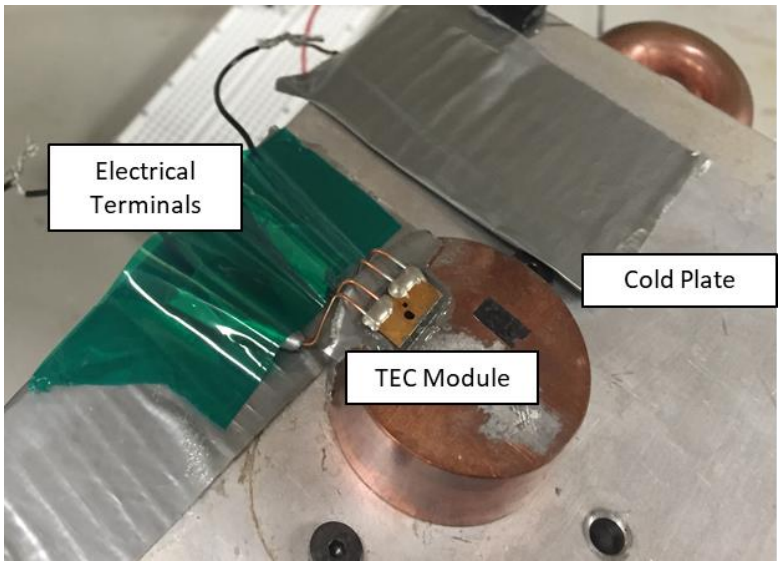


Figure 35: Experimental setup for accelerated high current stressing test

In order to experimentally investigate the possibility of electromigration, the standard geometry (without Cu UBM) modules from RTI/Micross was put under high-current stress tests for 12, 24 and 36 hours, where the current densities were roughly 5 times the expected ICECool structure current density. The experimental setup is shown in Figure 35. As can be seen from Figure 36, there was no visible degradation in the device-level performance due to electromigration or for any other failure mechanism that could take place. These results demonstrate that even without any Cu UBM it is unlikely that electromigration will be an issue, especially if we are operating at the minimum required current (7A) instead of the optimum current (13.5A).

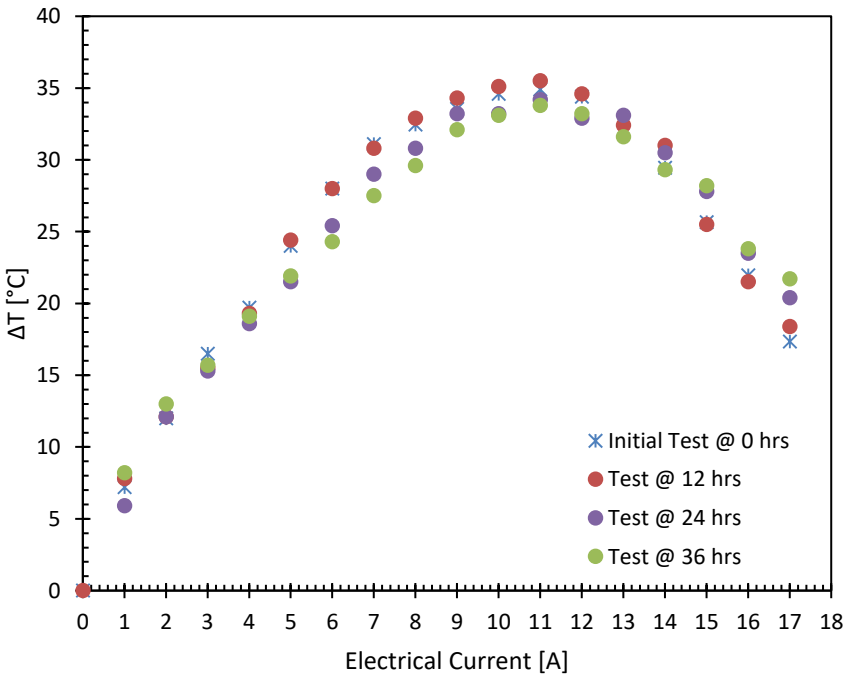


Figure 36: Results of high-current stress tests at 12, 24 and 36 hours

2.6 TEC Fabrication

The fabrication of the TFTEC module for ICECool project sub-contracted and was assigned to RTI (and subsequently Micross AIT. to design a thermoelectric module that fits the specification called for in the final deliverable. This involved several iterations of design structures, followed by modeling at UMD (with assistance from RTI) to determine whether the design would provide the necessary performance metrics.

One of the primary challenges of this design was the constraint that current needed to travel top-to-bottom through the device, as opposed to the standard "Stonehenge" configuration in which both current leads are on the bottom of the device. Such a top-to-bottom current-flow device has not been previously reported.

2.6.1 Prototype Layout

This section discusses the improved design of the TEC after constant communication with the subcontractor RTI on their capabilities of the module. In order to enable a top-to-bottom current-flow configuration, an odd number of TE elements are necessary. As discussed in a previous section, various modeling iterations led to the choice of a 6p/5n design, meaning there are six p-type elements and five n-type elements. A TEC with such an "unbalanced" element design has not previously been reported either. Based on these constraints and UMD's modeling, a schematic of the module design was produced as shown in Figure 37.

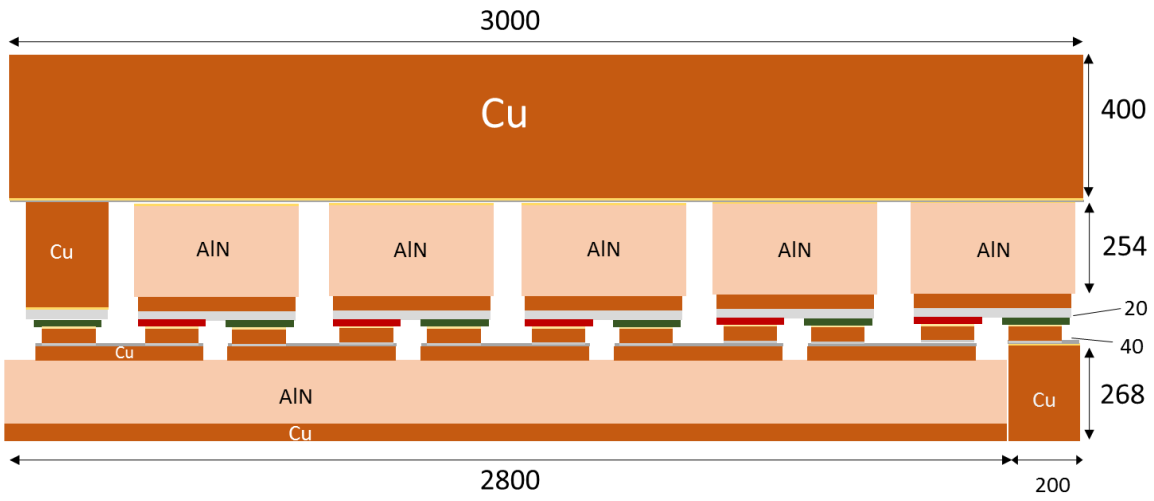


Figure 37: Schematic of the TE module design for the ICECool project. All dimensions are in µm [43]

The dark green rectangles represent p-type TE material, while the red rectangles represent n-type. The structure is 800 µm deep into the plane of the page. This innovative TEC structure can provide the performance needed in the ICECool project, but is an extremely challenging design due to new geometries, tight tolerances, the requirement of bonding of TE directly to metal, and the aforementioned top-to-bottom current path.

To build this TEC prototype, several individual components needed to be manufactured and subsequently bonded together. The AlN based bottom header was straightforward to fabricate. However, several challenges were met in the fabrication of the Cu header which bonds to the final p-type leg, as shown in the lower right of the Figure 37. The specific problems with this part were both the dimensions and the material. Due to the soft nature of the material, RTI was unable to successfully dice the In-plated copper into useable headers. Many engineering solutions were tested (pre-bonding the Cu to rigid AlN, repetitive shallow cuts, hand-separating shallow cut pieces) but none were successful;

and thus we were unable to provide parts that were usable in the module as designed. For this reason, the modules delivered from RTI to UMD did not have a bottom header connected to the far-right p-type element.

The Cu based bottom header relatively straightforward to fabricate. The bowing problems RTI experience before with their Cu bottom header were once again present in this configuration as well. However, due to the larger size of the piece, this bowing was more manageable.

The AlN-based TE die were fabricated using a Sn-bonding technique that RTI has used successfully on their previous DARPA programs. This process had to be modified to fabricate the Cu-based single-element die. These single-element die were very sensitive to bending during processing due to the ductility of Cu, and once again dicing presented significant difficulties. Despite these challenges, RTI/Micross was able to successfully fabricate enough single-element die to build some full-scale modules, however it could not be assembled to the rest of the module as will be discussed.

2.6.2 TE Material Growth

The thin-film materials used as the active material in the die were a p-type 10Å/50Å Bi_2Te_3/Sb_2Te_3 superlattice, and an n-type δ-doped $Bi_2Te_{3-x}Se_x$ alloy. Both materials were grown heteroepitaxially using an MOCVD reactor. The approximate growth rate was 0.3 nm/sec. Thickness of the films was determined via cross-section SEM analysis.

The n-type δ-doped structure was grown by periodically interrupting the growth of $Bi_2Te_{3-x}Se_x$ and dosing the flow with Te and Se species. These growth interruptions were performed at 12-second intervals, and each interruption lasted 1.5 seconds. This δ-doping process was shown to result in an increase in carrier concentration without a reduction in electron mobility. Additionally, this process has been shown to lead to higher values of the thermoelectric figure of merit, ZT, and better cooling as compared to the standard $Bi_2Te_{3-x}Se_x$ structures.

Organometallic trimethylbismuth, diisopropyltellurim, and trisdimethylaminoantimony were used as the Bi, Te, and Sb sources, respectively, and gaseous hydrogen selenide was used as the Se source. Growth temperature for these materials ranged from 375°C to 425°C. The materials were grown heteroepitaxially on semi-insulating (100) GaAs substrates off-cut by 2°. GaAs was chosen as the substrate material due to its low cost, relatively low lattice mismatch with bismuth telluride (3.9%), and ease of etching (using 3:1 H_2O_2:NH_4OH).

Once all the components of the module were fabricated, attention was turned toward the module builds. ZT measurements were taken of a representative set of die which were to be used in the module, and these results are provided in Figure 38.

706C	As measured			Gain correction		
Die #	VT	V0	VR	V0	VR	ZT
1	--	--	--	--	--	--
2	20.6	6.0	14.6	52.2	127.0	0.41
3	17.4	6.0	11.4	52.2	99.1	0.53
4	17.8	5.6	12.2	48.7	106.1	0.46
5	17.8	6.8	11.0	59.1	95.7	0.62
6	19.0	6.0	13.0	52.2	113.0	0.46
7	19.2	5.6	13.6	48.7	118.3	0.41
8	20.2	5.8	14.4	50.4	125.2	0.40
9	--	--	--	--	--	--
10	18.4	6.8	11.6	59.1	100.9	0.59
11	18.6	5.8	12.8	50.4	111.3	0.45
12	23.0	8.0	15.0	69.6	130.4	0.53
13	29.8	7.8	22.0	67.8	191.3	0.35
14	20.4	6.6	13.8	57.4	120.0	0.48
15	20.8	6.8	14.0	59.1	121.7	0.49
16	20.4	6.8	13.6	59.1	118.3	0.50
17	20.4	7.2	13.2	62.6	114.8	0.55
18	8.8	1.4	7.4	12.2	64.3	0.19

Figure 38: ZT values of the TE die to be used in the module build, measured via the Harman technique [43]

Based on die-level ZT values, a module level ZT of 0.40 - 0.45 is estimated. This ZT would correspond to a ΔT_{max} value of 40 - 45K. Heat pumping is more difficult to predict because of the novel geometry used; however, Q_{max} ~ 125 W/cm^2 would be expected at T=298K, where as it is expected to rise up to 230-250W/cm^2 at the saturation temperature of the coolant fluid, which is assumed as 110°C(383K) in the analysis section.

2.6.3 Prototype Builds

There was a total of five progressive prototypes built in this project. The purpose and take away from each are described below.

Figure 39: ICECool module-1 [43]

For the first prototype the goal was to test the bonding of four AlN-based TE die to both the AlN bottom header and the Cu top header. No p-type-on-metal element was used, nor was attachment to the far-right metal header. Alternatively, Ag wires were attached for potential device testing. This module is presented in Figure 39.

Some cupping was observed in the top Cu header, as a result of dicing the soft Cu. More problematically, electrical testing showed that this prototype is an open circuit. Moreover, flux cleaning issues left a heavy residue in the module which prevented further inspection and/or characterization.

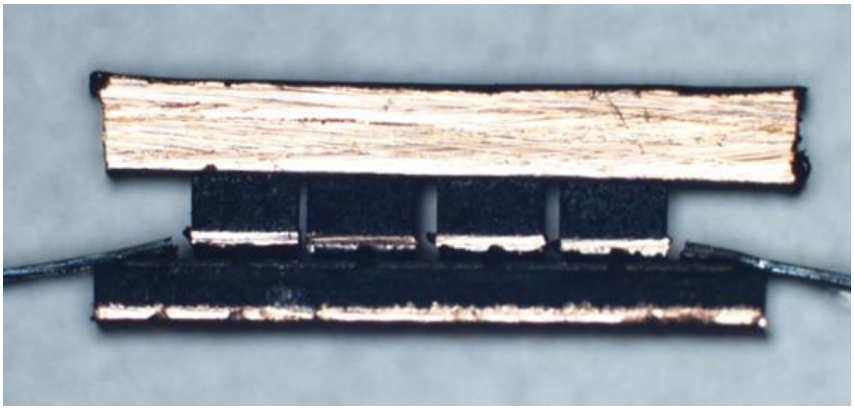


Figure 40: ICECool module-2[43]

The second prototype mimicked the first in that it was a 4p/4n structure with no p-type-on-metal element, but with Ag wires attached for potential electrical testing. It is shown in Figure 40. Microscopy revealed that the flux cleaning problem had been resolved; however, the module had a very high resistance. The microscopy seemed to indicate that the die were bonded well, but wire contacts to the module were poor, which likely led to the high resistance in the overall module. The results indicated that it was necessary to abandon the Ag wire process and instead incorporate the p-only element in all future builds.

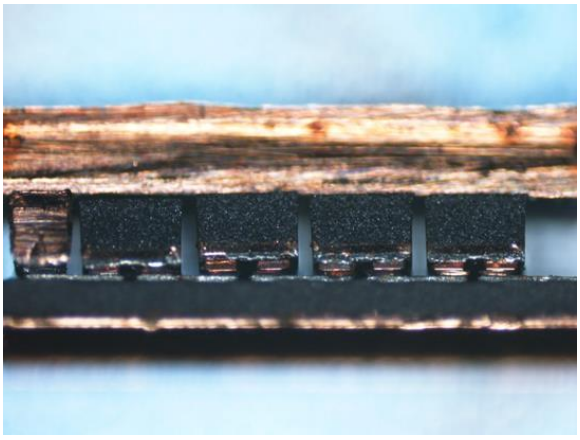


Figure 41: ICECool module-3 [43]

The third prototype shown in Figure 41 was the 5p/4n module which was the first to incorporate the p-only element. No attempt was made to provide an electrical connection to the bottom of the module; thus this sample was built for optical inspection only. Electrical connections looked intact and the module was once again free of flux residue. This sample was sent to UMD for inspection.

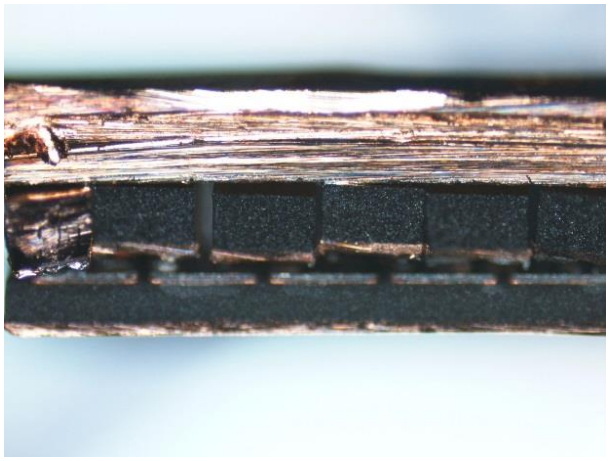


Figure 42: ICECool module-4 [43]

The fourth prototype shown in Figure 42 was the first attempt at a full 6p/5n sample, but there were severe alignment issues. A second attempt at the 6p/5n was necessary. This module was received for potential use as a mechanical sample.

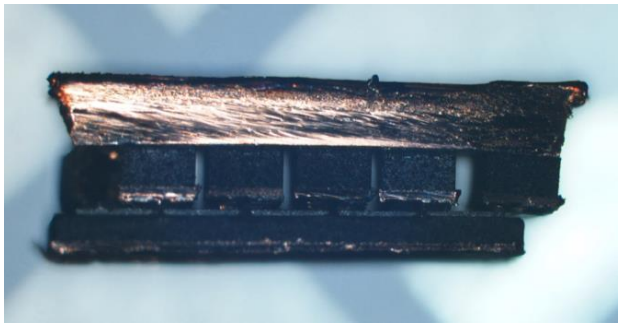


Figure 43: ICECool module-5 [43]

The fifth prototype shown in Figure 43 was a repeated attempt at a full 6p/5n sample. This module showed marked improvement over module 4, but tolerances were not within the tight specifications necessary for integration. Additionally, there was no electrical connection to the far-right p-type leg due to the challenges in building the small Cu bottom header, as discussed previously.

Unfortunately, due to the difficulties inherent in the fabrication of the desired module—specifically the small copper contact to connect the far-right p-type element to the bottom current lead—as well as the tight tolerances that were called for in the module, we were unable to fabricate a fully functional TEC for integration.

2.7 Alternative Design for Future Work

The difficulties of manufacturing the bottom-to-top TEC module has encouraged for a different design that would simplify the electrical current path for easier manufacturing in similar project in the future. A novel approach was developed to enable the typical Stonehenge structure for the TEC while making the wiring of the module much easier. The approach is presented in Figure 44 and Figure 45 below.

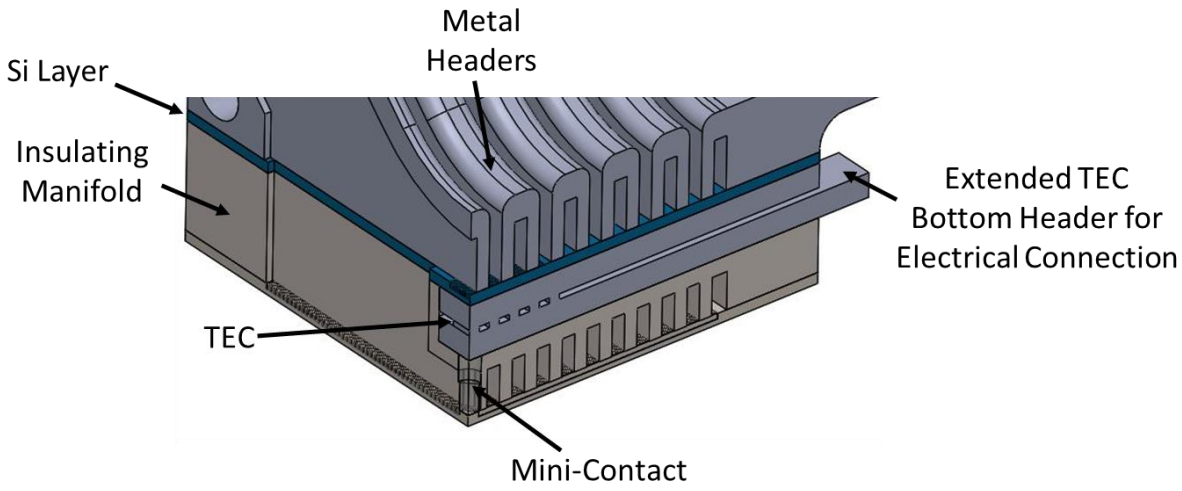


Figure 44: Cross-sectioned 3D CAD view of the new integration approach

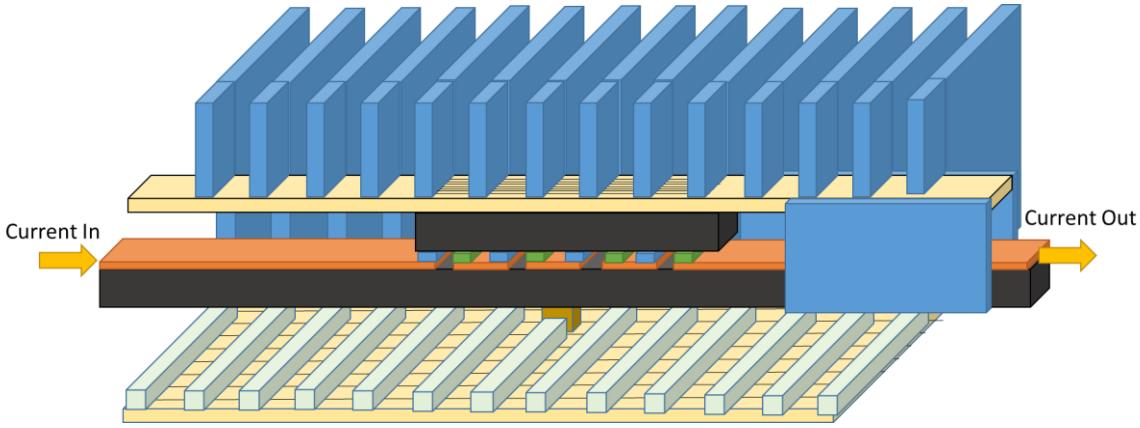
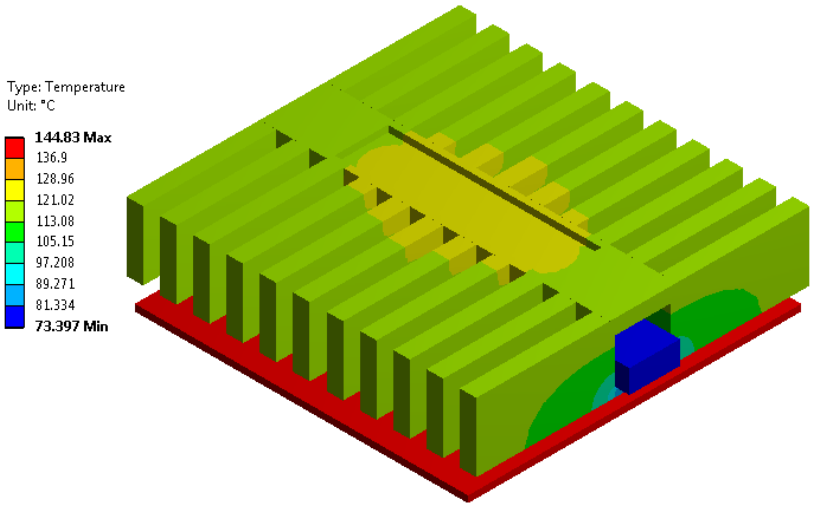


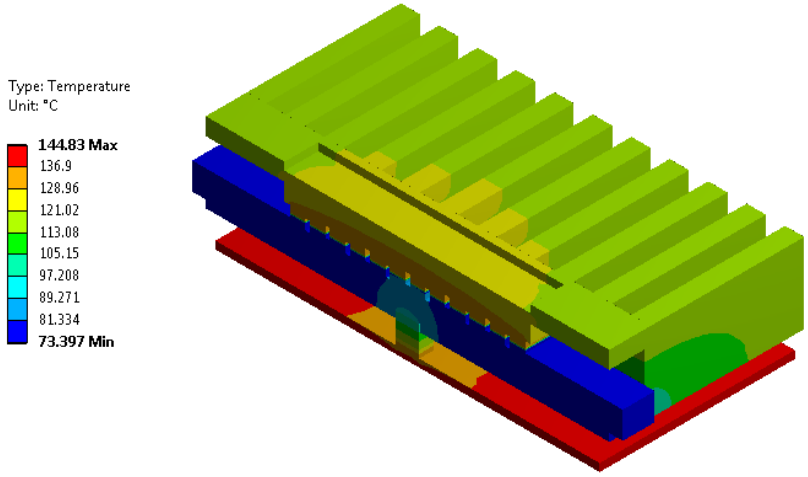
Figure 45: Schematic representation of the new approach

In such configuration, the TEC is elongated and the two terminals stick out from the outer wall of the manifold structure. This architecture not only allows the TEC to be in the typical configuration, but also allows eliminating the mid manifold and the Cu traces to be deposited on top and bottom for electrical connection. This would increase the overall integration reliability and also provide easier fabrication of the manifold. The only drawback of this approach is that the elongated TEC module spans more footprint thus disturbs the flow more than the original approach. However, it was found in single phase CFD simulations that as long as the TEC is not wide but long, the disturbance is minimum and the additional disturbance due to elongated structure is not significant.

The proposed approach is modeled in Ansys-Workbench as can be seen in Figure 46. 4 different cases are investigated, glass manifold, maraging steel manifold, copper minicontact and diamond minicontact. The results of these 4 cases are presented in Table 4, which shows that the approach can be utilized in the future and is promising.



a)



b)

Figure 46: Results for maraging steel manifold and copper minicontact at I=12A; a) full 3D view b) cross sectioned view

Table 4: Hotspot temperatures for various materials

Manifold Material	Mini-Contact Material	Min. Current to Achieve the Hotspot Metric(145°C) [A]	Hotspot Temperature at Optimum Current [°C]
Maraging Steel (k=12W/mK)	Copper (k=400W/mK)	12	144.62 @I=14A
Maraging Steel (k=12W/mK)	Diamond (k=1000W/mK)	6.5	141.20 @I=14A
Glass (k=1W/mK)	Copper (k=400W/mK)	8	142.44 @I=14.5A
Glass (k=1W/mK)	Diamond (k=1000W/mK)	5.5	138.88 @I=14.5A

2.8 Conclusions

A novel cooling approach was presented to address the non-uniform high heat fluxes dissipated by today's power electronics, where the operating temperature is typically limited at around 150°C. The cooling mechanism involves integrating a thermoelectric cooler into a manifold microchannel system to cool 1 kW/cm^2 global surface and 5kW/cm^2 hotspot heat fluxes as uniformly as possible. The saturation temperature of the fluid is assumed to be 110°C, which reflects the boiling temperature of pressurized water. This temperature, of course, is relevant to power electronics and for different types of coolants can be used for applications other than power electronics. The main components in the integration structure were modeled in ANSYS-Workbench and numerically optimized. Possible challenges such as electrical wiring of the TEC, thermal short-circuiting through the manifold walls and hermetic sealing of the TEC module from the surrounding system were addressed. Relying on the experimentally obtained heat pump curves, important parameters such as contact resistances and material properties of the thermoelectric element were successfully determined. The inner structure of the TEC was optimized considering a number of design variables such as quantity of TE elements, element width, corresponding optimum thickness and electrical currents. Important system level structural parameters are also investigated and their size was optimized to minimize the hotspot temperature rise. As a result, with 30 °C temperature rise at the background surface, less than 35 °C of hotspot temperature rise with respect to the coolant fluid temperature (110°C) was numerically demonstrated. Moreover, to circumvent the electromigration issues raised by the sponsor, an accelerated test was performed on the standard RTI module, and the results show no visible degradation. To mitigate any possible future electromigration

concerns, a well proven Cu UBM approach was discussed and applied to the ICECool TEC structure.

Finally, challenges in building a TEC in a top-to-bottom current-flow configuration is discussed. Unfortunately, due to the difficulties inherent in the fabrication of the desired module as well as the tight tolerances, RTI/Micross was unable to fabricate a fully functional TEC for integration. However, as mentioned previously, manufacture of such TEC has never been reported, and the work done by RTI/Micross in this project has made progress in making such a device viable in the near future.

3 Thermal De-coupling of Optical Arrays Using a Thermoelectric Cooler

3.1 Introduction

The purpose of this project is to thermally-decouple electronic components with different operational temperature using a thermoelectric cooler. While electronic dies can operate at temperatures up to 105°C, PD/VCSEL optical array usually operate at temperatures below 85°C. One solution is to overcool the case lid down to approximately 65°C such that electronic dies are cooled down to 80°C, and the PD/VCSEL arrays are operating at 85°C, which is within their range. Another approach is to place a thermoelectric cooler between the electronic die and the PD/VCSEL array in order to decouple their temperatures. Doing so would allow the case lid to operate at 90°C, while still operating below the thermal ceiling. The VCSEL and PD arrays each are 3mmx3.5mm, and they dissipate 1.6W and 0.32W respectively, whereas the electronic die has a footprint of 21mmx21mm and dissipates a total of 100W heat.

3.2 Evaluation of packaging schemes

3.2.1 Option-1

In the first concept shown in Figure 47, a thermoelectric cooler is placed between the PD/VCSEL arrays and the interposer. The thermoelectric cooler has electric vias arranged around the perimeter to power the PD/VCSEL array.

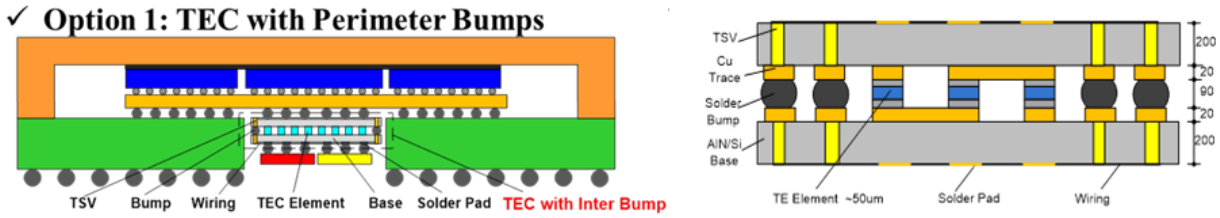


Figure 47: Concept-1 [44].

The biggest concern with this concept is managing the thermal short-circuiting that would occur through the electric vias placed on the perimeter of the TE device. Due to the high thermal conductivity of the solder, the hot-side of the thermoelectric device will conduct heat back to the cold-side, thereby reducing the net cooling effect. To evaluate this effect, a device-level model was created and is shown in Figure 48.

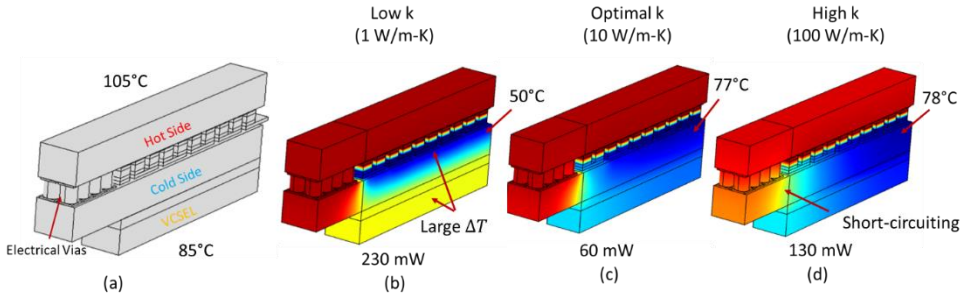


Figure 48: (a) Concept 1 device-level model (b) results for low k (c) optimal k, and (d) high k.

The thermal conductivity of the cold-side header was varied using the model. The results indicate that an optimal cold-side header thermal conductivity exists. For high values of thermal conductivity (see Figure 48(d)), a large amount of thermal short circuiting occurs, increasing the required thermoelectric power consumption. For low values of thermal conductivity (see Figure 48(b)), a large temperature drop occurs in the cold-side header, which also increases thermoelectric power consumption. For a moderate value of conductivity, a minimum amount of power is required due to a reduction in thermal short circuiting without the resulting large temperature drop through the cold-side header. Accordingly, for a given thermoelectric device, an optimal cold-side thermal conductivity exists.

To get the best of both worlds, a concept involving etching thermal (and electrical) copper vias into a quartz cold-side header was conceived as shown in Figure 49. The low conductivity of the quartz would prevent thermal short circuiting and spreading to the electric vias, while the thermal vias would conduct heat from the optical arrays to the cold side of the thermoelectric device. However, when sizing the electrical leads required to carry the necessary current for the optical devices, it was discovered that the electric leads themselves will provide a significant thermal short-circuiting path, which almost doubles thermoelectric power consumption. Instead, for optimal performance, the electric vias themselves will have to be changed to minimize the thermal short-circuiting that occurs for this concept.

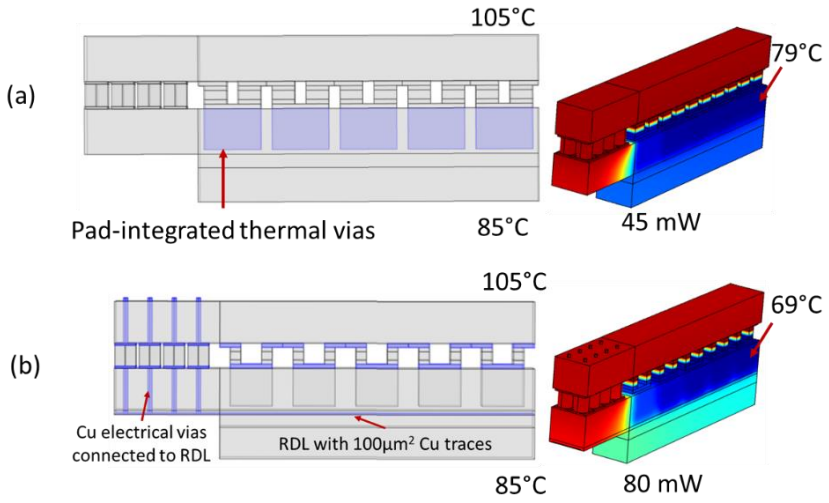


Figure 49: (a) Pad-integrated thermal vias concept (b) Pad integrated thermal vias with sized electrical traces.

3.2.2 Option-2

The second concept is similar to the first as shown in Figure 50, except the electric vias and thermoelectric elements are dispersed within each other for a more compact design.

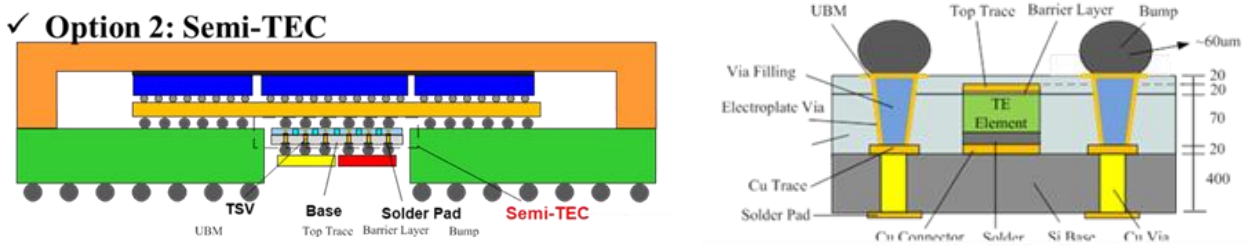


Figure 50: Concept-2 [44].

The main concern of this design, similar to the first concept, is thermal short-circuiting. A simple device-level model was created, and is shown in Figure 51. The results indicate that for a mold material thermal conductivity of 1 W/m-K, a 11K temperature rise in the cold-side can be expected for the same current and hot-side temperature. This would

therefore significantly increase the required thermoelectric power, and might reduce the system COP below the sponsor's required minimum. It is worth noting that this device-level model did not include back-conduction through the embedded electric vias, and accordingly, the cold-side temperature rise can be expected to be even worse. Thus, the third concept was evaluated.

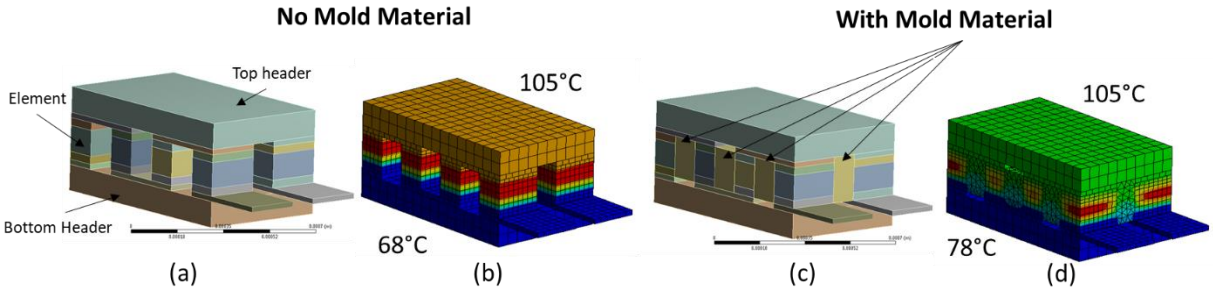


Figure 51: Concept 2 device-level model and results (a) device-level model with no mold material (b) thermal results with no mold material (c) device-level model with mold material (d) thermal results with mold material (1 W/m-K). Results are relative only.

3.2.3 Option-3

In the third concept shown in Figure 52, the thermoelectric cooler is integrated into the interposer. It is worth noting that the TEC can be partially embedded into the interposer, resulting in a fourth concept which is in between concept 1 and 3.

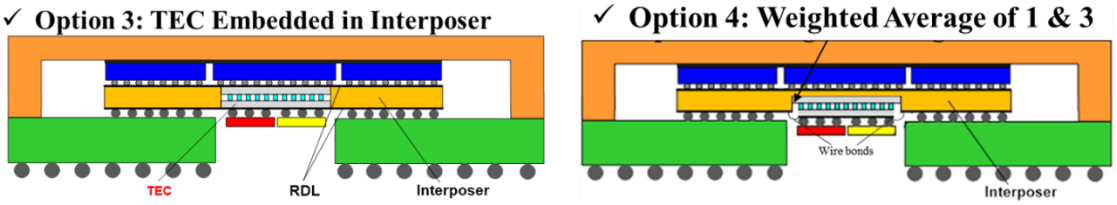


Figure 52: (a) Concept 3 (b) a new concept suggested by UMD, which is a weighted average of concept 1 and 3 [44].

Once again, the main concern here is thermal short-circuiting from the cold-side header. Since the cold-side header is connected to the interposer, and the interposer is connected to the hot-side, significant thermal short circuiting could occur if the interposer material is not sufficiently insulating. Accordingly, a device-level model was created to evaluate this effect, and is shown in Figure 53.

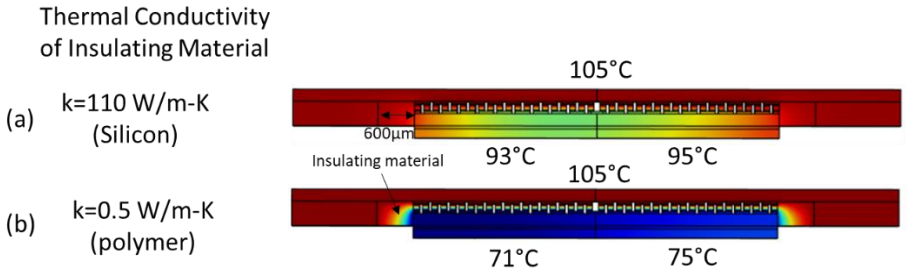


Figure 53: Concept 2 (a) silicon insulating layer i.e. no insulating layer (b) polymer insulation.

To reduce thermal short circuiting, a 600µm thick layer of insulating material is placed between the cold-side and the interposer. The thermal conductivity of the insulating material was varied from a value of 110 W/m-K i.e. silicon and the equivalent of no insulating material, to that of 0.5 W/m-K i.e. polymer. The results indicate that without an insulating layer (i.e. pure silicon), a temperature drop of 11K is achieved, whereas including a polymer insulating layer increases the temperature drop to 32K, nearly tripling the temperature drop under the same load. Accordingly, thermal short circuiting a significant concern for this concept.

There are various challenges associated with the inclusion of an insulation layer between the cold-side and the interposer. The first is the challenge associated with achieving a flat and level surface, such that the electrical connections between the PD/VCSEL arrays and the interposer can be made. However, even if these connections

could be made, one possible concern is that thermal expansion of the polymer would stretch and break the electrical connections. One possible fix is using wire bonds instead of an insulating material. However, due to the limited working area, wire bonds might not be possible.

3.3 System Level Modeling and Optimization

To achieve the optimum cooling for both PD and VCSEL arrays, a numerical model is created with a TEC module placed on the interposer, as can be seen in Figure 54. The TE element thickness is varied from 100 to 300 μm, for both Bi_2Te_3 bump and Sn bump cases. Heat flux from the heat source was 9.5W/cm^2 and the electronic die dissipates 22.7W/cm^2 to the copper lid underneath, which has a fixed temperature boundary condition at T_{lid}=90°C.

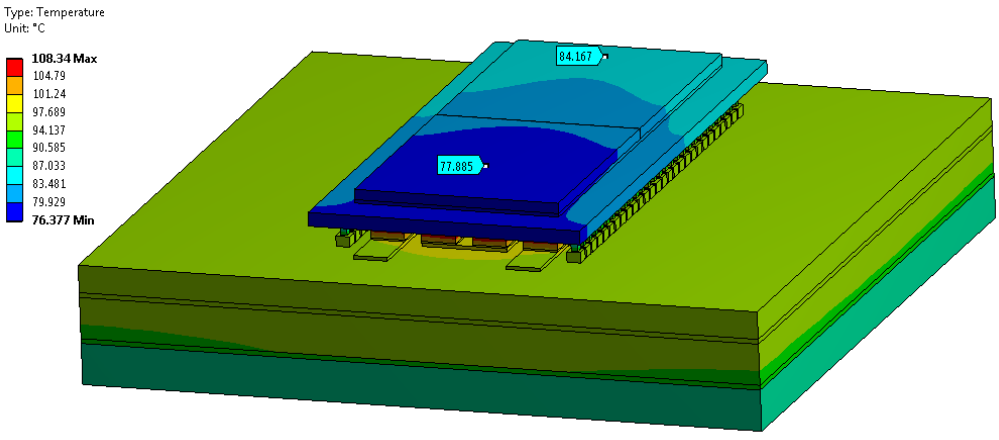


Figure 54: Numerical model for TE thickness optimization

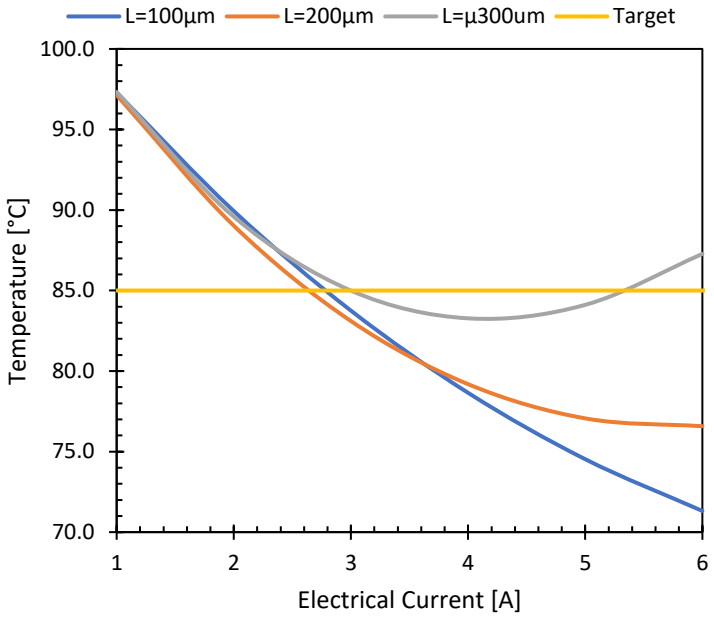


Figure 55: Source temperature as a function of current for the structure with Sn Bumps at various thicknesses

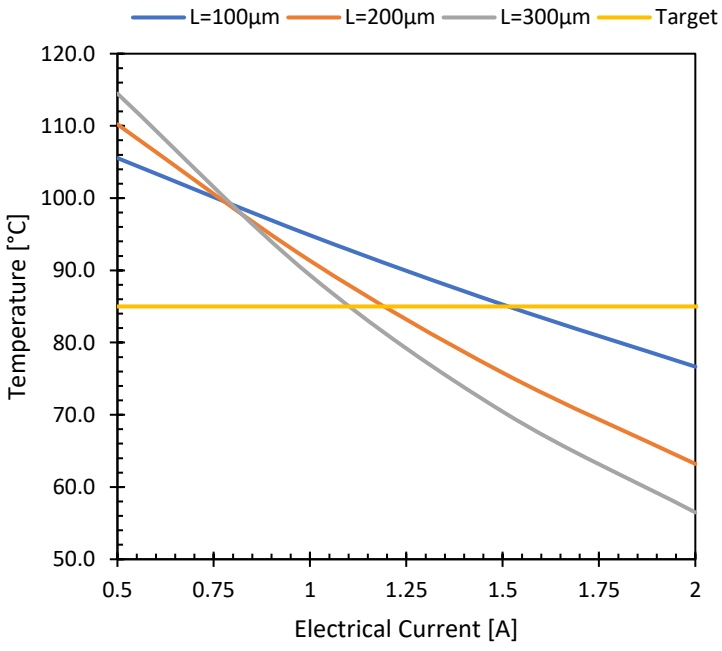


Figure 56: Source temperature as a function of current for the structure with Bi_2Te_3 Bumps at various thicknesses

As it can be seen from the Figure 55 and Figure 56, the optimum thickness and current depends on how much back conduction occurs in the system. If the perimeter bumps can be made out of Bi_2Te_3 material, the optimum thickness is 300 microns and the required electrical current input is about 1.2A, which is desirable so that the joule heating at the external leads are minimized. Whereas if the bumps are made out of Sn, there will be larger back conduction, thus the effective heat flux pumped by the TE elements are significantly increased. Expectedly at such scenario, the optimum thickness has to be smaller to achieve larger fluxes, while the larger electrical current input is required to hit the target temperatures for both VCSEL and PD arrays, as can be seen in Figure 53. However, considering the fact that it is still doable with the Sn perimeter bumps is encouraging.

3.4 Experimentation

3.4.1 Device Level Characterization

For the phase 1 design, a commercially available bulk TEC (See Figure 57(b)) is used to demonstrate the approach and prove its viability. In the configuration shown in Figure 57(a), the TEC module is placed on a ceramic heater that acts as the electronic die in the actual system. The temperature of the ceramic heater's bottom surface is controlled using a chiller. Since the module is not a custom design, the perimeter bumps (whether Sn or Bi_2Te_3) will not exist within the structure. Therefore, to mimic the effect of back conduction, Cu wire bonds are placed between the cold side of the TEC and the upper surface of the ceramic heater. And the heat flux coming from the PD+VCSEL arrays is generated by the laser (later by the platinum heater is deposited on the cold side).

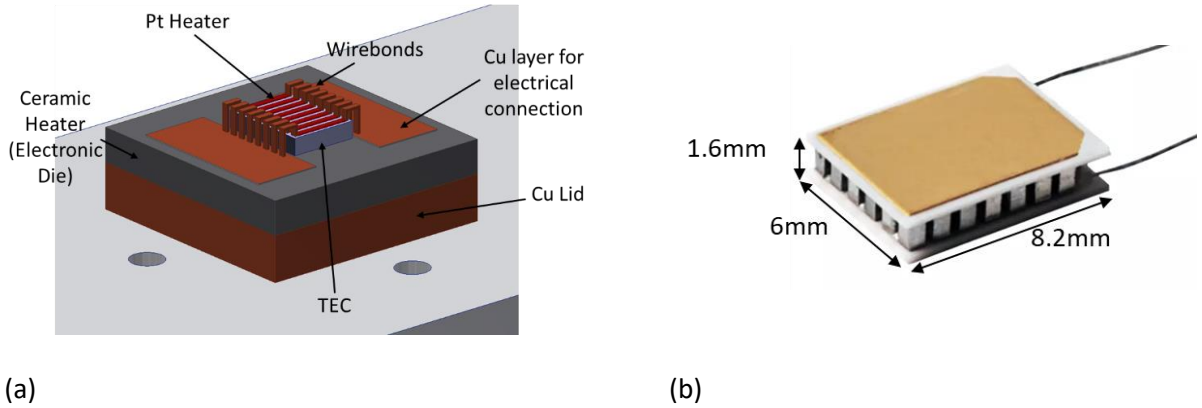


Figure 57: (a) The phase 1 configuration (b) Marlow TEC module "CM23-1.9"[45].

The acquired TEC is experimentally characterized to determine the cooling performance curves and the optimal operating electrical current. The experimentally obtained performance curves are then matched with simulations for further system-level analysis. The hot side of the module was kept at 85°C (the highest chiller temperature) and heat was applied on the cold side using the laser. The cu spreader on the cold side of the module spreads the heat evenly and the temperatures are recorded using IR camera. The results indicate that the maximum cooling is achieved at 2 Amps as can be seen in Figure 58 and the highest heat load at 2A is roughly 3.5W as represented in Figure 59.

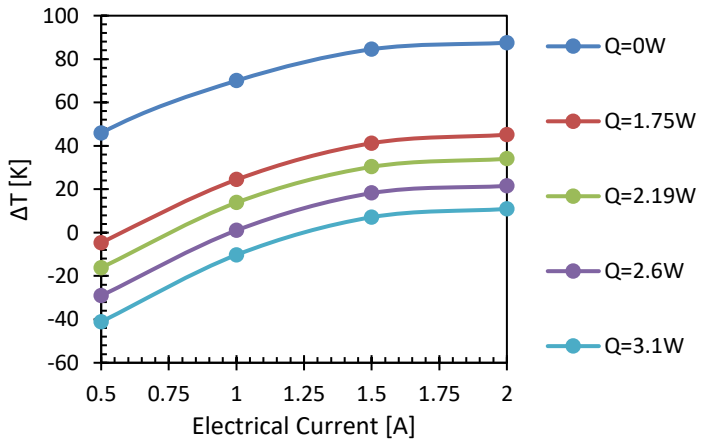


Figure 58: Optimum current test results at various heat flows

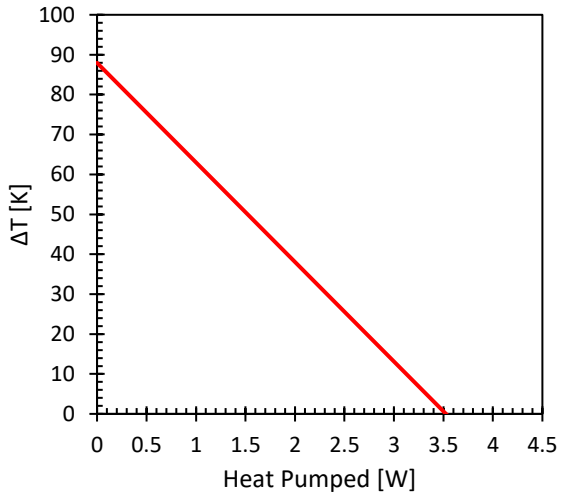


Figure 59: Heat pump characterization at I=2A.

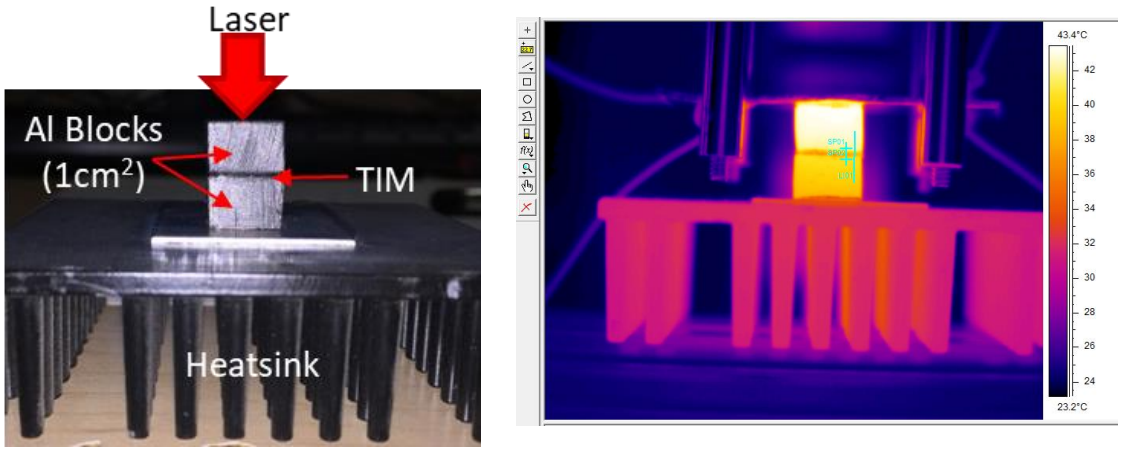
The overall uncertainty in the laser/IR camera experimental setup is shown in the Table 5.

Table 5: Uncertainty analysis for the experimental setup

Laser Power:	**Uncertainty**
Power Detector[66]	+/- 5% of reading
Laser Stability[67]	+/- 2% of reading
Calibration Curve Fit	+/- 0.1%
Total Power Unvertainty	+/- 5.57%
Temperature:	**Uncertainty**
Infrared Camera[68]	+/- 1K

3.4.2 System Level Thermal Resistance Investigation

In the actual system, the TEC will be bonded to the Electronic die with Sn bumps. Meaning that the effective conductivity of the layer will be lower than the bulk Sn. In order to mimic that, they are bonded using thermal interface materials in the experiments. However' there is still need to determine how much resistance will occur in this junction. To determine the areal thermal resistance between the TEC and Ceramic heater, two identical aluminum blocks (1cmx1cm) are bonded to each other using two different TIM materials with and without pressure as shown in Figure 60. Laser is used to heat the samples and the temperature distribution along the components is observed via thermal camera. It is important to know the exact heat flux absorbed by the aluminum block, therefore the blocks are coated in high emissivity graphite (emissivity=0.9) and the laser power is measured using the power meter with 5% uncertainty.



a) b)

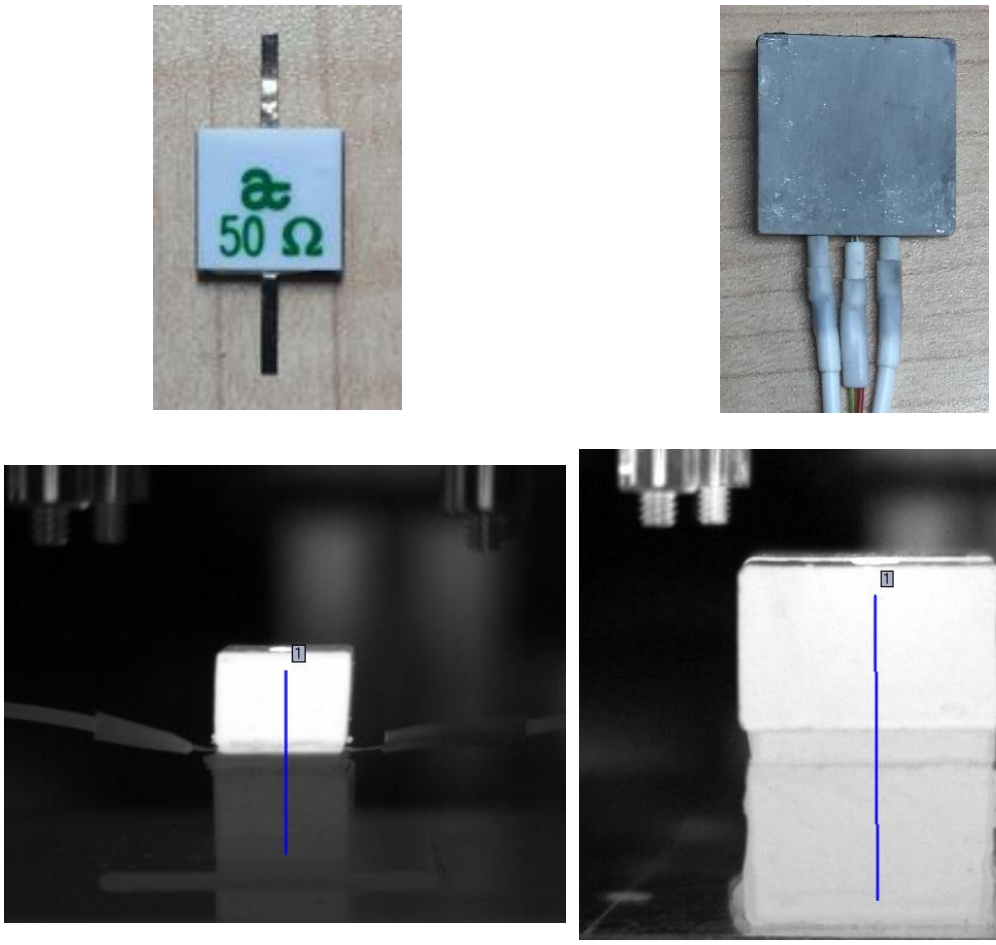
Figure 60: (a) Experimental setup (b) IR camera results

Table 6: TIM resistance results

Assembly Type	Applied Compression Force (lbs.)	Resistance of the Interface (mm^2K/W)
No TIM	0	1630
No TIM	5	496
Arctic Silver 5	0	83
Arctic Silver 5	5	24
Shin-Etsu	0	33

As it can be seen in the Table 6, Arctic silver-5 cannot provide sufficient conductance unless it is under pressure. Shin-Etsu on the other hand, has shown $33mm^2K/W$ thermal resistance even without any pressure. Therefore, Shin-Etsu material is used in the further experimental analysis.

In order to be able to bring the hot side temperature down, a more conductive heater was required. Therefore, a new heater was acquired from Watlow, which is 19x19mm in size. Both heaters were tested to obtain and compare their thermal resistances. A $0.8W/cm^2$ heat flux was applied on them using the laser and the temperature drops are recorded. As can be seen in Figure 61, the temperature drop across the Watlow heater is around 1K, whereas the Atceramics heater has 9.5K temperature drop. This clearly indicated that the smaller heater had very high internal resistance and cannot be utilized for further analysis. Thus, the following system level experimentation was conducted using the19mmx19mm heater from Watlow.



a) b)

Figure 61: Thermal resistance test for the smaller and larger heater used in the system level experiments

3.4.3 System Level Experiments without Wire Bonds

The configuration of the preliminary system level experiment is shown in Figure 62-a. The Cu spreader placed on the TEC module represents the combined PD+VCSEL arrays. The TEC is then placed on a ceramic heater that represents the electronic die, which is placed on the cold plate as can be seen in Figure 62-b.

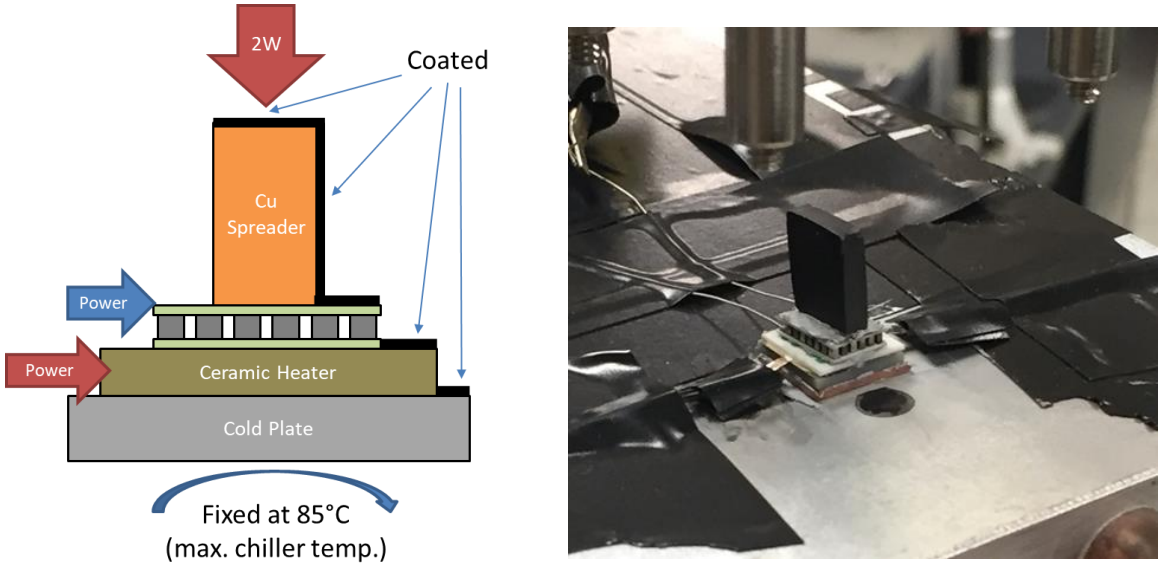


Figure 62: (a) System level schematic (b) System level experimental setup.

The initial tests were conducted using a 50 Ω resistor heater from Atceramics that is 10x10 mm in footprint. The resulting temperatures were a lot higher than expected, such as the junction between the TEC and the ceramic heater was above 130°C as shown in Figure 63. This is a result of the heater having a very low thermal conductance as discussed in the earlier section, and it is probably due to poor contact between its aluminum nitride base and the alumina cap on top. However, although the TEC hot side was 130°C instead of 105°C, the module could still cool the Cu spreader down to 85°C, which shows that the TEC is capable of operating at higher temperatures and still achieve the objectives. This

was also performed using Ansys and there is a good agreement between the results as can be seen in Figure 64.

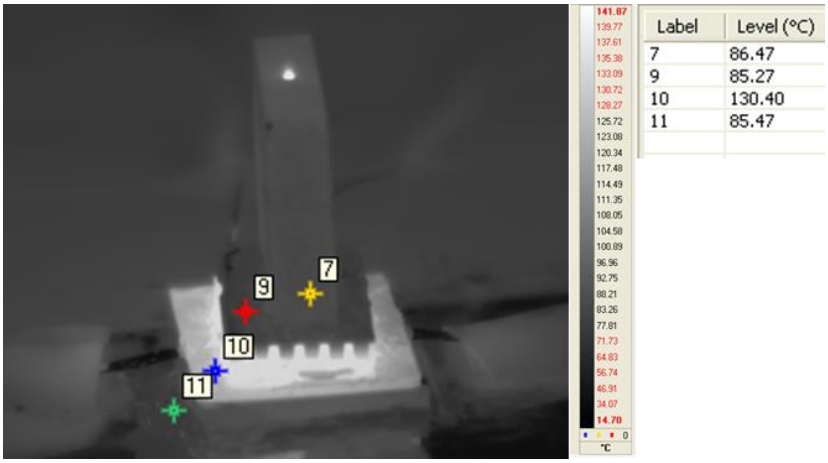


Figure 63: Experimental results of the system.

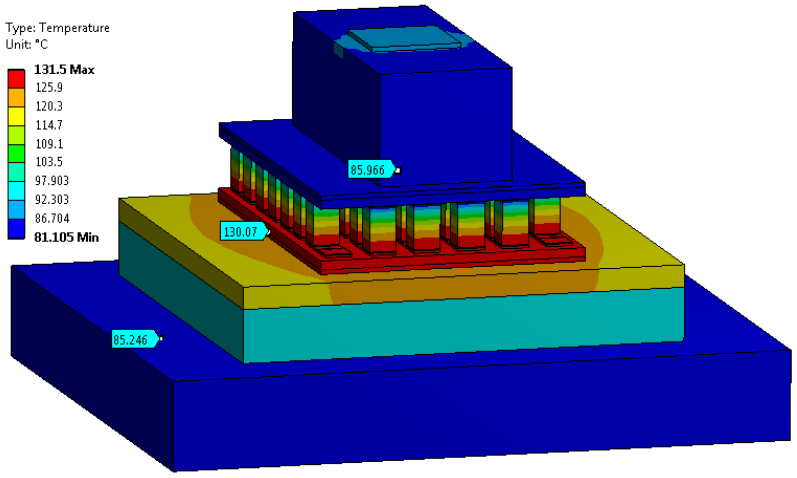


Figure 64: Numerical results of the system with the contact resistances fine-tuned.

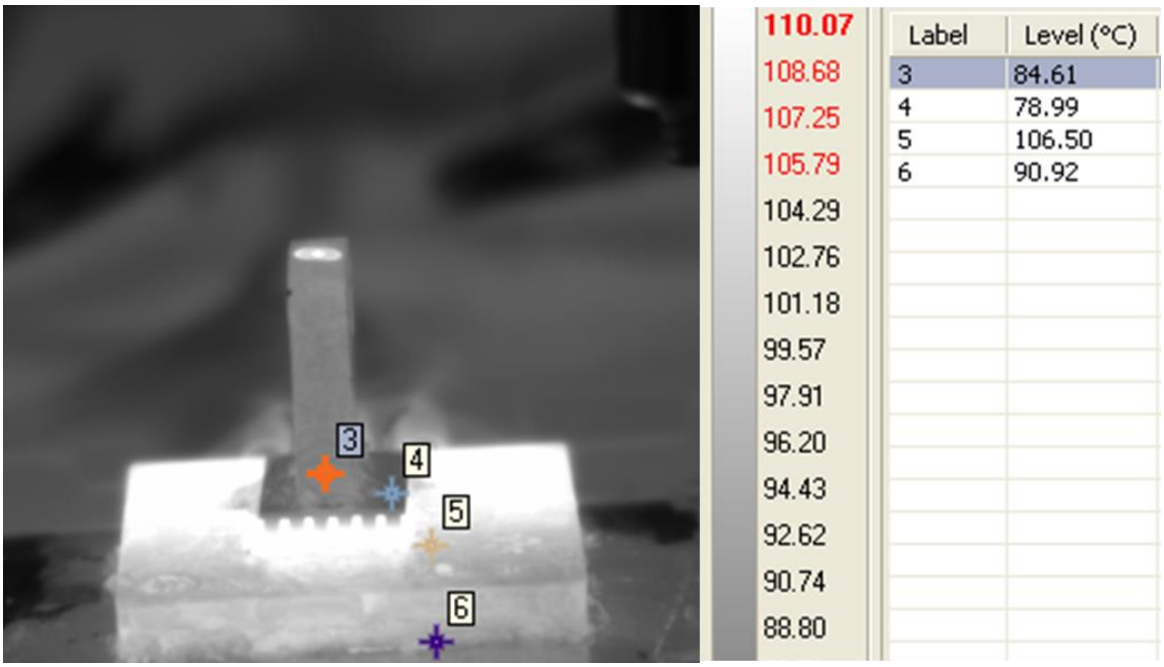
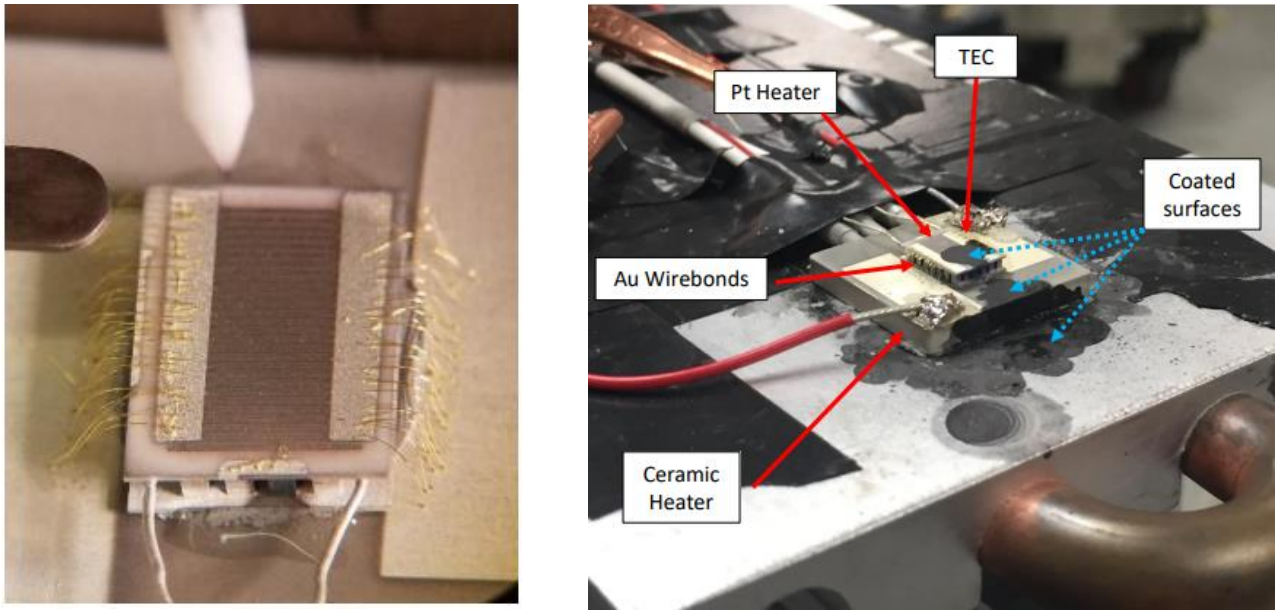


Figure 65: System level experimental result without wire bonds

As the final step in the system level experiments without wire bonds, the setup was placed on the larger (more conductive) heater and the same procedure was conducted as with the smaller heater. Since the heater is bigger in this test, the power dissipated at the heater is 81W to match the designated heat flux. The results in Figure 65 shows that the Lid temperature is 90.9°C and the module could successfully cool down 2W of heat supplied by the laser using an electrical current of 1A. The source (VCSEL and PD arrays) temperature is brought down to 84.6°C and the total energy consumed by the TEC was 2.409 Watts, which means the COP=0.83. This shows us that the approach is valid and viable.

3.4.4 System Level Experiments with Wire bonds

In order to mimic the back conduction through the Bi_2Te_3 bumps at the perimeter of the TEC, gold wire bonds are added to the system. The wire bonds were also designated to serve as electrical connections to the platinum heater deposited on the cold side of the thermoelectric cooler. The TEC was taken to the FABLAB at Univ. of Maryland and a platinum heater with various number of strips and nominal Pt thicknesses were produced as can be seen in Figure 66-a. Later on, the wire bonding machine in CALCE laboratories was utilized to make Cu wire bonds. However, due to the surface roughness and other technical issues with the wire bonding machine, the success rate was very low with Cu.



a) b)

Figure 66: a) The Pt heater and wire bonds on the TEC-Ceramic Heater assembly b) Experimental Setup for system level cooling

As a solution to this problem, gold wire bonding was performed using the utilities in FABLAB. Due to the softness of gold, it can be bonded at lower temperatures and the

success rate was close to 100%. In total, 56 ball-wedge gold wire bonds were made from the TEC cold side to the ceramic heater top surface.

It was later observed that the Pt heater had pinholes and could not be used for the wire bonded structure as the heat source. Therefore, the laser approach is again employed to create the heat flux on the TEC. The paint on the Pt heater is carefully cleaned using acetone. TIM is applied between the bare Pt heater and the Cu block, as shown in Figure 67.

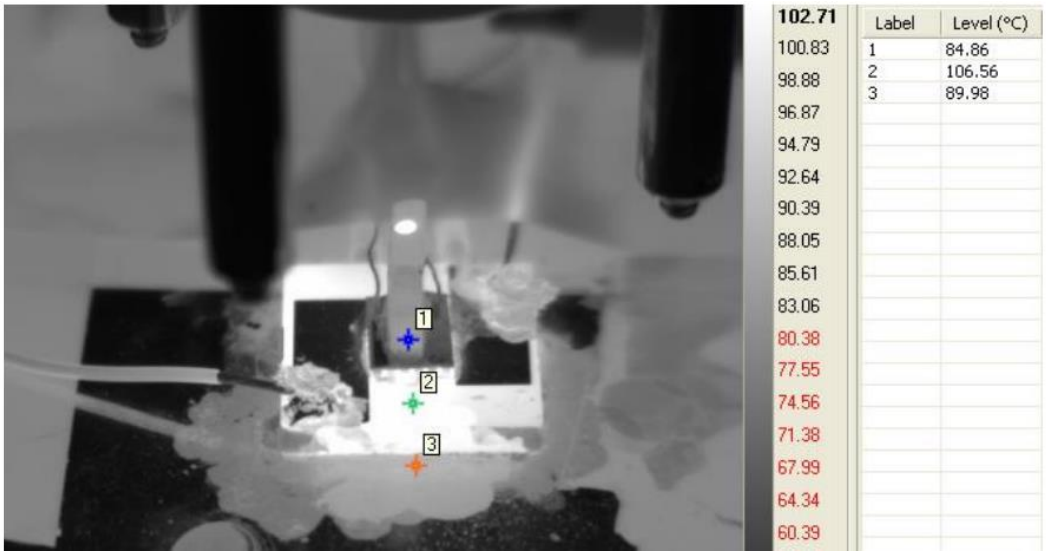
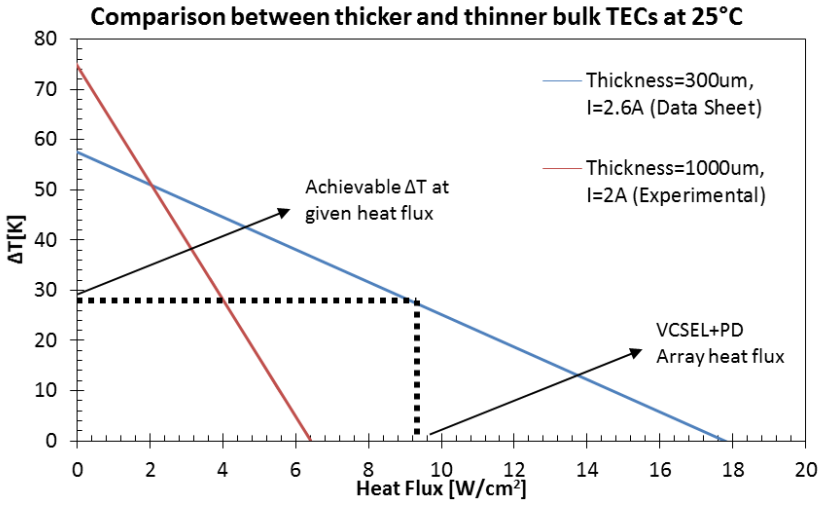


Figure 67: System level experimental result with wire bonds and using the laser heating approach

As expected, due to the presence of back conduction through the gold wires, the overall system performance was slightly reduced. The energy used by the TEC was 2.409W (COP=0.83) before the wire bonds, and it increased to 2.703W (COP=0.74). Since the project metric was COP>0.3, the results successfully satisfy the requirements.

For the second phase of the project, thinner proprietary modules from Marlow have been obtained as shown in Figure 68(a). Dimensions of the new module are much closer to the sponsor provided limitations, with a footprint of 8mmx2.8mm, and a thickness of 880 µm. The expected cooling power of the device is shown in Figure 68-b and it is capable of creating ΔT=20K at the VCSEL+PD array heat flux, which is 9.5W/cm^2. Further discussions with Marlow has revealed that they in fact can go below 100µm element thicknesses, thus the overall TEC thickness can be further reduced below 600 µm.

a)



b)

Figure 68: a) Images of the old (thicker) and new (thinner) TEC modules b) the heat flux curves comparison [46]

3.5 Conclusions

The aim of this project is to demonstrate that a thermoelectric cooler is successfully capable of de-coupling an electronic die from optical arrays found in many electronic applications. The experimental and numerical efforts for the phase 1 section of the project and preliminary predictions for the Phase-2 illustrated that, even with bulk thermoelectric coolers the goal can be achieved. The major accomplishments of the project are summarized in the Table 7 below, in which the green color denotes that the metric is satisfied and red denotes not satisfied.

Table 7: Project accomplishments at the end of phase 1

Project Metrics	Target Values	Phase-1	Phase-2
PD+VCSEL Heat Flux	9.5W/cm^2	2W (9.5W/cm^2) using Laser approach	Future work
PD+VCSEL Temperature	≤85°C	84.9°C	Future work
Electronic Die Heat Flux	22.67 W/cm^2	81W (22.5W/cm^2)	Future work
Electronic Die Temperature	≥105°C	106.6°C	Future work
TEC Footprint	8mmx4mm	8mmx6mm	8mmx2.8mm
TEC Height	≤0.6mm	1.65mm	0.6mm

4 Thermoelectric Cooling of High Power Quantum Cascade Lasers

4.1 Introduction

Thin film thermoelectric cooler are suitable for cooling of high flux electronics. One example for this can be Quantum Cascade Lasers (QCL), which can be used in military applications where high optical output is required. However the generated heat flux at their junction can easily exceed 100s of W/cm^2, which cause a significant thermal management challenge. Thin film thermoelectrics with the aid of a powerful sink side cooling, such as porous metal heat exchangers (PMHX), is a promising solution for such problem. Thus, as a part of DARPA-Matrix program, a thin film TEC is modeled and optimized to meet the requirements of the project, which is cooling of 100W (~280W/cm^2) QCL array with an ultra-thin film thermoelectric module, with the assistance of a PHMX. The state-of-the-art TFTEC modules from RTI/Micross is experimentally investigated to extract important properties, and a futuristic model of the TEC design is made in Ansys-Workbench to numerically demonstrate the outcomes of such integrated system.

4.2 Seebeck Value Measurements

The Seebeck value is one of the most important material properties in thermoelectric cooling. In terms of modeling point of view, it has to be accurately known to reflect realistic results in a thermoelectric cooling system. One way of measuring Seebeck coefficient is by externally applying heat to the device, generating certain temperature difference and measuring the voltage generated by the TE legs. However, there are difficulties in

measuring the cross plane Seebeck values in superlattice thermoelectric modules. This is mainly because the thermoelectric elements are generally below 10μm, and it is practically not possible to place thermocouples to observe the hot and cold junction temperatures.

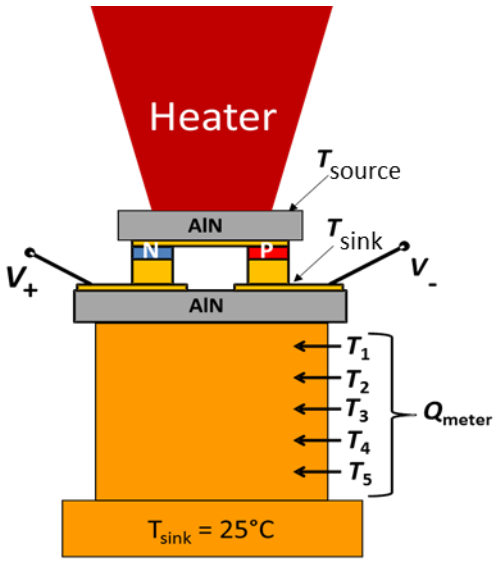


Figure 69: The schematic of the experimental setup used by RTI/ Micross [47]

RTI/Micross has attempted to measure the Seebeck value of their superlattice thermoelectric elements using the explained methodology. They measured the cold side temperature at the AlN header (source side) and measured the hot side temperature at the Cu trace on the sink side header, as seen in Figure 69. However, the calculations they performed using the measured voltage drops and temperature differences almost always led to lower than expected Seebeck values. This was so because the element level temperature drop was in fact significantly lower than the temperature drop they measured at the mentioned locations. This is caused by the thermal resistance associated with the internal layers, which are found to be comparable with the TE element leg, thus the external temperature difference ΔT_1 shown in Figure 70 cannot be assumed same as the internal temperature difference ΔT_2.

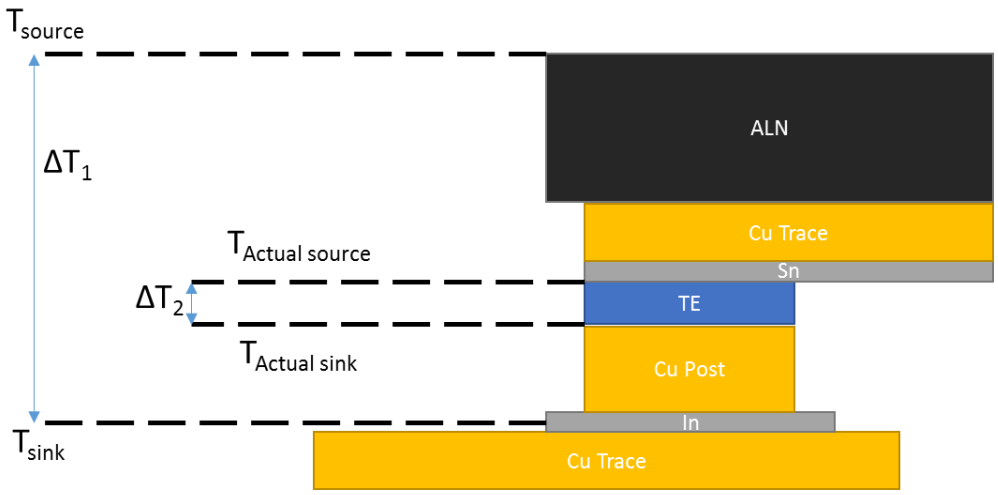


Figure 70: The actual element level ΔT and experimentally measured ΔT, denoted as ΔT_2 and ΔT_1 respectively.

To investigate the effect of the structural resistances to the discrepancy on the Seebeck values calculated using ΔT_1, a model is built in Ansys and various TE element thicknesses with different TCRs are simulated. The results are shown in Table 8.

Table 8: Numerical results for various TCR values and their corresponding module level calculated Seebeck values

TCR [m^2-K/W]	Thickness [µm]	ΔVoltage [mV]	External ΔT [°C]	Calculated Seebeck [µV/K]
10^{-6}	7	7.144	27.58	129.505
	15	14.509	45.79	158.44
10^{-7}	7	7.064	22.40	157.655
	15	14.396	40.65	177.065
10^{-8}	7	7.039	21.84	161.17
	15	14.356	40.05	179.225

As discussed, due to the small features of thin film thermoelectric coolers, it is not easy to measure the actual temperature drop across the TE elements. Thus, a method is introduces in this section to accurately calculate the cross plane Seebeck values from the

TFTEC modules. Since the external structural thermal parasitics affect the measurement due to the ΔT associated with these layers, a smart way to eliminate them is by fabricating two TFTEC modules with different TE element thickness, but same structural architecture. Given that the same heat flux is applied on these modules, the observed ΔT across them are different. This difference is solely caused by the TE elements, thus, if the observed voltages and ΔT are subtracted from each other for the two modules, the actual Seebeck value can be accurately calculated.

To demonstrate this, the Seebeck values are calculated using the external ΔT results given in Table 8. The voltage drops and temperature drops for 14 micron and 7 micron devices are subtracted from each other. Then their ratio is taken, which presents the Seebeck value for the PN couple. Dividing it into two reveals the effective ±Seebeck value for single leg. Of course this can be done using a single TE leg, which would yield more accurate results for that specific TE material, rather than an effective ±Seebeck value.

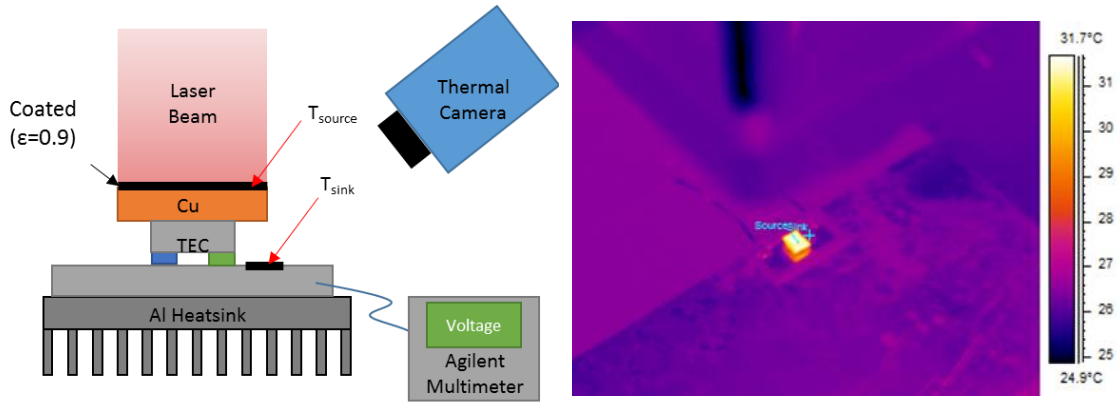
$$\text{Seebeck Coefficient} = \frac{\Delta V_{15\mu m} - \Delta V_{7\mu m}}{\Delta T_{15\mu m} - \Delta T_{7\mu m}} \tag{4.2.1}$$

$$= 1/2 \times \frac{14.356mV - 7.039mV}{40.05℃ - 21.84℃} \tag{4.2.2}$$

$$= \frac{1}{2} \times \frac{0.4017\ \text{mV}}{\text{K}} = 200.8\ \mu\text{V/K} \tag{4.2.3}$$

Which is the exact Seebeck Value used in the simulation for generating the values in the Table 8. This shows that the method is valid and can be used to determine the actual Seebeck values experimentally. Consequently, two modules with the same structural architecture are fabricated at RTI/micros and same amount of heat is applied on the modules using a laser, as shown in Figure 71. The generated ΔT is observed using an IR

camera and a multimeter is used to created voltage drop across the TE module. Using the same methodology, the Seebeck values were calculated and plotted in the Figure 72.



a) b)

Figure 71: a) Schematic of the experimental setup, b) The IR image of the TEC module

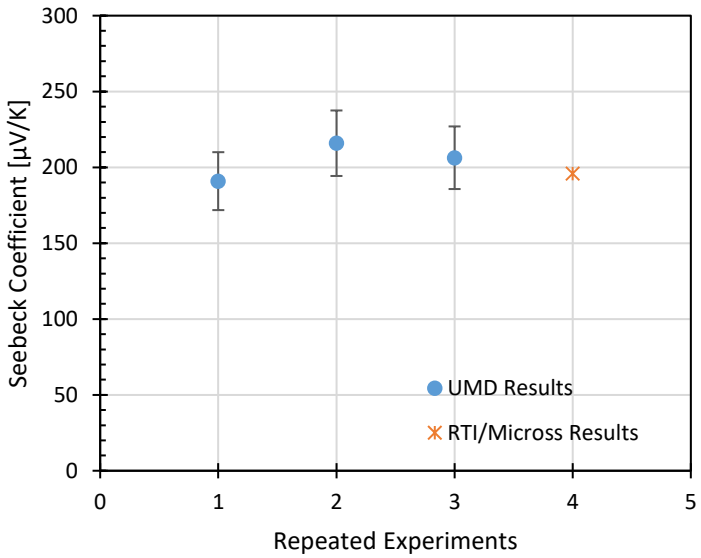


Figure 72: Experimentally calculated Seebeck values for three repeated experiments at UMD and one at RTI [47]

The Seebeck value is found to be ~200 µV/K, which is in line with the expectations that are based on historical data. In the following sections of the project, the measured Seebeck value is utilized for accurate analysis.

4.3 Device Level Characterization

The two modules with different thickness discussed in the previous section are characterized using the laser approach. As expected, the thinner module reached higher cooling flux, while the thicker device achieved larger ΔT at lower heat flux. This has one more time experimentally proven the initial claim that higher cooling fluxes are achievable as the thickness of the TE element is decreased, as shown in Figure 73.

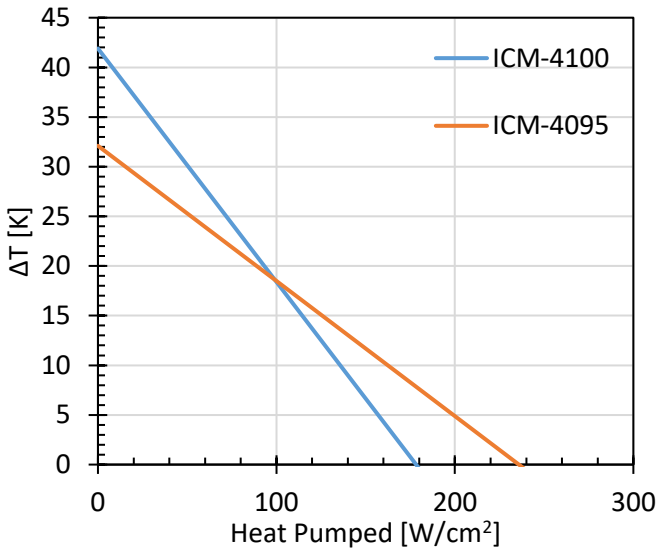
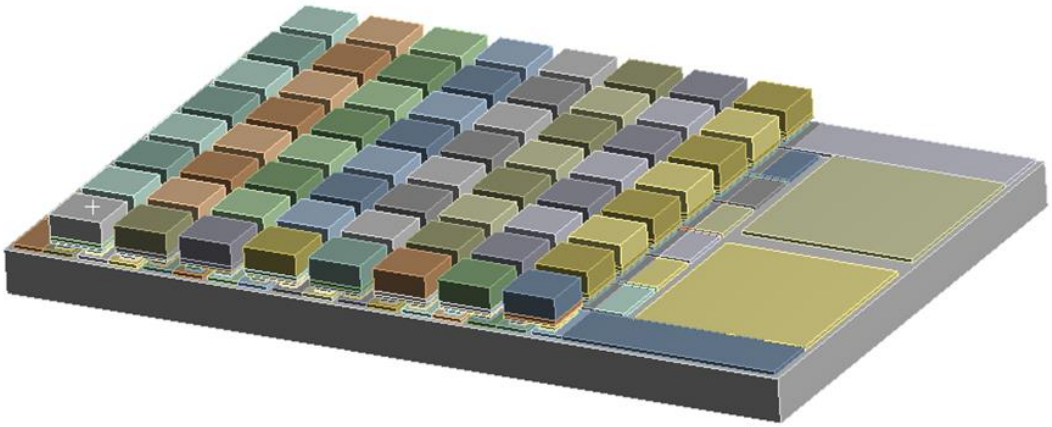


Figure 73: The experimental results of the two TEC modules. Blue curve represents the module with 15 micron and the orange curve represents the results from 7 micron device

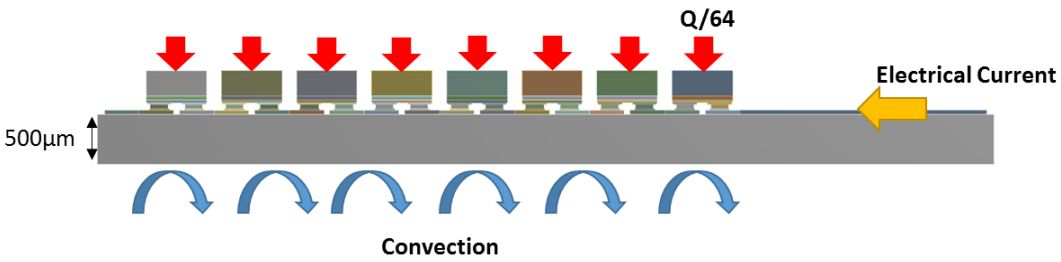
4.4 Numerical Model

In the actual laser cooling system, the TEC module consists of 64 P-N couples, that are identical to each other and also very similar in geometry to the modules experimented in the previous section. One of the main goals of DARPA-Matrix project is to decrease the electrical contact resistance to operate at larger electrical currents. As discussed in the previous sections, the electrical and thermal contact resistances were experimentally found to be roughly 1e-10 ohm-m^2 and 1e-7 m^2K/W respectively. However to meet the project's

goal, cooling of 100W of heat coming from the Quantum Cascade Laser(QCL), analytical calculations have shown that these values need to be decreases in the order of 1 or 2 magnitudes. To prove this claim a numerical model was created in Ansys-Workbench, including all 64 P-N couples. Since the sink side of the module will be subjected to liquid cooling via porous metal heat exchanger, a convection boundary condition was applied, with an effective base HTC of 200,000W/m^{2}K that was taken from the other subcontractor of the project responsible for the manufacture of the PMHX. The 3D model of the TEC module can be seen in Figure 74.



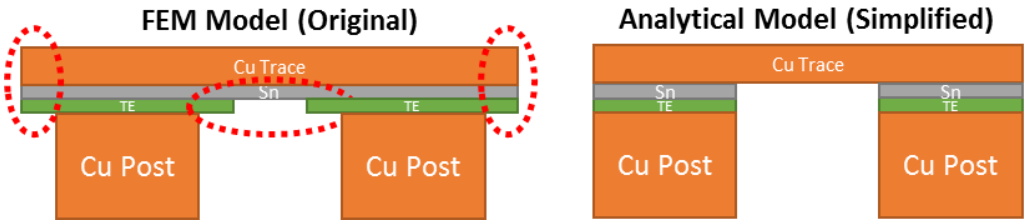
a)



b)

Figure 74: a) The overall 3D model of the TEC in Ansys-Workbench, b) The applied boundary conditions

Since the total heat dissipated from the QCL array is 100W, it is equally distributed on each one of the AlN headers on the source side of the TEC module, which comes to 1.5625W per header. The aggressively low contact resistances (1e-8 m^2K/W and 1e-12 ohm-m^2) were assumed and the electrical current was applied from the Cu terminal. The optimum TE element thickness and its corresponding electrical current value that minimizes the source temperature are investigated. In order to validate the numerical findings, a 1D system level analytical model was built in EES (Engineering Equation Solver) software in which the spreading resistances are also included using the correlations introduced by Lee et al.[53] In the real module the TE elements are larger in footprint than the Cu posts that make the connection with the sink side traces, but the analytical model assumed that the TE elements were the same size as the Cu posts, as can be seen Figure 75.



a) b)

Figure 75: a) The FEM model with the large TE elements, b) The analytical model and the simplifications

The Figure 76 shows the source side temperature results calculated with both models and the corresponding COPs of each case. The results indicate that there is an optimum thickness that minimizes the source side temperature, which is found to be 6 microns. The optimum current was approximately 25A, which is only possible by means of the decreased electrical contact resistances. Although 6 micron elements provide the lowest source temperature, the graph indicates that the COP is better at thinner elements, simply because

COP is a function of the element level ΔT and the electrical power consumed. Thinner elements can provide lower than optimum cooling however due to the increased ΔT and decreased power consumption, the COP values are much higher than the thicker elements of same DT. This demonstrates that there is a wide variety of choices for the thickness, which would depend on relative importance of COP and the source junction temperature.

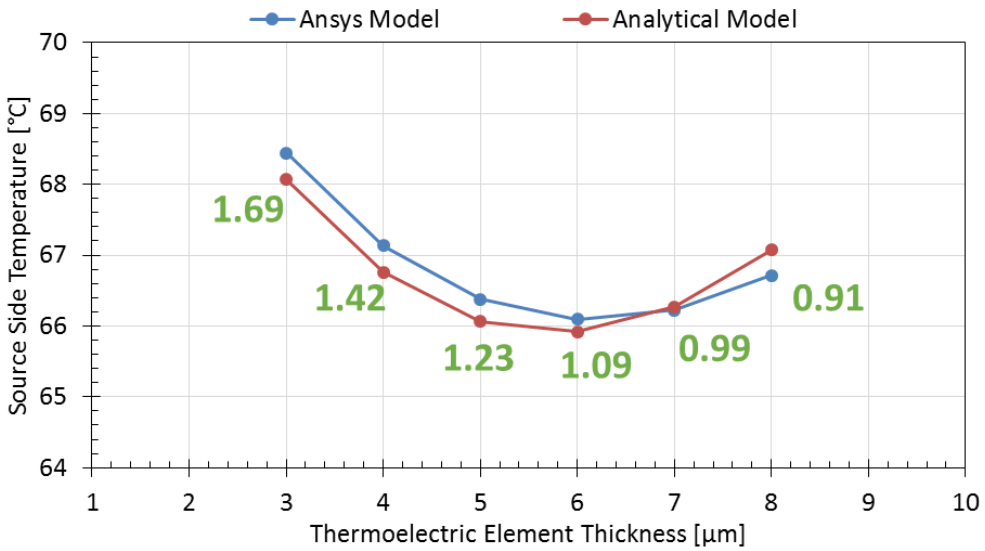


Figure 76: Source side temperature as a function of TE element thickness. The green values represent the COP at the given data points

Although the ECR values are decreased, the source temperatures are still considerably high and using PMHX alone could actually yield better performance. It was determined that this is mainly due to low packing fraction of the TEC module. Although the TE elements have a packing fraction of about 50%, the Cu post contacts between the TE elements and the solder layer limit the effective packing fraction to 30% as shown in Figure 77. Analysis were performed to demonstrate the outcome of improved packing fractions simply by having the Cu posts match the TE element footprint. The Figure 78 shows the outcome of various packing fractions at optimized thickness and current values.

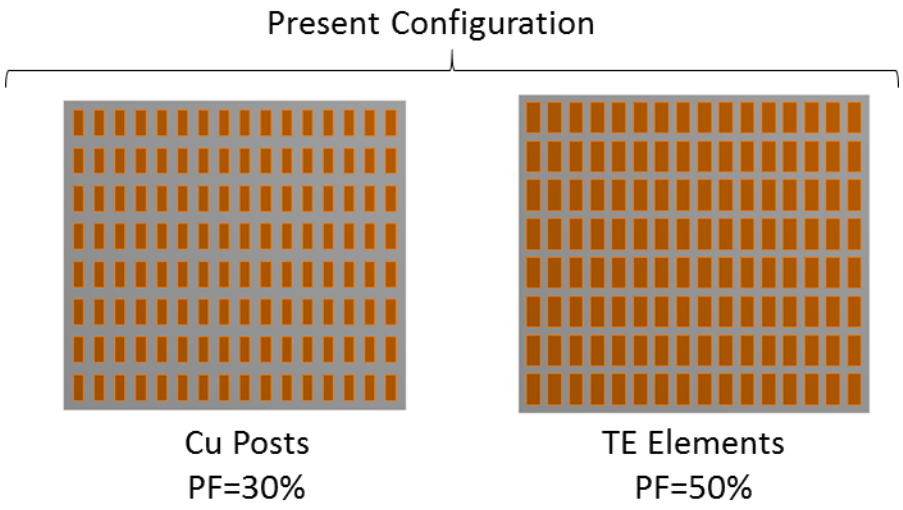


Figure 77: Discrepancy between TE element and Cu post packing fractions

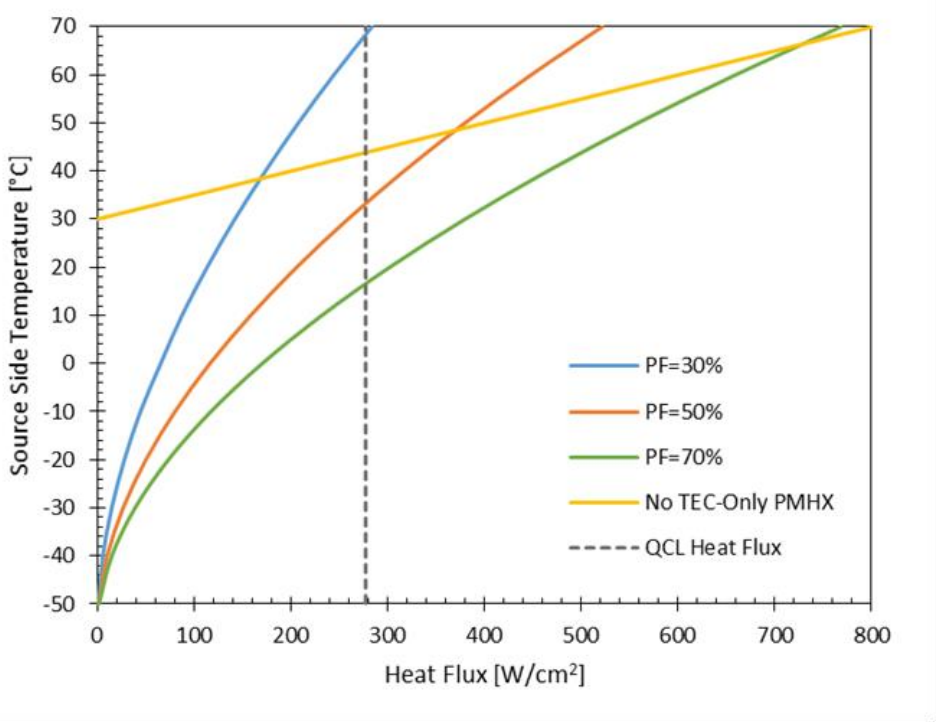


Figure 78: Optimal cooling results for various packing fractions by the chip heat flux

4.5 Conclusions

In this project, a method to accurately calculate the cross plane Seebeck coefficient of superlattice thin film thermoelectrics was introduced and explained in detail. The method circumvents the structural parasitic thermal resistances which in turn yields accurate measurements as it was verified using a numerical model. Using the material properties and a futuristic contact resistance value, a complete 3D numerical model of the TEC was built in Ansys Workbench to demonstrate cooling of a 100W dissipating QCL module. The results indicate that there is an optimum thickness that provides the maximum cooling, however the COP of this thickness is not necessarily the highest among the other thicknesses. This shows a variety of choices of thickness for the future module, depending on the relative importance of COP and source junction temperature.

5 System-Level Pareto Frontiers for On-Chip Thermoelectric Coolers

5.1 Introduction

Thermoelectric (TE) devices are solid state heat pumps that can be used for various purposes such as refrigeration and temperature stabilization. Their use in electronic cooling applications is extensively studied and explored [48-50]. Although their coefficients of performance (COPs) are considerably lower than other refrigeration cycles, the fact that they can be scaled to such small sizes and have no moving parts makes them advantageous in electronic cooling applications. This is particularly so for high flux electronics and military applications where lower COPs can be tolerated, because the prime purpose is to minimize the chip temperatures to ensure high reliability and chip efficiency. There are a

number of studies focused on embedded thermoelectric cooling using thin film devices, demonstrating that thinner structures are capable of removing very high localized heat fluxes and remediate chip hotspots [7,8,51,52].

The fundamental thermoelectric equations governing the heat pumped by a TE element are shown below [48-50]. An electrical current I passes through an element of length L and cross-sectional area A which results in rate of heat absorbed Q_c at the cold junction of the element and heat released Q_h at the hot junction of the element.

$$Q_c = ST_cI - \frac{1}{2}I^2R_{elec,TE} - K(T_h - T_c) \tag{5.1}$$

$$Q_h = ST_hI + \frac{1}{2}I^2R_{elec,TE} - K(T_h - T_c) \tag{5.2}$$

$$R_{elec,TE} = \rho\frac{L}{A_{TE}} \tag{5.3}$$

$$K = k\frac{A_{TE}}{L} \tag{5.4}$$

where S is the seebeck coefficient of the element, ρ its electrical resistivity, and k its thermal conductivity, K is the thermal conductance and $R_{elec,TE}$ is the electrical resistance of the TE element. T_c and T_h are the steady state temperature of the cold and hot junction, respectively, and Q_h is the heat rejected at the hot junction – larger than Q_c by an amount $I^2R_{TE} + SI(T_h - T_c)$. There are various electrical and thermal resistances discussed throughout the study, thus to better communicate with the readers, the electrical resistances are denoted with "elec" subscript. Any resistance that is not denoted with "elec" subscript signifies that it is a thermal resistance.

It is a well-established fact that a thermoelectric cooler's maximum heat pumping capacity can be significantly increased by decreasing the thickness of the semiconductor legs that form the TE elements [48-50,52-54]. Shorter legs decrease the electrical resistance of the semiconductor, which in turn allows operation at larger electrical currents and then larger cooling power. It can be derived from the thermoelectric equations above that the maximum cooling power Q_c, achieved when the temperature difference between the cold and hot junctions is zero ($\Delta T_e = (T_h - T_C) = 0$), is inversely proportional to the element thickness. A very recent study has experimentally reached 258W/cm^2 heat flux with an 8μm thick Bi_2Te_3 based TE element where they measured their device level[1] ΔT =0. [25]

However, a real thermoelectric module consists of not only thermoelectric elements, but also headers, metal trace layers and adhesion layers. And, as shown in Figure 79, a thermoelectric module is usually attached to a heat sink in practical cooling applications. Therefore, these parasitic thermal and electrical resistances need to be considered in the design and analysis of thermoelectric cooling systems. It is important to note that a decrease in the leg thickness also leads to a decrease in the maximum achievable system-level ΔT_{sys} at zero external heat flux. This is because as the TE thickness "L" is decreased, the thermal conductance of the TE element "K" increases, leading to a larger thermal back conduction from the hot junction to the cold junction and lowering the achievable ΔT_e. From an application point of view, thermoelectric coolers are typically designed to generate a desired amount of system-level $\Delta T_{sys} = (T_{sink} - T_{source})$ at a given cooling heat flux. Thinning down the material to further increase the cooling flux at the

[1] The ΔT in that study was measured from the source side of the AlN header to the sink side Cu trace. This leaves out the sink side AlN header from thermal resistance.

expense of decreasing available ΔT_{sys} may not be the best strategy in all cases. This phenomena has been discovered and discussed in other studies [55, 56], where the thickness is optimized for better thermoelectric cooling.

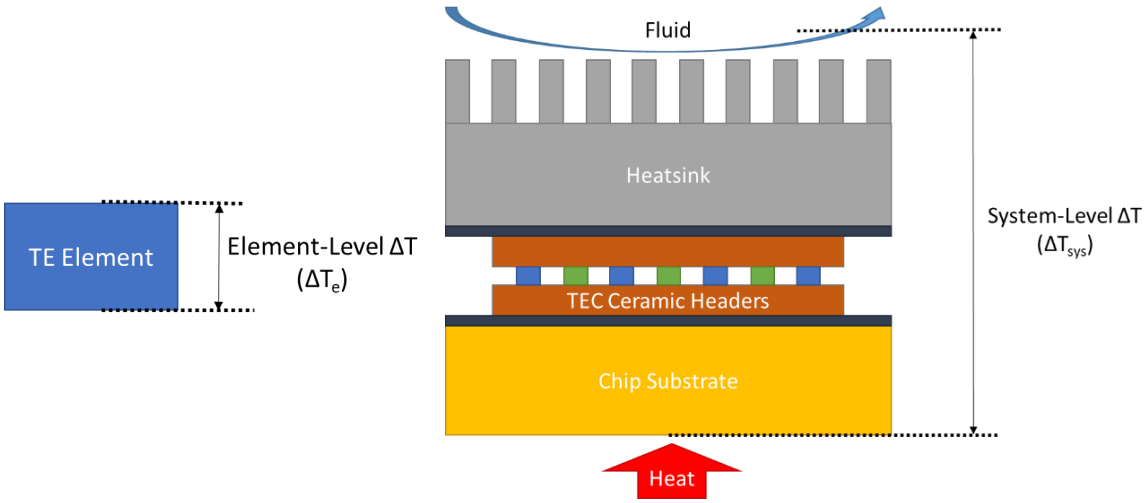


Figure 79: Schematic of a) Element level temperature difference ΔT_e b) System level temperature difference ΔT_{sys} in a typical thermoelectric cooling system architecture

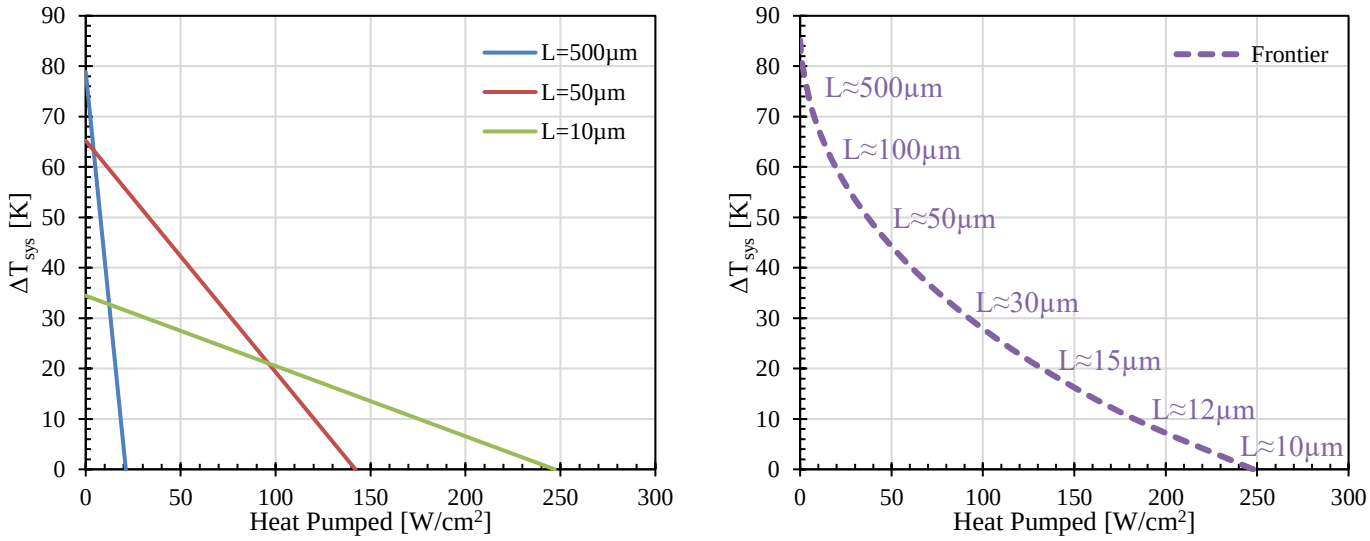
The optimum thickness and electrical current depend highly on the architectural structure of the system, where the mentioned thermal and electrical parasitics impact these optimal values. The external thermal parasitics result in a lower system-level temperature difference, ΔT_{sys}, established between the active heat dissipating surface to be cooled (source) and the ambient to which heat is rejected (sink) than the ΔT_e established across the TE elements. Meanwhile, the external electrical parasitics result in a discrepancy between the heat dissipated by the source, Q_s and the heat that must be absorbed by the cold junction Q_c.

Thus, this optimization study focuses on two interrelated topics. First, optimizing both thickness and current to minimize the source temperature (w.r.t to ambient) traces out a Pareto frontier curve for $Q_s\ vs\ \Delta T_{sys}$, which indicates the limitations of thermoelectric cooling for a given system architecture. Second, particular attention is paid to the effects of the system-level thermal/electrical parasitics on the optimized thickness and electrical current, which in turn dictates the shape and bounds of the associated Pareto frontier. An analytical system-level model is formulated and verified using commercially available finite element modeling (FEM) software, Ansys-Workbench. Finally, a case study is performed to provide an in-depth demonstration of the optimization procedure for an example application. The material properties of the thermoelectric element is chosen as S=±220μV/K (opposite in sign, same in magnitude for p- and n-type legs), k=1.25/Wm-k, and $\rho=1x10^{-5}$ ohm-m, that comes to a ZT value of 1.2 at 300K, which are typical values for Bi_2Te_3 type thermoelectric materials.[57]

5.2 Pareto Frontier Curve and Optimization Methodology

To understand how the Pareto frontier curve is formed, Figure 80-a demonstrates device-level cooling curves of 3 different TE element thicknesses, where the unit cell based device (see Figure 85) is assumed to have structural parasitic thermal resistance, R_{str} summing up to 20K/W per unit cell. The curves are generated using the revised TE equations (5.9-5.12), which are discussed in detail. For the shown curves, one can easily see that if the heat flux is higher than 100W/cm^2, the device with 10 μm elements would result in larger ΔT_{sys} than the device with 50μm element thickness. However, for applications where the heat flux value is less than 100W/cm^2, 50 μm elements perform better. The same situation exists between the 50 and 500 μm curves, but at a threshold

value where the two curves intersect at ~5W/cm^2. This illustrates that there exists an optimum thickness for any given heat flux value that can be obtained by considering more and more choices of thickness. By plotting the envelope of these separate cooling curves, the Pareto frontier curve shown in Figure 80-b is obtained. The individual pumping curves for a device of fixed element thickness are tangent to this frontier. Of course, the bounds and shape of the frontier depends on many parameters such as the operating temperature, system level structural resistances, and packing fraction of the device. Besides demonstrating the optimum thickness dependency on heat flux, it is also useful to understand the limits of a thermoelectric cooler in terms of the achievable system-level ΔT_{sys} at a specific heat flux.



a) b)

Figure 80: a) Heat pumped vs system level ΔT_{sys} curves for different TE thicknesses and b) the corresponding frontier curves for a given system level architecture that sums up to a structural resistance Rstr=20K/W, obtained using the revised TE equations. (8-11)

As discussed before, the system-level (structural) thermal resistances have an impact on cooler performance. These include thermal contact resistances, solder layers, ceramic headers, and especially convective resistance between the cooler and ambient sink. The sum of these resistances is defined as;

$$R_{str} = R_{layer,1} + R_{layer,2} + \cdots + R_{layer,n} + R_{thermal\ contact\ resistances} + R_{convection} \tag{5.5}$$

Because some structural resistances carry flux Q_s and others carry Q_h which is larger in magnitude, it is useful to categorize them based on location within the thermal path:

$$R_{str} = R_{source} + R_{sink} \tag{5.6}$$

where R_{source} includes all of the layers between the heat source and TE element cold junction, and R_{sink} includes all of the layers after the TE hot junction, with an additional convective resistance term.

The structural thermal resistance has a strong influence on the frontier curve and the corresponding optimal variables. For this reason, the thermoelectric equation alone is unfortunately not enough to analyze a system where the structural thermal resistance are comparable to that of the TE element. This can be explained by realizing that in the presence of structural resistance, the temperature difference across the semiconductor legs does not reflect the actual temperature difference across the module (or system), as seen in Figure 81. This necessitates integrating the thermal and electrical parasitics into the thermoelectric cooling equation for accurate system-level analysis.

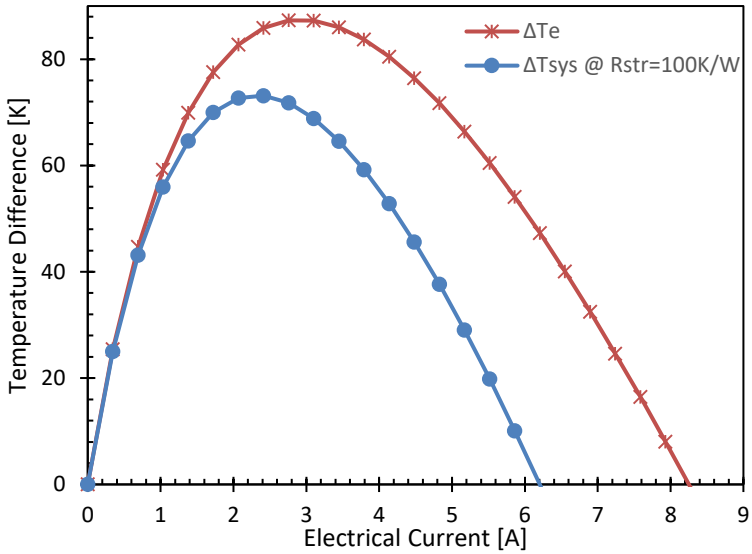


Figure 81: Discrepancy between element level ΔT_e and system level ΔT_{sys} due to structural thermal parasitics for an example module with 100μm thick TE element.

The electrical contact resistances, ρ_{ECR}, and the Cu trace resistances, $R_{elec,trace}$, are added to equation (5.1) by replacing the term $R_{elec,TE}$ with $R_{elec,eff}$, which is defined as;

$$R_{elec,eff} = R_{elec,TE} + 2\left(\frac{\rho_{ECR}}{A_{TE}} + R_{elec,trace}\right) \tag{5.7}$$

Thus the revised thermoelectric equations become;

$$Q_{c,rev} = Q_s = ST_cI - \frac{1}{2}I^2R_{elec,eff} - K(T_h - T_c) \tag{5.8}$$

$$Q_{h,rev} = ST_hI + \frac{1}{2}I^2R_{elec,eff} - K(T_h - T_c) \tag{5.9}$$

where the discrepancy between $Q_{h,rev}$ and Q_s is by the amount $^1/_2\, I^2[R_{elec,eff} - R_{elec,TE}]$.

For the thermal parasitics, the hot and cold junction temperatures T_c and T_h can be written in the forms below;

$$\Delta T_{source} = T_{source} - T_c = Q_s R_{source} \tag{5.10}$$

$$\Delta T_{sink} = T_h - T_{sink} = Q_{h,rev} R_{sink} \tag{5.11}$$

where T_{sink} could either be the temperature of the fluid (if the convective resistance is taken into consideration in R_{sink}) or it can be taken as the surface temperature of the last solid layer if a fixed temperature boundary is assumed. Solving equations (5.8-5.11) simultaneously and performing some algebraic manipulation, the equation defining the source side temperature is given as;

$$T_{source} = R_{source} Q_s + \frac{Q_s + \frac{1}{2} I^2 R_{elec,eff} + \varphi\left[T_{sink} + R_{sink}\left(Q_s + I^2 R_{elec,eff}\right)\right]}{SI + \varphi} \tag{5.12}$$

where φ for convenience is defined as;

$$\varphi = \frac{K}{1 - R_{sink} SI} \tag{5.13}$$

It is this equation that is then optimized to achieve the lowest possible T_{source} for a given T_{sink} and Q_s. The optimization variables considered are the current I and the element thickness L, which influences $R_{elec,eff}$ and K. It is important to keep in mind that equation (5.12) is defined per TE leg, where the unit for Q_s is in Watts and units for R_{source} and R_{sink} are in K/W.

5.3 Effect of Electrical Parasitics

The previous section introduced the importance of both thermal and electrical parasitics in the system and their effects on thermoelectric cooling behavior. In this section, the effect of electrical parasitics is discussed in more detail. In thermoelectric cooling, joule heating is the main factor that restricts the optimum current because it has a quadratic relationship with current while the Seebeck cooling term has a linear relationship. Therefore after a certain value, increasing the electrical current does not further improve the performance, and that value is the optimum current for that device. Therefore, decreasing the electrical resistance in the current path allows operating with higher current and thus improves the maximum cooling flux capacity.

In the revised form of the thermoelectric equation (5.8), we have already introduced an effective electrical resistance that includes the ECR (Electrical contact resistances) and the electrical resistances due to the Cu traces within the module. These two parasitics are of minor importance for bulk TECs, where the total electrical resistance is dominated by the thick thermoelectric elements. However, when approaching the thin film regime, the parasitics constitute a much larger portion of the total electrical resistance as can be seen in Figure 82, which makes it an important concern for high flux thin-film thermoelectric cooling applications.

a) b)

Figure 82: Percentage breakdown of electrical resistances for; a) thin film TEC and b) Bulk TEC, when the Cu trace thickness is 50µm and the electrical contact resistance is ECR=1x10^{-10} ohm-m^2 , which reflect today's capabilities[25,58]

The significance of electrical contact resistances are well known in the thermoelectric cooling community and there are studies for measuring and decreasing them for better device performances [58]. From a thermal design standpoint, it is important to know how the ECR limits the performance and what could be achieved if the resistances could be minimized. Figure 83 demonstrates the achievable cooling fluxes at $\Delta T_{sys} = 0$ for various system level structural resistances. Results clearly indicate that as both thermal and electrical parasitic resistances are eliminated, heat fluxes over 1 kW/cm^2 are achievable.

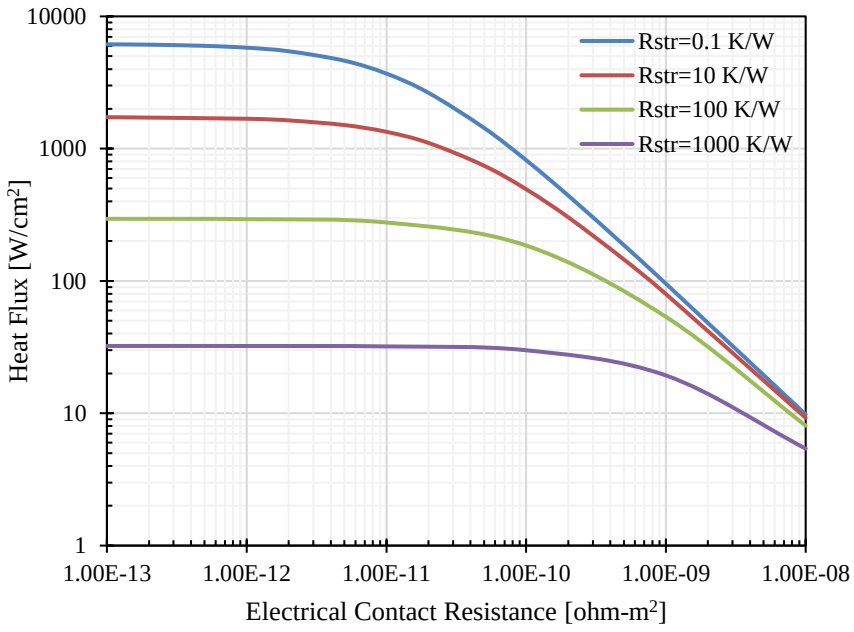


Figure 83: Effect of electrical contact resistance on achievable heat fluxes when ΔT=0. For comparison with the following sections of the paper, the corresponding "areal" resistance for the R_{str}=0.1K/W curve is $R_{str,areal}$ =1.23x10^{-4}cm^{2}K/W.

The second added term contributing to the overall electrical resistance is the resistance of the Cu traces carrying the current from one TE element to another. Unlike ECR, the traces have both thermal and electrical resistances that simultaneously affect the system performance, and it is possible to perform an optimization on their thickness to enhance cooler performance.

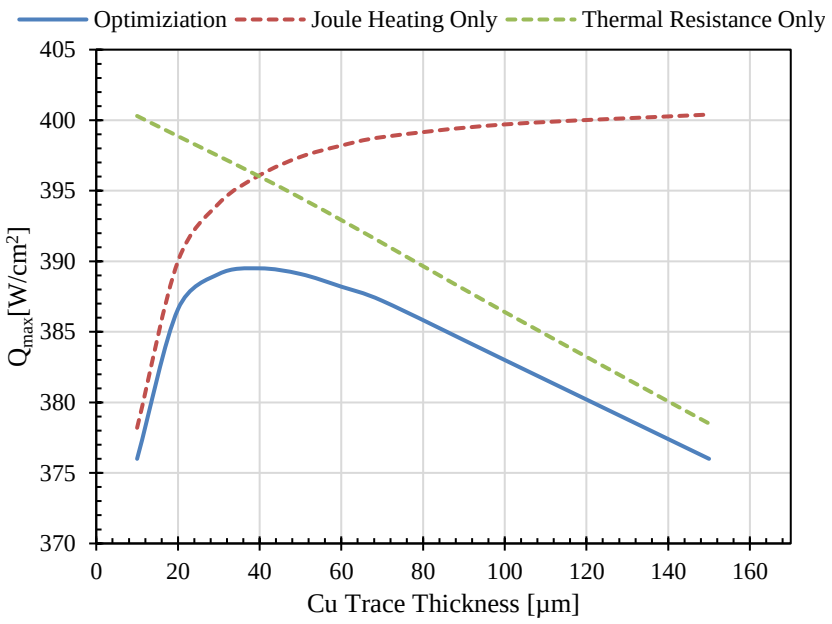


Figure 84: Cu trace thickness optimization

For bulk TECs, where the electrical resistance of the module is already dominated by the thick TE leg, the electrical current is not very high and thus an optimization of the Cu trace thickness yields limited benefit. However, when approaching the thin film regime, the operating electrical current is significantly increased and can cause tremendous amount of joule heating. Over-increasing the trace thickness to circumvent joule heating will start to limit the performance due to the increased thermal resistance in the heat flow pathway. Therefore, there is a certain optimum Cu trace thickness, unique for each of the sink and source sides, that minimizes the degradation on the device performance. It is important to note that while both sides experience the same electrical current flow, the sink side experiences much higher heat fluxes than the source side. Therefore the optimized thickness of the source side Cu trace is always larger than the sink side Cu trace.

To demonstrate this effect, an aggressively reduced value for electrical contact resistance is chosen (10^{-12} ohm-m^2) whereby the trace resistance is the dominant parasitic. The

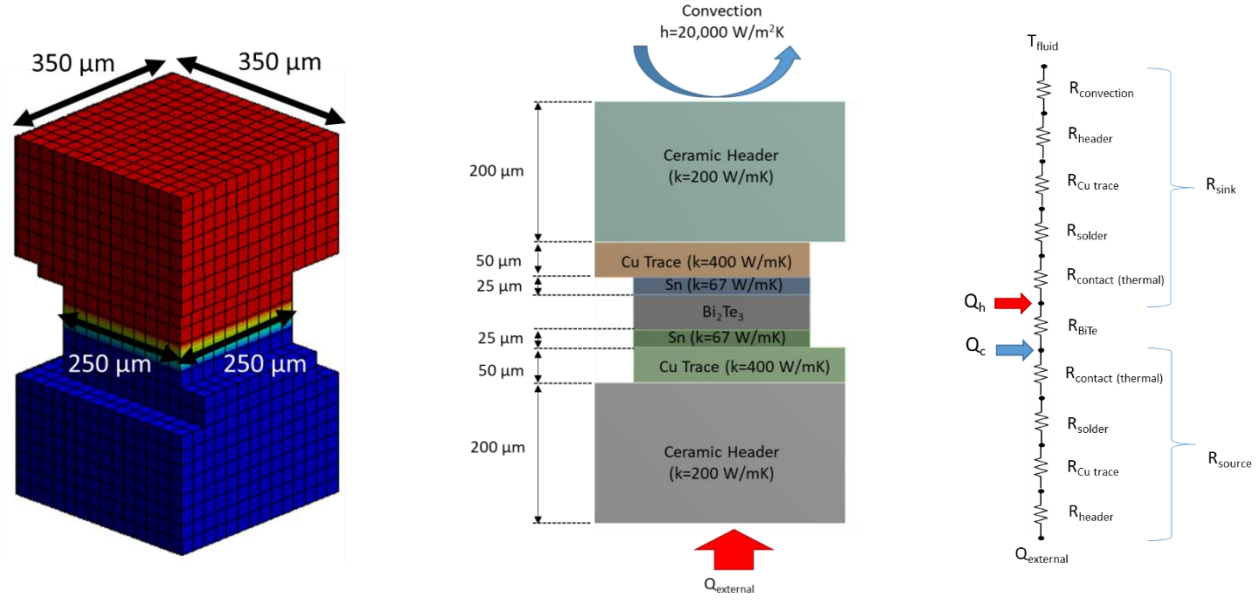
optimum thickness of the sink-side Cu trace is found which maximizes the cooling flux Q_{max} at $\Delta T_{sys} = 0$. The geometry of the source and sink side in the optimization study are those used in the FEM validation (discussed in the next section). The convective boundary condition was specified as HTC=200,000W/m^{2}K at T_{sink}=400K, reflective of power electronics cooled by a microchannel cold plate [61-65]. In a more comprehensive optimization study, the change in the Cu trace thickness would also change the optimum TE element thickness, but for simplicity the element thickness is fixed at 20μm. Also shown in Figure 84 is the resulting Q_{max} when incorporating only trace conductive thermal resistance and only trace joule heating. These are obtained by setting trace thermal resistivity and electrical resistivity in turn to zero. Expectedly, the optimum thickness is located where the two parasitic curves intersect. For this particular case, the optimum thickness was found to be 40 μm.

In the following sections of this study, the electrical contact resistance and Cu trace thicknesses on both sink and source side have fixed values at 1e-10 ohm-m^2 and 50μm respectively, which are within the range of today's capabilities [25]. They are kept constant throughout the optimization and case study sections of the analysis.

5.4 Analytical Model Verification

As can be seen in equation (5.12), the source side temperature depends on various parameters including material properties K, $R_{elec,eff}$, S and other parameters such as Q_s, T_{sink}, R_{source}, R_{sink}, L, I of which I and L can be simultaneously optimized to minimize T_{source} for a given architecture. To verify the viability of the equation before starting the optimization process, a numerical model was built on commercially available FEM software ANSYS-Workbench, and T_{source} was obtained for various model parameters. The

model used in this study is a single unit cell, assuming a fixed 50% element area packing fraction with a TE element footprint of 250µmx250µm and header footprint of 350µmx350µm, as shown in Figure 85.



a) b) c)

Figure 85: a) Unit cell based, numerical model geometry, b) dimensions and material properties of the system c) Thermal resistance network of the system

For the analytical model, the thermal resistance of each solid layer and for the convection boundary is calculated. Because there is change in area from the TE element to the Cu layer and the ceramic header, the constriction and spreading resistances for affected layers are calculated using analytical correlations from Lee et al. [59]. The resultant sink and source side resistances are found to be R_{sink}=427K/W and R_{source}=18K/W per TE leg (the unit cell). The large disparity between the two thermal resistances is due to the impact of the fluid convection boundary.

All of the structural parameters along with the boundary conditions were substituted into equation (5.12) to analytically calculate the source side temperature. Results and comparison for a wide variety of boundary conditions are shown in Table 9, where TE thickness L, Electrical current I, T_{sink} and heat flux values are varied. Very good agreement is obtained between the numerical and analytical models, with a maximum difference in temperature of less than 0.2K between the two models.

Table 9: Comparison of the analytical and numerical results for specified boundary conditions

TE thickness [μm]	**T_{sink} [K]**	**Electrical Current [A]**	**Heat Flux [W/cm^2]**	**$T_{source,}$ Ansys [K]**	**$T_{source,}$ Analytical [K]**	**Difference [K]**
50	300	0.5	10	295.26	295.42	0.16
50	300	1.5	10	279.85	279.99	0.14
150	300	0.5	10	280.70	280.86	0.16
150	300	1.5	10	261.38	261.51	0.13
50	400	0.5	20	401.11	401.25	0.14
50	400	1.5	20	374.89	374.95	0.06
25	350	1	20	350.09	350.25	0.16
25	350	3	20	350.62	350.81	0.19

Moreover, calculations were performed with the analytical model to compare the results from an experimental study conducted by Bulman et al.[25] The dimensions (TE element thickness (8.1μm) and dimensions of other layers) and material properties were taken from that study. The heat load curve was generated using the analytical model and the results have a good agreement with the reported experimental findings as shown in Figure 86.

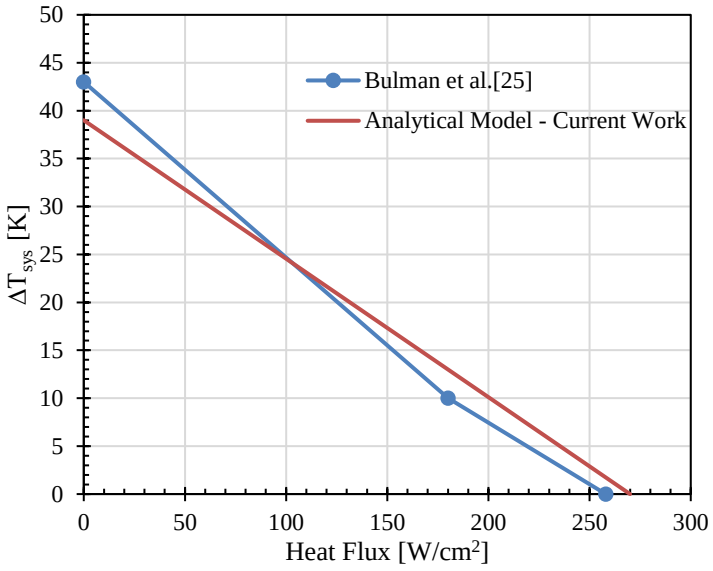


Figure 86: Analytical model results comparison with experimental results obtained by Bulman et al. [25]

5.5 Optimization Results and Discussion

In order for the thermoelectric cooler to achieve higher cooling fluxes, the external structural resistances must be minimized. As discussed before, the convective resistance generally dominates the overall structural resistance, making it the bottleneck of the system on the sink side. On the source side, the resistances can be high enough to be comparable to that of the sink side if the thermoelectric cooling is enhanced by a mini-contact pillar, which concentrates the cooling flux of the TEC on a much smaller heat source, such as a hotspot [7,8,51]. However, in many electronic cooling applications this is not the case and the source side resistance will be a much smaller portion of the overall structural resistance. For applications where thermoelectric coolers are utilized, it is important understand the limitations of a design. The frontier line which was introduced in the previous sections is a good way to predict the performance of a design at the system level. Thus, a wide analytical optimization study is carried out to give a general overlook on the system-level

behavior of thermoelectric cooling, where the sink- and source-side resistances are incorporated into the analysis. Using (5.12), it is possible to do a multi-variable, single-objective optimization where both thermoelectric element thickness and TEC electrical current are optimized to obtain the minimum source temperature. Because system ΔT_{sys} and Q_s are linked one-to-one along the Pareto frontier, together they form the single objective to be maximized. Thus, the optimization can be achieved by either holding Q_s constant and maximizing ΔT_{sys} (as in Equation (5.12)) or vice versa. The first pair of graphs in Figure 87 represents maximized cooling fluxes while holding the system ΔT_{sys} (from source to sink) constant, with the left graph representing the results at T_{sink}=300K and right at T_{sink}=400K. The other two pairs of graphs in Figure 88 and Figure 89 are the corresponding optimized thickness and current densities, respectively. The resistances R_{str} and electrical currents are converted to area-based resistance $R_{str,areal}$ and current density in order to be used as an approximate guide for other geometries as well. Two temperatures, 300K and 400K are considered as the fluid temperature to mimic air cooling and two-phase cooling on the sink side for power electronic cold plates Considering that the percentage of sink and source side resistances contributing to the overall structural resistance has significant effect on the optimal geometries and performance, a new variable gamma is introduced as;

$$\gamma = \frac{R_{sink}}{R_{str}} \tag{14}$$

The influence of this ratio on the optimal geometry and cooling is reduced as the R_{str} approaches zero, as demonstrated in Figure 87, Figure 88 and Figure 89. All of the temperature differences in the graphs are system level ΔT_{sys}.

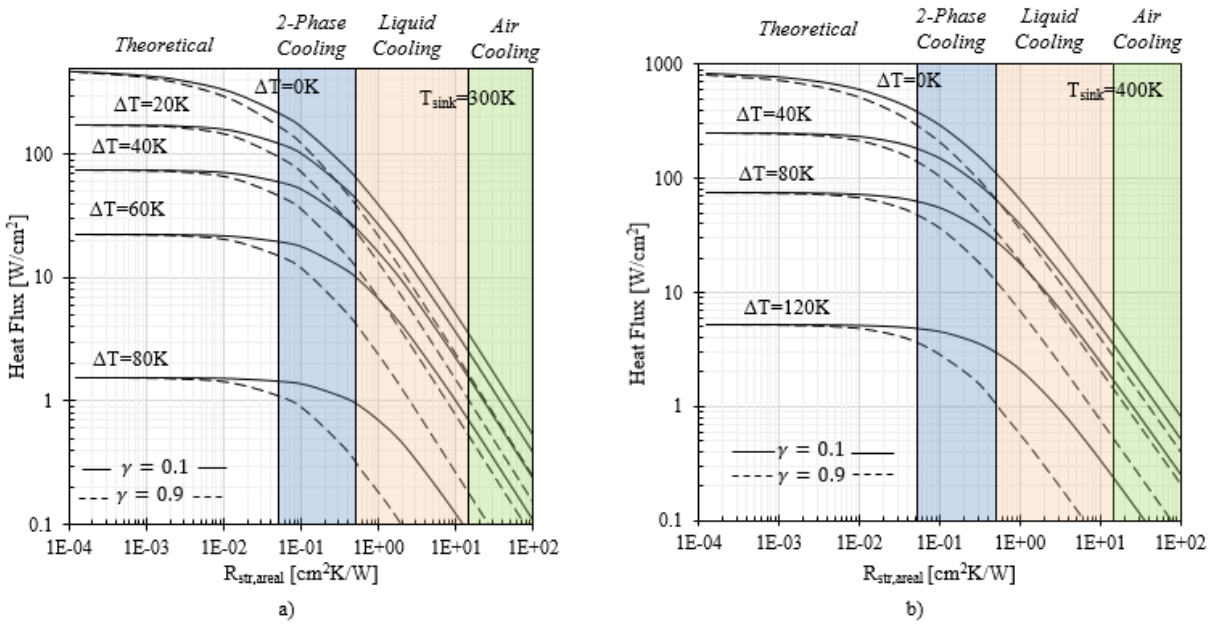


Figure 87: Master curves of Q-ΔT for various structural resistances at a)T_{sink}=300K, and b) T_{sink}=400K

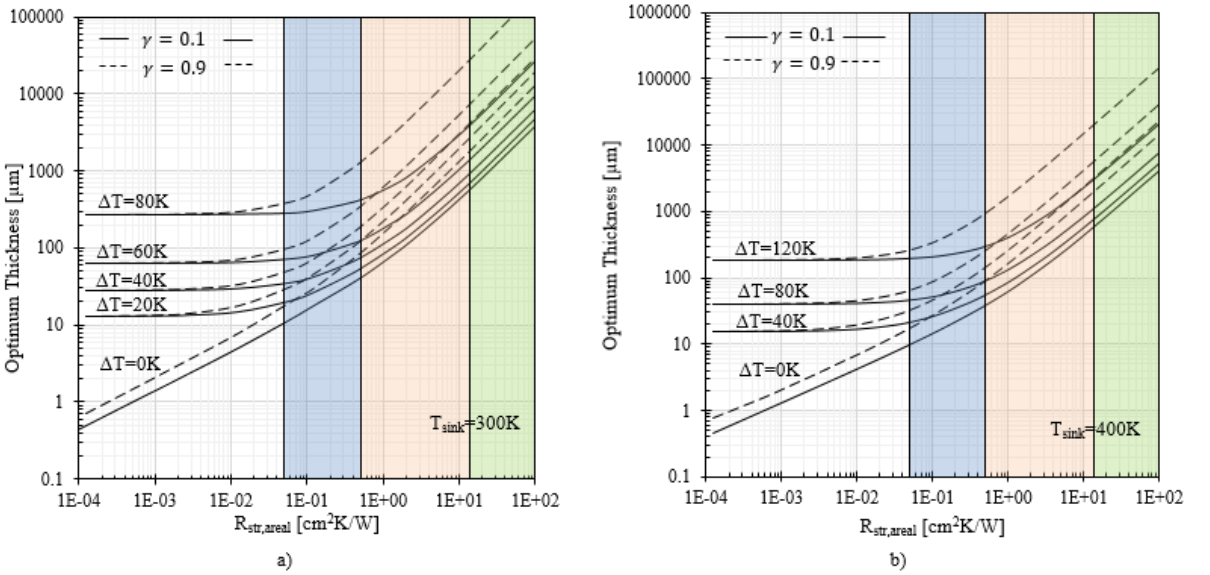


Figure 88: Master curves of optimized TE element thicknesses for various structural resistances at a)T_{sink}=300K, and b) T_{sink}=400K

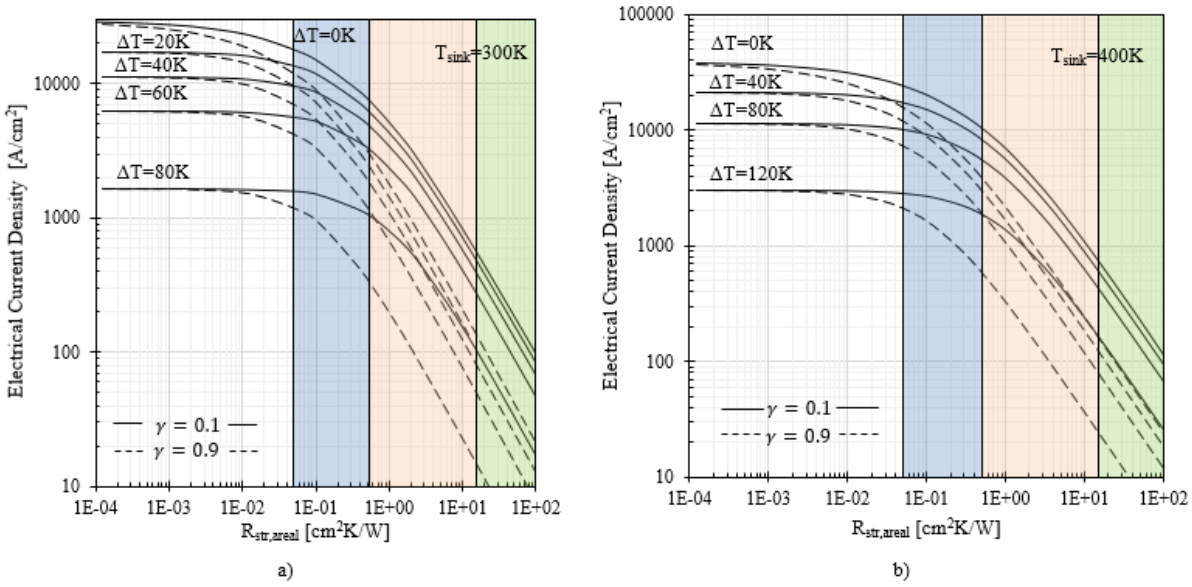


Figure 89: Master curves of optimal current densities for various structural resistances at a)T_{sink}=300K, and b) T_{sink}=400K

Applications in which thermoelectric cooling is used vary in the method of heat rejection from the hot junction to the environment. Typically for traditional or bulk TECs the heat removal is handled by an air cooled system where the heat transfer coefficient (HTC) is very limited [60]. Superior cooling mechanisms such as liquid cooling or two phase cooling are required in order to operate with thinner TECs and higher heat fluxes. Figure 87 shows various system level ΔT_{sys} curves and their achievable heat fluxes as a function of $R_{str,areal}$. As a guide, the graphs in Figure 87, Figure 88 and Figure 89 are divided into four regions, demonstrating the heat flux capabilities per different sink side cooling mechanisms based on their achievable HTCs. The heat transfer coefficients are converted to areal resistances simply by $R_{conv,areal} = 1 \,/\, h$ and later on converted from m^2 to cm^2. The maximum HTCs used in formation of the bands are 200 kW/m^2K for two-phase cooling, $20kW/m^2K$, for liquid cooling and 500 W/m^2K for air cooling [60-65]. It can be

seen from the figures that while air cooling can allow heat pumping up to 3-5W/cm^2, liquid cooling can allow the TEC to pump up to 50-100W/cm^2. Two-phase cooling, on the other hand, enables up to 300-400W/cm^2. The white region on the left contains systems that exist in the theoretical limit of zero structural thermal resistance. Even with a perfect convection boundary condition, i.e. fixed temperature, the structural resistances due to ceramic headers, Cu traces and solder layers limit the performance.

The region below 1x10^{-2}cm^{2}K/W is especially unrealistic, as such $R_{str,areal}$ would require that even the Cu traces should be eliminated, which implies element-level thermoelectric cooling. However, it is important to note that the results shown in in Figure 87, Figure 88 and Figure 89 still include the electrical parasitics, meaning that equation (5.12) does not converge (in the limit) to equation (5.1) without also allowing equation (5.7) to converge to the element-only electrical resistance.

5.6 Case Study

The master curves generated in the previous section are the links that connect the system-level architecture with the frontier curves. For a given R_{str}, a line crossing each one of the ΔT curves would give the corresponding achievable heat flux value. Thus, if plotted, a pareto frontier for that particular structural resistance is obtained. To demonstrate this, a power electronic case study is performed. A thermoelectric cooler to be designed for an embedded cooling system architecture is investigated. The sink side is subjected to evaporative cooling that can provide an effective base HTC of 50,000W/m^2-K. The TEC has 1.4mmx1.4mm footprint, 16 TE elements at 50% packing fraction, and it is bonded to a silicon chip substrate and an aluminum microchannel heatsink with 10 μm thick Sn solder. For simplicity, the fluid saturation temperature is assumed to be 400K (127°C) and

the heat flux from the Si chip is 50W/cm^2. In such a scenario, we are demonstrating the optimization procedure to find the optimal TE element gemoetry and the optimum electrical current to minimize the source chip temperature.

Table 10: Dimensions and assumed thermal conductivities for the case study model

Layers	**Thermal Conductivity [W/m-K]**	**Thickness [µm]**
Aluminum Heatsink Base	180	500
Aluminum Nitride Headers	250	200
Silicon Substrate	150	100
Copper Traces	400	50
Tin Solders (within TEC module)	67	25
Tin Solders (outside of TEC module)	67	10

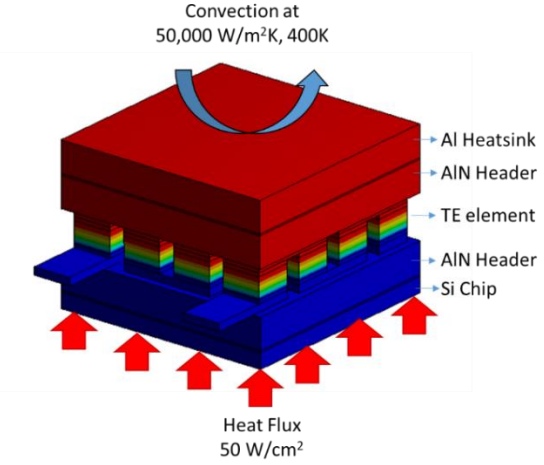


Figure 90: The 3D model of the system built in Ansys-Workbench

Since the architecture of the system is known from Table 10 and Figure 90, the structural resistances can be calculated as,

$$R_{str} = \frac{L_1}{k_1 A_1} + \frac{L_2}{k_2 A_2} + \cdots + R_{spr,1} + R_{spr,2} + \cdots + \frac{1}{hA} \tag{5.15}$$

Based on the given geometry and convective boundary condition, we find R_{sink}=12.76 K/W and R_{source}=1.48 K/W, summing to $R_{structural}$=14.25 K/W with $\gamma = 0.9$.

One way of determining the optimum thermoelectric element geometry and current is graphically by using the curves provided in the Figure 87, Figure 88 and Figure 89. To do that, the areal structural resistances should be obtained first by:

$$R_{str,areal} = R_{str} \times A_{TEC} \tag{5.16}$$

which results in $R_{str,areal}$=0.279 cm^2K/W. This particular resistance can now be used to find the Q_s&ΔT_{sys} values using the $\gamma = 0.9$ master curves and a heat flux frontier curve can be generated as denoted with green dotted lines in Figure 91.

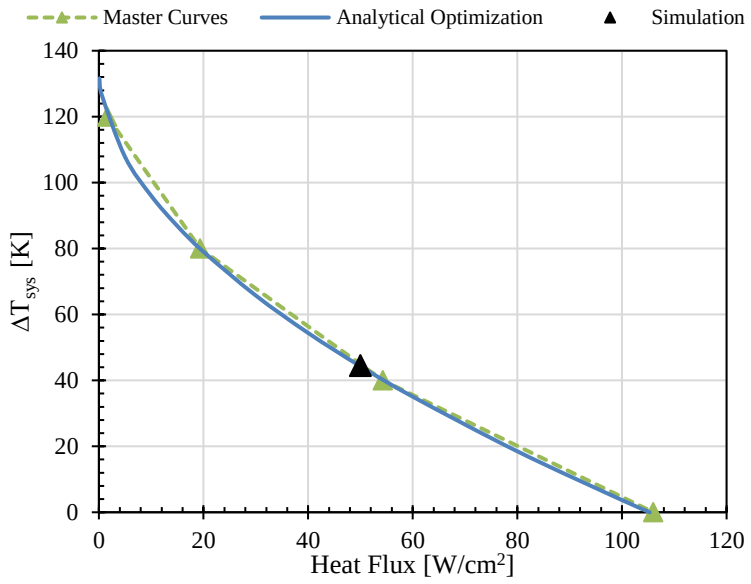
A more detailed optimization approach is to utilize equation (12). Since the equation (12) is defined per leg, the structural resistance can be multiplied by the number of elements to obtain the *per leg structural resistance*;

$$R_{str,per\ leg} = R_{str} \times N_{TE} \tag{5.17}$$

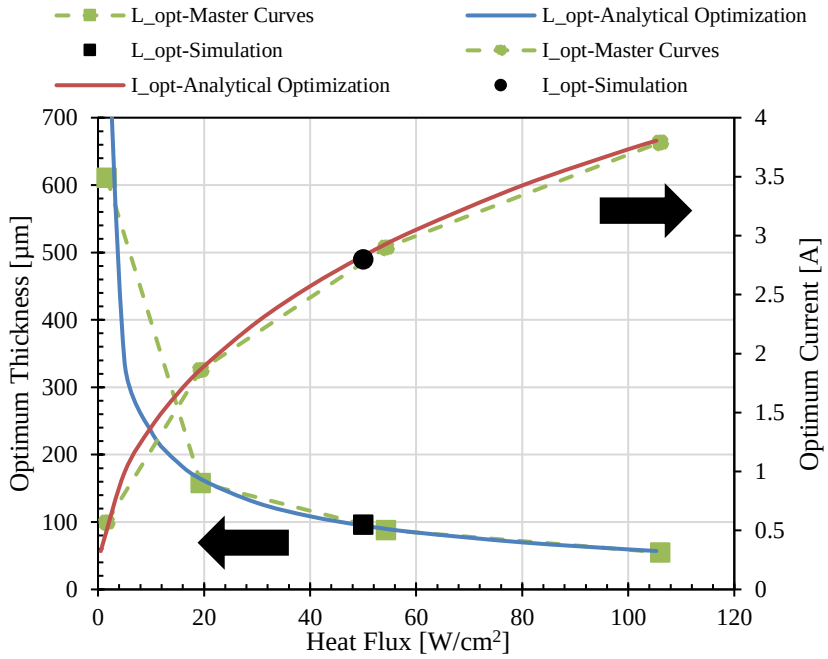
Resulting in R_{sink}=204.2 K/W and R_{source}=23.7 K/W per TE leg. Similarly, the Q_s in the equation 12 can be calculated as;

$$Q_s = \frac{q'' A_{TEC}}{N_{TE}} \tag{5.18}$$

Which gives Qs=0.06127 W per leg. These values can now be substituted in the equation (5.12), and using a multi-variable optimization method such as conjugate gradient method, the TE thickness and electrical current can be optimized to obtain the minimum source temperature. For reader's convenience, most of the common programming software include pre-made multivariable optimization tools that can be easily utilized for such optimization.



a)



b)

Figure 91: a) Pareto frontier b) Optimal values of the variables obtained using three different methods; the master curves, analytical optimization and simulation

5.7 Conclusions

In this study, two interrelated subjects in thermoelectric cooler optimization were introduced and evaluated. First, the heat flux dependency of optimum thermoelectric element thickness and optimum current was demonstrated through the establishment of a Pareto frontier load curve. The frontier curve shows the amount of achievable system-level ΔT at any given source heat flux. Thus, it is very useful to understand the limitations of thermoelectric cooling in a particular architecture. It benefits the designers to understand what values of thickness and electrical current can provide the necessary cooling, or shows when the desired source temperatures at the given heat fluxes are not possible.

Second take away from this study is that the shape and bounds of the frontier curve heavily depend on certain system level parameters, such as structural thermal/electrical parasitics. The parasitics significantly affect the optimum thickness and electrical current, which in turn impacts the frontier curve. Therefore the thermoelectric phenomena are analytically evaluated in the presence of system level parasitics and a comprehensive equation is derived, which is later used in the optimization. The analytical model results are compared with numerical results using the commercially available FEM software Ansys-Workbench. A very strong agreement is obtained between the two models, with a maximum discrepancy within 0.2K. Using this analytical model, a wide optimization study is performed and 3 pairs of master curves are obtained at T_{sink}=300K and 400K. The master curves are the links between the effects of the structural thermal resistances and the Pareto frontier curve. Once the structural resistance of a particular application is known, the master curves can be used to form the appropriate frontier curve. The formed frontier curve illustrates the limitations of thermoelectric cooling for that particular application. This was finally

demonstrated via a case study where the geometry and boundary conditions are explained in detail. Both simulation and analytical optimization is used along with the values obtained graphically from the master curves, and the Pareto frontier formation is demonstrated.

6 Conclusions and Future Work

6.1 Conclusions

Overheating of electronics often limit the performance and compromise system reliability. Especially hotspots can cause very high localized temperature rises that needs to be addressed. This thesis demonstrates that thin film thermoelectrics, with the use of a mini-contact, can remediate high flux hotspots in power electronics. Besides hotspot cooling, for applications where the background heat fluxes are only within 100s of W/cm^2, thin film thermoelectric coolers can be utilized for background cooling as well.

Two novel cooling approaches were presented in DARPA-ICECool project, to address the non-uniform high heat fluxes dissipated by today's power electronics. The cooling mechanism involves integrating a thermoelectric cooler into a manifold microchannel system to cool 1 kW/cm^2 global surface and $5kW/cm^2$ hotspot heat fluxes as uniformly as possible. The main components in the integration structure were modeled in ANSYS-Workbench and numerically optimized. As a result, with 30 °C temperature rise at the background surface, less than 35 °C of hotspot temperature rise with respect to the coolant fluid temperature (110°C) was numerically demonstrated. Moreover, to circumvent the electromigration issues raised by the sponsor, an accelerated test was performed on the

standard RTI module, and the results show no visible degradation. To mitigate any possible future electromigration concerns, a well proven Cu UBM approach was discussed and applied to the ICECool TEC structure.

As a part of this thesis, it was also demonstrated that a thermoelectric cooler is successfully capable of de-coupling two different heat sources with different operating temperatures in a highly packed electronic device. The electronic die can operate at higher temperatures, thus using a thermoelectric cooler, it is de-coupled from the optical arrays which operate at lower temperatures. This allows eliminating the need to over-cool the entire package and improves overall system efficiency. The experimental and numerical efforts for the phase 1 and preliminary predictions for the phase-2 has illustrated that even with miniature bulk thermoelectric coolers, the de-coupling is possible.

Another possible field of electronics that TFTECs can be made use of is the Quantum Cascade Lasers, which dissipate heat fluxes in the order of 100s of W/cm^2. The heat fluxes are much larger than any TFTEC can handle with today's capabilities. However, by decreasing the electrical and thermal contact resistances, it was numerically and analytically demonstrated that the cooling of such QCL modules are possible. There is a variety of thickness options to choose depending on the relative importance of the COP of the operating system and the source temperature.

Finally, the heat flux dependency of optimum thermoelectric element thickness and optimum current is demonstrated through the establishment of a Pareto frontier load curves.

The frontier curves show the amount of achievable system ΔT at any given source heat flux. In addition, it was observed that the shape and bounds of the frontier curve heavily depends on certain system level parameters, such as structural thermal/electrical parasitics. The parasitics significantly affect the optimum thickness and electrical current, which in turn impacts the frontier curve. To further investigate their effects, the thermoelectric phenomena is analytically evaluated in presence of system level parasitics and a comprehensive equation is derived, which is later used in the optimization. 3 pairs of master curves that show the relationship of structural resistances with the optimal variables and achievable cooling fluxes are obtained at T_{sink}=300K and 400K. This optimization methodology and master curves can be used as an approximate guide to narrow down the design options for the designers and understand the TE cooling capability for any given system.

6.2 Future Work

6.2.1 Integration of Micro-Contact Enhanced TFTEC in Microchannel Manifold System

Extensive numerical studies have indicated the capability of thin film thermoelectric coolers in remediation of a 200μmx200μm hotspot with 5kW/cm^2 heat flux. Various integration concepts with important system-level considerations are discussed in detail, and 5K hotspot temperature rise with respect to the background is demonstrated. However, due to fabrication challenges of the novel thermoelectric module design, experimental validation of the integration is to be accomplished. With the introduction of an improved integration design, where the TECs bottom header sticks out from the sides

of the manifold, the difficulty in fabricating certain TEC components can be circumvented. Through collaboration with experienced thin film manufacturers, the actual integration can be realized in the future after successful fabrication of the module.

6.2.2 Thermal De-Coupling of Optical Arrays Using a Thermoelectric Cooler

Thermally de-coupling the two heat sources, electronic die and optical array, in the electronic package configuration given by Huawei is both numerically and experimentally demonstrated. Except for the dimensional limitations, all of the requirements including the thermal and electrical performance is satisfied using a bulk thermoelectric cooler. For the second phase, the same approach can be used with the obtained miniaturized bulk TECs from Marlow or thin film TEC modules from another manufacturer, which would lead to successful completion of the project with having all requirements satisfied.

6.3 Major Contributions

6.3.1 Micro-Contact Enhanced Cooling

Numerical:

- Designed possible thermoelectric coolers for successful removal of hotspot heat flux
- Proposed two alternative configurations for integration of the TFTEC into the manifold microchannel system
- The inner structure of the TEC; number of TE elements, width/thickness of the elements and operating electrical current are optimized.

- Effect of important system-level components, such as mini-contact size, mini-contact height and Cu spreader size are discussed and optimized
- Electrical/thermal short-circuiting through the manifold walls is investigated and ways to circumvent these critical issues are discussed
- Numerically investigated the implementation of Cu UBMs in ICECool design to mitigate any electromigration concerns

Experimental:

- Experimentally characterized similar state-of-the-art TFTEC modules from the subcontractor RTI/Micross using laser heating and IR thermography
- Heat flux vs. ΔT curves obtained to fine tune with the numerical simulations
- Contact resistances within the module were accurately extracted
- Tests were conducted to investigate the reliability of the TEC module in the presence of high current stressing

6.3.2 Thermal De-Coupling of Optical Arrays

Numerical:

- Modeled and investigated the given three packaging options from Huawei to observe the possible benefits/drawbacks
- Investigated ways to mitigate thermal back conduction through the surrounding layers, electrical vias and perimeter bumps
- For phase-1, the model is fine-tuned with the experimentally obtained device and system level findings for further analysis
- For phase-2, the optimum TE element thickness and electrical current to the TEC that minimizes the source temperature is investigated

Experimental:

- Device level characterization is performed on the obtained bulk thermoelectric modules
- Thermal resistance of important layers in the experimental setup (TIM, Ceramic Heater etc.) are investigated
- Laser was utilized and system level experiments with and without the presence of wire bonds(to mimic the back conduction from perimeter bumps) are performed
- Thermal de-coupling of the electronic die (mimicked by the ceramic heater) and the optical arrays (mimicked by the laser and Cu spreader) is demonstrated

6.3.3 Thermoelectric Cooling of High Power QCLs

Numerical:

- Numerically investigated the effect of electrical contact resistance on the performance of ultra-thin film thermoelectric coolers
- The optimum thickness that minimizes the source temperature and maximized the COP is explored

Analytical:

- An analytical model of the RTI's TFTEC design was built to further validate the numerical findings and the results are matched with modeling efforts from RTI

Experimental:

- Two modules with different TE element thickness is experimented to obtain device level ΔT and voltage drops
- The experimentally obtained ΔT and voltage values are used to accurately extract the Seebeck value of the P-N couple

- The device level cooling curves are obtained to validate the higher cooling flux capability of thinner elements

6.3.4 System Level Pareto-Frontiers for On-Chip Thermoelectric Coolers

Analytical:

- The concept of Pareto frontier load curve is introduced and evaluated
- Electrical and thermal parasitics present in a typical thermoelectric cooling system are incorporated into the basic thermoelectric equations
- An expression for source temperature is derived, which is only a function of the *a priori* geometry and boundary conditions (T_{sink} and Q_{source})
- A comprehensive optimization study was carried out in which the TE element thickness and electrical current is optimized to minimize the source temperature for a wide range of system structural resistances
- 3 pairs of master curves that represents the optimal thickness and electrical current for any given system architecture are established at T_{sink}=300K and 400K.

Numerical:

- A unit cell based model was created to verify the analytical model results
- A case study was performed for a power electronic cooling application, where the numerically obtained optimization variables are compared with the analytical optimization results

6.4 Publications

6.4.1 Journal Publications

1. **S.U. Yuruker**, E. Tamdogan, M. Arik "An Experimental and Computational Study on Efficiency of White LED Packages With a Thermocaloric Approach", IEEE CPMT, Volume: 7, Issue: 2, Feb 9, 2017 .

2. **S.U. Yuruker**, M.C. Fish, Z. Yang, A. Bar-Cohen, B. Yang, "System-Level Pareto Frontiers for On-Chip Thermoelectric Coolers", Frontiers in Energy, (Submitted).

3. D. Bae*, **S.U. Yuruker***, R. K. Mandel, P. Barletta, P. McCluskey, B. Yang, A. Bar-Cohen, and M. M. Ohadi, "Integration, Fabrication, and Characterization of a Micro-contact Enhanced TFTEC within a FEEDS Cooler", IEEE-CPMT, (Submitted).

4. J. Song, C. Chen, Z. Yang, **S.U. Yuruker**, Y. Kuang, T. Li, Y. Li, B. Liu, S. He, T.Gao, J.Y. Zhu, B.Yang, L.Hu "Highly Compressible, Anisotropic Aerogel with Aligned Cellulose Nanofibers", ACS Nano, (Submitted).

6.4.2 Conference Proceedings

1. **S.U. Yuruker**, M. Arik, E. Tamdogan, R. Melikov, S. Nizamoglu, D. A. Press, I. Durak "Thermal and Optical Performance of Eco-Friendly Silk Fibroin Proteins as a Cavity Encapsulation Over LED Systems", IPACK-2015.

2. **S.U. Yuruker***, D. Bae*, R. K. Mandel, P. Barletta, P. McCluskey, B. Yang, A. Bar-Cohen, and M. M. Ohadi "Integration of Micro-contact Enhanced Thermoelectric Cooler with a FEEDS Manifold Microchannel System for Cooling of High Flux Electronics", ITHERM 2017 (Outstanding Paper/Invited Talk).

3. P. Barletta, L. Diehl, M.T. North, B. Yang, **S.U. Yuruker**, N.G. Baldasaro, D.S. Temple, "Advanced thermal management of high-power QCL arrays for infrared countermeasures" (Submitted), (Invited Paper).

7 Appendices

Appendix A. Analytical Derivation of Expression for T_{source}

- The goal is to find an expression for T_{source}, as a function of the boundary conditions T_{sink}, Q_s , and the structural resistances R_{sink} and R_{source}

- To do that, first we need to eliminate the intermediate terms such as T_h,T_c,Q_h,Q_c, etc. by defining them in terms of the boundary values T_{sink} and Q_s

$$T_h = T_{sink} + R_{sink} * Q_h$$

- Q_h can be rewritten as;

$$T_h = T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff} + S * I * (T_h - T_c)\right)$$

$$T_h - R_{sink} * \left(S * I * (T_h - T_c)\right) = T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right)$$

- Subtracting T_c from each side of the equation

$$T_h - T_c - R_{sink} * \left(S * I * (T_h - T_c)\right) = T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right) - T_c$$

$$(T_h - T_c) * (1 - R_{sink} * S * I) = T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right) - T_c$$

$$(T_h - T_c) = \frac{T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right) - T_c}{1 - R_{sink} * S * I}$$

- Multiplying both sides with the conductance value “K”

$$K * (T_h - T_c) = \frac{K}{1 - R_{sink} * S * I} * \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right) - T_c\right)$$

- To get rid of the T_h completely, “$K*(T_h-T_c)$” term can be written in the form of Q_s as follows;

$$Q_s = S * T_c * I - \frac{1}{2} * I^2 * R_{eff} - K * (T_h - T_c)$$

$$K * (T_h - T_c) = -Q_s - \frac{1}{2} * I^2 * R_{eff} + S * T_c * I$$

- Substituting this into the earlier equation;

$$-Q_s - \frac{1}{2} * I^2 * R_{eff} + S * T_c * I = \frac{K}{1 - R_{sink} * S * I} * \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right) - T_c\right)$$

$$S * T_c * I = Q_s + \frac{1}{2} * I^2 * R_{eff} + \frac{K}{1 - R_{sink} * S * I} * \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right) - T_c\right)$$

- Gathering all T_c on the left side of the equation

$$S * T_c * I + \frac{K * T_c}{1 - R_{sink} * S * I} = Q_s + \frac{1}{2} * I^2 * R_{eff} + \frac{K}{1 - R_{sink} * S * I} * \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right)\right)$$

- Leaving T_c out alone

$$T_c = \frac{Q_s + \frac{1}{2} * I^2 * R_{eff} + \frac{K}{1 - R_{sink} * S * I} * \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right)\right)}{S * I + \frac{K}{1 - R_{sink} * S * I}}$$

- Writing T_c in terms of T_{source};

$$T_c = T_{source} - Q_s * R_{source}$$

$$T_{source} = R_{source} * Q_{source} + \frac{Q_s + \frac{1}{2} * I^2 * R_{eff} + \frac{K}{1 - R_{sink} * S * I} * \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right)\right)}{S * I + \frac{K}{1 - R_{sink} * S * I}}$$

- Finally, introducing a " φ " term to make the equation more concise;

$$T_{source} = R_{source} * Q_s + \frac{\left(Q_s + 0.5 * I^2 * R_{eff}\right) + \left(T_{sink} + R_{sink} * \left(Q_s + I^2 * R_{eff}\right)\right) * \varphi}{S * I + \varphi}$$

$$\varphi = \frac{K}{1 - R_{sink} * S * I}$$

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