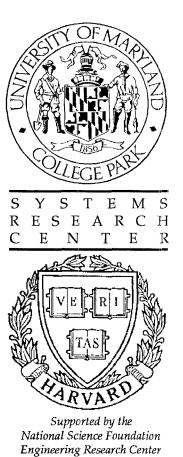
An Accurate and Efficient Approach to Statistical Simulation for Large-Scale Analog Circuits

by C.Y. Chao and L. Milor

TECHNICAL RESEARCH REPORT



Program (NSFD CD 8803012), Industry and the University

AN ACCURATE AND EFFICIENT APPROACH TO STATISTICAL SIMULATION FOR LARGE-SCALE ANALOG CIRCUITS

C.Y. Chao and Linda Milor

The System Research Center
and Department of Electrical Engineering
University of Maryland
College Park, MD 20742

Abstract

A systematic approach to statistical simulation for large scale analog circuits is presented. The statistical model takes into account mismatch between devices due to variations in the process and noise, as well as interdie variations. The number of statistical parameters is O(n), where n is the number of devices. Additionally, because large-scale analog circuits are very computationally intensive to simulate, a two level approach is used, combining a behavioral model relating block performances to circuit performances and regression models relating a set of primary statistical variables to block performances. The efficiency of this approach to statistical simulation is demonstrated with the example of an A/D converter.

1. Introduction

A accurate approach to statistical simulation of analog and digital integrated circuits is important for investigating the manufacturability of a design. Applications of statistical simulation include predicting yield, worst case analysis, design centering, and minimizing production testing time[1, 2, 3, 4]. Previous approaches to statistical simulation have mainly been developed for digital circuits. The main thrust of this work has been to identify a set of independent and primary statistical variables that explain most of the observed variation in a chip. In one approach, 4 parameters (device width(w), device length(L), oxide capacitance(Cox), flat-band voltage(Vfb)) were determined to be the critical factors responsible for the statistical variations of device characteristics and circuit performance [5, 6, 7]. In another approach, seven most important process parameters were found including W, L, Vfb, oxide thickness(Tox), substrate doping(Nsub), lateral diffusion(Ld) and junction depth(Xj)[8]. Because digital circuits are assumed, both approaches make the assumption that intradic variations are much smaller than interdic variations and therefore can be neglected without loss of accuracy. In other words, no mismatch effects are considered, only wafer to wafer and die to die process variations are considered to be important. This is not true for analog circuits.

Recently, statistical simulation for analog circuits and the issue of mismatch have been investigated in [9]. The methodology used in [9] is to model variation in the response of bipolar circuits using some critical process parameters and some mismatch pairs which were picked by the designers based on past experience. The methodology in this paper can get out of hand if the number of transistors becomes large in a circuit and too many mismatch pairs have to be considered. Suppose there are n transistors in a circuit, a total of $C_2^n = n(n-1)/2$ mismatch pairs need to be considered. In other words, the number of parameters that need to be considered by a variable screening experiment in order to find critical mismatch pairs is $O(n^2)$. In this paper, we propose a mismatch model model where O(n) process and device mismatch parameters are considered for variable screening. This approach is much more efficient than previous methods because the screening experiment is linear in complexity in

the number of variables considered. Hence, our approach requires O(n) circuit simulations in a screening experiment, as opposed to $O(n^2)$, to identify the critical mismatch pairs.

Besides the selection of critical mismatch pairs, another major problem with previous approaches to statistical simulation for large-scale analog circuits is the computational cost of simulation, especially because statistical simulation requires not one but multiple simulations and for large-scale analog circuits, even one simulation is computationally intensive. Under those circumstances, we propose a methodology of dividing a large circuit into several subcircuits using a behavioral model to build the relation between the output responses of the circuit and the performances of each sub-circuit. However because the performances of each sub-circuit are correlated, a set of independent parameters needs to be found in order to perform accurate statistical simulation. To do this, a set of independent primary process and devices parameters and mismatch parameters are assumed to explain most of the variation in the sub-circuits. A critical subset is found of these parameters for each sub-circuit using a screening experiment, after which a regression model is built relating the critical and independent variables to sub-circuit performances. In addition to process variations, the effect of noise on sub-circuit performances is included. Then for statistical simulation, instead of performing multiple circuit simulations of the sub-circuits, the regression model coupled with the behavioral model are used to perform multiple simulations. This approach is very efficient computationally.

In this paper, we begin by discussing our parametric model for interdie and intradie process variation for analog components. Based on this model, then we present our screening experiment. In the next section, we will compare three different experimental designs for screening: one variable at a time sensitivity analysis, resolution III fractional factorial design and resolution IV fractional factorial Design. In Section 3, we also present our approach for building regression models for sub-circuit performances. Finally in Section 4, we apply our methodology to a cyclic A/D converter which is simulated using a behavioral model[10], and we conclude in Section 5.

2. Two Level Parametric Variation Model

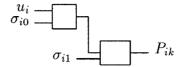


Figure 1: Two level parametric model

We begin this section by presenting some notation for the purpose of brevity of illustration. We define:

 Y_l : The circuit response of l^{th} specification (Voffset, gain ...)

 P_{ik} : The value of i^{th} process or device parameter for k^{th} device

 u_i : The mean value for i^{th} process or device parameter

 σ_{i0} : The standard deviation for i^{th} process or device parameter due to interdie variation

 σ_{i1} : The standard deviation for i^{th} process or device parameter due to intradic variation

Since the interdie variation from wafer to wafer or die to die and intradie variation within a certain die are due to many independent process steps, we can reasonably assume both variations are independent and normally distributed. For a certain process run, the interdie variation can be modeled by $N(u_i, \sigma_{i0})$. Under this process run, we also assume normally distributed intradie variations which introduce the mismatch among devices in the same die. Therefore, we propose a two level parametric model to characterize the process and device parameters for each device similar to the approach in [11] as shown in Figure 1.

For a certain process run, the two level parametric model of the i^{th} process or device parameter of the k^{th} device in an arbitrary die is described by

$$P_{ik} = u_i + \xi_j \sigma_{i0} + \eta_{ik} \sigma_{i1}$$

where i = 1, ..., n are indices of the n process or device parameters, k = 1, ..., m are indices of the m devices in a circuit, $\xi_j \sigma_{i0}$ represents interdie variation for i^{th} parameter for all devices in an arbitrary die, $\eta_{ik}\sigma_{i1}$ represents intradie variation for i^{th} parameter of k^{th} device in an

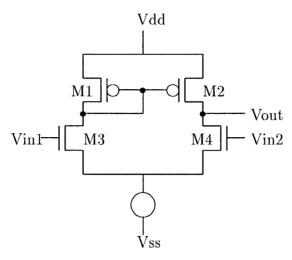


Figure 2: CMOS differential input stage

arbitrary die, ξ_j is a random number ($\in N(0,1)$), fixed in an arbitrary chip, and η_{ik} is a random number ($\in N(0,1)$)

The idea behind this model is that the interdie standard deviation, σ_{i0} , models variations between each die, where the value of a parameter in a certain die is modeled by global value $u_i + \xi_j \sigma_{i0}$, where $\xi_j \sigma_{i0}$ is the deviation of the i^{th} parameter from its global nominal and its mean value on a given chip. On this chip, the intradie standard deviation, σ_{i1} , is an additional deviation for each device by the amount of $\eta_{ik}\sigma_{i1}$. Therefore, the total deviation from nominal of the i^{th} parameter for each device is the sum of these two deviations. In this model, if a chip contains n devices, n variables model intradie variations, and hence O(n) parameters are needed to model mismatch. In order to further clarify this idea and show how to use this model to investigate the mismatch problem, we use an simple example shown in Figure 2.

To further simplify this illustration, we assume that channel length is the only critical process parameter which affects the input offset voltage of the source coupled pair in Figure 2. Let $Y = Y_l$ be the input offset voltage of the circuit, $P_k = P_{lk}$ be the value of channel length in k^{th} device, $M_{ij} = P_i - P_k$ be the mismatch in channel length between the i^{th} and j^{th} device, and let $\sigma_0 = \sigma_{i0}$ and $\sigma_1 = \sigma_{i1}$.

In this simple design, u_1 is the global mean value of the channel length of of M_1 , M_2 and u_2

is the global mean value of the channel length of M_3 , M_4 . By using the two level parametric model, we can represent the value of channel length in each device in the circuit within a certain die by

$$P_k = u_i + \xi \sigma_0 + \eta_k \sigma_1$$
 where $k = 1, \dots, 4$ and $i = 1, 2$

and the input offset voltage by

$$Y = f(\xi, M_{12}, M_{13}, M_{14}, M_{23}, M_{24}, M_{34})$$

Y could be represented by multiple linear regression using these parameters.

$$Y = a_0 \xi + a_1 M_{12} + a_2 M_{13} + a_3 M_{14} + a_4 M_{23} + a_5 M_{24} + a_6 M_{34}$$

By replacing $M_{ij} = P_i - P_j = (\eta_i - \eta_j)\sigma_1$, we get

$$Y = a_0 \xi + \sum_{i=1}^4 b_i \eta_i \sigma_1 + k$$
 where b_i and k are constants and functions of the a_i 's

We know $\eta_i \sigma_1$ is the *intradie deviation* for i^{th} device; therefore y can represented by

$$Y = f(\xi, \eta_1 \sigma_1, \eta_2 \sigma_1, \eta_3 \sigma_1, \eta_4 \sigma_1)$$

In other words,

$$Y = f($$
 global variation, intradic variations for each device.)

This idea can be extended to the general case where obviously only O(n) parameters are needed to undergo a screening experiment to find the critical independent process variables explaining most of the observed variation of a performance.

Noise can be thought of as an additive effect in the output response of a circuit. Thermal noise and flicker noise are the two most important noise sources within a device. The flicker noise and thermal noise in each device can be approximated by applying a voltage source to the gate of a transistor with mean squared values of $\frac{k\Delta f}{C_{ox}WLf}$ and $\frac{8KT\Delta f}{3g_m}$ respectively[12, 13].

Flicker noise is often the dominant noise mechanism at low frequencies. By investigating g_m and K, We can see that each individual noise source is affected by $\frac{1}{f}$, $\frac{1}{W}$, $\frac{1}{L}$, $\frac{1}{C_{ox}}$ at low frequency and $\frac{W}{L}$, C_{ox} , V_{to} , T at higher frequency.

Most of time, output deviation due to noise is negligible when compared with deviation due to the process. Based on this idea, we first test the significance of output deviation due to noise at nominal process parameters. The output deviation, denoted by Y_m , due to noise at nominal process parameters is obtained by applying a constant voltage source, which is different for each device, at the gate of each device, where the constant voltage source is calculated by adding the values of $\frac{k\Delta f}{C_{ox}WLf}$ and $\frac{8KT\Delta f}{3g_m}$ for each device.

If Y_m is negligible when comparing with the mean square deviation due to the process variations, we can neglect the deviation due to noise without loss of accuracy. Otherwise, we have to check whether the variation of noise deviation itself due to process variations is significant or not. If not, noise can be treated as an independent source of variation, in addition to the primary process parameters. Otherwise there will be some correlation between noise and process parameter variations. A test for the significance of noise variation is similar to the screening experiment for process parameters discussed earlier, where noise is a function of independent process parameters. If both tests of deviation due to noise and variation in noise are significant, we can apply the same two level parametric model here to describe the noise response at low frequency by a regression equation:

$$Y_l^{noise} = f\left(\text{ global and intradie variations of } \frac{1}{f}, \frac{1}{w}, \frac{1}{L}, \frac{1}{C_{ox}}\right)$$

At higher frequency, noise can similarly be modeled by a regression equation

$$Y_l^{noise} = f\left(\text{ global and intradie variations of } \frac{W}{L}, C_{ox}, V_{to}, T\right)$$

Therefore, the overall output response of a circuit is described by variations due to noise and the process, both of which depend on a single set of independent primary variables, obtained by screening a much larger set of independent variables coming from our two level parametric model. We now turn to the screening experiment itself.

3. The Screening experiment and Regression model

In order to build a regression model, a small subset of interdie and intradie parameters have to be found. The most common approach is one variable at a time sensitivity analysis, in which each variable is perturbated from nominal, one at a time, while others are kept at nominal values for each simulation. For n variable, a total of n + 1 simulations are needed. In addition, the amount a performance changes due to the change in each variable is found and denoted by ΔY_i , i = 1, ..., n. The total change in performance is then assumed to be the sum of the changes due to each variable

$$\Delta Y = \sum_{i=1}^{n} |\Delta Y_i|$$

where | | denotes absolute value. The contribution for each variable can be determined by the percentage change in performance due to each variable to the total change in performance due to all variables acting together, expressed by

$$\delta_i = \frac{|\Delta Y_i|}{\Delta Y} \times 100 \qquad i = 1, \dots, n$$

By comparing and ordering δ_i for each variable, we will find some significant variables which can be selected as primary parameters to be used in regression modeling. Obviously, in using this model when determining the sensitivity (δ_i) to one variable, the impact of others, varying within tolerance, is not considered.

A more accurate approach would be to simulate the circuit at all vertices of a hypercube(factorial analysis) [14], where vertices at the hypercube are defined by positive and negative extremes of each parameter. Since the sensitivity of each parameter can be affected by the settings of other parameters, the impact of other parameters varying within tolerance is taken into account by computing an average of sensitivity over tolerance box, defined by positive and negative extremes of all parameters. Let v_k , $k = 1, ..., 2^n$ be the vertices of the hypercube, located at various combinations of the positive and negative extremes of parameters. Let J^+ be the set of vertices with the j^{th} parameter at its positive extreme, and its complement J^- be the set with the j^{th} parameter at its negative extreme. Then the impact of changing each variable can be found by computing the difference between the average performance on opposite faces of the hypercube, J^+ and J^- . The total change in Y, ΔY , is

$$\Delta Y = \frac{\left(\sum_{k \in J^+} Y_i(v_k) - \sum_{k \in J^-} Y_i(v_k)\right)}{2^{n-1}}$$

However if there are n parameters, 2^n circuit simulations are required for this approach, which is not usually feasible and will not be adopted in this paper.

A more efficient approach, which takes into account the variations of a sensitivity within tolerance is fractional factorial experimental design. For a fractional factorial experimental design, simulations are made at carefully selected vertices of the hypercube, making sure that equal numbers are in the sets J^+ and J^- for each of the n parameters. The fractional factorial design which requires fewest simulations is a resolution III design. The number of simulations required is 2^l , where $2^l \leq n$. Sensitivities of performance to each variable are obtained by

$$\Delta Y = \frac{(\sum_{k \in J^+} Y_i(v_k) - \sum_{k \in J^-} Y_i(v_k))}{2^{l-1}}$$

Since the main effects are confounded with two-factor interaction effects in a resolution III fractional factorial design, a resolution IV fractional factorial design is proposed to avoid the confounding between main effects and two-factor interaction effects, but number of simulation needed is twice as many as the resolution III, 2^{l+1} . Once the sensitivities are computed using either resolution III or resolution IV experimental designs, the variables can be ranked, as was done with sensitivity analysis. Clearly, sensitivity analysis and resolution III fractional factorial experimental designs require fewer simulations than the resolution IV fractional factorial design. On the other, the resolution IV fractional experimental design is more accurate than the resolution III fractional factorial design. However, it is difficult to compare

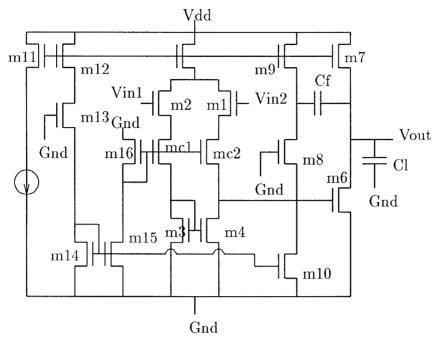


Figure 3: Two stage OP amp

the fractional factorial design with one variable at a time sensitivity analysis without empirical data.

As an illustration, we use the example [15] shown in Figure 3. Let $L_i = \xi \sigma_{i0}$ be the interdie variation for i^{th} parameter such as length reduction,...etc, $S_i = \eta_{i1}\sigma_{v_{to}1} + \eta_{i2}\sigma_{\frac{w}{l}1}$ be the intradic variation for i^{th} device, and the variables l_i and s_i be normalized variables corresponding to L_i and S_i , obtained by dividing L_i and S_i by $3\sigma_{i0}$ and $3\sigma_{v_{to}1} + 3\sigma_{\frac{w}{l}1}$ respectively.

In this example, the interdie variables that we have included in our model are W, L, T_{ox} , N_{sub} , L_d , X_j , and V_{to} (zero-bias threshold voltage). Except for T_{ox} , these parameters have been assumed for n-channel add p-channel devices. We could have supplemented our model with a small deviation in each of these parameters for each device to model mismatch. However in our example, as in many circuits, most mismatch can be traced to deviation in drain currents [16]. Hence we can further reduce the intradic parameters into a smaller set composed of $\frac{W}{L}$, T_{ox} , u_n and V_{to} . Furthermore, by investigating our example in Figure 3, we

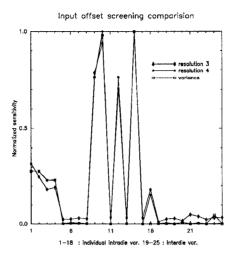


Figure 4: Screening result of input offset voltage

have found intradie variations of the $\frac{W}{L}$ ratio and V_{to} to be dominant effects over T_{ox} and u_n in generating mismatch between devices. Therefore, we only consider the $\frac{W}{L}$ ratio and V_{to} as sources of intradie variations and include these two variations as an individual parameter related to each device. Based on this idea, all the screening experiments were completed.

We have applied three screening methods to four parameters (gain, output resistance, transconductance and input offset voltage) of this circuit and the comparison of the three screening methods for *input offset* voltage is shown in Figure 4. From this figure, we can find that there is no significant difference in all three methods. All three methods give almost the same critical parameters but only differ in the *ranking*.

As we can see in Figure 4, The ranking of critical parameters for the input offset voltage is

Sensitivity analysis 1^{st} group s_{14} s_{10} s_{9} s_{12} 2^{nd} group s_{2} s_{1} s_{4} s_{3}

Resolution III 1^{st} group s_{14} s_{10} s_{9} s_{12} 2^{nd} group s_{1} s_{2} s_{4} s_{3}

Resolution IV 1^{st} group s_{14} s_{10} s_{9} s_{12} 2^{nd} group s_{2} s_{1} s_{4} s_{3}

After the critical process, device and mismatch parameters are found by screening experiment, we then begin fitting regression model for each response as a function of the critical

independent process parameters by assuming a generalized linear model of the form:

$$Y_l = \beta_0 + \sum_{i=1}^p \beta_i l_i + \sum_{i=1}^r \alpha_i s_i$$

In order to generate an accurate regression model and to test lack of fit, we follow two principles:

- (1) N points are generated according to a Latin hypercube—design by selecting the value randomly from each of N intervals formed by dividing up the range of each critical variable. The N points are obtained by randomly pairing the values of each critical variable.
- (2) Noncritical variables are varied randomly to be used in the estimation of pure error in the regression model.

The criteria to test the adequacy of this model are

$$F_{model} = \frac{MS_{reg}}{MS_{residue}} \ge F_{k-1,n-k,1-\alpha}$$
 Significant test
$$F_{LOF} = \frac{MS_{LOF}}{MS_{PE}} \le F_{r-k,n-r,1-\alpha}$$
 Lack of fit test
$$R^2 = \frac{SS_{regression}}{SS_{corrected total}} \ge 0.9$$
 Percentage explained by model

From the screening experimental design, the parameters in 1^{st} group are more significant than those in 2^{nd} group which are more significant than the rest. The parameters in the 1^{st} group are chosen to be the primary independent variables in the multiple linear regression model initially. If the three criteria of regression model can not be met, the variables in 2^{nd} group are added using a stepwise regression technique which add the most important variables from 2^{nd} group to the multiple linear regression model one at a time. If the three criteria are met after adding a variable from 2^{nd} group, the generalized linear model is adequate and we can stop here. Failure to meet three criteria in the linear model will force us to use a more complicated model:

$$Y_{l} = \beta_{0} + \sum_{i=1}^{p} \beta_{i} l_{i} + \sum_{i=1}^{r} \alpha_{i} s_{i} + \sum_{i=1}^{k} \sum_{j=1}^{k} \beta_{ij} l_{i} l_{j} + \sum_{i=1}^{k} \sum_{j=1}^{k} \alpha_{ij} s_{i} s_{j} + \sum_{i=1}^{k} \sum_{j=1}^{k} \gamma_{ij} l_{i} s_{j} + \ldots + \epsilon$$

Testing the adequacy of this complex model is more complicated. We propose to use sequential regression analysis by testing the significance of each β_{ij} , α_{ij} and γ_{ij} . This significant test is done by testing F statistics of the extra sum of square for each step in sequential regression analysis. The three criteria above are still valid for each step in sequential regression analysis and can be used as stopping criterions in this analysis.

The regression models for four relevant responses are

$$Y_{offset} = -0.0009118 + 0.00706333 \ s_{10} - 0.00615897 \ s_{12} - 0.00604082 \ s_{14}$$

$$+0.005967247 \ s_9 + 0.00374926 \ s_2 - 0.00149385 \ s_1$$

$$Y_{gain} = +13973.94 - 1791.72 \ T_{ox} + 810.86 \ l - 335.17 \ N_{sub}$$

$$+300.57 \ s_{10} + 223.31 \ V_{to} - 58.88 \ s_{14}$$

$$Y_{ro} = +9.298618 + 0.637372 \ T_{ox} - 0.5258596 \ s_7 + 0.5192886 \ s_{11}$$

$$+0.3073354 \ l - 0.3005598 \ v_{to} + 0.1817653 \ s_{14} + 0.0469412 \ N_{sub}$$

$$Y_{gm} = +0.059298160 - 0.004253116 \ t_{ox} - 0.00180258 \ L + 0.00165234 \ V_{to}$$

$$-0.00135140 \ s_{11} - 0.001551701 \ s_{14}$$

The ANOVA table for *Input offset* is:

Source	SS	df	MS	F_{test}	F_{cri}	Significant
Model	0.000603835	6	0.000100639	163.085	3.87	YES
Error	0.00000431986	7	$6.1709e^{-7}$			
Lack of Fit	0.00000117986	3	$3.93e^{-7}$	0.501	6.26	NO
Pure Error	0.000003140	4	$7.87e^{-7}$			
R^2				0.9929	0.9	YES

The ANOVA table for Gain is:

Source	SS	df	MS	F_{test}	F_{cri}	Significant
Model	14966357.18	6	2494392.86	230.865	3.87	YES
Error	75632.01	7	10804.57			
Lack of Fit	26240.00	3	8746.67	0.885	6.26	NO
Pure Error	49392.41	4	9878.48			
R^2				0.9950	0.9	YES

The ANOVA table for Output resistance is:

Source	SS	df	MS	F_{test}	F_{cri}	Significant
Model	115.70264	7	16.5289484	832.236	4.21	YES
Error	0.1191653	6	0.01986088			
Lack of Fit	0.0369120	2	0.0184560	0.897	6.94	NO
Pure Error	0.0822534	4	0.0205634			
R^2				0.9990	0.9	YES

The ANOVA table for Transconductance is:

Source	SS	df	MS	F_{test}	F_{cri}	Significant
Model	0.000117216	6	16.5289484	126.575	3.87	YES
Error	0.0000010804	7	0.000000154			
Lack of Fit	0.000000290	3	0.000000096	0.780	6.26	NO
Pure Error	0.000000790	4	0.000000263			
R^2				0.9909	0.9	YES

Note that from all the above discussion, we have shown that there are little difference in the screening experimental design when variables are to be used only in a linear regression model. If a complicated model is needed, we need to have some information on the two-factor interaction effects of some variables. In our investigation, we found the two-factor interaction effects of a smaller set formed by variables in the 1^{st} and 2^{nd} groups, using a screening experiment, are more significant than any other interaction effects. Based on this observation and above discussion, we propose a efficient and complete algorithm to fit a regression model.

The algorithm:

- Step 1. Apply a resolution III fractional factorial design to do a screening experiment. The number of simulations needed is 2^l , where $2^l \ge n$, n is the number of parameters.
- Step 2. Discard insignificant parameters and obtain a reduced set of m parameters, formed by the 1^{st} and 2^{nd} group in our results, where $m \ll n$.
- **Step 3.** Apply regression analysis to build a multiple linear model using the parameters in a reduced set. Three criteria are used as stopping criteria here. If the three criteria are met, stop.
- Step 4. If the three criteria are not met in step 3, apply a resolution IV screening experiment to the parameters of the reduced set, formed in step 2, and extract the significant higher order effects of these parameter (usually the interaction effects are enough). The number of

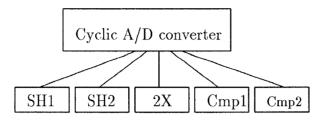


Figure 5: Block Decomposition

simulation needed is $2^{\alpha+1}$, where $2^{\alpha} \geq m$

Build a regression equation using sequential regression analysis. Even in the worst case, the total number of simulations needed in the whole run is $2^l + 2^{\alpha+1} + N$ which is less than the 2^{l+1} needed in resolution IV fractional factorial design, if $m \leq \frac{n}{4} - \frac{N}{2}$, which is usually true.

4. High level decomposition

A large analog circuit is not usually simulatable using standard circuit simulation tools. Instead the design is partitioned functionally, components are simulated using standard tools, and a behavioral model is built for system simulation relating component performances to system performances. The behavioral model forms a bridge between the performances of each sub-block and the system. Because statistical simulation requires multiple simulations and multiple simulations are computationally intensive even for the sub-blocks, we can apply the algorithm we developed in Sections 3 and 4 to obtain performance models for each sub-block with high accuracy. The performance models for the sub-blocks form a front end to the behavioral model and the output responses of whole circuit can be computed for nominal and statistically varying process and device parameters. Since interdie variations, mismatch and noise effects have been considered in building the performance model for each sub-block, the overall circuit responses are a function of all of these effects.

This approach has been applied to a cyclic A/D converter[10]. We begin by partitioning the cyclic A/D converter into several sub-blocks. The partitions are shown in Figure 5. Basically, all the sub-blocks in our example are formed by an op amp and some switching

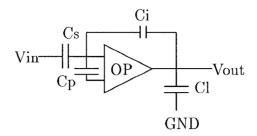


Figure 6: Sample Block

capacitors as shown in Figure 6. Then a behavioral model is built to relate the outputs of the A/D converter to performances from each sub-block. We have used the behavioral model developed in [10]. For complex blocks, like the op amps, sub-block output responses are used as inputs of the behavioral model. In this cyclic A/D converter, for the op amp we need input offset voltage, transconductance, output resistance and gain. This step involves building a parametric statistical model for each of the sub-block performances, as outlined in Section 3. For simple blocks, the relation between critical parameters and block performance can be obtained by circuit simulation or analytically.

The behavioral model coupled with the front end relating primary process parameters to block performances can be used by a Monte Carlo algorithm to efficiently compute statistics of the performances of the circuit. The independent parameters used in the regression equations should be varied according to their distributions. This approach has been applied to the cyclic A/D converter to obtain a statistical distribution diagram of the code transitions. The A/D converter has 256 codes. To demonstrate the accuracy of our approach, Figure 7 shows the statistical distribution of 5 code transitions computed using our method. Our results are compared with a statistical distribution obtained by combining detailed circuit simulation for the components and the behavioral model. It can be seen that our results are very accurate. Furthermore our approach required 28.90 seconds on a IPX SUN workstation to generate 10 points, while coupling a circuit simulation to a behavioral model required 817.50 seconds to generate 10 points.

Finally it should be noted that our approach to statistical simulation is not limited to

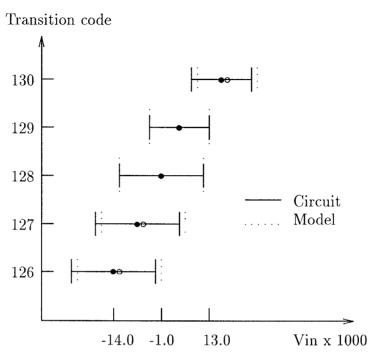


Figure 7: Statistical distribution of code transitions

applications involving Monte Carlo analysis. Deterministic algorithms used for worst case analysis and design centering can also use our approach to statistical simulation.

5. Conclusion

A systematic and efficient approach to statistically simulate large-scale analog integrated circuits has been presented and applied to the example of a cyclic A/D converter. The approach involves dividing the circuit into sub-blocks where a behavioral model relates sub-block performances to circuit performances. Secondly, performance models relating an independent set of primary process parameters to sub-block performances are built using regression techniques. Statistical simulation is then done by coupling the behavioral simulation with the regression models, and the accuracy of the approach depends both on the accuracy of the behavioral simulation and the regression models.

In addition to our two-stage approach to statistical simulation, a novelty is our handling of mismatch in analog circuits. For a circuit containing n devices, we require O(n) parameters to model mismatch among devices. This is especially important because these parameters are

inputed to a variable screening algorithm that requires at least one simulation per variable.

In developing our regression models, which are used in statistical simulation, we have compared three approaches to screening: one variable at a time sensitivity, resolution III fractional factorial design and resolution IV fractional factorial design. We have found that the best approach to screen variables is to use resolution III initially to obtain a reduced set which can be used as primary variables in a linear regression model. If our three stopping criteria can not be met by a linear model, a resolution IV fractional factorial design is applied to the reduced set to find important higher-order interaction components as primary variables in a higher order regression model.

Acknowledgements

The authors wish to thank Gani Jusuf for providing the A/D converter and its behavioral model.

References

- [1] L. Milor and A. Sangiovanni-Vincentelli, "Computing parameter yield accurately and efficiently," in *Proc. ICCAD*, pp. 116–119, 1990.
- [2] V. Visvanathan, "Variation analysis of integrated circuits," in *Proc. ICCAD*, pp. 228–231, 1986.
- [3] D. E. Hocevar, P. F. Cox., and P. Yang, "Parametric yield optimimization for mos circuits," *IEEE Trans. Computer-Aided Design*, vol. 7, pp. 645-658, June 1988.
- [4] L. Milor and A. Sangiovanni-Vincentelli, "Optimal test set design," in *Proc. ICCAD*, pp. 294–297, 1990.
- [5] P. Cox, P. Yang, S. Manhant-Shetti, and P. Chatterjee, "Statistical modeling for efficient parametric yield estimation of mos vlsi circuits," *IEEE J. of Solid-State Circuits*, vol. SC-20, pp. 391–398, Feb. 1985.

- [6] P. Yang, D. E. Hocevar, P. F. Cox, C. Machala, and P. K. Chatterjee, "An integrated and efficient approach for mos vlsi statistical circuit design," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 5–14, Jan. 1986.
- [7] T. K. Yu, S. M. Kang, I. H. Hajj, and T. N. Trick, "Statistical performance modeling and parametric yield estimation of mos vlsi," *IEEE Trans. Computer-Aided Design*, vol. CAD-6, pp. 1013–1022, Nov. 1987.
- [8] S. Liu and K. Singhal, "A statistical model for mosfet," in Proc. ICCAD, pp. 78–80, 1985.
- [9] N. Salamina and M. R. Rencher, "Statistical bipolar circuit design using mstat," in Proc. ICCAD, pp. 198–201, 1989.
- [10] G. Jusuf, P. R. Gray, and A. Sangiovanni-Vincentelli, "Cadics-cyclic analog-to-digital converter synthesis," in *Proc. ICCAD*, pp. 286–289, 1990.
- [11] C. J. B. Spanos and S. W. Director, "Parameter extraction for statistical ic process characterization," *IEEE Trans. Computer-Aided Design*, vol. CAD-5, pp. 66–78, Jan. 1986.
- [12] P. R. Gray and R. G. Meyer, Analysis and Design of Analog Integrated Circuits. John Wiley and Sons. Inc., 1984.
- [13] R. Gregorian and G. C. Temes, Analog MOS Integrated Circuits for Signal Processing. John Wiley and Sons. Inc., 1986.
- [14] G. E. P. Box, W. G. Hunter, and J. S. Hunter, Statistics for Experimenters. John Wiley and Sons. Inc., 1980.
- [15] H. Y. Koh, C. H. Sequin, and P. R. Gray, "Automatic synthesis of operational amplifiers based on analytic circuit models," in *Proc. ICCAD*, pp. 502–505, 1987.

[16] K. R. Lakshmikumar, R. A. Hadaway, and M. A. Copeland, "Characterization and modeling of mismatch in mos transistors for precision analog design," *IEEE J. of Solid-State Circuits*, vol. SC-21, pp. 1057–1066, Dec. 1986.