ABSTRACT

Title of Thesis: MINIATURE THERMOELECTRIC COOLERS FOR ON-CHIP HOT SPOTS

Viatcheslav Litvinovitch, Master of Science, 2009

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Following Moore's Law, semiconductor transistor density has doubled roughly every 18 months to alleviate increasing IC performance demands. Growing microprocessor complexity and performance, coupled with the functional integration of logic and memory components in chip architecture, have led to highly non-uniform on-chip power distribution. The resulting localized high heat flux "hot spots" are becoming a major difficulty due to their propensity for degrading microprocessor performance and for significantly reducing chip reliability.

Most conventional cooling techniques provide uniform cooling to the device and do not focus much attention on the hot spots themselves. Therefore, other innovative and novel thermal management techniques must be explored to aggressively and selectively combat the deleterious effects of on-chip hot spots. This thesis explores two previously proposed thermal management techniques utilizing thermoelectrics to cool on-chip hot spots: the silicon microcooler with an integrated SiGe superlattice layer and the mini-contact enhanced conventional thermoelectric cooler (TEC).

# Miniature Thermoelectric Coolers for On-Chip Hot Spots

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# 1. Introduction

## 1.1 Description of hot spot problem and motivation for research

In the 1970's, Moore predicted that semiconductor transistor density would double roughly every 18 months in an effort to alleviate ever increasing IC performance demands. This trend, also known as Moore's Law, has proven itself to be an accurate forecast of future development in the IC packaging industry. The 2005 International Technology Roadmap for Semiconductors (ITRS), shown in figure 1.1, illustrates projected logarithmic increases in on-chip transistor density and logarithmic decreases in feature size over the next ten years, while chip size is expected to remain unchanged [1]. Smaller feature sizes on semiconductors lead to faster and more functional chips, although at the penalty of greater on-chip power dissipation. As a result of ever escalating chip power, elevated chip temperatures are becoming a significant problem that must be addressed.

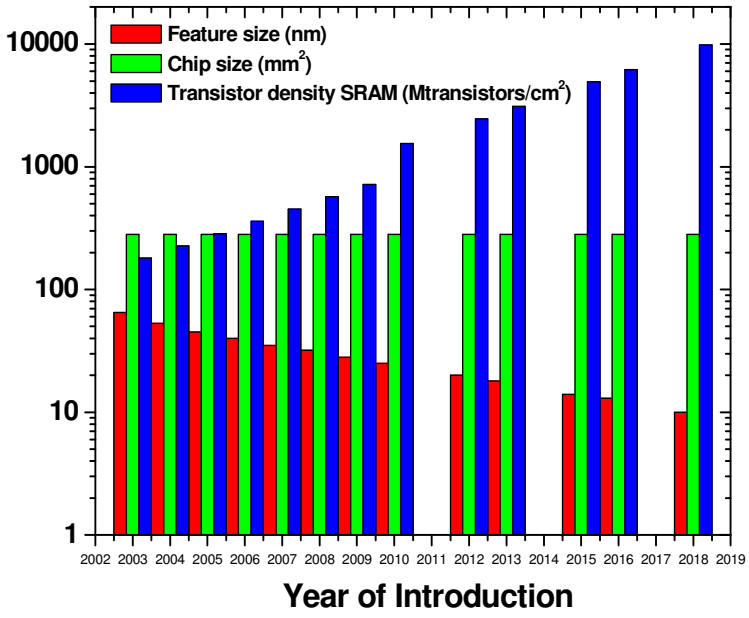



**Figure 1.1: The 2005 ITRS predictions of feature size, chip size and transistor density for high performance microprocessor chips [1]**

Thermal management issues in IC packaging will be a key design driver in the next generation of semiconductor microprocessors. New and innovative thermal solutions will have to be developed to overcome the hurdle of rapidly growing on-chip heat generation that limits current device clock speeds and feature sizes. Precise temperature control is necessary in many of today's applications where performance depends on chip temperature uniformity, such as in power electronics and microprocessors. Performance may also be temperature sensitive, such as in IR detectors and semiconductor lasers, where device material properties often change with temperature.

In addition to performance concerns, reliability can also be expected to degrade in overheated devices. Some failure mechanisms, such as electromigration, are temperature dependent and can adversely affect device reliability at elevated temperatures. Also, transistor gate leakage current increases exponentially with temperature [2]. A relation for the mean time to failure (MTF) in semiconductor devices is given by Black's equation [3]:

$$MTF = AJ^2 \exp(\frac{E_A}{k_B T}) \tag{1.1}$$

where A is a constant, J is the current density, $E_A$ is the active energy where the value for typical silicon failures is approximately 0.68eV, $k_B$ is Boltzmann's constant and T is the absolute operating temperature. It had been observed that even a 5-10K overall temperature reduction can double the device reliability, in the normal operating temperature range [4].

Thermal challenges in microprocessor packaging are likely to intensify as chip power dissipation levels are expected to climb in upcoming years. The 2006 iNEMI roadmap for maximum chip power of high performance servers shows that chip power

levels will soon reach over 500W (figure 1.2) [5]. The thermal barrier doesn't necessarily reside in coping with such high power levels, but in managing the uneven distribution of this power.

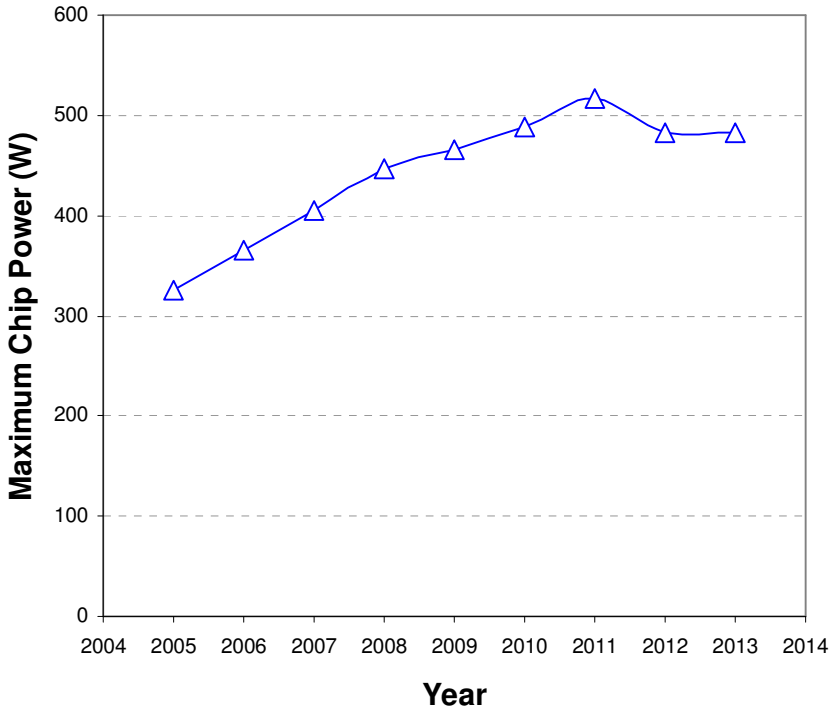



**Figure 1.2: 2006 iNEMI road map for chip power in high performance servers [5]**

Today's microprocessors accommodate many functional blocks that can produce an average heat flux of about 10 ~ 50 W/cm$^2$ and a peak flux that can reach six times that of the surrounding areas [6]. Growing microprocessor complexity and performance, coupled with the functional integration of logic and memory components in chip architecture, have led to highly non-uniform on-chip power distribution. The resulting localized high heat flux "hot spots" are becoming a major difficulty due to their propensity for degrading microprocessor performance and for significantly reducing chip reliability.

Examples of on-chip hot spots are shown in figures 1.3 and 1.4. Figure 1.3 shows two different Intel chips containing hot spot regions [7] and figure 1.4 shows a typical on-chip heat flux map with accompanying temperature map [8].

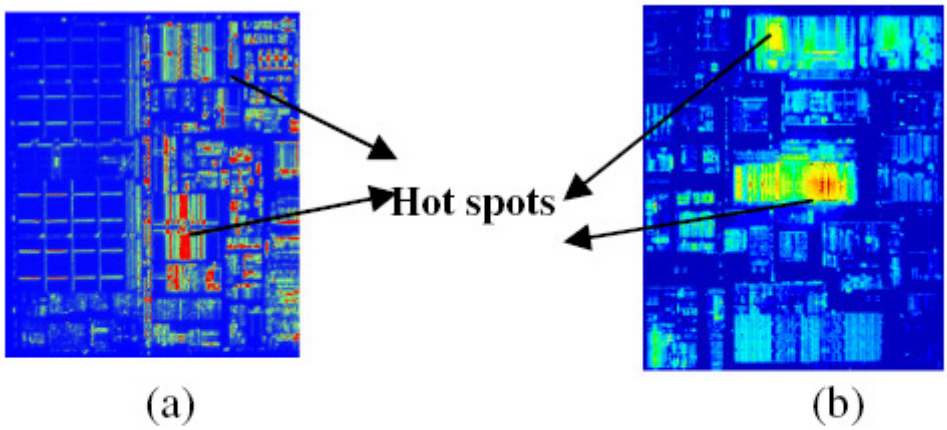



**Figure 1.3: Hot spots resulting from non-uniform power on an Intel Pentium ® III processor (a) and an Intel Itanium ® processor [7]**

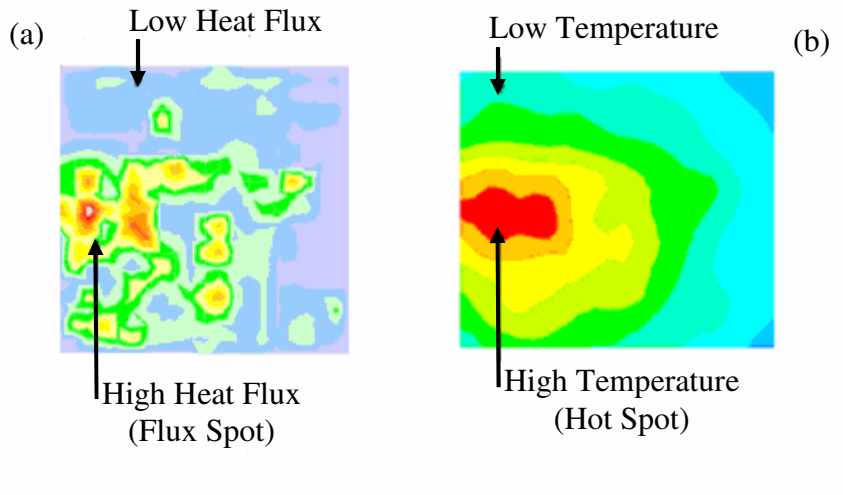



**Figure 1.4: Schematic illustrating typical die power map (a) and hot spot on the corresponding temperature map (b) [8]**

Hot spots often drive the thermal design of the IC package because often they constitute the maximum on-chip junction temperatures (depending on the application,

maximum junction temperatures will be in the range of 90 to 110°C) [9]. Most conventional cooling techniques provide uniform cooling to the device and do not focus much attention on the hot spots themselves. This often results in unnecessarily overcooling the rest of the chip in an effort to bring down hot spot temperatures. Therefore, other innovative and novel thermal management techniques must be explored to aggressively and selectively combat the deleterious effects of on-chip hot spots.

## 1.2 Overview of Thermal Management Techniques

### 1.2.1 Passive Cooling

Passive cooling is one of the most commonly used thermal management techniques in today's IC packaging technology. This method relies mainly on heat conduction, spreading, and natural convection. Research in passive cooling focuses on engineering high thermal conductivity materials and low thermal resistance interfaces. Advantages of passive cooling include low complexity, low cost and high reliability, while some disadvantages may include low heat removal, bulkiness, and the inability to cool below ambient temperature. Some examples of passive cooling techniques include heat spreaders, natural convection heat sinks, pool boiling, and reconfiguring the chip architecture to achieve a more uniform heat dissipation and to take maximum advantage of conduction spreading.

### 1.2.2 Active Cooling

Active cooling is typically more expensive than passive cooling and involves moving parts and/or the input of electrical power. This method actively pumps heat from a heat source to a heat sink. Some common forms of active cooling involve fan cooled

heat sinks, fluid pumped through microchannels, and jet impingement cooling. Thermoelectric coolers, or TECs, are also a form of active cooling and offer a unique and promising solution to the hot spot problem. Some advantages of TECs include their solid state design, the absence of moving parts, high reliability, and their capability to selectively target and cool hot spots.

Recently, Chowdhury *et al* demonstrated that a high heat flux on-chip hot spot could be cooled by 15°C using an integrated miniature thermoelectric cooler [10]. This advancement in chip scale cooling was achieved by a 3.5mm x 3.5mm thin film TEC (TFTEC) with only a ~100µm total device thickness. The thermoelectric material within the device consisted of 5-8µm thick p-type $Bi_2Te_3/Sb_2Te_3$ and n-type $Bi_2Te_3/Bi_2Te_{2.83}Se_{0.17}$ superlattices that were grown by metal–organic chemical vapor deposition (MOCVD) on GaAs substrates [10]. Figure 1.5 shows a thermal image of the Si chip with a localized heater that simulates the active hot spot to be cooled by the miniature thermoelectric cooler (heat spreader and TEC are not shown). In this study, the 400µm x 400µm hot spot produced a heat flux of 1250W/cm$^2$.

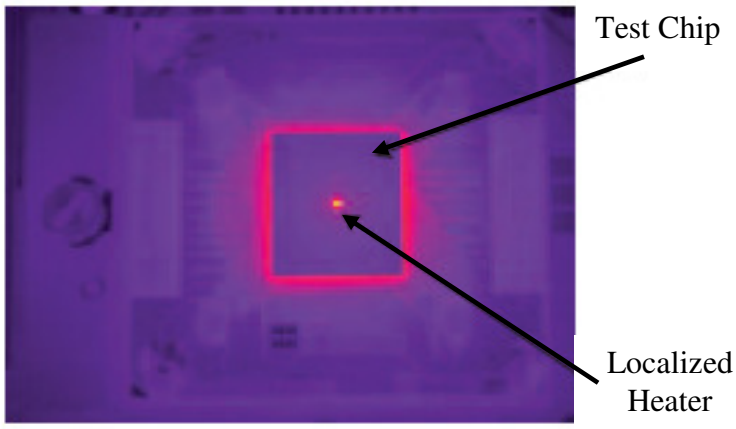



**Figure 1.5: Infrared image of the test chip when only the localized, high heat flux, "hot spot" heater is powered [10]**

Since miniaturized thermoelectric devices can be focused directly on the hot spots and not overcool the rest of the device, they offer a distinctive and energy efficient way of cooling on-chip semiconductor hot spots. Moreover, this technology has been experimentally demonstrated to work and yield significant hot spot temperature reductions. In order to understand the physics behind thermoelectrics, a brief overview is provided in the next section.

#### 1.2.2.1 Principles of Thermoelectrics

The thermoelectric effect can be described as the conversion of energy between electricity and heat. There are three types of thermoelectric effects that occur: the Seebeck effect, the Peltier effect, and the Thomson effect. These effects are found to be thermodynamically reversible and act in conjunction with irreversible effects such as Joule heating and thermal conduction.

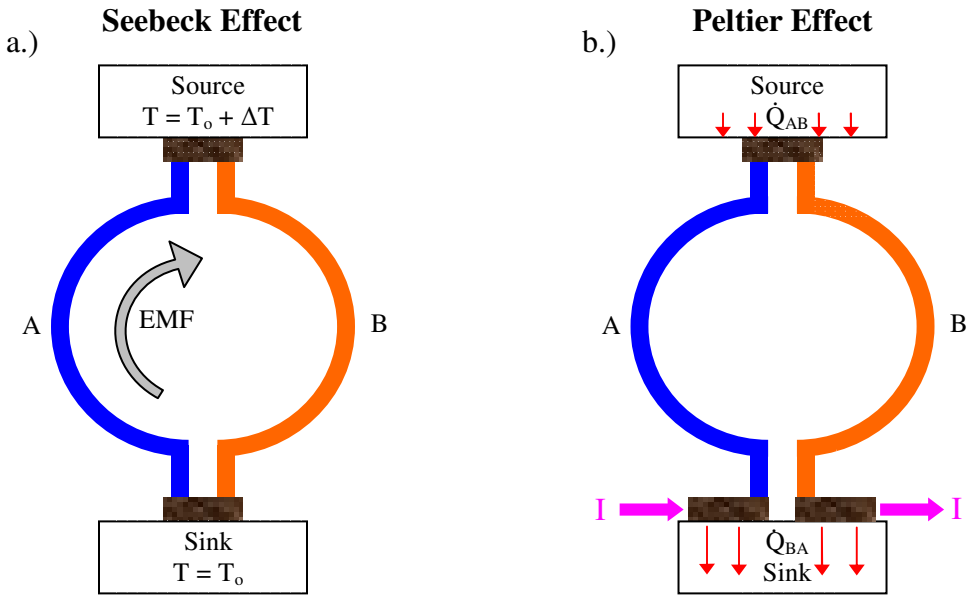



**Figure 1.6: Conceptual schematic of the Seebeck effect (a) and the Peltier effect (b) [12]**

The Seebeck effect occurs when two dissimilar conductors are joined at two points that are maintained at different temperatures. An electromotive force will develop over the closed loop that can be measured by inserting a voltmeter into the loop; it is also known as the thermocouple voltage [11].The Seebeck effect for materials A and B, shown in figure 1.6a, is interfacial and arises when charge carriers in a conductor are exposed to a temperature gradient within the conductor. The hotter electrons will diffuse more readily than colder electrons and tend to migrate to the colder area. This produces an electric flow of current that lasts as long as there is a temperature difference along the conductor.

The Peltier effect is the principal effect concerned with thermoelectric refrigeration or heat pumping. This effect is also interfacial and transports heat between two different conductors, from one junction to another, when an electric current passes through the closed loop circuit. In figure 1.6b, heat is absorbed at one junction and carried to the other. The Peltier heat is linear with respect to current, in contrast to the irreversible Joule heat, which is quadratic with respect to current. The rate at which heat is absorbed is proportional to the current and depends on the nature of the two materials comprising the junction. Compared to the Seebeck effect, where heat flow induces an electric current, the Peltier effect is opposite, with an electric current induced a heating or cooling effect.

Also noteworthy is the Thomson effect, which is a bulk effect that transports heat within a current carrying material at one temperature to the same material at a different temperature (i.e. in a material with a temperature gradient). Phonons and electrons act as the two modes of heat transfer and this effect can be thought of as the

evolution/absorption of heat in a conducting material whenever a current traverses that material with a temperature gradient, thereby transporting electrons of one temperature to a zone with electrons at another temperature. Thomson heat, like the Peltier heat, is reversible and is in addition to any irreversible Joule heat [11].

A conventional thermoelectric device is typically comprised of an array of p- and n-type semiconductor materials that are oriented in series electrically but in parallel thermally. A high conductivity metal such as copper is typically used to electrically connect the semiconductor pillars and complete the electric circuit. This circuit is usually sandwiched between two ceramic substrates that are electrically insulated but thermally conductive, such as AlN. Schematics of a thermoelectric cooler and thermoelectric generator are shown in figures 1.7a and 1.7b, respectively. Bismuth telluride ($Bi_2Te_3$) and its alloys are commonly used as the semiconductor materials in many applications because of their high thermoelectric properties, reflected in the commonly-used thermoelectric metric ($Z = S^2/\rho k$) at near room temperature, which is described later. In particular, $Bi_2Te_3$ shows the best thermoelectric properties at the desired temperature range for on-chip thermal management [13].

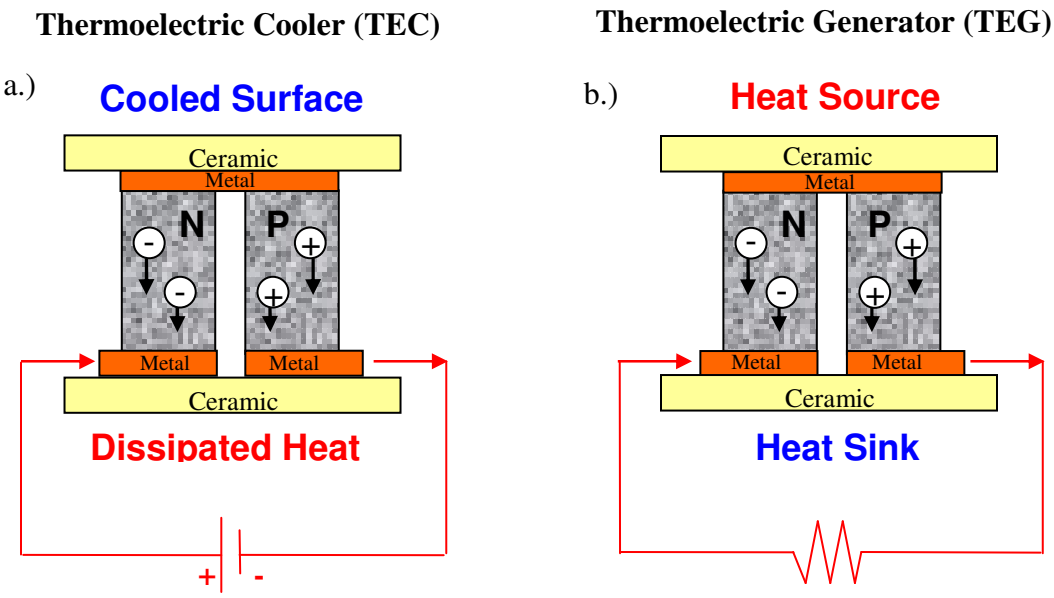



**Figure 1.7: Functional diagram of a thermoelectric cooler (a) and thermoelectric generator (b)**

Since the goal of this thesis is to utilize thermoelectrics as heat pumps, the Peltier effect will be of most interest. Equation 1.2 shows the defining function that describes the Peltier effect [11]:

$$Q = (S_p - S_n)T_cI - \tfrac{1}{2}I^2R - K(T_h - T_c) \qquad (1.2)$$

where Q is the net rate of heat transfer in watts, $S_n$ and $S_p$ are the Seebeck coefficients for the negative and positive thermoelectric legs, respectively, $T_c$ and $T_h$ are the temperatures at the cold and hot sides of the TEC, respectively, I is current, R is the electrical resistance, and K is the thermal conductance. This equation shows the competition between the Seebeck coefficient term, which is responsible for TEC cooling, and the parasitic effects of Joule heating and back heat conduction from the electrical resistance and thermal conductance terms, respectively. The power input in watts required to produce the effect described in (1.2) can be written as [11]:

$$W = I^2R + (S_p - S_n)(T_h - T_c)I \quad (1.3)$$

and the coefficient of performance for a TEC heat pump can be written as:

$$COP = Q/W \quad (1.4)$$

The COP is a common metric used to quantify the effectiveness of a heat engine. It is also important to quantify the amount of heat that a TEC can transfer and the maximum temperature difference across the TEC. Derived from the efficiency equation of a TEC, the equation for maximum heat flux pumping capability can be written as [14]:

$$q_{max} = \frac{1}{L}\left[\frac{S^2T_c^2}{2\rho} - k(T_h - T_c)\right] \quad (1.5)$$

and the maximum temperature reduction across the TEC can be estimated as:

$$\Delta T_{max} = \frac{S^2T_c^2}{2k\rho} = \frac{ZT_c^2}{2} \quad (1.6)$$

where L is the height of the thermoelectric legs, ρ is the electrical resistivity, and k is the thermal conductivity. Equations 1.5 and 1.6 imply having thin TE legs and maximizing the $S^2T/\rho k$ term, which is commonly known as the thermoelectric figure of merit (ZT), reflected in equation 1.6.

#### 1.2.2.1.1 Thermoelectric Figure of Merit

The thermoelectric figure of merit (ZT) is a dimensionless parameter used to assess the usefulness of a semiconductor for use in thermoelectric heat engines. This

parameter is derived from the efficiency equation of the thermoelectric device and combines the coefficients of the electrical and thermal properties of the semiconductor materials. A principal aim of research and development in thermoelectric materials is to fabricate semiconductors having a value as high as possible for the figure of merit over the applicable temperature range of the device [12]. The terms Z and T are shown in equations 1.7 and 1.8 respectively, where T is the mean temperature of the TE leg [11].

$$Z = \left[ \frac{S_p - S_n}{\sqrt{k_p \rho_p} + \sqrt{k_n \rho_n}} \right]^2 \tag{1.7}$$

$$T = \frac{T_c + T_h}{2} \tag{1.8}$$

When the positively and negatively charged thermoelectric semiconductor materials have similar thermal and electrical properties, Z can be written in a more simplified form:

$$Z = \frac{S^2}{\rho k} \tag{1.9}$$

where S, ρ, and k are the average Seebeck coefficients, electrical resistivities, and thermal conductivities of the p- and n-type elements. In equation 1.9, k is kept low to reduce conduction from the hot side back to the cold side, ρ is kept low to reduce Joule heating, and S is kept high to get the greatest possible temperature difference per given amount of electrical potential (voltage), or vice versa.

Recent advancements in improving ZT values include the work of Poudel *et al*, who achieved a peak ZT of 1.4 at 100°C from a bismuth antimony telluride (BiSbTe) p-type nanocrystalline bulk alloy [15]. This material is an alloy of $Bi_2Te_3$ and is made by hot pressing nanopowders that are ball-milled from crystalline ingots. Figure 1.8 shows ZT values as a function of temperature for the nanocrystalline BiSbTe alloy compared to state-of-the-art based $Bi_2Te_3$ material. ZT is about 1.2 at room temperature and peaks at about 1.4 at 100°C, which makes these materials useful for microprocessor cooling applications.

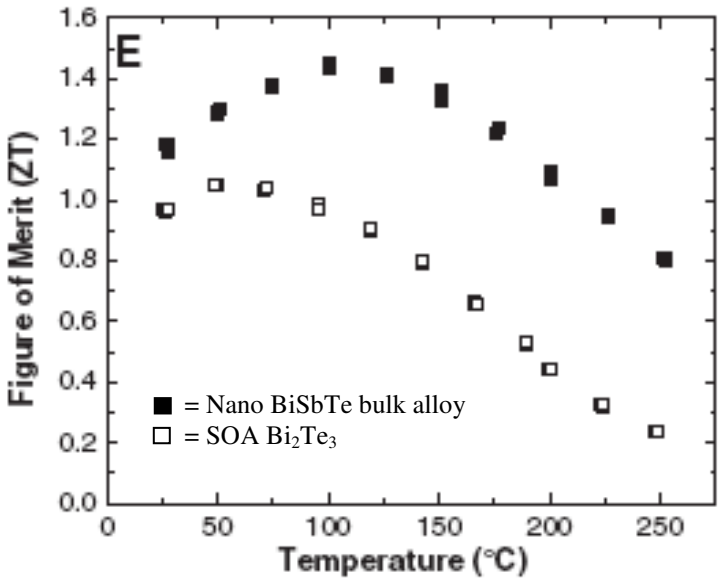



**Figure 1.8: ZT temperature dependence for nanocrystalline BiSbTe alloy and state-of-the-art $Bi_2Te_3$ material [15]**

Since the 1950s, the ZT of $Bi_2Te_3$ based alloys near room temperature has remained around 1. The improvement in ZT, in this study, results from low thermal conductivity caused by random nanoscale inclusions in the bulk material; causing increased phonon scattering by grain boundaries and defects. The thermoelectric properties of this material were also found to be isotropic, compared to state-of-the-art

$Bi_2Te_3$ based alloys, which have layered structures and, consequently, anisotropic thermoelectric properties [15]. Advancements in the figure of merit ZT have been a major driver in the development of high performance, low cost bulk thermoelectric materials.

#### 1.2.2.2 Past Research in TEC Cooling of On-chip Hot Spots

Proposed uses of miniaturized TECs (μTECs) for on-chip thermal management have included attachment of conventional TECs (using bulk TE materials), as well as the formation of superlattice thin film TE material layers, on the back of the microprocessor chip. Conventional TECs have been attached to the back side of a flip chip and cooled the entire surface area of the chip [16,17] and bulk bismuth telluride pellets have also been directly attached to a silicon chip to form an on-chip TEC without ceramic interfaces [18]. Additionally, thin film $Bi_2Te_3$ [19,20] and silicon germanium (SiGe) [21,22] layers have been grown directly on silicon substrates before, but none of these studies have considered the thermal effects of the μTEC on a hot spot.

Previous research efforts by Wang *et al* have investigated various hot spot cooling applications of μTECs on the back side of a microprocessor chip [23-25]. One of the studied approaches, termed the silicon microcooler, consisted of a doped semiconductor chip that contained a hot spot and a very thin deposited SiGe cap layer and peripheral ring electrode layer on the surface of the chip opposite of the hot spot. This approach takes advantage of the high power factor ($S^2/\rho$) of the silicon and essentially utilizes the silicon chip itself as the thermoelectric cooler. Wang *et al* have built a numerical [23] and analytical model [24] of the silicon microcooler problem to explore parametric trends in hot spot temperature reduction associated with varying chip and microcooler geometry, boundary conditions, and Si doping concentration. Another μTEC hot spot cooling

approach researched by Wang, Bar-Cohen, and Yang has been the mini-contact TEC [25]. The mini-contact is a high thermal conductivity pad, usually made of copper, which is attached to a conventional TEC in order to concentrate and optimize the cooling flux of the TEC. The tip of the mini-contact is attached to the back side of the chip and is used to selectively remove hot spot heat.

### 1.3 Scope of Work

The passive and active thermal management techniques described above have been researched in depth but many of them do not offer a comprehensive solution to the semiconductor hot spot problem. Conventional chip cooling techniques involving heat sinks or heat pipes uniformly cool the entire surface of the chip and do not focus on particular high heat flux regions such as hot spots. The research focus of this thesis expands on the work of Wang, Bar-Cohen, and Yang and examines unexplored applications of the silicon microcooler and mini-contact TEC hot spot cooling approaches. The specific contributions of this thesis are: (1) a numerical model of a modified silicon microcooler, with an integrated SiGe superlattice layer, and parametric comparison to the original silicon microcooler; (2) a parametric investigation into the viability of commercially available TEC technology compatible with the mini-contact hot spot cooling approach; (3) a study of thermal contact resistance impact on mini-contact TEC cooling; (4) a multi-optimization and functional dependence analysis of various parameters in a mini-contact TEC chip package; and (5) new experimental results for a mini-contact enhanced conventional TEC with 130μm thick $Bi_2Te_3$ thermoelectric legs. It is to be noted that all of the subsequent chapters are based on published and/or submitted

papers on the silicon microcooler [23,24,26,27] and the mini-contact enhanced TEC [25,28,29].

This thesis presents various numerical results for the two outlined hot spot cooling approaches (silicon/superlattice microcooler and mini-contact enhanced TEC) and presents experimental results to validate the numerical model. The thesis is organized as follows:

Chapter 1 discusses present and future thermal challenges in the IC microprocessor industry and outlines the presence of the hot problem. Thermoelectrics are introduced as potential candidates to alleviate on-chip hot spots and a brief overview into the background of thermoelectrics is given. Past research into thermoelectrics along with the objective of this thesis are also presented.

Chapter 2 provides the results of three-dimensional, electro-thermal, finite-element modeling of a superlattice microcooler, focusing on the hot spot temperature and superlattice surface temperature reductions, respectively. Simulated temperature distributions and heat flow patterns in the silicon, associated with variations in microcooler geometry, chip thickness, hot spot size, hot spot heat flux, and superlattice thickness are provided. Comparison is made to hot spot cooling achieved by the Peltier effect in the silicon microprocessor chip itself.

Chapter 3 focuses on the mini-contact TEC cooling approach and outlines the numerical simulation results for three different chip packages proposed by a Taiwanese national laboratory [30], two containing Taiwanese designed TECs, and one containing a commercially available thin film TEC (TFTEC) [31]. A Taiwanese IC package with an actual on-chip hot spot is presented and modeled numerically using ANSYS™ FE

software. A description of the model assumptions and parameters is given and the thermal behavior of the Taiwanese and commercial TEC devices, as well as the hot spot, is characterized. Several optimizations were completed to enhance thermal performance and suggestions were made to improve overall cooling for future studies of the mini-contact TEC approach.

Chapter 4 studies another variation of the mini-contact TEC hot spot cooling approach. This chapter presents numerical simulations, with a finite-element package-level model, to examine the parasitic effects of the thermal contact resistance, at the interfaces of the mini-contact and TEC, on the cooling efficacy of this thermal solution. Particular attention is devoted to the deleterious effect of contact resistance on the thermoelectric leg height and the mini-contact size required to achieve the greatest hot spot temperature reduction on the chip. Data from experiments with TEC's, having a leg height of 130μm, combined with several sizes of mini-contact pads, are used to validate the modeling approach and the overall conclusions.

Chapter 5 outlines a proof of concept experiment designed to demonstrate the spot cooling capability of a mini-contact enhanced conventional TEC. A brief description of the experimental setup is provided. The experimental results are used to validate the ANSYS™ numerical model and provide confidence in further using this numerical model to investigate the effects of on-chip hot spots and thermal contact resistance.

Chapter 6 recapitulates the findings of this research and offers recommendations for future work.

# Chapter 2

# 2. Superlattice μTEC Hot Spot Cooling

## 2.1 Introduction

Driven by shrinking feature sizes, microprocessor "hot-spots" – with their associated high heat flux and sharp temperature gradients – have emerged as the primary "driver" for on-chip thermal management of today's advanced IC technology. Among the techniques proposed to combat the effects of hot spots, thermoelectric microcoolers (μTECs) provide unique advantages. Their solid state design, the absence of moving parts, and their ability to target micron-sized, high heat flux areas, make such μTECs an ideal micro-cooling solution.

Miniaturized silicon thermoelectric coolers have been shown to provide significant hot spot remediation capability, e.g. removing nearly 80% of the hot spot temperature rise in a 70x70μm hot spot with a heat flux of 680W/cm$^2$ on a 50μm thick silicon chip [23]. Silicon-Germanium superlattice structures, formed on the back of a silicon chip, have also been proposed for hot spot remediation [32], but there have been few detailed studies on the cooling capability of such devices.

Superlattice structures are typically comprised of tens-to-hundreds of alternating layers of nanometer thick films, together forming a composite thin film structure several microns thick, as exemplified in figure 2.1. The large number of very thin active layers in such superlattices is known to reduce phonon thermal conductivity, through "phonon trapping" at the interfaces between the alternating layers, and to achieve a far more rapid response time than conventional TEC's [21], due to the low mass of the microcooler, as well as to display high heat flux removal capability, due to the reduced joule heating in

the thin superlattice. The present interest in the use of superlattice TEC's has been prompted by these attributes, and most prominently, the relatively high value of the TEC figure-of-merit, ZT ($S^2T/\rho k$) reported in the literature [33].

The objective of this study is to evaluate hot spot cooling performance of a thermoelectric silicon microcooler, comprised of a silicon chip and a SiGe cap layer on top of the chip, compared to a microcooler with an integrated SiGe superlattice layer between the silicon chip and the SiGe cap layer. The study will explore the influence of superlattice thickness, silicon chip thickness, microcooler size, hot spot size, and hot spot heat flux intensity on the hot spot and superlattice temperatures, respectively. This chapter is based on previous publications [23,24,26,27,34].

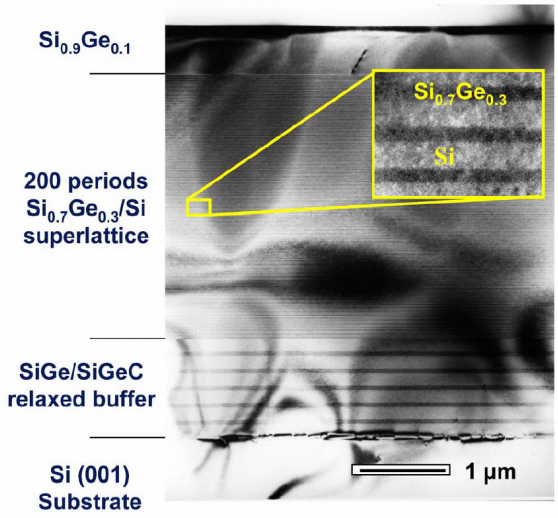



**Figure 2.1: Transmission Electron Micrograph of Superlattice Microcooler from Shakouri '06 [21]**

## 2.2 TE Microcooler Thermophysics

Two thermoelectric microcooler configurations are examined in this study: one containing a superlattice structure and one without. First, a simple silicon microcooler

will be introduced and explained, followed by an integrated superlattice structure for comparison. These two models will be referred to as the silicon TE microcooler and the superlattice TE microcooler, respectively.

The structure of an on-chip silicon thermoelectric microcooler used for hotspot cooling is illustrated in figure 2.2. It is a single element silicon microcooler that uses the thermoelectric properties of the silicon chip itself. Electric current conducts laterally through the silicon chip and flows out of the ring electrode, which can be located adjacent to or displaced from the microcooler. In the illustrated configuration, the ring electrode is located on the periphery of the chip. The metal lead, which is electrically isolated from the silicon chip with a very thin $SiN_x$ passivation layer (<0.3µm), is employed to deliver an electric current to the microcooler through the metal contact and silicon cap layer. A thermoelectric cooler uses an electric current to induce the Peltier effect, at the junction of two materials with different Seebeck coefficients, to provide localized cooling, and to transport the absorbed heat to the hot side of the thermoelectric circuit.

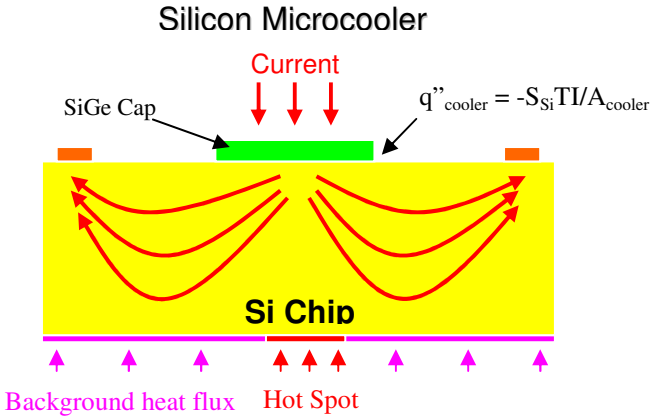



**Figure 2.2: Schematic of the thermoelectric microcooler model**

The figure 2.2 schematic of the silicon μTEC cooler shows that the electric current flowing through the indicated circuit results in Peltier cooling at the junction of the metal contact/silicon cap and again at the silicon cap/silicon chip interface, but causes Peltier heating at the silicon chip/ring electrode interface, where energetic electrons must shed some of their energy in entering the highly-conductive metal. In addition, the resistance to current flow leads to Joule heating in the elements of the thermoelectric circuit, most notably in the silicon chip.

The Peltier cooling rate at the metal contact/silicon cap interface can be expressed:

$$q_{TE,1} = (S_{metal} - S_{cap})T_1 I \approx -S_{cap} T_1 I \qquad (2.1)$$

where $S_{metal}$ and $S_{cap}$ are the Seebeck coefficients of the metal contact and silicon cap layer, respectively, and $T_1$ is the absolute temperature at the interface between the metal contact and the silicon cap layer**.** It is to be noted that by comparison to the high Seebeck coefficient of silicon materials under consideration, the Seebeck coefficient of the metal contact, $S_{metal}$, is negligibly low [26]. The Peltier cooling rate at the silicon cap/silicon chip interface is given by:

$$q_{TE,2} = (S_{cap} - S_{Si})T_2 I \qquad (2.2)$$

where $S_{Si}$ is the Seebeck coefficient of the silicon chip, which varies with the doping concentration [35], and $T_2$ is the absolute temperature at the interface between the silicon cap layer and silicon chip. Since the highly-doped silicon cap layer is very thin (<1μm) and the thermal conductivity is large (100~110W/mK at 373K), the temperature

difference between these two interfaces can be neglected, i.e. $T_1 \approx T_2 = T_c$. Thus, the overall Peltier cooling rate of the silicon TE microcooler can be expressed as:

$$q_{TE,c} = q_{TE,1} + q_{TE,2} = -S_{cap}T_1I + (S_{cap} - S_{Si})T_2I \approx -S_{Si}T_cI \quad (2.3)$$

where $T_c$ is defined as the microcooler temperature. Therefore, in such a silicon thermoelectric microcooler configuration, to a very good first-approximation, the overall intrinsic Peltier cooling rate depends only on the Seebeck coefficient of the silicon chip, the microcooler temperature, and the applied current.

Similarly, the Peltier heating at the silicon chip/ring electrode interface of the present microcooler configuration can be expressed as:

$$q_{TE,h} = S_{Si}T_hI \quad (2.4)$$

where $T_h$ is the absolute temperature on the ring electrode. However, due to the large surface area covered by the ring electrode/silicon chip interface, Peltier heating at the electrode can be expected to result in a minimal local temperature rise and a negligible effect on the hot spot temperature.

In order to facilitate the numerical modeling and thermal simulation of the IC package without the penalty of very large node counts and long computational runs, the detailed structures of the microcooler, including the silicon cap and the metal contact layer, were combined into a single ANSYS™ "surface entity" attached to the top of the silicon chip. This "surface entity" is capable of generating a cooling heat flux equal to the combined Peltier cooling effect at the metal contact/silicon cap interface and at the silicon cap/silicon chip interface, as in equation 2.3. Due in part to the 0.3μm thickness of

the silicon cap layer, volumetric Joule heating in the silicon cap layer was found to typically produce a heating flux two orders of magnitude lower than the cooling flux produced by the microcooler and was therefore neglected. The net Peltier cooling effect can then be expressed as an internal heat flux boundary condition on the surface of the microcooler:

$$q''_{TE,Si,\ cooler} = -S_{Si}TI/A_{cooler} \qquad (2.5)$$

where $A_{cooler}$ is the area of the microcooler. This approximation significantly simplifies the numerical computations.

Next, we turn to the superlattice microcooler, with the understanding that at the limit of a zero thickness superlattice, the superlattice μTEC devolves back into the silicon thermoelectric microcooler. Figure 2.3 provides a 3-dimensional representation of a SiGe superlattice, including the distinct thickness of the alternating layers of the Si and Ge that constitute the superlattice. The corresponding boundary conditions for the superlattice microcooler are also shown in figure 2.3.

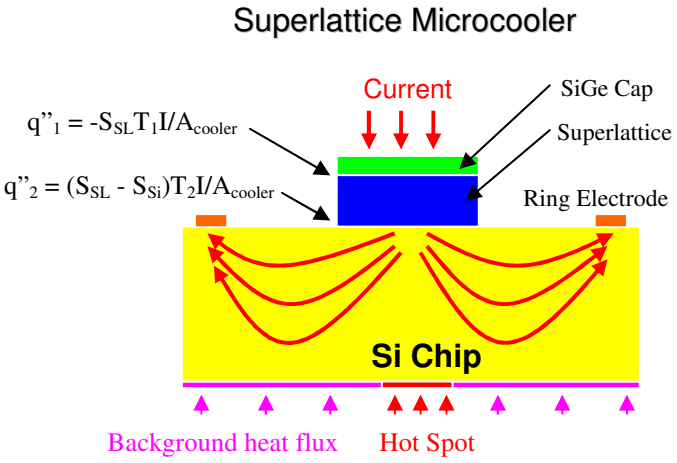



**Figure 2.3: Thermoelectric Microcooler with Integrated SiGe Superlattice Layer**

For the superlattice microcooler, equation 2.5 changes to:

$$q''_{TE,SL,\ cooler} = (S_{SL} - S_{Si})T_2 I/A_{cooler} \quad (2.6)$$

where $S_{SL}$ is the Seebeck coefficient of the superlattice and $T_2$ is the absolute temperature at the superlattice/silicon chip interface. This change is made in order to recognize that the effective superlattice Seebeck coefficient falls between the metal lead and the silicon and that, consequently, Peltier cooling occurs on both sides of the superlattice structure. The Peltier cooling at the top of the superlattice is, thus, given by:

$$q''_{TE,SL} = -S_{SL} T_1 I/A_{cooler} \quad (2.7)$$

where $T_1$ is the temperature at the top of the superlattice. Conceptually, equations 2.6 and 2.7 can be summed to yield the effective cooling rate at the interface between the superlattice μTEC and the silicon chip.

**2.3 Modeling Methodology for On-chip Hot Spot Cooling**

The commercial finite element software, ANSYS™, was used in this study to simulate the thermal and thermoelectric behaviors of the silicon and superlattice microcoolers, using a half-symmetry three dimensional (3-D) thermal-electrical model with a total element number of 100,000 - 200,000 for the entire package. Several "help volumes" were created inside the Si chip and around the microcooler to accurately model the high heat flux of the hot spot compared to the much lower surrounding heat flux. The average runtime for a typical simulation was approximately 15 minutes on a Dell Dimension 2400 computer with Intel Pentium 4 processor. Below, figure 2.4a represents the full model including the microcooler centered at the top of the silicon chip, the two

thermal interface layers, the integrated heat spreader, and the heat sink. The lateral dimensions of the chip, heat spreader, and heat sink are 1.1cm x 1.3cm, 3.1cm x 3.1cm, and 5cm x 5cm, respectively.

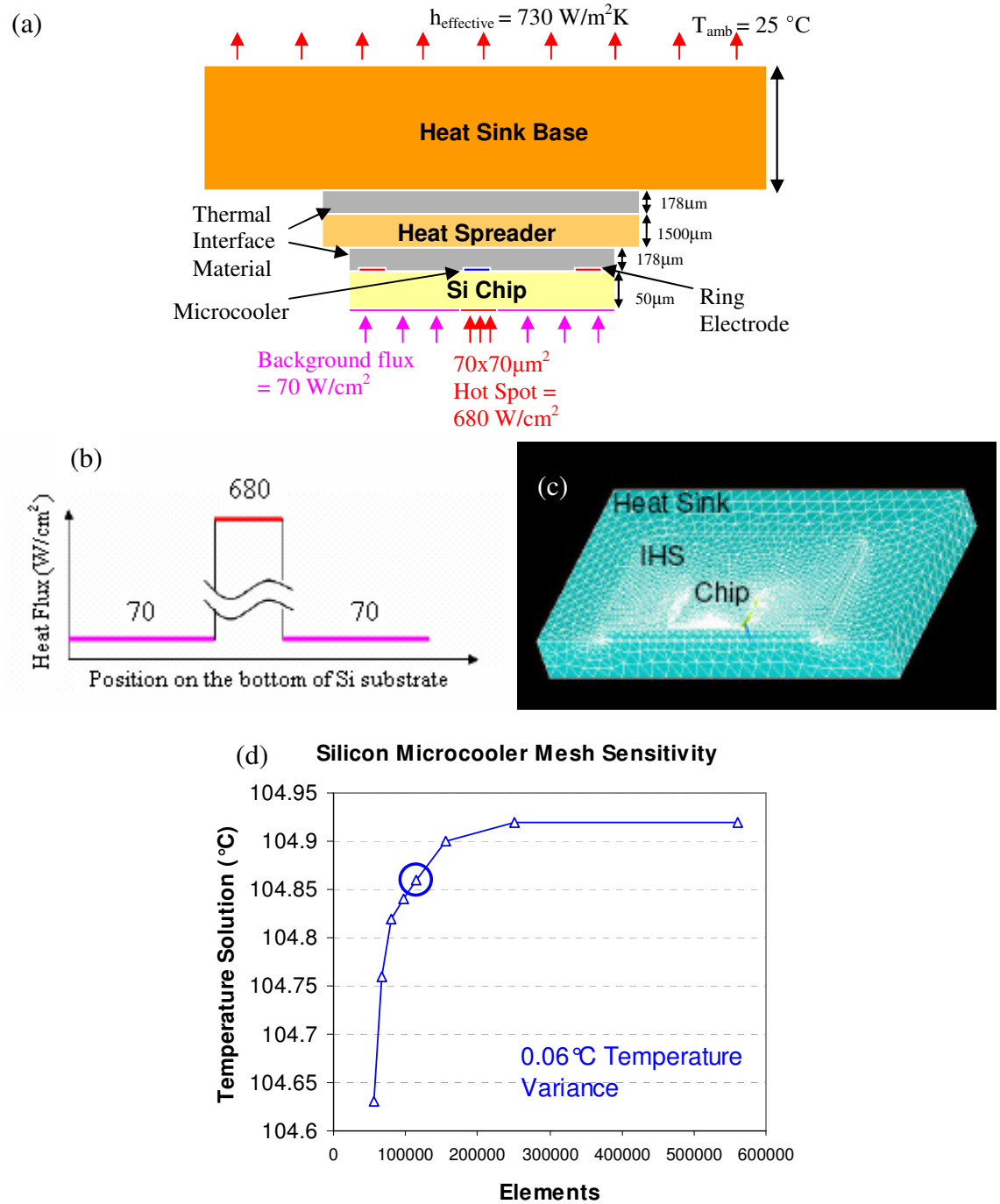



**Figure 2.4: Finite Element Model of Chip Cooled by µTEC (a) Entire chip package FE model, (b) Heat flux distribution on the bottom of the chip surface, (c) Image of the model meshing in ANSYS™, (d) Mesh sensitivity for the silicon microcooler**

ANSYS™' thermal-electrical element - Solid 69 - automatically calculates the bulk Joule heating in each element and hence throughout the modeled space by solving the current continuity and heat conduction equations [26]. This feature allows both thermal and electric fields to be resolved through thermal-electrical coupling. As illustrated in figure 2.4a, a ground voltage of zero is applied as a boundary condition on the surface of the ring electrode. Electric current is then applied as a surface load onto the microcooler surface, for the non-superlattice case, and onto the top of the superlattice structure, for the superlattice case. In this way, Joule heating from the silicon chip could be simulated directly using the thermo-electrical mode of ANSYS™. The elements are densely located for both cases around the microcooler and the hotspot where the largest temperature gradient is expected to occur. Mesh density in the silicon chip around the microcooler is also high in order to accurately calculate the thermal and electrical spreading effects and three dimensional distribution of Joule heating, as indicated in figure 2.4c. For purposes of the thermoelectric modeling study presented herein, the details of the solid-state circuitry in the active regions of the chip, including individual transistors, gates, capacitors, etc., are ignored and the heat generated from these components is represented as a 680W/cm$^2$ 70µmx70µm$^2$ hotspot surrounded by a background heat flux of 70W/cm$^2$ on the bottom surface of the silicon chip, as depicted in figure 2.4b. A ring electrode at a distance of 4mm from the center and a width of 0.3mm is also included. The mesh sensitivity for the silicon microcooler numerical model in figure 2.4d shows a very small temperature difference in a solution with increased element count.

The major heat transfer path in the modeled space is assumed to be from the active region at the bottom of the silicon chip to the top side, then through the heat spreader to the heat sink by conduction, and from the heat sink to the ambient air by forced convection. Two layers of solder-like thermal interface material (TIM) - on either side of the heat spreader - are included in the model. The thermal contact resistances at these two interfaces are included in the effective thermal conductivity value of 30W/mK used for the 178μm TIM's [26]. To simplify the modeling geometry, the details of the heat sink fins are not included in this model and, instead, an equivalent convective heat transfer coefficient of 730 $W/m^2$-K is applied as a boundary condition on the top surface of the heat sink base to achieve a commonly attained heat sink-to-ambient thermal resistance of about 0.55K/W [23]. Also, homogeneous material properties and uniform thicknesses are assumed for the silicon chip, thermal interface materials, heat spreader, and heat sink base. The geometric parameters and material properties for the packaging materials are listed in table 2.1.

**Table 2.1: Geometry and Material Properties for μTEC-cooled Chip Package**

| | Dimension (L×W×H) | Thermal Conductivity (W/mK) | Electric Resistivity (Ωcm) |
|---|---|---|---|
| Silicon Chip | 11mmx13mmx (20 to 200μm) | 110 | 0.00462 |
| TIM (1st layer) | 11mmx13mmx178μm | 30 | 100 |
| IHS | 31mmx31mmx1.5mm | 150 | 100 |
| TIM ($2^{nd}$ layer) | 31mmx31mmx178μm | 30 | 100 |
| Heat sink base | 50mmx50mmx5mm | 360 | 100 |

While in this study the thickness of the superlattice ranges from 1μm to 20μm, its cross sectional area is always the same as the microcooler. Following Zhang et al [36], the superlattice has a thermal conductivity of 6.5 W/mK, an electric resistivity of 0.0016

Ωcm, and a Seebeck coefficient of 200μV/K. The thermoelectric material properties of the silicon chip, i.e. the Seebeck coefficient and the electrical resistivity, are determined largely by the doping concentration in the silicon. An optimum silicon doping concentration of $2.5x10^{19}$ $cm^{-3}$, which yields the highest silicon power factor ($S^2/\rho$=5.79 [27]) at the μTEC operating temperature of approximately 100°C, and assumed negligible electrical contact resistances in the μTECs structure were chosen to produce the most favorable temperature reduction results.

### 2.3.1 FEM Model Validation

The present analysis of integrated SiGe superlattice microcoolers builds on a fabricated superlattice, with measured material properties as above, which was studied experimentally by Shakouri and co-workers**.** In this heterostructure thin film microcooler experiment, a 3μm thick superlattice, with contact areas of $60x60\mu m^2$, $70x70\mu m^2$, $100x100\mu m^2$, and $150x150\mu m^2$, respectively, was used to cool a 535μm thick silicon chip, as shown in the schematic representation in figure 2.5 [36]. The chip was placed on a temperature controlled heat sink at a fixed ambient 25°C. Standard E-type thermocouples were placed on top of the microcooler and at the chip, and an ILX Lightwave LDX3220 current source powered the microcooler through probes [36]. A maximum temperature reduction of 4.5°C was achieved with the $60x60\mu m^2$ microcooler at the surface of the metal contact. These results are used to validate the Finite Element model and simulation approach developed in this study and to facilitate a detailed exploration of the parametric sensitivities of such μTEC devices.

An FEM ANSYS™ model, geometrically matched to Zhang et al's [36] laboratory microcooler, was created. The boundary conditions and material properties used in the

simulation were based on information provided in [36]; including a Si chip Seebeck coefficient of 325μV/K and a superlattice Seebeck coefficient of 200μV/K. Figure 2.6 shows a sample numerical solution of the experimental superlattice microcooler.

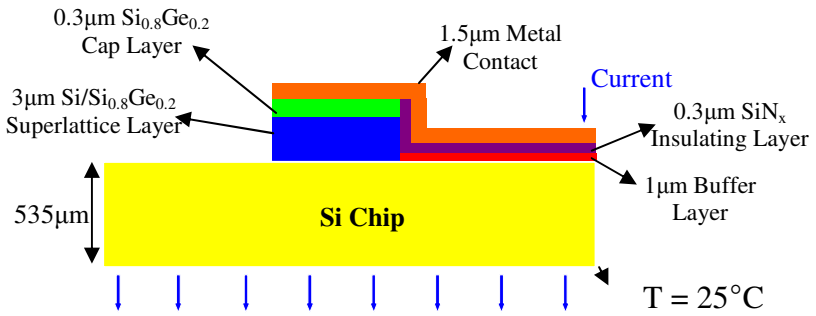
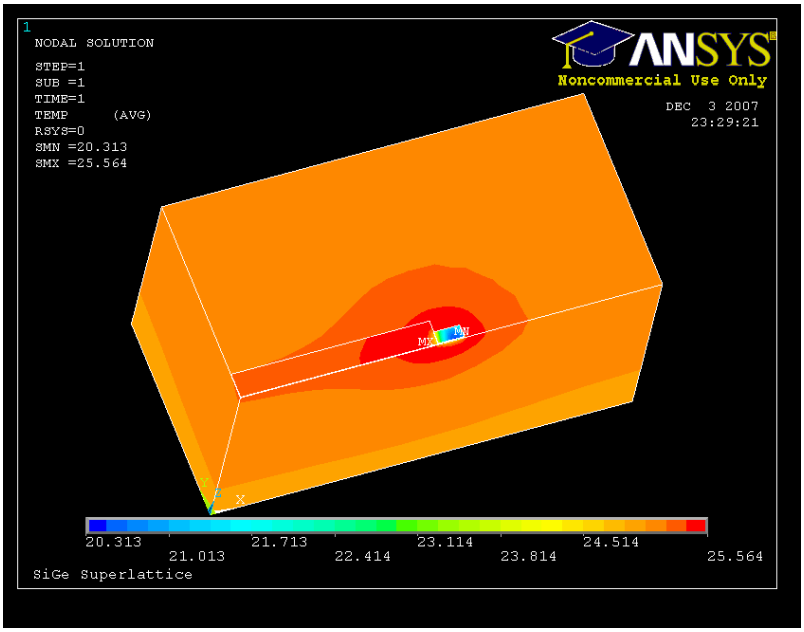



**Figure 2.5: Zhang *et al* "3D Electrothermal Simulation of Heterostructure Thin Film Micro-coolers" 2003 [36]**



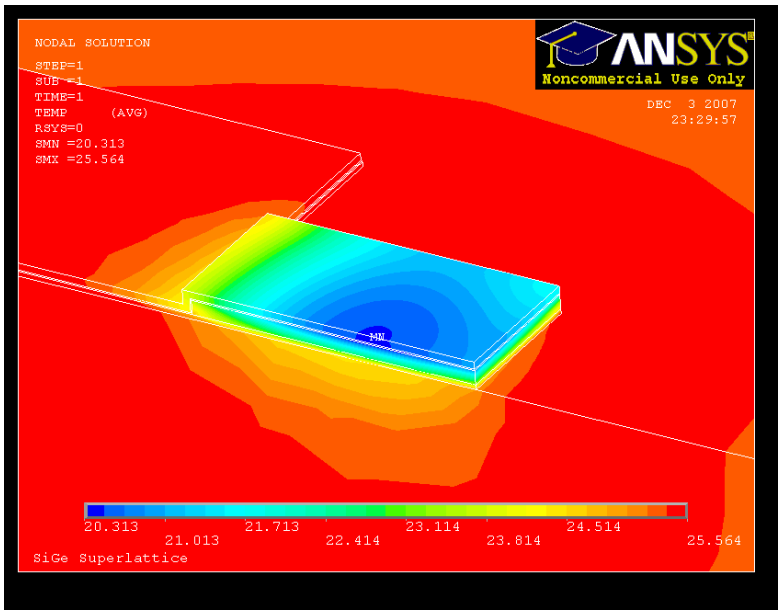
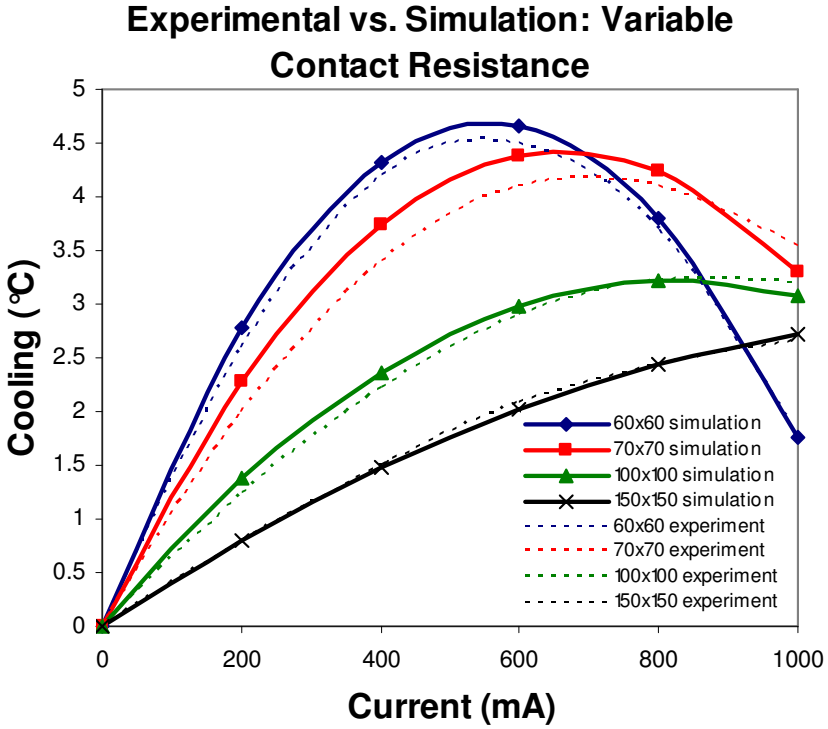



**Figure 2.6: Temperature Distribution in Chip with Integrated Superlattice Microcooler [Chip=535μm Silicon; Superlattice = 3μm thick, 60x60μm$^2$, 0.6A, and 7.11x10$^{-7}$ Ω–cm$^2$ contact resistance; ambient temperature = 25°C]**

In developing an ANSYS™ model for such a superlattice thermoelectric microcooler, attention must be devoted to the thermal contact resistance that occurs between the superlattice and the silicon chip, due to lattice mismatches and the somewhat imperfect adhesion of the two structures. In the absence of a direct empirical measurement of this contact resistance, a comparison between the results of the ANSYS™ simulation and the experimental data can be used to determine the value of the electrical contact resistance which provides the best agreement between the two. For best results the contact resistances were found to vary between 7x10$^{-7}$ Ω–cm$^2$ and 20x10$^{-7}$ Ω–cm$^2$ and to fall in the range of the values suggested by Zhang et al, which was 6x10$^{-7}$ Ω–cm$^2$ [36].

Figure 2.7 displays the experimental and simulated temperature reductions achieved by the superlattice microcooler on the surface of the metal contact. The

parabolic variations in surface cooling with current reflect the interplay between the Peltier cooling effect, which increases linearly with the electrical current, and Joule heating, which increases with the square of the current, and yields an optimum current at which the best cooling is achieved. Since the actual temperature depends on the current flux, larger microcoolers require higher optimum currents, as shown. The predicted values in this figure reflect the use of the "best fit" contact resistance determined for each individual cooler size and seen to fall in the anticipated range. The resulting root-mean-square discrepancies between the empirical results and simulated values range between 0.37°C – 0.20°C. The agreement in the functional form of the temperature variation and the actual cooling values between simulation and experimental results creates confidence in the modeling methodology and provides the foundation for more detailed parametric studies of SiGe superlattice microcoolers.



| | Contact Resistance | $\Delta T_{rms}$ |
|---|---|---|
| $60x60\mu m^2$ | $7.11x10^{-7}$ Ω-cm$^2$ | 0.08822 |
| $70x70\mu m^2$ | $7.89x10^{-7}$ Ω-cm$^2$ | 0.20122 |
| $100x100\mu m^2$ | $18.13x10^{-7}$ Ω-cm$^2$ | 0.12428 |
| $150x150\mu m^2$ | $19.81x10^{-7}$ Ω-cm$^2$ | 0.03737 |

**Figure 2.7: Surface Temperature Reductions with Superlattice Microcoolers**

### 2.3.2 Model Simplifications

To reduce the complexity of the FE model and reduce the computational time, certain assumptions are made about the structure of the superlattice. Typically the superlattice is comprised of alternating layers of materials, taken in this study to be SiGe and Si, each on the order of 5-10nm thick, layered on top of one another for approximately 100 periods. The result is a superlattice structure with a thickness from 1μm to 20μm. In reality it is difficult to fabricate a 20μm thick superlattice. However, ANSYS™ can easily model the theoretical behavior of such a structure. In the model, it is assumed that the superlattice is one homogeneous layer with a set of "effective" material properties that reflect the overall Seebeck coefficient, thermal conductivity, and electric resistivity of the 3D structure. This assumption is made to facilitate the efficient simulation of the surface temperatures and effect of the μTEC on the hot spot temperature but does sacrifice the ability to determine the temperature of the individual layers within the superlattice.

Moreover, in the present study, focused on the comparative effectiveness of hot spot cooling by two configurations of thermoelectric microcoolers (with and without an integrated superlattice), it is assumed that all of the interfaces are perfect and lossless and that there is no electrical contact resistance between the microcooler and the silicon, or

elsewhere in the model. Simulations show that even with the addition of a readily achievable contact resistance of $2x10^{-6}$ Ωcm at the top of a 200x200μm$^2$ microcooler with a 10μm thick superlattice on a 50μm Si chip, the maximum achieved cooling at the hot spot and microcooler interface is only reduced by about 0.1K and the relative temperature reductions for the various configurations remain unaffected.

## 2.4 Results and Discussion

### 2.4.1 Thermal Characteristics of a TE Microcooler

The FEM simulated thermal characteristics of thermoelectric microcoolers are displayed in figures 2.8 and 2.9, showing the heat flow pattern in the through-thickness direction in the vicinity of a 200x200μm$^2$ microcooler across from a 70x70μm$^2$ hot spot on the bottom of a 50μm thick chip. Figure 2.8a, showing the nearly hemispherical heat flux vector distribution for the uncooled situation is to be contrasted with figure 2.8b which displays the heat flux vectors when Peltier cooling is produced at the silicon chip surface by an electric current of 0.6A. The effectiveness of the silicon microcooler in altering the pure conduction heat flow pattern and attracting heat from the hot spot, as well as the peripheral areas, is clearly visible in figure 2.8b.

While this same general behavior is on display in figures 2.9a and 2.9b for the dormant/activated superlattice μTEC, in the uncooled chip the presence of the low thermal conductivity 10μm thick superlattice layer, with a thermal conductivity of 6.5W/mK, is seen to pose an impediment to heat flow normal to the chip surface, leading to a distinct enhancement of the in-plane heat flow away from the microcooler. Activation of the superlattice with a 0.6A current does draw the heat from the chip towards the superlattice microcooler but at somewhat reduced intensity, due again to the

low thermal conductivity superlattice layer. The resulting temperature distributions for the two activated microcoolers are shown, respectively, in figure 2.10**,** revealing similar patterns, but somewhat warmer hot spot temperatures for the superlattice configuration. The temperature profiles for the active μTECs follow a characteristic "W" pattern, as previously observed in the literature [28]. This pattern helps mediate the large temperature spike caused by the hot spot and helps achieve temperature uniformity along the bottom (active) surface of the chip.

Figure 2.11 shows the normal heat flux distributions along the top of a 50μm Si chip, cooled by a silicon microcooler or a superlattice microcooler, both with no background heat flux imposed on the bottom of the chip (only an active 680W/cm$^2$ hot spot) and with an operating current of 0.6 Amps and 0 Amps, respectively. It is seen that for the uncooled chip, as well as in the presence of an operating microcooler, the superlattice integrated on the back of the chip provides somewhat lower heat removal capability (by approximately 5%), than achievable with the silicon microcooler. When operating at their optimum current, the μTECs dramatically increase the normal heat flux on top of the chip, particularly at the center of the chip where the peak heat flux increases by approximately 150W/cm$^2$ (for each respective cooler) over the flux when the μTECs are turned off, reaching approximately 250W/cm$^2$. For comparison, the normal heat flux distributions along the top of the chip are also shown for a 20μm chip and a 100μm chip in figures 2.12 and 2.13, respectively. For the thinner 20μm chip, the peak normal heat flux at the center of the chip with the silicon microcooler (operating at 0.6A) reaches 400W/cm$^2$ some 60% of the hot spot heat flux. The peak normal heat flux for the same

case with a 100µm chip is increased by approximately 180W/cm$^2$ to more than 210W/cm$^2$, or by a factor of approximately 7, with an activated microcooler.

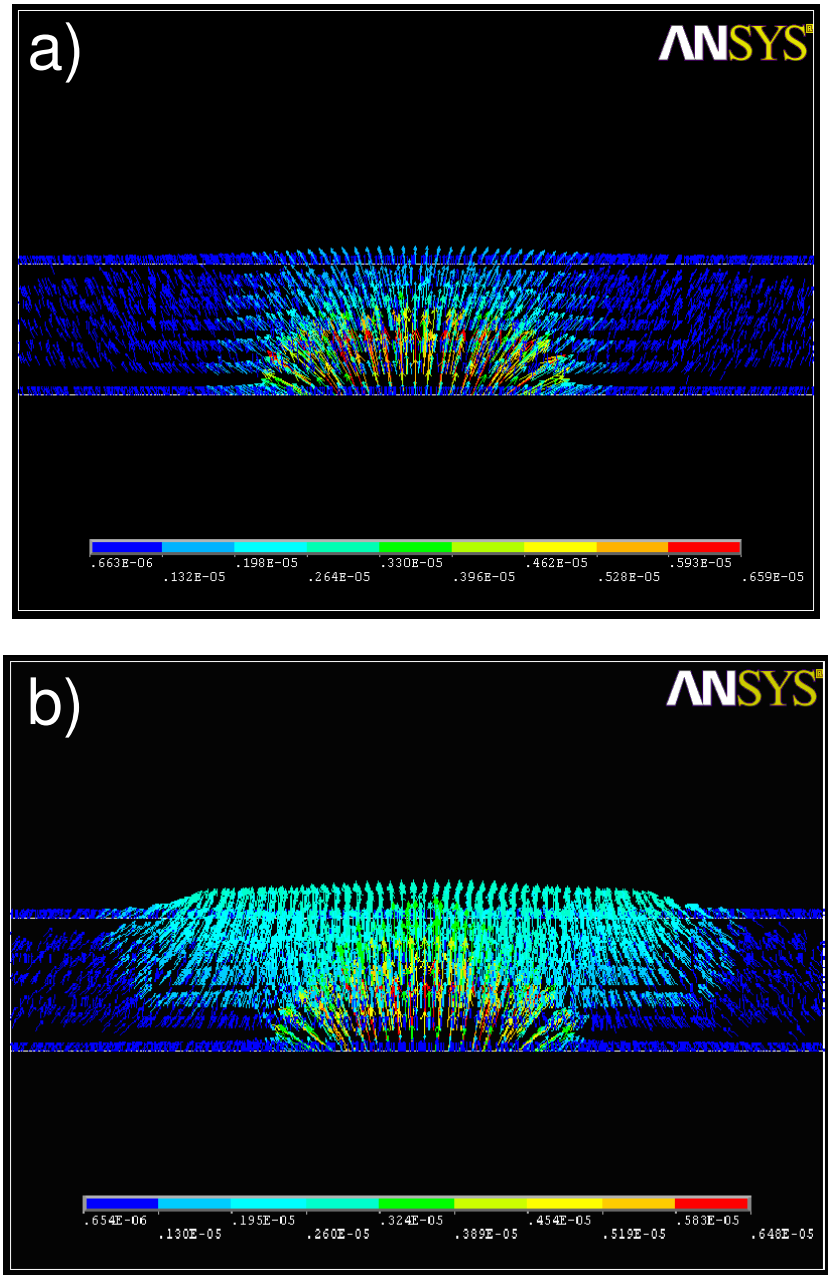



**Figure 2.8: Heat flux distribution in silicon chip with hot spot [q"=680W/cm$^2$, L=70µm] (a) no TEC cooling and (b) with TEC cooling from a silicon microcooler operating at 0.6Amps.**

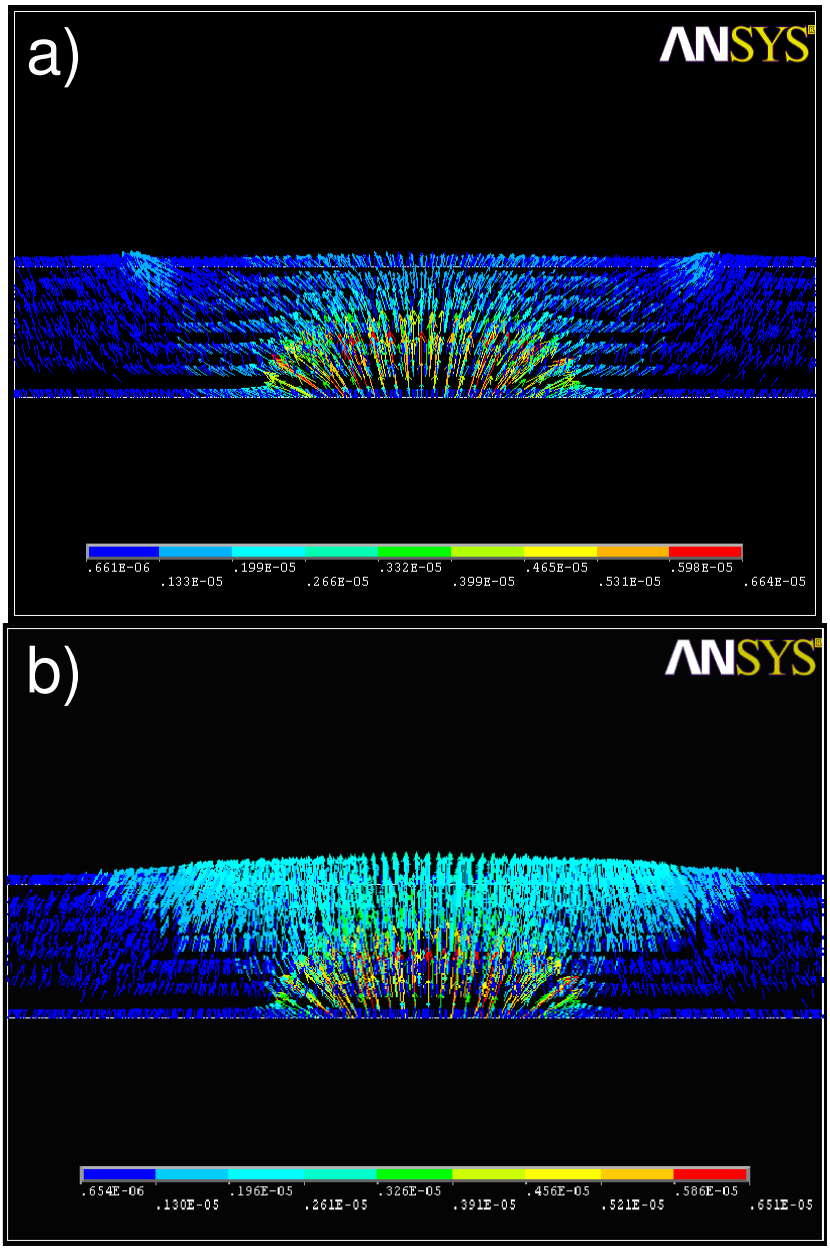



**Figure 2.9: Heat flux distribution in the silicon chip with hot spot [q"=680W/cm$^2$, L=70µm] (a) no TEC cooling and (b) with TEC cooling from a superlattice microcooler operating at 0.6Amps.**

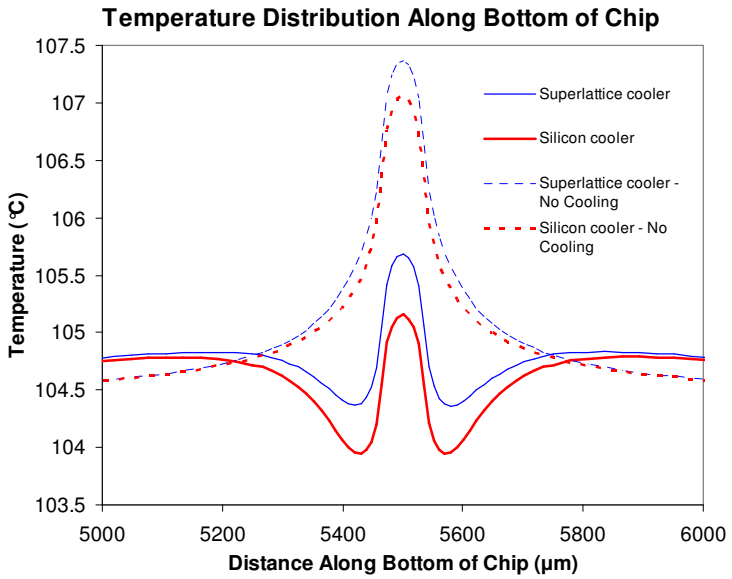



**Figure 2.10: Temperature distribution along the bottom of a µTEC-cooled silicon chip die with hot spot [operating at 0.6Amps and 0Amps, respectively]**

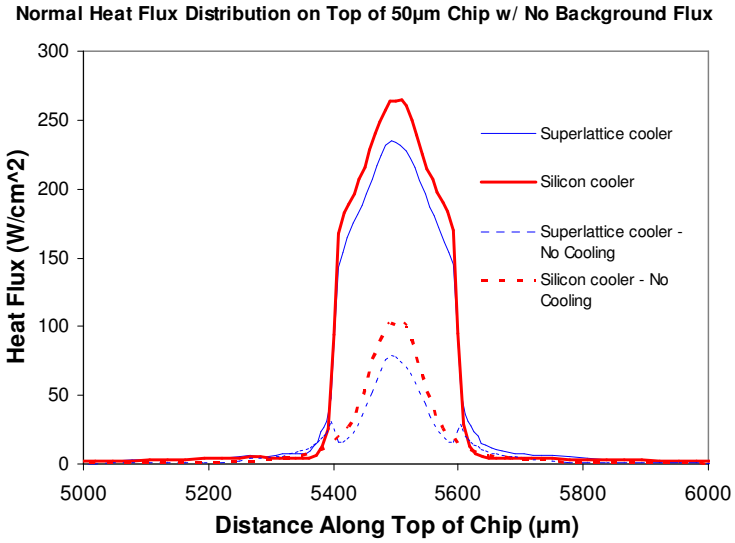



**Figure 2.11: Normal heat flux profile along the top of a µTEC-cooled 50µm thick silicon chip [0.6 Amps and 0 Amps, 200x200µm$^2$ microcooler, 70x70µm$^2$ hot spot, 680 W/cm$^2$ heat flux at hot spot.]**

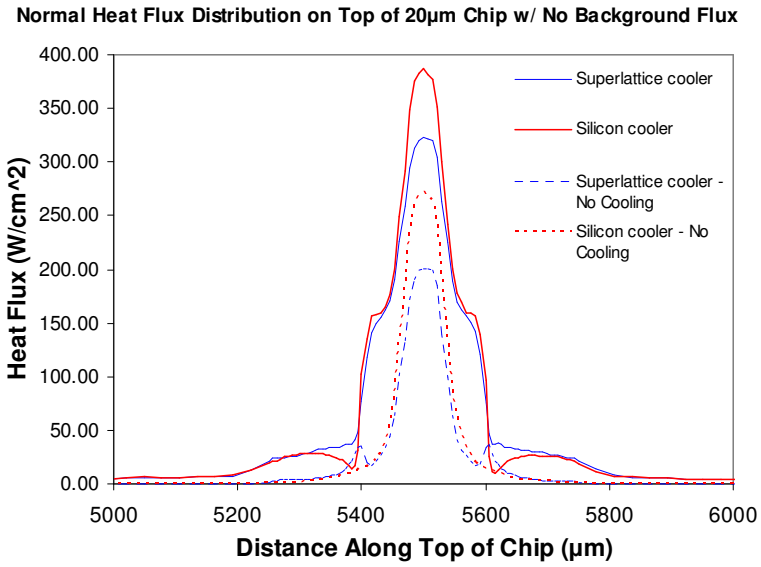



**Figure 2.12: Normal heat flux profile along the top of a µTEC-Cooled 20µm thick silicon chip [0.6 Amps and 0 Amps, 200x200µm$^2$ microcooler, 70x70µm$^2$ hot spot, 680 W/cm$^2$ heat flux at hot spot.]**

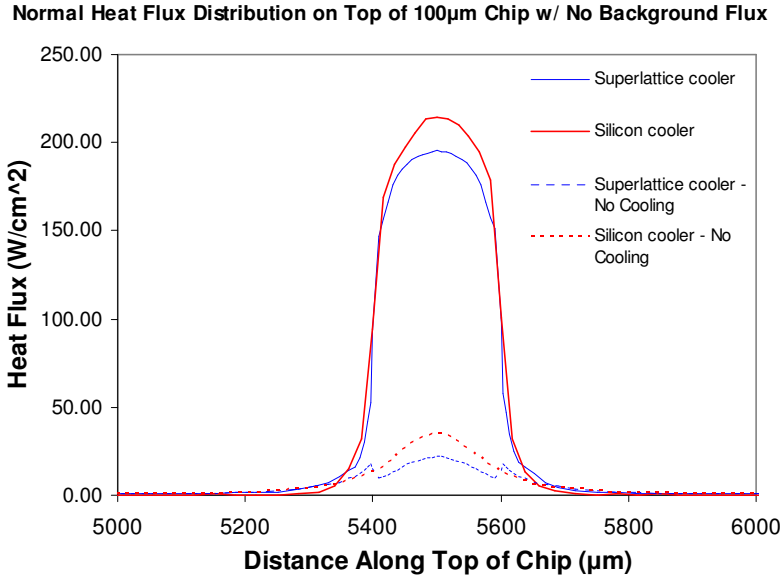



**Figure 2.13: Normal heat flux profile along the top of a µTEC-cooled 100µm thick silicon chip [0.6 Amps and 0 Amps, 200x200µm$^2$ microcooler, 70x70µm$^2$ hot spot, 680 W/cm$^2$ heat flux at hot spot.]**

### 2.4.2 Parametric Analysis

To gain a better understanding of the detailed behavior of a superlattice equipped microcooler, it is helpful to observe the effect of distinct variations in the geometric

parameters and boundary condition, relative to a baseline design. The previously described baseline design involves a 10μm thick superlattice, operating at 0.6 Amps, a 50μm thick Si chip, a 200x200$\mu m^2$ microcooler, a 70x70$\mu m^2$ hot spot region, and a 680W/$cm^2$ hot spot heat flux, along with a 70W/$cm^2$ background heat flux on the bottom of the chip.

#### 2.4.2.1 Superlattice Thickness

Figure 2.14 shows several key temperatures in the integrated superlattice microcooler chip, including the minimum hot spot temperature, the minimum superlattice temperature, and the temperature of the interface between the chip and the microcooler, respectively, as a function of the superlattice thickness in the range of 0μm to 20μm. It is important to note that the temperatures shown are achieved at different currents, each μTEC configuration requiring an optimum current to achieve its best performance, with current typically ranging from 0 to 1Amp. It should be noted that the zero-thickness superlattice microcooler – by definition – becomes the silicon μTEC.

As is clearly visible in figure 2.14, the lowest hot spot temperatures are achieved with vanishingly thin superlattice thicknesses, i.e. with the silicon thermoelectric microcooler. It is evident that as the superlattice thickness increases, the minimum hot spot and chip/microcooler interface temperatures rise almost linearly, by approximately 1K over the indicated thickness range, leading to progressively poorer cooling at the semiconductor hot spot. Alternatively, the surface temperature on the top of the superlattice – the furthest removed from the hot spot and separated from this heat source by the relatively low thermal conductivity "phonon trapping," alternating layers of SiGe – is seen to decrease by some 1.5K as the superlattice thickness increases to 20μm. Thus,

use of a thicker superlattice does significantly lower the temperature at the top of the superlattice surface, but not at the base surface where contact is made with the chip and, hence, not at the semiconductor hot spot.

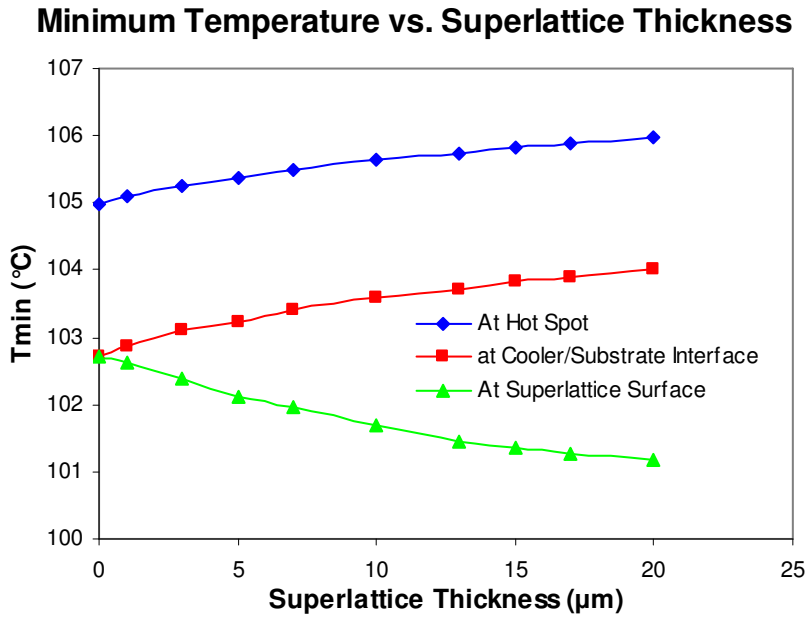



**Figure 2.14: Temperature variation in superlattice cooled silicon chip – varying superlattice thickness [200x200µm$^2$ cooler, 50µm Si chip, 70x70µm$^2$ hot spot, and 680W/cm$^2$ hot spot heat flux].**

### 2.4.2.2 Si Chip Thickness

Variation in the hot spot temperature with chip thickness from 0 to 200µm, for the baseline 10µm superlattice configuration, is shown in figure 2.15. The thickness of the silicon (or chip) is seen to have a profound effect on the temperature of the hot spot, decreasing with chip thickness until a minimum temperature is reached and then rising as the chip thickness approaches zero. The minimum hotspot temperature, with both the silicon microcooler and the superlattice microcooler, respectively, is seen to occur at nearly the same chip thickness of 40-50µm. This provides an "optimal" ratio of

microcooler width to hot spot width in the previously observed range of 5-6 [Wang *et al*, 27]. However, it is clear that the silicon μTEC provides a 1.3K lower hot spot temperature than achieved with the superlattice μTEC.

Figure 2.16 shows maximum hotspot cooling achieved by the silicon microcooler and the superlattice microcooler. Starting with a silicon chip of 200μm thickness, the cooling achieved with and without a superlattice structure improves as the Si chip becomes thinner. However, when the chip thickness approaches 10-20μm, the maximum cooling for both cases levels off. Once again, the maximum hot spot cooling achieved by the silicon μTEC is greater by about 0.5K than the maximum cooling value of the superlattice μTEC.

The variation in hot spot temperature with the thickness of silicon reflects the competing effects of lower conductive resistance (beneficial) and greater proximity to Joule heating in the chip (detrimental) associated with a reduced separation distance between the microcooler and the hot spot.

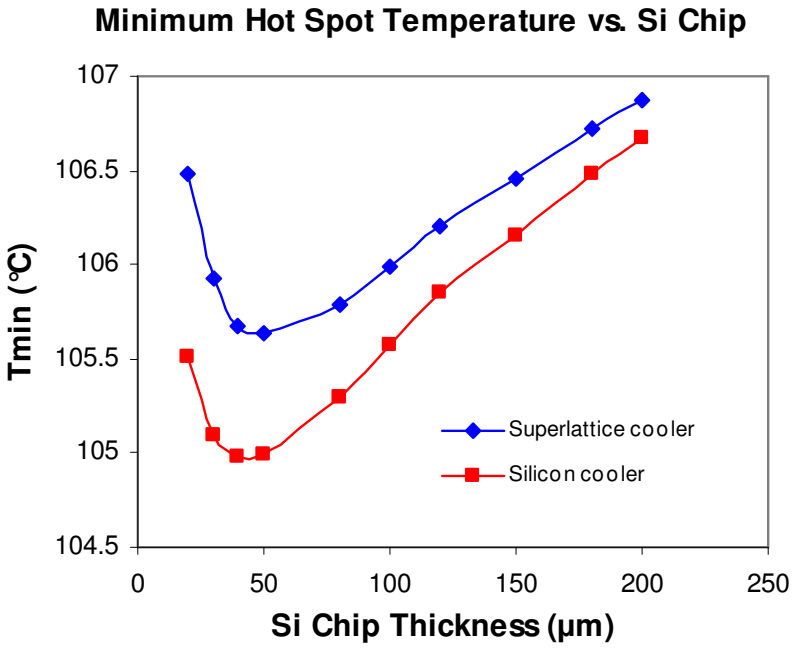



**Figure 2.15: Temperature variation in µTEC cooled silicon chip – varying chip thickness [200x200µm$^2$ cooler, 10µm superlattice, 70x70µm2 hot spot, and 680W/cm$^2$ hot spot heat flux].**

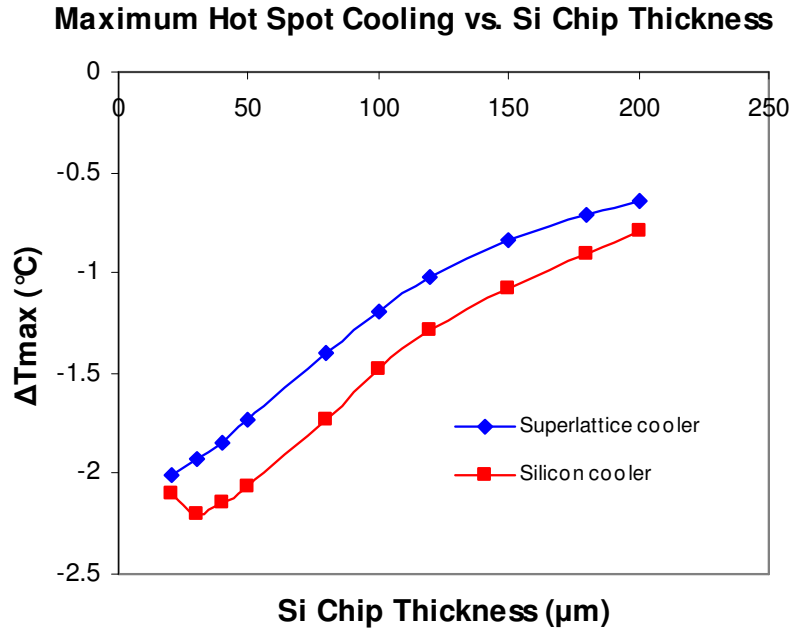



**Figure 2.16: Temperature reduction in µTEC cooled silicon chip - varying chip thickness [200x200µm$^2$ cooler, 10µm superlattice, 70x70µm$^2$ hot spot, and 680W/cm$^2$ hot spot heat flux].**

### 2.4.2.3 Microcooler Size

To clarify the effect of microcooler and Si chip geometry, the impact of microcooler size on hot spot cooling, for a fixed chip thickness of 50µm, was explored. Figure 2.17 reveals a relatively broad optimum for the microcooler dimension, falling within 200x200µm$^2$ to 300x300µm$^2$ for the silicon microcooler and within 300x300µm$^2$ to 400x400µm$^2$ for the superlattice microcooler, and providing only a modest improvement beyond the cooling achieved with the 200x200µm$^2$ microcoolers. As seen in figure 2.18, the silicon microcooler was able to reduce the hot spot temperature by more than 2.2K at 250x250µm$^2$, or about 0.6K greater than the superlattice microcooler. However, this advantage begins to diminish as the microcooler becomes larger and the effects of the superlattice become less pronounced. The apparent optimal microcooler-to-chip ratio of 5-6 is again in agreement with the previously findings by Wang *et al* [24].

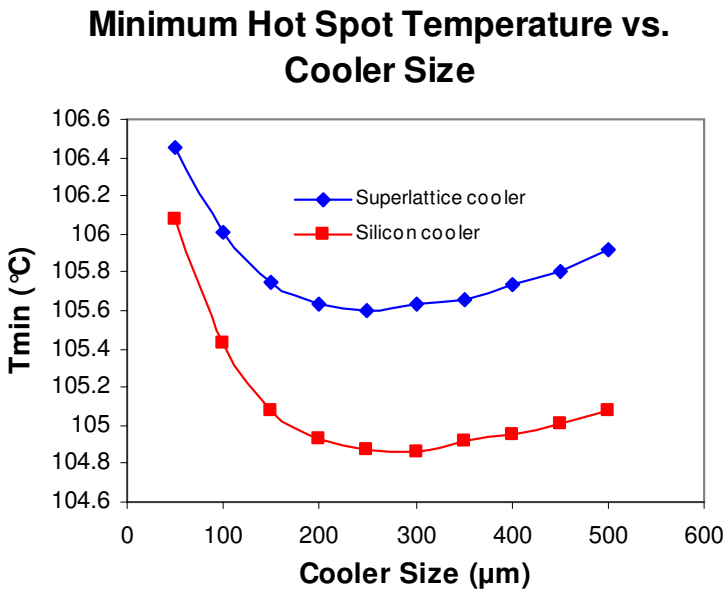



**Figure 2.17: Temperature variation in µTEC cooled silicon chip – varying microcooler size [10µm superlattice, 50µm Si chip, 70x70µm$^2$ hot spot, and 680W/cm$^2$ hot spot heat flux].**

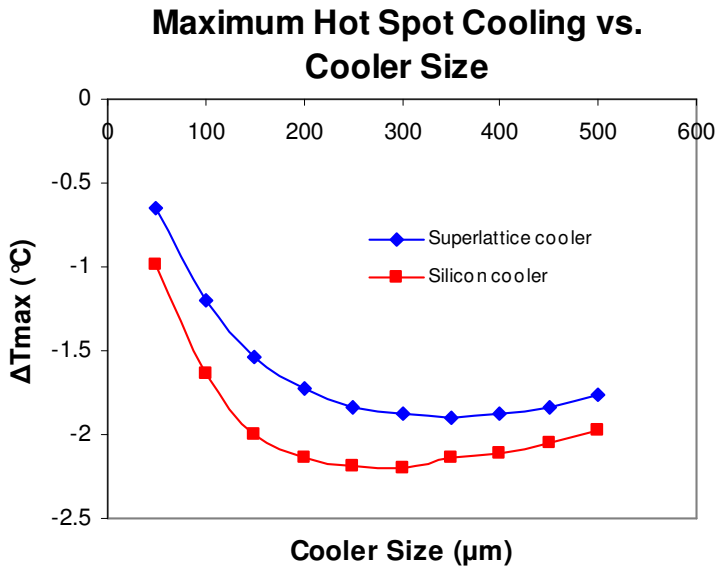



**Figure 2.18: Temperature reduction in μTEC cooled silicon chip - varying microcooler size [10μm superlattice, 50μm chip, 70x70μm$^2$ hot spot, and 680W/cm$^2$ hot spot heat flux].**

### 2.4.2.4 Hot Spot Size and Hot Spot Heat Flux

To complete the parametric exploration of the potential benefits associated with the use of superlattice microcoolers, the hot spot size and heat flux – providing thermal boundary conditions for the ANSYS™ model - will be varied for the fixed baseline geometry. As evident in figures 2.19 and 2.20, the hot spot temperature increases nearly linearly with these two boundary conditions. Despite the relatively thin chip analyzed in this study, it is noteworthy that the linear dependence of the hot spot temperature with hot spot heat flux and hot spot side length is reminiscent of the classical result for a discrete heat source, i.e. hot spot, on a semi-infinite slab, given by equation 2.8 [37]:

$$\Delta T_{semi-\inf} = \frac{q''_{hs,semi} w_{hs}}{\pi^{0.5} k_{Si}} \tag{2.8}$$

where $q_{hs,semi}$'' is the heat flux of the hot spot on the semi-infinite slab, $w_{hs}$ is side length of the hot spot, and $k_{si}$ is the thermal conductivity of the silicon chip, or semi-finite slab.

However, the thermoelectric-induced cooling of the hot spot is nearly invariant with hot spot heat flux and size, remaining virtually constant across the range examined. Thus, as seen in figures 2.21 and 2.22, respectively, the superlattice equipped microcooler reduces the hot spot temperature by nearly 1.75K, while the 200x200μm$^2$ silicon microcooler lowers the temperature by close to 2.1K, for hot spots ranging from 20x20μm$^2$ - 200x200μm$^2$, as the hot spot heat flux increases from 300 to 1000W/cm$^2$. Clearly, these results show once again that the silicon microcooler achieves greater hot spot cooling than the superlattice microcooler.

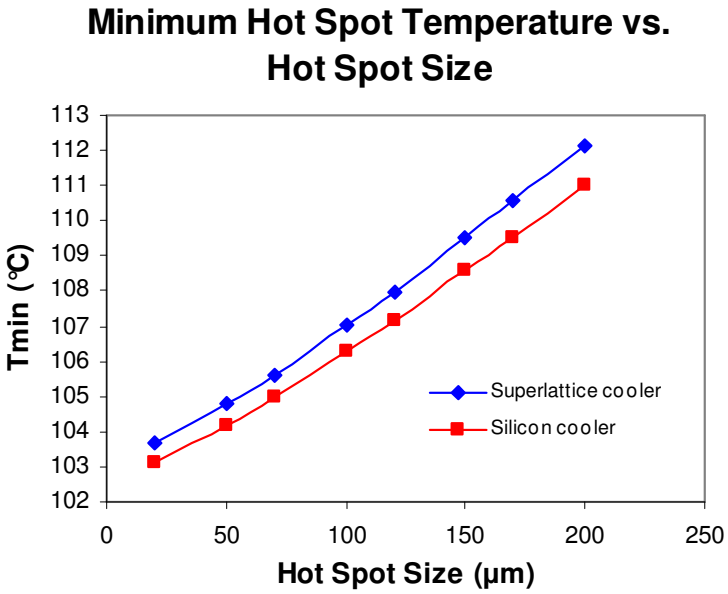



**Figure 2.19: Temperature variation in μTEC cooled silicon chip - varying hot spot size [10μm superlattice, 50μm chip, 200x200μm$^2$ microcooler, and 680W/cm$^2$ hot spot heat flux].**

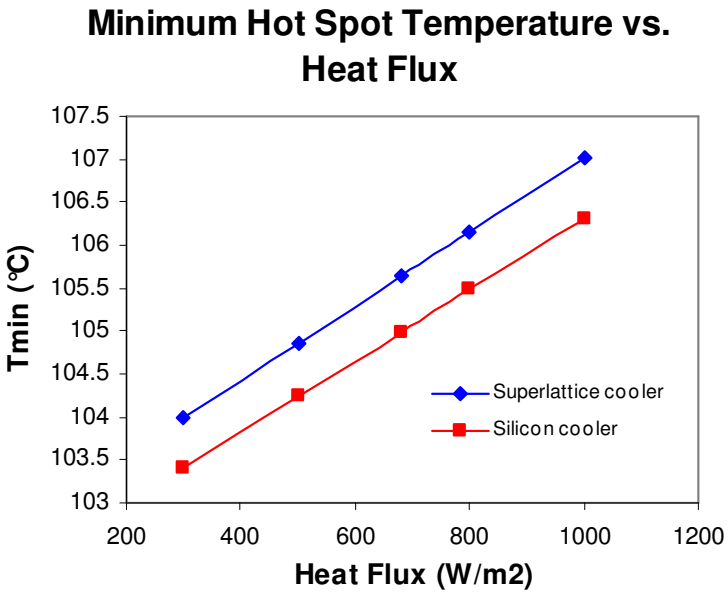



**Figure 2.20: Temperature variation in µTEC cooled silicon chip – varying hot spot heat flux [10µm superlattice, 50µm Si chip, 200x200µm$^2$ microcooler, and 70x70µm$^2$ hot spot].**

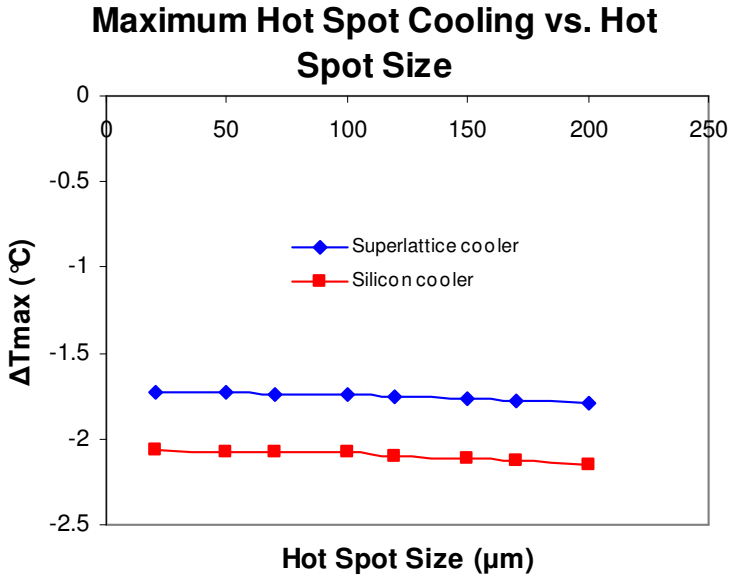



**Figure 2.21: Temperature reduction in µTEC cooled silicon chip - varying hot spot size [10µm superlattice, 50µm chip, 200x200µm$^2$ microcooler, and 680W/cm$^2$ hot spot heat flux].**

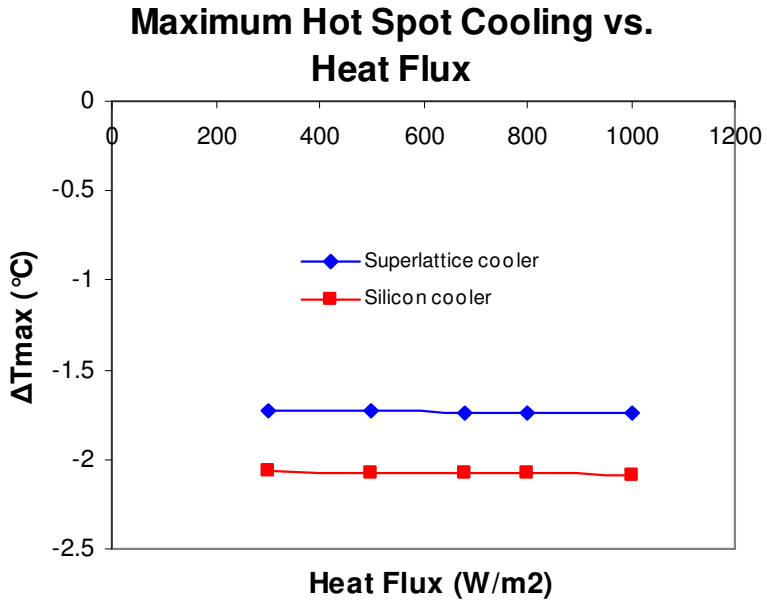



**Figure 2.22: Temperature reduction in µTEC cooled silicon chip – varying hot spot heat flux [10µm superlattice, 50µm Si chip, 200x200µm$^2$ microcooler, and 70x70µm$^2$ hot spot].**

## 2.5 Conclusion

A geometric and thermal boundary condition parametric analysis of hot spot cooling has been performed using the results of a finite element simulation of a thermoelectric microcooler, with and without an integrated superlattice structure. Superlattice thickness, silicon chip thickness, microcooler size, hot spot size, and hot spot heat flux were systematically varied while the other four parameters were held constant. It was determined that while the top surface of the superlattice always achieves the lowest local temperatures, hot spot cooling and hot spot temperature reduction does not benefit from the use of a microcooler with an integrated superlattice.

# Chapter 3

# 3. TEC Mini-Contact Cooling of On-chip Hot Spot

## 3.1 Introduction

The work detailed in this chapter has been a collaborative effort between the University of Maryland College Park (UMD) and a Taiwanese national lab [30] to explore the potential use of mini-contact TEC's for cooling on-chip "hot spots" within Taiwanese packages. The mini-contact, which is attached between the Si chip and TEC, is a high thermal conductivity pad that concentrates and increases the cooling flux of the TEC. UMD has used a numerical ANSYS™ finite element (FE) model to design and identify the optimum dimensions of the mini-contact pads for three different chip package configurations; two using Taiwanese designed TECs (with 250μm and 500μm TE leg heights) [30] and one configuration with a commercially available thin film TEC (TFTEC) [31]. These simulations were used to determine on-chip hot spot temperature reductions and temperature distributions along the active surface of the chip.

This chapter also outlines the parameters and assumptions used in the ANSYS™ FE analysis. Model geometry, boundary conditions, material properties, and meshing are discussed and a solution for the maximum hot spot cooling, as a function of mini-contact size, is presented. Under the assumption that thermal contact resistance is very low at the Si chip/mini-contact/TEC interfaces, ANSYS™ simulations project hot spot cooling of 18.6°C and 17.7°C for active Taiwanese TEC's with TE leg heights of 250μm and 500μm TECs, respectively, and hot spot cooling of 3.6°C for an active commercial TFTEC relative to when the TEC device is turned off.

Additional ANSYS™ simulations were performed to reduce negative effects associated with the presence of the TEC/mini-contact using a hypothetical TEC with optimized TE leg height and mini-contact size. The optimized TEC produced 13.3°C of hot spot cooling when operating at optimum current and reduced the hot spot temperature by 9.3°C compared to a chip package with no TEC/mini-contact present. ANSYS™ simulations were also performed to reduce negative effects associated with the presence of the TFTEC/mini-contact using a decreased lateral heat spreader gap. This chip package configuration only produced 2.6°C of hot spot cooling when operating at optimum current. Suggestions are made to improve overall cooling performance of mini-contact TEC's and for future studies of this cooling approach.

## 3.2 Mechanism and Simulation of Mini-Contact Enhanced TEC for Hot Spot Cooling

### 3.2.1 Concept of Mini-Contact Pad

The implementation of a thermally conductive copper mini-contact between a silicon chip and a TEC can serve to dramatically increase the cooling flux of the TEC by concentrating it onto a smaller, more localized area [38].

One of the main advantages of this novel cooling approach is that it enhances the thermal performance of TEC technology achievable with present commercial practice. Wang *et al* have previously investigated this approach and predicted hot spot temperature reductions of as much as 10-15K, depending on thermal contact resistance [28,29].

Figure 3.1 shows the concept of the mini-contact enhanced TEC. Uniform thermoelectric cooling of the chip in, figure 3.1a, results in elevated temperatures on the active surface of the chip near the hot spot. Alternatively, implementing the mini-contact,

in figure 3.1b, focuses the cooling flux of the TEC directly over the hot spot and allows the TEC to remove a significantly larger fraction of the hot spot heat dissipation. Another unique feature of this novel cooling technology is that it only introduces a thin TEC/mini-contact/spacer layer on the backside of the chip that can be integrated with a conventional heat spreader and/or heat sink.

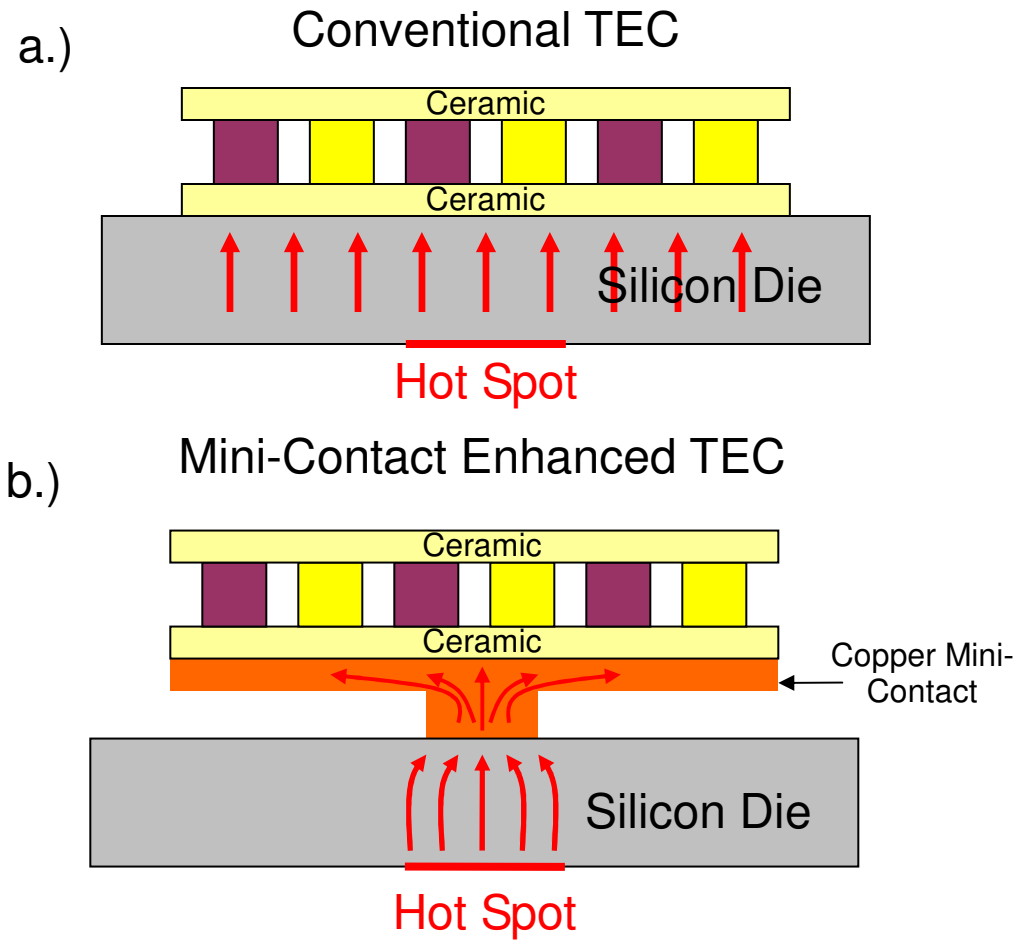



**Figure 3.1: Concept of the mini-contact enhanced TEC for on-chip hot spot removal**

### 3.2.2 Numerical simulation of Taiwanese Mini-Contact Package

#### 3.2.2.1 Package Geometry

Figures 3.2 and 3.3 below display the proposed Taiwanese chip packages with the Taiwanese designed TEC and commercial TFTEC, respectively. Both package

configurations feature an integrated mini-contact. Tables 3.1 and 3.2 provide the dimensions and thermal conductivity values for the Taiwanese TEC and commercial TFTEC packages, respectively. The Taiwanese TEC chip package, as described in an email from the Taiwanese lab [39], is comprised of a JEDEC thermal test board, solder ball layer, silicon substrate, micro bump/filler layer, and a silicon thermal test chip attached to a mini-contact, TEC, and TIM2 interface, listed in sequence starting at the silicon substrate. The heat spreader surrounds the Si chip, mini-contact, and TEC and dissipates heat towards the TIM1 interface and heat sink above. The commercial TFTEC package, shown in figure 3.3 and described in an email from the Taiwanese lab [40], is very similar to the package described above, but features the commercial cooler and contains a diamond-like carbon (DLC) layer between the TIM2 layer and the Al heat spreader. DLC is a very thin 2µm deposited layer with very high thermal conductivity (~467W/mK - assumed isotropic) and high electrical resistivity; it acts as an electrical insulator such that metal traces can be deposited onto it to enable wire bonding to the TEC. Both packages feature similar dimensions and material properties; however, the commercial TFTEC is much smaller than the Taiwanese designed TECs.

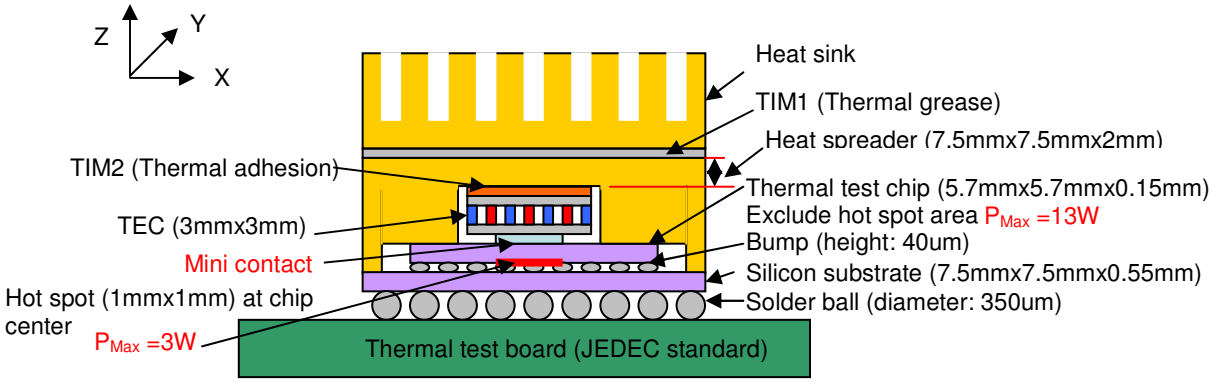



**Figure 3.2: Proposed Taiwanese mini-contact chip package with Taiwanese designed TEC [39]**

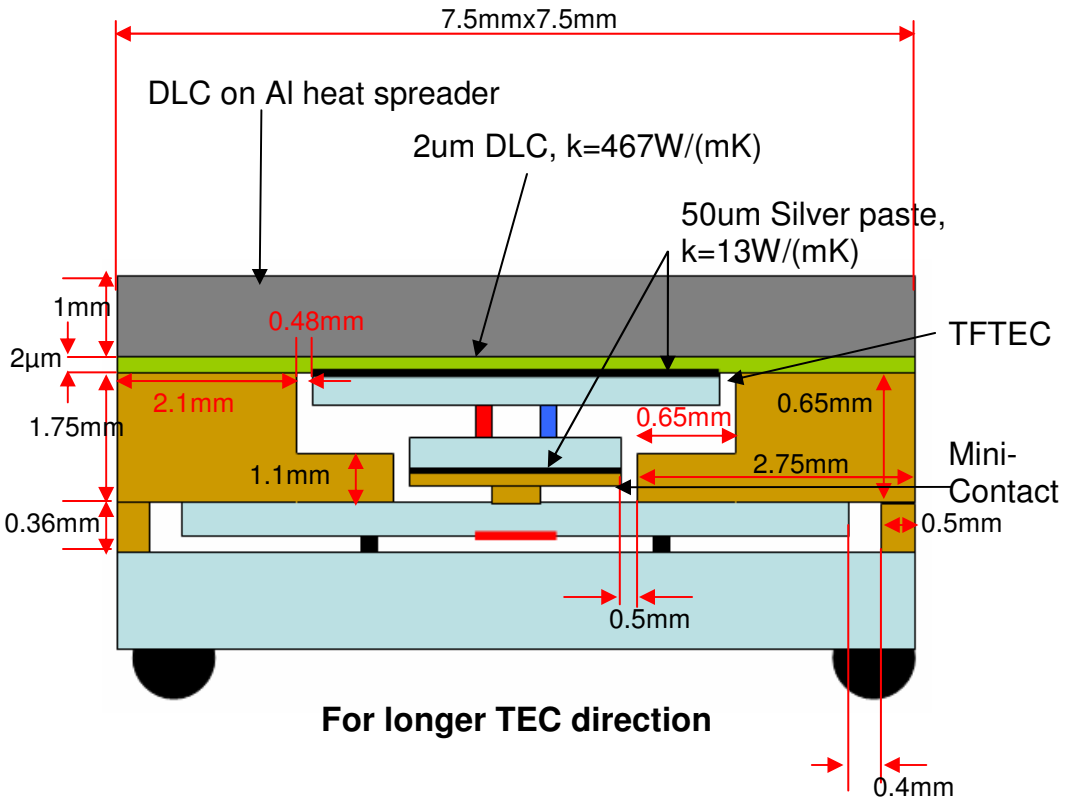



**Figure 3.3: Proposed Taiwanese mini-contact chip package with commercial TFTEC [40]**

**Table 3.1: FE Package Geometry and Thermal Conductivity for Taiwanese TEC**

| | Geometry (X Y Z) | Materials | Thermal Conductivity |
|---|---|---|---|
| **Silicon Substrate** | 7.5mm x 7.5mm x 0.55mm | Si | 95-120 W/mK* |
| **Micro Bump Layer** | 5.7mm x 5.7mm x 40µm | Cu/Sn | 5 W/mK ** |
| **Silicon Chip** | 5.7mm x 5.7mm x 150µm | Si | 95-120 W/mK* |
| **Mini Contact Tip** | 50µm in z-direction*** | Cu | 360 W/mK |
| **Mini Contact Base** | 3mm x 3mm x 100µm | Cu | 360 W/mK |
| **Bottom Ceramic Substrate** | 3mm x 3mm x 380µm | AlN ceramic | 180 W/mK |
| **TE Elements** | Z dim. of 250µm & 500µm | Bi2Te3 | 0.35-0.66 W/mK* |
| **Bottom Ceramic Substrate** | 3mm x 3mm x 380µm | AlN ceramic | 180 W/mK |
| **TIM2** | 3mm x 3mm x 100µm | | 30 W/mK |
| **Heat Spreader** | 7.5mm x 7.5mm x 2mm | Cu | 360 W/mK |
| **TIM1** | 7.5mm x 7.5mm x 175µm | | 30 W/mK |
| **Heat Sink** | 3cm x 3cm x 1cm | Al | 180 W/mK |

**Table 3.2: FE Package Geometry and Thermal Conductivity for commercial TFTEC**

| | Geometry (X Y Z) | Materials | Thermal Conductivity |
|---|---|---|---|
| **Silicon Substrate** | 7.5mm x 7.5mm x 0.55mm | Si | 95-120 W/mK* |
| **Micro Bump Layer** | 5.7mm x 5.7mm x 210µm | Cu/Sn | 5 W/mK ** |
| **Silicon Chip** | 5.7mm x 5.7mm x 150µm | Si | 95-120 W/mK* |
| **Mini Contact Tip** | 500µm in z-direction**** | Cu | 360 W/mK |
| **Mini Contact Base** | 740µm x 740µm x 500µm | Cu | 360 W/mK |
| **TIM1** | 740µm x 740µm x 50µm | | 13 W/mK |
| **Bottom Ceramic Substrate** | 740µm x 740µm x 250µm | AlN ceramic | 180 W/mK |
| **TE Elements** | 300µm x 300µm x 20µm | Bi2Te3 | 1 W/mK***** |
| **Top Ceramic Substrate** | 2.34mm x 1.24mm x 250µm | AlN ceramic | 180 W/mK |
| **TIM2** | 740µm x 740µm x 50µm | | 13 W/mK |
| **Cu Heat Spreader** | 7.5mm x 7.5mm x 2mm | Cu | 360 W/mK |
| **DLC** | 7.5mm x 7.5mm x 2µm | | 467 W/mK |
| **Al Heat Spreader** | 7.5mm x 7.5mm x 1mm | Al | 180 W/mK |
| **TIM3** | 7.5mm x 7.5mm x 50µm | | 13 W/mK |
| **Heat Sink** | 3cm x 3cm x 1cm | Al | 180 W/mK |

* Temperature dependent thermal conductivity is used.

** The micro bump layer is assumed to be a single homogeneous layer with an effective isotropic thermal conductivity to reflect the combined effect of the Cu bumps and Sn filler. The preliminary thermal conductivity of this layer is estimated at 5W/mK.

*** The x-y dimensions of the mini-contact tip vary from 100µm x 100µm to 1800µm x 1800µm; the z-dimension remains constant.

**** The x-y dimensions of the mini-contact tip vary from 200µm x 200µm to 700µm x 700µm; the z-dimension remains constant.

***** The thermal conductivity of the $Bi_2Te_3$ is assumed to be lower than the bulk value of ~1.5W/mK because the $Bi_2Te_3$ is epitaxially grown in layers.

The FE model was built in ANSYS™ finite element software according to the dimensions and materials specified in the mini-contact package design provided by the Taiwanese lab [39,40]. The width and length of the mini-contact base were assumed to be the same as the bottom of the TEC ceramic substrate (3mm x 3mm and 740µm x 740µm for the Taiwanese TEC and commercial TFTEC configurations, respectively) and the in-

plane dimensions of the mini-contact tip varied anywhere from 100µm x 100µm to 1800µm x 1800µm, depending on the TEC that was being used. The total height (or thickness) of the mini-contact was assumed to be 150µm for the Taiwanese TEC package. This dimension was changed to 1mm for the commercial package as a result of assembly constraints. Difficulties in securing the tiny copper mini-contact while machining led to the larger 1mm thickness.

For the Taiwanese TEC package, the lateral gap between the heat spreader/TEC and the heat spreader/Si chip is assumed to be 100µm and the thicknesses (z-direction) of the TIM1 and the TIM2 are assumed to be 175µm and 100µm, respectively. It should be noted that the height of the doped $Bi_2Te_3$ "legs" in the Taiwanese TEC's, at 250µm and 500µm, is relatively large for the localized, high flux cooling required to remove on-chip hot spots [25] and may have limited success in reducing the hot spot temperature in the Taiwanese defined chip package.

Images of the commercial TFTEC are shown in figure 3.4, including a photograph (a) [41], perspective view (b) and side view (c) [42]. The small size of this device will minimize the detrimental effects, on the thermal resistance from the top of the Si chip, caused by the presence of the mini-contact and air gap. Additionally, figures 3.5 and 3.6 show SEM images that were taken at the Taiwanese lab of the commercial TFTEC [43]. In figure 3.5 the AlN substrates are not shown to get a better view of the Cu and $Bi_2Te_3$ layers. Figure 3.6 shows the dimensions of the inner components of the TFTEC and some voids that occur in the solder layer.

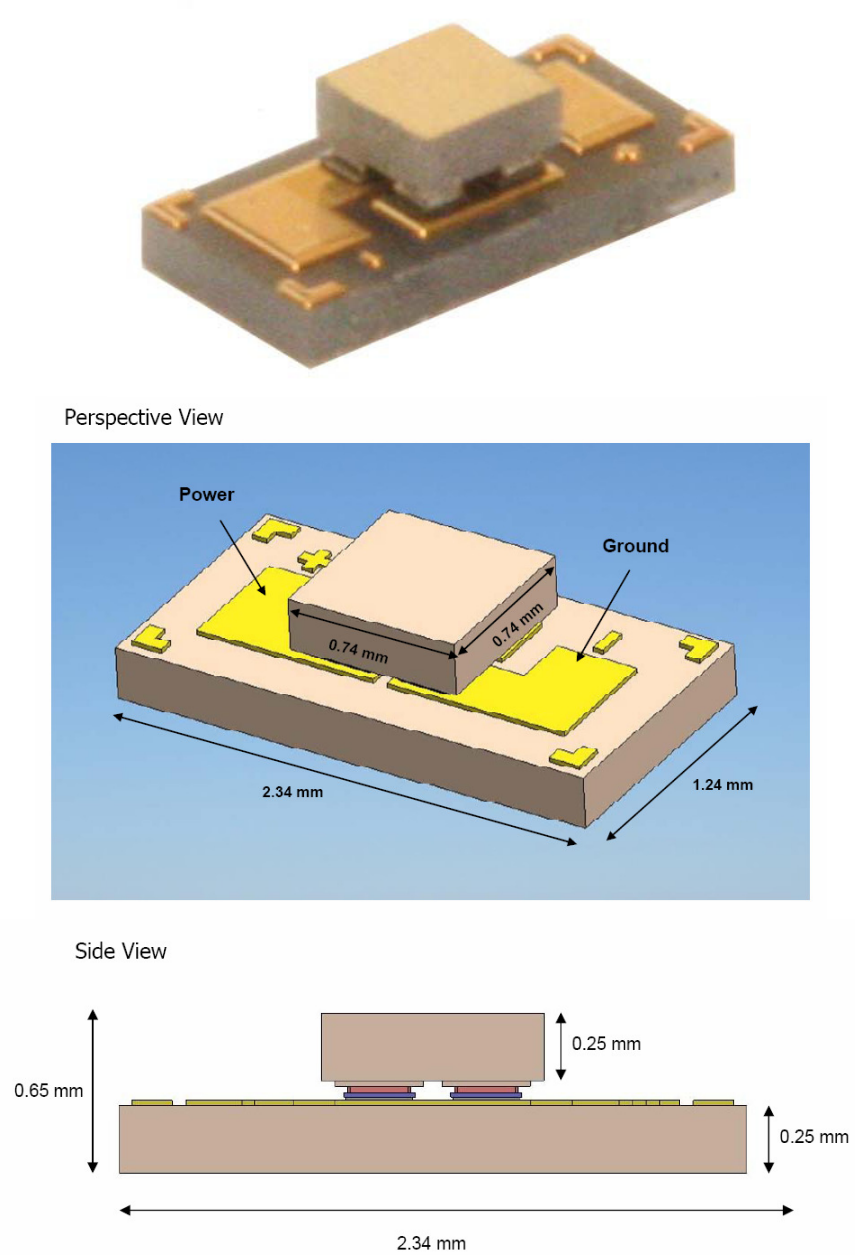



**Figure 3.4: Photograph of the commercial TFTEC (a) [41], perspective (b) and side views of the TFTEC with dimensions (c) [42]**

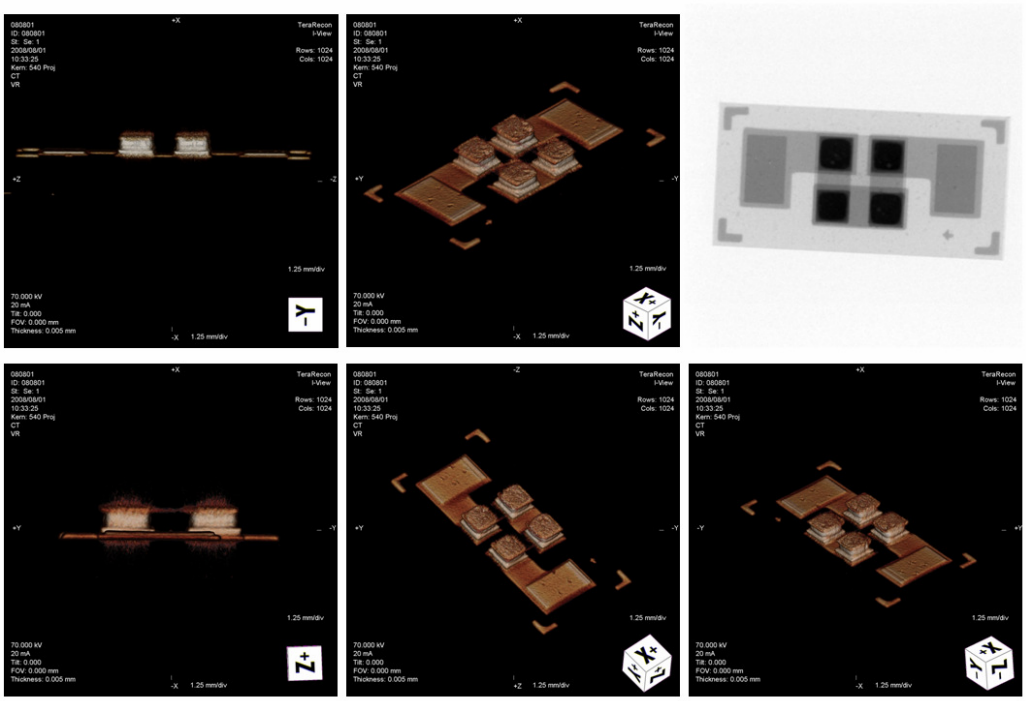


**Figure 3.5: SEM images of the TFTEC [43]**

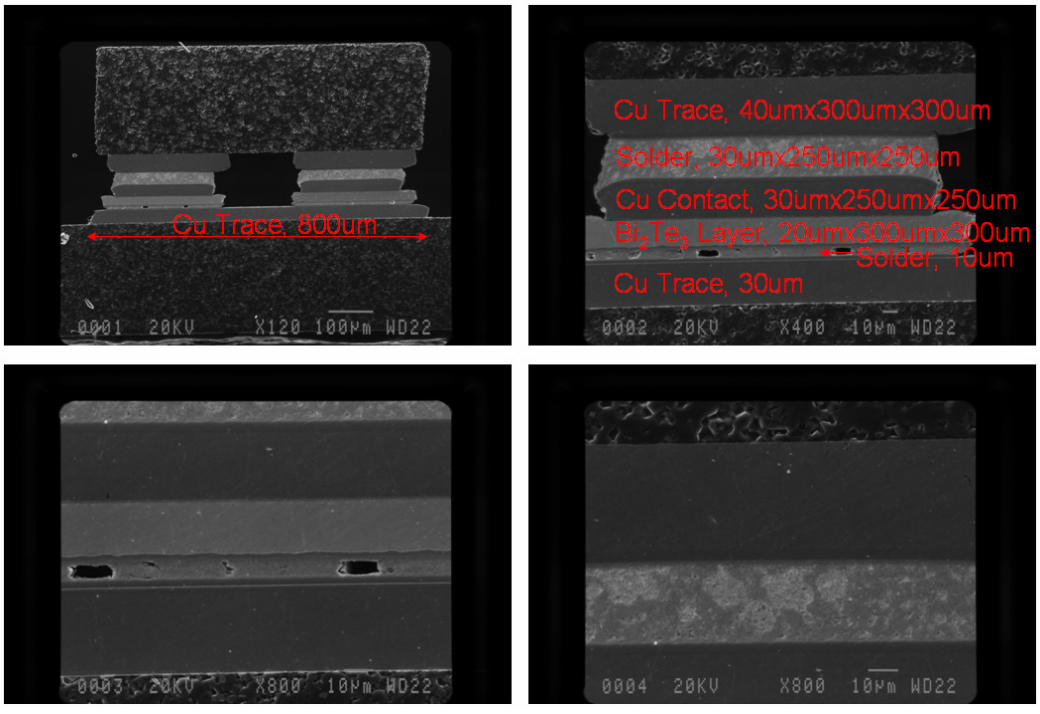



**Figure 3.6: Zoom SEM images of the Cu trace, solder, and $Bi_2Te_3$ layers in the TFTEC with dimensions [43]**

#### 3.2.2.2 Boundary Conditions

A convective heat transfer coefficient of 730W/mK was imposed on the top of the heat sink to simulate the capability of an aggressive heat sink working in forced air convection [27] to an ambient temperature of 25°C. The heat sink was modeled as a block without fins to reduce the total element number and avoid lengthy solution times.

A 1mm x 1mm hot spot producing 3W was modeled on the bottom of the Si chip as a 300W/cm$^2$ heat flux. A background heat flux of 40W/cm$^2$ was imposed on the remaining bottom area of the Si chip to provide a total chip heat generation of 13W.

##### 3.2.2.2.1 Contact resistance

In order to faithfully model the thermal behavior of the mini-contact package, a thermal contact resistance was assumed at several interfaces within the FE model, as shown in figure 3.7. The interface between the Si chip and the mini-contact tip, the interface between the mini-contact base and the TEC bottom ceramic, and the interface between the TEC top ceramic and TIM2 were all assumed to have a thermal contact resistance of $3.3 \times 10^{-7} m^2K/W$. This thermal contact resistance is also assumed for the interface between the Si chip and heat spreader, along the edge of the chip. The nominal contact resistance value of $3.3 \times 10^{-7} m^2K/W$ was selected to represent the lower range of values for clean surfaces attached with an organic bonding material [25].

In addition to thermal contact resistance, an electrical contact resistance of $1 \times 10^{-7}$ $\Omega$-cm$^2$ is assumed at both TE element/ceramic interfaces [25]. This electrical contact resistance produces a very modest heating effect (proportional to the square of the current) that nonetheless somewhat reduces the Peltier cooling that occurs at these interfaces.

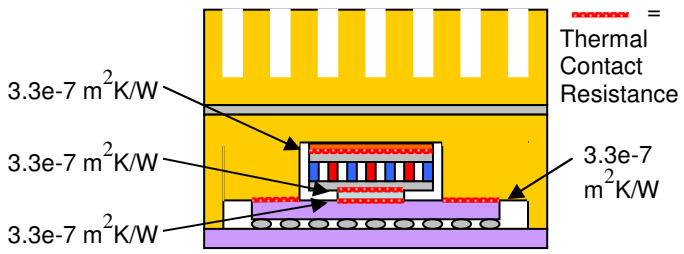



**Figure 3.7: Thermal contact resistance modeled in the Taiwanese chip package**

### 3.2.2.3 Material Properties

The Taiwanese designed TEC has lateral dimensions of 3mm x 3mm. Assuming this TEC is assembled of cubes with side lengths of 250µm and 500µm, respectively, with a 250µm separation gap in each direction and 125 µm gap along the edge, the TEC can accommodate a 6x6 array of the 250µm TE legs and a 4x4 array of the 500µm TE legs. The 6x6 array offers a $Bi_2Te_3$ coverage area of 25% and the 4x4 array offers a coverage area of 44.4%, yielding a weighted-average, effective thermal conductivity of 0.35W/mK and 0.65W/mK for the TECs assembled with these two TE leg dimensions. The figure below depicts a quarter-symmetry model of the Taiwanese TEC for the two different TE heights.

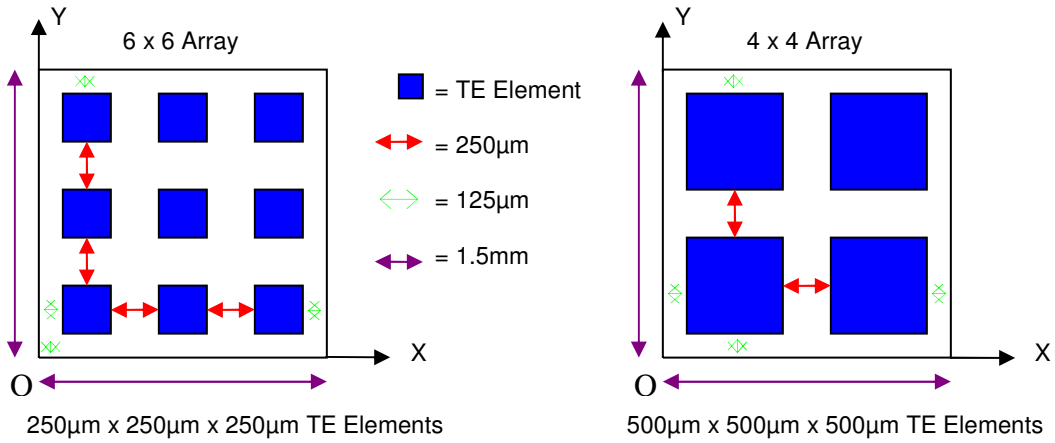



**Figure 3.8: Quarter-symmetry model of TEC**

To more accurately capture the thermal behavior of the bismuth telluride ($Bi_2Te_3$) in the TEC, the temperature dependence of the properties of this material is included in the model. For the operating conditions of the Taiwanese package, and as seen in preliminary simulations, the temperature of the $Bi_2Te_3$ can be expected to range from 90°C to 130°C. Following [25], figure 3.9 displays the temperature variation of thermal conductivity, electric resistivity, and the Seebeck coefficient for $Bi_2Te_3$.

For simplicity, the material properties of the $Bi_2Te_3$ in the commercial TFTEC package were assumed to be constant with temperature. The following values were used: a Seebeck coefficient of 210μV/K, a thermal conductivity of 1W/mK, and an electric resistivity of 53.3Ω-μm. These values produce TFTEC cooling values nearly identical to those given by [42].

For both package configurations, the silicon chip and silicon substrate are known to have a temperature dependent thermal conductivity. In the anticipated silicon chip temperature range, of approximately 75°C to 145°C, ANSYS™ uses a linear fit between the four data points, shown in figure 3.10 to assign the corresponding thermal conductivity value to the silicon.

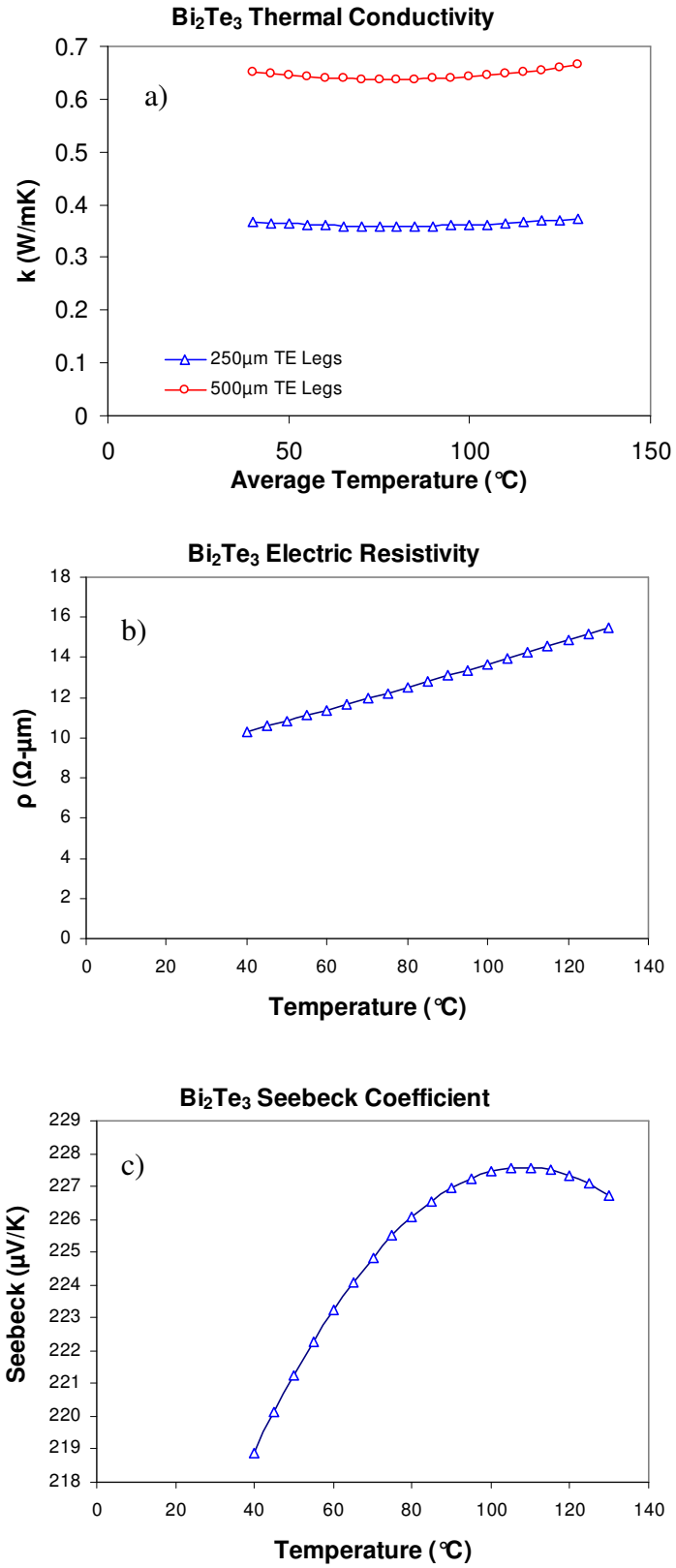



**Figure 3.9: Temperature dependent properties for $Bi_2Te_3$: a) Thermal conductivity, b) Electric Resistivity, c) Seebeck coefficient**

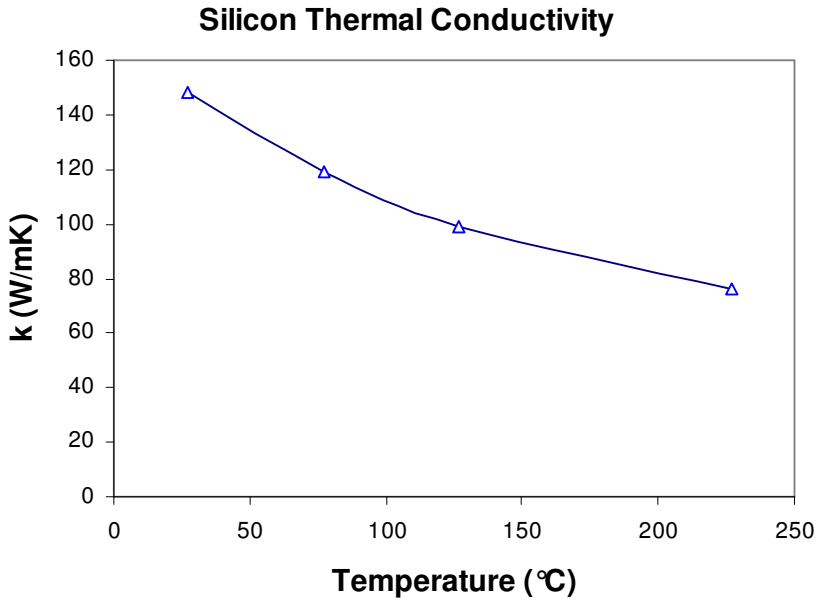
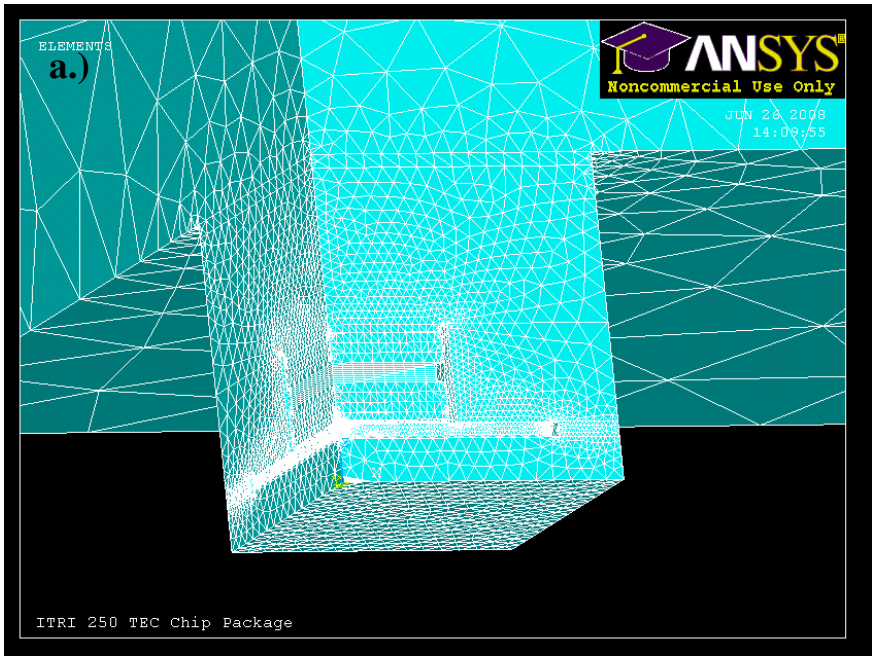



**Figure 3.10: Temperature dependent thermal conductivity for silicon**

### 3.2.2.4 Element and Mesh Description

The ANSYS thermal solid element - Solid70 - was used to build a quarter-symmetry model of the Taiwanese package and to perform the required thermal simulation. This element was used to solve for the steady state heat diffusion field within the FE model with one degree of freedom at each node (Temperature). The element count for the quarter-symmetry FE model was approximately 130,000-180,000 and 12 help volumes were generated within the Si chip, mini-contact, ceramic substrates and TE elements to produce a finer mesh in those regions. The $Bi_2Te_3$ layer is map-meshed for greater accuracy. The mesh distributions are shown for the Taiwanese TEC and TFTEC packages in figures 3.11a and 3.12a, respectively. Mesh sensitivity is also given for the two different packages (figures 3.11b and 3.12b) and the temperature solution is observed to have little variance with greatly increased element count. The absolute temperatures at the $Bi_2Te_3$/ceramic substrate interfaces were required to solve for the Peltier cooling and

heating fluxes at the TEC. Since these temperatures were unknown, they were guessed and verified in the solution. The guessed temperature was always within 0.5K of the solved temperature at the TEC interfaces. This process took anywhere from 2 to 5 iterations to determine the correct TEC interface temperatures per each current load.



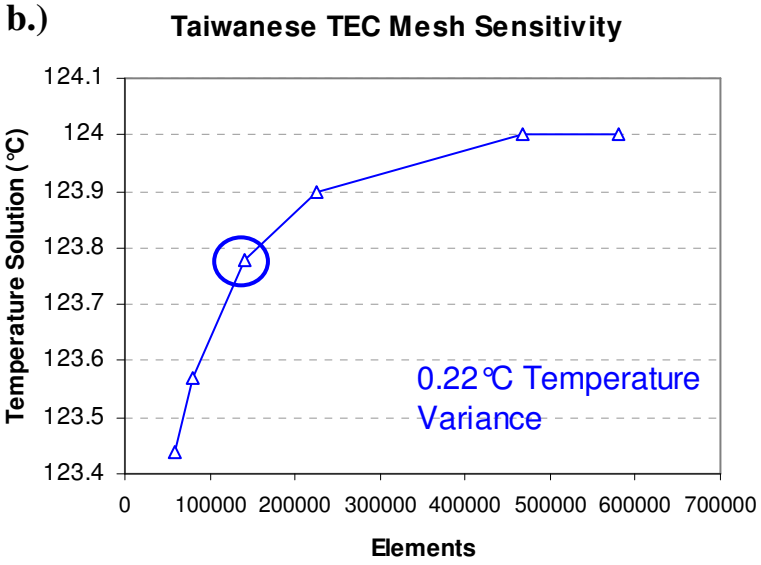




**Figure 3.11: Image of the ANSYS™ mesh distribution (a) and mesh sensitivity (b) for the Taiwanese TEC Package**

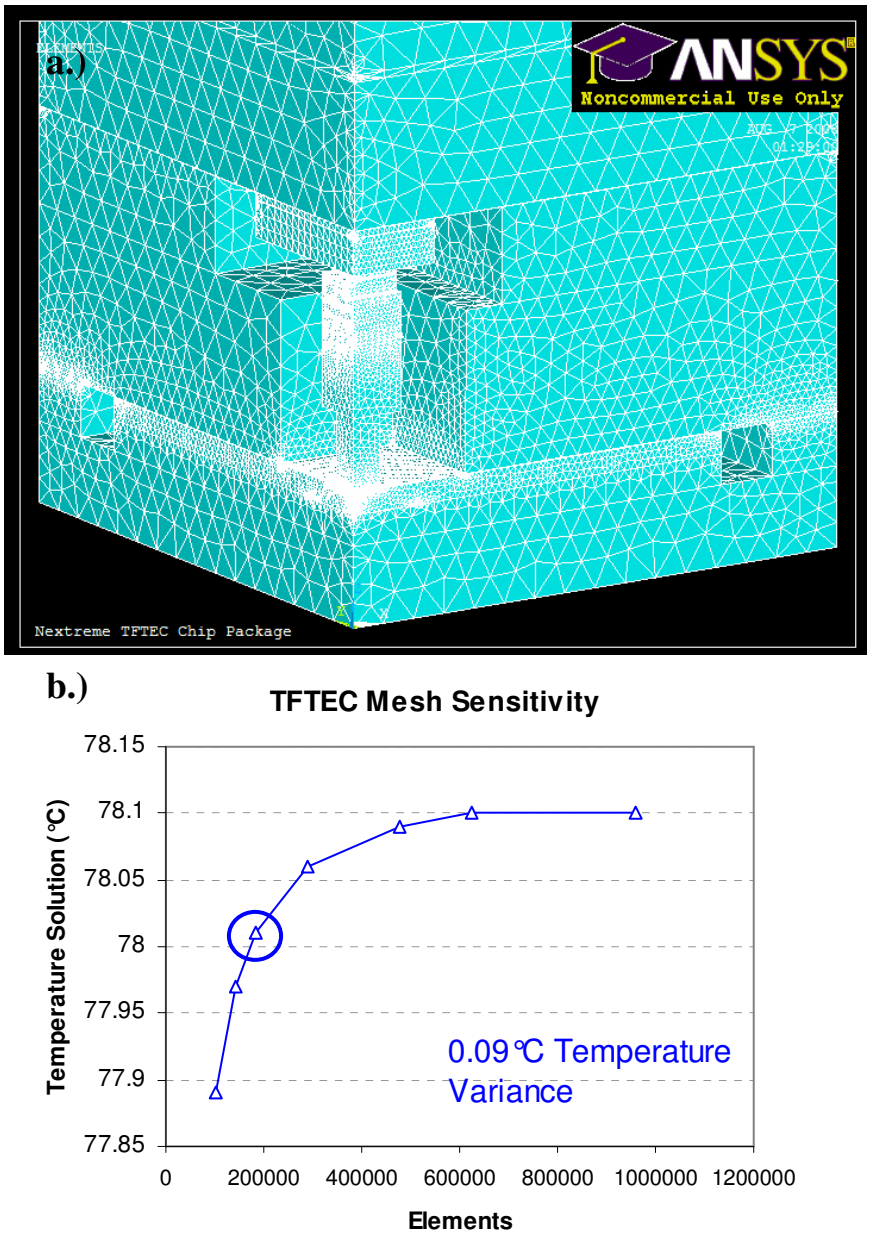



**Figure 3.12: Image of the ANSYS™ mesh distribution (a) and mesh sensitivity (b) for the TFTEC Package**

## 3.3 Results

### 3.3.1 Temperature Field

A temperature contour plot for the 500µm TEC with 300µm x 300µm mini-contact operating at a current of 2.05A is shown in figure 3.13, in a vertical cross-section

of the Taiwanese TEC chip package. Also, a temperature contour plot for the commercial TFTEC with optimized 400µm x 400µm mini-contact operating at a current of 3.29A is shown in figure 3.14.

For comparison, the temperature profile along the bottom of the Si chip for both TEC package configurations is shown in figures 3.15 and 3.16, each operating at its optimum mini-contact size and current and at a zero current. When the Taiwanese TECs are producing their maximum cooling, the active surface of the chip features a characteristic "M" temperature profile, where the greatest temperature reduction occurs at the center of the hot spot with increased temperatures at the edges of the hot spot. Both of these figures also display the temperature profile that could be expected to develop in a similar package without an integrated mini-contact TEC, in which the chip is attached directly to the heat spreader. The TFTEC package features a 50µm TIM interface (thermal conductivity of 13W/mK) between the TFTEC and heat spreader.

When powered and operating at optimum current, the Taiwanese TECs appear to yield a hot spot temperature reduction of approximately 18°C and the TFTEC yields a hot spot temperature reduction of approximately 3.6°C, relative to the unpowered condition. However, for both configurations studied, when the TEC is inactive, it appears that the low thermal conductance of the TEC and the air gap surrounding the mini-contact leads to warmer temperatures along the bottom of the chip than would be encountered in a conduction-cooled package.

The commercial TFTEC device pumps 0.61W at a stage temperature of 85°C and has an active footprint of 740um x 740um (lower AlN substrate), which equates to a cooling flux of about 112W/cm$^2$ [42]. Since this device only removes 0.61W and the hot

spot used in the Taiwanese package is 3W with an additional 13W of background heat on the bottom of the chip, the commercial TFTEC device doesn't produce a significant temperature reduction.

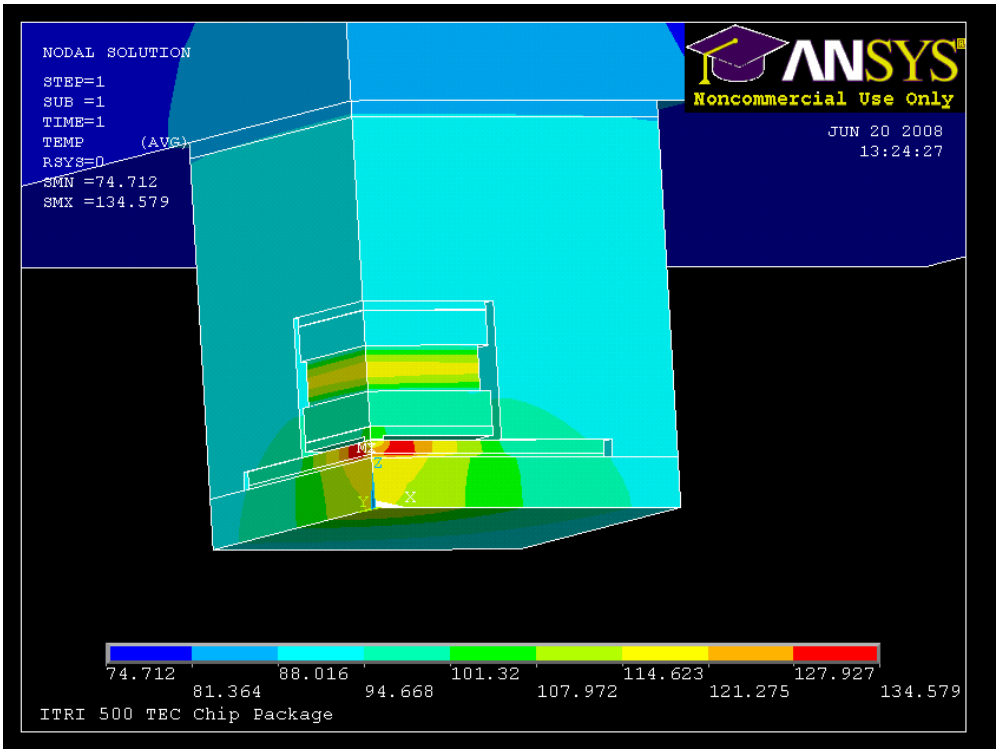



**Figure 3.13: FEM temperature distribution for an Si chip with a 1mm x 1mm hot spot producing a 300W/cm$^2$ heat flux and background heat flux of 40W/cm$^2$. The 500µm Taiwanese TEC is used with the 300µm x 300µm mini-contact**

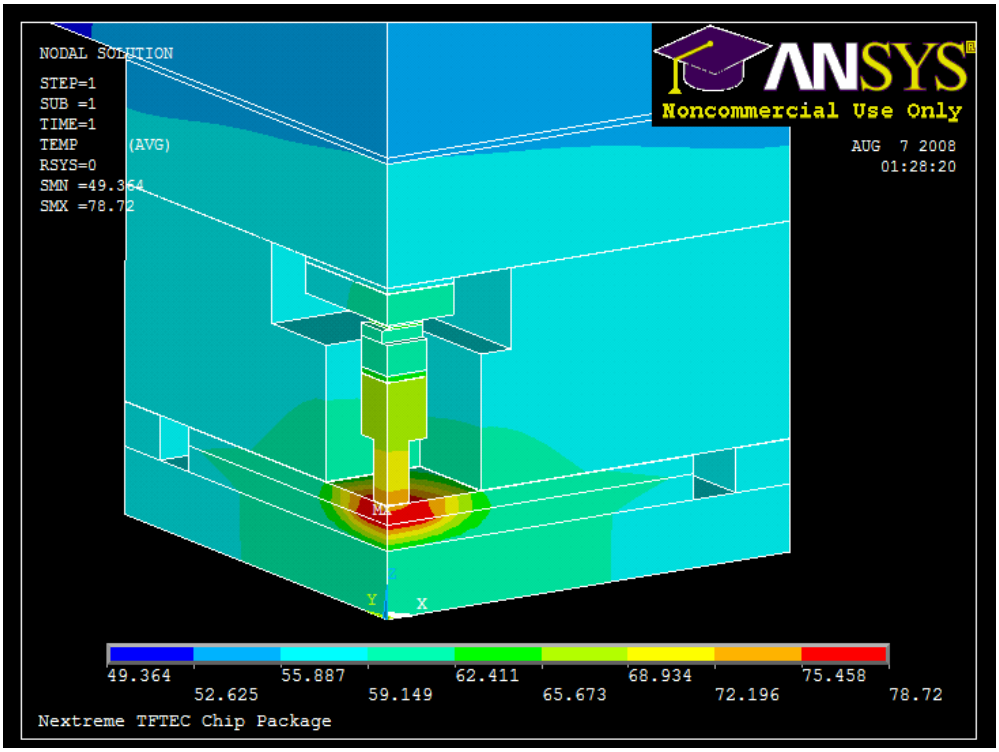



**Figure 3.14: FEM temperature distribution for an Si chip with a 1mm x 1mm hot spot producing a 300W/cm$^2$ heat flux and background heat flux of 40W/cm$^2$. The TFTEC is used with the 400µm x 400µm mini-contact**

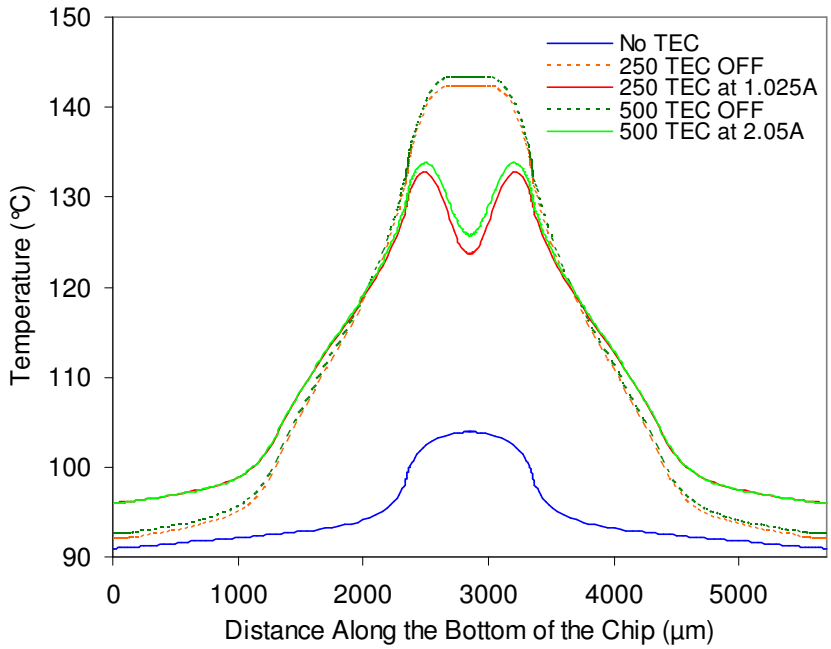



**Figure 3.15: Temperature profile along the bottom of the silicon chip, each respective TEC is operating at its optimum current and the optimum mini-contact size of 300µm x 300µm is used with the TECs**

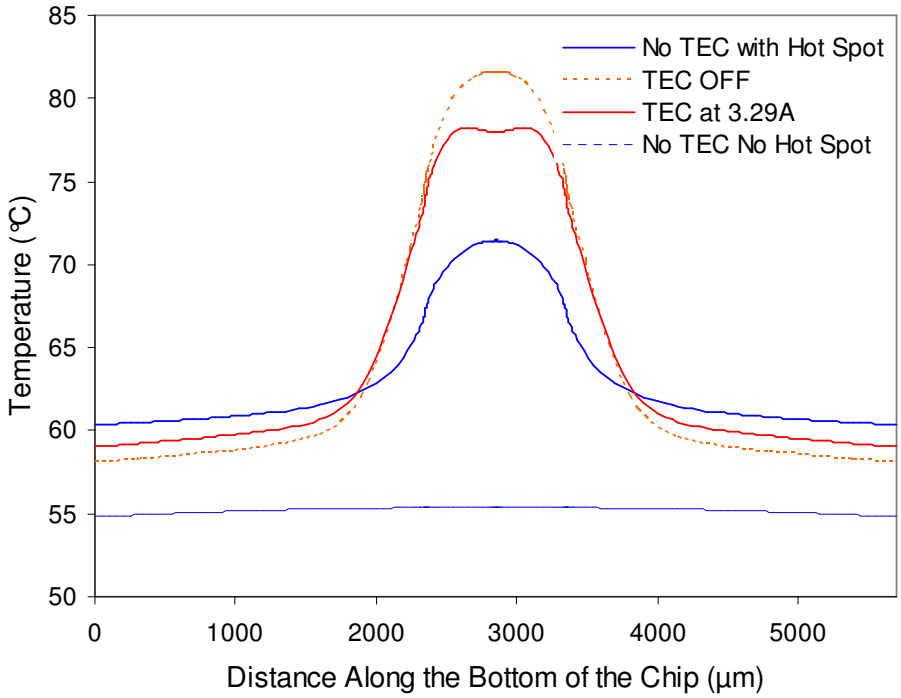



**Figure 3.16: Temperature profile along the bottom of the silicon chip. Commercial TFTEC is operating at its optimum current of 3.29A and the optimum mini-contact size of 400µm x 400µm is used**

### 3.3.2 Influence of Electric Current

The hot spot temperature reduction depends on the electric current flowing through the TEC, for the various mini-contact sizes and the two TEC leg lengths considered. The mini-contact sizes simulated varied from 100x100µm$^2$ to 1800x1800µm$^2$ for the Taiwanese TEC packages and from 200x200µm$^2$ to 700x700µm$^2$ for the commercial TFTEC package. Figures 3.17 to 3.19 show hot spot temperature reductions per input current for the three types of TECs studied. Initially, as the current increases the cooling at the hot spot increases, as well, reflecting progressively greater Peltier cooling, until the temperature reaches a minimum value. For further increases in current, the parasitic effect of Joule heating in the TE legs overcomes the Peltier cooling effect, leading to a reduction in hot spot cooling. For the conditions examined the optimum

currents are seen to fall in the range of 0.7 to 2 amps for the Taiwanese TEC packages and 3 to 3.5 amps for the commercial TFTEC package. The power consumed by the TEC depends on input current, the electrical resistance of the $Bi_2Te_3$, the number of TE legs, the temperatures at the hot and cold junctions of the TEC, the Seebeck coefficient at those junctions, and the electrical contact resistance at those junctions. In the parametric range studied, the Taiwanese TECs and commercial TFTEC typically consumed 3W and 0.5W, respectively.

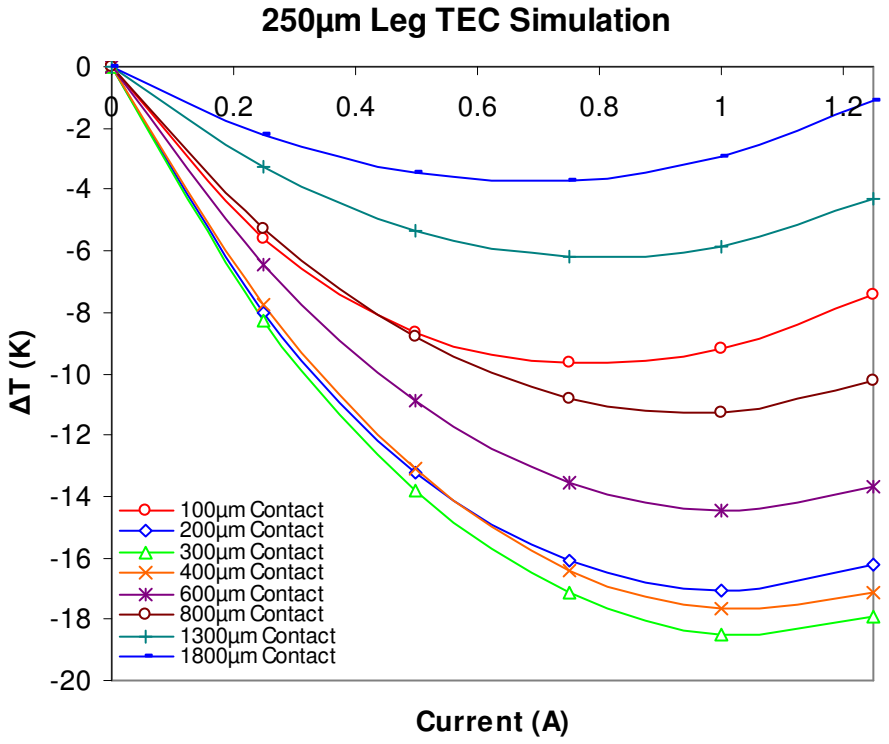



**Figure 3.17: Cooling as a function of input current to the 250µm Taiwanese TEC for various mini-contact sizes**

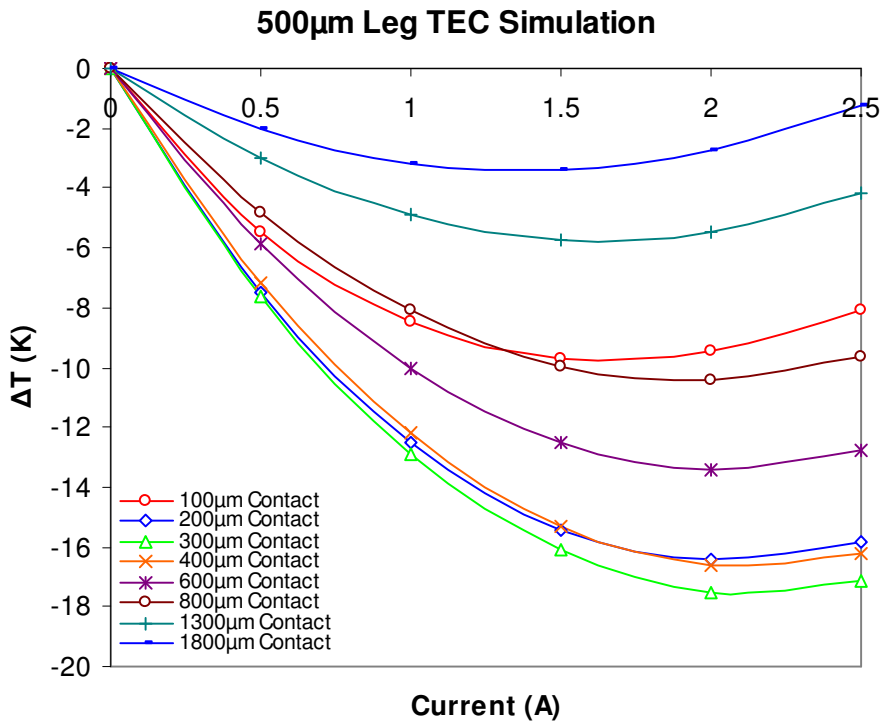



**Figure 3.18: Cooling as a function of input current to the 500µm Taiwanese TEC for various mini-contact sizes**

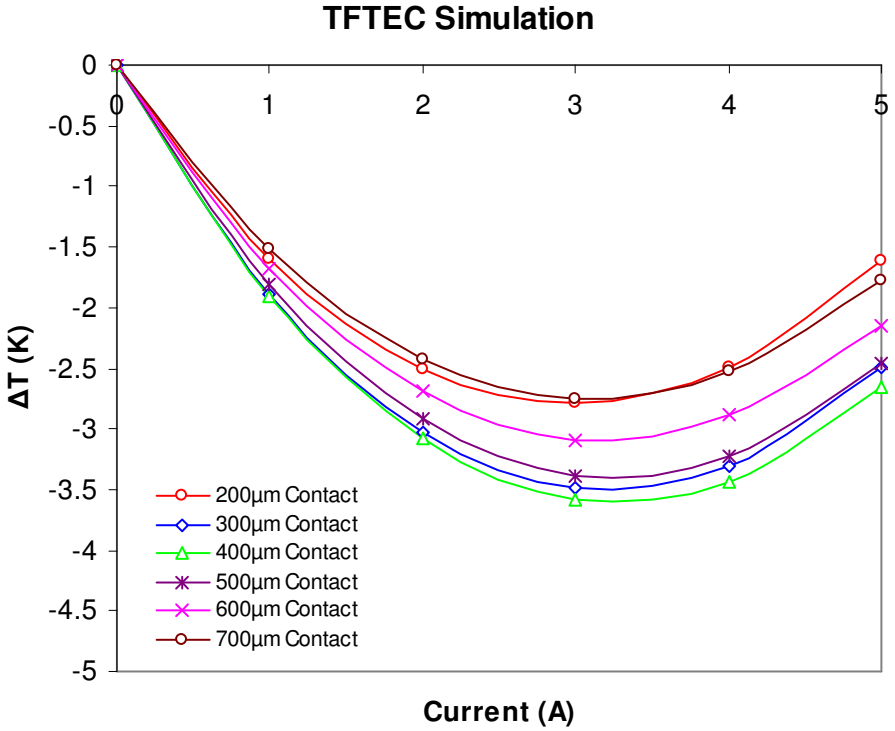



**Figure 3.19: Cooling as a function of input current to the commercial TFTEC for various mini-contact sizes**

### 3.3.3 Mini-Contact Size

The maximum temperature reduction for each respective mini-contact size and optimum current value is plotted below for the 250µm and the 500µm TE leg height TECs in figure 3.20 and for the TFTEC in figure 3.21. The 300µm x 300µm mini-contact dimensions appear to yield the largest cooling effect, with 18.6K and 17.7K temperature reductions for the 250µm and 500µm TECs, respectively. Similarly, the 400µm x 400µm mini-contact dimensions yield the largest cooling effect for the TFTEC, with 3.6K of cooling.

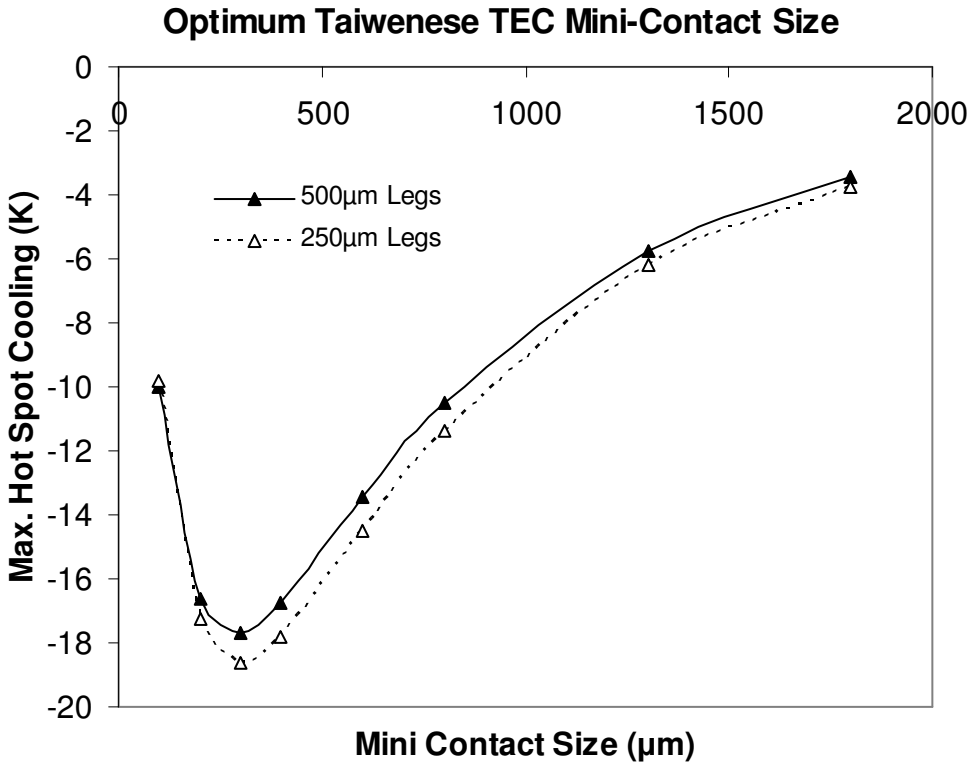



**Figure 3.20: Maximum achievable hot spot cooling as a function of mini-contact size for the Taiwanese TECs**

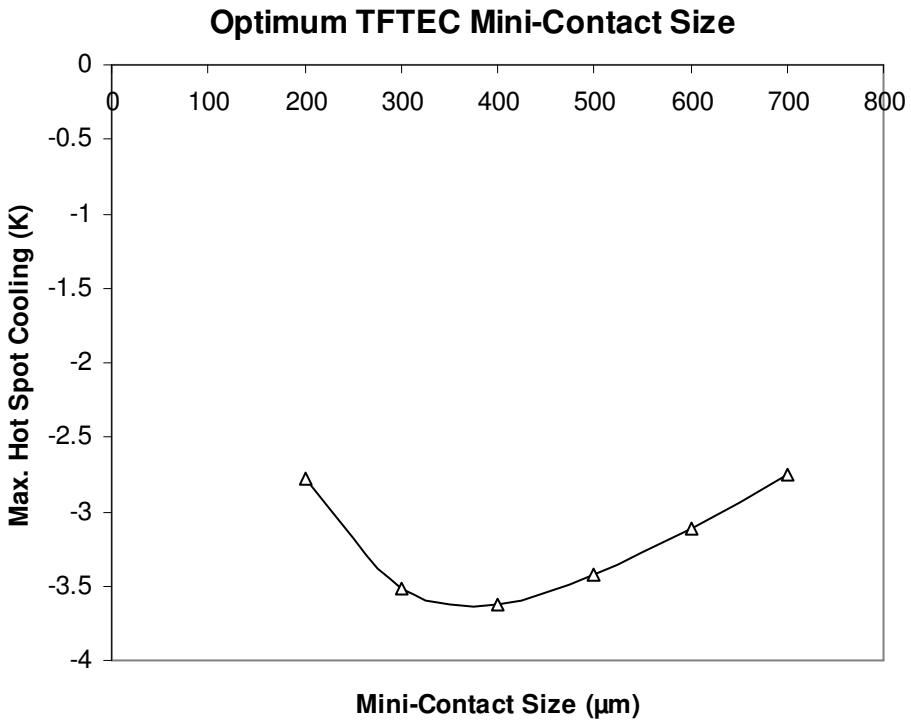



**Figure 3.21: Maximum achievable hot spot cooling as a function of mini-contact size for the TFTEC**

### 3.3.4 Optimized TEC

As shown by the temperature profile in figure 3.15, for the Taiwanese TEC configurations studied, the presence of the TEC and mini-contact within the chip package does not offer a reduction in hot spot temperature relative to a more conventional, conduction-only cooling approach. For the TEC geometry and dimensions selected by the Taiwanese lab to cool the specified chip, the additional thermal resistance resulting from the presence of the TEC increases the chip temperature more than the temperature reduction achieved by the operation of the TEC device, even after thermal optimization. Several factors could be responsible for the large temperature increase that results from the presence of the TEC/mini-contact, including the thermal resistance of the TEC and the large air gap above the hottest portion of the chip. This relatively large "TEC

coverage area" of approximately 28% of the chip area leads to poor heat dissipation and higher temperatures at the center of the chip. In order to better understand and hopefully minimize these negative effects, a hypothetical TEC specifically designed for this particular chip and hot spot has been explored.

The TE legs and gaps between the elements have been reduced to help decrease the dimensions of the TEC and the overall TEC/mini-contact covered area on top of the chip. A 6x6 array of 150µm x 150µm x 40µm TE legs with 50µm gaps was used in order to increase the $Bi_2Te_3$ coverage for the TEC to 56.25%. Also, due to the smaller TE legs, the ceramic substrates can be reduced to 1200µm x 1200µm x 380µm (the 380µm thickness remains the same), which results in a mini-contact/TEC coverage area of only 4.43% above the top of the chip. The optimized mini-contact dimensions and TEC leg length were found to be 400µm x 400µm and 40µm, respectively. This configuration results in a maximum hot spot cooling value of 13.3K.

The resulting temperature profile for this proposed TEC is shown below in figure 3.22. While it is clear that due to the geometric changes, operation of the TEC can provide substantial cooling, the re-designed mini-contact TEC still fails to provide better cooling than having no TEC/mini-contact present.

This is due, in part, to the geometry and low power dissipation of the chip. The hot spot dissipation is nearly 20% of the chip heat generation and is relatively large in relation to the rest of the chip (1mm x 1mm compared to 5.7mm x 5.7mm). Also, the chip is relatively thick (150µm) in relation to its lateral dimensions, which results in much of the hot spot heat flux diffusing through the rest of the chip, raising the overall chip bottom temperature by 10K, and not causing a drastic temperature gradient at the hot

spot. The mini-contact is perhaps best suited for cooling more aggressive hot spots – smaller in area and higher in flux – than what has been attempted here.

Nevertheless, there is still a considerably large temperature reduction that occurs when implementing the mini-contact enhanced conventional TEC for hot spot cooling. This measurable improvement serves to validate the basic mini-contact TEC methodology and provides a basis for later re-design and optimization for thermal packaging configurations more conducive to this thermal management approach.

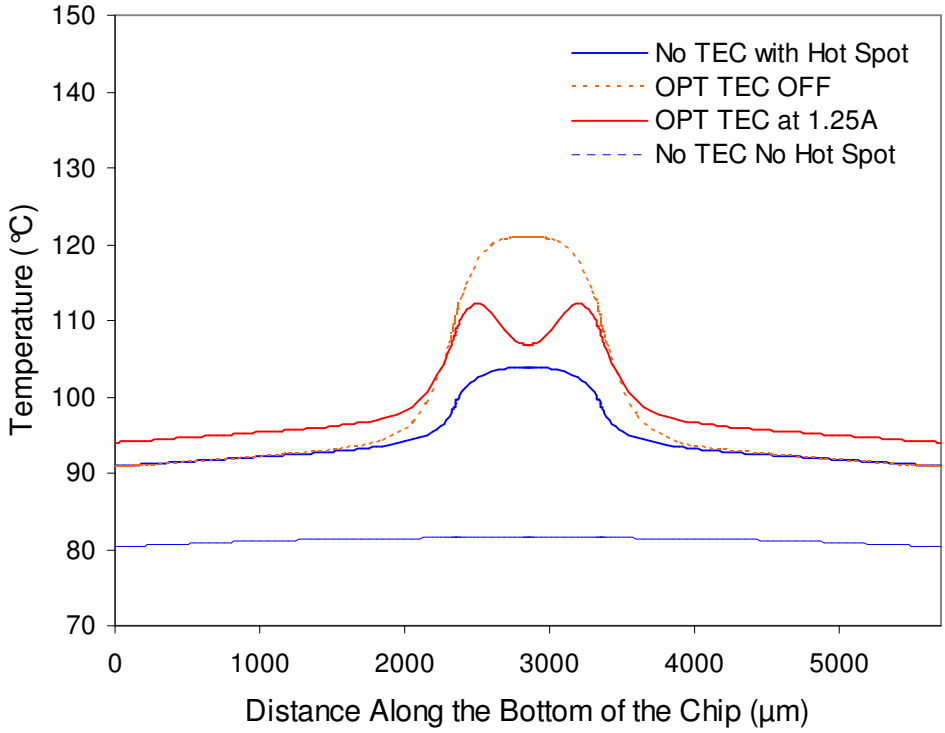



**Figure 3.22: Optimum 40µm TEC leg length with optimum 400µm x 400µm mini-contact TE legs have lateral dimensions of 150µm x 150µm with 50µm gaps. 1.25A produces a maximum cooling value of 13.3K**

### 3.3.5 Impact of the TIM2 layer on hot spot temperature

Additional ANSYS™ simulations were performed to more accurately model the hot spot and to further refine the Taiwanese TEC chip package with no TEC/mini-contact

present. A TIM2 layer was inserted between the Si chip and the heat spreader; in the previous case only a thermal contact resistance of $3.3x10^{-7}m^2K/W$ was present at this interface. A TIM2 layer at this interface relieves thermal stresses caused by the hot spot and high heat flux of the chip and is a more realistic representation of an actual packaging configuration. The presence of a TIM2 layer between the chip and the spreader increases the thermal resistance of the heat flow path that is parallel to the TEC/mini-contact. Therefore, there is less of a thermal "penalty" to be paid for the insertion of the TEC/mini-contact. The resulting hot spot in the new configuration is 12.2K hotter and consequently, the simulations of the optimized TEC show a "real" improvement when the TEC is activated, not just a cool-down.

Figure 3.23 shows the temperature profile of the Taiwanese 250µm and 500µm leg TECs compared to the newly modeled chip package with no TEC/mini-contact present. The new TIM2 layer above the chip in the configuration with no mini-contact/TEC present is 175µm thick and has a thermal conductivity of 30W/mK. This is the same thickness and thermal conductivity as the TIM1 layer between the heat spreader and the heat sink. This type of TIM depicts a solder interface with thermal contact resistance factored into the effective thermal conductivity of 30W/mK. Both 250µm and 500µm leg TECs still do not create an advantage compared to the case with no TEC/mini-contact present; however, the situation has greatly improved compared to the previous case with a thermal contact resistance layer compared to a TIM2 layer. The TEC must still be further optimized or perhaps utilized in a different package configuration.

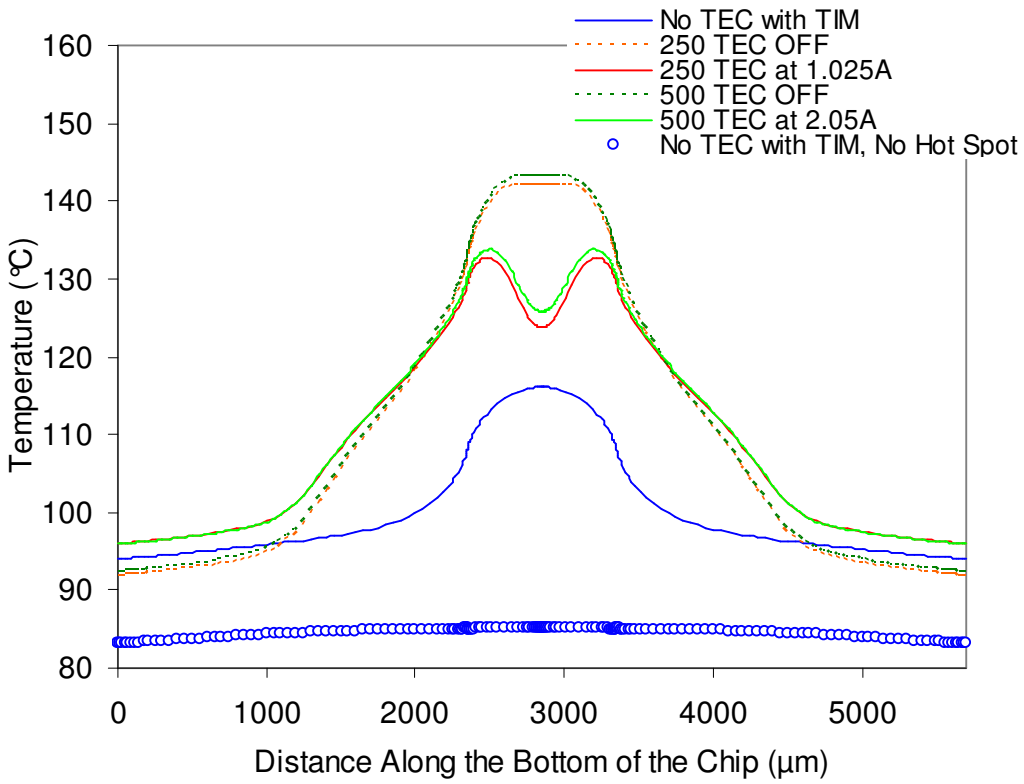



**Figure 3.23: Original Taiwanese TEC temperature profiles with new hot spot temperature profile**

In figure 3.24, the optimized 40µm leg TEC with 400µm x 400µm mini-contact is compared to the case with no TEC/mini-contact present that contains the new TIM2 layer between the Si chip and heat spreader. The optimized TEC now produces about 9.3K of cooling over the case with no mini-contact/TEC present. This is a significant improvement compared to the previous configuration with a thermal contact resistance layer instead of a TIM2 layer between the chip and heat spreader.

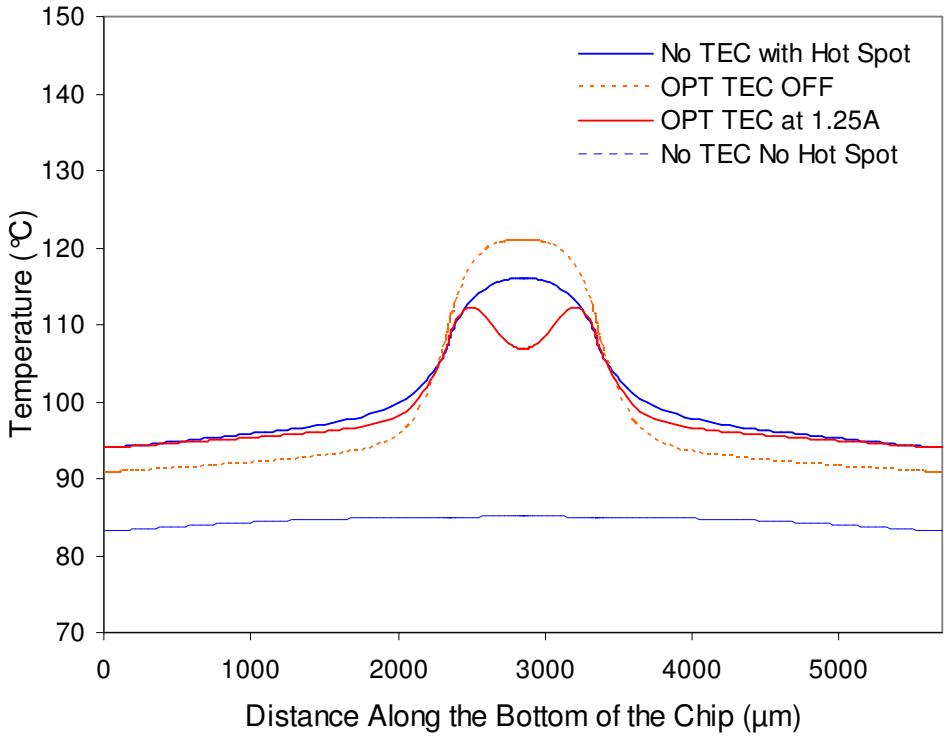



**Figure 3.24: TEC with optimized leg length and mini-contact with new hot spot temperature profile**

### 3.3.6 Decreased Lateral Heat Spreader Gap in TFTEC Package

As shown by the temperature profile in figure 3.16, for the Taiwanese configurations studied, the presence of the TFTEC and mini-contact within the chip package does not offer a reduction in hot spot temperature relative to a more conventional, conduction-only cooling approach. Additional ANSYS™ simulations were also performed in an attempt to determine the conditions under which the TFTEC would produce a more favorable temperature profile on the bottom of the Si chip.

The lateral gap between the mini-contact and Cu heat spreader was decreased from its original value of 500µm to 100µm. A greater machining tolerance is needed to accommodate for a smaller heat spreader gap. This change decreased the thermal

resistance caused by the air gap above the Si chip and greatly improved the temperature profile on the bottom of the chip, as shown in figure 3.25. When the TFTEC is operating at its optimum current, it produces a slight 1K of cooling advantage over the package configuration with no TFTEC/mini-contact present. Further optimization of the TEC, and possibly the package geometry or hot spot characteristics, is needed to identify the configuration best suited to TFTEC cooling.

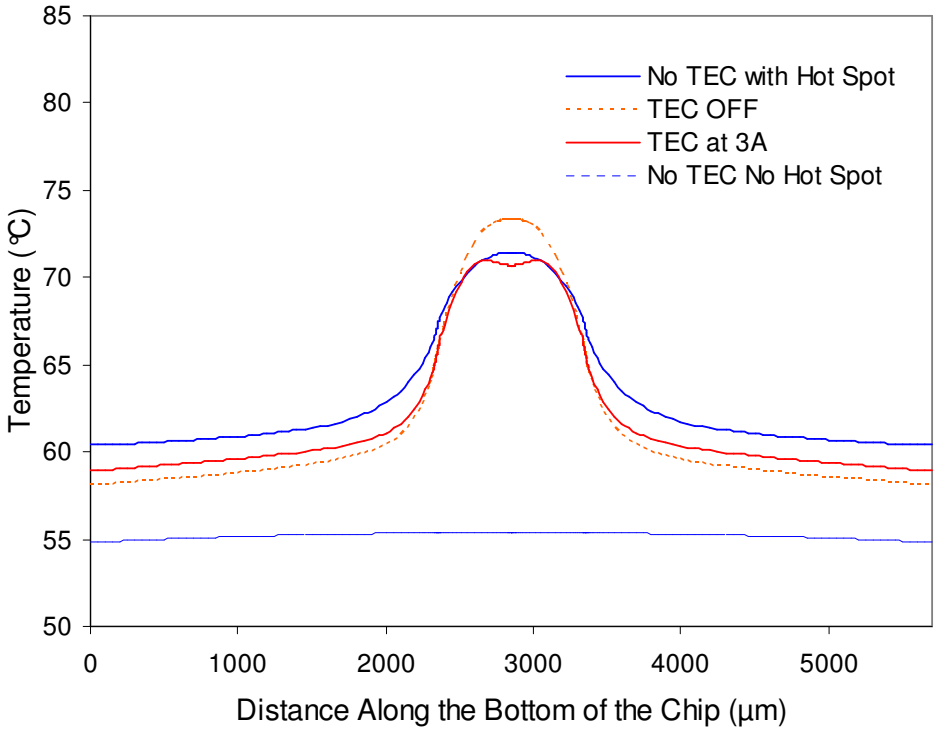



**Figure 3.25: Temperature Profile for TFTEC with a 100µm lateral heat spreader gap. TFTEC is operating at its optimum current of 3A with an optimum mini-contact size of 300µm x 300µm.**

### 3.3.7 Additional Simulations for the Taiwanese 250µm and 500µm TECs

Some additional ANSYS™ simulations were performed at the Taiwanese national lab to explore various package operating conditions such as no applied background heat flux on the chip and a chip thickness reduction from150µm to 25µm. Figures 3.26 and 3.27 display the temperature profiles with no background heat flux on the bottom of the

Si chip for the Taiwanese designed TEC and optimized TEC packages, respectively. When there is only a hot spot acting on the bottom of the chip, there is somewhat of an improvement in the temperature profiles but the Taiwanese 250µm and 500µm TECs are still unable to show an improvement when operating at their optimum currents compared to the case with no TEC/mini-contact present.

The optimized TEC, however, shows a significant improvement over the case with no TEC/mini-contact present in figure 3.27. Although it only produces 7.2K of cooling over the case with no mini-contact/TEC present, as compared to 9.3K in figure 3.24 where the chip has a background heat flux. The drop in cooling is due to the much lower power dissipation and lower temperature of the chip (3W hot spot compared to the 16W with active hot spot and background flux).

Additionally, a 25µm thick Si chip was simulated. The mini-contact size for this much thinner chip was optimized to 150µm x 150µm, shown in figure 3.28. Compared to the packages with the 150µm thick Si chip, this case showed drastic cooling of about 57K at the center of the hot spot. Despite this, the temperature profile, given in figure 3.29, still shows elevated temperatures on the bottom (active side) of the chip compared to the case with no TEC/mini-contact present. However, in this 25µm thick Si chip configuration, the average temperature on the chip when the Taiwanese TECs are operating at optimum current is about 122.2°C, approximately equal to the average chip temperature when the TECs are turned off. There is, thus, no net cooling achieved by use of the Taiwanese TEC in this configuration.

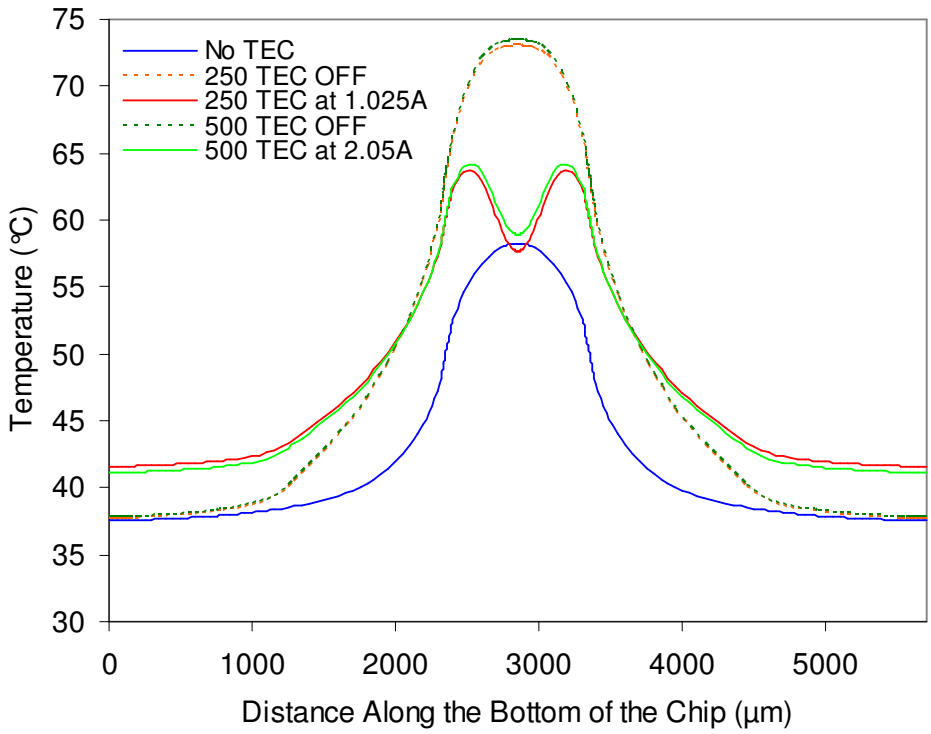



**Figure 3.26: Temperature Profiles for Taiwanese 250µm and 500µm Leg TEC with No Background Heat Flux on Chip. Each respective TEC is operating at its optimum current and the optimum mini-contact size of 300µm x 300µm**

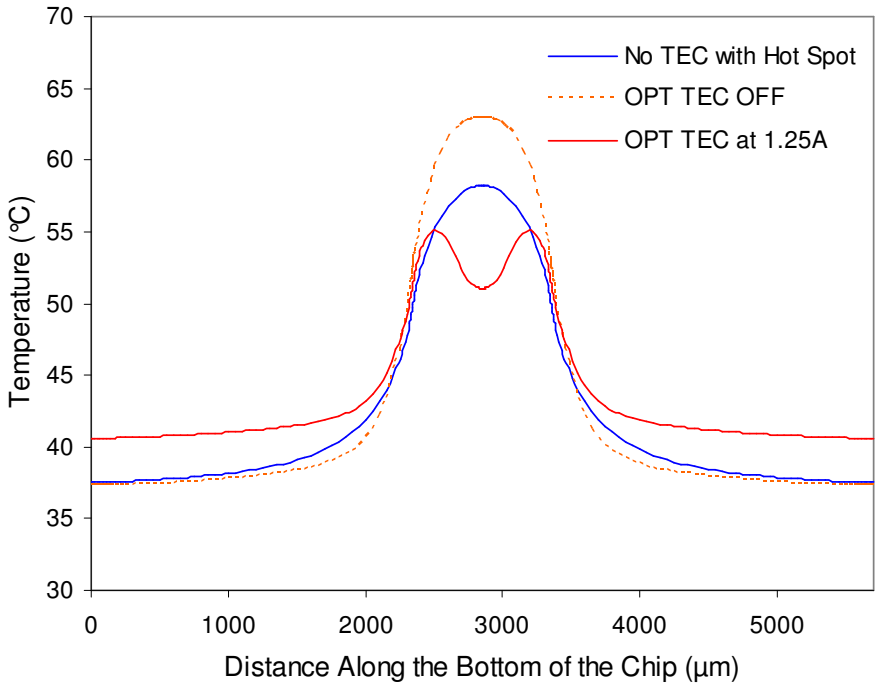



**Figure 3.27: Temperature Profiles for the Optimized TEC with No Background Heat Flux on Chip. Optimum 40µm TEC leg length with optimum 400µm x 400µm mini-contact**

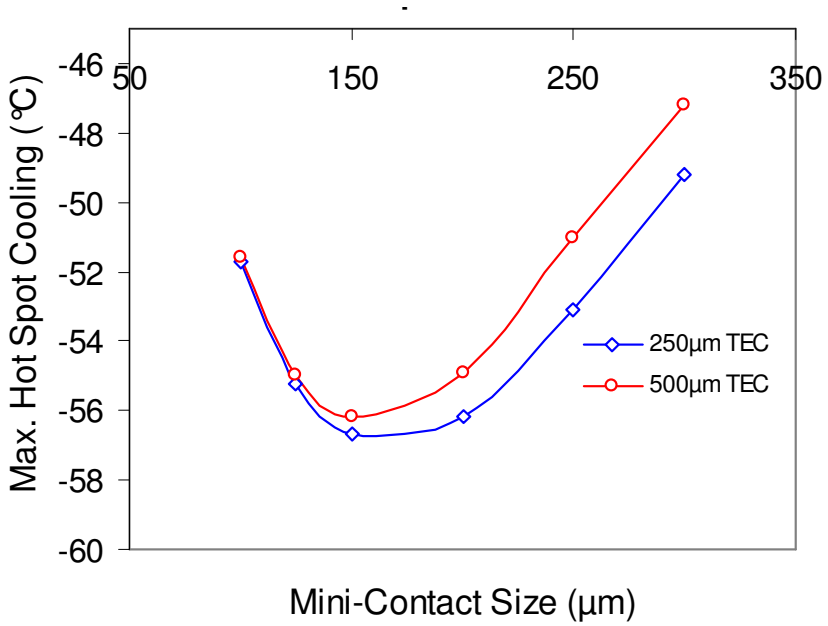



**Figure 3.28: 25µm Thick Si Chip: Optimum Mini-Contact Size for 250µm and 500µm Taiwanese TECs**

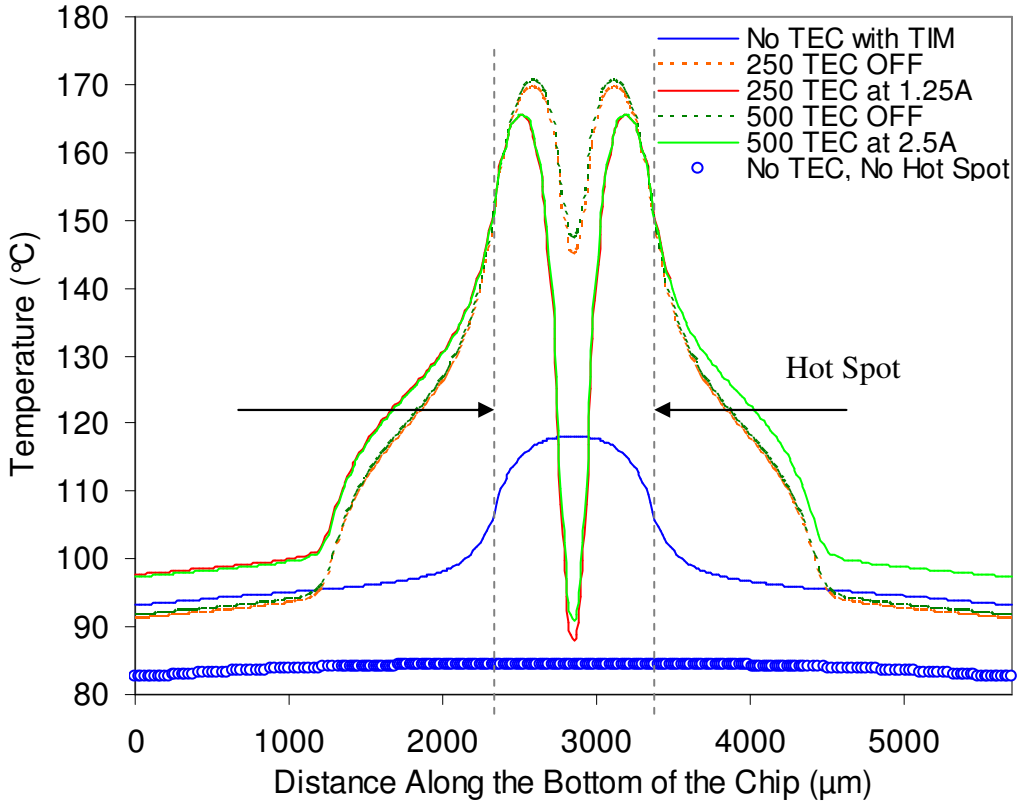



**Figure 3.29: Temperature profile along the bottom of a 25µm Thick Si Chip for the 250µm and 500µm Taiwanese TECs operating at optimum current and the optimum mini-contact size of 150µm x 150µm**

### 3.3.8 Additional simulations for the TFTEC

Additional ANSYS simulations were also performed for the commercial TFTEC with various hot spot configurations. Figure 3.30 displays the temperature profile on the bottom of the Si chip for the TFTEC, operating at its optimum mini-contact size and current, with a 1mm x 1mm hotspot producing 1W (compared to the previously simulated cases with a 3W hot spot). Since the hot spot heat flux is now 100 W/cm$^2$ and the background heat flux is still 40W/cm$^2$, the temperature rise from the hot spot is less pronounced. Figure 3.31 shows a similar case but with no background heat flux on a chip containing a 1W hot spot. Finally, in figure 3.32, the hot spot size was reduced from 1mm x 1mm to 0.5mm x 0.5mm. The temperature profiles for all three of these cases do not show an improvement from a package with an integrated TFTEC operating at its optimum mini-contact size and current compared to the conduction only case without a TEC/mini-contact preset.

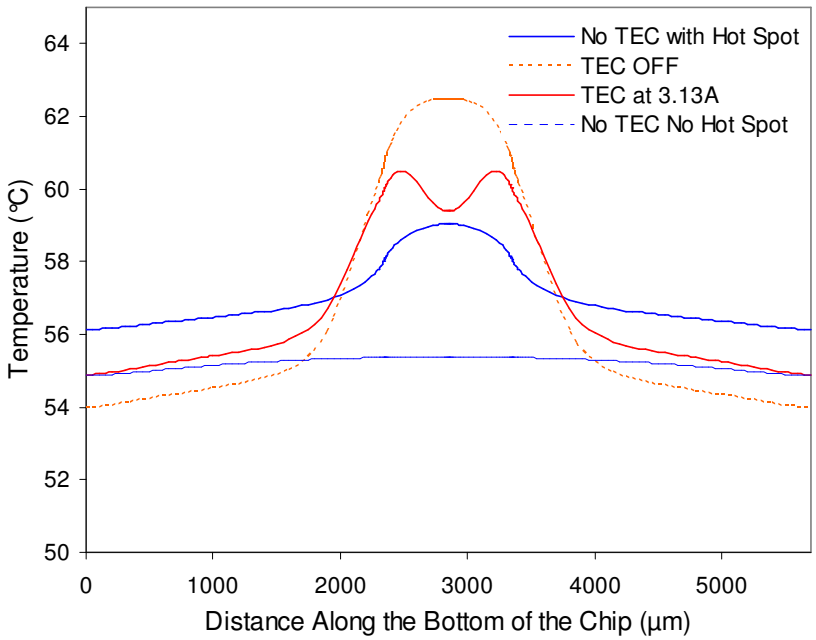



**Figure 3.30: Temperature Profile for TFTEC: Hot Spot has a heat flux of 100W/cm$^2$. TFTEC is operating @ optimum current of 3.13A and with 400x400µm$^2$ mini-contact. Hot spot heat flux has been reduced from 300W/cm$^2$ to 100W/cm$^2$**

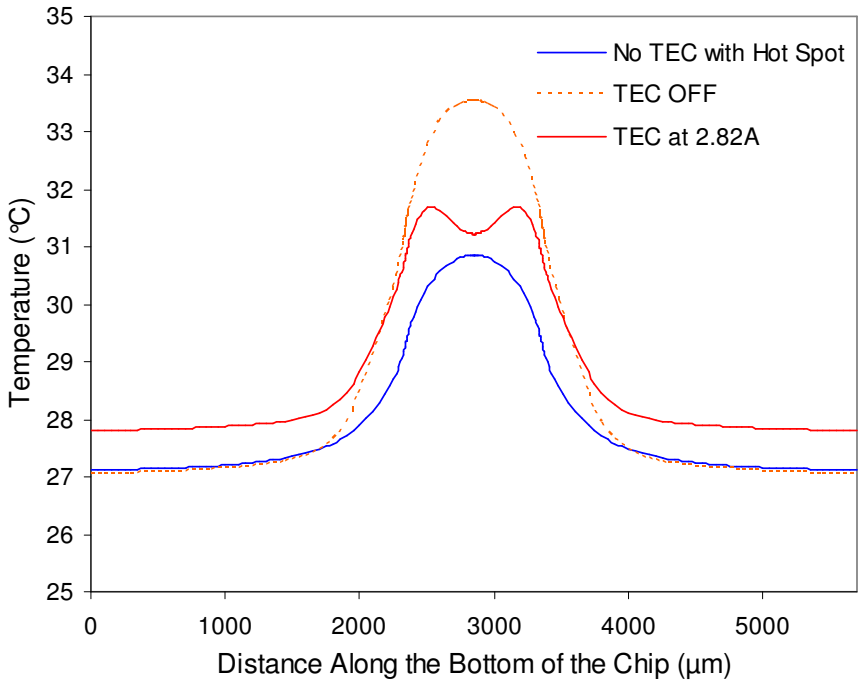



**Figure 3.31: Temperature Profile for TFTEC: No Background Heat Flux and Hot Spot has a heat flux has been reduced from 300W/cm$^2$ to 100W/cm$^2$. TFTEC is operating @ optimum current of 2.82A with 400x400µm$^2$ mini-contact**

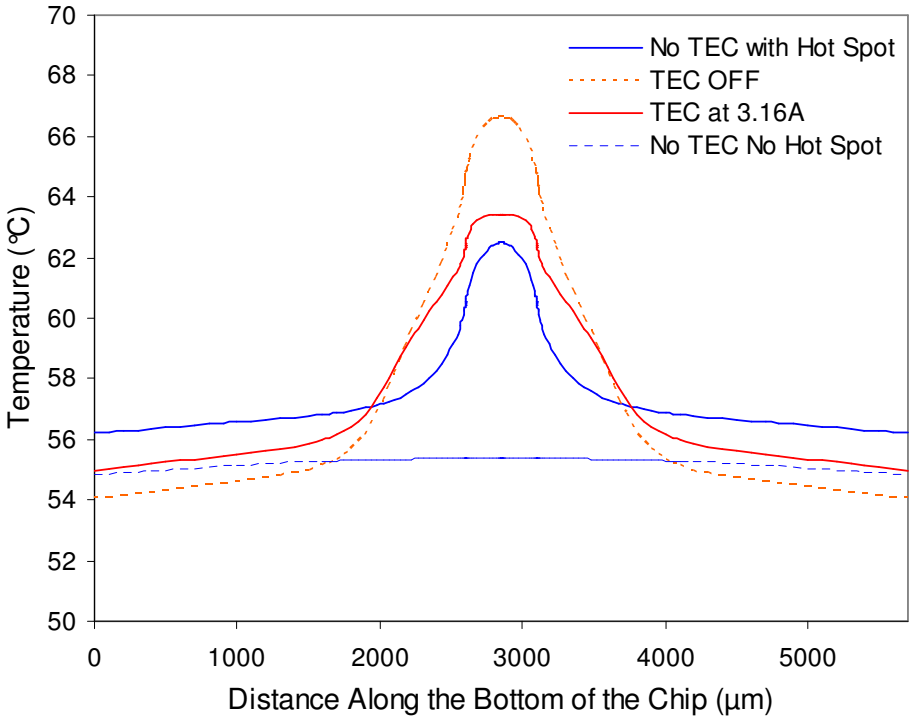



**Figure 3.32: Temperature Profile for TFTEC: Hot Spot is reduced to 500µm x 500µm. TFTEC is operating @ optimum current of 3.16A with 400x400µm$^2$ mini-contact. Hot spot flux remains 300W/cm$^2$**

### 3.4 Conclusion

This chapter summarizes the results obtained in simulating the performance of miniature mini-contact TEC's used for the thermal management of a Taiwanese-specified on-chip "hot spot." Two Taiwanese TEC designs – with 250μm and 500μm TE leg height, respectively - and a commercial TFTEC – with 20μm TE leg height - were considered. ANSYS™ simulations of optimized mini-contact configurations revealed possible hot spot cooling of 19K and 18K for the 250μm and 500μm TECs, respectively, and a hot spot temperature reduction of nearly 4K for the TFTEC device. It would thus appear that operation of mini-contact TEC's can provide significant cooling of on-chip hot spots for the Taiwanese designs studied.

However, for these configurations, the insertion of any of the proposed mini-contact TEC's was found to raise the chip temperature, due to the additional thermal resistance created by the cooling device. Consequently, the mini-contact TEC's were unable to lower the chip temperature below that achieved in a package containing no mini-contact TEC. Nevertheless, the large temperature differences predicted to occur when operating the TEC devices facilitate experimental validation of the mini-contact TEC methodology and provide a basis for later re-design and optimization for thermal packaging configurations more conducive to this thermal management approach.

# Chapter 4

# 4. Effect of Thermal Contact Resistance on Optimum Mini-Contact TEC Cooling of On-Chip Hot Spots

## 4.1 Introduction

Non-uniform microprocessor power dissipation can result in localized high heat flux "hot spots" that may reduce chip performance in addition to degrading chip reliability [e.g. 44-46]. Among the several techniques proposed for mitigating the negative effects of "hot spots" [47-52], miniaturized thermoelectric coolers, or μTECs, appear to offer a most promising alternative [28,29]. Recently, a thin film TEC was shown to provide a 15K temperature reduction of a 0.16mm$^2$ hot spot, producing 1250W/cm$^2$ [10].

Although thermoelectric devices require input power and generate Joule heating, miniaturized TECs can be used to cool localized IC hot spots and create more uniform chip temperatures without the penalty of significantly increasing the average chip temperature. Other TEC advantages include their solid state design, no moving parts, high reliability, and compact structure.

In the present study, a package-level finite element model is created to investigate on-chip hot spot temperature reduction using a miniaturized conventional $Bi_2Te_3$ TEC [53], enhanced with a copper mini-contact pad. It is observed that to achieve the greatest temperature reduction at the hot spot, the mini-contact size and thermoelectric leg height must be optimized. Attention is focused on the effects of parasitic thermal contact resistance, that occurs at the Si chip, mini-contact, and TEC interfaces.

## 4.2 Simulation Study of Mini-Contact Enhanced TEC for Hot Spot Cooling

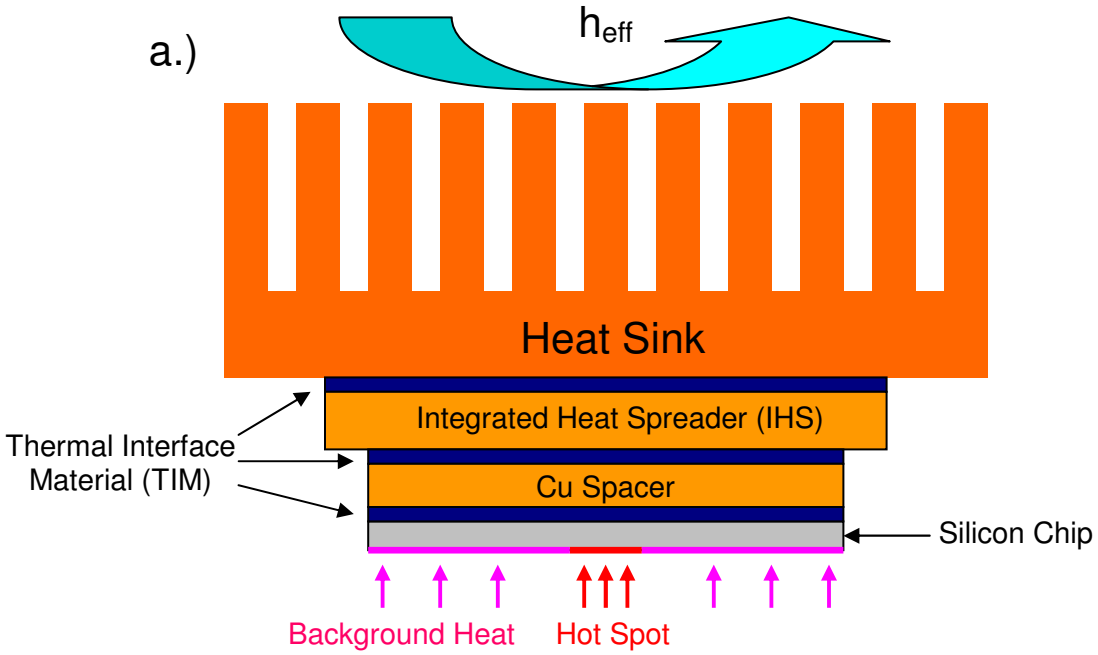
### 4.2.1 Description of Numerical Model

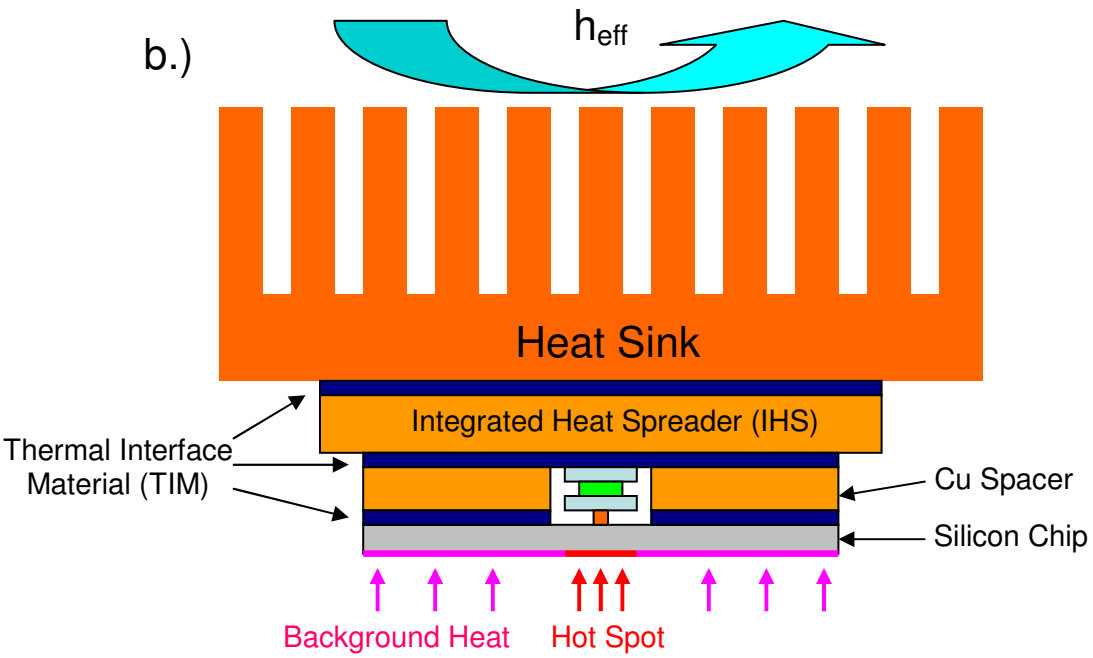
Commercially available finite element software, ANSYS™, was used to construct the three dimensional (3D) numerical thermal model of the TEC/mini-contact cooled IC package, described below in figure 4.1. Thermal solid element - Solid70 - was used and the total element count ranged from 100,000 to 200,000 elements for the quarter-model package. Extra attention was focused on the mesh within the silicon chip near the hot spot and at the individual thermoelectric (TE) legs within the TEC due to the larger temperature gradients that occur at these locations. The mesh sensitivity for this numerical model, given in figure 4.1c, shows that the temperature solution varies by only 0.1°C as the number of elements is tripled.

The model consists of an 11mm x 13mm silicon chip, TIM1 layer, TEC/mini-contact/spacer layer, TIM2 layer, copper heat spreader, TIM3 layer, and heat sink, in ascending order. For comparison, chip packages with and without an integrated mini-contact/TEC are shown in figures 4.1b and 4.1a, respectively. The Si chip includes a central 400µm x 400µm hot spot, producing a heat flux of 1250W/cm$^2$, and the heat generated by the active circuitry on the chip is modeled as a background heat flux of 40W/cm$^2$ on the periphery of the chip. The 150µm thick copper mini-contact is attached to the top of the Si chip and the TEC is attached to the top of the mini-contact. The TEC in this study is consistent with commercially available TECs and is comprised of top and bottom 250µm thick ceramic substrates, two solder/copper metallization layers, and a central 6x6 array of $Bi_2Te_3$ legs, each 20µm high. A thin copper spacer surrounds the TEC/mini-contact and thermal grease interfaces are used at TIM's 1, 2, and 3. The

geometric dimensions and material properties used in this study are displayed in table 4.1.

The heat sink was modeled as a block without fins to simplify model geometry, reduce total element count, and avoid lengthy solution times. An effective heat transfer coefficient of 730W/m$^2$K was applied to the top of the heat sink and the ambient temperature was assumed to be 25°C [28,29]. This relatively large value for $h_{eff}$ was used to compensate for the reduced area of the heat sink in the FE model. Additionally, thermal contact resistance was modeled at the Si chip/mini-contact, mini-contact/TEC, and TEC/TIM2 interfaces. As in previous studies of miniaturized TEC's, the three thermal contact resistance values chosen for this study were $1x10^{-7}$, $1x10^{-6}$, and $5x10^{-6}$ m$^2$K/W, representing a very clean (low thermal resistance) interface, a slightly degraded (increased thermal resistance) interface, and a moderately poor (higher thermal resistance) interface, respectively.





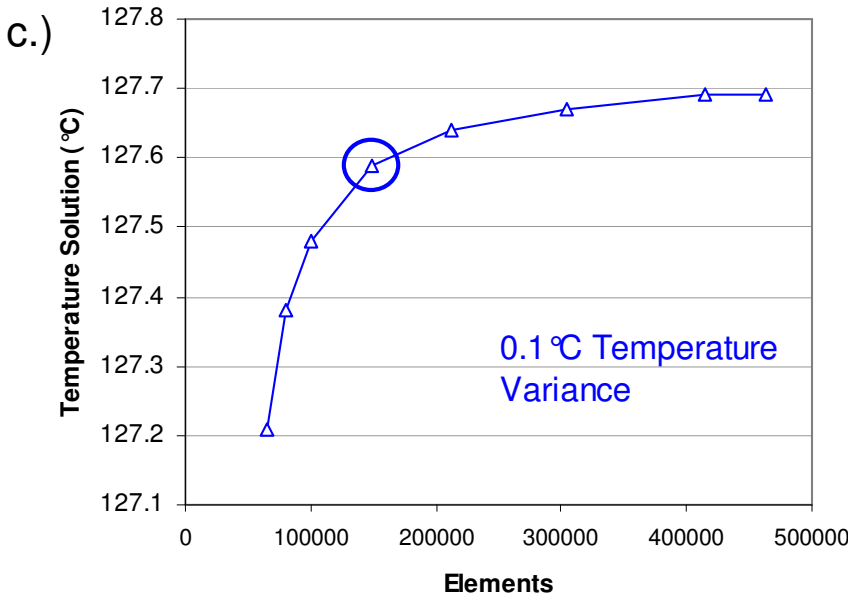




**Figure 4.1: Schematic of a typical package (a), schematic of package with a mini-contact enhanced TEC (b) (not drawn to scale), and ANSYS™ model mesh sensitivity (c)**

**Table 4.1: Package dimensions and material properties**

| | Geometry (l x w x h) | Material | k (W/mK) |
|---|---|---|---|
| **Heat Sink** | 50mm x 50mm x 5mm | Al | 180 |
| **TIM3** | 31mm x 31mm x 175µm | | 1.75*** |
| **HIS** | 31mm x 31mm x 1.5mm | Cu | 360 |
| **TIM2** | 11mm x 13mm x 50µm | | 1.75*** |
| **Spacer** | 11mm x 13mm* | Cu | 360 |
| **Top Ceramic** | 1.79mm x 1.56mm x 250µm | AlN | 180 |
| **Upper Solder/ Metallization Layer** | z = 40µm** | Cu/solder | 290 |
| **TE Legs (6x6 Array)** | 115µm x 90µm* | $Bi_2Te_3$ | 1 |
| **Lower Solder/ Metallization Layer** | z = 100µm** | Cu/solder | 290 |
| **Bottom Ceramic** | 0.99mm x 1.56mm x 250µm | AlN | 180 |
| **Mini-Contact Base** | 0.99mm x 1.56mm x 50µm | Cu | 360 |
| **Mini-Contact Tip** | z = 100µm* | Cu | 360 |
| **TIM1** | 11mm x 13mm x 50µm | | 1.75*** |
| **Chip** | 11mm x 13mm* | Si | **** |
| **Hot Spot** | 400µm x 400µm | | |

* = The z dimension varies
** = The lateral dimensions are equal to the TE legs dimensions
*** = Thermal conductivity for a thermal grease, consistent with value used in [10]
**** = Temperature dependent thermal conductivity

### 4.2.2 Modeling the TEC

The $Bi_2Te_3$ TEC was modeled separately from the rest of the chip package to characterize its thermal performance. The goal of this model was to facilitate use of numerical regression to determine plausible TEC material property values, capable of yielding a target thermal performance ($\Delta T \approx 50K$ @ $I \approx 1A$) achievable by existing TEC's. Once the material properties were determined, they were integrated into the TEC within the FE chip package model so that TEC/mini-contact hot spot cooling could be investigated. The modeled TEC featured a 6x6 array of 20µm high TE legs with the same lateral dimensions as described in table 4.1. A quarter model of the TEC is shown in figure 4.2.

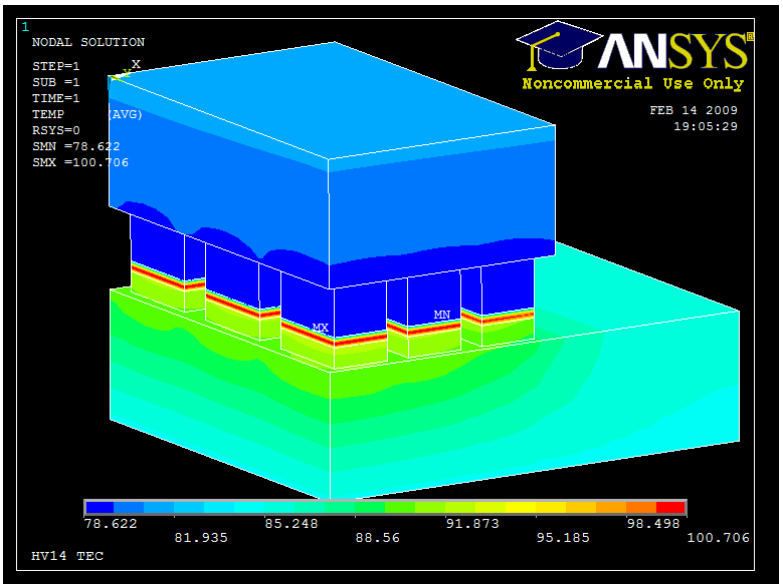



**Figure 4.2: Quarter model image of the TEC used in the numerical simulations operating at 1.1A**

The Seebeck coefficient of the $Bi_2Te_3$ was assumed to be 287μV/K, which is consistent with reported values for the same material at comparable temperatures and thicknesses [54]. The resistivity of the $Bi_2Te_3$ was assumed to be 88Ω-μm and the total electrical resistance of the device was 2.9Ω. The thermal conductivity of the $Bi_2Te_3$ was assumed to be 1W/mK. Also, an electrical contact resistance of $3.3x10^{-7}$Ω-cm$^2$ was assumed at the interfaces of each TE leg to represent the lower range of values for clean surfaces attached with an organic bonding material [29]. The bottom ceramic of the TEC, which is larger than the top (to accommodate the placement of copper traces that provide power to the device) was held at a stage temperature of 85°C. A heat flux of 110W/cm$^2$ was imposed on the top ceramic and the device was cycled through a range of applied current values. The heat flux boundary conditions, shown in equations (4.1) and (4.2), were applied to the hot and cold side, respectively, of each TE leg:

$$q''_{TE,\,hot} = (ST_hI + I^2R_e)/A_{TE} \qquad (4.1)$$

$$q''_{TE,\,cold} = (-ST_cI + I^2R_e)/A_{TE} \quad (4.2)$$

where S is the Seebeck coefficient, $T_h$ and $T_c$ are the absolute temperatures at the hot and cold TE leg interfaces, I is current, $R_e$ is the electrical contact resistance and $A_{TE}$ is the lateral area of the TE leg. Equation 4.1 relates to the Peltier heating that occurs at the hot side of the TEC and equation 4.2 relates to the Peltier cooling that occurs at the cold side of the TEC. The volumetric Joule heating associated with the electrical resistance of the TE legs, and proportional to the square of the input current, was modeled as a thermal body force on each TE leg. The average cooling at the top ceramic of the TEC, as a function of current input, is shown below in figure 4.3, where the parabolic dependence of cooling on current – reflecting the competition between Peltier cooling and parasitic Joule heating – is in clear evidence. The TEC achieved 51K of cooling at 1.1 Amps and transferred 1.7W of heat from the cold side to the hot side. It is important to note that the orientation of the TEC used in the package simulations is flipped upside down such that the cold side is facing downward.

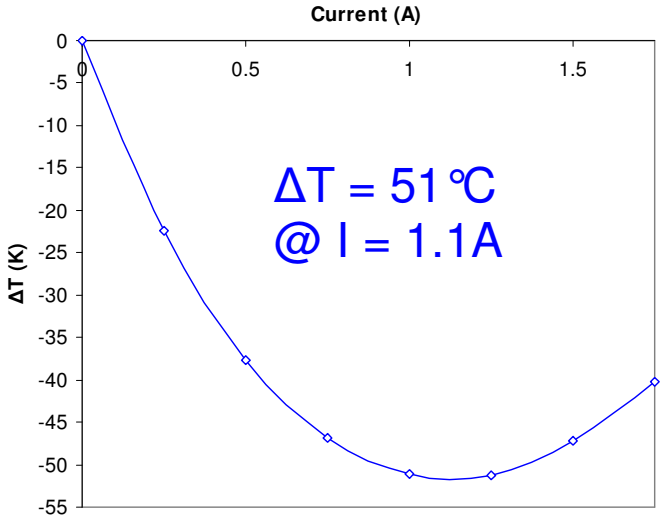



**Figure 4.3: Temperature reduction at the cold side of the TEC as a function of input current (only the TEC is modeled)**

### 4.3 Simulation Results and Discussions

#### 4.3.1 Mini-Contact TEC Temperature Profiles

The temperature profiles on the bottom (active) surface of a chip cooled by a mini-contact assisted miniature TEC are shown in figures 4.4 and 4.5 for the 100µm and 500µm thick Si chips, respectively. The optimum mini-contact size is used, in each figure, for three values of thermal contact resistance at the mini-contact-TEC interfaces.

For the 100µm chip in figure 4.4, it is observed that when the TEC/mini-contact is present within the chip package, but turned off, there is a passive hot spot cooling effect that occurs, compared to the case with no TEC/mini-contact present within the spacer layer. This effect only occurs at thermal contact resistance values of $1x10^{-7}$ and $1x10^{-6}$ $m^2K/W$ and is due to the low thermal conductivity of the thermal grease between the Si chip and Cu spacer, which is replaced by the presence of the higher conductivity mini-contact and TEC. When the thermal contact resistance becomes $5x10^{-6}$ $m^2K/W$, then the presence of the mini-contact/TEC operating at 0A results in a 3.7K increase at the hot spot compared to the temperature when only a copper spacer is present. The hot spot temperature reductions achieved (at the optimum current and mini-contact size for each thermal contact resistance value), compared to the state when the TEC is turned off, are 13.5K, 12.3K, and 9.3K at $1x10^{-7}$, $1x10^{-6}$, and $5x10^{-6}$ $m^2K/W$, respectively. Hot spot cooling capacity intuitively decreases with increasing thermal contact resistance.

The temperature profile for the 500µm chip in figure 4.5 shows the effects of increased chip thickness. Most notably, hot spot cooling has greatly decreased and the TEC/mini-contact does not have a passive cooling advantage at any of the thermal contact resistance values. Even at low thermal contact resistance values, there is only

modest hot spot cooling, approximately 1K, that occurs relative to the case with no TEC/mini-contact present. Additionally, it was observed that the low input power to the TEC does not result in noticeably elevated temperatures at the periphery of the chip, for either chip thickness.

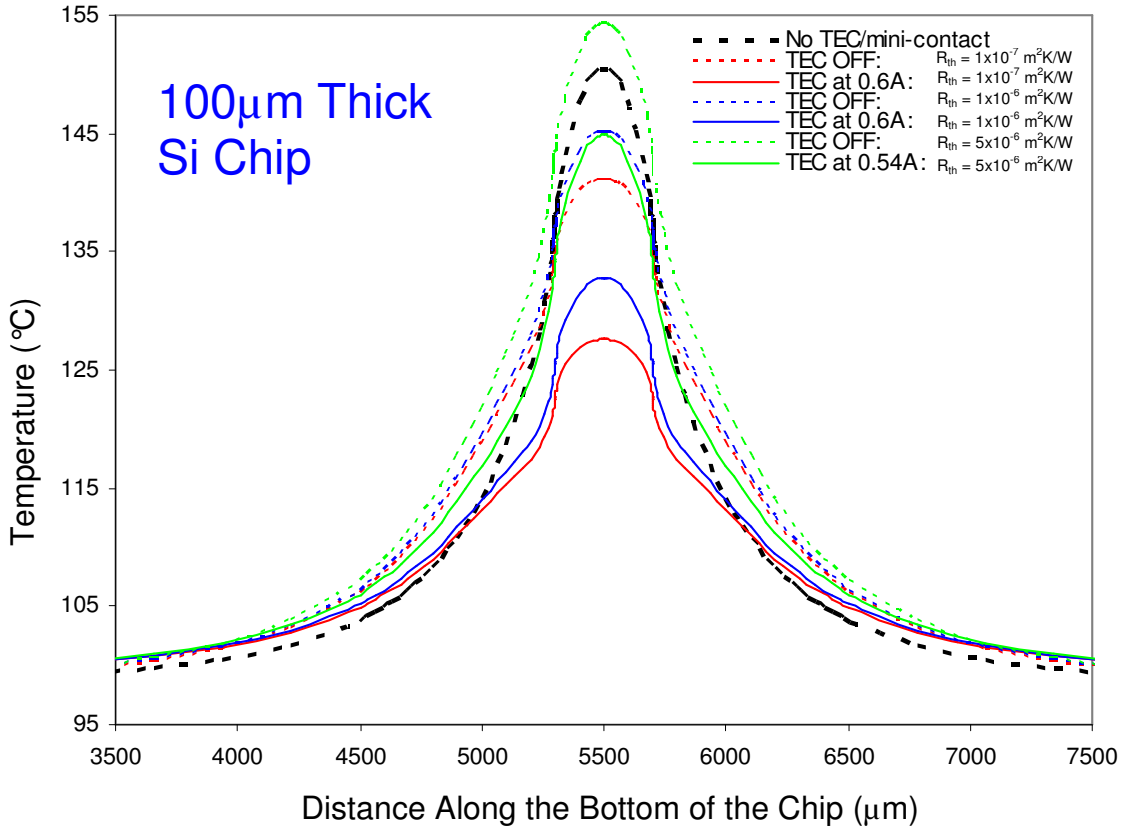



**Figure 4.4: Temperature distribution on the bottom (active) surface of the chip at various thermal contact resistances; zoomed in on hot spot region. Mini-contact size is optimized (refer to figure 14), TE leg length = 20µm**

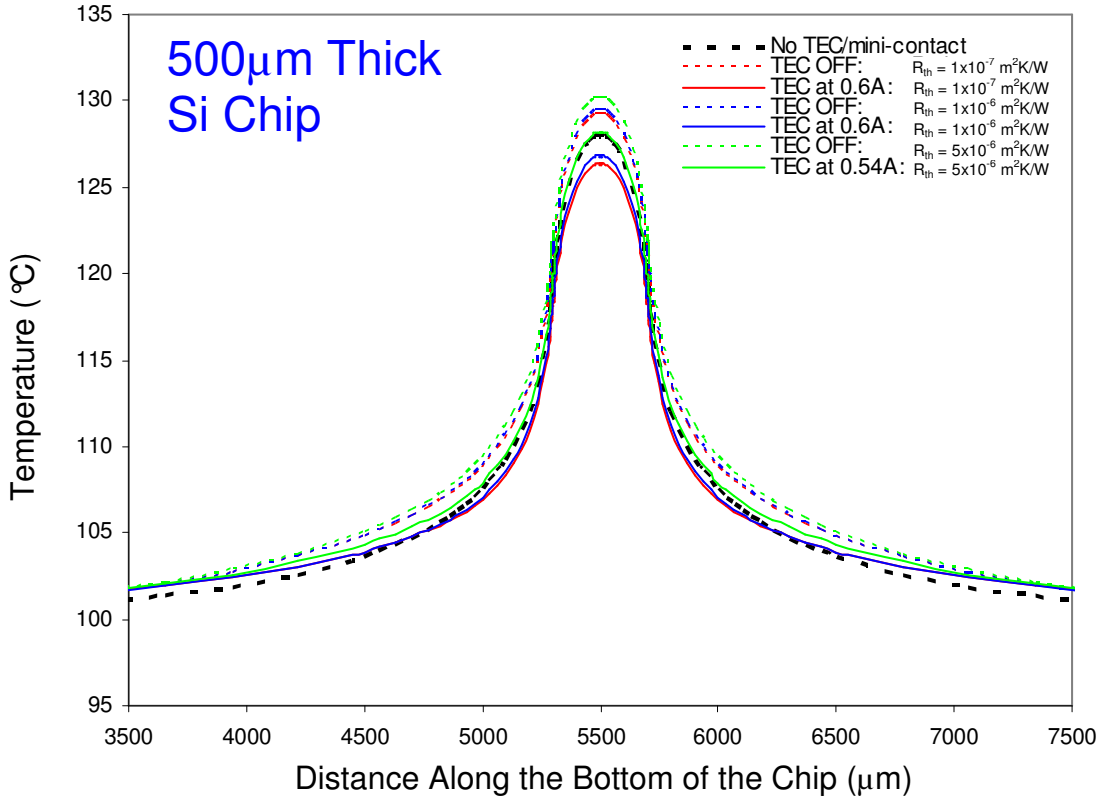



**Figure 4.5: Temperature distribution on the bottom (active) surface of the chip at various thermal contact resistances; zoomed in on hot spot region. Mini-contact size is optimized (refer to figure 15), TE leg height = 20µm**

Figures 4.6a and 4.6b show a sample solution for the complete temperature field of a thermally-optimized mini-contact assisted µTEC chip package operating at its optimum current of 0.38A and with an imposed thermal contact resistance of 1x10$^{-7}$m$^2$K/W at the mini-contact/TEC and mini-contact/Si die interfaces.

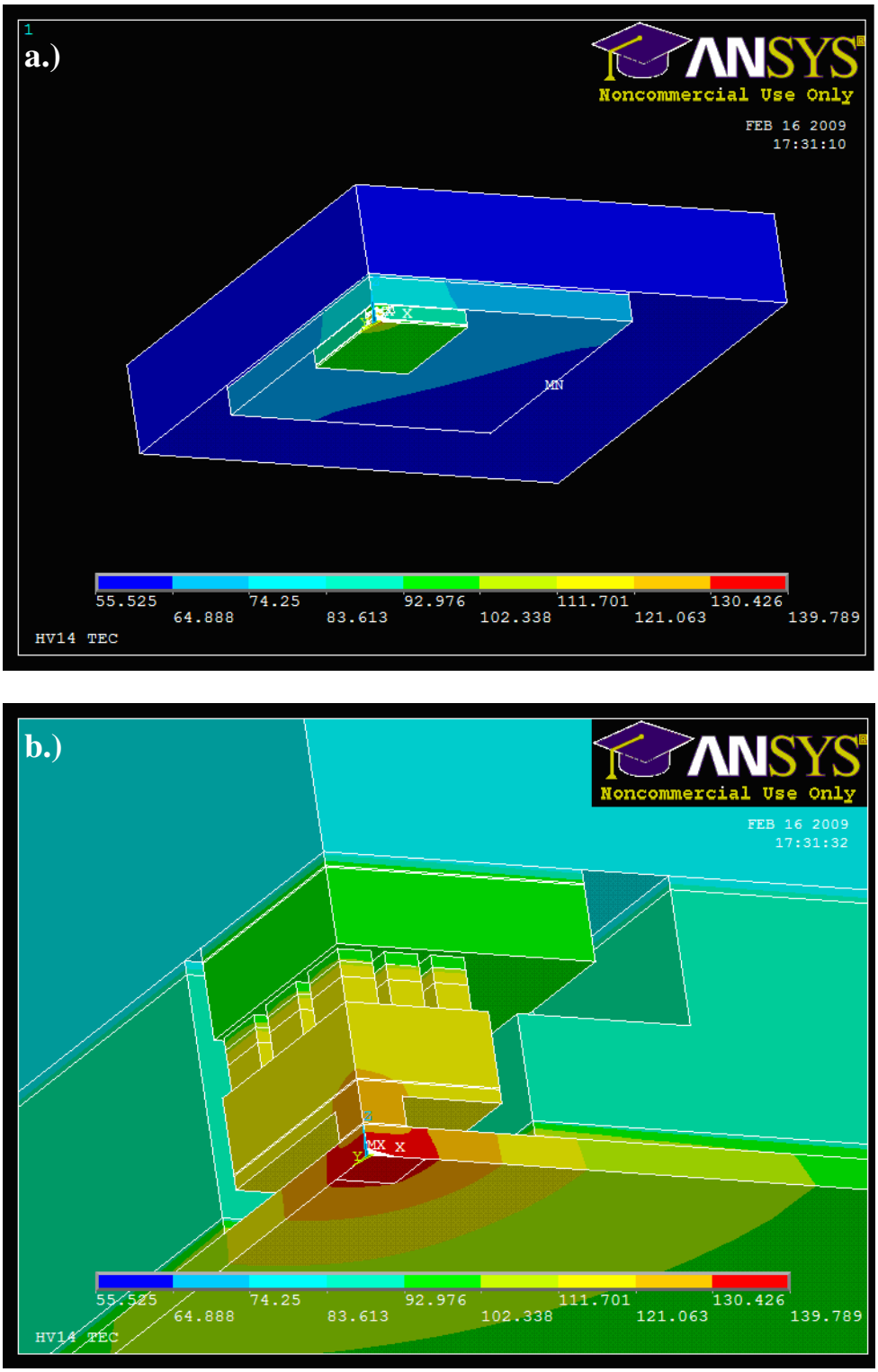



**Figure 4.6: The chip package (a) and zoomed in on mini-contact/TEC (b) for the optimized TE leg height and mini-contact size at $R_{th}$ = 1x10$^{-7}$ m$^2$K/W. (TEC current = 0.38A, TE leg height = 50µm, mini-contact = 300x300µm$^2$, Si chip thickness = 100µm**

### 4.3.2 Effect of Input Power on TEC

Figure 4.7 shows the predicted hot spot temperature reductions with varying input current to the TEC for the package shown in figure 4.1b and described in table 4.1, with a silicon die thickness of 100 μm. The TE leg height is assumed to be 20μm and the thermal contact resistance is assumed to be $1x10^{-7}$ $m^2K/W$, a nearly-ideal interface. Various mini-contact tip sizes are examined.

An initial cool down at the hot spot is observed that is related linearly to current and the Seebeck coefficient of the $Bi_2Te_3$. With increasing current, the parasitic Joule heating, associated with the electrical resistance of the $Bi_2Te_3$, begins to dominate due to the quadratic dependence on current. These two competing effects result in an optimum current for hot spot cooling of approximately 0.6 A, in the configuration considered herein, which appears to be invariant with the mini-contact size. It is obvious, however, that the actual hot spot temperature reduction does vary with the mini-contact size and reaches a remarkable 13.5K for the $1.2kW/cm^2$, 0.4mmx0.4mm hot spot for an advanced μTEC, with 20μm thick TE legs, as examined in this study.

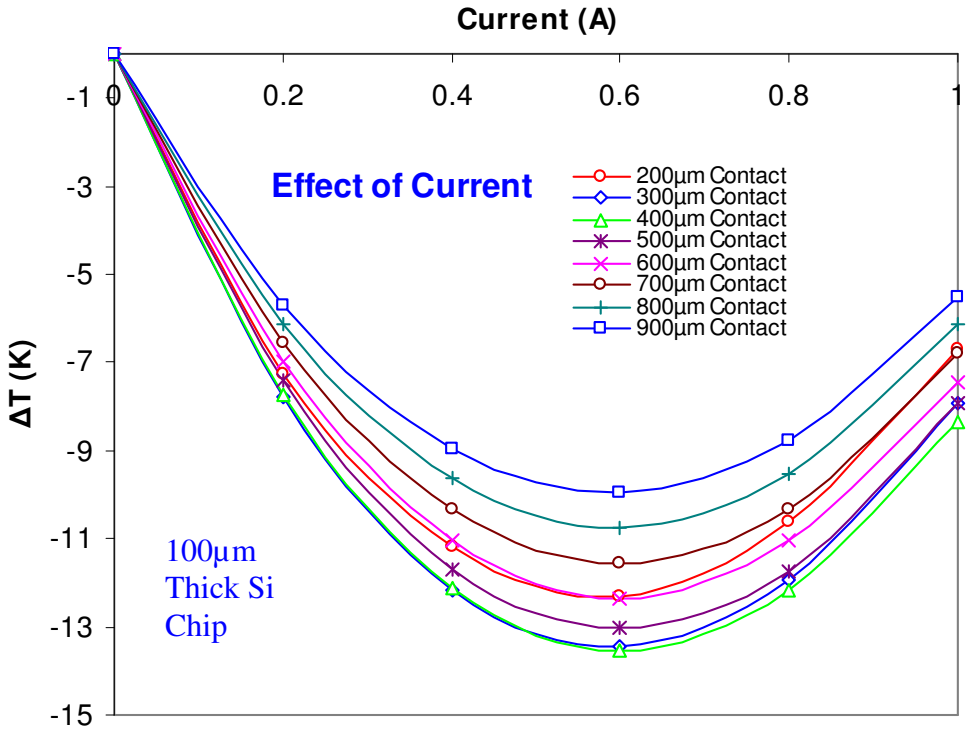



**Figure 4.7: Effect of TEC input current on hot spot temperatures for different mini-contact tip sizes. TE leg height = 20µm, $R_{th}$ = 1x10$^{-7}$m$^2$K/W**

### 4.3.3 Effect of Thermal Contact Resistance

The thermal contact resistance at the various package interfaces plays a key role in determining the optimum package dimensions as well as the thermal performance of the mini-contact enhanced TEC cooling approach. It is largely determined by the roughness and cleanliness of the surfaces, the material preparation, and the overall robustness of the thermal package assembly. Previous studies have shown if thermal contact resistance values reach 1x10$^{-5}$ m$^2$K/W, the mini-contact TEC begins to lose its viability as a hot spot cooling solution [28]. Therefore, thermal contact resistance is one of the driving factors in the design, assembly, and implementation of this thermal management approach.

#### 4.3.3.1 Combined with Effect of Mini-Contact Size

As noted in figure 4.7, the effectiveness of hot spot cooling varies with the dimensions of the mini-contact tip that is bonded directly to the backside of the chip, above the hot spot. The mini-contact concentrates the cooling power of the TEC and if the mini-contact tip size is too large, the TEC cools more of the surrounding silicon and not enough of the hot spot. Alternatively, if the tip size is too small, the TEC does not remove enough heat from the hot spot. Therefore, there exists an optimum mini-contact tip size, or "effective cooler" size above the hot spot. This effect is also observed in section 2.4.2.3 of chapter 2. The strong dependence of hot spot cool-down on the mini-contact size is also clearly visible in figure 4.8, where to the locus associated with the figure 4.7 results, for a nearly ideal interface, are added loci for two higher resistances at the TEC/mini-contact interface, while maintaining the other interfaces at fixed values of $1x10^{-7}$, $1x10^{-6}$, and $5x10^{-6}$ $m^2K/W$, respectively. For the TEC-mini-contact interfaces spanning values from $1x10^{-7}$ $m^2K/W$ to $1x10^{-5}$ $m^2K/W$, the hot spot temperature reduction is seen to vary parabolically with the contact size, achieving the minimum temperature at between 400μm and 700μm side length. Beyond the expected deterioration in the maximum hot spot cooling with increasing interface resistance, the poorer thermal interfaces result in larger, optimal mini-contacts. Thus, for the progressively higher interface resistances, the optimum hot spot cool-downs of 13.5K, 12.3K, and 9.3K were observed for mini-contact sizes of $400x400\mu m^2$, $500x500\mu m^2$, and $700x700\mu m^2$, respectively, for a 100μm thick silicon chip. It is important to note that each of the optimum mini-contact cooling values may occur at different optimum current values.

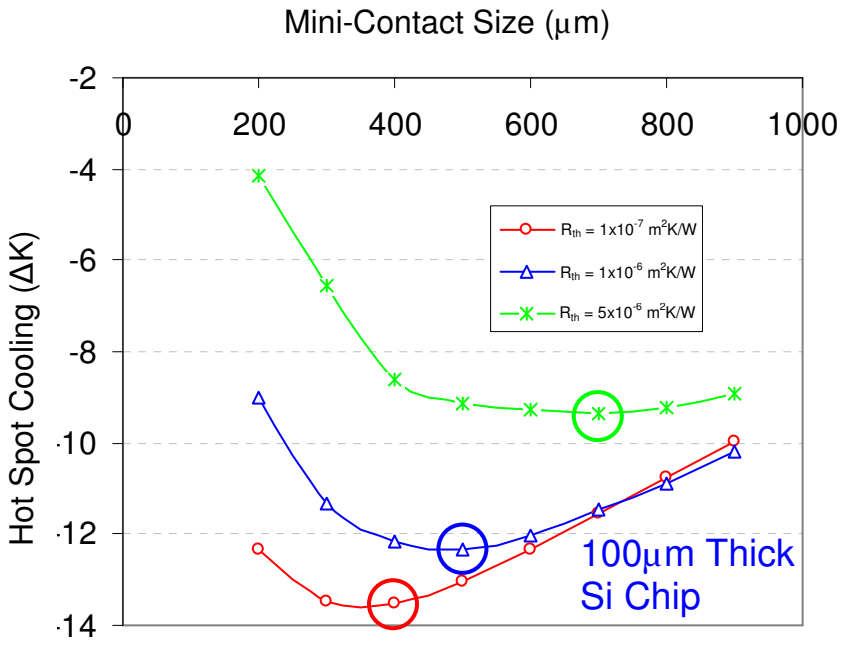



**Figure 4.8: Hot spot temperature reduction associated with optimum mini-contact sizes at different thermal contact resistances. TE leg height = 20µm**

#### 4.3.3.2 Combined with Effect of Silicon Chip Thickness

The hot spot temperature reduction associated with the TEC-mini-contact approach is limited by the heat spreading that occurs inside the Si chip. In thicker chips, the cooling effect of the mini-contact extends laterally and is less effective in attracting heat from the on-chip hot spot. Consequently, a thinner chip allows the µTEC to remove more of the hot spot heat and produce greater hot spot cooling. Figure 4.9 shows the optimum mini-contact sizes at various thermal contact resistances for a 500µm Si chip. It is easily observed that these hot spot cooling values of approximately 2-3K are significantly lower than those observed in figure 4.8 for the 100µm chip and occur at far larger optimum mini-contact sizes, reaching 1000µm or 1mm - for the 5 x $10^{-6}$ m2K/W. These results show the dependence of hot spot temperature reduction on Si chip thickness in addition to thermal contact resistance, and mini-contact size.

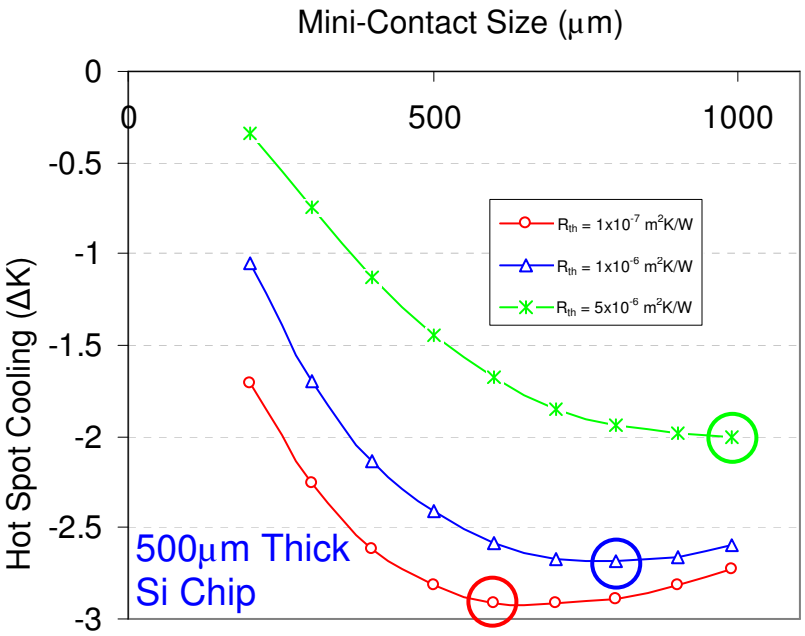



**Figure 4.9: Hot spot temperature reduction associated with optimum mini-contact sizes at different thermal contact resistances. TE leg height = 20µm**

#### 4.3.3.3 Combined with Effect of Thermoelectric Leg Height

Thermoelectric cooling is limited by the heat conduction through the TE legs from the hot side to the cold side. This effect depends on the thermal conductivity of the TE legs and their height. The heat rejected at the hot side of short TE legs will more easily conduct back to the cold side and reduce net cooling. However, the higher electrical resistance of taller TE legs will produce additional Joule heating. There is, thus, an optimum TE leg height.

To gain insight into the dependence of hot spot cooling purely on variations in TE leg height, a sample configuration was chosen that featured a 400x400µm$^2$ mini-contact tip with both low and modestly high thermal contact resistance values of 1x10$^{-7}$ and 5x10$^{-6}$ m$^2$K/W. Figure 4.10 shows a clear optimum TE leg height of 40µm for the nearly ideal thermal interface but far weaker hot spot cooling sensitivity to leg height with a higher thermal contact resistance. With the higher, 5x10$^{-6}$ m$^2$K/W, thermal contact resistance,

hot spot temperature reduction varied by only 0.5K over a range of 20µm-90µm TE leg heights.

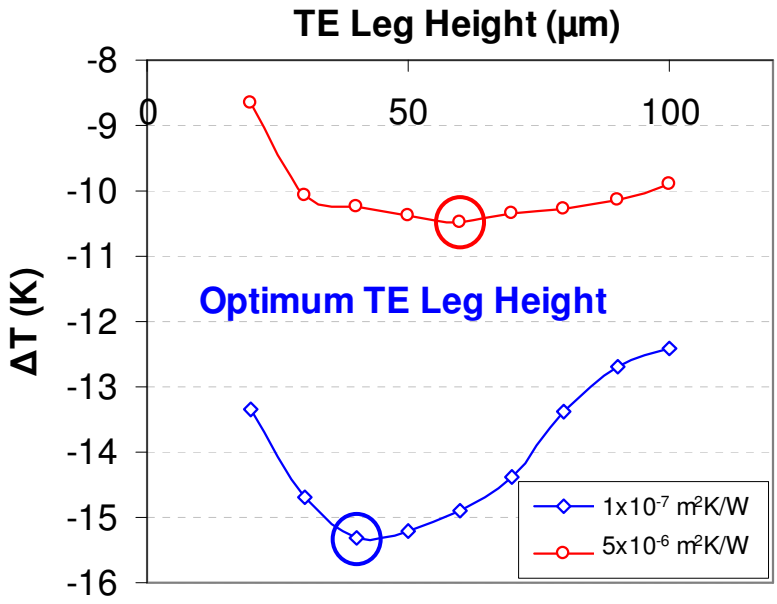



**Figure 4.10: Hot spot temperature reduction associated with variations in TE leg height. A 400x400µm$^2$ mini-contact is used and two different thermal contact resistances are explored**

A dual ANSYS optimization was performed for TE leg heights and mini-contact sizes at each of the thermal contact resistance values in this study, with the 100µm thick Si chip. Table 4.2 shows the sensitivity of hot spot cooling relative to variations in mini-contact size and TE leg height; the optimum cooling achieved for both of these parameters is highlighted in red. At very low values of thermal contact resistance and optimized package dimensions, the hot spot temperature can be reduced by as much as 16K, relative to the case when the TEC is present but turned off. Hot spot cool-down values relative to the package configuration with no TEC or mini-contact present, were 11K for $1x10^{-7}$ $m^2K/W$, 10K for $1x10^{-6}$ $m^2K/W$, and only 0.1K for $5x10^{-6}$ $m^2K/W$. It may also be noted that the multi-dimensional optimization softens the impact of the primary variables, such as mini-contact tip size and leg height, on hot spot cooling but that –

under all circumstances - increasing interface resistance leads to a loss in cooling effectiveness and a shift to larger optimum mini-contact tip dimensions.

The optimum TE leg height did not vary significantly (40µm-50µm) over the range of thermal contact resistances studied and the mini-contact size seemed to increase with increasing thermal contact resistance (from 300x300µm$^2$ to 600x600µm$^2$). Even with modest thermal contact resistance of 5x10$^{-6}$m$^2$K/W, 11.6K of hot spot cooling can occur with optimized dimensions. These observed hot spot temperature reductions can be expected to decrease with increased chip thickness.

**Table 4.2: Hot spot temperature reduction for optimized TE leg height and mini-contact sizes at each thermal contact resistance, with surrounding sensitivity. Si chip thickness = 100µm**

| $R_{th}$ = 1x10$^{-7}$m$^2$K/W | Mini-Contact Size (µm$^2$) | | |
|---|---|---|---|
| TE Leg Height (µm) | 200x200 | 300x300 | 400x400 |
| 40 | -14.43 | -15.15 | -15.3 |
| 50 | -15.5 | **-15.97** | -15.2 |
| 60 | -15.4 | -15.5 | -15.02 |
| | | | |
| $R_{th}$ = 1x10$^{-6}$m$^2$K/W | Mini-Contact Size (µm$^2$) | | |
| TE Leg Height (µm) | 300x300 | 400x400 | 500x500 |
| 30 | -12.84 | -13.4 | -13.42 |
| 40 | -14.15 | **-14.56** | -14.22 |
| 50 | -14.45 | -14.45 | -14.25 |
| | | | |
| $R_{th}$ = 5x10$^{-6}$m$^2$K/W | Mini-Contact Size (µm$^2$) | | |
| TE Leg Height (µm) | 500x500 | 600x600 | 700x700 |
| 30 | -10.97 | -11.22 | -11.05 |
| 40 | -11.47 | **-11.62** | -11.49 |
| 50 | -11.07 | -11.15 | -11.4 |

## 4.4 Conclusion

A package-level numerical model was built to investigate hot spot temperature reduction associated with the application of a conventional $Bi_2Te_3$ based TEC with an integrated mini-contact pad that focuses, and increases, the cooling flux of the TEC. Attention is placed on the effects of thermal contact resistance at the interfaces of the

TEC and mini-contact on optimum package dimensions. Parametric variations in microprocessor hot spot cooling occurred at different mini-contact tip sizes, TE leg heights, and Si chip thicknesses. For an optimized chip package with nearly ideal thermal interfaces, hot spot cooling by as much as 16K may be achieved relative to when the TEC is present but turned off and as much as 11K relative to the package configuration with no TEC or mini-contact present.

# Chapter 5

# 5. Experimental Testing of Mini-Contact Enhanced TEC

## 5.1 Introduction

A proof-of-concept experiment, designed to demonstrate the spot cooling capability of the mini-contact/TEC, was performed. In this experiment, thin film heaters are used to create uniform heating on the test chip and attention was focused on the ability of the mini-contact/μTEC to locally cool the substrate. The observed temperature reductions serve to establish the feasibility of spot cooling with the mini-contact enhanced TEC and validate the model used to predict hot spot remediation in operating chips. Experimental results for miniature TEC's, with 130μm TE leg heights, are presented with a matching fit to a numerical FE model. These results also serve as a point of reference for the numerical FE model used in previous chapters.

## 5.2 Experimental Setup

Conceptually, the experimental chip package was the same as the simulated package in Chapter 4, although with different dimensions and without a hot spot. Figure 5.1 shows the experimental package with uniform heating on the silicon substrate. To simulate the power dissipation of the chip, four thin film heaters were attached to the Si die. The TECs used in this experiment, shown in figure 5.2, were provided by Thermion™ [55] and feature a 6x6 array of 370μm x 370μm x 130μm $Bi_2Te_3$ legs. The top and bottom AlN TEC ceramic substrates each had a thickness of 635μm and lateral dimensions of 3.6mm x 3.6mm and 4.8mm x 4.8mm, respectively. The ceramic substrates were also pre-plated with indium tin to promote solder adhesion. The thermal conductivity of the bismuth telluride was 1.3-1.4W/mK, the Seebeck coefficient was in

the range of 200μV/K, and the electrical resistivity was in the range of 10Ω-μm, with a figure of merit Z of $3x10^{-3}K^{-1}$ [57]. A more detailed description of the experimental apparatus and procedure can be found in [9]. The experimental apparatus and procedure was initially designed and fabricated by Dr. Peng Wang.

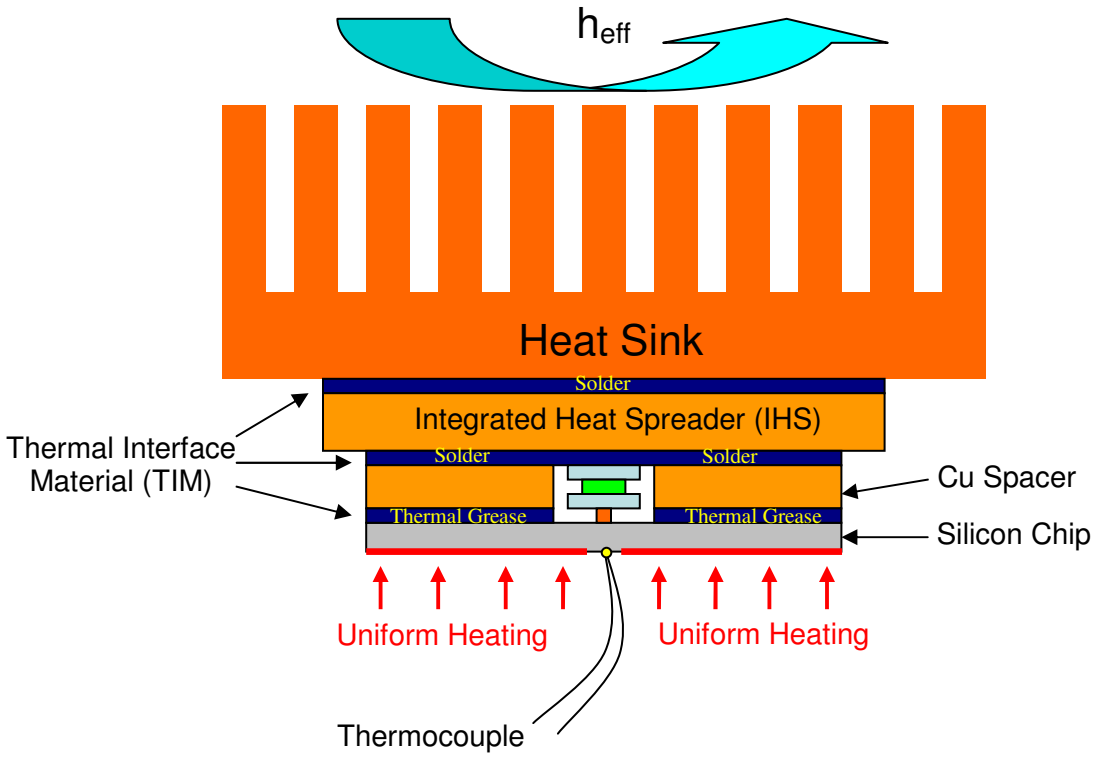



**Figure 5.1: Schematic of the experimental package with a mini-contact enhanced TEC (not drawn to scale)**

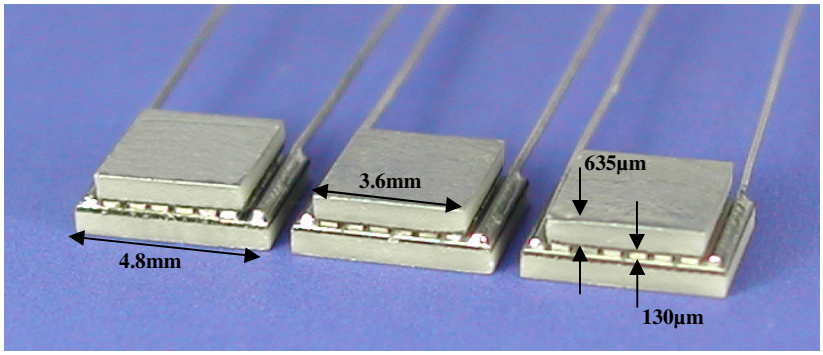



**Figure 5.2: Thermion™ TEC's with a 6x6 array of 130μm thick bismuth telluride TE legs [57]**

### 5.2.1 Preparing the Si Die

The 500µm thick silicon wafers, used in the experiment, were prepared by the Fab Lab at Maryland NanoCenter. Since solder will not adhere directly to silicon, a 200nm layer of Cr was deposited on the back of the wafer followed by a 200nm layer of Au to facilitate the solder bond with the mini-contact tip. The wafers were then hand cut into 25mm x 25mm dies. At 156.6°C, the indium solder used to attach the mini-contact tip to the Si die will react with gold and form an intermetallic compound ($AuIn_2$) that acts as the bond between these two components. The Cr layer is used as an adhesion layer between Au and Si because Au, also, does not adhere directly to Si. A photograph of the gold coated Si wafer and dies is shown in figure 5.3.

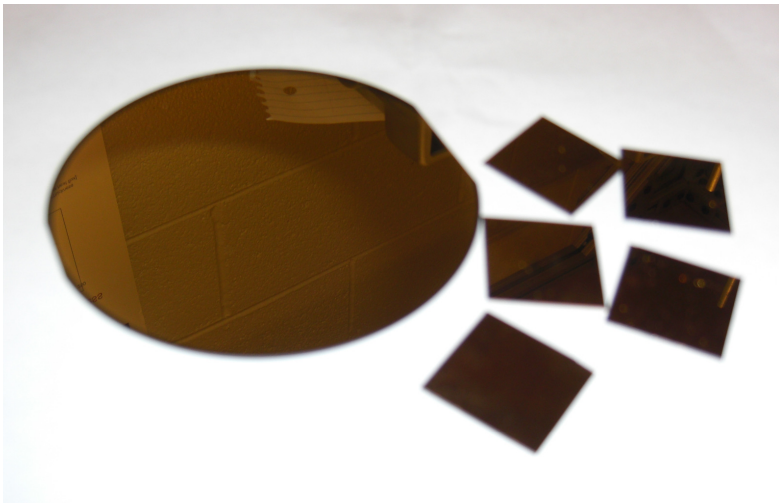


**Figure 5.3: Au coated Si wafer and dies used in the experiment**

### 5.2.2 Machining the Mini-Contact

2mm thick copper mini-contact are then machined to be later attached to the back of the Si die. The first step in machining the mini-contacts is reducing them to tiny copper blocks whose lateral dimensions match those of the Thermion™ TEC (3.6mm x 3.6mm). From this point, the two sides of the mini-contact are polished with 800grit sand

paper to produce a smooth, flat finish. This is done before the mini-contact tip is machined because polishing the tip, while maintaining it parallel to the polishing surface is nearly impossible to do by hand, due to the tip's small dimensions. Once the mini-contact is polished, the tip is machined and the finished mini-contact is cleaned with acetone. The machining procedure for the mini-contacts is shown in figure 5.4.

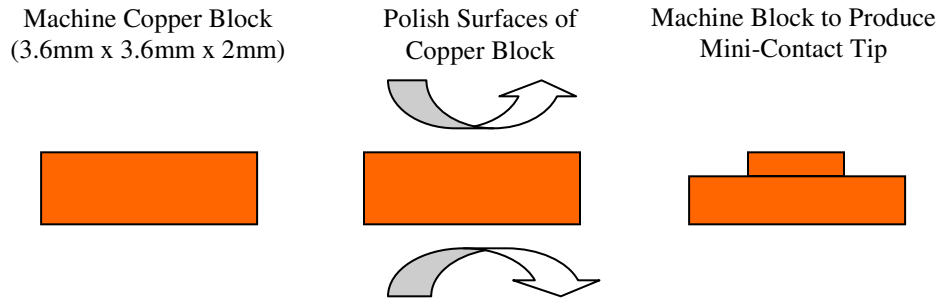



**Figure 5.4: Mini-contact machining process**

### 5.2.3 Attaching the Mini-contact

The mini-contact tip is bonded to the Si die using indium based solder. In this study, two different mini-contact tip sizes were tested (1.3x1.3mm$^2$ and 3.6x3.6mm$^2$). Achieving a good bond between the Si die and the mini-contact tip is particularly difficult for the 1.3x1.3mm$^2$ tip because of the very small contact area with the Si die. This is performed on a hot plate set at a stage temperature of 160°C; the die and mini-contact are placed on the hot plate and allowed to heat up. Then, a 1.3x1.3mm$^2$ sheet of indium solder foil is cut and placed on the tip of the heated mini-contact, which has already been coated with flux. The indium solder melts on the mini-contact tip and the mini-contact is removed from the hot plate and allowed to cool. Then, the mini-contact is turned upside down and the tip is placed on the Au coated Si die that is still on the hot plate. The indium solder reflows and the mini-contact stabilizes on top of the die. Slight pressure needs to be applied to the mini-contact to facilitate a good solder bond. The die, with

soldered mini-contact, is then carefully removed and from the hot plate and allowed to cool. Figure 5.5 shows the mini-contact tip soldered to the Si die.

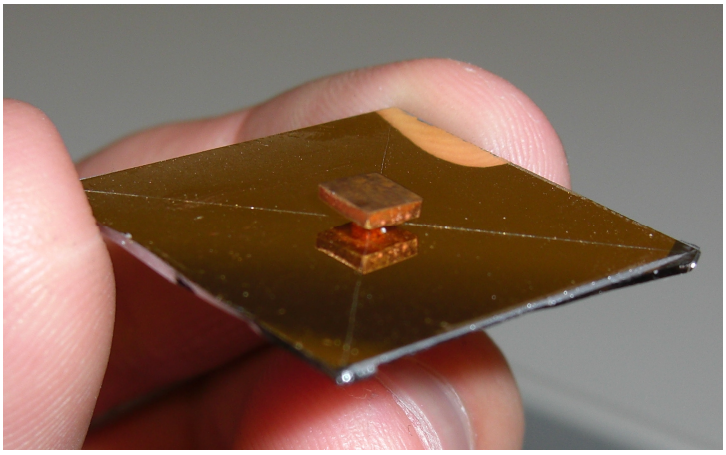


**Figure 5.5: Mini-contact soldered onto Si die**

### 5.2.4 Attaching the TEC

The TEC is bonded to the mini-contact base with indium-tin solder, which has a lower melting point than the indium solder bond at the mini-contact tip. The Si die, with soldered mini-contact, is placed on the hot plate at a stage temperature of 130°C, such that the indium solder would not melt, and flux is applied to the top (base) surface of the mini-contact. A small amount of indium-tin solder, which melts at 118°C, is then applied to the mini-contact base surface and the TEC is gently placed on top of the solder/mini-contact base. Slight pressure is applied to the top of the TEC to promote a good solder bond with the mini-contact.

### 5.2.5 Attaching the Cu Spacer, Heat Spreader, and Heat Sink

A machined copper spacer is placed around the mini-contact/TEC and thermal grease (Arctic Silver 5) [58] is used to bond the bottom of the spacer to the top of the Si die. The Cu spacer has a central cavity to accommodate the mini-contact/TEC and two

machined trenches along its top surface to accommodate the wires that provided input power to the TEC. The top of the TEC and top of the Cu spacer are bonded to a copper heat spreader using indium tin solder. Thermal grease is used between the top of the heat spreader and the copper heat sink with attached fan. The experimental setup is shown below in figure 5.6.

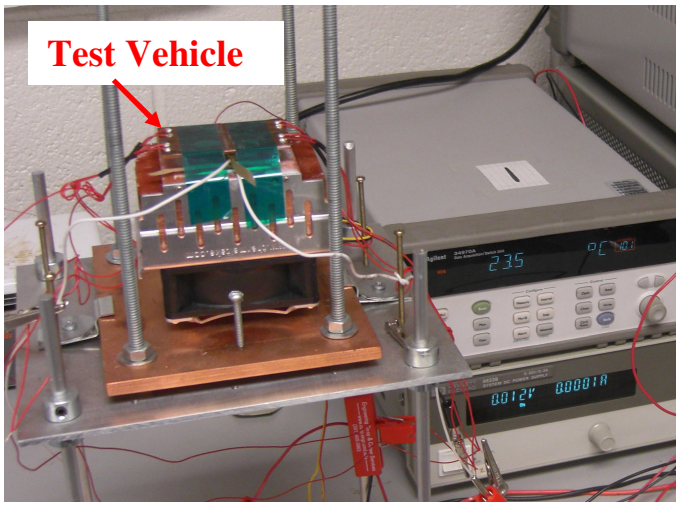



**Figure 5.6: Experimental test package with power supply and temperature measurement equipment**

### 5.3 Thermal Test and Experimental Results

Power is supplied to the bottom of the silicon die using four thin-film Minco heaters [59] activated by an HP E3611A System DC Power Supply to simulate different chip power dissipations on the silicon chip. An OMEGA E-type thermocouple, with a diameter of 76μm, is bonded to the bottom of the silicon wafer using thermal epoxy to measure the spot cooling performance. Based on thermocouple calibration at 0°C and 100°C, respectively, the measurement uncertainty is estimated to be +/- 0.2°C [28]. The tip of the thermocouple is aligned at the center of the Si die and separated by the silicon from the copper mini-contact pad and the TEC. For each particular heat load on the

silicon die, an electric current is applied to the TEC by an Agilent 6038A System Power Supply and the temperature, current and voltage are recorded by an Agilent 34970A Data Acquisition/Data Logger System. The thermal data reported herein relate to steady-state conditions, usually obtained some 10~30 minutes after the test vehicle was powered [28].

Two experiments were performed, one with a mini-contact tip size of $3.6x3.6mm^2$ (same size as the mini-contact base) and a second test with a tip size of $1.3mmx1.3mm^2$ (close to the optimized tip dimensions). In both test cases, the current applied to the TEC was increased in increments of 0.5A and temperature reductions on the chip were measured at steady state; the measurements were repeated three times to obtain average values. In the first test, with the $3.6x3.6mm^2$ mini-contact, 0W, 30W, and 67W of heat were applied uniformly to the bottom of the Si die and in the second test, with the $1.3x1.3mm^2$ mini-contact, 0W, 29W, and 54W were applied.

To support detailed evaluation of mini-contact TEC cooling and comparison to the results of numerical simulation, experimental measurements of the electrical resistance, for the two mini-contact tests, were performed. It was experimentally observed that as the temperature increased in the $3.6x3.6mm^2$ mini-contact test, the electrical resistance also increased. The opposite occurred in the $1.3x1.3mm^2$ mini-contact test, where the resistance decreased with increasing temperature. These trends, shown in figure 5.7, led to the development of temperature dependent functions for the thermoelectric properties, S and $\rho$, for each of the two configurations. The role played by the electrical contact resistance and its possible dependence on temperature and/or current, relative to the variance in the bulk properties of the $Bi_2Te_3$, could not be ascertained.

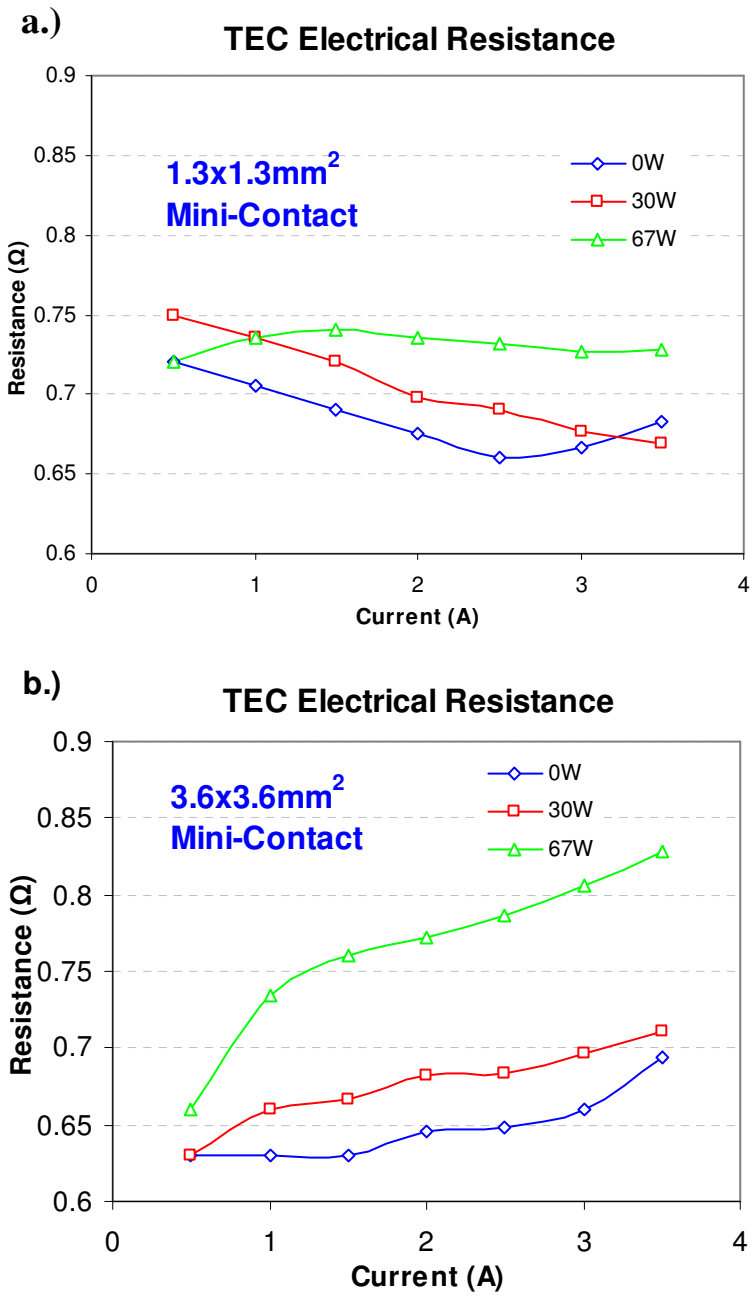



**Figure 5.7: Experimentally observed TEC electrical resistance variations at different input currents and temperatures for the 1.3x1.3mm$^2$ (a) and 3.6x3.6mm$^2$ (b) mini-contacts**

The temperature reductions achieved for the two mini-contact geometries are shown in figures 5.8 and 5.9. The expected parabolic dependence of temperature reduction on electrical current is observed for each case considered and it is seen that a

peak temperature reduction of 8.5K was achieved. Although it was expected that the optimized mini-contact tip of 1.3x1.3mm$^2$ would yield higher spot cooling values than the larger 3.6x3.6mm$^2$ tip, these experiments yielded similar cooling results. It appears that the difficulties in precise assembly of the smaller mini-contact may be responsible for this outcome, as discussed below.

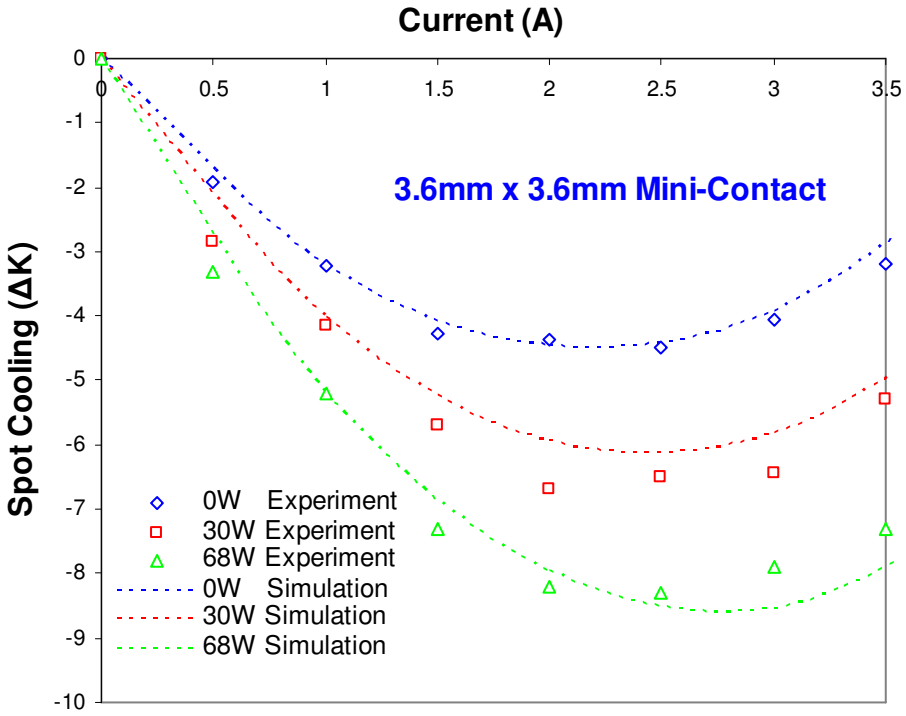



**Figure 5.8: Experimental and numerical spot cooling values, as a function of current, on a 500µm thick Si die with a TEC and 3.6x3.6mm$^2$ mini-contact. TE leg height = 130µm, $R_{th}$ = 9x10$^{-6}$ m$^2$K/W at the TEC and 2x10$^{-6}$ m$^2$K/W at the mini-contact/Si die**

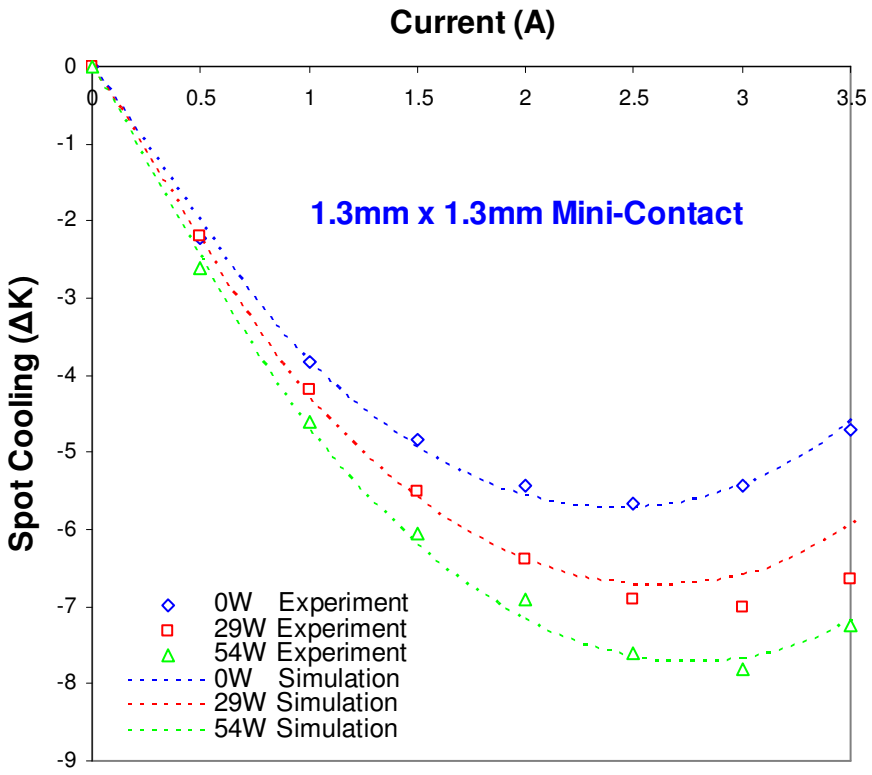



**Figure 5.9: Experimental and numerical spot cooling values, as a function of current, on a 500µm thick Si die with a TEC and 1.3x1.3mm$^2$ mini-contact. TE leg height = 130µm, $R_{th}$ = 8.5x10$^{-5}$ m$^2$K/W at the TEC and 2x10$^{-6}$ m$^2$K/W at the mini-contact/Si die**

### 5.3.1 Numerical Validation

The ANSYS™ model was used to numerically determine the thermal contact resistances ($R_{th}$) at the interfaces of the TEC and mini-contact through an "inverse calculation," based on equating the numerical and experimental results. While the precise Seebeck coefficient (S) and electrical resistivity (ρ) of the bismuth telluride in the TEC's are dependent on the manufacturing process and were not explicitly known, the literature does provide a possible range for each of these material properties [33]. Temperature dependent values of the Seebeck coefficient and electric resistivity, within the range of reported values, were used to fine tune the numerical FE model to fit the experimental

results for the 3.6x3.6mm$^2$ and 1.3x1.3mm$^2$ mini-contact experiments. Equations 5.1a and 5.1b show the temperature dependent S and ρ values used to fine tune the numerical model to the 3.6x3.6mm$^2$ mini-contact experiment and equations 5.2a and 5.2b show the S and ρ values used for the 1.3x1.3mm$^2$ mini-contact experiment.

$S = -0.00185*T_j^2 + 1.41*T_j - 41.6\ \mu V/K$ (3.6x3.6mm$^2$ m.c. experiment) (5.1a)

$\rho = 0.02*T_{avg} + 5.64\ \Omega\text{-}\mu m$ (3.6x3.6mm$^2$ m.c. experiment) (5.1b)

$S = -0.22*T_j + 262\ \mu V/K$ (1.3x1.3mm$^2$ m.c. experiment) (5.2a)

$\rho = -0.0056*T_{avg} + 9.0183\ \Omega\text{-}\mu m$ (1.3x1.3mm$^2$ m.c. experiment) (5.2b)

In the equations for S, $T_j$ is the junction temperature at each interface of the $Bi_2Te_3$ leg and in the equations for ρ, $T_{avg}$ is the average temperature of the $Bi_2Te_3$ leg.

For the 3.6x3.6mm$^2$ mini-contact tip, the Seebeck coefficient (S) increased by approximately 11μV/K and the electric resistivity (ρ) by 1Ω-μm, across the experimental temperature range. By contrast, for the 1.3x1.3mm$^2$ mini-contact tip, the Seebeck coefficient decreased by approximately 10μV/K and the electric resistivity by 0.3Ω-μm. This variance of the TEC electrical resistivity with increased temperature was reflected in the measured values of electrical resistance in figure 5.7.

The fine-tuned ANSYS™ model was used to extract the thermal contact resistance values at the TEC ceramic substrate interfaces with the mini-contact (below) and the heat spreader (above). An electrical contact resistance of $1x10^{-6}$ Ω-μm$^2$ was assumed at the interfaces of each TE leg and a thermal contact resistance of $2x10^{-6}$ m$^2$K/W was assumed at the mini-contact/Si die interface, based on previous work [9,28].

The thermal contact resistance at the TEC interfaces was observed to be $9x10^{-6}$ $m^2K/W$ and $8.5x10^{-5}$ $m^2K/W$ for the $3.6x3.6mm^2$ and $1.3x1.3mm^2$ mini-contact tests, respectively. Figures 5.8 and 5.9 show that the dependence of the experimental temperature reduction values on the applied current and the applied heating rate are in very good agreement with the values obtained from the tuned numerical FEM model for the two test cases. This agreement serves to establish that the numerical model did capture the underlying physical phenomena responsible for the effectiveness of the mini-contact TEC in producing significant local cooling on a heated substrate.

It appears that the relatively high thermal contact resistance of the $1.3x1.3mm^2$ mini-contact is most likely the reason for the less than expected cooling achieved with this mini-contact configuration. Figure 5.10 displays the localized cooling – reaching 14K at 3.5 amps and 54 W - that could have been achieved if the thermal contact resistance value at the TEC ceramic substrate interface with the mini-contact (below) and TIM2 (above) was equal to $9x10^{-6}$ $m^2K/W$, the value determined for the larger mini-contact tip dimension. Comparing the results shown in figure 5.8 with the values in figure 5.10, the significant and most beneficial effect of the reduced mini-contact tip dimension is clearly seen.

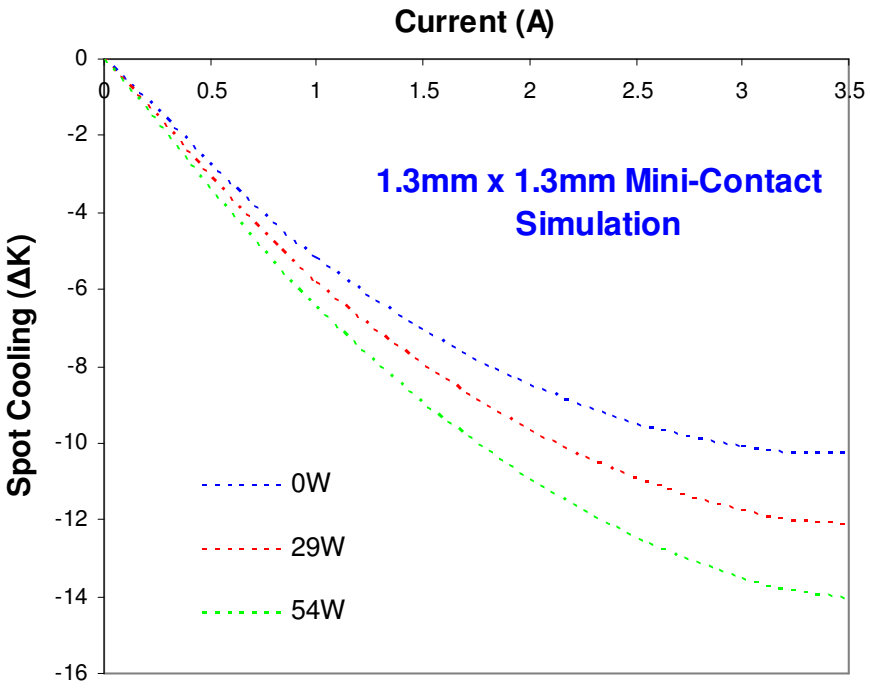



**Figure 5.10: Numerical model of 1.3x1.3mm$^2$ mini-contact experiment with low thermal contact resistance found in the 3.6x3.6mm$^2$ experiment ($R_{th}$ = 9x10$^{-6}$ m$^2$K/W)**

### 5.4 Conclusion

An experiment designed to demonstrate the feasibility of the mini-contact enhanced TEC cooling approach. The experimental setup and procedure are described and experimental mini-contact/TEC spot cooling measurements are presented. These results show significant spot cooling values of ~8.5K that display the viability of this cooling approach. A numerical ANSYS™ FE model, depicting the experiment, is also built to extract thermal contact resistance values from the experimental results. The close agreement achieved between the numerical and experimental results for the uniformly heated chip, seen specifically in the parametric variation of spot cooling with the electrical current and heater power, establishes the validity of using the numerical model

to investigate parametric variations of the on-chip hot spot temperature with package dimensions and thermal contact resistances.

# Chapter 6

# 6. Conclusions and Future Work

## 6.1 Conclusions

This thesis explores novel thermoelectric hot spot cooling techniques originally developed by Bar-Cohen, Wang, and Yang. One of the objectives of this research is to study and further develop the silicon microcooler, which is a novel thermoelectric cooling technique utilizing the silicon in the microprocessor itself as the main thermoelectric material. A numerical model has been developed for a silicon microcooler with an integrated silicon germanium superlattice layer to study the impact of various package parameters on hot spot temperature reduction and to compare this approach with the original silicon microcooler. This thesis also expands on research of the mini-contact enhanced TEC, another novel thermoelectric hot spot cooling technique that utilizes commercially available TEC technology and concentrates the cooling flux of the TEC to dramatically improve hot spot cooling performance. The objectives of this thesis are to understand and accurately model the thermal physics associated with thermoelectric hot spot heat removal, to develop qualitative parametric trends and optimizations for certain package dimensions and boundary conditions that influence hot spot temperature, and to predict and quantify the thermal performance of the μTECs.

### 6.1.1 Conclusions for the Superlattice Microcooler

The numerical ANSYS™ comparison of the superlattice microcooler and the silicon microcooler in chapter 2 determined that, for the parametric range of dimensions and boundary conditions studied, the silicon microcooler always produces a greater hot spot cool down than the superlattice microcooler. This is most likely due to the low

thermal conductivity of the SiGe superlattice and corresponding increased thermal resistance above the hot spot. Although the top surface of the superlattice always achieves the lowest local temperatures, it appears that the integration of a superlattice layer into a silicon microcooler would not be beneficial for hot spot cooling.

### 6.1.2 Conclusions for the Mini-Contact Enhanced TEC

The numerical simulations in this thesis have shown how the cooling flux of a conventional miniature TEC can be dramatically enhanced with a mini-contact pad and how thermal contact resistance can adversely affect this thermal management approach. Although the experiments in this thesis could not physically show a change in cooling with different mini-contact tip sizes, detailed numerical analysis of the experiments shows that this is most likely due to differing thermal contact resistance values, for the two experiments, that equalized the spot cooling results for the smaller and larger mini-contact tip sizes. However, an improvement in cooling due to an optimum mini-contact size can actually be observed in the experiments of Wang [9].

The results of the ANSYS™ simulations in chapter 3, as well as comparison of the Taiwanese-defined packaging and hot spot configurations to previously studied miniature TEC-cooled, on-chip hot spots, suggest that: (1) The relatively large size (11% of the chip area) and dissipated power (19% of chip power) in the Taiwanese "hot spot" place a heavy burden on the spot cooling TEC's and limit their effectiveness; (2) Reducing the TE leg height of the Taiwanese thermoelectric devices, to yield greater cooling heat fluxes, could result in "real" hot spot temperature reductions of nearly 10K; and (3) The small thermoelectric element area fraction of the commercial TFTEC device and the further dilution of the cooling effect by use of a relatively large Si chip (5 times

larger than the device) greatly compromises the effectiveness of this TEC cooler and makes it unsuitable for use for this application. Nevertheless, noticeable hot spot temperature reductions should be achievable with a robust package assembly process.

The numerical study in chapter 4 verifies that thermal contact resistance at the Si chip, mini-contact, and TEC interfaces is one of the key driving factors in the design of optimum package dimensions as well as in the viability of the mini-contact enhanced TEC cooling approach. It was also observed that a thinner Si chip is more likely to yield greater hot spot temperature reductions than a thicker chip. Overall, this chapter provides guideline for maximizing the hot spot cooling performance associated with the mini-contact cooling approach.

Chapter 5 experimentally verifies the feasibility of the mini-contact cooling approach for spot cooling of a heated die and provides inversely-determined thermal contact resistances achieved in the assembled thermal test package. The numerical model shows excellent agreement with the experimental results and establishes the efficacy of using the numerical model to investigate thermoelectric mini-contact cooling of a chip with a hot spot.

### 6.2 Future Work

Unfortunately, due to fabrication delays at the Taiwanese national lab, experimental testing of the assembled Taiwanese chip package could not be performed prior to the completion of this thesis. Future experimental temperature measurements of the Taiwanese package should be completed and the ANSYS™ numerical model should be validated. Detailed efforts should be focused on improving the package assembly process to ensuring clean thermal interfaces. Based on the initial results and additional

FEM simulations, it is proposed to continue the development of miniaturized TEC coolers for hot spot remediation on Taiwanese chips.

Due to the current low efficiency of thermoelectric heat pumps future efforts in this research must also focus on reducing thermal contact resistance at the interfaces of the TEC. One of the most promising ways of achieving this goal is through material deposition, which is capable of yielding some of the lowest thermal contact resistance values attainable. Future research may include the formation of thermoelectric materials directly on the back surface of a chip. This will likely produce the most promising cooling results but the major hurdles to this approach will be finding a cost effective way to implement this technology and physically building and testing a successful specimen.

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