

ABSTRACT

Title of Dissertation: MODELING AND CHARACTERIZATION OF 4H-SiC
MOSFETS: HIGH FIELD, HIGH TEMPERATURE, AND
TRANSIENT EFFECTS

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We present detailed physics based numerical models for characterizing 4H-Silicon Carbide lateral MOSFETs and vertical power DMOSFETs for high temperature, high field, DC, AC and transient switching operating conditions. A complete 2-D Drift-Diffusion based device simulator has been developed specifically for SiC MOSFETs, to evaluate device performance in a variety of operating scenarios, and to extract relevant physical parameters.

We have developed and implemented room and high temperature mobility models for bulk phonon and impurity scattering, surface phonon scattering, Coulomb scattering from interface traps, and surface roughness scattering. High temperature models for interface trap density of states and occupation probability of interface traps are also implemented. By rigorous comparison of simulated I-V characteristics to experimental data at high temperatures, physical parameters like interface trap density of states, surface step height, saturation velocity, etc. have been extracted. Insight into relative importance of scattering mechanisms influencing transport in SiC MOSFETs has been provided. We

show that the strongest contribution to low current in SiC MOSFETs is from the loss of mobile inversion charge due to large amount of trapping at the interface, and due to very low surface mobility arising due to a rough SiC-SiO₂ interface. We show that surface roughness scattering dominates at high gate biases and is the most important scattering mechanism in 4H-SiC MOSFETs.

Switching characteristics of SiC lateral MOSFETs have been modeled and simulated using our custom device simulator. A comprehensive generation-recombination model for interaction between inversion layer electrons and interface traps has been developed. Using this model, we have modeled the time-dependent occupation of interface traps spread inside the SiC bandgap. We have measured the transient characteristics of these devices, and compare our simulation to experiment and have extracted capture cross-sections of interface traps. Using the coupled experiment and modeling approach, we are able to distinguish between fast interface traps and slow oxide traps, and explain how they contribute to threshold voltage instability.

High power 4H-SiC DMOSFET operation in the ON and the OFF states has also been analyzed. We show that in current generation SiC DMOSFETs, the ON resistance is dominated by the channel resistance instead of the drift-layer resistance. This makes the design of SiC DMOSFETs far from ideal. OFF state blocking capability and breakdown due to impact ionization of the DMOSFETs are also modeled and simulated. We show that the 4H-SiC DMOSFETs have excellent leakage characteristics and can support extremely high OFF state drain voltages.

MODELING AND CHARACTERIZATION OF 4H-SIC MOSFETS: HIGH FIELD,
HIGH TEMPERATURE AND TRANSIENT EFFECTS

by

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Dedication

To Datta,

My friend, my wife, and my champion.

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Chapter 1

1. Introduction

Silicon Carbide (SiC) MOSFETs are at their early stages of development. There is great interest in developing SiC MOS devices because of their promising applications in high temperature high power environments. The wide bandgap of SiC makes it ideal for operation in high temperature environments like engines, and oil-wells for power conversion and sensor application. The high bandgap leads to extremely low leakage currents making it suitable for UV sensor device design. The high thermal conductivity of SiC and ten times higher breakdown field than Silicon makes it the material of choice for high power MOSFET design capable of switching several amperes of current, while blocking several kilovolts of voltage in the OFF state. Finally, as SiC has a natural oxide in SiO₂, making MOSFETs out of SiC is not hard. The benefits in terms of intrinsic electrical and thermal properties of SiC over Silicon are highlighted in Table 1.1. Amongst the various polytypes of SiC, 4H-SiC is considered the most promising for MOSFET development, primarily due to its high intrinsic carrier mobility.

Table 1.1 Important physical properties of Silicon and polytypes of SiC

	Si	3C-SiC	6H-SiC	4H-SiC
Bandgap (eV)	1.1	2.39	2.86	3.26
Intrinsic Electron Mobility (cm ² /Vs)	1400	1000	600	1070
Saturation Velocity ($\times 10^7$ cm/s)	1	2	2	2
Critical Breakdown Field (MV/cm)	0.3	2	3	3
Thermal Conductivity (W/K·cm)	1.5	4.9	4.9	4.9

However, the issues of reliability, repeatability and stability of MOSFET structures that had plagued Silicon several decades ago are very relevant today for SiC. The biggest problem faced by the SiC MOS community today is the issue of very low surface mobility. The low mobility is as a result of two main shortcomings of the SiC-SiO₂ interface. i) The presence of a large number of interface traps [1][2][3] and ii) the rough surface of the semiconductor [4][5]. These two disadvantages have the potential to make SiC MOSFETs completely unviable.

The large number of interface states distributed over the entire bandgap of SiC gives rise to large amount of Coulombic scattering of the inversion layer mobile carriers. This lowers the surface mobility significantly. Further, the traps get occupied before the inversion layer can form on application of a gate bias. This leads to low mobile charge and hence lower currents. This also causes problems in proper engineering of the threshold voltage of SiC MOSFETs. Understanding these interface traps, their causes, their effects in various operating conditions, and their behavior at high temperatures is very essential in order to use SiC MOSFETs in various circuit applications.

The roughness of the SiC-SiO₂ interface is another cause of low surface mobilities. The 8° off-axis step flow growth of the SiC substrate and thermal oxidation causes step bunching at the interface. This step bunching gives rise to small nanosteps and large macrosteps. These steps cause scattering of surface mobile carriers giving low mobilities. Further, recent studies have found evidence of a Si-C-O transition region at the interface, which may be another cause of high surface roughness scattering.

Other physics related issues in the development of SiC MOS devices are the presence of oxide traps and fixed charge, oxide reliability, effects of ion implantation,

and phenomenon causing breakdown in the substrate. All these issues need to be addressed before SiC MOS devices can be reliably used in high temperature high power circuits.

1.1. Research Goals

The overall goal of this Ph.D. research is to formulate a comprehensive device model for 4H-SiC MOS devices. The device model should be able to explain, extract and predict the operation of 4H-SiC MOSFETs and DMOSFETs for a variety of operating modes at room and high temperatures. The problem has been divided in to three distinct parts – High temperature characterization of 4H-SiC MOS devices, transient modeling and characterization of 4H-SiC MOSFETs, and modeling of 4H-SiC power DMOSFETs. Details regarding the approach taken to achieve these goals, and the results of the research will be discussed in the following chapters.

1.1.1. High Temperature Modeling and Characterization of 4H-SiC MOSFETs

We will develop mobility models, interface trap physics models and other relevant physical models for 4H-SiC MOSFETs for temperatures ranging from 25°C to 200°C. These models will be extensively tested and calibrated by comparison to experimental I-V data. Typical issues that will be investigated include the behavior of traps at the SiC-SiO₂ interface at elevated temperatures, change in current with temperature, and how well the mobility models work for SiC devices at high temperatures. The focus of mobility modeling at high temperatures will be on Coulomb scattering mobility model, surface roughness mobility model, and high field saturation velocity based mobility model. Density of states for the interface traps as a function of temperature will be extracted by comparing simulated I-V curves to experiment.

1.1.2. Dynamics of Trap Occupation and Time Dependent Characterization of 4H-SiC MOSFETs

We will investigate the behavior of 4H-SiC MOSFETs in transient switching conditions. The focus of this research will be on characterizing the time dependent occupation of interface and near-interface traps. We will investigate how this affects threshold voltage shifts with time, current transience in the devices, and what effect will it have on switching circuits. We will try to extract a very important physical characteristic of the interface traps, namely the trap capture cross-section. A time dependent trap occupation and generation-recombination model will be developed to extract this quantity. We will also carry out transient experiments to calibrate our models and get values for the trap cross section.

Using the dynamic trapping model described above, we will extract small signal AC parameters like small signal conductance, capacitance, etc. for 4H-SiC MOSFETs. We will extend our device simulator to calculate C-V curves and compare them to experiment to further characterize the effects of interface traps on small signal circuits.

1.1.3. Physical Modeling and Characterization of High Power SiC DMOSFETs

Finally, the physical models we develop for lateral SiC MOS devices will be applied to power DMOSFET structures. Other phenomena relevant to high power DMOSFETs such as impact ionization and breakdown will be investigated. Various resistances of the DMOSFET will be analyzed and pointers would be suggested to

improve performance of these devices. Finally we will discuss mixed-mode modeling and simulation of a boost-converter circuit using 4H-SiC DMOSFET.

In the next section we present the key contributions of this research effort. In section 1.3 we review previous work on SiC device modeling and characterization. In section 1.4, we review some of our own previous work on room temperature low field modeling of SiC lateral MOSFETs.

1.2. Key Contributions

- Development of a comprehensive 2-D Drift-Diffusion based device simulator for SiC MOSFETs and DMOSFETs.
- Extraction of temperature dependence of interface states showing a spreading of the tail of the distribution inside the 4H-SiC bandgap with temperature.
- Development of surface roughness mobility model incorporating the effects of step flow growth process of SiC epi-layers.
- Quantifying the effect of quantum confinement on interface trap occupation in 4H-SiC MOSFETs.
- Extraction of variability across chips and devices on a single wafer using SPICE parameter extraction for SiC MOSFETs.
- Development of a comprehensive generation-recombination model for describing the dynamic interaction of interface, near-interface and oxide traps with inversion layer electrons.
- Development of a time-dependent trap occupation model and extraction of capture cross-sections of interface traps.
- Experimental measurement of characteristic current transients in 4H-SiC MOSFETs.
- Extraction of the relative contributions of channel resistance and drift layer resistance to total ON resistance in 4H-SiC DMOSFET.
- Modeling OFF state characteristics of a 4H-SiC DMOSFET including impact ionization related breakdown.

- Mixed mode modeling and simulation of 4H-SiC DMOSFET boost converter circuit.

1.3. Experimental and analytical work on SiC device characterization

Several groups have measured physical parameters for SiC MOS devices using a variety of methods. Zeng et al. [6] have shown a method of extracting energy dependent interface trap density for 6H and 4H-SiC MOSFETs in the subthreshold region of operation. Scozzie et al. [7] have shown the detrimental effects of interface-trapped charge on the SiC MOSFET characteristics. Arnold et al. [8] have shown that interface traps in SiC are responsible for decrease in transconductance, lower mobile inversion charge density and low drift mobility of inversion layer electrons. Saks et al. [9] have shown that severe trapping of electrons at the SiC-SiO₂ interface in 4H-SiC devices causes a reduction in the number of free electrons in the inversion layer, and also a drop in the mobility. Correlation between channel mobility and interface traps in SiC MOSFETs has also been described by Suzuki et al.[10][11]. All these observations have been made on the basis of experiments or compact modeling of SiC devices. Physics based simulations of deep submicron 4H-SiC MOSFETs have been presented by Dubaric et al.[12], but the authors have assumed that there are no interface charges at the SiC-SiO₂ interface. Roschke et al. [13] have proposed electron mobility models for 4H, 6H, and 3C SiC, which describe the dependence of the electron mobility on doping concentration, temperature and electric field. They too, have not shown any effect of interface traps in their mobility models. Nilsson et al. [14][15] have described Monte

Carlo and drift diffusion simulations of 4H and 6H-SiC field effect transistors. But they have only considered acoustic phonon scattering, polar and non-polar optical phonon scattering, and ionized impurity scattering. Mickevicius et al. [16] have carried out Monte Carlo simulations for SiC, but he has focused on phonon scattering and ionized impurity scattering. Roldán et al. [17] include the effect of a net interface charge in their work. However, their interface trap model is not energy dependent. But experimental measurements of interface state density of states for SiC have shown that the density of states is energy dependent. Vathulya et al. [18] have used an energy dependent interface state density of states model for 4H and 6H-SiC MOSFETs, and have extracted the inversion layer mobility by fitting the current equations to experimental data. They have used compact modeling and numerical methods to solve sets of equations simultaneously to extract an average mobility. Powell et al. [19][20] have described in detail various mobility models for 6H SiC MOSFETs. Their mobility model incorporates the effect of scattering due to occupied interface traps. But they do not show how scattering varies with depth inside the inversion layer. Their method for dealing with screening of the scattering charge centers in deep inversion is empirical. All this work is largely based on trying to extract relevant physics using experiment. A recent paper by Tilak et al. [21] describes scattering mechanisms in heavily doped SiC MOSFETs in an analytical model. Not much work has been done in terms of developing transport models for the effects seen in SiC MOS devices.

Recently, Lelis et al. [22][23] and Gurfinkel et al. [24] have shown the presence of oxide traps in SiC MOSFETs. They have shown their effects on long term threshold

voltage instability in these devices. Their work is mostly experimental and no models exist for time-dependent characterization of SiC MOSFETs.

There is not much research on the characterization of SiC devices at higher temperatures, and in real world application environments for example in switching applications. This needs detailed understanding of not only steady state DC but also time dependent, AC and transient behavior of SiC MOSFETs. We have tried to extract this behavior and the underlying physics as part of this research.

1.4. Our Previous Work on Low Temperature Modeling and Characterization of 4H-SiC MOSFETs

Previously, we have carried out detailed analysis of 4H-SiC MOSFET operation at room temperature in DC bias conditions by numerically solving the steady state semiconductor Drift-Diffusion equations. Room temperature mobility models for bulk phonon scattering, surface phonon scattering, surface roughness scattering, and Coulomb scattering by interface traps and oxide charges were developed and implemented [25][26]. To determine the effects of the large density of interface traps found at the SiC-SiO₂ interface, we extended previous work on Coulombic scattering [29][30][31][32][33][34] by developing a first principles Coulomb scattering mobility model specifically to model the physics of the inversion layer in 4H-SiC MOSFETs. The Coulomb scattering model took into account, scattering of mobile charges by occupied interface traps and fixed oxide charges, distribution of mobile charges in the inversion layer, and screening. Simulated I-V curves were compared to experimental data and the

density of states for the interface traps was extracted. Simulations indicated that occupied interface traps in 4H-SiC MOSFETs are responsible for mobility degradation, low currents and high threshold voltages. Their effect diminished at high gate voltages due to increased screening. It was also found that at high gate voltages, surface roughness scattering plays a major role in mobility degradation in 4H-SiC MOSFETs. The main results of these studies are given below.

Due to the very high density of interface traps at the SiC-SiO₂ interface, there is significant amount of immovable charge at the interface. This charge causes Coulombic scattering of inversion layer electrons lowering their mobility. This mobility reduction reduces the amount of current flowing through the device. Fig. 1.1 shows the different mobility mechanisms controlling the total low field mobility in a 4H-SiC device for a gate bias of 2V at room temperature. Coulomb scattering mobility is the dominant mechanism close to the interface. As the gate voltage is increased, there is an increase in the number of mobile carriers at the interface which screen the scattering charges causing an overall reduction in Coulombic scattering. Also, the surface field rises with increase in gate voltage giving increased surface roughness scattering. So, as shown in Fig. 1.2, at $V_{GS} = 12V$, surface roughness mobility dominates the total low field mobility in the device.

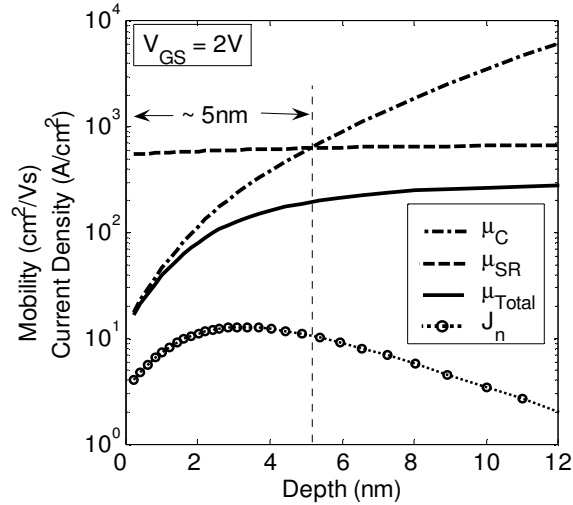


Fig. 1.1 Comparison between Coulomb scattering mobility (μ_C) and surface roughness mobility (μ_{SR}) at a gate-source voltage of 2V. Coulomb scattering mobility become greater than, and hence less important than, surface roughness mobility at a depth of around 5nm [26][27].

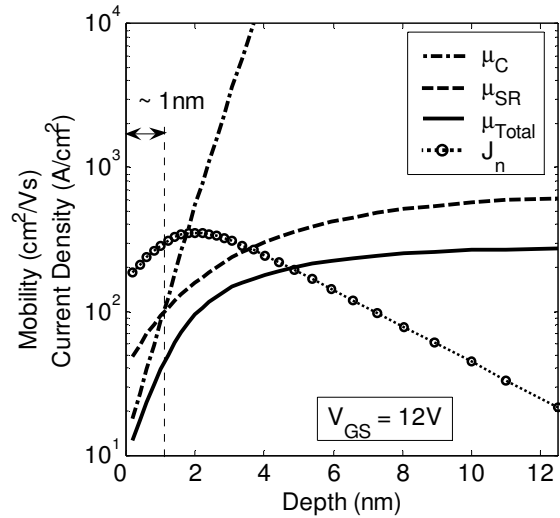


Fig. 1.2 Comparison between Coulomb scattering mobility and surface roughness mobility at a gate-source voltage of 12V. Coulomb mobility dominates the total low field mobility (μ_{Total}) only near the surface. Beyond a depth of around 1nm, the surface roughness mobility dominates the total low field mobility for most of the distance over which the current (J_n) is spread [26][27].

An interesting effect of the large amount of Coulombic scattering at the interface is that the peak of the current density curve occurs some distance away from the interface [26][27]. Even though the electron concentration is highest at the interface, due to the very low surface mobility, most of the current in a 4H-SiC MOSFET flows a few nanometers away from the interface. As gate voltage increases, more electrons are pulled closer to the interface and screening increases, and hence the peak of the current density shifts towards the interface. This is shown in Fig. 1.3.

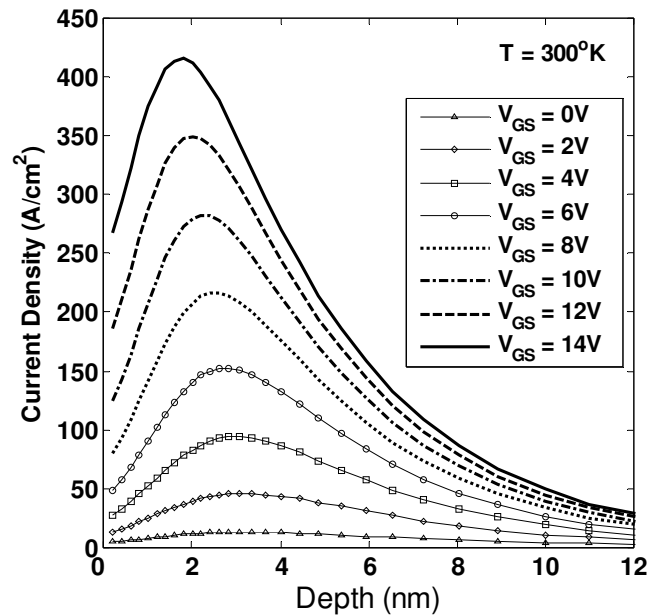


Fig. 1.3 Current density variation with depth for a 4H-SiC MOSFET at room temperature. Because of the extremely low mobility near the surface, the maximum current does not flow at the surface, but some distance below it [26] [27].

We also extracted the density of states for the interface traps (D_{it}) by comparing simulated I_D - V_{GS} curves to experiment as shown in Fig. 1.4. This interface trap density is for a Nov 2004 4H-SiC MOSFET sample. The extremely large values of D_{it} seen here are responsible for low currents and low surface mobilities ($<15\text{cm}^2/\text{Vs}$) in the 4H-SiC MOSFET.

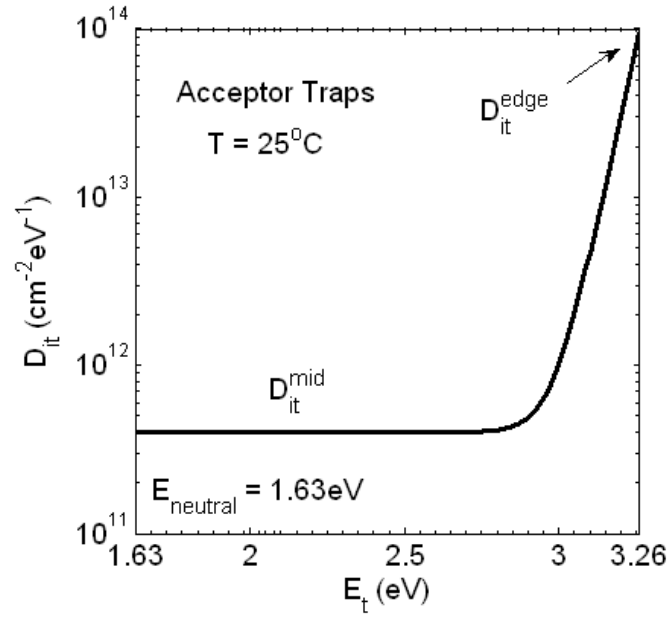


Fig. 1.4 Interface trap density of states for 4H-SiC MOSFET. $D_{it}^{edge} = 9.5 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$
 $D_{it}^{mid} = 4.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ [26][27]

1.5. Device Modeling

The Drift Diffusion equations serve as the basic building blocks for semiconductor device modeling. These equations are derived from the Boltzmann transport equation by doing certain approximations. The drift diffusion equations consist of the Poisson's equation, the electron and hole current equations, and the current continuity equations for electrons and holes. In this section, we describe these equations in brief and then elaborate on the numerical methodology that is implemented to solve them for a SiC MOSFET.

1.5.1. Drift Diffusion Model Equations

Poisson Equation: The Poisson equation governs the behavior of the electrostatics in the semiconductor device. It relates the electrostatic potential (ϕ), to the net charge density inside the semiconductor. The charge inside the semiconductor is made up of negatively charged electrons (n), positively charged holes (p), and ionized dopants (N_D^+ , N_A^-). The Poisson equation can be written as

$$\vec{\nabla} \cdot (\boldsymbol{\varepsilon} \vec{\nabla} \phi) = -q(-n + p + N_D^+ - N_A^-) \quad (1.1)$$

Here, $\boldsymbol{\varepsilon}$ is the permittivity of the medium.

Current Equations: Current flowing inside a semiconductor is made up of two components. The drift component arises due to the flow of electrons (or holes) in presence of an electric field. The diffusion component of current is due to the flow of electrons (or holes) from a region of higher concentration to a region of lower concentration. Thus, the diffusion current depends on the concentration gradient of

electrons and holes. The total electron (and hole) current is a combination of the drift and diffusion currents, and is given as

$$\vec{J}_n = -qn\mu_n\vec{\nabla}\phi + qD_n\vec{\nabla}n \quad (1.2)$$

$$\vec{J}_p = -qp\mu_p\vec{\nabla}\phi - qD_p\vec{\nabla}p \quad (1.3)$$

Here, μ_n and μ_p are the electron and hole mobilities, and D_n and D_p are the electron and hole diffusion constants. The diffusion constants are related to the mobilities by the Einstein relations given by

$$D_n = \mu_n \frac{k_B T}{q} \quad (1.4)$$

$$D_p = \mu_p \frac{k_B T}{q} \quad (1.5)$$

Current Continuity Equations: The continuity equations are based on the conservation of mobile charge. They relate the change in mobile charge concentration in time to the gradient of the current density, and the rates of generation and recombination of carriers. The continuity equations for electrons and holes are written as,

$$\frac{\partial n}{\partial t} = \frac{1}{q} \vec{\nabla} \cdot \vec{J}_n - R_n + G_n \quad (1.6)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \vec{\nabla} \cdot \vec{J}_p - R_p + G_p \quad (1.7)$$

Here G_n and G_p are the electron and hole generation rates, R_n and R_p are the electron and hole recombination rates, and $\vec{\nabla} \cdot \vec{J}_n$ and $\vec{\nabla} \cdot \vec{J}_p$ are the net flux of electrons and holes in and out of the specific volume. The current continuity equations state that the total current flow into or out of a volume of space is equal to the time varying charge

density within that volume plus any additions due to generation or recombination that may occur.

The electron and hole concentrations can be written in terms of the electron and hole quasi Fermi levels (ϕ_n and ϕ_p) as

$$n = n_i \exp\left(\frac{\phi - \phi_n}{V_T}\right) \quad (1.8)$$

$$p = n_i \exp\left(-\frac{\phi - \phi_p}{V_T}\right) \quad (1.9)$$

Here, ϕ is the electrostatic potential, n_i is the intrinsic carrier concentration and V_T is the thermal voltage.

The advantage of writing electron and hole concentrations in terms of the quasi-Fermi levels is that we can directly solve for ϕ_n and ϕ_p to obtain values for n and p . The range of ϕ_n and ϕ_p is the same as that of the electrostatic potential ϕ . This allows for better convergence in the numerical solvers. We show the discretization of the semiconductor equations in n and p further in this chapter; but while solving the discretized set of equations using the Gummel or the Newton's methods described later on, we always solve for ϕ_n and ϕ_p .

1.5.2. Important Parameters of the Drift Diffusion Model

We solve the Drift Diffusion equations everywhere inside the device for the electrostatic potential (ϕ), electron concentration (n) and hole concentration (p). To characterize the performance of a semiconductor device, we need to include the relevant physical mechanisms that govern transport in the device. The physical transport models

are incorporated as the mobility models for electrons and holes (μ_n and μ_p) and generation-recombination models. For 4H-SiC MOSFETs, charge at the SiC-SiO₂ interface is also a very important and critical physical parameter.

Mobility: We incorporate detailed models for electron and hole mobility in 4H-SiC MOSFETs in to our device simulator. We consider bulk phonon scattering (μ_B), impurity scattering in the bulk, surface phonon scattering (μ_{SP}), Coulombic scattering from interface traps (μ_C), and surface roughness scattering (μ_{SR}) while devising our comprehensive mobility models for 4H-SiC MOSFETs. The details of these models are given in Chapter 2. The different mobility mechanisms are summed up using Matheissen’s rule as

$$\frac{1}{\mu_{Total}} = \frac{1}{\mu_B} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} \quad (1.10)$$

Using a combination of device modeling and experimental I-V measurement, we can extract physical parameters governing the different mobility mechanisms in 4H-SiC MOSFETs. We develop the mobility models from basic physics with as few empirical parameters as possible. We then calibrate our simulated I-V characteristics to experimental data over a wide range of biases and temperatures to extract the values of the physical parameters. This gives us thorough understanding of the mobility mechanisms governing transport in 4H-SiC MOSFETs.

Generation and Recombination: Various mechanisms for generation and recombination are also incorporated into our device simulator. We include Shockley-

Reed-Hall recombination due to trap centers, Auger recombination due to direct particle recombination, and a new generation-recombination mechanism involving interface traps and inversion layer electrons which will be discussed in more detail in Chapter 3.

Impact ionization related generation is also included in our 4H-SiC MOSFET device simulator. This generation mechanism is important to characterize breakdown of the 4H-SiC power DMOSFET. More details about impact ionization breakdown and the associated generation model are given in Chapter 4.

Shockley-Reed-Hall (SRH) Recombination: The capture and emission of holes and electrons by traps that reside in the mid-band energy zone is modeled using the well known Shockley-Read-Hall (SRH) mechanism of recombination. The SRH recombination rate is given by

$$(G - R)^{SRH} = \frac{np - n_i^2}{\tau_p(n + n_i) + \tau_n(p + n_i)} \quad (1.11)$$

where, τ_n and τ_p are the minority carrier lifetimes of electrons and holes respectively. The minority carrier lifetimes for SiC are in order of a few hundred nanoseconds.

For a n -doped SiC slab, when there is a current flowing through the device, the electron concentration is much higher than the hole concentration ($n \gg p$). If the carrier lifetimes of electrons and holes are taken to be equal ($\tau_n \approx \tau_p$), then the SRH recombination rate can be rewritten as

$$(G - R)^{SRH} \approx \frac{np}{\tau_p n} = \frac{p}{\tau_p} \quad (1.12)$$

At room temperature, the intrinsic carrier concentration of 4H-SiC is around $2 \times 10^{-8} \text{ cm}^{-3}$. For a slab of SiC doped with n -type impurity of the order of 10^{18} donor atoms per cubic centimeters, at room temperature, the hole concentration is going to be around $(10^{-8})^2/10^{18}$ which is approximately 10^{-30} cm^{-3} . Hence, it is easy to see that the SRH recombination rate in SiC is going to be very small (around $10^{-20} \text{ cm}^{-3}/\text{s}$).

Auger Recombination: SiC is an indirect bandgap semiconductor. Therefore, the probability of a direct band-to-band recombination by transfer of energy to another carrier is very small. Hence, this recombination mechanism, known as the Auger recombination is rare in SiC devices. In the direct recombination process, a free electron in the conduction band combines with a free hole in the valence band, and the net momentum of the two particle system is carried off by a third free particle, which can be an electron or a hole. The Auger recombination rate is given by

$$(G - R)^{Auger} = (np - n_i^2)(C_n n + C_p p) \quad (1.13)$$

where, C_n and C_p are the coefficients representing interactions in which the remaining carrier is an electron and a hole respectively.

1.5.3. Boundary Conditions

In order to solve the coupled partial differential equations comprising the drift diffusion system of equations, a proper methodology has to be followed. The equations are solved for 2D structure, which is a section cut parallel to the channel of the MOSFET.

These equations are solved for the electrostatic potential (ϕ), the electron concentration (n) and the hole concentration (p) at discrete mesh points inside the device, in the source, drain, bulk and the oxide regions. Appropriate boundary conditions for ϕ , n and p , based on the applied voltages at the various regions, are built in to the system.

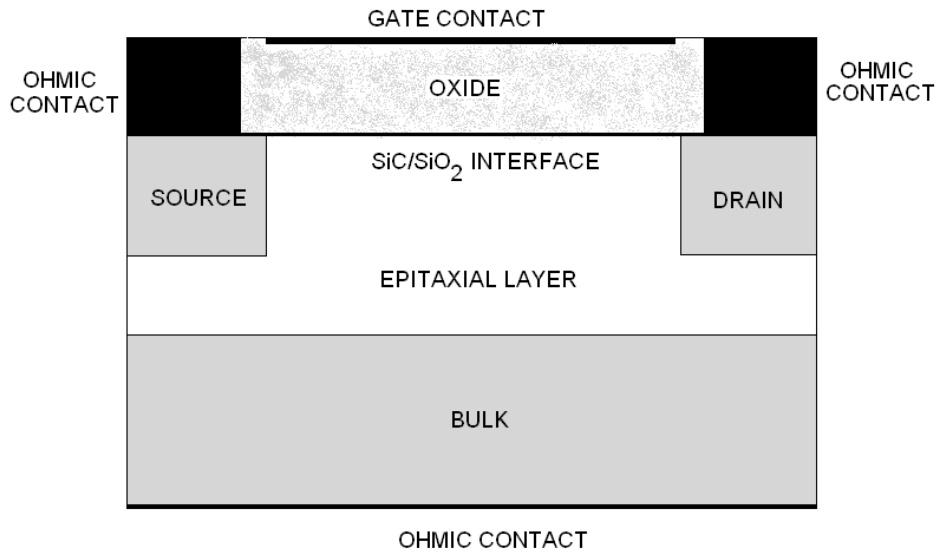


Fig. 1.5 Structure of a 4H-SiC lateral MOSFET.

The MOSFET device structure is shown in Fig. 1.5. It is divided into the source, drain, bulk, oxide and interface regions, where the semiconductor equations are to be solved. The boundary regions are the regions where external voltage is applied or an artificial boundary is created.

Ohmic Contacts: The source, bulk and drain contacts are modeled as Ohmic contacts. The boundary condition for the electrostatic potential is therefore given by

$$\phi_{Contact} = V_{Contact} + \phi_n \quad (1.14)$$

for Ohmic contacts on n -type material and

$$\phi_{Contact} = V_{Contact} + \phi_p \quad (1.15)$$

for Ohmic contact on p -type material.

Here, ϕ_n and ϕ_p are the built in potentials for n -type and p -type semiconductors in thermal equilibrium. For an n -type material with a doping of N_D^+ , and a p -type semiconductor doped to N_A^- , the built in potentials respectively are

$$\phi_n = V_T \ln \frac{N_D^+}{n_i} \quad (1.16) \quad \text{and} \quad \phi_p = -V_T \ln \frac{N_A^-}{n_i} \quad (1.17)$$

where, n_i is the intrinsic carrier concentration at temperature T and V_T is the thermal voltage.

Since we are at thermal equilibrium, $np = n_i^2$. Hence, for a n -type semiconductor with a doping of N_D at the Ohmic contact,

$$p = \frac{n_i^2}{n} \quad (1.18) \quad \text{and} \quad n = \frac{N_D}{2} + \frac{\sqrt{N_D^2 + 4n_i^2}}{2} \quad (1.19)$$

Similarly, for a p -type semiconductor region doped to N_A at the Ohmic contact,

$$n = \frac{n_i^2}{p} \quad (1.20) \quad \text{and} \quad p = \frac{-N_A}{2} + \frac{\sqrt{N_A^2 + 4n_i^2}}{2} \quad (1.21)$$

Gate Contact: There are no mobile charge carriers inside the gate oxide. Hence, only the Poisson's equation is solved inside the oxide with the charge density taken as zero. The semiconductor equations are not solved for n and p inside the oxide; hence no boundary conditions are needed for n and p at the gate contact. The boundary condition for the electrostatic potential on the gate contact is defined as

$$\phi_{Gate} = V_G + VGB \quad (1.22)$$

V_G is the applied gate voltage and VGB is the built-in gate voltage. It is equal to the metal-semiconductor work function difference between the gate metal and the semiconductor epi-layer of the 4H-SiC MOSFET.

Artificial Boundaries: Artificial boundaries consist of all boundaries in which the device structure ceases to exist for simulation purposes, but in reality, this boundary may not exist on the device physically. The artificial boundaries are placed far enough away from the carrier transport activity where the change in electrostatic potential, electron concentration and hole concentration, across the boundary, is negligible. At the artificial boundaries, we have the conditions

$$\frac{\partial \phi}{\partial N} = \frac{\partial n}{\partial N} = \frac{\partial p}{\partial N} = 0 \quad (1.23)$$

where $\frac{\partial}{\partial N}$ is the derivative taken in the direction normal to the artificial boundary.

1.5.4. Discretized Drift-Diffusion Equations

The Drift-Diffusion system of equations is discretized in space and time using a finite difference methodology. The Poisson's equation is solved inside the semiconductor and the oxide, whereas the current continuity equations are solved only inside the semiconductor. At the semiconductor-oxide interface, the Gauss's law is implemented in order to solve for the electrostatic potential.

Each equation is discretized in two dimensions using the finite difference method where each position, (x, y) , in the device is mapped to a mesh point, (i, j) . The position of x , at the i^{th} mesh line is designated by the notation x_i ; likewise, the position of y , at the j^{th} mesh line is designated by the notation y_j . If needed, additional points can be defined as lying between two consecutive mesh points. These points are designated by $\left(i \pm \frac{1}{2}, j\right)$ or $\left(i, j \pm \frac{1}{2}\right)$. The distance between two mesh points are designated by the variables h_i and k_j .

$$h_i = x_{i+1} - x_i \quad (1.24)$$

$$k_j = y_{j+1} - y_j \quad (1.25)$$

Poisson Equation: The Poisson equation gives an analytical representation of the relationship between electrostatic potential (ϕ) and the net charge distribution.

Semiconductor-Insulator Interface: At the semiconductor-oxide interface, it is assumed that there are no free electrons and holes, and that the difference in the electric displacement vectors in the insulator and the semiconductor is equal to the effective surface charge.

$$\hat{a}_{surf} \cdot (\vec{D}_i - \vec{D}_s) = Q_{surf} \quad (1.26)$$

where, \vec{D} is the electric displacement vector and Q_{surf} is the effective surface charge density at the semiconductor-oxide interface, and \hat{a}_{surf} is a unit vector in the direction of the semiconductor-oxide interface. This equation can be rewritten in form of Gauss's law by writing the electric fields at the semiconductor-oxide interface.

$$\epsilon_{ox} E_{ox} - \epsilon_s E_s = Q_{surf} \quad (1.27)$$

Here, the electric fields are the fields perpendicular to the interface. Writing them using the electrostatic potentials, we have

$$\epsilon_{ox} \left(-\frac{\partial \phi}{\partial y} \right)_{ox} - \epsilon_s \left(-\frac{\partial \phi}{\partial y} \right)_s = Q_{surf} \quad (1.28)$$

Writing the discretized forms of the first order derivatives we have the equation for the electrostatic potential at the interface.

$$F_{i,j_{ox}}^\phi = \phi_{i,j_{ox}+1} \left(\frac{\epsilon_s}{k_{j_{ox}}} \right) + \phi_{i,j_{ox}-1} \left(\frac{\epsilon_{ox}}{k_{j_{ox}-1}} \right) - \phi_{i,j_{ox}} \left(\frac{\epsilon_s}{k_{j_{ox}}} + \frac{\epsilon_{ox}}{k_{j_{ox}-1}} \right) + Q_{surf} = 0 \quad (1.29)$$

where, j_{ox} represents the mesh-line j which defines the interface. Q_{surf} is the net effective surface charge at the mesh-point (i, j_{ox}) . It is the sum of the fixed oxide charge and the interface trapped charge at that mesh-point.

Inside the Oxide: There is no charge present inside the oxide. Hence, the Poisson's equation will look like a simple Laplacian.

$$\nabla^2 \phi = 0 \quad (1.30)$$

Finite difference discretization of the above equation has the following form.

$$F_{i,j}^\phi = \frac{\phi_{i+1,j}}{h_1^2} + \frac{\phi_{i-1,j}}{h_2^2} + \frac{\phi_{i,j+1}}{k_1^2} + \frac{\phi_{i,j-1}}{k_2^2} - \phi_{i,j} \left(\frac{1}{h_1^2} + \frac{1}{h_2^2} + \frac{1}{k_1^2} + \frac{1}{k_2^2} \right) = 0 \quad (1.31)$$

where,

$$h_1^2 = \frac{h_i(h_i + h_{i-1})}{2}, h_2^2 = \frac{h_{i-1}(h_i + h_{i-1})}{2}, k_1^2 = \frac{k_j(k_j + k_{j-1})}{2}, k_2^2 = \frac{k_{j-1}(k_j + k_{j-1})}{2} \quad (1.32)$$

Inside the Semiconductor: Rewriting the Poisson's equation inside the semiconductor,

$$\nabla^2 \phi_{i,j} = -\frac{q}{\epsilon_s} \left(-n_{i,j} \exp\left(\frac{\phi_{i,j} - \phi_{n_{i,j}}}{V_{T_{i,j}}}\right) + n_{i,j} \exp\left(-\frac{\phi_{i,j} - \phi_{p_{i,j}}}{V_{T_{i,j}}}\right) + D_{i,j} \right) \quad (1.33)$$

Finite difference discretization of the above equation has the following form.

$$F_{i,j}^\phi = \frac{\phi_{i+1,j}}{h_1^2} + \frac{\phi_{i-1,j}}{h_2^2} + \frac{\phi_{i,j+1}}{k_1^2} + \frac{\phi_{i,j-1}}{k_2^2} - \phi_{i,j} \left(\frac{1}{h_1^2} + \frac{1}{h_2^2} + \frac{1}{k_1^2} + \frac{1}{k_2^2} \right) + \frac{q}{\epsilon_s} \left(-n_{i,j} \exp\left(\frac{\phi_{i,j} - \phi_{n_{i,j}}}{V_{T_{i,j}}}\right) + n_{i,j} \exp\left(-\frac{\phi_{i,j} - \phi_{p_{i,j}}}{V_{T_{i,j}}}\right) + D_{i,j} \right) = 0 \quad (1.34)$$

Steady State Electron Current Continuity Equations: The steady state electron and hole current continuity equations are solved at all mesh-points inside the semiconductor. They are discretized by the Scharfetter-Gummel scheme [28]. The temperature term in the equation is modeled as a local temperature $T_{i,j}$. If the drift diffusion equations are coupled with the heat flow equation, then we would be able to extract the heat characteristics of the device. We have not used the heat flow equation in my simulations, so the local temperature is in effect constant, and is equal to the operating temperature of the device. The Scharfetter-Gummel discretization of the steady state electron current continuity equation is given as

$$\begin{aligned}
F_{i,j}^n &= \beta(\alpha_{i+\frac{1}{2}}) \frac{\mu_{n_{i+\frac{1}{2},j}} V_{T_{i+1,j}} n_{i+1,j}}{h_1^2} + \beta(-\alpha_{i-\frac{1}{2}}) \frac{\mu_{n_{i-\frac{1}{2},j}} V_{T_{i-1,j}} n_{i-1,j}}{h_2^2} \\
&+ \beta(\alpha_{j+\frac{1}{2}}) \frac{\mu_{n_{i,j+\frac{1}{2}}} V_{T_{i,j+1}} n_{i,j+1}}{k_1^2} + \beta(-\alpha_{j-\frac{1}{2}}) \frac{\mu_{n_{i,j-\frac{1}{2}}} V_{T_{i,j-1}} n_{i,j-1}}{k_2^2} - (R_{i,j} - G_{i,j}) \\
&- n_{i,j} V_{T_{i,j}} \left[\beta(-\alpha_{i+\frac{1}{2}}) \frac{\mu_{n_{i+\frac{1}{2},j}}}{h_1^2} + \beta(\alpha_{i-\frac{1}{2}}) \frac{\mu_{n_{i-\frac{1}{2},j}}}{h_2^2} + \beta(-\alpha_{j+\frac{1}{2}}) \frac{\mu_{n_{i,j+\frac{1}{2}}}}{k_1^2} + \beta(\alpha_{j-\frac{1}{2}}) \frac{\mu_{n_{i,j-\frac{1}{2}}}}{k_2^2} \right] \\
&= 0
\end{aligned} \tag{1.35}$$

$n_{i,j}$ is the electron concentration at mesh-point (i, j) . $\beta(\gamma)$ is the Bernoulli function defined as

$$\beta(\gamma) = \frac{\gamma}{\exp(\gamma) - 1} \tag{1.36}$$

and,

$$\alpha_{i+\frac{1}{2}} = \frac{\phi_{i+1,j} - \phi_{i,j}}{V_{T_{i,j}}}, \alpha_{i-\frac{1}{2}} = \frac{\phi_{i,j} - \phi_{i-1,j}}{V_{T_{i,j}}}, \alpha_{j+\frac{1}{2}} = \frac{\phi_{i,j+1} - \phi_{i,j}}{V_{T_{i,j}}}, \alpha_{j-\frac{1}{2}} = \frac{\phi_{i,j} - \phi_{i,j-1}}{V_{T_{i,j}}} \tag{1.37}$$

The mobility terms in the above equation are written as,

$$\mu_{n_{i\pm\frac{1}{2},j}} = \frac{\mu_{n_{xi\pm 1,j}} + \mu_{n_{xi,j}}}{2} \text{ and } \mu_{n_{i,j\pm\frac{1}{2}}} = \frac{\mu_{n_{yi,j\pm 1}} + \mu_{n_{yi,j}}}{2} \tag{1.38}$$

Here, $\mu_{n_{xi,j}}$ and $\mu_{n_{yi,j}}$ stand for the x -direction and the y -direction electron mobility respectively, at mesh-point (i, j)

Steady State Hole Current Continuity Equations: The hole current continuity equation can be discretized the same way as the electron current continuity equation.

$$\begin{aligned}
F_{i,j}^p &= \beta\left(-\alpha_{i+\frac{1}{2}}\right) \frac{\mu_{p_{i+\frac{1}{2},j}} V_{T_{i+1,j}} p_{i+1,j}}{h_1^2} + \beta\left(\alpha_{i-\frac{1}{2}}\right) \frac{\mu_{p_{i-\frac{1}{2},j}} V_{T_{i-1,j}} p_{i-1,j}}{h_2^2} \\
&+ \beta\left(-\alpha_{j+\frac{1}{2}}\right) \frac{\mu_{p_{i,j+\frac{1}{2}}} V_{T_{i,j+1}} p_{i,j+1}}{k_1^2} + \beta\left(\alpha_{j-\frac{1}{2}}\right) \frac{\mu_{p_{i,j-\frac{1}{2}}} V_{T_{i,j-1}} p_{i,j-1}}{k_2^2} + (R_{i,j}^p - G_{i,j}) \\
&- p_{i,j} V_{T_{i,j}} \left[\beta\left(\alpha_{i+\frac{1}{2}}\right) \frac{\mu_{p_{i+\frac{1}{2},j}}}{h_1^2} + \beta\left(-\alpha_{i-\frac{1}{2}}\right) \frac{\mu_{p_{i-\frac{1}{2},j}}}{h_2^2} + \beta\left(\alpha_{j+\frac{1}{2}}\right) \frac{\mu_{p_{i,j+\frac{1}{2}}}}{k_1^2} + \beta\left(-\alpha_{j-\frac{1}{2}}\right) \frac{\mu_{p_{i,j-\frac{1}{2}}}}{k_2^2} \right] \\
&= 0
\end{aligned} \tag{1.39}$$

The mobility terms in the above equation are written as,

$$\mu_{p_{i\pm\frac{1}{2},j}} = \frac{\mu_{p_{xi\pm 1,j}} + \mu_{p_{xi,j}}}{2} \quad \text{and} \quad \mu_{p_{i,j\pm\frac{1}{2}}} = \frac{\mu_{p_{yi,j\pm 1}} + \mu_{p_{yi,j}}}{2} \tag{1.40}$$

Here, $\mu_{p_{xi,j}}$ and $\mu_{p_{yi,j}}$ stand for the x -direction and the y -direction hole mobility respectively, at mesh-point (i, j)

1.5.5. Numerical Methods

There are two numerical methods that are used to solve the set of discretized equations. The first method is an iterative Gummel Iterative method which starts with an initial guess for ϕ , ϕ_n and ϕ_p , at all mesh-points inside the device and solves the three equations consecutively, to get to a solution. This solution acts like the initial guess for the next solver, which is the Newton solver. The Newton solver solves for all three variables ϕ , ϕ_n and ϕ_p at all mesh-points simultaneously, using the Gauss-Newton Algorithm.

Gummel Iterative Method: The Poisson, electron current continuity, and the hole current continuity equations are solved for the electrostatic potential (ϕ), electron

quasi-Fermi level (ϕ_n), and the hole quasi-Fermi level (ϕ_p), respectively, one after the other, using an iterative solver.

First, the discretized Poisson's equation is solved for ϕ at all points in the mesh using an iterative method. In this case, ϕ_n and ϕ_p are kept constant. Next, using the new ϕ calculated over the mesh, the discretized electron current continuity equation is solved for ϕ_n over the mesh. In this case, ϕ and ϕ_p are not allowed to change. Finally, using the new ϕ and ϕ_n values, the hole current continuity equation is solved at all mesh points and the new ϕ_p is obtained.

The discretized finite-difference equations are solved using the iterative Gauss-Seidel method. Here, as an example, we show how the solution for ϕ is obtained iteratively. The discretized Poisson's equation is arranged in the form

$$f_\phi(\phi^k, \phi_n, \phi_p) = 0 \quad (1.41)$$

where, k denotes the current iteration. The solver begins with an initial guess for ϕ at all mesh points in the device. According to Newton's method for solving nonlinear equations, we can write

$$f_\phi(\phi^{k+1}, \phi_n, \phi_p) = f_\phi(\phi^k, \phi_n, \phi_p) + \Delta\phi^k \cdot \left(\frac{\partial f_\phi}{\partial \phi} \right)^k = 0 \quad (1.42)$$

Hence, we have,

$$\Delta\phi^k = \frac{-(f_\phi)^k}{\left(\frac{\partial f_\phi}{\partial \phi} \right)^k} \quad (1.43) \quad \text{and} \quad \phi^{k+1} = \phi^k + \Delta\phi^k \quad (1.44)$$

Here, $\phi = \phi_{i,j}$ = electrostatic potential at the mesh point (i, j). The iterations continue till the error $\Delta\phi^k$ falls below a prescribed error criterion. Once convergence is

reached for the electrostatic potential, a similar method is used to solve for the electron quasi-Fermi level (ϕ_n) and then for the hole quasi-Fermi level (ϕ_p). Once we have convergence for all three, we switch to the faster Newton's method.

Newton Method: Unlike the Block Gummel Method, the drift-diffusion equations remain coupled in this method. So ϕ , ϕ_n and ϕ_p are computed simultaneously. This is accomplished by defining a Jacobian matrix and solving for the changes in the three variables between iterations. This process is represented as matrix equation as

$$\begin{bmatrix} \frac{\partial F_{\phi}^k}{\partial \bar{\phi}} & \frac{\partial F_{\phi}^k}{\partial \bar{\phi}_n} & \frac{\partial F_{\phi}^k}{\partial \bar{\phi}_p} \\ \frac{\partial F_{\phi_n}^k}{\partial \bar{\phi}} & \frac{\partial F_{\phi_n}^k}{\partial \bar{\phi}_n} & \frac{\partial F_{\phi_n}^k}{\partial \bar{\phi}_p} \\ \frac{\partial F_{\phi_p}^k}{\partial \bar{\phi}} & \frac{\partial F_{\phi_p}^k}{\partial \bar{\phi}_n} & \frac{\partial F_{\phi_p}^k}{\partial \bar{\phi}_p} \end{bmatrix} \begin{bmatrix} \Delta \bar{\phi}^{\rightarrow k} \\ \Delta \bar{\phi}_n^{\rightarrow k} \\ \Delta \bar{\phi}_p^{\rightarrow k} \end{bmatrix} = - \begin{bmatrix} F_{\phi}^k \\ F_{\phi_n}^k \\ F_{\phi_p}^k \end{bmatrix} \quad (1.45)$$

where, the vectors $\bar{\phi}, \bar{\phi}_n, \bar{\phi}_p$ signify that the matrix operation is performed for all non-boundary mesh points of the variables ϕ , ϕ_n and ϕ_p . Once the above matrix equation is solved, the new values for ϕ , ϕ_n and ϕ_p are obtained as

$$\phi^{k+1} = \phi^k + \Delta \phi^k, \quad \phi_n^{k+1} = \phi_n^k + \Delta \phi_n^k \quad \text{and} \quad \phi_p^{k+1} = \phi_p^k + \Delta \phi_p^k \quad (1.46)$$

F_{ϕ}, F_{ϕ_n} and F_{ϕ_p} are the discretized Poisson, electron continuity and hole continuity equations of the Drift-Diffusion system.

The Newton solver is allowed to iterate till it reaches the specified convergence condition for all three variables. Then the current is calculated inside the channel, at the drain contact, at the source contact and at the substrate contact. If the current is

continuous across the device, then the simulation is proper and all relevant data is stored in various files. A simple flowchart for the simulator is shown in Fig. 1.6.

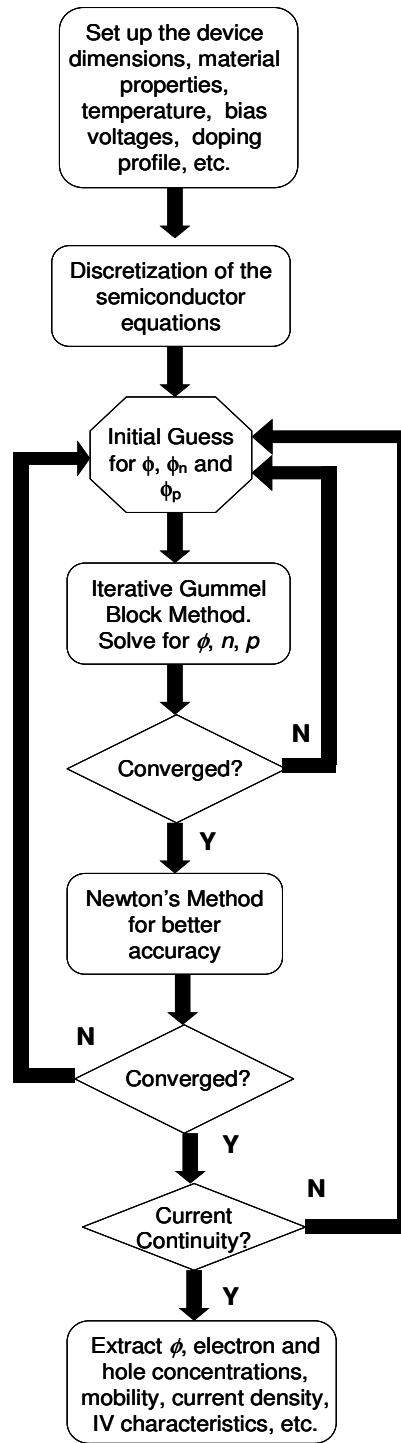


Fig. 1.6 Flowchart for solving the drift-diffusion semiconductor equation system

1.5.6. 2D Mesh

A 2D non-uniform mesh has been created for discretizing the drift-diffusion equations for the MOSFET structure. The mesh is very fine near the drain and the source junctions where there is rapid change in potential and charge concentration. Whereas, near the center of the device, the mesh is coarse as there is not much variation in these physical quantities there. In order to capture the physics of the inversion layer, the mesh is kept very fine near the interface. The mesh spacing is kept as low as 2\AA near the interface. This enables us to extract detailed physics of the inversion layer. For example, we can extract mobility variations as a function of depth near the interface, or the current density variation as a function of depth in a 4H-SiC MOSFET. The mesh is carefully crafted so that the electrostatic potential does not vary by more than the thermal voltage between adjacent mesh points.

1.6. Thesis Outline

The rest of the thesis is dedicated to the discussion of the above mentioned research goals.

The various aspects of developing high temperature models for 4H-SiC MOSFETs will be discussed in Chapter 2. The models for interface trap density of states, Coulomb scattering, Surface Roughness Scattering, etc. will be discussed in detail. Simulation and experimental results will be compared for extracting the model parameters. Details regarding the physics of transport in these devices with emphasis on channel mobility will be part of this chapter. Quantum confinement in the channel and its effect on interface trap occupation will also be discussed in this chapter. The chapter ends with a discussion on variability in current SiC MOS devices as understood by SPICE parameter extraction.

In Chapter 3, the dynamic response of 4H-SiC MOSFETs will be discussed. We will derive a robust generation-recombination methodology describing interaction between interface trap states and surface electrons, and use it to derive the time dependent occupation of interface traps. The experimental setup and measurement technique used to corroborate simulations, and to extract “effective” capture cross-sections of the interface, near-interface and oxide traps will also be discussed.

Chapter 4 deals with the modeling of the transport in 4H-SiC power DMOSFETs. ON state and OFF state characteristics are derived and model parameters are extracted by comparison to experiment. Turn ON resistance is quantified and the role of channel resistance in the behavior of these devices is explained. Further, modeling the breakdown characteristics is discussed near the end of the chapter.

Chapter 5 summarizes the research work and focuses on the important physical phenomenon controlling transport in 4H-SiC MOSFETs.

Chapter 2

2. High Temperature Modeling and Characterization of 4H-Silicon Carbide MOSFETs

Typical proposed operating temperatures for SiC devices is from 25°C to well beyond 400°C. This makes the characterization of the behavior of SiC devices at elevated temperatures absolutely essential. We build on our previous work by developing temperature dependent models for characterizing the working of SiC MOSFETs at high temperatures. We extract the physics of the interface trap distribution at high temperatures by comparing simulations to experiment. We observe a spreading of the interface trap density of states near the conduction band edge with increase in temperature. This coupled with the reduction in trap occupation probability at high temperatures gives a complex relationship of occupied trap density and temperature. We see an increase in current with temperature for 4H-SiC MOSFETs. A rigorous surface roughness mobility model is developed which incorporates the effects of step flow growth process of growing SiC wafers. We also estimate the saturation velocity of electrons in the inversion layer and its change with temperature.

In the later part of the chapter we discuss modeling the quantum effects in the MOSFET channel using a Density-Gradient modeling approach. We see that due to the large oxide thickness (50nm), quantization does not have a significant effect on transport in current SiC MOSFETs.

Finally we introduce a methodology for extraction of SPICE parameters for 4H-SiC MOSFETs. Details regarding parameter extraction and variation in key parameters across devices on a single wafer are presented.

2.1. Interface Traps and the effect of Temperature

Interface traps density of states inside the 4H-SiC semiconductor bandgap is modeled as consisting of two parts. The trap states in the middle of the bandgap that have a constant density with energy; and the traps near the band edges that are modeled as the tail end states of some trap(s) lying in the conduction band (and/or valence band). These band-tail states are very large in number generating the huge number of occupied traps at the interface. They are therefore responsible for the detrimental effects observed in SiC MOSFETs.

The density of interface traps for acceptor type traps that are located in the upper half of the bandgap can be written as -

$$D_{it}(E_t, T) = D_{it}^{mid} + D_{it}^{edge}(T) \exp\left(\frac{E_t - E_C}{\sigma(T)}\right) \quad (2.1)$$

Where, E_t are the energy trap levels inside the bandgap, E_C is the conduction band energy, D_{it}^{mid} is the density of states for the traps located near the middle of the bandgap, $D_{it}^{edge}(T)$ is the density of states for traps at the conduction band edge, and $\sigma(T)$ is the temperature dependent band tail energy parameter that governs the distribution of the states close to the band edge. A similar expression can also be written for the donor states located in the lower half of the bandgap.

The number of occupied traps depends upon the location of the Fermi level at the interface, and hence is dependent on the applied gate voltage. We can write the probability of occupation of the interface states as

$$f_t(E_t) = \frac{1}{1 + \frac{1}{2} \exp\left(\frac{E_t - E_F}{k_B T}\right)} \quad (2.2)$$

E_F is the Fermi level at the interface. The $\frac{1}{2}$ term is included to account for the double degeneracy in trap occupation. The density of occupied acceptor-like interface traps is given by [26]

$$N_{it}^{acc} = \int_{E_{neutral}}^{E_c} D_{it}(E_t) f_t(E_t) dE_t \quad (2.3)$$

Where, $E_{neutral}$ is the neutrality point. We take the neutrality point to be the center of the bandgap. The values for D_{it}^{mid} , $D_{it}^{edge}(T)$ and $\sigma(T)$ are estimated by comparing the simulated I-V curves at various temperatures to experimental data.

In the subthreshold and near-threshold regions of n -MOSFET operation, the electron Fermi level is closer to the center of the bandgap. Because of this, the interface traps in the midgap region of the 4H-SiC bandgap become occupied. Therefore, comparisons of the simulated subthreshold and near threshold I_D - V_G characteristics of the device with experimental data give us an estimate of the midgap density of states of the interface traps. Fitting the subthreshold region of the I_D - V_G curve also enables us to estimate the value of the band tail energy. Above threshold, in deep inversion, the electron Fermi energy is closer to the conduction band-edge, causing traps at energies closer to the band-edge to be occupied. Thus, we can extract the density of states of traps near the band-edge by comparing the simulated and measured I_D - V_G characteristics in the linear region.

Our results show a trend of spreading of the density of states near the edge of the bandgap with rise in temperature. We believe that as temperature increases, the tail of the

density of states for the trap(s) located in the conduction band (valence band in case of donor states) will spread deeper into the bandgap. This is reflected as an increase in the value of bandtail energy σ in the density of states equation for interface traps. While our extracted values portray a temperature dependence of interface trap density in SiC, there has been little direct experimental evidence for this in the literature. However, temperature variation of trap densities has been deduced for a Si–SiO₂ system [35], which is similar to what we extracted for SiC. Increase in temperature does not have any significant effect in the midgap densities (D_{it}^{mid}) and their value remains constant. Furthermore, increase in temperature also causes bandgap narrowing causing the conduction band edge to move closer to the valence band. As a result there is a reduction in the value of the band-edge density of states (D_{it}^{edge}) with rise in temperature.

With increase in temperature, the probability of occupation of the interface traps decreases. This would cause a net reduction in the occupied interface trap density. This gives us an effectively higher mobile inversion charge in the MOSFET. Also, the Coulomb scattering at the interface is reduced leading to a net increase in surface mobility. These two effects in combination cause SiC MOSFET current to increase with temperature.

2.2. High Temperature Mobility Models

We have developed and implemented mobility models representing various scattering phenomenon for 4H-SiC MOSFETs. These models have been developed for low and high temperatures. At low temperatures, Coulomb scattering and surface roughness scattering are the two dominant scattering mechanisms governing the total current in low lateral field conditions. As temperature increases, Coulomb scattering will become less important, and other scattering mechanisms like surface phonon and bulk phonon scattering may become the dominant ones. For high lateral fields, we employ a velocity saturation model to calculate the high field mobility.

The total mobility in the channel of a 4H-SiC MOSFET will be a net result of the contributions of all these different mobility mechanisms. The different scattering rates can be summed together to give the total scattering rate inside the semiconductor.

$$\left(\frac{1}{\tau}\right)_{Total} = \left(\frac{1}{\tau}\right)_{Bulk} + \left(\frac{1}{\tau}\right)_{SP} + \left(\frac{1}{\tau}\right)_{C} + \left(\frac{1}{\tau}\right)_{SR} \quad (2.4)$$

As mobility is inversely proportional to the scattering rate, the total mobility inside the semiconductor is written using Matheissen's rule as

$$\frac{1}{\mu_{Total}} = \frac{1}{\mu_B} + \frac{1}{\mu_{SP}} + \frac{1}{\mu_C} + \frac{1}{\mu_{SR}} \quad (2.5)$$

Using device modeling and rigorous comparison to experiment, we extract values for the physical parameters such as interface trap density of states, surface step height and surface electron saturation velocity which determine these different mobilities. The mobility models and their temperature dependence are described below.

2.2.1. Low Field Bulk Mobility

Phonon scattering and ionized impurity scattering in the bulk are the mechanisms limiting low field bulk mobility of charge carriers [20][36]. Introduction of impurities (dopant atoms) in the semiconductor lattice gives rise to a perturbation of the periodic potential of the crystal lattice. This perturbation (Coulombic potential) scatters the mobile carriers flowing in the bulk semiconductor. For high doped regions of the MOSFET (source and drain), ionized impurity scattering is an important scattering mechanism. Further, lattice vibrations (phonons) in the bulk semiconductor also causes scattering of the mobile carriers. The bulk mobility in 4H-SiC devices has been measured very accurately using Hall measurements for a variety of dopings and temperatures. We have used the Caughey - Thomas method for modeling bulk mobility [37]. The bulk mobility can be represented as being dependent on the doping density and temperature according to the following relation.

$$\mu_B = \frac{\mu_{\max} \left(\frac{300}{T} \right)^\alpha - \mu_{\min}}{1 + \left(\frac{D}{N_{ref}} \right)^\beta} + \mu_{\min} \quad (2.6)$$

The following table gives the values for the temperature dependence parameter (α), and doping dependence parameters (N_{ref} and β) [16][38].

Table 2.1. Parameter values used for calculating the bulk mobility in a 4H-SiC MOSFET [16][38].

Parameter	Symbol	Unit	Value
Maximum Bulk Mobility	μ_{max}	cm ² /Vs	1071.0
Minimum Bulk Mobility	μ_{min}	cm ² /Vs	5.0
Temperature Dependence	α	-	2.4
Doping Dependence	N_{ref}	cm ⁻³	1.9×10 ¹⁷
Doping Dependence	β	-	0.40

2.2.2. Surface Phonon Mobility

Acoustic phonon scattering the surface is responsible for reduction in surface mobility in MOSFETs. Surface phonon scattering is especially important at high temperatures because of increase in phonon activity with increase in temperature. Surface phonon mobility is modeled as being dependent on the surface field, the acoustic phonon deformation potential and the average depth of the inversion layer at the surface. Various values of the deformation potential from 11eV to 23.8eV have been listed in literature [15][16][18].

The surface phonon mobility can be written as [19][26]

$$\mu_{ac} = \frac{A}{E_{\perp}} + \frac{B}{TE_{\perp}^{1/3}} \quad (2.7)$$

Where, A and B are parameters having the following forms [26]

$$A = \frac{3 \hbar^3 \rho_{bulk} v_s^2}{2 m^* m_c D_{ac}^2} \quad (2.8)$$

$$B = \frac{e \hbar^3 \rho_{bulk} v_s^2}{m^* m_c D_{ac}^2 k_B} * \left(\frac{9 \hbar^2}{4 q m_{\perp}} \right)^{1/3} \quad (2.9)$$

m^* is the 2D density of states effective mass, m_c is the conductivity effective mass and m_{\perp} is the perpendicular effective mass. ρ_{bulk} is the bulk density, v_s is the velocity of sound in the semiconductor, D_{ac} is the acoustic phonon deformation potential, E_{\perp} is the perpendicular electric field, e is the electronic charge, T is temperature, \hbar is Planck's constant and k_B is Boltzmann's constant. The measured and calculated values of the parameters defining the surface acoustic phonon mobility in 4H-SiC MOSFETs are given in Table 2.2.

Surface acoustic phonon mobility reduces with increase in perpendicular field. So, it has more effect at higher gate voltages. Also, with increase in temperature, phonon vibrations increase, causing increased phonon scattering of mobile charges. Hence, the surface acoustic phonon mobility decreases with increase in temperature.

Table 2.2 Parameter values for calculating surface acoustic phonon mobility in 4H-SiC MOSFETs [16][39]

Parameter	Symbol	Unit	4H-SiC
Bulk Density	ρ_{bulk}	g/cm ³	3.2
Velocity of Sound	v_s	cm/s	1.37×10 ⁶
Acoustic Deformation Potential	D_{ac}	eV	20
Effective Mass	m_1, m_2, m_3 (for electrons)		0.29, 0.58, 0.33
Effective Mass	m^*, m_c, m_{\perp} (for electrons)		0.41, 0.39, 0.41
Calculated Parameter	A	cm/s	7.8243×10 ⁷
Calculated Parameter	B	(V/cm) ^{-2/3} •°K•cm/s	9.9240×10 ⁶

2.2.3. Coulomb Scattering Mobility

Coulomb scattering of inversion layer charges by trapped charges and fixed charges at the interface is the dominant scattering mechanism at low temperatures and low gate fields in 4H-SiC MOSFETs. The Coulomb mobility (μ_c) for electrons at a depth z in the inversion layer, due to scattering caused by charges located at a distance z_i inside the oxide, at a temperature T is given as [25]

$$\frac{1}{\mu_c(z, z_i, T)} = \frac{m^* e^3 N_{2D}(z_i)}{16\pi\epsilon^2 \hbar k_B T} \cdot F(z, z_i, T) \quad (2.10)$$

Where,

$$F(z, z_i, T) = \int_{\alpha=0}^{\pi/2} \left(1 - \frac{q_{sc}^2}{\frac{8m^* k_B T}{\hbar^2} \sin^2 \alpha + q_{sc}^2} \right) \exp \left[-2 \sqrt{\frac{8m^* k_B T}{\hbar^2} \sin^2 \alpha + q_{sc}^2} (z - z_i) \right] d\alpha \quad (2.11)$$

Here, $N_{2D}(z_i)$ is the density of scattering charges located at z_i inside the oxide, q_{sc} is the screening wavevector that depends on the inversion charge density and the depth of the inversion layer, and α is the scattering angle. For our modeling and simulations, we consider that all the trapped charges are located at the interface ($z_i=0$).

At high temperatures, the mobile charges have higher energy, and so they scatter less from the trapped charges. Hence, Coulomb mobility increases with temperature. Further, due to lower probability of trap occupation at higher temperatures, the scattering charge density also reduces, thereby giving higher mobility. Thus, the effect of Coulombic scattering will be less at higher temperatures, giving a higher effective mobility and thereby higher current in the SiC MOSFET.

2.2.4. Surface Roughness Mobility

Surface roughness mobility arises from the scattering of mobile carriers by imperfections of the SiC surface [39][40]. 4H-SiC MOSFETs are grown on an 8° off-axis substrate. This step flow growth procedure gives rise to surface steps that are about 1nm high and repeat every 7nm. These steps are termed as nanosteps. Furthermore, there is evidence of step bunching due to formation of very high (3-5 nm) and very long (30nm-70nm) macrosteps along with the nanosteps at the SiC-SiO₂ interface [39][42][43]. A schematic for such a SiC surface is shown in Fig. 2.1. This makes the SiC surface very

complex and also causes significant surface roughness scattering at high fields perpendicular to the interface.

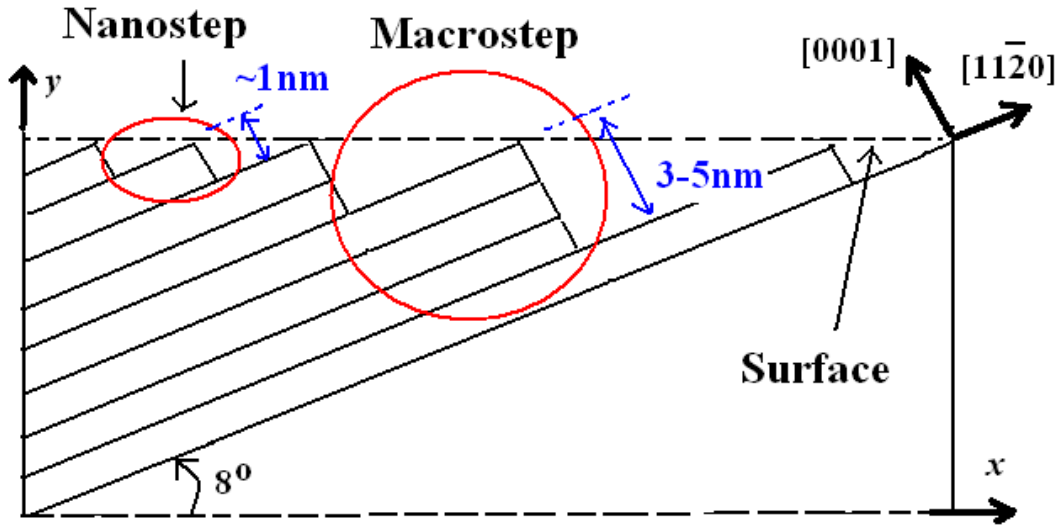


Fig. 2.1 Surface of a 4H-SiC MOSFET consisting of step bunches which are a combination of nanosteps and macrosteps.

The surface roughness scattering rate is calculated by first writing a perturbation potential arising from the fluctuations in the surface of the semiconductor. The perturbation potential is written as

$$V_{\text{perturb}}(\vec{r}) = \delta(\vec{r}) \cdot \frac{\partial V}{\partial z} \quad (2.12)$$

$\delta(\vec{r})$ represents the surface roughness which is the variation in the height of the surface steps as a function of position, and $\frac{\partial V}{\partial z}$ gives the electric field at the semiconductor surface.

Surface roughness gives rise to fluctuations in the potential energy that electrons feel, in essence, varying the depth of the local potential well. Thus, electrons directly at

the interface, as well as those slightly away from the interface in the channel, are affected by surface roughness. To account for the depth dependence of surface roughness scattering, we consider the electrons to be free in the plane parallel to the surface, and bound in the direction perpendicular to the interface. We then express the scattering as a series of 2-dimension matrix elements at each depth. We evaluate the matrix element at each depth in the channel thereby providing the surface roughness scattering rate as a function of depth into the channel.

Fermi's Golden Rule describes the probability of an electron scattering from an initial state to a new state.

$$\Gamma_{kk'} = \frac{2\pi}{\hbar} |H_{kk'}|^2 \delta(E(k) - E(k')) \quad (2.13)$$

Where $H_{kk'}$ is the matrix element describing the interaction of the electron wavefunction with the perturbation potential. The matrix element for the perturbation potential for surface roughness scattering can be written as

$$H_{kk'} = \int e^{i\vec{k}\cdot\vec{r}} \delta(\vec{r}) \frac{\partial V}{\partial z} e^{-i\vec{k}'\cdot\vec{r}} d\vec{r} \quad (2.14)$$

As the perpendicular field is independent of r , the matrix element can be written in terms of the scattering wave vector q as

$$H_{kk'} = F_{\perp}(z) \int \delta(\vec{r}) e^{-i\vec{q}\cdot\vec{r}} d\vec{r} \quad (2.15)$$

$F_{\perp}(z)$ is the perpendicular component of the electric field at a depth z inside the MOSFET away from the interface, \vec{k} and \vec{k}' respectively represent the electron wavevector before and after the scattering event, and scattering wavevector \vec{q} is the vector difference $\vec{k}' - \vec{k}$.

Thus, from the above equation, we can see that the matrix element is essentially the Fourier transform of the fluctuation in the surface morphology as described by the function $\delta(r)$. In Fermi's Golden Rule, the square of the scattering matrix element is used to calculate the scattering probability and it is written as [44]

$$|H_{kk'}|^2 = e^2 F_{\perp}(z)^2 S(q) \quad (2.16)$$

Here, $S(q)$ is the square of the Fourier transform of the roughness function $\delta(r)$ and is known as the roughness power spectrum. By convolution, the power spectrum is also the Fourier transform of the autocovariance function $\mathfrak{R}_{\delta}(\delta(r))$ of $\delta(r)$ [45]. We represent the surface roughness using an exponential autocovariance function as [45]

$$\mathfrak{R}_{\delta} = \langle \delta(\mathbf{r}), \delta(\mathbf{r}-\mathbf{r}') \rangle = \Delta^2 \cdot e^{-r/L} \quad (2.17)$$

Where, Δ is the average step height and L is the step repetition frequency or correlation length [44][45]. Therefore, the roughness power spectrum can be written as

$$S(q) = \langle \mathbf{k} | \mathfrak{R}_{\delta} | \mathbf{k} \rangle = \frac{\pi \Delta^2 L^2}{\left[1 + \frac{q^2 L^2}{2} \right]} \quad (2.18)$$

The roughness power spectrum represents the amount of scattering that can occur for a given value of the scattering wavevector. The nanosteps give a very wide (small L) power spectrum with small amplitude (small Δ), whereas the macrosteps give a very narrow (large L) power spectrum with large amplitude (large Δ). As shown in Fig. 2.2, we use a power spectrum that is a combination of the two to represent the step bunching phenomenon at the 4H-SiC surface.

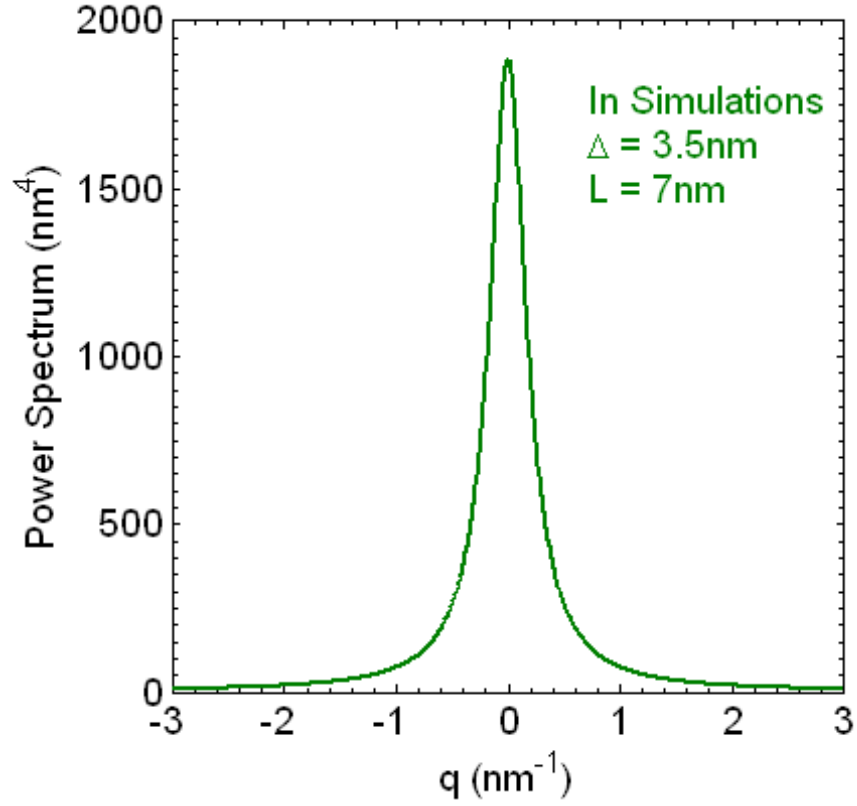


Fig. 2.2 Power spectrum for the surface steps incorporating the effect of step bunching (both nanosteps and macrosteps) and used in simulations to fit to experimental data.

Using Fermi's Golden Rule and the scattering matrix element defined above, the probability of scattering an electron with wavevector \vec{k} and energy E to a new state with wavevector \vec{k}' and energy E' is then written as

$$S_{kk'}(z) = \frac{2\pi}{\hbar} |H_{kk'}|^2 \delta(E - E') = \frac{2\pi^2 e^2 \Delta^2 L^2 F_{\perp}(z)^2}{\hbar \left(1 + \frac{q^2 L^2}{2}\right)} \delta(E - E') \quad (2.19)$$

Including the effect of screening on surface roughness scattering [46], and using the scattering probability given above, the scattering rate is written as [46][47]

$$\frac{1}{\tau_{SR}(z)} = \frac{1}{4\pi^2} \iint_{\theta, k'} S_{kk'}(z) \left(\frac{q}{q+q_{sc}} \right) (1 - \cos \theta) d\theta k' dk' \quad (2.20)$$

E and E' represent the initial and final energies for the scattered electron. θ is the angle between \vec{k} and \vec{k}' . q_{sc} is the screening wavevector that is dependent on inversion layer charge density. This scattering rate is then used to write the depth dependent surface roughness mobility as

$$\mu_{SR}(z) = \frac{m_c}{e} \left\langle \left\langle \frac{1}{\tau_{SR}} \right\rangle \right\rangle = \left(\frac{\hbar^3}{2m_c m^* e \Delta^2 L^2} \right) \frac{1}{F_{\perp}(z)^2} \frac{1}{\Omega_{SR}} \quad (2.21)$$

where Ω_{SR} is given as

$$\Omega_{SR} = \int_0^{\pi/2} \frac{\sin^3(\alpha) d\alpha}{\left(\sin(\alpha) + \frac{q_{sc}}{\sqrt{8m^* k_B T / \hbar^2}} \right) \left(1 + \sin^2(\alpha) L^2 \cdot \frac{4m^* k_B T}{\hbar^2} \right)} \quad (2.22)$$

Here, $\mu_{SR}(z)$ is the depth dependent surface roughness mobility, \hbar is Planck's constant, e is the electronic charge, m_c is the conductivity effective mass, m^* is the density of states effective mass, T is temperature, k_B is Boltzmann's constant, α is the scattering angle and q_{sc} is the screening wavevector.

As temperature increases, the carrier concentration at the interface becomes less dense thereby reducing the shielding of the surface potential perturbations by the channel mobile electrons. This results in electrons, that are deeper into the channel and away from the rough surface, to scatter at a rate which is slightly too high. To compensate for this reduced shielding at higher temperatures, we introduce an effective field at each depth $F_{eff}(z, T)$ inside the semiconductor as

$$F_{eff}(z, T) = F_{\perp}(z) \cdot \left(\frac{300}{T} \right)^{\gamma} \quad (2.23)$$

where γ is an empirical parameter between zero and one.

For the MOSFET under measurement and simulation, we have extracted the root mean squared height of the surface steps (Δ) as 3.5nm and the correlation length as $L = 7$ nm. Simulations and comparison to experiment of I_D - V_{GS} curves at high temperatures has given us the value of γ as 0.65.

2.2.5. High Field Mobility – Saturation Velocity

The effect of high lateral field on the total mobility in a 4H-SiC MOSFET is given in terms of the saturation velocity. The total mobility that includes the low field and the high field components is written using Thornber's model [48] as

$$\mu_T(T) = \frac{\mu_{LF}(T)}{\left[1 + \left(\frac{\mu_{LF}(T)E_{\parallel}}{v_{sat}(T)} \right)^{\delta} \right]^{1/\delta}} \quad (2.24)$$

Where, v_{sat} is the saturation velocity, E_{\parallel} is the lateral field, μ_{LF} is the total low field mobility obtained by summing up the different mobility using Matheissen's rule. μ_T is the total mobility, and δ is an empirical parameter.

The saturation velocity decreases with temperature due to increase in phonon scattering and is given as -

$$v_{sat}(T) = v_{sat}(300) \cdot \left(\frac{300}{T} \right)^{\eta} \quad (2.25)$$

Our simulations and comparison to experiment have given us the values of these parameters as: $v_{sat}(300) = 10^7$ cm/s, $\delta = 2$, and $\eta = 0.5$.

2.3. Parameter Extraction Methods

We employed two strategies for extracting the physical parameters of the interface trap density of states and the mobility models. The main parameters responsible for governing transport in the devices are the interface trap density of states (D_{it}^{edge} , D_{it}^{mid} , σ), and the surface roughness step height (Δ). These quantities affect very distinct regimes of device operation. The interface traps get occupied very quickly when gate bias is increased, reaching close to the maximum occupied values close to threshold. Therefore, comparison of the subthreshold I_D - V_{GS} simulated characteristics to experiment enables us to extract the interface trap parameters. At large gate biases, the inversion charge screens out the Coulomb scattering from occupied traps. In this case, the total low field mobility is controlled by surface roughness scattering. Therefore, comparison of simulated and measured I_D - V_{GS} characteristics at high gate bias would give values for the surface roughness parameters. We extract these values by using an automated curve-fitting method and also by directly varying the parameters based on past knowledge and some available experimental data.

2.3.1. Automated Parameter Extraction

A curve fitting method involving the steepest descent Newton's method algorithm is used to extract the physical parameter values. For the four values to be extracted, four distinct gate biases are chosen to represent the subthreshold, near-threshold, and large gate bias region of the I_D - V_{GS} characteristics. Further, the parameters D_{it}^{edge} and D_{it}^{mid} are several orders of magnitude larger than the band-tail energy σ and the surface roughness

step height Δ . Therefore, we extract the logarithms of D_{it}^{edge} and D_{it}^{mid} instead of the real values.

The curve-fitting problem is set up as follows. Four points on the experimental I_D - V_{GS} characteristics are chosen. Then using an initial guess for the parameter values, we simulate the four bias points. The cost function is evaluated as the difference between the simulated and measured current values. The simulator is run four more times, each time varying one of the parameters by a small amount. The calculated values of current in each case are used to evaluate the derivative of the cost function due to each parameter. These derivatives are then used in the Newton's method to calculate the step direction for each parameter. The new parameters are evaluated and the process is repeated until the cost function reaches an acceptable error limit.

This method is simple, but it takes a very long time to get the extracted values. The reason for this being the need to use the device simulator each time a derivative of the cost function needs to be calculated. Therefore, the simulator needs to be run four times in each Newton's cycle. Also, if the initial guesses are not close to the final solution, the method diverges very quickly. Also, as the change in current with gate bias is exponential in subthreshold, quadratic in near-threshold, and linear at high gate biases, the effects each parameter has on the cost function cannot be predicted very well.

2.3.2. Custom Parameter Extraction

During our work on extracting the physical parameters that govern transport in SiC MOSFETs, we have found that using a more direct approach on selecting the values for the interface trap density of states and surface roughness, provides a much quicker

method of obtaining fits to experiment. Our strategy involves obtaining fits to experiment by choosing interface trap parameters that are close to values reported in literature, and also measured by our collaborators at the Army Research Laboratory. We ensure that the parameters do not go out of bounds with respect to the experimentally measured values. Further, on obtaining close match to experiment, we use the steepest descent algorithm to get to the final solution.

2.4. High Temperature Lateral MOSFET Results

We have implemented the mobility models and the interface trap physics described above in our 4H-SiC MOSFET device simulator and carried out simulations for various devices with different bias voltages and temperatures. Here we present some of the results and the physics we have extracted from them.

2.4.1. Linear and Subthreshold Current vs. Temperature Characteristics

We use a close correlation between simulation and measurement of I_D - V_{GS} in subthreshold and linear regions to extract the density of states of the interface traps. Interface traps have a strong effect on the sub-threshold and near-threshold regions of the I_D - V_{GS} characteristics of 4H-SiC MOSFETs. In the sub-threshold region, increase in gate voltage causes a rapid occupation of the mid-gap states. As the gate voltage increases further, the Fermi level moves closer to the band edge and thereby causes occupation of band-edge traps. Therefore, simulation of the subthreshold characteristics and comparison to experimental measurements gives us a measure of the mid-gap density of states and the band-tail energy, whereas comparison of near-threshold characteristics enables us to extract the band-edge density of states of the interface traps.

Fig. 2.3 and Fig. 2.4 show the low-field I_D - V_{GS} simulations and comparison to experiment for a $424\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET at 25°C , 100°C and 200°C . The solid lines are the experimental measurements while the circles are the simulations. The drain bias in these measurements and simulations was kept at 50mV. The match between simulations and experiment at all three temperatures and in the subthreshold, near-

threshold and high gate bias regions can be clearly seen from the two figures. This agreement gives us confidence that the models are an accurate description of the internal operation of the device.

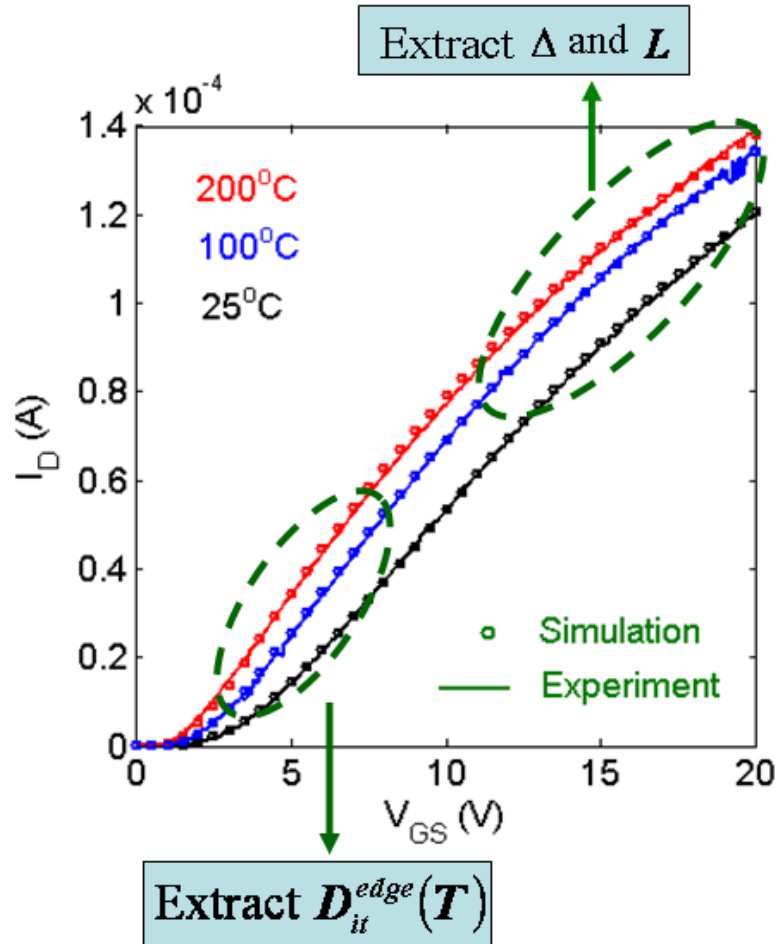


Fig. 2.3 Simulated I_D - V_{GS} characteristics and comparison to experiment for a 4H-SiC MOSFET at different temperatures. $V_{DS} = 50$ mV.

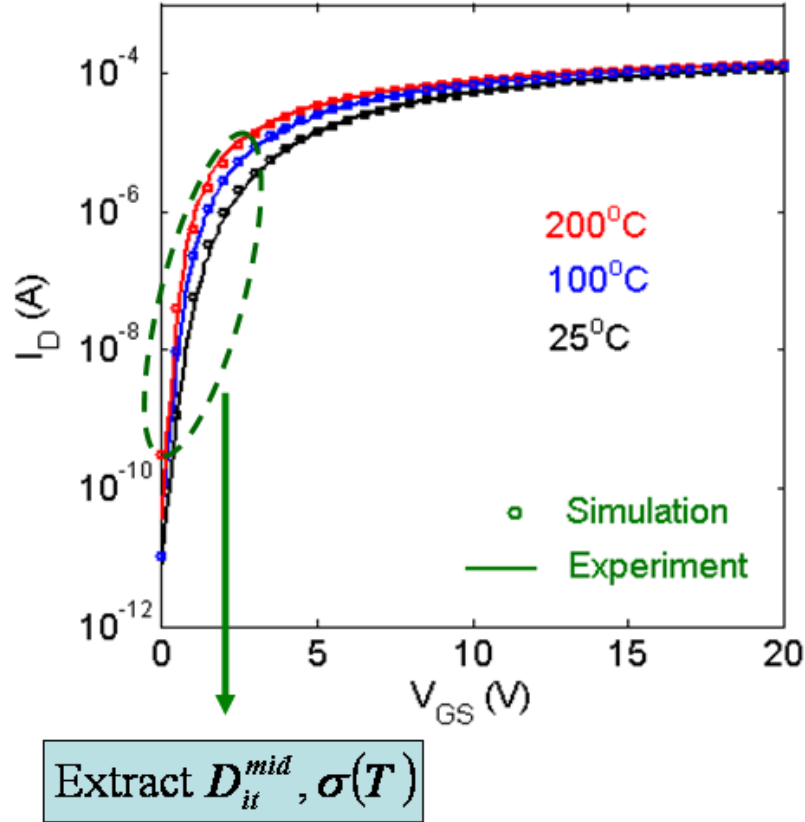


Fig. 2.4 Simulated I_D - V_{GS} characteristics and comparison to experiment for a 4H-SiC MOSFET at different temperatures. $V_{DS} = 50\text{mV}$. (Plotted on log scale for subthreshold region comparison.)

2.4.2. Extracting Interface Trap Density of States at Different Temperatures

As mentioned before, in the subthreshold region of operation, the Fermi level is located towards the middle of the bandgap, indicating the occupation of the interface traps located near midgap. Therefore, the good agreement between simulations and experiment in the subthreshold region at the three temperatures enables us to extract the value for the midgap density of states (D_{it}^{mid}), and the temperature dependent band-tail energy parameter ($\sigma(T)$). We see a constant value of $2.4 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$ for the midgap density of states for all three temperatures. The band-tail energy parameter increases

monotonically from 67 meV to 93 meV as the temperature rises from 25°C to 200°C. We believe this monotonic increase is due to the spreading of the band-tail states of the interface traps with rise in temperature.

As gate voltage is increased, the Fermi level moves closer to the conduction band and more of the band-edge states become occupied. Agreement between simulations and experiment in this near-threshold region gives us the value of the band-edge density of states ($D_{it}^{edge}(T)$). The value of the band-edge density of states reduces from $5.7 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ to $4.1 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ from 25°C to 200°C due to narrowing of the 4H-SiC bandgap. The extracted interface trap density of states profiles at the three temperatures is shown in Fig. 2.5. The trap density of states is higher over part of the bandgap at higher temperatures. But, as the bandgap is larger at lower temperatures, traps located at larger energies are exposed, thereby resulting in higher band-edge density of states values.

We note that the extracted values for the trap density of states parameters are for the particular 4H-SiC MOSFET under test. We have observed different interface trap density of states for devices fabricated with different processes, and also from wafers from different lots. Thus, the precise extracted values are likely to be subject to the exact processing of the device.

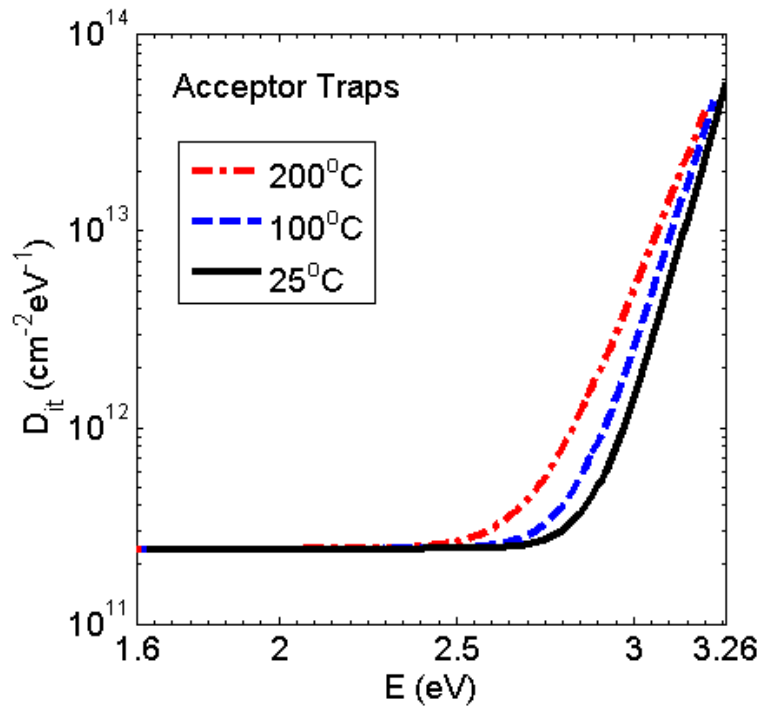


Fig. 2.5 Extracted interface trap density of states for different temperatures. Simulations and comparison to experiment indicate spreading of the band-tail states at high temperatures. Also, as the conduction band edge moves towards the middle of the bandgap, the band-edge value of the density of states reduces.

2.4.3. Extracting Surface Roughness

At large perpendicular electric fields, and hence large values of V_{GS} , surface roughness scattering becomes the mechanism that dominates mobility in the inversion layer. Therefore, by comparing simulated I_D - V_{GS} characteristics to experiment at high gate voltages, we are able to extract the values for the surface roughness scattering parameters Δ (rms height) and L (correlation length). The extracted values of Δ and L are 3.5 nm and 7.0 nm respectively for the 4H-SiC MOSFET under test. The step height is an order of magnitude higher than the current Silicon MOSFETs. This makes surface roughness scattering the dominant scattering mechanism in SiC MOSFETs, especially at high vertical fields.

As has been discussed previously, the large value of Δ is indicative of the presence of both nanosteps and macrosteps at the surface. In addition to step bunching at the SiC surface, high surface roughness parameters may also be attributed to the presence of a transition region between the 4H-SiC and SiO₂ regions near the interface. Recent studies of the 4H-SiC/SiO₂ interface by high-resolution transmission electron microscopy (TEM), Z-contrast scanning TEM, and spatially resolved electron energy-loss spectroscopy have revealed the presence of a 2nm-20nm thick interfacial layer containing Silicon, Carbon and Oxygen [49]. C-V measurements have verified that the inversion layer forms inside this transition region. Some researchers have suggested a direct relationship between the thickness of the transition region and surface mobility. This transition region may also be the reason why we extract such large values of surface steps.

2.4.4. Extracting Saturation Velocity

In the saturation region of operation for a MOSFET, a large lateral electric field forms at the drain-channel junction. This large field accelerates the channel electrons to high velocities. The surface velocity saturates due to phonon scattering giving rise to a high-field mobility component that is dependent on the saturation velocity and the lateral electric field. The current in the saturation region is limited by this high-field mobility. We simulate the high field I_D - V_{DS} curves for the 4H-SiC MOSFET for different gate biases and temperatures and compare them to experiment. This comparison enables us to extract the saturation velocity (v_{sat}), the parameter β in Thornber's high-field mobility model and the temperature dependence of saturation velocity (η). Fig. 2.6, Fig. 2.7 and Fig. 2.8 show the simulated and experimentally measured I_D - V_{DS} characteristics at room temperature, 100°C and 200°C respectively. We see reasonably good agreement between simulation and experiment. Our simulations indicate the value of saturation velocity at room temperature to be approximately 1.0×10^7 cm/s which is roughly half of the bulk saturation velocity. The temperature dependence of this saturation velocity ($\eta = 0.5$) is similar to the temperature dependence of bulk saturation velocity of 4H-SiC [50]. The extracted high-field mobility parameters are given in Table 2.3.

Table 2.3 Extracted parameter values from comparison of high temperature low field I_D - V_{GS} simulations to experiment

Parameter	Symbol	Units	25°C	100 °C	200 °C
Midgap Trap Density of States	D_{it}^{mid}	$\text{cm}^{-2}\text{eV}^{-1}$	2.4×10^{11}		
Bandedge Trap Density of States	D_{it}^{edge}	$\text{cm}^{-2}\text{eV}^{-1}$	5.73×10^{13}	5.0×10^{13}	4.1×10^{13}
Band tail energy	σ	meV	67	75	93
Fixed and Oxide Trap Charge	$N_f + N_{OT}$	cm^{-2}	1.33×10^{12}	1.15×10^{12}	1.05×10^{12}
Average Step Height	Δ	nm	3.5		
Average Correlation Length	L	nm	7.0		
Temperature Parameter for Effective Field in μ_{SR}	γ	-	0.65		
Saturation Velocity	v_{sat}	cm/s	1.0×10^7		
Thornber Model Parameter	δ	-	2.0		
Temperature Dependence of Saturation Velocity	η	-	0.5		

2.4.5. Saturation Current vs. Temperature Characteristics

The comparisons of the simulated and experimental I_D - V_{DS} characteristics for different temperatures are given in Fig. 2.6, Fig. 2.7, and Fig. 2.8. Good agreement of simulations and experiment is seen for different gate and drain biases for all three temperatures. This helps us verify our low and high temperature mobility models and extract the various physical characteristics of 4H-SiC MOSFETs.

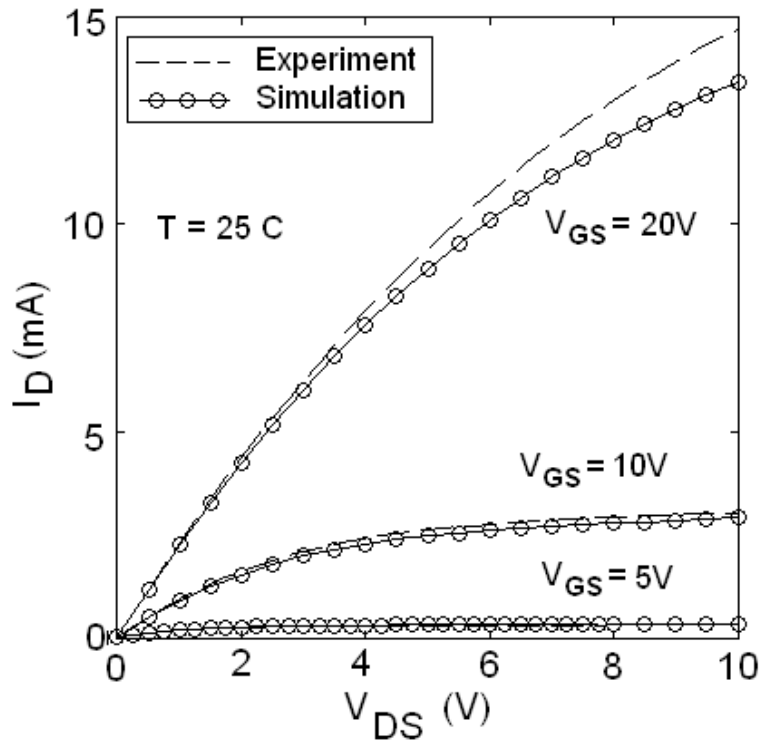


Fig. 2.6 Simulated and experimental I_D - V_{DS} curves at room temperature for a $424\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET for different gate biases.

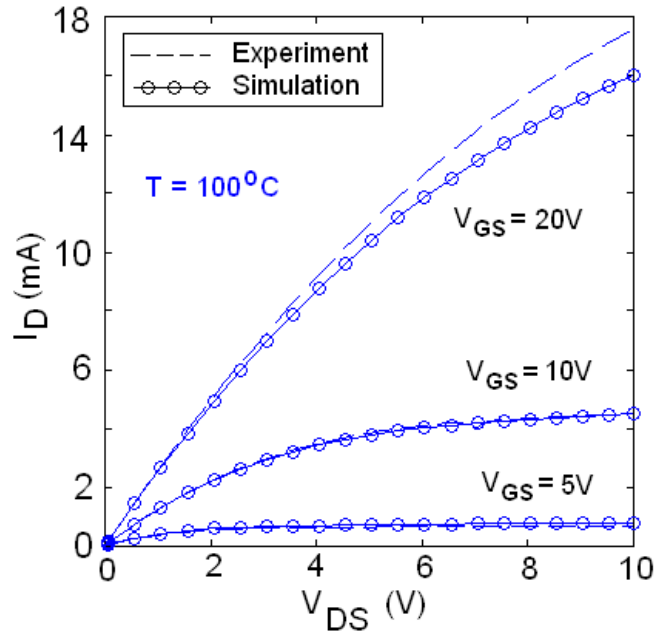


Fig. 2.7 Simulated and experimental I_D - V_{DS} curves at 100°C for a $424\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET for different gate biases.

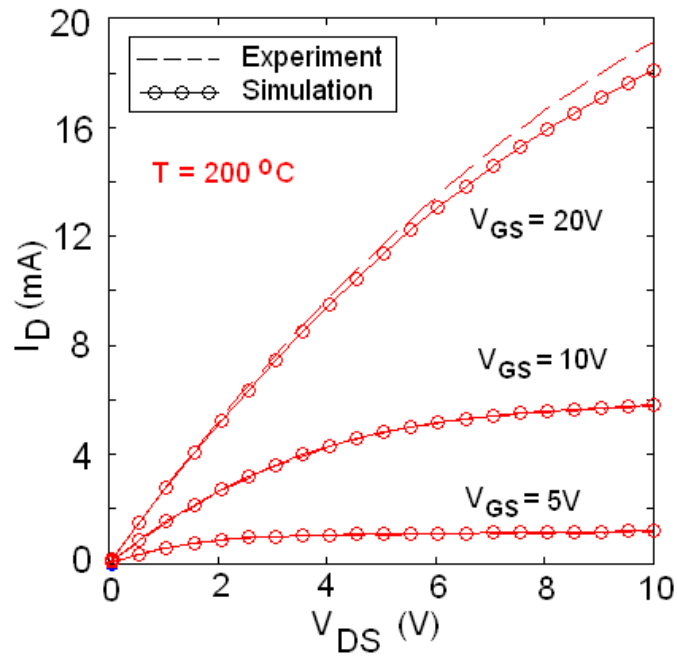


Fig. 2.8 Simulated and experimental I_D - V_{DS} curves at 200°C for a $424\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET for different gate biases.

2.5. Physics of High Temperature 4H-SiC MOSFET Operation

From our device simulations we can observe and interpret the physics of transport inside a 4H-SiC MOSFET. We can observe the effect of various mobilities at different temperatures and bias values, and thereby determine which scattering mechanisms dominate under the various conditions. Here we compare and contrast the two main scattering mechanisms observed in 4H-SiC MOSFETs, Coulomb scattering and Surface Roughness scattering, and characterize their effects at different biases. Further, we discuss the behavior of low-field and high-field mobility as a function of temperature and location inside the MOSFET. We examine how current changes with temperature in a 4H-SiC MOSFET and explain the rationale behind this behavior. Finally, using the device simulator, we show the working of a hypothetical 4H-SiC MOSFET that has a greatly reduced concentration of interface traps, and compare the results with the MOSFET under test.

2.5.1. Coulomb Mobility and Surface Roughness Mobility:

After obtaining agreement with experiment, we are now able to compare the effects of the various mobilities that help to determine 4H-SiC MOSFET behavior. Simulation indicates that Coulomb and surface roughness mobilities are dominant in the subthreshold and linear regions of operation. Fig. 2.9 and Fig. 2.10 show the Coulomb scattering mobility and the surface roughness mobility at the center of the channel as a function of depth inside the semiconductor for two different gate voltages. The plots in Fig. 2.9 are for a gate bias of 3V. For this low gate bias, the figure indicates that Coulomb scattering mobility has a greater effect limiting current than does surface roughness

mobility. However, Fig. 2.10 shows that for larger gate voltages, surface roughness mobility becomes the dominant mechanism. This transition from Coulombic dominated mobility to surface roughness limited mobility, is due to increased screening of interface charge by the inversion layer, and hence less interface state Coulombic scattering, allowing Surface roughness to dominate. The figures also indicate that mobility is a function of depth into the device. The $\frac{1}{r}$ dependence of Coulomb potential causes Coulomb mobility to rise very quickly with distance away from the interface. This effect is even more pronounced at large gate voltages where screening is high. The figures also indicate that surface roughness mobility increases with depth into the device. This is due to the reduction of the surface roughness scattering potential with distance into the device.

These results indicate that SiC MOSFET device processing should be focused on both, reduction of interface traps as well as on smoothing the surface.

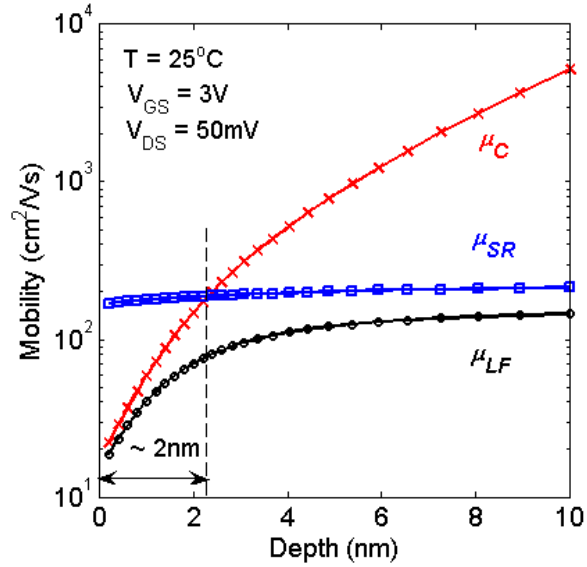


Fig. 2.9 Comparing Coulomb mobility (μ_C) and surface roughness mobility (μ_{SR}) at low gate bias. Coulomb mobility dominates near the interface due to less screening. Total low-field mobility (μ_{LF}) follows the Coulomb mobility curve near the interface.

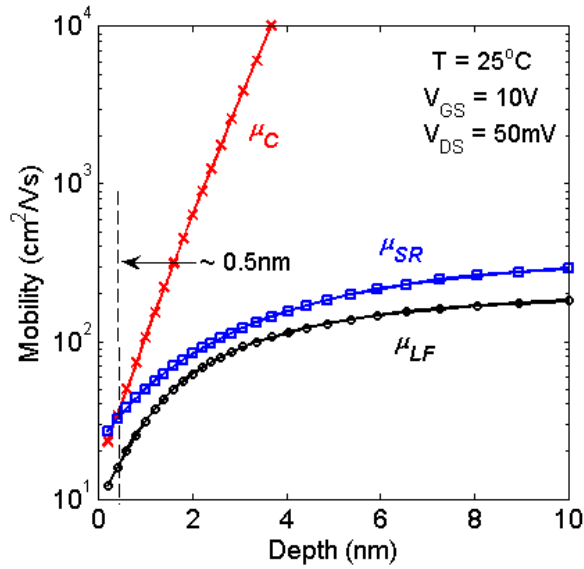


Fig. 2.10 Comparison of Coulomb mobility and surface roughness mobility at high gate bias shows that surface roughness mobility dominates near the interface. (The curves are for the mobilities at the center of the channel and are plotted as a function of depth away from the interface.)

2.5.2. Temperature Dependence of Low-Field Mobility

By comparing experiment with simulation we are able to quantify the values for mobility versus temperature and distance from the interface. Fig. 2.11 and Fig. 2.12 show the bulk phonon mobility and the surface phonon mobility at three different temperatures plotted as a function of depth. Both mobilities decrease with temperature. Hence, at much higher temperatures, they would become the dominant mechanisms. Bulk mobility obviously does not change with depth because the doping is constant in the epi-layer, whereas surface phonon mobility increases with depth as it depends upon the perpendicular electric field.

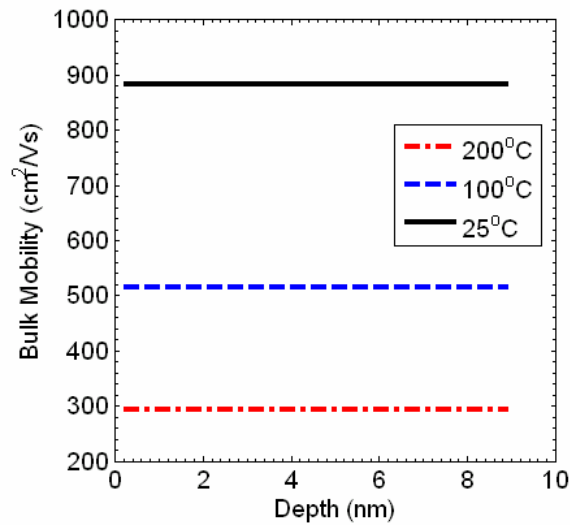


Fig. 2.11 Bulk mobility is constant with depth as the doping is constant in the epi-layer. It decreases with increase in temperature, but is still much higher than surface roughness and Coulomb mobilities.

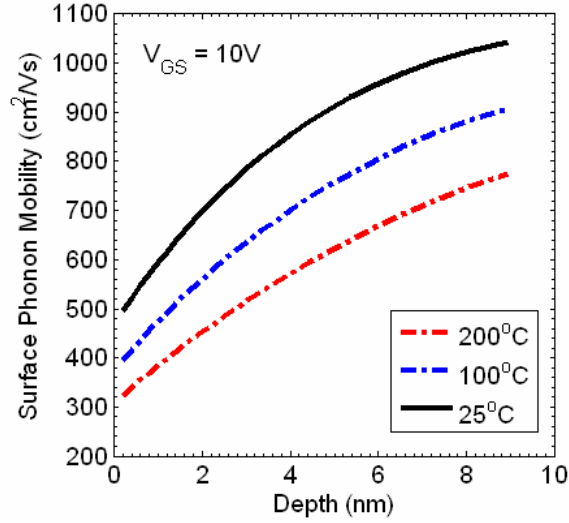


Fig. 2.12 Surface acoustic phonon mobility as a function of depth at different temperature. It also decreases with temperature, and may become the dominant mobility at elevated temperatures and larger gate fields. (The curves are for the mobilities at the center of the channel and are plotted as a function of depth away from the interface.)

Fig. 2.13 and Fig. 2.14 show the total low-field mobility as a function of distance from the interface at room temperature, 100°C and 200°C, for gate biases of 2V and 10V, respectively. As discussed above, at $V_{GS}=2V$, Coulomb scattering limits the mobility. Furthermore, we see from equations (2.8) and (2.9), that Coulomb scattering is inversely proportional to temperature. The higher the temperature, the more energy electrons have, and are therefore less affected by the Coulomb potential. Also, Coulomb scattering is directly proportional to the occupied trap density. As occupied trap density decreases with rise in temperature, Coulomb scattering also decreases. Since the total low-field mobility curve follows the Coulomb mobility curve at this gate bias, with increase in temperature, the low-field mobility increases. This increase in total low-field mobility with temperature at low gate bias can be seen from Fig. 2.13.

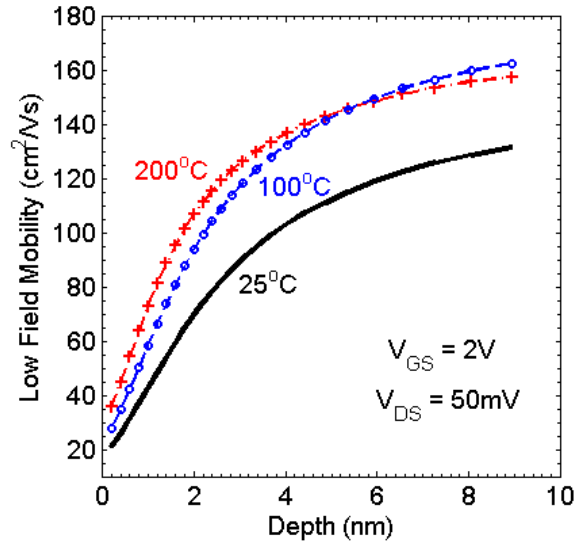


Fig. 2.13 The total low-field mobility near the interface (0-2nm) shows an improvement with temperature as at this gate bias condition, its value depends on the Coulomb mobility

At higher gate biases, surface roughness mobility dominates, as discussed in the previous section. Surface roughness mobility is only weakly dependent on temperature. Therefore, we do not see much effect of temperature on the total low-field mobility at higher gate biases (Fig. 2.14) near the interface. For deeper into the device, bulk phonons start to cause total mobility decrease with higher temperatures, as shown by the 200°C curve in Fig. 2.14.

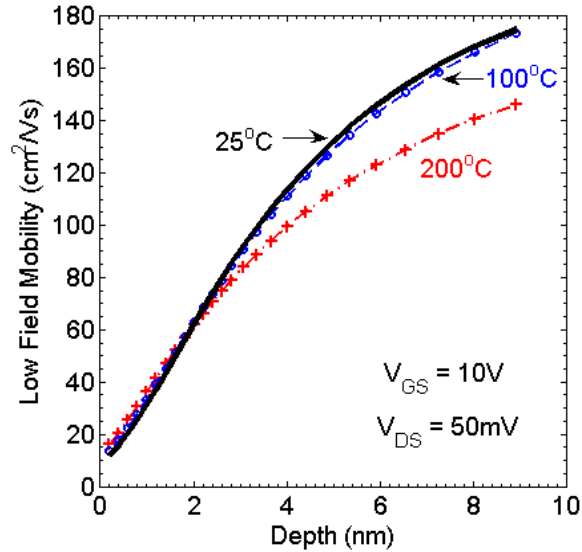


Fig. 2.14 Total low-field mobility near the interface (0-2nm) at high gate voltages does not change much with temperature as the increase in surface roughness mobility with temperature is quite small and it is opposed by the change in surface phonon mobility. (The curves are for the mobilities at the center of the channel and are plotted as a function of depth away from the interface.)

2.5.3. High-Field Mobility

The high-field mobility component becomes important in the saturation regime of MOSFET operation. At large drain biases, there is a large lateral field near the drain-bulk junction. This causes saturation of the velocity of surface mobile carriers causing high-field mobility to become very small near the drain. Therefore, velocity saturation limits the mobility and thereby current in the saturation region. The high-field mobility reduces with temperature mainly because optical phonon scattering increases causing the saturation velocity to decrease [47].

The behavior of total surface mobility near the drain-bulk junction is quite complex. With a large drain bias, a depletion region develops near the drain-bulk junction

causing the mobile electrons to be pushed away. This then causes a reduction in the amount of trap occupation near the drain as shown in Fig. 2.15, resulting in an improvement in the low-field mobility near the drain. This opposes the reduction in mobility due to velocity saturation. Therefore, the total surface mobility is a complex function of drain bias and temperature. As shown in Fig. 2.16, the total surface mobility increases slightly as we go from the source to the drain on account of the reduction in occupied trap density, but then near the drain boundary, owing to the large lateral fields, it shows a sharp decrease.

Furthermore, as seen in Fig. 2.15, the total occupied trap density over the entire gate length decreases with rising temperature. This causes an increase in the total mobility with temperature in most of the channel, except for in the pinch-off region, as shown in Fig. 2.16. The curves are for the surface mobilities plotted as functions of position along the channel from the source ($x < 0\mu\text{m}$) to the drain ($x > 5\mu\text{m}$). Finally, by observing the highly doped source and drain regions of Fig. 2.16, we see that the bulk mobility decreases with temperature.

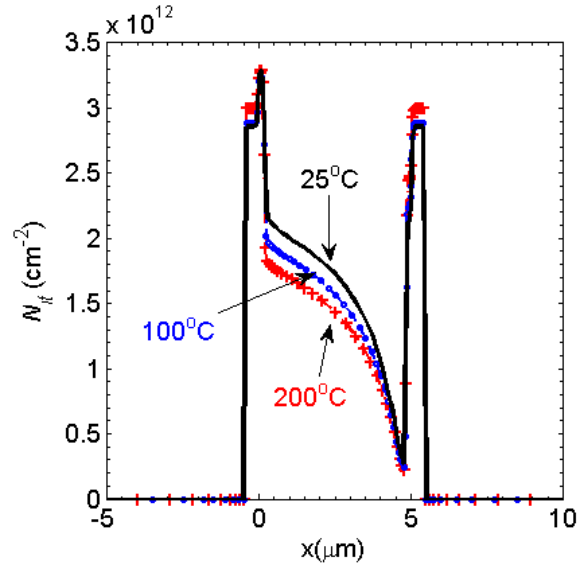


Fig. 2.15 Occupied interface trap density (N_{it}) as a function of position along the interface. N_{it} decreases with temperature along the entire length of the interface. Also, N_{it} reduces as we go from source to drain

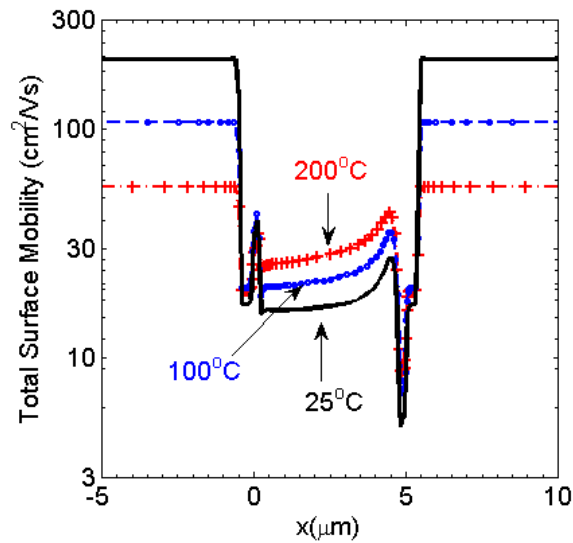


Fig. 2.16 Total surface mobility as a function of position along the channel. An initial increase in mobility is due to reduction in trap density as we go from source to drain. The sharp reduction is due to the effect of velocity saturation. Also, total mobility increases with temperature for most of the channel length. Curves are plotted for $V_{GS}=5\text{V}$ and $V_{DS}=10\text{V}$ bias condition.

2.5.4. Current Density vs. Temperature

Fig. 2.17 and Fig. 2.18 show the current density as a function of depth for four different gate biases and three temperatures for the 4H-SiC MOSFET. We can see that at low gate biases, the current is spread deep into the device. As the gate voltage increases, surface mobility improves slightly and also electrons are pulled closer to the interface. This causes the peak of the current density curves to shift towards the interface. We can also see that the current density is higher for higher temperatures. This effect is more pronounced at lower gate biases because the improvement in surface mobility with temperature is more significant at low gate voltages due to dominance of Coulomb scattering.

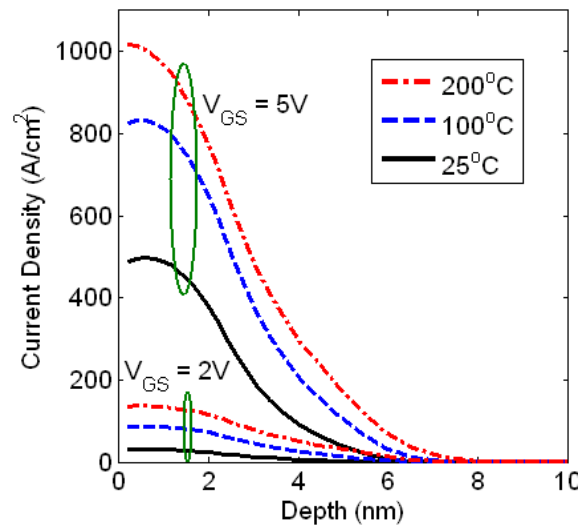


Fig. 2.17 Current density as a function of depth for different temperatures at low gate biases. Current is spread out more, and the peak is slightly away from the interface owing to large Coulombic scattering near the interface. Current density increases significantly with temperature.

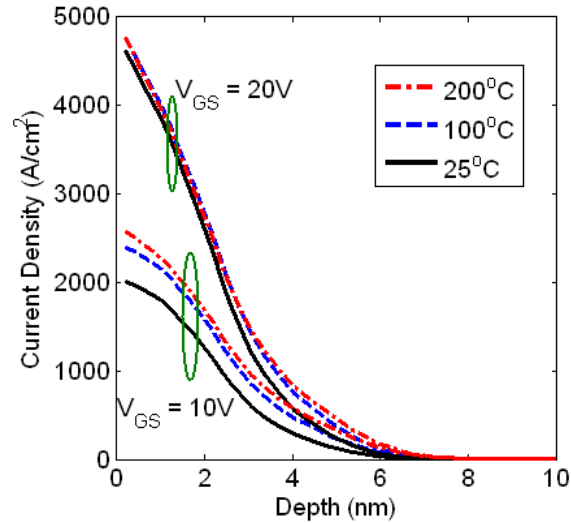


Fig. 2.18 Current density as a function of depth for different temperatures at high gate voltages. Peak of the current density curves is near the interface. Improvement in current density with temperature is not so significant. *(The curves are for the mobilities at the center of the channel and are plotted as a function of depth away from the interface.)*

2.5.5. Increase in Current with Temperature

In all three regions of the 4H-SiC MOSFET device operation (subthreshold, linear and saturation), current increases when temperature increases from 25°C to 200°C. This is shown in Fig. 2.19. There are numerous factors that affect the value of the current versus temperature. These factors include the various scattering mechanism and the density of interface states. However, simulations show that the dominant mechanism responsible for the increase in current is the decrease of occupied traps with increasing temperature. As a result, more electrons are available, at a given gate voltage, for conduction in the channel as temperature increases. The occupied interface trap density and the inversion charge, as a function of gate voltage, for three different temperatures is shown in Fig. 2.20. The figure also shows that the occupied trapped charge is larger than the mobile channel

charge, until gate biases become very large. This indicates that significant improvement in current and transconductance can be realized through reduction of the interface trap density.

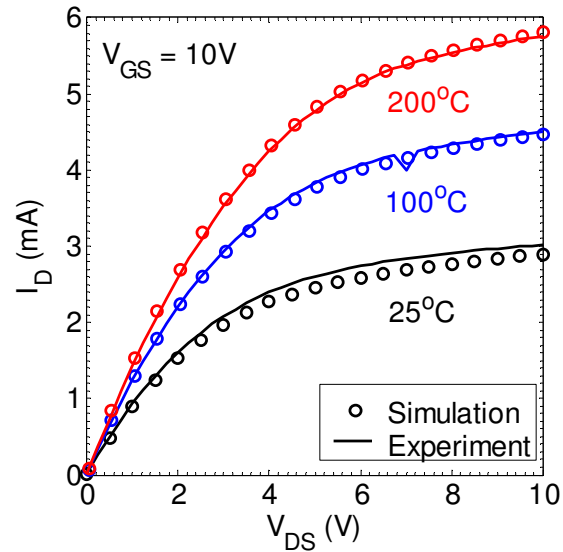


Fig. 2.19 Increase in current with temperature seen for a 4H-SiC MOSFET at a gate bias of 10V.

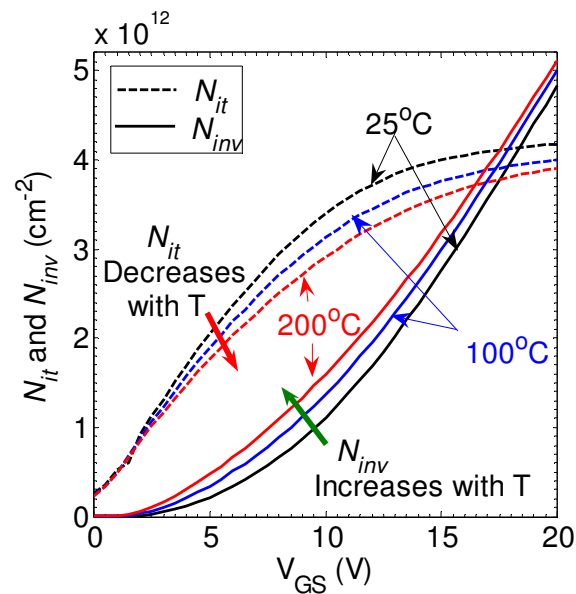


Fig. 2.20 Inversion charge density (N_{inv}) and occupied interface trap density (N_{it}) as a function of gate bias and temperature. A net increase in inversion charge with temperature occurs due to reduction in trap occupation with temperature.

2.5.6. Predicting Device Performance if Interface Trap Concentration is Reduced

A useful application of modeling is that once you have confidence in the physical models that define device operation, by obtaining agreement with experiment over a wide region of biases and temperatures, you can use simulation to design and predict the performance of devices that are not yet fabricated. Here, we use these capabilities to predict the performance of 4H-SiC MOSFETs that have significantly reduced interface state densities. In Fig. 2.21 we compare the I_D - V_{GS} characteristics of the experimental device with those of a hypothetical device that differs by only a factor of ten reduction in the band-edge density of states. The comparison is for the linear region of operation. In Fig. 2.22, we show a comparison for I_D - V_{DS} of the actual and hypothetical devices in the linear and saturation regions. The figures show that the reduction of interface traps yields large improvement in current-voltage characteristics. We further note that the temperature dependence of current changes when trap densities are reduced. We see a lesser relative increase in current with temperature at a given bias in the case of our hypothetical device with reduced trap density as compared to the experimental device. Eventually, when the trap density of states become much less than the current values (comparable to Silicon MOSFETs), we should actually see current reducing with increasing temperature because of lower surface mobility at high temperatures.

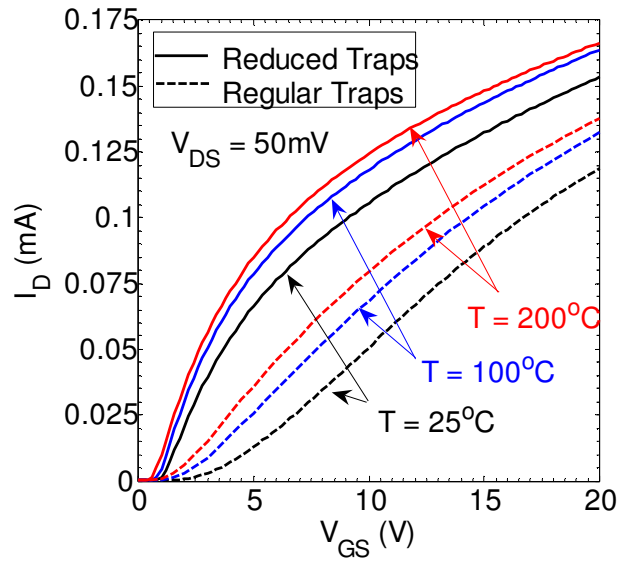


Fig. 2.21 Projected improvement current at three different temperatures, in a 4H-SiC MOSFET on reduction of band-edge density of states of the interface traps by a factor of 10, in the linear region of operation.

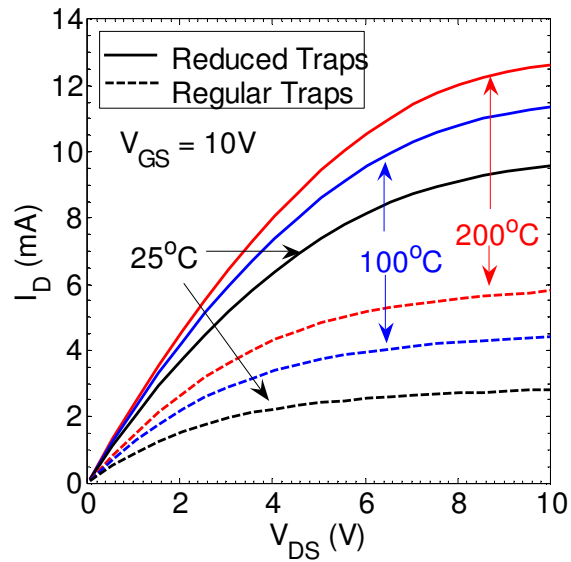


Fig. 2.22 Projected improvement current at three different temperatures, in a 4H-SiC MOSFET on reduction of band-edge density of states of the interface traps by a factor of 10, in the saturation region of operation.

2.6. Quantum Confinement in the Channel and Interface Trap Occupation

The Drift-Diffusion model for device simulation described in the previous sections does not include the effect of quantum confinement in the channel. For thin oxides, channel confinement is an important phenomenon. Quantum confinement pushes electrons away from the interface, and thereby increases the effective oxide thickness. The increase in oxide thickness translates to a lower oxide capacitance (C_{ox}) and lower current in the MOSFET. The current generation SiC MOSFETs have very thick oxides (~50nm). Therefore, an increase in the effective oxide thickness of a few nanometers due to confinement will not noticeably change the transport properties. However, the occupation of interface traps may be change if we considered a quantum confined channel. Here we describe a simple methodology of including quantum effects in SiC MOSFETs and using it to evaluate trap occupation. Our results show that effect of quantum confinement is negligible for the current generation of SiC devices. Finally we will discuss in brief the effect of quantization on channel mobility and how our classical and quantum simulations would affect the extracted values of the physical parameters which determine the scattering rates.

2.6.1. Quantum Correction using Density Gradient Method

To account for quantum effects, we incorporate the density gradient method to add quantum corrections to the calculation of the electron concentration inside the MOSFET channel. Equation (2.26) is the Schrodinger equation describing confinement in

the MOSFET channel. Here x is parallel to the MOSFET channel while y is perpendicular to it. E is the energy of the system, $V(x, y)$ is the potential inside the semiconductor, and ψ is the wavefunction of the electrons confined in this quantum well.

$$\left[-\frac{\hbar^2}{2} \left(\frac{1}{m_x} \frac{\partial^2}{\partial x^2} + \frac{1}{m_y} \frac{\partial^2}{\partial y^2} \right) + V(x, y) \right] \psi(x, y) = E \psi(x, y) \quad (2.26)$$

The square of the wavefunction at each location (x, y) inside the device gives the probability of finding an electron there. This means that the square of the wavefunction is a measure of the electron concentration at any point (x, y) inside the device. In the Density Gradient formalism, the Schrodinger equation is solved approximately by replacing the wavefunction by the square root of the electron concentration. The first term of the Schrodinger equation then becomes the quantum correction that needs to be applied to the current equations to get the quantum confined electron concentration values. We term this as the effective quantum potential ϕ_{QM} . Also, the channel is confined only in the y -direction, and so the quantum potential can be written as [51][52]

$$\phi_{QM} = -\frac{\hbar^2}{2q} \frac{1}{\sqrt{n}} \frac{1}{m_y} \frac{\partial^2 \sqrt{n}}{\partial y^2} \quad (2.27)$$

Here, m_y and n are the electron effective mass and the electron concentration respectively, and \hbar is the reduced Planck's constant.

The quantum-corrected electron current equation is then written as

$$\bar{J}_n = -qn\mu_n \bar{\nabla}(\phi + \phi_{QM}) + qD_n \bar{\nabla}n \quad (2.28)$$

Our new system of equations consists of the Poisson equation, electron and hole continuity equations, and the effective quantum potential equation of equation (2.27).

$$\nabla^2 \phi = -\frac{\rho}{\epsilon} \quad (2.29)$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla \cdot \bar{\mathbf{J}}_n + G_n - R_n \quad (2.30)$$

$$\frac{\partial p}{\partial t} = -\frac{1}{q} \nabla \cdot \bar{\mathbf{J}}_p + G_p - R_p \quad (2.31)$$

We first solve the classical Drift-Diffusion system ($\phi_{QM} = 0$) self-consistently. Then the quantum correction is calculated and the whole system is solved again to include the effects of quantum confinement.

Evaluating the occupation of interface traps involves knowing the surface Fermi level at each position x along the interface. We compare the Fermi level computed in the classical solution and two models for Fermi level computed in the quantum corrected solution. Then the occupation of traps is calculated and compared for the three cases.

2.6.2. Surface Fermi Level Obtained from Classical Solution

The Fermi level at each point along the interface is calculated by using the classical electron concentration at the surface ($n(x,0)$) and the effective density of states at the conduction band minima (N_C) for 4H-SiC as

$$E_F(x) = E_C - \frac{k_B T}{q} \ln\left(\frac{n(x,0)}{N_C}\right) \quad (2.32)$$

2.6.3. Extracting Fermi Level from Confined Inversion Layer

QM Model I: We follow the classical model methodology, but use the quantum surface electron concentration to calculate the Fermi level and thereby determine the trap

occupation. This model does not provide details of the quantization of the conduction band. Due to quantum confinement, the conduction band will be split into quantized levels, thereby moving the conduction band minima to a level higher than E_C . This effect on energy quantization is included in the second quantum trap occupation model.

QM Model II: Taking into account the splitting of the 3D conduction band into 2D sub-bands, the total inversion electron charge density (2-D electron density) for single sub-band occupation is written as [53][54]

$$n_{inv}(x) = \frac{M_C m^* k_B T}{\pi \hbar^2} \ln \left[1 + \exp \left(\frac{E_F(x) - E_1(x)}{k_B T} \right) \right] \quad (2.33)$$

Where, n_{inv} is the 2-D electron inversion charge density, M_C is the valley degeneracy, m^* is the density of states effective mass, k_B is Boltzmann's constant, T is temperature, and E_1 is the first sub-band energy level.

By considering triangular quantum well approximation, the solution of the Schrodinger equation can be given in terms of Airy functions, and the first sub-band minimum can be written in terms of the effective surface electric field (F_s) as [46][53][54]

$$E_1(x) = E_C + \left(\frac{\hbar^2}{2m_y} \right)^{1/3} \left[\frac{9}{8} \pi q F_s(x) \right]^{2/3} \quad (2.34)$$

Here, E_C is the classical conduction band minima, and E_1 is the first sub-band energy level. The sub-band level is a function of position along the channel because the surface field varies from the source to the drain.

Using equations (2.33) and (2.34) and calculating the inversion layer charge density ($n_{inv}(x)$) from the self-consistent solution of electron concentration obtained

through our device simulation, we can calculate the Fermi level that incorporates the effect of quantum confinement.

2.6.4. Comparison of Classical and Quantum Corrected Interface Trap Occupation

Fig. 2.23 shows the electron concentration as a function of depth away from the interface for the classical and quantum corrected cases at a gate-source voltage of 30V. As expected, quantum confinement at large gate bias caused a significant reduction in the electron concentration close to the interface.

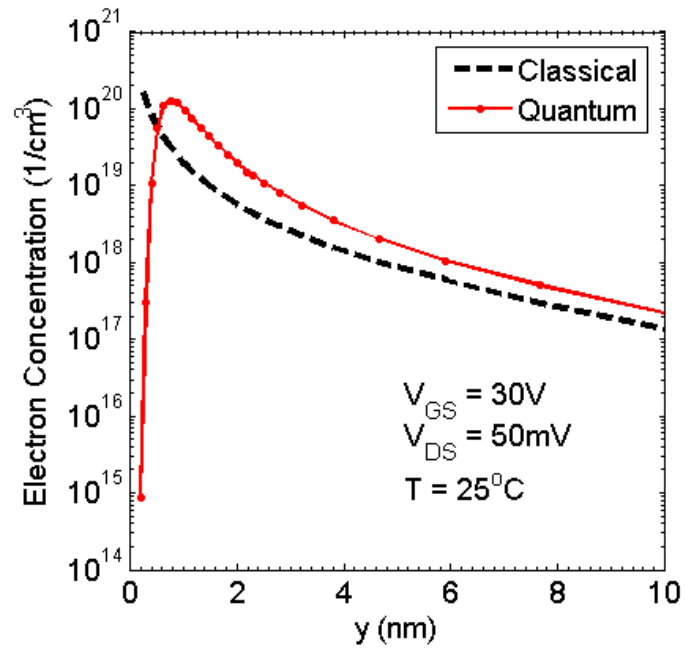


Fig. 2.23 Electron concentration as a function of distance away from the interface. The curve is plotted at the center of the channel.

Fig. 2.24 shows the occupied trap densities for the Classical and the QM Model I. Here, the Fermi level is calculated using the surface electron concentration alone. As the surface electron concentration drops due to quantum effects, for gate-source voltages between 0 and 15V, the occupied trap density predicted by QM Model I, is lower than the classical results. For V_{GS} between 15 and 30V, QM Model I predicts that the occupied trap densities are reduced even more. At higher temperatures, the channel confinement reduces and so the occupied trap densities in the quantum confined case calculated using the surface electron concentration alone, approach the classical values.

The results for lower gate biases seem to make physical sense, in that the quantization tends to move the electrons away from the surface, and so it seems reasonable to expect that quantum confinement gives reduced values of occupied traps. However, as V_{GS} increases above 15V, it also seems reasonable that QM Model I over predicts the reduction in trap occupation. This is likely to be attributable to the fact the QM Model I uses only the surface electron concentration to calculate the Fermi level and ignores the probability of electrons further away from the interface becoming trapped.

Fig. 2.25 shows the trap occupation calculated using the methodology outlined in QM Model II. This approach is more detailed than the previous one, because here we calculate the Fermi level relative to the first sub-band of the quantized conduction band. Furthermore, QM Model II removes the limitations intrinsic to QM Model I, because it allows for electrons in the entire inversion layer to contribute to trap occupation. It seems that physical intuitions would indicate that QM Model II may be over-predicting the population of occupied traps, because it assumes that electrons deeper into the channel

also have a relatively high probability of occupying interface traps. As can be seen from the figure, the calculated trap occupation is slightly higher than the classical case.

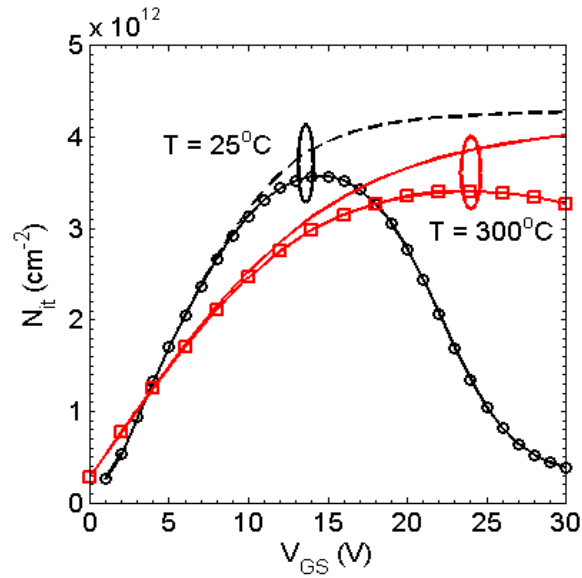


Fig. 2.24 Reduction of trap occupation due to quantum confinement as calculated by QM Model I. (Classical: Lines, QM Model I: Symbols). At high temperatures, trap occupation in the quantum case approaches the classical values.

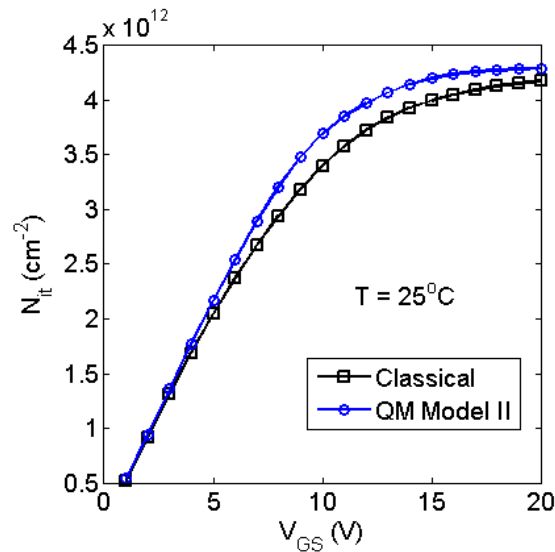


Fig. 2.25 Calculated occupied trap density using QM Model II and compared with the classical case. Slightly higher trap occupation seen in the quantum case at large gate biases.

In Fig. 2.26 we show the simulated I_D - V_{GS} characteristics for the Classical, QM Model I and QM Model II cases. The classical simulation has been fit to the experimental data and used to extract the density of states.

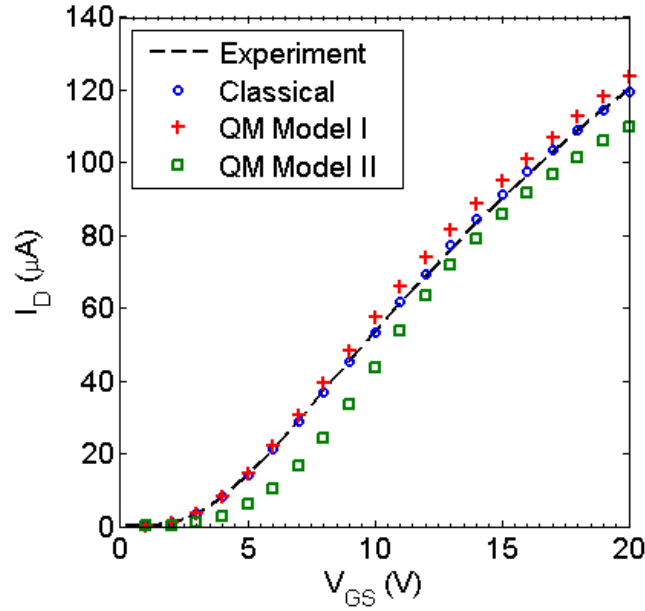


Fig. 2.26 Comparison of simulated room temperature classical and quantum corrected currents in the test 4H-SiC MOSFET to experiment.

We can clearly see that the I_D - V_{GS} curves obtained for the two quantum models differ slightly from the classical case. The difference is less than 10% at all the gate biases. Therefore as had been hypothesized, for thick oxides, quantum confinement effects will not be significant.

2.6.5. Channel Mobility and Quantum Confinement

In our modeling of the channel mobility and its various components, we have mainly considered classical transport. The two main scattering mechanisms responsible for mobility degradation in SiC devices, namely Coulombic scattering from interface traps and surface roughness scattering, are surface mobility models. In case of a quantum confined channel, the electrons will be some distance away from the surface. This means that their interaction with interface traps, and with the surface roughness will be slightly different than in the classical case.

Coulombic scattering from interface traps is only important in the sub-threshold and near-threshold regimes of operation. At these gate biases, the potential well near the surface is very wide, and therefore, quantization of the channel is minimal. In other words, electron concentration at the SiC-SiO₂ interface does not show a sharp decline as shown in Fig. 2.23. Therefore, the amount of Coulombic scattering of the inversion layer electrons in the quantum corrected case does not differ too much from the classical case. Any small difference in the amount of Coulombic scattering seen by the electrons at various depths in the quantum confined case will translate into a slightly higher extracted value of the band-edge interface trap density of states.

At higher gate biases, when quantum confinement is more pronounced and when there is a sharp decline in the electron concentration at the interface, surface roughness scattering is the dominant term. Surface roughness scattering (and therefore surface roughness mobility) is dependent on the perpendicular field. The high surface field extends several nanometers deep into the device away from the interface. Therefore the effect of surface roughness scattering will still be strong at 1-2nm away from the

interface where the electron concentration has its peak value. Thus, in the quantum confined case too, surface roughness scattering will dominate at higher gate biases. The difference between electron concentration at the surface in the classical and quantum confined cases, and the change in surface roughness mobility with depth, would translate to a slightly different value of the root mean square step height of the surface steps.

2.7. SPICE Parameter Extraction

Development of SPICE models for 4H-SiC MOSFETs is an essential first step in designing circuits using these devices. The SPICE models need to be consistent with existing circuit simulators and be based on the same set of rules that are used for traditional silicon devices. This requires having enough data, and consistency among devices and wafers to formulate equations for important circuit design parameters such as threshold voltage, mobility, length scaling, oxide thickness scaling, and others. Commercial parameter extraction tools have been used to extract SPICE parameters for SiC MOSFETs [55]. We have tried to understand the methodology of such parameter extraction tools and implemented them in MATLAB to extract some basic SPICE parameters for 4H-SiC MOSFETs. We show the extracted values for surface charge, substrate doping density, channel length modulation, low field mobility and threshold voltage for a set of devices manufactured on a single wafer. We show the variation of these parameters amongst devices on the same wafer to highlight the inconsistency in manufacturing SiC MOS devices.

2.7.1. SPICE Model Equations

We employ a set of equations to extract four important SPICE parameters, namely low field mobility (U_0), channel length modulation ($LAMBDA$), surface fixed charge (NSS) and channel doping density (NCH). Using these, we also extract two “derived parameters” namely the surface band bending (PHI) and the zero bias threshold voltage (VT_0). The set of equations is given below.

$$\text{PHI} = \frac{2k_B T}{q} \log\left(\frac{\text{NCH}}{n_i}\right) \quad (2.35)$$

$$\text{VT0} = \chi_M - \chi_S - \frac{E_g}{2} + \frac{\text{PHI}}{2} + \frac{\sqrt{2\epsilon_S q * \text{NCH} * \text{PHI}}}{C_{ox}} - q \frac{\text{NSS}}{C_{ox}} \quad (2.36)$$

$$I_D = U0 * C_{ox} * \left(\frac{W}{L}\right) * \left[(V_{GS} - \text{VT0}) * V_{DS_{min}} - V_{DS_{min}}^2 \right] * (1 + \text{LAMBDA} * V_{DS}) \quad (2.37)$$

Equation (2.35) relates the channel doping (NCH) to the derived parameter PHI using the intrinsic carrier concentration of 4H-SiC (n_i). Equation (2.36) relates the threshold voltage to the channel doping, surface charge and material parameters like bandgap (E_g), affinities of the gate metal (χ_M) and 4H-SiC (χ_S), and the oxide capacitance (C_{ox}). Equation (2.37) gives the current in the 4H-SiC MOSFET as a function of the low field mobility (U0), threshold voltage (VT0) and the channel length modulation parameter (LAMBDA). $V_{DS_{min}}$ is the minimum between $V_{GS} - \text{VT0}$ and V_{DS} , and is used to determine whether the MOSFET is in linear region of operation or in saturation. Some of the constants used in the compact model are listed in table below.

Table 2.4 Constants used for compact model and SPICE parameter extraction

Constant	Symbol	Unit	Value
Affinity of Gate Metal	χ_m	eV	4.10
4H-SiC Affinity	χ_s	eV	3.6
4H-SiC Bandgap	E_g	eV	3.26
Oxide Thickness	TOX	nm	50

2.7.2. Simulated Annealing Technique

Extraction of MOSFET parameters from the measured current-voltage data can be thought of as a non-linear least squares optimization problem. General purpose optimization techniques can be used to obtain values for a complete set of model parameters in a single operation. This is accomplished by simultaneously adjusting the values of all parameters to produce a nonlinear least squares fit of the model to a set of measured device characteristics.

\mathbf{p} is the vector of the parameters to be optimized. $f(\mathbf{p})$ is the error evaluated at each data point. The quantity to be minimized is given as [56]

$$Q = \|f(\mathbf{p})\|^2 = \sum_k f_k(\mathbf{p})^2 \quad (2.38)$$

where,

$$f_k(\mathbf{p}) = \frac{I_k(\mathbf{p}) - I_k^{measured}}{I_{min}} \quad (2.39)$$

I_k is the calculated drain current and $I_k^{measured}$ is the measured drain current at the k^{th} data point. The data points are the bias voltages at which measurements have been taken. I_{min} is a scaling factor.

The problem of parameter extraction for MOSFETs is a multi-minima non-linear least squares optimization problem. One possible solution to such a problem is to employ stochastic optimization technique such as the Simulated Annealing (SA) method [57]. Given infinite time, the SA method will converge to the globally optimal solution.

SA method is a stochastic method which simulates the annealing process in thermodynamics. It was developed by observing that there is a useful connection between statistical mechanics, in which systems have many degrees of freedom at a given

temperature, and minimization of a function dependent on many parameters. It has been applied successfully to solve many VSLI physical design optimization problems.

In the SA method, each new search step is determined randomly. If the error cost function reduces, the search step is accepted. Further, if there is an increase in the error cost function, then based on a probability function, the search step can be accepted. The probability function which decides whether such a step is accepted or not depends on the current annealing temperature

$$\text{if } P = \exp\left(-\frac{Q^{new} - Q}{T_{SA}}\right) > r, \text{ where } r \text{ is a random number between 0 and 1, then the}$$

step will be accepted.

The key to have a good SA method based minimization program is the cooling schedule. The algorithm will start with a large value of T_{SA} and gradually lower it as the iteration process progresses. When T_{SA} is large, the algorithm is unlikely to become trapped in local minima of Q , since the perturbations which increase Q can be accepted. A fixed number of random perturbations are allowed to occur at each temperature. After that, the temperature is reduced according to the cooling schedule. If the temperature is reduced too quickly, the optimized solution will not be reached.

The cooling schedule that gave the best results on both counts is to use $T_{SA}^{new} = \alpha T_{SA}$, with $\alpha = 0.95$.

2.7.3. SPICE Parameter Extraction Results

We extracted SPICE parameters for 14 4H-SiC MOSFETs with varying widths and lengths. All the MOSFETs were fabricated on one wafer in form of two separate chips, each containing seven devices. Fig. 2.27 shows the simulated and measured I_D - V_{DS}

characteristics of a few these MOSFETs. We get appreciable match between the simulated and experimentally measured data. It seems to be a very good match considering we only used four fitting parameters.

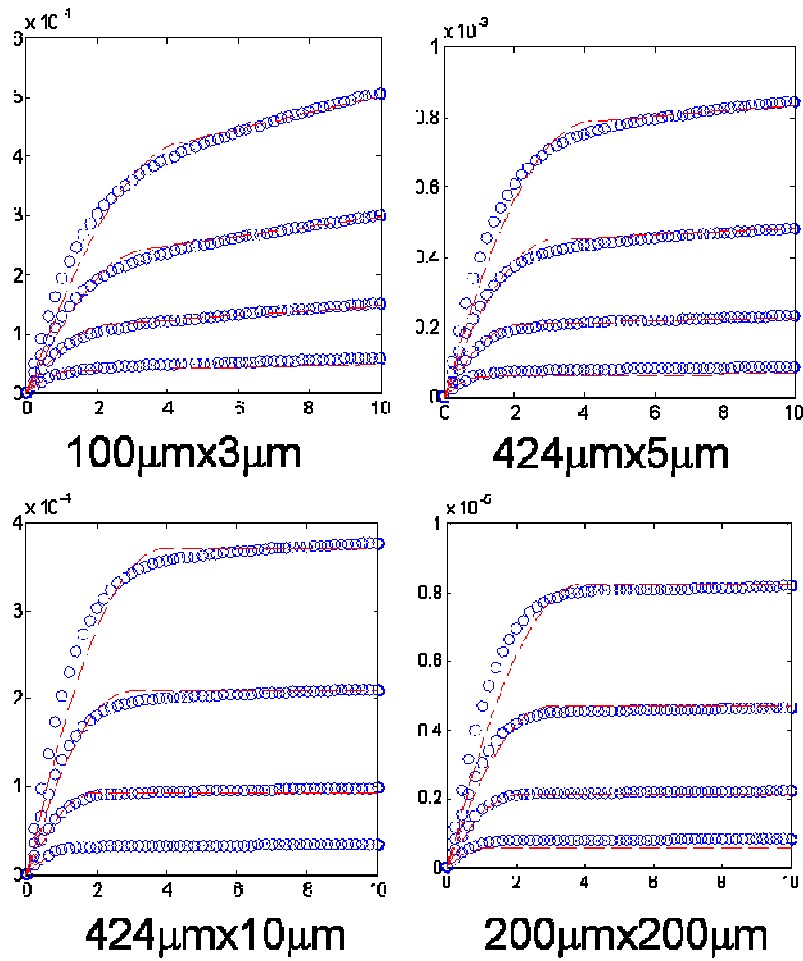


Fig. 2.27 Fits obtained to experimental I_D - V_{DS} curves using simulated annealing parameter extraction methodology for 4H-SiC MOSFETs. The circles are simulations and the dashed lines are experimental data.

Fig. 2.28 and Fig. 2.29 show the extracted threshold voltage and low field mobility respectively, for a set of seven devices. The x axis in the figures shows the sizes of the MOSFETs in microns ($W \times L$). As can be seen from the plots, the threshold voltage and the low field mobility vary significantly across the chip. The data is not sufficient to extract any statistical understanding for the parameters, but it clearly highlights the inconsistency in making these devices. The different threshold voltages may be attributed to variation of interface trap density of states across the wafer, while the variation in mobility may be attributed to both, variation in trap density and variation in surface roughness.

Fig. 2.30 and Fig. 2.31 show the variation in threshold voltage and channel doping respectively for the two chips containing seven devices each. The intra-chip and inter-chip variations are clearly seen. The manufacturer provided us with an approximate channel doping density of $5 \times 10^{15} \text{cm}^{-3}$. Our extracted channel doping densities are close to this number.

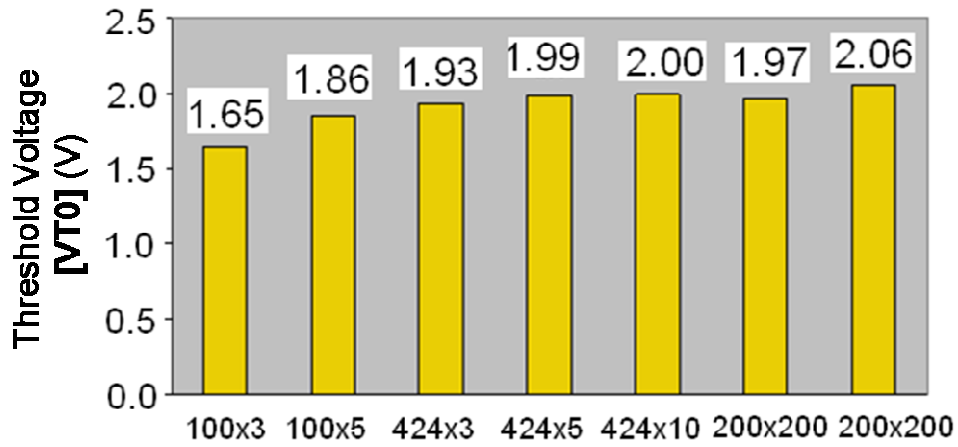


Fig. 2.28 Extracted values for the zero order threshold voltage for seven 4H-SiC MOSFETs on one chip.

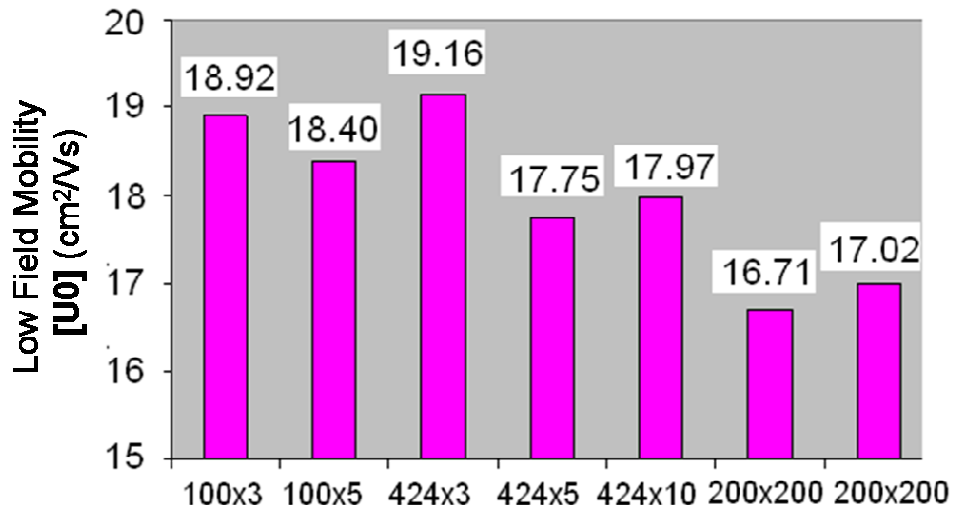


Fig. 2.29 Extracted values for the low field mobility for seven 4H-SiC MOSFETs on one chip.

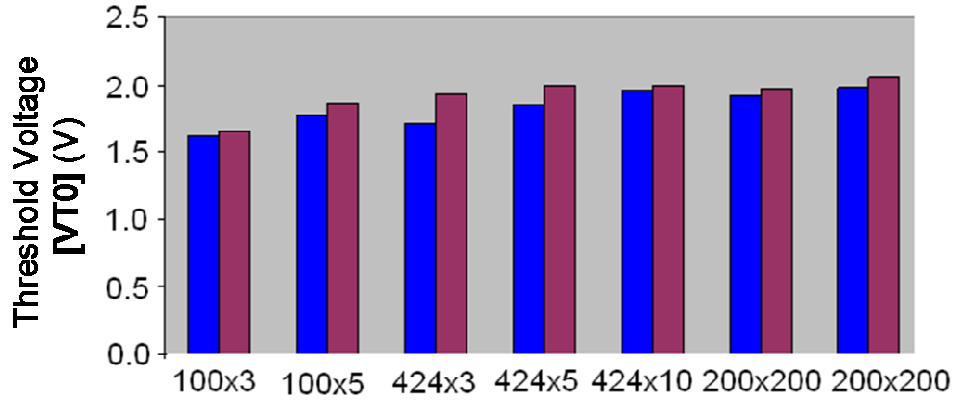


Fig. 2.30 Extracted zero order threshold voltage for two sets of 4H-SiC MOSFETs on two separate chips fabricated on the same wafer. Variability is seen between intra-chip and inter-chip devices.

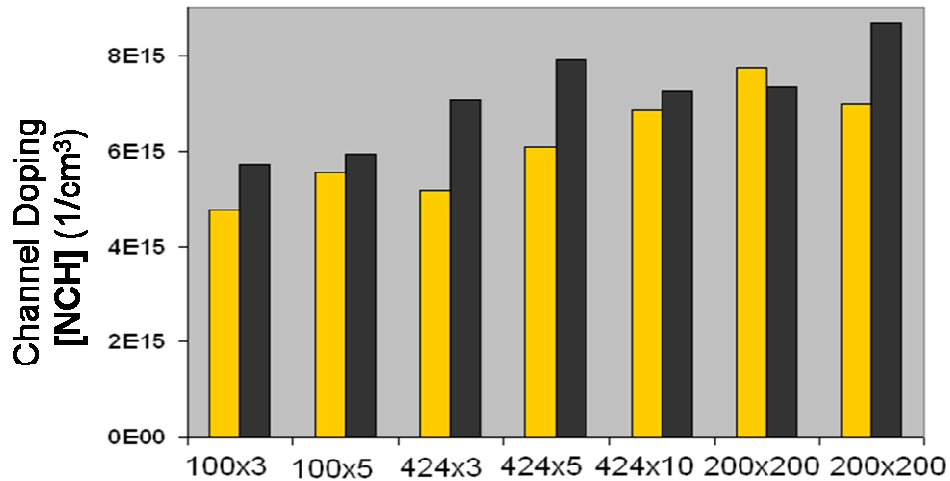


Fig. 2.31 Extracted channel doping density for two sets of 4H-SiC MOSFETs on two separate chips fabricated on the same wafer. Variability is seen between inter-chip and intra-chip devices.

2.8. Chapter Summary

We discussed high field high temperature 2D Drift-Diffusion based modeling and simulation of 4H-SiC lateral MOSFETs with emphasis on developing physics based models for interface traps and surface roughness scattering mobility.

Our simulations and comparison to experiment showed that interface trap occupation up to 200°C causes a reduction in the mobile charge in a 4H-SiC MOSFET leading to low current. A spreading of the band-tail states of the interface trap distribution inside the bandgap was also observed and quantified. Extracted trap density of states showed band-edge values close to the mid $10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ range whereas mid-gap values are close to the low $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ levels.

We showed that surface roughness scattering is the dominant mobility degradation mechanism. Extracted values of surface step height of approximately 3.5nm suggest presence of step bunching, and/or a Si-C-O transition layer at the SiC-SiO₂ interface. Detailed analysis of the mobility inside the device showed that screening plays a very important role in surface scattering.

Surface electron mobilities were found to be as low as 20 cm^2/Vs at room temperature.

High temperature simulations showed that current increases with rise in temperature in 4H-SiC lateral MOSFETs. This effect is primarily due to the reduction in trap occupation and consequent increase in mobile inversion charge at higher temperatures.

We also implemented the density-gradient method for solving the Schrodinger equation inside the MOSFET channel and showed that that due to the large oxide

thickness of approximately 50nm, quantum effects in the channel do not have a significant impact on trap occupation and current in the MOSFETs.

Finally, we implemented a genetic algorithm to extract SPICE parameters for 4H-SiC lateral MOSFETs. We find that extracted values for low field mobility, threshold voltage, and channel doping vary significantly across a chip and between chips on the same wafer.

Chapter 3

3. Dynamics of Trap Occupation and Time Dependent Characterization of 4H-SiC MOSFETs

The applications of SiC MOSFETs are going to be in power switching circuits that would alleviate the need of having bulky transformers. Recent measurements of threshold voltage instabilities by fast I-V methods have shown that the SiC-SiO₂ interface not only contains fast interface traps, but also slower near-interface and oxide traps [21][23][24]. Steady state modeling and simulations cannot characterize the effects of each of these defects. So, the switching or transient characterization of these devices is necessary. We have developed time dependent trap occupation models and carried out transient experiments to evaluate the switching properties of 4H-SiC MOSFETs. Using our dynamic trapping models, we can also extract physical parameters like the trap capture cross-sections of the interface and near-interface traps.

Experimental and analytical work on extracting the trap distribution in Si and SiC devices had been carried out by using various techniques including fast I-V , capacitance-voltage (C-V) and conductance-voltage (G-V) measurements; charge pumping; deep-level transient spectroscopy; and isothermal capacitance transient spectroscopy, among others [58][59][60][61][62][63]. In all the techniques, assumptions have to be made for the location of the Fermi level, or the amount of band-bending, or the trap cross-section in order to extract the trap density of states using this technique. We do

not need to make any such assumptions as we solve for the Fermi level, the number of occupied traps, the number of surface electrons and the surface potential self-consistently.

We have developed an algorithm that can be used to study the dynamics of the interface traps. The algorithm uses a time dependent trapping and generation-recombination model which provides information of trap occupation as a function of both, time and energy. While the model provides details of the dynamics of trapping in energy and time, it also fits into standard device simulation methodologies. It does not need to make any assumptions regarding the surface potential, the band bending or the trap cross-sections. We independently evaluate the trap density of states and the trap cross-section areas by comparing steady state DC simulations and transient simulations to experimental I_D-V_{GS} and I_D-t data.

3.1. Generation-Recombination Model and Time Dependent Trap Occupation

In an equilibrium scenario, the occupation of the interface traps distributed in energy space can be defined using an energy-dependent occupation probability that is associated with the location of the Fermi level at the surface. The Fermi level for electrons at the surface and for the interface traps will be the same under equilibrium conditions, enabling us to calculate the occupation of traps if the surface electron concentration (or Fermi level) is known.

However, when the MOSFET is subject to a switching signal at the gate, the surface electron concentration may change at a different rate than the rate of occupation of the interface traps. So, using the surface electron Fermi level directly to calculate the trap occupation will not give the correct dynamics of trapping. Therefore, we use a different formalism to write the time dependent occupation of interface traps, wherein the occupation of a trap at an energy E_t in the bandgap at a given time depends upon the occupation at that energy at a previous time and the rate at which surface electrons become trapped.

We begin by defining the rate of change of occupied trap density $\frac{\partial n_{it}(E_t, t)}{\partial t}$ at energy E_t , as the net capture/emission rate of surface electrons $u_{ce}(E_t)$.

$$\frac{\partial n_{it}(E_t, t)}{\partial t} = u_{ce}(E_t) \quad (3.1)$$

Our goal now is to derive an expression for this net capture/emission rate $u_{ce}(E_t)$ of electrons at the surface. As explained later in this paper, this is incorporated into our

device simulator to study the dynamics of interface trap occupation. (Note that since $u_{ce}(E_t)$ is only dependent on time implicitly, we have dropped time (t) from the function's argument.)

We model this capture/emission of an electron at the SiC-SiO₂ interface as a generation-recombination phenomenon between a trap and a surface electron in the device. This generation-recombination is quantified using a methodology similar to the Shockley-Hall-Read and the Boltzmann's equation-based formalisms employed to obtain expressions for bulk generation-recombination [64][65]. Here, the capture of a channel electron by an interface trap is represented as a recombination event at the surface, and the emptying of an interface trap into the semiconductor is viewed as a generation event.

3.2. Derivation of Expression for the Generation-Recombination

Rate $u_{ce}(E_t)$

Recombination is defined as the capture of a surface electron by an unoccupied trap. This recombination rate is therefore proportional to the number of occupied electron states and the number of unoccupied trap states, with a proportionality factor (capture probability) $c_n(E, E_t)$. For a trap energy level E_t , the density of unoccupied or free trap states $n_{it}^{empty}(E_t)$ is calculated using the density of states for the interface traps $D_{it}(E_t)$ and the probability of occupation of the traps $f_t(E_t)$

$$n_{it}^{empty}(E_t) = [1 - f_t(E_t)] D_{it}(E_t) dE_t \quad (3.2)$$

Similarly, the number of occupied electron states $n(E)$ at a given energy E is found using the conduction band density of states for electrons $g(E)$, and $f(E)$ which is the occupation probability of the electron state at energy E .

$$n(E) = f(E) g(E) dE \quad (3.3)$$

Thus, the rate of capture (recombination) of electrons at energy E into unoccupied interface traps at energy E_t , is written as the product of the right hand sides of equations (3.2) and (3.3) and the energy dependent capture probability $c_n(E, E_t)$ as

$$du_c(E, E_t) = [(1 - f_t(E_t)) D_{it}(E_t) dE_t] \cdot [f(E) g(E) dE] \cdot c_n(E, E_t) \quad (3.4)$$

Likewise, the emission (generation) rate of electrons from traps, is proportional to the number of occupied interface traps at energy E_t , and the number of free electron states at energy E , with the energy dependent emission probability $e_n(E, E_t)$ as the proportionality factor.

$$du_e(E, E_t) = [f_t(E_t) D_{it}(E_t) dE_t] \cdot [(1 - f(E)) g(E) dE] \cdot e_n(E, E_t) \quad (3.5)$$

The net generation-recombination rate for the capture-emission process between a trap at energy E_t and a surface electron at energy E , is then given as the difference of the capture and emission rates. Writing this difference and canceling out the common terms gives the generation-recombination rate below.

$$du_{ce}(E, E_t) = [(1 - f_t(E_t)) f(E) c_n(E, E_t) - f_t(E_t) (1 - f(E)) e_n(E, E_t)] \cdot D_{it}(E_t) dE_t g(E) dE \quad (3.6)$$

To simplify this expression, we first eliminate one of the two proportionality factors by determining a relationship between them. This gives the generation-recombination rate using only the capture probability $c_n(E, E_t)$. We then write the capture probability $c_n(E, E_t)$, which depends on trap energy and electron energy, as a product of two functions; the trap energy dependent effective trap capture cross-section $A_{it}(E_t)$ and the average thermal velocity $\langle v_{th} \rangle$ of electrons at all energies in the conduction band. Integration over the free electron energy provides an expression for the net generation-recombination rate ($u_{ce}(E_t)$) for traps at energy E_t . This expression involves the density ($D_{it}(E_t)$) and effective capture cross-section ($A_{it}(E_t)$) of traps at E_t , trap occupation probability ($f_t(E_t)$), and the electron concentration (n) in the channel. For the sake of clarity, we have put the details of this derivation in the Appendix. The final expression obtained for the net generation-recombination at a trap energy level E_t is given below. Here, N_C is the effective conduction band density of states for electrons and E_C is the conduction band minimum.

$$u_{ce}(E_t) = \langle v_{th} \rangle \cdot [D_{it}(E_t) A_{it}(E_t) dE_t] \cdot \left[n(1 - f_t(E_t)) - \frac{1}{2} N_C f_t(E_t) \exp\left(\frac{E_t - E_C}{k_B T}\right) \right] \quad (3.7)$$

The expression derived above gives the net generation-recombination rate for the mechanism of capture of surface electrons into interface traps, and emission of electrons from the occupied traps to the semiconductor, for traps located at different energy levels E_t in the 4H-SiC bandgap.

The total generation-recombination rate involving the traps located at all the energy levels in the 4H-SiC bandgap is calculated by integrating the trap energy dependent generation-recombination rate of the above equation, over all trap energies from the neutrality point ($E_{neutral}$) to the conduction band minimum (E_C).

$$U_{ce} = \langle v_{th} \rangle \int_{E_{neutral}}^{E_C} D_{it}(E_t) A_{it}(E_t) \left[n(1 - f_t(E_t)) - \frac{1}{2} N_C f_t(E_t) \exp\left(\frac{E_t - E_C}{k_B T}\right) \right] dE_t \quad (3.8)$$

It is important to emphasize that two critical functions have been obtained in this section. The above equation gives the total generation-recombination rate between channel electrons and traps. This expression is incorporated in to the electron current continuity equation of the standard Drift-Diffusion model to self-consistently account for trapping and de-trapping of channel electrons. Meanwhile, equation (3.7) yields the expression for the filling and emptying of interface traps distributed at each energy level inside the bandgap. This is used to calculate the dynamical filling of traps in energy and time, as will be discussed below.

3.3. Time Dependent Trap Occupation

The trap energy dependent generation-recombination rate of equation (3.7) is used to evaluate the trap occupation at each energy level in the 4H-SiC bandgap in the MOSFET as a function of time. The number of occupied traps at energy E_t and time $t+\Delta t$ can be written using Taylor's series expansion as:

$$n_{it}(E_t, t + \Delta t) = n_{it}(E_t, t) + \Delta t \cdot \frac{\partial n_{it}(E_t, t)}{\partial t} + O(\Delta t^2) \quad (3.9)$$

As the change in number of occupied traps over time has been defined as the capture/emission rate (equation (3.1)), the above expression is written using the generation-recombination term of equation (3.7) as:

$$n_{it}(E_t, t + \Delta t) = n_{it}(E_t, t) + \Delta t \cdot u_{ce}(E_t) + O(\Delta t^2) \quad (3.10)$$

To determine the dynamics of trap occupation, it is actually prudent to not solve for $n_{it}(E_t, t + \Delta t)$ directly, but obtain the time dependent trap occupation probability at each energy E_t . The occupied trap density can be written using the density of states and the trap occupation probability as:

$$n_{it}(E_t) = D_{it}(E_t) f_t(E_t) \Delta E_t \quad (3.11)$$

Now, by using the expression for $u_{ce}(E_t)$ in equation (3.7), as well as the relationship between occupied trap density and the trap occupation probability described above, the time dependence of occupation probability at each energy E_t inside the bandgap is written as:

$$f_t(E_t, t + \Delta t) = f_t(E_t, t) + \Delta t \cdot \frac{u_{ce}(E_t)}{D_{it}(E_t)\Delta E_t} + O(\Delta t^2) \quad (3.12)$$

Finally, the total occupied trap density at a given time t is written by summing over all trap energies as:

$$N_{it}(t) = \sum_{E_{neutral}}^{E_c} D_{it}(E_t) f_t(E_t, t) \Delta E_t \quad (3.13)$$

Having derived these expressions, we incorporate them into the drift-diffusion system of equations, and solve them numerically to obtain the time dependent behaviour of the carrier concentration, electrostatic potential, internal current densities, terminal currents and the occupied trap density, in a 4H-SiC MOSFET. In addition, by using equation (3.7) for the trap energy dependent generation-recombination rate, along with equation (3.12), the trap occupation probability at each trap energy level inside the 4H-SiC bandgap as a function of time is obtained. This allows us to track which trap levels in the bandgap become occupied first, and which ones take more time to be filled. We thereby generate a time dependent profile of the occupation of interface traps distributed in the bandgap of 4H-SiC.

3.4. Simulation Methodology and Algorithm

To simulate the device performance we solve the Drift-Diffusion model for 4H-SiC MOSFETs in two-dimensional space and time. This highly nonlinear model consists of a system of coupled partial differential equations, consisting of the Poisson, and Current-Continuity equations for electrons and holes. As part of the drift diffusion scheme, the time dependent occupied trap density ($N_{it}(t)$) of equation (3.13), and the total generation-recombination rate (U_{ce}) of equation (3.8) are incorporated into the Poisson and Electron Current Continuity equations, respectively. The Poisson equation for the interface can be written as

$$\epsilon_{SiC} \nabla \phi - \epsilon_{ox} \nabla \phi = -q(N_f - N_{it}(x, t)) \quad (3.14)$$

where, ϵ_{SiC} and ϵ_{ox} are the permittivities of 4H-SiC and SiO₂ respectively, N_f is the fixed charge at the interface, $N_{it}(t)$ is the occupied trap density at time t , and ϕ is the electrostatic potential.

The electron current continuity equation now incorporates the total recombination rate due to interaction between electrons and interface traps given by equation (3.8). Thus we write the new current continuity equation for electrons as

$$\frac{\partial n}{\partial t} = \frac{1}{q} \bar{\nabla} \cdot \bar{J}_n + (G - R)_{SRH} + (G - R)_{AUG} - U_{ce}(t) \quad (3.15)$$

The algorithm for the transient simulation is shown in form of a flowchart in Fig. 3.1. We start by setting up the device with an initial gate bias of 0V and the drain bias of 0.5V as in the experiment, and solve the Drift-Diffusion equations in steady state to

obtain the initial solution. This gives us the value for the occupied interface trap density at the initial biases, which is used to calculate the occupation probability $f_t(E_t)$ at time $t=0$. Using initial values of $f_t(E_t)$, and the initial electron concentration (n), we calculate the generation-recombination rate $u_{ce}(E_t)$ at each trap energy and the total generation-recombination rate U_{ce} at time $t=0$ using equations (3.7) and (3.8), respectively.

Now begins the time loop of our transient simulation. First, the time t is incremented and the gate bias is updated. The next step is to solve the Drift-Diffusion equations at this new time instant. At each iteration, while solving for the electrostatic potential (ϕ), electron concentration (n) and hole concentration (p), we use the current values of the electron concentration, and the occupation probability of the previous time step, to evaluate the trap energy-dependent generation-recombination rate and the net generation-recombination rate. Once convergence is reached for ϕ , n and p , the new occupation probability at each trap energy level (E_t) is calculated using equation (3.12), and the new occupied trap density is calculated by equation (3.13). Finally, the current density inside the device and terminal currents are calculated. Thus the trap dynamics and the behavior of device at a specific instant in time have been evaluated. We then repeatedly evaluate the time-loop for the duration required to resolve the transient dynamical response of the interface traps and the overall device

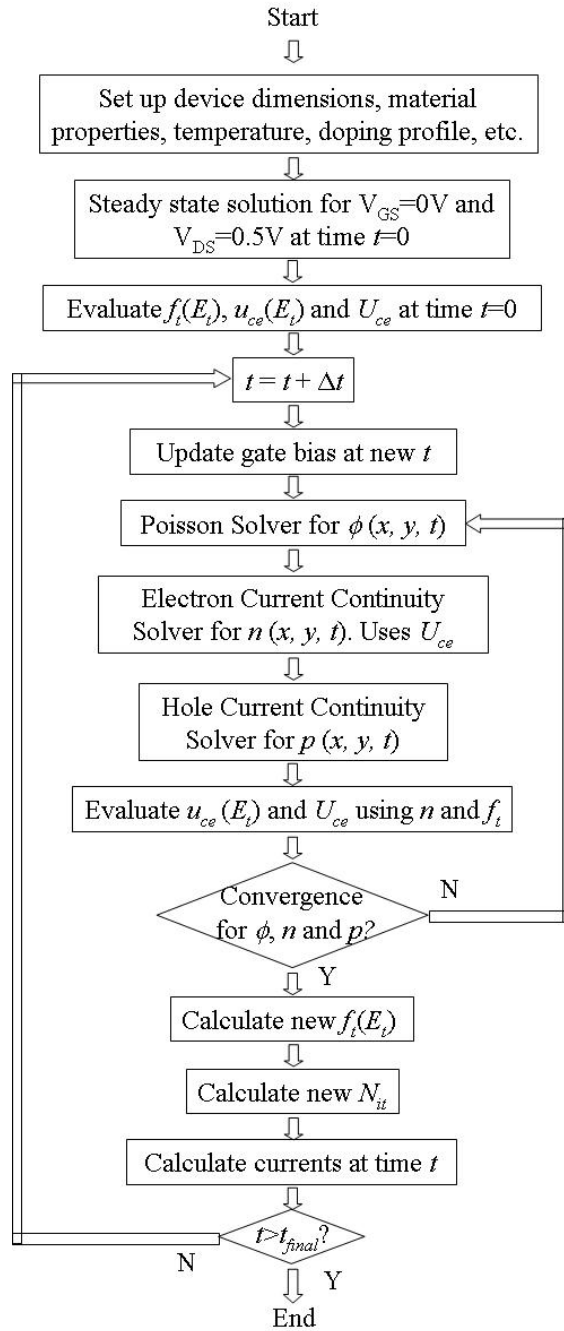


Fig. 3.1 Flowchart showing the methodology for transient simulation of 4H-SiC MOSFETs with time dependent trap occupation and the trap-surface electron generation-recombination models.

3.5. Experiment and Measurement

We have carried out experiments to measure the transient behavior of 4H SiC MOSFETs. The experiments have been carried out at UMD and NIST, Gaithersburg, MD.

In order to calibrate our model, and to extract the cross-sectional area for the interface traps as a function of energy, we carried out experiments to measure the transient current response of 4H-SiC MOSFETs. Using various circuits, we have tried to measure the drain current of a 4H-SiC MOSFET under fixed drain-source bias and a pulsed gate voltage signal. We observed that the MOSFET drain current shows an initial peak and then a slow decay to the steady state level on application of a fast gate pulse. We then performed simulations for the same device using the same biasing and gate pulse conditions to match the experimental measurement. This enabled us to extract the trap cross-section area for the interface traps.

The interface traps, especially the ones near the band-edge, react very quickly to the applied gate pulse. So in order to characterize them, the requirement for the rise time of the gate pulse was to be much less than the response time of the fast traps. Hence, we require gate pulses with rise times less than a nanosecond. Unfortunately, we have not been able to carry out error free measurements for such a fast pulse. Effects of stray capacitance, displacement current due to the large MOSFET capacitances (owing to large sized MOSFETs), and inductance of the measurement probes and cables, have stopped us from going below 100ns rise times. But, even then, we have been able to characterize the interface trap cross-section to a certain degree of satisfaction.

3.5.1. Circuit for transient measurement

Fig. 3.2 shows the schematic for a circuit used to measure the transient drain current in the 4H-SiC MOSFET.

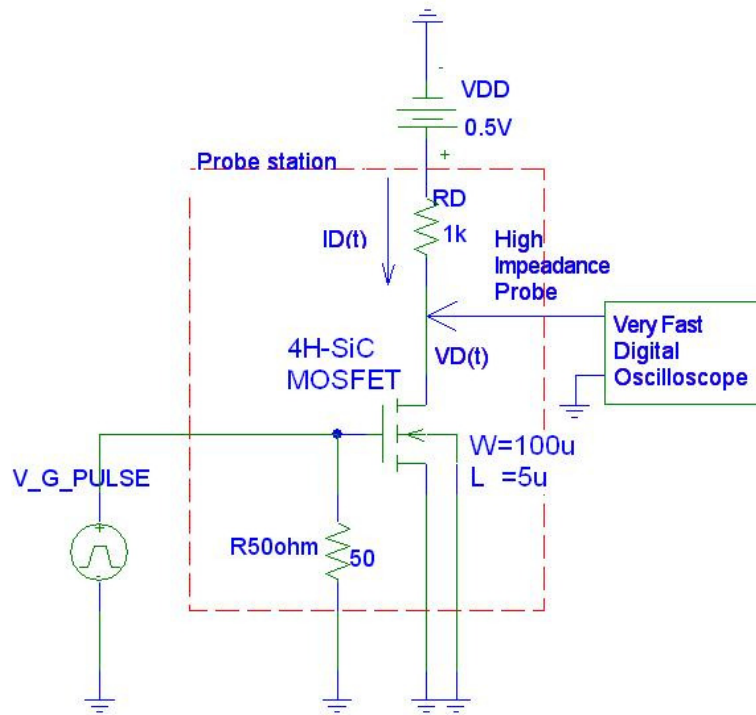


Fig. 3.2 Circuit used for transient current measurement in 4H-SiC MOSFETs

A fast pulse is applied to the gate of the MOSFET and the voltage at the drain resistor is measured using a fast digital oscilloscope. This gave us the measure of the drain current. Care was taken to minimize any stray capacitances and inductances that may affect the results. The circuit was kept as close to the probe station's probe as possible with high impedance low capacitance probe used to measure the drain voltage. The drain current is given as:

$$I_D(t) = \frac{V_{DD} - V_D(t)}{R_D} \quad (3.16)$$

To account for the change in drain current due to change in V_{DS} , a correction is applied to the drain current as:

$$I_D^{corr}(t) = I_D(t) \times \frac{V_{DD}}{V_D(t)} \quad (3.17)$$

The applied gate pulse had rise time of a 100ns and was from 0V to 5V. The drain resistance was chosen to give appreciable change in the drain voltage that could be easily detected and was well above the noise level for the oscilloscope.

3.5.2. Other Circuits

We also experimented with other circuits at NIST that enabled us to use SMA connectors for error free measurement of the rapidly changing transience in the drain voltage. But these circuits necessitated the use of operational amplifiers which were not fast enough for our sub 100ns fast pulse response measurement criteria.

We used an operational amplifier with a 1GHz unity gain bandwidth in the difference amplifier configuration shown in Fig. 3.3 to measure the fast transient drain voltage. This enabled us to use SMA cables instead of the high impedance probes for measuring the drain voltage. This configuration worked quite well for gate pulse rise times as low as 250ns, but was not good enough for the sub 100ns requirement we had. Fig. 3.4 shows the PCB layout for the difference amplifier. Care was taken to minimize stray capacitance and inductance on the PCB. The entire PCB was placed inside a shielded cage of the probe inside the probe station. The PCB layout was done using EAGLE layout tool.

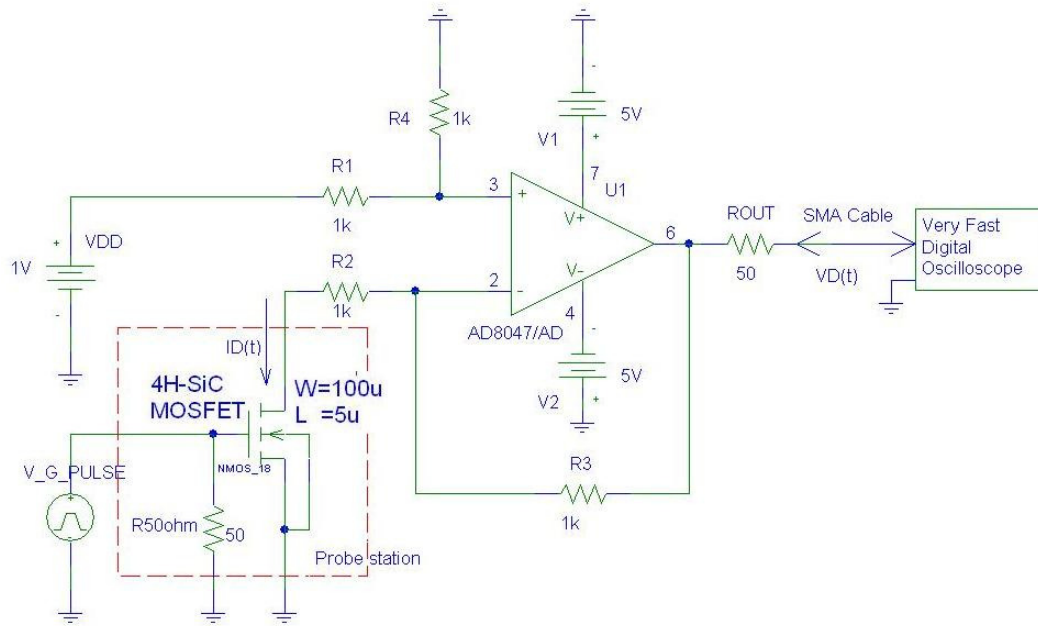


Fig. 3.3 Difference amplifier circuit used for transient current measurement of 4H-SiC MOSFETs.

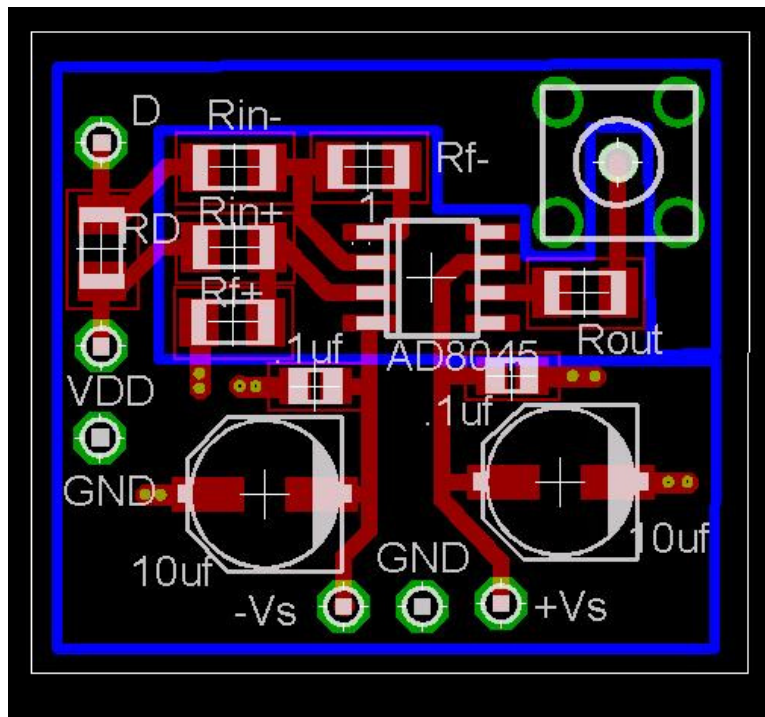


Fig. 3.4 Board layout for the difference amplifier used for transient current measurement.

3.6. Comparison of Simulation and Experimental Results and Parameter Extraction

The extraction of the underlying physics governing the transient behavior of SiC MOSFETs is carried out according to a systematic algorithm. The two unknown quantities that are responsible for the dynamic occupation of interface traps are the density of states and the effective capture cross-sections of the interface traps. We extract them individually by carrying out steady state and transient simulations.

3.6.1. Extracting Interface Trap Density of States ($D_{it}(E_t)$)

First, DC I_D - V_{GS} measurements and simulations are carried out to extract the trap density of states using methods we have reported previously. Interface trap density of states is typically modeled as having a flat distribution in the midgap and an exponential increase near the band-edges

$$D_{it}(E_t) = D_{it}^{mid} + D_{it}^{edge} \cdot \exp\left(\frac{E - E_C}{\sigma}\right) \quad (3.18)$$

Here, D_{it}^{mid} is the midgap density of states, D_{it}^{edge} is the band-edge density of states and σ is the band-tail energy.

A close correlation between the measured current and the simulated current in subthreshold and near-threshold regions gives us the values for the midgap and band-edge density of states, and the band-tail energy for the interface traps. In steady state DC, the measurement times are so large that all the traps located at all different energy levels can react to the applied bias completely. Therefore, the time-dependence of trap occupation, and capture cross-sections play a negligible role in the measured current

value. Thus, we can independently extract $D_{it}(E_t)$ using DC I_D - V_{GS} measurement and simulation.

The extracted interface trap density of states, as well as the comparison between simulated and experimentally measured DC drain current versus gate voltage (I_D - V_{GS}) characteristics of the tested $100\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET are shown in Fig. 3.5. The band-edge interface trap states are mainly responsible for mobility degradation and low currents in 4H-SiC MOSFETs. They also play the major role in determining the transient characteristics in these devices.

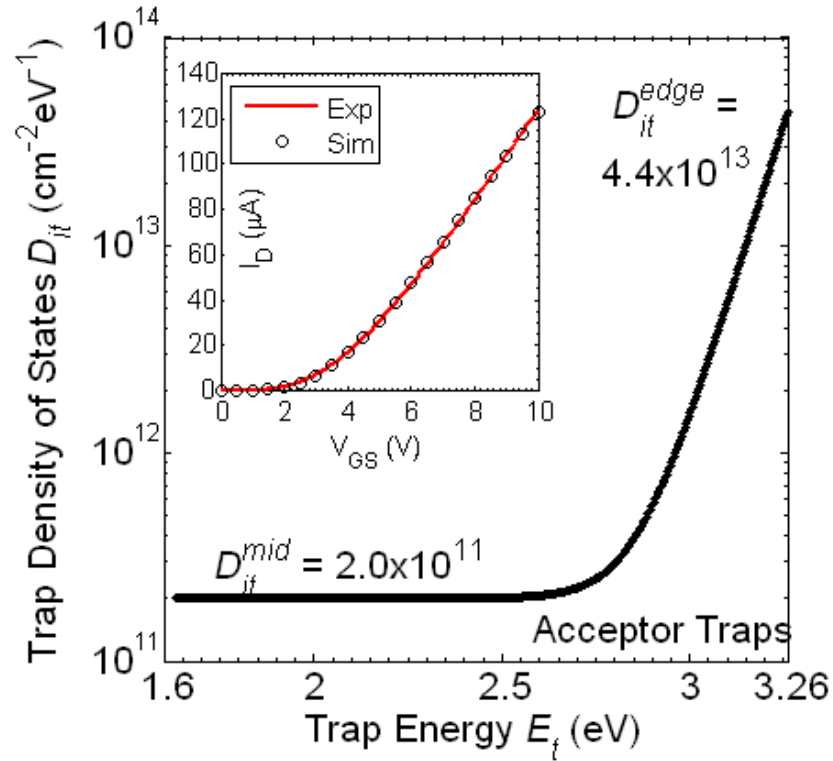


Fig. 3.5 Extracted $D_{it}(E_t)$ profile for acceptor type traps in a 4H-SiC MOSFET from DC drain current versus gate voltage (I_D - V_{GS}) comparison to experiment (inset). The extracted values for the midgap density of states D_{it}^{mid} , the band-edge density of states D_{it}^{edge} , and the band tail energy σ , are $2.0 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, $4.4 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$ and 75meV, respectively.

3.6.2. Extracting Energy Dependent Trap Effective Capture Cross-sections

$$(A_{it}(E_t))$$

Fig. 3.6 shows the simulated and experimentally measured transient current flowing through the 4H-SiC MOSFET on application of a 0-5V gate pulse with a rise time of 100ns. Initially, the current rises very quickly and reaches a peak because the interface traps respond slowly as compared to the inversion layer formation. As the traps get filled, conduction electrons become trapped and so the current decays to its steady state value.

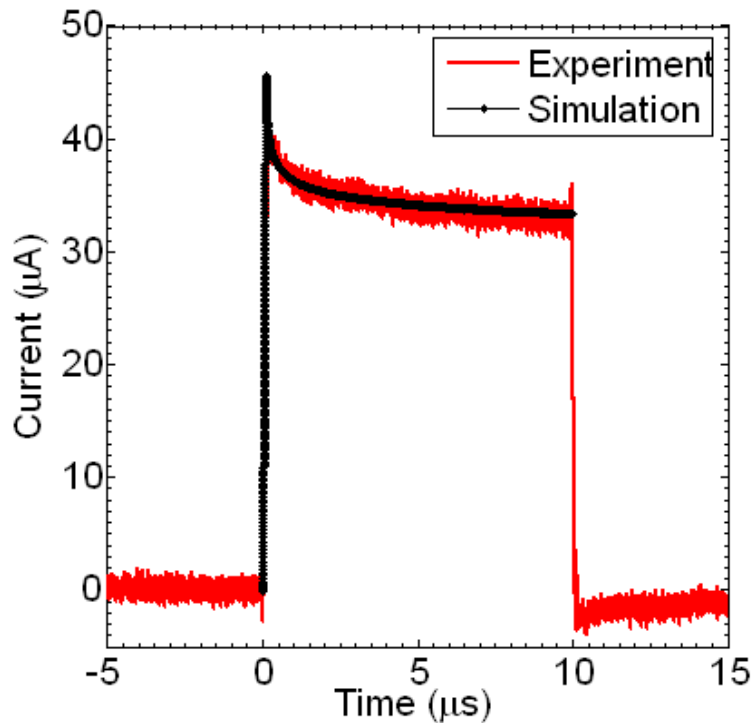


Fig. 3.6 Experimental and simulated transient current responses of a 4H-SiC MOSFET. The gate was pulsed from 0V to 5V with a rise time of 100ns. The simulated curve follows the experimental measurement; thereby verifying the dynamic trapping and generation-recombination models, and allowing us to extract the energy dependent trap capture cross-section profile.

From our transient simulations and comparison to experiment, we extract the trap capture cross-sections. The peak of the drain current is limited by the fastest traps, which are ones with the largest capture cross-sections. Therefore values for the capture cross-sections ($A_{it}(E_t)$) for the fast traps are extracted by comparing simulated and measured peak currents. On the other hand, the slow decay in the current is due to the filling of interface traps with smaller capture cross-sections or oxide traps. So, capture cross-sections for the slow traps are extracted by comparing the simulated and measured current decays. Since the capture cross-section relates to both interface and oxide traps, we will refer to $A_{it}(E_t)$ as an *Effective Capture Cross-section*. The values for effective capture cross-sections that provide agreement between experiment and simulation are shown in Fig. 3.7. The characteristics of this curve indicate two distinct general energy regions in the 4H-SiC bandgap for capture cross-sections. The traps near the band-edge show a large capture cross-section, while those approximately 0.3eV away exhibit much smaller capture cross-section. The traps lying near the band-edge behave as fast interface traps, whereas those lying towards the middle of the bandgap behave as slower interface traps, and oxide traps. The traps lying below 2.6eV are always completely filled at the range of applied gate biases, and hence have minimal effect on the transient response of the system. Therefore, we show capture cross-sections for energies higher than 2.6eV in this figure.

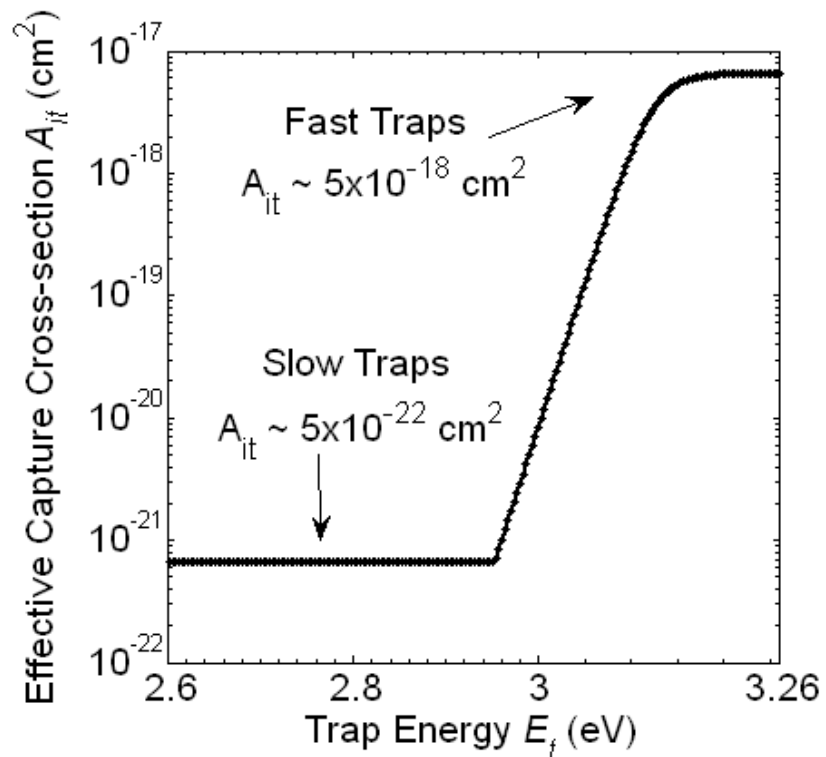


Fig. 3.7 Energy dependent trap capture cross-section profile that gave simulated transient current comparable to the measured characteristics. Two distinct levels of capture cross-section were obtained indicating the presence of fast traps lying near the conduction band and slow traps in the middle of the bandgap. The energy scale is shown from 2.6eV above the valence band (0eV) to the minimum of the conduction band for 4H-SiC.

3.6.3. Time and Energy Dependent Occupation Probability of Traps

Fig. 3.8 is a three dimensional plot of trap occupation probability as a function of energy and time. The plot can be thought of as a series of curves. The first curve represents occupation probability versus energy at 10^{-9} seconds (or immediately) after a voltage is applied to the gate, while the last curve gives the occupation probability approximately 10^{-5} seconds later. Fig. 3.9 shows the occupation probability versus energy of the interface traps for four different time instances equal to 0s, 100ns, 1 μ s and 10 μ s. The graphs are for traps that are at located at the interface halfway between the source and drain.

The occupation probability curves are explained as follows. At the beginning of the gate pulse when $V_{GS} = 0V$, the trap occupation probability follows the equilibrium Fermi-Dirac distribution with a Fermi level of about 2.9eV. As the band-edge traps are empty and have large capture cross-sections, they get occupied quickly. This is seen in the rise in the occupation probability near the conduction band. As time progresses, the traps further away from the band-edge start getting occupied, whereas those near the band-edge settle down to their final occupation levels. This is seen in the increase in occupation probability over time at trap energies away from the conduction band. Finally at some time greater than 10 μ s, the current reaches steady state and a new quasi-equilibrium with a Fermi level of approximately 3.2eV arises. Thus, as shown in the figures, a long time after application of a fast 0-5V gate pulse, a new Fermi-Dirac type distribution profile for interface trap occupation, with a higher occupation level corresponding to the new gate voltage emerges.

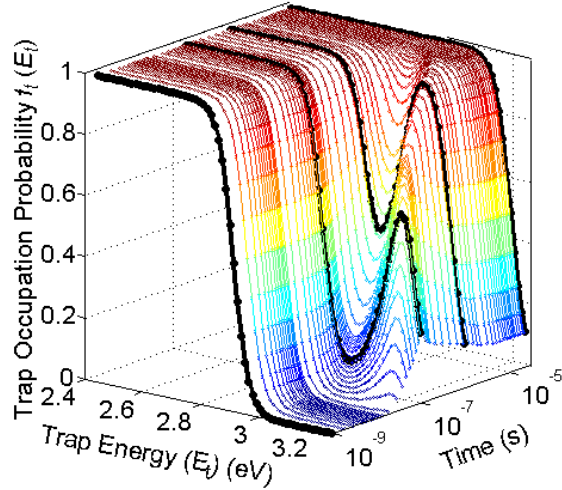


Fig. 3.8 Time dependence of the trap occupation probability at different trap energy levels inside the 4H-SiC bandgap. The time is shown in logarithmic scale.

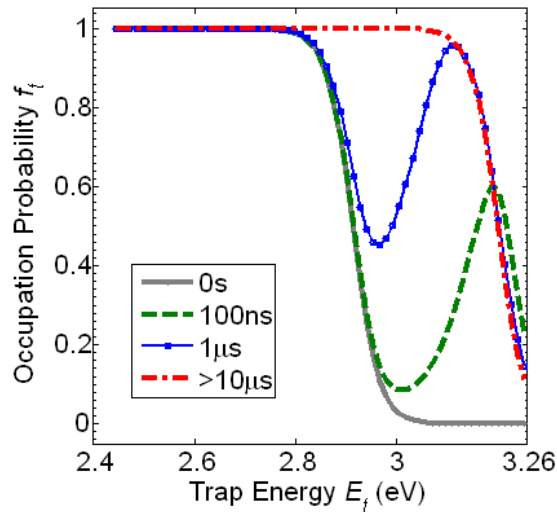


Fig. 3.9 The occupation probability curves at 4 different time instances (highlighted in Fig. 3.8) are shown here. At the beginning of the gate pulse when $V_{GS} = 0V$, the trap occupation probability follows the equilibrium Fermi-Dirac distribution with a Fermi level of about 2.9eV. With time, the fast traps at the band-edge get occupied before the traps lying deeper in the bandgap get filled. Finally at some time greater than 10 μ s, a new equilibrium with a Fermi level of approximately 3.2eV arises. The energy scales are shown from 2.4eV above the valence band (0eV) to the minimum of the conduction band for 4H-SiC.

3.6.4. Time Dependence of Occupied Interface Trap Density and Inversion Charge Density

We show the time dependent charging of the interface traps in real-space (along the channel), and the time dependence of the inversion layer charge density in the 4H-SiC MOSFET in Fig. 3.10 and Fig. 3.11, respectively. Fig. 3.10 shows a section of the interface from the center of the device to the edge of the drain. When the gate pulse is applied at time $t=0$, the occupied trap density is very small. The rise in trap density does not occur immediately. Until up to approximately 10ns, the trap density has not increased much. Then as the band-edge traps become occupied, the occupied trap density starts increasing, reaching close to its final value in the first few microseconds. After that, the change in occupied trap density is less because only the traps away from the conduction band edge are yet to be filled and the trap densities there are much lower. The figure also shows that near the drain, in the small gate-drain overlap region, the occupied trap density is very high. As there is a huge source of electrons in this narrow overlap region, almost all the traps are occupied, and the occupation does not change with time either.

As shown in Fig. 3.11, the behavior of the inversion charge is different from the interface trapped charge. As the traps do not respond immediately to the applied gate pulse, the inversion charge density rises quickly and attains a maximum. Then as the traps become occupied over time, the inversion charge density starts decreasing until it reaches its steady state value. This peak and subsequent decay in the inversion charge gives rise to the current transients observed in 4H-SiC MOSFETs.

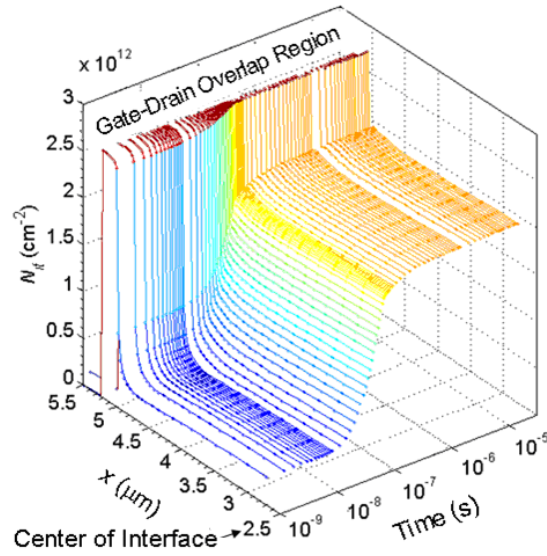


Fig. 3.10 Time dependent occupation trap density in a 4H-SiC MOSFET subject to a 0-5V gate pulse with a 100ns rise time. The interface from the middle of the device ($x=2.5\mu\text{m}$) to the drain-gate overlap ($x=5\mu\text{m}$) is shown. Traps do not start rising instantly and the first 10ns do not cause much trap occupation. Almost all traps are occupied at the interface over the drain overlap region due to the huge source of electrons below it.

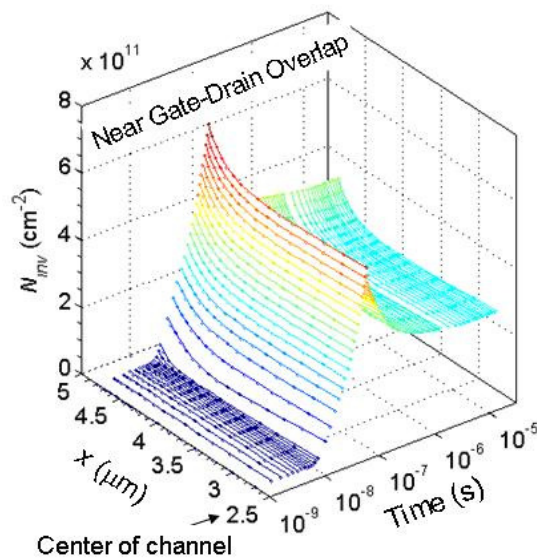


Fig. 3.11 Time dependence of inversion charge in the channel on application of 0-5V gate pulse with a 100ns rise time. The inversion charge rises to a maximum before decaying and settling down at the steady state value. This peaking of the inversion charge density causes the current transients shown in Fig. 3.6.

3.7. AC Characterization of 4H-SiC MOSFETs

The time dependent trap occupation model can be used to extract the AC small signal characteristics of the 4H-SiC MOSFET. The finite-time response of interface trap results in an extra capacitance in parallel to the inversion layer capacitance. Usually, this capacitance is thought of as a low-frequency effect alone, because it is assumed that the interface traps cannot respond to a high frequency signal. The difference between high frequency and low frequency C-V measurements can then be used to extract the interface trap density of states. Our modeling of the dynamic response of the interface trap showed that the assumption that interface traps do not respond to high frequency (1MHz) signals is not really valid. In fact, we found that interface traps in 4H-SiC MOSFETs can respond to signals as high as 100MHz. Therefore, it may be misleading to assume that C-V measurement done at 1MHz gives only the semiconductor capacitance, and therefore can be used as a reference against which the low frequency C-V could be compared. Our modeling of the high-frequency C-V characteristics indicated that using the standard hi-lo C-V method underestimates the interface trap density of states.

We calculate the gate capacitance of the 4H-SiC MOSFET in presence of interface traps by applying a small signal to the gate of the structure while keeping the source and drain connected to ground. We run the simulation in small time steps for several cycles of the input signal until AC steady state is reached. We then calculate the change in total charge of the device in one cycle. The ratio of the change in the total charge in the device to the small signal applied voltage gives the total capacitance of the device. This is carried out at different gate biases, and different small signal frequencies to get C-V curves for the 4H-SiC MOSFET. Fig. 3.12 shows C-V curves for three

different frequencies for a $100\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET with a 50nm gate oxide. The C-V curves differ from each other in three regions: accumulation, near threshold, and deep inversion. The difference in the capacitances in accumulation and deep inversion is due to the inability of the holes (in accumulation) and electrons (in inversion) to respond to high frequency signals. But, the difference in the C-V curves near threshold is due to the inability of the interface traps to respond to the various frequencies.

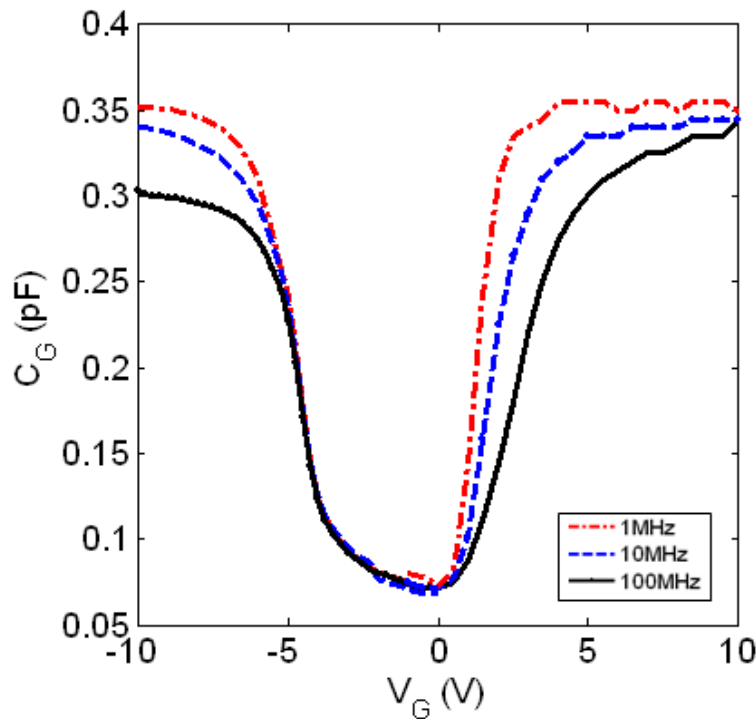


Fig. 3.12 C-V curves for a $100\mu\text{m} \times 5\mu\text{m}$ 4H-SiC MOSFET with a 50nm oxide, at three different frequencies. The different values of capacitance near threshold indicate the ability/inability of the interface traps to respond to an AC signal.

Fig. 3.13 shows the C-V curves in the near-threshold to deep inversion levels for a frequency of 100MHz and different trap capture probabilities. For the case of faster traps (with larger c_n values), the capacitance is higher as compared to the simulations involving

slower traps. The differences in the C-V curves clearly illustrate the effect of interface trapping on capacitance measurements.

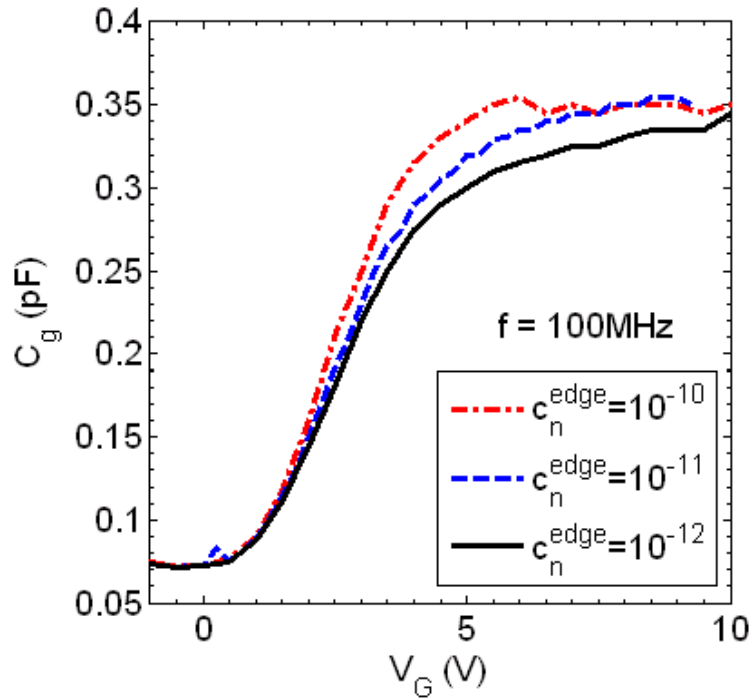


Fig. 3.13 High frequency C-V curves in the near threshold to deep inversion bias regime for different trap capture cross-section values. The bigger the trap cross-sections, the faster they respond, thereby giving higher capacitance.

3.8. Application to high- k gate stacked MOSFETs

The issues of interface and near-interface traps that are present in SiC MOSFETs are also seen in devices with high- k dielectrics. Silicon MOSFETs with gate stacks of SiO₂ and high- k dielectrics like HfO₂ have shown presence of high densities of interface traps at the SiO₂-HfO₂ interface and also at the Si-SiO₂ interface. These interface traps cause threshold voltage instability, irregular switching, and oxide reliability issues. The dynamic trapping model developed above can be applied to high- k Si MOSFETs too. Further improvement in terms of including a gate-tunneling model will enable us to probe deeper into the oxide and characterize the traps at the SiO₂-HfO₂ interface in terms of the traps density of states, and the trap cross-section areas.

3.9. Chapter Summary

A methodology for modeling and characterizing the transient response of 4H-SiC MOSFETs has been developed. The method combines new physical models, simulation techniques and experiment to provide insight into the details of MOSFET time-dependent dynamics. A new physical model for generation-recombination between interface traps and channel electrons was derived. Expressions were obtained for both, the total and the energy dependent generation-recombination rates. A set of algorithms was then developed that enabled these rates to be incorporated into the Drift-Diffusion model so that their effect on switching of 4H-SiC MOSFETs could be evaluated numerically.

Once the new physical models were incorporated into the simulator that solved the semiconductor equations in space and time, we could obtain results for drain current during the switching of the device. By correlating the simulated and measured peak and decaying values of the transient current, we were able to extract the effective capture cross-sections of these traps. We found that states near the band-edge would become occupied much more quickly and had much larger effective cross-sections than those that were several tenths of an eV away from the band-edge. This leads to the conclusion that the fast traps with large cross-sections are likely to be interface states, while the traps with the smaller cross-sections are a combination of midgap interface states and oxide traps. Finally, with the dynamics of trapping incorporated into the simulator, we were able to probe deeply into the physical basis of the switching characteristics of the device.

The simulations strongly indicate that the MOSFET turn-on begins with the establishment of a conducting channel. Establishment of the channel is then followed by

the reduction of the channel mobile electron concentration due to their subsequent occupation in interface and oxide traps, leading to reduced drain current.

By viewing the dynamics of the traps, we can further conclude that improvements in long-term device reliability (times greater than several microseconds) can be achieved by reducing oxide traps, while short-term stability can be controlled by focusing on reduction of interface traps.

3.10. Appendix: Details of the Derivation of the Generation-Recombination Model

The details of our derivation for the generation-recombination rate for traps and channel electrons are given below. Starting with equation (3.6), we have the generation-recombination rate between a trap at energy E_t and an electron at energy E as

$$du_{ce}(E, E_t) = [(1 - f_t(E_t))f(E)c_n(E, E_t) - f_t(E_t)(1 - f(E))e_n(E, E_t)] \cdot D_{it}(E_t)dE_t g(E)dE \quad (3.19)$$

Here, $f_t(E_t)$ represents the probability that a trap at energy level E_t inside the bandgap is occupied. Also, $f(E)$ represents the probability of occupation of an electron state at energy E in the conduction band. These two probabilities in equilibrium may be written using Fermi levels for traps (E_F^{trap}) and for surface electrons ($E_F^{electron}$) as:

$$f_t(E_t) = \frac{1}{1 + \frac{1}{2} \exp\left(\frac{E_t - E_F^{trap}}{k_B T}\right)} \quad (3.20)$$

$$f(E) = \frac{1}{1 + \exp\left(\frac{E - E_F^{electron}}{k_B T}\right)} \quad (3.21)$$

The $\frac{1}{2}$ term is due to double degeneracy in trap occupation probability. k_B is Boltzmann's constant and T is temperature.

To simplify equation (3.19), we first eliminate one of the two proportionality factors by determining a relationship between them. To obtain this relationship, consider the system of surface electrons and interface traps under equilibrium. Then, the rate of capture of a surface electron at energy E into a trap at energy E_t will equal the rate of

emission of a trapped electron at E_t to an empty conduction band state at E . $du_{ce}(E, E_t) = du_c(E, E_t) - du_e(E, E_t) = 0$. Further, the surface electron Fermi level will equal the trap Fermi level, that is $E_F^{electron} = E_F^{trap} = E_F$. For this case, by equating equation (3.19) to zero, we obtain a relation between the emission probability (e_n) and the capture probability (c_n) as:

$$\frac{e_n}{c_n} = \left(\frac{1}{f_t(E_t)} - 1 \right) \left(\frac{1}{1/f(E) - 1} \right) \quad (3.22)$$

Substituting equations (3.20) and (3.21), respectively, for $f_t(E_t)$ and $f(E)$ above, the ratio of emission and capture probabilities reduces to the following expression, which is a function of trap energy, electron energy and lattice temperature.

$$\frac{e_n}{c_n} = \frac{1}{2} \exp\left(\frac{E_t - E}{k_B T}\right) \quad (3.23)$$

We use this relationship to eliminate the emission probability from the net generation-recombination rate equation, and writing it using only one proportionality factor $c_n(E, E_t)$. Rewriting the generation-recombination rate (3.19) using the above relationship and the expression for $f(E)$ from (3.21), we obtain the following net generation-recombination rate.

$$du_{ce}(E, E_t) = \left[(1 - f_t(E_t)) - \frac{1}{2} f_t(E_t) \exp\left(\frac{E_t - E_F^{electron}}{k_B T}\right) \right] \cdot c_n(E, E_t) D_{ii}(E_t) dE_t f(E) g(E) dE \quad (3.24)$$

The net generation-recombination rate for a trap located at energy E_t in the bandgap due to the electrons distributed at all energies in the conduction band can be

obtained by integrating the above equation over electron energy E from conduction band minimum E_C to infinity, as:

$$u_{ce}(E_t) = \left[(1 - f_t(E_t)) - \frac{1}{2} f_t(E_t) \exp\left(\frac{E_t - E_F^{electron}}{k_B T}\right) \right] D_{it}(E_t) dE_t \cdot \left[\int_{E_C}^{\infty} f(E) g(E) c_n(E, E_t) dE \right] \quad (3.25)$$

To evaluate the integral in the above expression, we introduce an effective energy-dependent trap capture cross-section $A_{it}(E_t)$. We write the capture probability $c_n(E, E_t)$ as a product of this capture cross-section and an average thermal velocity $\langle v_{th} \rangle$ of electrons in the conduction band. Then, we pull the trap capture cross-section and average thermal velocity terms out of the integral reducing it to simply the electron concentration at the surface (n). Thus, the net generation-recombination rate for a trap at energy E_t simplifies to

$$u_{ce}(E_t) = \left\{ \left[(1 - f_t(E_t)) - \frac{1}{2} f_t(E_t) \exp\left(\frac{E_t - E_F^{electron}}{k_B T}\right) \right] D_{it}(E_t) A_{it}(E_t) dE_t \right\} \cdot n \cdot \langle v_{th} \rangle \quad (3.26)$$

Finally, writing the surface electron Fermi level $E_F^{electron}$ in terms of the surface electron concentration and an average conduction band density of states N_C as

$$E_F^{electron} = E_C - k_B T \ln\left(\frac{N_C}{n}\right) \quad (3.27)$$

we arrive at the final expression given below for the net recombination rate for traps located at energy E_t inside the 4H-SiC bandgap.

$$u_{ce}(E_t) = \langle v_{th} \rangle \cdot [D_{it}(E_t) A_{it}(E_t) dE_t] \cdot \left[n (1 - f_t(E_t)) - \frac{1}{2} N_C f_t(E_t) \exp\left(\frac{E_t - E_C}{k_B T}\right) \right] \quad (3.28)$$

Chapter 4

4. Physical Modeling and Characterization of High Power 4H-SiC DMOSFETs

Owing to the large critical breakdown field of 4H-SiC, power devices made using this material can theoretically exhibit excellent performance. A Double diffused MOSFET (DMOSFET) is a power device used primarily as a switch in a power converter or motor control circuit. In the ON state, the DMOSFET operates in the linear region close to zero volts drain-source bias and a high gate-source bias. In the OFF state the DMOSFET operates at zero volts gate-source bias and possibly several thousand volt drain-source bias. Modeling and characterization of the transport in 4H-SiC DMOSFET is very important to understand its operation, limitations, and design. Because the operation of a DMOSFET is similar to a lateral MOSFET, we can apply the same mobility mechanisms, interface trap models, etc. derived in the chapters above to model and simulate the 4H-SiC DMOSFET. A very important aspect of DMOSFET modeling is to understand the breakdown mechanism in the device.

The chapter is structured as follows. First we discuss the design and operation of a 4H-SiC power DMOSFET. Then we model the ON state behavior of the device and extract relevant physical information by comparing simulations to experiment. After that we model impact ionization in the 4H-SiC DMOSFET and characterize the OFF state behavior. Finally we discuss mixed-mode modeling and simulation of a boost converter circuit using a 4H-SiC DMOSFET.

4.1. DMOSFET Structure and Operation

The Double Diffused MOSFET (DMOSFET) is a semiconductor power device mainly used in power switching operation. The operating conditions of the DMOSFET requires it to block several hundred volts to kilo volts of DC voltage when the device is OFF, and pass several amperes of current when the device is ON. This requires a more complex structure than a standard MOSFET. The width of the DMOSFET is very large in order to allow high current flow, which necessitates a fingered or more exotic layout of the transistor. Also, the large blocking capability is achieved by using a vertical device structure. The 2-D cross-sectional structure of a single n -channel DMOSFET cell is shown in Fig. 4.1. The two sources are connected together. Two channels are formed in the p -well regions near the semiconductor-oxide interface when the device is ON. The current flows horizontally in the channel; but then once the electrons reach the low doped JFET region, the vertical field arising due to the drain bias pulls the electrons down in the vertical direction, thereby changing the direction of current.

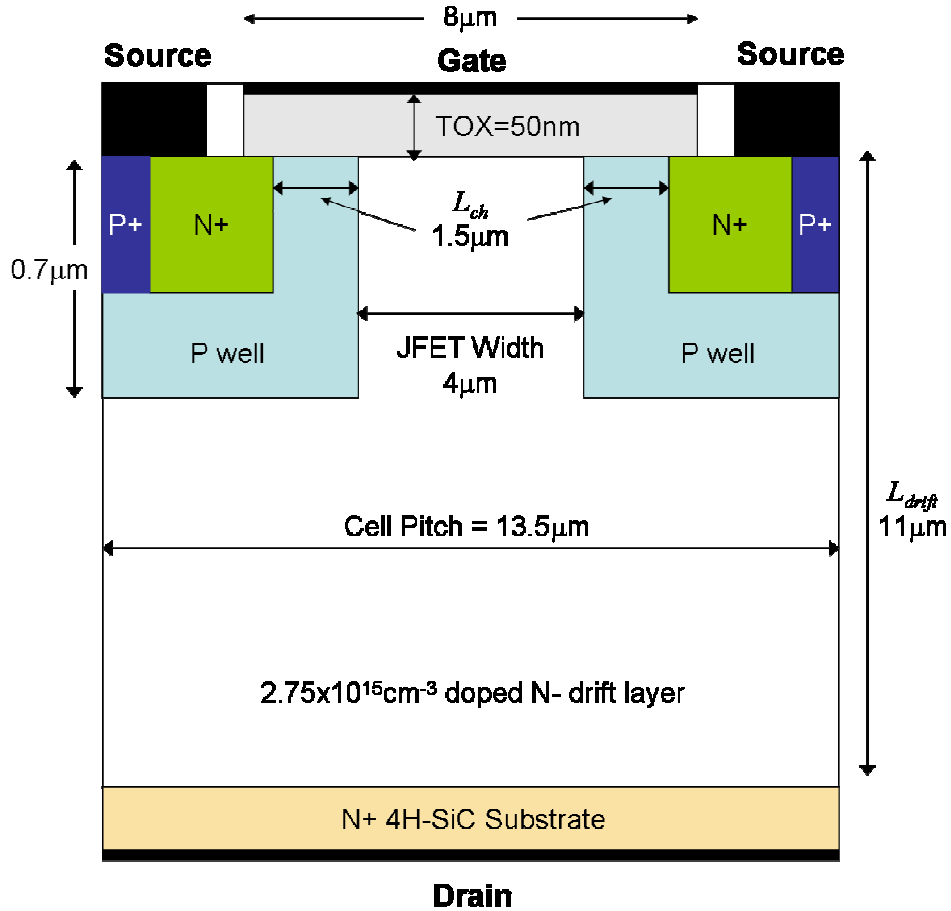


Fig. 4.1 Structure of the 4H-SiC DMOSFET under test.

4.1.1. DMOSFET Doping Profile

Important metrics for the design of a DMOSFET include the doping of the n- drift region, the length of the drift region, width of the JFET regions, and the p-well doping. Fig. 4.2 shows the typical doping profile of the DMOSFET. The p-well is Gaussian doped with a surface doping value of $5 \times 10^{16}\ \text{cm}^{-3}$, while the peak doping of $10^{19}\ \text{cm}^{-3}$ occurs approximately $0.5\ \mu\text{m}$ away from the interface. For the device under test, the n- drift region was doped to approximately $2.75 \times 10^{15}\ \text{cm}^{-3}$. Further, the length of the drift

region was $11\mu\text{m}$. The cell pitch was $13.5\mu\text{m}$. The gate was $8\mu\text{m}$ long with two channels of $1.5\mu\text{m}$ each. The oxide thickness was 50nm . The total area of the gate was 0.085cm^2 . This translates to a width of 83.55388cm . This huge width enables the device to pass currents as high as 5A .

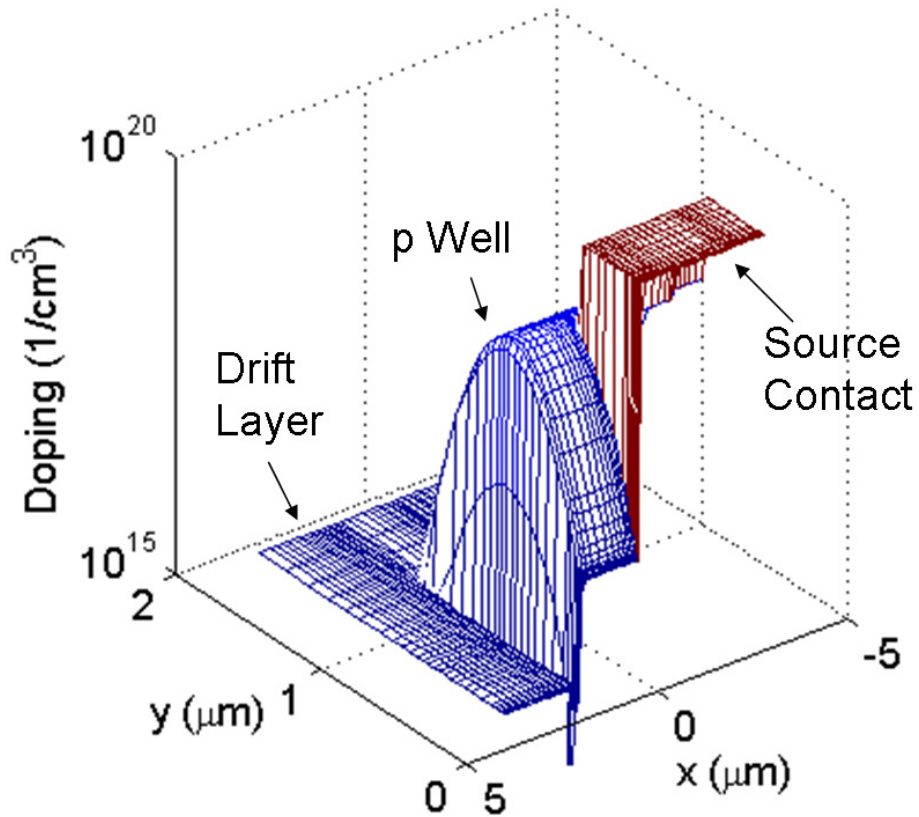


Fig. 4.2. Doping profile of the 4H-SiC DMOSFET. The p-well is Gaussian doped with a peak value of $1 \times 10^{19} \text{cm}^{-3}$ at $0.5\mu\text{m}$ away from the surface. The drift layer is uniformly doped to $2.75 \times 10^{15} \text{cm}^{-3}$. Only half of the device in the x -direction starting from the source contact to the middle of the JFET region is shown here. Only $2\mu\text{m}$ of the drift region (y -direction) is shown. The gate oxide is 50nm thick and stretches from $x=0\mu\text{m}$ to $x=8\mu\text{m}$.

4.1.2. Operation of the DMOSFET

The DMOSFET works exactly like an enhancement mode lateral MOSFET. When a positive bias is applied to the gate of a n -channel DMOSFET, the p -well regions near the interface start getting depleted. Once the gate bias crosses the threshold voltage, an inversion layer is formed in each of the p -wells near the interface. On application of a drain bias, electrons flow from both the sources, through the two channels and in to the lightly doped JFET region. From there, the vertical field due to the drain bias pulls the electrons to the drain contact and out of the device. During OFF state, the gate voltage is at or below zero volts. In this case the channel is turned off and the drain-source voltage drops across the drift region and the heavily doped p -well.

Typical operation scenario of the DMOSFET will be as a switching element in a power converter circuit. Fig. 4.3 shows an example of the boost converter with a SiC DMOSFET acting as the switch.

On application of a large positive voltage to the gate of the DMOSFET, a large current flows through the device. This brings down the voltage at the drain to a few millivolts, and thereby turns off the diode D1. In this case, the storage capacitor C2 is providing power to the load R. During this ON period, the current drawn from the battery charges up the inductor and thereby stores energy in it. The DMOSFET should be able to source a very large current without requiring a large drain bias. That is, the DMOSFET should remain in the linear region of operation during the ON cycle. This assures a linear increase in inductor current and also insures that the power being supplied by the battery is not wasted as heat in the DMOSFET itself. Thus, during the ON part of the switching

cycle, the DMOSFET has a very small drain voltage (a few hundred millivolts), while sourcing a large amount of current.

When the DMOSFET is switched OFF, the current through the inductor abruptly starts decreasing. This causes the entire inductor voltage to add to the battery voltage and appear across the DMOSFET. In this cycle, the inductor is supplying power to the load. For the boost converter operating as a voltage doubler (achieved for a 50% duty cycle), the DMOSFET has to block $2 \cdot V_{DD}$ voltage in the OFF state. A proper choice of inductor and DMOSFET is essential to make sure that the boost converter design works optimally for the load resistance. Thus, the ability to block a very high voltage when the DMOSFET is in OFF state is the other operating condition for the device.

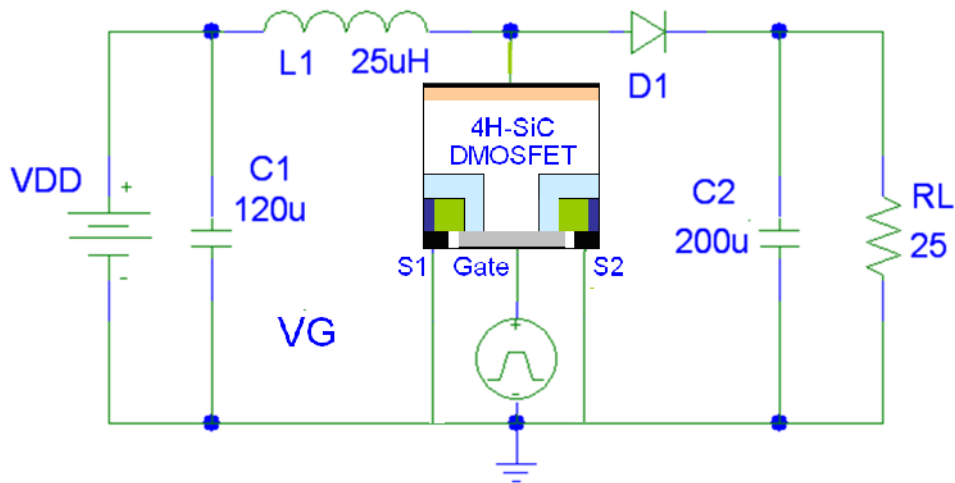


Fig. 4.3 Schematic of a boost converter using the 4H-SiC DMOSFET as a switch. VDD is the battery, VG provides the switching gate pulses to the DMOSFET, L1 and C2 are the energy storage units, and RL is the load.

Thus, it is important to characterize the DMOSFET in two distinct regions of operation. (1) ON State where a large current is flowing through the device while the

drain bias is at a few hundred millivolts and (2) OFF state when zero current is flowing but the drain bias is at few hundred volts. The device should have a very low ON resistance so that a large amount of current can be drawn through the device with very little ON state drain voltage. And at the same time it must be able to block a very large voltage in OFF state. Therefore, a figure of merit for such power devices is the blocking voltage to ON resistance ratio, which will be discussed in more detail later. Further, the DMOSFET needs to switch at a fast rate, to avoid power dissipation during switching. Therefore, modeling the dynamic response of DMOSFET is also of essence.

4.1.3. Figure of Merit of 4H-SiC DMOSFETs

The two distinct regions of operation of a DMOSFET govern its design metric. For a traditional DMOSFET, the ON resistance is controlled by the drift layer resistance. This is not true for the current generation of SiC DMOSFETs as we show later. For traditional DMOSFETs, a low ON resistance can be obtained by a short and high doped drift layer. But, a short and high doped drift layer would give rise to large electric fields during OFF state. These large electric fields would cause impact ionization in the device, leading to device breakdown. So, a tradeoff between low ON resistance and high blocking voltage ensues and is determined by the material properties of the semiconductor.

When a small drain bias is applied to the DMOSFET, the resistivity or the ON resistance of the uniformly doped n - drift region can be written in terms of the electron

concentration (n), bulk mobility (μ_n), the length of the drift region (L_{drift}), for a unit area device as

$$R_{on} = \frac{L_{drift}}{qn\mu_n} \quad (4.1)$$

Writing the electron concentration as equal to the doping, the ON resistance is given as

$$R_{on} = \frac{L_{drift}}{qN_D\mu_n} \quad (4.2)$$

During OFF state, when a large bias is applied to the drain, the drift region will be depleted. In this case, the maximum depletion width will correspond to maximum allowed drain voltage (blocking voltage V_B). As the maximum depletion width is equal to the length of the drift region (L_{drift}), it can be written in terms of the applied blocking voltage as

$$W_d^{\max} = L_{drift} = \sqrt{\frac{2\epsilon_{SiC}(V_B + \phi_{BI})}{qN_D}} \quad (4.3)$$

For $V_B \gg \phi_{BI}$,

$$L_{drift} = \sqrt{\frac{2\epsilon_{SiC}V_B}{qN_D}} \quad (4.4)$$

Substituting for qN_D in equation (4.2), we have

$$R_{on} = \frac{L_{drift}^3}{2\epsilon_{SiC}V_B\mu_n} \quad (4.5)$$

Now, if the device breaks down at the blocking voltage V_B , then the electric field inside the drift region at a drain bias of V_B must be equal to the critical breakdown field

(E_C) for SiC. Writing $E_C = V_B/L_{drift}$, and substituting for L_{drift} in the above equation we have

$$R_{on} = \frac{(V_B^3/E_C^3)}{2\epsilon_{SiC}V_B\mu_n} \quad (4.6)$$

The figure of merit is then written as [66]

$$FOM = \frac{V_B^2}{R_{on}} = 2\epsilon_{SiC}\mu_n E_C^3 \quad (4.7)$$

The figure of merit gives a measure of how high the blocking voltage could be for a specified ON resistance in the DMOSFET. It is dependent on the permittivity, the bulk electron mobility and the critical breakdown field of the material. Thus it provides a method to compare DMOSFETs fabricated using different materials. For example, Silicon and 4H-SiC have similar permittivity ($\epsilon_{Si}=11.8$, $\epsilon_{SiC}=9.8$), similar intrinsic bulk mobilities ($\mu_{Si} = 1400 \text{ cm}^2/\text{Vs}$, $\mu_{SiC} = 1071 \text{ cm}^2/\text{Vs}$), and similar dependence of mobility on doping. Therefore, the only real difference between Silicon and SiC in terms of the DMOSFET figure of merit is the critical field. As the breakdown field of 4H-SiC is approximately 10X that of Silicon, the figure of merit of 4H-SiC DMOSFET is almost a 1000X of that of Silicon DMOSFETs. That means that for a given ON resistance, SiC DMOSFETs will be able to switch almost 30 times higher voltages than Silicon DMOSFETs. This shows the tremendous advantage SiC enjoys over Silicon in terms of power DMOSFETs. Fig. 4.4 compares the theoretical limits of the ON resistance versus blocking voltage capabilities of Silicon and 4H-SiC DMOSFETs.

In the next two sections we will demonstrate modeling of the ON state and OFF state characteristics of 4H-SiC DMOSFETs.

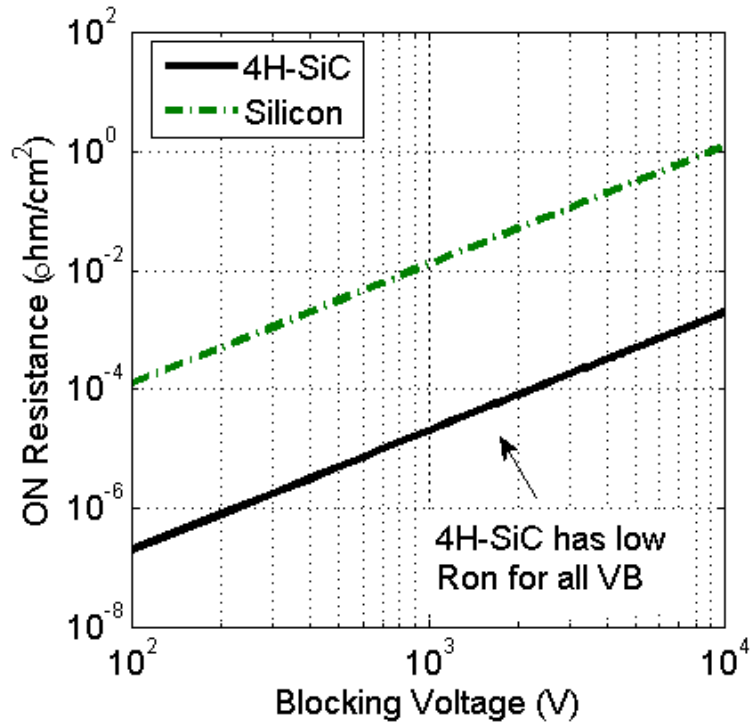


Fig. 4.4 Theoretical limits of the ON resistance versus blocking voltage capacity of Silicon and 4H-SiC DMOSFETs. 4H-SiC DMOSFETs have a much lower ON resistance than Si DMOSFETs at all blocking voltage values.

4.2. ON State Modeling and Characterization

We extend the physics based numerical models for surface mobility, interface trap densities, incomplete ionization, etc. that we had developed for lateral 4H-SiC MOSFETs to a vertical power DMOSFET. Mobility models for Coulombic scattering and surface roughness scattering, doping density dependent bulk mobility models, distribution of interface traps in energy space and incomplete ionization of dopants are incorporated in our custom 4H-SiC DMOSFET simulator. We follow the now familiar procedure of extracting interface trap density of states profile and the surface roughness parameters from the subthreshold and the linear I_D - V_{GS} characteristics respectively. Then, we model the turn-ON behavior of the DMOSFET and evaluate the various resistances in the device that control the total ON resistance.

4.2.1. Extracting Physical Parameters from I_D - V_{GS} Characteristics

The simulated I_D - V_{GS} characteristics (Fig. 4.5) are compared to experiment to validate our models and extract various physical parameters. As seen from the figure, excellent agreement is achieved between the simulated I-V curves and experiment. This allows us to extract the interface trap density of states profile and the surface roughness parameters for the DMOSFET. In Fig. 4.6 we show the extracted interface trap density of states profile for the DMOSFET. The band-edge density of states is approximately $3.6 \times 10^{13} \text{cm}^{-2} \text{eV}^{-1}$ which is comparable to the values extracted for the lateral MOSFET. Further, the extracted surface roughness step height is approximately 3.5nm which is the same as that obtained for lateral devices.

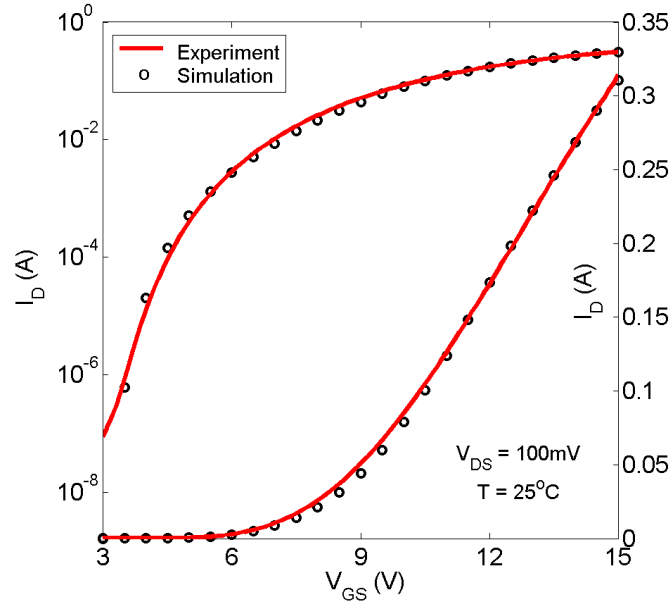


Fig. 4.5 Linear and subthreshold region I_D - V_{GS} curves for the 4H-SiC DMOSFET. Excellent match is achieved for the entire gate bias range which allows us to extract the interface trap density of states and the surface roughness values for the device.

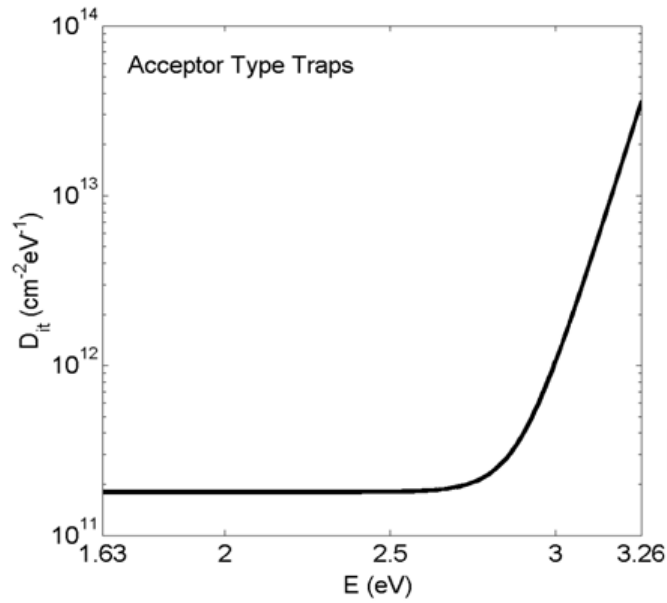


Fig. 4.6. Extracted interface trap DOS profile for the DMOSFET. The band edge DOS is $D_{it}^{edge} \sim 3.6 \times 10^{13} \text{ cm}^{-2} \text{ eV}^{-1}$, mid-band DOS is $D_{it}^{mid} \sim 1.8 \times 10^{11} \text{ cm}^{-2} \text{ eV}^{-1}$, and the band-tail energy is $\sigma = 70 \text{ meV}$

4.2.2. Turn-ON Characteristics and Channel Resistance

After extracting the physical parameters for the interface trap density of states and the surface roughness step height, we simulate the turn-ON characteristics of the DMOSFET. Fig. 4.7 shows the comparison of the simulated and experimentally measured turn ON behavior of the 4H-SiC DMOSFET. There is no fitting parameter involved in simulating the I_D - V_{DS} characteristics shown here. Thus, once the interface trap and surface roughness parameters are extracted from the I_D - V_{GS} characteristics, we can immediately and accurately predict the ON state behavior of the DMOSFET.

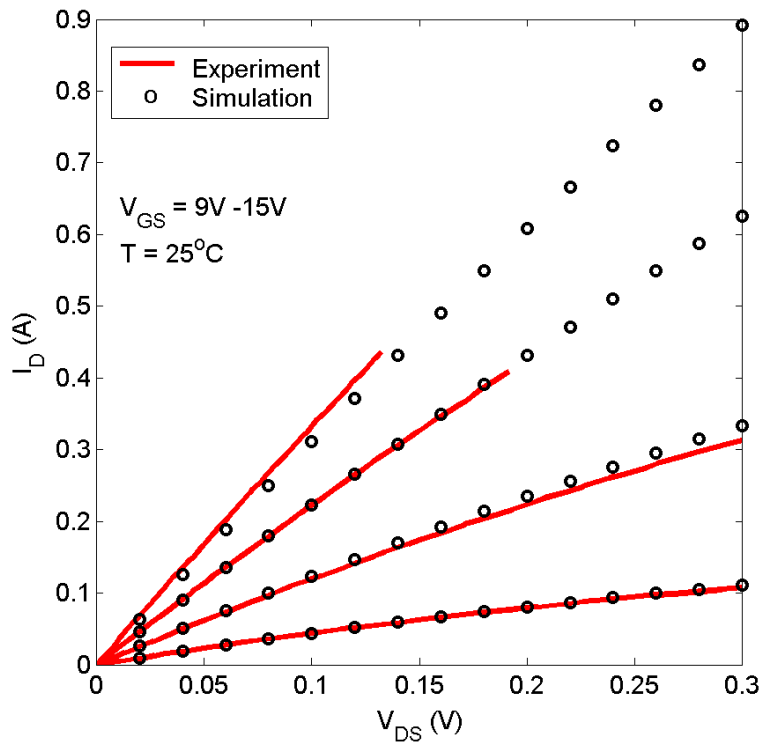


Fig. 4.7 Turn ON characteristics of the 4H-SiC DMOSFET. Excellent comparison is seen between simulations and experimental data.

The ON resistance of the DMOSFET can be calculated from the slope of the I_D - V_{DS} curves shown in Fig. 4.7. At a gate bias of 15V, the simulations and experiment show that the total ON resistance of the device is $300\text{mV}/0.9\text{A} = 333.33 \text{ m}\Omega$. For an area of 0.085cm^2 , this translates to a specific ON resistance of $25.8 \text{ m}\Omega\cdot\text{cm}^2$. By looking at the potential profiles inside the device, we can now find the areas which contribute to this ON resistance and thereby understand the mechanisms that are limiting transport in the DMOSFET.

In Fig. 4.8 we show the potential profile in the $1.5\mu\text{m}$ length channel ($x=0.5\mu\text{m}$ to $x=2.0\mu\text{m}$) of the DMOSFET. Now recall that there are two sources and two channels in our DMOSFET cell. At any given drain bias, the two channels will carry equal amounts of current (equal to half of the total drain current). Therefore, by evaluating the potential difference across any one channel at a given drain bias, and by calculating the drain current using our device simulator, we can calculate the channel resistance. As shown in the inset in Fig. 4.8, at the applied drain bias (V_{DS}) of 300mV , the voltage drop across one channel is approximately 225.7mV . With 0.45A of current passing through the channel, this gives the channel resistance of approximately $501\text{m}\Omega$. Thus, the total resistance of the two channels of the DMOSFET each carrying equal currents of 0.45A will be $250.5\text{m}\Omega$. Therefore, the channel component of the specific ON resistance is

$$V_{ch} = 225.7\text{mV}, I_{ch} = 0.9\text{A} \Rightarrow R_{ch} = \frac{V_{ch}}{I_{ch}} * \text{Area} = 21.31 \text{ m}\Omega \cdot \text{cm}^2 \quad (4.8)$$

This is approximately 75% of the total ON-resistance of the DMOSFET at $V_{GS} = 15\text{V}$! Thus, the ON resistance of the DMSOFET is almost completely controlled by the channel resistance. The drift layer plays a very small role in determining the ON resistance.

Recall that the design metric for a good DMOSFET is the tradeoff between blocking voltage and ON resistance, and that is optimized by varying the doping and the length of the drift region. Now, for the particular MOSFET under test, this design methodology will not work because the drift layer is responsible for only a small part of the total ON resistance. Thus, the current DMOSFET is far removed from the theoretically ideal 4H-SiC DMOSFET and substantial improvement is possible with regards to the ON resistance.

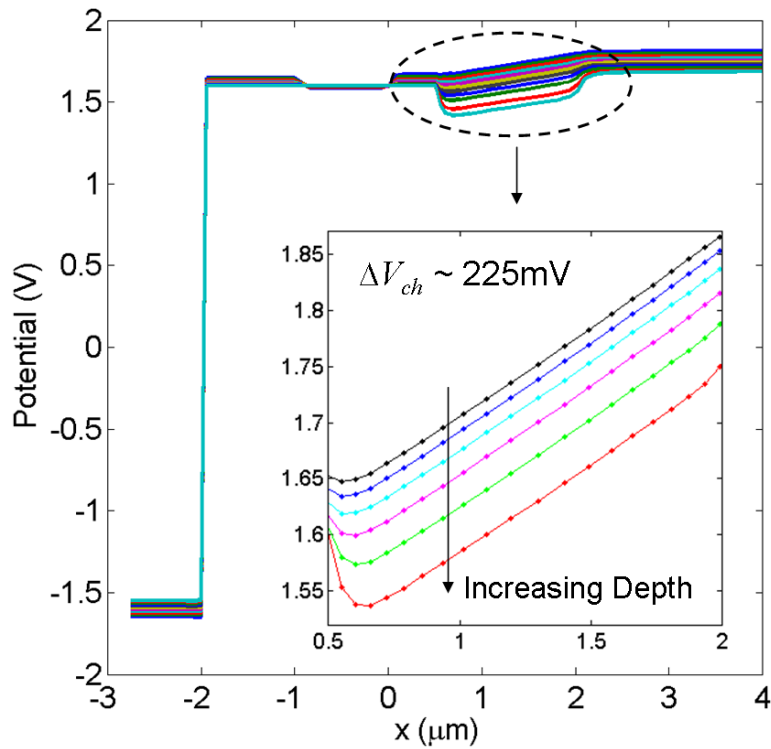


Fig. 4.8 Potential profile in the channel at $V_{DS}=300\text{mV}$ and $V_{GS}=15\text{V}$. The voltage drop of approximately 225mV in the channel is indicative of a large channel resistance.

Two physical effects contribute to this channel resistance. One is the reduced inversion charge density due to the large number of occupied interface traps. As shown in Fig. 4.9, at a gate bias of 15V, less than 50% of the total induced charge in the channel is available as mobile carriers for conduction while the rest occupies the interface traps. The extracted interface trap density of states profile has band-edge density of states values of $3.6 \times 10^{13} \text{cm}^{-2} \text{eV}^{-1}$ and midgap values of $1.8 \times 10^{11} \text{cm}^{-2} \text{eV}^{-1}$. The second performance degradation effect is the lowering of surface mobility due to Coulombic scattering from the interface traps and surface roughness scattering. The extracted value of surface roughness ($\Delta \sim 3.5 \text{nm}$) indicates the presence of step bunching at the interface. Fig. 4.10 shows the electron mobility in the channel at various depths inside the device. The surface mobility is as low as $6 \text{cm}^2/\text{Vs}$.

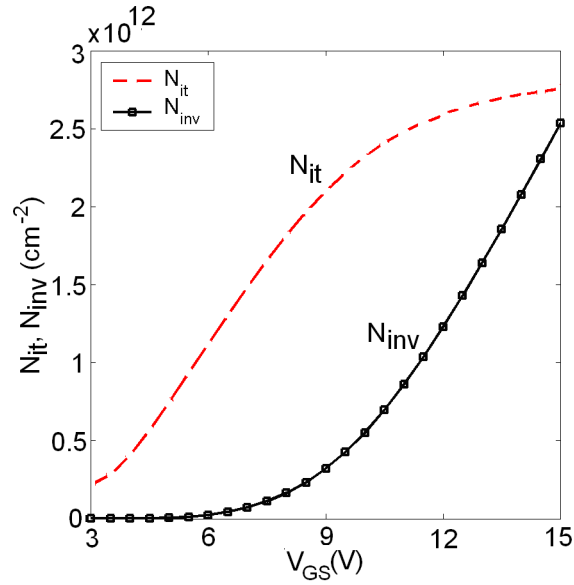


Fig. 4.9 Comparison of the immobile occupied interface trap charge density (dashed) and the mobile inversion charge density (solid with symbols) in the channel. Less than 50% of the total induced charge ($N_{it}+N_{inv}$) is available for conduction in the DMOSFET.

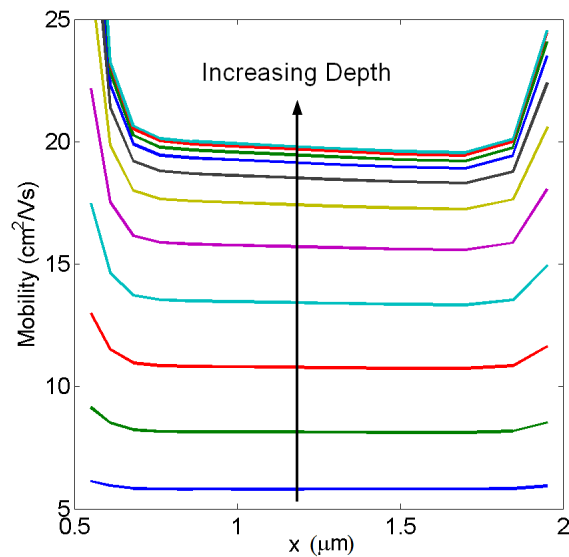


Fig. 4.10 Electron mobility in the channel at various depths into the device. Surface mobility at $V_{GS}=15\text{V}$ is as low as $6 \text{ cm}^2/\text{Vs}$ on account of surface roughness and interface trap scattering.

4.2.3. Optimization of Turn-ON Resistance

As a design experiment, we tried to optimize the ON resistance of the test DMOSFET by varying the width of the JFET region. The total resistance of the DMOSFET consists of the channel resistance, the JFET resistance, and the drift layer resistance. The flow of electrons inside the DMOSFET is from the two sources into the channels, then into the JFET region where the depletion regions near the p -wells force the electrons into a narrow region, and then from there into the drift region. Consequently, current flows into the device from the drain contact, vertically through the drift layer towards the surface. The field lines get constrained around the two p -wells directing the current into a narrow path (JFET region). From there, the current changes direction and flows laterally through the channels, and eventually out of the two sources. This flow of current is shown in Fig. 4.11. By varying the width of the JFET region for the given DMOSFET we would expect a change in the ON resistance.

Fig. 4.12 shows the same phenomenon in form of current density curves in half of the device. The lines represent the vertical component of the current density at various depths away from the interface. Close to the surface, the vertical current is constrained in the narrow JFET region. As we go deeper into the drift region, the electrons spread out more, and so the current density curves spread out too. Finally, near the drain contact, the current density is almost constant throughout the entire pitch of the DMOSFET cell.

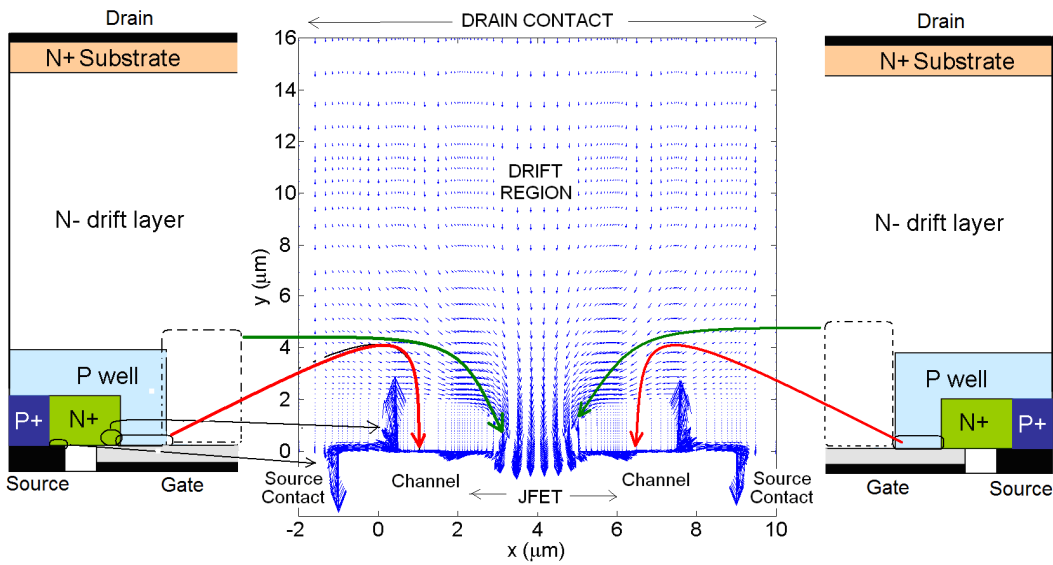


Fig. 4.11 Current flow inside a 4H-SiC DMOSFET. The arrows represent the direction of flow of current (from the drain to the sources)

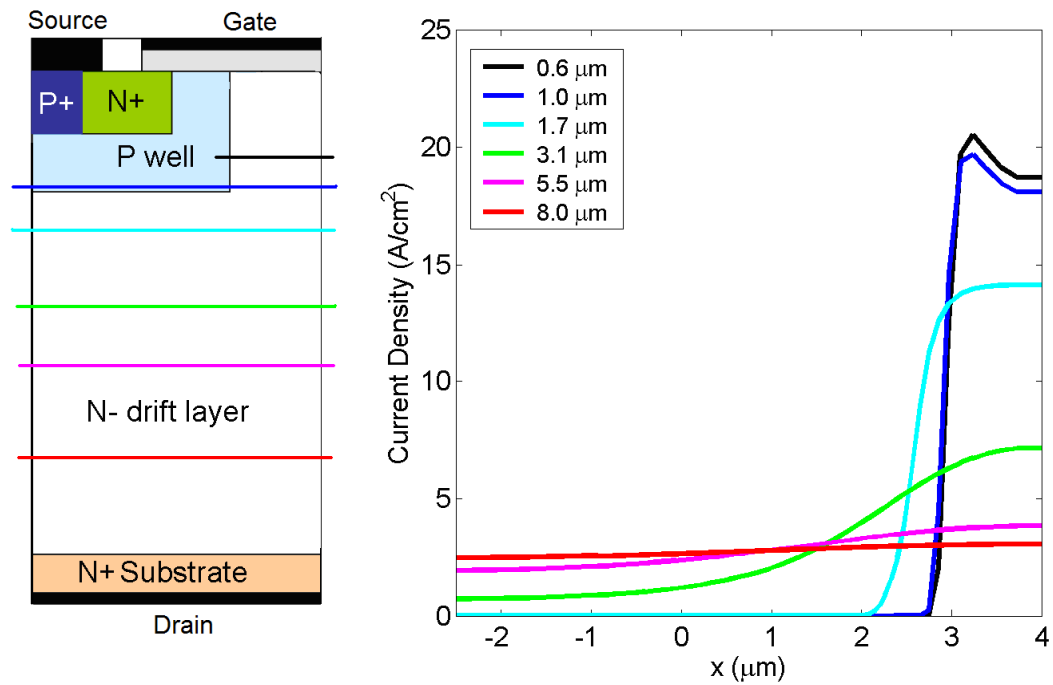


Fig. 4.12 Current spreading in the DMOSFET. In the JFET region, the current is confined to a narrow width, but as electrons move towards the drift region, they spread out and thereby the current density curves spread out over the entire width of the device.

We varied the width of the JFET region and simulated the turn ON characteristics each time. In Fig. 4.13 we show the extracted turn ON resistance as a function of width of the JFET region. We see that the best ON resistance is obtained at a JFET width of 4mm. Note that the value of the ON resistance is much higher than the theoretically achievable ON resistance at the given doping density. This is because the ON resistance is dominated by the channel resistance. Therefore, in the given DMOSFET, optimization of the JFET width may not look very important. But if the channel resistance can be eliminated, then careful design needs to be done to optimize the width of the JFET region.

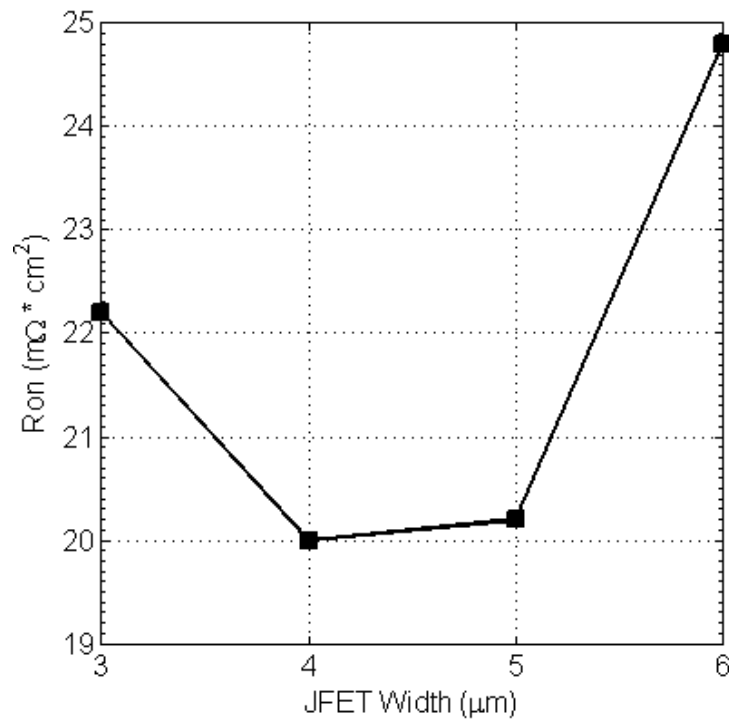


Fig. 4.13 Optimal JFET width can be obtained by simulating ON resistance for different device geometries. JFET width of 4 μm gave the best ON resistance at 20V gate bias.

4.3. OFF State Modeling and Characterization

For DC-DC converters, motor control and other power applications, SiC power DMOSFETs will be required to block several kilovolts in the OFF state, while at the same time limiting the leakage current to less than a few nanoamperes. This large drain-source voltage creates very high electric fields reaching several MV/cm inside the device. Using the device simulator, we can pin-point the places in the DMOSFET where the electric field is the highest, and then engineer the devices to control it. Impact ionization at large electric fields causes breakdown of the DMOSFET.

4.3.1. Impact Ionization Models

Impact ionization coefficients have been calculated or measured for holes and electrons in 4H-SiC [67][68][69]. Fig. 4.14 and Fig. 4.15 show a comparison of these published impact ionization coefficients respectively for holes and electrons, as a function of the electric field. For 4H-SiC, the hole ionization coefficients are larger than the electron ionization coefficients over most of the electric field range. This would indicate a higher probability of hole initiated impact ionization in 4H-SiC devices. The differences between the coefficients reported by the various groups arise from the methods used to measure them or from the Monte Carlo simulations employed to calculate them. This variation in the impact ionization coefficients translates to significantly difference impact ionization rates. Therefore, using these published coefficients will give considerable variety in the calculated breakdown voltages.

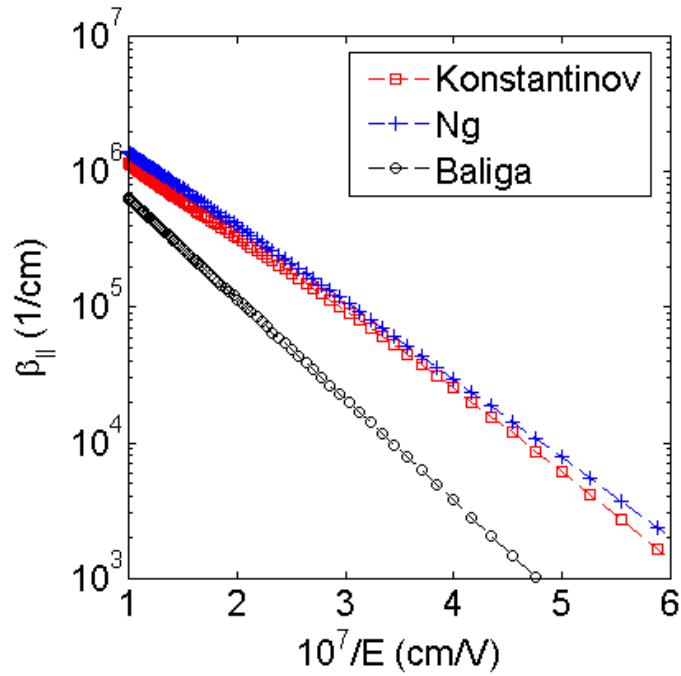


Fig. 4.14 4H-SiC hole impact ionization coefficients as reported in Konstantinov et al.[67], Ng et al.[68], and Baliga et al.[69]

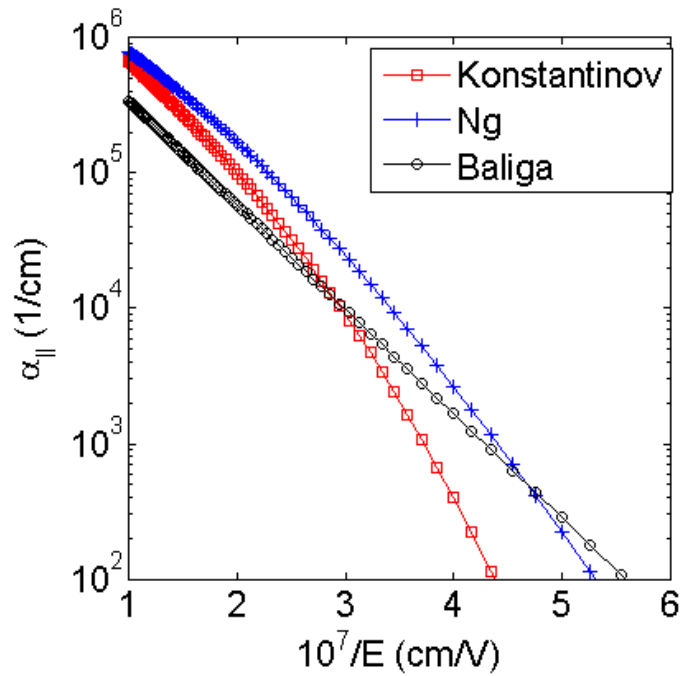


Fig. 4.15 4H-SiC electron impact ionization coefficients as reported by Konstantinov et al. [67], Ng et al., [68] and Baliga et al. [69]

The best way of choosing the proper ionization coefficients is to extensively calibrate the calculated breakdown characteristics with experimental data. Using the impact ionization coefficients published in literature, we simulated SiC avalanche photodiode (APD) breakdown characteristics for a number of devices manufactured by different groups and reported in literature [70]. This work showed that the ionization coefficients reported by Konstantinov et al. [67] gave consistently good match to experiment. The impact-ionization rates for holes (β_{ii}) and electrons (α_{ii}) which give the best match to experimental data in APDs are written as [67]

$$\beta_{ii} = \left(\frac{qE}{\xi_i^p} \right) \exp \left[- \frac{\xi_i^p \xi_o}{qE \lambda_p (\xi_o + qE \lambda_p)} \right] \quad (4.9)$$

$$\alpha_{ii} = \left(\frac{qE}{\xi_i^n} \right) \exp \left[- \frac{\xi_i^n \xi_o}{(qE \lambda_n)^2} \right] \quad (4.10)$$

Here, E is the local electric field, λ_p/λ_n are the electron/hole mean free paths ($\lambda_n = 2.99\text{nm}$, $\lambda_p = 3.25\text{nm}$), $\xi_o = 0.36\text{eV}$ is the optical phonon energy, ξ_i^n/ξ_i^p are the electron/hole ionization energies ($\xi_i^n = 10\text{eV}$, $\xi_i^p = 7\text{eV}$), and q is the electronic charge.

We use these coefficients to evaluate impact ionization and breakdown in the 4H-SiC DMOSFET. We do not have breakdown data for the DMOSFET, and so the results are predictions based on calibration carried out on 4H-SiC APDs [70].

4.3.2. Impact Ionization Simulation

The impact ionization coefficients given in equations (4.9) and (4.10) are used to calculate the impact ionization rate inside the device. The rate of impact ionization is given as

$$G_{ii} = \alpha_{ii} |J_n| + \beta_{ii} |J_p| \quad (4.11)$$

where J_n and J_p are the electron and hole currents.

The above equation is included in the Drift-Diffusion model as part of the steady state electron and hole current continuity equations.

$$\frac{1}{q} \bar{\nabla} \cdot \bar{J}_n + (G - R)_{SRH} + (G - R)_{AUG} + G_{ii} = 0 \quad (4.12)$$

$$-\frac{1}{q} \bar{\nabla} \cdot \bar{J}_p + (G - R)_{SRH} + (G - R)_{AUG} + G_{ii} = 0 \quad (4.13)$$

First the set of equations along with the Poisson equation are solved without including impact ionization to obtain a solution at the given bias point. Then the semiconductor equations are solved again using the aforementioned methodology and including impact ionization.

Modeling impact ionization in semiconductors is difficult. Near breakdown, the current in the device changes by several orders of magnitude for a small change in applied bias. This radical change is very difficult to capture in a device simulator. The problem becomes more complex for a 2-D device simulation as with the DMOSFET.

We employ a combination of several strategies to simulate impact ionization in the 4H-SiC DMOSFET. As a first step, we identify the regions in the device with the maximum electric field. Due to the exponential dependence of impact ionization rate on electric field, we expect to get the highest carrier multiplication values in the regions with

the highest field. We set up a fine mesh in these regions and continuously monitor them so that the mesh can be progressively refined in-order to achieve convergence. We employ two convergence criteria specifically to check for impact ionization convergence. We check for the convergence in the impact ionization rate itself, and also check for convergence in the electric field. We exit the simulation when one or the other criteria is met. Other numerical techniques used to achieve convergence include starting the simulation with a high impact ionization rate everywhere in the device, and progressively lowering the values till convergence is reached. We also continuously monitor various regions of the device to make sure that incomplete ionization does not complicate the simulation process.

4.3.3. Breakdown Characteristics of 4H-SiC DMOSFET

We simulate the OFF state characteristics of the 4H-SiC DMOSFET by applying zero volts to the gate and the source and a high voltage to the drain. The OFF state characteristics include the leakage current and the breakdown voltage calculation.

The first step in calculating breakdown in 4H-SiC DMOSFET is to calculate the electric field inside the device at large drain biases. Fig. 4.16 shows the electric field inside the DMOSFET when 2000V are applied to the drain. The peak electric field is observed near the p-well corner and along the p-well n-drift junction. The rest of the voltage is dropped across the entire drift layer depleting it completely. Our high voltage simulations show that the electric field reaches as high as 3MV/cm at the corner of the p-

well while the device is blocking 2000V. This large field initiates impact ionization in the device.

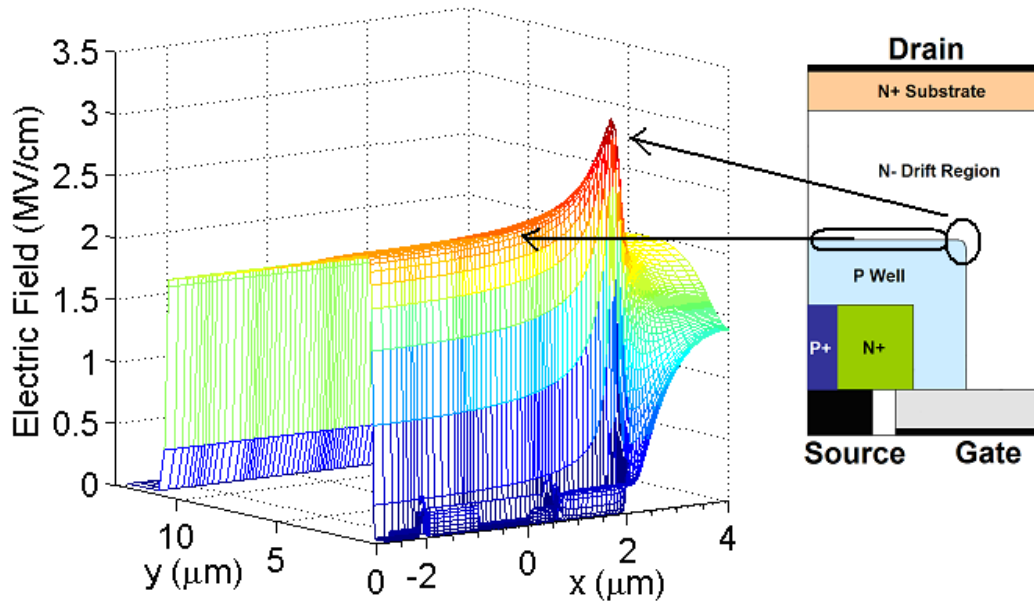


Fig. 4.16 Peak electric field of approximately 3MV/cm seen at the corner of the p-well region in the 4H-SiC DMOSFET structure under 2kV drain bias and 0V gate and source biases.

Fig. 4.17 shows the impact ionization rate (G_{ii}) inside the device just prior to breakdown. As can be seen clearly, the maximum ionization is observed at the corners of the p-well where the electric field is the maximum. The 4H-SiC DMOSFET breaks down at values of G_{ii} greater than $1 \times 10^{27} \text{ cm}^{-3} \text{ s}^{-1}$.

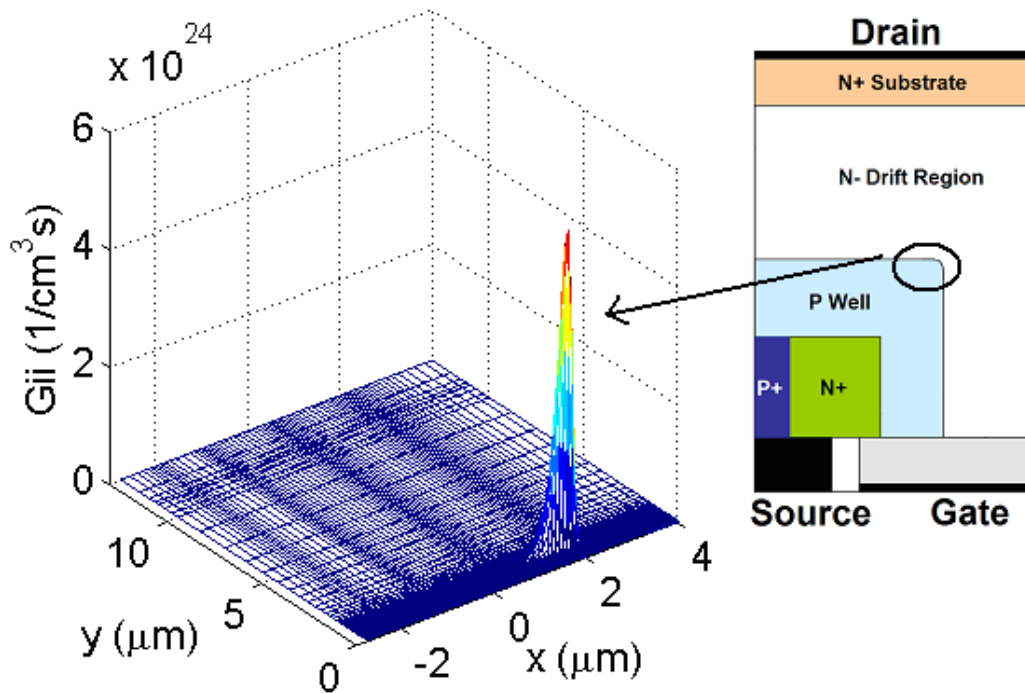


Fig. 4.17 Impact ionization rate inside the DMOSFET at 2kV drain bias. The largest impact ionization rate is seen at the *p*-well boundary where the electric field also has its maximum.

We ramp up the drain voltage in small steps and calculate the current at each value to find the maximum blocking voltage for the device. Fig. 4.18 shows the current density in the device at the onset of impact ionization (approximately drain voltage of 2043V). As can be seen in the figure, due to the generation of huge number of electrons and holes near the *p*-well junction, a low-resistance path between the source and the drain contacts passing through the high field region near the edge of the *p*-well is created. A large current begins flowing along this path and thereby further increases impact ionization in the device. This eventually leads to breakdown in the 4H-SiC DMOSFET.

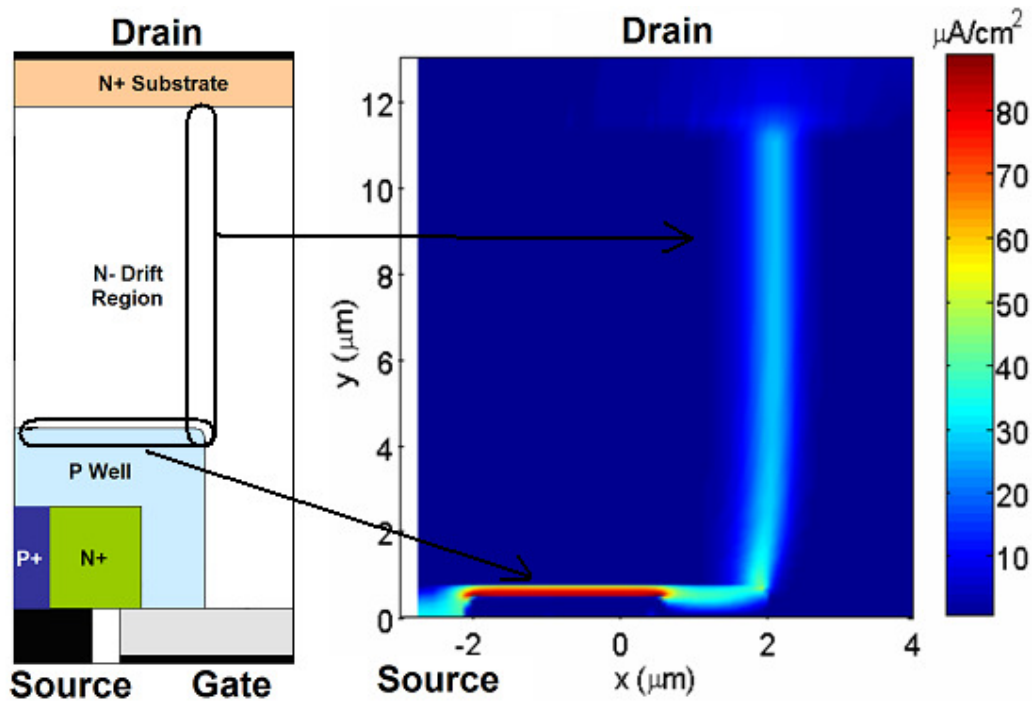


Fig. 4.18 Current density inside the DMOSFET just prior to breakdown shows creation of a very low resistance path from the source contact, through the *p*-well region and the completely depleted drift region, to the drain contact.

Finally, as shown in Fig. 4.19, we see breakdown due to impact ionization occurring at 2048V for the device under test, causing the current to rise exponentially from a few nanoamperes to several milliamperes. Another interesting feature of the 4H-SiC DMOSFET is the extremely low leakage current seen in Fig. 4.19. The large bandgap and extremely low intrinsic carrier density gives us this low leakage current of a few nanoamperes even at drain biases in excess of 2kV.

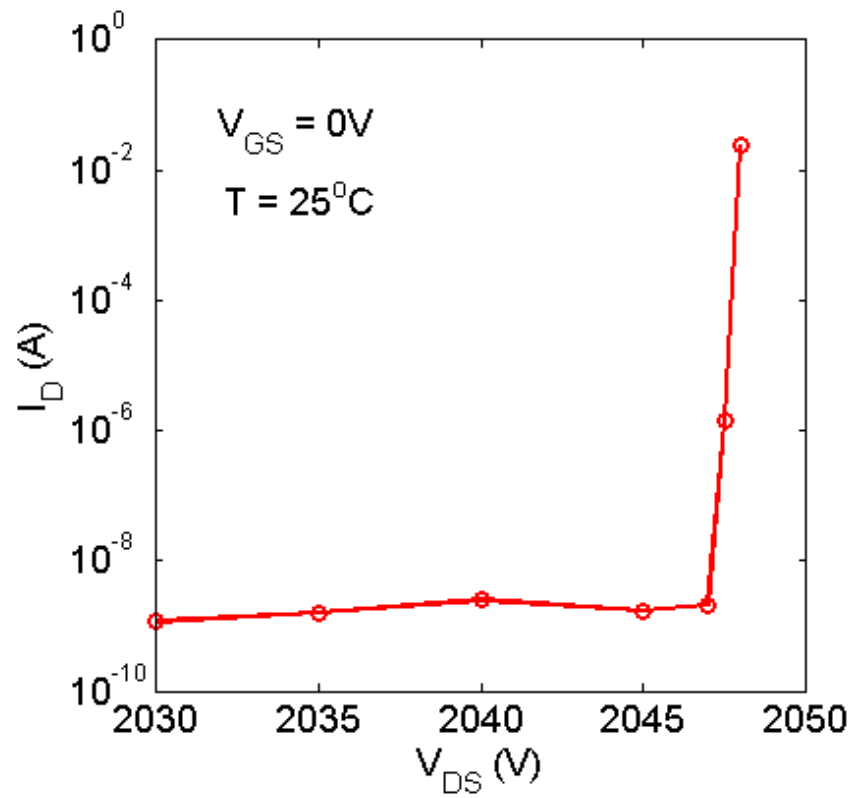


Fig. 4.19 I_D - V_{DS} showing impact ionization occurring at approximately 2048V in the 4H-SiC DMOSFET. The off-state current jumps from the nanoamperes level to several milliamps due to avalanching effect.

4.4. DC-DC Converter Mixed Mode Simulation

4H-SiC DMOSFETs are power devices which will be employed as switches in power converter modules. Typical operating scenario for a 4H-SiC DMOSFET would be in a transient switching mode at switching frequencies in excess of 20 kHz. The DMOSFET will require to pass a large current during ON state while block a large voltage during OFF. Fig. 4.20 shows a typical boost-converter circuit schematic in which the power DMOSFET is given a gate pulse to turn it ON and OFF.

When the DMOSFET is turned ON, it provides a low resistance path for current to flow. This causes the drain voltage to reduce close to zero, and the inductor is charged. The inductor current increases almost linearly with time, giving rise to a constant voltage close to the battery voltage across the inductor. During the ON cycle, the diode D1 is OFF and the storage capacitor C2 supplies power to the load RL.

When the DMOSFET is turned OFF, the current through the DMOSFET goes to zero and the inductor current starts decreasing. This changes the polarity of the inductor voltage and the sum of the battery voltage and the inductor voltage appears at the drain of the DMOSFET. This turns ON the diode D1, and the inductor current then charges the storage capacitor C2 and also supplies power to the load. Thus, the load resistor is supplied current via the inductor when the DMOSFET is turned OFF, and through the capacitor C2 when the DMOSFET is ON.

Variation of the duty cycle of the gate voltage enables us to change the output voltage across the load resistor. A 50% duty cycle causes twice the battery voltage to appear across the load resistance. The efficiency of such a boost converter circuit can be

higher than 90%. In order to achieve this high efficiency, the ON resistance of the DMOSFET needs to be as small as possible.

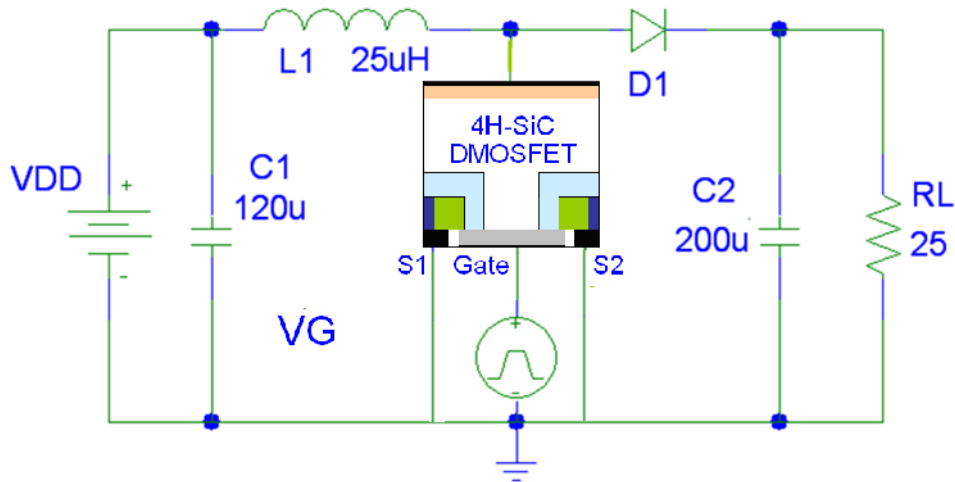


Fig. 4.20 Schematic of a boost converter using the 4H-SiC DMOSFET as a switch. VDD is the battery, VG provides the switching gate pulses to the DMOSFET, L1 and C2 are the energy storage units, and RL is the load.

4.4.1. Mixed Mode Simulation Methodology

The DMOSFET has an inductive load during ON state. Modeling the switching behavior of the DMOSFET under this inductive load is essential to understand the limitations imposed on switching frequency, interface trap dynamics, reverse recovery, etc. We carried out mixed-mode simulation of a 4H-SiC DMOSFET operating as a switch with an inductive load with a goal to eventually building a complete 4H-SiC MOSFET mixed-mode simulator for simulating complex power converter circuits.

Fig. 4.21 shows the circuit we simulated as part of this effort. The DMOSFET is switched from OFF to ON by applying a 10V pulse to the gate. We calculate the effect of the inductive load on the drain current and drain voltage of the DMOSFET when the device is turned ON and when it is turned back OFF.

The actual boost converter is designed with a $25\mu\text{H}$ inductor, and ten cells of the simulated 4H-SiC DMOSFET. We simulate a single cell of the DMOSFET, and so we scale all the components while simulating the circuit. The real circuit can be thought of as a parallel combination of the circuit shown in Fig. 4.21. As the inverse of the inductance is summed in a parallel circuit, ten inductors each of $250\mu\text{H}$ in parallel are equivalent to a single $25\mu\text{H}$ inductor. That is why we show a $250\mu\text{H}$ inductance for the mixed mode simulation.

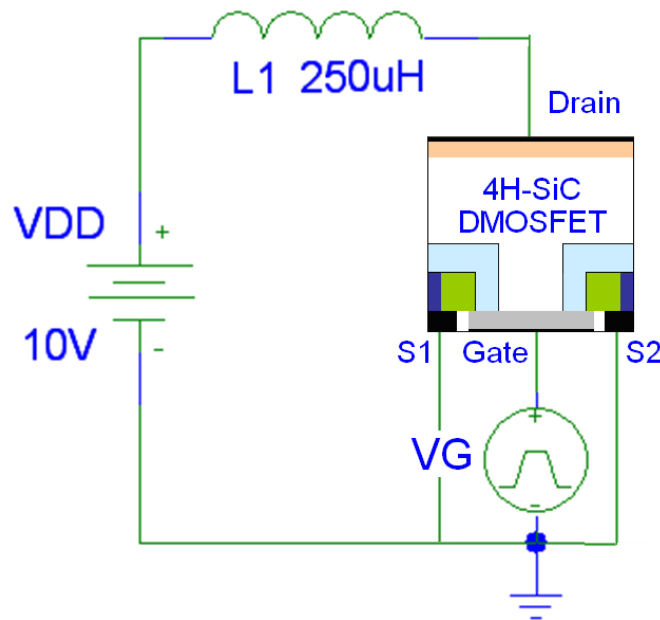


Fig. 4.21 Circuit with the inductively loaded 4H-SiC DMOSFET for mixed-mode simulation.

Mixed mode simulation of the above circuit involves solving Kirchoff's laws along with the semiconductor Drift-Diffusion equations self-consistently. For the circuit in Fig. 4.21, we can write Kirchoff's voltage law as

$$V_{DD} - L \frac{dI_L}{dt} = V_{DS} \quad (4.14)$$

Where I_L is the current flowing through the loop, L is the inductive load, V_{DD} is the battery voltage and V_{DS} is the voltage at the drain of the 4H-SiC DMOSFET.

The current flowing through the DMOSFET depends upon the drain bias and is calculated by solving the complete Drift-Diffusion system of equations (Numerical solution is described in chapters 2 and 3).

$$I_D(t) = f_{DD}(V_{DS}(t), V_{GS}(t)) \quad (4.15)$$

f_{DD} represents the solution of the drift-diffusion system of equations for the applied gate bias at time t , and the estimated drain voltage at time t . For the circuit of Fig. 4.21, the inductor current is equal to the drain current. Therefore, equations (4.14) and (4.15) are solved iteratively at each time t to obtain unique values of I_D and V_{DS} at that time.

We also simulate the above shown circuit along with a load resistor as shown in Fig. 4.28. We follow the same methodology as discussed above to solve for the drain voltage and current during the switching cycles. But in this case, the inductor current is equal to the sum of the drain current and the current through the load resistance.

$$I_L(t) = I_D(t) + I_R(t) = I_D(t) + \frac{V_D(t)}{R_L} \quad (4.16)$$

Equations (4.14), (4.15) and (4.16) are solved iteratively at each time t to obtain solutions for current through the DMOSFET and the drain voltage.

4.4.2. Mixed Mode Simulation Results

4H-SiC DMOSFET with Inductive Load (Fig. 4.21): As a first step towards mixed mode simulation of complete power converter circuits, we simulated a 4H-SiC DMOSFET with an inductive load and subject to a 0-10V gate pulse. When the gate pulse is applied to the DMOSFET, the device turns on and draws current from the battery and thereby charges the inductor. The DMOSFET provides a very low resistance path for the current to flow. Therefore, the voltage at the drain drops down quickly to a very low value as shown in Fig. 4.22 and Fig. 4.23.

As the inductor charges up, it draws more current from the supply, and so the drain voltage of the DMOSFET rises up. The DMOSFET remains in the linear region of operation during the entire charging cycle. The current rises almost linearly with time as shown in Fig. 4.24. The linear change in current with time translates to almost a constant voltage across the inductor. If the DMOSFET were an ideal switch with zero resistance, the entire supply voltage would appear across the inductor with zero voltage at the DMOSFET drain.

Fig. 4.25 shows the power dissipated by the 4H-SiC DMOSFET during this charging cycle. The power dissipated is limited to a few milliwatts and so most of the energy is stored in the inductor in the charging cycle. This energy is then transferred to the load when the DMOSFET is turned OFF.

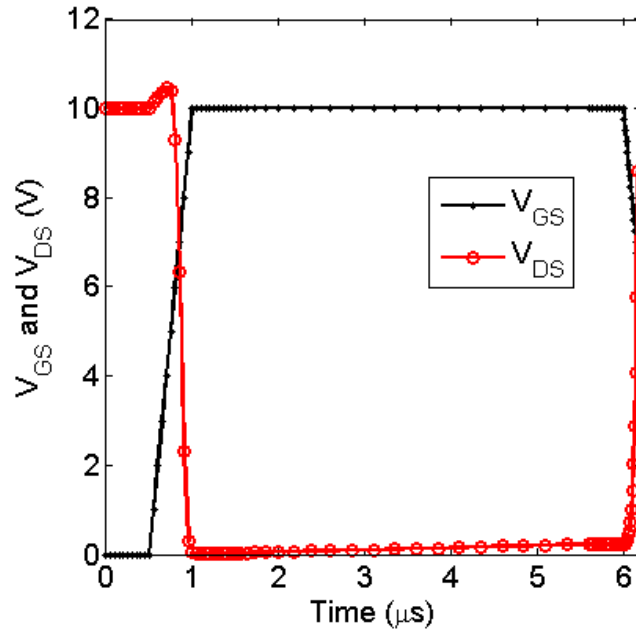


Fig. 4.22 Turn ON response of the 4H-SiC DMOSFET with an inductive load. The DMOSFET provides a low resistance path for the current to flow, and so the drain voltage decreases to a very small value during the ON (inductor charging) cycle.

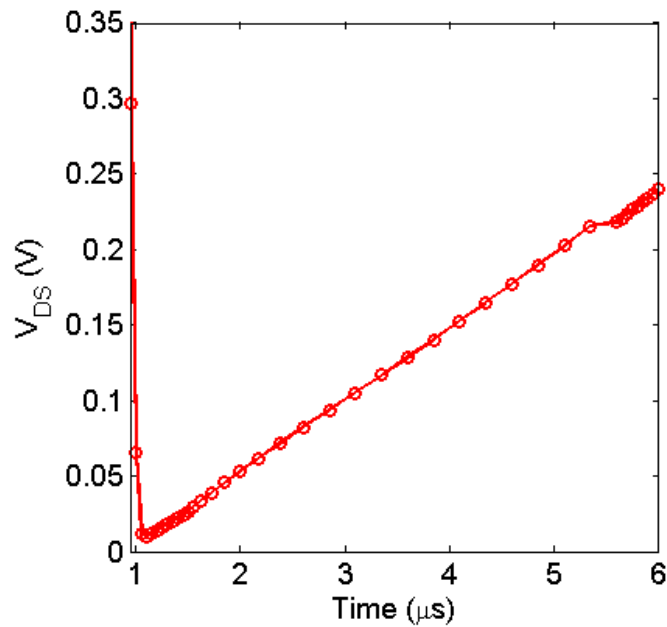


Fig. 4.23 Voltage at the drain of the 4H-SiC DMOSFET during the charging cycle of the boost converter. The drain voltage is very low as the DMOSFET provides a low resistance path for the inductor's charging current.

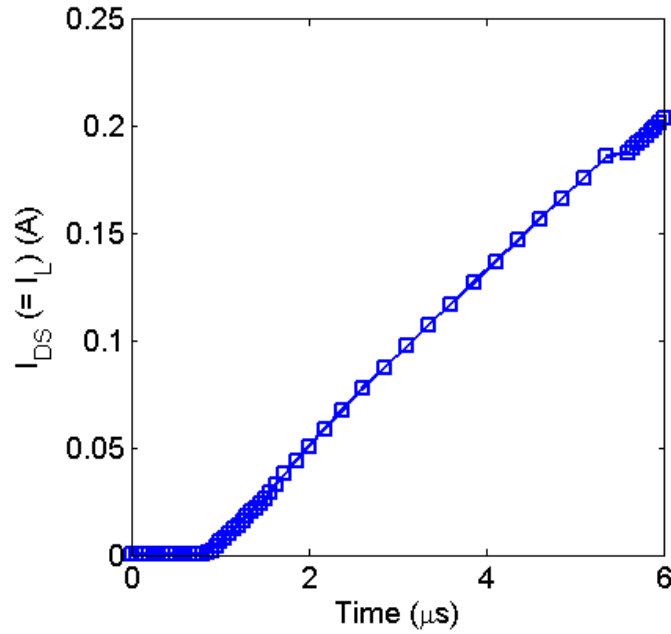


Fig. 4.24 Current during turn ON of a 4H-SiC DMOSFET with an inductive load. The current rises almost linearly with time thereby ensuring that the voltage across the inductor remains close to VDD, and the drain voltage remains very low.

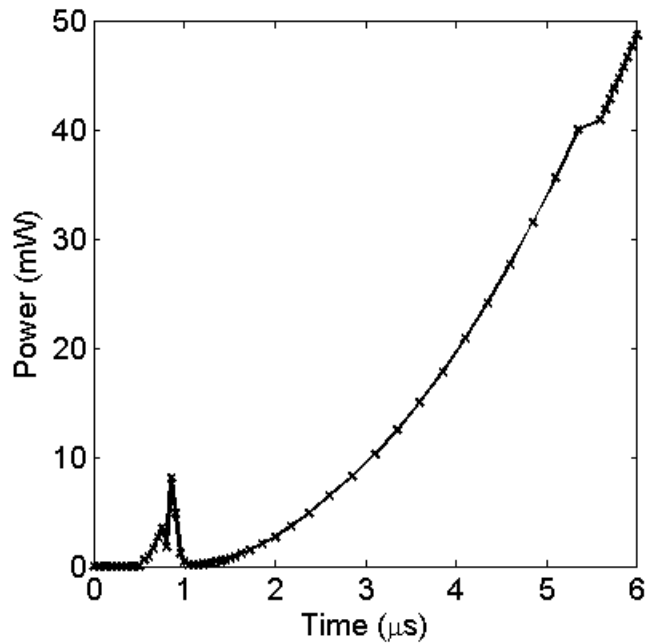


Fig. 4.25 Power dissipation in the 4H-SiC DMOSFET during the charging cycle of the boost converter.

Fig. 4.26 and Fig. 4.27 show the turn OFF behavior of the 4H-SiC DMOSFET with an inductive load. When the DMOSFET is turned off, the current in the DMOSFET tries to go to zero. But the inductor does not allow the current to reduce to zero instantaneously. As there is no other path for the current to flow through, the inductor and the drain-source capacitance of the DMOSFET form a leaky L-C tank circuit. This gives rise to large oscillations in the voltage at the drain and current in the 4H-SiC DMOSFET. In a complete boost-converter as shown in Fig. 4.20, the inductor supplies power (current) to the load resistance via the diode D1 when the DMOSFET is turned off. This effectively limits the voltage at the drain of the DMOSFET to a maximum of $2 \cdot V_{DD}$.

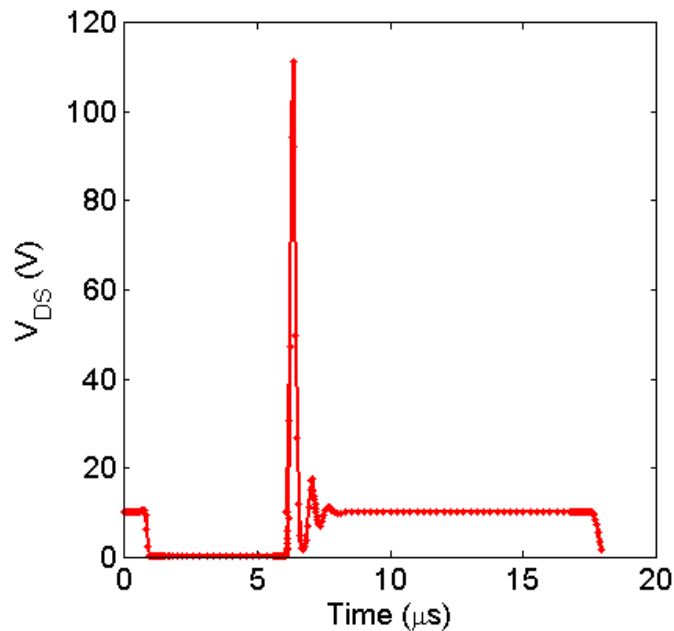


Fig. 4.26 Turn OFF behavior of the 4H-SiC DMOSFET with inductive load showing the voltage ripples which occur due to creating of a leaky L-C tank circuit.

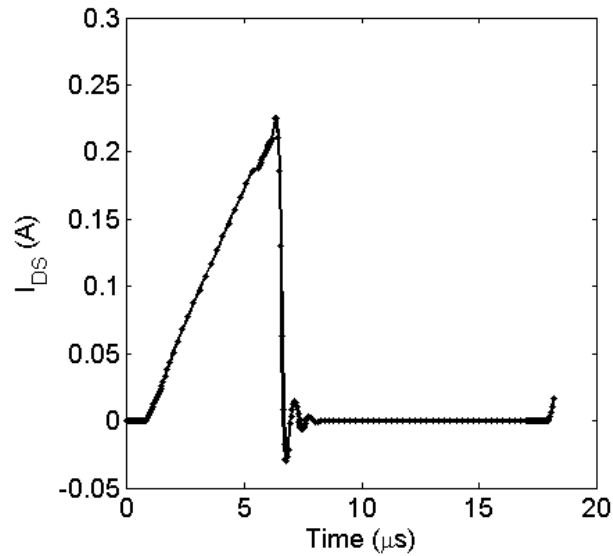


Fig. 4.27 Current in the inductively loaded 4H-SiC DMOSFET during ON and OFF state. Oscillations in the current can be seen due to formation of a leaky L-C tank circuit during turn OFF.

4H-SiC DMOSFET with Inductor and Load Resistance (Fig. 4.28): Finally we model the boost converter with a resistive load. The mixed mode simulation now consists of the battery, charging inductor, 4H-SiC DMOSFET and a resistance representing the electric motor load. Fig. 4.27 shows the circuit used for the mixed mode simulation.

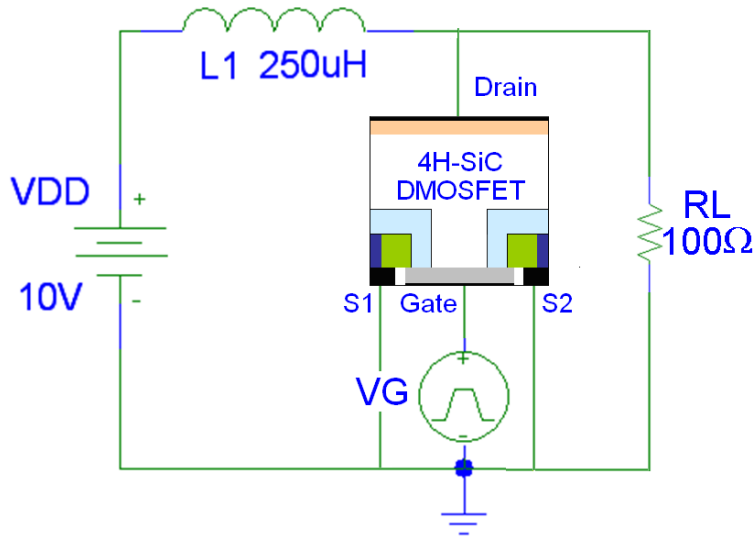


Fig. 4.28 Inductively loaded 4H-SiC DMOSFET and a load resistance mimicking the operation of a full boost converter.

Use of the resistive load provides a discharge path for the current that is stored in the inductor when the DMOSFET is ON. When the DMOSFET is turned ON, the DMOSFET provides a very small resistance path for the current to flow. Therefore, the drain voltage drops to a low value effectively shorting out the load resistance. In the complete boost converter circuit, a storage capacitor would be supplying power to the load resistance during this phase of the switching cycle. As shown in Fig. 4.29, when gate voltage is high, the drain voltage drops to a small value. The inductor current is equal to the DMOSFET drain current during this time, and it increases almost linearly with time. This is shown in Fig. 4.30. During this time, the load current is close to zero.

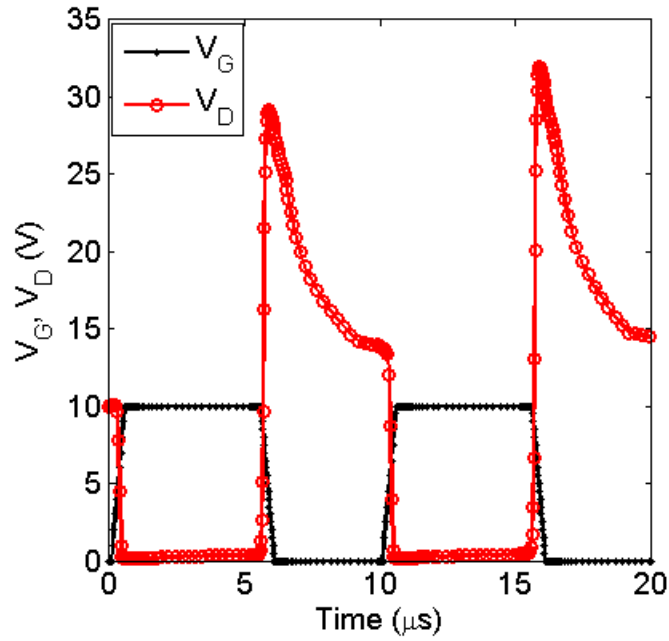


Fig. 4.29 Drain voltage on the 4H-SiC DMOSFET during the switching cycles of the mixed mode simulation of the boost converter circuit.

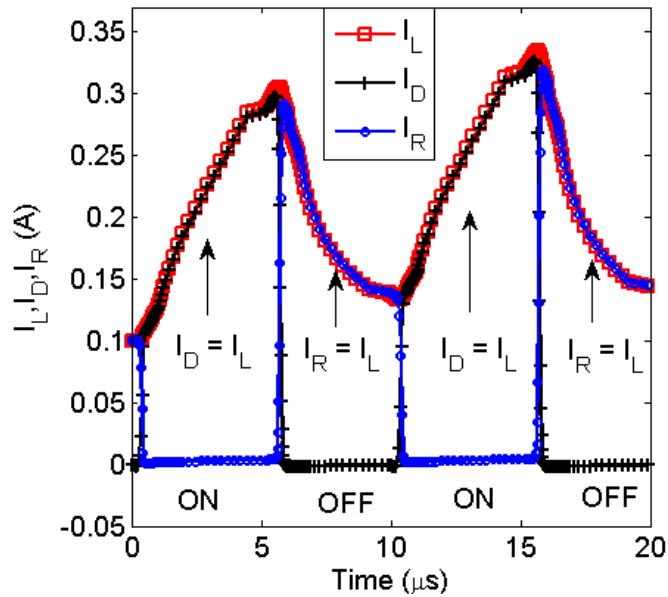


Fig. 4.30 Inductor (I_L), 4H-SiC DMOSFET drain (I_D), and load (I_R) currents during the ON-OFF switching cycles of the boost converter mixed mode simulation

When the DMOSFET is turned OFF, the drain current reduces to zero very quickly, leaving the inductor current to flow through the load resistance. During this OFF cycle, the inductor transfers power to the load resistance. The load current equals the inductor current and it slowly decreases with time. The drain voltage (voltage across the load) rises quickly at first as the polarity of the inductor voltage changes sign, but then decreases with time. This continues until the 4H-SiC DMOSFET is turned back ON, after which the whole inductor charging and discharging cycle is repeated.

We do not see the voltage and current oscillations of Fig. 4.26 and Fig. 4.27 in this simulation because the inductor current has a discharge path through the load resistance in this case. So there is no oscillatory L-C tank circuit as with the first case, leading to an absence of the voltage and current oscillations.

Mobile Charge inside the 4H-SiC DMOSFET during Turn-ON: Electron and hole concentrations inside the 4H-SiC DMOSFET change rapidly during the turn-ON part of the boost converter switching cycle. The electron and hole concentrations inside the DMOSFET are shown for different times during the turn-on phase of the switching cycle in Fig. 4.31. When the gate voltage in the DMOSFET is ramped up, electrons flow from the highly doped source into the channel and build up the inversion charge. These inversion layer electrons are pulled by the drain-source field into the JFET and drift regions, thereby creating a path for the DMOSFET current to flow. As shown in the figure, the entire inversion layer is formed in the $0.5\mu\text{s}$ it takes for the gate to ramp up to its maximum value. During this time, the hole concentration in the channel and JFET regions decreases rapidly from its depletion levels (close to the intrinsic concentration) to very small values ($\sim 10^{-30}\text{cm}^{-3}$). The majority carriers (electrons) and the minority carriers (holes) respond almost immediately to the applied gate signal, and so the DMOSFET can easily respond to a fast gate turn-on signal. From $0.5\mu\text{s}$ to $5.5\mu\text{s}$, the gate voltage is held constant at 5V. During this time the current in the DMOSFET is rising almost linearly with time as has been shown in Fig. 4.30. The electron concentration in the channel and JFET regions also rises correspondingly, but as the inversion layer is completely formed and surface electron concentration has already reached $\sim 10^{19}\text{cm}^{-3}$ levels during turn-ON, any further rise in electron concentration ($\sim 10^{19}\text{cm}^{-3}$ to $\sim 10^{20}\text{cm}^{-3}$) cannot be visualized on the log scale of the plots.

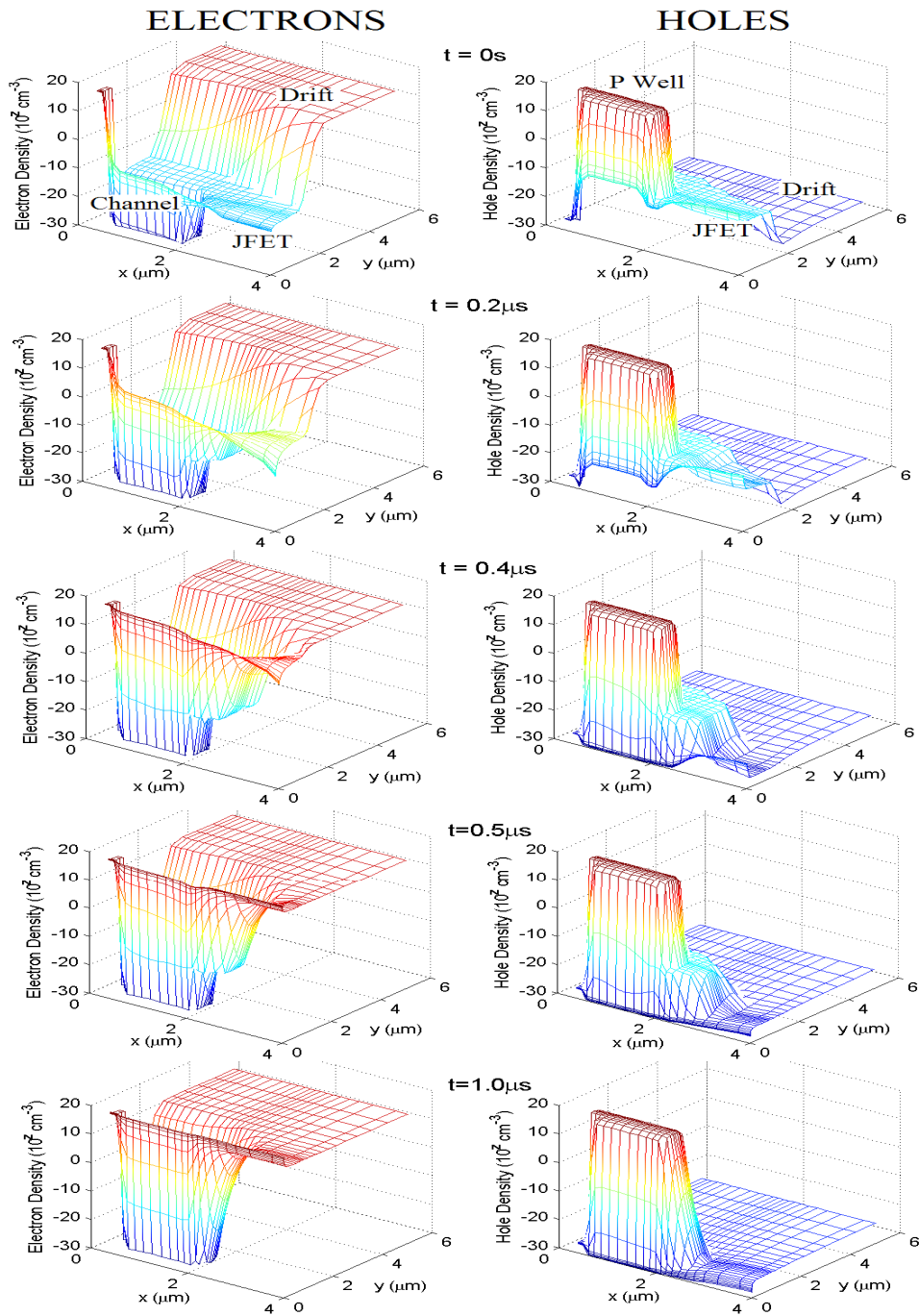


Fig. 4.31 Electron and hole concentration inside the 4H-SiC DMOSFET changing with time during turn on. Electron plots show the formation of the inversion layer in the channel and occupation of the JFET region by electrons leading to current flow. Hole concentration plots show decrease in concentration in the JFET regions with time as the gate voltage rises.

Mobile charge inside the 4H-SiC DMOSFET during TURN-OFF: Fig. 4.32 shows the changes in the electron and hole concentrations inside the DMOSFET during the turning OFF phase of the switching cycle. As the gate is turned off, the electrons in the channel and JFET regions rapidly decrease in concentration to the intrinsic carrier concentration levels. As seen in the plots of electron concentration, the JFET region loses its electrons before the channel. The hole concentration in the channel and JFET regions rises from the 10^{-30}cm^{-3} levels to the intrinsic carrier concentration values of approximately 10^{-8}cm^{-3} . The minority and majority carriers need a finite amount of time to go back to their steady OFF state levels. This time characterizes the minimum OFF time required for proper operation of the boost-converter circuit. In other words, the rate of change of minority and majority carriers during turn OFF determines the reverse recovery characteristic of the 4H-SiC power DMOSFET, and thereby imposes a limit on the maximum allowed switching frequency. After turn OFF has been achieved, a depletion region is reformed in the JFET and drift region whose width depends upon the value of the blocked drain-source voltage.

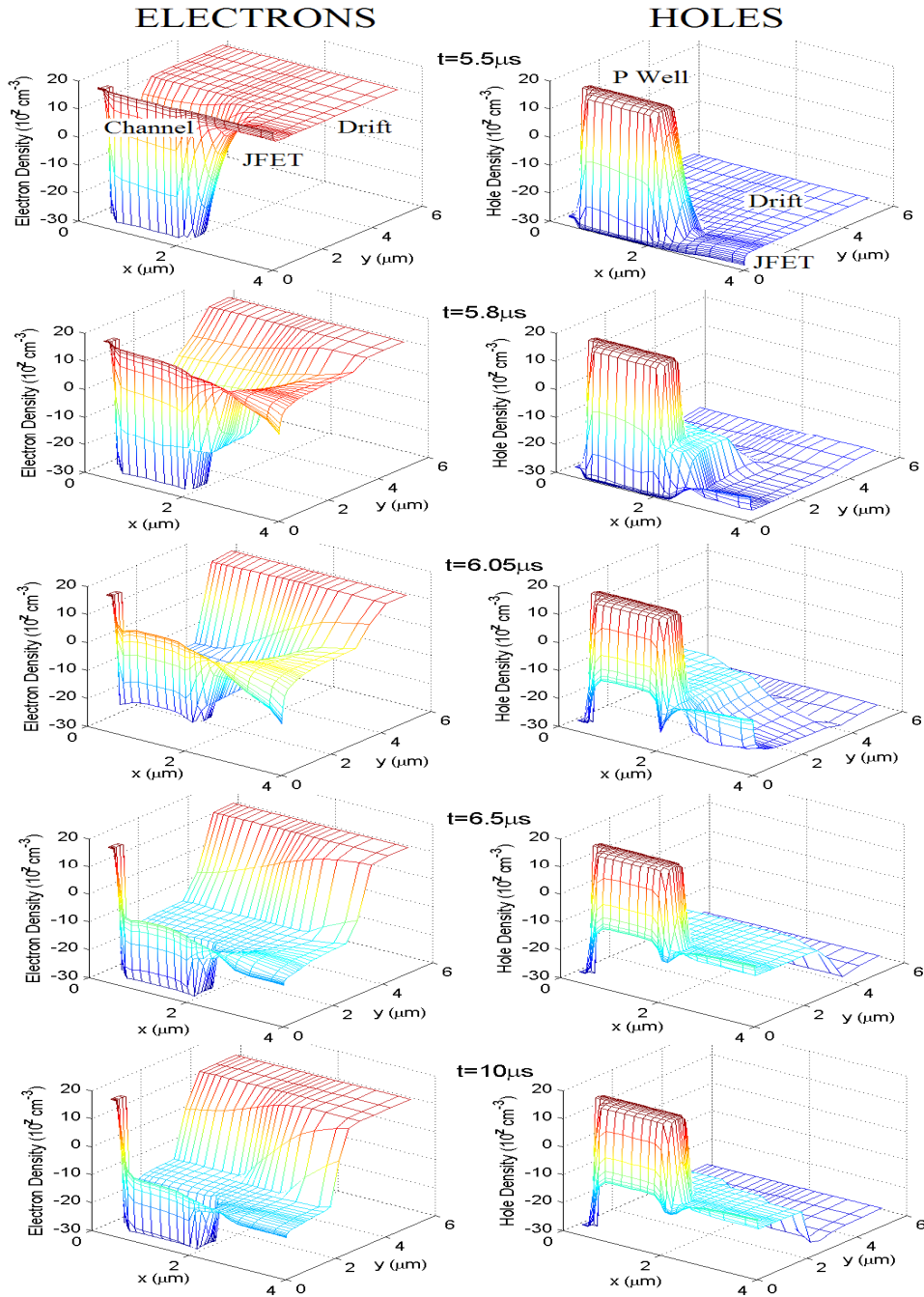


Fig. 4.32 Electron and hole concentration inside the 4H-SiC DMOSFET during the turn off cycle. Electron plots show rapid decrease in electron concentration in the JFET and channel regions with a final level equal to the intrinsic carrier concentration emerging there. Hole concentration rises from the 10^{-30} cm^{-3} ON state levels in the channel and JFET regions to the intrinsic carrier concentration. The OFF state depletion region in the drift and JFET regions evolves during this turn OFF phase.

4.5. Chapter Summary

We described the design and operation of a 4H-SiC power DMOSFET and compared it to a Silicon DMOSFET in terms of its blocking voltage and ON resistance capabilities. We saw that the SiC devices have a significantly higher figure of merit than Si power DMOSFETs.

We modeled the operation of a high power 4H-SiC DMOSFET in the ON and OFF states using our custom 2-D Drift-Diffusion simulator. The ON resistance of the test DMOSFET was approximately $25\text{m}\Omega$ at room temperature. Approximately 75% of this resistance was due to the channel resistance.

We extracted interface trap density of states and surface roughness parameter values for the DMOSFET by comparing simulated I-V curves to experiment. We saw that less than 50% of the total induced charge in the device serves as mobile inversion charge, while the rest just fills up the interface traps. We also calculated that at the operating conditions of high gate bias, surface roughness is the dominant mobility degradation mechanism in this device.

We also simulated the OFF state behavior of the 4H-SiC DMOSFET and modeled impact ionization related breakdown in the device. We found that impact ionization is initiated at the corners of the p -wells and at the p -well n -drift junctions. The calculated breakdown voltage for the device was found to be in excess of 2kV.

Finally, we implemented a mixed-mode simulator for simulating an inductive load on the 4H-SiC DMOSFET. We see how current is stored in the charging inductor when the DMOSFET is turned ON, and that the charged inductor supplies power to the load during the OFF period of the switching cycle.

Chapter 5

5. Summary, Conclusions and Future Work

In this chapter we summarize the results of this research, highlight the major conclusions and discuss the further course of research.

5.1. Summary of Research

Silicon Carbide MOSFETs and power MOSFETs have enormous potential for replacing Silicon based devices in high power, high temperature applications. The advantages of SiC over Si lie in its material properties such as high bandgap, high thermal conductivity and very high breakdown field. These properties enable us to fabricate SiC high power devices that can operate at very high temperatures ($>400^{\circ}\text{C}$), pass tens of amperes of current in the ON state while leaking only a few nanoamperes in the OFF state, and block tens of kilovolts without breaking down. While these properties make SiC MOS devices ideal for high power electronics applications, current generation devices are plagued with severe problems. Our research has focused on identifying, understanding, and quantifying the effects of these bottlenecks which degrade the performance of 4H-SiC MOSFETs.

We employed a robust and rigorous numerical modeling and electrical characterization approach to understand transport in 4H-SiC MOSFETs and power DMOSFETs, at room and high temperatures, in DC, AC and transient regimes of operation. We developed physical models for scattering mechanisms such as Coulomb

scattering from interface traps and surface roughness scattering, and incorporated them as mobility models in our custom 2D Drift Diffusion based device simulator for 4H-SiC MOS devices. We modeled and characterized the behavior of interface traps at room and high temperatures and extended the experimental characterization of interface trap density of states to the entire bandgap. We modeled I-V characteristics of 4H-SiC lateral MOSFETs and power DMOSFETs, and compared them to simulations to extract values for physical quantities such as interface trap densities, fixed oxide charge, surface electron saturation velocity, and roughness at the SiC-SiO₂ interface.

We developed a new generation-recombination model to explain the dynamic interaction between interface traps and inversion layer electrons during transient switching of the 4H-SiC MOSFET. Using this model, and with close comparison with ultra-fast transient current measurement, we were able to extract effective capture cross-sections of the traps in a SiC-SiO₂ system. On the basis of the extracted effective capture cross-sections we were able to distinguish between interface, near-interface, and oxide traps.

Finally, we developed numerical and physical models to characterize the ON state and OFF state performance of 4H-SiC power DMOSFETs. We analyzed the turn ON characteristics of the DMOSFET and extracted relevant physical parameters from close corroboration with experiment. We also simulated the breakdown behavior of these devices and evaluated blocking voltage capability of the test 4H-SiC DMOSFET. We developed a mixed-mode simulator to analyze the performance of an inductively loaded 4H-SiC DMOSFET in form of a DC-DC boost converter.

5.2. Major Conclusions

Listed below are the main conclusions of this research.

4H-SiC MOS Device Simulator: A comprehensive 2-D Drift Diffusion based device simulator has been developed for 4H-SiC MOS devices, which incorporates quantum corrections calculated using the Density Gradient methodology. Physical models for Coulombic scattering from interface traps, surface roughness scattering, interface trap density of states and occupation, generation-recombination, incomplete ionization, temperature dependence of mobility, dynamics of interface traps, impact ionization, and other physical effects typical to SiC devices have been developed and implemented.

Interface Traps in 4H-SiC MOSFETs: Interface traps play a major role in determining transport in 4H-SiC MOSFETs by reducing surface mobility at low gate biases, and by reducing the amount of mobile inversion charge. Less than 50% of total induced charge in current generation 4H-SiC MOSFETs is available for conduction. Extracted interface trap density of states show an exponential increase near the band edges, with values at the conduction band edge in the mid $10^{13} \text{ cm}^{-2}\text{eV}^{-1}$ range. The mid-gap density of states is in the low to mid $10^{11} \text{ cm}^{-2}\text{eV}^{-1}$ range. Interface trap states show more spreading into the bandgap at higher temperatures (band-tail energy increases with temperature), while the band-edge values decrease due to reduction in bandgap at high temperatures. Screening of interface traps plays a big role at high gate biases, effectively reducing Coulombic scattering by traps and thereby increasing Coulomb mobility significantly.

Surface Roughness: A robust surface roughness mobility model that incorporates the effect of step bunching arising due to the off-axis growth process of SiC wafers has been developed and implemented. Step bunching is observed at the interface, with an extracted root mean square step height of approximately 3.5nm. Surface roughness mobility dominates transport at high gate biases. Surface electron mobilities were found to be as low as $20 \text{ cm}^2/\text{Vs}$ at room temperature.

Trap Dynamics and Effective Capture Cross-sections: A generation-recombination model and a dynamic trapping model have been developed to characterize the interaction between interface traps and inversion layer electrons in 4H-SiC MOSFETs. Experiments to measure the transient characteristics of SiC MOSFETs show a characteristic decay in drain current with time indicating the presence of interface, near-interface and oxide traps. Extracted “effective capture cross-sections” of the traps showed that traps lying close to the band-edge were fast traps, while those away from the band-edge behaved like slow near-interface or oxide traps.

High Power DMOSFETs: The operation of a high power 4H-SiC DMOSFET in the ON and OFF states was modeled and analyzed. Extracted trap densities and surface roughness parameters were similar to those for lateral MOSFETs. Approximately 80% of the ON resistance in the test device was due to the channel resistance. Impact ionization related breakdown in the 4H-SiC DMOSFET was modeled and the calculated the breakdown voltage was in excess of 2kV. A mixed-mode simulator for simulating a boost converter circuit using a 4H-SiC DMOSFET was implemented.

5.3. Future Work

Significant effort needs to be put in to develop robust models for transport in SiC MOS devices. TCAD based device design requires thorough analysis of the physics of processing, and transport mechanisms typical to SiC devices. Further, due to the rather uncoordinated approach to process standardization for SiC devices, many physical parameters relevant to one manufacturer may not be applied to others. A few areas where our research can be extended to which would help in understanding, quantifying and eventually standardizing models for SiC MOS devices are given below.

One of the recent observations in 4H-SiC MOSFETs is the presence of a transition region comprising of Silicon, Carbon and Oxygen (Si-C-O layer) at the SiC-SiO₂ interface. It has been shown that this transition layer maybe several nanometers thick. Modeling and characterizing the effect of this transition region may serve to be very important in gaining better understanding of transport in the channel in SiC MOSFETs.

Modeling heat generation and dissipation especially during switching of SiC power DMOSFET is very essential for efficient circuit design. Solving the heat flow equation along with the semiconductor equations would allow us to extract the effect of rising lattice temperature, and also creation of hot spots in the device. Further, using the heat equation and thermal resistances associated with bonding and packaging materials, we would be able to generate temperature maps for the power DMOSFETs, and also suggest appropriate cooling methodologies for the power converter systems.

In our research, we briefly touched on deriving compact model parameters for SiC MOSFETs. More work can be done in this area to extract the complete BSIM model

for SiC, which can be then used to simulate circuits using SiC MOSFETs and DMOSFETs. Closely correlating the compact model to the more physical Drift-Diffusion model and to experimental measurements is another very interesting research area.

Device modeling and characterization techniques can be implemented to analyze the long term stability issues of current generation SiC MOS devices. Presence of deep oxide states causing threshold voltage instability and giving rise to hysteresis in I_D - V_{GS} curves can be analyzed by implementing an oxide tunneling model within the Drift-Diffusion framework.

Chapter 6

6. Thesis Publications

6.1. Journal Publications

- [1] S. Potbhare, N. Goldsman, et al., “A Physical Model of High Temperature 4H-SiC MOSFETs”, IEEE Trans. on Electron Devices, vol. 55, pp.2029-2040 (2008)
- [2] S. Potbhare, N. Goldsman, J. Suehle, et al., “Energy and Time Dependent Dynamics of Trap Occupation in 4H-SiC MOSFETs”, IEEE Trans. on Electron Devices, vol. 55, pp. 2061-2070 (2008)
- [3] S. Potbhare, N. Goldsman, et al., “A quasi-two-dimensional depth-dependent mobility model suitable for device simulation for Coulombic scattering due to interface trapped charges”, J. Appl. Phys., Vol. 100, 044516 (2006)
- [4] S. Potbhare, N. Goldsman, et al., “Numerical and experimental characterization of 4H-silicon carbide lateral metal-oxide-semiconductor field-effect transistor”, J. Appl. Phys., Vol. 100, 044515 (2006)

6.2. Conference Publications

- [5] S. Potbhare, N. Goldsman, et al., “Investigation of ON and OFF State Characteristics of 4H-SiC DMOSFETs”, ECSCRM 2008, Barcelona, Spain
- [6] S. Potbhare, N. Goldsman, et al., “Effects of Quantum Confinement on Interface Trap Occupation in 4H-SiC MOSFETs”, SISPAD 2008, Japan

- [7] S. Potbhare, N. Goldsman, A. Lelis, “Modeling and Characterization of a 4H-SiC DMOSFET”, MRS Spring 08 Workshop, San Francisco, CA (2008)
- [8] S. Potbhare, N. Goldsman, A. Lelis, “High Temperature High Field Numerical Modeling and Experimental Characterization of 4H-SiC MOSFETs”, Proc. of ISDRS 2007, College Park, MD (2007)
- [9] S. Potbhare, N. Goldsman, et al., “Transient Characterization of Interface Traps in 4H-SiC MOSFETs”, Proc. of SISPAD 2007 (2007)
- [10] S. Potbhare, N. Goldsman, et al., “Time Dependent Trapping and Generation-Recombination of Interface Charges: Modeling and Characterization for 4H-SiC MOSFETs”, Mat. Sci. Forums, Vols. 556-557, pg. 847 (2007)
- [11] S. Potbhare, N. Goldsman, et al., “Using a First Principles Coulomb Scattering Mobility Model for 4H-SiC MOSFET Device Simulation”, Mat. Sci. Forums, Vols. 527-529, pg. 1321 (2006)
- [12] S. Potbhare, N. Goldsman, et al., “Characterization of 4H-SiC MOSFET Interface Trap Charge Density Using a First Principles Coulomb Scattering Mobility Model and Device Simulation”, Proc. of SISPAD 05, pp. 95-98 Japan (2005)
- [13] D. Habersat, S. Potbhare, et al., “The Effect of Nitridation on SiC MOS Oxides as Evaluated by Charge Pumping”, Mat. Sci. Forums, vol. 600-603, pg. 743-746 (2009)
- [14] A. Lelis, S. Potbhare, et al., “Modeling and Characterization of Bias Stress-Induced Instability of SiC MOSFETs”, Proc. of IIRW 06, pg. 160 (2006)

- [15] G. Pennington, S. Potbhare, et al., "Electron Transport at Technologically Significant Stepped 4H-SiC/SiO₂ Interfaces", Proc. of SISPAD 2006, pg. 236 (2006)
- [16] G. Pennington, S. Potbhare, et al., "Impact of Surface Steps on the Roughness Mobility in 4H-SiC", Proc. of ISDRS 2005, pg. 143 (2005)
- [17] Jianzhou Wu, S. Potbhare, N. Goldsman, A. Lelis, "Numerical Modeling and Characterization of n-Channel 4H-SiC Double-Diffused Vertical Power MOSFET", Proc. of ISDRS 05, pg. 366 (2005)

Chapter 7

7. Bibliography

- [1] N. S. Saks, S. S. Mani, and A. K. Agarwal, "Interface trap profile near the band edges at the 4H-SiC/SiO₂ interface", *Appl. Physics Letters*, 76, pg. 2250 (2000)
- [2] H. Yano, T. Hirao, T. Kimoto, H. Matsunami, and H. Shiomi, "Interface properties in metal-oxide-semiconductor structures on n-type 4H-SiC (0338)", *Applied Physics Letters*, 81, pg. 4772 (2002)
- [3] G. Pensl, M. Bassler, F. Ciobanu, V. Afanasev, H. Yano, T. Kimoto, and H. Matsunami, "Traps at the SiC/SiO₂ Interface", *Mat. Res. Soc. Symp. Proc.*, 640, H3.2.1 (2001)
- [4] H. Linewih, and S. Dimitrijević, "Channel-carrier Mobility Parameters for 4H SiC MOSFETs", *Proc. 23rd International Conference on Microelectronics (MIEL 2002)*, 2, pg. 425 (2002)
- [5] H. Iwata, K. M. Itoh, and G. Pensl, "Theory of the anisotropy of the electron Hall mobility in n-type 4H- and 6H-SiC", *J. Appl. Phys.*, 88, pg. 1956 (2000)
- [6] Yu (Anne) Zeng, Amela Softic, and Marvin H. White, "Characterization of Interface Traps in Subthreshold Regions of Implanted 6H- and 4H-SiC MOSFETs", *International Semiconductor Device Research Symposium 2001*, pg. 213-215 (2001)
- [7] Charles J. Scozzie, and James M. McGarrity, "Effects of Interface-Trapped Charge on the SiC MOSFET Characteristics", *Proceedings: 4th International High Temperature Electrons Conference*, pg. 23 (1998)

- [8] Emil Arnold, and Dev Alok, "Effect of Interface States on Electron Transport in 4H-SiC Inversion Layers", *IEEE Trans. on Electron Devices*, 48, pg. 1870 (2001)
- [9] N. S. Saks, and A. K. Agarwal, "Hall mobility and free electron density at the SiC/SiO₂ interface in 4H-SiC", *Appl. Phys. Letters*, 77, pg. 3281 (2000)
- [10] S. Harada, R. Kosugi, J. Senzaki, W. Cho, K. Fukuda, K. Arai, and S. Suzuki, "Relationship between channel mobility and interface state density in SiC metal-oxide-semiconductor field-effect transistor", *J. Appl. Phys.*, 91, pg. 1568 (2002)
- [11] S. Suzuki, S. Harada, R. Kosugi, J. Senzaki, W. Cho, and K. Fukuda, "Correlation between channel mobility and shallow interface traps in SiC metal-oxide-semiconductor field-effect transistors", *J. Appl. Phys.*, 92, pg. 6230 (2002)
- [12] E. Dubaric, M. Hjelm, H-E. Nilsson, C. S. Petersson, and P. Käckell, "The Effect of Different Transport Models in Simulations of a 4H-SiC Ultra Short Channel MOSFET", *ICM '99: The Eleventh International Conference on Microelectronics*, (1999)
- [13] Matthias Roschke, and Frank Schwierz, "Electron Mobility Models for 4H, 6H, and 3C SiC", *IEEE Trans. on Electron Devices*, 48, pg. 1442 (2001)
- [14] H-E. Nilsson, K. Bertilsson, M. Hjelm, and E. Dubaric, "Numerical Simulation of Field Effect Transistors in 4H- and 6H-SiC", *J. of Wide Bandgap Materials*, 9, pg. 293 (2002)
- [15] H-E. Nilsson, U. Sannemo, and C. S. Petersson, "Monte Carlo simulation of electron transport in 4H-SiC using a two-band model with multiple minima", *J. Appl. Phys.*, 80, pg. 3365 (1996)

- [16] R. Mickevicius, and J. H. Zhao, "Monte Carlo study of electron transport in SiC", J. Appl. Phy., 83, pg. 3161 (1998)
- [17] J. B. Roldán, F. Gámiz, and J. A. López-Villanueva, "A Detailed Simulation Study of the Performance of β -Silicon Carbide MOSFETs and a Comparison with their Silicon Counterparts", Semiconductor Science and Technology, 12, pg. 655 (1997)
- [18] V. R. Vathulya, and M. H. White, "Characterization of Inversion and Accumulation Layer Electron Transport in 4H and 6H-SiC MOSFETs on Implanted p-type Regions", IEEE Trans. on Electron Devices, 47, pg. 2018 (2000)
- [19] S. K. Powell, N. Goldsman, C. J. Scozzie, A. Lelis, and J. M. McGarrity, "Self-Consistent Surface Mobility and Interface Charge Modeling in Conjunction with Experiment of 6H-SiC MOSFETs", International Semiconductor Device Research Symposium 2001, pg. 572-574A (2001)
- [20] S. K. Powell, N. Goldsman, J. M. McGarrity, J. Bernstein, C. J. Scozzie, and A. Lelis, "Physics-based numerical modeling and characterization of 6H-silicon-carbide metal-oxide-semiconductor field-effect-transistors", J. Appl. Phy., 92, pg. 4053 (2002)
- [21] V. Tilak, K. Matocha, and G. Dunne, "Electron-Scattering Mechanisms in Heavily Doped Silicon Carbide MOSFET Inversion Layers", IEEE Trans. on Elec. Dev., vol. 54, pg. 2823 (2007)
- [22] A. Lelis, D. Habersat, et al., "Time Dependence of Bias-Stress-Induced SiC MOSFET Threshold-Voltage Instability Measurements", IEEE Trans. on Elec. Dev., vol. 55, pg. 1835 (2008)

- [23] A.J. Lelis, D. Habersat, G. Lopez, J.M. McGarrity, F.B. McLean, and N. Goldsman, "Bias Stress-Induced Threshold-Voltage Instability of SiC MOSFETs," Mat. Sci. Forum Vols. 527-529, pg. 1317 (2006)
- [24] M. Gurfinkel, H. Xiong, et al., "Characterization of Transient Gate Oxide Trapping in SiC MOSFETs using Fast *I-V* Techniques", IEEE Trans. on Elec. Dev., vol. 55, pg. 2004 (2008)
- [25] S. Potbhare, N. Goldsman, G. Pennington, A. Lelis, and J. M. McGarrity, "A Quasi-2D Depth-Dependent Mobility Model Suitable for Device Simulation for Coulombic Scattering due to Interface Trapped Charges", J. of Applied Physics, 100, 044516 (2006)
- [26] S. Potbhare, N. Goldsman, G. Pennington, A. Lelis, and J. M. McGarrity, "Numerical and experimental characterization of 4H-silicon carbide lateral metal oxide semiconductor field-effect transistor", J. of Applied Physics, 100, 044515 (2006)
- [27] S. Potbhare, "Characterization of 4H-SiC MOSFETs Using First Principles Coulomb Scattering Mobility Modeling and Device Simulation", M.S. Thesis, University of Maryland, College Park (<http://hdl.handle.net/1903/3347>) (2005)
- [28] D. L. Scharfetter and H. K. Gummel, "Large-Signal Analysis of a Silicon Read Diode Oscillator", IEEE Trans. on Elec. Dev., vol. ED-16, pg. 64 (1969)
- [29] N. A. Poklonski, S. A. Vyrko, V. I. Yatskevich, and A. A. Kocherzhenko, "A semiclassical approach to Coulomb scattering of conduction electrons on ionized impurities in nondegenerate semiconductors", J. Appl. Phy., 93, pg. 9749 (2003)

- [30] D. Chattopadhyay, and H. J. Queisser, “Electron scattering by ionized impurities in semiconductors”, *Rev. of Modern Physics*, 53, pg. 745 (1981)
- [31] T. Ando, A. B. Fowler, and F. Stern, “Electronic Properties of 2D systems”, *Rev. of Modern Physics*, 54, pg. 437 (1982)
- [32] C. T. Sah, T. H. Ning, and L. L. Tschopp, “The Scattering of Electrons by Surface Oxide Charges and By Lattice Vibrations at the Silicon-Silicon Dioxide Interface”, *Surface Science*, vol. 32, pg. 561 (1972)
- [33] T. H. Ning, and C. T. Sah, “Theory of Scattering of Electrons in a Nondegenerate-Semiconductor-Surface Inversion Layer by Surface-Oxide Charges”, *Physical Review B*, vol. 6, pg. 4605 (1972)
- [34] F. Gámiz, A. López-Villanueva, J. A. Jiménez-Tejada, I. Melchor, and A. Palma, “A comprehensive model for Coulomb scattering in inversion layers”, *J. Appl. Phys.*, vol. 75, pg. 924 (1994)
- [35] F. Rahmoune and D. Bauza, “Si–SiO₂ interface trap capture properties,” *Microelectronics. Eng.*, vol. 59, no. 1, pg. 115–118, 2001.
- [36] C. Lombardi, S. Manzini, A. Saporito, and M. Vanzi, “A Physically Based Mobility Model for Numerical Simulation of Nonplanar Devices”, *IEEE Trans. on Computer-Aided Design*, vol. 7, pg. 1164 (1988)
- [37] D. Caughey, and R. Thomas, “Carrier Mobilities in Silicon Empirically Related to Doping and Field”, *Proceedings of IEEE*, vol. 52 (1967)
- [38] C. J. Scozzie, F. B. McLean, and J. M. McGarrity, “Modeling the temperature response of 4H silicon carbide junction field-effect transistors”, *J. Appl. Phys.*, vol. 81, pg. 7687 (1997)

- [39] G. Pennington, and N. Goldsman, “Self-consistent calculations for n-type hexagonal SiC inversion layers”, J. Appl. Phys., vol. 95, pg. 4223 (2004)
- [40] Hartstein, T. H. Ning, and A. B. Fowler, “Electron Scattering in Silicon Inversion Layers by Oxide and Surface Roughness”, Surface Science, vol. 58, pg. 178 (1976)
- [41] G. Pennington, S. Potbhare, N. Goldsman, J. M. McGarrity, A. Lelis, “Electron Transport at Technologically Significant Stepped 4H-SiC/SiO₂ Interfaces”, SISPAD 2006 (2006)
- [42] T. Kimoto, A. Itoh, and H. Matsunami, “Step bunching mechanism in chemical vapor deposition of 6H and 4H-SiC (0001)”, J. Appl. Phys., vol. 81, pg. 3494 (1997)
- [43] M. Syajarvi, R. Yakimova, and E. Janzen, “Step-bunching in SiC epitaxy: anisotropy and the influence of growth temperature”, J. Crystal Growth, vol. 236, pg. 297 (2002)
- [44] S. Yamakawa, H. Ueno, K. Taniguchi, et. al., “Study of interface roughness dependence of electron mobility in Si inversion layers using Monte Carlo method”, J. Appl. Phys., vol. 79, pg. 911 (1996)
- [45] S. M. Goodnick, D. K. Ferry, et. al., “Surface roughness at the Si (100) – SiO₂ interface”, Phys. Rev. B, vol. 32, pg. 8171 (1985)
- [46] G. Pennington, “Electron transport simulations and band structure calculations of new materials for electronics: Silicon carbide and carbon nanotubes,” Ph.D. dissertation, Univ. Maryland, College Park, MD, (2003)

- [47] C. Jacoboni and L. Reggiani, "The Monte Carlo method for the solution of charge transport in semiconductors with applications to covalent materials," *Rev. Mod. Phys.*, vol. 55, no. 3, pg. 645 (1983)
- [48] K. K. Thornber, "Relation of drift velocity to low-field mobility and high field saturation velocity," *J. Appl. Phys.*, vol. 51, no. 4, pg. 2127 (1980)
- [49] T. Zheleva, A. Lelis, G. Duscher, et al., "Transition layers at the SiO₂/SiC interface", *Applied Phys. Letters*, vol. 93, pg. 022108 (2008)
- [50] I. Khan and J. A. Cooper, Jr., "Measurement of high-field electron transport in silicon carbide," *IEEE Trans. Electron Devices*, vol. 47, no. 2, pp. 269, (2000)
- [51] A. Akturk, G. Pennington, and N. Goldsman, *IEEE Trans. Elec. Dev.*, vol. 52, no. 4, pg.577 (2005)
- [52] M. G. Ancona and G. J. Iafrate, *Phys. Rev. B, Condens. Matter*, vol. 39, no. 13, pg. 9536 (1989)
- [53] F. Stern and W. E. Howard, "Properties of Semiconductor Surface Inversion Layers in the Electric Quantum Limit," *Physical Review*, vol. 163, pg. 816 (1967)
- [54] H Wu, Y. Zhao, and M. H. White, "Quantum mechanical modeling of MOSFET gate leakage for high-k gate dielectrics," *Solid State Electronics*, vol. 50, pg. 1164 (2006)
- [55] T. McNutt, A. Hefner, et al., "Silicon Carbide Power MOSFET Model and Parameter Extraction Sequence", *IEEE Trans. on Power Electronics*, vol. 22, pg. 353 (2007)

- [56] Donald E. Ward and Kyriakos Doganis, "Optimized Extraction of MOS Model Parameters", IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems, Vol. CAD-1, No. 4, (1982)
- [57] S. Kirkpatrick, C. D. Gelatt, Jr. and M. P. Vecchi, "Optimization by Simulated Annealing", Science, Vol. 220, pg. 671 (1983)
- [58] S. Ozder, I. Atilgan, and B. Katircioglu, "Temperature dependence of the capture cross-section determined by DLTS on a MOS structure," Semicond. Sci. Tech., vol. 10, no. 11, pg. 1510 (1995)
- [59] D. Vuillaume, J. C. Bourgoin, and M. Lannoo, "Oxide traps in Si-SiO₂ structures characterized by tunnel emission with deep-level transient spectroscopy," *Phys. Rev. B, Condens. Matter*, vol. 34, no. 2, pg. 1171 (1986)
- [60] H. Lakhdari, D. Vuillaume, and J. C. Bourgoin, "Spatial and energetic distribution of Si-SiO₂ near-interface states," *Phys. Rev. B, Condens. Matter*, vol. 38, no. 18, (1988)
- [61] H. Okushi, Y. Tokumaru, S. Yamasaki, H. Oheda, and K. Tanaka, "Energy dependence of electron-capture cross section of gap states in *n*-type a-Si:H," *Phys. Rev. B, Condens. Matter*, vol. 25, no. 6, pg. 4313 (1982)
- [62] Y. Maneglia and D. Bauza, "Extraction of slow oxide trap concentration profiles in metal-oxide-semiconductor transistors using the charge pumping method," *J. Appl. Phys.*, vol. 79, no. 8, pg. 4187 (1996)
- [63] D. Bauza and Y. Maneglia, "In-depth exploration of Si-SiO₂ interface traps in MOS transistors using the charge pumping technique," IEEE Trans. Electron Devices, vol. 44, no. 12, pg. 2262 (1997)

- [64] W. Liang, N. Goldsman, I. Mayergoyz, P. J. Oldiges, "2-D MOSFET Modeling Including Surface Effects and Impact Ionization by Self-Consistent Solution of the Boltzmann, Poisson, and Hole-Continuity Equations", IEEE Trans. on Electron Devices, vol. 44, pg. 257 (1997)
- [65] W. Shockley and W. T. Read, Jr., "Statistics of the recombination of holes and electrons," Phys. Rev., vol. 87, no. 5, pg. 835 (1952)
- [66] B. J. Baliga, "Power Semiconductor Device Figure of Merit for High-Frequency Applications", IEEE Elec. Dev. Letters, vol. 10, pg. 455 (1989)
- [67] A. O. Konstantinov, Q. Wahab, et al., Appl. Phys. Lett., vol. 71 (1), pg. 90 (1997)
- [68] W. S. Loh, B. Ng, et al., "Impact Ionization Coefficients in 4H-SiC", IEEE Trans. on Elec. Dev., vol. 55, pg 1984
- [69] R. Raghunathan, and B. J. Baliga, "Temperature Dependence of Hole Impact Ionization Coefficients in 4H and 6H-SiC", Solid-State Electronics, vol. 43, pg. 199 (1999)
- [70] A. Akturk, N. Goldsman, et al., "Comparison of 4H-SiC Impact Ionization Models Using Experiments and Self-Consistent Simulations", J. Appl. Phys., vol. 104, 026101 (2008)