

ABSTRACT

Title of dissertation: INTEGRATED CMOS CAPACITANCE
SENSOR AND MICROACTUATOR
CONTROL CIRCUITS FOR
ON-CHIP CELL MONITORING

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“Cell Clinics,” CMOS/MEMS hybrid microsystems for on-chip investigation of biological cells, are currently being engineered for a broad spectrum of applications including olfactory sensing, pathogen detection, cytotoxicity screening and biocompatibility characterization. In support of this effort, this research makes two primary contributions towards designing the cell-based lab-on-a-chip systems.

Firstly it develops CMOS capacitance sensors for characterizing cell-related properties including cell-surface attachment, cell health and growth. Assessing these properties is crucial to all kinds of cell applications. The CMOS sensors measure substrate coupling capacitances of anchorage-dependent cells cultured on-chip in a standard *in vitro* environment. The biophysical phenomenon underlying the capacitive behavior of cells is the counterionic polarization around the insulating cell bodies when exposed to weak, low frequency electric fields. The measured capacitance depends on a variety of factors related to the cell, its growth environment and

the supporting substrate. These include membrane integrity, morphology, adhesion strength and substrate proximity. The demonstrated integrated cell sensing technique is non-invasive, easy-to-use and offers the unique advantage of automated real time cell monitoring without the need for disruptive external forces or biochemical labeling.

On top of the silicon-based cell sensing platform, the cell clinics microsystem comprises MEMS structures forming an array of lidded microvials for confining single cells or small cell groups within controllable microenvironments in close proximity to the sensor sites. The opening and closing of the microvial lids are controlled by actuator hinges employing an electroactive polymer material that can electrochemically actuate. In macro-scale setups such electrochemical actuation reactions are controlled by an electronic instrument called potentiostat. In order to enable system miniaturization and enhance portability of cell clinics, this research makes its second contribution by implementing and demonstrating a CMOS potentiostat module for *in situ* control of the MEMS actuators.

The original contributions of this dissertation include:

- First generation single electrode capacitance sensors based on charge sharing for establishing proof of concept for the on-chip cell sensing approach. Demonstration of novel cell sensing applications including cell adhesion characterization, viability monitoring and proliferation tracking.
- Second generation fully-differential rail-to-rail capacitance sensors with on-chip gain tuning capability for achieving improved performance in terms of

higher sensitivity, capacitance resolution, dynamic range and noise immunity. Shielded current routing bus architectures for incorporating the capacitance measurement circuit in high density sensor arrays and conserving individual sensor performance. Mismatch compensation and sensor output offset cancellation by employing in-circuit floating gate trimming.

- An integrated CMOS potentiostat module custom designed for *in situ* control of the microactuators housed in cell clinics. Demonstration of potentiostat operation for control of off-chip and on-chip electroactive polymer-based microactuators.

INTEGRATED CMOS CAPACITANCE SENSOR AND
MICROACTUATOR CONTROL CIRCUITS FOR
ON-CHIP CELL MONITORING

by

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Dedication

To my parents, grandparents and everyone in my family!

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Chapter 1

Introduction

1.1 Cell clinics overview

Integrated sensor and actuator systems can offer versatile solutions for complex biosensing problems involving the acquisition of responses from individual cells. This lab-on-a-chip approach to cell biology has potential for enabling a wide spectrum of applications, including studies of specific biochemical mechanisms, fast medical diagnosis, pharmaceutical tests, and detection of biochemicals of military or environmental relevance [1–4].

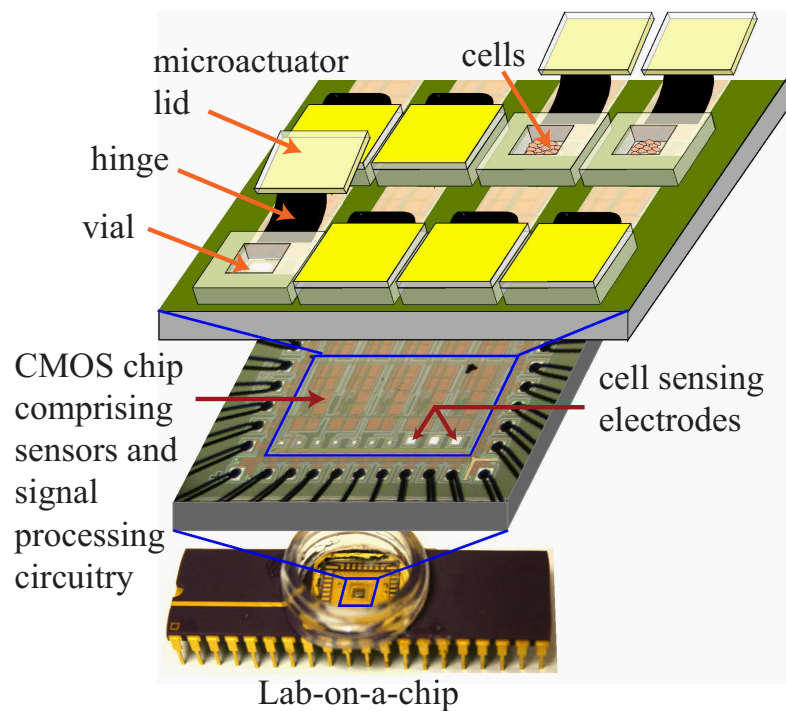


Figure 1.1: Conceptual visualization of the cell clinics microsystem (figure courtesy of Dr. E. Smela, Dr. P. Abshire and M. Urdaneta).

Motivated by its many potential applications, cell clinics, a CMOS/MEMS hybrid microsystem for capturing and performing *in-situ* investigation of living cells, aims at providing an integrated, automated, and high-speed solution for cell monitoring applications. CMOS sensors are being developed for extracellular signal amplification, cell-substrate capacitance sensing, contact imaging, and fluorescence detection. The MEMS platform provides an array of lidded microvials for confining living cells in close proximity to the CMOS sensors and isolating them within controllable microenvironments. Fig. 1.1 provides a conceptual illustration of the microsystem being developed. The biolab SoC (System-on-Chip) comprises electrodes, sensors, microstructures for isolating and containing living cells, and CMOS circuitry for on-chip signal conditioning of sensor responses to cells [5,6].

1.2 Integrated electronic sensing of biological cells

The electrical properties of biological cells and tissues have a strong correlation with their morphological and physiological states [7,8]. For example, the existence of the membrane potential is a feature that can be used to distinguish between living and non-living cells. In special cell types such as neurons and muscle cells, the time-varying electrical potential across the cell membrane reflects changes in the cellular environment and serves as a mechanism for both intra- and inter-cellular communication. Impedance measurements can be used to sense cell morphology and motion [9], to monitor cell adhesion and growth [10], to measure transepithelial and transendothelial electrical resistances of cultured cell monolayers [11], and also

to differentiate between normal and abnormal cell types [12].

Miniaturized electronic biosensing techniques have many advantages to offer in comparison to traditional biochemical detection approaches. Firstly, it is possible for complex measurements to be minimally disruptive in that the responses of living cells can be monitored in real time without altering the biochemical composition of the extracellular environment. This prevents unnecessary modification of the *in vitro* cellular environment which can interfere with the analysis procedure and produce unintended side effects. In addition, microfabrication technologies can readily produce sensing interfaces with physical dimensions matched to the living samples under study, including single cells or even subcellular structures [13]. This enables novel measurement methodologies with capability for exquisite sensitivity and spatial resolution. Electronic biosensing also offers the flexibility of probing living samples over time scales varying over many orders of magnitude and tailored to the specific application. Further, lab-on-a-chip microsystems may provide versatile solutions to complex biosensing problems by automating the sensing and analysis procedures. Such automated, integrated systems offer the potential to reduce infrastructure and cost requirements and, ultimately, to make such sophisticated measurements possible outside the confines of a cell biology laboratory.

1.3 Research contributions

1.3.1 Design and characterization of CMOS-only capacitance sensors for on-chip cell monitoring

The primary contribution of this research involves development of CMOS-only capacitance sensors for on-chip cell sensing applications including characterizing cell adhesion, monitoring cell viability and tracking cell proliferation by sensing the capacitive coupling between sensing electrodes and the cellular matrix. The proposed technique employs electrodes arranged in a planar configuration within the substrate of the growth chamber and insulated from the growth medium using the passivation layer of the chip. The underlying biophysical phenomenon is that, on exposure to low frequency, low strength electric fields, living cells in growth medium behave as insulating structures surrounded by ionic clouds compensating fixed charges present in their membranes [14]. An electric field polarizes the counterionic cloud, giving rise to electric dipoles which are the dominant factor responsible for the low frequency capacitive behavior of cells. Healthy cells with well formed plasma membranes sustain stronger electric dipoles than dead or unhealthy cells with compromised membrane structures, so the measured capacitance is higher for healthy cells [15, 16]. In addition, healthy cells adhere more tightly to a surface in comparison with dead or unhealthy cells, which results in stronger capacitive coupling between the cells and underlying electrodes. Both of these properties can be exploited to monitor the health and growth of cells, and also their interaction with substrates.

The proof of concept for the integrated capacitance sensing approach was established through the design of single electrode sensors that operated based on the charge sharing principle [17–21]. The sensors were tested on-bench and characterized with living cells cultured on the chip surface. The sensors were demonstrated to track the cell adhesion and proliferation processes. Also promising correlations were obtained between the variations in sensed capacitance and changes in cell viability. In addition to delivering encouraging experimental results, the first generation sensors posed a set of problems related to parasitic capacitance effects, interference noise coupling, limited output dynamic range and limited spatial resolution.

In response to the above mentioned problems, a second generation fully differential rail-to-rail capacitance measurement circuit was designed based on the charge based capacitance measurement (CBCM) technique [22,23]. The design extends previously reported CBCM circuits with single-ended output configurations [24–27] to a differential output architecture. The differential sensor achieves improved performance by compensating for parasitic capacitances, by suppressing correlated noise and by providing a higher output dynamic range. Novel array architectures based on a shielded current routing bus were developed for incorporating the differential capacitance measurement circuit in sensor arrays. Apart from improving sensor spatial resolution, the shielded current bus also conserves sensor evaluation speed and provides protection from junction leakage in large sensor arrays. The sensor employs a 3-phase clocking scheme for enabling on-chip gain tuning and also for limiting output voltage offsets. The differential sensor in combination with the shielded current bus exhibits a maximum sensitivity of 200 mV/fF, a maximum achievable resolution

of 15 aF and an output dynamic range of 65 dB. In addition to this, another novel differential sensor circuit incorporating floating gate transistors for output offset cancellation was also designed and fabricated. Output offset cancellation was achieved using a combination of impact ionized channel hot electron injection and Fowler-Nordheim tunneling. Both versions of the differential sensor circuits incorporated in test arrays using the shielded current routing bus were successfully fabricated and tested [28].

1.3.2 Design and demonstration of a CMOS potentiostat for control of integrated MEMS actuators

The microvial lids in the cell clinics microsystem are opened and closed using electrochemically controlled bilayer actuators. The actuators comprise an electroactive polymer layer in combination with a gold contact layer. The polymer layer has the property of changing volume due to electrochemical oxidation and reduction. At the macro-scale, such electrochemical reactions are controlled using an instrument known as a potentiostat. In the first generation of cell clinics the bilayer actuators were controlled using an external potentiostat instrument. In addition to developing the capacitance sensing platform for on-chip cell sensing, another contribution of the current research was to integrate the necessary potentiostat circuitry for control of and integration with the microactuators on top of the CMOS chip. This effort has enabled miniaturization and enhanced portability of the cell clinics system.

The potentiostat module was tailored in accordance with the driving require-

ments of the microactuators [29,30]. The design was optimized in terms of on-chip area requirements for the cell clinics application. A test chip comprising the control circuit connected to on-chip electrodes was designed and fabricated. The electrode set comprised: counter, reference and working electrodes, necessary for the operation of the electrochemical actuators. Tests were performed for validating the control circuit for actuation of off-chip polymer films and lidded microactuators [29]. The operation of the integrated potentiostat was also successfully demonstrated for *in situ* actuation of lidless microactuators fabricated on top of the CMOS chip [30].

Part I

INTEGRATED CAPACITANCE SENSING FOR ON-CHIP CELL MONITORING

Chapter 2

Capacitance Sensing Using CMOS Technology

Capacitance sensing involves (i) exposing an object or system under analysis to electric fields, (ii) performing current, voltage or charge based measurements and (iii) computing the capacitance value of the given object or system from the measured data. The measured capacitance is a parameter that can be employed for a variety of applications involving detection of material properties, sensing location, proximity and motion of either conductive, dielectric or semi-insulating objects.

The design and development of cell clinics, a cell-based lab-on-a-chip technology, poses several requirements concerning manipulation of cells and sensing of different aspects of cell morphology, growth and physiology. From an electrical perspective the cellular environment is a complex heterogeneous system comprising ionic conductors and organic dielectrics. In addition to this the system also exhibits temporal changes due to cell activity (e.g., adhesion, proliferation, movement). Understanding the behavior of such complex systems requires extensive characterization through various biochemical and biophysical techniques. In this direction, capacitance sensing can serve as a useful technique for integrated sensing, characterization and monitoring of biological systems at the cellular level.

Capacitance sensors have several inherent features that favor their utility in cell sensing. They can be tailored to perform non-contact sensing. This can be

an extremely critical requirement while sensing biological samples. These sensors generally operate at low power. Capacitance sensing being highly amenable to integration enables array-based sensing. They also provide better temperature stability in comparison with piezoresistive and piezoelectric sensors, easier A/D conversion, better reliability and lower cost when batch fabricated. Capacitance sensing offers additional advantages in comparison to other cell sensing modalities such as optical detection [31], fluorescence sensing [32] and frequency based measurements [33]. These include reduced system complexity, elimination of off-chip optics, no post-fabrication requirements, and prevention of electrochemical side-effects which are prominent in electrode based sensors with sensing surfaces exposed directly to the cell medium.

One of the first efforts towards sensing microscopic cell capacitances employed microfluidic flow cytometry, with measurements performed using an external capacitance bridge [34]. Capacitance changes in the fF range were evoked by passing individual cells through a 1 kHz electric field across a pair of microelectrodes. Another lab-on-a-chip system employed capacitance sensing in combination with dielectrophoretic actuation for short-term cell detection and manipulation, with the cells suspended in a microchamber and the capacitances measured in between the on-chip microelectrodes and an external conductive glass lid [35]. Detection and manipulation were performed in a modified in vitro environment using mannitol instead of growth medium. An aqueous solution of 280 mM mannitol provided the low conductivity conditions required for detection and manipulation, and preserved the osmotic pressure required for the cells to survive. This work, in contrast,

employs integrated capacitance sensors for long-term monitoring of anchorage dependent cells in a standard in vitro environment using normal cell growth medium. Since many living cells need to be attached to a solid surface before they can grow and proliferate, this approach can be applied for monitoring a wide spectrum of cell types. Through this research, we have demonstrated the utility of this technique for characterizing adhesion, monitoring viability and tracking proliferation of living cells cultured on the sensor chips [17–21]. This approach in contrast to previous efforts does not require specialized 3D arrangement of electrodes and is well suited to monitoring cells in a standard cell culture environment by employing on-chip passivated coplanar microelectrodes.

2.1 Sensor basics

The capacitance as seen by the sensor arises from the combination of a drive electrode, a sense electrode and the material under test (MUT). The electric field lines travel across the drive and sense electrodes, passing through the MUT. The measured capacitance is determined by the geometrical configuration of the drive and sense electrodes, and the dielectric properties and spatial orientation of the MUT. A CMOS-only sensor, constrained by the planar nature of its fabrication process, is restricted to coplanar electrode configurations. Coplanar electrodes offer the additional advantage of one-sided access for biological sensing applications, leaving the other side open to the isolated and sterile biological environment. The electric field resulting from the excitation of coplanar electrodes is entirely fringing

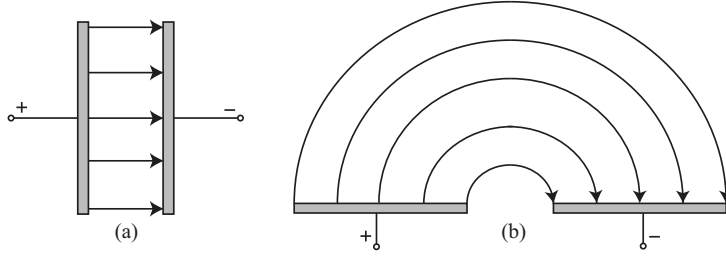


Figure 2.1: (a) Parallel plate capacitor (b) coplanar plate capacitor creating fringing electric field.

in contrast to a direct normal field inside an ideal parallel plate capacitor. Fig. 2.1 illustrates this distinguishing feature. The penetration depth of the fringing electric field above the coplanar electrodes is proportional to the spacing between the centerlines of the sense and drive electrodes. This is an important aspect to consider while designing sensors for biological samples (e.g., tissues, cells, microbes, proteins, DNA) whose dimensions scale across several orders of magnitude. Typical cellular dimensions being at the micron scale, are easily sensed by microelectronic sensors comprising integrated microelectrodes.

Fig. 2.2 illustrates the equivalent circuit of the most basic capacitance sensor configuration [36]. The figure shows a parallel guard plane underlying the sense and drive electrodes. The drive electrode is connected to the excitation source. The sense electrode is connected to the measurement and signal processing circuitry. The interelectrode conductances G_{10} , G_{20} and G_{12} , the interelectrode capacitances C_{10} , C_{20} and C_{12} , and the input capacitance of the measurement circuit C_L , comprise the impedance network excited by the source V_S . The guard plane driven by a potential $V_G = V_L$, serves to nullify the impedance formed by G_{20} and C_{20} . This eliminates their effect on the circuit response and enhances sensitivity.

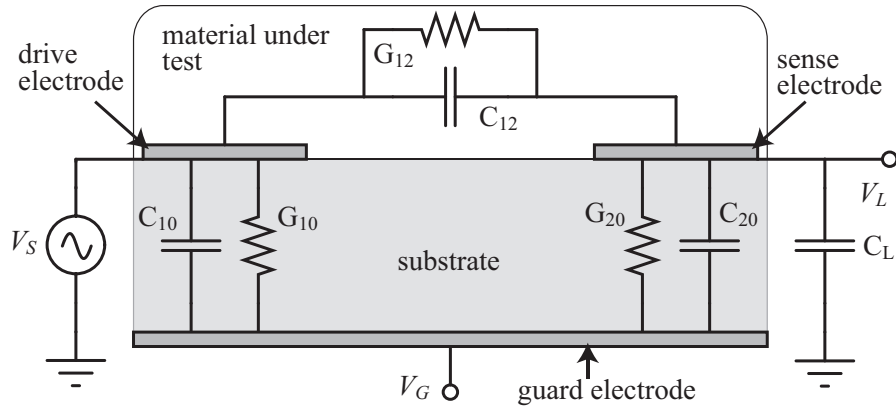


Figure 2.2: Generic capacitance sensor configuration.

2.2 A review on CMOS capacitance sensors

Integrated CMOS capacitance sensors have been previously employed for a variety of applications including fingerprint sensing [37], position sensing [38], interconnect characterization [39], humidity sensing [40], and particle detection [27]. The goal of this research is to demonstrate the application of this technology for on-chip cell sensing applications including adhesion characterization, viability monitoring and proliferation tracking. Capacitance sensing techniques using CMOS technology can be broadly classified under four categories: (i) amplitude based, (ii) frequency based, (iii) time based and (iv) charge based measurements. These techniques are discussed in the following sections. Table 2.1 gives a brief overview of each of these approaches.

Table 2.1: Integrated capacitance sensing approaches using CMOS circuits

Approach:	Amplitude based	Frequency based	Time based	Charge based
Transduction type:	capacitance to ac amplitude	capacitance to frequency	capacitance to pulse duration	capacitance to charge storage or motion
Measurement circuit:	synchronous demodulators	oscillators	integrators	switched capacitors
Advantages:	<ul style="list-style-type: none"> • precision • flexibility • noise immunity 	<ul style="list-style-type: none"> • precision • linearity • noise immunity 	<ul style="list-style-type: none"> • precision • linearity 	<ul style="list-style-type: none"> • small on-chip area (suitable for array-based applications) • low power
Disadvantages:	<ul style="list-style-type: none"> • high on-chip or on-board area 	<ul style="list-style-type: none"> • high on-chip area 	<ul style="list-style-type: none"> • high on-chip area 	<ul style="list-style-type: none"> • sensitivity to stray capacitances • low noise immunity
Applications:	position sensing, proximity detection, accelerometry, pressure sensing, humidity sensing, process control			
	fingerprint sensing, particle detection, interconnect characterization			

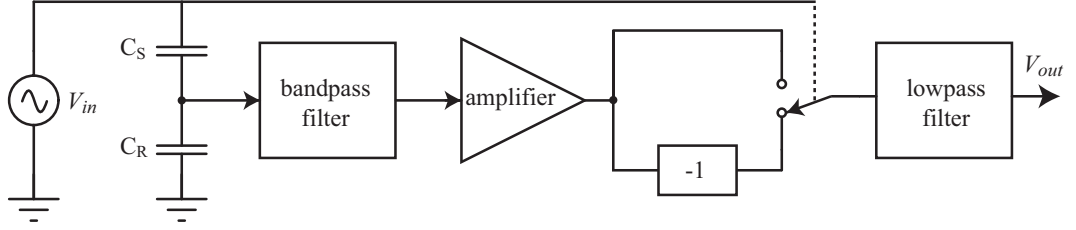


Figure 2.3: Capacitance measurement using synchronous demodulation.

2.2.1 Amplitude based capacitance measurement

The amplitude based measurement approach involves excitation of a capacitive network comprising a reference capacitor C_R and the sensed capacitance C_S by a high frequency excitation signal (10kHz - 1MHz) followed by amplification and synchronous demodulation of the capacitively modulated signal [41]. Fig. 2.3 shows a block diagram of a full-wave demodulation scheme, with both positive and negative half-cycles of signal contributing to the output. The bandpass filter is added to limit the noise bandwidth. Commercially available high-quality amplifiers and filters can be used for on-board implementation of the synchronous demodulator required to implement precise and low-noise capacitance measurements.

2.2.2 Frequency based capacitance measurement

The frequency based approach involves translation of sensed capacitance values to frequencies or digital pulses using oscillator circuits. In the oscillator based capacitance sensors, the sensed capacitor replaces the tuning element in the oscillator. Sensors comprising discrete components can employ RC or LC oscillators, where for an RC oscillator, the frequency is proportional to $1/RC$ and for an LC oscillator frequency is proportional to $1/\sqrt{LC}$. Integrated oscillator circuits imple-

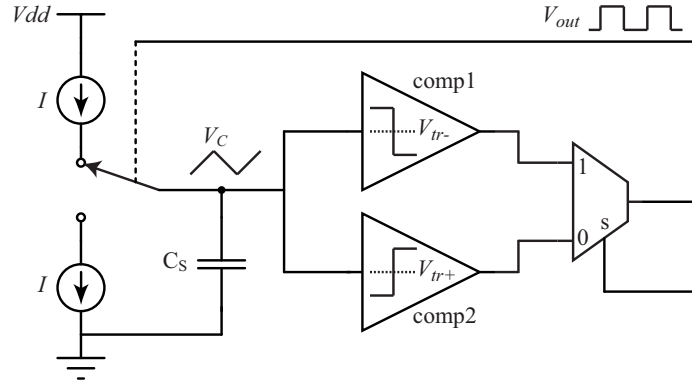


Figure 2.4: Capacitance measurement using oscillator circuit.

mented in CMOS involve charging and discharging of the sensed capacitor using transistors acting as controlled current sources.

For example, Ferri et al. designed an oscillator as a capacitive sensor interface mapping a capacitance range of 10 fF - 100 pF to a frequency span of 300 Hz - 3 MHz [42]. Fig. 2.4 shows the block diagram of the designed oscillator. The circuit comprises a hysteresis comparator and a current starved inverter in a loop. The sensed capacitor C_S is charged and discharged with constant currents I from the current starved inverter. The hysteresis comparator comprises two traditional comparators with different threshold voltages V_{tr+} and V_{tr-} . The comparator converts the triangular voltage across C_S into a square wave of output frequency:

$$f_{osc} = \frac{I}{2(V_{tr+} - V_{tr-})} \times \frac{1}{C_S} \quad (2.1)$$

The chip area was reported to be 0.2 mm². Frequency measurement or pulse counting would require additional on-chip or off-chip circuitry.

The frequency based technique offers a wide range of measurable capacitances.

Since the oscillators can be designed to produce digital outputs, the sensors can operate under noisy conditions.

2.2.3 Time based capacitance measurement

This approach employs a linear relationship to map the sensed capacitance to the pulse width of the output signal. Based on this technique, Bruschi et al. designed a capacitance-to-pulse width converter that generates a pulse width modulated (PWM) signal in accordance to the sensed capacitance [43]. Fig. 2.5 shows a schematic of the implemented system along with the relevant waveforms.

The sensed capacitance is represented by the capacitance C_S along with the parasitic capacitances C_{P1} and C_{P2} . The measurement circuit comprises three integrators INT1-3. The transconductance amplifier OTA2 has 2 identical, in-phase, current output ports. CMP is a comparator. C_R and C_I are reference capacitors. Currents I_{RMP} , I_{SH} and I_{DIS} are obtained from precision current mirrors and are scaled according to:

$$I_{SH} = k_1 I_{RMP}, \quad I_{DIS} = k_2 I_{RMP} \quad (2.2)$$

k_1 and k_2 being scaling constants.

When clock (CLK with period T_{CLK}) is low, I_{RMP} is integrated by INT1 resulting in a final output voltage of V_f ,

$$V_f = \frac{T_{CLK} I_{RMP}}{2 C_R} \quad (2.3)$$

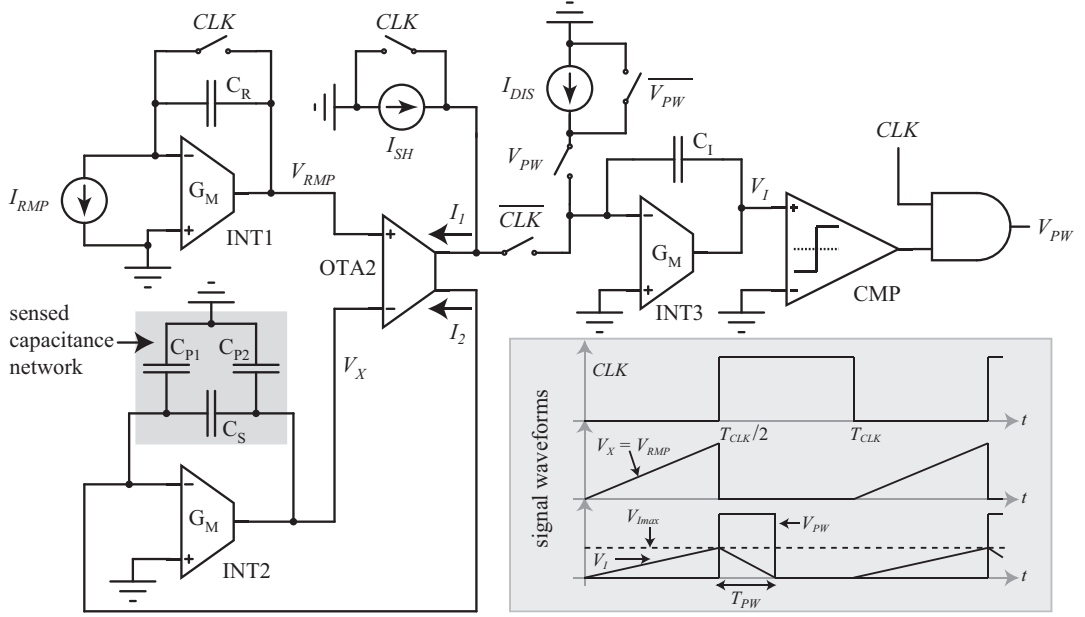


Figure 2.5: Capacitance measurement using pulse width modulation.

INT2 forms a negative feedback loop around OTA2. Since V_{RMP} and V_X track each other from 0 to V_f ,

$$\int_0^{T_{CLK}/2} I_2 dt = C_S V_f = \frac{T_{CLK} I_{RMP}}{2} \left(\frac{C_S}{C_R} \right) \quad (2.4)$$

Concurrently, the current $I_1 - I_{SH}$ is integrated by INT3. Assuming $I_1 = I_2$, the charge stored on C_I , at the end of CLK low can be computed as

$$Q_I = \frac{T_{CLK} I_{RMP}}{2} \left(\frac{C_S - k_1 C_R}{C_R} \right) \quad (2.5)$$

CMP output is high during the entire CLK low phase.

When CLK goes high, $I_1 - I_{SH}$ is disconnected from INT3, and C_I is discharged by I_{DIS} . When $V_I = 0$ after discharging, CMP output goes low and the discharge stops. From the above discussion, the PWM signal duration T_{PW} can be evaluated

as:

$$T_{PW} = \frac{Q_I}{I_{DIS}} = \frac{T_{CLK}}{2k_2} \left(\frac{C_S}{C_R} - k_1 \right) \quad (2.6)$$

T_{PW} is proportional to C_S . The ratio T_{PW}/T_{CLK} depends on the current ratio k_1/k_2 and the capacitance ratio C_S/C_R . The measurement circuit exhibits low sensitivity to temperature and process variations because these variations are largely canceled by the computation of the ratio.

2.2.4 Charge based capacitance measurement

The approaches described above for capacitance measurement offer several advantages including high precision, good linearity, noise immunity, wide signal range and low temperature sensitivity. However, the measurement circuitry employs several signal processing or conditioning modules which increases their on-chip area. Since the sensor for the current application needs to be tailored for on-chip cell sensing, employing any of the above approaches would lead to very few sensing sites. In contrast to the above approaches, charge based techniques have proven to result in sensors having minimal on-chip footprints and resolution in the aF range. These factors have favored the adoption of the charge based capacitance measurement approach for the cell sensing application demonstrated here. Recently, charge based capacitance measuring circuits have been employed for several applications including fingerprint sensing, interconnect characterization of fabricated chips and particle detection. This section briefly reviews related architectures reported in the literature.

2.2.4.1 Fingerprint sensing

Charged based capacitance sensor arrays have been used to sample fingerprint patterns by detecting the electric field variation induced by the skin surface. The sensing electrodes are covered by a dielectric material on top of which a finger is placed. The presence of a finger above the sensing electrode produces a capacitor. The ridge and valley patterns on the fingers translate to the capacitive patterns sensed across the array.

Tartagni et al. designed a fingerprint sensor based on a feedback capacitive sensing scheme [44]. Fig. 2.6(a) illustrates the sensing technique. Each sensor cell comprises two coplanar plates interacting with the overlying finger surface. This is shown in the figure as the feedback capacitance C_f connected across the amplifier input and output terminals. C_f is formed by the two coplanar electrodes facing a third electrode modeling the finger surface. If the input capacitive node is discharged by a δQ amount of charge, the output voltage ΔV_o can be derived as:

$$\Delta V_o = \frac{\delta Q}{\frac{C_i}{A_o} + \left(1 + \frac{1}{A_o}\right) C_f} \quad (2.7)$$

where A_o is the gain of the charge amplifier OP. C_f can be approximated as:

$$C_f \approx \frac{\epsilon_0 S}{2d} \quad (2.8)$$

where S is the plate overlap area and d is the distance between the coplanar electrodes and the third electrode. If $A_o \gg 1$, the output voltage signal ΔV_o can be

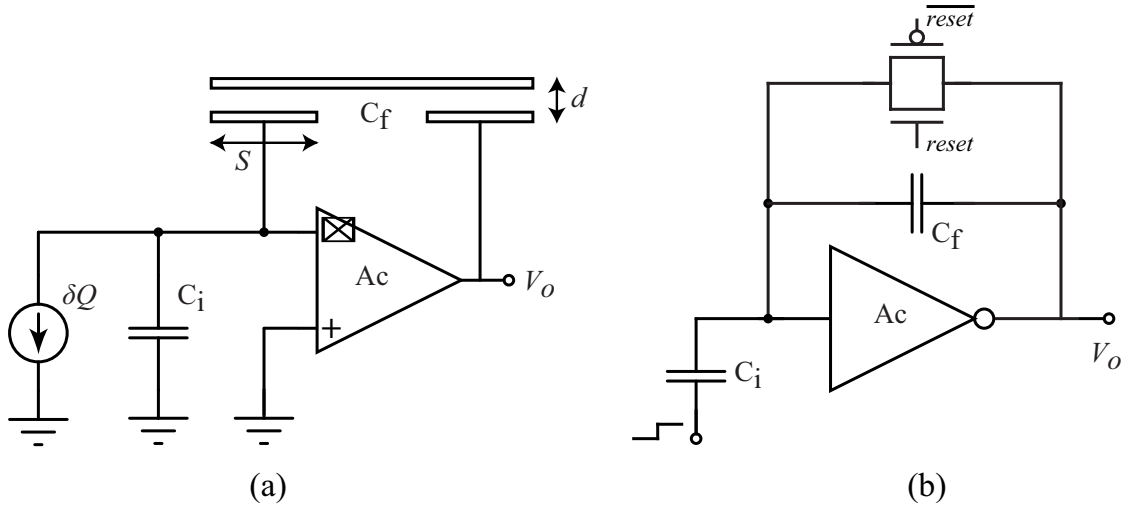


Figure 2.6: (a)Feedback capacitive sensing scheme. (b)Implemented sensor circuit.

approximated as:

$$\Delta V_o \approx \frac{\delta Q}{C_f} = \frac{2\delta Q}{\epsilon_0 S} d \quad (2.9)$$

The charge amplifier Ac is implemented as a high gain inverter as shown in 2.6(b). The sensing operation proceeds in two phases. During the reset phase, the charge amplifier is reset by shorting the input and output using the reset switch, so that the input and output are set to V_T , the logical threshold of the inverter. During the evaluation phase, a voltage step is applied across an input capacitance C_i , resulting in an output voltage signal proportional to the feedback capacitance as shown in Eqn. 2.9 [44].

2.2.4.2 Interconnect capacitance characterization

Interconnect capacitance characterization in conjunction with simulations during design phases can provide circuit designers an accurate assessment of speed and noise issues arising due to interconnect capacitances. Sylvester et al. developed a

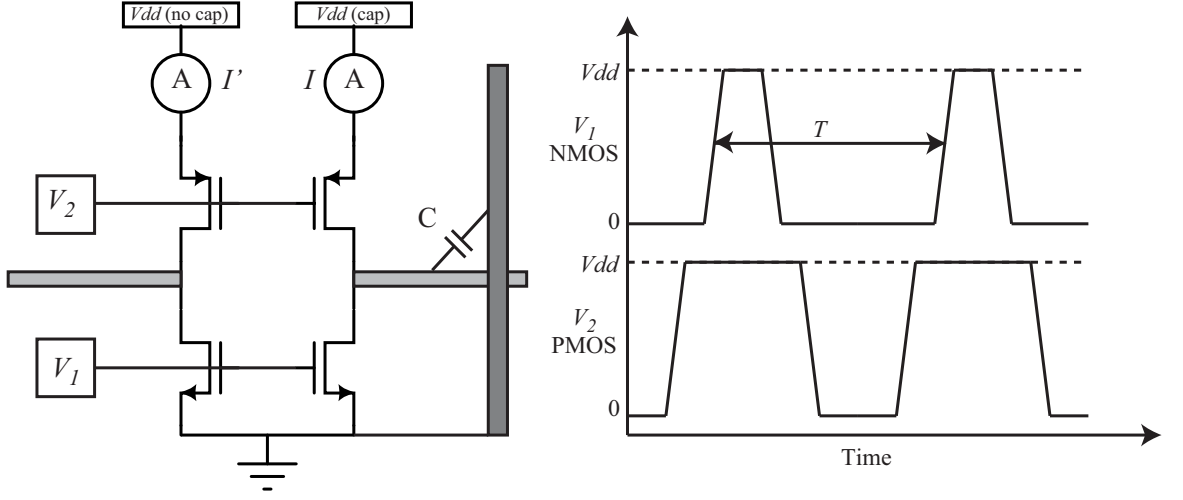


Figure 2.7: Left, capacitance measurement test structure. Right, nonoverlapping switching waveforms.

charge based capacitance measurement (CBCM) technique for interconnect characterization [39, 45]. Fig. 2.7 shows a schematic of the test structure used.

It comprises complimentary pairs of NMOS and PMOS transistors. The structure on the left is identical to the one on the right except for the test capacitance to be measured. Both structures are driven by two nonoverlapping signals V_1 and V_2 . Turning on the PMOS transistor charges the interconnect capacitance which is subsequently discharged by the NMOS transistor. Ammeters are used to measure the average values of the charge/discharge currents. The difference between the two average currents I and I' is used to extract the value of the interconnect capacitance to be measured.

$$I' - I = I_{net} \quad (2.10)$$

$$I_{net} = C \cdot V_{dd} \cdot f \quad (2.11)$$

For the purpose of extracting capacitance values, I_{net} is plotted as a function of V_{dd} for specific frequencies. C is extracted by dividing the slope of the fitted line by the corresponding frequency. The resolution of this technique is limited by the mismatch in the drain junction and the overlap capacitances of the left and right transistor pairs.

2.2.4.3 Particle detection

Microelectronic capacitance transducers can be used in miniaturized electrical tomography systems for industrial applications. In this direction Evans et al. designed a CMOS capacitance sensor for detecting dispersed particles in an oil medium [27]. They extended the previously developed CBCM technique by incorporating a measurement circuit along with the CBCM sensing front-end, instead of using external current measurement instrumentation. The sensor circuit is shown in Fig. 2.8. As in CBCM, the sensed capacitance, the stray capacitances (parasitic capacitances arising from the measurement circuitry) at the sensing node and the standing capacitance (capacitance offered by the sensing electrodes themselves) of the sensing electrodes are charged through Q_1 when Clk_1 is low and discharged through Q_2 when Clk_2 is high. Clk_1 and Clk_2 are nonoverlapping clocks. A current mirror comprising Q_3 and Q_4 mirrors, amplifies and integrates the charging current over a capacitor C_{int} . Q_6 and Q_7 buffer the resulting voltage. Q_5 resets the sensing node after every measurement cycle. The relation between the sensing node voltage

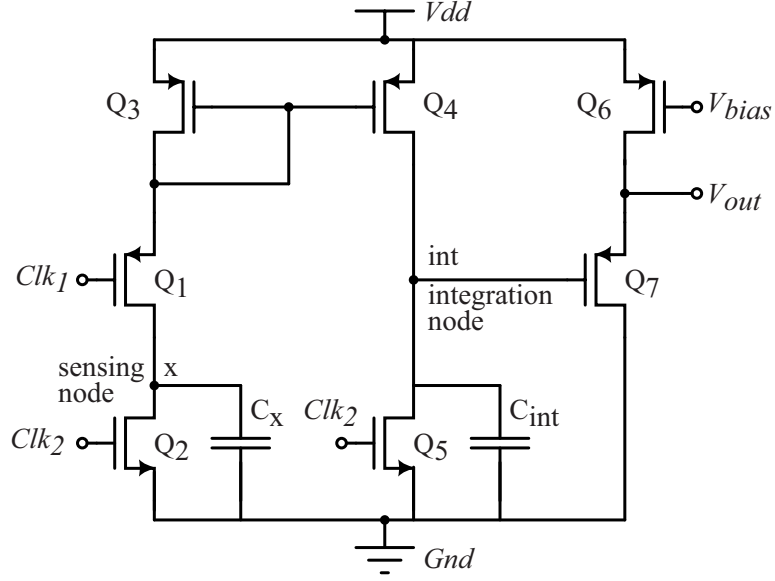


Figure 2.8: CBCM circuit for particle detection.

V_x and the output voltage V_{int} can be derived as:

$$\frac{V_{int}}{V_x} = \frac{C_x \int I_4 dt}{C_{int} \int I_3 dt} = \frac{C_x(W_4/L_4)}{C_{int}(W_3/L_3)} \quad (2.12)$$

C_x represents the sum of the sensed, stray and standing capacitances at the sensing node. The voltage at the sensing node rises to within one threshold voltage of the power supply, after which Q_3 is cut-off and the sensor output voltage evaluates to:

$$V_{int} = \frac{C_x(W_4/L_4)}{C_{int}(W_3/L_3)}(V_{dd} - |V_{tp}|) \quad (2.13)$$

V_{dd} is the supply voltage and V_{tp} is the threshold voltage of the PMOS transistor. The equation exhibits a linear relation between the sensor output voltage and the sensed capacitance. Circuit simulation predicted a sensitivity of 42 mV/fF, with a mirror gain of 10 and an integrating capacitor of 1.2 pF.

Chapter 3

Cell Adhesion, Viability, Proliferation, Techniques & Biophysics

Interaction with a substrate plays a crucial role in the lifecycle of a majority of cell types. This is because most cells are anchorage-dependent, that is, they need to be attached to a solid surface before they can grow and proliferate [46, 47]. The mechanisms by which living cells adhere to substrates and their subsequent viability and proliferation have been extensively studied in cell biology [46, 47]. In addition to its physiological significance, understanding cell adhesion and growth has many practical applications in the fields of medicine, bioengineering and environmental sciences. For example, the formation of biofilms (complex aggregations of microorganisms on solid surfaces) is important in a variety of applications in food and water quality assessment and treatment [48]. Studying and enhancing cell adhesion to body implants is extremely important for improving biocompatibility, reliability, lubrication and self-regeneration of the adjacent tissues [49].

3.1 Characterizing cell adhesion

Living cells exhibit a variety of modes of attachment to substrates [50]. Cell adhesion is a complex process that results from interplay between many molecular and macro-molecular forces including receptor mediated forces, membrane elasticity

and different kinds of interfacial forces including electrostatic, undulation, van der Waals interaction and hydration forces [46]. The diversity of mechanisms underlying cell adhesion ultimately enables cells to adapt to different kinds of surfaces and living conditions. The factors influencing the interactions between cells and their substrates can be characterized by quantifying cell adhesion.

In this direction, previous efforts employed techniques like centrifugation and shear flow measurements [51], wherein cells cultured on a substrate are subjected to centrifugal and flow forces respectively. The adhesion strength is related to the fraction of cells that become detached from the surface during mechanical manipulation. Such macroscopic measurements on entire cell populations provides limited information regarding individual cell behavior and the statistical variations among cells, and are inherently disruptive of the cell-substrate coupling. Bowen et al. used atomic force microscopy to measure the adhesive force of a yeast cell by immobilizing it at the end of a cantilevered beam and making force-distance measurements for cell retraction from the surface [52]. Barbee et al. developed a thickness shear mode piezoelectric sensor for continuous measurement of interfacial processes between endothelial cells and gold electrodes [53]. Fan et al. studied the adhesion and viability of central neural cells on silicon wafers with different surface roughness conditions using scanning electron microscopy [54].

3.2 Assessing cell viability

Quantification of cell viability has become an essential requirement for cell based studies. Viability sensors may be useful for optimization of cell culture conditions and also for a variety of commercial applications such as drug screening and biocompatibility characterization of implants.

Cell viability can be measured either directly by counting the number of healthy cells in a sample or indirectly by measuring an indicator of cell health and proliferation. Most existing methods for estimation of cell viability can be classified into two categories. The first class is based on quantifying the metabolic activity of cells [55, 56]. This is accomplished by incubating cells along with an indicator dye or a tetrazolium salt that is reduced to a colored compound only by metabolically active cells. Color development is a function of the number of metabolically active cells, and gives a measure of cell viability. Quantification is normally accomplished using spectrophotometry. The other class of cell viability methods probe the cell membrane integrity using dye-exclusion techniques [56]. This approach takes advantage of the fact that healthy cells with well formed plasma membranes exclude dyes such as trypan blue, whereas dead and unhealthy cells with compromised membranes allow dyes to stain internal cellular components. Microscopic analysis is required in order to count only healthy cells and reject unhealthy cells in the sample.

3.3 Assessing cell proliferation

Quantifying cell growth is essential for many applications in cell biology and biotechnology. It is required for optimizing cell culture conditions, for studying substances that inhibit or promote cell growth, for studying cancer progression, for drug screening, for cytotoxicity testing of anticancer agents, and also for engineering biocompatible implants [57–59].

Assessment techniques for cell proliferation measure the number of actively dividing cells in a sample. A majority of existing proliferation assays measure DNA synthesis as a direct indicator of cell growth [60]. Assessment involves addition of a labeled DNA precursor to the cell culture medium, followed by sample incubation and then quantification of the labeled DNA precursor which has been incorporated into genomic DNA during replication by means of spectrophotometry. Other indirect techniques for proliferation assessment involve measuring the activity of molecules that regulate the cell division cycle [61]. Most traditional proliferation assays are label-based endpoint assays that require sample preparation and sophisticated lab equipment. Time-lapse microscopy is an example of a well-established, alternative, label-free technique that is currently being employed for automating cell proliferation studies. This involves microscope translation, auto-focusing, optical filtering, image acquisition and sophisticated image processing [62]. This can serve as a very useful technique for validating the operation of the integrated sensors that are currently under development for on-chip monitoring of different kinds of cell phenomena.

3.4 Previous efforts towards characterizing cell-related properties using electronic sensing techniques

3.4.1 Electric cell-substrate impedance sensing (ECIS)

The most well established form of “whole cell” biosensing using electrical means has been impedance-based measurements. The technique of electric cell-substrate impedance sensing was first introduced by Keese and Giaver [9, 63]. It involves small signal impedance measurement of gold detecting electrodes immersed in the cell culture medium. When the cells attach and spread on the detecting electrode, the measured electrical impedance changes. This is due to the insulating nature of the cell membrane and the formation of adhesion contacts to the electrode, both of which impedes current flow. Changing impedance reveals information regarding cell morphology and behavior which in turn depends upon coordination of many biochemical reactions sensitive to parameters such as pH, temperature and chemical compounds.

Fig. 3.1 illustrates the measurement setup. The gold detecting electrodes have a diameter of $250\ \mu\text{m}$. The current returns through a larger area counter electrode (area $\approx 100\ \text{mm}^2$). A 1 V sinusoid of a particular frequency is applied to the sample through a $1\ \text{M}\Omega$ resistance. Since the electrode resistance is a few $\text{k}\Omega$ s, the current flow is approximately constant. An external lock-in amplifier is used to measure the magnitude and phase of the voltage across the sample. The in-phase voltage is proportional to the series resistance and the out-of-phase voltage is proportional

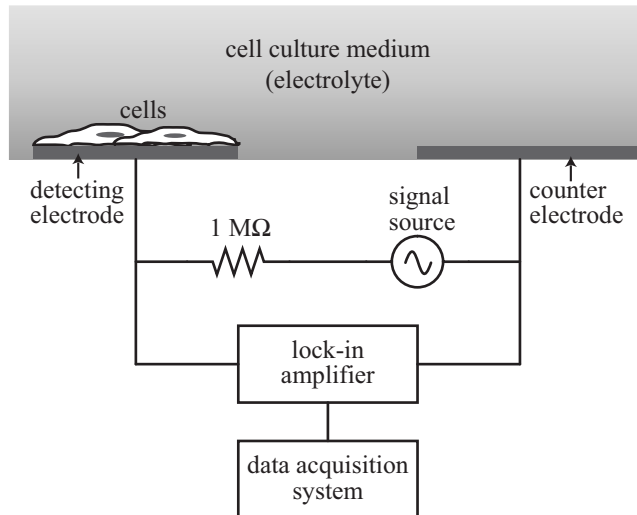


Figure 3.1: A schematic of the ECIS system.

to the series reactance of the sample. The measured impedance is formed by the electrode/electrolyte interface [64] and the cell layer over the electrode. The resistive component of the cell layer results from the ionic current under and between the cells. The reactive component results from the capacitive current flow across the cell membranes.

Giaver and Keese used impedance sensing to monitor cell proliferation, morphology, and motility [9,63]. Since then there have been several reports of impedance measurements addressing a variety of cell sensing applications. Ehret et al. monitored impedance changes of cells cultured on interdigitated electrodes during cell adhesion and growth [10]. Lin et al. used this technique to differentiate between normal and abnormal cell types [12]. Xiao et al. used ECIS for on-line assessment of cell cytotoxicity [65].

3.4.2 Microfluidic capacitance cytometry

A recent effort towards measuring microscopic cellular capacitances employs flow cytometry in a microfluidic channel. Sohn et al. detected capacitance changes evoked by the passage of individual cells across a 1 kHz electric field in a microfluidic channel [34]. The capacitive change has been attributed to the polarization response of a cell as it passes through an electric field region. The authors also found an interesting linear relation between the DNA content of eukaryotic cells and the change in capacitance. Fig. 3.2 shows a schematic of the microfluidic system. It comprises a pair of gold microelectrodes ($50\ \mu\text{m}$ wide) on a glass substrate separated by a distance of $30\ \mu\text{m}$. The microfluidic channel was made of polydimethyl siloxane (PDMS) and measured $30\ \mu\text{m}$ in height. Capacitance measurements were performed using a commercial capacitance bridge. Distinct capacitive peaks in the range of $3\ \text{fF} - 12\ \text{fF}$ were detected corresponding to flow of cells past the electrodes.

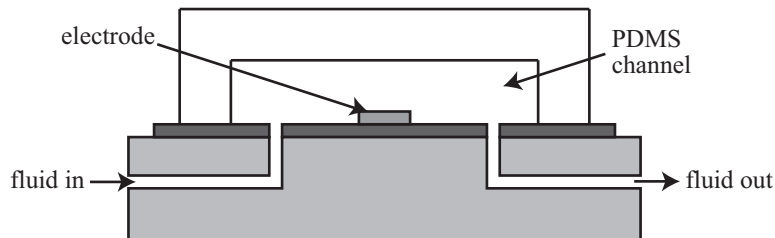


Figure 3.2: Schematic of the microfluidic device for capacitance cytometry.

3.5 Our approach using integrated capacitance sensing

All the traditional approaches mentioned in section 3.1 for characterizing cell adhesion and section 3.2 for monitoring cell viability employ specialized techniques

and processes. In addition, most of them require sophisticated laboratory equipment. Almost all of the cell viability assessment techniques involve an inherent process of sampling which may not be feasible for samples with extremely small volumes.

With reference to nontraditional electronic sensing techniques discussed in section 3.4, although ECIS employs integrated electrodes for cell sensing, it still requires external measurement instruments such as lock-in amplifiers and LCR-meters. The measurements are also subject to electrochemical side-effects, since the electrodes are directly exposed to the culture medium, an aqueous ionic solution. The electrodes require custom fabrication for biocompatibility and electrochemical corrosion resistance purposes. The integrated microfluidic capacitance cytometry approach, although impressive in terms of its sensitivity, still uses an external capacitance bridge for making measurements.

In contrast to the previous efforts, CMOS sensors can integrate passivated electrodes with the capacitance measurement circuitry on the same substrate overcoming the above mentioned limitations and also eliminating the need for external instruments. This work has developed integrated capacitance sensors that can be designed and fabricated using conventional CMOS technology, for inexpensive, portable and reproducible characterization of cell adhesion and viability properties, without the need for extensive laboratory infrastructure. The integrated cell sensing approach presented here offers the unique advantage of long term continuous cell monitoring in a standard culture environment without any modification, and without the need for disruptive external forces or biochemical agents employed in

the traditional techniques.

3.6 Biophysics of cell-substrate capacitance

In the presence of low frequency, low strength electric field excitations, living cells behave as insulating structures embedded in an electrically conductive growth medium which is an aqueous ionic solution [14]. Cell surfaces generally carry a surface charge density, which can be positive or negative depending upon the cell type [14]. The majority of cell surfaces are negatively charged. This induces a counterionic cloud around the cells in the surrounding medium. When exposed to an external electric field these counterions are displaced tangentially around the cell surface giving rise to an induced dipole moment as illustrated in Fig. 3.3. Both the insulating nature of cells at low excitation frequencies and the counterionic polarization are responsible for the low frequency capacitive behavior of cells [14]. At low excitation frequencies, the plasma membrane shields out the cell interior, and therefore all charges and dipoles present inside the cell have no influence on the dielectric properties of cells [14].

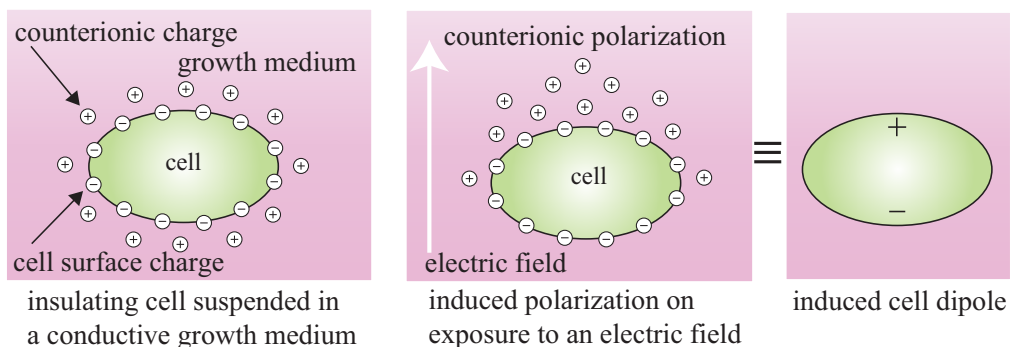


Figure 3.3: Cellular counterionic polarization in the presence of external electric fields.

3.6.1 Correlating capacitance with cell-substrate interaction

Next we examine the behavior of a cell suspension when it comes into contact with a solid biocompatible substrate. Upon contact with a solid substrate, proteins in the growth medium spontaneously adsorb onto the substrate. The interaction between cells and substrate begins with the sedimentation phase when the suspended cells gradually drift downwards and settle on the surface. This is followed by the adhesion phase when cells anchor themselves to the surface through various mechanisms at both molecular and cellular levels [46]. This is accompanied by a significant change in cell morphology wherein the cells exhibit a spreading behavior. Under favorable conditions there is a proliferation phase during which cells divide and proliferate. In the presence of weak, low frequency electric fields all three phases can be modeled as a process of cell dielectric layer formation as shown in Fig. 3.4.

The capacitance arising from this dielectric layer successively increases in the phases described above. The capacitance between cells and substrate is lowest in the sedimentation phase since the cells are far from the surface and the cellular dielectric layer is not yet completely formed. The conductive growth medium screens out the suspended cells from the electric fields. Once the cells completely settle on the substrate and start attaching to the surface, they undergo polarization on account of being exposed to the electric fields. This gives rise to the cell-substrate capacitance. During the adhesion phase there is a remarkable decrease in the dielectric layer thickness due to cell spreading and anchoring mechanisms. In addition, the effective dielectric constant of the cell layer increases due to increasing cell membrane surface

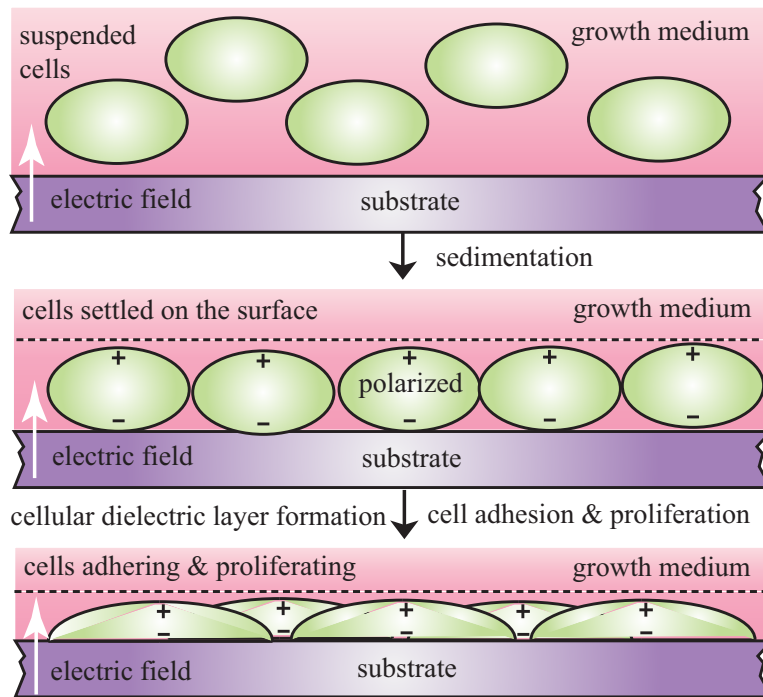


Figure 3.4: Cell dielectric layer formation in the presence of weak, low-frequency electric fields: sedimentation phase (top), initiation of adhesion (middle), adhesion and proliferation phases (bottom).

area and increasing cell dipole density. Both factors contribute to a steady increase in the cell dielectric layer capacitance. Once the cells have adhered to the surface and adjusted to the culture conditions, the proliferation phase begins and the measured capacitance reflects ongoing cellular activity. In cases of adverse conditions, the growth phases described above may be superseded by a cell death phase during which the plasma membranes begin to disintegrate, causing a reduction in capacitance of the cell dielectric layer.

The above discussion regarding correlating the sensed capacitance with the cell-substrate interaction process provides an explanation for the observations made during the experiments that were performed with actual biological cells cultured on fabricated capacitance sensor chips. Several experiments involving three different

cell types have been performed with the sensor chips and the results have been found to be in agreement with the model presented here. These experimental results are presented in the next chapter. This model is entirely based upon the low frequency dielectric properties of living cells as discussed in [14].

Chapter 4

First generation capacitance sensors for establishing proof of concept

4.1 Single electrode capacitance sensor: design and operation

A custom CMOS capacitance sensor for the cell sensing application was designed using the topology shown in Fig. 4.1 [20,66]. The first generation capacitance sensor employed a single electrode configuration. The passivation layer of the CMOS fabrication process was used for electrical insulation and biochemical isolation of the sensing electrode from the aqueous ionic cell medium. The single electrode configuration provides maximum penetration depth for a given excitation field. Since the already available passivation layer of the chip is used as the insulating cover for the sensing electrode which is approximately $1\ \mu\text{m}$ thick, penetration depth is an important factor to consider in the sensor design. For a single electrode capacitance sensor that functions as a proximity detector, output voltage is non-linearly related to object proximity which results in an increase in sensitivity with proximity of the sensed object to the chip surface [17]. This characteristic of the sensor makes it appropriate for monitoring anchorage dependent cells that are directly coupled to the chip surface.

The sensor operation is based upon the charge sharing principle. The sensor

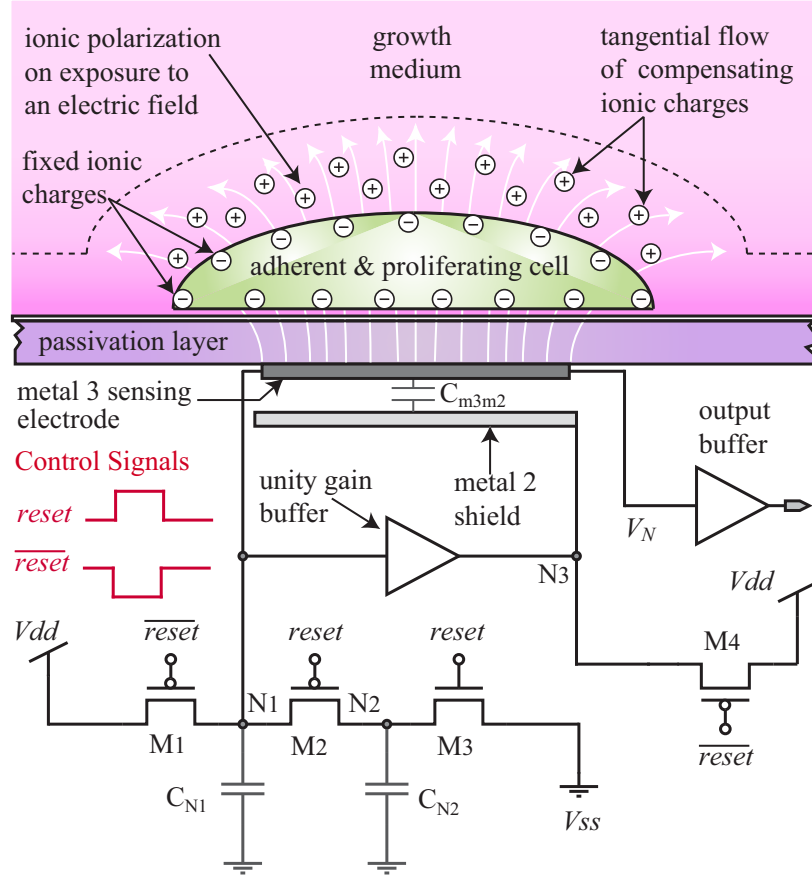


Figure 4.1: Cell-substrate capacitance sensor: design and operation.

circuit has two nodal parasitic capacitances C_{N1} and C_{N2} whose charging and discharging are controlled by a set of three MOSFET switches M1, M2 and M3. The sensor operates in two phases. In the reset phase, switches M1 and M3 are turned on, charging node N1 to V_{dd} and node N2 to V_{ss} , while M2 is off. In the evaluation phase, M2 is turned on, while M1 and M3 are off, redistributing the charges between C_{N1} and C_{N2} . The joint nodal voltage V_N is a function of the sensed capacitance C_{sensed} as a result of the charge redistribution.

$$V_N = \frac{(C_{N1} + C_{sensed})V_{dd} + C_{N2}V_{ss}}{C_{N1} + C_{N2} + C_{sensed}} \quad (4.1)$$

Here C_{sensed} refers to the effective capacitance value of the capacitive network as seen by the sensing electrode in Fig. 4.1. The topmost metal layer, metal3, forms the sensing electrode. Sensitivity and dynamic range of the measurement is maximized by minimizing the nodal parasitics. For this purpose, the substrate coupling capacitance of the sensing electrode is shielded by means of a larger area metal2 plate in the lower layer. The large capacitance C_{m3m2} between the sensing electrode and the shield is canceled by driving the metal2 shield with a potential that tracks the sensing electrode potential using a unity-gain buffer. Sensor input dynamic range improves with increasing sensing electrode area.

4.2 Sensed capacitance modeling

Several factors influence the capacitance measured at the sensing electrode by the circuit.

4.2.1 Cell layer capacitance C_{cell}

As discussed in the previous chapter, after sedimentation the cells form a complex dielectric layer at the growth medium-passivation layer interface. Ionic conductances are neglected in the model since the cell environment is exposed to weak electric fields with no conduction current flow (the sensing electrode is totally insulated from the cell environment using the chip passivation layer, a very good insulator). Thus the cell layer is regarded as purely capacitive. In reality, the cells form a heterogeneous layer which exhibits both spatial and temporal variation of

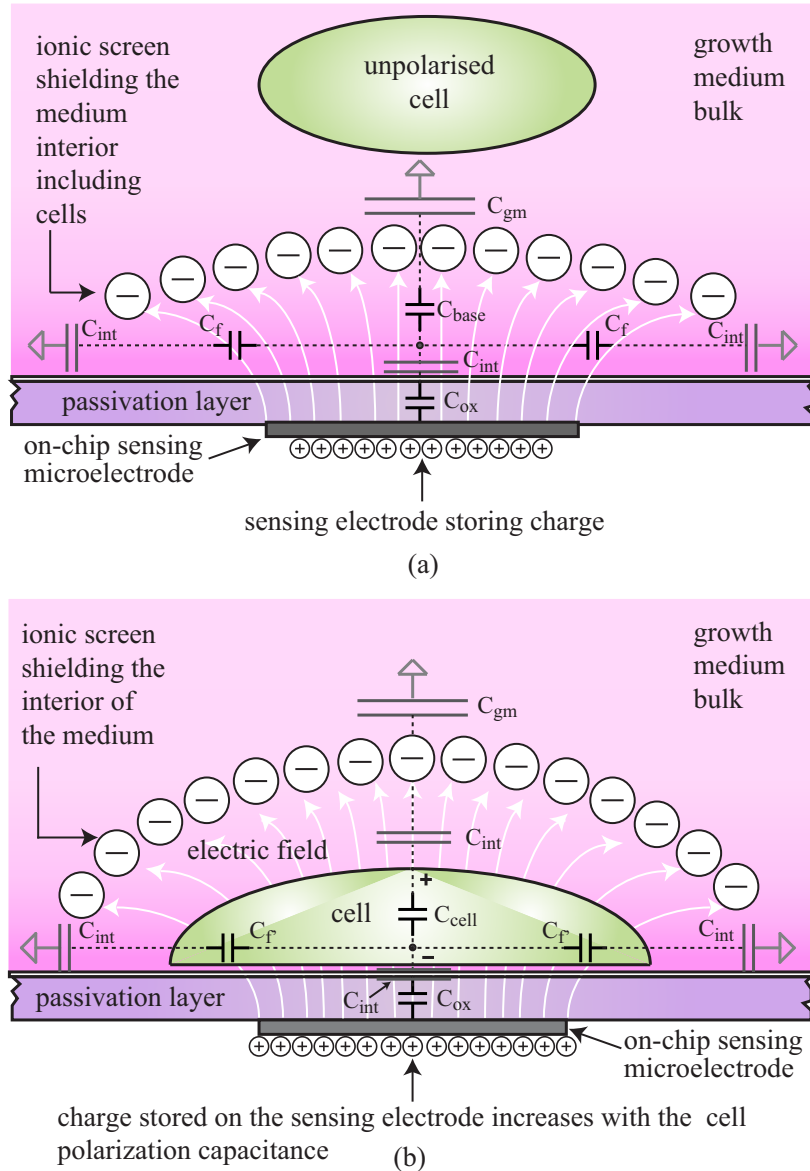


Figure 4.2: Models of sensed capacitance during the different phases of the interaction process between cells and substrate: (a)pre-adhesion phase, (b)post-adhesion phase.

dielectric properties. Results from capacitance cytometry experiments have previously reported capacitances on the order of a few fF's on account of the polarization response of the cells as they pass through an electric field across microelectrodes [34]. Therefore the cell layer capacitance is on the order of magnitude of $0.01 \text{ fF}/\mu\text{m}^2$. It is important to note that this capacitance is the whole cell capacitance which is

different from the cell membrane capacitance which is on the order of magnitude of $10 \text{ fF}/\mu\text{m}^2$ [67].

4.2.2 Passivation layer capacitance C_{ox}

The passivation layer of the fabrication process electrically isolates the sensing electrode from the cell environment. The chip passivation layer comprises silicon dioxide (dielectric constant: 4) and silicon nitride (dielectric constant: 7.5). So the effective dielectric constant of the passivation layer was assumed to be 6. For a passivation layer with uniform thickness of $1 \mu\text{m}$ and a dielectric constant of 6, the capacitance per unit area is approximately $0.05 \text{ fF}/\mu\text{m}^2$. In the sensed capacitance network C_{ox} and C_{cell} appear in series, and their order of magnitudes are comparable. Thus in order to increase the input dynamic range of the sensor, the insulation layer above the sensing electrode should be as thin as possible. The value of C_{ox} can be increased, and overall dynamic range enhanced, by thinning the passivation layer over the electrodes. However, this would require custom process development, raising significant practical issues as well as associated cost, and would limit the generality of the technique. The chip was fabricated in a commercially available CMOS technology, so the sensor design was constrained by the limitations imposed by the process technology.

4.2.3 Interfacial capacitance C_{int}

The passivation layer (a solid surface) is in direct contact with the cell growth medium (an aqueous ionic solution), resulting in a layered polarized interface according to Gouy-Chapman-Stern theory [68]. The adhesion process of cells introduces additional solid-liquid interfaces. In addition to the electrified interface there is also a diffuse layer capacitance arising from the diffuse charge extending from the interface to the liquid electrolyte bulk. The spatial extent of this space-charge region is characterized by the Debye length which, for a univalent electrolyte, can be expressed as [68]:

$$L_{DE} = (\epsilon_e kT / 2n^0 q^2)^{1/2} \quad (4.2)$$

where ϵ_e is the electrolyte permittivity and n^0 is the ionic density. The Debye length in the electrolyte is normally lesser than 10 Å for electrolytes with concentrations greater 10^{-5} M [68]. Both the interfacial and the diffuse layer capacitances occur in series and end up being on the order of 100 fF/ μm^2 , 3-4 orders of magnitude larger than the passivation layer capacitance [68].

4.2.4 Fringe capacitance C_f

The electric field originating from the sensing electrode can be resolved into vertical and lateral components. The vertical component dominates at the electrode center while the lateral component dominates at the electrode periphery. The lateral coupling gives rise to fringe capacitances. The interlayer fringe capacitances inside the chip (derived using the process parameters provided by the vendor) are on the

order of $10 \text{ aF}/\mu\text{m}$. The fringe capacitances arising from the lateral coupling of the sensing electrode with all the neighboring metal lines through the passivation layer, cells and growth medium will be on the same order of magnitude and therefore their effect cannot be ignored.

4.2.5 Growth medium capacitance C_{gm}

The growth medium, a strong electrolyte, produces an ionic screen that shields its interior from the sensing field as shown in Fig. 4.2(a). Due to this, the sensor responds to cell-related phenomena only after the cells are inside the ionic screen and exposed to the sensing field as shown in Fig. 4.2(b). This happens when they settle onto the surface and form physical contacts with it during adhesion and proliferation. Under equilibrium conditions the bulk of the growth medium is electrically neutral and is free of potential gradients, and can be considered as an ideal ionic conductor. This conductor above the cell layer is capacitively coupled to all the neighboring conductors (including metal lines for power, voltage biases and a grounded metal case housing the sensor fixture) resting at DC potentials, excluding the sensing electrodes. The sum total of all these capacitances evaluates to C_{gm} . The self capacitance of the ionic conductor places a lower bound on C_{gm} and is on the order of pF when the dimensions of the sensor well are in the cm range. For example, the self-capacitance of a conducting sphere of radius R (capacitance between the conducting sphere and another grounded hollow sphere of infinite radius and centered on the conducting sphere) is given by $C = 4\pi\epsilon_0 R$. So in our case, the

bulk of the growth medium is the ionic conductor which is capacitively coupled to the grounded metallic case housing the sensor test fixture. This capacitance will be greater than the self capacitance of the isolated growth medium bulk which is on the order of pF.

C_{gm} is expected to vary for different configurations of the sensor well. As long as the total volume of the growth medium is on the order of 100s of μLs (or higher), as in the reported sensor configuration, C_{gm} is on the order of pF's (or higher) and will not influence sensor operation.

4.2.6 Baseline capacitance C_{base}

The baseline capacitance represents the capacitance due to dielectric properties of residual materials on top of the passivation layer. These include surface residues resulting from the polymer used for encapsulation of the bond wires and from adsorption of materials from the growth medium onto the surface. The initial capacitance recording obtained from each of the sensors, at the start of every experiment (when the sensor chip was tested with biological cells) as soon as the sensor well was loaded with the cell culture suspension, is dominated by this baseline capacitance. On compiling the data obtained from all the experiments, the initial capacitance sensed by a $40 \times 40 \mu\text{m}^2$ sensor was found to vary between sub-fF values to approximately 10 fF (for a $30 \times 30 \mu\text{m}^2$ sensor, between sub-fF values to approximately 2 fF, and for a $20 \times 20 \mu\text{m}^2$ sensor, between sub-fF values to approximately 1 fF). We attribute these variations in initial sensed capacitances to different values

of C_{base} at the start of different experiments. C_{base} is sensitive to a variety of factors including surface residues on the passivation layer, microscopic air bubbles and hydrodynamic disturbances.

4.2.7 Effective sensed capacitance C_{sensed}

From the above discussion, the capacitance as seen by the sensing electrode equates to the effective capacitance offered by the network of passivation layer, cell layer, fringe parasitics and all interfacial capacitances between various liquid-solid boundaries. The sensed capacitance must be modeled separately for the pre-adhesion and the post-adhesion phases, since during the adhesion phase the interface between the growth medium and the substrate undergoes a drastic change in its structural and dielectric properties resulting in an appreciable variation in the sensed capacitance. Both models of sensed capacitance are illustrated in Fig. 4.2.

During the pre-adhesion phase of Fig. 4.2(a), the growth medium produces an ionic screen in response to the electric field originating from the sensing electrode. The ionic screen at the boundary between the growth medium and the substrate shields the interior of the solution including the suspended cells as a result of electrostatic induction. The sensed capacitance network comprises the passivation layer capacitance C_{ox} and interfacial capacitances C_{int} in series with the baseline capacitance C_{base} and C_{gm} . The fringe capacitance C_f appears in parallel with C_{base} (see Fig. 4.2(a)).

The reference potential for the fringe capacitance originates from adjacent

metal interconnects resting at DC potentials. Under equilibrium conditions the bulk of the growth medium is electrically neutral and is free of potential gradients, and can therefore be regarded as an ideal ionic conductor. The reference potential for the capacitances associated with vertical electric field coupling originates from all nearby conductors resting at DC potentials (mainly the grounded metallic case housing the sensor test fixture) to which the bulk of the growth medium is capacitively coupled to. When a ground electrode was introduced in the growth medium, we observed the sensor outputs to saturate, which indicates the presence of a grounded conducting plane on the chip surface. This can be explained by the grounding of the surface conductances that are formed at the passivation layer-growth medium interface, that effectively screen out all the components of the sensed capacitance network except for the passivation layer capacitance. This way the sensed capacitance is limited to just the passivation layer capacitance. In the absence of a ground electrode in the growth medium, the surface conductances are floating which prevents the screening of the sensed capacitance network.

The combined effect of all the different contributions towards the sensed capacitance can be visualized using the capacitance network shown in Fig. 4.2(a), with the sensed capacitance expressed as:

$$\frac{1}{C_{sensed}} = \frac{1}{C_{base} + C_f} + \frac{1}{C_{ox}} + \frac{1}{C_{int}} + \frac{1}{C_{gm}} \quad (4.3)$$

Considering the relative orders of magnitude of the various capacitances, the effective value of pre-adhesion sensed capacitance can be modeled as:

$$\frac{1}{C_{sensed}} \cong \frac{1}{C_{base} + C_f} + \frac{1}{C_{ox}} \quad (4.4)$$

The cells do not influence the cell-substrate capacitance until they have settled on the substrate below the ionic screen (that arises as a result of electrostatic induction), and are exposed to the varying electric fields (see Fig. 4.2(b)). This happens during the adhesion phase when the cellular dielectric layer begins to form on the surface of the passivation layer. So the space between the ionic screen and the solid surface can be viewed as being permeated with cellular dipoles enhancing its dielectric constant. This effect is modeled by replacing C_{base} with C_{cell} , as illustrated in Fig. 4.2(b). During this process C_f is also influenced by the cells present in neighboring regions. This effect is incorporated into the model by replacing C_f with $C_{f'}$. Again comparing the relative orders of magnitude of the various capacitances in the sensed capacitance network, the effective value of post-adhesion phase sensed capacitance can be modeled as:

$$\frac{1}{C_{sensed}} \cong \frac{1}{C_{cell} + C_{f'}} + \frac{1}{C_{ox}} \quad (4.5)$$

It is important to note that C_{base} , C_{cell} , C_f and $C_{f'}$ represent lumped parameter values of their corresponding capacitances which are actually distributed in nature due to their heterogenous and time-varying characteristics. As mentioned previously, the cell layer capacitance C_{cell} is a function of many factors influencing its structural and dielectric properties [7, 8, 69]. These include membrane integrity, membrane potential, cell morphology, adhesion strength, extra-cellular ionic distributions and

also number and surface area coverage of cells above the sensing electrode.

The above discussed models for the pre-adhesion, adhesion and post-adhesion phases have been developed to explain the observations made during the experiments that were performed with actual biological cells cultured on fabricated capacitance sensor chips. Several experiments involving three different cell types have been performed with the sensor chips and the results have been found to be in agreement with the models presented here. The experimental results are presented in the following sections. The models are based upon the low frequency dielectric properties of living cells as discussed in [14].

4.3 Chip design, fabrication and bench testing

The capacitance sensor was designed using the Cadence Design Suite by employing the technology parameters for a commercially available $0.5\ \mu\text{m}$ standard CMOS process. The sensor circuit was designed for a 3 V supply and for an operating frequency of 1 kHz. The design was simulated using the Cadence Spectre Simulator by employing the parametric analysis feature for varying the input sensed capacitance. The sensor chip layout was drawn using the Cadence Virtuoso Layout software. The layout information was then submitted to the MOSIS service for chip fabrication. The sensor chip measuring $1.5\times 1.5\ \text{mm}^2$ was fabricated in a commercially available $0.5\ \mu\text{m}$, 2-poly, 3-metal standard CMOS technology.

Sensor dynamic range improves with increasing sensing electrode area. For studying the influence of this dependence on the sensor response to cells, three

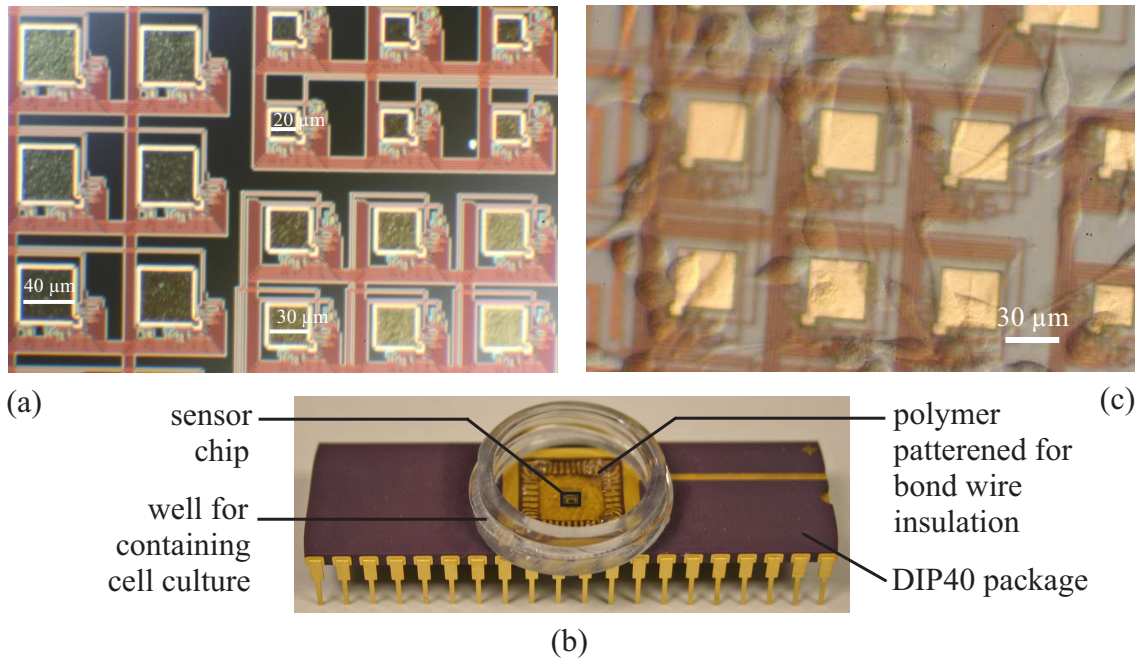


Figure 4.3: (a) Photomicrograph of the fabricated sensors showing the three sensor groups with sensing electrode areas: $20 \times 20 \mu\text{m}^2$, $30 \times 30 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$. (b) Photograph of a biocompatibly packaged capacitance sensor chip. (c) Photomicrograph of MDA-MB-231 human breast cancer cells cultured *in vitro* on top of a capacitance sensor chip.

sensor groups with electrode areas of $20 \times 20 \mu\text{m}^2$, $30 \times 30 \mu\text{m}^2$ and $40 \times 40 \mu\text{m}^2$ were designed and tested. The chip comprised an array of 28 sensors (9 sensors of size $20 \times 20 \mu\text{m}^2$, 9 sensors of size $30 \times 30 \mu\text{m}^2$ and 10 sensors of size $40 \times 40 \mu\text{m}^2$) confined within an area of $400 \times 400 \mu\text{m}^2$. Fig. 4.3(a) shows a photomicrograph of the fabricated sensors.

The chip was bench tested by calibrating the sensors as proximity detectors [bench testing was performed along with J. Van Sickle]. Calibration was performed by using an external metal electrode whose vertical positioning was controlled by means of a piezoelectric micropositioner. The micropositioner was controlled by means of a hand terminal that specified the vertical distance through which the

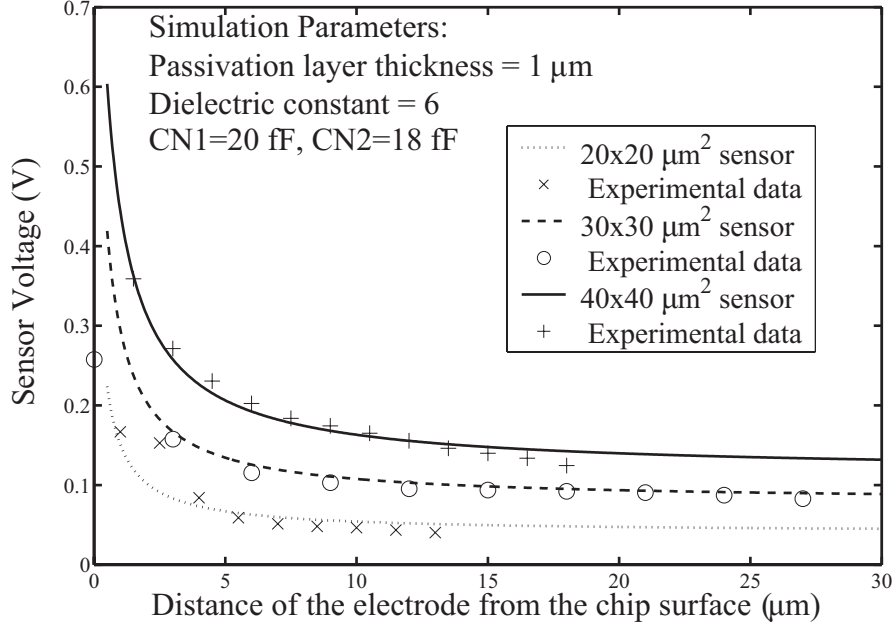


Figure 4.4: Variation of the sensor voltages with electrode distance.

metal electrode was to be translated. The metal electrode was an insulated needle held by the translation stage comprising the micropositioner. The needle was electrically floating and was not connected to any DC source or the ground. So for the proximity detection application, the environment is employed as the return path for the capacitive current [41]. Fig. 4.4 shows the test results superimposed on the simulated sensor voltages. The symbols represent experimental values of sensor voltage obtained by moving the micropositioned electrode in steps of 2 to 3 μm . The output voltage ranges for the 20x20, 30x30 and 40x40 μm^2 sensors were found to be 100 mV, 200 mV and 400 mV respectively. The solid curves are the sensor outputs simulated using the charge sharing relation Eqn. 4.1 for the three sensor groups. Upon knee-fitting the bench test results with the simulated curves using the least squares technique, the nodal parasitic capacitances C_{N1} and C_{N2} were estimated using least squares fits to be 20 fF and 18 fF respectively [17].

In order to translate the sensor outputs to sensed capacitance values, the output voltages during the evaluation phase are subtracted from their corresponding voltages during the reset phase for offset cancelation. In some cases, this results in negative values of sensed capacitances due to small voltage fluctuations. The inverse relation for C_{sensed} as a function of this voltage difference can be derived from (4.1) as

$$C_{sensed} = \frac{(V_{dd} - V_{ss})C_{N2} - V_{diff}(C_{N1} + C_{N2})}{V_{diff}} \quad (4.6)$$

where $V_{diff} = V_{reset} - V_{eval}$ and $V_{reset} = V_{dd}$. Here both V_{reset} and V_{eval} refer to the voltages before the readout buffer.

4.4 Sensor resolution analysis

For the single electrode capacitance sensor functioning as a proximity detector, sensitivity is a function of object proximity. Sensor sensitivity increases with object proximity to chip surface as can be seen from the simulated plots in Fig. 4.4. This characteristic is appropriate for the present application, since the cells are directly coupled to the chip surface. Due to the nonlinear relation between proximity and the sensor output, the distance resolution varies with the object proximity. The distance resolution $R(d_i)$ at a distance $d = d_i$ from the chip surface can be computed using the relation:

$$R(d_i) = \frac{\sigma_{noise}}{\frac{\partial V_{diff}}{\partial d}(d_i)} \quad (4.7)$$

where σ_{noise} is the sensor output noise level and

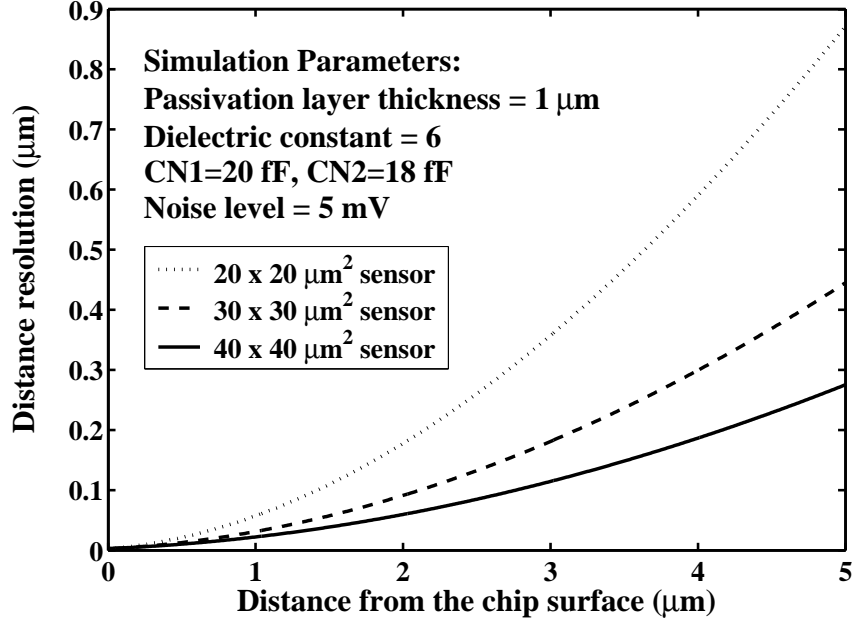


Figure 4.5: Sensor distance resolution as a function of object proximity.

$$\begin{aligned}
V_{diff} &= V_{reset} - V_{eval} \\
&= V_{dd} - \left[\frac{(C_{N1} + C_{sensed})V_{dd} + C_{N2}V_{ss}}{C_{N1} + C_{N2} + C_{sensed}} \right] \\
&= \frac{C_{N2}(V_{dd} - V_{ss})}{C_{N1} + C_{N2} + C_{sensed}} \tag{4.8}
\end{aligned}$$

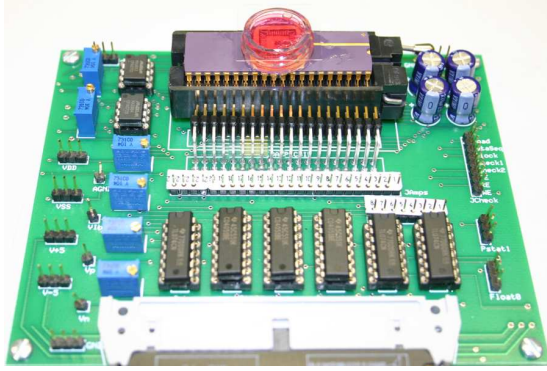
Distance resolution improves with increasing proximity to the surface, increasing electrode area and decreasing noise level. So for a given sensor with a fixed sensing electrode area, the best possible resolution is achieved when the object is in contact with the chip surface. Fig. 4.5 shows a plot of distance resolution for the three sensor groups with different electrode areas as a function of proximity, for a measured noise level of 5 mV (standard deviation of the output voltage fluctuations). The sensors exhibit a distance resolution of 3 nm when the sensed object is in contact with the chip surface ($R(d_i = 0 \mu\text{m}) = 3$ nm in Fig. 4.5). The corresponding capacitance resolution was evaluated to be 135 aF, with a maximum sensor gain of 37 mV/fF

(this is the maximum sensor gain as was derived from the simulated plots shown in Fig. 4.4).

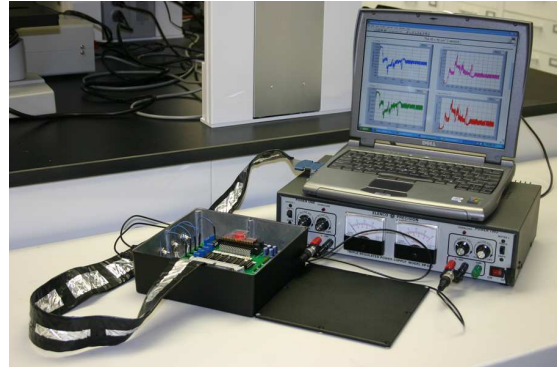
4.5 *In vitro* experiments demonstrating sensor response to cell phenomena

For the purpose of testing the sensors *in vitro*, the sensor chip in a DIP40 ceramic carrier was encapsulated using a biocompatible polymer for bond wire insulation and isolation of cells from toxic materials of the DIP40 chip carrier [biocompatible chip packaging was performed by M. Urdaneta]. The encapsulation material is a photopatternable polymer (Loctite 3340, Henkel) [70]. A well (diameter = 1.5 cm, height = 0.5 cm) was glued on top of the packaged chip for containing the cell culture medium. Fig. 4.3(b) shows a photograph of the final test fixture.

Fresh unused chips possessing clean surfaces without any additional surface modification or functionalization were used for all the experiments. Prior to cell loading, the biocompatibly packaged chip was rinsed with deionized water, sterilized using UV light, and then rinsed with the corresponding cell growth medium. The UV light does not affect the capacitance characteristics of the chip (sensor outputs did not change before and after exposure to UV light) and was used for sterilization only before the sample is loaded. In every experiment, 500 μL of the cell suspension was loaded into the sensor well using standard aseptic techniques. The sensor well was sealed using either a cover slip or a gas permeable Breathe-Easy membrane (Fisher Scientific). Fig. 4.3(c) shows a photomicrograph of MDA-MB-231 human breast



(a)



(b)

Figure 4.6: (a) Photograph of a cell loaded chip mounted on the test board. (b) Photograph of the data acquisition setup.

cancer cells cultured on a capacitance sensor chip. To date, the sensor chips have been tested with three different cell types namely: bovine aortic smooth muscle cells (BAOSMC), human breast cancer cells (MDA-MB-231) and human colonic adenocarcinoma cells (Caco-2).

The sensor chip with cells loaded into the well was then mounted on a test board with a data acquisition interface. The board was placed inside a grounded metal case (functioning as a Faraday shield) and was powered using a regulated supply. The chip was monitored using a laptop running LabVIEW 7.1 (National Instruments) and interfaced to the test board using a PC-CARD-DAS16/16AO data acquisition card (Measurement Computing). A shielded PCMCIA cable was used to connect the data acquisition card to the test board. The test fixture containing the sensor chip was maintained at 37°C , 5% CO_2 inside an incubator during the monitoring period.

The above described procedure was common to all the experiments involving

monitoring sensor responses to cells cultured on the chip surface. These experiments are described in the following sections.

4.5.1 Tracking cell adhesion

4.5.1.1 Experiment 1: Averaged sensor response to cell adhesion

This experiment was performed with bovine aortic smooth muscle cells [bio-compatible chip packaging and cell loading was performed by N.M. Nelson]. The cells were cultured in a T25 flask in growth medium (pH 7.4 and buffered for CO₂) in a commercially prepared medium supplemented with serum, growth factors and antibiotics (Cell Applications Inc.). The cells were allowed to grow in the flask until they were confluent and were then detached by using a cell scraper. After cell detachment a suspension with an approximate density of 1×10^6 cells/mL was prepared. The sensor chip was first calibrated by adding the BAOSMC growth medium alone without cells and measuring the capacitive coupling between the solution and electrodes. The well was then loaded with the high density BAOSMC suspension so that all the sensors in the test array were exposed to similar conditions. The sensor outputs were monitored over a period of 24 hours. This experiment was conducted before the above described data acquisition system was developed and therefore the sensor measurements were recorded manually. In between measurements the fixture was maintained inside an incubator at 37°C, 5% CO₂. Coupling of cells to every sensor was confirmed through visual observation [visual observation was performed along with N.M. Nelson].

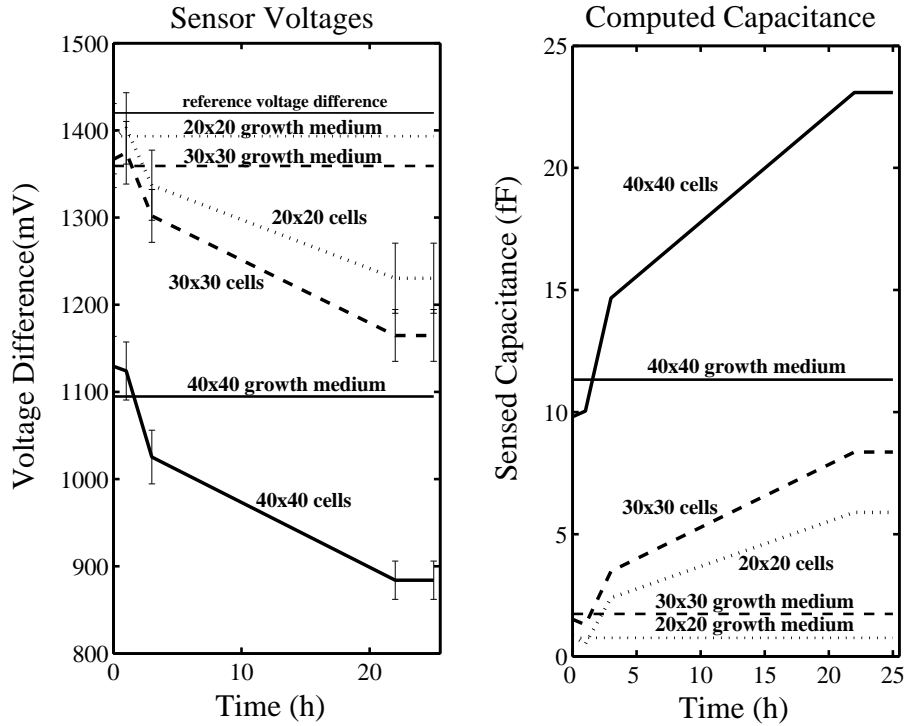


Figure 4.7: Averaged sensor response to cell adhesion. The data points show the average output voltage differences and standard deviation values across the sensors in each of the three groups. The horizontal lines plotted are the average sensor recordings with the chip exposed to growth medium alone before the sensor well was loaded with cells and have been plotted here across the time frame for comparing with the averaged sensed capacitances that were recorded in response to cell adhesion.

The sensed capacitances were computed as discussed previously. Fig. 4.7 shows a plot of the average voltage differences for the three sensor groups. Error bars indicate the standard deviation in response between all sensors of the same size. The voltage differences for all three sensor groups decreased with time, tracking the adhesion process as expected and indicating an increase in capacitive coupling between the cells and the on-chip electrodes after they were allowed to settle on the chip surface over a period of time. Based upon these measurements the computed average sensed capacitances increased by 5.1 fF, 6.9 fF and 13.2 fF for the 20x20,

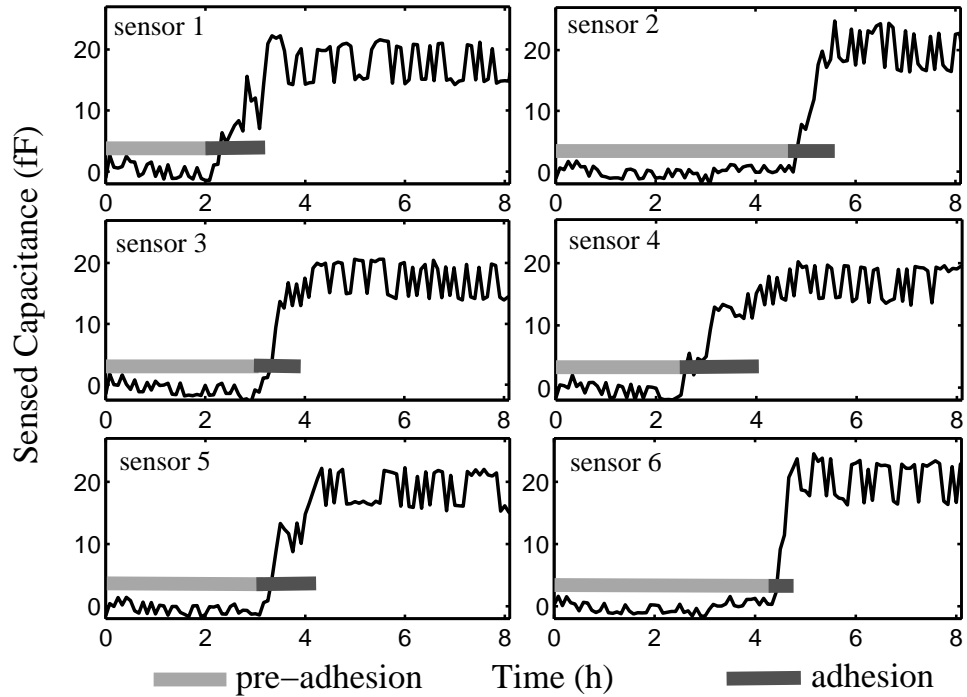


Figure 4.8: Online tracking of cell adhesion process by six $40 \times 40 \mu\text{m}^2$ sensors.

30×30 and $40 \times 40 \mu\text{m}^2$ sensor groups respectively as shown in Fig. 4.7.

4.5.1.2 Experiment 2: Online tracking of cell adhesion

In this experiment the previously described data acquisition system was set up for online monitoring of the sensor responses to BAOSMC loaded on top of the chip surface and placed inside an incubator. BAOSMC loading and incubation were performed using standard aseptic techniques [biocompatible chip packaging was performed by M. Urdaneta]. The test fixture containing the sensor chip was maintained at 37°C , $5\% \text{CO}_2$ inside an incubator during the monitoring period. The sensor readings were recorded every 5 minutes with the cells exposed to electric field excitations only during the short recording intervals.

Fig. 4.8 shows the sensed capacitances as recorded concurrently by six 40×40

μm^2 sensors during the first 8 hours of cell incubation. The capacitance plots are indicative of the pre-adhesion and adhesion phases as discussed in the previous chapter (experimental observation agrees with the proposed model). The cells took around 2.5-4.75 hours to initiate adhesion after sedimentation and around 30 minutes to 1.5 hours to adhere (pre-adhesion: 3.29 ± 1.05 hours, adhesion: 1.08 ± 0.34 hours). The figure also shows phase delays in the initiation of cell adhesion as recorded by sensors in different locations. The capacitance fluctuations observed throughout the monitoring interval (predominantly in the post-adhesion phase) have been attributed to interference noise coupling to the sensing node during the sensor evaluation phase. This is discussed further in Section 4.5.5.

4.5.2 Monitoring cell viability

4.5.2.1 Experiment 1: Averaged sensor response to changes in cell viability and sensor response validation using Neutral Red

This experiment with BAOSMC monitored the sensor response to changes in cell viability. For this the procedure in section 4.5.1.1 was repeated but this time with BAOSMC stained with Neutral Red in a colorless growth medium [biocompatible chip packaging was performed by M. Urdaneta and cell loading was performed by N.M. Nelson]. The sensors were monitored over a period of 48 hours. This experiment too was conducted before the data acquisition system was developed and therefore the sensor measurements were recorded manually. Cell viability was assessed independently through visual inspection of the stained cells. Living healthy

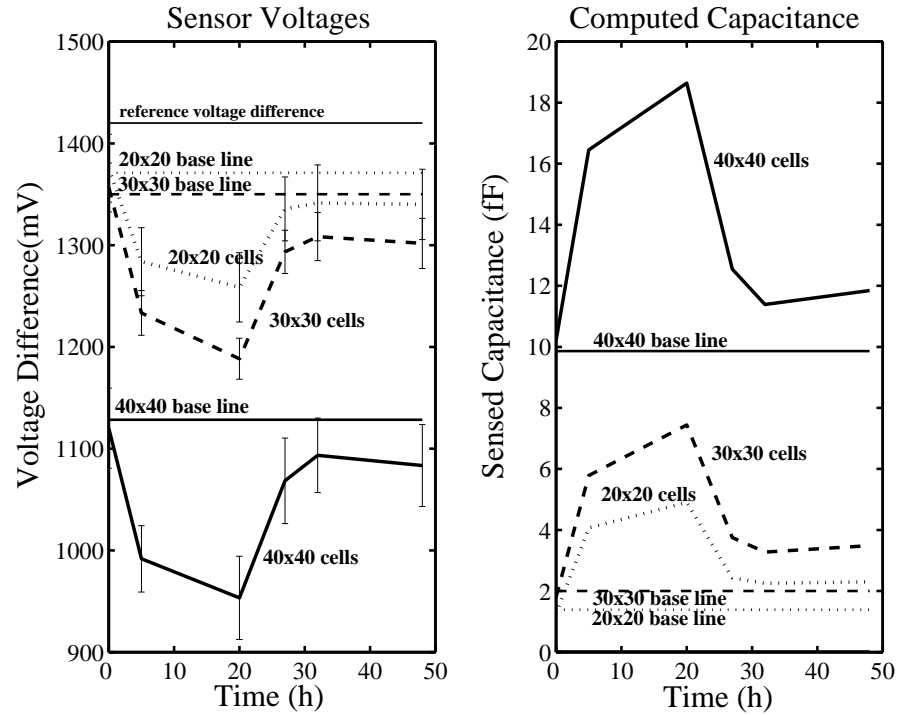


Figure 4.9: Averaged sensor response to changes in cell viability.

cells have the characteristic property of taking up and retaining Neutral Red stain whereas non-viable cells do not retain the stain [47]. Fig. 4.9 shows the averaged response of the three sensor groups over the 48 hour period. Over the first day the cells were able to retain the stain (confirmed along with N.M. Nelson through visual observation: colorless medium remained colorless) and the sensors showed an increase in capacitive coupling between cells and sensor electrodes. On the second day, however, it was observed that the cells no longer retained the stain and had released the dye into the growth medium (visual confirmation was performed along with N.M. Nelson), an indication of non-viability. Accordingly the sensors showed a decrement in the measured capacitance values. The compromised cell viability was attributed to the gas-impermeable cover slip that was used to seal the sensor well after cell loading in order to maintain sterility.

4.5.2.2 Experiment 2: Online monitoring of cell viability and sensor response validation using Alamar Blue

In this experiment the data acquisition system was set up for online monitoring of the sensor responses to changes in BAOSMC viability [biocompatible chip packaging was performed by M. Urdaneta]. The sensor responses were continuously acquired every 5 minutes for a period of 29 hours with BAOSMC incubated on top of the chip surface. For validation purposes cell viability was confirmed using Alamar Blue (obtained in aqueous form from Biosource International), a cell viability dye. Alamar Blue is commercially available in an oxidized, blue, nonfluorescent form (resazurin), which becomes gradually reduced to its pink fluorescent form (resorufin) in a medium containing viable cells [56]. The dye molecules are reduced by a class of enzymes called reductases found in mitochondrial membranes and the cytosol [71]. Reduction of Alamar Blue is directly correlated with the number of viable cells, incubation time and temperature. The resazurin reduction test has increasingly been used in cytotoxicity assays for high-throughput screening in pharmacological applications [72] because it is nontoxic and nonterminal, that is, it does not require that the cells in the sample be killed in order to make the measurement.

BAOSMC loading and incubation were performed as in the previous experiments, with Alamar Blue mixed into the growth medium in a 1:10 ratio by volume. The culture well has a sample capacity of approximately 500 μl . Fig. 4.10 shows the sensed capacitances as recorded concurrently by three of the on-chip sensors, one representative trace from each sensor group with different sensing electrode area.

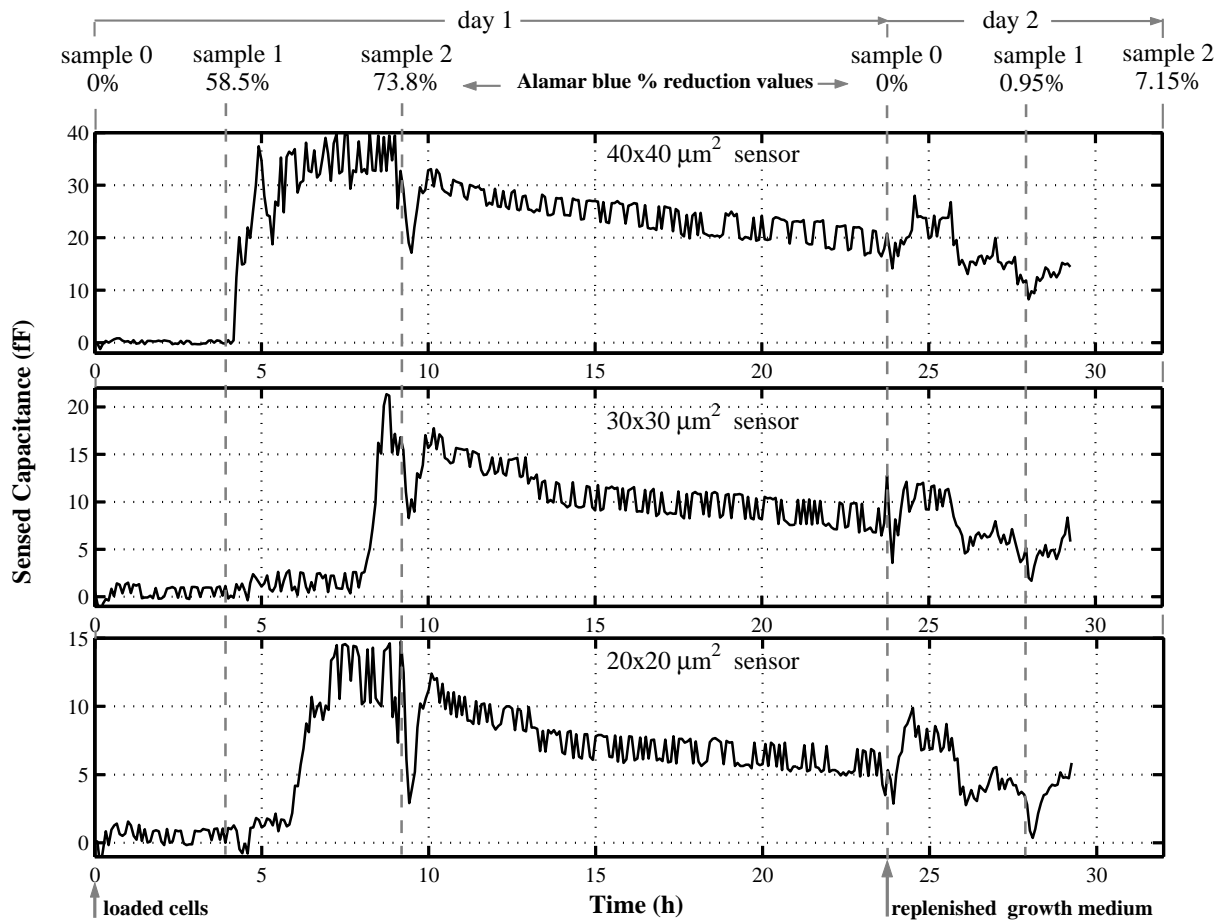


Figure 4.10: Online monitoring of cell viability with concurrent measurements using Alamar Blue dye. Alamar Blue % reduction values obtained from spectrophotometric analysis are shown above the times corresponding to extraction of the microsample.

The fraction of Alamar Blue in reduced form was evaluated by measuring the absorbance of the growth medium at 570 nm and 600 nm. This was accomplished by performing spectrophotometric analysis on 20 μL samples extracted from the sensor well at instances during the monitoring period denoted by the vertical time lines in Fig. 4.10.

The sensed capacitance values tracked the pre-adhesion and adhesion phases as in the previous experiments. After adhesion the sensed capacitances remained

high until the 9th hour of incubation, which is indicative of viability. Alamar Blue was gradually reduced to its pink form during this 9 hour interval, confirming positive cell viability. According to spectrophotometric readings, the fraction of Alamar Blue in reduced form was found to be 0%, 58.5% and 73.8% at 0, 4 and 9 hours, respectively, with reference to the initial cell loading time. Over the next 15 hours, however, the sensed capacitances began to fall gradually, which is indicative of compromised viability. This decrease is attributed to oxygen deprivation resulting from the presence of a gas impermeable glass cover slip over the sensor well. The cover slip served to maintain sterility of the sample well during the extended observation period. In order to confirm the observed reduction in cell viability, the sensor well was replenished at the beginning of the second day with a fresh solution of growth medium and Alamar blue. As seen in Fig. 4.10, over the next 1 hour interval the capacitances increased and stabilized, possibly due to the fresh oxygen and nutrient supply. However, over the next few hours the capacitances decreased again, which is indicative of compromised viability. This result is confirmed by the concurrent Alamar Blue measurements: minimal color change was observed, in contrast to measurements of the previous day. Alamar Blue % reduction values were found to be 0%, 0.95% and 7.15% at 0, 4 and 8 hours, respectively, with reference to the growth medium replenishment time on the second day. The transient drops in the sensed capacitance values at the microsample extraction times can be attributed to hydrodynamic disturbances created by introducing the micropipette tip inside the culture well. Hydrodynamic effects have the potential to disturb the ionic equilibrium responsible for the biophysical origin of the cell-substrate capacitance. (The parasitic

capacitances inside the circuit are fixed and are not influenced by disturbances in the off-chip environment. Therefore they are not responsible for the observed transient drops.)

In this experiment, good correlation was observed between on-chip measurements of the capacitance between cells and substrate, and the Alamar Blue reduction measurements of cellular metabolism.

4.5.2.3 Experiment 3: Long term monitoring of cell viability in a closed undisturbed environment

In this experiment BAOSMC were continuously monitored in a closed, undisturbed environment on top of the sensor chip, without growth medium replenishment for a period of four days [biocompatible chip packaging was performed by M. Urdaneta]. This experiment was mainly performed to test the reliability of the biocompatible package and also consistency in the experimental results in comparison to the previous experiments with the bovine cells. This experiment was again performed using the gas-impermeable cover slip for sealing the sensor well. Fig. 4.11 shows a four day plot of the sensed capacitance as recorded by a sensor with a sensing electrode area of $40 \times 40 \mu\text{m}^2$. As shown in the figure, the capacitance tracked the initial pre-adhesion and adhesion phases over the first few hours. Then the capacitance exhibited many fluctuations, indicating ongoing cell activity. Over the last two days the time averaged value of the measured capacitance leveled out, indicating compromised viability and inactivity due to starvation and lack of oxygen.

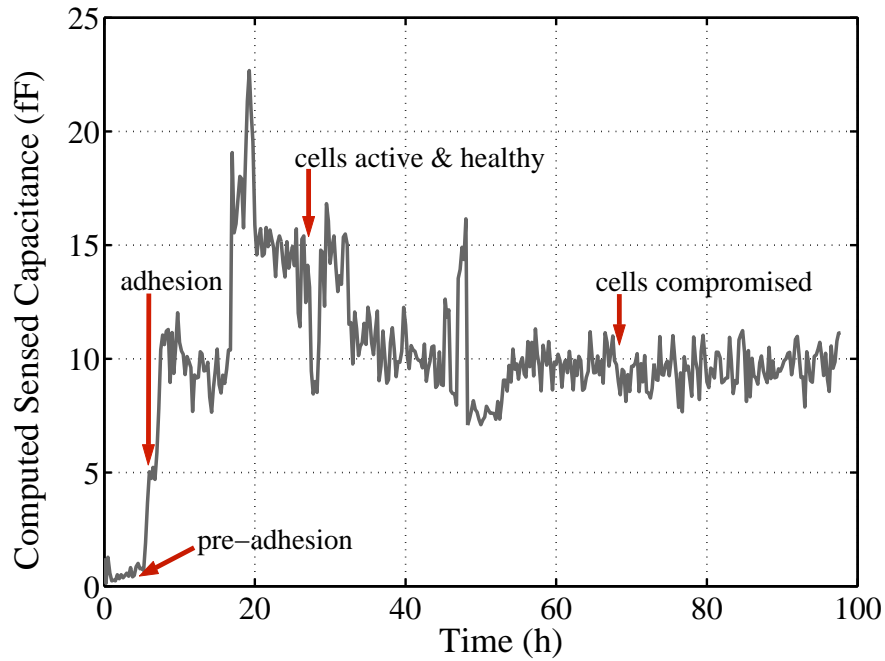


Figure 4.11: Long term measurement of cell capacitance with cells monitored in a closed undisturbed environment for a period of four days.

The above interpretation of the experimental results is entirely based on the results obtained from previous experiments performed with BAOSMC wherein the initial capacitance increase within the first 8 hours of incubation was attributed to cell adhesion, sensed capacitances remaining high was attributed to good cell health and a decrease in sensed capacitance was attributed to compromised viability. These correlations between the time varying characteristics of the sensed capacitance, and the adhesion and viability properties of cells have already been established through visual observation and validation using Neutral Red and Alamar Blue dye tests performed in the previous experiments.

4.5.3 Tracking cell proliferation

4.5.3.1 Experiment and results

This experiment was performed with MDA-MB-231 human breast cancer cells [cells acquired from Dr. H. Ghandehari and Dr. A. Nan] with the purpose of tracking cancer cell proliferation using the integrated capacitance sensors. So for this, firstly a low cell density suspension was employed (in comparison to a cell density of 1×10^6 cells/mL employed in the previous experiments) in order to ensure that all the sensors do not get coupled to the cells during the adhesion phase. Secondly, the gas-impermeable cover slip was replaced with a gas permeable Breathe-Easy membrane (Fisher Scientific) allowing for gas exchange so that cell viability was not compromised due to oxygen deprivation [employing Breathe-Easy membrane was suggested by Dr. W.E. Bentley]. MDA-MB-231 human breast cancer cells are actively dividing cells with a short doubling time of 26 hours.

MDA-MB-231 cells were cultured in a T25 flask in growth medium (pH 7.4 and buffered for CO₂) comprising 94.7% improved minimum essential medium (IMEM; Invitrogen), 5.0% fetal bovine serum (Invitrogen), and 0.3% penicillin-streptomycin (100x) (Invitrogen) by volume. The cells were allowed to grow in the flask until they were well into their exponential growth phase, which requires around 48 hours for the MDA-MB-231 cells. The cells were then detached by using 0.25% Trypsin/EDTA (Invitrogen). After cell detachment a suspension with an approximate density of 1×10^5 cells/mL was prepared. Cell density was determined using a hemocytometer. The sensor well was loaded with the cancer cell suspension using the procedure

stated at the beginning of this section. The sensor well was sealed using a gas permeable Breathe-Easy membrane (Fisher Scientific) allowing for gas exchange. Fig. 4.3(c) shows a photomicrograph of MDA-MB-231 cells cultured on the sensor chip.

A total of 16 sensors (5 sensors of size $20 \times 20 \mu\text{m}^2$, 5 sensors of size $30 \times 30 \mu\text{m}^2$ and 6 sensors of size $40 \times 40 \mu\text{m}^2$) were monitored over a period of 18 hours. Fig. 4.12 shows sample responses obtained from 4 of the monitored sensors. For those sensors the time averaged value of the sensed capacitances remained low until the 6th hour of incubation which is indicative of the pre-adhesion phase during which the cells settle onto the surface passively, but have not yet made any adhesion contacts with the chip surface. The capacitance plots then showed increases during the 6th, 7th and 8th hours with different phase delays in the capacitance increases at the different sensor locations. The capacitance fluctuations observed throughout the monitoring interval (predominantly in the post-adhesion phase) have been attributed to interference noise coupling to the sensing node during the sensor evaluation phase. This is discussed further in Section 4.5.5.

Table 4.1 displays the initiation time T_i , duration time T_d , and overall change ΔC , for the capacitance increases as observed from recordings of the 16 monitored sensors. For extracting T_i and T_d values the sensor data was first smoothed using an algorithm employing Hamming filtering with a window size of 10 samples. T_i reflects the time at which the adhesion phase began and was quantified as the first time point at which the sensed capacitance exceeded its starting value by more than two standard deviations:

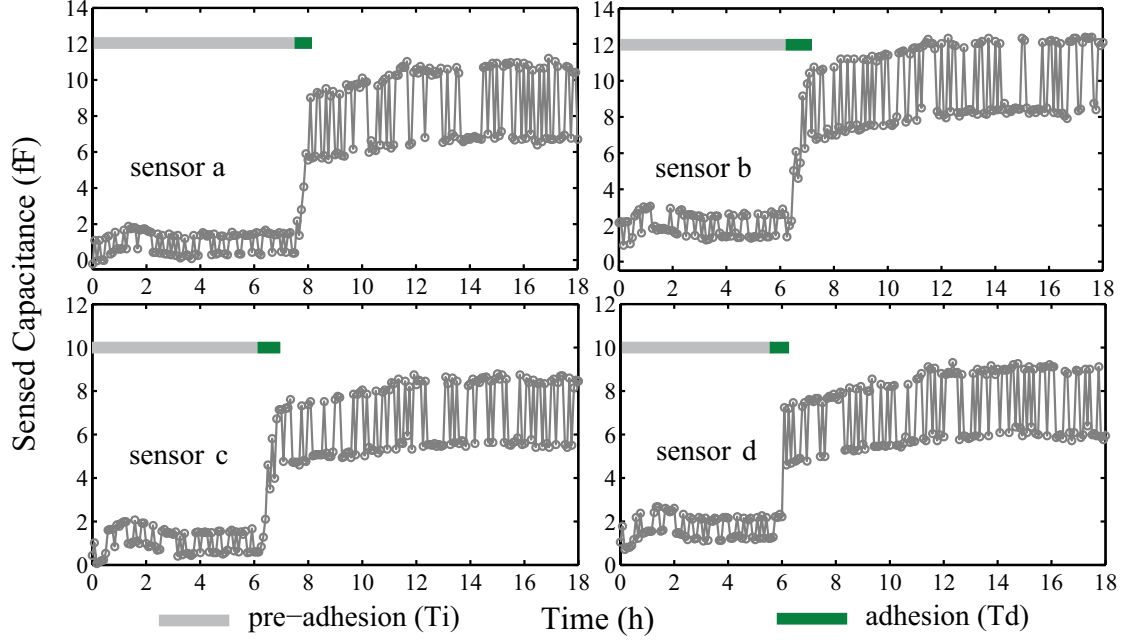


Figure 4.12: Sample capacitance plots showing sensor response to MDA-MB-231 cell adhesion; sensors a and b have a sensing electrode area of $30 \times 30 \mu\text{m}^2$; sensors c and d have a sensing electrode area of $20 \times 20 \mu\text{m}^2$.

$$Ti = t_n \iff C(t_n) - \mu_{start} \geq 2\sigma_{start} \quad \text{for } T_{start} < t_n < T_{end} \quad (4.9)$$

where $C(t_n)$ is the sensed capacitance at time $t = t_n$, T_{start} and T_{end} are the beginning and ending of the observation period, and μ_{start} and σ_{start} are the mean and standard deviation of the capacitance during the time period $t = 0$ to T_{start} . The gradients of all the sensed capacitance measurements vs. time were consistently observed to first rise, attain a peak value, and then fall over the periods during which the capacitances increased. Td was chosen to be the time interval after which the gradient $\partial C/\partial t$ of the sensed capacitance dropped to zero or below after having attained its peak at $t = t_{max}$:

$$Td = t_n - Ti \iff \frac{\partial C(t_n)}{\partial t} \leq 0 \quad \text{for } t_n > t_{max}, T_{start} < t_n < T_{end} \quad (4.10)$$

ΔC values were computed from the difference in the means of 10 capacitance samples acquired before and after the capacitance increase.

Table 4.1: Initiation time T_i , duration time T_d , and overall change ΔC values obtained from sensed capacitance plots for all 16 monitored sensors across the three sensor groups. Cell loading performed at $t = 0$ hr.

20×20 μm^2 sensors			30×30 μm^2 sensors			40×40 μm^2 sensors		
T_i	T_d	ΔC	T_i	T_d	ΔC	T_i	T_d	ΔC
(h)	(min)	(fF)	(h)	(min)	(fF)	(h)	(min)	(fF)
5.83	30	4.48	5.92	50	4.58	5.75	45	17.90
5.83	30	4.59	6.25	55	6.12	9.92	85	26.66
5.92	45	3.43	6.58	40	6.88	10.58	70	21.66
5.92	50	5.71	7.58	50	6.22	11.17	105	19.98
6.33	50	4.90	7.58	105	5.90	14.83	110	18.03
*	*	*	*	*	*	16.17	110	22.59

All 5 of the 20×20 μm^2 sensors, all 5 of the 30×30 μm^2 sensors and just 1 of the 40×40 μm^2 sensors recorded a capacitance increase around the 6th, 7th and 8th hours of incubation. The sensor response to cell adhesion was similar to those recorded in previous experiments with BAOSMC. For example, in the experiment reported in section 4.5.1.2 a cell suspension of higher concentration was employed to ensure that all the sensors were covered with cells during adhesion, as a result of which all sensors recorded an increase in capacitance within the first 5 hours of incubation with a 3 hour spread in the T_i values

Fig. 4.13 shows sample responses as obtained from 4 of the 6 40×40 μm^2 sensors that were monitored. The inset also shows relative positions of all the 40×40 μm^2 sensors (both monitored and not monitored) that are distributed over

an on-chip area measuring $120 \times 400 \mu\text{m}^2$. The location corresponding to each of the sensing electrodes where the capacitance increase was recorded has been indicated by the shaded squares in the respective sensor panels. Electrode locations with dashed outlines were not monitored during the experiment. As indicated from the plots and the timing information in Table 4.1, the sensed capacitances as recorded by sensors 2 to 6 of the $40 \times 40 \mu\text{m}^2$ sensor group remained low during the first 10 hour interval while all the sensors in the other two groups and 1 of the $40 \times 40 \mu\text{m}^2$ sensors (sensor 1) recorded a capacitance rise by the end of the 8th hour. This indicates that no cells had adhered to locations above sensors 2 to 6, since the cell density of the suspension was not high enough to cover the entire active area of the chip with cells. Sensors 2 to 6 then recorded capacitance increases during the 10th, 11th, 12th, 15th and 17th hours of incubation with a wider distribution in T_i values (spread over a period of 6.25 hours) which is suggestive of cell proliferation. This agrees well with the fact that MDA-MB-231 breast cancer cells are actively dividing cells with a short doubling time of approximately 26 hours [73]. As expected, the cells began to proliferate once they adhered to the surface.

An interesting observation can be drawn from the sensed capacitance values recorded by sensors 3, 5 and 6. These sensors are located adjacent to each other on the chip. In Fig. 4.13 it can be seen that the sensed capacitance plots indicate a proliferation wavefront traveling from sensors 3 and 5 towards 6, over a span of 6 hours. Such a progression in the responses of the sensors located in a very small area over a relatively long duration is clearly suggestive of an underlying process of cell proliferation in that area.

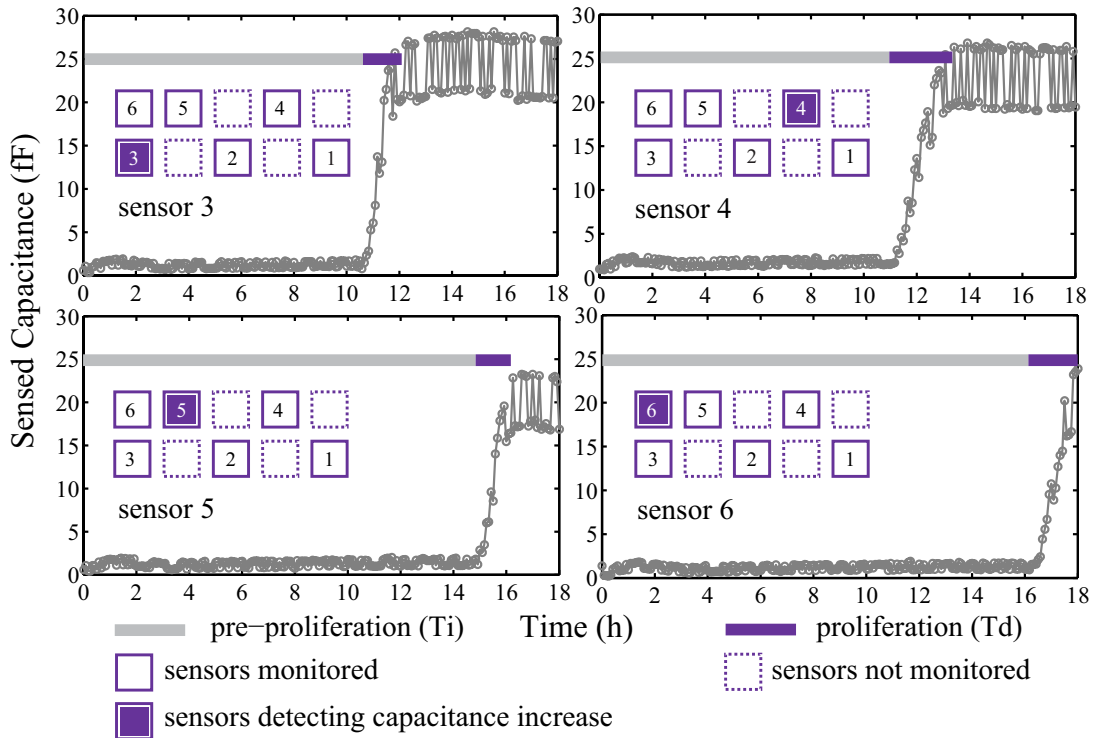


Figure 4.13: Sample capacitance plots showing sensor response to MDA-MB-231 cell proliferation. The 10 squares in each panel display the relative locations of the 10 $40 \times 40 \mu\text{m}^2$ sensors. The term “pre-proliferation phase” refers to the period before cell proliferation during which the sensors were not coupled to any cells.

In this experiment, validation of the sensor response to cell proliferation was carried out through microscopic analysis at the end of the 18 hour long monitoring period. At that time it was found that all sensors were covered by well attached, adherent cells. Due to technical constraints, this microscopic analysis was performed only at the end of the monitoring because it imposed conditions which interrupted the ongoing measurement. Microscopic imaging of cells on the chip requires reflectance-mode optics. Fluid above the chip surface introduces optical distortion, so it must be removed prior to imaging, thus disrupting the experimental continuity.

4.5.3.2 Estimating cell doubling time

Summarizing the experimental results, a total of 16 sensors (5 sensors of size $20 \times 20 \mu\text{m}^2$, 5 sensors of size $30 \times 30 \mu\text{m}^2$ and 6 sensors of size $40 \times 40 \mu\text{m}^2$) were monitored. Out of these 16 sensors, all 5 of the $20 \times 20 \mu\text{m}^2$ sensors, all 5 of the $30 \times 30 \mu\text{m}^2$ sensors and just 1 among the $40 \times 40 \mu\text{m}^2$ sensors recorded capacitance increases indicating cell adhesion. Later on, the remaining 5 of the $40 \times 40 \mu\text{m}^2$ sensors (sensors labeled 2 to 6 in Fig. 4.13) recorded capacitance increases during the 10th, 11th, 12th, 15th and 17th hours of incubation which are suggestive of cell proliferation.

The T_i and T_d values listed in Table 4.1 for the $40 \times 40 \mu\text{m}^2$ sensors provide an indirect measure of the cell proliferation rate and the sensed capacitance plots provide temporal traces of the actual proliferation process. The narrow 1.83 hour spread in the T_i values corresponding to the $20 \times 20 \mu\text{m}^2$ sensors, the $30 \times 30 \mu\text{m}^2$ sensors and sensor 1 in the $40 \times 40 \mu\text{m}^2$ group suggests an underlying process of cell adhesion occurring in those locations, while a wider 6.25 hour spread in the T_i values corresponding to sensors 2 to 6 suggests an underlying process of cell proliferation. T_d values can be compared for sensors only within a group because of varying dynamic ranges across the three groups.

The growth curve of the cells growing over the sensor region can be assessed by monitoring the cumulative number of sensors that have recorded capacitance increases with respect to incubation time, denoted by CS . Fig. 4.14 shows such a plot as obtained using the 16 sensors monitored during the experiment. Note

that the initial rise between hours 6 and 8 indicates adhesion, while only the later changes during hours 10 to 18 can be attributed to proliferation. The total number of sensors that record capacitance increase in response to cell adhesion (N_a) is directly proportional to the initial number of cells that were seeded into the sensor well. The time required for the cumulative number of sensors that record capacitance increase in response to cell proliferation (N_p) to equal N_a (or $CS = 2N_a$), can be considered to be an estimate for the cell doubling time. The following analysis assumes that a homogeneous array of equally distributed sensors on the chip was exposed to a homogeneous cell suspension. The statistical accuracy of the doubling time estimate and the growth curve for the entire on-chip cell population improves with the total number of sensors that are monitored (N_t).

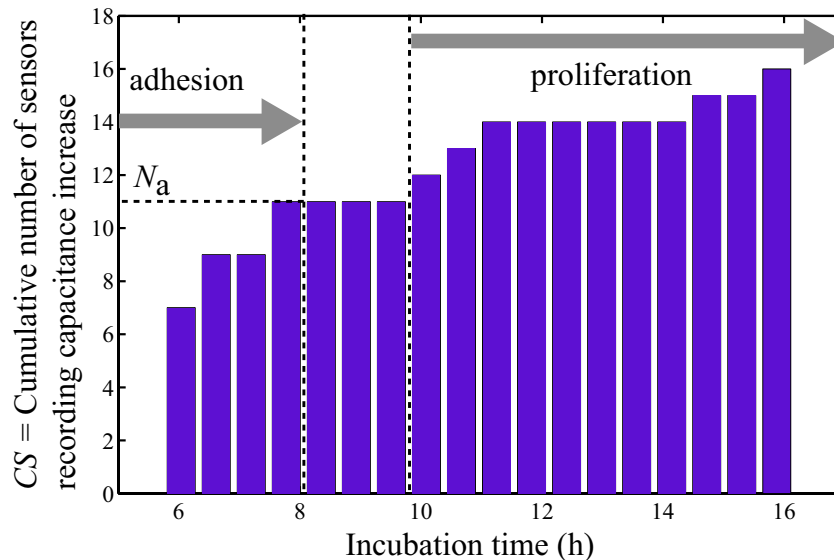


Figure 4.14: A plot of cumulative number of sensors that recorded capacitance increase (CS) vs. incubation time. A total of 16 sensors were monitored.

In the current experiment, a total of 16 sensors ($N_t = 16$) with different electrode sizes and inter-electrode distances were monitored. The $20 \times 20 \mu\text{m}^2$, 30×30

μm^2 and $40 \times 40 \mu\text{m}^2$ sensors have effective inter-electrode distances of $82 \mu\text{m}$, $79 \mu\text{m}$ and $88 \mu\text{m}$ respectively. For simplicity, we approximate the set of 16 monitored sensors to be a homogeneous array of equally distributed sensors with an average inter-electrode distance of $83 \mu\text{m}$ and an average electrode area of $30 \times 30 \mu\text{m}^2$. In Fig. 4.14, the value of N_a for this experiment was found to be 11 at the end of first 10 hours of incubation. At the end of the next 8 hours of incubation the remaining 5 sensors detected an increase in capacitance that was attributed to the proliferation process ($N_p = 5$). As a first order estimate, the rate of detecting capacitance increase (R) during the proliferation phase can be evaluated to be $5/8$ sensors/hour. Here R is representative of the proliferation rate of the cells growing over the small on-chip area that corresponds to the monitored sensor locations. Assuming homogeneous proliferation, it would require another 9.6 hours for $N_p = N_a = 11$. This projects a value of 27.6 hours for the cell doubling time as measured from the initial cell loading time $t = 0$ hr.

In order to measure the cell doubling time experimentally, the total number of sensors monitored (N_t) should be greater than or equal to twice the number of sensors detecting cell adhesion (N_a). If this condition is met, the time required for the number of sensors detecting cell proliferation (N_p) to equal N_a reflects the actual cell doubling time irrespective of whether the cells are undergoing symmetrical or asymmetrical cell divisions. In the current analysis, the assumption of homogeneous cell proliferation was used only to project a value for cell doubling time, since in this experiment $N_t (= 16) < 2N_a (= 22)$. Often cells proliferate asymmetrically, especially in the case of cancer cells which are not contact inhibited.

It should be noted that the above analysis is specific only to the cells growing over the monitored region confined to an area of $400 \times 400 \mu\text{m}^2$ (just 0.1% of the total sensor well area) where the sensors are located. The data obtained are not representative of the entire cell population in the sensor well. This is because cells growing at different locations in the sensor well (both on-chip and off-chip) might be proliferating at different rates depending upon their local microenvironment and their state in the cell division cycle. So the accuracy of this technique for quantifying proliferation of the entire on-chip cell population and estimating parameters such as cell doubling time can be significantly improved by increasing the number of monitored sensors.

4.5.4 Detecting cell detachment

In continuation with the previous experiment with the MDA-MB-231 cells, after the 18 hour monitoring period the cells were treated with 0.25% Trypsin/EDTA and the sensor chip was monitored for the next 4 hours. It was found that all the sensors recorded a decreased capacitance after treatment with trypsin which indicates cell detachment from the chip surface. Fig. 4.15 shows sample capacitance plots as recorded by 2 of the sensors before and after trypsinization. Table 4.2 displays the capacitance drop values as recorded by the 16 monitored sensors.

This further confirms the fact that cells were coupled to the chip surface at all monitored sensor locations prior to trypsinization. From Table 4.2 it can be seen that for some of the sensors, the capacitance drop values were greater than

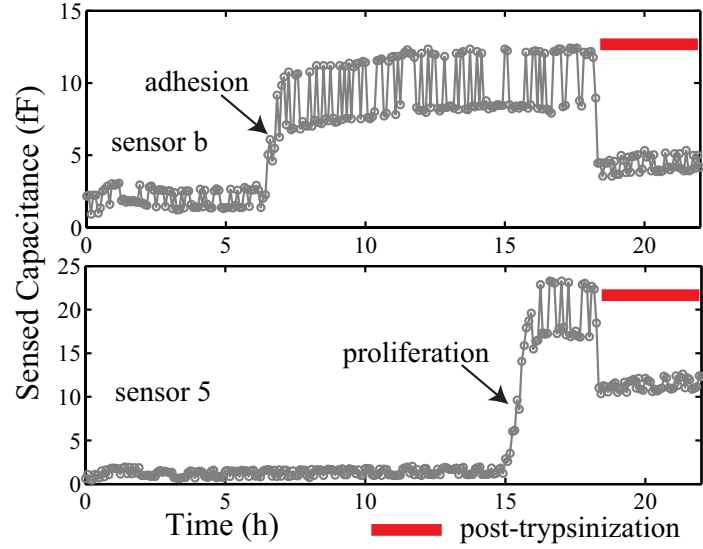


Figure 4.15: Sample capacitance plots showing sensor response to MDA-MB-231 cell detachment upon trypsinization; sensors b and 5 correspond to the same 2 sensors referred to in Figs. 4.12 and 4.13 respectively.

Table 4.2: Capacitance drop values ΔC_{drop} recorded by the three sensor groups after trypsinization

$20 \times 20 \mu\text{m}^2$ sensors	$30 \times 30 \mu\text{m}^2$ sensors	$40 \times 40 \mu\text{m}^2$ sensors
ΔC_{drop} (fF)	ΔC_{drop} (fF)	ΔC_{drop} (fF)
4.26	5.34	10.87
4.51	7.03	11.21
4.85	5.42	11.55
7.26	5.80	9.49
5.44	5.42	8.70
*	*	8.47

the capacitance rise values in Table 4.1. This is because those sensors recorded a gradual increase in the time averaged capacitance during the interval between the capacitance rise and fall. Also, the sensed capacitances do not return to their initial pre-adhesion levels after trypsinization. This could possibly be due to the residual

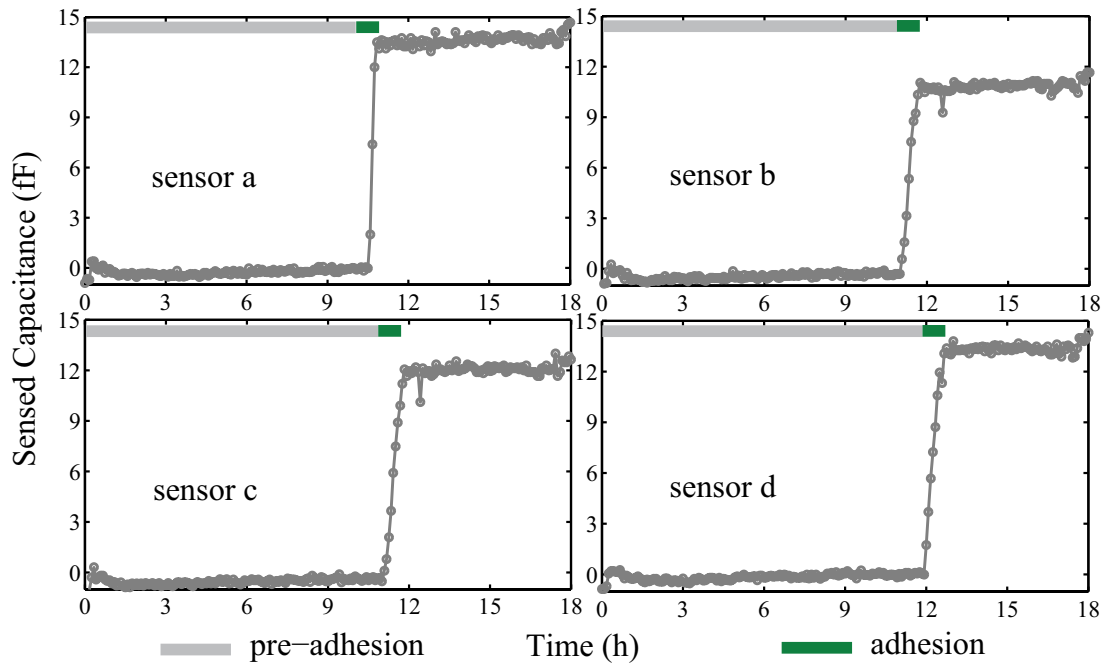


Figure 4.16: Capacitance sensor response to adhesion of human colonic adenocarcinoma cells (Caco-2) on the chip surface. All sensors measure $30 \times 30 \mu\text{m}^2$. Cell density employed for the experiment $\approx 1 \times 10^6$ cells/mL.

materials that are deposited onto the chip surface by the cells.

4.5.5 Notes on experiments characterizing capacitance sensor response to cell phenomena

4.5.5.1 Repeatability, reusability and control experiments

The proximity sensitivity of the capacitance sensors along with the shielding effect of the growth medium produce responses to phenomena occurring only on the chip surface. The sensor chip has been tested with bovine aortic smooth muscle cells (BAOSMC) [17–20], human breast cancer cells [21] and human colonic adenocarcinoma cells (Caco-2) (see Fig. 4.16). The sensor response to adhesion of cells on

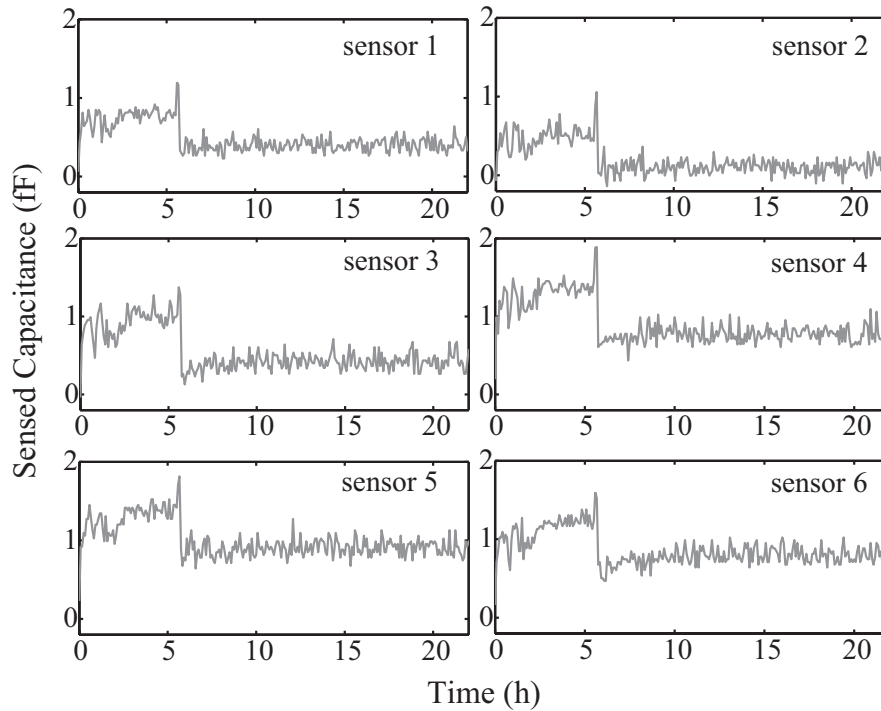


Figure 4.17: Capacitance sensor response with sensor well loaded with growth medium alone, without any cells. Sensors 1 and 2 measure $40 \times 40 \mu\text{m}^2$, sensors 3 and 4 measure $30 \times 30 \mu\text{m}^2$, sensors 5 and 6 measure $20 \times 20 \mu\text{m}^2$.

the chip surface has been consistent among the different cell types. In control experiments involving monitoring of chips without cells inside the incubator, with the sensor well containing the growth medium alone, and in actual experiments wherein it was found that there were no cells coupled to the chip surface, the sensors did not show any capacitance increase. For example, Fig. 4.17 shows sample sensor responses from a control experiment in which the sensors were monitored with growth medium alone for a period of 22 hours inside an incubator. As can be seen, the sensed capacitance values remained below 1.5 fF throughout the monitoring period. The sensor responses exhibiting distinct capacitance risings as is shown in Figs. 4.8, 4.10, 4.11, 4.12, 4.13, 4.16 are characteristic of only the experiments in which the cells were present on the chip surface.

Cell culture on the chip results in strongly attached surface residues which greatly influence baseline capacitance readings. Chip reusability for integrated cell capacitance sensing requires thorough cleaning of the chip surface and also a reliable biocompatible package. The packaging technique using the photopatternable polymer that has been employed in this work has been found to be reliable for a maximum period of only four days. Alternate packaging strategies [by Dr. E. Smela, M.P. Dandin, M. Piyasena] for long-term reliability and chip surface cleaning solutions [by Dr. P. Abshire] are currently being explored for enabling chip reusability.

4.5.5.2 Capacitance fluctuations

In most of the experiments described previously, the sensed capacitances exhibited non-periodic fluctuations before and after the adhesion phase (see Figs. 4.8, 4.10, 4.11, 4.12, 4.13 and 4.15). These fluctuations were evaluated under different conditions for the three sensor groups; Table 4.3 summarizes the standard deviations (σ_{40} , σ_{30} and σ_{20}) as computed from measurements obtained in one of the experiments. The fluctuations in response to cells after adhesion are 1-2 orders of magnitude higher than when the sensors were exposed to just growth medium or air. Such fluctuations were consistently observed in the presence of cells. This has been attributed to increased capacitive crosstalk between the metal interconnects and the sensing node (node in the sensor circuit to which the sensing electrode is connected to in Fig. 4.1), due to increased dielectric constant of the passivation layer surface after cell adhesion. The sensing node during the evaluation phase is a

high impedance node and is therefore susceptible to interference noise coupling.

The origin of the interfering noise responsible for the non-periodic fluctuations in the capacitance recordings was traced back to the data acquisition card that was used to generate the clock signal for the sensor operation. This noise has now been eliminated by employing a clean clock signal generated using a function generator. Fig. 4.16 shows capacitance traces with significantly reduced noise that were obtained in response to adhesion of Caco-2 cells on the chip surface.

Table 4.3: Standard deviations of capacitance fluctuations

Stimulus	σ_{40} (fF)	σ_{30} (fF)	σ_{20} (fF)
air	0.067	0.085	0.091
growth medium without cells	0.164	0.361	0.314
cell culture (pre-adhesion)	0.344	0.798	0.745
cell culture (post-adhesion)	3.463	2.454	2.511

4.5.5.3 Influence of biocompatible chip package on baseline capacitance

The baseline capacitance readings have always been sensitive to the employed packaging technique and the packaging material. For example, the baseline capacitances recorded at the start of the experiments presented in sections 4.5.1.1 and 4.5.2.1 were much higher than in the remaining experiments. This is because the material employed for packaging the chips in these experiments was not photopatternable, so they had to be manually patterned which resulted in residues on the

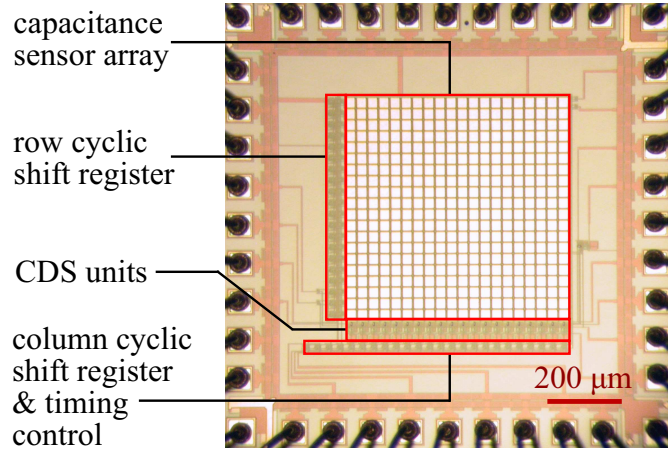


Figure 4.18: Photograph of the fabricated capacitance imager chip.

chip surface (see Figs. 4.7, 4.9). In the remaining experiments, chips packaged using the photopatternable polymer were employed, which resulted in much cleaner chip surfaces and low baseline capacitance readings (see Figs. 4.8, 4.10, 4.11, 4.12, 4.13 and 4.15).

4.6 A capacitance imager chip based on the first generation sensor

A capacitance imager test chip incorporating the first generation sensors in an array format was designed and fabricated. Fig. 4.18 shows a photograph of the fabricated chip. This is a tiny chip measuring an area of $1.5 \times 1.5 \text{ mm}^2$ and comprising an array of 400 sensors with a sensing electrode area of $30 \times 30 \text{ }\mu\text{m}^2$. In addition to the sensor array the chip also comprised row and column cyclic shift registers for addressing the sensor pixels. All sensor pixels in a column are multiplexed onto a common column line by incorporating a *rowselect* switch in the sensor circuit output buffer. Below every sensor column is placed a CDS unit for readout. Fig. 4.19(a) shows a schematic of the CDS unit [74]. The purpose of the

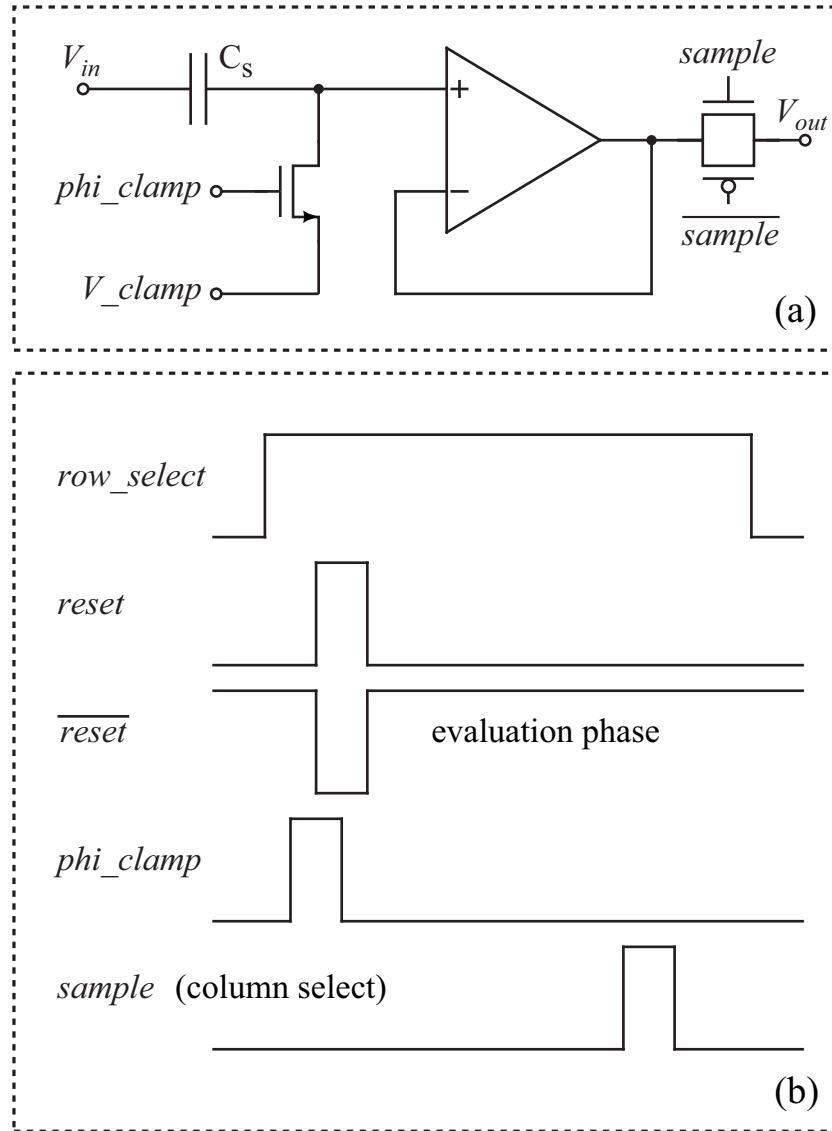


Figure 4.19: (a) Schematic of the Correlated Double Sampling (CDS) unit shared by a column of sensor pixels. (b) Timing diagram showing the control signals for sensing and readout. The signals $reset$ and \overline{reset} are the same as shown in Fig. 4.1 that control the sensor operation.

CDS unit is to subtract the evaluated output voltage from reset output voltage so that only the difference between the two is measured instead of the absolute value of the evaluated signal. This cancels DC offset errors in the readout path and also reduces low frequency correlated noise. The imager follows a row-wise select and a column-wise readout architecture. Fig. 4.19(b) shows the timing relation between

all the control signals responsible for the sensor operation and pixel readout.

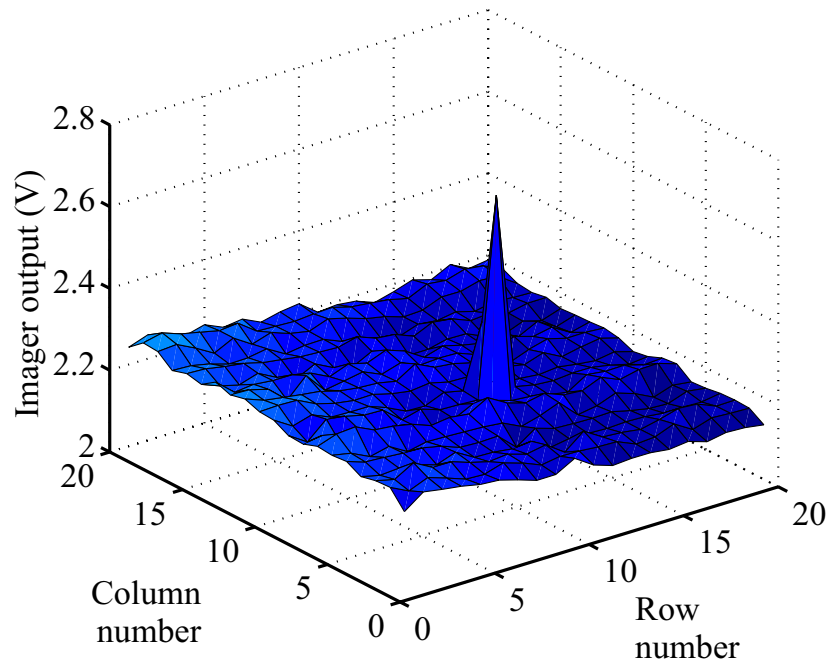


Figure 4.20: Imager output representing the capacitance profile of a metal probe placed in contact with the chip surface.

The imager chip was bench tested by placing a metal electrode on the chip surface using a piezoelectric micropositioner. All the timing signals were generated using a SX microcontroller. Fig. 4.20 shows the imager output representing the capacitance profile of the metal probe tip.

4.7 Summary

A first generation CMOS capacitance sensor chip was designed to measure cell-substrate capacitance, a sensing modality that can be employed for on-chip investigation of cell phenomena. Biophysical factors contributing to the sensed capacitance were identified and discussed. Three groups of sensors with electrodes of different sizes were bench tested for calibration of the relationship between ca-

capacitance and measured voltage. *In vitro* test results from experiments with bovine heart muscle cells, human breast cancer cells and human intestinal cells showed that the sensors are able to detect cell-substrate capacitive variations in the fF range, with different sensing ranges for the three sensor groups. Results from the online monitoring experiments showed that the sensors were effective in tracking cell adhesion, variations in cell viability and cell growth. Sensor response to changes in cell viability was validated by establishing good correlation between on-chip measurements of cell-substrate capacitance and concurrent assessments involving Neutral Red dye retention test and Alamar Blue dye reduction measurements.

The CMOS-based integrated cell capacitance sensing technique demonstrated here offers an important monitoring capability for the development of cell-based miniaturized systems [75, 76]. Such systems can be employed for a wide spectrum of applications including medical diagnosis, cytotoxicity assessment, drug screening and biocompatibility characterization.

Chapter 5

Second generation fully differential rail-to-rail capacitance sensors for improved performance

5.1 Motivation for a fully differential sensor

The performance of the first generation single-ended sensors for cell capacitance measurement was limited by the parasitic effects resulting from the growth environment and the sensor itself. The main contributors to such parasitics include stray capacitances (C_{stray}) from the measurement circuit (this includes the parasitic capacitances associated with the transistors and interconnects) and the standing capacitances ($C_{standing}$) of the sensing electrodes along with the cell environment. In other words, sensor sensitivity and dynamic range (defined as the ratio of the total signal swing to the noise resolution) were limited by the magnitude of the nodal parasitic capacitances C_{N1} and C_{N2} shown in Fig. 4.1. Also as mentioned in the previous chapter, the baseline capacitances were greatly influenced by the residual packaging material on the chip surface which forms a part of the on-chip cell environment. From a futuristic perspective, when this sensor will be incorporated in lab-on-chip (LOC) systems like cell clinics, the standing capacitances of the microstructures will also contribute to the sensing node capacitance causing a significant capacitive offset at the input [25], thereby further reducing the sensor

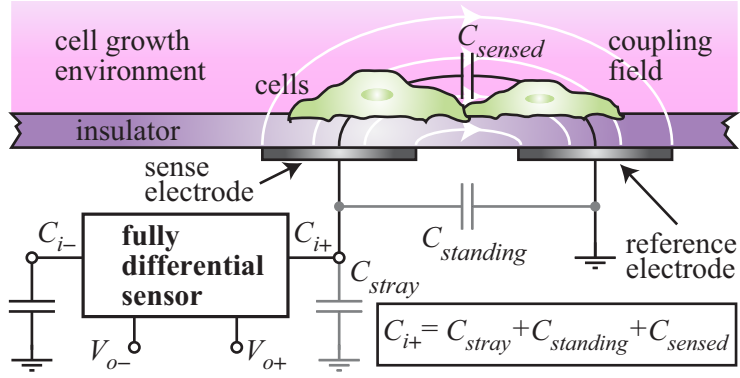


Figure 5.1: Fully differential sensor block diagram and associated capacitances.

dynamic range.

The first generation single-ended capacitance sensor described in the previous chapter is based on the charge sharing principle [20]. The sensing node (node N1 in Fig. 4.1) in the measurement circuit is held in a high impedance state during readout (evaluation phase) which makes it susceptible to interference noise coupling. In addition to this, the presence of an aqueous ionic medium above the chip surface further increases capacitive crosstalk with the sensing node (see Section 4.5.5.2).

A fully differential sensor can resolve the above mentioned problems concerning parasitic capacitance effects and interference noise coupling arising in single-ended sensors. Fig. 5.1 shows a block diagram representation of the fully differential sensor along with the associated capacitances. C_{i-} and C_{i+} represent the input nodal capacitances. The differential input capacitance is given by:

$$\Delta C_i = C_{i+} - C_{i-} \quad (5.1)$$

In this discussion the cell sensing electrode and hence the sensed capacitance (C_{sensed}) will always be connected to node C_{i+} . Thus the total capacitance at node C_{i+} is

the sum of C_{stray} , $C_{standing}$ and C_{sensed} as shown in Fig. 5.1. The capacitance at node C_{i-} depends upon the capacitance compensation scheme implemented by the sensor as discussed below. Under ideally matched conditions, a linear differential sensor eliminates effects of C_{stray} and $C_{standing}$ on the sensor response. Differential readout further improves sensor resolution by suppressing correlated noise and also increasing the output dynamic range.

5.2 Implementable capacitance compensation schemes

A differential capacitance sensor can be configured to follow different compensation schemes depending upon the application. The success of these schemes relies on matching between the various sensor components. In all the schemes discussed below, the capacitance at node C_{i+} is as shown in Fig. 5.1.

5.2.1 Stray capacitance compensation scheme

In this scheme node C_{i-} is left unconnected, compensating for C_{stray} alone [27].

$$C_{i-} = C_{stray} \Rightarrow \Delta C_i = C_{standing} + C_{sensed} \quad (5.2)$$

This reduces sensor dynamic range as $C_{standing}$ at node C_{i+} results in a positive capacitive offset at the input. This scheme can be employed in array-based applications for cell detection where sensor dynamic range is not a critical requirement.

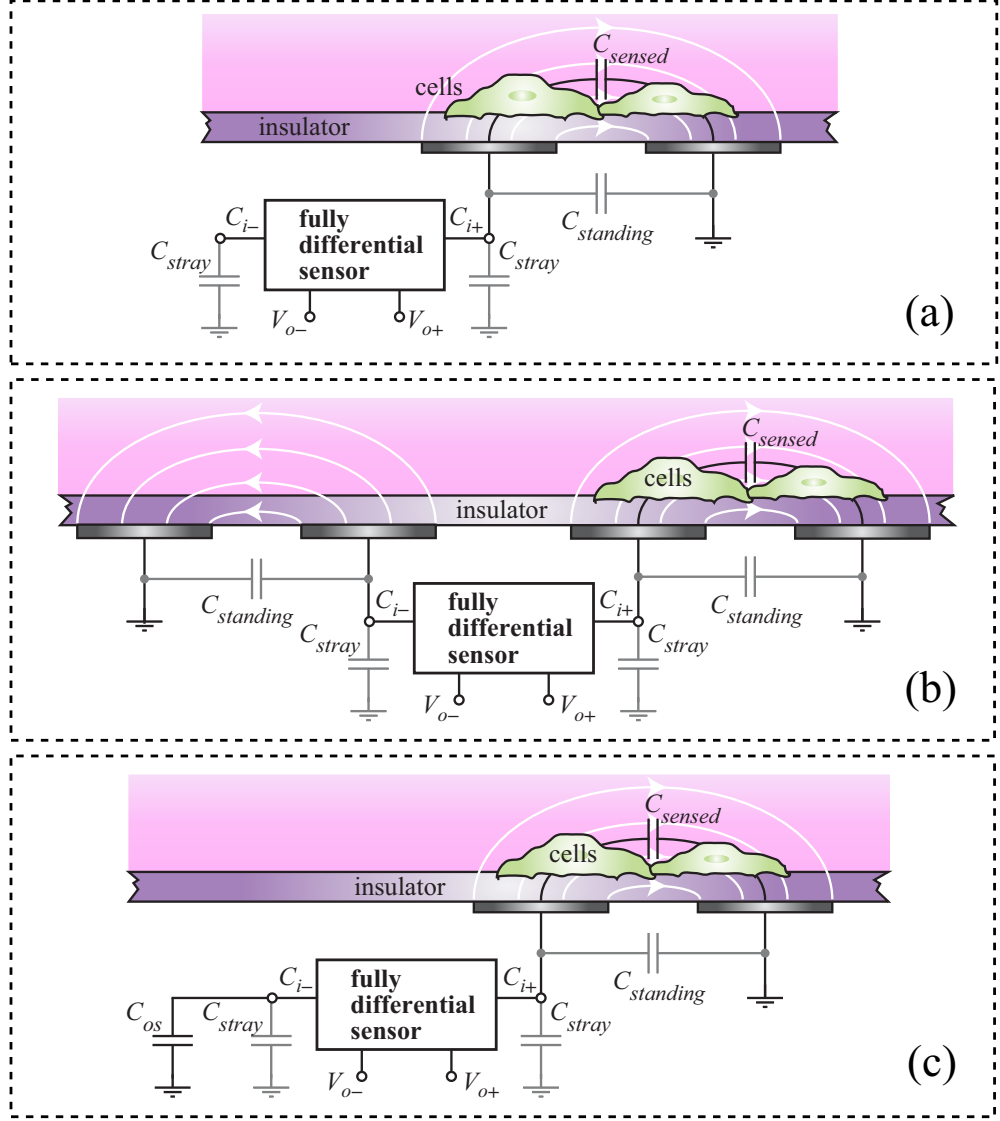


Figure 5.2: Implementable capacitance compensation schemes: (a) stray capacitance compensation scheme, (b) standing capacitance compensation scheme and (c) standing capacitance overcompensation scheme.

5.2.2 Standing capacitance compensation scheme

In this scheme identical sensing electrodes are attached to both C_{i+} and C_{i-} nodes [27].

$$C_{i-} = C_{stray} + C_{standing} \Rightarrow \Delta C_i = C_{sensed} \quad (5.3)$$

This compensates for both C_{stray} and $C_{standing}$. Replication of microstructures in

LOC systems along with the sensing electrodes also compensates for standing capacitances arising from them. In conjunction with a high gain measurement circuit, this can enable very sensitive cellular measurements for applications like on-chip cytometry. The sensor dynamic range is higher than in the previous case.

5.2.3 Standing capacitance overcompensation scheme

Instead of replicating sensing structures at both the input nodes, an offsetting capacitor C_{os} can be attached to node C_{i-} . $C_{os} > C_{standing}$ results in a negative capacitive offset at the input.

$$C_{i-} = C_{stray} + C_{os} \Rightarrow \Delta C_i = C_{sensed} + C_{standing} - C_{os} \quad (5.4)$$

The value of C_{os} should be chosen such that $C_{os} - C_{standing}$ is within the sensor input range. C_{os} can be formed by one of the inter-layer capacitances that offers best possible matching in the low fF range. This scheme allows for an even higher dynamic range compared to the previous two schemes. Also, by choosing an appropriate value for C_{os} , the sensor can be made to operate in its mid-range where the sensor exhibits maximum linearity. This can be useful for applications where dynamic range and linearity requirements are critical. For example, cell viability monitoring requires larger area sensing electrodes which offer a wider input capacitance range. In such applications, capacitance variations can signal important cell-related responses.

5.3 Fully differential rail-to-rail capacitance sensor: design and operation

Over the last decade, the charge based capacitance measurement (CBCM) technique has evolved as a popular sensing approach for measuring fF capacitances with aF resolution. The CBCM approach was primarily developed for interconnect capacitance characterization over a decade ago [45]. Since then it has been employed in several other applications including measurement of MOS device C-V characteristics [77], particle detection for industrial and biomedical purposes [24–27], and DNA sensing [78].

This work presents a sensor design tailored for on-chip cell monitoring which requires the circuit to measure capacitances over a few 10's of fFs [20–22]. It extends previously reported CBCM circuits with single-ended output configurations [24–27] to a differential output architecture. The fully differential measurement circuit compensates for parasitic capacitances associated with on-chip cell sensing, increases sensor dynamic range, and suppresses correlated noise for improved assessment of cell phenomena [22,23]. The sensor circuit presented here employs a 3-phase clocking scheme that allows for gain tuning in accordance with the conditions in a particular cell sensing application. These conditions include sensing electrode areas and configurations, and the dielectric parameters of the cell-substrate interface and the growth medium.

Fig. 5.3 shows a schematic of the capacitance measurement circuit. It comprises a standard CBCM front-end (M1-M4), a pair of complementary current mir-

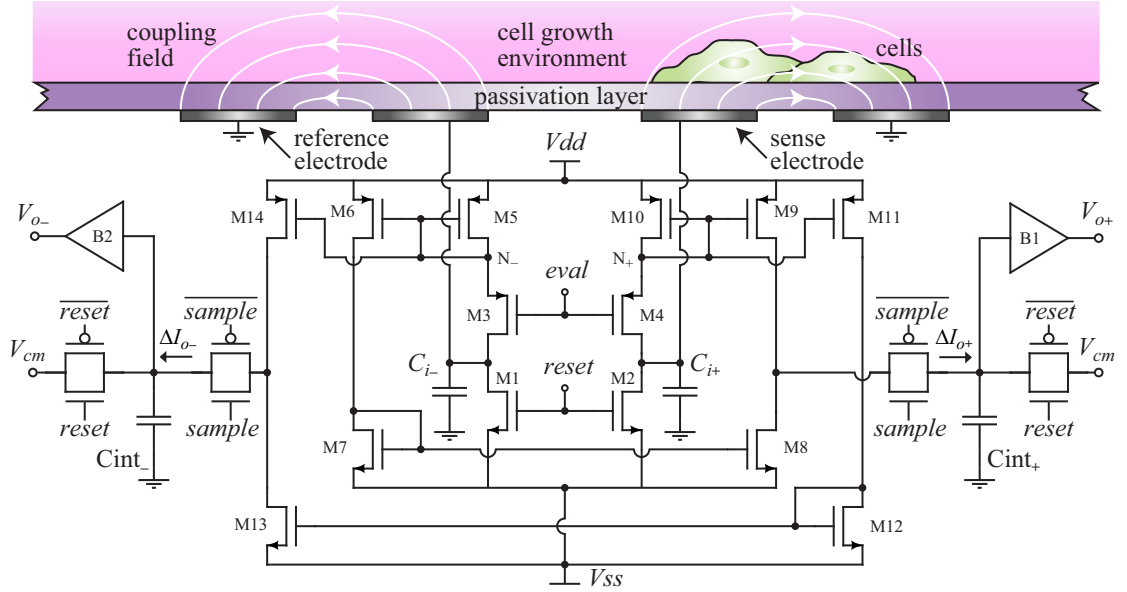


Figure 5.3: Fully differential rail-to-rail capacitance measurement circuit design with sensor configured for standing capacitance compensation.

rors (M5-M8 and M10-M13), current subtractors (M8-M9 and M13-M14), integration capacitors (C_{int-} and C_{int+}) and rail-to-rail readout buffer amplifiers (B1 and B2).

The CBCM unit comprises two identical pairs of minimum size NMOS and PMOS transistors (M1,M3) and (M2,M4), that are switched using two non-overlapping clock signals *reset* and *eval*. The sensing operation proceeds in three phases: reset, evaluation and sample. Fig. 5.4 shows the timing control signals corresponding to the three phases and the sensor response waveforms. During reset, C_{i-} and C_{i+} are discharged to V_{ss} through M1 and M2, and C_{int-} and C_{int+} are reset to the common-mode voltage V_{cm} . During evaluation, C_{i-} and C_{i+} are charged to $V_{dd} - |V_{thp}|$ through M3 and M4, where V_{thp} refers to the PMOS threshold voltage.

The average values of the charging currents I_{c-} and I_{c+} can be expressed as:

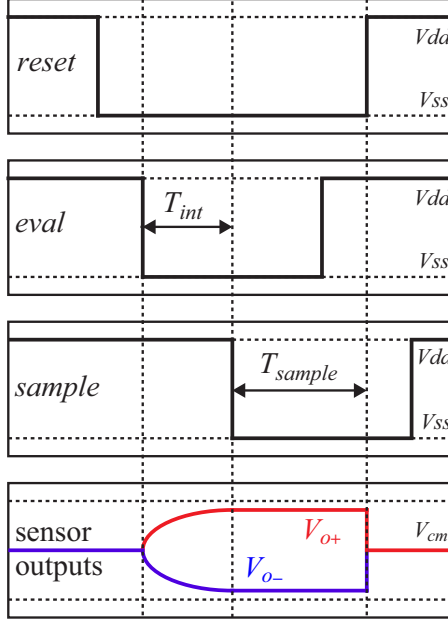


Figure 5.4: Timing diagram illustrating the relation between the clock phases and sensor outputs.

$$\bar{I}_{c\pm} = C_{i\pm} \cdot V_{step} \cdot f \quad (5.5)$$

where $V_{step} = V_{dd} - V_{ss} - |V_{thp}|$ and $f = 1/T$ is the sensing cycle frequency. I_{c-} and I_{c+} are amplified by the current mirrors M5-M8 and M10-M13 with gain A_c and then subtracted by the transistors M8-M9 and M13-M14 to yield complementary difference currents ΔI_{o+} and ΔI_{o-} , whose average values can be expressed as:

$$\overline{\Delta I_{o\pm}} = \pm A_c \cdot \Delta C_i \cdot V_{step} \cdot f + I_{os\pm} \quad (5.6)$$

where I_{os-} and I_{os+} are the offset currents in the current subtractors. C_{int-} and C_{int+} then integrate ΔI_{o-} and ΔI_{o+} over a period T_{int} that is determined by the time interval between the negative edges of $eval$ and $sample$ (see Fig. 5.4) to yield sensor output voltages V_{o-} and V_{o+} . Here $sample$ is a variable delay pulse that allows

for varying T_{int} . If the current pulses $\Delta I_{o\pm}$ are approximated to be ideal pulses of amplitudes $\overline{\Delta I}_{o\pm}$ and widths T_{pw} such that the total charge delivered/removed to/from the integration capacitors remains the same, the sensor output voltages can be expressed as:

$$V_{o\pm} = \frac{1}{C_{int}} \cdot \int_0^{T_{int}} \Delta I_{o\pm} dt + V_{cm} \approx \pm A_c \cdot V_{step} \cdot \frac{T_{int}}{T_{pw}} \cdot \frac{\Delta C_i}{C_{int}} + V_{os\pm} + V_{cm} \quad (5.7)$$

where $T_{int} \leq T_{pw}$, C_{int} is the value of the integration capacitance, and V_{os-} and V_{os+} are the offset voltages from integration of I_{os-} and I_{os+} . The differential output voltage ΔV_o is given by:

$$\Delta V_o = V_{o+} - V_{o-} \approx 2 \cdot A_c \cdot V_{step} \cdot \frac{T_{int}}{T_{pw}} \cdot \frac{\Delta C_i}{C_{int}} + \Delta V_{os} \quad (5.8)$$

where $\Delta V_{os} = V_{os+} - V_{os-}$. Under ideal conditions when both sides of the differential sensor are perfectly matched $\Delta V_{os} = 0$. In reality, $\Delta V_{os} \neq 0$ due to device mismatch effects. From (5.8), T_{int} being variable allows for gain tuning. The relation between the sensor gain and T_{int} is actually nonlinear because ΔI_{o-} and ΔI_{o+} are transient current pulses and not ideal rectangular pulses as considered above. The *sample* pulse also limits the sensor output voltage offsets by limiting the durations over which I_{os-} and I_{os+} are integrated. The sensor output is finally buffered by a pair of rail-to-rail buffer amplifiers B1 and B2, the details of which are presented in the later sections.

5.4 Shielded current routing bus architectures for implementing differential capacitance sensor arrays

In order to achieve high density, sensor arrays require a small on-chip footprint for the measurement circuit. The area of the sensor circuit presented here can be significant because of the large device sizes necessary for improved matching and for incorporation of additional calibration circuitry. In order to realize differential sensor arrays, we have developed a current routing bus architecture. Fig. 5.5 illustrates a column parallel array architecture along side the pixel circuit and the timing diagram.

In this architecture each sensor pixel comprises four minimum size digital transistors (M1-M4). In Fig. 5.3 nodes N_- and N_+ connect the CBCM unit to the rest of the circuit, referred to as the sensor evaluation module (SEM). In Fig. 5.5 nodes N_- and N_+ extend to form current bus lines that allow a column of CBCM pixel units to share a common SEM comprising the complementary current mirrors, subtractors, integration capacitors and output buffers. The timing diagram shown is for a row-wise select and a column-wise readout addressing scheme. Here *row select* and *sample* are active low, and *reset* is active high. All pixels are reset globally in every clock cycle. In order to address a particular row of pixels for sensing, its corresponding *row select* goes low enabling all sensors in the row for evaluation. The sampling of the SEM output is triggered by the negative edge of the *sample* signal.

In a large sensor array implementing this architecture, the bus-to-substrate capacitances of the current bus lines and the source-to-bulk junction capacitances

C_{sb} 's of transistors M3 and M4 in the sensor pixel contribute to the parasitic capacitances at the nodes N_- and N_+ . All these capacitances can sum up to 100's of fF which degrades sensor evaluation speed. Also, the source-to-bulk junctions contribute to leakage currents from the current bus. For this purpose a larger area metal shield fabricated in a lower metal layer can be used for isolating the bus line from the substrate as shown in Fig. 5.5. The effect of the bus-to-shield capacitance, the C_{sb} 's and the source-to-bulk junction leakage are canceled out by driving the shield line and the N-wells of transistors M3 and M4 in each pixel with a potential that tracks the bus line potential. This is achieved using the buffer amplifiers B3 and B4 as shown in Fig. 5.5. This requires transistors M3 and M4 to be placed in individual N-wells. Such shielding also improves immunity of the current bus to substrate noise. In technologies with many metal layers the bus lines can be shielded from both top and bottom.

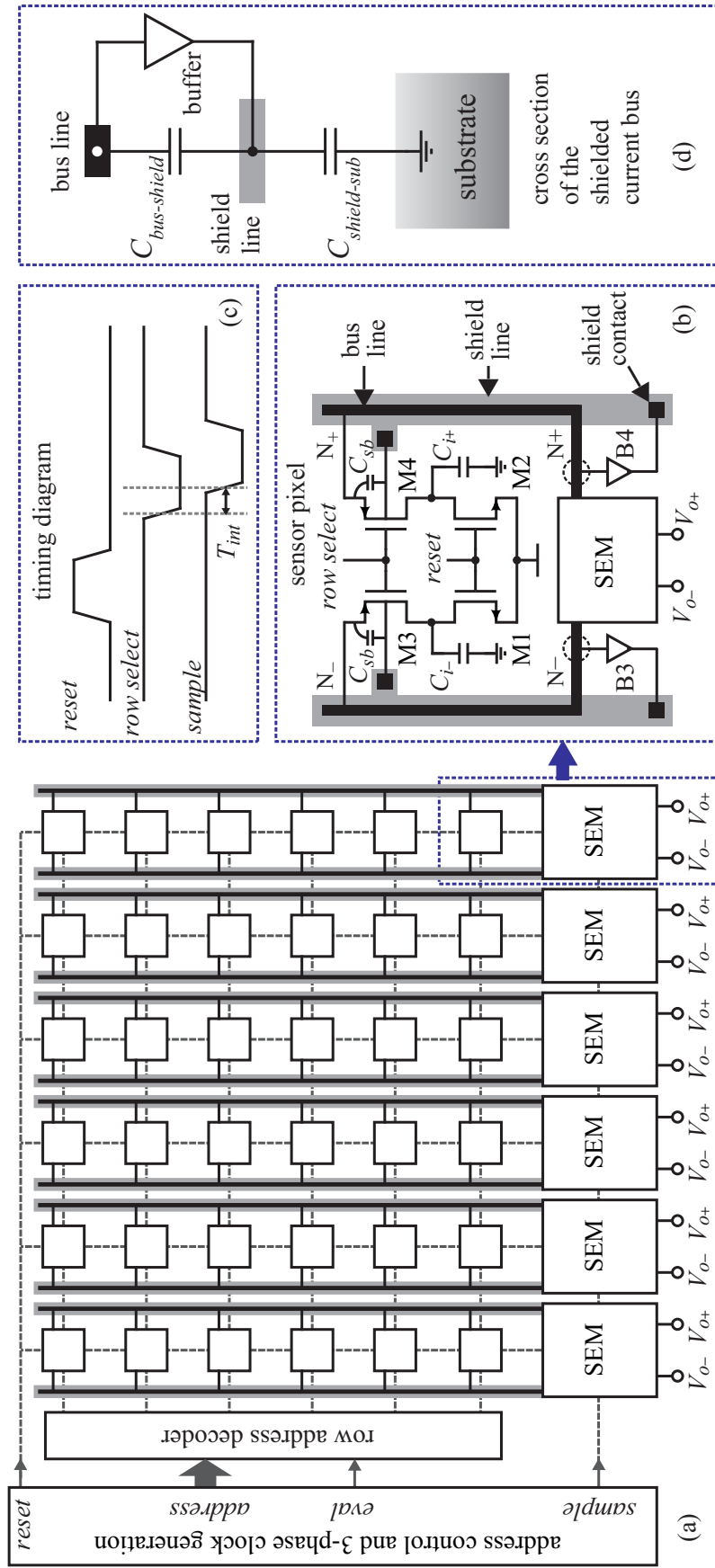


Figure 5.5: A fully differential capacitance sensor array with a column parallel architecture based on a shielded current routing bus. (b) Schematic of the sensor pixel. (c) Timing diagram for pixel readout. (d) Horizontal view of the shielded current bus.

It is important to note that the input capacitances of the buffer amplifiers B3 and B4 used to drive the shield lines of the current bus, add on to the nodes N_- and N_+ in the capacitance measurement circuit. So the evaluation speed of a sensor incorporated in an array employing a shielded current routing bus will always be lower than that of an individual sensor. The advantages of the shielded current routing bus in terms of conserving the sensor evaluation speed and guarding the bus against leakage will be more prominent in a high density large sensor array, wherein the summation of all the parasitic capacitances associated with the current bus exceeds the value of the buffer input capacitance.

The column parallel array architecture although achieves a high spatial resolution of just four minimum sized digital transistors in every pixel, requires an entire row of SEM modules to be calibrated. The column parallel architecture also poses the challenge of pitch-matching the layout of the SEM module (along with additional calibration circuitry if incorporated) with the layout of a very narrow column of sensor pixels in a high density array scenario. An alternate solution to the problem of incorporating the measurement circuit in a sensor array is to multiplex the entire two dimensional array of pixels onto a single SEM module. This simplifies array calibration and eliminates the challenge of layout pitch-matching, but at the cost of increasing the sensor pixel foot-print and decreasing the array readout speed. Fig. 5.6 illustrates the single SEM sensor array architecture alongside the pixel circuit and the timing diagram.

In this architecture each sensor pixel comprises six minimum size digital transistors (M1-M4, M3', M4'). In Fig. 5.6 nodes N_- and N_+ extend to form current

bus lines that allow an entire array of CBCM pixel units to share a common SEM. The timing diagram shown is for a row-wise select and a column-wise readout addressing scheme. Here *row select*, *column select* and *sample* are active low, and *reset* is active high. All pixels are reset globally in every clock cycle. In order to address a particular pixel for sensing, its corresponding *row select* first goes low followed by the *column select* enabling the sensor for evaluation. The sampling of the SEM output is triggered by the negative edge of the *sample* signal. The current bus is shielded in the same way as described in the column parallel architecture case.

High density sensor arrays with reduced electrode areas will require thinning of the chip passivation layer in order to improve input signal strength and dynamic range. Capacitance sensor arrays can achieve fill factors (the fraction of surface area covered with sensors) over 90% in advanced CMOS processes with more metal layers since the active elements comprising the measurement circuit can be placed directly underneath the sensing electrodes. Such high density capacitance imager chips can generate a time sequence of capacitance “images” providing more insight into the on-chip cell behavior. Such maps can be used to track the adhesion and growth processes of cells cultured on-chip by 1) monitoring the time-varying signals recorded from sensors that become covered as the cells adhere and show a spreading behavior [20,21] and 2) tracking the cumulative number of sensors that are coupled to cells over time [21].

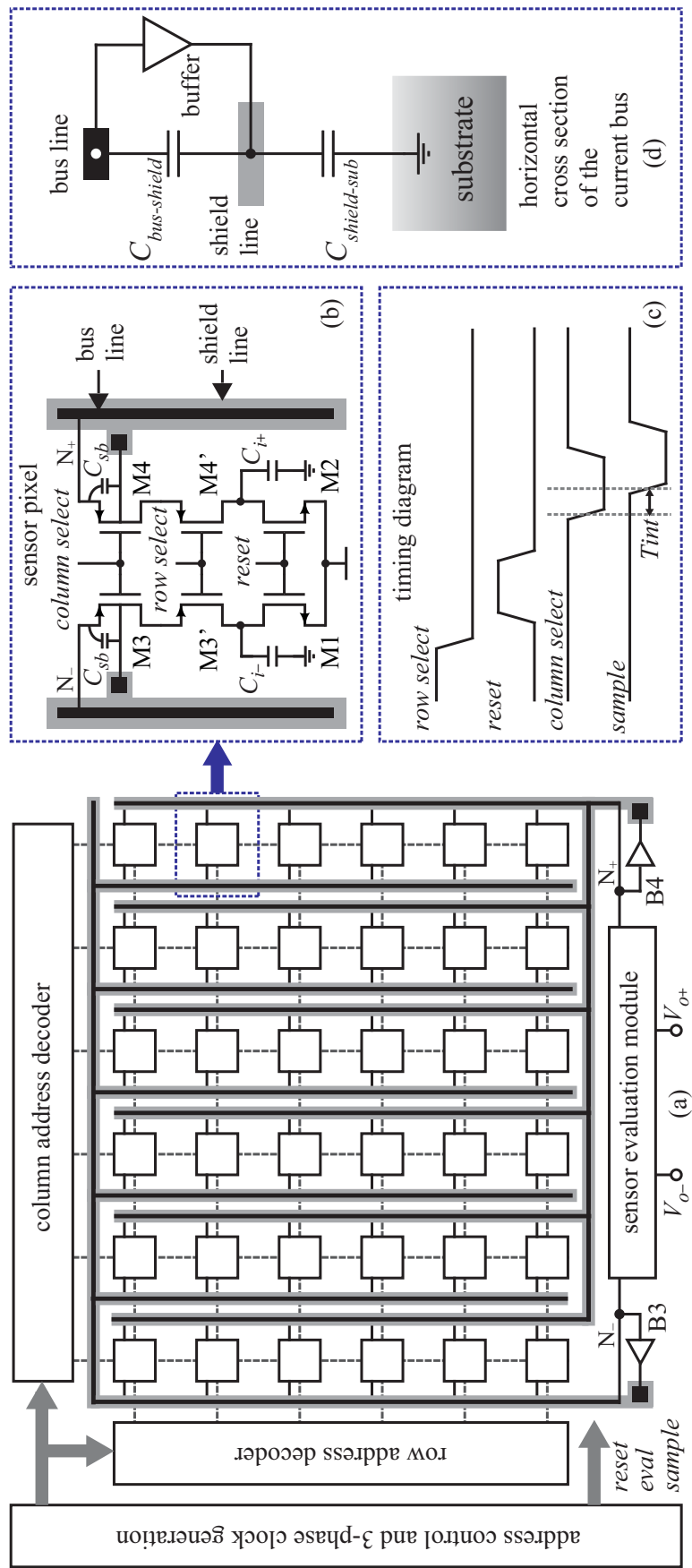


Figure 5.6: A fully differential capacitance sensor array with a single SEM architecture based on a shielded current routing bus. (b) Schematic of the sensor pixel. (c) Timing diagram for pixel readout. (d) Horizontal view of the shielded current bus.

5.5 Test chip version 1: Individual sensor characterization

5.5.1 Sensor design and simulation

The sensor circuit as shown in Fig. 5.3 was designed in a $0.5\ \mu\text{m}$, 2-poly, 3-metal standard CMOS technology for operation with a 3 V supply. The circuit was designed and laid out with a mirror gain $A_c = 8$. A base transistor (M5 and M10 in Fig. 5.3) size of width $1.75\ \mu\text{m}$ and length $1.75\ \mu\text{m}$ was chosen for the design. The sensor output was buffered by a pair of rail-to-rail operational amplifiers connected in voltage follower configuration. The custom rail-to-rail op-amp was designed using the topology shown in Fig. 5.7. It consists of a rail-to-rail input stage, a summing circuit, and a rail-to-rail output stage with feedforward class-AB control [79]. The op-amp design and operation will be discussed in Chapter 7.

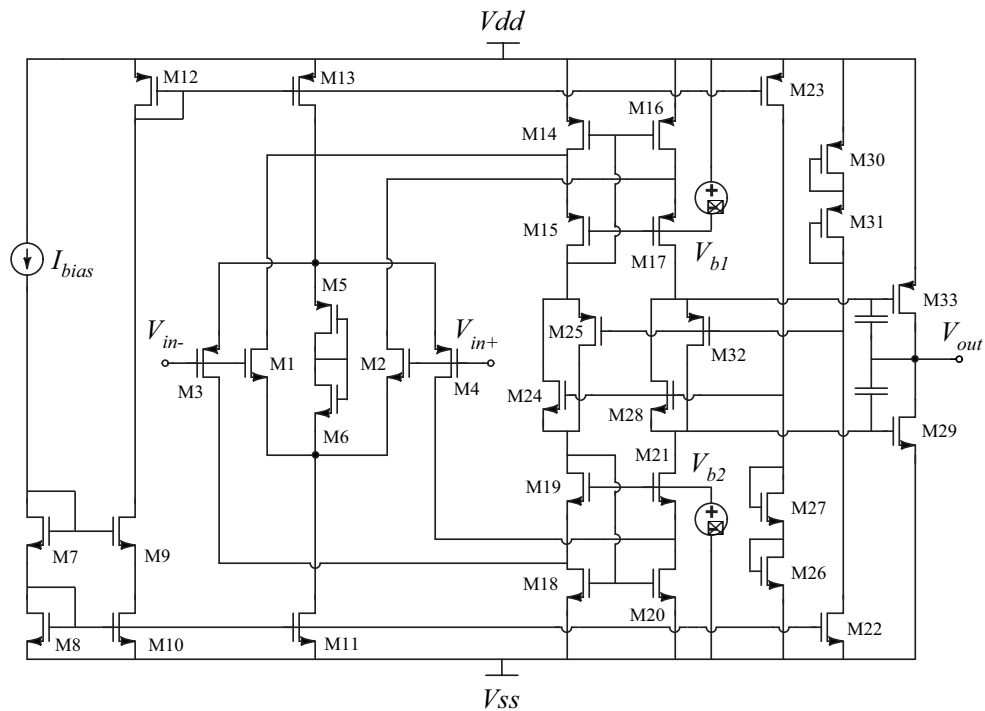


Figure 5.7: The custom wide-swing op-amp used for buffering the sensor output.

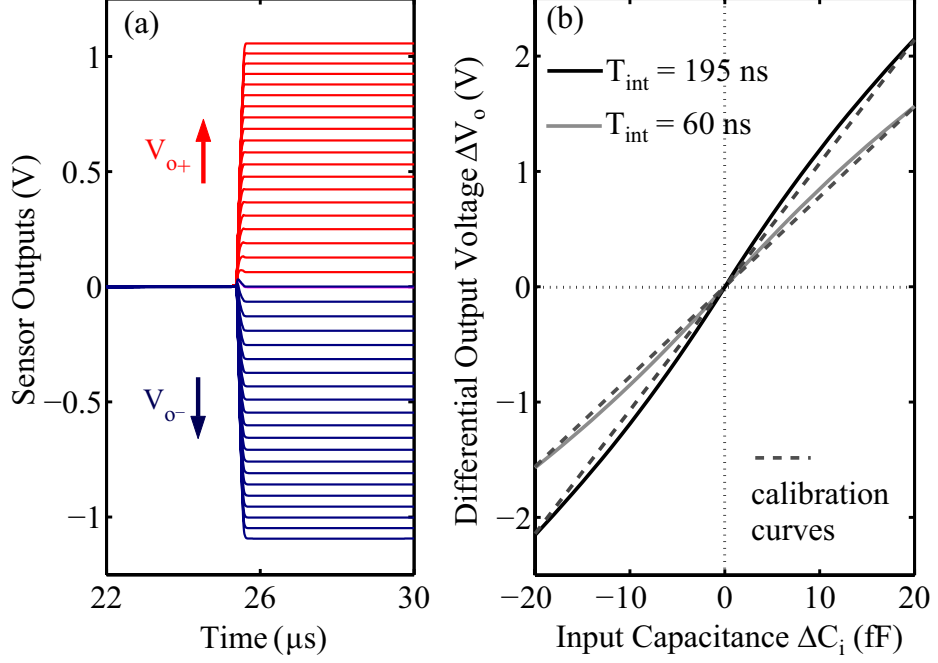


Figure 5.8: (a) Simulated transient response of the differential sensor for ΔC_i between 0 and 20 fF. (b) Simulated sensor static response curves with corresponding calibration curves for $T_{int} = 60$ ns and 195 ns.

The extracted layout was simulated using Cadence Spectre for an input capacitance range of ± 20 fF. Input standing capacitances were assumed to be 10 fF. A sensing cycle period of 10 μ s was used. The circuit employs 200 fF poly1-poly2 integration capacitors. The rail-to-rail buffer amplifiers were designed to drive off-chip loads. The buffer op-amp circuit offers an input capacitance of ~ 140 fF. This results in an effective integration capacitance $C_{int} \sim 340$ fF.

Fig. 5.8(a) shows the simulated transient response of the sensor after integration and buffering. ΔC_i was varied between 0 fF and 20 fF in steps of size 1 fF. Fig. 5.8(b) shows the static response curves obtained from transient simulations of the extracted layout for $T_{int} = 60$ ns and 195 ns. The mid-range sensitivities of the sensor were estimated to be 90 mV/fF and 130 mV/fF for $T_{int} = 60$ ns and 195 ns,

respectively, from the plots. The figure also shows corresponding linear calibration curves, which were computed in order to estimate nonlinearity errors for the sensors. The slope of the calibration curve $\alpha = \overline{\beta_i}$, where β_i is the slope of the static response curve at the i^{th} simulation point. An estimate of nonlinearity error [24] of the sensor can be expressed as:

$$NLE = \frac{\sqrt{(\beta_i - \alpha)^2}}{\alpha} \cdot 100 \quad (5.9)$$

The nonlinearity errors were estimated to be 9.8% and 12.1% for $T_{int} = 60$ ns and 195 ns respectively.

5.5.2 Chip fabrication and testing

The sensor test chip comprised test structures with the measurement circuit connected to metal3 (top-most metal layer) plates configured according to the stray capacitance compensation scheme [22]. Fig. 5.9(a) shows a photomicrograph of one such test structure. The chip comprised 5 such test structures with the metal3 plates varying in dimensions such that the metal3-to-substrate capacitances varied across the input range of 0 to 20 fF. Fig. 5.9(b) shows a test structure connected to interdigitated electrodes. This structure compensates for stray capacitances and overcompensates for standing capacitances such that the operation range of the measurement circuit lies in the linear portion of the static response curve. This can be useful for certain cell monitoring applications with critical linearity requirements [22].

The chip also included 3-phase clock generation circuitry with the *reset* and

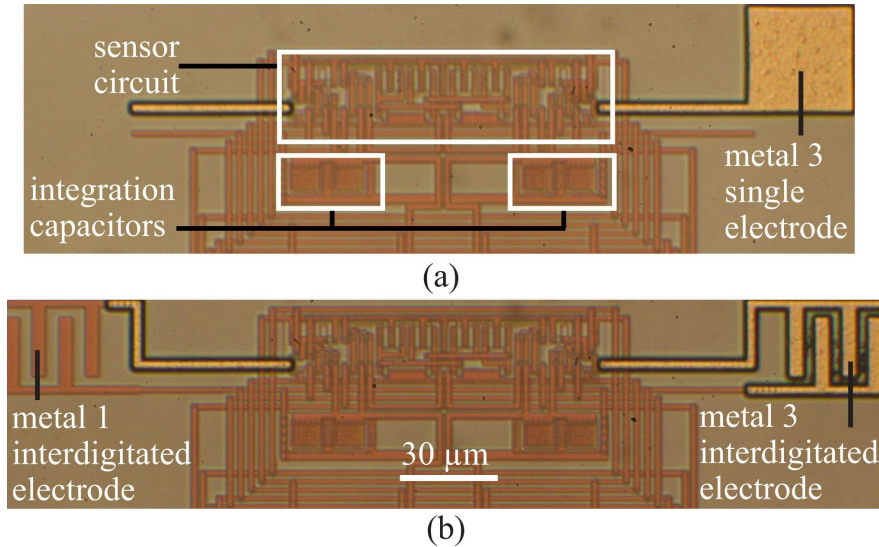


Figure 5.9: Chip photomicrographs showing (a) a test structure with stray capacitance compensation for measuring the standing capacitance of a metal3 electrode, (b) a test structure overcompensating for the standing capacitance of an interdigitated metal3 (top-most layer) electrode using an interdigitated metal1 (bottom-most layer) electrode.

eval signals generated using a standard 2-phase nonoverlapping clock generator [80]. The *sample* signal was generated by delaying the *eval* signal using a voltage controlled variable delay element comprising a current-starved inverter chain. Five of these chips were fabricated and tested.

Fig. 5.10 presents the test results showing the sensor output voltage distributions among the 5 test structures across the 5 chips for $T_{int} = 60$ ns and 195 ns. The standing capacitance values of the metal3 plates were estimated using the process run parameters provided by the vendor. The solid lines are the best fit curves for the measured data points, the slopes of which were used to estimate the detection sensitivity. The plots indicate successful sensor operation with mean sensitivities of 91 mV/fF and 126 mV/fF for $T_{int} = 60$ ns and 195 ns, respectively. The output

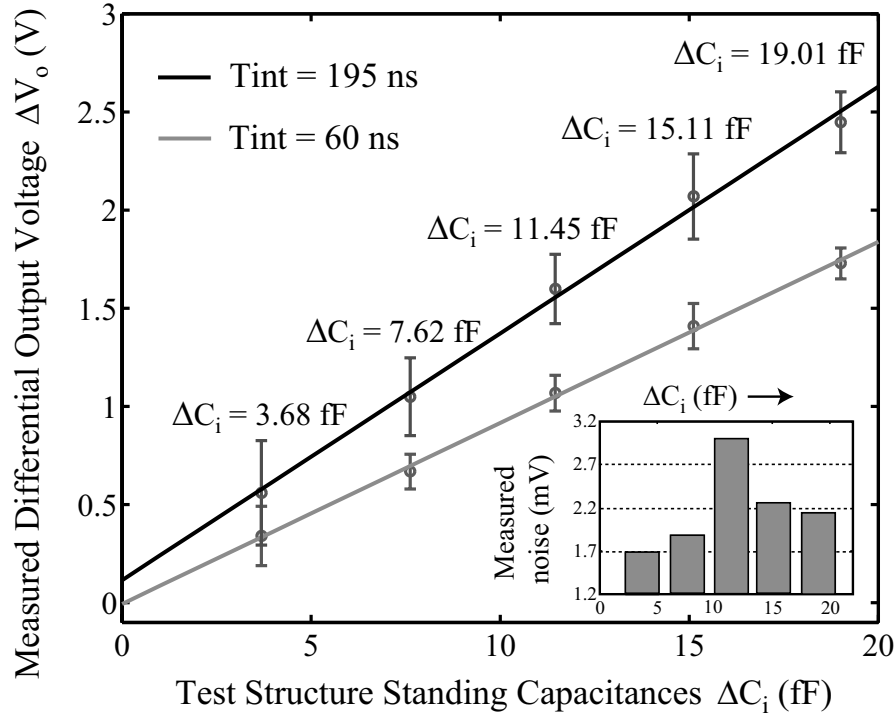


Figure 5.10: Test results showing the mean and standard deviations of the measured sensor output voltages in correspondence to the standing capacitances of metal3 electrodes for the 5 test structures across the 5 chips. The inset shows the output noise levels as measured from one of the sensor chips.

voltage spread among identical test structures across the different chips can be attributed to process mismatch. The proposed array architectures require individual calibration for only the SEM components of every chip in order to compensate for such mismatches.

The sensor output noise is expected to vary with ΔC_i . The inset located in Fig. 5.10 shows the output noise levels recorded from one of the test chips for different values of ΔC_i with $T_{int} = 195$ ns. The minimum and maximum noise levels were measured to be 1.7 mV and 3.0 mV for ΔC_i values of 3.68 fF and 11.45 fF respectively which translates to corresponding capacitance resolutions of 14 aF and 24 aF. With a differential output voltage swing of 5 V, the maximum achievable

sensor output dynamic range evaluates to 69.4 dB.

5.6 Test chip version 2: Sensor array and shielded current bus testing

5.6.1 Chip design

A second version of the differential capacitance sensor chip was designed to test the shielded current bus architecture for the sensor array. The column parallel architecture shown in Fig. 5.5 was employed for this purpose. For this chip, the core of the Sensor Evaluation Module (SEM) comprising the complementary current mirrors, subtractors and the integration capacitors was retained as in the previous version. But the buffer op-amps B1 and B2 in Fig. 5.3 were now replaced by smaller, single-stage rail-to-rail amplifiers. The new buffer amplifier circuit is shown in Fig. 5.11.

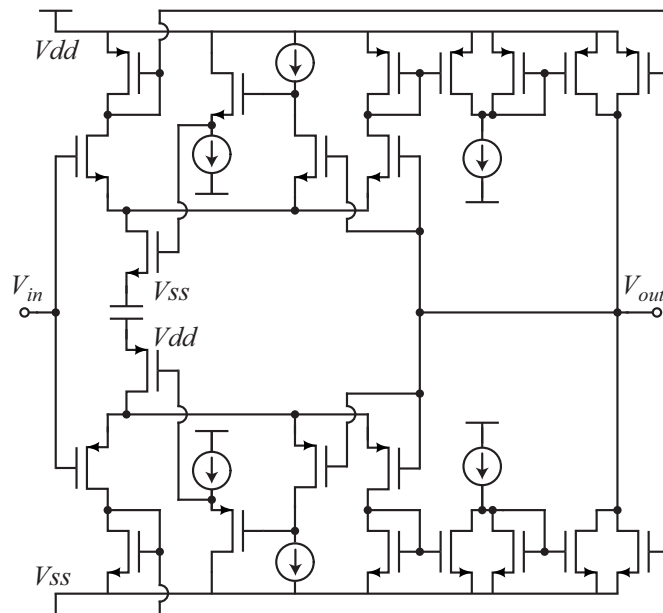


Figure 5.11: A single stage rail-to-rail amplifier circuit comprising class-AB differential cells employed for buffering the sensor output.

It is a single stage amplifier comprising two complementary class-AB differential cells along with current mirroring stages that drive the output node from rail-to-rail [81]. The amplifier is appropriate for buffering the capacitance sensor because it preserves rail-to-rail operation, has a small on-chip footprint and offers a low input capacitance. This is important for conserving sensor sensitivity since the input capacitances of B1 and B2 appear in parallel with the integration capacitors. The buffer amplifier designed in the $0.5 \mu\text{m}$ technology offers an input capacitance of 60 fF. This results in an effective integration capacitance $C_{int} \sim 260 \text{ fF}$ in the capacitance measurement circuit.

5.6.2 Chip fabrication and testing

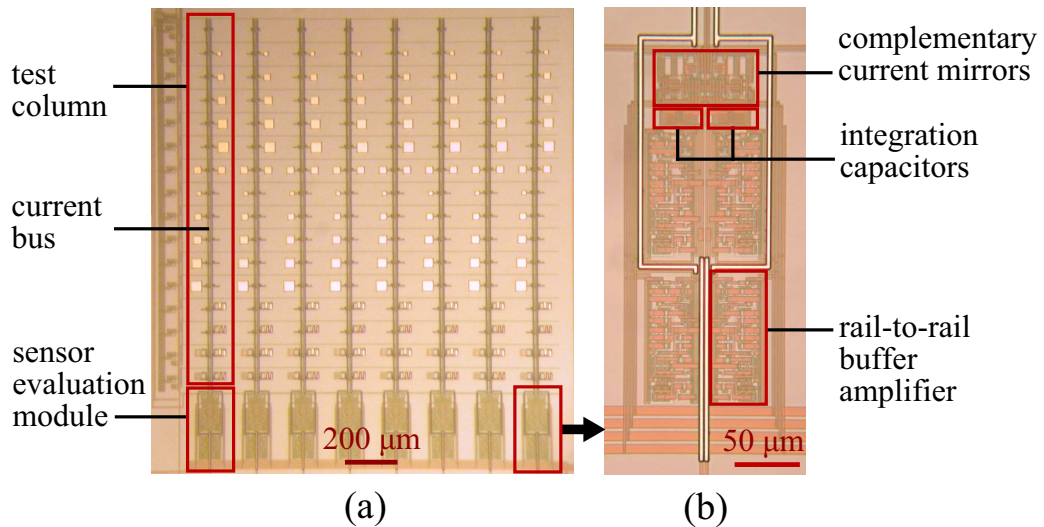


Figure 5.12: (a) Photograph of the fabricated differential capacitance sensor test array employing column parallel shielded current bus lines. (b) Photomicrograph of a single Sensor Evaluation Module (SEM).

Fig. 5.12(a) shows a photograph of the fabricated differential capacitance sensor test array. It follows a column parallel architecture (shown in Fig. 5.5) with

Table 5.1: Summary of the differential input capacitances corresponding to the 16 test structures in every column.

Test structure No.	Test capacitance type	Capacitance compensation type	Calibration capacitance ΔC_i (fF)
1	m3-sub ^a	stray	0
2	m3-sub	stray	5.07
3	m3-sub	stray	10.31
4	m3-sub	stray	15.38
5	m3-sub	stray	20.19
6	m3-sub	stray	25.31
7	m3-sub	standing	0
8	m3-sub	stray	-5.07
9	m3-sub	stray	-10.31
10	m3-sub	stray	-15.38
11	m3-sub	stray	-20.19
12	m3-sub	stray	-25.31
13	2f-m3 ^b	stray	*
14	4f-m3 ^c	stray	*
15	2f-m3 (C_{i+}) ^d 2f-m1 (C_{i-}) ^e	standing overcompensation	*
16	4f-m3 (C_{i+}) ^f 4f-m1 (C_{i-}) ^g	standing overcompensation	* ^h

^am3-sub: metal3-substrate coupling capacitance at C_{i+}

^b2f-m3: 2-finger metal3 interdigitated capacitance at C_{i+}

^c4f-m3: 4-finger metal3 interdigitated capacitance at C_{i+}

^d2f-m3 (C_{i+}): 2-finger metal3 interdigitated capacitance at C_{i+}

^e2f-m1 (C_{i-}): 2-finger metal1 interdigitated capacitance at C_{i-}

^f4f-m3 (C_{i+}): 4-finger metal3 interdigitated capacitance at C_{i+}

^g4f-m1 (C_{i-}): 4-finger metal1 interdigitated capacitance at C_{i-}

^h*: ΔC_i values estimated from test results are listed in Table 5.2

8 test columns. Each column comprises 16 test structures sharing a common SEM placed at the bottom. Each test structure comprises a 4-transistor CBCM front

end connected to a test capacitance. Table 5.1 provides details regarding the test capacitances created in each of the 16 structures in every column.

Structures 1 to 6 and 8 to 12 were configured for stray capacitance compensation and were used for sensor calibration in which the differential input capacitances varied between -25 fF and +25 fF, the target input range for the differential sensor. These structures comprised single metal3 (top-most metal layer) electrodes of varying sizes as can be seen in Fig. 5.12(a). The values of the single electrode metal3-substrate calibration capacitances were estimated using the process run parameters provided by the vendor. Structures 13 and 14 were also configured for stray capacitance compensation, but comprised 2-finger and 4-finger metal3 interdigitated electrodes respectively. Structures 15 and 16 were configured for standing capacitance overcompensation. In structure 15, C_{i+} node was connected to a 2-finger metal3 interdigitated electrode and C_{i-} node was connected to a 2-finger metal1 (bottom-most metal layer) interdigitated electrode. In structure 16, C_{i+} node was connected to a 4-finger metal3 interdigitated electrode and C_{i-} node was connected to a 4-finger metal1 interdigitated electrode. The ΔC_i values corresponding to structures 13 to 16 were estimated from test measurement results as will be described in section 5.7.

The single stage rail-to-rail amplifier shown in Fig. 5.11, in addition to buffering the sensor output as B1 and B2, was also used as buffers B3 and B4 (shown in Fig. 5.5) for driving the shield lines in the sensor test array. Therefore every SEM block comprised 4 of these buffer amplifiers (B1-B4). Fig. 5.12(b) shows a photomicrograph of a single SEM block.

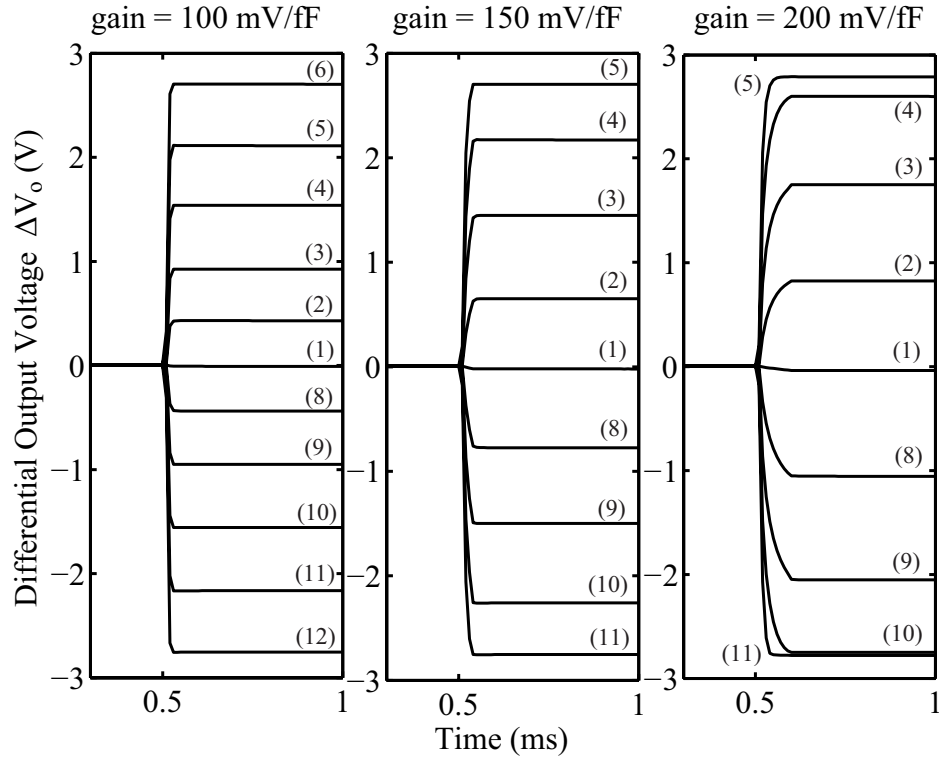


Figure 5.13: Recorded transient responses from one of the fabricated capacitance measurement circuits. The numbers in the parenthesis correspond to the test structures listed in Table 5.1.

In addition to the sensor test array, the chip also included 3-phase clock generation circuitry with the *reset* and *eval* signals generated using a standard 2-phase nonoverlapping clock generator [80]. The sensors were operated at a clocking frequency of 1 kHz, which is appropriate for monitoring the low frequency capacitive behavior of cells, our current target application. The *sample* signal was generated by delaying the *eval* signal using a voltage controlled variable delay element comprising a current-starved inverter chain. Five of these chips were fabricated and tested.

Fig. 5.13 shows the transient responses as recorded from one of the capacitance measurement circuits when the ΔC_i was varied between -25 fF and +25 fF, by

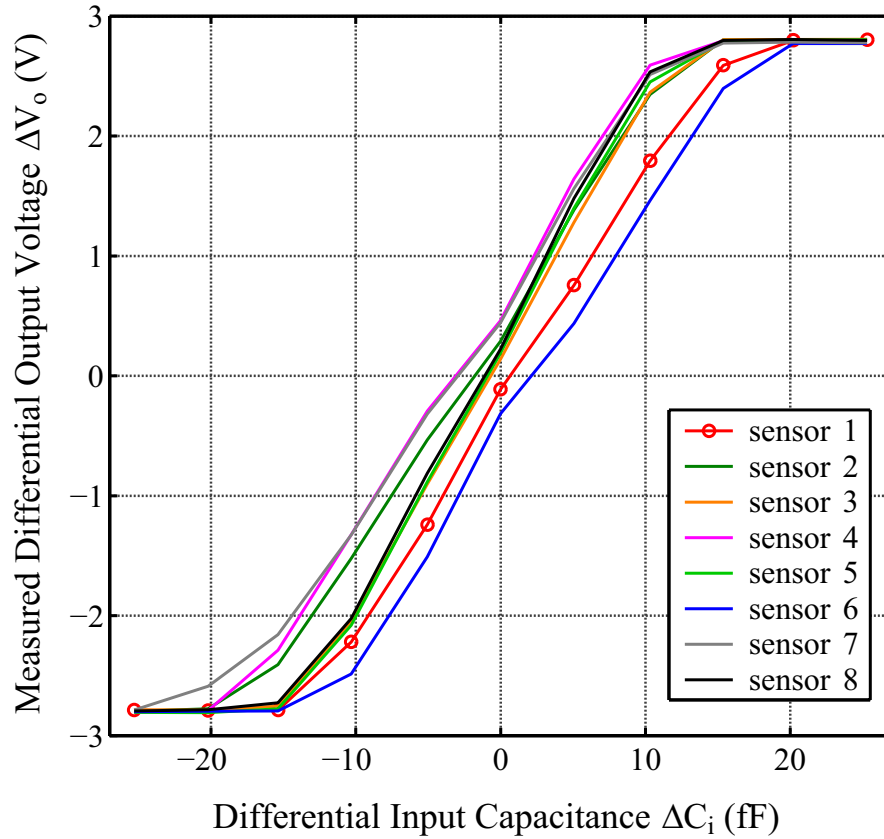


Figure 5.14: Measured transfer functions corresponding to the 8 SEMs from one of the test chips with sensor gain set to 200 mV/fF.

switching across the calibration structures 1 to 6 and 8 to 12. Sensor responses were recorded for the 3 different sensor gains of 100, 150 and 200 mV/fF. The sensor gains were varied by delaying the *sample* pulse by 14 μ s, 38 μ s and 112 μ s respectively. The maximum achievable gain was measured to be 200 mV/fF. Based upon noise measurements, the sensor circuit incorporated in the test array employing the shielded current bus was able to achieve a resolution of 15 aF and an output dynamic range of 65 dB.

Fig. 5.14 shows the sensor transfer curves as measured from one of the test chips. The 8 curves correspond to the transfer functions of the 8 SEMs connected to their respective test columns. The data points correspond to calibration structures

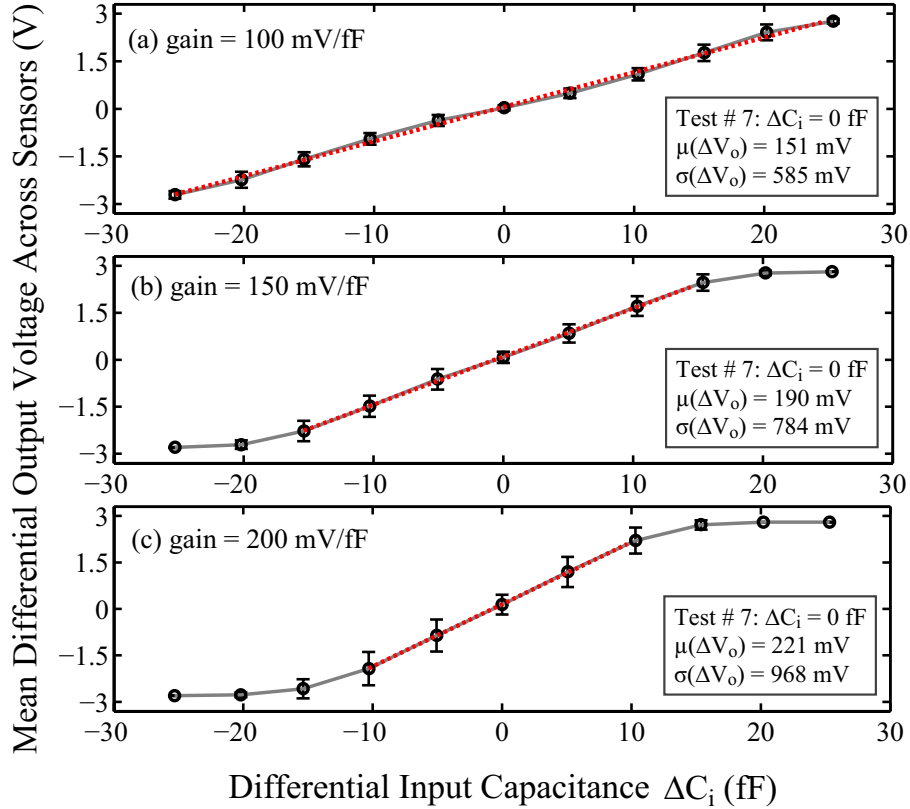


Figure 5.15: Averaged transfer functions across all the SEMs across all the 5 fabricated chips corresponding to sensor gains of 100, 150 and 200 mV/fF. The error bars indicate the spread in the sensor outputs due to process and device mismatch effects. The insets display the mean $\mu(\Delta V_o)$ and standard deviation $\sigma(\Delta V_o)$ values of the sensor outputs corresponding to test structure 7 (with $\Delta C_i = 0$ fF) as listed in Table 5.1. The dotted red lines are the linear calibration curves used to estimate the sensor gain values.

1 to 6 and 8 to 12 as listed in Table 5.1. The curves were recorded with the sensor configured to achieve a maximum gain of 200 mV/fF.

Fig. 5.15 shows the averaged transfer functions across all the SEMs in all the 5 fabricated chips corresponding to sensor gains of 100, 150 and 200 mV/fF. The error bars indicate the spread in the sensor outputs corresponding to the fixed values of input calibration capacitances corresponding to test structures 1 to 6 and 8 to 12. As can be observed the sensor output spread increases with increasing gain.

This is due to the integration of the sensor output offset currents I_{os-} and I_{os+} over longer durations for achieving higher gains. The inset located in each of the panels in Fig. 5.15 displays the mean $\mu(\Delta V_o)$ and standard deviation $\sigma(\Delta V_o)$ values of the sensor outputs corresponding to test structure 7 which is configured for standing capacitance compensation with $\Delta C_i = 0$ fF. The $\mu(\Delta V_o)$ and $\sigma(\Delta V_o)$ values can be employed to estimate the average input capacitance offset and the average input capacitance offset spread across all the fabricated sensors. For example, in the plot corresponding to gain = 200 mV/fF in Fig. 5.15, the $\mu(\Delta V_o)$ and $\sigma(\Delta V_o)$ values for test structure 7 are 221 mV and 968 mV respectively. These translate into an average input capacitance offset of 1.1 fF and an average input capacitance offset spread of 4.84 fF respectively.

The output offset voltage spread across the different sensor modules tested above can be unacceptable for applications where in the usable dynamic range of the sensor circuits is critical. Such applications will require output offset cancelation for optimizing sensor performance. We next present an approach to solve this problem by incorporating floating gate transistors in the capacitance measurement circuit.

5.7 Test chip version 3: Capacitance sensor incorporating floating gate trimming for mismatch compensation

Floating gate transistors have been previously employed for mismatch compensation and offset cancelation in CMOS imagers [82], current sources [83–85], autozero amplifiers [86, 87], adaptive comparators [88] and ADCs [89]. They can

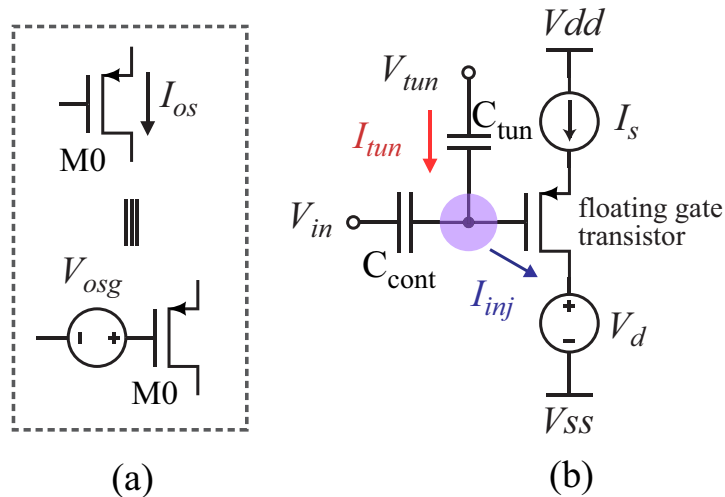


Figure 5.16: (a) Representing output offset current in a PMOS transistor as a gate offset voltage. (b) Conceptual illustration of a floating gate transistor.

be employed as in-circuit trimming elements for either creating or canceling offsets. Advantages of employing floating gate transistors for this purpose include programming capability, long-term retention and standard CMOS fabrication. Fig. 5.16(a) provides a conceptual representation of the offset cancellation scheme that can be applied to the capacitance measurement circuit presented here. The PMOS transistors M9 and M14 in the current subtractors of the sensor circuit (see Fig. 5.3) are represented by the transistor M0 in Fig. 5.16(a). I_{os} represents the offset currents I_{os-} and I_{os+} flowing in the corresponding current subtractors. The offset current I_{os} can be translated into the gate offset voltage V_{osg} as shown in Fig. 5.16(a). By modifying M0 to be a floating gate transistor, V_{osg} and therefore the sensor output offset currents I_{os-} and I_{os+} can be canceled.

Fig. 5.16(b) provides a conceptual illustration of a floating gate transistor. The gate of this transistor is completely isolated by SiO_2 , a high quality insulator. This provides a non-volatile charge storage node at the transistor gate. In a 2-

poly CMOS process, the poly1 layer is employed for the floating gate and poly2 is employed for the control gate. The control and the floating gates together form the capacitor C_{cont} . The capacitor C_{tun} shown in 5.16(b) is a PMOS-capacitor, with its gate connected to the floating gate, and the drain, source and bulk connected to the tunneling terminal V_{tun} .

The floating gate transistor can be programmed using two different mechanisms:

- Impact Ionization Hot Electron Injection [86, 87]: In this mechanism a high source-to-drain voltage is imposed on the transistor because of which electrons are created at the drain edge of the drain-to-channel depletion region via hot-hole impact ionization. These electrons in the presence of a high enough vertical electric field, gain sufficient kinetic energy to cross the Si-SiO₂ barrier thereby getting injected onto the floating gate. This mechanism results in a negative shift in the gate offset voltage V_{osg} . In Fig. 5.16(b) the rate of injection can be controlled by the source-to-drain current I_s . The injection current I_{inj} is modeled using the empirical relation [90]:

$$I_{inj} = \alpha \cdot I_s \cdot \exp \left[-\frac{\beta}{(V_{gd} + \delta)^2} + \lambda(V_{gd} - V_{gs}) \right] \quad (5.10)$$

where I_s is the source-to-drain current, V_{gd} and V_{gs} are the gate-to-drain and gate-to-source voltages, and α , β , λ and δ are fitting parameters.

- Fowler-Nordheim Tunneling [91]: In this mechanism a very high electric field

is imposed on the PMOS-capacitor C_{tun} so that the effective width of the potential barrier between the poly-Si gate and the Si below the gate oxide is reduced to a few nanometers. This allows for the electrons in the conduction band of the poly-Si gate to tunnel through the oxide bandgap to the Si conduction band on the other side of the oxide. This field-assisted tunneling is called Fowler-Nordheim Tunneling. This mechanism results in a positive shift in the gate offset voltage V_{osg} . The tunneling current I_{tun} depends on the gate oxide voltage and can be approximately expressed as [90]:

$$I_{tun} = -I_{tun0} \cdot W \cdot L \cdot \exp\left[-\frac{V_f}{V_{ox}}\right] \quad (5.11)$$

where I_{tun0} is a pre-exponential current, W and L are the width and length of the PMOS tunneling capacitor, V_{ox} is the gate oxide voltage and V_f is a constant which varies with oxide thickness.

5.7.1 Sensor circuit design incorporating floating gate transistors

The capacitance measurement circuit employed in the version 2 chip was modified to incorporate the floating gate transistors M9 and M14 as shown in Fig. 5.17. Each floating gate transistor is connected to a dedicated injection/tunneling (I/T) structure that programs the sensor output offset by enabling and controlling the injection or tunneling processes.

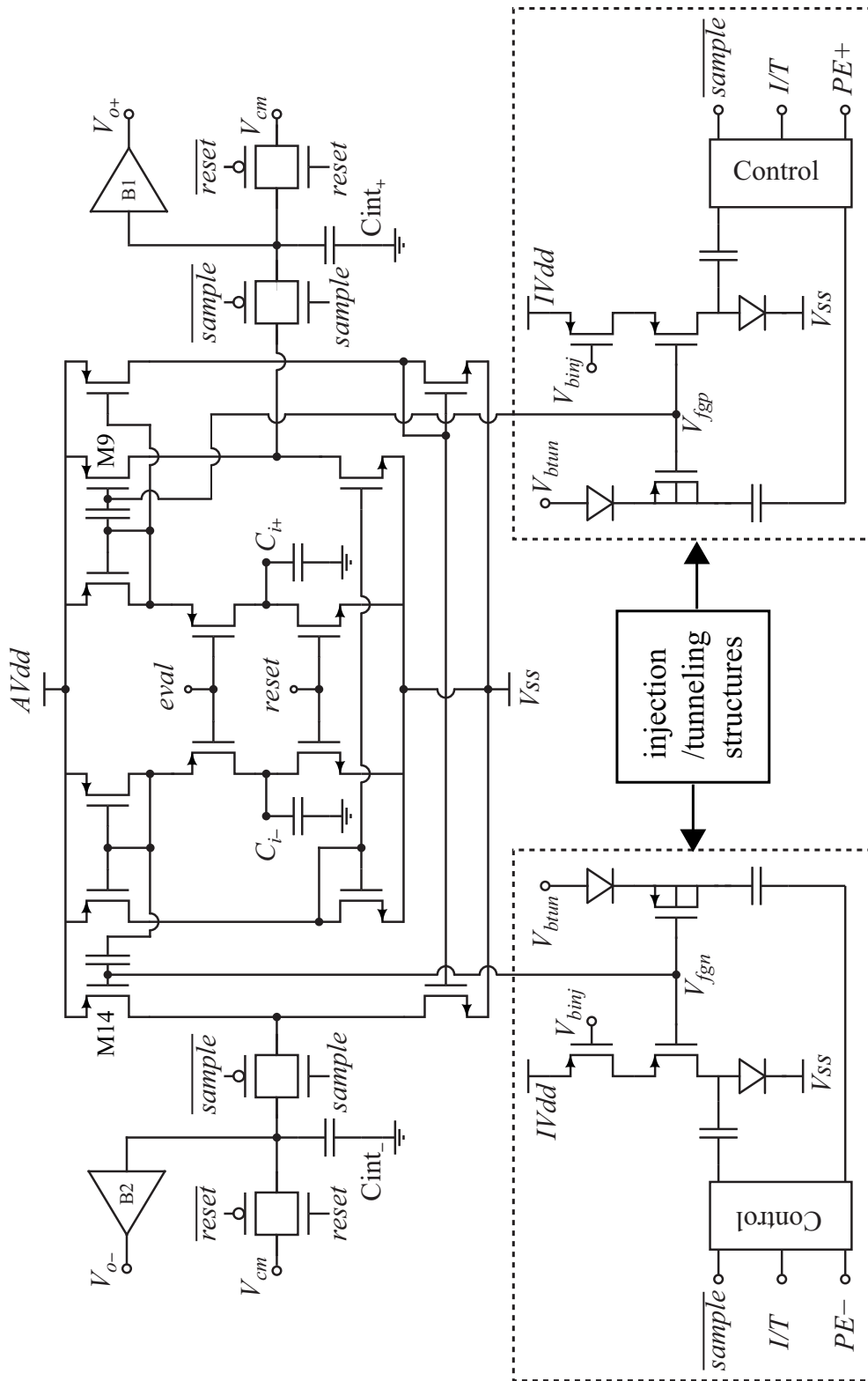


Figure 5.17: Schematic of the floating gate capacitance measurement circuit with injection/tunneling (I/T) structures. Control signals employed in the I/T structures include: (a) \overline{sample} , for synchronizing floating gate trimming process with sensing clock cycle, (b) I/T , for selecting between injection or tunneling processes, (c) $PE\pm$, for enabling the trimming process.

The capacitance sensor circuit and the I/T structures employ separate supply rails $AVdd$ and $IVdd$ respectively. During normal operation, both $AVdd$ and $IVdd$ are set to 3 V. During programming, the sensor circuit supply $AVdd$ is retained at 3 V, and $IVdd$ is raised to a higher voltage.

Fig. 5.18 illustrates the design and operation of the I/T structure for performing floating gate trimming. The I/T structure employed here was previously developed for performing adaptation in a floating gate quantizer inside a flash ADC [89]. In Fig. 5.18, M9 is the floating gate PMOS transistor in the current subtractor of the capacitance measurement circuit. As can be seen the floating gate is shared by two other transistors Mi1 and Mt1 in the I/T structure. Mi1 is the injection transistor and Mt1 is the tunneling transistor. Mi2 serves as a current source for controlling the rate of injection in Mi1. The capacitor and diode pairs, (Ci, Di) and (Ct, Dt) form charge pumps for generating the high voltages necessary for enabling injection and tunneling. The (Ci, Di) pair forms a negative charge pump for generating a high source-to-drain voltage for Mi1 and the (Ct, Dt) pair forms a positive charge pump for generating a high voltage across the gate oxide of Mt1. The terminal V_{btun} can be raised above the nominal supply voltage during tunneling. For the test chip presented here the V_{btun} pin in the padframe comprised ESD (Electrostatic Discharge) protection diodes. So in order to prevent these diodes from turning on, $IVdd$ also had to be raised along with V_{btun} while performing tunneling. In order to further ensure that injection in transistor Mi1 was fully disabled when $IVdd$ was raised to 9 V, the current source transistor Mi2 was turned off whenever tunneling was enabled.

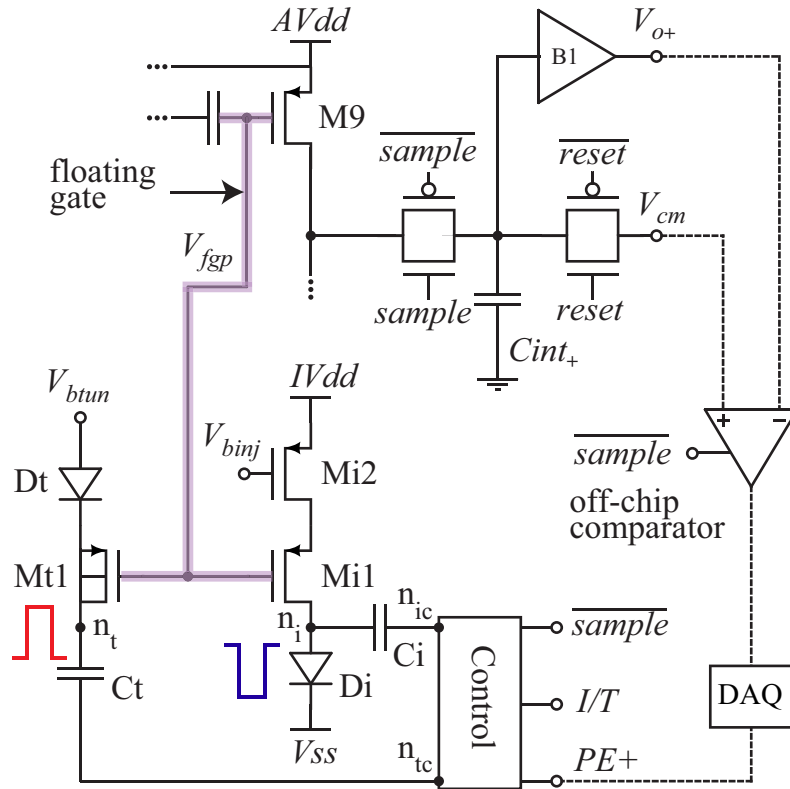


Figure 5.18: Schematic showing the design and operation of the injection/tunneling (I/T) structure.

Charge injection and tunneling were performed in small steps in synchrony with the *sample* phase of the sensing clock cycle. The $\overline{\text{sample}}$ signal served as the control pulse for performing injection or tunneling. The control logic block shown in Fig. 5.18 is responsible for enabling or disabling programming, and for selecting between injection or tunneling. During programming the supply voltage $IVdd$ is raised to 5 V for performing injection and 9 V for performing tunneling. The logic block drives the charge pumps by employing high voltage buffers that are powered by $IVdd$. When injection is disabled (or during normal operation when $IVdd = 3$ V), node n_{ic} sits at 5 V (normal operation: 3 V) and node n_i is at approximately 0.65 V (built-in potential of the diode D_i). With this condition, the source-to-drain

voltage across Mi1 is not sufficient to enable impact-ionized hot electron injection. When injection is enabled, node n_{ic} goes to ground and n_i is pulled to $-5\text{ V} + 0.65\text{ V}$. This increases the source-to-drain voltage of Mi1 enabling a small amount of charge to be injected onto the floating gate. The duration over which the node n_i stays at $-5\text{ V} + 0.65\text{ V}$ depends upon the source-to-drain current set by Mi2, since this current gets integrated over the junction capacitance of diode Di thereby continually reducing the source-to-drain voltage of Mi1 until Di turns on. When tunneling is disabled or during normal operation, node n_{tc} sits at ground causing node n_t to be at $V_{btun} - 0.65\text{ V}$. This does not impose a sufficient voltage across the gate oxide of Mt1 for tunneling to happen. When tunneling is enabled, node V_{btun} is set to 8 V , n_{tc} is pulled to 9 V causing n_t to be pulled to $8\text{ V} - 0.65\text{ V} + 9\text{ V}$. This creates a high enough voltage across the gate oxide of Mt1 to induce tunneling. For the $0.5\text{ }\mu\text{m}$ CMOS technology employed here, tunneling requires a minimum voltage of around 15 V across the gate oxide.

5.7.2 Chip fabrication and testing

The chip designed for testing the floating gate differential capacitance sensor comprised the same test array as in version 2 but with 4 test columns instead of 8. The chip was fabricated in a $0.5\text{ }\mu\text{m}$, 2-poly, 3-metal standard CMOS process. Each column comprised the same 16 test structures as described in Table 5.1, sharing a common SEM incorporating the modified capacitance sensor with the floating gate transistors and the I/T structures. Fig. 5.19 shows a photomicrograph of a modified

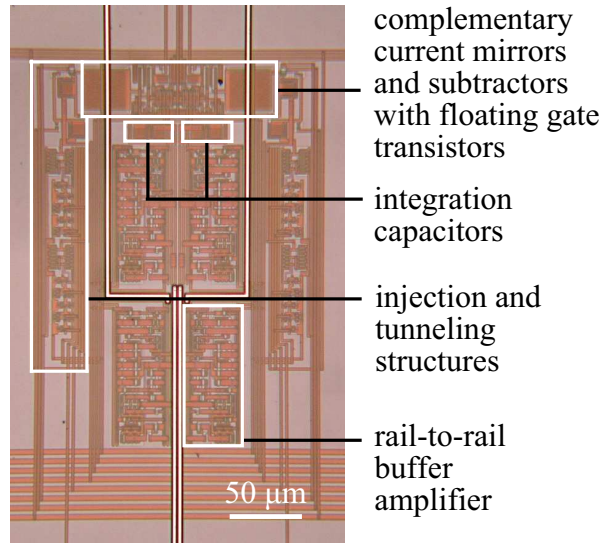


Figure 5.19: Photomicrograph of the modified version of the Sensor Evaluation Module incorporating the floating gate transistors and the I/T structures.

SEM block employed in this version of the chip. Five of these chips were fabricated and tested.

The sensor output offset cancelation was performed with test structure 7 (configured for standing capacitance compensation with $\Delta C_i = 0$ fF, see Table 5.1) selected. This was the test case which exhibited an unacceptable spread of 968 mV across the sensor outputs in version 1 of the sensor chip. Before programming, all the chips were exposed to UV radiations in order to erase all existing charges on the floating gate. After this, for every chip, all the 4 SEMs were selected for programming with the tunneling mode enabled. For the I/T structure fabricated in the 0.5 μm CMOS process appreciable amount of tunneling was observed when V_{btun} was set to 8 V and $IVdd$ was raised to 9 V. Tunneling was continued until all the sensor outputs V_{o-} and V_{o+} settled to arbitrary voltages well below the common mode voltage V_{cm} which was set to 1.5 V (mid-supply voltage). V_{btun} was otherwise tied

to ground during normal operation. Later on injection was enabled sequentially for each of the outputs V_{o-} and V_{o+} for every sensor. For this $IVdd$ was set to 5 V and V_{binj} was adjusted to have a low rate of injection in order to visually observe the progress of the output offset cancelation on an oscilloscope. Injection was enabled until the output voltages V_{o-} and V_{o+} settled close to V_{cm} resulting in $\Delta V_o \sim 0$ V. For programming this version of the chip an off-chip strobe comparator (strobed by \overline{sample} signal) was employed to form the feedback control loop shown in Fig. 5.18 while performing injection. The output of the comparator was continuously monitored by a data acquisition software in order to generate the $PE\pm$ (program enable) signal for the I/T control block.

To summarize the programming procedure, the tunneling mechanism was first employed for an initial global course tuning of the output voltages V_{o-} and V_{o+} to arbitrary values below V_{cm} . This was followed by injection for fine tuning of V_{o-} and V_{o+} to voltages close to V_{cm} .

Fig. 5.20 shows the individual sensor transfer curves as measured from two of the test chips after performing floating gate trimming at the operating point corresponding to test structure 7. The 4 curves in each of the plots correspond to the transfer functions of the 4 SEMs connected to their respective test columns. The data points correspond to test structures 1 to 6 and 8 to 12 as listed in Table 5.1 that are configured for stray capacitance compensation, with ΔC_i values varying between -25 fF and +25 fF. The curves were recorded with the gain set to 200 mV/fF. On comparing Fig. 5.20 with Fig. 5.14 it can be seen that there is an appreciable degree of mismatch compensation over the entire operating range for all

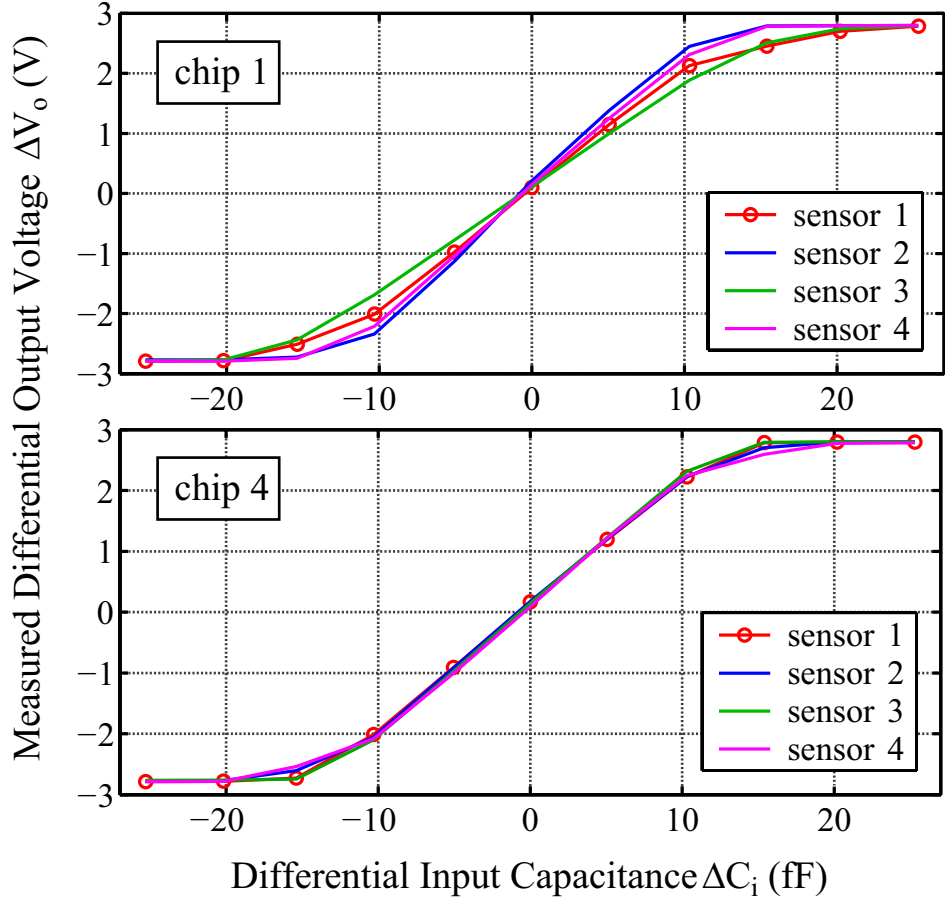


Figure 5.20: Measured transfer functions from two of the test chips after floating gate trimming at the operating point corresponding to test structure 7.

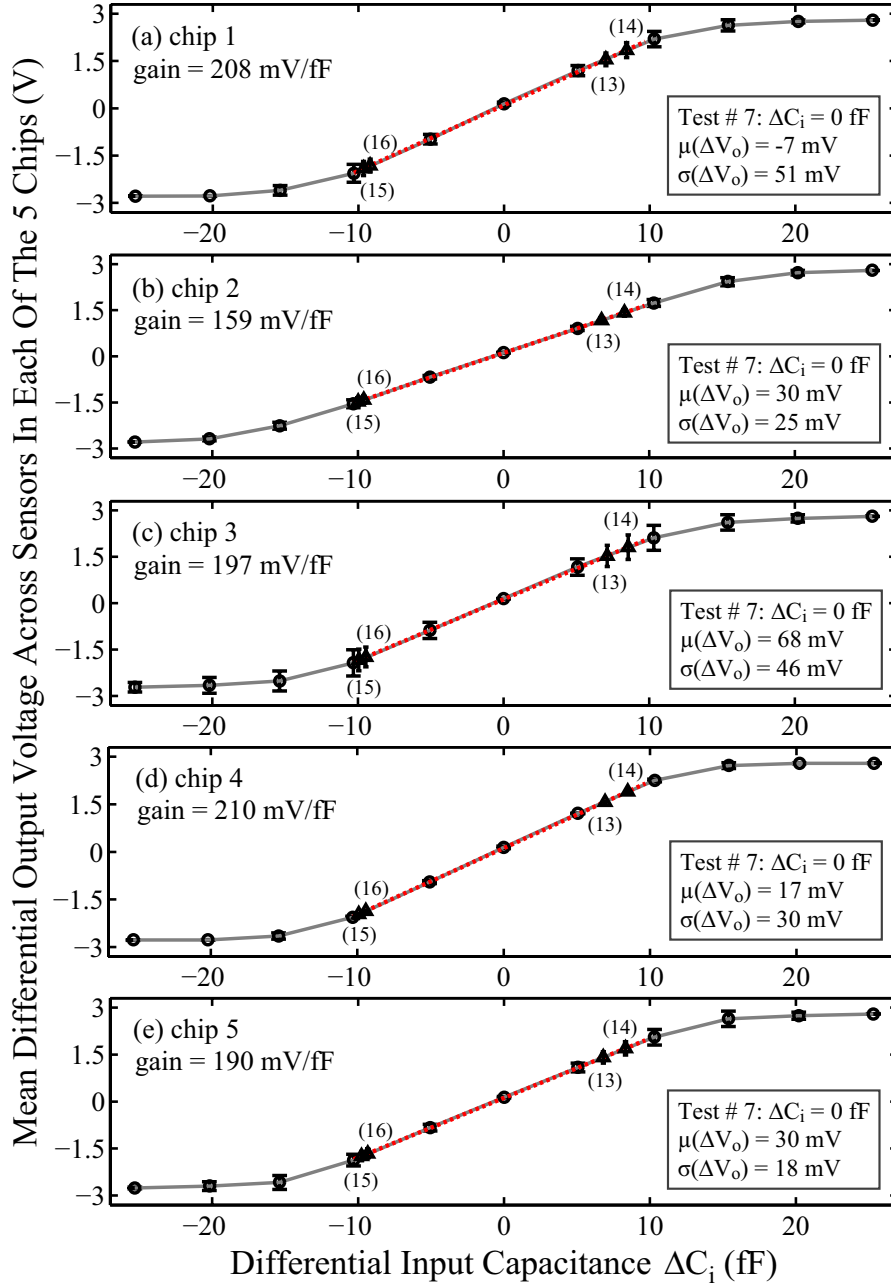
the sensors. Also, linearity of the transfer functions has significantly improved after performing floating gate trimming. The sensors in chip 1 exhibited a small degree of gain mismatch in comparison to those in chip 4 due to process mismatch effects.

Fig. 5.21 shows the averaged transfer functions across the 4 SEMs for each of the 5 fabricated chips after floating gate trimming. The error bars indicate the spread in the sensor outputs corresponding to the fixed values of input calibration capacitances corresponding to test structures 1 to 6 and 8 to 12. The insets shown alongside the corresponding curves in Fig. 5.21 displays the mean $\mu(\Delta V_o)$ and standard deviation $\sigma(\Delta V_o)$ values of the sensor outputs corresponding to test structure

7 which is configured for standing capacitance compensation with $\Delta C_i = 0$ fF. This is the operating point at which the floating gate trimming was performed.

On evaluating the data from all the 5 chips, the average values of $\mu(\Delta V_o)$ and $\sigma(\Delta V_o)$ corresponding to the test structure 7 are 27 mV and 34 mV respectively. Considering a maximum achievable sensor gain of 200 mV/fF, this translates into an average input capacitance offset of 0.13 fF with an average input capacitance offset spread of 0.17 fF. So the floating gate trimming of the differential capacitance sensors resulted in an average reduction of 88% in $\mu(\Delta V_o)$ and 96.5% in $\sigma(\Delta V_o)$ with reference to the result obtained using the previous version of the measurement circuit which did not incorporate floating gate trimming. The average $\mu(\Delta V_o)$ and $\sigma(\Delta V_o)$ values stated above are indicative of the accuracy and precision of the employed floating gate trimming mechanism. These values can be significantly improved by employing on-chip floating gate comparators with extremely low input offsets [88] and on-chip generation of the I/T and $PE\pm$ signals for feedback control during programming.

The dotted red lines in each of the panels in Fig. 5.21 are the linear calibration curves for the sensors in each of the test chips. These curves were used to estimate the differential input capacitance ΔC_i values corresponding to test structures 13 to 16. These are listed in Table 5.2. Structures 13 and 14 were configured for stray capacitance compensation, and comprised 2-finger (dimensions: length = 19.6 μm , width = 9.8 μm , spacing = 11.2 μm) and 4-finger (dimensions: length = 19.6 μm , width = 4.2 μm , spacing = 4.9 μm) metal3 interdigitated electrodes respectively. Structures 15 and 16 were configured for standing capacitance overcompensation.



○ : Calibration points corresponding to test structures 1 to 6 and 8 to 12
 ▲ : ΔC_i Estimation points corresponding to test structures 13 to 16

Figure 5.21: Averaged transfer functions across the 4 SEMs in each of the 5 chips after floating gate trimming. The error bars indicate the spread in the sensor outputs after programming. The insets display the mean $\mu(\Delta V_o)$ and standard deviation $\sigma(\Delta V_o)$ values of the sensor outputs corresponding to test structure 7. The dotted red lines are the linear calibration curves employed to estimate the ΔC_i values corresponding to structures 13 to 16.

Table 5.2: Differential input capacitance values corresponding to test structures 13 to 16 as estimated from measurement results.

Test #	chip 1 ΔC_i (fF)	chip 2 ΔC_i (fF)	chip 3 ΔC_i (fF)	chip 4 ΔC_i (fF)	chip 5 ΔC_i (fF)
13	6.99	6.73	7.11	6.93	6.80
14	8.41	8.30	8.55	8.48	8.33
15	-9.65	-9.97	-9.94	-9.89	-9.76
16	-9.19	-9.60	-9.45	-9.42	-9.34

In structure 15, C_{i+} node was connected to a 2-finger metal3 (top-most metal layer) interdigitated electrode and C_{i-} node was connected to a 2-finger metal1 (bottom-most metal layer) interdigitated electrode. In structure 16, C_{i+} node was connected to a 4-finger metal3 interdigitated electrode and C_{i-} node was connected to a 4-finger metal1 interdigitated electrode.

5.8 Summary

A second generation of fully differential rail-to-rail CMOS capacitance sensors were designed, fabricated and tested. The core sensor circuit employs the CBCM technique for linearly mapping differential input capacitances to rail-to-rail differential output voltages. The differential sensor can compensate for all the stray capacitances arising from the cell growth environment and the measurement circuit itself that are responsible for degrading the performance of single-ended sensors. The differential readout increases output dynamic range and suppresses correlated noise, thereby improving sensor resolution.

The presented array architecture based on the shielded current routing bus en-

ables the measurement circuit to be employed in high density sensor arrays without compromising performance, and in addition it simplifies calibration and improves immunity to noise and junction leakage. The sensor array architecture with on-chip gain-tuning can provide the capability for readout of heterogeneous sensor arrays, which is potentially useful for simultaneously studying different aspects of cell behavior on a single chip platform.

The sensor operation was demonstrated by measuring on-chip test capacitances comprising single and interdigitated metal electrodes configured using different capacitance compensation schemes. The measurement circuit was tested in individual sensor configuration and also in a test array employing the shielded current routing bus. After successful demonstration of the sensor operation, the measurement circuit was modified to include floating gate trimming for mismatch compensation. The sensor output offset cancelation was performed using a combination of impact ionized hot electron injection and Fowler Nordheim tunneling mechanisms. The performance metrics of the sensor including the dynamic range, sensitivity, resolution, post-trimming output voltage offset and offset spread that were obtained from bench test results have been found to be appropriate for on-chip cell monitoring applications.

Chapter 6

Conclusions: Part I

On-chip capacitance sensing was demonstrated as a promising label-free technique for integrated cell sensing applications, specifically for, characterizing cell-surface attachment, monitoring cell health and tracking cell growth. Several experiments were conducted using the first generation capacitance sensors, with living cells cultured on the sensor chips. The sensors were observed to consistently exhibit a distinct response to the cultured cells as shown in the experiments described in Chapter 4. A first attempt at providing a circuit-based model was made for explaining the sensor responses to biological cells as was observed during the experiments. The model was developed based on the low-frequency dielectric properties of cells as discussed in the Biophysics literature.

The claims made with regard to the monitoring capabilities of the cell capacitance sensing approach were entirely based on validation results obtained from either post-experiment visual inspection of cells on the sensor chips or standard cell biology techniques (such as Neutral Red retention test and Alamar Blue reduction test) that were able to assess cell properties without interfering with the capacitance measurements. A more thorough validation of the cell capacitance sensing technique will require performing time-lapse microscopy of the cells on the sensor chips over long monitoring intervals. Microscopic imaging of cells on the chip re-

quires specialized reflectance-mode optics. So a microscope with optics corrected for intervening fluid needs to be assembled inside an incubator and suitable chip package needs to be developed for allowing concurrent imaging of cells on top of the chip surface along with sensor response monitoring.

In addition to providing encouraging experimental demonstrations, the first generation single-ended sensors posed problems with regard to parasitic capacitance effects and noise coupling. Also the sensor output range was limited to a few 100s of mVs and the sensor spatial resolution was limited by 12 transistors, 4 of which were digital switches and the remaining 8 performed analog operations.

In order to resolve the above issues, a second generation fully-differential rail-to-rail capacitance measurement circuit was developed. In comparison to the first generation single-ended sensor, the second generation differential sensor exhibits linear capacitance versus output voltage characteristic, offers higher sensitivity, higher resolution, higher dynamic range and better immunity to interference noise coupling. The nonlinear distance versus output voltage characteristic resulting from the single electrode configuration (employed in the first generation sensor operating as a proximity detector) was found to be appropriate for tracking surface attachment of cells. The differential sensor presented here can also employ the single electrode configuration to take advantage of this feature. (Employing interdigitated electrodes for on-chip cell sensing will require passivation layer thinning in order to overcome penetration depth limitations imposed by the passivation layer thickness in standard CMOS processes.) The flexibility of configuring the differential sensor using different capacitance compensation schemes offers a more versatile solution for the

cell sensing problem by allowing custom-tailoring according to the application requirements. The shielded current routing-based sensor array architecture developed in this work enables the measurement circuit to be employed in high density sensor arrays without compromising performance. The sensor array architecture in combination with the on-chip gain-tuning feature can provide the capability for readout of heterogeneous sensor arrays, which is potentially useful for simultaneously studying different aspects of cell behavior on a single chip platform.

The differential sensor circuit was also modified to incorporate in-circuit floating gate trimming in order to compensate for the device and process mismatch effects in the fabricated sensors. The floating gate trimming further improves the sensor performance by canceling output voltage offsets and linearizing the transfer function characteristics.

The integrated cell capacitance sensing platform developed in this dissertation can enable cell-based lab-on-a-chip (LOC) systems for high speed, automated and real-time monitoring of biological cells. Such systems can be very useful for performing interesting scientific investigations of cellular properties (related to adhesion, viability and proliferation) at a microscopic level. The temporal information present in the sensor responses can provide new insights with regard to individual cell behavior. The demonstrated cell sensing approach can also be employed in several industrial applications such as automated drug screening and biocompatibility characterization of materials.

Part II

A CMOS POTENTIOSTAT FOR CONTROL OF INTEGRATED MEMS
ACTUATORS

Chapter 7

Research Background

7.1 First generation cell clinics

The first generation prototype of the cell clinics microsystem comprises an array of lidded microvials for confining single cells or small cell groups at the sensing sites corresponding to an array of CMOS bioamplifiers for amplifying weak extracellular potentials from electrogenic cells [5]. The purpose of the lidded microvials is to confine the living cells and isolate them within controllable microenvironments. The bioamplifiers provide a means of monitoring the electrical activity of cells within the controlled environment. Fig. 1.1 in Chapter 1 provides a conceptual illustration of the microsystem. The microvial lids are opened and closed by actuator hinges employing an electroactive polymer that changes volume due to electrochemical oxidation and reduction. At the macro-scale, such reactions are controlled using an instrument known as a potentiostat. In the first generation of cell clinics these control signals were supplied by an external potentiostat instrument [5]. This research enables system miniaturization of cell clinics by integrating the necessary driver circuitry for *in situ* control of the microactuators right on top of the CMOS chip.

7.1.1 Cell clinics microstructure: configuration and operation

The closing action of the microvial lids is accomplished by bending of the hinge, as shown in Fig. 7.1 (a).

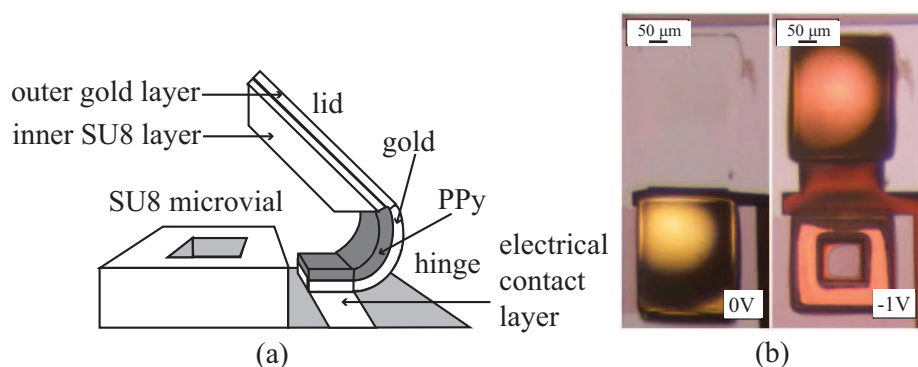


Figure 7.1: (a) Schematic illustration of a lidded microvial with bilayer hinge. Dark layer represents PPy [Illustration based on an original figure courtesy of Y. Liu and Dr. E. Smela]. (b) Photomicrograph of the fabricated cell clinics microvials [Photomicrographs courtesy of Dr. M. Christophersen and Dr. E. Smela].

The electroactive polymer employed in the cell clinics microactuators is polypyrrole doped with dodecylbenzenesulfonate, PPy(DBS), a well-studied material whose properties depend on the imposed potential and the resulting oxidation level [92,93]. The hinge's upper layer is made of the conjugated polymer PPy(DBS). The lower layer is made of gold. The gold layer acts as both a structural layer and an electrical contact to the PPy. It serves as an inert electrode to electrochemically address the electroactive polymer. When immersed in an electrolyte (in our case 0.1 M NaDBS), PPy changes volume according to the applied potential, while the gold does not. Reducing the polymer draws hydrated Na^+ cations into the polymer matrix, increasing the volume of the film, whereas oxidizing it expels the ions, decreasing the volume [94]. Also associated with the change in the electronic state of the polymer

(change in oxidation level) is a change in color [92]. The potentiostat controls the direction and extent of the electrochemical reaction, which in turn determines the degree of expansion or contraction of the polymer film. The out-of-plane expansion of thin films in aqueous Na^+ -containing electrolytes is substantial, approximately 30% between the fully oxidized and reduced states, as established with techniques such as AFM and mechanical profilometry [92,94–96]. The bilayered actuator structures can be miniaturized using standard microfabrication techniques [5,94,97–99]. The volume changing property of electroactive polymers has also been exploited to realize microfluidic valves [100].

The closing and opening of the microvial lids in the cell clinics microsystem requires a control voltage operating between 0 V and -1 V with respect to a Ag/AgCl reference potential [101]. The polymer is in the reduced state at -1 V and becomes oxidized at 0 V vs. Ag/AgCl [94,97]. Fig. 7.1 (b) shows photomicrographs of two fabricated microvials with their lids in the opened and closed positions corresponding to the two electrochemical states of the polymer. The electrochemical reaction requires a maximum current density on the order of $10 \text{ pA}/\mu\text{m}^2$ for actuation.

7.1.2 Prototype testing

The first generation cell clinics prototype comprised a CMOS chip with an array of bioamplifiers connected to on-chip cell sensing electrodes and an array of MEMS structures comprising lidded microvials. The amplifiers were tested by recording the extracellular electrical potentials from bovine aortic smooth mus-

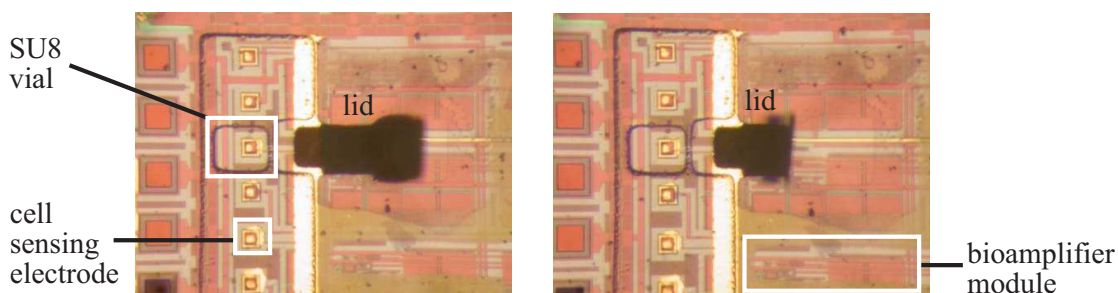


Figure 7.2: Prototype microstructures fabricated on a custom CMOS bioamplifier chip [Photographs courtesy of Y. Liu and Dr. E. Smela].

cle cells on a packaged bioamplifier chip (without any MEMS structures) [5, 19]. The MEMS structures were tested by fabricating prototype microstructures on the bioamplifier chip. The function of the bilayer actuators was demonstrated by placing the chip in an electrolyte solution, making electrical connection to the chip surface through a micromanipulator probe, and applying voltages between 0 and -1 V vs. Ag/AgCl using an external potentiostat. Fig. 7.2 shows the resulting actuation of the microvial lid [fabrication and testing was performed by Y. Liu]. A vial is positioned around a gold-plated sensing electrode, visible as a small square. The PPy/Au bilayer hinge was successfully actuated, as shown by the different positions of the lid in these images.

7.2 Potentiostat basics

7.2.1 Electrochemical cell

An electrochemical cell [64] comprises a set of electrodes immersed in an electrolyte. An electric current resulting from a net movement of charged species through the cell gives rise to an electrochemical reaction. Electrons are the charge

carriers in the electrodes and ions constitute the charge carriers in the electrolyte.

An electrochemical cell typically comprises a set of three electrodes:

- Working electrode (WE) [64]: This provides the surface on which the electrochemical reaction occurs. It is made of an inert material such as gold or platinum.
- Reference electrode (RE) [64]: This is the electrode with reference to which a control potential is applied to the WE for the electrochemical reaction to occur. It is to be connected to a high impedance node allowing no current to flow through it. Saturated Calomel Electrode (SCE) and Silver/Silver Chloride (Ag/AgCl) electrodes [64] are the standard REs used in laboratory applications. Field applications normally employ pseudo REs made of inert materials.
- Counter electrode (CE) [64]: The current that enters the electrolyte through the WE exits through the CE or vice versa. Laboratory applications employ inert conductors such as platinum or graphite as CEs. Field applications employ another piece of WE as the CE.

In the cell clinics microsystem the on-chip PPy/Au microactuator behaves as the WE in the electrochemical cell. For the first generation prototype testing, the PPy/Au bilayer was actuated by employing an off-chip Ag/AgCl RE and an off-chip Ag CE, in 0.1 M NaDBS electrolyte.

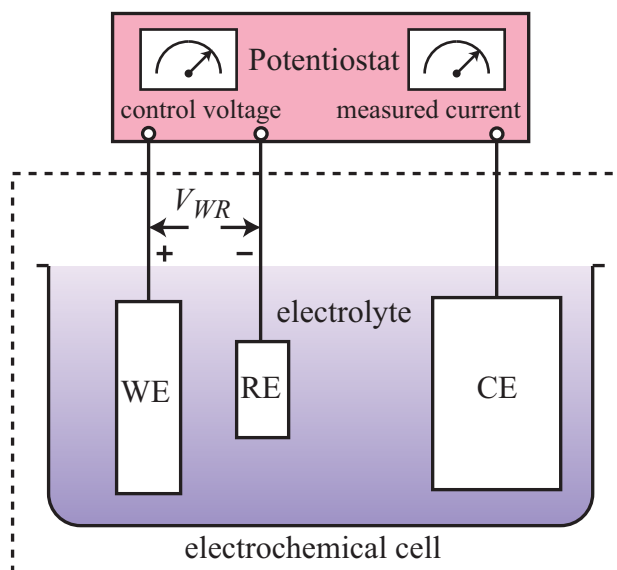


Figure 7.3: An illustration showing an electrochemical cell connected to a potentiostat instrument.

7.2.2 Potentiostat instrument

A potentiostat is an electronic instrument used to control the reaction in an electrochemical cell [102]. It controls the current between the WE and CE, so that the potential V_{WR} of the WE relative to the RE follows a required control voltage. At any instant the potential applied to the WE is maintained at the control voltage, irrespective of the ongoing electrochemical reaction. Fig. 7.3 shows the connection between an electrochemical cell in a typical three electrode configuration and a potentiostat.

Chapter 8

Integrated Potentiostat Design

Previous reports on integrated potentiostats have demonstrated their utility in electrochemical sensors for detecting minute concentrations of biochemical analytes [103–108]. The potentiostats primarily served as current measurement instruments for precise low-level current detection (nA to pA) with low noise. In recent years a new class of applications have emerged that employ electrochemical actuators for capturing, manipulating, and positioning of objects in the micro-regime [109, 110]. The control of such microactuators requires a modified design for the potentiostat, giving it the ability to robustly drive relatively high currents (μA to mA) with accurate voltage control and low output distortion. This work demonstrates such a CMOS potentiostat and its use for *in situ* control of the electrochemical oxidation level, and thus the volume, of an electroactive polymer film. The integrated control technique can enable complete miniaturization of a variety of electrochemical microsystems for micromanipulation [98, 110], cell clinics [5, 6, 99], drug delivery [111], and combinatorial electrodeposition of materials [112]. For the cell clinics application the potentiostat serves to drive the PPy/Au bilayer microactuators. Lid actuation requires the application of a control voltage, which was provided by an external potentiostat instrument in the first generation of cell clinics. In order to reduce system complexity, this research contributes a custom VLSI

potentiostat for control of, and integration with the MEMS structures.

8.1 Implemented potentiostat architecture

All potentiostats follow a common control architecture, but with various constraints or additional circuit elements depending on the application. A potentiostat mainly comprises two functional units: (i) a core control unit that maintains a set desired potential difference between the working and reference electrodes by sourcing or sinking a current through the counter electrode, the value of which is regulated by a feedback mechanism, and (ii) a current-sensing unit that measures the current flowing through the cell for electrochemical analysis or detection [102]. Microactuator control requires a control unit that exhibits good accuracy, robust driving, and stability, while current-measurement requirements are less demanding, since the currents are relatively large. One of the key constraints on the potentiostat for our target cell clinics is minimal footprint on the chip, since the chip must carry out many other functions as well. In order to minimize area and power requirements, we have elected to integrate a single, compact driver for controlling an array of actuators, rather than a separate driver for each actuator. The control circuit follows the architecture of a single-ended amperometric potentiostat [29,30,102] Fig. 8.1(b) illustrates the working (WE), reference (RE) and counter (CE) electrodes, and the associated circuitry. The circuit architecture implemented is that of a traditional single-ended amperometric potentiostat [113]. Fig. 8.1(b) illustrates the connection between the electrodes and the associated control circuitry.

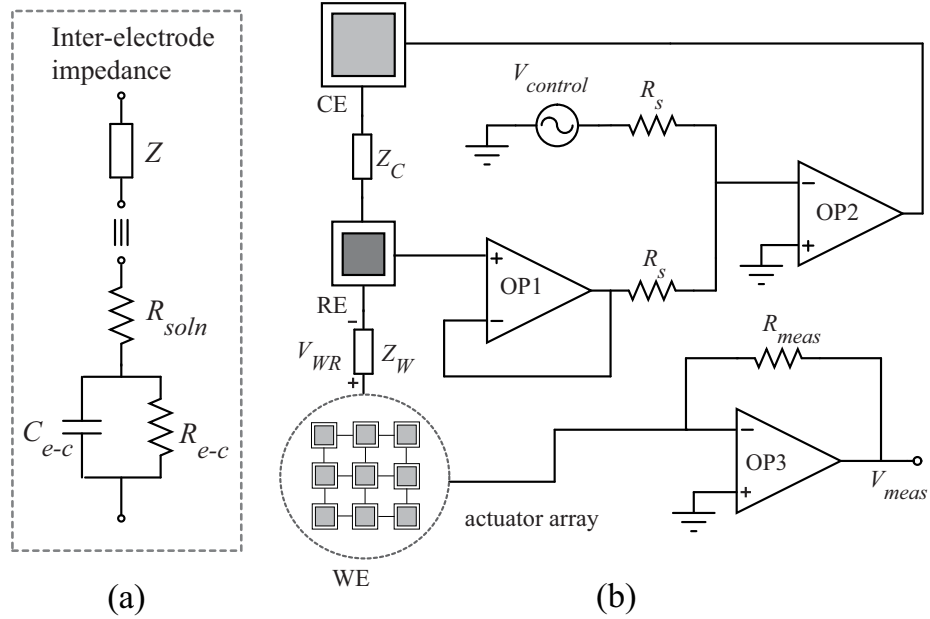


Figure 8.1: (a) A model for the interelectrode impedance. (b) Potentiostat circuit for integration with the microactuators.

The control circuitry comprises three operational amplifiers:

- OP1 buffers the electrochemical reference potential in the feedback control loop. It provides a high input impedance to the RE, keeping the reference chemical reaction at equilibrium and allowing no current to flow through it.
- OP2 sources/sinks the current specified by the control voltage to/from the counter electrode to enable the reduction/oxidation reaction.
- OP3, along with the off-chip feedback resistance R_{meas} , operates as a current-to-voltage converter for measuring the current flowing through the electrochemical cell, and also provides a virtual ground potential at the WE. Current measurement using R_{meas} is required to determine the voltage range for actuation from oxidation and reduction peaks obtained using cyclic voltammetry. The value of R_{meas} is determined by the range of currents to be measured.

Z_C denotes the impedance between CE and RE, and Z_W denotes the impedance between WE and RE. The electrical impedances Z_C and Z_W are formed by a series combination of the solution resistance R_{soln} and the electrode impedance Z_{e-c} that arises from charging of the double layer capacitance (modeled by C_{e-c}) and electron transfer resistance (modeled by R_{e-c}) at the electrode-electrolyte interface. This is illustrated in Fig. 8.1 (a).

The transfer function from the source control voltage $V_{control}$ to the electrochemical cell potential V_{WR} can be written as:

$$\frac{V_{WR}}{V_{control}} = \frac{A_2 Z_W}{A_2 Z_W + 2(Z_C + Z_W)} \quad (8.1)$$

where A_2 is the gain of op-amp OP2. The circuit ensures that the electrochemical cell voltage V_{WR} tracks the source control voltage $V_{control}$, provided A_2 is high enough.

8.2 Wide swing op-amp design for microactuator control

The potentiostat implementation requires an op-amp that satisfies the following specifications for driving electrochemical actuators:

- High gain (>50 dB) to maintain the desired electrochemical cell potential.
- Phase margin > 60° for stable operation.
- Rail-to-rail inputs and outputs to maximize the range of the electrochemical potentials that can be applied.
- High current handling capability for parallel driving and control of actuator

arrays. For example, the PPy(DBS)-based electrochemical reaction requires peak current densities on the order of $10 \text{ pA}/\mu\text{m}^2$ for actuation. In this case the op-amp could be required to source or sink currents up to 1 mA while driving an array of PPy(DBS)/Au actuators [94].

- Low output distortion for accurate voltage tracking during electrochemical control.

A custom wide-swing op-amp has been designed using the topology shown in Fig. 8.2. It consists of a rail-to-rail input stage, a summing circuit, and a rail-to-rail output stage with feedforward class-AB control [79]. The NMOS input pair M1-M2 and the PMOS input pair M3-M4 together constitute the rail-to-rail input stage. In the low common-mode input voltage range the PMOS input pair is active, in the intermediate common-mode input voltage range both NMOS and PMOS input pairs are active and in the high common-mode input voltage range the NMOS input pair is active. In order to preserve the rail-to-rail capability, the complementary input pairs are loaded with folded cascodes formed by transistors M14-M17 and M18-M21. The diode-connected transistors M5 and M6 in the input stage provide a constant voltage source across the complementary input transistor pairs in order to reduce transconductance variation across the input common mode voltage range. This is required for optimal frequency compensation and reduced signal distortion. The output stage is biased in the class-AB mode by maintaining a constant voltage difference between the gates of the output transistors M29 and M33. The biasing is provided by a feedforward class-AB control circuit formed by transistors M28

and M32. The class-AB control is combined with the summing circuit formed by transistors M14-M17 and M18-M21. Transistors M24-M25 form a floating current source. The class-AB control sets up two translinear loops, M26-M29 and M30-M33 which fix the voltage between the gates of M29 and M33. The rail-to-rail output stage with feedforward class-AB control provides a good compromise between power efficiency and output signal cross-over distortion for a given supply power [79]. The output transistors M29 and M33 are suitably sized for supporting high current drives of up to 1 mA.

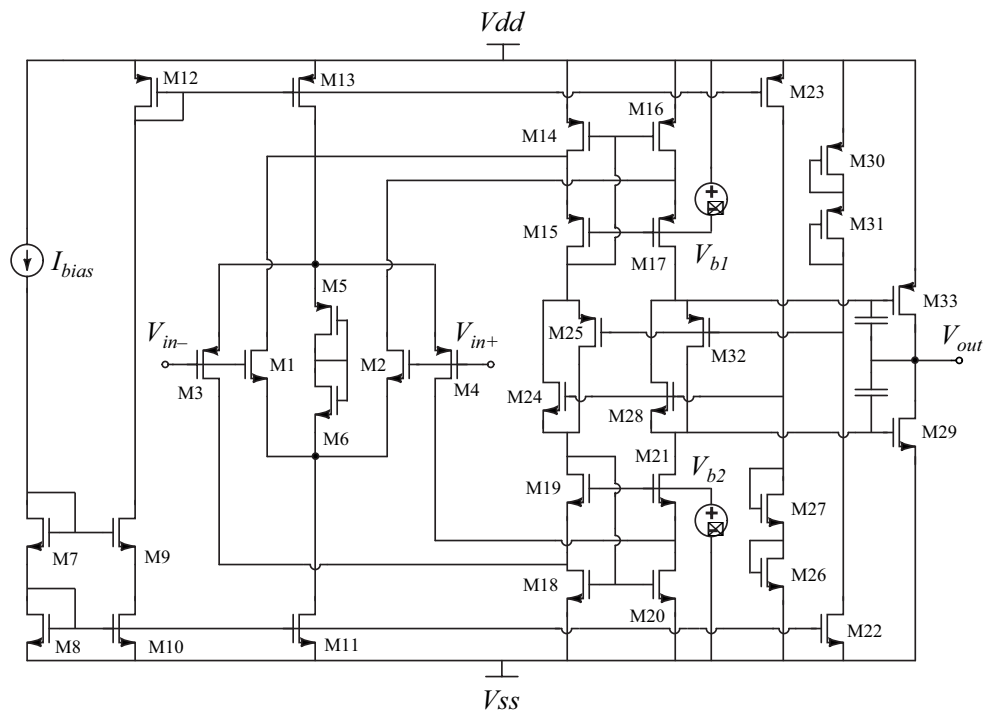


Figure 8.2: Rail-to-rail operational amplifier constituting the potentiostat.

The op-amp circuit was designed and fabricated in a commercially available $0.5 \mu\text{m}$, 2-poly, 3-metal standard CMOS technology for a supply voltage of $\pm 1.5 \text{ V}$. Table 8.1 summarizes the performance metrics [80] for the op-amp obtained from bench testing.

Table 8.1: Performance metrics of the operational amplifier

Parameter	Value	Unit
On-chip area	0.021	mm ²
Open loop gain	66	dB
3 dB bandwidth	3.5	kHz
Phase margin	85	°
Unity gain frequency	2	MHz
CMRR	110	dB
Slew rate ($R_L=1\text{ M}\Omega$, $C_L=95\text{ pF}$)	7.5	V/ μ s

8.3 Potentiostat test chip

The potentiostat chip implements the control circuit of Fig. 8.1(b) connected to on-chip microelectrodes: 6 WEs measuring $100\times 100\text{ }\mu\text{m}^2$ each (for a total area of $6\times 10^4\text{ }\mu\text{m}^2$, a CE measuring $400\times 800\text{ }\mu\text{m}^2$, and a RE measuring $50\times 800\text{ }\mu\text{m}^2$.

Fig. 8.3(a) shows a photomicrograph of the fabricated chip.

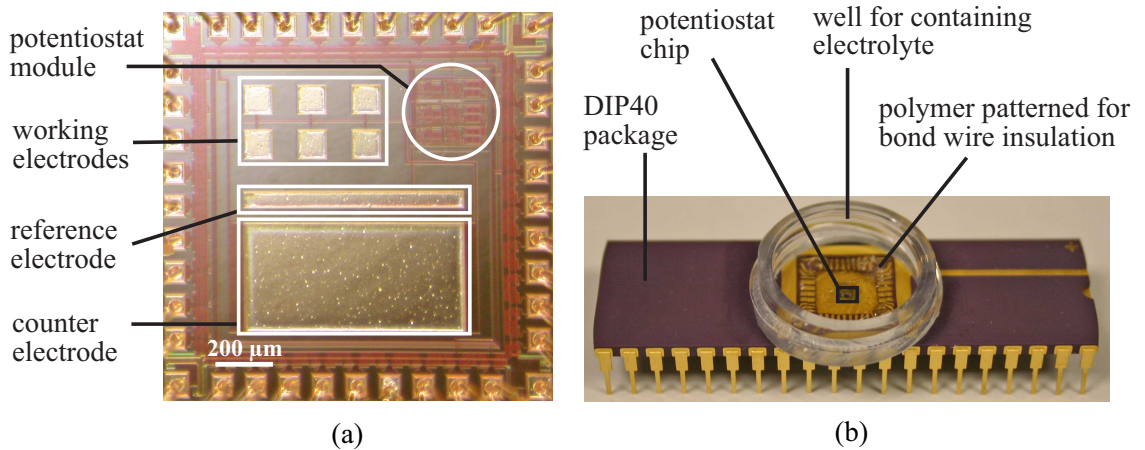


Figure 8.3: (a) Photomicrograph of the fabricated chip comprising the potentiostat module integrated with the microelectrodes constituting the electrochemical cell. (b) Photograph of a fully packaged potentiostat test fixture after postprocessing.

The RE is placed close to the WEs in order to minimize the voltage drop across the RE/WE electrolyte resistances. The CE area has been maximized in order to allow sufficient current flow during actuation. The WEs mimic the actuator array that will be employed in the cell clinics; after post-processing of the chip they comprise the same materials and have the same areas as the cell clinic actuators. The chip, measuring $1.5 \times 1.5 \text{ mm}^2$, was fabricated in a commercially-available $0.5 \text{ }\mu\text{m}$, 2-poly, 3-metal CMOS process. The on-chip area of the potentiostat circuit is $7.07 \times 10^4 \text{ }\mu\text{m}^2$ (6% of the active chip area). The electrodes were fabricated using the top metal layer in the CMOS process, with the aluminum exposed using glass cuts, or openings in the passivation layer which are commonly used to create bond pads for external connections via bonding wires. In addition to the internal connections shown in Fig. 8.3(a), the electrodes are connected to bond pads that permit external connections to be made during electrodeposition of polymer films.

The driver circuit can be employed to control the actuators either in parallel for all actuators or sequentially for individual actuators. Sequential control requires the working electrodes to be addressed through a switching network that is controlled by a decoder circuit. Since the potentiostat can also be employed for electrodeposition, sequential control can enable on-chip combinatorial electrochemistry.

Chapter 9

CMOS/MEMS Integration & Testing

9.1 Validating potentiostat operation by cycling an off-chip PPy(DBS) film in a standard electrochemical cell

The potentiostat chip was tested for actuation of an off-chip PPy(DBS) film of area 2 cm^2 with thickness 2000 \AA on a gold-covered silicon substrate in 0.1 M NaDBS solution [PPy(DBS) sample was prepared by M. Urdaneta. Electrochemical cell was set up by M. Urdaneta]. PPy(DBS) is electrochromic, so it changes color during oxidation and reduction [92]. The cycling test was performed by connecting the working electrode pin of the on-chip potentiostat to an exposed gold region of the PPy(DBS) sample, the reference electrode pin to an external Ag/AgCl electrode, and the counter electrode pin to an external graphite electrode [Chip testing was performed along with M. Urdaneta]. A signal generator was used to ramp the control potential linearly at 100 mV/sec between 0 and -1 V .

As shown by the photographs in Fig. 9.1, in every cycling period the film was observed to change from salmon color (oxidation at 0 V vs. Ag/AgCl), to transparent (reduction at -1 V vs. Ag/AgCl), confirming the electrochemical reaction of the film [Color changes were observed along with M. Urdaneta]. The color observed at 0 V is due to optical interference, and is thus a function of the PPy film thickness.

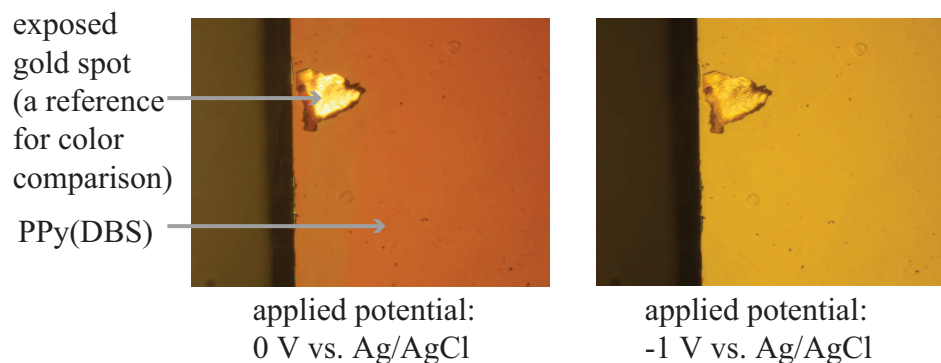


Figure 9.1: Color change observed during cycling of the PPy(DBS) film using the on-chip potentiostat [Photographs were captured along with M. Urdaneta].

PPy itself is brown in the oxidized state, appearing darker with increasing thickness. Fig. 9.2 shows the cyclic voltammogram (CV, a plot of current vs. voltage) obtained. The CV shows current peaks at -0.6 V and -0.4 V (vs. Ag/AgCl), which are typically observed during the reduction and oxidation of PPy(DBS). To validate the operation of the potentiostat chip, the cycling experiment was repeated using an external potentiostat (EcoChemie pgstat30) [Validation experiment was performed along with M. Urdaneta]. The CV obtained using the external potentiostat has been superimposed upon the CV obtained using the on-chip potentiostat in Fig. 9.2. There is good agreement between the CVs obtained from the external and on-chip potentiostats. The reason for the 2 plots to be not exactly identical to each other could be the disturbance in the electrode positions when the connections were changed from the on-chip potentiostat to the external potentiostat instrument.

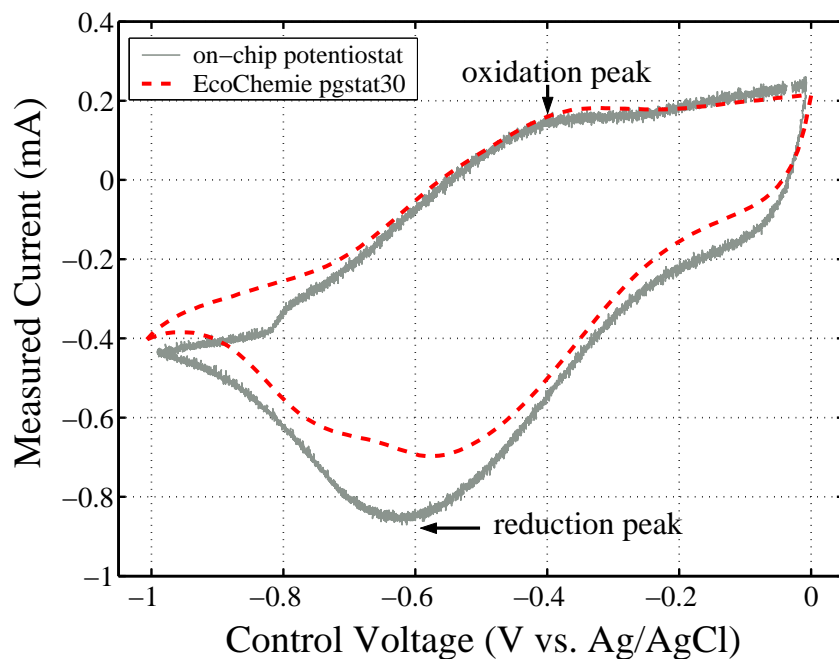


Figure 9.2: Cyclic voltammograms obtained during electrochemical cycling at 100 mV/sec of a PPy(DBS) film using the on-chip potentiostat and an external potentiostat (EcoChemie pgstat30) [Cyclic voltammograms were recorded along with M. Urdaneta].

9.2 Potentiostat testing for control of an off-chip array of PPy(DBS)/Au lidded microactuators in a standard electrochemical cell

The on-chip potentiostat was further tested for the actuation of PPy/Au bilayer microactuators with lids comprising a top SU8 layer and a bottom gold layer [Microactuators were fabricated by Dr. M. Christophersen]. The fabrication and characterization of these microactuators is described in [5, 94, 97]. The actuation test was performed on an array of 416 microactuators with varying hinge lengths ranging from 20 μm to 800 μm . All microactuators had a PPy thickness of 3000 \AA and a gold thickness of 1000 \AA . The array samples were placed face-up and flat in a custom-fabricated electrochemical cell. A graphite plate was used as the counter

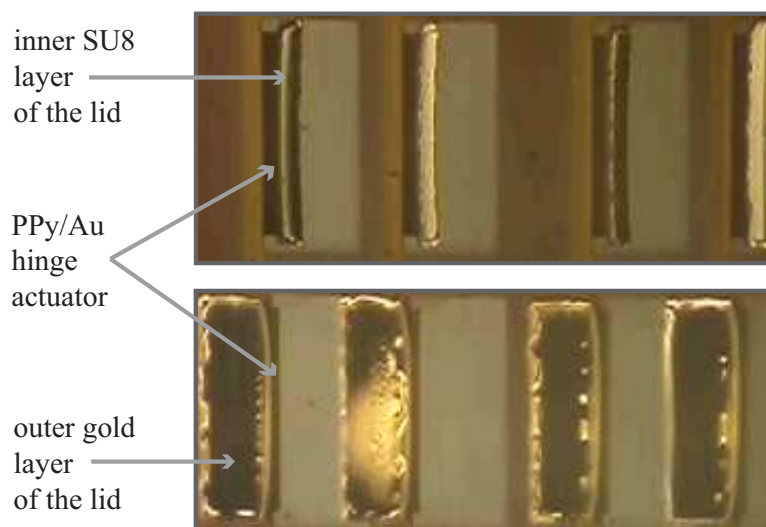


Figure 9.3: Photomicrographs of a portion of the actuated array of actuators [Photomicrographs and videos were captured by Dr. M. Christophersen]. Top, lids open (at -1 V vs. Ag/AgCl) and bottom, lids closed (at 0 V vs. Ag/AgCl).

electrode along with an external Ag/AgCl reference electrode [Electrochemical cell was set up by Dr. M. Christophersen]. Actuators were viewed from directly overhead using a Leica Z16 APO stereomicroscope.

Actuation of the microactuator samples was performed using the on-chip potentiostat by applying a cyclic control potential between 0 and -1 V (vs. Ag/AgCl) at 0.25 Hz (500 mV/sec) in 0.1 M NaDBS [Chip testing was performed along with Dr. M. Christophersen]. The actuators rotated the lids from 90° (open position) to 180° (closed position) during the cycling. Fig. 9.3 shows a photomicrograph of part of the array of actuators with a bilayer hinge length of 600 μm . When the cycling was performed at a lower frequency of 0.01 Hz (20 mV/sec), the actuators rotated the lids from 0° (open position) to 180° (closed position).

9.3 Demonstrating *in situ* control of on-chip PPy(DBS)/Au lidless microactuators

9.3.1 Chip postprocessing

To enable deposition of PPy(DBS) and to avoid corrosion, all the aluminum electrodes on the potentiostat chip (described in the previous chapter) were electrolessly plated with gold [Electroless gold-plating of on-chip electrodes was performed by M. Urdaneta]. Another purpose for the gold-plating is to make the on-chip electrodes biocompatible for the cell clinics application. The chip was immersed in a series of solutions for surface treatment (TAS 3Z, Technic Inc., Cranston, RI, USA), nickel deposition (EN 2600 A and B, Technic Inc., Cranston, RI, USA), and gold deposition (Oromerse SO, Technic Inc., Cranston, RI, USA). Approximately $1.5\ \mu\text{m}$ of nickel was deposited to prepare the surface for the subsequent $1\ \mu\text{m}$ of gold. All solutions were prepared and used according to the manufacturer's instructions.

Since the electrochemical reaction occurs in an aqueous ionic environment, the chip bond wires needed to be insulated from each other and the conducting electrolyte. The wirebonds were encapsulated using a photopatternable polymer (Loctite 3340, Henkel, Rocky Hill, CT, USA) such that the active chip surface was exposed, as described by Delille et al. [70] [Chip encapsulation was performed by M. Urdaneta]. Using epoxy, a well was placed over the encapsulation for containing $\sim 500\ \mu\text{L}$ of electrolyte. Fig. 8.3(b) in the previous chapter shows a photograph of a fully packaged potentiostat chip.

PPy(DBS) films were deposited using an external potentiostat instrument (EcoChemie pgstat30, Autolab, Westbury, NY, USA). PPy(DBS) was electrodeposited in an aqueous 0.1 M NaDBS, 0.1 M pyrrole solution as described in [93, 94] [PPy(DBS) films were deposited by M. Urdaneta]. When using the external potentiostat, deposition was performed at a voltage of 0.48 V (vs. Ag/AgCl), and PPy(DBS) was deposited on both the WEs and the CE. The WEs here mimic the actuator array that will be employed in cell clinics. They comprise the same materials and have the same areas as the cell clinic actuators, the only difference being that they are lidless. Indicators of actuation in this experiment were instead color change and out-of-plane thickness change in the polymer films. The purpose of depositing PPy(DBS) on the CE was to provide a known electrochemical reaction with sufficient charge-delivery capability, rather than requiring pH-changing hydrolysis to supply the necessary current. PPy(DBS) on CE provides better charge transfer and also better control over the electrochemical reaction. Furthermore, PPy(DBS) has a large internal surface area due to its lamella structure [94, 114]. This helps to prevent the electrochemical reaction to be limited by the size ratio of WE and CE.

The chip employed a gold quasi-reference electrode (Au quasi-RE) because thin film Ag/AgCl REs have been found to be unstable for long-term applications [105]. It is well known that using a quasi-RE in an electrochemical cell can result in shifting of the oxidation and reduction peaks, and scaling of the cyclic voltammogram (CV), when compared to CVs obtained employing an Ag/AgCl RE [98]. So the control potential range for the actuation of PPy(DBS) had to be determined experimentally.

9.3.2 Test setup

The potentiostat chip was mounted on a test-board interfaced to a data acquisition system (National Instruments DAQCard-6036E interfaced to a laptop running Labview 7.1). An Agilent 33220A arbitrary waveform generator was used to generate control potential signals. An off-chip resistance of 21.58 k Ω was used for current measurement. The chip was viewed from above using a Leica Z16 APO stereomicroscope. The electrolyte well was filled with 500 μ L of 0.1 M NaDBS solution. Images were recorded with a digital camera (Nikon Coolpix 995).

9.3.3 *In situ* PPy(DBS) actuation

The CMOS potentiostat was tested for actuating PPy(DBS) films on the 6 WEs that had been deposited using the external potentiostat instrument [Testing was performed along with M. Urdaneta and Dr. M. Christophersen]. Chip operation was demonstrated by performing cyclic voltammetry at a scan rate of 40 mV/sec while monitoring the color of the films on the WEs and recording CVs. The applied voltage range was successively incremented until distinct electrochromic changes, as shown in Fig. 9.4, were observed [Instructions for application of control voltages were provided by Dr. M. Christophersen, Color changes observed along with M. Urdaneta and Dr. M. Christophersen]. The final voltage range for complete electrochemical cycling was between +200 mV (oxidized, dark brown color) and -200 mV (reduced, light orange color). Thus, the chip was able to actuate the polymer films *in situ*.

Fig. 9.5 shows the CVs, which were recorded over 135 cycles at a sampling rate

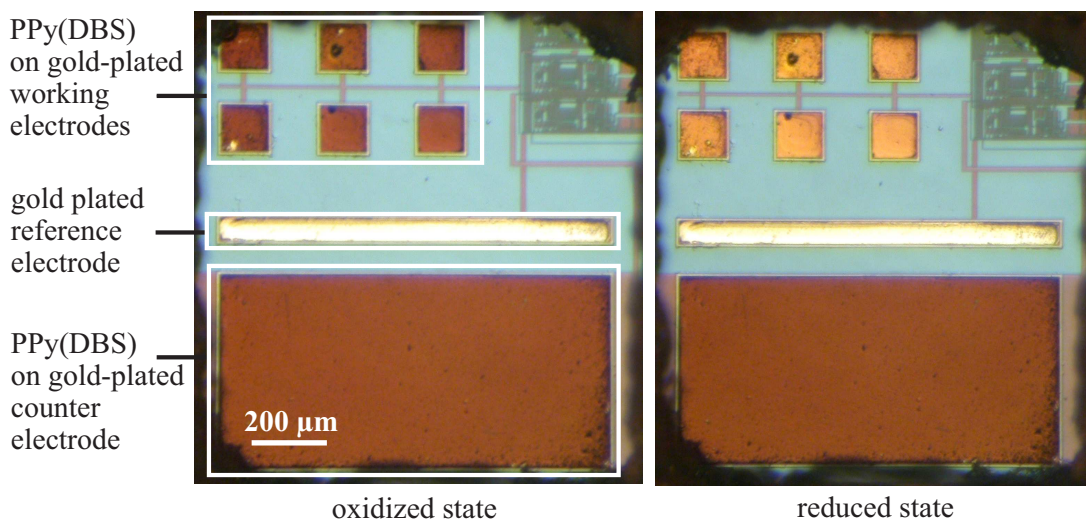


Figure 9.4: *In situ* cycling of PPy(DBS) films on gold-plated WEs using the on-chip potentiostat connected to an external waveform generator [Photomicrographs were captured along with M. Urdaneta and Dr. M. Christophersen]. Left, PPy(DBS) in the oxidized state. Right, PPy(DBS) in the reduced state.

of 50 Hz. The data were time-averaged over every 5 points, and across every 3 cycles, to produce the 45 traces in the figure. There are distinct oxidation and reduction current peaks at +40 mV and -85 mV (vs. Au) respectively. However, as expected, due to the quasi-RE, the oxidation/reduction peaks were shifted; vs. Ag/AgCl they typically appear at -0.4 V (oxidation) and -0.6 V (reduction). Mean oxidation and reduction peak currents of $1.0 \mu\text{A}$ and $2.5 \mu\text{A}$ were recorded during the cycling. These currents correspond to current densities of $16.7 \text{ pA}/\mu\text{m}^2$ and $41.7 \text{ pA}/\mu\text{m}^2$, which are comparable to those observed in standard macroscale setups. Peak currents on the order of 1 mA were recorded in the previous experiment when the potentiostat was used to drive an array of PPy(DBS)/Au microactuators fabricated on an off-chip substrate [29]. The shape of the CVs also resemble those obtained from measurements of PPy samples using external potentiostat instruments.

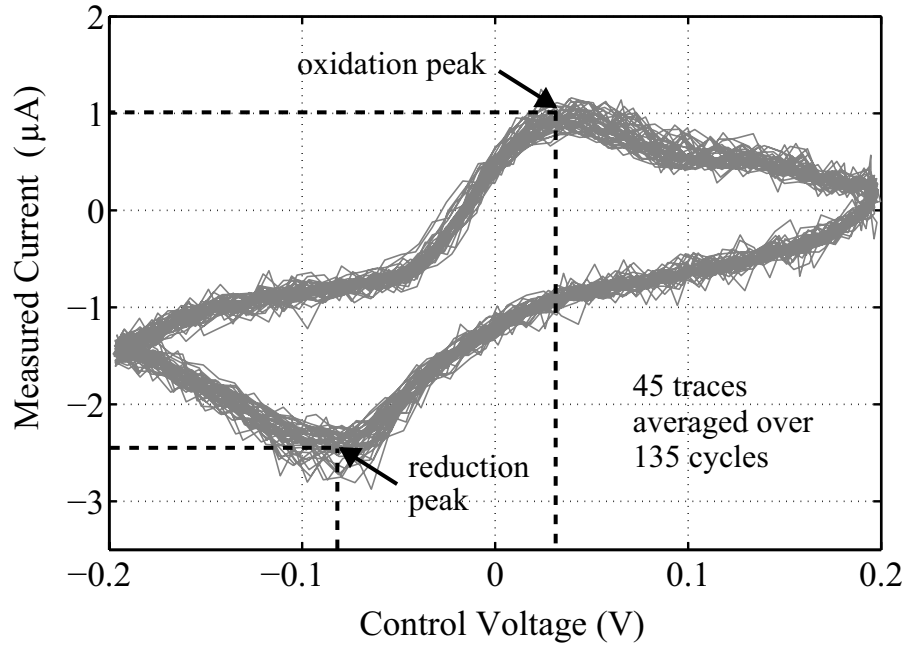


Figure 9.5: Cyclic voltammograms recorded during *in situ* oxidation and reduction of PPy(DBS) films [Cyclic voltammograms were recorded along with M. Urdaneta and Dr. M. Christophersen].

9.3.4 *In situ* PPy(DBS) deposition

Cycling was also performed on PPy(DBS) films deposited *in situ* using the potentiostat chip [Experiment was performed along with M. Urdaneta]. In this experiment, the CE was not covered with PPy(DBS) since it is unfeasible to do that using the on-chip circuitry. Electrodeposition was performed potentiostatically at +250 mV (vs. Au) for 20 minutes. Polymer deposition on the WEs was observed visually. The polymer films were then cycled, and the typical current peaks and electrochromic changes were observed.

9.4 Summary

A CMOS potentiostat chip was designed for driving *in situ* electrochemistry, for applications such as the deposition and control of electroactive polymer films. This was the first demonstration of such an integrated system. The potentiostat module was tested and validated for off-chip actuation of PPy(DBS) films and PPy/Au bilayer microactuators. The control circuit was then tested for both the deposition and actuation of PPy(DBS) films *in situ* on the CMOS chip, as confirmed by the distinct electrochromic changes observed during electrochemical cycling and the recorded CVs. The data confirmed that the chip met its design goals for the required current drive together with accurate voltage control.

Chapter 10

Conclusions: Part II

A CMOS potentiostat chip was designed for *in situ* driving of electrochemical actuation reactions. The operational amplifier constituting the potentiostat was custom-designed according to the specifications for the electrochemical control of PPy(DBS), an electroactive polymer. The employed circuit architecture enables rail-to-rail operation and robust current driving in addition to providing a good compromise between power efficiency and output signal cross-over distortion. The potentiostat module was tested for control of both off-chip lidded and on-chip lidless PPy/Au bilayer microactuators. An estimate for the maximum microactuator array size that the potentiostat will be able to drive in parallel is approximately 1000. The operational amplifier currently consumes 660 μW of power, with the output driving stage consuming 72% of the total power. The power consumption the operational amplifier output stage can be scaled according to the microactuator array size in future designs.

Control of on-chip actuators was demonstrated by employing a Au-plated quasi-reference electrode. This simplified post-processing, but required experimental determination of the control voltage range for achieving optimal actuation. Since the control voltage range is expected to change over time in the presence of a quasi-reference electrode, this step needs to be automated. This can be accomplished

by incorporating peak detection circuitry [115] along with the potentiostat module. This way, the current peaks in the cyclic voltammograms can be detected and compared on-chip, and the appropriate control voltage range can be set automatically.

The current target application for the integrated potentiostat demonstrated here is to drive and control PPy(DBS)/Au-based lidded actuators in the cell clinics microsystem. Another potential application of the integrated electrochemical reactor is drug delivery, wherein drug dosage can be regulated by electrochemical control of electroactive polymers within which the drug molecules are stored [111]. Because of their electrochromic behavior, conjugated polymers are used in display applications [116, 117]; therefore the potentiostat and electroactive polymer film system presented here can also be considered as a fully integrated demonstration of electroactive polymer display technology. *In situ* fabrication capability using the on-chip potentiostat may also enable novel applications such as combinatorial electrochemical deposition [118], automated postprocessing [119] after CMOS fabrication, and reconfigurable implants [120].

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