ABSTRACT

Title of dissertation: HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS FOR MODERN SATELLITE RECEIVERS: DESIGN VERIFICATION TEST AND SENSITIVITY ANALYSIS

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Mixed-signal System-on-chip devices such as analog-to-digital converters (ADC) have become increasingly prevalent in the semiconductor industry. Since the complexity and applications are different for each device, complex testing and characterization methods are required. Specifically, signal integrity in I/O interfaces requires that standard RF design and test techniques must be integrated into mixed signal processes. While such techniques may be difficult to implement, on-chip test-vehicles and RF circuitry offer the possibility of wireless approaches to chip testing. This would eliminate expensive wafer probing solution to verify the design of high-speed ADC functionality currently required for high-speed product evaluation.

This thesis describes a new high-speed analog-to-digital converter test methodology. The target systems used on-chip digital de-multiplexing and clock distribution. A detail sequence of performance testing operations is presented. Digital

outputs are post processed and fed into a computer-aided ADC performance characterization tool which is custom-developed in a MATLAB GUI. The problems of high sampling rate ADC testing are described. The test methodologies described reduce test costs and overcome many test hardware limitations. As our focus is on satellite receiver systems, we emphasize the measurement of inter-modulation distortion and effective resolution bandwidth. As a primary characterization component, Fourier analysis is used and we address the issue of sample window adjustment to eliminate spectral leakage and false spur generation. A 6-bit 800 MSamples/sec dual channel SiGe-based ADC is used as a target example and investigated on the corner lot process variations to determine the impact of process variations and the sensitivity of the ADCs to critical process parameter variations.

# HIGH-SPEED ANALOG-TO-DIGITAL CONVERTERS FOR MODERN SATELLITE RECEIVERS: DESIGN VERIFICATION TEST AND SENSITIVITY ANALYSIS

by

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# Preface

This work is about the design verification and production test methodologies for high-speed analog-to digital converters(ADCs), which is an example of system-on-chip devices. It came to our attention that there are few references available to enlighten the design/test engineer on the concepts of design verification and production testing of high-speed ADC system-on-a-chip (SoC) devices. The research intention developed here is to link RF design and test concepts to mixed-signal SoC testing for developing high-speed ADCs.

Throughout this research, we define any system whose operation requires a 100 MHz or faster system clock as a "high-speed" or "high-sampling" system. In the digital output of ADCs, we refer to any system requiring greater than or equal to 8-bits as "high-accuracy." Under the topic of high-speed ADCs, there are three major categories of both analog and digital: design, testability, and sensitivity. ADC design and testability is closely related to ADC input and output interface configurations. ADC sensitivities are more related to a semiconductor process technology and to design maturity.

Indeed, many component descriptions presented here are based on the conventional ADC characterization and ADC design. We extend these to the more capable ADC design verification methodologies for a modern satellite receiver that are the

subject of the dissertation. These research topics are taken two steps further:

- Describing a new cost effective dynamic test methodology;
- Explaining how to implement design verification and production testing solutions for high-sampling rate ADCs.

Test and measurement are both unique and exceptionally important to the development of modern electronics technology. Tests and measurements of RF/mixed-signal and SoC devices are routine bench-top activities in laboratories, but design verification and production tests add more complexities and constraints to perform those tests and measurements while maintaining the same level of quality. It is erroneously thought that testing is a "low technology" arena that is well understood. Current day integrated circuits (ICs) must merge analog and digital function and operate in the millimeter wave regime. RF design techniques must be brought to bear at all levels of design. Simply getting test signals into such systems is a challenge and to recover the circuit response without distortion is more of a challenge. In the past, most effort was devoted to chip design and fabrication. The result was a product that was not factory testable - a guaranteed failure in the field.

This work merges high-speed ADC design approaches with "design for testability." It is a primal target to provide a test stand capable of evaluating analog-to-digital converter systems designed to sample at a rate near a giga-sample per second or faster. Exploring the limits of performance of high sampling rate ADC (high-speed mixed signal ICs) is also a part of the work. Throughout this work, novel test

methodologies are highlighted. This research is intended to show the step-by-step approach to high-speed ADC design verification and production tests to help many of ADC design engineer in both industry and academia.

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# Dedication

*To my loving parents for being the best parents that any son could wish for.*
*I would be lost without their love and guidance.*

*To my wise brother and beautiful sisters,*
*who define strength and determinations.*

♣

*You always believe in me.*

*I love you all*
*and*
*Thank you to teach me how to appreciate all that my life hands to me.*

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collaboration.

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# List of Abbreviations

| | |
|---|---|
| ADC | Analog-to-digital converter |
| AGC | Automatic Gain Controller |
| ASIC | Application Specific Integrated Circuit |
| ATE | Automated Test Equipment |
| AWG | Arbitrary Waveform Generator |
| BJT | Bipolar Junction Transistor |
| BER | Bit Error Rate |
| BIST | Built-in Self Test |
| BPF | Bandpass Filter |
| CDM | Charge Distribution Model |
| CE | Concurrent Engineering |
| CLK | Clock |
| CML | Current Mode Logic |
| COTS | Commercial Off The Shelf |
| CW | Continuous Wave |
| DAC | Digital-to-analog converter |
| dBm | dB refereed 1 milli-Watt (mW) |
| dBFS | dB referred full-scale (0 dBFS is assigned to the maximum possible level) |
| DETS | Defect and Enhancement Tracking Systems |
| DFT | Discrete Fourier Transform |
| DfT | Design-for-Test |
| DIB | Device Interface Board |

| | |
|---|---|
| DIV | Divider |
| DLA | Digital Logic Analyzer |
| DNL | Differential Non-linearity |
| DRC | Design Rule Checking |
| DSP | Digital signal processing |
| DSO | Digital Storage Oscilloscope |
| DUT | Device Under Test |
| DVT | Design Verification Test |
| ECN | Engineering Change Notice |
| ENOB | Effective Number of Bits |
| EOC | End-of-conversion |
| EOS | Electrical Over Stress |
| ERB | Effective resolution bandwidth |
| ESD | Electrostatic Discharge |
| EVM | Error vector magnitude |
| FFT | Fast Fourier Transform |
| FSO | Final-sign-off |
| GND | Ground |
| GS/s | Giga-samples per second |
| GUI | Graphical User Interface |
| HBM | Human Body Model |
| HBT | Hetero Junction Transistor |
| HD | Harmonic Distortion |
| HVT | Hardware Verification Test |
| HLD | High level design or discription |
| HNS | Hughes Network Systems, LLC |
| IEC | International Electro-technical Commission |
| IEEE | Institute of Electrical and Electronic Engineers |
| INL | Integral Non-linearity |
| IMD | Intermodulation distortion |
| IP3 | $3^{rd}$ order Intercept point |
| ISO | International Organization for Standardization |
| JEDEC | Joint Electronic Device Engineering Council |
| LAB | Laboratory |

| | |
|---|---|
| LAN | Local Area Network |
| LFPM | Linear Feet per Minute |
| LLD | Low level design or description |
| LPF | Lowpass filter |
| LSB | Least significant bit |
| LVDS | Low Voltage Differential Signals |
| LVS | Layout versus schematic check |
| MSB | Most significant bit |
| MS/s | Mega-samples per second |
| PC | Personal Computer |
| PCB | Printed Circuit Board |
| PDF | Probability Density Function |
| PDK | Process Design Kit |
| PDR | Preliminary design review |
| RF | Radio frequency |
| SAR | Successive approximation resistor |
| SiGe | Silicon germanium |
| SINAD | Signal-to-noise-and-distortion ratio |
| SFDR | Spurious-free dynamic range |
| SNR | Signal-to-noise ratio |
| SoC | System-on-chip |
| SPR | System problem report |
| SVT | System Verification Test |
| THD | Total harmonic distortion |
| TQFN | Thin Quad Flat Pack |
| Voffset | ADC input offset voltage |
| VFS | Full scale ADC input voltage |
| VTS | Verification Test Software |

Chapter 1

# Introduction

## 1.1 Overview

This introduction establishes a general philosophy of system verification to serve as a guide for the work presented in the body of the thesis to follow. This is followed by a statement of the unique contributions this thesis makes to the fields of testing and system validation. The introduction concludes with a glossary of the many mysterious and arcane terms used as a jargon in these fields.

## 1.2 General philosophy for the validation of complex integrated systems

A mixed-signal system-on-chip (SoC) device is defined as a group of on-chip integrated subsystems consisting of both digital and analog elements, and their associated components. Generally, validation of complex integrate systems follows basic steps: (1) building prototype - SoC design data produced under the electronic design automation (EDA) or computer aid design (CAD) environment [4, 5]; (2) preparing event based test vectors based on the SoC design data produced in the EDA environment; (3) applying the event based test vectors derived from the SoC design data to the prototype silicon by an event based test system; and (4) evaluating the response output of the prototype silicon; and (5) modifying the event based test vectors to acquire desired response outputs from the silicon prototype; and (6) applying the modified event based test vectors to the EDA environment to modify the design data, thereby correcting design errors in the SoC design. Developing SoC devices or products requires numerous collaborations among design engineers, test engineers, product engineers, and system engineers. To have a fully characterized product for customers or for system applications, system engineers must define and document customer requirements so that the rest of the engineering team can design the product and successfully release their design to production. After the system engineers define the product technical requirements, the design engineers develop the corresponding integrated circuits according to the specified needs.

Test engineers generate hardware and software that will be used to guarantee the performance of each SoC product after fabrication. That is, they assess the safe-operating areas (SOAs) of chip bias and input range. They must also develop the hardware and software approaches necessary to adjust parameters like DC offset and AC gain, or to compensate for manufacturing defects, etc. They are also responsible for reducing the cost of the testing by test time reductions and cost-saving measurements.

We must be careful to state that testing is important from start to finish in the manufacturing of integrated circuits (ICs). First, test consideration is required early in the SoC design cycle. In the low frequency and static regimes of operation, "standard" sub-system parameter evaluations (such as voltage and current off-sets) must be characterized by testing in the design phase. System-specific information, such as linearity, for example, is also necessary for ADCs.

Second, we must provide quick, straight-forward methods for evaluating the functionality of large numbers of parts in the production phase of system development. One of the major problems encountered here is the large number of probes required at wafer-level test. This issue is addressed with the use of on-chip "RF reporting circuits." It must be noted that the testing of packaged chips is also a problem in volume production facilities. Characterizations and modeling of the packaged chips must be carefully conducted in order to reduce down parasitic due to the packages and on-board level systems in the test-vehicles. This thesis does

not address wafer-level probe testing for production in detail. Instead, the thesis concentrates on evaluating packaged chip testing both in the initial design release and production environments.

Nowadays, automated test equipment (ATE) is available from various commercial vendors, such as Teradyne, LTX, Agilent Technologies, and Schlumberger, etc. Common high-end ATE testers usually consist of three major components: a test head, a workstation, and the mainframe tester for production test [6, 7]. Basically, a workstation is the interface between a tester and the user. Test engineers build test programs and debug the programs. The mainframe consists of power supplies, measurement instruments and control computers for these components. Usually, the test head contains the most sensitive measurement electronics. A device interface board (DIB) can be included in the test head and plays an interface role between the ATE tester and the device under test (DUT). Successful SoC diagnosis and characterization depends on the design of electromechanical fixtures and on our ability to eliminate parasitics (such as stray inductance, and capacitance) introduced by the test apparatus.

There are differences between digital testing and mixed-signal testing [6]. Digital circuits can be tested as stand-alone units, but mixed-signal circuits are normally evaluated for their performance in system-level applications. For example, digital circuits such as AND gates, NAND gates, flip-flops, and counters can be tested by their logic levels and digital output. As a comparison, a particular mixed-signal sub-

circuit can be tested with a totally different suite of tests depending on its intended functionality in the system-level application. This thesis explains the detailed test and characterization procedures for full evaluation of a high-speed ADC and a novel compressing ADC as examples of mixed-signal SoCs. The author concentrates on the characterization of high speed data converters for telecommunication applications.

## 1.3 Motivation and objective

Mixed-signal integrated circuit test requirements have grown in complexity due to the expansion of the telecommunications, image-processing industries. Mixed-signal circuits, such as analog-to-digital converters (ADCs), are generally required in many advanced systems. In telecommunications (especially in modern satellite and digital radio receivers such used in ultra-wide-band (UWB) telecommunications) ADCs are used to sample the analog signals and to transfer them to the digital registers for base-band applications in high speed and high-resolution systems. There is much research in design prospects. However, testing high-speed ADCs is still a relatively unknown field compared with high-speed ADC design itself.

While the subjects of digital integrated circuit testing and testability have been covered in many books and references [8, 9, 10, 11], it is difficult, in practice, to find the best testing methods for analog and mixed-signal test and measurement. Testing SoCs for high frequency and wider bandwidth applications is normally a

lengthy, elaborate task. This is mainly because of the limitation of reference signal sources or the difficulty of creating testable circuit or system designs. For example, characterizing and testing ADCs require measurement of a large number of parameters to fully specify the performance of the system. The presence of both analog and digital signals often makes the test and characterization more difficult and challenging.

In addition, test equipment complexity and the breadth of expertise of the test engineer create hidden obstacles to characterizing and testing Mixed-signal SoCs. Demanding custom designed measurement systems are necessary for characterizing ADCs as mixed signal SoCs. It is challenging to come up with a complete characterization system for mixed-signal SoCs such as high speed data converters in modern satellite receiver applications. The performance of characterization equipment is frequently insufficient for the test at hand and the available tool base may differ from test site to test site. In this work, the characterizations and testing techniques are developed in response to limitations on test equipment for a high speed and wide bandwidth ADC and a compressing ADC.

Demystifying testing and characterization techniques for a high speed, broad bandwidth ADCs is the main goal of this thesis, as is merging standard analog and digital test techniques with "design-for-test" (DfT) methodology throughout the life of the ADC development. The thesis also intends to bridge Radio Frequency (RF) and microwave circuit design and test and measurement techniques to validate and

characterize high-speed ADC designs.

It is a primal target to provide a test stand capable of evaluating high-speed ADC systems in a modern satellite receiver. The work is intended to show the step-by-step approach to high-speed ADC design verification and production tests to help many of ADC design engineer in both industry and academia.

**Objective:**

To develop full production-ready cost effective design verification test methodology for the high-speed ADC used in modern satellite receivers, the following lists are summarizing what this research provides and accomplishes:

- Case study for a high-speed ADC:
  - Design-for-Test (DfT) enhanced approach
  - Testability
- Demystify high-speed ADC operation
- Develop concurrent engineering design verification test (DVT) procedures
- Provide a DVT program development (test flow or test plan) to serve as a basis for a verification test suite (VTS)
- Provide Cost-effective ATE solutions

## 1.4 Outline of thesis

Our main mixed-signal SoC test examples are linear/compressing ADCs (4-bit low-speed compressing ADCs and 8-bit high-speed linear ADCs). In this thesis, we focus on the required test parameter sets for modern satellite receiver applications.

In Chapter 1, general philosophy for validation of complex integrated circuits is introduced with research motivations and objectives to develop high-speed ADC design verification test techniques. Glossary terms for ADCs are also included.

Chapter 2 describes an overview of ADCs and ADC validation test requirements and prerequisite criteria to perform robust and cost-effective design verification tests from the prototype to the full production level testing. Successful product developments are based on concurrent engineering.

Chapter 3 presents the Design-for-Test(DfT) philosophy of high-speed ADC characterization in a modern satellite receiver. A general overview of testing ADC architectures and their operating principles are presented before the verification tests are detailed. Mixed signal circuits to be tested for telecommunication system applications are described .

Chapter 4 addresses the fixture and test bench setup requirements needed to characterize ADC performance. The high-speed ADC verification fixture design and subsystem periphery development are described with cost-effective interface between the ADC and the test equipment. In a high speed ADC prototype design environment, a robust test methodology and the selection of an adequate test fixture and

subsystem are significant parts of the ADC design process enabling mass production. Chapter 4 shows the test setup and test fixture designs to overcome the limitation for test equipment.

In Chapter 5, Design verification software development and detail test methodologies for high-speed ADCs are discussed. The ADC verification analysis software development is presented along with the test methodology. Testing limitations and difficulties are described. Developed a computer-aided ADC device verification software (VTS) tool consists of four major parts: sine wave power spectrum tests, linearity tests, error code tests and two-tone intermodulation (IMD) tests. The linearity test is described with a sine wave histogram test techniques to provide both the differential nonlinearity (DNL) and the integral nonlinearity (INL). A Fast Fourier transform (FFT) module, which is a workhorse of the sine wave power spectrum tests and the two-tone IMD tests, yields several critical ADC specifications, including the effective resolution bandwidth (ERB), analog power versus spurious free dynamic range (SFDR), effective number of bits (ENOB), and intermodulation destortion (IMD).

In this thesis, a common test setup configuration is used for the entire device verification test (DVT) process and a sine wave is primarily used as the analog input signal due to its easiness of generation and analysis. The advantages of using DSP routines for data analysis are mentioned. The detailed sequence of testing operations necessary for verification testing of high speed ADCs in modern commu-

nication systems. These results pave the way for future developments in the field of automated high speed ADC verification methodology. Various aspects such as hardware settings, testing programs, noise and jittering issues are discussed for high speed analog and mixed-signal SoC device testing. Tests and characterizing procedures for dynamic performance of a high speed ADC are proposed and bench test limitations and challenging factors are also discussed.

As ADC characterization routine, both static and dynamic test procedures are described so that ADC systems can be characterized. Both compressing and linear ADC's static and dynamic characterization procedures are described and the test results are shown each.

The production test of the fabricated high-speed ADC is also described in the end of Chapter 5. Test results are summarized as they apply to volume part fabrication. Necessity of system level test and wafer level test vehicle structures are also briefly addressed.

Chapter 6 shows that the sensitivity analysis of the designed high-speed ADC. Dynamic performances of high-speed (800 MS/s) dual channel 6-bit analog-to-digital converters (ADCs) were investigated and reported on the corner lot process variations to determine the impact of process variations. The ADCs sensitivity analysis results to critical process parameter variations provide ADC design limits.

Chapter 7 concludes the work on design verification test for the high-speed analog-to-digital converters in modern satellite receivers. The chapter summarizes

the research works and their achievements and contributions from the developed design verification test methodology and the test program. Future works are also addressed, so that further research can be extended based on the thesis.

## 1.5 Contributions

The thesis provides a generalized optimal high-speed ADC testing methodology in detail. The methodology is suitable for duplicating the test method and the results for testing reproducibility. Improved test methodology in dynamic performance of ADCs for satellite communications is employed with the device verification test software, VTS suite. The methodology is also developed so that less experienced personnel could perform the rigorous testing needed for proficient verification. Design-for-Test (DfT) concept are applied to succeed in the high-speed ADC design verification tests (DVTs) as a part of process from the design phase to the full productions.

The VTS suite developed in this dissertation has been delivered to Hughes Network Systems [12] and now is in wide spread use to validate their custom ADC ASIC and ADC system development project such as the *Thames* ASIC projects (dual channel 800 MSamples/sec 6-bit ADC ASIC projects).

The corner lot study of *Thames* ASIC projects is also reported for the first time to show the effects of ADC dynamic parameters due to the process variations.

## 1.6 Glossary of terms

The glossary provides a detailed description of AC dynamic performance terms related to high-speed ADCs and their ASIC. It also gives some insight into the test conditions these parameters are specified for.

ADC - Analog-to-Digital Converters, a device or circuit used to convert analog information to digital words.

Aliasing/Anti-aliasing - Conversion of an input frequency to another frequency as a result of the conversion processes. The output frequency of an ADC can not exceed a half of the sampling frequency of the ADC without aliasing. When the input frequency does exceed 1/2 the sampling frequency (Nyquist limit), the signal is folded back (aliasing) or replicated at other frequencies in the frequency spectrum above and below Nyquist (see also Nyquist Frequency). Caused by unwanted signal components above Nyquist, aliasing can be avoided by introducing front-end anti-aliasing filters to attenuate those signals.

Aperture Delay - Aperture delay is the time defined between the rising edge (50% point) of the sampling clock and the instant when an actual sample is taken.

Aperture Jitter - Aperture jitter is the sample-to-sample variation in the time between sampling events.

Aperture Width - Aperture width is the time that a track/hold (T/H) circuit requires to disconnect the hold capacitor from the input circuit (for example, to

turn off the sampling and put the T/H amplifier in hold mode).

Characteristic Impedance - The impedance a transmission line such that, when driven by a circuit with that output impedance, the line appears to be of infinite length such that it will have no standing waves, no reflections from the end and a constant ratio of voltage to current at a given frequency at every point on the line.

Corner Lots - Wafer fabrication where the process is deliberately skewed to produce either fast, or slow wafers so that ASIC performance can be physically evaluated at process extremes.

DNL - Differential Non-Linearity. The measure of the maximum deviation from the ideal step size of 1.00 LSB.

ENOB - Effective Number Of Bits. A specification that helps to quantify dynamic performance. ENOB says that the converter performs as if it were a theoretically perfect converter with a resolution of ENOB. That is, an ENOB of 5.4 says that the converter performs, as far as SINAD is concerned, as if it were a perfectly ideal ADC with a resolution of 5.4 bits (assuming you could have fractional bits). The idea behind ENOB comes from the fact that the absolutely perfect ADC has an SNR that comes only from quantization noise and has absolutely no distortion. When this is the case, SINAD is then equal to SNR. Since SNR of the absolutely perfect ADC is SNR $= 6.02 \times n + 1.76$,

where "$n$" is the number of ADC output data bits, SINAD = SNR for a perfect converter, so SINAD $= 6.02 \times n + 1.76$ and $n = (\text{SINAD} \times 1.76)/6.02$ and we say that ENOB = (SINAD $\times$ 1.76)/6.02 .

ERB - Effective-Resolution-Bandwidth. The ERB is the input frequency point where the SINAD has dropped 3dB (or ENOB 1/2 bit). The signal bandwidth is an important parameter for the ADCs. The ADC bandwidth is limited by the analog bandwidth of the input circuits and the sampling frequency of the ADC.

FFT - Fast Fourier Transform. The FFT is a mathematical operation that converts signals between the time and frequency domains. We generally call the frequency domain (amplitude vs.. frequency) plot an FFT.

Full-Scale Input Swing - The difference between the maximum and minimum input voltages that will produce a valid ADC output without going over- or under-range.

Gain Error - The error in the slope of the ADC transfer characteristic. It is the difference in the actual and ideal full scale input range values.

IMD - Intermodulation Distortion. This is the creation of new spectral components that result from two or more input frequencies modulating each other when the circuit is nonlinear.

INL - Integral Non-Linearity. The maximum departure of the ADC transfer curve from the ideal transfer curve. INL is a measure of how straight is the transfer function curve. There are two popular methods of measuring INL: End Point and Best Fit. The End-Point method is the most conservative, while the Best Fit method gives lower (better-looking) values. National uses the End Point method.

Input Dynamic Range - For an ADC, the range of voltages that can be applied to the input without going under or over range.

Input Offset - The difference between the input value of 1.0 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

Input Offset Error - The difference between the ideal input value of 0.5 LSB and the input voltage that causes the ADC output code to transition from zero to the first code.

IP3 - $3^{rd}$ order intercept point. It is a measure for weakly nonlinear systems and devices, for example receivers, linear amplifiers and mixers. It is based on the idea that the device nonlinearity can be modeled using a low order polynomial, derived by means of Taylor series expansion. The third-order intercept point relates nonlinear products caused by the 3rd order term in the nonlinearity to the linearly amplified signal. The intercept point is a purely mathematical

concept, and does not correspond to a practically occurring physical power level. In many cases, it lies beyond the damage threshold of the device.

LSB - Least Significant Bit. The bit that has the least weight.

Nyquist Rate - The minimum sampling rate (or frequency) needed to prevent frequency aliasing.

Nyquist Frequency - The maximum input frequency beyond which frequency aliasing results.

Offset Error - This is the same as Input Offset Error.

PCB - Printed Circuit Board.

Quantization - The process of dividing a range of analog voltages or currents into smaller range of voltages or currents such that each value is represented by a single digital code.

Quantization Error - The error introduced as a result of the quantization process. The amount of this error is a function of the resolution of the quantizer. By definition, the quantization error of an ADC is 1/2 LSB. Quantization Noise . The noise at the ADC output that is caused by the quantization process. It is defined as $20 * \log(2(n-1) \times \sqrt(6))$, or about $6.02 \times n + 1.76$ dB, where "$n$" is the number of output bits of the ADC. Quantizer . A circuit that carries out the quantization process. Another name for an Analog-to-Digital Converter.

Reference Voltage . For an ADC, the reference voltage is the voltage against which the analog input or an ADC is compared to determine the ADC output code.

Resolution - A measure of how well the ADC input is resolved, or how well the value of an LSB represents the analog input. Resolution is usually expressed in bits, and then indicates the number of bits available in the ADC output word. The number of discrete output states or values of an ADC can be expressed in the number of digital bits in the output.

Sampling Noise - The inherent noise of an ADC that comes from the steps in the transfer function.

SFDR - Spurious-Free Dynamic Range. A term used to specify ADCs and SFDR is the ratio of the rms amplitude of the carrier frequency (maximum signal component) to the rms value of the next largest noise or harmonic distortion component. SFDR is usually measured in dBc (with respect to the carrier frequency amplitude) or in dBFS (with respect to the ADC's full-scale range).

SINAD - Signal-to-Noise And Distortion ratio.A combination of the SNR and THD specifications, SINAD is defined as the rms value of the fundamental signal to the rms value of all of the other spectral components below half the clock frequency, including harmonics but excluding d.c. SINAD can be calculated from SNR and THD. Because it compares all undesired frequency compo-

nents at the output with desired frequency. It is an overall measure of the dynamic performance of the ADC. SINAD is also known as SNDR, S/(N+D) and Signal-to-Noise Plus Distortion. SNR . Signal-to-Noise Ratio. The ratio of the power in the signal to the power in all other spectral components below 1/2 the sampling frequency, excluding harmonics and d.c.

Spurious - Spurious in a spectrum defines as lacking authenticity or validity in essence or origin signal frequency component; not genuine signal or false signal including noise, and harmonics.

THD - Total Harmonic Distortion. The ratio of the rms total of a specified number of harmonic components to the rms value of the output signal. This thesis uses the first nine harmonics ($f_2$ through $f_{10}$).

Undersampling - Undersampling occurs when the sampling rate of an ADC is much lower ($f_{\text{SAMPLE}} < 2 \times f_{\text{IN}}$) than the applied input frequency, usually resulting in a loss of signal information, thereby causing aliasing (see also Aliasing/Anti-Aliasing). With proper filtering and an adequate input tone and clock frequency selection, the aliased components that contain the signal information can be shifted from a higher-frequency band to a lower-frequency band and converted.

# Chapter 2

# An Overview of ADCs and ADC Test Procedures

## 2.1 Overview

An Analog-to-Digital Converter (ADC) is a device or circuit used to convert analog information to digital words. This chapter describes a number of ADC architectures commonly employed in high-performance modern telecommunication systems.

This chapter explores general ADC architectures to study design verification test requirements and prerequisite criteria to perform robust and cost-effective design verification tests from the initial design release phase prototype testing to the full production level testing. Successful product developments are based on concurrent engineering and the chapter guides how concurrently approach the final

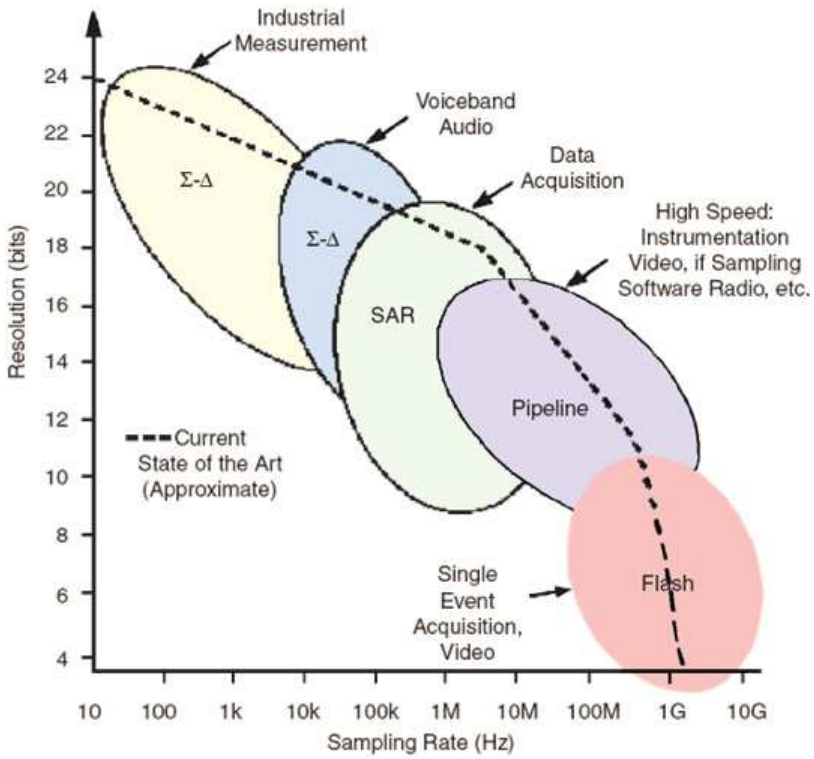



Figure 2.1: ADC architectures, applications, resolution and sampling rates [13]

productions.

## 2.2 ADC architectures

There are many ADC architectures commonly employed in high-performance modern electronic systems [14, 15, 16, 17, 18]. Deciding on the correct ADC requires tradeoffs between resolution, channel count, power consumption, size, conversion time, static performance, dynamic performance, and price [19]. System designers or test engineers need to know the key features, and have a basic understanding of the

architectures and their design limitations.

The classification in Figure 2.1 shows, in a general way, how these application segments and the associated typical architectures relate to ADC resolution and sampling rate. The dashed lines represent the approximate state of the art in mid-2005 [20].

### 2.2.1 Flash ADC

Flash analog-to-digital converters, also known as parallel ADCs, are the fastest way to convert an analog signal to a digital signal. Typical flash ADC is shown in Figure 2.2. They use large numbers of comparators. An N-bit flash ADC consist of $2^N$ resistor and $2^N$-1 comparators. Each comparator has a reference voltage from the resistor ladder string which is 1-LSB step apart between resistors. The outputs from $2^N$-1 comparators are a thermometer code and then processed to N-bit binary output by a decoder logic.

Flash ADCs are suitable for applications requiring very large bandwidths. However, flash converters consume a lot of power, have relatively low resolution, and can be quite expensive. This limits them to high frequency applications that typically cannot be addressed any other way. Examples include data acquisition, satellite communication, radar processing, sampling oscilloscopes, and high-density disk drives [20].

The input to a flash ADC is applied to a large number of comparators, which

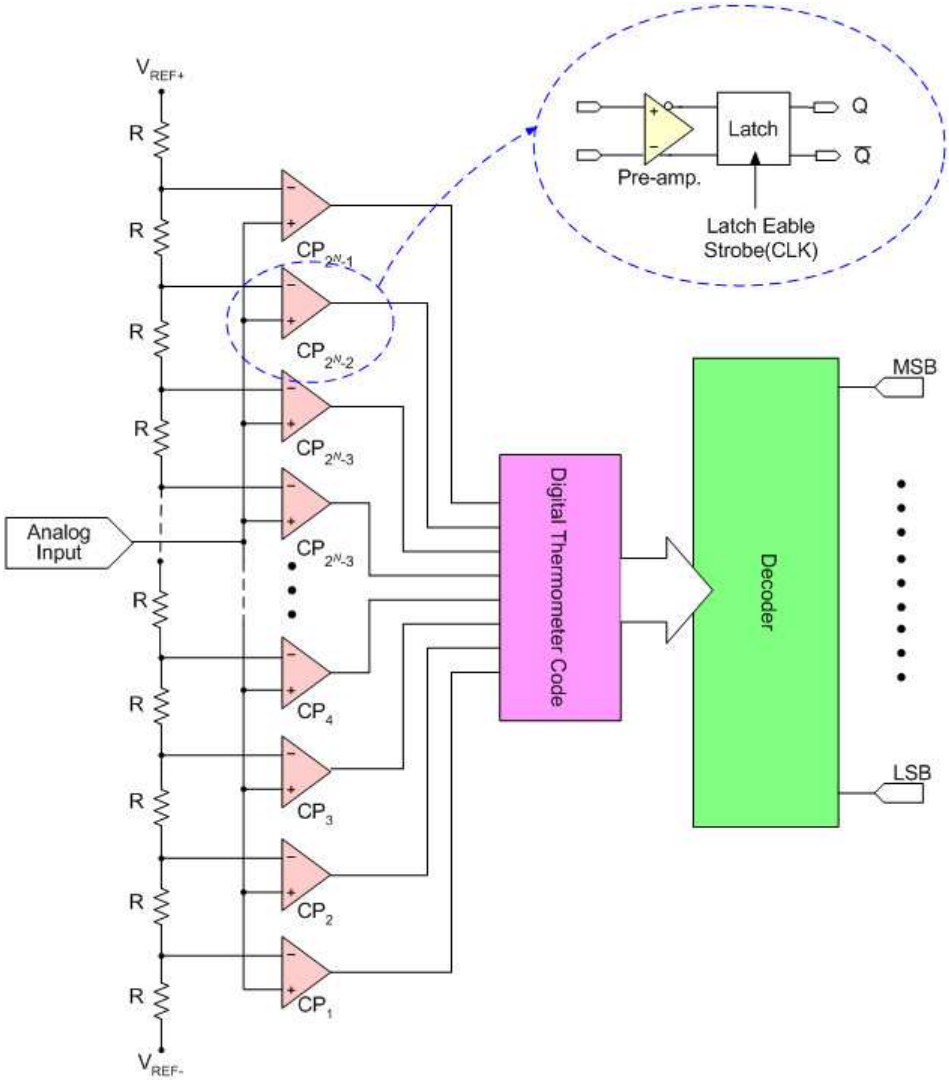
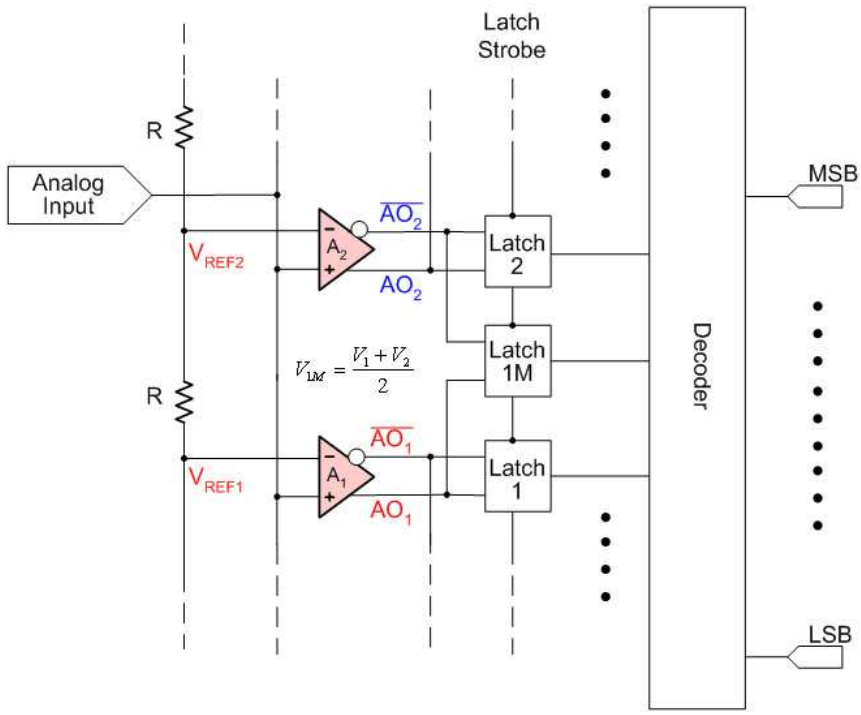
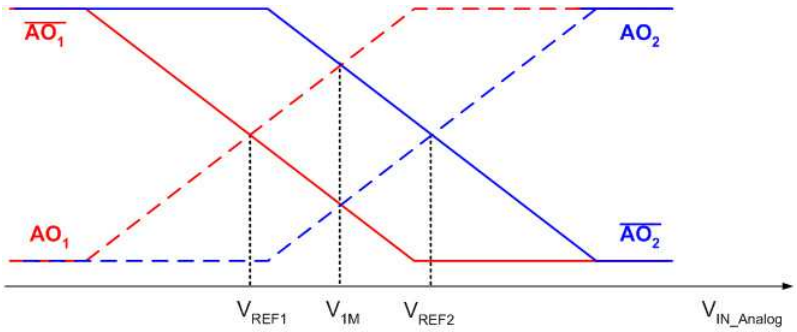



Figure 2.2: Typical flash ADC Architecture




(a) Interpolating block diagram




(b) I/O characteristics of pre-amplifiers

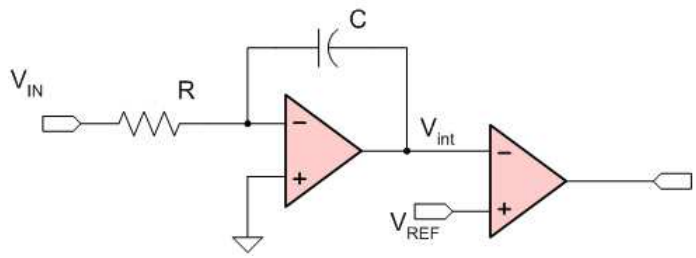
Figure 2.3: Interpolation scheme in a flash ADC

have an voltage variable input capacitance, each. Those capacitances are signal-dependent and result in degrading effective-number-of-bits (ENOB) of the converter [16, 20]. They can add distortion for high frequency analog input. A wide bandwidth, low-distortion comparator designs are challenging in a flash ADC design for high frequency operations.

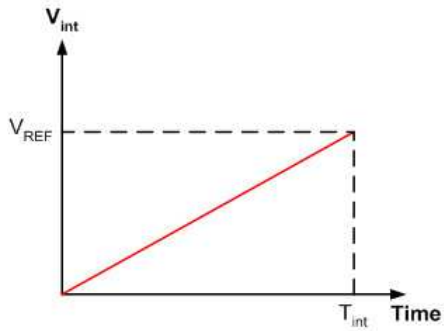
To minimize the number of comparators in typical flash ADCs, an interpolation scheme can be applied [21, 19] as shown in Figure 2.3. In contrast with a simple flash ADC, the interpolating flash ADC scheme halves the number of preamplifiers but maintains the same number of latches. The preamplifier A1 and A2 compare the analog input with the node references, $V_{REF_1}$ and $V_{REF_2}$, respectively. Voltage input/output characteristics of the preamplifiers are shown in Figure 2.3(b). Assuming zero offset for both preamplifiers, we can find that $V_{\overline{AO_1}} = V_{AO_1}$ when $V_{IN} = V_{REF_1}$, and $V_{\overline{AO_2}} = V_{AO_2}$ when $V_{IN} = V_{REF_2}$. If $V_{AO_2} = V_{\overline{AO_1}}$, then we can find that $V_{IN} = V_{1M} = (V_{REF_1} + V_{REF_2})/2$.

### 2.2.2 Integrating ADC

Integrating analog-to-digital converters (ADCs) provide high resolution analog-to-digital conversions, with good noise rejection [18]. These ADCs are ideal for digitizing low bandwidth signals, and are used in applications such as digital multi-meters and panel meters. They often include LCD or LED drivers and can be used stand alone without a microcontroller host [22].




(a) Block diagram




(b) Operation

Figure 2.4: Single-slope ADC Architecture

A. Single-slope ADC:

A single-slope ADC in Figure 2.4 is the simplest architecture of an integrating ADC. Here, an unknown input voltage ($V_{IN}$) is integrated and the value compared against a known reference value ($V_{REF}$). The time it takes for the integrator to trip the comparator is proportional to the unknown voltage ($T_{int}/V_{IN}$). In this case, the known reference voltage must be stable and accurate to guarantee the accuracy of the measurement.

One drawback to this approach is that the accuracy is also dependent on the tolerances of the integrator's R and C values. Thus, slight differences in each component's value change the conversion result and make measurement repeatability

quite difficult to attain in a production environment. To overcome this sensitivity to the component values, the dual-slope integrating architecture is used.

B. Dual-slope ADC:

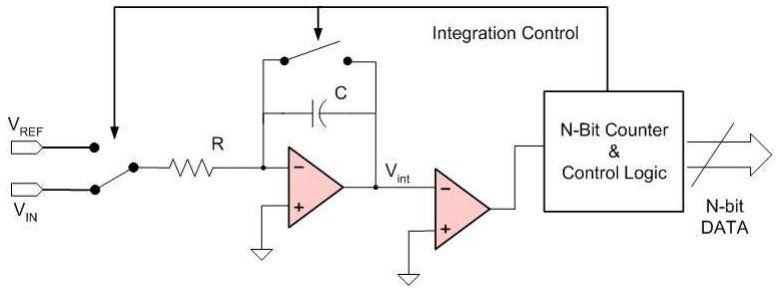
A dual-slope ADC architecture is shown in Figure 2.5. The operation is following: the integrator integrates an unknown input voltage ($V_{\mathrm{IN}}$) for a fixed amount of time ($\mathrm{T_{int}}$), then "de-integrates" using a known reference voltage ($\mathrm{V_{REF}}$) for a variable amount of time ($\mathrm{T_{de\text{-}int}}$). The operation meets the following condition [20, 13]:

$$\mathrm{T_{de\text{-}int}} = \mathrm{T_{int}} \times \frac{\mathrm{V_{IN}}}{\mathrm{V_{REF}}}. \tag{2.1}$$

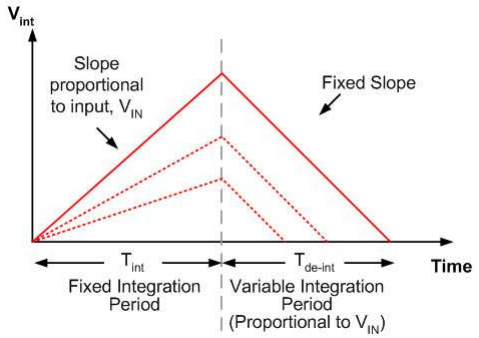
The key advantage of this architecture over the single-slope is that the final conversion result is insensitive to errors in the component values. That is, any error introduced by a component value during the integrate cycle will be canceled out during the de-integrate phase [20].

This tradeoff between conversion time and resolution is inherent in this implementation. It is possible to speed up the conversion time for a given resolution with moderate circuit changes. Unfortunately, all improvements shift some of the accuracy to matching, external components, charge injection, etc. In other words, all speed-up techniques have larger error budgets [19].

Even in the single-slope ADC converter in Figure 2.4, there are many potential error sources to consider such as power-supply rejection (PSR), common-mode rejection (CMR), finite gain, over-voltage concerns, integrator saturation, compara-




(a) Block diagram




(b) Operation

Figure 2.5: Typical dual-slope ADC Architecture

tor speed, comparator oscillation, capacitor leakage current, parasitic capacitance, charge injection, etc.

Single, dual and multi-slope ADCs can achieve high resolutions (16-bits or more) and are relatively inexpensive and dissipate materially less power versus flash ADCs. These devices support very low conversion rates, typically less than a few hundred samples per second. Most applications are for monitoring DC signals in the instrumentation and industrial markets.

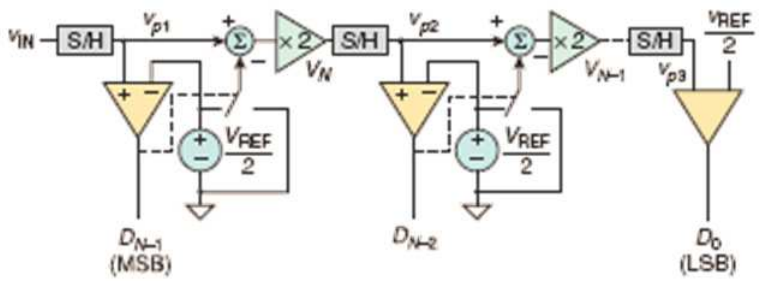



Figure 2.6: A pipeline ADC block diagram [20]

### 2.2.3 Pipelined ADC

The pipelined analog-to-digital converter (ADC) has become the most popular ADC architecture for sampling rates from a few megasamples per second (MS/s) up to 100MS/s or more, with resolutions from 8 to 16 bits [20]. They offer the resolution and sampling rate to cover a wide range of applications, including charge-coupled device (CCD) imaging, ultrasonic medical imaging, digital receiver, base station, digital video (for example, HDTV), xDSL, cable modem, and fast Ethernet.

A pipelined ADC employs a parallel structure in which each stage works on one to a few bits (of successive samples) concurrently as shown in Figure 2.6. The inherent parallelism increases throughput, but at the expense of power consumption and latency. Latency in this case is defined as the difference between the time an analog sample is acquired by the ADC and the time when the digital data is available at the output. For instance, a five-stage pipelined ADC will have at least five clock cycles of latency. In a pipeline converter, a B-bit converter requires only

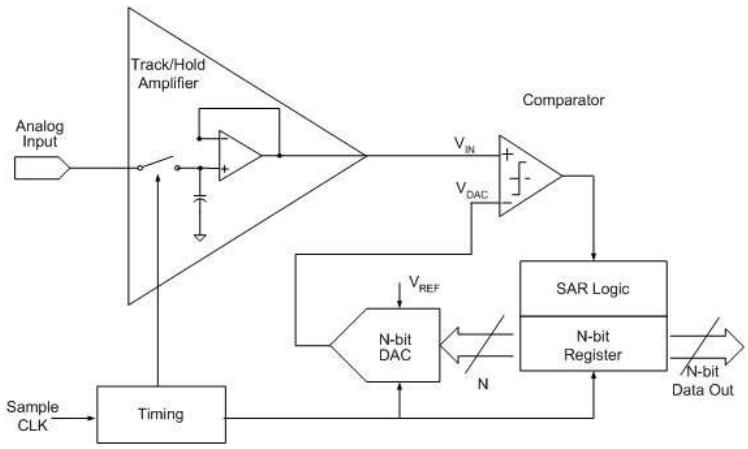
B comparators, and the output of each comparator is a bit in the final converter output (i.e., no thermometer code) [20].

A pipelined ADC requires accurate amplification in the DACs and interstage amplifiers, and these stages have to settle to the desired linearity level. By contrast, in a flash ADC, the comparator only needs to be low offset and be able to resolve its inputs to a digital level (i.e., there is no linear settling time involved). However, some flash converters require pre-amplifers to drive the comparators. Gain linearity needs to be carefully specified.

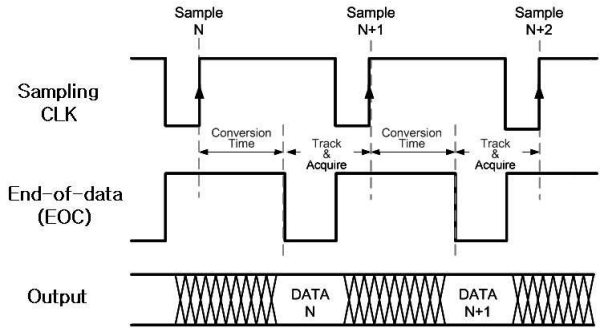
### 2.2.4 Successive-approximation-resister(SAR) ADC

SAR ADCs are frequently the architecture of choice for medium-to-high-resolution applications, typically with sample rates fewer than 5 megasamples per second (Msps). SAR ADCs most commonly range in resolution from 8 to 16 bits and provide low power consumption as well as a small form factor. This combination makes them ideal for a wide variety of applications, such as portable/battery-powered instruments, pen digitizers, industrial controls, and data/signal acquisition [20].

The basic architecture in a SAR ADC is shown in Figure 2.7(a) [16, 19] and the comparator and the N-bit DAC are two critical components in this architecture. The analog input voltage ($V_{IN}$) is held on a track/hold. To implement the binary search algorithm, the N-bit register is first set to mid-scale (for, 100... $.00_2$, where the MSB is set to '1'). This forces the DAC output ($V_{DAC}$) to be $V_{REF}/2$, where




(a) SAR basic building block diagram




(b) Typical SAR ADC Timing

Figure 2.7: Successive-approximation-resister (SAR) ADC

$V_{REF}$ is the reference voltage provided to the ADC. A comparison is then performed to determine if $V_{DAC}$ is less than or greater than $V_{DAC}$. If $V_{IN}$ is greater than $V_{DAC}$, the comparator output is a logic high (or '1') and the MSB of the N-bit register remains at'1'. Conversely, if $V_{IN}$ is less than $V_{DAC}$, the comparator output is a logic low (or '0') and the MSB of the register is cleared to logic '0'. The SAR control logic then moves to the next bit down, forces that bit high, and does another comparison. The sequence continues all the way down to the LSB. Once this is done, the conversion is complete, and the N-bit digital word is available in the register. The fundamental timing diagram is shown in Figure 2.7(b). The end of conversion is generally indicated by an end-of-conversion (EOC).

In a SAR converter, the bits are decided by a single high-speed, high-accuracy comparator one bit at a time (from the MSB down to the LSB), by comparing the analog input with a DAC whose output is updated by previously decided bits and thus successively approximates the analog input [14]. This serial nature of the SAR limits its speed to no more than a few Msps, while flash ADCs exceed giga-sample per second (GS/s) conversion rates.

### 2.2.5 Sigma Delta (Σ-Δ) ADC

Σ-Δ ADCs are used predominately in lower speed applications requiring a trade off of speed for resolution by oversampling, followed by filtering to reduce noise. 24-bit Sigma Delta converters are common in Audio designs, instrumentation and Sonar.

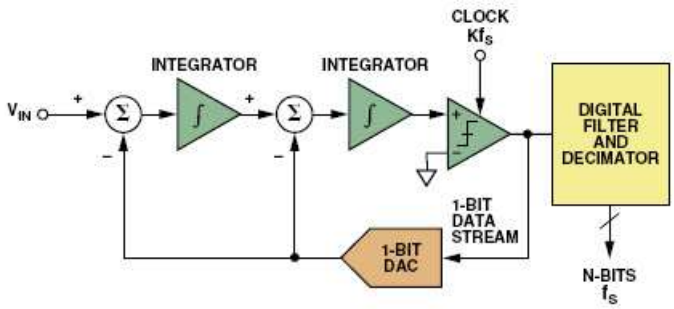
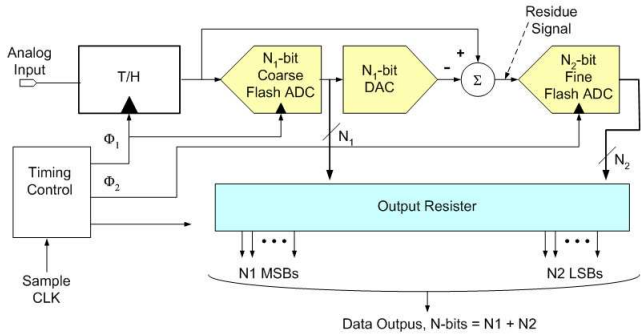
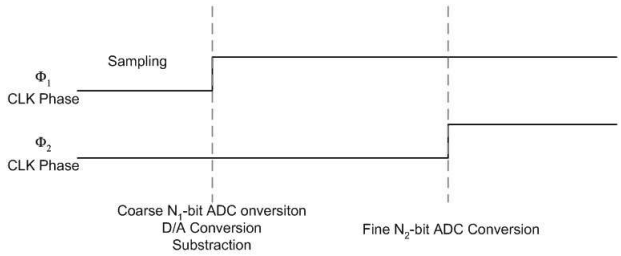



Figure 2.8: Second order Sigma-delta (Σ-Δ) ADC [20]

Bandwidths are typically less than 1MHz with a range of 12 to 18 bits [13, 23]. A 2nd-order Σ-Δ ADC basic building block is shown in Figure 2.8. These converters are capable of the highest resolution possible in ADCs. They require simpler anti-alias filters (if needed) to bandlimit the signal prior to conversion. They trade speed for resolution by oversampling, followed by filtering to reduce noise. However, these devices are not always efficient for multi-channel applications. This architecture can be implemented by using sampled data filters (also known as modulators) or continuous time filters. For higher frequency conversion rates the continuous time architecture is potentially capable of reaching conversion rates in the hundreds of Msps range with low resolution of 6 to 8-bits. This approach is still in the early research and development stage and offers competition to flash alternatives in the lower conversion rate range [24].




(a) Two-step ADC basic building block




(b) Control clock phases

Figure 2.9: Two-step ADC architecture

### 2.2.6 Two-step ADC

Two-step ADCs are also known as subranging converters and sometimes referred to as multi-step or half flash (slower than Flash architecture). This is a cross between a Flash ADC and pipeline ADC. Two-step ADCs can achieve higher resolution or smaller die size and power for a given resolution are needed versus a Flash ADC. This approach combines ideas from successive approximation and flash architectures.

Sub-ranging ADCs reduce the number of bits to be converted into smaller groups, which are then run through a lower resolution flash converter. This approach reduces the number of comparators and reduces the logic complexity, compared to a flash converter [14, 15].

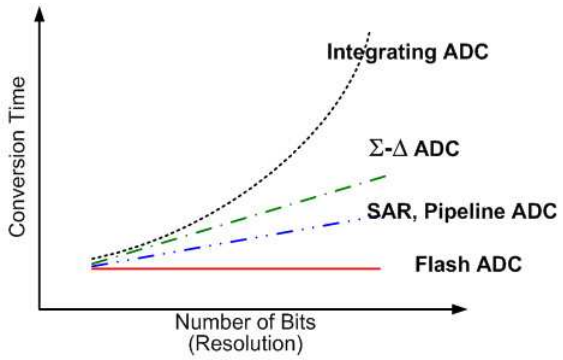
A simplified two-step ADC architecture is shown in Figure 2.9(a). A first conversion is completed with a $N_1$-bit converter. A residue is created, where the result of the $N_1$-bit conversion is converted back to an analog signal (with an higher resolution ($2\times N_1$-bit) accurate DAC) and subtracted from the input signal. This residue is again converted by the $N_2$-bit ADC and the results of the first and second pass are combined to provide the N-bit ($N_1+N_2$) digital output. As shown in Figure 2.9(b), the coarse ADC and the fine ADC data conversion are controlled by two clock signals, $\Phi_1$ and $\Phi_2$, each by the timing control unit.

## 2.3 ADC architecture tradeoffs

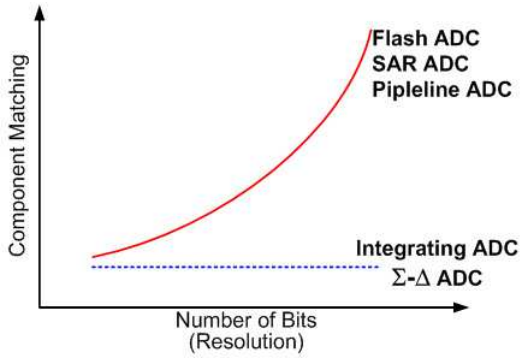
ADCs can be implemented by employing one of architectures in the previous section. ADC's architectural tradeoffs can be addressed in terms of their sampling data conversion time, on-chip device component matching and die size, cost and power [22].

In Figure 2.10(a), the tradeoffs are shown with respect to ADC data conversion time. For flash converters, the conversion time does not change significantly with increased resolution. The conversion time for Successive Approximation Register (SAR) or Pipelined converters increases approximately linearly with an increase in resolution. For integrating ADCs, the conversion time doubles with every bit increase in resolution. The tradeoffs is illustrated in Figure 2.10(a).

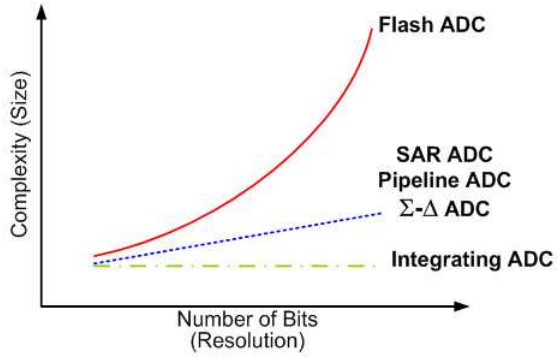
Device matching requirements in on-chip ADC design are shown in Figure 2.10(b).




(a) ADC Conversion time vs. Resolution




(b) Component Matching Vs. Resolution




(c) Complexity Vs. Resolution

Figure 2.10: ADC architecture tradeoffs [19, 22, 20]

For flash ADCs, device component matching typically limits resolution to around 8-bits. Calibration and trimming are sometimes used to improve the matching available on chip. Component matching requirements double with every bit increase in resolution. This applies to flash, successive approximation or pipelined converters, but not integrating converters. For integrating converters, component matching does not materially increase with an increase in resolution

ADCs' die size, cost and power are also important factor to choose which ADC architecture to use. For flash converters, every bit increase in resolution almost doubles the size of the ADC core circuitry. As a result, it also doubles the power. In contrast, For SAR, Pipelined, or sigma-delta ADCs, a die size is linearly increasing with its resolution. For integrating ADCs, a core die size is not materially changed with an increase in resolution. Figure 2.10(c) shows the tradeoffs. A complexity is increased as an increase in die size, and ADC cost can be higher.

## 2.4 ADCs as mixed-signal SoCs for modern satellite communications

Rapid progress has been made in the field of analog-to-digital converters with high sampling rates ($\geq$ 800 MSamples/s, or more) and 4-8 bits of resolution. These integrated systems are now in wide-spread use in satellite receivers, digital radars, electronic warfare, electronic measurement equipment, etc [25, 26]. As integration levels increase and enhanced process technology becomes available, signal-to-noise ratio (SNR), spurs and distortion guide our selection of components for systems

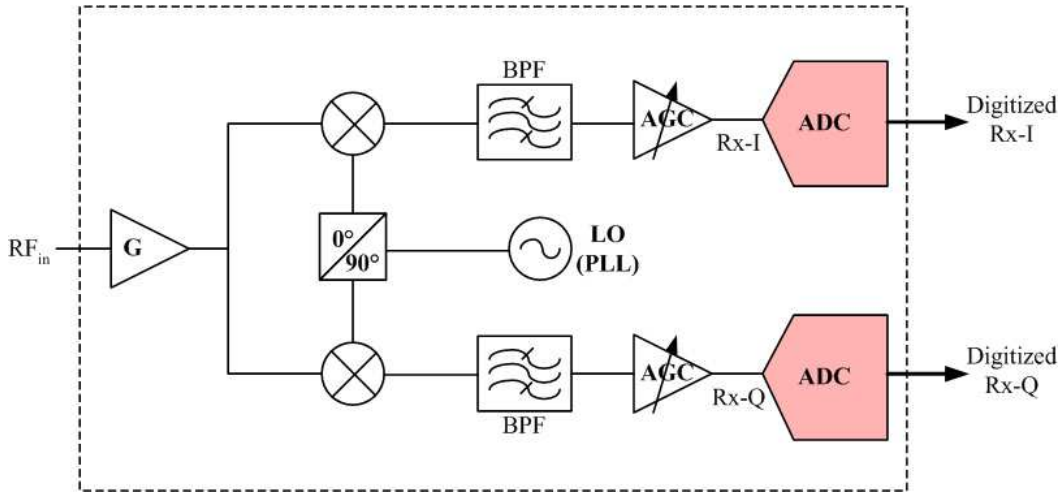



Figure 2.11: Typical satellite receiver function block. Accurate sampling channel testing and calibration must be prior to characterize and validate the integrated ADCs. Traditional test metrics are not directly applicable to verify the ADC design. RF/mixe-signal test and digital signal processing (DSP) based test methodologies are required.

application. Typically, the interface between the radio and the base-band processor is realized using ADCs.

In most modern satellite communication systems, the sampled analog signals can be separated into in-phase (I) and quadrature (Q) data channels that are down-converted to the base band. The input analog modulated signal can be directly injected into the IF (intermediate frequency) section of a superheterodyne receiver; or, the RF signal can be stored and processed in the case of a direct conversion receiver. A system functional block is illustrated in Fig. 2.11 where the base-band spectrum is sampled by the data converter and processed by digital-signal processing (DSP) cores.

Recently, error vector magnitude (EVM) testing has been used to quantify a typical satellite receiver system performance in Fig. 2.11. EVM tests are advantageous since they can reduce both test time and complexity compared to a traditional test methodology for a wireless communication systems [27]. The EVM test method is hindered by the fact that the sampling ADC performance must be pre-defined for accurate full system characterization; otherwise, the system gain and phase may be distorted by the personality of the ADCs.

Traditional static measurement techniques used in ADC quality assessment provide ADCs static transfer characteristics such as gain, offset, integral and differential non-linearity (INL and DNL). In the static measurements, a static or slowly varying input ramp signals are used to characterize the ADC. For dynamic ADC tests, ADCs critical parametric specifications, such as effective number of bits (ENOB), total harmonic distortion (THD), signal-to-noise-and-distortion (SINAD), are mostly estimated from characterizing the dynamic performance of ADCs in the communication systems [28].

As semiconductor process (CMOS or BiCMOS) technology has advanced, and system-on-chip (SoC) solutions become more prevalent, digital buffering interfaces appear between the point of signal observation and the data converter. This digital buffering problem makes it difficult to apply traditional metrics to validate system performance since the buffered sampled signal is no longer an analog signal but a representation of that signal as a bit-wise digital logic signal. Therefore, the digital

signal containing the sampled analog information must be analyzed accounting for error introduced in buffering.

Testing and verification of the dynamic performance of high sampling clock rate ADCs are major problems facing data-converter manufacturers [26, 29]. Knowledge of the Full speed ADC performance over the frequency range of interest is critical to specify and characterize the suitability of a communication receiver system. Only an assessment of the dynamic performances over the ADCs entire operating frequency range can assure the validity of the encoded analog signal. High speed ADC dynamic testing is essential to provide a correct representation of ADC resolution and bit accuracy over the full bandwidth of operation.

In this work, a test methodology is described to verify the dynamic performance of ADCs used in a modern satellite receiver. To accomplish this goal, we have developed evaluation hardware and software to characterize the full operation of high speed ADCs. A high speed ADC developed by Hughes Network Systems, LLC (HNS) is used as an target example of our approach. The design comprises dual channel, 6-bit converters with de-multiplexed low voltage differential signal (LVDS) outputs and a common sampling clock at 800 MSamples/s for each converter.

## 2.5 Design verification tests: From component characterization to production testing

Testing of ADC (a design under test: DUT) can be carried in a numerous ways. It is critical to produce quality and properly working ADC products and verify their designs, so that their specific functionality are fully tested. It is a challenging to develops means to provide an efficient and comprehensive test and verification methodology, so that the test and verification methodology can accurately sort good product parts from defective ones, and even at a low cost. The cost of testing high-speed ADCs has become a significant part of the overall cost of a product development.

Ultimate goal for high-speed ADC production testing is performing numerous tests in a short amount of time on high volumes of parts. In other words, to have high throughput and low overhead, or low cost of test is the major objective of the production testing.

When ADC test program reaches the stage of the full production testing, there should be a minimal number of tests utilized to reduce total testing cost. In contrast, during the early stage of production runs, the test is often conservatively planed and performed, so that redundant tests for the ADC are common.

This is attributed to the number of people involved in the development of the device, which is a high-speed ADC for a modern satellite communication systems in the research. Design engineers and hardware and material engineers must work

concurrently together to reach the final stage of the full production.

Therefore, each specific set of tests must be developed to satisfy individual design and functional performance criteria. In early stages of the production life cycle, the design and manufacturing engineers of the ADC seek awareness of potential production flaws and tolerances. Therefore, by feeding back excessive quantities of information from the tests and characterizations of the ADC, the final production test and test program can be matured over a period.

This section explores general design verification test requirements and prerequisite criteria to perform robust and cost-effective design verification tests from the initial design release phase prototype testing to the full production level testing. Successful product developments are based on concurrent engineering and the chapter guides how concurrently approach the final productions.

## 2.6 Capital expensive items for design verification tests

There are not many general information available on these topics. However, to succeed in verifying and full characterizing high-speed ADCs, several expensive items are required as listed below:

- Test programs
- Production test equipment
- Rack and stack

- Automated test equipment (ATE)
- Interfacing with the test equipment
  - Handlers
  - Load boards
  - Contactor sockets
  - Wafer probing
  - Packaging
- Calibration
- Accuracy, repeatability and correlation
- Design-for-Test(DfT) and built-in self test(BIST)

Test programs must reflect ADC test plan and flow and define test equipment controls and hardware configurations. After a high-speed ADC has been fabricated on wafer as a bare-die or placed into a package, testing of the device occurs in a laboratory environment. The production test equipment defines a test system. In general, production test equipment has two major architectures: rack-and-stack, automated test equipment.

For example, if an initial design released ADC is fabricated, rack-and-stack can provide more flexible rudimentary ADC test systems since the configuring tester is

customized to a specific part which can characterize prototype stages of the fabricated high-speed ADCs. On the other hand, ATE is a tester as a complete standalone unit for optimal production testing of the devices.

## 2.7 Conduct a design verification test

This section can be used as instructions to plan and conduct design verification tests (DVTs) in general. Although this section emphasizes the detailed approach for a design verification test, the principles also apply to any higher level tests required by the development process and the project plan. A typical product will consist of many modules integrated to form the hardware product, which itself will be integrated with software to form the system. Test plans for hardware verification tests (HVT) and system verification tests (SVT) must address the same issues as defined here. The purpose of this section is to show guidelines, and a possible template for a design verification test plan.

### 2.7.1 Process of a design verification test

The hardware development usually takes account for conducting a DVT for each developed module or design. The task of creating the DVT plan, and actually doing the testing, is usually and classically assigned to the design engineer who is familiar to the design itself. Depending on the complexity of the design and/or associated risks going into high volume production, the DVT may be split into two

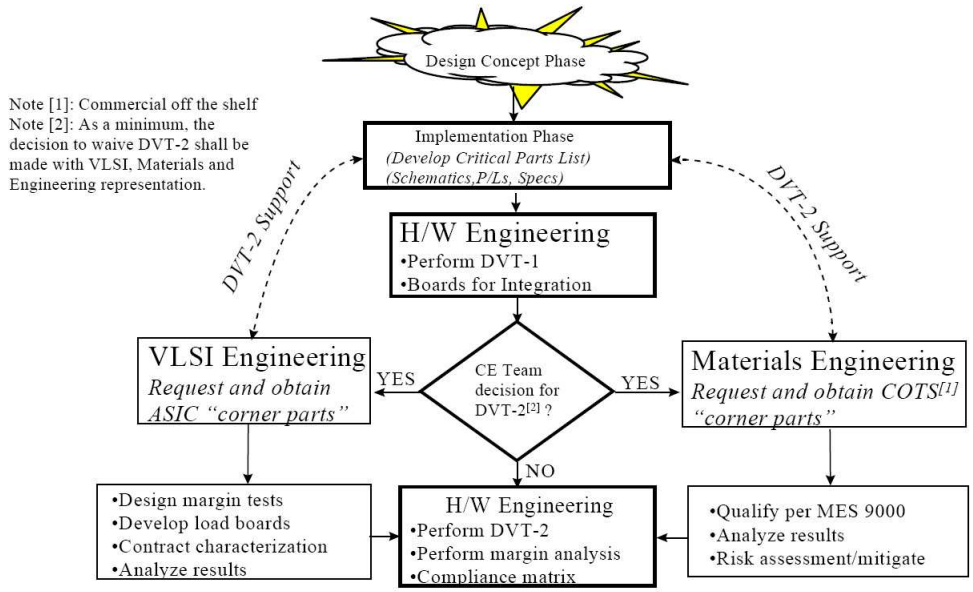



Figure 2.12: Design verification process outline

phases, DVT-1 and DVT-2. The decision on whether to perform the additional testing (DVT-2) will be made by the concurrent engineering team. Usually, in the industry, if the decision is made to perform only DVT-1, the tests will be run by the designer or the test engineer. When the decision is made to include DVT-2, the DVT shall be performed by the test engineer in conjunction with VLSI design engineer and Hardware engineer and Material engineer. The process outline is illustrated in Figure 2.12.

#### 2.7.1.1 DVT-1

DVT-1 shall verify by testing the module as designed meets the minimum requirements as stated in the module specification. As a minimum, DVT-1 shall demon-

strated that the sample module(s) meets the functional performance specifications and that the design is adequately stable such that the module will serve as a stable platform for firmware, software, and other development.

In this thesis, Chapter 3 to 5 is providing the detail DVT-1 procedures and test results for the high-speed ADC. The purpose of DVT-1 is summarized as following:

- Verify that the ADC module as designed meets the requirements as stated in the module specification.
- Reveal and discuss limitations (if any) of the design. All limitations shall be documented within the hardware module specification.
- Decide on any final changes to the design.
- If DVT-2 tests are to be run, DVT-1 provides a knowledge base to design effective DVT-2 tests.
- Verify that components intended to be added to the design parts list as an "alternate part" are compatible with the design in all respects.

#### 2.7.1.2 DVT-2

DVT-2 extends the testing done in DVT-1 to include the use of corner lot parts [30], (parts that represent the expected variations due to process variations in the manufacturing of ICs). The tests in DVT-2 will typically be done at voltage and temperature extremes to stress the module design in an attempt to quantify the limitations

(if any) of the design and to determine how much margin the design has to accommodate manufacturing tolerances [9, 5]. Limitations of the design investigated in DVT-2 are, at a minimum, functional performance over specified operational and non-operational environments and the vulnerability (if any) of the design to variances in application specific integrated circuit (ASIC), and critical commercial off the shelf (COTS) individual part performance. DVT-2 will be run, in general, on designs that employ ASICs, or many complex field programmable gate arrays (FPGAs).

In this thesis, Chapter 6 is providing the detail DVT-2 procedures and test results for the high-speed ADC. The purpose of DVT-2 is summarized as following:

- Identify the limitations (if any) of the ADC design with respect to design margin using statistical methods.

- Identify ADC system component variability which may affect the long term manufacturing yields and field performance by varying the circuit voltage and/or temperature.

- Increase the ADC test coverage by purposely testing "hard to simulate" PCB effects and ADC system's internal part performance. This would include the effects of cross talk and signal integrity of the interconnects of the ADC system ASICs, and COTs with known performance variances.

DVT-2 minimum requirements are that all attempts shall be made to utilize ADC

Table 2.1: Summary for a hardware design physical testing

| Test Name | Minimum Requirement |
|---|---|
| DVT-1 | Verification of performance of all nodes within the module |
| DVT-2 | Verification of performance of all nodes within the module including voltage, corner parts and temperature stress |
| HVT | Verification of performance of all module interface |

system ASICs, and critical commercial-off-the-shelf parts(COTs) that represent the "corners" of parametric variation that could be delivered to testers by the supplier over time and volume. In the case where corner parts, which are with known variances, cannot be obtained within the DVT-2 schedule constraints, the added risk shall be considered and reviewed in the DVT results and DVT-2 shall proceed with the available parts.

### 2.7.2 DVT plan and hardware verification test (HVT)

The two phased plan is divided into various testing phases ranging from unpowered and isolated, to powered in a system test environment. The purpose is to find and solve the basic problems as early as possible and to quantify the design margin before production.

The plan should be prepared by the HW Engineer with inputs from VLSI Engineering and Materials Engineering if the decision is made to perform DVT-2. This is important because both what is essential to the system applications and what is essential to the ADC system module must be considered simultaneously.

The over all flow of the two phased DVT and the relationship to HVT is

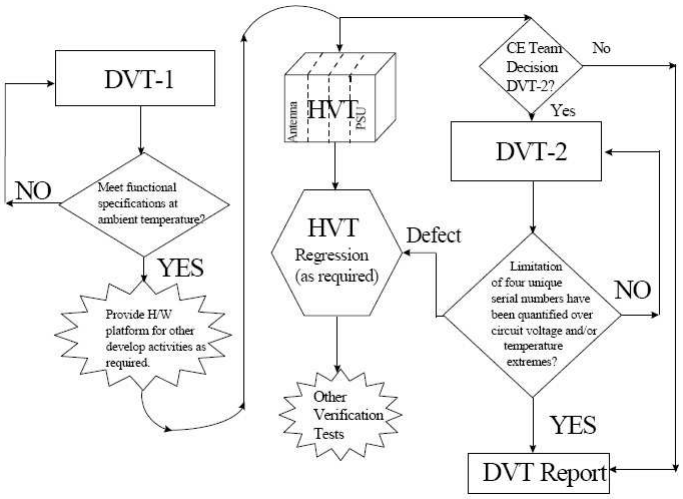



Figure 2.13: Over all flow of the two phased design verification tests (DVT) and their relationship to hardware verification test (HVT)

summarized in Fig. 2.13.

## 2.8 Product development process

The product development process should take the following steps:

1. Prepare the two phased DVT Plans: DVT-1 and DVT-2.

2. Review the plan for accuracy and completeness.

3. Conduct the testing as specified in the plan, collecting data and observations as needed.

4. Analyze the data, quantify the design margin and decide if the ADC system design and testing module pass the test and manufacturability requirements

(if DVT-2 is performed).

There are two ways to perform a DVT in a production. The first way (and probably the most common) is to functionally debug the entire ADC system module and then go back and perform the formal DVT process. The second way is to functionally debug a section and then perform the DVT on that section immediately following. The latter is the preferred method, for the following reasons:

- A concurrent DVT/functional debug will take less time to perform because you will have less repeated effort.
- You will be less likely to fudge the DVT results or take short-cuts if you use the concurrent approach. Using the independent approach, you will be likely to say to yourself "I've already debugged this, and besides it's working", and then you will fudge the DVT results to take short-cuts in the DVT process.

At the end of the DVT process, a post DVT design review should be conducted. During this design review all the DVT results should be made available along with any changes that were required to fix problems. In addition, the engineer should have a summary sheet noting the limitations of the module. In other words, what you must do to make the module fail. All of this vital information should be discussed in detail with all present and more than likely the engineer will leave this design review with a list of action items. These action items should be followed up by the same team until they are resolved to satisfactions for everyone. Finally, a design goes to production.

## 2.9 Summary

In this chapter, some of basic ADC architectures and their tradeoffs are explored. We also study design verification test requirements and prerequisite criteria to perform robust and cost-effective design verification tests from the initial design release phase prototype testing to the full production level testing. Successful product developments are based on concurrent engineering and the chapter guides how concurrently approach the final productions. The chapter also provides a guidance to plan design verification tests by describing DVT phase 1 and 2 and production development process. This chapter is served as a design verification test template in this thesis work.

# Chapter 3

# High-speed ADC Characterization: New Results

## 3.1 Overview

In this chapter, a general overview of ADC test architecture and operating principles are presented. Next, a detailed description of verification tests is provided. It should be noted that members of the circuit design and test teams interfaced throughout high-speed ADC ASIC project. This has led to the implementation of "design for test (DfT)" methodology throughout the life of the project. Details are discussed more broadly in this chapter and the following subsections includes all information required for product application and the design of the ADC, and defines all parameters necessary to interface with the software.

### 3.1.1 The test specification process

The test specification process is actually a series of activities: generating test programs and converting or translating from a device data sheet to a test plan. The test plan structure and the DUT functionality will be directly related to the characterization of a production and product cost, so that the well-organized and well-developed test plan will eliminate unnecessary characterization efforts.

Generating test plans for mixed-signal devices such data converters can take a great deal of time for the test engineer. It is difficult to derive a feasible data specification document even for proto-type designs. In general, the data sheet serves as the formal communication channel between the marketing and engineering personnel engaged in a project. The data sheet provides a blueprint for design: when the development of a new device begins, the data sheet serves as the design target. Thus, design engineers refer to the data sheet as a blueprint to make sure they realize marketing and system engineering organization goals. The test and product engineers refer to the data sheet in order to define the test lists if manufactured devices meet their specification as the project progresses. Therefore, the test list must be comprehensive enough to guarantee that the manufactured device meets field engineering requirements. After engineers design a new SoC based on this design specifications, the test and production engineers must carry on the verification of the designed specifications.

### 3.1.2 A test design example:

We begin with a concrete design example: An ADC designed by Hughes Network Systems, LLC (HNS). The ADC is used for a next-generation satellite telecommunication system, called *SPACEWAY*, whose unique capabilities will enable high-speed data networking, groundbreaking applications, and unlock a wealth of value-added HughesNet services. Operating in a globally assigned Ka-band spectrum, *SPACEWAY* employs high-performance, onboard digital processing, packet switching, and spot-beam technology to offer direct site-to-site connectivity at rates of from 512 Kbps up to 16 Mbps. *SPACEWAY* combines the traditional advantages of a satellite system. It exhibits ubiquitous reach and efficient broadcast/multicast, with high data rates and mesh connectivity to give customers a fast, efficient, flexible and cost-effective communications solution [31].

The *SPACEWAY* high-speed ADC has a dual 6-bit analog to digital converter operating at a sample rate of 800 MHz. Its main features and requirements are summarized here:

- The ADC is a two channel 6-bit device
- It converts at an 800 Msps conversion rate for each channel
- The ADC samples from each converter are demultiplexed by a 6:12 demultiplexer
- The output data from the converter is LVDS compliant with IEEE 1596.3-1996

- The ADC provides an output clock signal at 1/2 of the input clock frequency
- The ADC provides a mid-scale reference voltage output
- The ADC provides an over-range output signal, which is common for both converters and is active for one 400 MHz output clock cycle when triggered
- The ADC output saturates at positive or negative full scale when overdriven in the positive or negative direction, respectively
- The ADC operates using a positive supply rail

Design-for-test (DfT) methodology is implemented at the start of design. Based on the main features and requirement, the top-level chip architecture can be planned and layed out. A top level functional block diagram is illustrated in Figure 3.1. This is the starting point for test design. For example, The 1/2 speed of synchronizing clock outputs from an input clock and demultiplexing digital outputs are considered for the system applications and feasibilities to interface with limited hardware. Over range outputs from the front-end quantizer are used for the ADC input driving conditions so that accurate ADC performance extractions are possible.

The main objective of the system development described here is the replacement of a proto-type *SPACEWAY* system ADC (MAX 105 [32]) to HNS custom designed ASIC for cost reductions. This is the so-called "*Thames*" chip, utilizing the VLSI design procedure shown in Appendix 7.3. After the ADC architecture is

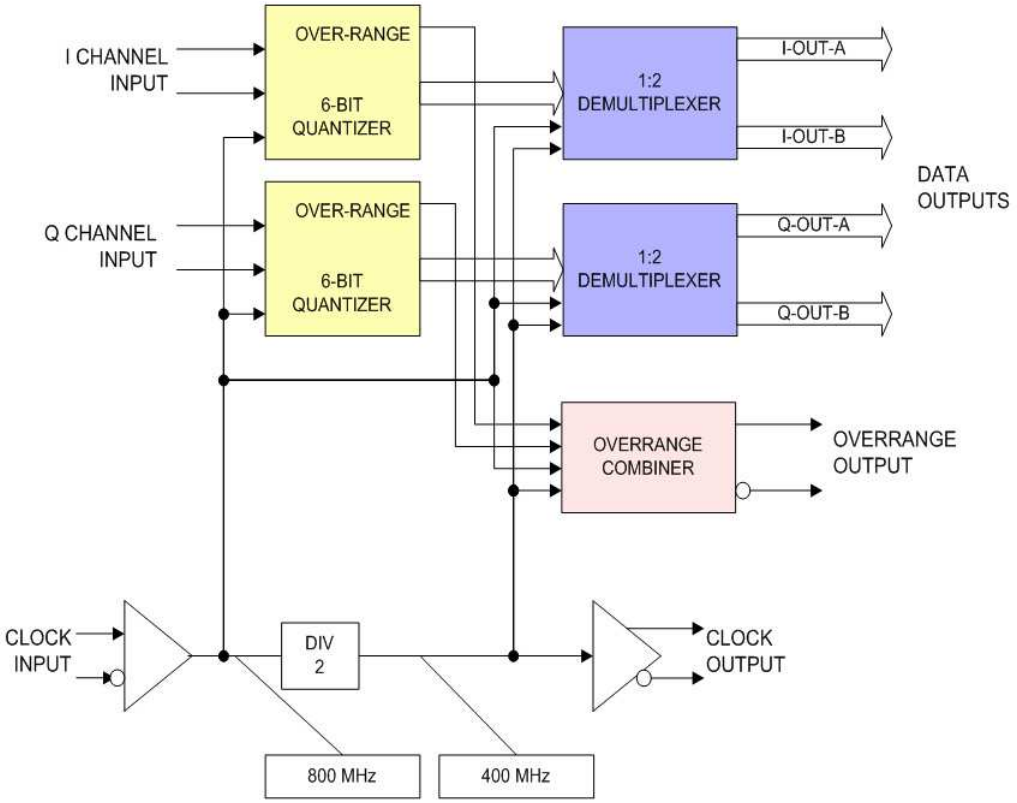



Figure 3.1: Top level functional block for the HNS *SPACEWAY* high-speed ADC (planning and design phase): The SPACEWAY ADC is a dual 6-bit analog to digital converter at a sample rate of 800 MHz. The ADC is a two channel 6-bit device and samples from each converter are demultiplexed by a 6:12 demultiplexer. The output data from the converter is LVDS compliant with IEEE 1596.3-1996. The ADC provides an output clock signal at 1/2 of the input clock frequency and a mid-scale reference voltage output. The ADC also provides an over-range output signal, which is common for both converters and is active for one 400 MHz output clock cycle when triggered. The output saturates at positive or negative full scale when overdriven in the positive or negative directions, respectively. The ADC operates on positive supply voltages only.

decided (flash-type ADC) based on the top-level system requirement, the project enters the circuit design and digital design phases. To pursue circuit design and digital design, a more specified block diagram is necessary as illustrated in Figure 3.2. After final SPICE-type circuit simulation, the physical layouts are generated.

The *Thames* ASIC is a dual 6-bit 800 MSamples/sec flash ADC fabricated in the Atmel SiGe AT46000 technology [33]. The ADC is designed using standard flash data-converter techniques, and converters both the 'I' and 'Q' data channel in a modern high performance digital radio receiver where accurate gain and phase matching between the two channels is necessary. At the output, a 6:12 demultiplexer is used halve the speed of the data output from the ADC to the baseband processor. All the digital outputs, which connect the ADC to the baseband processor, have an low voltage differential signal driver (LVDS) compatible with IEEE standard 1596.3-1996 [34, 35].

## 3.2 High-speed ADC functionality

A functional block diagram of the sample has ADC shown in Fig. 3.2. It embeds two identical ADCs on a single chip. The general operation of the ADC is based on the flash converter principle [14]. The key to this high speed architecture lies in the comparator design. Each ADC employs a fully differential input stage, and each quantizer and downstream logic function translates the comparator output into 6-bit, parallel thermometer codes. An unique encoding scheme is also employed to

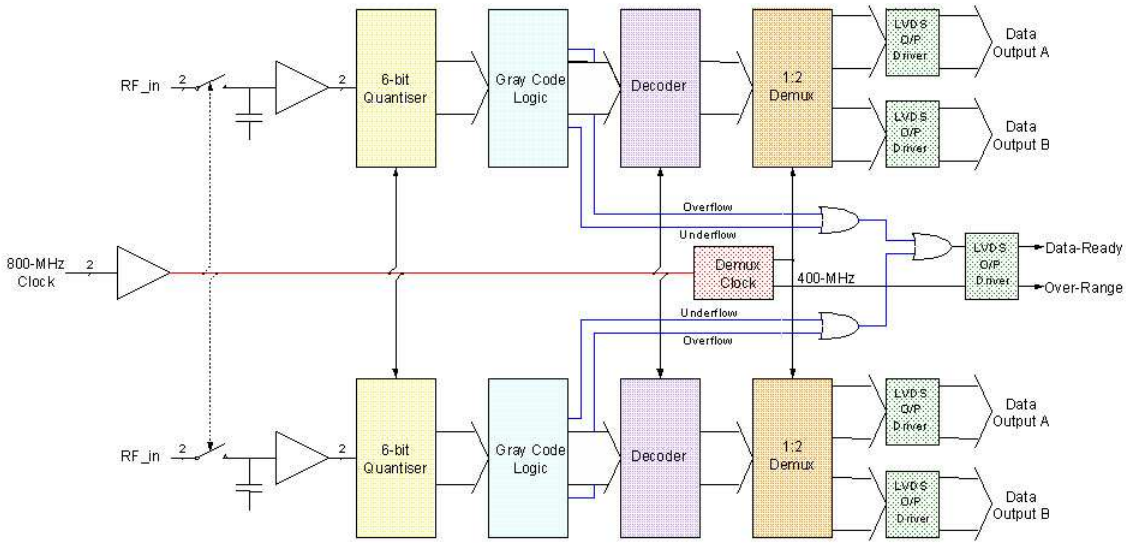



Figure 3.2: HNS *SPACEWAY* high-speed designed ADC ASIC block diagram - detailed specification for ADC design phase

limit metastability. The output logic data are formatted in two's complement code, compliant with the IEEE low voltage differential signals (LVDS) standard 1596.3-1996 [34, 35].

The benefits of the 'Data_Ready' and 'Over_Range' pin functions will be discussed in detail in a later chapter. For now, note that the digital output data is de-multiplexed (6:12) and fired out at half the rate of the input sampling clock (800MHz). We need a fast data acquisition system to meet the data ready rate (400 MHz or 400 Mbps) as the digital data acquisition clock beats time. The 'Over_Range' is a good indicator of calibration and a monitor of the input power level. This over-range indicates if the input level is within the full scale range. This pin serves a purpose in actual component use. But it also serves a dual function

in component validation. This approach fully exploits the concept of design-for-test (DfT) to enhance the testability and the cost effectiveness of testing in manufacturing, as this pin is used for system operations and for component test.

The data converter is designed using standard flash data-converter techniques, and sources both the 'I' and 'Q' data channel in a modern high performance digital radio receiver where accurate gain and phase matching between the two channels is necessary. At the output, a 6:12 demultiplexer is used to halve the speed of the data output from the ADC to the baseband processor. All the digital outputs, which connect the ADC to the baseband processor, have an LVDS driver compatible with IEEE standard 1596.3-1996.

### 3.2.1 Theory of operation

The complete block diagram of the *Thames* ASIC, ready for design verification testing, is shown in Figure 3.3. The two data converters are identical. In order to minimize the effects of clock jitter on the Effective Numbers of Bits (ENOB); the input signal is first sampled by a track-and-hold amplifier. The sampled input signal is then digitally quantized by $64-(2^2)-$ parallel comparators that produce a thermometer output code with increasing signal level. The 64 comparator outputs are combined, using sequential logic, to produce a 6-bit Gray code, with one-bit changes between adjacent codes.

The final step of the conversion process is to decode the 6-bit Gray code to

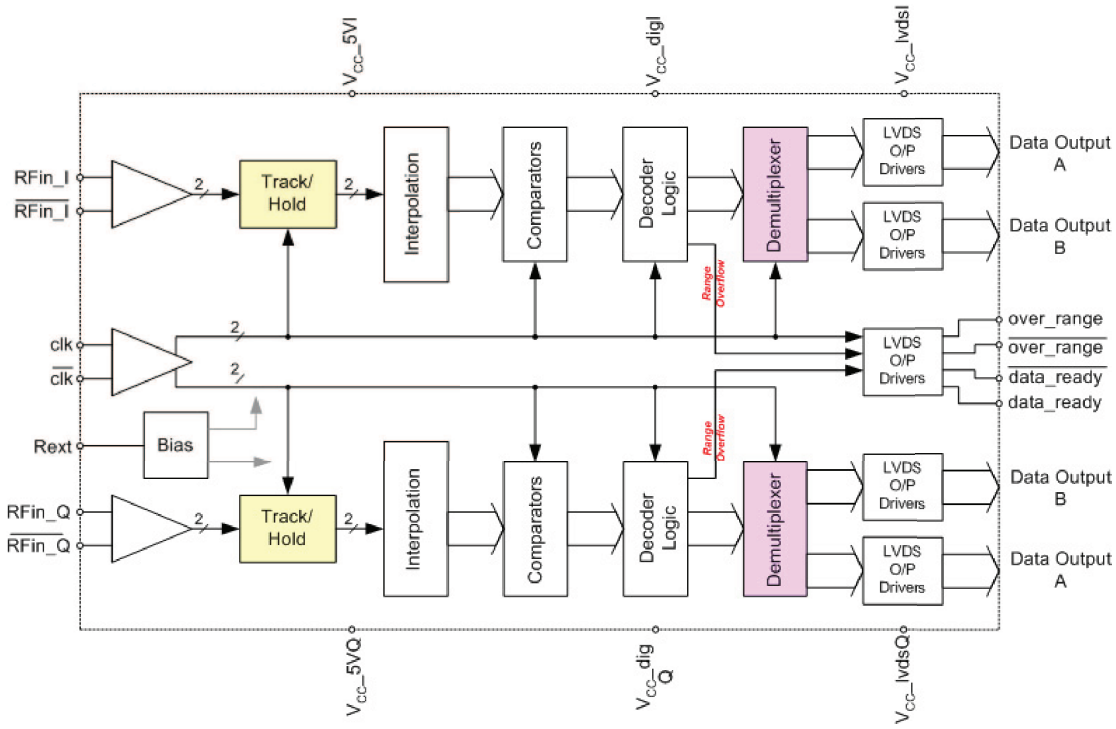



Figure 3.3: HNS high-speed designed ADC ASIC block diagram for design verification tests

a 6-bit two's compliment code using a series of Exclusive-OR(XOR) gates. At this stage the data is re-synchronized to original 800-MHz systems clock for transfer to the baseband processor.

Due to the problem of transferring data at the 800 MSamples/sec rate, a 6:12 demultiplexer is used to halve the output data rate. The output data signals are fully differential, and the interface to the baseband processor is compliant with IEEE LVDS standard 1396.3-1996. The two output data streams, for both 'I' and 'Q' channels, are concurrently output from the ADC. All data outputs are clocked to the baseband processor on the same rising edge of the 'data-ready' signal.

### 3.2.2 Digital output timing

Figure 3.4 illustrates the timing relationship between the 'data_ready' output (pins 51 and 52) and the four data output streams. The timing relationship, as shown in Figure 3.4, assumes a clock input of 800MHz applied to pins 10 and 11. The signal may be applied as either a differential or single-ended input; for further details reference should be discussed in the later section for the clock input.

The 'data_ready' output is designed to have a square wave with 50% duty cycle. For an 800MHz clock, the period of the 'data_ready' signal is 2.5ns ±3% (±75ps).

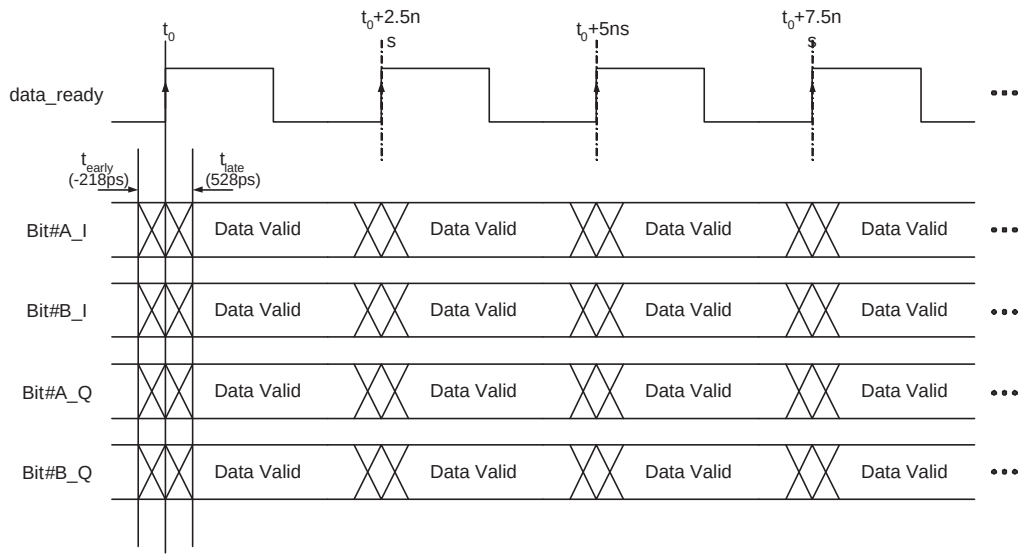



Figure 3.4: HNS *SPACEWAY Thames* high-speed ADC ASIC data output timing relationship

### 3.2.3 Latency

Latency is the time taken for the data conversion process and is defined as the time, in clock cycles, from when the input signal is acquired (and the analog to digital conversion process start,) to the time when the digital data is available for processing as signaled by the rising edge of the 'data_ready' output. The demultiplexed outputs are presented in dual 6-bit two's complement format with two consecutive samples in the primary (A-channel) and auxiliary output (B-channel) data ports. The B-channel data port always contains the older sample. The A-channel always contains the most recent data sample, regardless of the Data-Ready clock phase. The target latency for the *Thames* ASIC is four (4) clock cycles for the A-channel and five (5) clock cycles for the B-channel as illustrated in Figure 3.5. In other words, data in

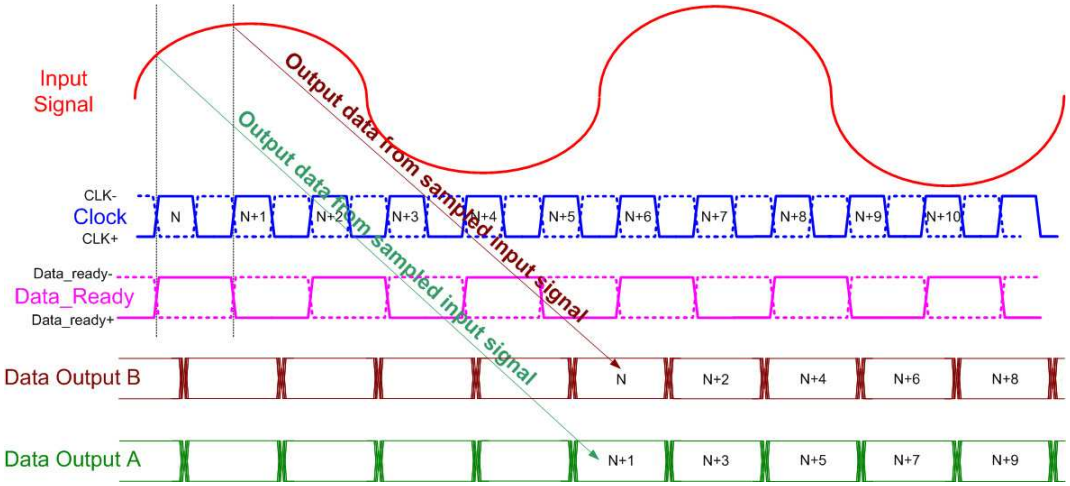



Figure 3.5: HNS *SPACEWAY Thames* high-speed ADC latency

the A-channel (primary) output port is delated by (4) clock cycles while data in the B-channel (auxiliary) output port is delayed by (5) clock cycles.

### 3.2.4 Track-and-Hold requirements

The Thames ASIC has a fully integrated track and hold circuit designed to operate at 800Ms/s. In the "hold mode" charge, equivalent to the input-signal is stored on capacitor internal to the ASIC. Should the ADC be operated at a conversion rate lower than 800Ms/s, problems/inaccuracies may be experienced due to the leakage of charge to or from this capacitor.

## 3.3 Differential I/O designation

The polarity of differential input and output signals, depending on whether they are classed as analog or digital, have the following designation:

- Analog differential I/O: the signal pins will be marked with a plus (+) and minus (−) sign to denote polarity (i.e. ⟨ pin_name+⟩ and ⟨ pin_name−⟩).

- Digital differential I/O: the negative (complimentary) signal pin will be denoted with an overbar (i.e. $\overline{pin\_name}$ )

In all cases without exception, the pins which comprise each differential input or output will have an identical ⟨pin_name⟩.

Throughout this document, all general reference to a differential input and outputs will be made in the singular. This reference, though applies to both (whether they are analog or digital) positive and negative terminals.

## 3.4 Logic-level definitions

Unless otherwise stated all input and output logic-levels have the following definition. Logic '1(High)' is equivalent to $V_{XH}$ and logic '0(Low)' to $V_{XL}$ ($V_{XH} > V_{XL}$), where the subscript 'X' is defined as 'I' for input or 'O' for output. For the case of differential digital I/O (i.e. LVDS drivers) the logic-states of the two pins are defined in Table 3.1

Table 3.1: HNS *Thames* ASIC high-speed ADC logic-level definition

| | pin_name | $\overline{pin\_name}$ |
|---|---|---|
| Logic '1' | $V_{XH} > V_{XL}$ | $V_{XH} < V_{XL}$ |
| Logic '0' | $V_{XL} < V_{XH}$ | $V_{XL} > V_{XH}$ |

## 3.5 Package

The chip layout is shown in Figure 3.6. The chip layout bond pad designation is illustrated in Figure 3.7. The *Thames* ASIC is assembled in an 80-pin, thermally enhanced thin quad flat package (TQFP) with a 12×12mm body. The package pad to ASIC bare die pad bonding diagram is shown in Figure 3.8. The package dimensions as supplied by the vendor should be compliant with JEDEC standard MS-026 variant 'ADD-HD'. An outline of the package is illustrated in Figure 3.9.

Primary package dimensions are listed in Table 3.2; for full mechanical details of the package reference should be made to either information supplied by the manufacturer or JEDEC standard MS-026.

The coplanarity of the leads for the packaged parts is $< 0.1$ mm (4 mils). The package used for *Thames* ASIC has an exposed paddle beneath the package. the exposed paddle allows for improved thermal conductivity and heat dissipation. To allow for this, the paddle must be soldered directly to a contiguous pad on the printed circuit board (PCB). To further improve heat dissipation this pad may be connected by a micro-via array to another layers within the PCB.

The ASICs are handled after pre-baked and dried to remove moisture from

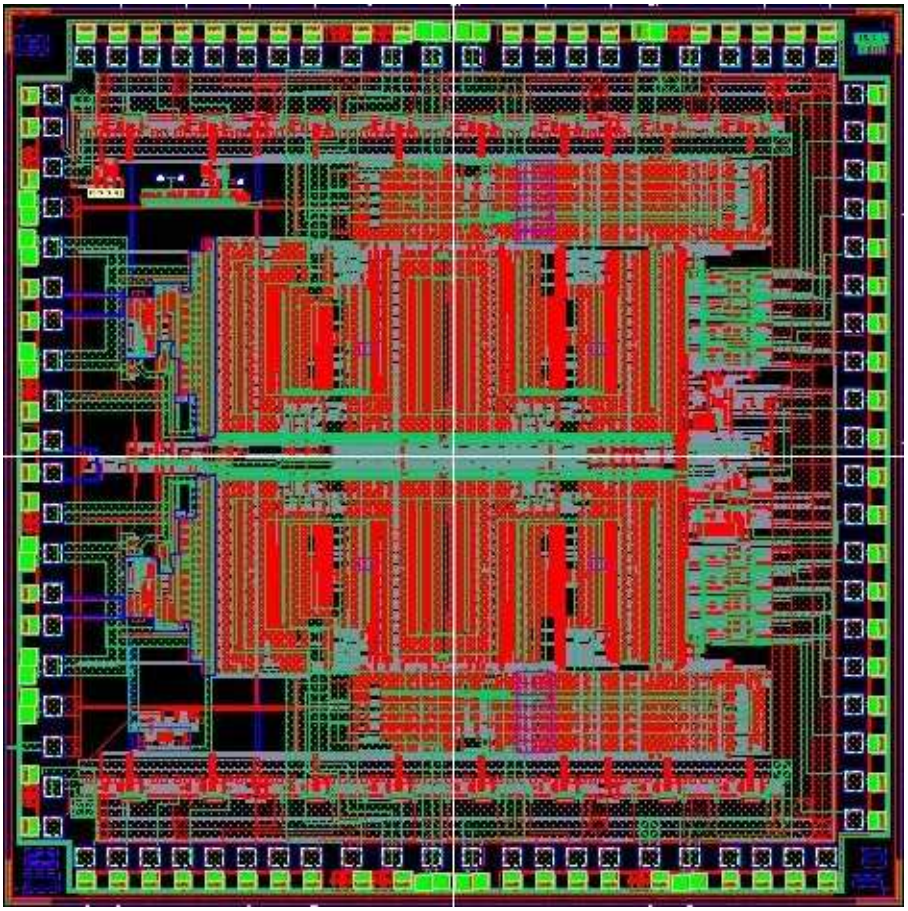


Figure 3.6: HNS *Thames* high-speed ADC ASIC layout view: die size 3.2mm × 3.2mm (fabricated in ATMEL's AT46K process (BiCMOS)

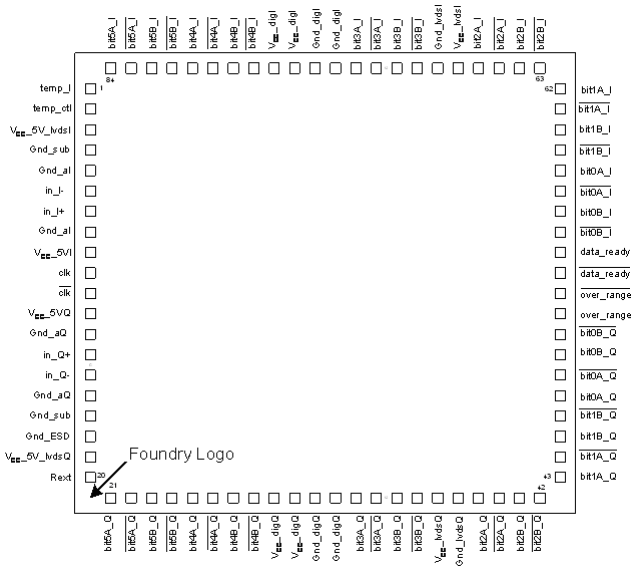



Figure 3.7: HNS *Thames* ASIC bond pad designation (total pad numbers count 84.)

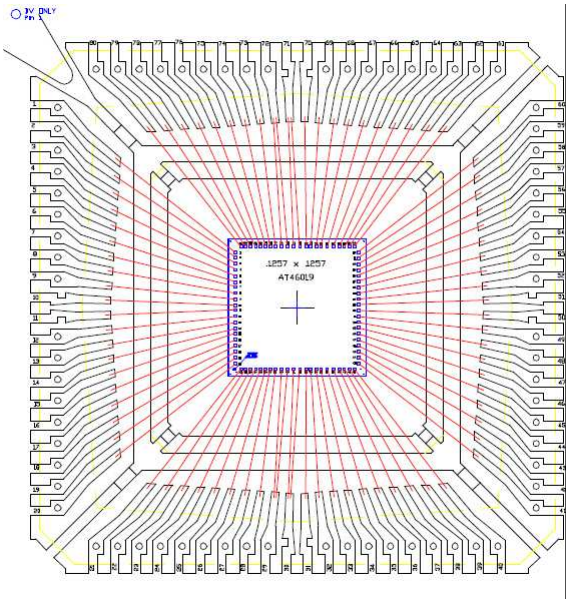


Figure 3.8: HNS *Thames* ASIC bonding diagram for 80-pin TQFP

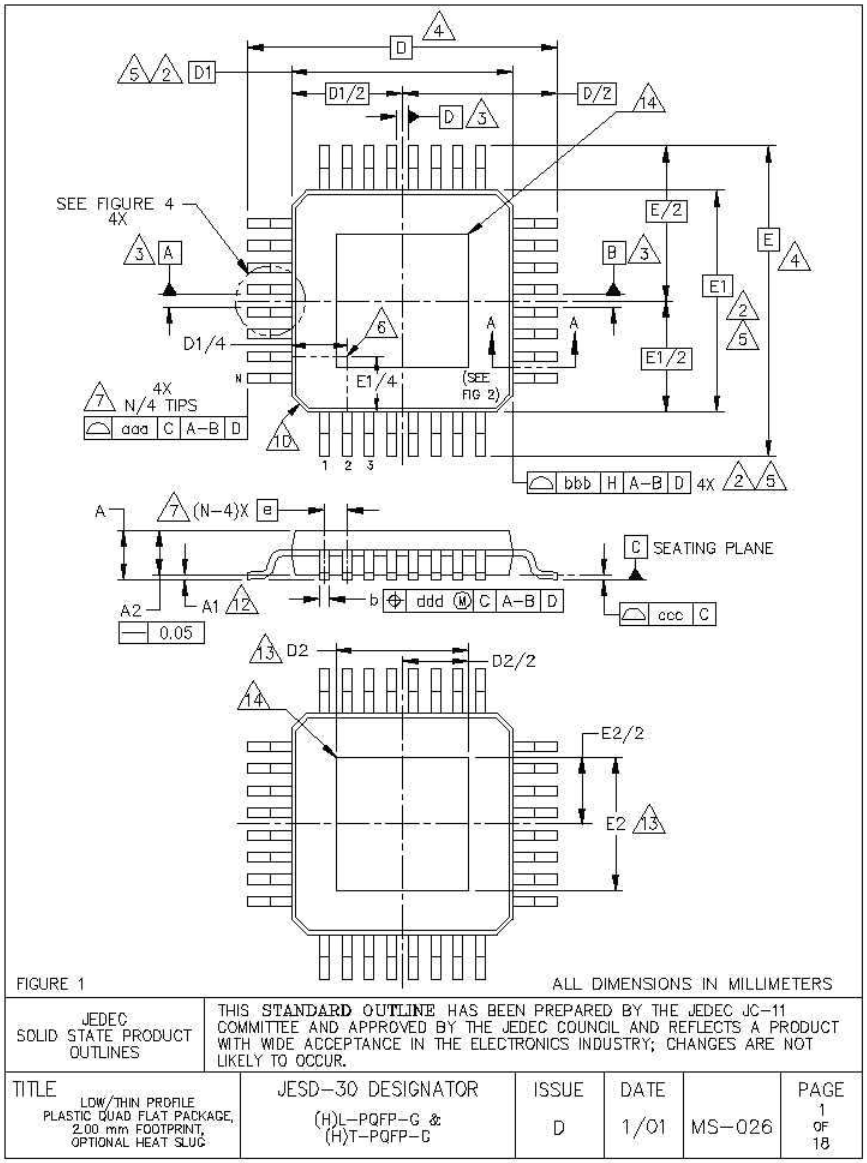



Figure 3.9: HNS *SPACEWAY Thames* high-speed ADC ASIC package outline diagram

Table 3.2: HNS *Thames* ASIC high-speed ADC Package dimensions*

| Symbol * | Min. | Typ. | Max. | Conditions |
|---|---|---|---|---|
| A | | | 1.20 | |
| A1 | 0.05 | | 0.15 | Distance from the seating plane to the lowest point on the package body. |
| A2 | 0.95 | 1.00 | 1.05 | |
| b | 0.17 | 0.22 | 0.27 | |
| b1 | 0.17 | 0.20 | 0.23 | |
| D | 14.00 BSC ‡ | | | |
| D1 | 12.00 BSC ‡ | | | |
| e | 0.50 BSC ‡ | | | Lead Pitch |
| E | 14.00 BSC ‡ | | | |
| E1 | 12.00 BSC ‡ | | | |
| N | 80 | | | |

1. Dimensions taken from JEDEC package standard outline MS-026, referece table 'ADD-HD', 80-pin 12×12 $mm^2$ body.
2. All dimensions are in millimeters (mm) unless otherwise stated.
3. BSC.A basic dimension. It is the theoretical exact size or location of a feature or datum.

the package encapsulation in accordance with JEDEC/EIA joint standard J-STD-033. Note that the ADC thermal management is also considered in the packaging process. A thermal heat sink within the package enhances the thermal conductivity from the TQFP packaged ADC to the bottom of the test fixture board platform. Figure 3.10 shows the exposed pad package cross-section.

## 3.6 Interface

### 3.6.1 I/O designation

This section describes the function of all input and output signals of the *Thames* ASIC. A summary of the I/O is listed in Table 3.3. Pin # is pin number of the pack-

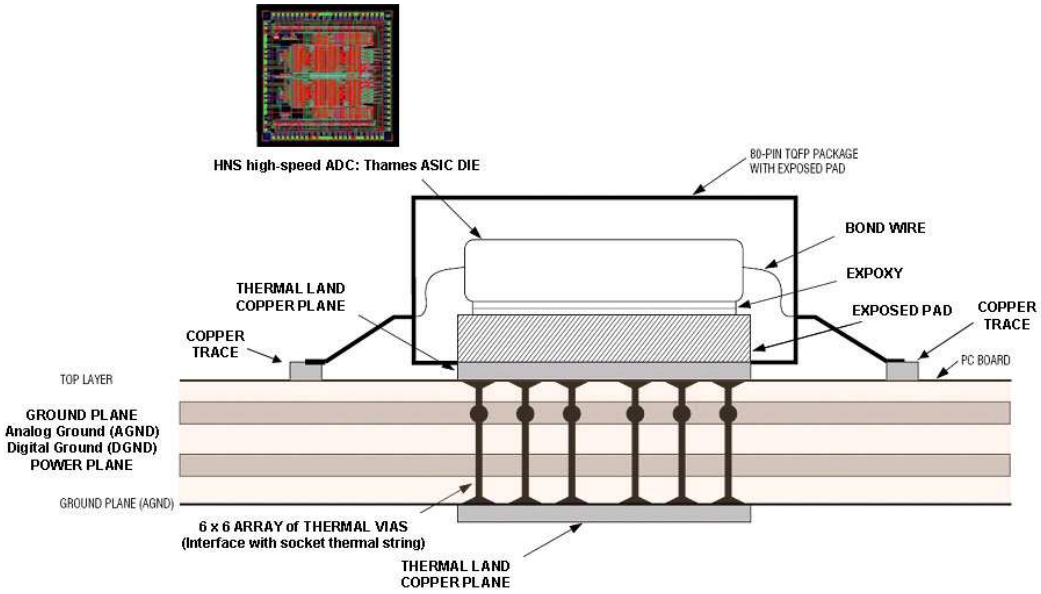



Figure 3.10: High speed dual channel 6-bit TQFN packaged ADC thermal management

age shown in Figure 3.11. Pad # refers to the die pad number which is illustrated in Figure 3.7.

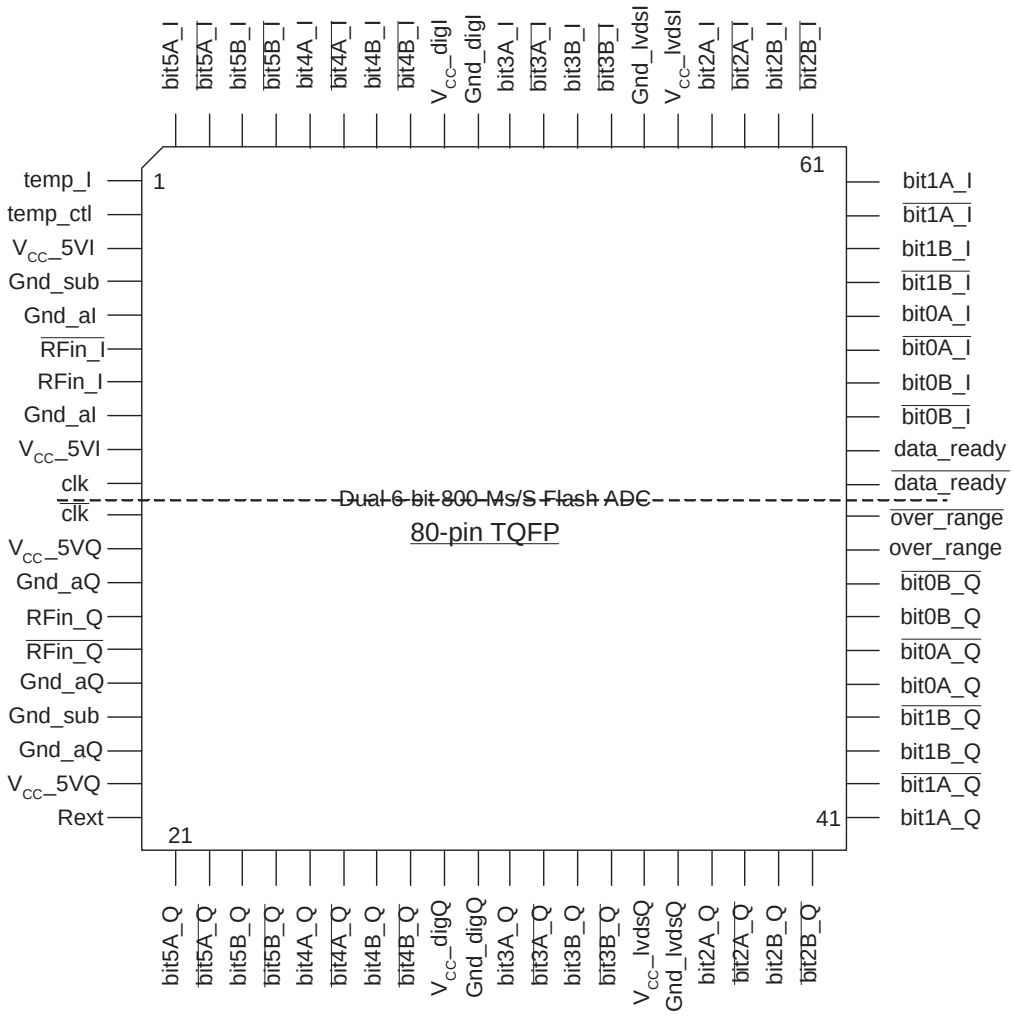



Figure 3.11: HNS *Thames* I/O Designation for 80-pin TQFP

Table 3.3: HNS *Thames* ASIC high-speed ADC I/O pin description

| **Pin #** | **Pad #** | **Pin Name** | **Description** | **Direction** | **Condition** |
|---|---|---|---|---|---|
| 1 | 1 | temp_I | Temperature Sense | Signal | |
| 2 | 2 | temp_ctl | Temperature Sense circuit control | Signal | |
| 3 | 3 | $V_{CC}$_5V_lvdsI | 5V supply, LVDS Drivers for converter I | Supply | +5V±5% |
| 4 | 4 | Gnd_sub | substrate ground | Ground | |
| 5 | 5 | Gnd_aI | Analog ground - Converter I | Ground | |
| 6 | 6 | in_I− | RF input, Converter I | Signal | RF Input 0.8$V_{pp}$200MHz |
| 7 | 7 | in_I+ | | Signal | |
| 8 | 8 | Gnd_aI | Analog ground - Converter I | Ground | |
| 9 | 9 | $V_{CC}$_5VI | Analog supply, Converter I | Supply | +5V±% |
| 10 | 10 | clk | Clock input | Signal | 0.5$V_{pp}$800MHz |
| 11 | 11 | $\overline{\text{clk}}$ | | Signal | |
| 12 | 12 | $V_{CC}$_5VQ | Analog supply, Converter Q | Supply | +5V±% |
| 13 | 13 | Gnd_aQ | Analog ground - Converter Q | Ground | |
| 14 | 14 | in_Q+ | RF input, converter Q | Signal | RF Input 0.8$V_{pp}$200MHz |
| 15 | 15 | in_Q− | | Signal | |
| 16 | 16 | Gnd_aQ | Analog ground - Converter Q | Ground | |
| 17 | 17 | Gnd_sub | substrate ground | Ground | |
| 18 | 18 | Gnd_ESD | | Ground | |
| 19 | 19 | $V_{CC}$_5V_lvdsQ | 5V supply, LVDS Drivers for converter Q | Supply | +5V±5% |
| 20 | 20 | Rext | External bias setting resistor | Bias | Rext 2.0kΩ |

Continued on next page

Table 3.3 – continued from previous page

| Pin # | Pad # | Pin Name | Description | | Direction | Condition |
|---|---|---|---|---|---|---|
| 21 | 21 | bit5A_Q | Bit 5 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 22 | 22 | $\overline{bit5A\_Q}$ | | Negative output | Signal | |
| 23 | 23 | bit5B_Q | Bit 5 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 24 | 24 | $\overline{bit5B\_Q}$ | | Negative output | Signal | |
| 25 | 25 | bit4A_Q | Bit 4 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 26 | 26 | $\overline{bit4A\_Q}$ | | Negative output | Signal | |
| 27 | 27 | bit4B_Q | Bit 4 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 28 | 28 | $\overline{bit4B\_Q}$ | | Negative output | Signal | |
| 29 | 29 | $V_{CC}$_digQ | Digital Supply for converter Q | | Signal | +3.0V ±10% |
| | 30 | | | | Signal | |
| 30 | 31 | Gnd_digQ | Digital Ground for converter Q | | Ground | |
| | 32 | | | | Ground | |
| 31 | 33 | bit3A_Q | Bit 3 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 32 | 34 | $\overline{bit3A\_Q}$ | | Negative output | Signal | |
| 33 | 35 | bit3B_Q | Bit 3 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 34 | 36 | $\overline{bit3B\_Q}$ | | Negative output | Signal | |
| 35 | 37 | $V_{CC}$_lvdsQ | LVDS Driver Supply for converter Q | | Supply | +3.0V±10% |
| 36 | 38 | Gnd_lvdsQ | LVDS Driver Ground for converter Q | | Ground | |
| 37 | 39 | bit2A_Q | Bit 2 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 38 | 40 | $\overline{bit2A\_Q}$ | | Negative output | Signal | |
| 39 | 41 | bit2B_Q | Bit 2 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 40 | 42 | $\overline{bit2B\_Q}$ | | Negative output | Signal | |

Continued on next page

Table 3.3 – continued from previous page

| Pin # | Pad # | Pin Name | Description | | Direction | Condition |
|---|---|---|---|---|---|---|
| 41 | 43 | bit1A_Q | Bit 1 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 42 | 44 | $\overline{bit1A\_Q}$ | | Negative output | Signal | |
| 43 | 45 | bit1B_Q | Bit 1 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 44 | 46 | $\overline{bit1B\_Q}$ | | Negative output | Signal | |
| 45 | 47 | bit0A_Q | Bit 0 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 46 | 48 | $\overline{bit0A\_Q}$ | | Negative output | Signal | |
| 47 | 49 | bit0B_Q | Bit 0 output | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 48 | 50 | $\overline{bit0B\_Q}$ | | Negative output | Signal | |
| 49 | 51 | over_range | Input signal over range | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 50 | 52 | $\overline{over\_range}$ | | Negative output | Signal | |
| 51 | 53 | data_ready | Data ready signal | Positive output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 52 | 54 | $\overline{data\_ready}$ | | Negative output | Signal | |
| 53 | 55 | $\overline{bit0B\_I}$ | Bit 0 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 54 | 56 | bit0B_I | | Positive output | Signal | |
| 55 | 57 | $\overline{bit0B\_Q}$ | Bit 0 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 56 | 58 | bit0B_Q | | Positive output | Signal | |
| 57 | 59 | $\overline{bit1B\_I}$ | Bit 1 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 58 | 60 | bit1B_I | | Positive output | Signal | |
| 59 | 61 | $\overline{bit1B\_Q}$ | Bit 1 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 60 | 62 | bit1B_Q | | Positive output | Signal | |
| 61 | 63 | $\overline{bit2B\_I}$ | Bit 2 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 62 | 64 | bit2B_I | | Positive output | Signal | |

Continued on next page

Table 3.3 – continued from previous page

| Pin # | Pad # | Pin Name | Description | | Direction | Condition |
|---|---|---|---|---|---|---|
| 63 | 65 | $\overline{bit2B\_Q}$ | Bit 2 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 64 | 66 | bit2B_Q | | Positive output | Signal | |
| 65 | 67 | $V_{CC}$_lvdsI | LVDS Driver Supply for converter I | | Supply | +3.0V±10% |
| 66 | 68 | Gnd_lvdsI | LVDS Driver Ground for converter I | | Ground | |
| 67 | 69 | $\overline{bit3B\_I}$ | Bit 3 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 68 | 70 | bit3B_I | | Positive output | Signal | |
| 69 | 71 | $\overline{bit3B\_Q}$ | Bit 3 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 70 | 72 | bit3B_Q | | Positive output | Signal | |
| 71 | 73 | Gnd_digI | Digital Ground for converter I | | Ground | |
| | 74 | | | | Ground | |
| 72 | 75 | $V_{CC}$_digI | Digital Supply for converter I | | Signal | +3.0V ±10% |
| | 76 | | | | Signal | |
| 73 | 77 | $\overline{bit4B\_I}$ | Bit 4 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 74 | 78 | 4_I | | Positive output | Signal | |
| 75 | 79 | $\overline{bit4B\_Q}$ | Bit 4 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 76 | 80 | bit4B_Q | | Positive output | Signal | |
| 77 | 81 | $\overline{bit5B\_I}$ | Bit 5 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 78 | 82 | bit5B_I | | Positive output | Signal | |
| 79 | 83 | $\overline{bit5B\_Q}$ | Bit 5 output | Negative output | Signal | LVDS Output, $R_{load}$: $100\Omega \pm 10\%$ |
| 80 | 84 | bit5B_Q | | Positive output | Signal | |

Table 3.4: *Thames* ASIC I/O summary

| Pin Type | Total |
|---|---|
| Signal | 58 |
| Supply | 8 |
| Ground | 11 |
| Miscellaneous | 3 |
| Not connected | 0 |

As I/O pin designation summary, there are 58 signal pins, 8 supply pins, and 11 ground pins, each. There are 3 miscellaneous pins for temperature-sense, -control, and external bias resistance. *Thames* ASIC bond-wired package diagram is also illustrated in Figure 3.8.

### 3.6.2 I/O description

Throughout this subsection the terms "analog I/O" and "digital I/O" refer to inputs and outputs which have signals (analog or digital) and data (digital) on them respectively. The functionality of all other pins (excluding power supply and ground) are listed under the sub-heading "miscellaneous I/O."

### 3.6.3 Power supply

All ground (GND) and power supply voltages must be present for the duration of the tests. The impedance of any power supply or ground connection should be $< 0.1\Omega$. Table 3.5 lists the pins which should be connected to ground. The power supply voltages listed in Table 3.6 should be connected to the *Thames* ASIC for

Table 3.5: HNS *Thames* ASIC ground connections

| Pin # | Signal Name |
|---|---|
| 4 | Gnd_sub |
| 5 | Gnd_aI |
| 8 | Gnd_aI |
| 13 | Gnd_aQ |
| 16 | Gnd_aQ |
| 17 | Gnd_sub |
| 18 | Gnd_ESD |
| 30 | Gnd_digQ |
| 36 | Gnd_lvdsQ |
| 66 | Gnd_lvdsI |
| 71 | Gnd_digI |

Table 3.6: *Thames* ASIC supply voltages

| Pin # | Signal Name | Voltage | Current Limits (mA) |
|---|---|---|---|
| 3 | $V_{CC}$_5V_lvdsI | 5.0 | 150 |
| 9 | $V_{CC}$_5VI | 5.0 | 75 |
| 12 | $V_{CC}$_5VQ | 5.0 | 75 |
| 19 | $V_{CC}$_5V_lvdsQ | 5.0 | 150 |
| 29 | $V_{CC}$_digQ | 3.0 | 650 |
| 35 | $V_{CC}$_lvdsQ | 3.0 | 120 |
| 65 | $V_{CC}$_lvdsI | 3.0 | 120 |
| 72 | $V_{CC}$_digI | 3.0 | 650 |

the duration of the test. The voltages listed in Table 3.6 should have a tolerance of $\pm 1\%$ and a voltage overshoot of $\leq 10\%$. A suggested excess current limit as listed in Table 3.6 should be observed as each power-supply connection.

The power supply sequencing and decoupling are also important. The ASIC does not require any sequencing of the supply voltages during power-up. All supply voltages should be applied at the same instance in time. All power supply pins

require external decoupling using good quality capacitors. Dependent on whether pin is used to supply analog or high-speed logic circuitry, standard de-coupling practice should be used.

### 3.6.4 Analog inputs

The chip has two pairs of differential analog inputs; in_I+ and in_I− (pins 7 and 6), and in_Q+ and in_Q− (pins 14 and 15). Each of the two input pairs is one input to a differential amplifier, as shown in Figure 3.12 below. The inputs to each transistor pair are self-biased internal to the ASIC ensuring the optimal common-mode voltage is maintained over all operating conditions. In application signals should be AC coupled to the inputs through a high quality capacitor. The input signal can be applied differentially or single-ended. If a single-ended signal is applied to either input, the unused input should not, under any circumstance, be left floating but coupled to a low-impedance node (usually ground) through the same value and type of capacitor used to couple the signal into the other input.

The self-biasing is achieved by connecting each of the inputs (in_I+ and in_I−, in_Q+ and in_Q−) to a low impedance voltage reference internal to the ASIC through a 9 kΩ resistor. If for any reason the signal source is DC-coupled to the differential input, care must be taken to ensure the mean level of the drive signal falls within the common-mode range of the transistor pair. The driving source must be able to source or sink sufficient DC-current, to compensate for the voltage

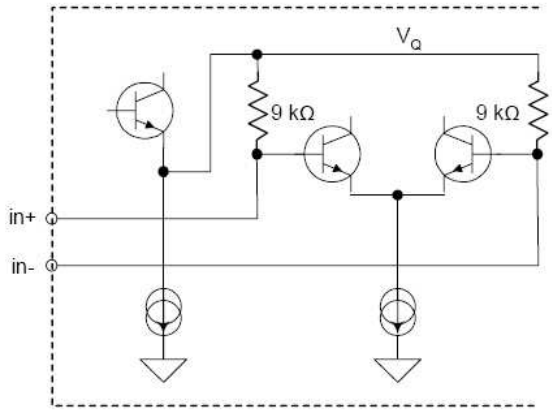



Figure 3.12: HNS *Thames* ASIC RF input equivalent circuit for I-channel input (Q-channel is the same)

differential with the low impedance source internal to the chip.

For a DC-coupled, single-ended drive, the unused input must be biased from a low-impedance voltage source equal to the mid-point of the drive signal. DC offsets between the analog inputs (+ and −) may result in performance degradation and an increase in distortion products.

### 3.6.5 Digital inputs

The chip has a differential logic input, 'clk' and '$\overline{\text{clk}}$' (pin 10 and pin 11) comprised of a differential transistor pair. The configuration of the input is similar to that described in Section 3.6.4 for differential analog inputs and illustrated in Figure 3.13.

In applications, the input is designed to be driven from a continuous waveform

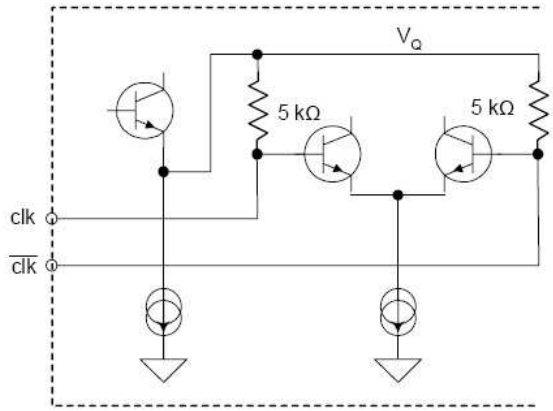



Figure 3.13: HNS *Thames* ASIC RF input equivalent circuit for sampling clock input

signal generator (or source). The input should never be driven from a signal with standard 3.3 or 5V logic levels.

The clock inputs (pin 10 and pin 11) are self-biased through a 5 kΩ resistor. If for any reason the signal source is DC coupled to the differential input, care must be taken to ensure the mean level of the drive signal falls within the common-mode range of the transistor pair. The driving source must be able to source or sink sufficient DC-current, to compensate for the voltage differential with the low impedance source internal to the *Thames* ASIC.

For a DC-coupled, single-ended drive, the unused input must be biased from a low-impedance voltage source equal to the mid-point of the drive signal. Any offset between the bias voltage and the midpoint of the drive-signal will result in the loss of sensitivity at the digital input. If the voltage offset between the two inputs is

Table 3.7: Electrical parameters for custom differential clock inputs

| | Parameter | | min. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| $V_{IH}$ | High-level input voltage (differential) | clk | $V_Q + 0.125$ | $V_Q + 0.2$ | V | $V_{CC}$-dig : 3.0V; $V_Q$ : 2.2V±200mV |
| | | $\overline{\text{clk}}$ | $V_Q - 0.125$ | $V_Q - 0.2$ | | |
| $V_{IL}$ | Low-level input voltage (differential) | clk | $V_Q - 0.125$ | $V_Q - 0.2$ | V | $V_{CC}$-dig : 3.0V; $V_Q$ : 2.2V±200mV |
| | | $\overline{\text{clk}}$ | $V_Q + 0.125$ | $V_Q + 0.2$ | | |
| $V_{IH}$ | High-level input voltage (single-ended) | clk | $V_Q + 0.25$ | $V_Q + 0.3$ | V | $V_{CC}$-dig : 3.0V; $V_Q$ : 2.2V±200mV |
| | | $\overline{\text{clk}}$ | $V_Q$ | $V_Q$ | | |
| $V_{IL}$ | Low-level input voltage (single-ended) | clk | $V_Q - 0.25$ | $V_Q - 0.3$ | V | $V_{CC}$-dig : 3.0V; $V_Q$ : 2.2V±200mV |
| | | $\overline{\text{clk}}$ | $V_Q$ | $V_Q$ | | |
| $V_{IH}$ | High-level input voltage (single-ended) | clk | $V_Q$ | $V_Q$ | V | $V_{CC}$-dig : 3.0V; $V_Q$ : 2.2V±200mV |
| | | $\overline{\text{clk}}$ | $V_Q - 0.25$ | $V_Q - 0.3$ | | |
| $V_{IL}$ | Low-level input voltage (single-ended) | clk | $V_Q$ | $V_Q$ | V | $V_{CC}$-dig : 3.0V; $V_Q$ : 2.2V±200mV |
| | | $\overline{\text{clk}}$ | $V_Q + 0.25$ | $V_Q + 0.3$ | | |

larger than 100-mV, functionality cannot be guaranteed.

There are three different ways the logic signal can be applied to the clock input; drive conditions are listed in Table 3.7. The quiescent voltage ($V_Q$) is the 'self' bias voltage of the input as measured in later chapter.

Termination of these input(s) is left at the discretion of the 'test authority'. There should be no DC current leakage from the ASIC input pin through the termination to ground (or terminating node).

#### 3.6.5.1 Clock-cycle

The term "clock-cycle" refers to the application of a static (as opposed to free-running) clock applied to the clock input (pin 10 and pin 11). A clock-cycle is defined as the application of a '$0 \rightarrow 1 \rightarrow 0$' logic sequence in accordance with the levels defined in Table 3.7.

Table 3.8: HNS *Thames* ASIC electrical parameters for LVDS output drivers

| | Parameter | min. | Max. | Unit |
|---|---|---|---|---|
| $V_{OD}$ | Differential output voltage | 0.20 | 0.45 | V |
| $V_{OS}$ | Offset voltage | 1.125 | 1.375 | V |
| $\Delta V_{OD}$ | \|Change to $V_{OD}$\| | | 50 | \|mV\| |
| $\Delta V_{OS}$ | \|Change to $V_{OS}$\| | | 50 | \|mV\| |

I/O Supply voltage $V_{DD}$: 3.0V
-40°C $\leq T_{amb} \leq$ +85°C except where specified.

### 3.6.6 Logic outputs: LVDS [36, 37]

All the digital outputs of the evaluated chip are differential and should be compliant with IEEE standard 1596.3 [34, 35]. The logic state of each output pair is determined by the polarity of the differential output voltage ($V_{OD}$) between any output (< pin_name >) with respect to its compliment (< $\overline{\text{pin\_name}}$ >); for example < Bit5A_I > and < $\overline{\text{Bit5A\_I}}$ >. Logic '1' is defined as $V_{\text{Bit5A\_I}} > V_{\overline{\text{Bit5A\_I}}}$ ($V_{OD}$ is positive), and logic '0' is defined as $V_{\text{Bit5A\_I}} < V_{\overline{\text{Bit5A\_I}}}$ ($V_{OD}$ is negative).

Table 3.8 lists the electrical parameters for the LVDS output drivers. Figure 3.14 shows the relationship between the offset voltage($V_{OS}$) and the differential output voltage ($V_{OD}$).

The relationships of the offset voltage ($\Delta V_{OS}$ and $\Delta V_{OD}$ are illustrated in Figure 3.15. The output code format from the ADC is Two(2)'s complement as shown in Table 3.9

The output drivers are designed to operate into a differential terminating impedance of 100 Ω. The suggested method of terminating each differential output

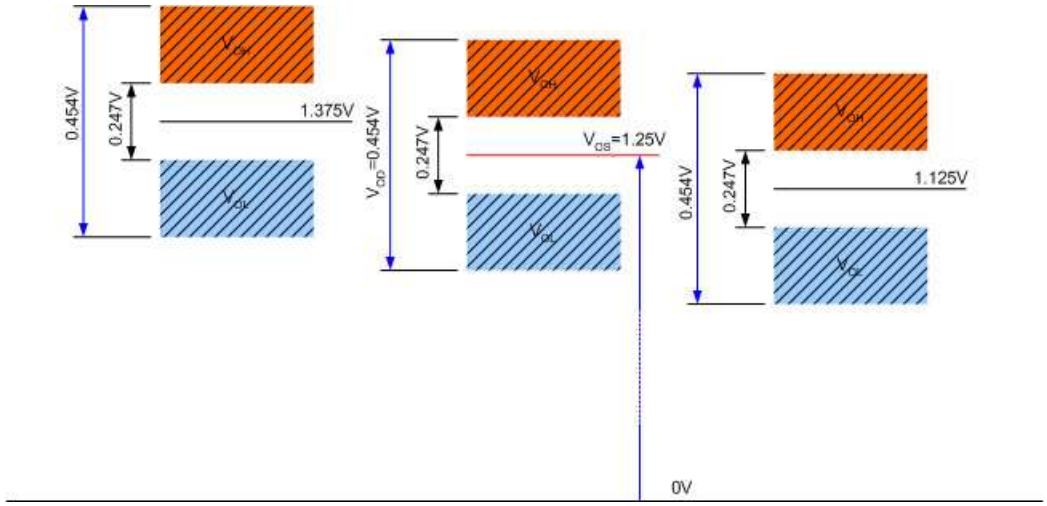



Figure 3.14: LVDS output voltage levels

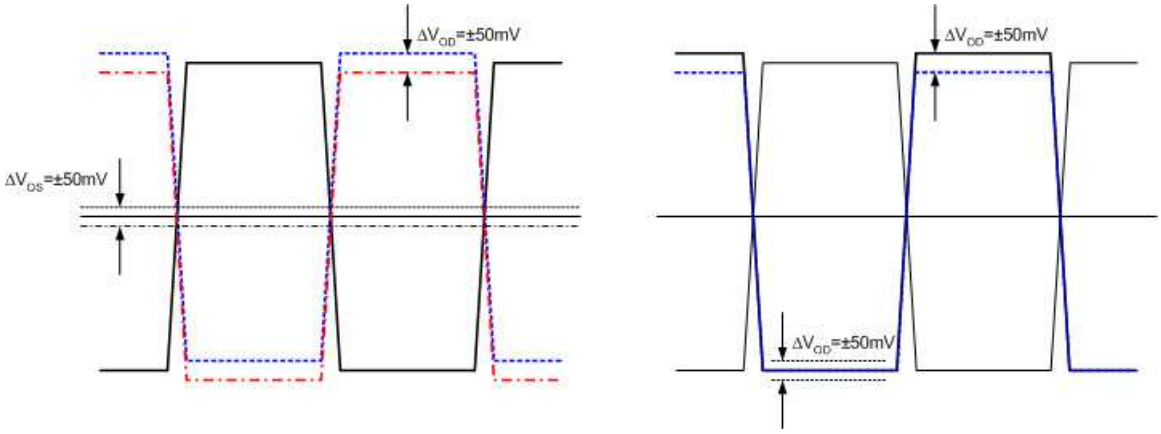



Figure 3.15: LVDS digital output signals and LVDS offset

Table 3.9: Digital output code

| **Scale** | **Over range** | **Output Code**[1] |
|---|---|---|
| +full scale + 1LSB | 1 | 011111 |
| +full scale | 0 | 011111 |
| +full scale − 1LSB | 0 | 011110 |
| +full scale − 2LSB | 0 | 011101 |
| | 0 | 011100 |
| ⋮ | ⋮ | ⋮ |
| | 0 | 000011 |
| mid-range + 2LSB | 0 | 000010 |
| mid-range + 1LSB | 0 | 000001 |
| mid-range | 0 | 000000 |
| mid-range − 1LSB | 0 | 111111 |
| mid-range − 2LSB | 0 | 111110 |
| | 0 | 111101 |
| ⋮ | ⋮ | ⋮ |
| | 0 | 100011 |
| −full scale + 2LSB | 0 | 100010 |
| −full scale + 1LSB | 0 | 100001 |
| −full scale | 0 | 100000 |
| −full scale − 1LSB | 1 | 100000 |

note[1] : MSB ('bit5') is shown on the left-hand side

All code sequences read from left to right MSB to LSB ('bit0')

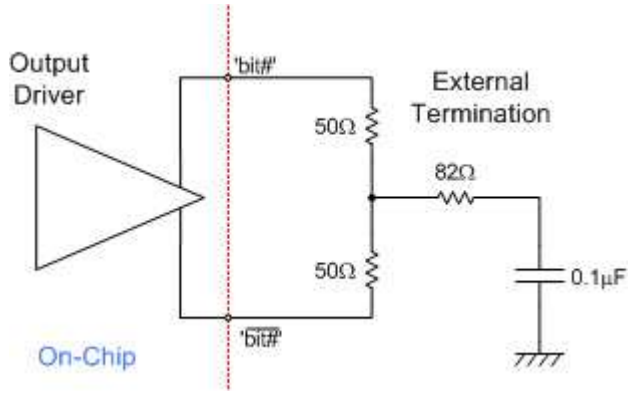



Figure 3.16: LVDS output driver termination

is illustrated in Figure 3.16. $R_{Load}$, as used throughout this document and unless otherwise stated, refers to the composite load presented to each output and not an individual resistor values.

### 3.6.7 Miscellaneous I/O

A precision external resistor of 2.0kΩ ±1% is used to set the bias current for the Current Mode Logic (CML). The resistor is connected between 'Rext' (pin 20) and '$V_{CC}$_digQ' (pin 72).

The Thames ASIC contains additional circuitry for monitoring the die temperature. A voltage, which changes proportionally with temperature, is output through 'temp_I' (pin 1); the monitoring circuit is controlled (switched on or off) using 'temp_ctl' (pin 2).

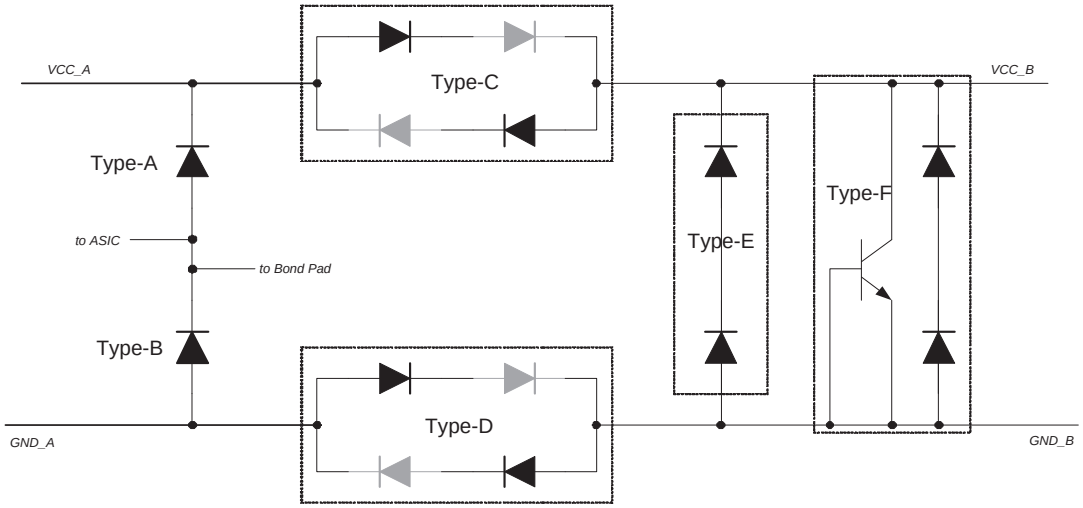


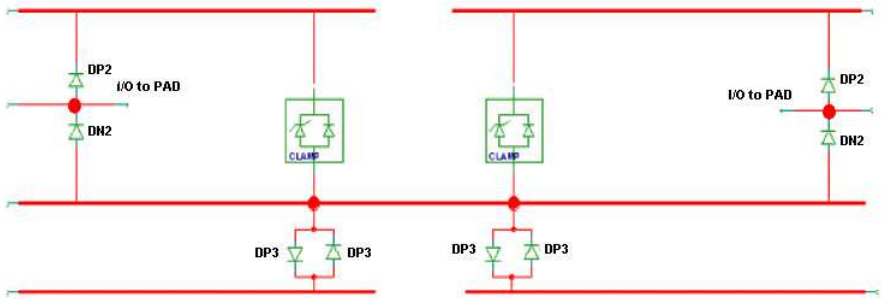

Figure 3.17: ESD diode structure types

## 3.7 Electrostatic-discharge(ESD) protection

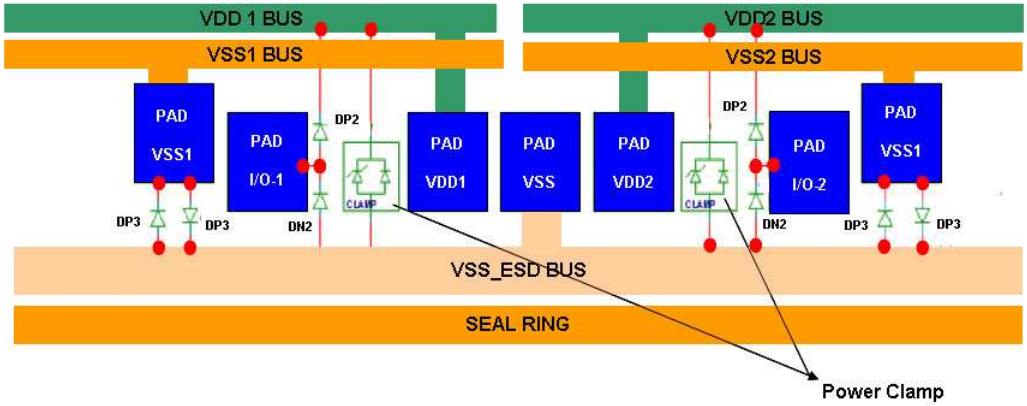
The chip core circuitries are vulnerable to damage from any electrostatic discharge. All steps where the chip is handled or probed (wafer test, dice-and-pick operations, shipping, packaging, module testing, card assembly, and customer handling) can cause ESD damage [38].

Absence of the ESD protection or Low ESD tolerance can cause numerous problems in qualification, manufacturing, test, and assembly operations. Therefore, ESD must be addressed at the beginning of the design cycle. Because ESD protection circuits interact with the design, the product must be developed and debugged with the ESD circuit loads present. Also, ESD protection can require design iterations.

The chip ESD diode type follows the structure in Figure 3.17 and the con-




(a) Schematic




(b) Layout

Figure 3.18: HNS *Thames* ASIC General configuration of multi-supply clamp and input protection scheme

nections are listed in Table 3.10. Note that pin number 3, 9, 12, 19, 29, 36, 65, and 72 has the supply shunt configuration. The chip I/O protection scheme follows the ATMEL's general configuration of multip-supply clamp and input protection as shown in Figure 3.18 ESD-diodes connected to the signal pins are reversed-biased under normal operating conditions.

Table 3.10: HNS *Thames* ASIC high-speed ADC ESD diode connections

| **From** | | **To** | | **Type** | **Cell Library Name** |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Pin #** | **Pin Name** | | |
| 1 | temp_I | 3 | Vcc_5V_lvds | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 2 | temp_ctl | 3 | Vcc_5V_lvds | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 3 | Vcc_5V_lvdsI | 18 | Gnd_ESD | F | DP2/DN2 |
| 4 | Gnd_sub | 18 | Gnd_ESD | D | DP3//DP3 |
| 5 | Gnd_aI | 18 | Gnd_ESD | F | DP3//DP3 |
| 6 | in_I− | 12 | Vcc_aQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 7 | in_I+ | 12 | Vcc_aQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 8 | Gnd_aI | 18 | Gnd_ESD | D | DP3//DP3 |
| 9 | Vcc_aI | 18 | Gnd_ESD | F | DP2/DN2 |
| 10 | clk | 72 | Vcc_digI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 11 | $\overline{\text{clk}}$ | 72 | Vcc_digI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 12 | Vcc_aQ | 18 | Gnd_ESD | F | DP2/DN2 |
| 13 | Gnd_aQ | 18 | Gnd_ESD | D | DP3//DP3 |

Continued on next page

Table 3.10 – continued from previous page

| From | | To | | Type | Cell Library Name |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Pin #** | **Pin Name** | | |
| 14 | in_Q+ | 12 | Vcc_aQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 15 | in_Q− | 12 | Vcc_aQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 16 | Gnd_aQ | 18 | Gnd_ESD | D | DP3//DP3 |
| 17 | Gnd_sub | 18 | Gnd_ESD | D | DP3//DP3 |
| 18 | Gnd_ESD | 12 | Vcc_aQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 19 | Vcc_5V_lvdsQ | 18 | Gnd_ESD | F | DP2/DN2 |
| 20 | Rext | 19 | Vcc_5V_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 21 | bit5A_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 22 | $\overline{\text{bit5A\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 23 | bit5B_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 24 | $\overline{\text{bit5B\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 25 | bit4A_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 26 | $\overline{\text{bit4A\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 27 | bit4B_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 28 | $\overline{\text{bit4B\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 29 | Vcc_digQ | 18 | Gnd_ESD | F | DP2/DN2 |
| 30 | Gnd_digQ | 18 | Gnd_ESD | D | DP3//DP3 |

Continued on next page

Table 3.10 – continued from previous page

| From | | To | | Type | Cell Library Name |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Pin #** | **Pin Name** | | |
| 31 | bit3A_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 32 | $\overline{\text{bit3A\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 33 | bit3B_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 34 | $\overline{\text{bit3B\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 35 | Vcc_lvdsQ | 18 | Gnd_ESD | F | DP2/DN2 |
| 36 | Gnd_lvdsQ | 18 | Gnd_ESD | D | DP3//DP3 |
| 37 | bit2A_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 38 | $\overline{\text{bit2A\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 39 | bit2B_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 40 | $\overline{\text{bit2B\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 41 | bit1A_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 42 | $\overline{\text{bit1A\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 43 | bit1B_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 44 | $\overline{\text{bit1B\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 45 | bit0A_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 46 | $\overline{\text{bit0A\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 47 | bit0B_Q | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |

Continued on next page

Table 3.10 – continued from previous page

| From | | To | | Type | Cell Library Name |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Pin #** | **Pin Name** | | |
| 48 | $\overline{\text{bit0B\_Q}}$ | 35 | Vcc_lvdsQ | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 49 | over_range | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 50 | $\overline{\text{over\_range}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 51 | $\overline{\text{data\_ready}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 52 | data_ready | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 53 | $\overline{\text{bit0B\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 54 | bit0B_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 55 | $\overline{\text{bit0A\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 56 | bit0A_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 57 | $\overline{\text{bit1B\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 58 | bit1B_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 59 | $\overline{\text{bit1A\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 60 | bit1A_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 61 | $\overline{\text{bit2B\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 62 | bit2B_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 63 | $\overline{\text{bit2A\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |

Continued on next page

Table 3.10 – continued from previous page

| From | | To | | Type | Cell Library Name |
|---|---|---|---|---|---|
| **Pin #** | **Pin Name** | **Pin #** | **Pin Name** | | |
| 64 | bit2A_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 65 | Vcc_lvdsI | 18 | Gnd_ESD | F | DP2/DN2 |
| 66 | Gnd_lvdsI | 18 | Gnd_ESD | D | DP3//DP3 |
| 67 | $\overline{\text{bit3B\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 68 | bit3B_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 69 | $\overline{\text{bit3A\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 70 | bit3A_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 71 | Gnd_digI | 18 | Gnd_ESD | D | DP3//DP3 |
| 72 | Vcc_digI | 18 | Gnd_ESD | F | DP2/DN2 |
| 73 | $\overline{\text{bit4B\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 74 | bit4B_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 75 | $\overline{\text{bit4A\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 76 | bit4A_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 77 | $\overline{\text{bit5B\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 78 | bit5B_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 79 | $\overline{\text{bit5A\_I}}$ | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |
| 80 | bit5A_I | 65 | Vcc_lvdsI | A | DP2 |
| | | 18 | Gnd_ESD | B | DN2 |

This device is ESD sensitive and may suffer damage from Electrical Over-Stress (EOS). We observed standard ESD precautions should be applied. That is, wrist ground straps and ESD gloves are worn, ESD work surface mats are used while handling this device during test.

The general EOS requirement for the *Thames* ASIC is a 2kV Human Body Model (HBM) or 500V Charge Distribution Model (CDM) on all pins and pin-to-pin combinations unless otherwise stated.

## 3.8 Summary

In this chapter, the author described all the I/O functions of the *Thames* chip used as examples in this thesis. The design specifications were defined as were the functional requirements, performance requirements, electrical specifications, packaging and other mechanical specifications such as environmental specifications. This component will be used in modern satellite base-band receivers requiring accurately defined gain and phase matching. As we shall see, this requirement describes the test plan generated in the following chapter.

The HNS *Thames* ASIC design approach fully exploits the concept of design-for-test (DfT) to enhance the testability and the cost effectiveness of testing in manufacturing, as this pins are used solely for component test. Following is the lists for employing DfT functions on the *Thames* chip:

- Common sampling clock (800MHz) for each channel (I/Q)

- sampling clock synchronization output
- Demultiplexed (6:12) digital output
- 'data_ready' - transfering data rate at 400 MHz
- 'over_range' - monitoring an analog input voltage saturation
- Two's complement digital outputs compliant with IEEE LVDS standard (1596.3)
- Temperature sensing and control
- External bias setting resistor

The DfT enhanced pin designations and their functional descriptions are detailed with a testing fixture and a test set-up in the next chapter.

# Chapter 4

# Test Fixture and Design Verification Test Setup

## 4.1 Overview

Mechanical mounting has an enormous impact on an ability to accurately and precisely measure system performance parameters. To conduct device verification tests (DVTs) for high speed ADCs, an optimum test fixture must be developed to meet not only functional performance specifications but also design stability requirements. That is, test mount must minimize matching and environmental noise issue. The ADC DVT fixture should be able to verify if the ADC design meets the requirements as stated in the design specification and reveal the limitations of the ADC design.

This chapter describes a methodology for hardware development of high-speed

ADC testing fixtures. The author provides both functional performance specifications and design stability requirements. From the moment the designed ADC has been fabricated on a wafer or placed into a package, testing of the ADC occurs in a laboratory environment. Prior to establishing the laboratory test equipment, an efficient means to route the signals from the test equipment to the high-speed ADC (HNS *Thames*) must be determined. In this stage, many puzzling questions can be brought such as load boards, contactors, handlers, wafer probes and probers, and etc. This chapter provides a guide, showing how to group equipment in a common locale for maximally efficient test execution

## 4.2 Test fixture and periphery subsystem design for speed

ADC chips must admit high-frequency signals. This make it imperative to maintain a quiet and stable noise environment. The ADC DVT fixture design must be built around the performance specification of the instrumentation which is used for the test. The fixture must also ensure that the performance of the ADC is maintained and not limited by the test instrument and/or DVT fixtures and boards. Therefore, consideration needs to be given to the loads and matching circuits used on the characterization board, and any wafer probing requirements. To reduce the high test cost associated with wafer-level characterization and a complex probe card design, most ADC testing is done on packaged devices. For our work, the ADC is mounted in a 0.5 mm pin-pitch 80-pin, thermally enhanced thin quad flat package

(TQFP) with a 12 × 12 mm body.

The high speed ADC fixture design process includes development of a production level DUT socket design, matching networks, thermal controllers, and a power supply decoupler. The fixture design process leads to the fabrication of a printed circuit board (PCB) design to optimize test signal coupling to the device-under-test (DUT). The process also lead to the definition of a test system, as it has all of the test equipment in one location to perform all necessary tests. During the proto-type design verification process, the DVT fixture is not yet fully production worthy but extendable. The fixture must have the means to quickly place a DUT (ADC) into and out of the test setup and virtually eliminate human interaction when testing in large volume.

The following sections are about the interfacing socket and handler and subsystem peripheries required to characterize and to verify the designed high-speed ADC. Figure 4.1 shows the test fixture PCB with an ADC socket input built assembly of this thesis work. The details follow:

### 4.2.1 The ADC socket

The interface between the ADC and load board can be provided by contactor sockets, or contactors, or simply DUT sockets. Actually, the contactor sockets are the most critical element of the testing and the production test solution. Commonly, an expensive automatic test equipment(ATE) and handler equipment have been inter-

Figure 4.1: High speed dual channel 6-bit ADC test fixture with a mounting socket

faced with an testing load board. A poorly designed contactor can destroy the entire setup. The redesign of a contactor can significantly delay the device time-to-market window.

There are many kinds of contactor socket technologies available. A selection depends on the style of package to be tested. The contactor sockets are mechanical and have a limited lifetime, minimizing the number of DUT insertion possible. When selecting a contactor socket, we require that it can be replaced quickly and easily, as it will be replaced frequently on the final production-test floor. It is essential to meet certain electrical, mechanical, and thermal performance requirements when selecting or designing a contactor socket.

There are also cost's accuracy trade-offs. If utmost accuracy of measurements is needed, it is recommended to select an expensive contactor with a low lifetime. For engineering and characterization purposes, it is often desired to have a contactor socket with a clamp, so that a test engineer may manually place a DUT onto the load board. This can be critical during load board debugging since impedance matching can be performed on the load board.

As mentioned earlier, the designed high-speed ADC is assembled in a 0.5 mm pin-pitch 80-pin, thermally enhanced thin quad flat package (TQFP) with a 12 $\times$ 12 mm body. For our design example, we chose a contactor socket with a clamp as shown in Figure 4.2. The mounting contactor socket consists of two part: socket assembly (bottom) and lid (top) as shown in Figure 4.3 and Figure 4.4, each. The

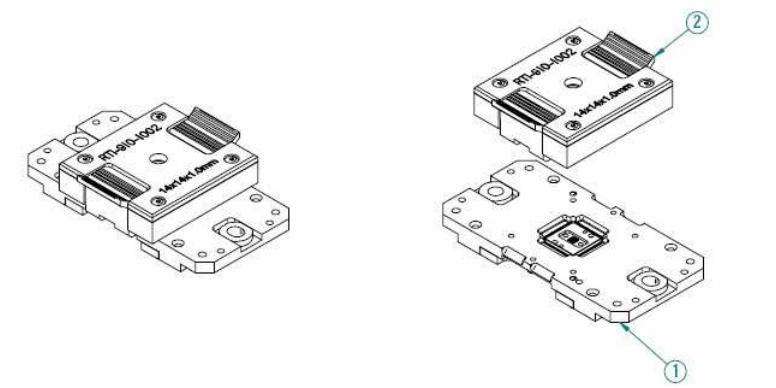



Figure 4.2: High speed dual channel 6-bit ADC (TQFN packaged) mounting socket: 1 - socket assembly (bottom), 2 - socket lid (top) developed for this work

contactor socket mechanical details are also illustrated in Figure 4.5.

The main high-speed socket design considerations are: contact resistance, parasitic inductance, and capacitance between outputs and ground. These parasitics can be minimized when the ADC is soldered directly to the PCB in system-level applications. However, direct soldering is usually not an option as the part must be de-mounted for sale. To minimize parasitics, we used a front-access spring loaded customized pogo pin socket with a dual-latch clip-on socket top. This insures a stable and reliable electrical contact. The placement of the ADC is also mechanically facilitated by the use of a planarized ADC mounting platform in the socket. Finally, a thermal heat sink within the testing socket enhances the thermal conductivity from the TQFP packaged ADC to the bottom of the test fixture board platform.

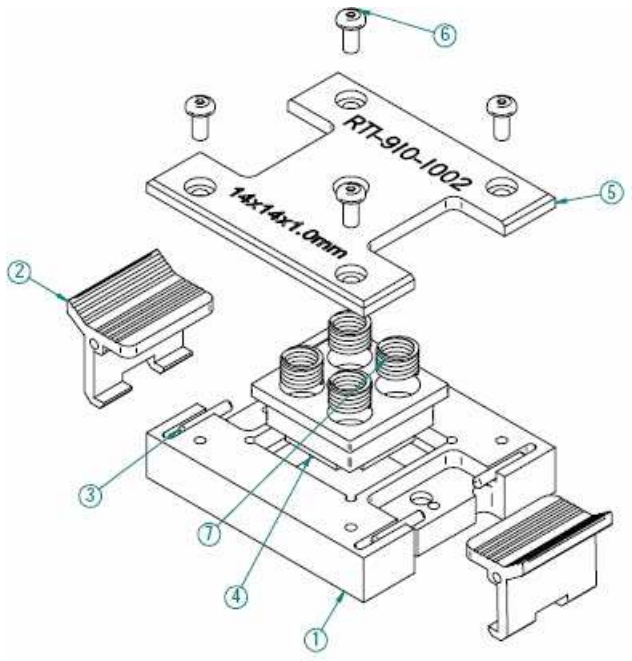



Figure 4.3: High speed dual channel 6-bit ADC (TQFN packaged) mounting socket dual latch lid assembly: 1 - Lid base, 2 - Latch, 3 - Dowel pin, 4 - Pressure plate, 5 - Lid top, 6 - Button head screw, 7 - Spring

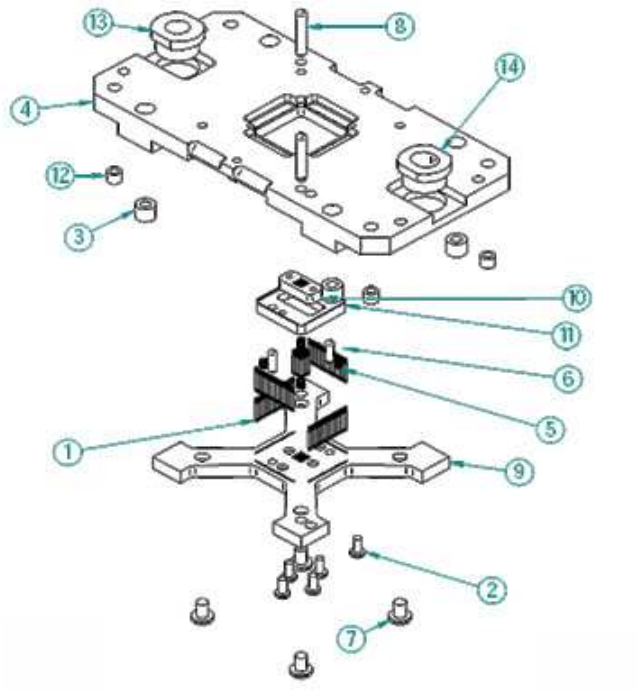



Figure 4.4: High speed dual channel 6-bit ADC (TQFN packaged) mounting socket assembly (bottom): 1 - Pogo pin, 2 - Button head screw, 3 - Threaded insert, 4 - Socket top, 5 - Sring, 6 - Dowel pin, 7 - Button head screw, 8 - Dowel pin, 9 - socket base, 10 - Retainer, 11 - Floating base, 12 - Threaded insert, 13 - Guide bushing, 14 - Guide bushing

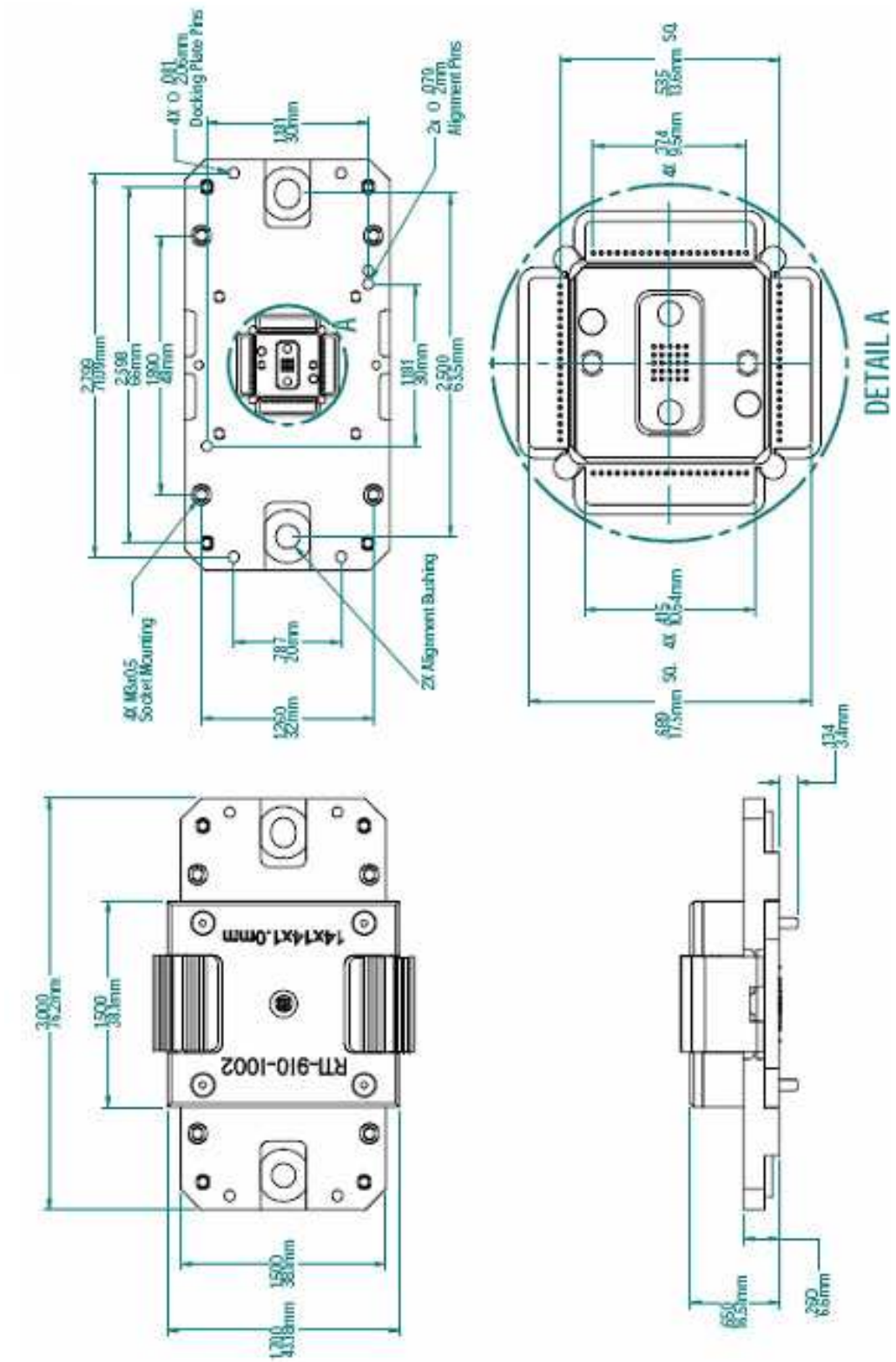



Figure 4.5: High speed dual channel 6-bit ADC (TQFN packaged) mounting socket mechanical drawing

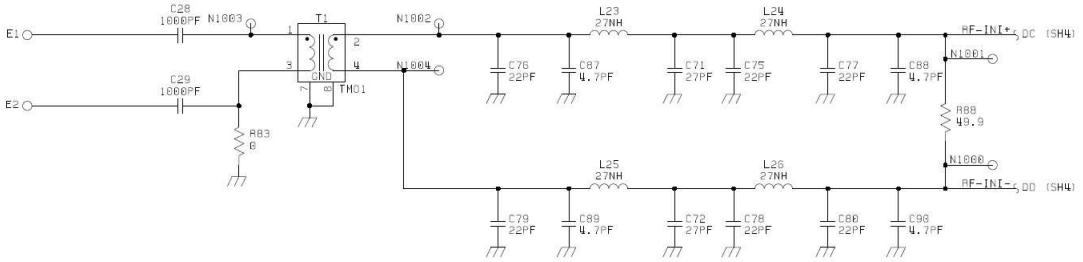



Figure 4.6: High speed dual channel 6-bit ADC *Thames* RF input for I-channel

### 4.2.2 Sub-system design for I/Os

The HNS 6-bit dual channel ADC has differentially driven inputs that are internally biased. The ADC clock input is also based on differential inputs and is driven with internal bias circuit. Each of 3-input pairs for these analog inputs (I/Q) and clock inputs comprise a differential transistor pair and require on-chip self-biasing. This ensures that the common-mode voltage to the pair is always optimal. Ideally, external signals should be AC coupled into these inputs. If any of differential inputs are DC-coupled, care must be taken to ensure the mean level of the driving signal falls within the common-mode range of the input differential-pairs, and the differential transistors are not over-driven. This reduced the complexity of the peripheral subcircuit design effort for DfT techniques. Analog input driving network for I-channel (Q-channel is identical) and clock input network are shown in Figure 4.6 and Figure 4.7.

The logic outputs are configured as fully differential outputs which are compli-

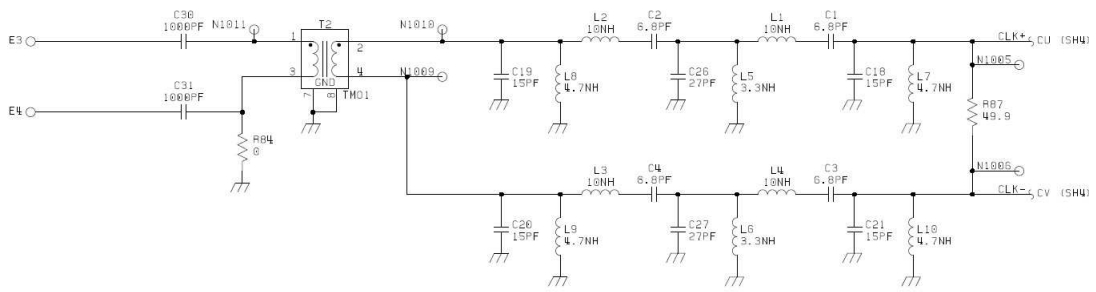



Figure 4.7: High speed dual channel 6-bit ADC *Thames* RF input for clock

ant with IEEE low voltage differential signals (LVDS) Standard 1596.3-1996 [34, 35]. The logic outputs can be optionally buffered with conventional LVDS buffers to convert differential output logic signals to single-ended TTL signals to measure the output logic data. However, the single-end buffered TTL outputs limit the maximum speed of the ADC clock and cause the characterization and verification can only occur below 400 Mbits/s rate due to the external LVDS receiver electrical performance.

### 4.2.3 Power supply decoupling

All power supply pins require external decoupling using good quality capacitors. The main power supply block must have ferrite beads and decoupling capacitors to filter out the high frequency noise coupled from the power supply [40]. The +5.0 V analog supply, +3.0 V digital supply, and +3.0 V and +5.0 V LVDS buffer supplies have independent decoupling capacitors. The separating each analog and

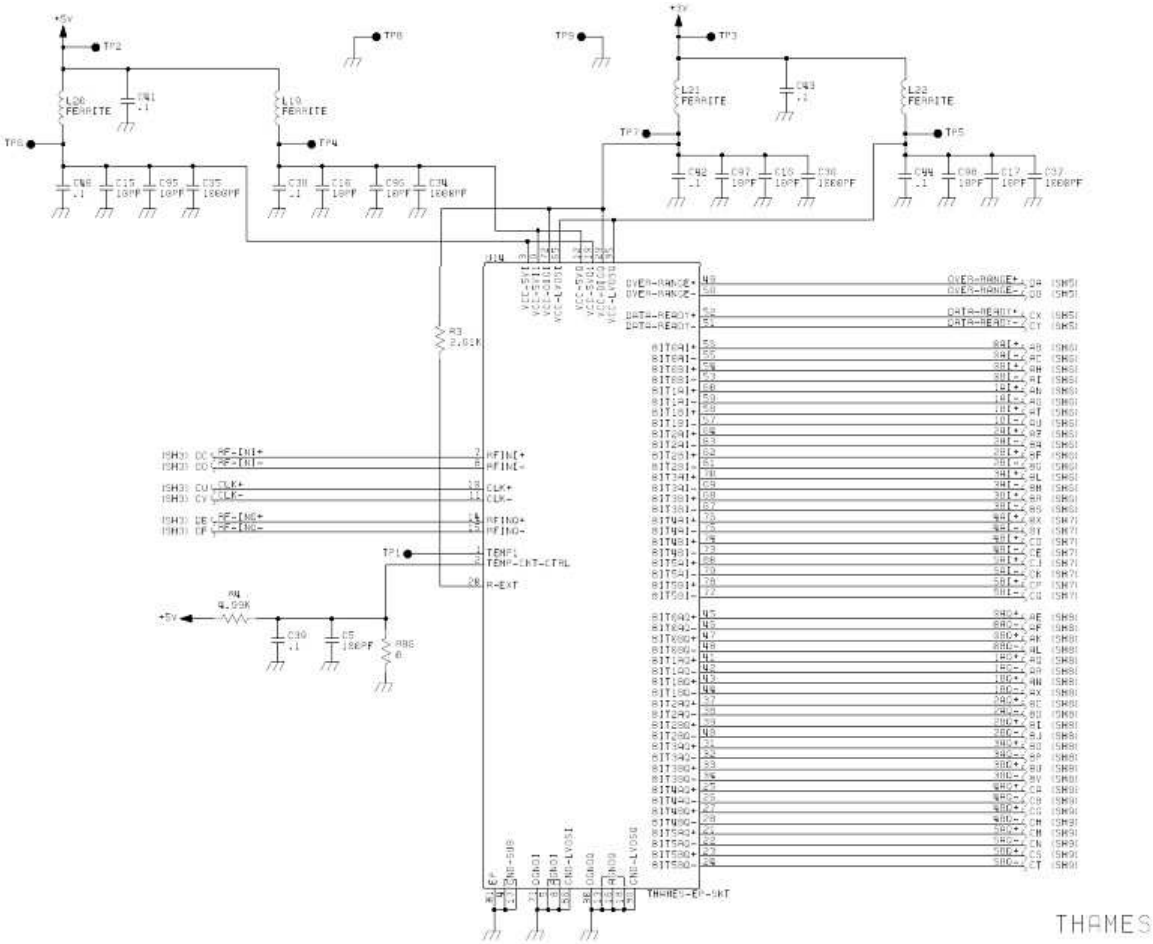



Figure 4.8: High speed dual channel 6-bit ADC ASIC power supply decoupling circuit schematic capture

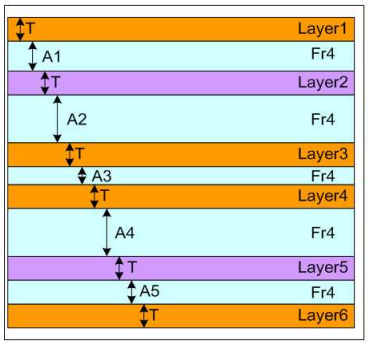
power supplies can lead to monitor the core circuit power consumption carefully. The power supply decoupling schematic is shown in Figure 4.8.

### 4.2.4 Device interface board (DIB) design

A DIB is defined as a printed circuit-board assembly used to route all of the tester pin-out biases to the DUT at the appropriate time. There are several common problems or mistakes in DIB design: power supply hook-ups, grounding, crosstalk, impedance mis-match, tester instrument parasitics, oscillations, poor PCB layout and component placement, and etc. All serve to invalidate a test. Poor power and ground layout results in one of the most common sources of noise injection in mixed-signal DIBs. Crosstalk between analog and digital signal lines is also a common problems [41, 42].

The DIB is independent of the tester and is almost always unique to each DUT that is tested. Developing a DIB for a full production-test solution is one of the most time-consuming process because all of the dc power supply, digital control, mixed signal, and RF signal lines must be routed through this board. Wiring is dense and wiring conflicts are common, so that multilayered DIB are inevitable. Figure 4.9 shows the assembly of the fabricated high-speed ADC DIB layer stack-up information.

The 0.065-inch thickness six-layered PCB is fabricated to isolate signal paths using striplines filled with FR-4 material. Top and bottom layers (layer-1 and layer-




| Layer Name | Layer Refs | Thickness (mil) | Ref Name |
|---|---|---|---|
| Layer 1 | Components Pads Fanouts | 1.4 | T |
| Fr4 | Er | 10.0 | A1 |
| Layer 2 | Ground | 1.4 | T |
| Fr4 | Er | 14 | A2 |
| Layer 3 | Signal | 1.4 | T |
| Fr4 | Er | 10.0 | A3 |
| Layer 4 | Signal | 1.4 | T |
| Fr4 | Er | 14 | A4 |
| Layer 5 | Power Plane +1.0V +1.8V +3.3V | 1.4 | T |
| Fr4 | Er | 8.0 | A5 |
| Layer 6 | Components Pads Fanouts | 1.4 | T |

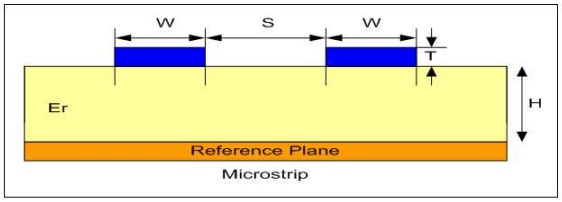
Figure 4.9: High speed dual channel 6-bit ADC test device interface board (DIB) layer stack-up information

6) are used for the component pads of the ADC socket, the subsystem peripherals, and the connectors. Layer-2 is the ground plane and layer-5 is used for the power plane to provide good signal isolation from unwanted external noise sources. Layer-3 and layer-4 are used to distribute the differential analog and clock inputs, as well as the digital outputs. The use of the power plane, as opposed to ground traces, minimizes parasitic inductance and provides overall noise immunity. The power traces must be spaced wide enough to minimize possible parasitic inductive pick-up from signal lines. The signal routes for the clock and analog inputs in layer-3 are optimized to ensure smooth transitions of the equipment port impedance from 50 Ω characteristic impedance to both ADC analog and clock input impedances so that

the device test board fixture can keep unwanted signal skew and phase mismatch at a minimum [40, 43].

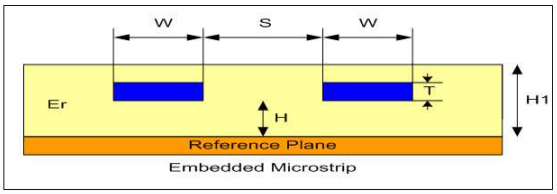
A DIB creation process includes design, layout, fabrication, assembly and test, and possibly multiple redesigns [40, 44, 45]. The making of the DIB is somewhat similar to the actual ADC ASIC physical layout and fabrication. The final impedance matching and tuning (which is necessary after the DIB is fabricated) are often overlooked while a DIB creation process, so that it is better to allow ample time for those efforts. To save significant time in this area, four different signal transmission paths are considered [46]: microstrip, embedded microstrip, and symmetrical and asymmetrical striplines. Figure 4.10 and Figure 4.11 show the examples how the differentially driven analog and clock input signal routes can be designed to create the minimum impedance mismatch.

When laying out the board based on the DIB design schematic shown in Figure 4.12, it is necessary to keep the differential-analog-input subsystems symmetrically disposed so that all parasitics are balanced equally. It is also important to route high speed digital signal traces away from the sensitive analog traces, clock, and reference lines, so that the DIB can avoid or minimize undesirable crosstalk [43]. The fabricated DIB each layer assembly artwork is shown in Figures from 4.13 to 4.22.




| Examples | Height (H) | Width (W) | Thickness (T) | Er | Space (S) | Constant N | Zo | Zdf |
|---|---|---|---|---|---|---|---|---|
| 1 | 5 | 5 | 1.4 | 4.3 | 5 | 5.71 | 62.31144631 | 101.7186275 |
| 2 | 12 | 5 | 1.4 | 4.3 | 5 | 5.71 | 94.18583326 | 127.7624005 |
| 3 | 10 | 4 | 1.4 | 4.3 | 5 | 5.71 | 93.38561717 | 131.2971842 |
| 4 | 12 | 7 | 1.4 | 4.3 | 12 | 5.71 | 84.73745446 | 138.3273552 |
| 5 | 25 | 5 | 1.4 | 4.3 | 11 | 5.71 | 120.9084522 | 165.7349071 |
| 6 | 10 | 5 | 1.4 | 4.3 | 10 | 5.71 | 87.54780314 | 142.9150325 |
| 7 | 10 | 5 | 1.4 | 4.3 | 9 | 5.71 | 87.54780314 | 139.672548 |
| 8 | 10 | 5 | 1.4 | 4.3 | 8 | 5.71 | 87.54780314 | 136.1033538 |
| 9 | 10 | 5 | 1.4 | 4.3 | 7 | 5.71 | 87.54780314 | 132.174531 |
| 10 | 10 | 5 | 1.4 | 4.3 | 6 | 5.71 | 87.54780314 | 127.8498436 |

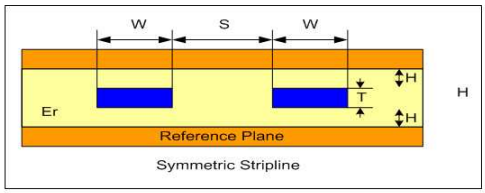
(a) Microstripline impedance calculation




| Examples | Height (H) | Height1 (H1) | Width (W) | Thickness (T) | Er | Space (S) | Constant M | Zo | Zdf |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 10 | 15 | 5 | 1.4 | 4.3 | 5 | 3.879531191 | 68.36635995 | 89.07432012 |
| 2 | 12 | 17 | 5 | 1.4 | 4.3 | 5 | 3.821557054 | 74.10580665 | 94.57033142 |
| 3 | 10 | 15 | 4 | 1.4 | 4.3 | 5 | 3.879531191 | 72.92512763 | 95.0139245 |
| 4 | 12 | 25 | 7 | 1.4 | 4.3 | 12 | 4.129760948 | 64.13569206 | 89.43416538 |
| 5 | 25 | 16 | 5 | 1.4 | 4.3 | 11 | 2.705412595 | 113.0646224 | 170.0291478 |
| 6 | 10 | 25.4 | 5 | 1.4 | 4.3 | 10 | 4.216121418 | 65.58062126 | 88.01887608 |
| 7 | 10 | 25.4 | 5 | 1.4 | 4.3 | 9 | 4.216121418 | 65.58062126 | 86.35709248 |
| 8 | 10 | 25.4 | 5 | 1.4 | 4.3 | 8 | 4.216121418 | 65.58062126 | 84.6312993 |
| 9 | 10 | 25.4 | 5 | 1.4 | 4.3 | 7 | 4.216121418 | 65.58062126 | 82.83903098 |
| 10 | 10 | 25.4 | 5 | 1.4 | 4.3 | 6 | 4.216121418 | 65.58062126 | 80.977727 |

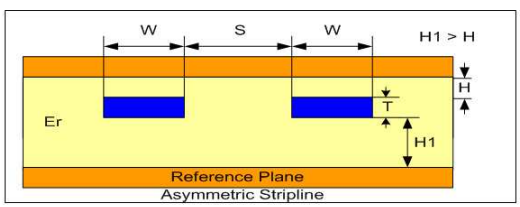
(b) Embedded microstripline impedance calculation

Figure 4.10: Microstriplines impedance calculation chart




| Examples | Height (H) | Width (W) | Thickness (T) | Er | Space (S) | Zo | Zdf |
|---|---|---|---|---|---|---|---|
| 1 | 5 | 5 | 1.4 | 4.3 | 5 | 40.19209268 | 72.5659636 |
| 2 | 6 | 5 | 1.4 | 4.3 | 5 | 44.86911558 | 79.185583 |
| 3 | 10 | 4 | 1.4 | 4.3 | 5 | 63.05388087 | 103.8845748 |
| 4 | 12 | 7 | 1.4 | 4.3 | 12 | 55.86376789 | 101.8767232 |
| 5 | 25 | 5 | 1.4 | 4.3 | 11 | 83.76827217 | 136.282511 |
| 6 | 10 | 5 | 1.4 | 4.3 | 10 | 58.41443535 | 106.3732517 |
| 7 | 10 | 5 | 1.4 | 4.3 | 9 | 58.41443535 | 104.8558774 |
| 8 | 10 | 5 | 1.4 | 4.3 | 8 | 58.41443535 | 103.1182938 |
| 9 | 10 | 5 | 1.4 | 4.3 | 7 | 58.41443535 | 101.1285429 |
| 10 | 10 | 5 | 1.4 | 4.3 | 6 | 58.41443535 | 98.85002893 |

(a) Symmetric stripline impedance calculation




| Example s | Height (H) | Height1 (H1) | Width (W) | Thickness (T) | Er | Space (S) | Constant M | Zo | Zdf |
|---|---|---|---|---|---|---|---|---|---|
| 1 | 10 | 15 | 5 | 1.4 | 4.3 | 5 | 0.83333333 | 64.90492816 | 103.802022 |
| 2 | 12 | 17 | 5 | 1.4 | 4.3 | 5 | 0.82352941 | 69.5856138 | 109.1981117 |
| 3 | 10 | 15 | 4 | 1.4 | 4.3 | 5 | 0.83333333 | 70.05986764 | 112.0462826 |
| 4 | 12 | 25 | 7 | 1.4 | 4.3 | 12 | 0.88 | 65.54682099 | 112.7142251 |
| 5 | 25 | 16 | 5 | 1.4 | 4.3 | 11 | 0.609375 | 68.06172113 | 113.8638473 |
| 6 | 10 | 25.4 | 5 | 1.4 | 4.3 | 10 | 0.9015748 | 70.2199774 | 118.2795739 |
| 7 | 10 | 25.4 | 5 | 1.4 | 4.3 | 9 | 0.9015748 | 70.2199774 | 116.4625865 |
| 8 | 10 | 25.4 | 5 | 1.4 | 4.3 | 8 | 0.9015748 | 70.2199774 | 114.4966195 |
| 9 | 10 | 25.4 | 5 | 1.4 | 4.3 | 7 | 0.9015748 | 70.2199774 | 112.3694578 |
| 10 | 10 | 25.4 | 5 | 1.4 | 4.3 | 6 | 0.9015748 | 70.2199774 | 110.0678846 |

(b) Asymmetric stripline impedance calculation

Figure 4.11: Striplines impedance calculation chart

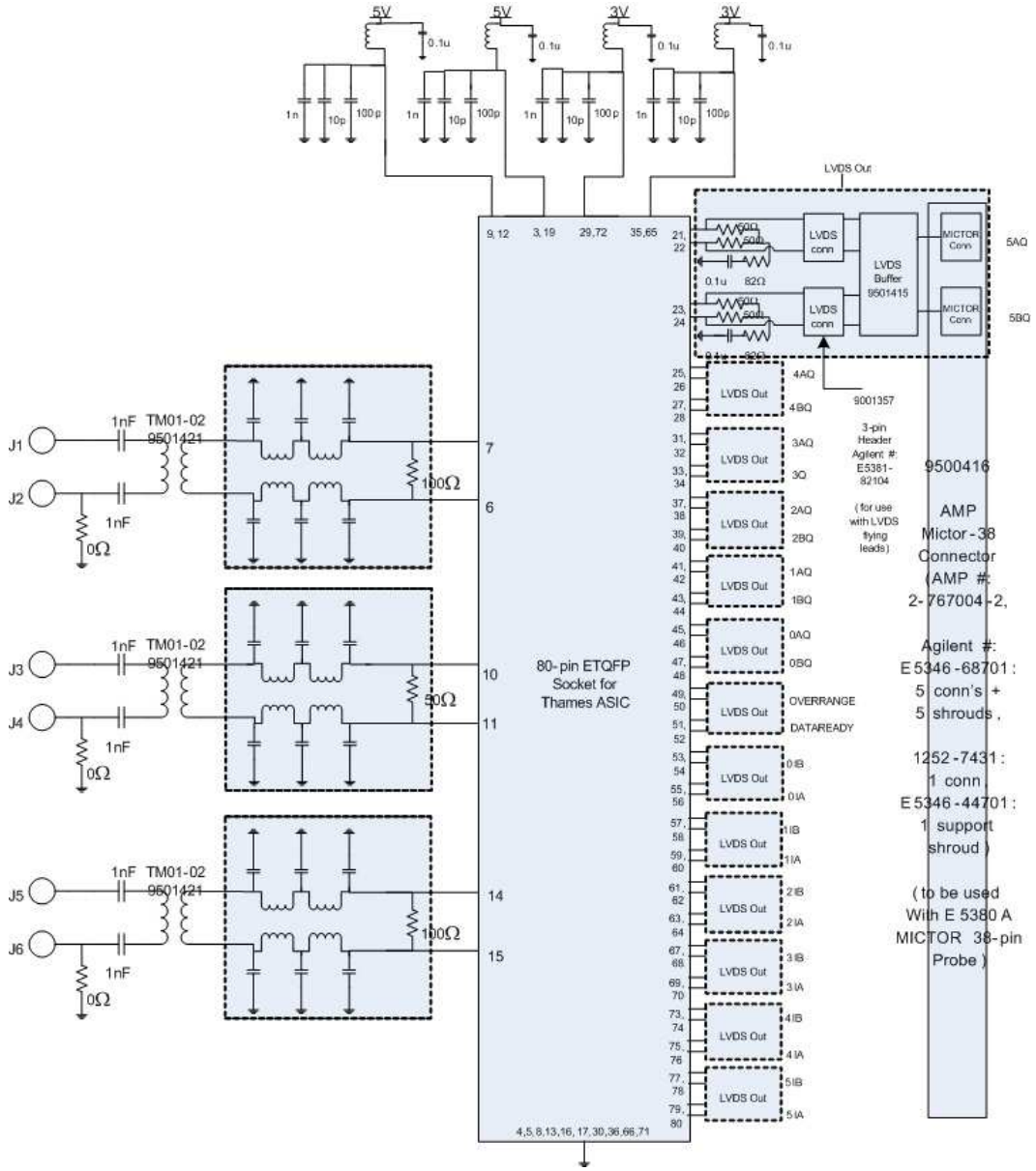



Figure 4.12: High speed dual channel 6-bit ADC test fixture DIB total schematic design

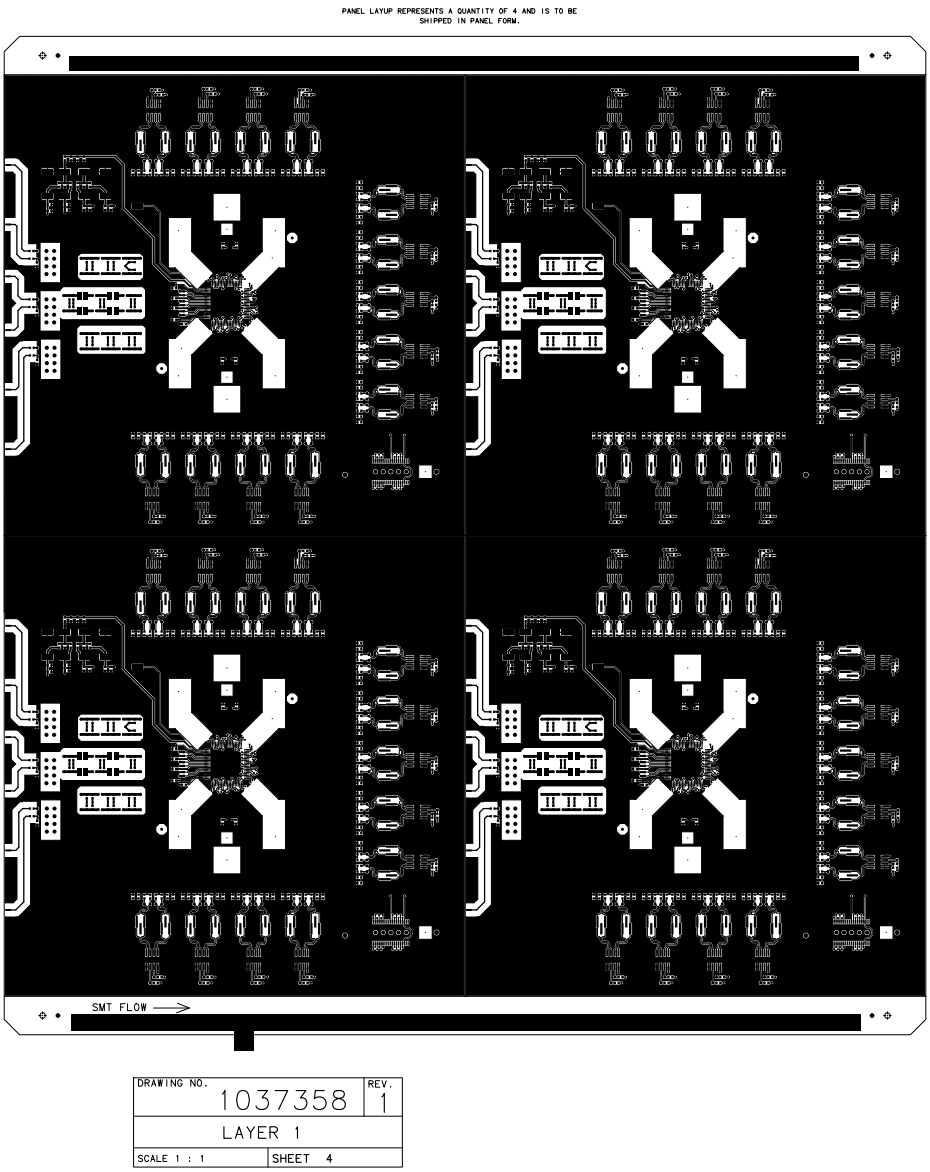



Figure 4.13: High speed dual channel 6-bit ADC test fixture DIB Layer 1: artwork for ADC testing fixture component pads and socket foot-prints

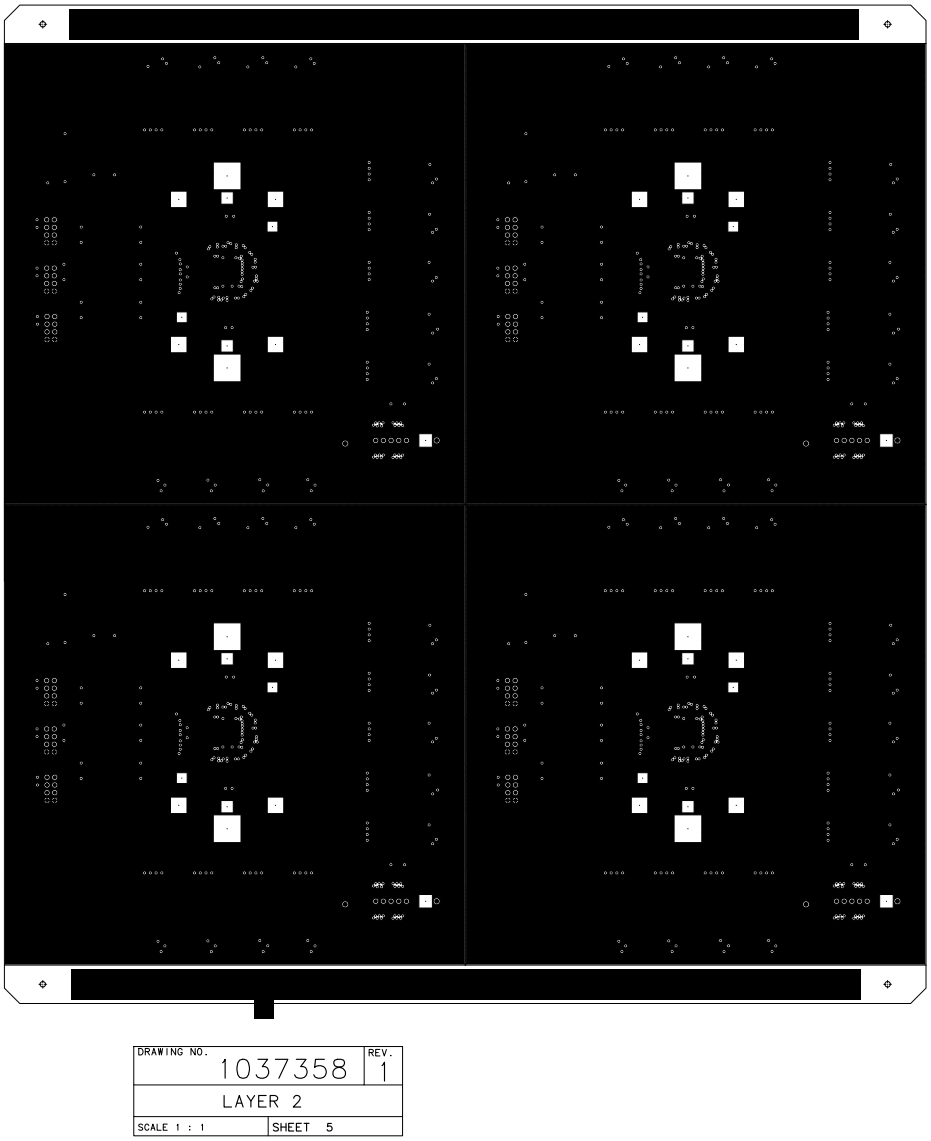



Figure 4.14: High speed dual channel 6-bit ADC test fixture DIB Layer 2: artwork for ground plane - wide ground planes are also used for a good heat-sinking purpose.

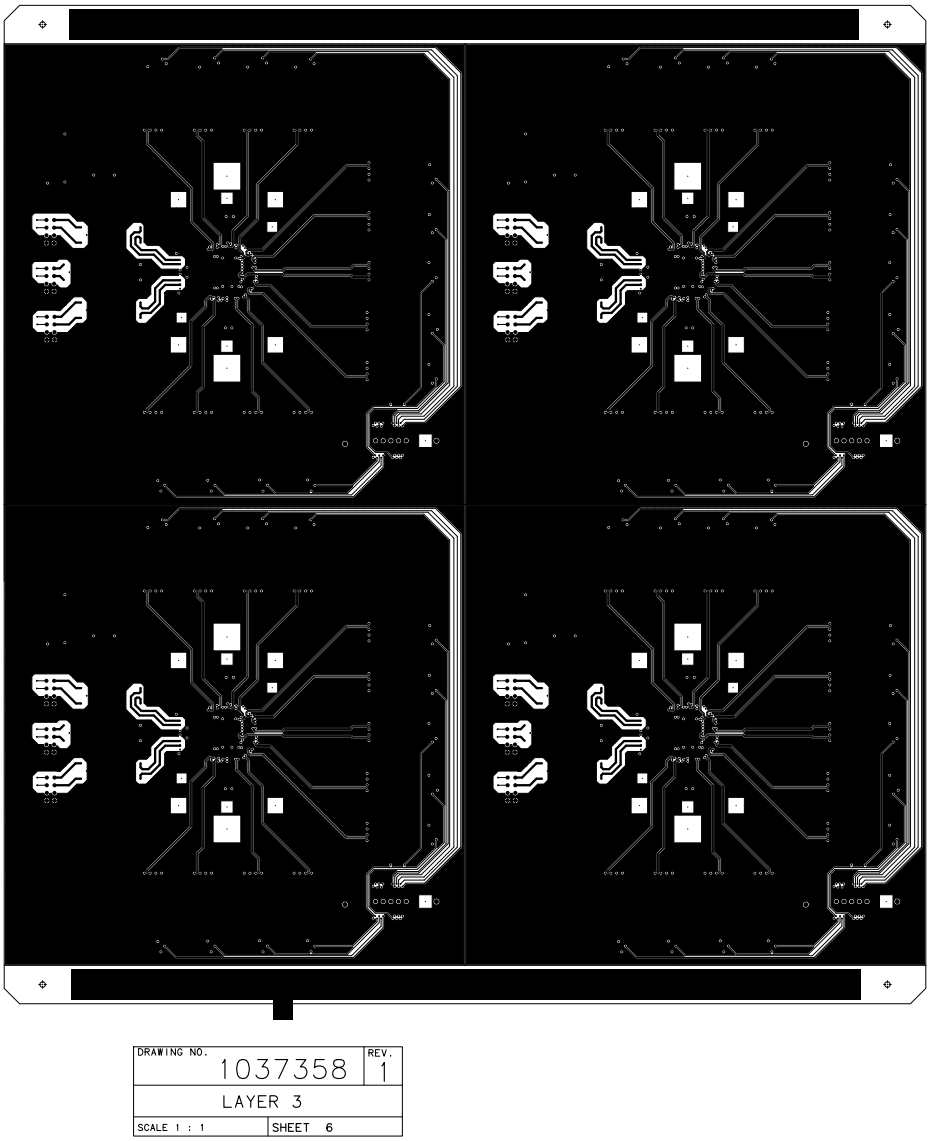



Figure 4.15: High speed dual channel 6-bit ADC test fixture DIB Layer 3: signal traces

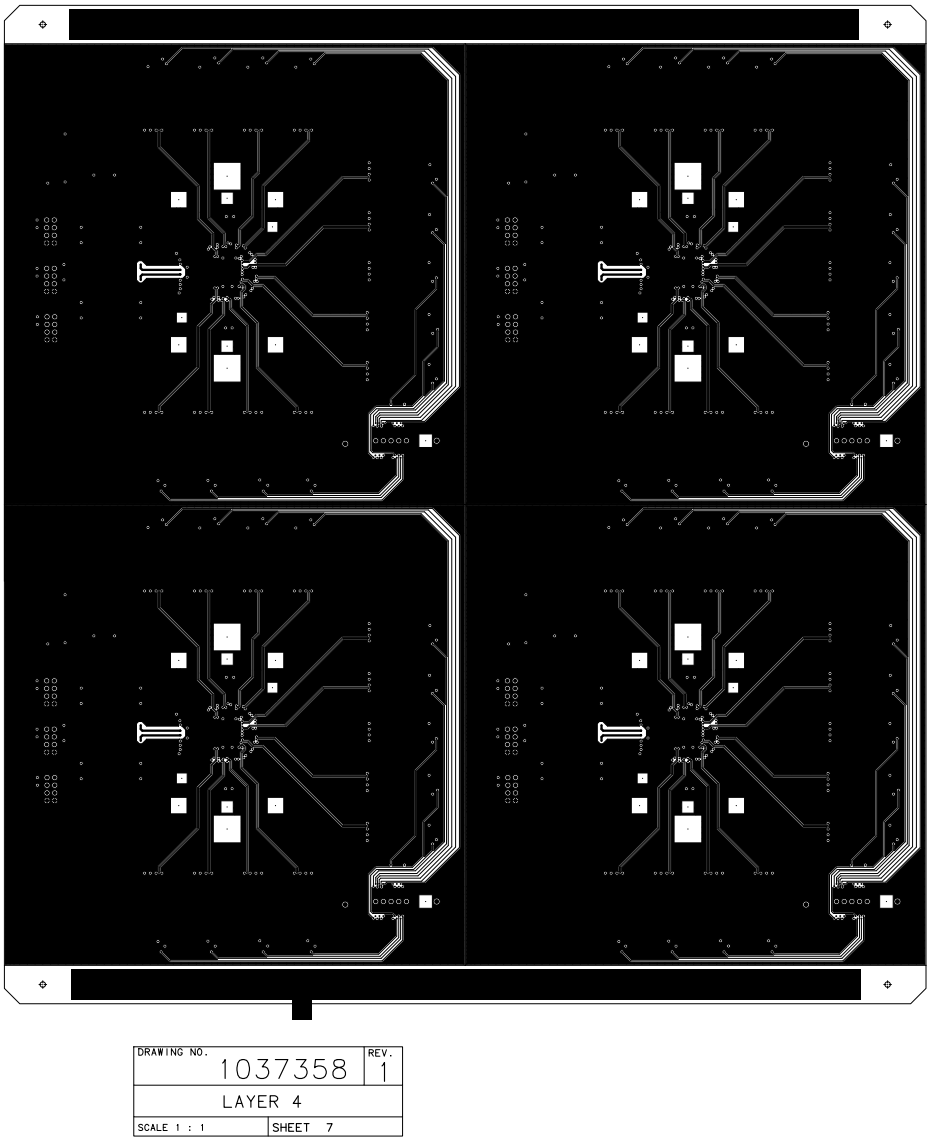



Figure 4.16: High speed dual channel 6-bit ADC test fixture DIB Layer 4: signal traces

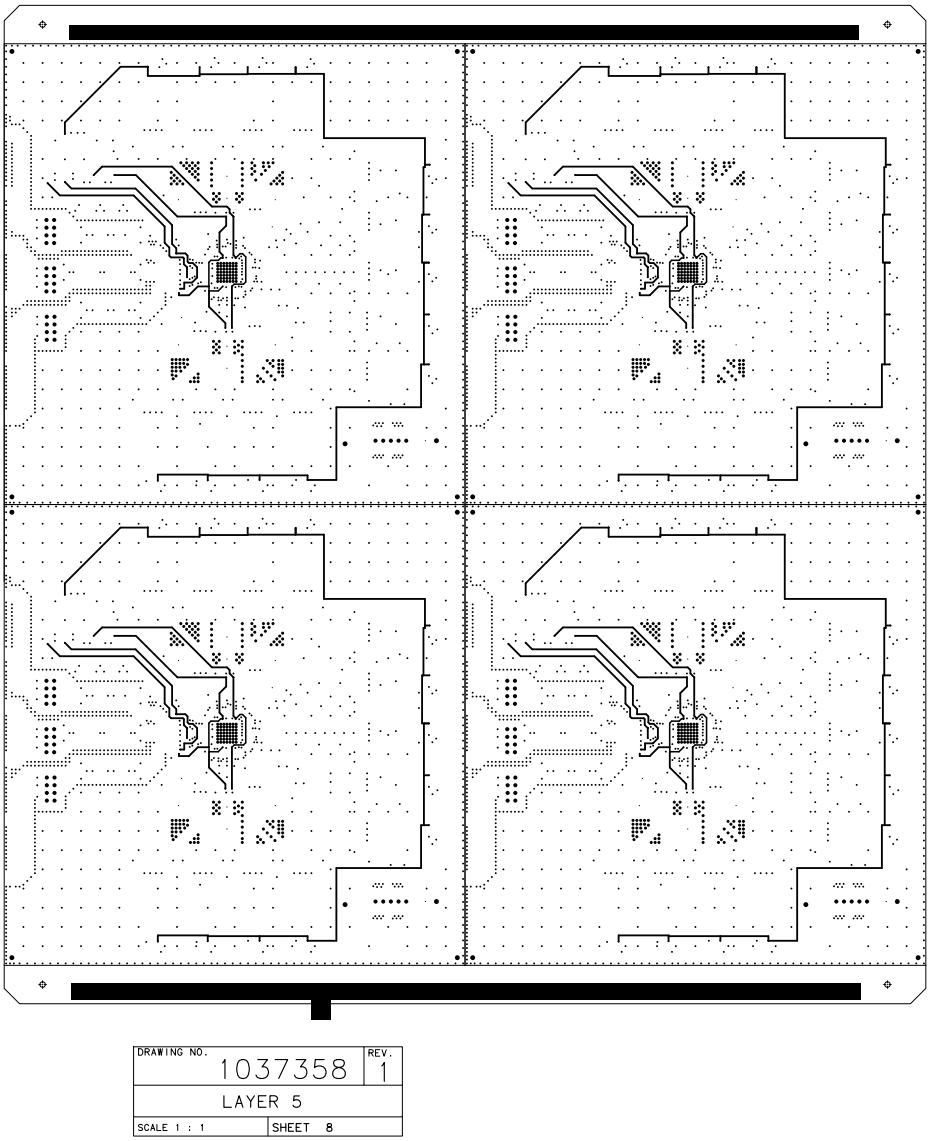



Figure 4.17: High speed dual channel 6-bit ADC test fixture DIB Layer 5: power plane (3V and 5V))

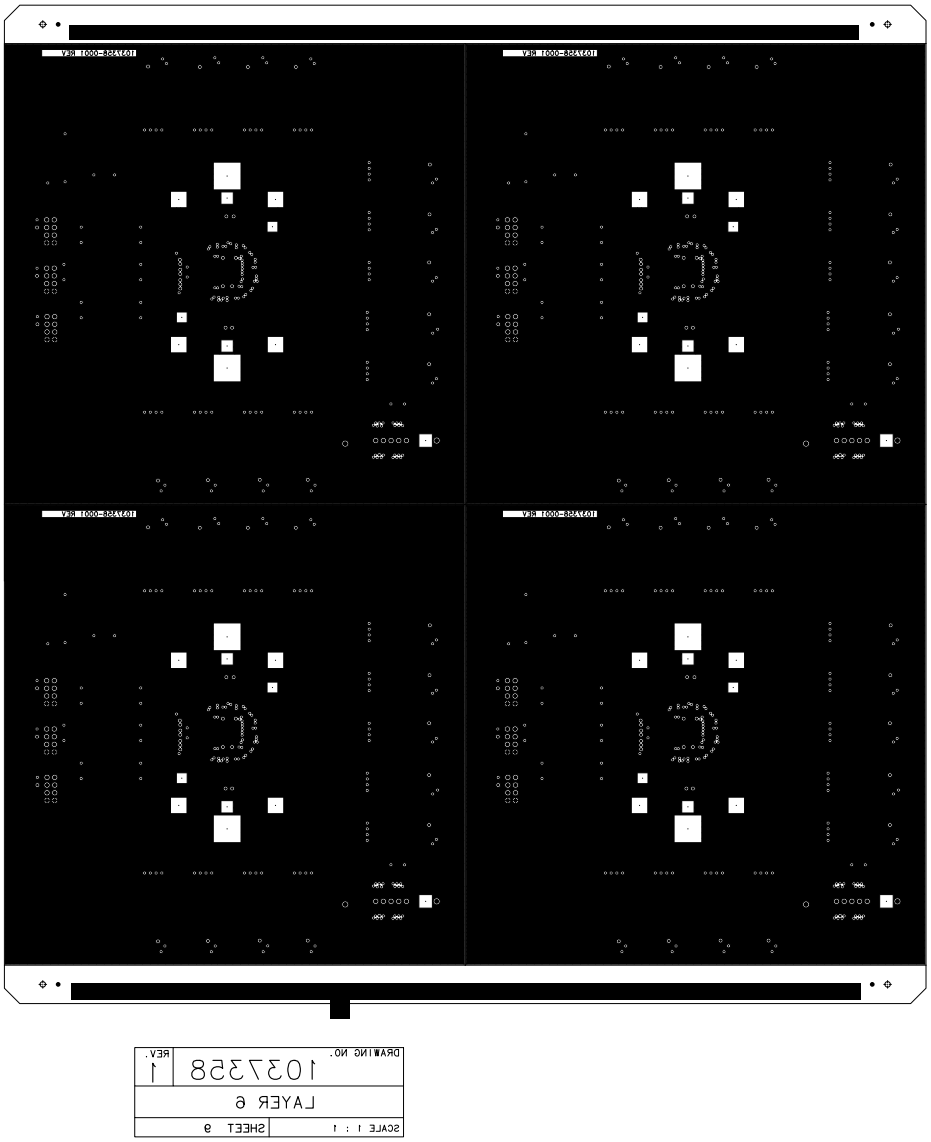



Figure 4.18: High speed dual channel 6-bit ADC test fixture DIB Layer 6

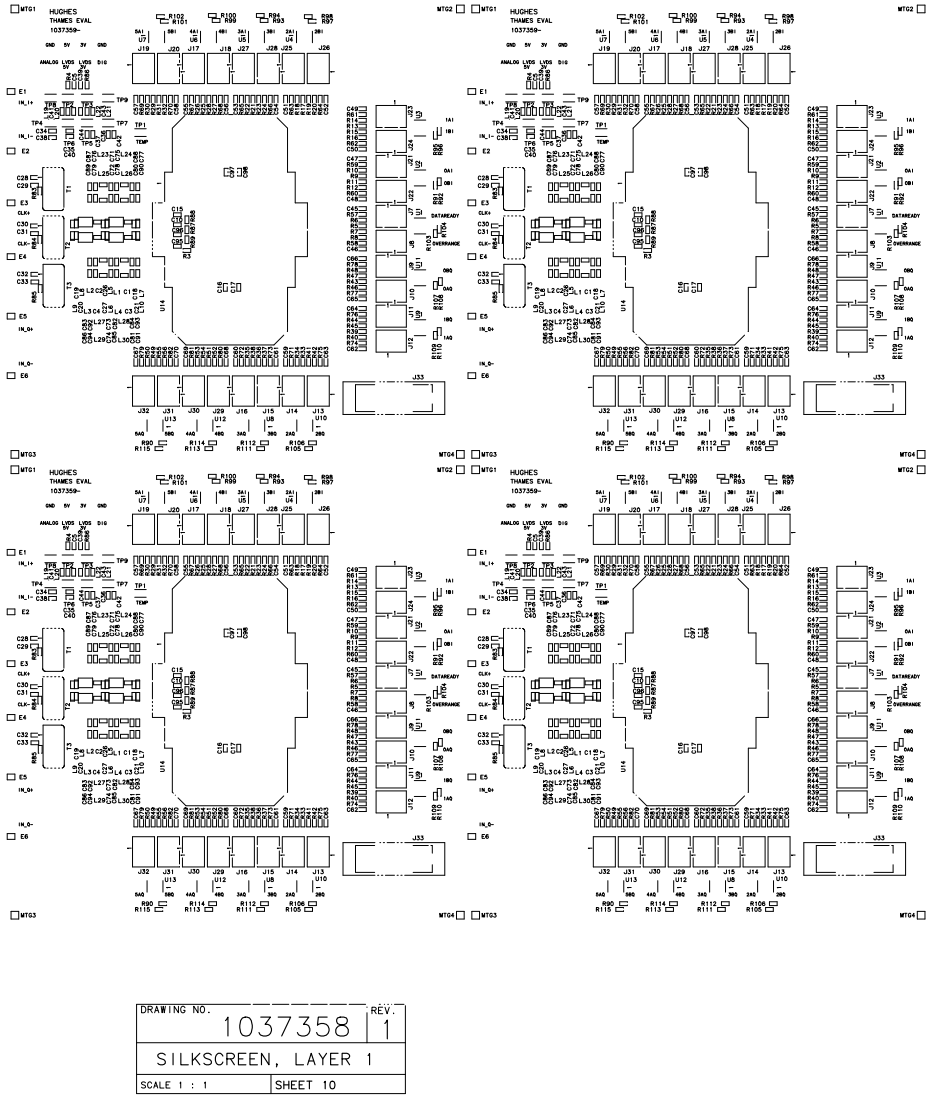



Figure 4.19: High speed dual channel 6-bit ADC test fixture DIB Layer 1 silkscreen:

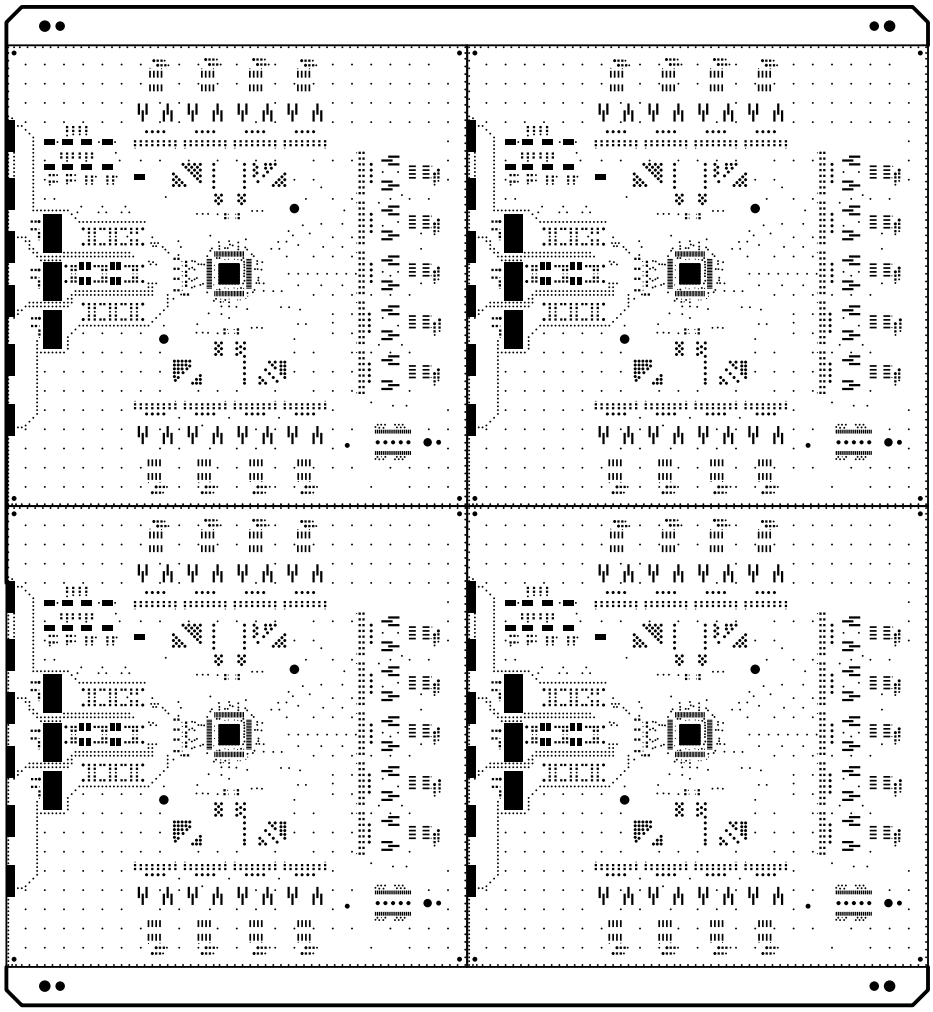



Figure 4.20: High speed dual channel 6-bit ADC test fixture DIB Layer 1 soldermask

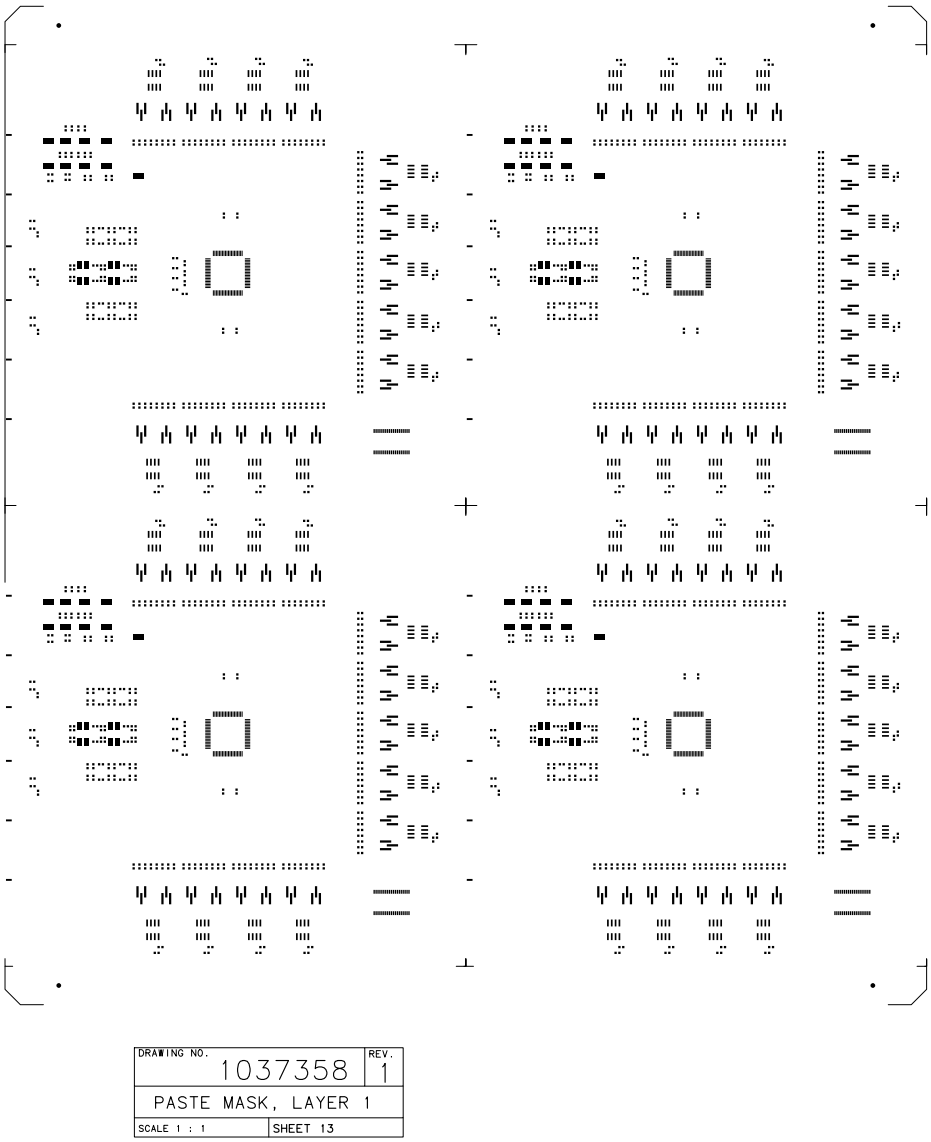



Figure 4.21: High speed dual channel 6-bit ADC test fixture DIB Layer 1 pastemask

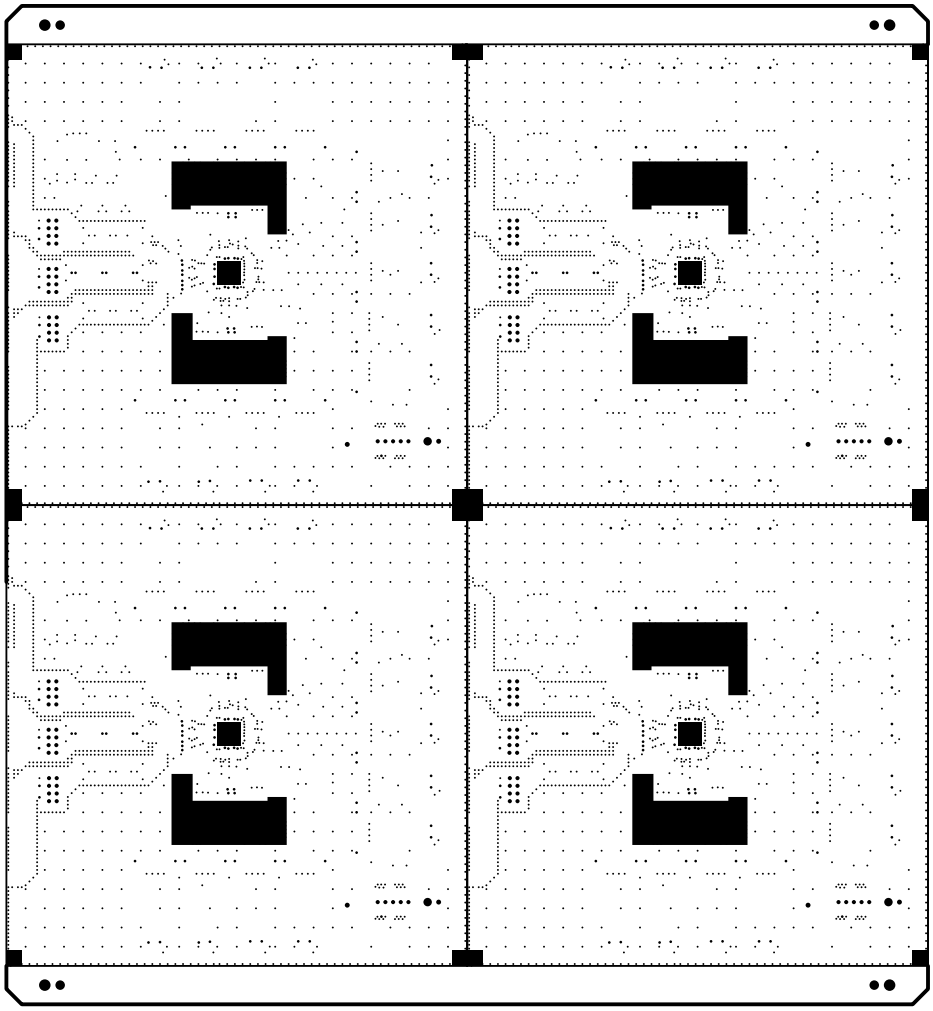



Figure 4.22: High speed dual channel 6-bit ADC test fixture DIB Layer 6 soldermask

## 4.3 Test setup and equipment suite

Design-for-testability (DfT) is the hallmark of good ADC design. This approach is described fully in this section. The example ADC used in this study has de-multiplexed logic outputs (6:12) running at a 400 MHz data rate. The high speed sampling clock (800 MHz) can be driven directly from a continuous signal synthesizer to ADC clock buffered input. Otherwise, tests and measurements for the ADC require a state-of-art high speed logic analyzer with deep digital memory to capture digital logic outputs, and a high frequency pattern generator as a clock source.

Figure 4.23 shows the test bench setup block diagram which is used for the entire DVT process. Separated DC power supplies are used for each of the analog (+5.0 $V_{cc}$) and the digital (+3.0 $V_{cc\_dig}$) supply nodes and for each of the 5.0 V and 3.0 V LVDS drivers. The clock is synthesized with an HP/Agilent 83712A (10 MHz to 20 GHz continuous waveform generator with 1 Hz frequency resolution). The single-driven clock signal for the generator is converted to a differential signal with a commercial RF transformer (Mini-Circuits®), with a 3dB bandwidth from 1 MHz to 800 MHz. The clock signal is filtered with a $5^{th}$-order bandpass filter embedded on the fixture DIB, before being applied to the ADC clock input to suppress the high frequency harmonics which may distort the input clock signal from the generator. The schematics are shown in Figure 4.7.

An HP/Agilent ESG-2000A (250 kHz to 2 GHz continuous waveform generator with 0.01 Hz frequency resolution) is used for the analog input source and is driven

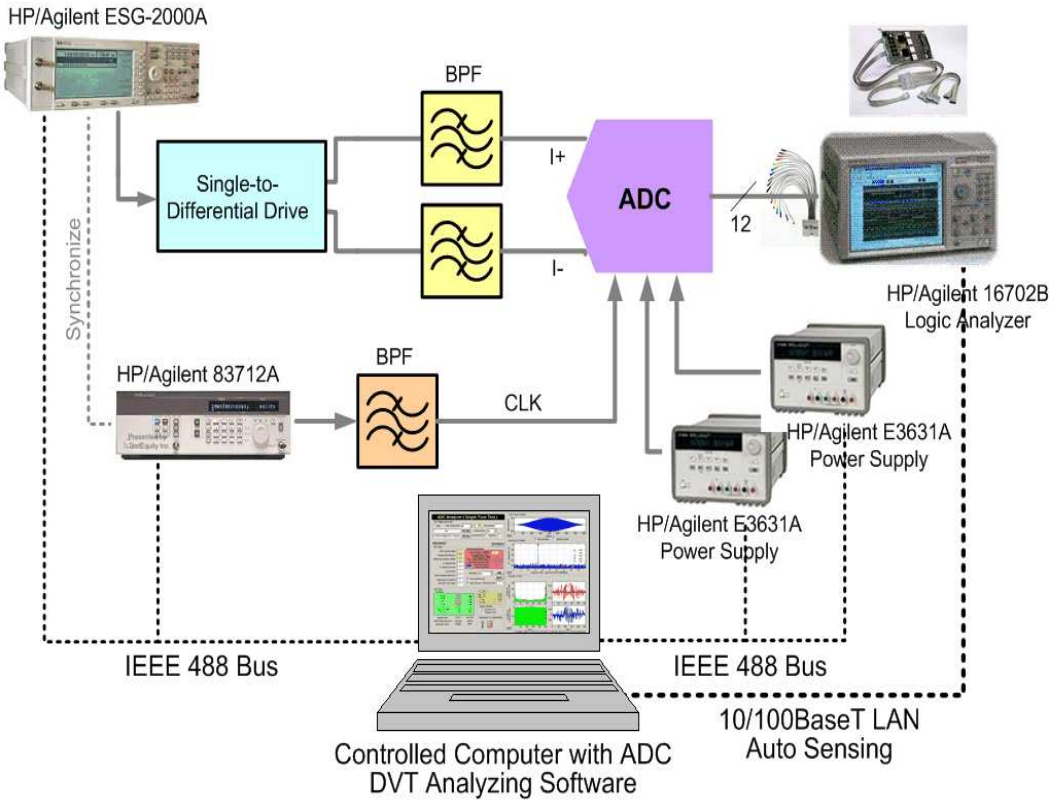



Figure 4.23: Single channel differential ADC dynamic testing configuration

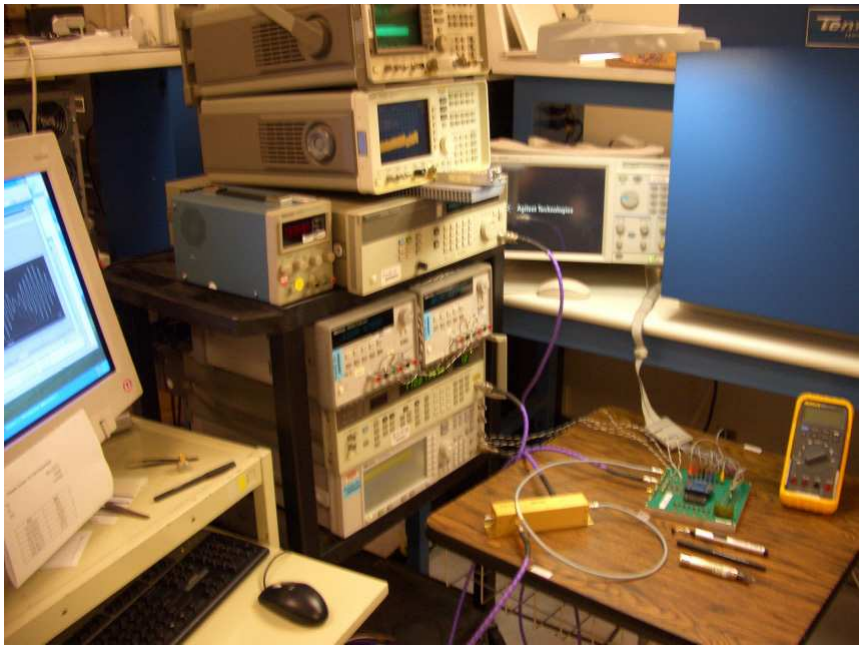


Figure 4.24: *Thames* ASIC test bench setup photograph

differentially using an RF transformer embedded in the fixture board similarly to the clock input. The single-ended-to-differential analog inputs are also filtered to suppress harmonic distortions of the generator. The clock generator has an optional precision timing reference output at 10 MHz, and the timing reference must be synchronized (or phase-locked) with the input analog signal generator.

To examine ADC two-tone intermodulation distortion (IMD), minor configuration changes are necessary. Two separate, continuous signal generators are required, and the generator outputs can be combined using an RF power combiner or a hybrid junction coupler operating over a 2 MHz - 2 GHz range and 0° - 180° phase shift capability over the 10 octave bandwidth. Finally, the combined signals can be

applied to the ADC analog inputs to test and measure the two-tone IMD. The input signal source is chosen for its high stability, high signal purity and low harmonic distortion. This is necessary, as the signal source SSB phase noise is -120 and -116 dBc at 500 MHz and 1 GHz respectively. The harmonics are less than -30 dBc, and the non-harmonic spurious signals are less than -65 dBc. This is a critical concern for assuring adequate ADC dynamic performance. This will be discussed in more detail below.

The digital logic output data are captured by an HP/Agilent 16702B logic analyzer system main-frame with a 16760A timing and state module. In an actual test, the digital outputs acquire 8092 sampled data points using the ADC 400 MHz 'data_ready' output as the logic analyzer state clock rate (capable of operation up to 800 Mb/s). Each of the 6:12 demultiplexed data outputs (A and B) are, therefore, acquired. There are 16384 sampled data points in total for the 6-bit ADC. The acquired samples (2 sets of 8092 samples) are transferred to the host PC completing the sampling data set with a 16384 record size and analyzed for specific ADC performance parameters via the 10/100BaseT LAN connection.

## 4.4 Summary

Chapter 4 provides detailed high-speed ADC test fixture designs including contactor socket and subsystem peripheries. A DIB is one of the most critical elements in a successful ADC test solution. Without good DIB performance, the ADC may be

unable to meet its specifications, regardless of the quality of the test program or test code. Many factors must be considered to be lead to good high-speed ADC testing DIB design. It includes elaborate designs for PCB traces and DIB subsystem peripheries.

A good DIB layout must be accompanied by a good schematic design as well. The only way to produce a good DIB schematic is to have a complete test plan and device specification to begin with. However, if the DIB design is for a proto-type ADC design verification, then the DIB design must be also initiated from the ADC proto-type design phase to minimize possible incompatibility between ADC and its DIB. Therefore, concurrent engineering is critical to successful ADC product development.

Chapter 5

# ADC Design Verification Software and Test Methodologies

## 5.1 Overview

A design verification software tool is a test program and a computer program that tells the test system how to configure its hardware to make the needed measurements. This program is developed under a graphical interface for easy of use and going to be extended to a full production testing. Once the test plan and test flow are established to characterize or to verify the high-speed ADC design, the test program must be developed to fulfill many requirements. Within this program, instructions to the hardware and information such as how to determine if the ADC has passed or failed the test can be provided. The program can be extended to the

automated test equipment (ATE) which is designed as complete stand-alone unit for optimal production testing of the designed ADCs. This is the primary advantage of ATE and beneficial to the full productions [49].

This chapter provides the engineering foundations necessary to assemble ATE systems suitable for validating mixed-signal systems such as the *Thames* chip. The primary aim is to develop a methodology for device verification testing (DVT) of high speed ADCs used in high quality RF receivers produced in significant volume. Precision at low cost is the test goal. Testing and measurement techniques are described for two chips: a linear dual channel 6-bit ADC (the HNS *Thames* chip) and a novel 4-bit compressing flash ADC. Full scale testing of the *Thames* chip is described and static and sine-wave dynamic test results are provided for the compressing ADC chip.

## 5.2 ADC DVT and characterization

While characterizing the data converters, various parameters must be measured. These parameters fall into two categories: (1) performance parameters and (2) intrinsic parameters [15]. First, data conversion characteristic values such as gain, signal-to-noise ratio, signal to total harmonic distortion, and more are included to performance parameters. Note that performance parameters are set by the quality of all the sub-circuits in the integrated data converter. Second, intrinsic parameters define errors of data conversion such as quantization error, integral nonlinearity, dif-

ferential nonlinearity, and etc. These parameters are intrinsic to the data converter circuit itself and generally do not depend on the nature of the test stimulus. On the contrary, the performance parameters are dependent on the nature of the test stimuli, such as transmitted signals. Both intrinsic and performance parameters are discussed in more detail below.

Data conversion system testing consists of two parts: "static" testing and "dynamic" testing. ADC testing starts from DC measurements such DC gain, DC offset, Integrate nonlinearity (INL), differential nonlinearity (DNL), and worst-case absolute voltage errors in decision levels, relative to the ideal decision levels. Basically, the DC testing or the static test is focused on verifying the transfer function of the designed ADCs, so that test result shows if the ADC circuits are designed correctly and working properly. In dynamic testing, we verify ADC operations in term of sampling time-varying analog signals, digitizing them, and reconstructing the analog signal. Dynamic test of ADCs clearly differs from the static testing (e.g., DC gain test and offset test, INL and DNL measurements, finding missing codes and etc.) Dynamic tests follow timing specification: maximum sampling frequency, maximum conversion time, minimum recovery time, aperture jittering, and etc.

The most popular static testing method for an ADC is a ramp-based method [28]. The primary purpose of static testing is to determine the transition levels of the ADC output code. In digital receiver applications, the critical ADC parameters, (spurious free dynamic range (SFDR), signal-to-noise-and-distortion ratio (SINAD)

and the intermodulation distortion (IMD) product), are obtained under dynamic drive conditions. ADC linearity is also important and characterized under dynamic drive conditions as discussed below. A primary aim of this chapter is to develop device verification tests (DVTs) for high speed ADCs used in high quality RF receivers produced in significant volume. Precision at low cost is the test goal. Testing and measurement techniques will be described with linear dual channel 6-bit ADC characteristics and a novel 4-bit compressing flash ADC characterization follows with the static test result.

### 5.2.1 Linear ADC

The "generic" flash type ADC is shown in Figure 5.1. The operations of flash ADCs and various sub circuit designs have been researched extensively [14, 15, 16, 17, 50, 51, 52]. A flash converter use a brute force to compares the input signal against all possible decision levels simultaneously. N-bit ADC in Figure 5.1 need $2^N - 1$ comparators and the divided reference voltages at each node in the resistive ladder are compared with the input signal voltage. The comparators produce the digital input signal for the decoded logic. Digital decode logic determines which of the comparators producing a logic one has the highest threshold voltage. Finally, the N-bit conversion result is followed by the digital decoder. Therefore, the all conversion codes must be verified when the flash ADC is under testing, so that any defect can be found and debugged from any resister or comparator.

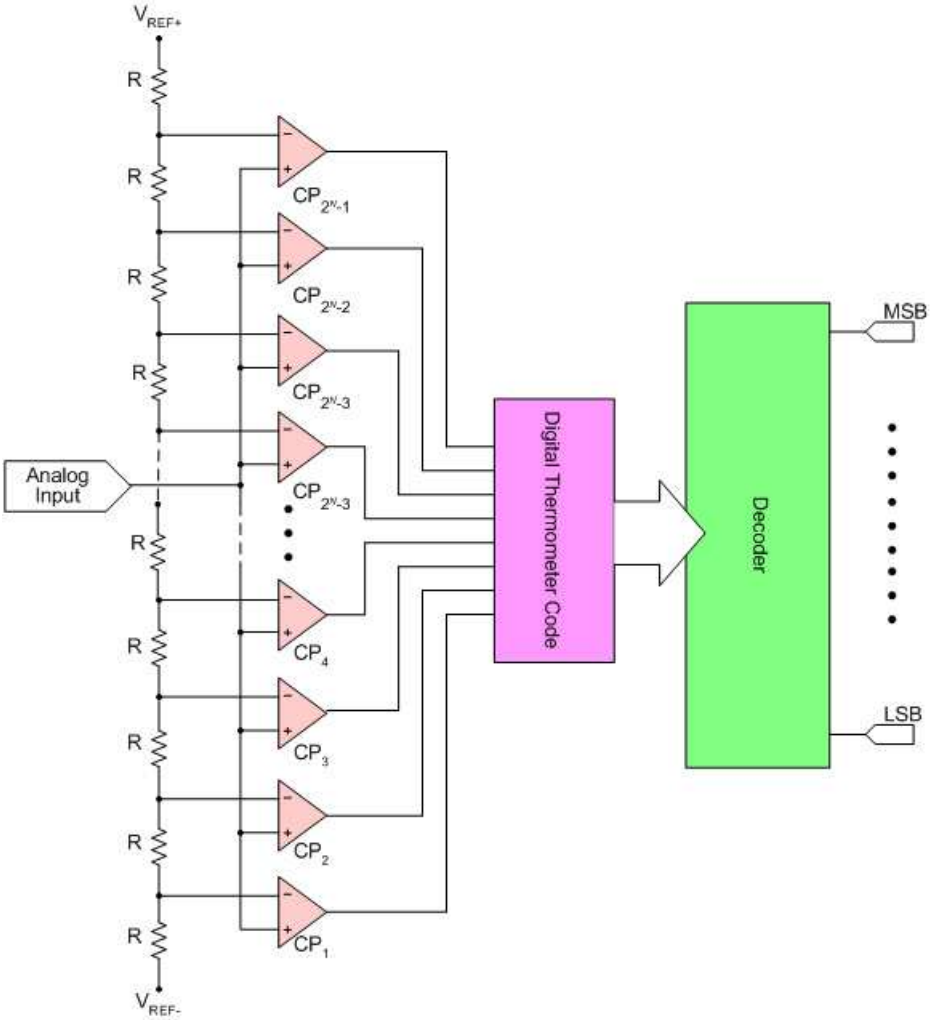



Figure 5.1: Flash ADC basic architecture

Ideally, sample-and-hold amplifier (S/H) or track-and-hold amplifier (T/H) is not necessary for the flash type ADC because constant holding input signal is not required. However, each comparator is required for each decision level so that the more precise decision code can be produced by including S/H amplifier in the front end of the flash ADC architecture. When resolution increases, the flash ADC becomes prohibitively expensive. High speed and precision and relatively high resolution ADC can be designed with flash type architecture if the foundry can provide better manufacturing control and component matching for the comparators and resistors [16].

As mentioned before, this thesis does not cover ADC design, but focuses on characterizing ADCs. Writing a test plan is the first step in characterizing a linear ADC. Each test ascertains a key characterizing parameter, and a detailed methodology must be added to the plan. As stated above, the plan must include the purpose: characterizing of both intrinsic parameters and performance parameters.

Basic functionality can be verified by transfer function testing. The ADC transfer function contains many characteristics from ADC's intrinsic parameters. As mentioned earlier, these parameters are intrinsic to the ADC circuit itself rather than the nature of the test stimulus.

An ideal 3-bit linear ADC transfer function is shown in Figure 5.2. The actual transfer function can be obtained by static ramp testing using the test setup is illustrated in Figure 5.3. There is also another method to obtain the transfer func-

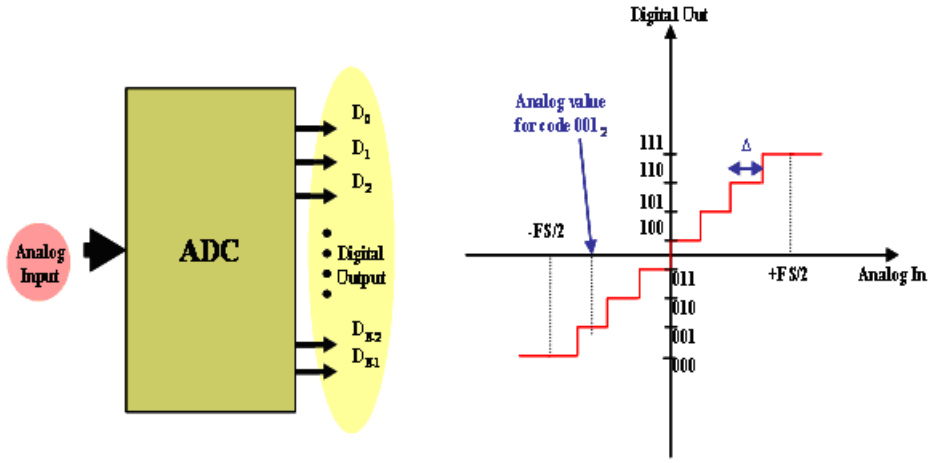



Figure 5.2: General ADC and 3-bit ADC transfer function

tion: servo (loop) testing [14, 15, 16, 50, 51, 52]. The servo test setup is depicted in Figure 5.4. The static transfer curve is obtained by inputting the ramp signal to the ADC. In practice, the actual transfer curve which is obtained from the bench can not be ideal. Thus, there are some differences between ideal and actual transfer functions, which are gain error and gain offset. Figure 5.5 shows the gain errors of ADC.

The ideal $N$-bit ADC has digital word bits proceeded an output code, $Y_d$, which is

$$Y_d = (D_{N-1}, D_{N-2}, \cdots, D_2, D_1, D_0). \tag{5.1}$$

The digital bit $D_{N-1}$ is the most significant bit(MSB), and D0 is the least significant bit(LSB) and all the bits are 0 or 1. The analog input value of the ADC is defined to $X_a$. A staircase static transfer function for 3-bit ADC is depicted in the

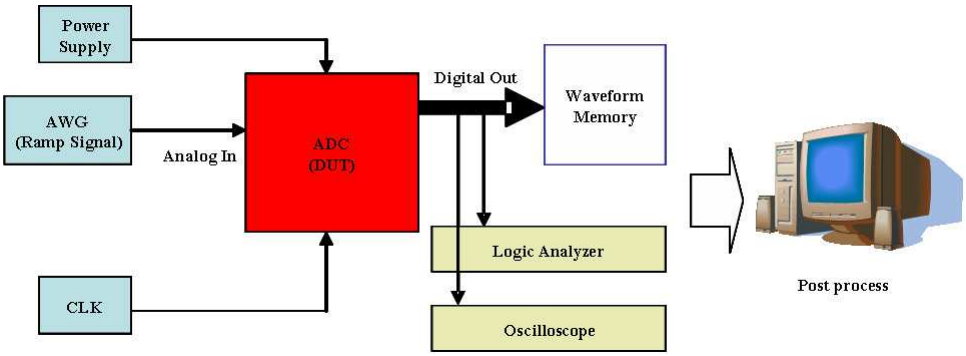



Figure 5.3: ADC static ramp testing

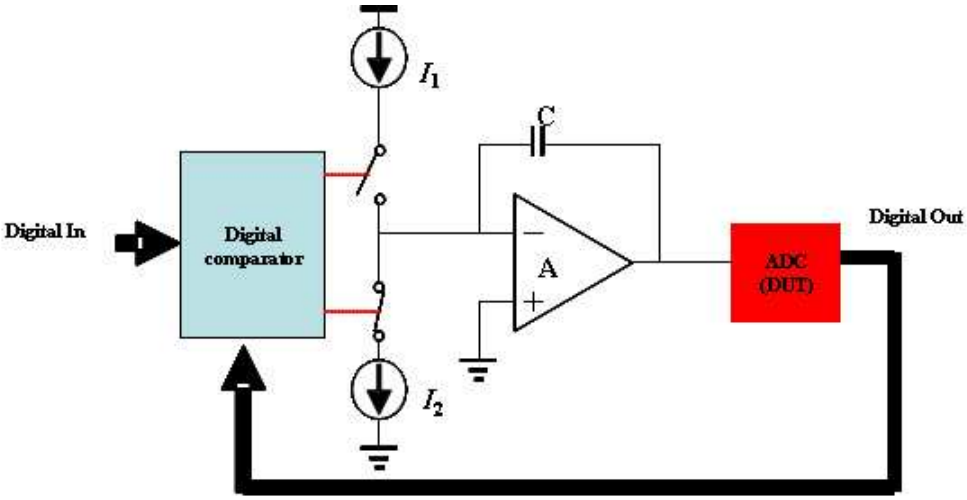



Figure 5.4: ADC static test - servo loop testing

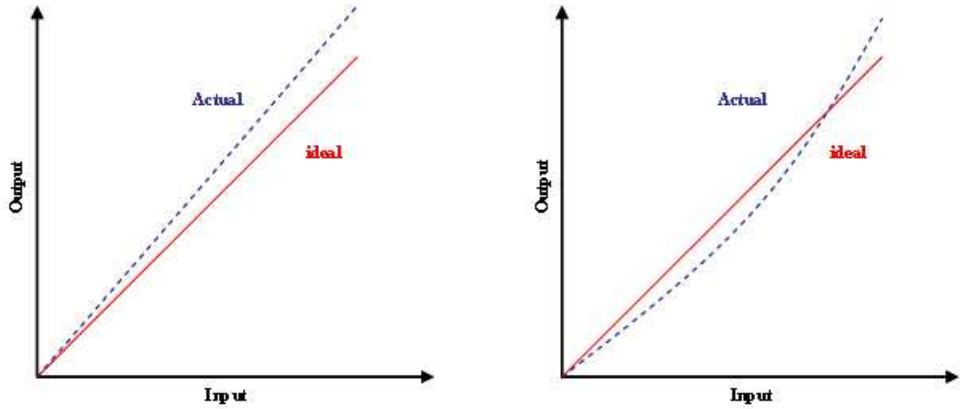



Figure 5.5: Gain errors of ADC

Figure 5.2. It is noticeable that the input signal should never be in the saturated range since this gives rise to large conversion errors. From the staircase curve, the step size, $\Delta$, is equal to the analog value of the LSB and the full scale range ($FS$) of the converter is defined as the conversion range up to saturation. The step size can be express as

$$\Delta = \frac{FS}{2^N}. \tag{5.2}$$

where $N$ is the resolution of ADC.

The analog signal range maybe bipolar (-$FS/2$ to $+FS/2$), or unipolar (0 to $+FS$). Due to non-ideal circuit elements in the actual implementation of a data converter, the code transition points in the transfer function will be moved as illustrated in Figure 5.6. It is important to find the analog transition levels where the output signal changes between two digital output codes. It is noticeable that the static ramp test requires precision ramp generators to precise code transition

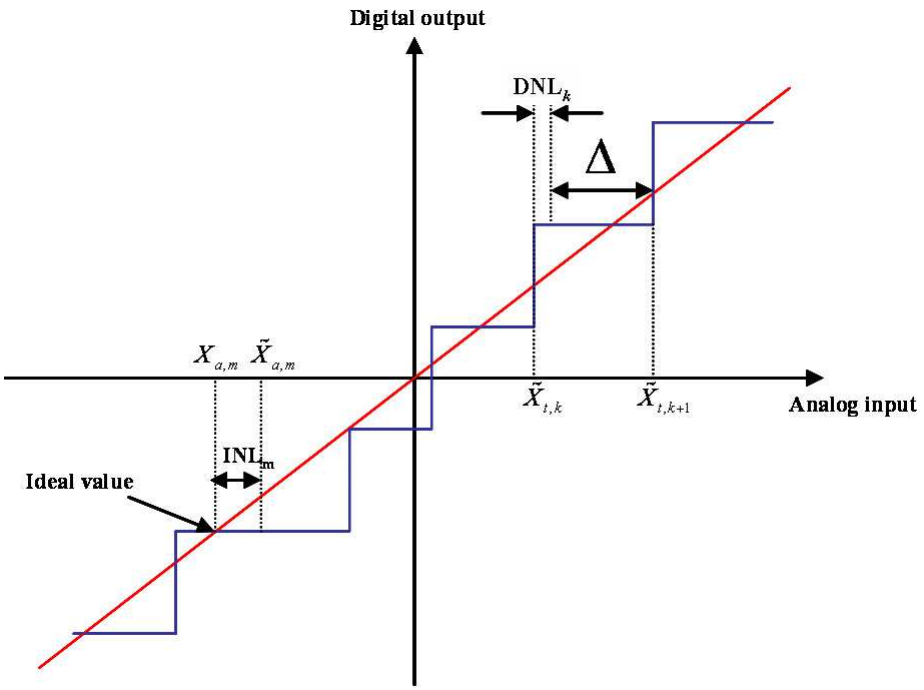



Figure 5.6: ADC transfer function and non-linearity

characterization. A ramp signal is usually a built-in function of an arbitrary waveform generator(AWG). Therefore, the test setup is simple to set up, as in Figure 5.3. Given an AWG set up to provide the required ramp at a low slew rate, the transition point for each digital output can be measured precisely.

The digital waveforms from the each bit out can be either recorded in the memory or obtained by other data acquiring systems. A logic analyzer can be used to synchronize all the output bits. When a logic analyzer is not available, an oscilloscope can be used. The oscilloscope, however, may require multi-channel functions and careful synchronization for precision characterization. As contrasted

with the static ramp test, the servo test does not require the precision ramp signal generator for input. For example, the ADCs compromising the integrator may have substantial nonlinearity without any adverse effect on the measurement accuracy. This is because the digital comparator introduces a virtually infinite gain in the feedback loop, suppressing the integrator nonlinearity.

The differential nonlinearity(DNL) error can be defined as the difference between the ideal step size and that of the non-ideal ADC [15]. In the Figure 5.6, normalized DNL of the ADC can be expressed as

$$DNL_k = \frac{\widetilde{X}_{t,k+1} - \widetilde{X}_{t,k} - \Delta}{\Delta}, \tag{5.3}$$

where $\widetilde{X}_{t,k}$ corresponds to the actual analog input value for digital output code $Y_{d,k}$ as illustrated in Figure 5.7 and means the actual measured value which tells the code edge. The subscript, $k$, is the index for the digital codes and can be calculated as

$$k = \sum_{l=0}^{N-1} D_l \cdot 2^l. \tag{5.4}$$

Therefore, the $k$-th digital code is denoted $Y_{d,k}$, while the corresponding ideal analog value is denoted $X_{a,k}$. This is illustrated in the Figure 5.7 . The total deviation of an analog input value from the ideal value is called integral nonlinearity (INL) and shown in Figure 5.6 as well. The normalized value for INL can be defined as [15]:

$$INL_k = \frac{\widetilde{X}_{a,k} - X_{a,k}}{\Delta} \tag{5.5}$$

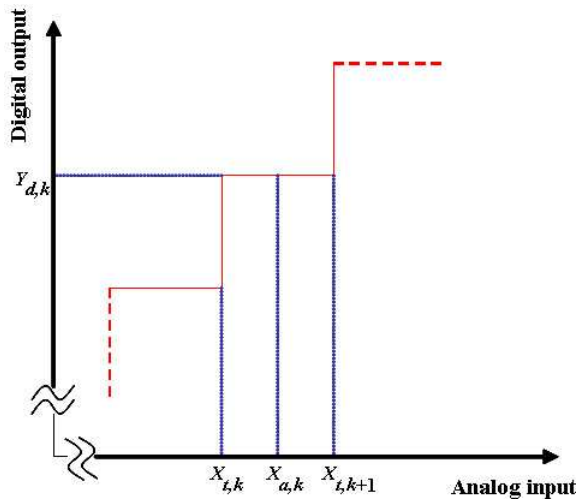



Figure 5.7: Non-ideal ADC transfer function with INL and DNL errors

and both INL and DNL can be related by

$$INL_k = \sum_{l=1}^{k} DNL_l. \tag{5.6}$$

The offset, $X_{offset}$ can be found with the least square method. To find the offset, the minimum $X_{offset}$ must be calculated at the point where the derivative of $X_{offset}$ is zero:

$$\frac{\partial}{\partial X_{offset}} \sum_{k=0}^{2^N-1} (\widetilde{X}_{a,k} - X_{a,k} - X_{offset})^2 = 0 \tag{5.7}$$

Therefore, $X_{offset}$ can be calculated as:

$$X_{offset} = \frac{1}{2^N} \cdot \sum_{k=0}^{2^N-1} \widetilde{X}_{a,k} - X_{a,k} \tag{5.8}$$

The offset corresponds to the average of all the errors in the ADC. To eliminate the offset from the INL calculations, the offset should be subtracted from all the analog values of $\widetilde{X}_{a,k}$

As compared to the ideal transfer curve, which should be a straight line, the actual output of ADCs exhibit a linear/nonlinear gain error illustrated in Figure 5.5. Note that the linear gain error does not cause any distortion of the quantized input signal as long as the output signal is not clipped. The actual output with a linear gain error and offset error can be written as

$$\widetilde{X}_a = G_E \cdot X_a + X_{offset} \tag{5.9}$$

where $G_E$ is the gain error. The actual output for a non-linear gain can be expressed as following

$$\widetilde{X}_a = G_{E1} \cdot X_a + G_{E2} \cdot {X_a}^2 + G_{E3} \cdot {X_a}^3 + \cdots + X_{offset}. \tag{5.10}$$

Non-linear errors can be reduced by using pre-distortion [15, 53]. In Eqn. 5.10, the $2^{nd}$ and higher order terms can be ignored and approximated to the output like in Eqn. 5.9. In practice, if the transfer function test result shows non-linear errors, obtaining accurate gain errors and offsets from Eqn. 5.10 are more complicate, and defining INL and DNL can be more difficult. In this case, using pre-distortion on the static transfer function measurement can reduce non-linear error calculation complexity [54]. The actual gain and offset error can be found by using the least square method setting the derivatives with respect to $X_{offset}$ and $G_E$ to zero [15]:

$$\frac{\partial}{\partial G_E} \sum_{k=0}^{2^N-1} [\widetilde{X}_{a,k} - (G_E \cdot X_{a,k} + X_{offset})]^2 = 0, \tag{5.11}$$

and

$$\frac{\partial}{\partial X_{offset}} \sum_{k=0}^{2^N-1} [\widetilde{X}_{a,k} - (G_E \cdot X_{a,k} + X_{offset})]^2 = 0. \tag{5.12}$$

From Eqn. 5.11 and Eqn. 5.12, the gain and offset can be found as

$$G_E = \frac{\langle \widetilde{X}_a \cdot X_a \rangle - \langle \widetilde{X}_a \rangle \cdot \langle X_a \rangle}{\langle {X_a}^2 \rangle - \langle X_a \rangle^2}, \tag{5.13}$$

and

$$X_{offset} = \langle \widetilde{X}_a \rangle - G_E \cdot \langle X_a \rangle \tag{5.14}$$

where $\langle X \rangle$ indicates a mean values:

$$\langle \widetilde{X}_a \rangle = \frac{1}{2^N} \sum_{k=0}^{2^N-1} \widetilde{X}_{a,k}, \tag{5.15}$$

and

$$\langle X_a \rangle = \frac{1}{2^N} \sum_{k=0}^{2^N-1} X_{a,k}. \tag{5.16}$$

The intrinsic parameters are found, as shown above, by static ramp testing. The errors affect the accuracy of the decision levels of the converter. Deviations from the ideal levels cause DNL and INL errors. Errors in the reference levels shown in Figure 5.6, are normally caused by resistor mismatch (usually in the order of 2 to 0.1 % without laser trimming [15, 16]) and offsets in the comparators. Therefore, the intrinsic parameters are more depend on the ADC circuit itself.

The next step for ADC testing is finding performance or transmission parameters. While static ADC tests can be utilized ramp waveforms to determine the input to the output characteristic, dynamic tests are often performed using sinusoidal inputs. In dynamic testing, errors are extracted as differences between digitally reconstructed sinusoidal signals and an input sinusoidal signal. These dynamic errors typically increase with input sine wave frequency and at high sampling

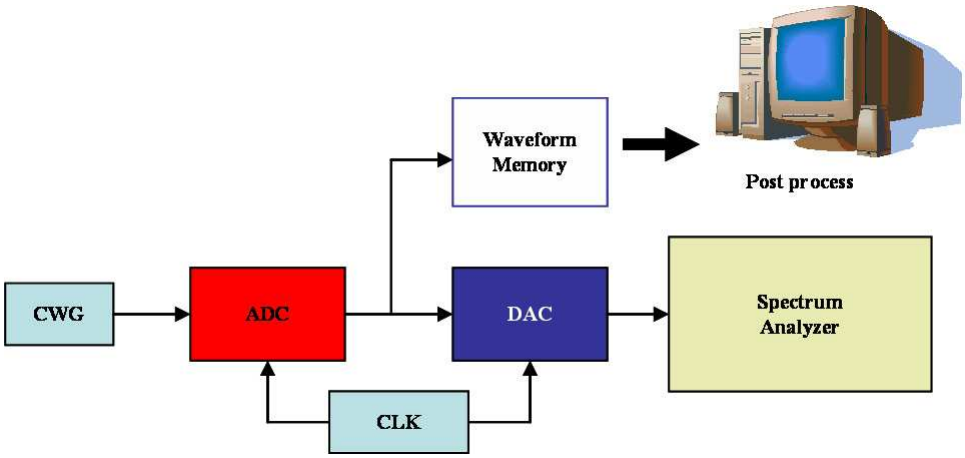



Figure 5.8: Dynamic ADC test setup

rates. Figure 5.8 illustrates the dynamic ADC testing setup. It is important that the ADC under test is followed by a digital-to-analog converter (DAC) that has higher linearity (typically two bits higher resolution) and lower noise than the ADC under test [16]. It is convenient for analog design/test engineers to interpret both input and output analog signals using back-to-back ADC test setups. It is clear that the dynamic errors are mainly caused by timing errors. If the noise and distortion contributed by the DAC are negligible, Signal-to-noise ratio (SNR) and the signal-to-noise and distortion ratio (SINAD) measured by the spectrum analyzer correspond to those of the ADC under test. If such a DAC is not available, a waveform memory can be used. After the post process, the reformed analog signal out of the tested ADC can be analyzed by fast Fourier transform (FFT). The major advantage of the direct ADC-to-DAC test setup is that it allows a quick and easy dynamic testing

and provides real-time feedback regarding the circuit's behavior as test conditions are varied. It does not require digital processing of the data post processing. As intrinsic parameters such as quantization errors (INL and DNL) are defined, performance parameters can be also defined. Performance parameters depend highly on the test stimulus characterizing ADC parameters such as signal-to-noise ratio (SNR), spurious free dynamic range (SFDR), harmonic distortion (HD), total harmonic distortion (THD), effective number of bits (ENOB), dynamic range (DR), effective resolution bandwidth (ERB), inter-modulation distortion (IMD), and etc. For example, in Figure 5.9, a typical FFT spectrum of MAX1448, 80Msps 10-bit ADC from MAXIM IC which is applied for the ultrasound imaging and the baseband/IF frequencies is shown [55, 56]. Figure 5.9 is obtained using a single tone sinusoidal signal input and the input signal appears as the fundamental in the FFT spectrum. The quantization error generates a white noise floor. The nonlinearities in the ADC architecture cause harmonic tones to appear above the noise floor where some of the harmonics may be folded from higher frequencies due to the sampling process.

Based on the FFT output or output from a spectrum analyzer (as depicted in Figure 5.9), ADC performance parameters can be defined with the following parameters:

- Signal-to-Noise Ratio (SNR):

The SNR is a ratio of the signal power to total noise power within a certain frequency

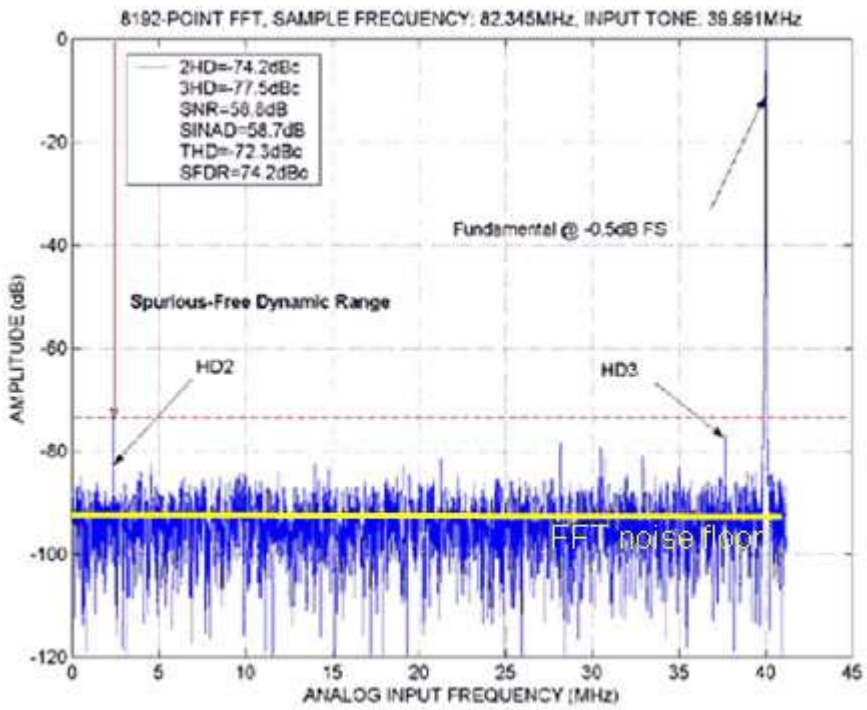



Figure 5.9: MAXIM MAX1148 (80 MS/s 10-bit ADC) FFT spectrum

band, excluding the harmonic components of the signal. It can be expressed as the formula:

$$\text{SNR} = 10 \cdot \log\left(\frac{\text{Signal Power}}{\text{Total Noise Floor}}\right). \tag{5.17}$$

The total noise floor can be measured as shown in the Figure 5.9. When a sinusoidal signal is used to characterize ADCs, the maximum unsaturated amplitude of a sinusoidal input signal is $\Delta \cdot 2^{N-1}$, and the average power of the sine wave is given by [15, 16]:

$$P_s = \frac{\Delta \cdot 2^{N-1^2}}{2}. \tag{5.18}$$

For the ideal ADC, the SNR with a sinusoidal input signal can be calculated as [15] and it is denoted to:

$$\begin{aligned} \text{SNR} &= \frac{P_s}{P_n} \\ &= \frac{(\Delta \cdot 2^{N-1})^2/2}{\Delta^2/2} \\ &= 1.5 \cdot 2^{2N} \end{aligned} \tag{5.19}$$

or, expressed in decibels:

$$\text{SNR}_{\text{dB}} = 10 \log \frac{P_s}{P_n} = 6.02 \cdot N + 1.76 \quad [\text{dB}]. \tag{5.20}$$

It is noticeable that the $SNR_{dB}$ is increased by approximately 6 dB for every bit in the ADC.

- Spurious Free Dynamic Range (SFDR) :

The SFDR is the ratio of the power of the signal and the power of the largest spurious within a certain frequency band. Spurious signals describe false signals or false signal

components in a frequency spectrum including noises and harmonics. For example, harmonic distortion signal (HD2) is the largest spurious and the calculated SFDR is 75 dBc in Figure 5.9. The SFDR is expressed in units of dBc and defined as

$$\begin{aligned} \mathrm{SFDR_{dBc}} &= 10\log\frac{\text{Signal Power}}{\text{Largest Spurious Power}} \\ &= 10\log\frac{{X_{Fundamental}}^2}{{X_{Spurious}}^2}, \end{aligned} \tag{5.21}$$

where $X_{Fundamental}$ is the *rms* value of the fundamental signal and $X_{Spurious}$ is the *rms* value of the largest spurious. It is also common to express SFDR with the full scale input (dBFS) and

$$\mathrm{SFDR_{dBFS}} = 10\log\frac{(FS/(2\sqrt{2}))^2}{{X_{Spurious}}^2}. \tag{5.22}$$

- Harmonic Distortion ($\mathrm{HD}_m$) :

The $m$-th harmonic distortion ($\mathrm{HD}_m$) is the power ratio between the $m$-th harmonic and the fundamental signal and expressed as

$$\mathrm{HD}_m = 10\log\frac{{X_m}^2}{{X_{Fundamental}}^2} \tag{5.23}$$

where $X_m$ is the $m$-th harmonic *rms* value. harmonics contain less power than the fundamental signal and the $\mathrm{HD}_m$ is a negative.

- Total Harmonic Distortion (THD) :

The THD is defined as the ratio of the total harmonic distortion power and the power of the fundamental in a certain frequency band,

$$\mathrm{THD} = 10\log\sum_{m=2}^{\infty}\frac{{X_m}^2}{{X_{Fundamental}}^2}. \tag{5.24}$$

Practically, calculating the total harmonic power is impossible since there are infinite numbers of the harmonic signals. However, the calculation can be done summing the harmonic signal power until the harmonics can not be distinguished from the noise floor. Here, the value is also negative.

- Signal-to-Noise and Distortion Ratio (SINAD) :

The ratio of the power of the fundamental and the total noise and distortion power within a certain frequency band is defined as the SINAD,

$$\text{SINAD} = 10 \log \frac{S}{N + D} \tag{5.25}$$

where $S$ is the signal power, $N$ is the total noise power, and the $D$ is the distortion power in watts. For example, $N$ can be readable from Figure 5.9 as it provides a graphic readout of the noise floor and $D$ is the same as the sum of the power for the harmonics. Ideally, the distortion and the noise powers would be zero, so that the SINAD would be a very large number. It is interesting to note that the SINAD is a very similar indicator to those used in characterizing a mixer in a wireless system. In communication system applications, SINAD is often employed for baseband measurements while THD is used for RF measurements.

- Effective Number of Bits (ENOB) :

The measurement of ENOB is based on the SNR of the ADC with a full scale sinusoidal input signal. This value describes the real operating range of the ADC

or the mixed-signal SoC device. The ENOB is calculated as:

$$\text{ENOB} = 10 \log \frac{\text{SINAD} - 1.76}{6.02}. \tag{5.26}$$

- Analog power testing and dynamic range

The characterizing parameters in the dynamic testing are both frequency and input signal range (power) dependent. While the ADC performance in the lower input amplitude (or power) levels is usually limited by the quantization error (noise), it is noticeable that the performance at the higher signal levels are limited by the distortion. The SINAD is commonly used to provide the frequency band or signal level characterization [20]. Figure 5.10 is a SINAD plot as a function of input signal levels and frequencies. The result is obtained from input power testing.

Dynamic Range (DR) :

The operating range for the ADC is also characterized by the DR which is the range from the full scale (maximum un-saturated) to the smallest detectable signal (where the SINAD is equal to 0).

$$\text{DR} = 10 \log \frac{Max.[\text{Signal Power}]}{min.[\text{Signal Power}]} \tag{5.27}$$

- Effective Resolution Bandwidth (ERB) :

In specifying the frequency behavior of the ADC, it is commonly to plot the SINAD, SFDR, or SNR as function of input signal frequency. This is illustrated in the Figure 5.11. The effective resolution bandwidth (ERB) is the input frequency point

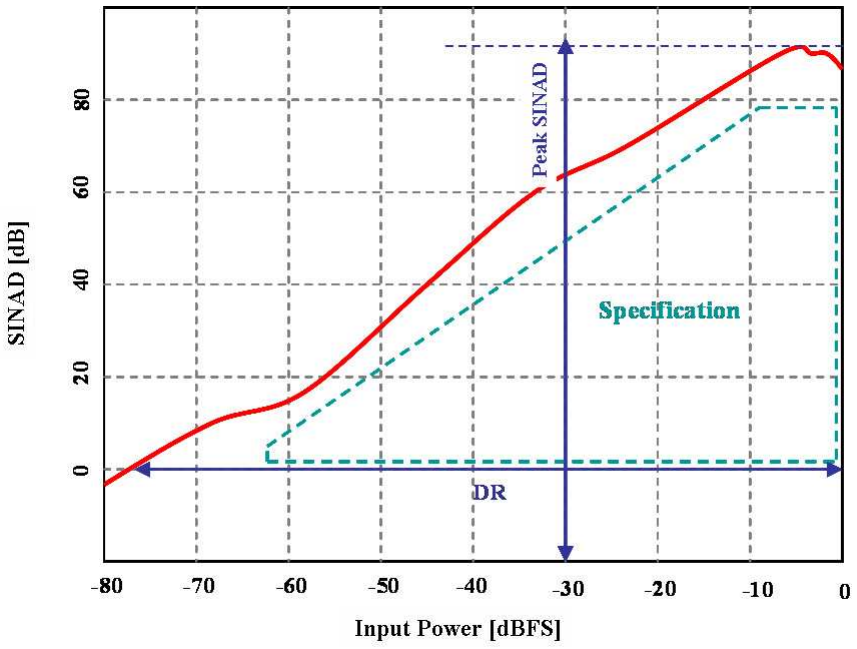



Figure 5.10: Signal-to-noise-and-distortion vs. input power defines the ADC input specification

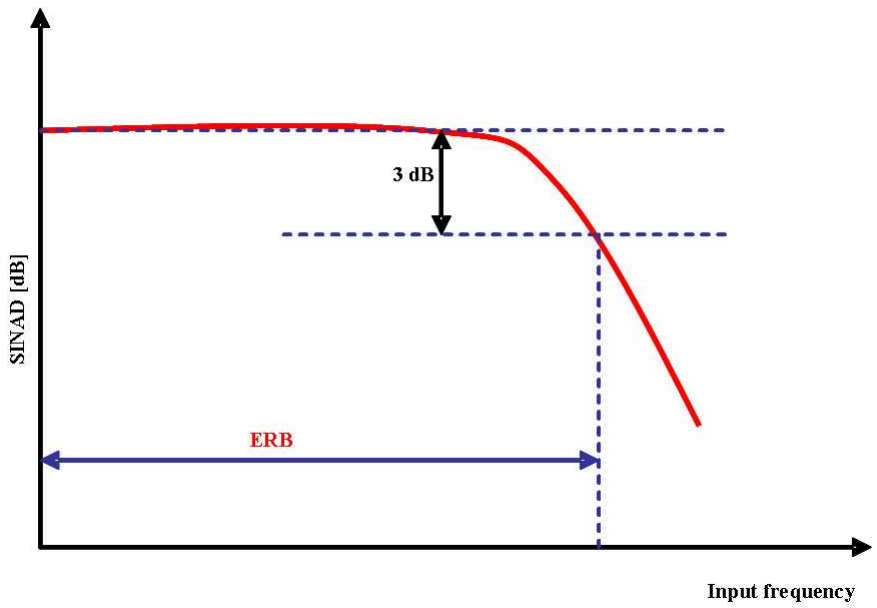



Figure 5.11: Effective resolution bandwidth of ADC

where the SINAD has dropped 3dB (or ENOB 1/2 bit). The signal bandwidth is an important ADC parameter. The ADC bandwidth is limited by the analog bandwidth of the input circuits and the sampling frequency of the ADC.

- Inter-modulation Distortion (IMD) :

Testing ADCs with a single tone sinusoidal input signal is not sufficient to characterize the dynamic performance of ADCs, especially for communication applications. The ADCs are also characterized by multi-tone measurements. Therefore, the inter-modulation distortion, SNR with multi-tone signals, and multi-tone power ratio are another important parameter to characterize ADCs.

When a multi-tone signal is used for characterizing ADCs, IMD appears. First,

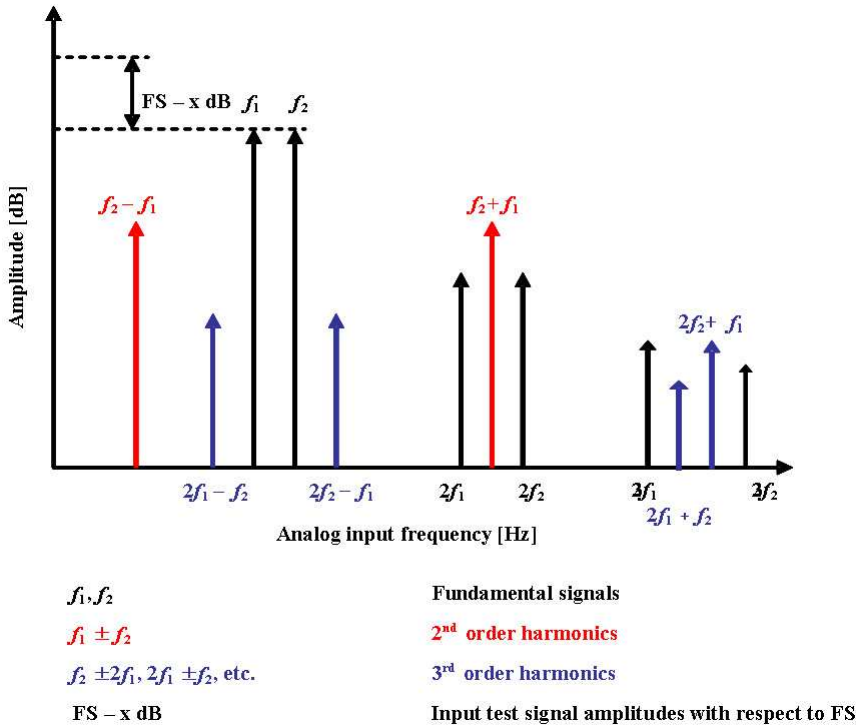



Figure 5.12: Intermodulation distortions of ADC

two tone signal can be considered as f1 and f2 with sampling rate fs. The 2nd and 3rd IMD products appear as Figure 5.12. The IMD appears at the frequencies where

$$k \cdot f_1 \pm m \cdot f_2 \tag{5.28}$$

where $k$ and m are integers and $k \neq 0,\ m \neq 0$, and $f_1 \neq f_2$. The IMD is calculated as:

$$\text{IMD} = 10 \log \frac{\sum {X_{k,m}}^2}{{X_{Fundamental}}^2}, \tag{5.29}$$

where $X_{Fundamental}$ is the *rms* value of the fundamental signal and $X_{k,m}$ is the *rms* value for the harmonics at the frequency given in Eqn. 5.28.

The performance of the ADC can be characterized by measuring the intrinsic parameters and performance parameters using the static and the dynamic testing methods [13, 20]. Characteristic parameters are also defined and briefly explained in this chapter. The intrinsic parameters, such as quantization errors, INL and DNL, are also not sufficient to fully characterize the performance of ADCs especially in a communication systems application. Static testing must be performed along with the dynamic testing, so that the ADC performance can be fully characterized with performance parameters. Typically, dynamic errors are more significant at higher sampling rates and signal frequencies. These cause settling errors, glitches, and other issues on [44, 55, 56, 57, 58, 52]. In the frequency domain, SINAD, SFDR, and ENOB are introduced and two-tone (or multi-tone) test is also applied to ensure the full characterization of the ADC which is used in the communication systems. The test suite developed for this thesis is unique in the industry, in that it includes

all these elements.

### 5.2.2 Compressing ADC

Compressing ADCs are used in a variety of applications in which extremely wide dynamic range is required. Testing compressing ADCs is not so different from testing linear ADCs. A typical compressing ADC topology is shown in Figure 5.13 [59]. The architecture of the compressing ADC is illustrated in Figure 5.14. While the comparators compare the node voltages using an equal resistor divider ladder, the compressing ADC uses the basic linear flash approach with unequal ladder resistors. The node voltages are compared to a single reference voltage and the digital output code can be produced. The ideal static compressing transfer curve for a 3-bit compressing ADC is shown in Figure 5.15. The static ramp testing can be also performed to characterize the static performance of the compressing ADC. Test setup is the same as illustrated in Figure 5.8. The only challenge for the static ramp testing is ascertaining the bit-wise digital output signals from the each. These are difficult to observe, especially for the LSB out. Synchronization of each output bit is also carefully maintained to determine precision code edge verifications.

Since the compressing flash ADC can provide outstanding dynamic range of sampling signal. This characteristic of the compressing ADC can be observed from the transfer function or from bitwise digital outputs. Therefore, to determine the digital code edges precisely, the programmable power supply can be used as the

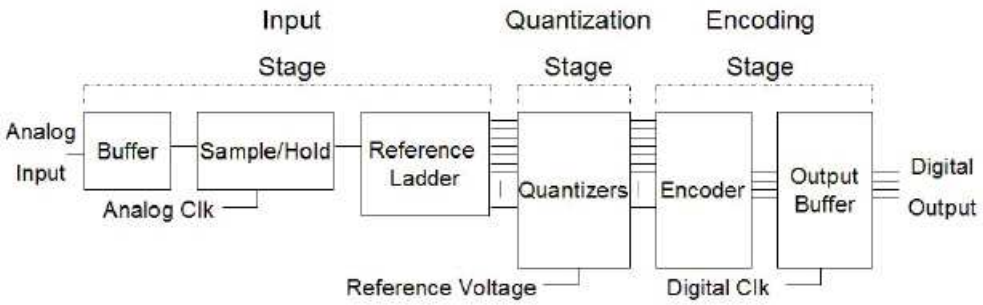



Figure 5.13: Block diagram of the characterized compressing ADC [59]

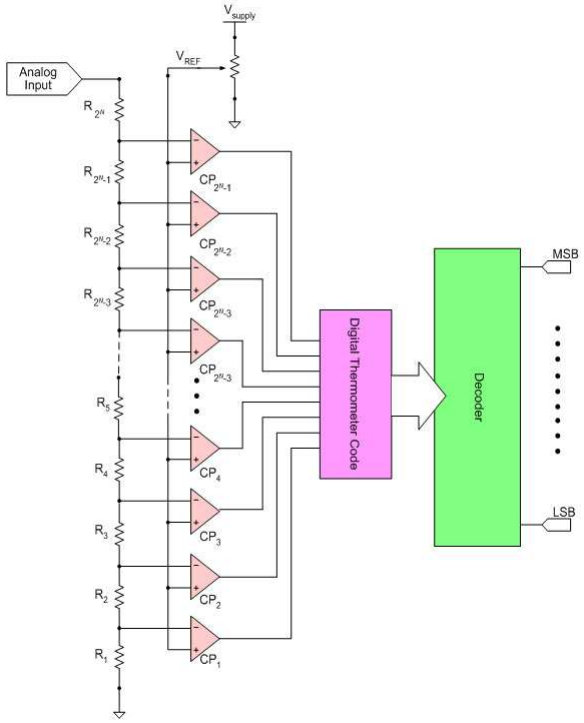



Figure 5.14: The compressing flash ADC architecture [59] characterized in this thesis

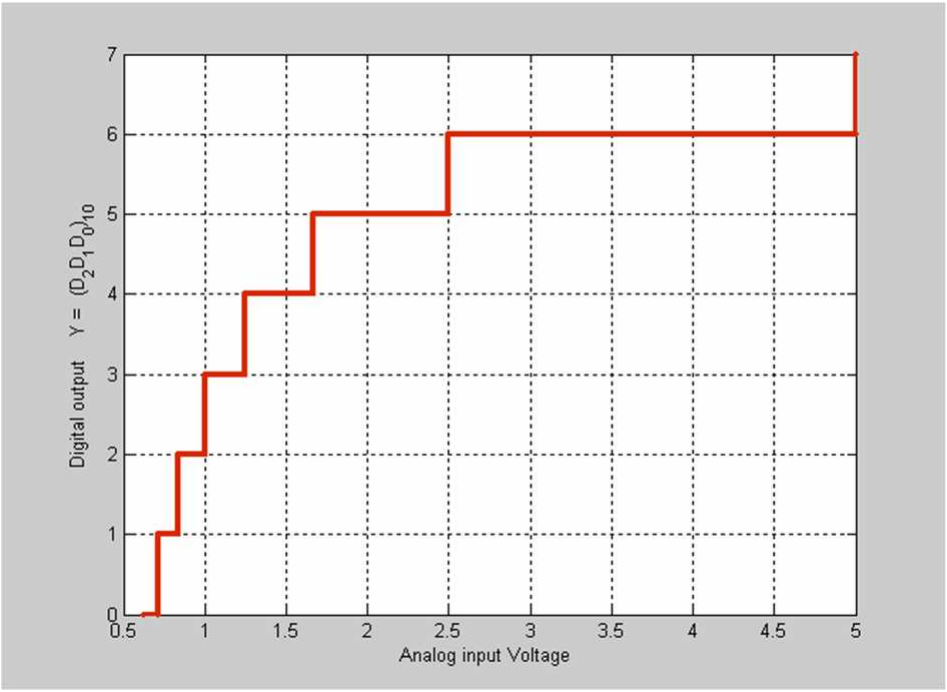



Figure 5.15: 3-bit compressing ADC transfer function

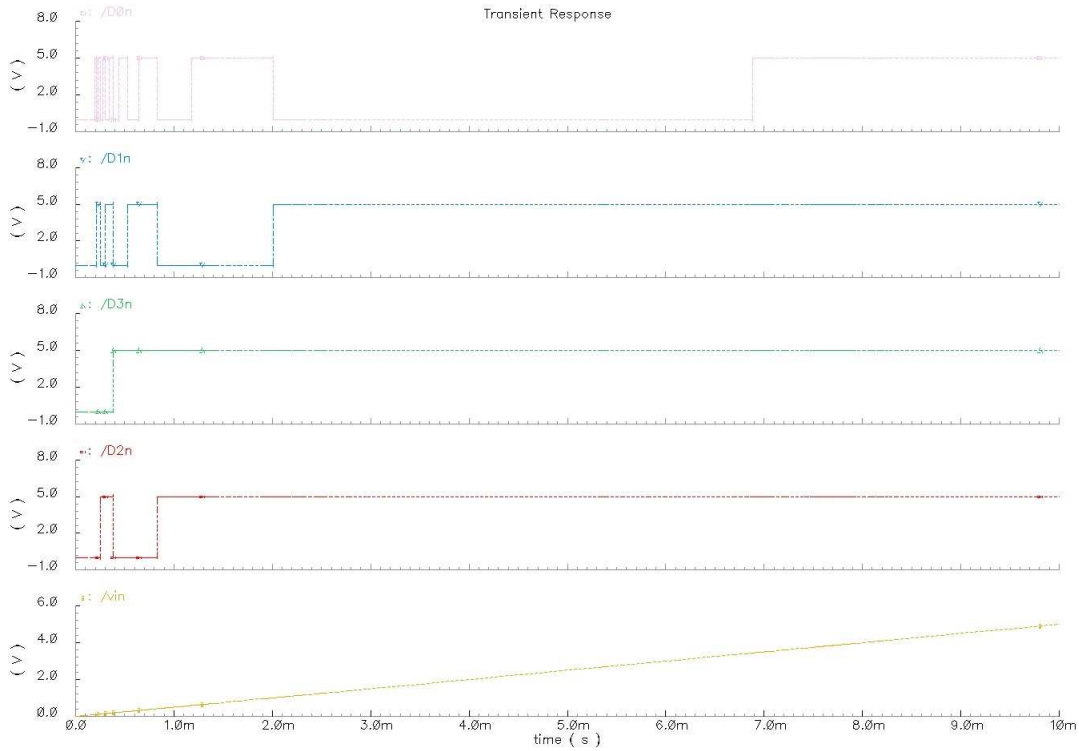



Figure 5.16: 3-bit compressing ADC bitwise digital output waveforms ($V_{ref}$ = 100 mV)

source for the static ramp generator. However, if the input is generated with too many points with the full scale range, acquiring the digital bitwise outputs requires the large memory for the capturing.

The ADC studied here was fabricated with the AMI Semiconductor (AMIS) CMOS 0.5 $\mu m$ process in a 4-bit 80 MS/s compressing configuration [59]. The static test result is derived to show a simple compressing ADC static testing sequence. Ideal bitwise digital outputs for 100 [mV] reference voltage with 100 [Hz] ramp input signal are simulated in *Cadence*® and shown in Figure 5.16. In bench testing,

the test setup followed shown in Figure 5.8. Here, we employ a buffer memory to acquire the digital outputs. Bitwise digital outputs are not captured as these are distorted by noise and by glitches. The noisy bitwise output can be filtered using a quiet DC source reference voltages, or by using a simple LRC passive filter. The glitches are directly related to the performance of the chip circuit design.

Static ramp testing is performed at several voltage reference levels. With designer's SPICE simulations, we verified that glitches result from the low gain of the amplifiers. Thus, when the reference voltage is increased, the glitches are significantly reduced. The bitwise digital outputs with 1 V reference voltage and the input ramp signal at 100 Hz is shown in Figure 5.17. The final static transfer function is plotted after the post process and followed in the Figure 5.18.

Timing errors are significant with sparkling in the transfer function plot in the Figure 5.18. For precision characterization for the designed ADC, the static transfer function must be repeated. Flash type ADCs often exhibit "sparkling" which is due to a digital timing race conditions. This sparkling (seen in Figure 5.18) is different from noise-induced errors which are mainly from code edge transitions. Typically, the ADCs are monotonic, which means the analog amplitude level increases with increasing of the digital code. However, the test result shows that the compressing flash ADC studied here has some monotonic errors. Test methodology for sparkling varies in the choice of input signal. From the static ramp test, we can visualize sparkling as obtained. The sinusoidal high frequency signal can also be applied to

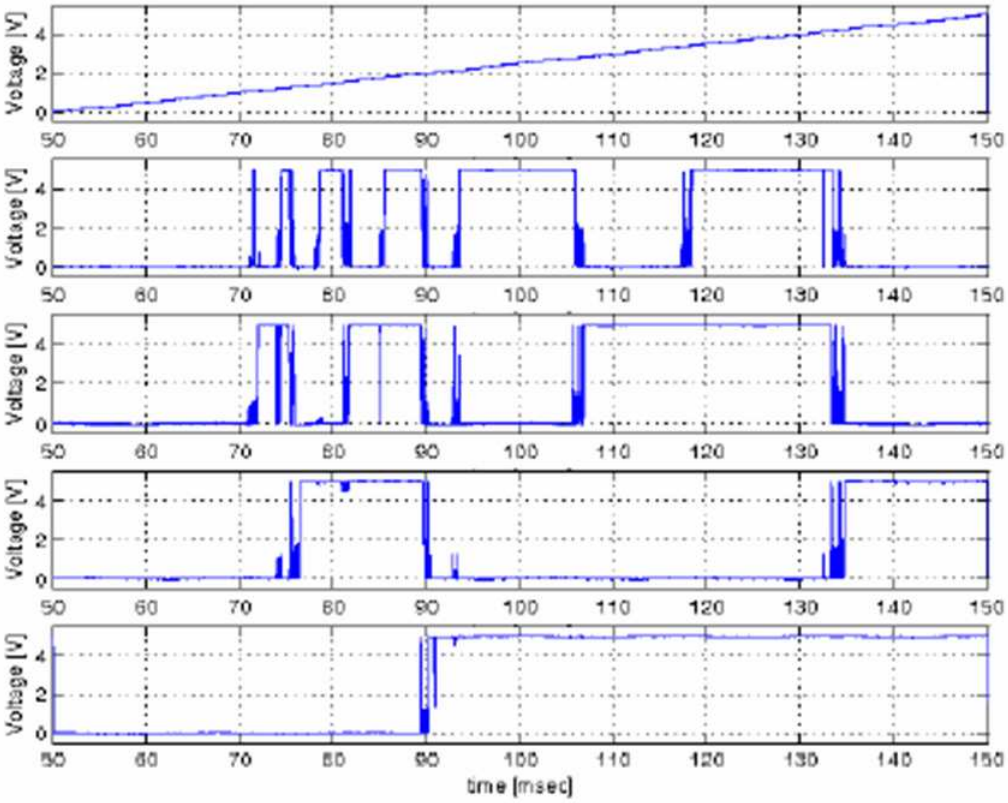



Figure 5.17: Characterized 4-bit 80 MS/s compressing ADC digital outputs: Bitwise digital output waveform with Vref = 1 [V] and the ramp input signal at 100 [Hz]

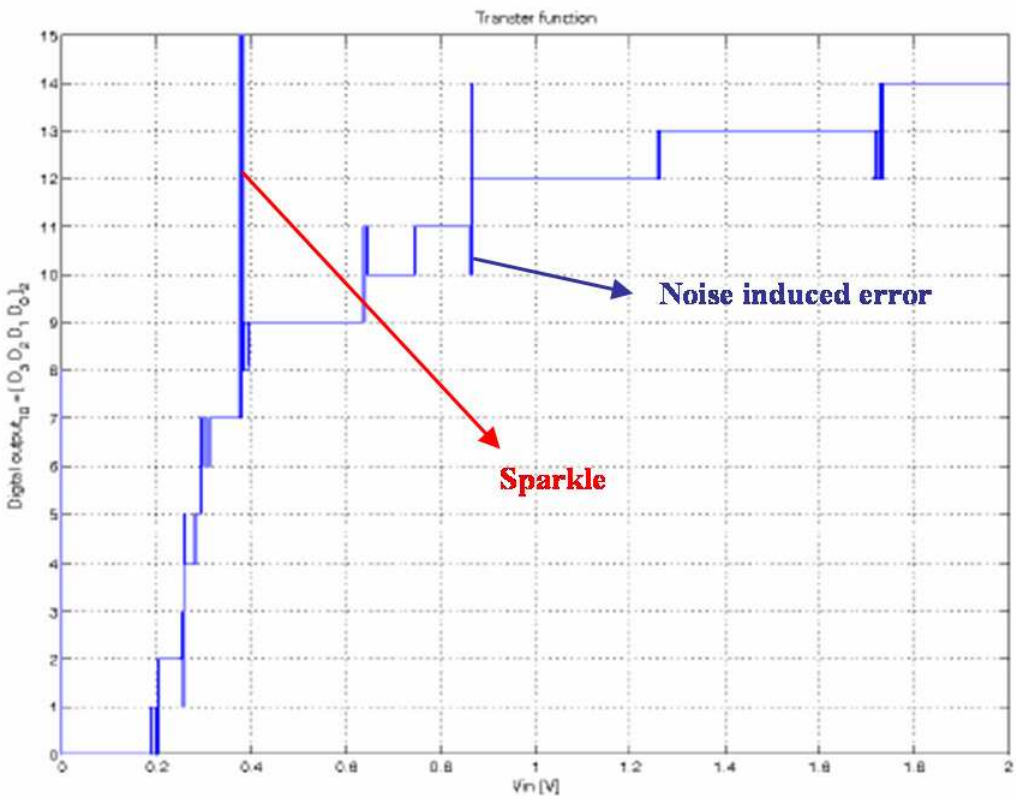



Figure 5.18: Measured static transfer function for 4-bit 80 MS/s compressing ADC

the ADC so that the sparkle-related time domain spikes in the collected samples can be measured.

The dynamic test for the given compressing ADC must be also performed. The dynamic testing schemes are basically the same as previously discussed. The sampling rate is 80 MS/s so that the input signal must be less than 40 MHz. Some of the dynamic testing results for the given 4-bit compressing ADC are shown in Figure 5.19 and Figure 5.20

To characterize and verify compressing ADC performance, requisite tests can be summarized:

- Static test:
  - Linear ramp test with AWG
- Low frequency (sampling clock speed $\leq$ 100 MHz) dynamic test

The lesson learned here is that design-for-test (DfT) procedures could be very important in improving final system performance. Especially, missing functional pin-outs for an internal reference voltage generation, an input voltage over-range detection, and a converter data-ready buffer are adding testing and characterizing ambiguity.

## 5.3 A verification test software (VTS) suite for automated testing

As seen above, manual testing of a complex system is time consuming and difficult. One of the primary achievement of this work was the development of an ADC

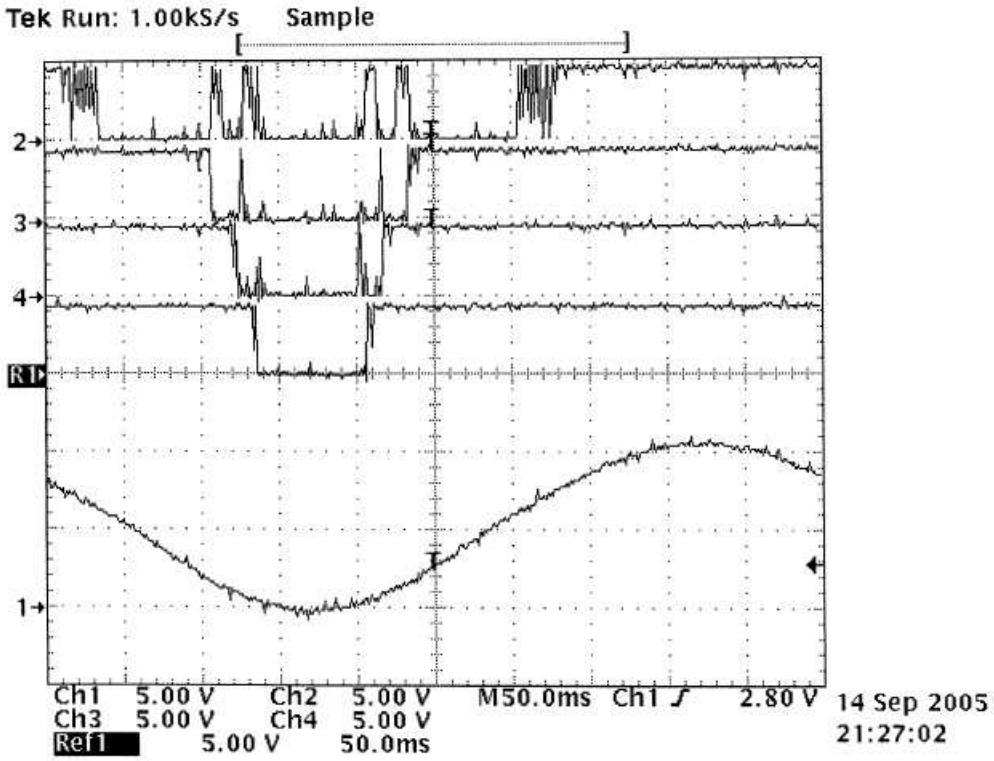



Figure 5.19: Dynamic performance of a 4-bit 80MS/s compressing ADC: 2Hz sine wave input (amplitude: 5 [V], DC offset: 5 [V], $V_{ref}$: 0.2 [V], Design-for-test philosophy is not applied initially, so that the testing and characterizing contains many factors of ambiguity.

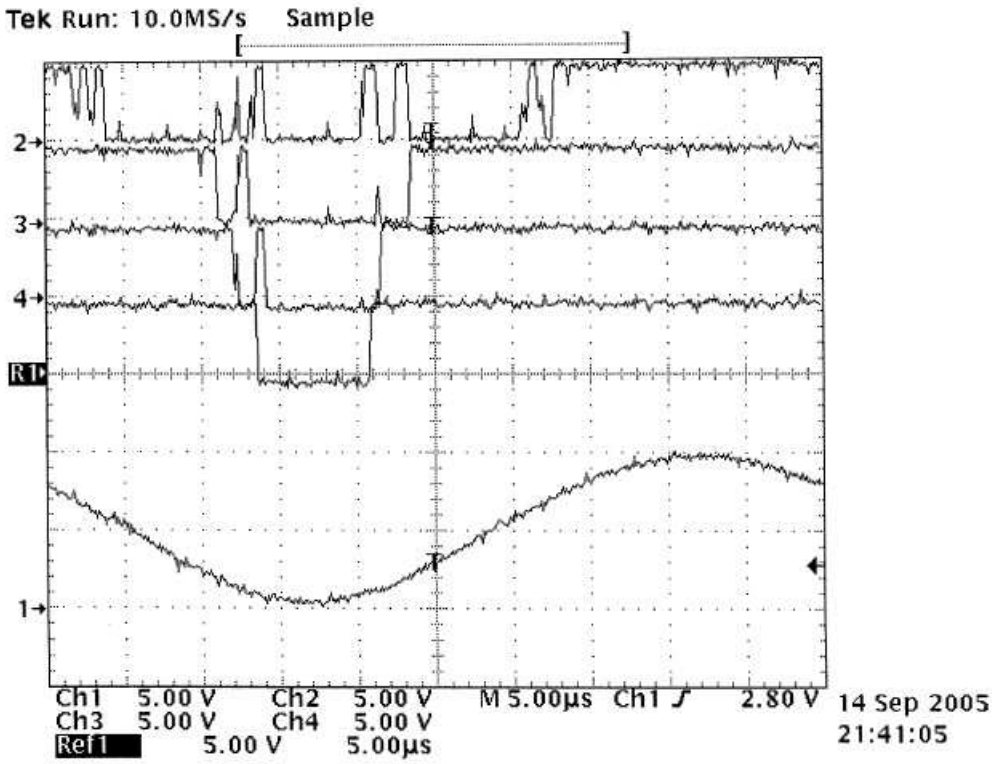



Figure 5.20: Dynamic performance of a 4-bit 80MS/s compressing ADC: 20 kHz sine wave input (amplitude: 5 [V], DC offset: 5 [V], $V_{ref}$: 0.2 [V], Design-for-test philosophy is not applied initially, so that the testing and characterizing contains many factors of ambiguity.

verification software suite to assist in logging and analyzing performance data at high speed and with wide dynamic range. The verification test software (VTS) suite has a graphical user interface (GUI) written in MATLAB and Figure 5.21 shows the main frame of the high-speed ADC VTS suite. A primary aim of the software is to proceed device verification tests (DVTs) for high speed ADCs used in high quality RF receivers. Since the ADCs are produced in significant volume and will be applied into HNS *SPACEWAY* receiver systems [31], the ADCs as devices-under-test (DUTs) are mostly tested under ADC dynamic driving conditions.

High-speed ADC design verification test software extract the ADC performance parameters and specify their electrical characteristics under dynamic testing condition with input sine-waves. Most dynamic tests consist of two major parts: single-tone and two-tone testing.

ADC single-tone test result provides the bulk of the ADC's dynamic performance parameters. By characterizing ADC with single-tone sine-wave, the critical system parameters can be extracted.

The two-tone test is a good indicator of internal system device linearity. Intermodulation distortion (IMD) can be measured with a two-tone test and the result is used for estimate the receiver performances.

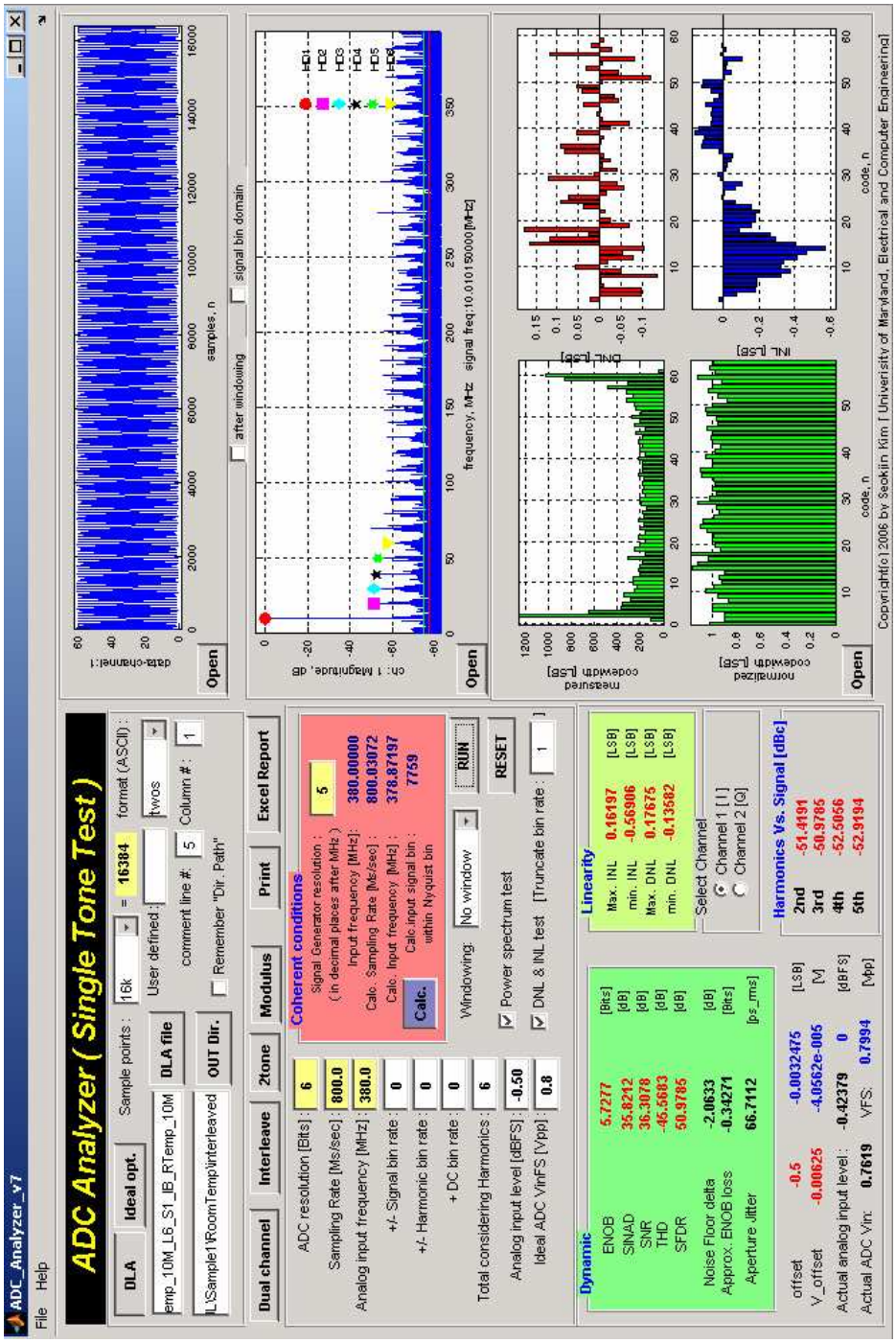



Figure 5.21: High-speed ADC design verification test software main frame interface: VTS suite

### 5.3.1 VTS features

The VTS suite main features are summarized below:

- Integrated coherent sampling calculator
- Integrated ideal ADC simulator
- Integrated windowing function for the input signal tone
- Fast ADC performance evaluations and parameter extractions

### 5.3.2 Why the VTS is unique?

Troubleshooting sophisticated high-speed ADC design is all about detecting problems quickly, getting to the root cause and working efficiently. Your success starts with having the right debug tools, and the VTS suite can be one of the most effective system engineering tool-box with better repeatability and automated laboratory test setup. The VTS key advantages are:

- Since the VTS configures the test equipment, the same instrument settings are applied to each time an evaluating ADC is characterized.
- When the VTS is acquiring data, it accesses to a saved data file that is captured by a modern deep-memory logic analyzer. This can eliminate errors due to incorrect data entry such like manually entering data into a spreadsheet or into a file for post-processing.

- The VTS can be driving in the host computer for ADC testing or stand-alone, so that thousands of the sampling data points from an evaluating ADC can be acquired in minutes and can be save in a text file (ASCII format).

- The analysis result can be summarized in Microsoft Excel spreadsheets or can be printed out from the VTS suite graphical user interface (GUI) in a portable-document-format(PDF) file format.

- The VTS suite can diagnose a full input sampling channel. Test engineers and VTS users may gain deep insight into system performance issues by utilizing the VTS suite window functions and graphic of optimization of ADC input signal frequency leakages. Therefore, the VTS can be extended to fully characterize an input sampling channel, later on.

- The Matlab based graphical user interface (GUI) is suitable for easy program access, data handling and advanced mixed-signal testing features.

### 5.3.3 Spectral leakage and windowing

The dynamic parameter extraction of ADC under test is performed by the fast Fourier transform (FFT) algorithm fully integrated into the VTS suite single/two-tone test modules. By necessity, every sampled signal must be of finite extent for a signal processing [60, 61]. First, let's consider the case of performing an N-point FFT on a pure (ideal) sinusoidal sample signal. The ratio between the sampling

frequency and the input sine wave frequency is set such that precisely an integral number of cycles is contained within the data window frame (recorded samples in a logic analyzer) as shown in Figure 5.22. FFT algorithm assumes that a periodic waveform can be formed by placing an infinite number of those window end-to-end. FFT output of the (continuous) waveform without any discontinuity results in that the single tone located at the input frequency. This situation corresponds to a "coherent" sampling condition in testing ADCs.

Second, When the number of sine wave cycles is not an integral number within a sampling window frame, the discontinuities occur at the end points of the sampling data frame as shown in Figure 5.23 This result in spectral leakage in the frequency domain. If a time record does not contain an integral number of cycles, the continuous spectrum of the sampling window frame is shifted from the main lobe center at a fraction of the frequency bin that corresponds to the difference between the frequency component and the FFT frequency lines [62]. This shift causes side lobes to appear in the spectrum. Thus, the side-lobe characteristics directly affect the extent to which adjacent frequency components "leak into" the neighboring frequency bins. The FFT result of the input sine wave appears over several frequency bins with a main lobe and side-lobes. This situation corresponds to a "non-coherent" sampling condition in test ADCs and conventional spectral analysis results are not accurate to evaluate ADC dynamic performance (assumed that a sampled sine wave is a pure and does not have any discontinuity within a sampling window frame).

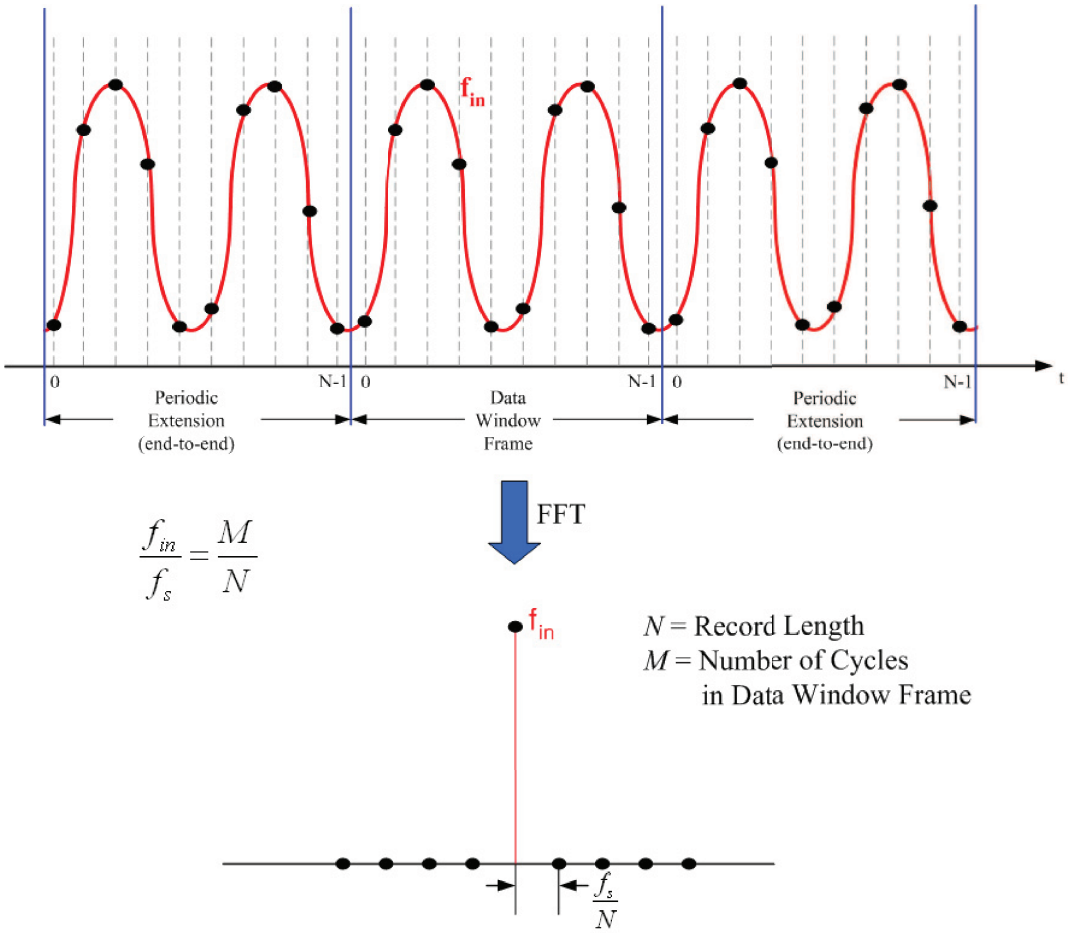



Figure 5.22: FFT representation of pure sine wave having integral number of cycles in a sampling data window

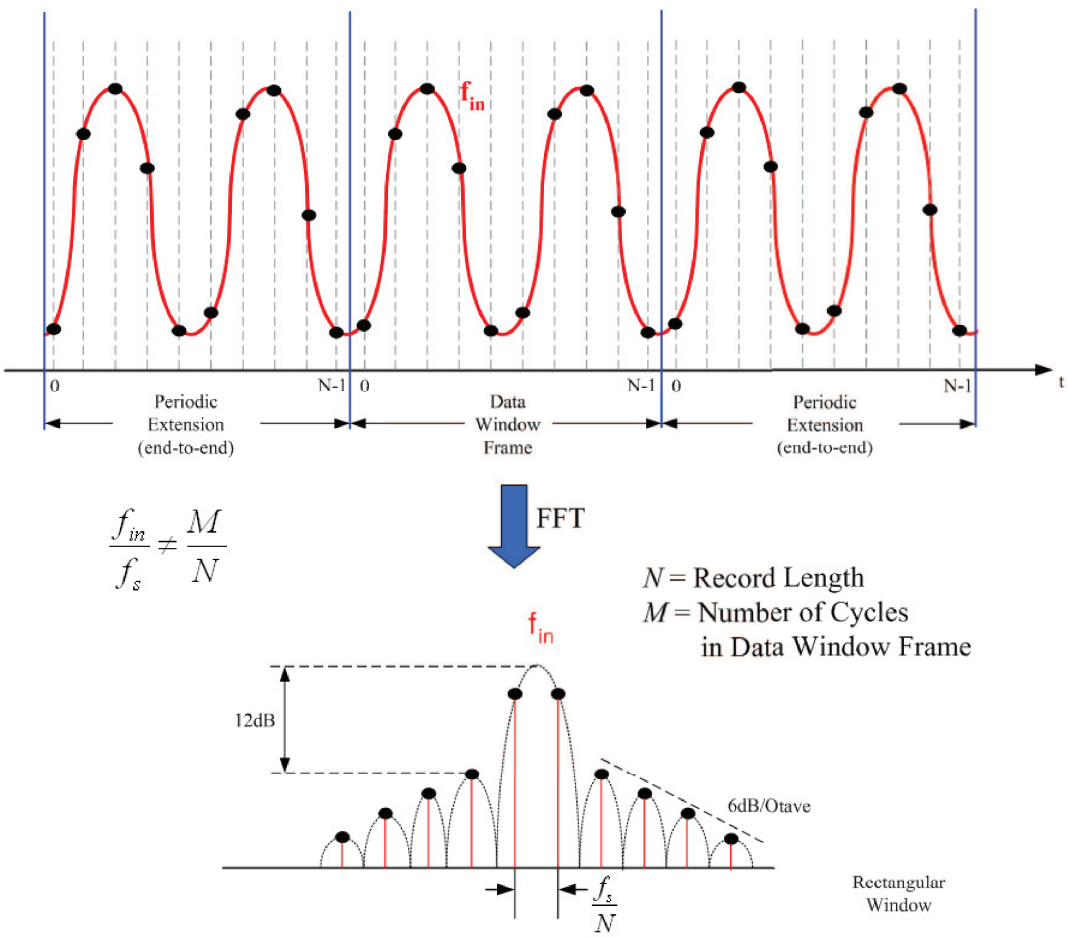



Figure 5.23: FFT representation of pure sine wave having non-integral number of cycles in a sampling data window

Practically, even though the pure sine wave is used to test ADCs, the coherent sampling condition may not be feasible due to the signal source imperfection or sampling clock signal jitters. In those case, the VTS is applying windowing functions to a sample signal to minimize those side lobes. The acquired samples are multiplied by an appropriate window function, which forces the acquired signal to be continuous at the edges of a sampling window frame.

With windowing functions, the VTS is considering multiple signal frequency bins, harmonic bins and DC components in testing ADC spectral analysis. This result is used for calibrating the testing environment to calculate critical ADC parameters for telecommunications such as SNR, SINAD, THD, IMD, and noise floor.

Various sampling signal windowing functions such as Hanning, Hamming, Blackman, Kaiser, and etc., are adding to cost effective ATE setup for input signal generator. An in-depth treatment of windowing functions for harmonic analysis can be found in [63, 64]. Those windowing functions are useful for a case of ADC dynamic testing with an imperfect signal sources for clock or input signal generator. Higher resolution ADCs (above 8-bit) have more difficulties to be characterized accurately in a non-coherent sampling condition, since the phase noise of a sampling clock generator must be low enough to reduce the jittering effect (sampling aperture ambiguity). The most convenient method to improve the measurement accuracy of a non-coherent waveform is to increase the size of the sampling frame (numbers of sampling points).

Before choosing an appropriate window, it is necessary to define the parameters and the characteristics that enable users to compare windows. Such characteristics include the 3dB main-lobe width, the 6dB main-lobe width, the highest side-lobe level, and the side-lobe roll-off rate. Figures of merit for 4 popular windowing functions are summarized in Table 5.1 and their mathematical expressions follow [63, 62, 65]:

- Hamming:

$$w(n) = 0.54 - 0.46 \cos\left[\frac{2\pi n}{N}\right]$$

- Blackman:

$$w(n) = 0.42 - 0.5 \cos\left[\frac{2\pi n}{N}\right] + 0.08 \cos\left[\frac{4\pi n}{N}\right]$$

- Hanning:

$$w(n) = 0.5 - 0.5 \cos\left[\frac{2\pi n}{N}\right]$$

- Minimum 4-term Blackman Harris:

$$\begin{aligned} w(n) = 0.35875 \quad &- \quad 0.48829 \cos\left[\frac{2\pi n}{N}\right] \\ &+ \quad 0.14128 \cos\left[\frac{4\pi n}{N}\right] \\ &- \quad 0.01168 \cos\left[\frac{6\pi n}{N}\right] \end{aligned}$$

where, $0 \leq n \leq N - 1$, and $N$ is the total number of sampling points.

To choose the right spectral window, one has to guess the signal frequency content. If the signal contains strong interfering frequency components distant from

Table 5.1: Popular ADC input window functions and figures of merit

| Window Function | 3dB BW (Bins) | 6dB BW (Bins) | Highest sidelobe (dB) | Sidelobe rolloff (db/Octave) |
|---|---|---|---|---|
| **Rectangle** | 0.89 | 1.21 | -12 | 6 |
| **Hamming** | 1.30 | 1.81 | -43 | 6 |
| **Blackman** | 1.68 | 2.35 | -58 | 18 |
| **Hanning** | 1.44 | 2.00 | -32 | 18 |
| **Minimum 4-term Balckman-Harris** | 1.90 | 2.72 | -92 | 6 |

the frequency of interest, you should choose a window whose side lobes have a high-rolloff rate. If strong interfering signals are close to the frequency of interest, a window with low maximum levels of side lobe is more suitable. If the interest frequency band contains two or more signals close to each other, spectral resolution becomes important. In that case, a window with a narrow main lobe is better. For a single frequency component in which the focus is on amplitude accuracy rather than its precise location in the frequency bin, a window with a broad main lobe is recommended.

## 5.4 High-speed ADC DVT methodology

Real time instrument acquisition controls are run through an IEEE 488 bus and the 10/100baseT LAN connection is able to transfer the test data to a personal computer (PC) for post-processing. The algorithms used in post-processing comply with IEEE Standard 1241 [28]. The basic steps needed to characterize the data

converter are:

1. Set up and configure the test bench;
2. Acquire the sampled data;
3. Transfer the logged data into a host PC; and
4. Calculate the ADC parameter set using the VTS suite.

### 5.4.1 Operations

To perform the ADC dynamic testing using the VTS suite, the test frequency and sample frequency must be properly selected to insure that all digital codes in the testing ADC are exercised. Make sure that the measurements for the signal-to-noise ratio(SNR) and harmonic distortion rate(HD) are not compromised by the test methodology. Using the integrated coherent signal tone calculator, a prime number of test-tone cycles can be acquired. This results in the sampling window frame does not have any discontinuity between the data endpoints and the FFT output produces a spectrally pure result, where the test-tone and harmonics are contained in one frequency bin, each. Properly selected sample and input test-tone frequencies result in all the energy from the test-tone appearing in a single frequency bin.

Once, high-speed ADC test set-up and graphical configuration (Figure 4.23) were finished as explained in Chapter 4. Test operation flow follows the routine in

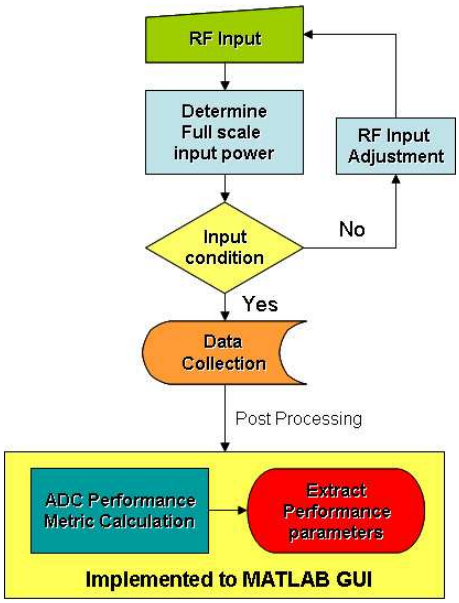



Figure 5.24: High-speed ADC DVT operations with VTS

Figure 5.24. RF analog input is applied by referencing to the sampling clock generator. This step, so-called "synchronization," is critical to lock the phase between reference sampling clock generator and RF signal generator. Then, the applied RF signal level is determined in the units of the input full scale signal(dBFS) and digital outputs of the testing ADC are captured by using a conventional digital logic analyzer. The collected data are transferred to the local host computer and post-processed using the VTS suite.

As shown in Figure 4.23(Chapter 4), ADC digital outputs are captured by the digital logic analyzer (DLA) from Agilent technology using its state mode analysis feature. The DLA (Agilent 16702B mainframe)has a 64M state memory and an 800 Mb/s (or 800 MHz) sampling frequency. Agilent 16760A timing and state

testing module and the operating software must be setup as shown in Figure 5.25. 'Analyzer<A>' stands for the DLA operating software testing main frame setup. 'TEXT_WAVEFORM' is listing capturing data sets and graph 'A', 'B', and 'OVER-DRIVE' are sample plots for demultiplexed digital output channel A and B, and over_range pin, each; 'AOUT' and 'BOUT' indicate the automatic data storing in the local hard drive (ASCII decimal format).

It should be note that both demultiplexed digital output channel data A and B must be re-coded to make a full 800 MS/s data string. That is, the digital outputs acquire 8092 sampled data points using the ADC 400 MHz 'data_ready' output as the logic analyzer state clock rate (capable of operation up to 800 Mb/s). Each of the 6:12 demultiplexed data outputs (A and B) are, therefore, acquired. There are 16384 sampled data points in total for the 6-bit ADC. The acquired samples (2 sets of 8092 samples) are transferred to the host PC completing the sampling data set with a 16384 record size and analyzed for specific ADC performance parameters via the 10/100BaseT LAN connection.

To achieve the best data acquiring result, an eye analysis can be use to trigger each digital outputs. Agilten 17660A state testing module are used testing ADC "data_ready" signal as the data acquisition signal, so that the larger eye opening can be obtained as shown in Figure 5.26 . If a successful digital logic output capture is achieved, the graph 'A' and 'B' in Figure 5.25 show the capture sample plots and their state logic clearly. The screen shot is shown in Figure 5.27.

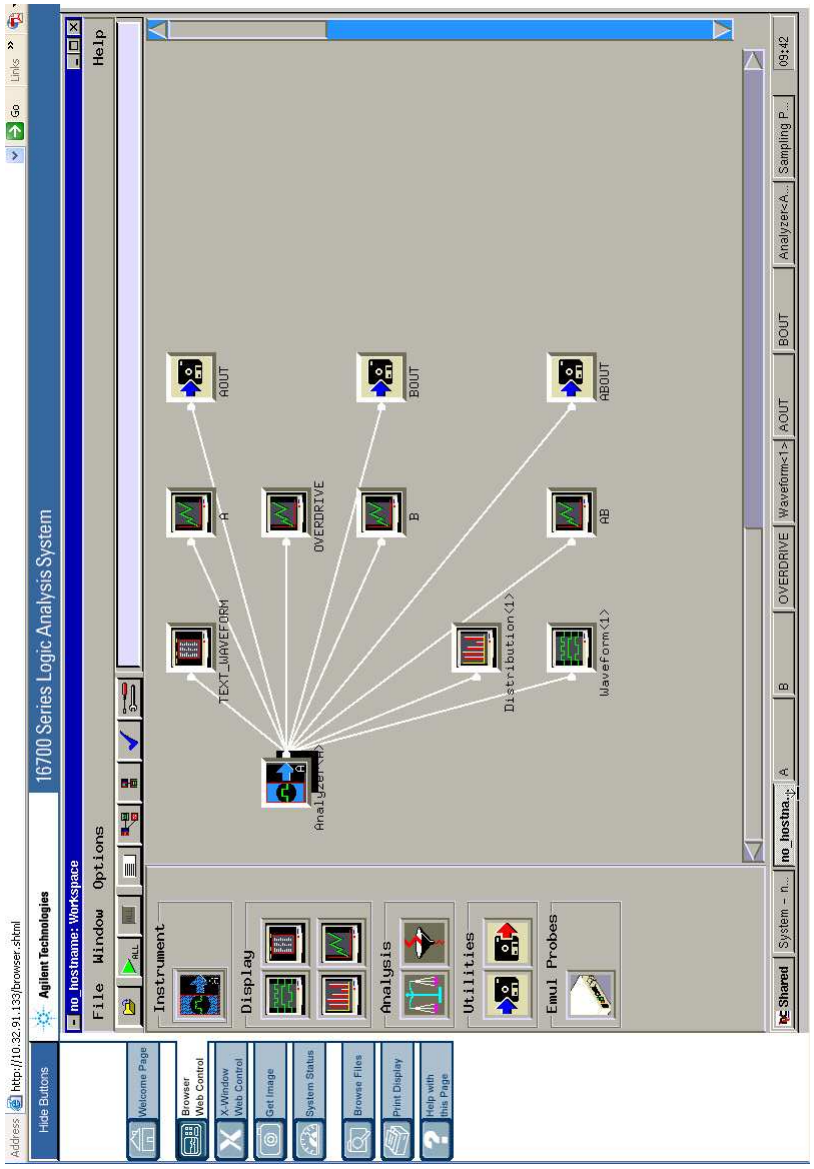



Figure 5.25: *Thames* ADC DVT DLA setup configuration: 'Analyzer<A>' stands for the DLA operating software testing main frame setup; 'TEXT_WAVEFORM' is listing capturing data sets; and graph 'A', 'B', and 'OVERDRIVE' are sample plots for demultiplexed digital output channel A and B, and over_range pin, each; 'AOUT' and 'BOUT' indicate the automatic data storing in the local hard drive.

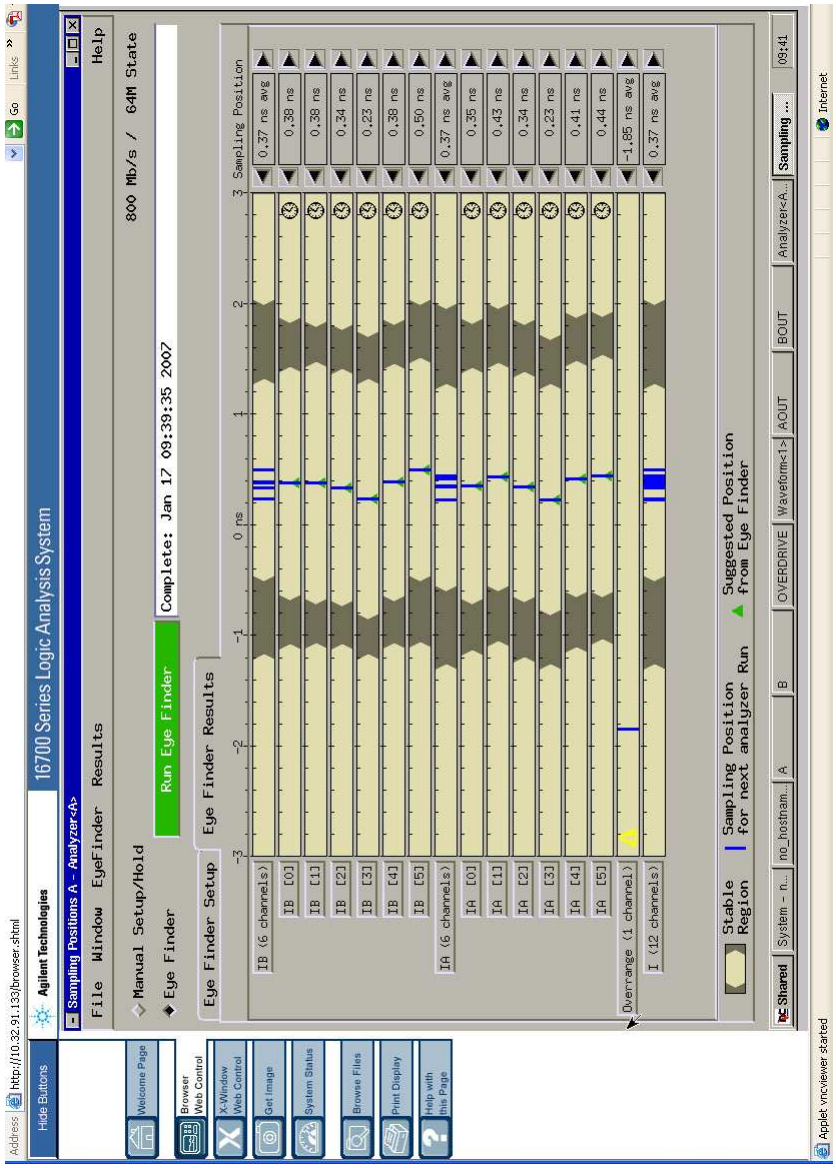



Figure 5.26: *Thames* ADC demultiplexed digital output DLA eye analysis for the best triggering: Channel A and B for analog input channel I

The following steps are used to complete the data collection and to analyze the performance of testing ADC:

1. Initialize the logic analyzer and signal generators.

2. Press "Reset" button in the VTS to initialize a program.

3. Use the integrated coherent calculator to find the input and the sampling test-tone frequency. The resolution of the test ADC (bits), target sampling rate (MS/sec), target input test-tone frequency (MHz), and the resolution of the signal generator are set.

4. Click the "Calc." button to calculate the coherent sampling condition.

5. Set the signal generators to the coherent calculator result

6. Enter a filename where the converter digital output data will be stored.

7. Select the acquiring data points for sampling. All points are used in the FFT. The data format is also set.

8. Enter or select a file location.

9. Enter or select a output directory.

10. Set "± Signal bin rate", "± harmonic bin rate", and "DC component bin rate." All parameters are set to zero, initially.

11. Set "Total numbers of considering harmonics." (Default is 9)

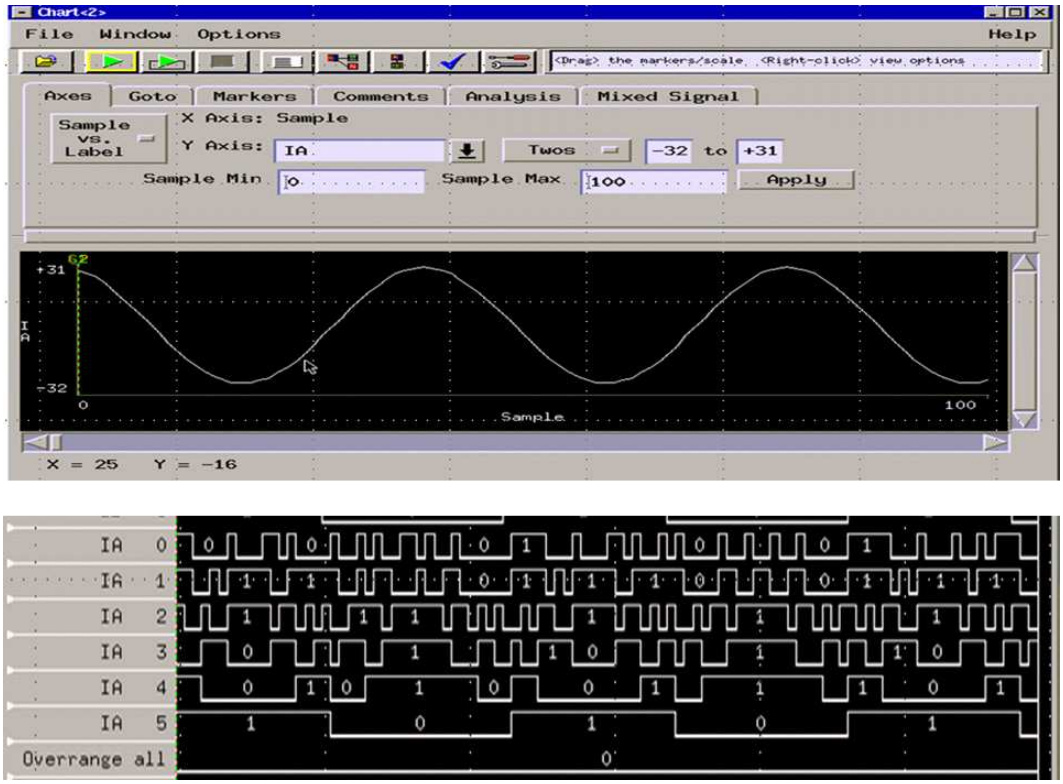



Figure 5.27: *Thames* ADC demultiplexed digital output channel A data successful acquiring using the DLA: clear sample plot for channel A data is plot along with each bit-wise digital output state mode graph. 'data_ready' (400MHz) signals is used for synchronizing external clock for the DLA state mode analysis. Acquiring samples are 800 MS/s ADC digital bitwise outputs under 400 MS/s state mode data analysis using Agilent 16702B digital logic analyser.

12. Press “Run” button to run the VTS suite.

The VTS is capable of analyzing the sampling signal in a time domain for easy bench debugging as using a sine wave code error testing modules as shown in Figure 5.29. The single-tone sine wave testing and two-tone sine wave testing VTS modules are shown in Figure 5.21 and Figure 5.28, each.

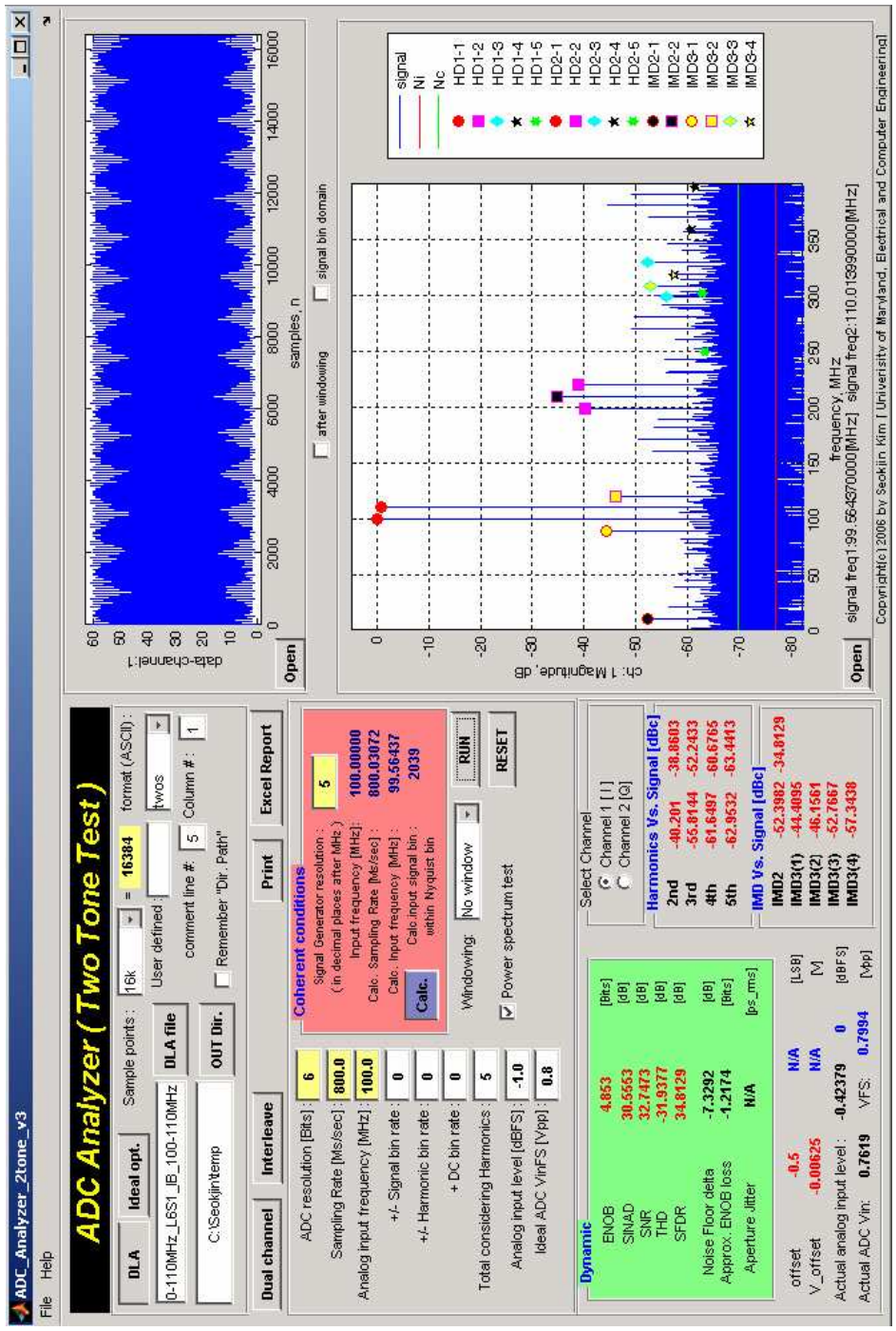



Figure 5.28: High-speed ADC DVT VTS suite two-tone testing module GUI

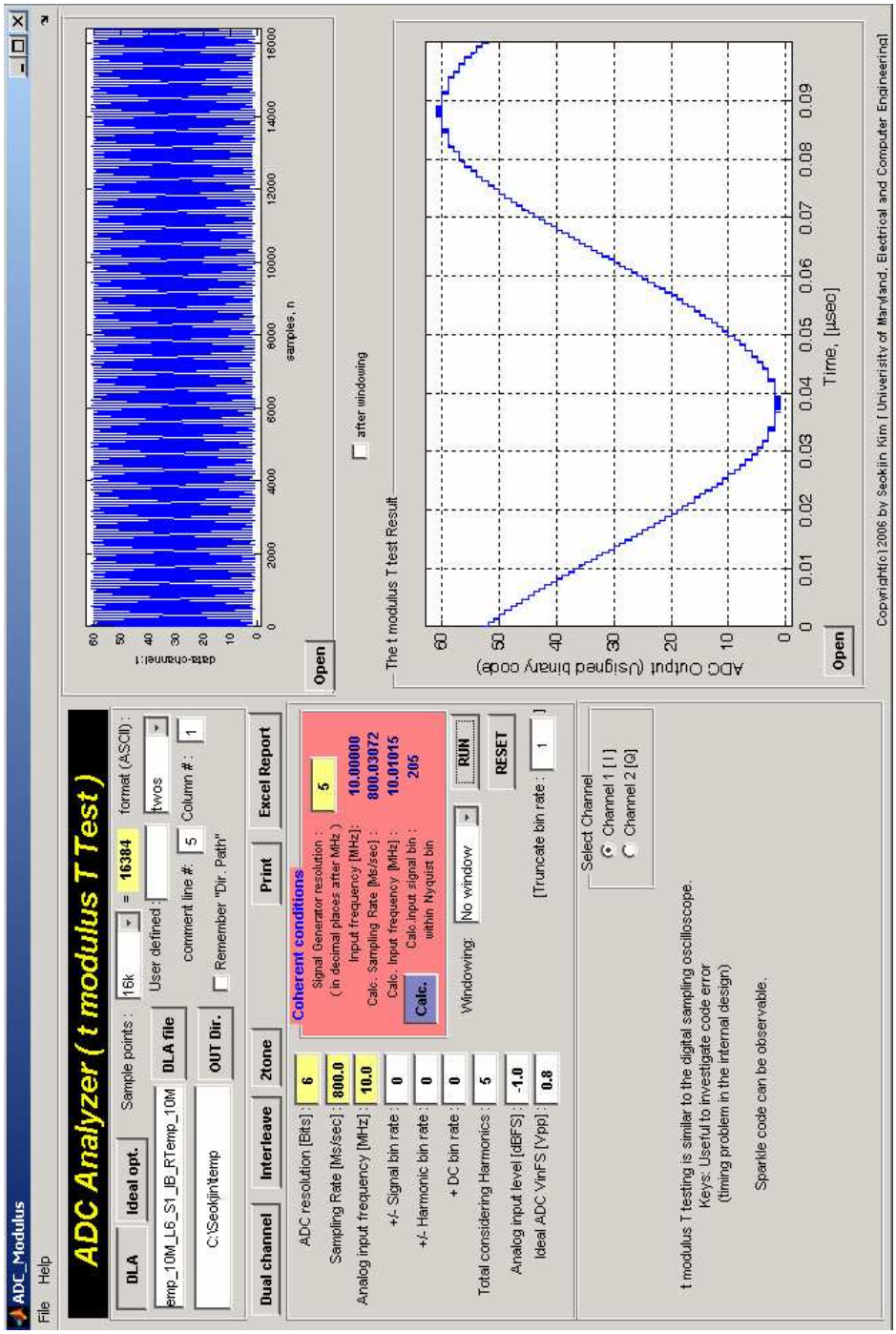



Figure 5.29: VTS time-domain analysis tool: code-error testing module

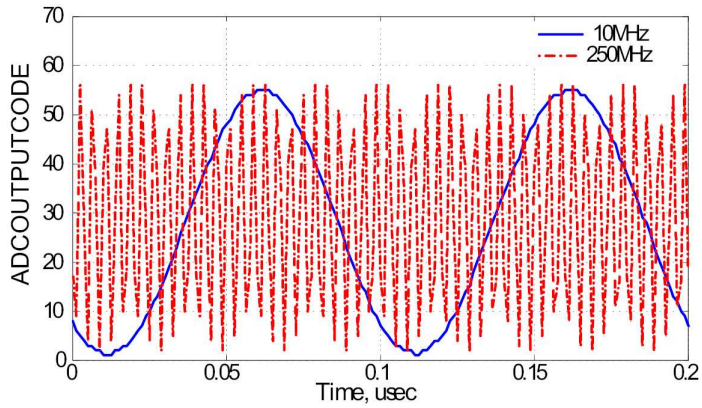



Figure 5.30: Sine wave reconstruction test result: 10 MHz and 250 MHz sine waves are each sampled at 800 MS/s rate.

### 5.4.2 Sine wave reconstruction test

An input sine wave is sampled and reconstructed from the acquired data by the software. This test provides an indicator of basic functionality and it provides a basic path for trouble-shooting and de-bugging. Many logic analyzers have this test already built in. The 10 MHz and the 250 MHz reconstructed sine waves are illustrated in Figure 5.30. The reconstructed input sine wave test provides a measurement of the amplitude of the input signal from the envelope of the acquired sample sets, and the output signal's spectral purity can be assessed by FFT [66].

### 5.4.3 Sine wave code error test

After we reconstruct the acquired sine wave, it is useful to investigate the code errors existing among the sample data sets. This allows us to assess possible timing

problems in the internal ADC designs or in the test fixture. The sine wave reconstruction test result is not the best way to observe possible sparkle codes or timing errors. This is because the waveform will eventually start to show aliasing as the input analog signal frequency increases.

In the sine wave code error test, the acquired sine waveform is tested by plotting the waveform over a single period of the input signal using all the acquired sample points. In this test, also known as the "$t$ modulus $T$ test" performed by the VTS suite [67], the ADC output codes are sent to the computer buffer memory over the acquisition time. Only one period of the waveform is re-plotted by a simple calculation of the sampling time. When the data acquisition time is over one cycle of the input signal, the sample code is stored in the position where the input analog wave form is located in computer buffer memory. Simply, this result shows the overlayed image of the acquired samples into a single period of the input signal waveform to maximize the probability of finding possible sparkle codes or glitches. This procedure is also very similar to the basic operation of a sampling oscilloscope. The one period of the overlay input analog waveform is depicted in Figure 5.31 when 250 MHz sine wave is sampled at 800 MHz with the HNS 6-bit ADC.

### 5.4.4 The fast Fourier transform

The power spectrum is an important tool in data converter characterization [65]. The spectrum is derived by Fast-Fourier transforming data from buffer memory or

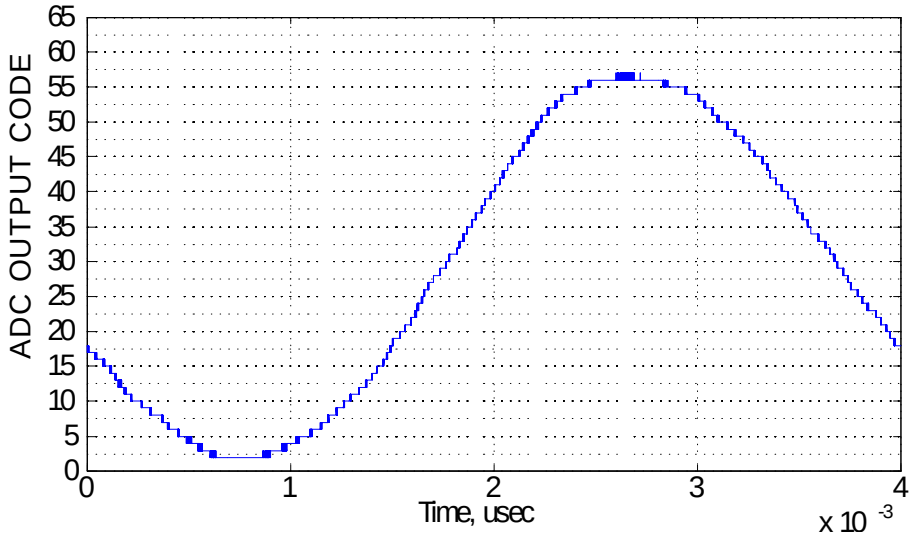



Figure 5.31: Sine wave code error test ('$t$ modulus $T$' test) result: 250 MHz input sine wave is sampled at 800 MS/s rate.

directly from the measurement equipment (such as the digital logic analyzer.) The FFT can capture time-domain signals and measure their frequency content without any digital filtering. However, to perform the FFT-based measurements, one must be aware that the FFT results are usually the result of averaging of an acquired signal over the time interval of the test. Thus, it is easy to analyze the FFT results for a stationary signal like a sine wave. The VTS software ADC parameter calculation blocks are based on a sine wave dynamic input.

The VTS software FFT tests convert a two-sided power spectrum to a single-sided spectrum. It adjusts the frequency resolution, and displays the spectrum in the first Nyquist zone. The power spectrum is discretized and each discrete element is proportional to the amplitude squared of each frequency component. For the case

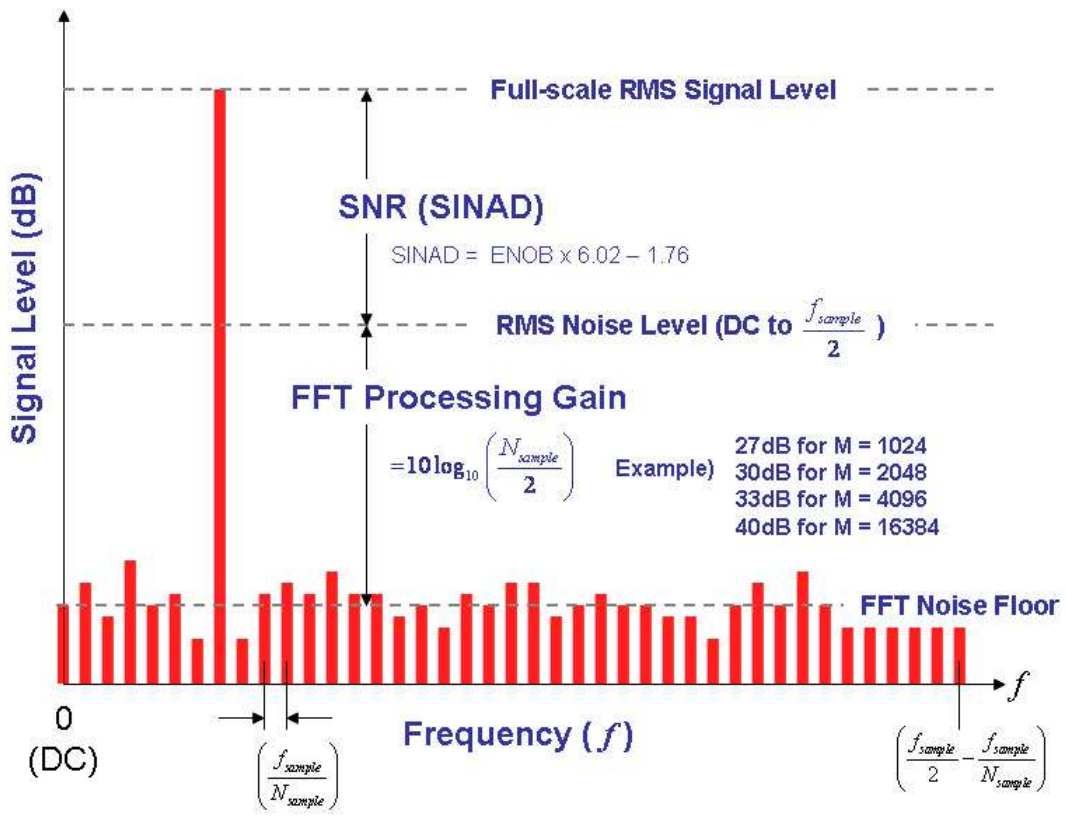



Figure 5.32: FFT output with effects of processing gain

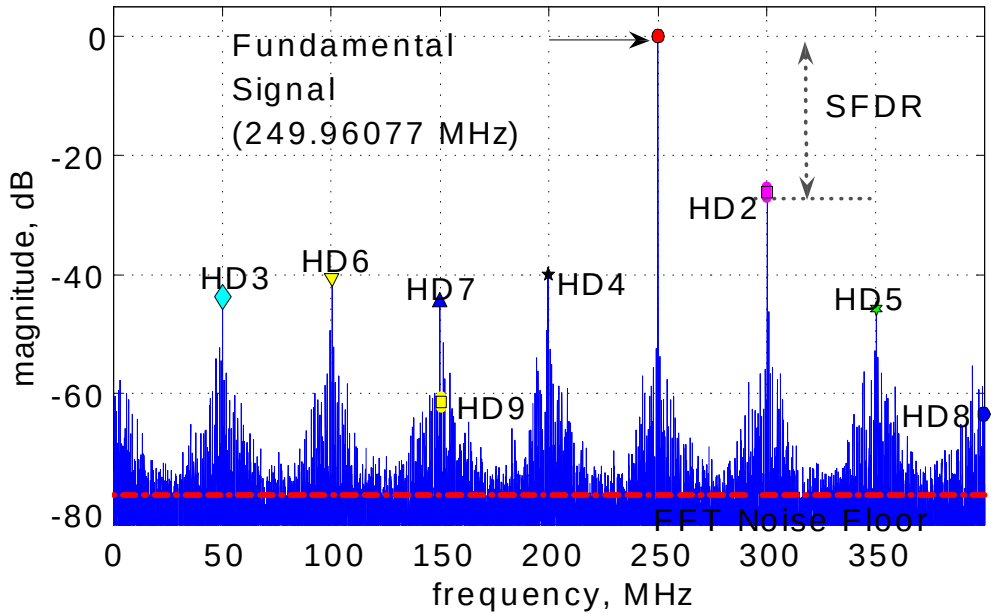



Figure 5.33: Power spectrum FFT result of *Thames* ASIC ADC with 250 MHz Sine wave sampled at 800 MS/s rate

at hand, the calculated FFT result is depicted in Figure 5.33 in which a 250 MHz input sine wave is sampled at 800 Msamples/sec.

The amplitude of each bin in the frequency range is determined by the input sampling clock frequency ($f_{sample}$) and the total acquired data size, $N_{sample}$. This is the same as the number of data records. In the spectral domain display, the number of frequency points is half of the data record, $N_{sample}/2$. For example, a total of 16384 sample points are used in the spectral plot in Figure 5.33. It is important to know that the first frequency bin always represents the DC component of the signal and the last frequency bin is located at $f_{sample}/2$ - $f_{sample}/N_{sample}$.

The magnitude of each spectral bin component is expressed on a dB scale relative to the magnitude of the fundamental signal at -1 dBFS. This is done to avoid a possible clipping over the input analog full scale range, thus maintaining purity of the sine input tone. In a physical test, the clipping of directly monitored by the 'over_range' bit signal. By increasing input power level of the synthesizer slowly from a relatively low level, we easily find when the 'over_range' bit starts to fire.

The test frequency and the actual sampling frequency must be carefully selected since the FFT result is affected by windowing. It must be kept in mind that there exist certain input test tones that can hide ADC errors for any given sampling clock frequency. The optimum input test frequency is the one for which the signal phase can be uniformly distributed between 0° and 360° in the sampling window, $N_{sample}$ (or, over the entire data record). In that way we assure ourselves that we are sampling a periodic signal over an integral number of the signal cycles.

It is important to choose a data record of length sufficient to produce at least one representative sample in each spectral bin [66]. The VTS software has a built-in coherent sampling frequency calculator aimed at providing coherent sampling conditions. It should be noted that the test setup might require a high-resolution signal synthesizer to provide an accurate reading of the input frequency. However, a suitable high resolution signal synthesizer may not be accessible or affordable for volume testing requirements. Therefore, the VTS software adapts the algorithm

which can provide the clock frequency offset from its exact calculated frequency point to overcome such a stringent demand.

For example, the 800 MHz sampling rate with 16384 data record size can determine the bit-resolution of an ADC spectrum which is 48.8281250 kHz. An available signal generator may not offer enough resolution of the calculated frequency with sufficient phase noise margin for both input and sampling frequencies. Our test setup uses a synthesizer with 1 Hz resolution and sets the synthesizer testing resolution at 10 Hz for more stable frequency selections. The coherent sampling condition for this case is when the input is 249.96077 MHz with 800.03072 MHz sampling frequency. The input test spectral bin is located at bin 5119 and the frequency resolution of the FFT spectrum is 48.83kHz in Figure 5.33.

ADC testing techniques are usually based on a spectrally pure sine wave source in which distortion and broadband noise are well below the corresponding ADC figures of merit [13]. Even though the coherent sampling condition is enhanced by the purity of the input sine wave and the accuracy of the generated signal frequency and repeatability of the sampling process, possible DC leakage or spectral leakage must be taken into account. The VTS software algorithm takes these points into consideration. It controls for signal uncertainties and for finite sample record length as well as for test equipment and set-up stability. The algorithm used by the program is based on methods that optimize windowing for the data record at hand [29].

The sine wave FFT test result is analyzed with the VTS suite. The soft-

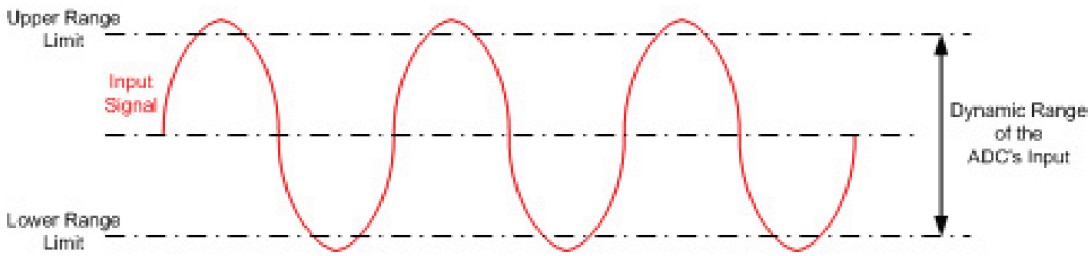



Figure 5.34: ADC Histogram Sine wave input

ware calculates the common ADC dynamic parameters such as a signal-to-noise ratio (SNR), signal-to-noise-and-distortion ratio (SINAD), total harmonic distortion (THD), spurious-free dynamic range (SFDR), and effective number of bits (ENOB) for sine wave as analog inputs.

### 5.4.5 Sine wave histogram test and linearity

The sine-wave histogram test is based on code density test [67]. The frequency of the input signal and clock can be set such that every state of the ADC is tested. The relationship between the input frequency ($f_{\text{Signal}}$) and the clock frequency ($f_{\text{Clock}}$) is given by:

$$f_{\text{Signal}} = f_{\text{Clock}} \times \frac{N_{prime}}{M_{Samples}}, \tag{5.30}$$

where $N_{prime}$ is a prime number (i.e. 2, 3, 5, 7, $\cdots$, 127, $\cdots$, and etc.) and $M_{Samples}$ is the number $2^N$ of data samples.

The code-density model relies on an empirically developed probability distribution to predict the linearity of the converter. A high, frequency stability, low

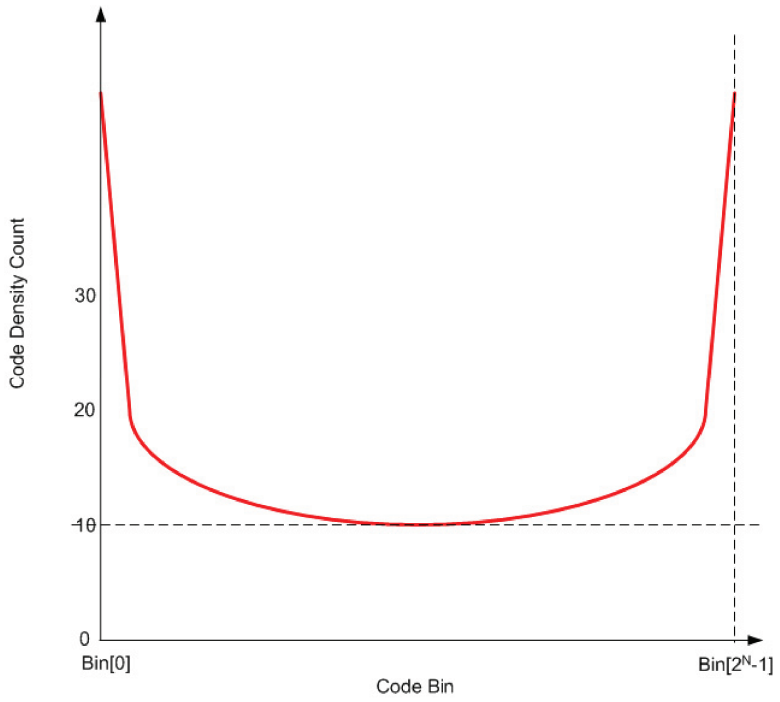



Figure 5.35: Bath tub shape code probability distribution of a sine wave

distortion sine-wave is applied to the input of the converter the amplitude of which exceeds the dynamic range of the input.

As the input signal is now non-linear, the probability of each code occurrence is no-longer uniform. For a sine-wave with peak amplitude A, the probability of a voltage between the two points $V_1$ and $V_2$ is given by the equation[14]:

$$P(V_1 < V < V_2) = \frac{1}{\pi} \cdot \left[ \sin^{-1}\left(\frac{V_1}{A}\right) - \sin^{-1}\left(\frac{V_2}{A}\right) \right]. \tag{5.31}$$

The histogram needs to be normalized to remove the effects of the sinusoidal waveform's non-uniform voltage distribution. The normalization process is complicated because the gain and the offset of the ADC is an unknown. The gain and offset are calculated using the number of hits at the upper and lower codes in the histogram. The mismatch between the two numbers is the offset, whilst the total number of hits relates to the amplitude.

For a converter with a resolution of $N$ bits, the equations that relate the upper and lower hits to the offset (relative to the midscale) and peak amplitude of the sinusoid expressed in terms of LSBs are[23, 67]:

$$C_1 = \cos\left[\pi \cdot \frac{H(2^N - 1)}{M_{Samples}}\right] \tag{5.32}$$

$$C_2 = \cos\left[\pi \cdot \frac{H(0)}{M_{Samples}}\right] \tag{5.33}$$

Where $H(2^N - 1)$ is the number of times the upper code is hit at Bin[$2^N - 1$], and H(0) is the number of times the lower code is hit (at Bin[0]).

$$Offset = \left[\frac{C_2 - C_1}{C_2 + C_1}\right] \cdot \left(2^N - 1\right), \tag{5.34}$$

and

$$Peak = \frac{(2^{N-1} - 1) - Offset}{C_1} \tag{5.35}$$

Once the values of Peak and Offset are known, the distribution of code hits for an ideal sine wave can be calculated, denoted by $H_{sin}$, which would be expected from a perfectly linear ADC excited by a sinusoid:

$$H_{sin}(i) = \frac{M_{Samples}}{\pi} \cdot (\sin^{-1}\left[\frac{(Bin[i]+1) - 2^{N-1} - Offset}{Peak}\right] - \sin^{-1}\left[\frac{Bin[i] - 2^{N-1} - Offset}{Peak}\right]) \tag{5.36}$$

Where $i = 1, 2, \cdots\cdots, 2N-2$, and $H_{sin}(i)$ represents the probable number of hits per code and therefore will not necessarily be an integer.

The width of the $i$-th code word in units of LSB's is calculated by dividing the actual $i$-th code count by $H_{sin}(i)$:

$$CW_{norm}(i) = \frac{H(i)}{H_{sin}(i)} \quad [LSB] \tag{5.37}$$

In the above calculation exclusion of the highest $(2^N - 1)$ and lowest code count (0) is necessary, as these two codes do not have a defined code width. In effect, the end codes are infinitely wide since there are no decision levels above the highest code and below the lowest code points.

A sine wave histogram test is performed in the amplitude domain of a data converter. The input sine wave signal with bathtub distribution is applied to the

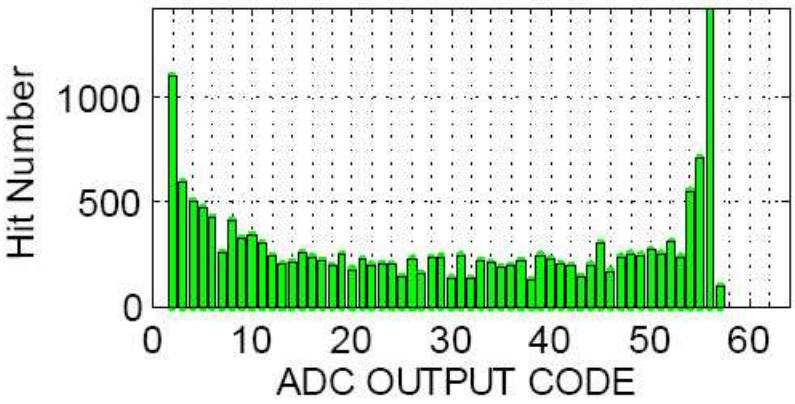



Figure 5.36: Histogram test result based on a code density test: 250 MHz sine wave is sampled at 800 MS/s rate

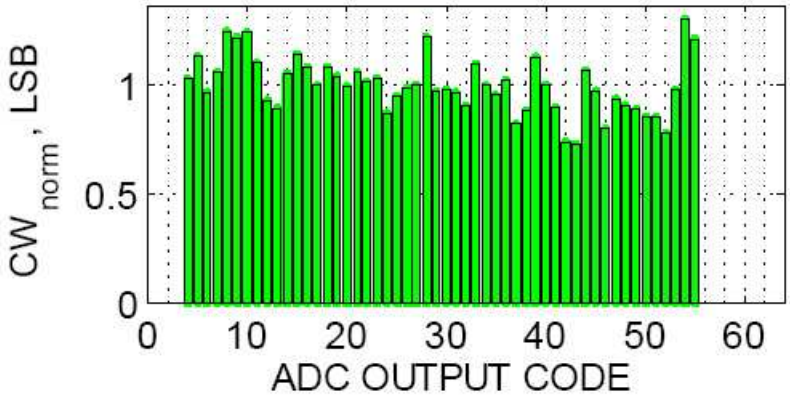



Figure 5.37: Normalized codewidth LSB result from Figure 5.36: 250 MHz sine wave sampling at 800 MS/s rate.

ADC during a histogram test, and the VTS software compares the ideal sine wave histogram to a corresponding distribution of digital codes from the ADC outputs. A converter with a 2's compliment output code should have $2^N - 1$ added to the collected samples to shift them into unsigned binary format. Figure 5.36 shows the sine wave histogram test result when the 250 MHz sine wave is sampled with an 800 MHz sampling clock. The sine wave histogram is directly indicating the code hit numbers and Figure 5.37 shows the normalized code hit numbers which are the normalized code widths for each code in LSB units. From the shown histogram test, the ADC has $-2$ LSB offset error.

#### 5.4.5.1 Differential nonlinearity (DNL)

Once the VTS software finishes calculating the probability of each code for the recorded data array set, the software starts to compare the result with an ideally expected sine wave histogram. As a result, the differential nonlinearity (DNL) can be calculated by taking the difference from the ratio of the measured histogram of samples in each code to the ideal histogram of the expected ideal sine wave histogram for one LSB. That is, the Differential Non-linearity (DNL) error can be calculated in units of LSBs by subtracting one LSB from each code width:

$$DNL(i) = CW_{norm}(i) - 1. \tag{5.38}$$

To ensure the accuracy of the calculation, there must be enough sample points per each code bin. The maximum DNL is 0.299 [LSB] and the minimum is -0.270 [LSB]

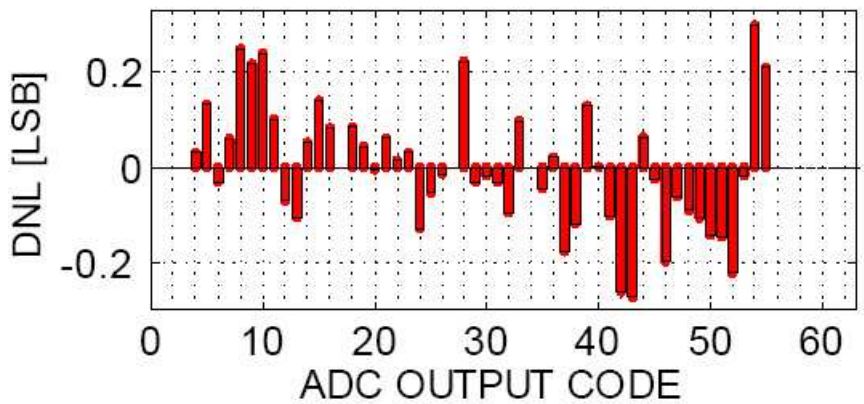



Figure 5.38: Differential nonlinearity result: single channel (I) result with 250 MHz sine wave sampling at 800 MS/s rate

from Figure 5.38.

#### 5.4.5.2 Integral nonlinearity (INL)

The DNL curve can be integrated using a running sum to calculate the endpoint Integral Non-linearity (INL) curve in units of LSBs:

$$INL(i) = \sum_{k=1}^{i-1} DNL(k). \tag{5.39}$$

Errors may be apparent in the plot of INL where the finishing point is not zero. The problem is due to subtracting numbers of near equal size, small errors in measurement and/or round-off error which become highly magnified during the computation [2]. This effect can be compensated for in the INL by taking the average of the DNL vector and subtracting the result from DNL vector prior to calculating

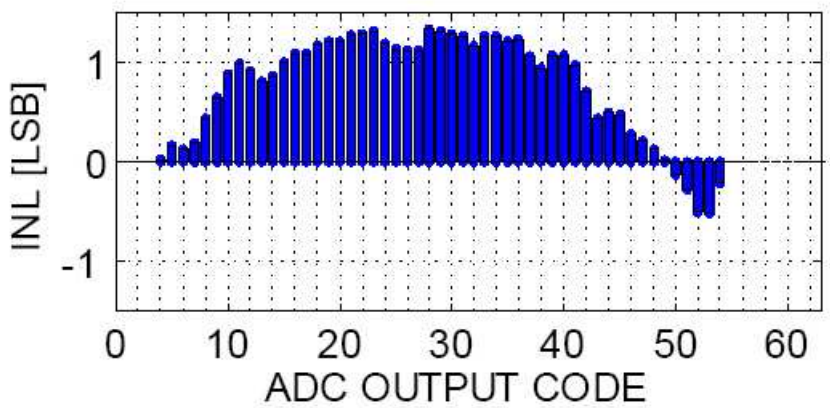



Figure 5.39: Integral nonlinearity result: single channel (I) result with 250 MHz sine wave sampling at 800 MS/s rate

INL. The error correction can be adjusted by:

$$sum = \sum_{i=1}^{i-2} DNL(i), \tag{5.40}$$

$$average = \frac{sum}{i-2}, \tag{5.41}$$

$$avgDNL(i) = DNL(i) - average, \tag{5.42}$$

and error compensated INL values can be obtained:

$$INL(i) = \sum_{k=1}^{i-1} avgDNL(k). \tag{5.43}$$

The integral nonlinearity is within the range from -0.510 to 1.337 [LSB] for the case illustrated in Figure 5.39.

### 5.4.6 Effective resolution bandwidth test

In the effective resolution bandwidth (ERB) test, as with the analog power test, the stimulus of the input variance for testing is the ADC input frequency. The sampling rate and the input power for each frequency point are both fixed during this test. The VTS software analyzes the effective-number-of-bits (ENOB) from the data set for each frequency. The ERB test result is depicted in Figure 5.40.

Note that the sine wave input power level must be re-calibrated for each frequency point since the signal amplitude at the ADC input incurs losses within the test equipment suite. This suite includes coax cables and the test fixtures where the single-to-differential driver, the harmonic suppression filters and the test socket reside. This is a unique and challenging aspect of a high speed ADC testing. High frequency effects in the test fixture and interconnects and in ADC packaging. All interact with each other. Therefore, we must use RF analysis to avoid such parasitic coupling losses.

### 5.4.7 Two-tone sine wave intermodulation test

Two-tone intermodulation distortion (IMD) is measured by applying two spectrally pure sine waves which are relatively close to each other. The amplitude must be chosen not to over-drive the input analog range so that the ADC does not clip when the two tones are added in-phase. The value of the IMD is in dBc relative to either of the two original input tones. The VTS software calculates the values of IMD

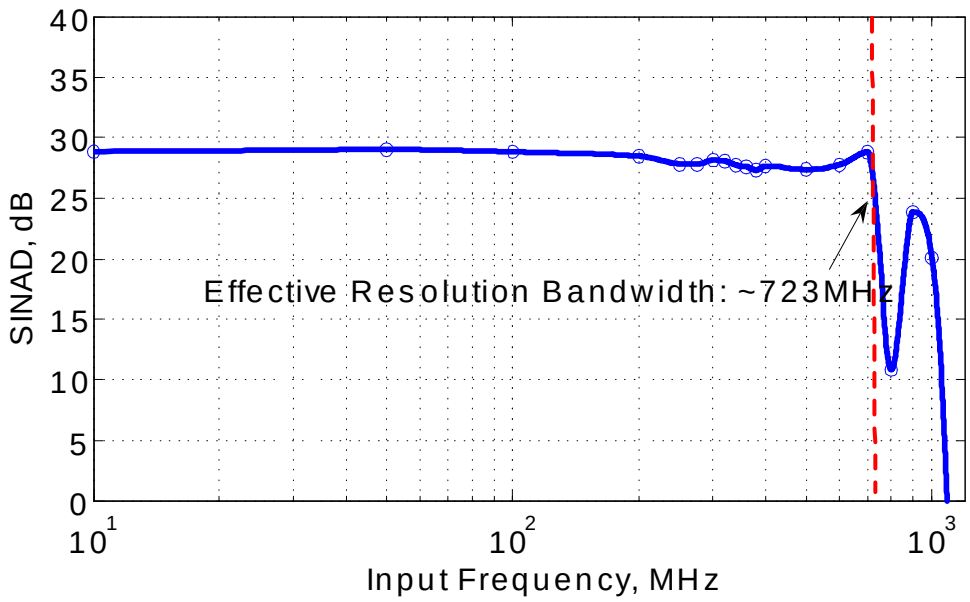



Figure 5.40: Effective resolution bandwidth under 800 MS/s sampling rate

products and displays the spectral domain two-tone FFT result. Figure 5.41 shows the result when 100 MHz and 110 MHz signals are coupled together and sampled by at 800 MHz for the ADC.

#### 5.4.7.1 $IMD_3$ and $IP_3$

In ADC testing, two-tone sine waves are applied to the ADC, and the output is examined by taking spectral plot to find the two-tone $IMD_3$ products. The ratio of each of the tones to the $IMD_3$ products is in the unit of dBc. It is noticeably that $IMD_3$ depends on signal level. If a signal level is too high, it results in excessive distortion, and if a signal level is too low, it is difficult to detect distortions in

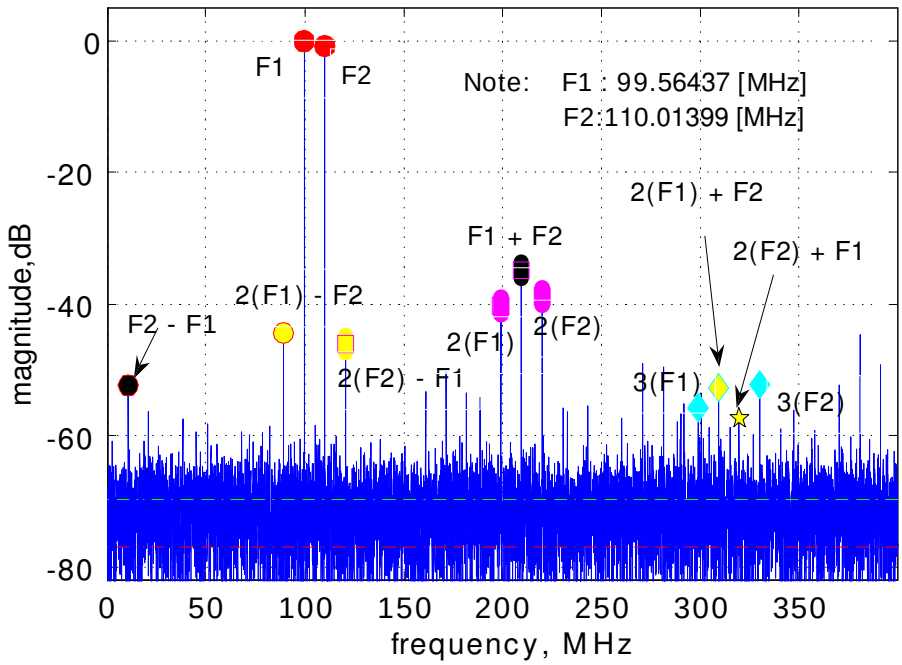



Figure 5.41: Two-tone sine waves (100 MHz and 110 MHz) IMD product test result at 800 MS/s

the presence of nose and among other spurious components. IMD products remain relatively constant regardless of signal level for low level input signals. When the input signal is within a few dB of the exact level of ADC FS range, the IMD may start to increase, but it might not in a very well-designed ADC. Some ADC doesn't show significant increases in the IMD products over FS. However, most ADC will.

The concept for $IP_2$, $IP_3$ is not valid for the designed HNS *Thames*ASIC 6-bit ADC. The distortion products do not vary in a predictable manner as a function of signal amplitude. The ADC behaves a hard limiter as the ADC input level is driving over its full-scale range. That is, there is no 1 dB compression point for the ADC. The ADC suddenly produce extreme amounts of distortion because of input clipping and blew FS, the distortion floor remains relatively constant and is independent of signal level as shown in Figure 5.42.

Two-tone or multi-tone spurious-free-dynamic range (SFDR) specification is the most acceptable way to measure data converter distortion. Two-tone SFDR is characterized in Figure 5.43 for *Thames* ASIC 6-bit ADC at 800 Msamples/sec rate.

### 5.4.8 Analog power test and dynamic range

ADC dynamic parameters can be obtained for each input power level to which the ADC is subjected. The analog power test results are captured by sweeping the output power level of the input sine wave synthesizer while fixing the ADC input frequency and the sampling rate as illustrated in Figure 5.44. The VTS software

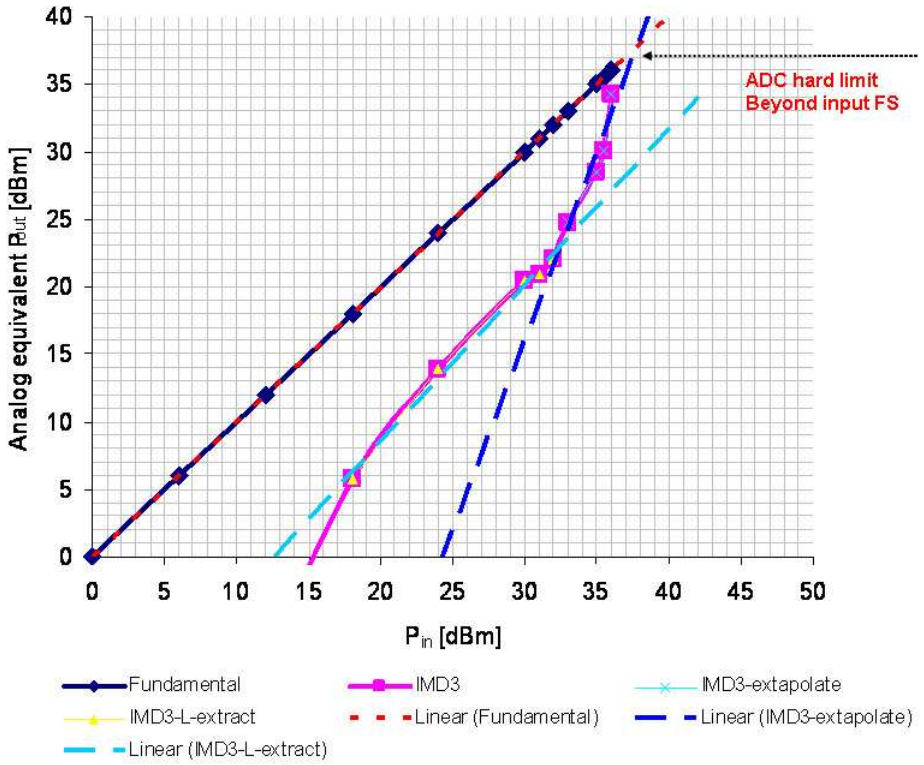



Figure 5.42: Intercept points for *Thames* ASIC ADC: Hard limiter-When the input signal is within a few dB of the exact level of ADC FS range, the IMD starts to increase.

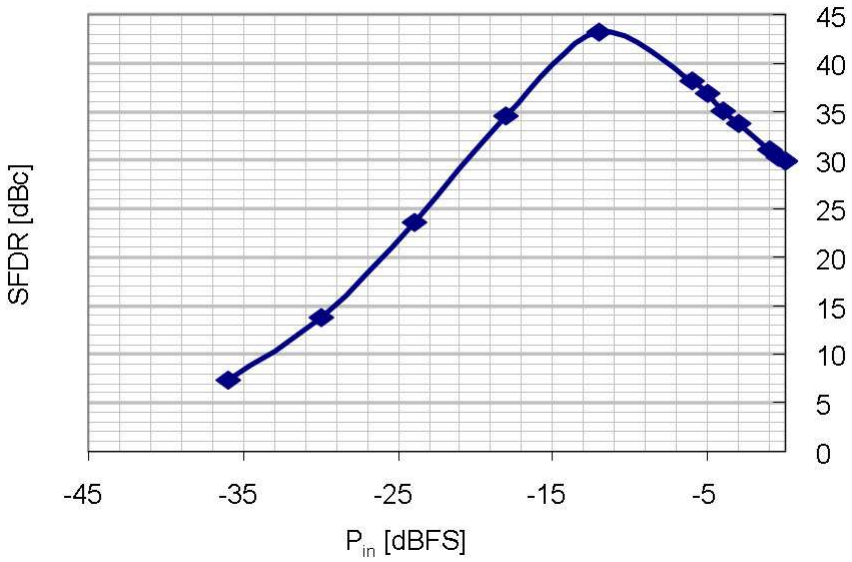



Figure 5.43: Two-tone (100 and 200 MHz) spurious free dynamic range characteristics for *Thames* ASIC ADC (800 MS/s)

analyzes each data set and calculates the signal-to-noise-and-distortion (SINAD), the spurious-free-dynamic-range (SFDR), the effective-number-of-bits (ENOB), total harmonic distortion (THD), and the amplitude of each harmonic. Figure 5.45 shows the SINAD versus input power. The calculated ENOBs for the input power levels (compensating the fact that the input signal is below full-scale range) are illustrated in Figure 5.46 based on Eqn.( 5.44) from Eqn. (5.26):

$$\text{ENOB} = \frac{\text{SINAD} - 1.76 + L_S}{6.02}, \tag{5.44}$$

where $L_S$ is the level of the sampled signal in units of dB.

By analyzing through the VTS, Figure 5.47 depicts SFDR versus input power for cases when the input frequency is at 10, 100, and 200 MHz each.

### 5.4.9 Testing in the temperature extremes

ADC testing is mostly performed at room temperature (25 $°C$). However, the temperature extremes of operation ($-40$ $°C$ and 80 $°C$)have also been investigated. We have verified that these temperature extremes do not affect our test socket reliability and full temperature range measurements are possible with our setup. The calculated ENOB is 4.99 and 3.35 bits for $-40$ $°C$ and 80 $°C$, respectively, for a 250 MHz sine wave input.

The Tenney JR. temperature control bench-top chamber (manufactured by Thermal Product Solutions(TPS)) is used for temperature extreme tests. Note that when testing in the temperature in a lower/higher temperature than a room

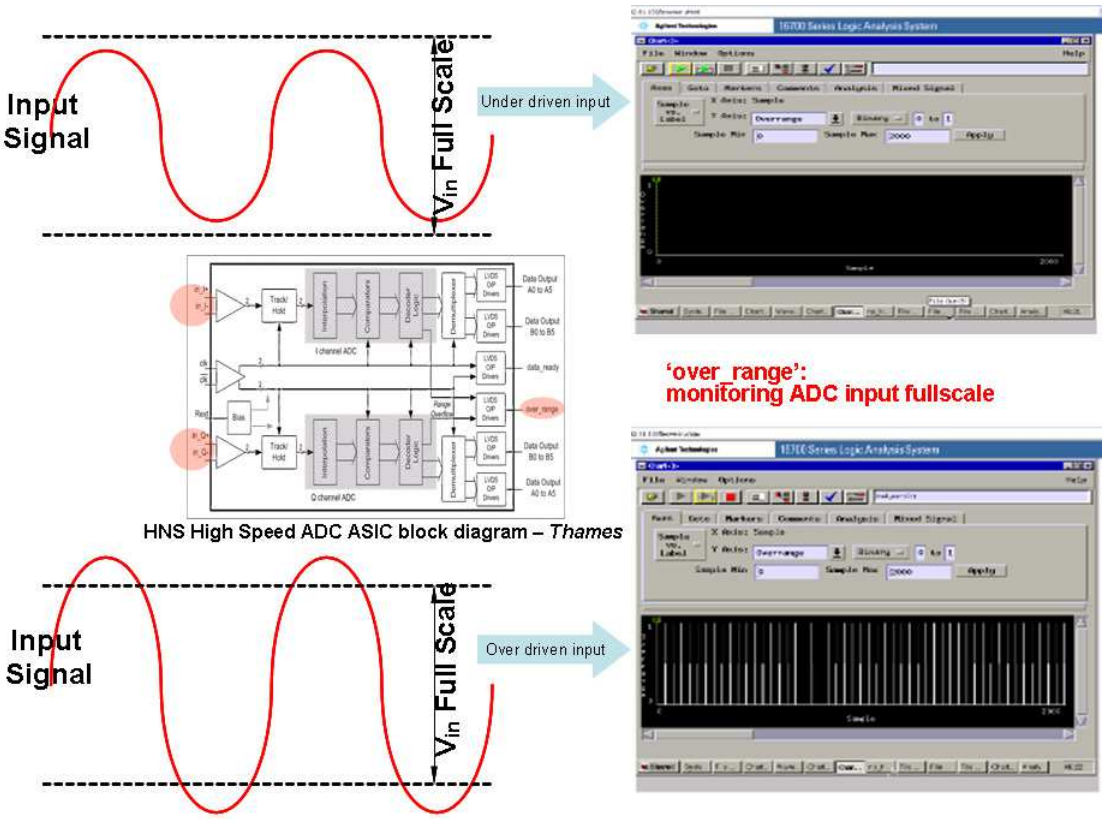



Figure 5.44: *Thames* ASIC ADC analog power testing calibration: ADC input analog power level is calibrated by monitoring 'over_range' pin out signal. Fist, drive ADC analog input power adjusting at lower level and gradually increasing while continuously capturing the digital bitwise outputs and 'over_range'. Once, the pin-'over_range' is toggle, then that's the maximum ADC analog input power level.

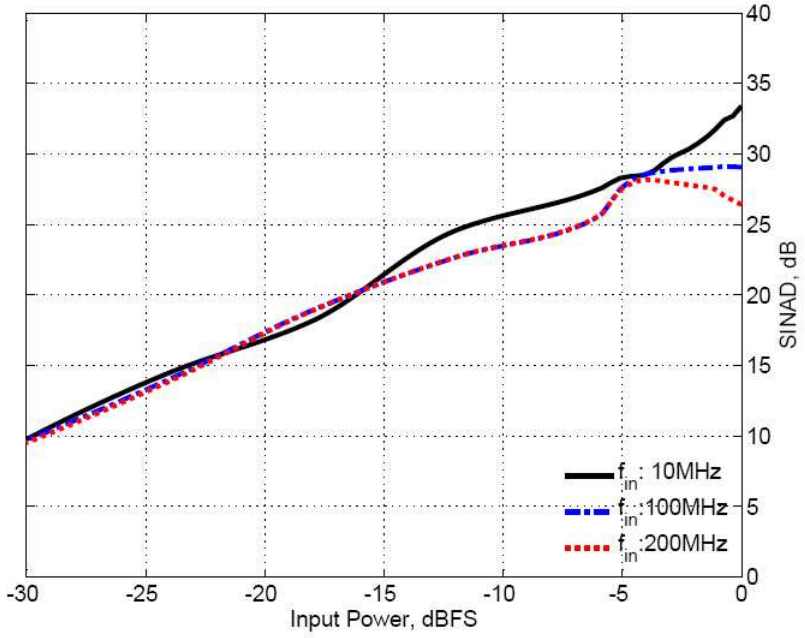



Figure 5.45: Signal-to-noise-and-distortion (SINAD) to ADC analog input power: ADC is operating at 800 MS/s sampling rate

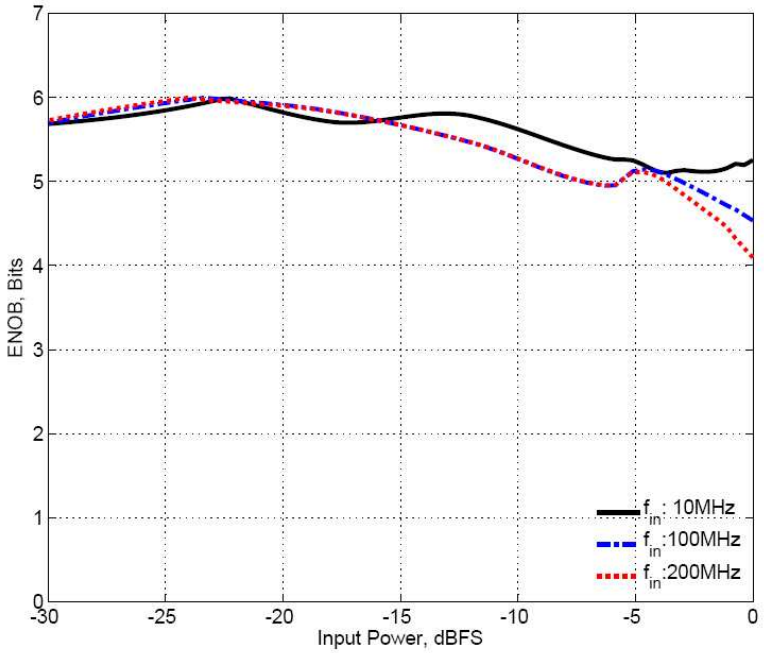



Figure 5.46: Effective-numbers-of-bit (ENOB) to ADC analog input power: ENOB is calculated from full-scale SINAD using the Eqn. (5.26). If the input signal is less than the full-scale, Eqn. (5.26) must be corrected as Eqn. (5.44) in order to compare it to the ENOB value predicted by the input sinewave power level.

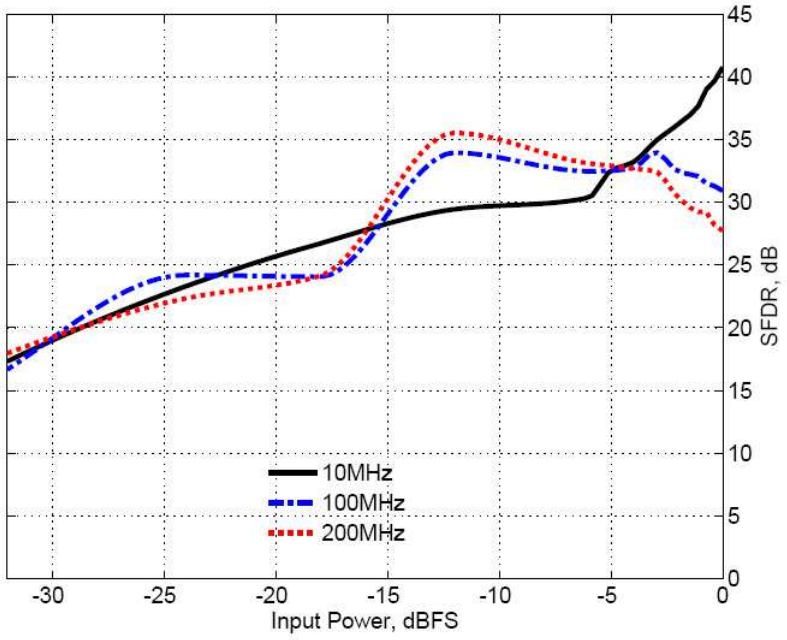



Figure 5.47: Spurious free dynamic range (SFDR) characteristics for *Thames* ASIC analog input levels

temperature, it requires to wait the temperature goes back to a room temperature again before opening the chamber to modify the test fixture.

## 5.5 Production tests

Time is money, especially when a design comes to its final production stage. A high-performance tester may cost several million dollars, depending on its configuration. Probers and handlers may approach the million dollar mark. Providing services and production personnel further drives the cost higher. This is why testing is an expensive business.

The *Thames* chip final production testing can be directly extended from its proto-type verification test by using developed test fixture and test program (VTS suite). The following production test specifications can provide clear references to both the design engineer and the ASIC vendor for the full production.

In this section, check-up lists are provided for developing a mainframe ATE equipment design to minimize ADC test time and cost, and to maximize overall product throughput. High-speed ADC production testing is divided into three major sections: DC, static, and dynamic (RF) tests. The *Thames* required tests are listed in Table 5.2. Recommended tests for wafer level or final assembly (package) test are denoted by an ✓.

Table 5.2: High-speed ADC tests - wafer and final production

| Test | Wafer | Final |
|---|---|---|
| ESD and Continuity Checks | | ✓ |
| Supply Current | ✓ | ✓ |
| Quiescent Voltage: Inputs | ✓ | ✓ |
| Input Full Scale (Over_range) | ✓ | ✓ |
| Input Full Scale (Under_range) | ✓ | ✓ |
| LVDS driver output logic level | | ✓ |
| Input offset | ✓ | ✓ |
| 'OVER_RANGE' output parameters | | ✓ |
| 'DATA_READY' Test | | ✓ |
| Code Density Test: Low frequency | | ✓ |
| ENOB Test: Low frequency | | ✓ |
| Code Density Test: High frequency | | ✓ |
| ENOB Test: High frequency | | ✓ |

### 5.5.1 Continuity($I_{DDQ}$) test

A normal foundry test procedure can be adopted for the *Thames* chip continuity testing. The continuity test (or IDDQ test) with known ESD-connections is allowing detection of non–catastrophic defects mostly in digital logic[23, 68, 69]. An $I_{DDQ}$ test configures all the gates in a CMOS device into a static digital state and then measures the tiny current leakage from power to ground, especially after the ADC is shocked by the electrostatic-discharge(ESD) or electrical over stress(EOS). That is, excessive $I_{DDQ}$ current indicates one or more resistive defects between power and ground that may or may not be detectable as a catastrophic failure in the operation of the DUT. Therefore, $I_{DDQ}$ testing result can the semiconductor wafer fabrication to monitor its process to detect and correct problems quickly and effectively.

## 5.6 Test result summary

As addressed earlier, the dynamic performance of the ADC is critical for a modern communication systems. Most of the dynamic test results presented here are gathered by our VTS software suite through FFTs. Single tone ADC testing characterizes the ENOB, SINAD, SNR, SFDR, THD, and the INL and DNL of the device. In addition, the analog power test and the effective resolution bandwidth (ERB) test yield several important parameters of the ADC. The tested ADC performance versus input power level is shown from Figure 5.45 to Figure 5.47 for cases when the input frequency is at 10, 100, and 200 MHz each. The results suggest that the ADC under test operates most linearly when the input power level is below 5 dBFS.

As the input approaches the full-scale range, the tested ADC exhibits more nonlinear behavior. The analog power testing result can be used as a way to select the optimum power level for each input frequency at the same sampling rate as shown in Figure 5.45. The maximum operating frequency characteristics of the ADC are derived from the ERB test result shown in Figure 5.40. The ERB of the ADC is the 3-dB bandwidth of the SINAD versus the frequency and the tested ADC rolls off at about 723 MHz with an 800MHz sampling rate. This tells us how the performance of the ADC degrades as the test frequency increases.

The single-tone FFT testing result provides the SFDR that is calculated from the ratio of the strongest spurious signal power to the desired signal power. The

Table 5.3: Summary of HNS 6-bit Dual Channel ADC at room temperature ($25°C$).

| **Frequency** | **10 MHz** | | **100 MHz** | | **200 MHz** | | **250 MHz** | |
|---|---|---|---|---|---|---|---|---|
| **Channel** | **I** | **Q** | **I** | **Q** | **I** | **Q** | **I** | **Q** |
| **ENOB** [Bits] | 5.62 | 5.40 | 4.60 | 4.43 | 4.08 | 3.95 | 3.82 | 3.81 |
| **SINAD** [dB] | 34.55 | 33.58 | 28.43 | 27.72 | 25.37 | 24.80 | 25.56 | 23.96 |
| **SNR** [dB] | 35.68 | 35.81 | 34.83 | 34.91 | 33.66 | 33.72 | 33.11 | 32.95 |
| **THD** [dB] | -41.89 | -38.18 | -29.63 | -28.87 | -26.13 | -25.41 | -25.27 | -24.56 |
| **Offset** [LSB] | -2.2 | -1.0 | -1.8 | -0.9 | -1.0 | -0.3 | -0.5 | 0.4 |
| **INL**$_{MAX}$ [LSB] | 0.45 | 0.88 | 0.86 | 0.98 | 1.85 | 1.34 | 2.01 | 1.76 |
| **DNL**$_{MAX}$ [LSB] | 0.21 | 0.28 | 0.26 | 0.28 | 0.33 | 0.29 | 0.13 | 0.35 |

second harmonic of the sampled analog input signal is the most significant source limiting the SFDR in the target example ADCs. As a result, the SINAD is degraded and limits the channel capacity in systems applications [70]. In a modern communication systems, the SINAD (or SNR) is the the most important factor affecting the the received or transmitted data. The SFDR is also an important indicator of quality in digital radar applications [71], since spurious signals present themselves as false targets.

The majority of measurements are made within the target signal bandwidth ($10 - 250$ MHz) to verify the performance of the dual channel 6-bit HNS ADC. The summarized test results are shown in table. 5.3 for 10, 100, 200, 250 MHz. However, as shown in Figure 5.40, the ADC is characterized fully up to a 1.2 GHz input single-tone frequency while the sampling rate is fixed at 800 MHz.

It found that the code error test is useful to determine the presence of the timing error from the ADC and/or the test fixture. When the timing error is determined, the VTS software can easily identify poor spectral response and an unacceptable ENOB, SINAD, and SFDR parameter set. As shown in Figure 5.31, the sparkle code is normally not observed during tests, but there are still some glitches that appear when the ADC codes are close to one another.

This chapter with a comparison of the VTS suite with "competitor" approaches as summarized in Table 5.4:

When a design is first released to production, the new product undergoes a characterization process to determine whether or not it meets the customer's requirements or the design specifications. The first-pass design often has problems that must be corrected before a final version of the design can be released to production. In order to produce a production-worthy design in a short time-frame, characterizing the design IC performance and diagnose internal circuit problems are concurrently managed and planned from the initial design process using proper DfT concept. The VTS suite and the test fixture is ready for the production testing.

In order to develop cost effective mainframe high-speed ADC ATE equipment in the production, the final check-up lists are reviewed and leads to high-speed ADC mainframe ATE equipment design to minimize ADC test time and maximize overall product throughput in this chapter.

Table 5.4: VTS suite vs. other program

| Features | VTS | Competitor |
|---|---|---|
| **Coherent Calculator** | Yes | Yes |
| **Sine-wave Reconstruction** | Yes | Yes |
| **Code error test** | Yes | No |
| **Single-tone test** | Yes | Yes |
| **Two-tone test** | Yes | No |
| **Leakage handling** | Yes | No |
| **Windowing functions** | more than 4 functions | 1 or 2 functions |
| **General ADC evaluation** | Yes | No |
| **Ideal ADC evaluation** | Yes | No |
| **PDF print** | Yes | No |
| **MS Excel report** | Yes | No |
| **ATE adaptive** | Yes | No |

# Chapter 6

# Sensitivity Analysis on High-speed ADCs: Corner Lot Study

## 6.1 Overview

In a perfect world, where silicon integrated circuit(IC) fabrication process would be perfectly predictable, all IC chips would meet their predicted design parameters. Every chip would be absolutely identical, no variations exist from wafer to wafer, or lot to lot. Ideally, all chips would run perfectly at the designers' intentions. However, we do not live in such a wonderful paradise. Silicon fabrication processes vary, sometimes widely, and in ways that are unpredictable.

Corner lots defines a wafer fabrication where the process is deliberately skewed to produce either fast, or slow wafers so that ASIC performance can be physically

evaluated at process extremes [3]. Limited numbers of test samples require skew part to be used in testing [24]. In deep-submicron designs, especially for temperature and power sensitive designs, major integrated circuits need to be tested for their process corners.

There are a number of studies commonly employed to evaluate the sensitivity of integrated circuits, due to the statistical variations in the processing parameters [30, 72, 73]. Corner or Monte Carlo statistical simulations are sometimes efficient methods to determine the impact of process variation in custom analog and mixed-signal designs [74].

Along with the allowed voltage and temperature range in ADC design verification tests, the impact of allowed process variations on the product performance must be carefully considered. Actually, proper accounting of process variations often enhances design effectiveness allowing us to achieve high yield designs and short design-turn-around-time, simultaneously.

Dynamic performances of high-speed (800 MS/s) dual channel 6-bit analog-to-digital converters (ADCs) were investigated on the corner lot process variation here. To determine the impact of process variations and to analyze the sensitivity of the ADCs to critical process parameter variations, the method used in this chapter is to fabricate the ADC by skewing some critical parameters that are monitored in-line and affect the ADC performance in a dominant manner.

Conventional statistical simulations of worst-case corner analysis [30, 72, 73]

cannot be applied to HNS *Thames* high-speed custom ASIC ADC designs and verifications because of the prohibitive long-run times and lack of accuracy. In order to ensure robust ADC chip designs and verifications for productions, it is crucial to assess the impact of these process variations on the ADC performance.

## 6.2 Process variations

Most of foundry process design kits (PDKs) provide device simulation models contain two kinds of statistical variations:

- Global variations
- Mismatch variations.

Global statistical variations account for variations in device characteristics from chip-to-chip, wafer-to-wafer, and lot-to-lot over the lifetime of production. Mismatch statistical variations account for the variations in device characteristics within a chip [76].

### 6.2.1 Global variations

Many technology and device parameters are monitored during the fabrication of chips through the device structures in dicing channels between the chips (kerf). These kerf parameters help the manufacturing engineers keep the line on or near target [5]. A subset of these monitored parameters across all the supported devices

or structures in a design are chosen as critical parameters and are part of wafer acceptance criterion. The monitored parameters have target nominal values, but can lie anywhere in the range between the upper limit (UL) and the lower limit (LL). Manufacturing control strives to bring all of these parameters near their target values. The device models approximate the global random variations in the process and device parameters (including chip-to-chip, wafer-to-wafer, and lot-to-lot variations) using Gaussian statistical distributions with the target value as the mean and the UL and LL as 3-$\sigma$ limits. ($\sigma$: the standard deviation.) This is expected to represent the long-term statistical behavior of the parameters.

Many device model parameters are defined in terms of the physical process parameters, such as dimensional biases, layer thicknesses, sheet resistances, and so on. The targets and the variations of these process parameters (referred as skew parameters) are assumed to have Gaussian distributions. Individual models refer to this skew profile, so device parameters vary in accordance with these statistically defined skew parameters. The characteristics of the devices that share any of the statistically varying skew parameters get correlated automatically during statistical simulation because of this formulation. The details of the skew parameters that affect different devices are given in the model reference guide that is supplied with the design kit [33].

### 6.2.2 Mismatch variations

Devices drawn identically on a chip have subtle variation in their characteristics, referred to as device mismatch. Through component characterization, records component matching statistics. These statistical variations are defined in such a way as to allow them to be fed as input to iterative Monte-Carlo based simulation [73, 72]. The standard deviations of the mismatch parameters are extracted from measurements on identically drawn, adjacent devices. "Corner lot" hypothesis testing provides "confidence levels" for the validity of this simulation.

The skew parameters are also defined as a function of some corner parameters that are used as handles to vary the characteristics of the different types of devices relatively independent of each other.

### 6.2.3 Corner lot definition

Corner lot defines a wafer fabrication where the process is deliberately skewed to produce either fast, or slow wafers so that ASIC performance can be physically evaluated at process extremes. A statistical data analysis is used in a corner lot study and the result can improve the process.

In a corner lot study, design parameters are set to produce either slow (high resistance, high capacitance, low-$g_m$ or $\beta$) or fast performance (low resistance, low capacitance, high-$g_m$ or $\beta$). the study can be combined with a skew analysis, which not all parameters track in the same direction during a fabrication processing. the

skew parameter tries to accommodate this effect. Monte-Carlo analysis is used to study the process by introducing a random mismatch between components. This mismatch usually has a pre-defined spread and distribution shape. Note that as a minimum, all foundry supplied design kits should contain corner models. However, not all design kit will be capable of skew and parametric analysis.

## 6.3 *Thames* ASIC corner lot study

Corner lot study involves skewing process parameters, device parameters, or both to some predetermined extreme values. The advantage is that it provides an overall answer to the designer's question about whether or not the circuit will function under process extremes.

Conventionally, study of corner lots involves the use of two predefined sets of device models: high-performance and low-performance models. These could refer to high sampling rate vs. "nominal sampling" rate, or high frequency vs. low frequency, etc. These represent the extreme ranges of the processing technology. The high and low device models are developed in turn by defining an objective system-level parameter set and then skewing the device model parameters to their extreme limits observed in production hardware in a way such that the objective system-level parameter exhibit its full range variations. For example, defining the target as the characteristic time-constant of an analog circuit results in skewed device parameters for the fast case that maximizes active device currents, and otherwise

minimizes capacitances and resistances.

The corner lot test results can be applied to a number of types of simulations. However, there are difficulties in actual application. Those specific combinations of model parameters do not always yield the extremes in system-level performance for all types of analog/mixed-signal applications in complex technologies having several types of devices. This means that the simulation results obtained using this quick method could be inaccurate. This affects our ability to study how performance is impacted by a single parameter variation.

An Alternating approach is to actually fabricate the ADC and intentionally skew some critical parameters that are monitored in-line and affect the ADC performance. We thus experimentally determine which parameter fluctuation eliminates system-level performance.

To decide the critical parameters, consider the fact that ADC dynamic specifications such as effective-number-of-bit (ENOB), signal-to-noise-and-distortion ratio (SINAD), total-harmonic-distortion (THD), and spurious-free-dynamic-range (SFDR) are extracted from ADC dynamic performance test [28, 26, 29]. The performance of input buffers, track-and-hold amplifiers and comparators are based on differential bipolar junction transistor (BJT) amplifiers for the *Thames* chip studied here. These, in turn, are dependent on the process-induced variation of BJT-$\beta$ values and emitter areas. Poly-resistor values for the ladder voltage references are also expected to depend on process, and the extremes of these "corner" process

Table 6.1: *Thames* ASIC corner lot process variation condition

| Corner Lot Split | REpoly Rsheet | RNpoly Rsheet | BJT-$\beta$ | BJT Emitter Area |
|---|---|---|---|---|
| **1** | Normal | Normal | Normal | Normal |
| **2** | High | High | Normal | Normal |
| **3** | High | Low | Normal | Normal |
| **4** | Low | High | Normal | Normal |
| **5** | Normal | Normal | High | High |
| **6** | Normal | Normal | High | Low |
| **7** | Normal | Normal | Low | High |
| **8** | Low | Low | Low | Low |
| **9** | High | High | High | High |

All parameters were varied ±10% from nominal for the corner lot fabrication. This is less than the 3-$\sigma$ variation used in the device simulations (about ±10%).

variations contribute to quantization error.

The ATMEL AT46000 process design kit (PDK) [33] states that the majority of the components in AT46K device library include corner parameters as well for simulations. Since the ADC has a common flash type architecture, the passive components are primitive resistors such as REpoly(emitter poly resisitor, 210Ω/sq) and RNpoly(poly resisitor, 150Ω/sq) and the PDK statistics can serve as a starting point for an accurate corner lot study. Other active circuits are employed with bipolar transistors which has the process variations of BJT-$\beta$ values and emitter areas. The complete corner process variations are summarized for *Thames* ASIC in Table 6.1. All parameters were varied ±10% from nominal for the corner lot fabrication. This is less than the 3-$\sigma$ variation used in the device simulations (about ±10%). However, anything more would be impractical for the *Thames* fabrication. That is, given the additional variation in processing, there would be too many system-failure.

## 6.4 Test description

The corner lot evaluation of the *Thames* ASIC is divided into two sections: a DC test section and a dynamic performance test section. All tests are performed using the custom-designed test fixture which described in Chapter 4. The test fixtures includes DIB evaluation board, and socket which enable multiple samples to be tested in the same environment without the need to solder each sample to the testing fixture evaluation board.

### 6.4.1 Test requirements and setup

For testing, the following extreme lot corners must be fabricated (as summarized in Table 6.1). Corner lot samples of The *Thames* are fabricated in 9 different splits which consist of total 25 wafers and 24 lots, varying 4 process parameters. For Lot 1: all parameters nominal case; for Lot 8: all parameters low case; and for Lot9:all parameters high case, each. The complete lot reference follows in Table 6.2.

Go/NoGo wafer-level probe tests were done first. These probe tests consist of continuity and $I_{DDQ}$ tests[23]. Wafer yield maps are shown in Figures 6.1, 6.2, and 6.3. These maps display the locations of failing die on each tested wafer in a production lot. Unlike general lot summaries that only show the number of devices that fail each test category, wafer maps can show the physical distribution of each failure category.

Test-setup and test methodology for the ADC corner lot study are consistent

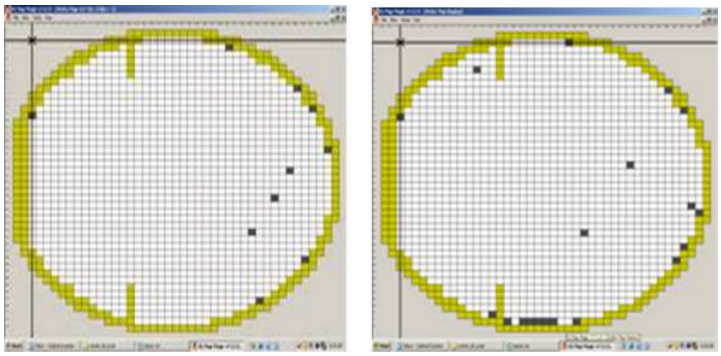
Table 6.2: HNS *Thames* ASIC corner lot split, designation, and variation condition

| Corner Lot Split | Wafers | Lot Designation | REpoly Rsheet | RNpoly Rsheet | BJT-$\beta$ | BJT Emitter Area |
|---|---|---|---|---|---|---|
| **1** | 1, 10 | A, J | Nominal | Nominal | Nominal | Nominal |
| **2** | 2, 11, 19 | B, S | High | High | Nominal | Nominal |
| **3** | 3, 12, 20 | C, L, T | High | Low | Nominal | Nominal |
| **4** | 4, 13, 21 | D, M, U | Low | High | Nominal | Nominal |
| **5** | 5, 14, 22 | E, N, V | Nominal | Nominal | High | High |
| **6** | 6, 15, 23 | F, Z, W | Nominal | Nominal | High | Low |
| **7** | 7, 16, 24 | G, P, X | Nominal | Nominal | Low | High |
| **8** | 8,17, 25 | H, Q, Y | Low | Low | Low | Low |
| **9** | 9, 18 | I, R | High | High | High | High |

with methods in Chapter 4 and 5. The ADC test equipment list contains: (1) *Thames* high-speed ADC evaluation board (test fixture), (2) two dual DC power supplies (HP/Agilent E 3631A), (3) three RF signal generators (HP 83712A, 8657B, and Agilent ESG-2000A), (4) 2 Gs/s digital oscilloscope (Tektronix TDS-540), (5) digital logic analyzer and high-speed module (HP/Agilent 16702B and AT16760), (6) differential LVDS probe with flying leads (Agilent E5381A), (7) temperature chamber (Tenney), (8) multimeter (voltmeter), (9) various arrorted cables such as RF, serial PC, LAN , power supply cables, and differential and single-ended oscilloscope probes, DC block with SMA connectors, etc.

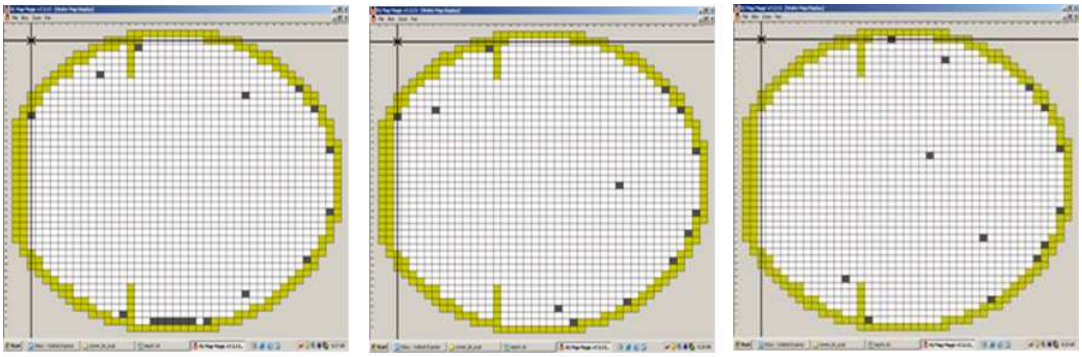
## 6.5 Test results

30 parts from each of the 9 corner splits were packages (total 270 ADC samples for studying corner lot) and tested at room, hot(+80°$C$) and cold(-40°$C$) temperature.



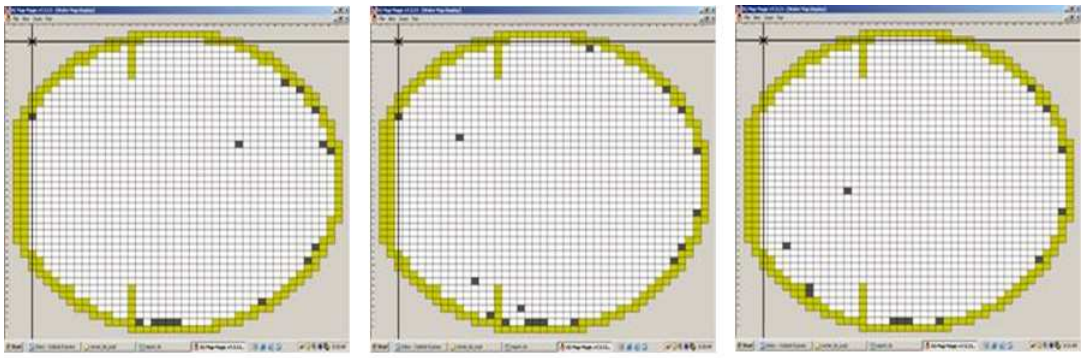
WAFER 1 WAFER 10

(a) Split 1



WAFER 2 WAFER 11 WAFER 19

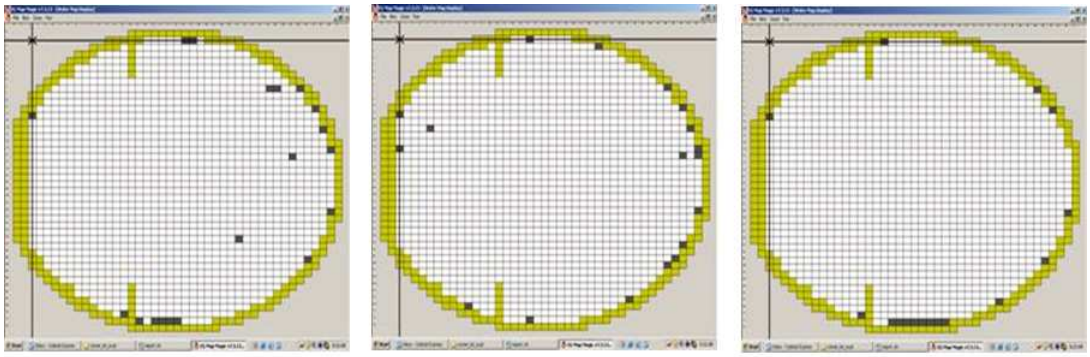
(b) Split 2



WAFER 3 WAFER 12 WAFER 20

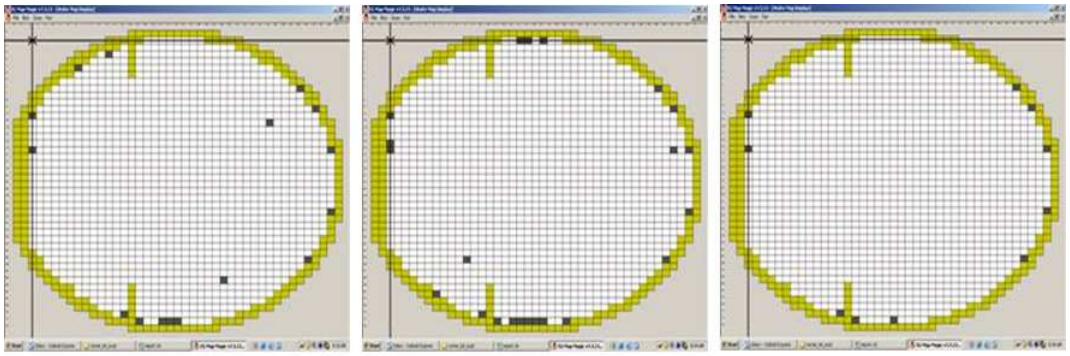
(c) Split 3

Figure 6.1: HNS *Thames* ASIC corner lot split 1, 2, and 3: black squares are failed dies during "Go/NoGo wafer-level probe tests for continuity and $I_{DDQ}$ [23]



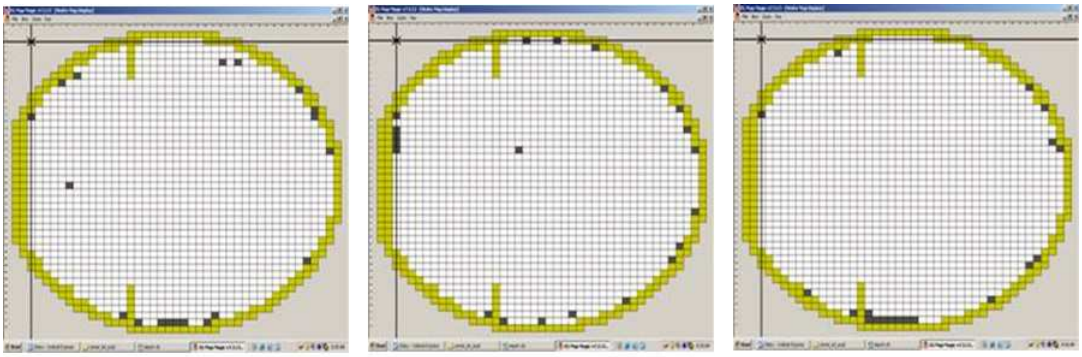
WAFER 4 WAFER 13 WAFER 21

(a) Split 4



WAFER 5 WAFER 14 WAFER 22

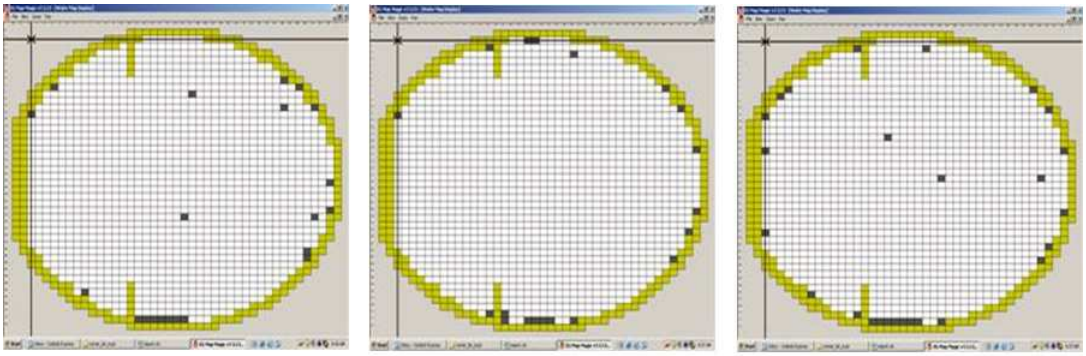
(b) Split 5



WAFER 6 WAFER 15 WAFER 23

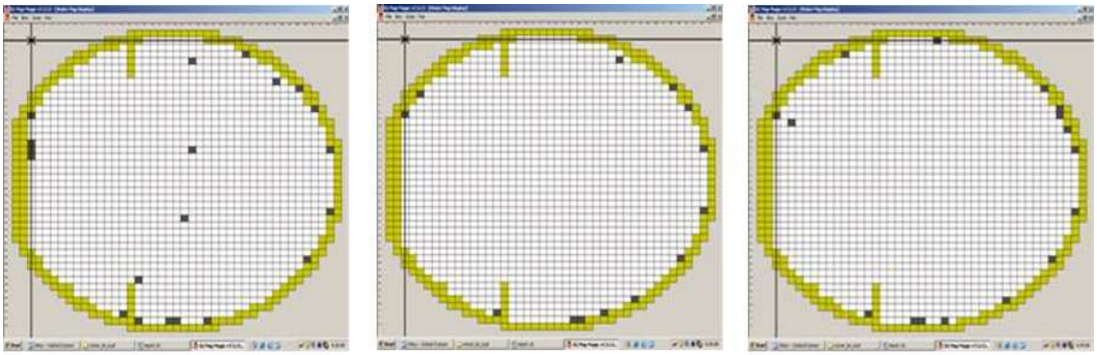
(c) Split 6

Figure 6.2: HNS *Thames* ASIC corner lot split 4, 5, and 6: : black squares are failed dies during "Go/NoGo wafer-level probe tests for continuity and $I_{DDQ}$ [23]



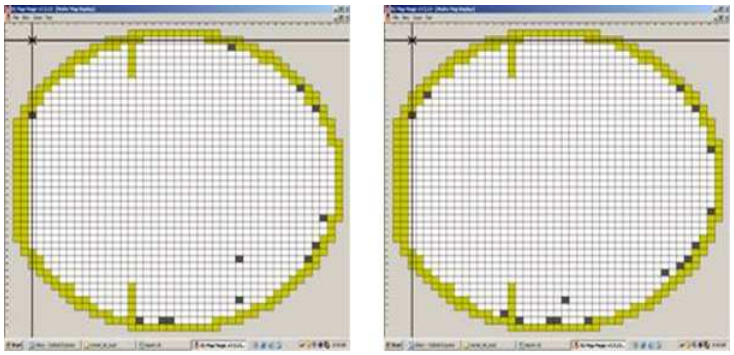
WAFER 7 WAFER 15 WAFER 24

(a) Split 7



WAFER 8 WAFER 16 WAFER 25

(b) Split 8



WAFER 9 WAFER 18

(c) Split 9

Figure 6.3: HNS *Thames* ASIC corner lot split 7, 8, and 9: : black squares are failed dies during "Go/NoGo wafer-level probe tests for continuity and $I_{DDQ}$ [23]

Table 6.3: *Thames* measured analog 5V supply current [mA]

| **DC** | **Temp.** $= -40\ ^{\circ}C$ | | | **Room Temp.** | | | **Temp.** $= 80\ ^{\circ}C$ | | |
|---|---|---|---|---|---|---|---|---|---|
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** |
| **Avg.** | 83.50 | 77.00 | 72.00 | 80.60 | 77.20 | 74.20 | 83.50 | 77.00 | 72.00 |
| **Std. Dev.** | 0.71 | 0.00 | 1.41 | 2.88 | 1.30 | 2.28 | 0.71 | 1.41 | 1.41 |

Table 6.4: *Thames* measured LVDS 5V supply current [mA]

| **DC** | **Temp.** $= -40\ ^{\circ}C$ | | | **Room Temp.** | | | **Temp.** $= 80\ ^{\circ}C$ | | |
|---|---|---|---|---|---|---|---|---|---|
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** |
| **Avg.** | 33.00 | 35.00 | 33.00 | 33.80 | 35.40 | 33.60 | 35.00 | 37.00 | 34.50 |
| **Std. Dev.** | 0.71 | 0.02 | 1.25 | 0.45 | 0.55 | 0.55 | 0.00 | 1.32 | 0.71 |

### 6.5.1 DC Test

During quiescent current and bias voltage tests, all supply voltages should be "on" and no RF signals are necessary at this point in the evaluation. Measurements of 5 V and 3 V supply currents can be performed by directly reading the HP E3631 dual DC power supply. All bias voltages should be measured using a voltmeter.

Bias voltages are monitored at room temperature for RF input, clock input, and output subsystem LVDS output buffer offset, each and summarized in Table 6.6.

Table 6.5: *Thames* measured digital and LVDS 3V supply current [mA]

| **DC** | **Temp.** $= -40\ ^{\circ}C$ | | | **Room Temp.** | | | **Temp.** $= 80\ ^{\circ}C$ | | |
|---|---|---|---|---|---|---|---|---|---|
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** |
| **Avg.** | 868.00 | 854.00 | 847.50 | 850.80 | 830.00 | 829.20 | 809.50 | 768.50 | 743.00 |
| **Std. Dev.** | 4.24 | 11.31 | 30.41 | 12.38 | 14.34 | 17.31 | 2.12 | 4.95 | 19.80 |

Table 6.6: *Thames* measured bias voltages [V]

| | RF Input Bias Voltage | | |
|---|---|---|---|
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** |
| **Avg.** | 1.69 | 1.68 | 1.65 |
| **Std. Dev.** | 0.03 | 0.03 | 0.02 |
| | **CLK Input Bias Voltage** | | |
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** |
| **Avg.** | 1.46 | 1.47 | 1.49 |
| **Std. Dev.** | 0.03 | 0.03 | 0.03 |
| | **LVDS Input Bias Voltage** | | |
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** |
| **Avg.** | 1.02 | 0.99 | 1.03 |
| **Std. Dev.** | 0.01 | 0.01 | 0.01 |

### 6.5.2 Dynamic performance test

Operating the ADC "at speed", a sinusoidal signal is applied to the ADC input and a number of data samples ($2^N$) are captured at the output. The sample set should not less than 4096 for accurate linearity tests (Integral non-linearity (INL) and differential non-linearity (DNL) tests). The amplitude of the applied input signals should be adjusted to $-0.5$ [dBFS] relative to the full-scale voltage of the ADC to prevent clipping. The captured sample set is post-processed via the developed VTS suite to compute ADC performance metrics such as full-scale voltage, offset, DNL, INL, SNR, THD, SFDR, SINAD, and ENOB. The details can be referred to the previous Chapter 3 to Chapter 5 with the HNS *Thames* proto-type verification test methodologies.

RF signal sources should be connected to the ADC input analog and clock simultaneously. The input clock source should be set to 800 MHz (for more ac-

Table 6.7: *Thames* Dynamic results summary - I channel at Room temperature

| Freq | 10 MHz | | | 100 MHz | | | 200 MHz | | | 250 MHz | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | |
| **ENOB** | 5.62 | 5.60 | 5.76 | 4.60 | 4.66 | 4.53 | 4.05 | 4.25 | 3.96 | 3.92 | 4.21 | 3.78 | [Bits] |
| **DNL** | 0.20 | 0.29 | 0.18 | 0.26 | 0.31 | 0.21 | 0.33 | 0.36 | 0.28 | 0.40 | 0.38 | 0.33 | [LSB] |
| **INL** | 0.52 | 0.57 | 0.32 | 0.86 | 0.56 | 0.77 | 1.65 | 0.83 | 1.57 | 2.02 | 1.07 | 2.05 | [LSB] |
| **SINAD** | 34.55 | 34.77 | 35.47 | 28.43 | 29.15 | 28.04 | 25.36 | 26.69 | 24.74 | 24.56 | 26.37 | 23.73 | [dB] |
| **THD** | -41.89 | -41.86 | -45.38 | -29.63 | -30.47 | -29.09 | -26.13 | -27.65 | -25.35 | -25.27 | -27.36 | -24.26 | [dB] |
| **SNR** | 35.51 | 35.77 | 36.02 | 34.84 | 35.06 | 34.83 | 33.65 | 33.77 | 33.64 | 33.11 | 33.39 | 33.23 | [dB] |
| $\mathbf{V}_{offset}$ | -2.00 | -0.10 | -1.90 | -1.80 | 0.10 | -0.60 | -1.00 | 0.50 | 0.00 | -0.50 | 0.60 | 0.50 | [LSB] |
| $\mathbf{HD}_2$ | -46.99 | -43.52 | -47.64 | -30.15 | -30.66 | -29.34 | -26.70 | -28.29 | -25.74 | -25.80 | -28.18 | -24.74 | [dB] |
| $\mathbf{HD}_3$ | -49.35 | -52.70 | -55.27 | -48.89 | -47.67 | -55.52 | -44.37 | -42.23 | -44.91 | -43.81 | -41.26 | -38.89 | [dB] |

curately, 800.03072 MHz when the input analog frequency is set as the coherent sampling case: 10.01015, 99.56437, 199.86119, and 249.96077 MHz with 1 Hz resolution RF signal source). As described in Chapter 5, the ADC encoded digital output power of each source will be adjusted to $-0.5$ dBFS during the test procedure. All supply voltages must be enabled and all RF sources turned on prior to performing the measurements. An oscilloscope with a differential probe should be used to verify that a differential clock signal ($\tilde{8}$00 MHz) is above 400 $\text{mV}_{pp}$ in the amplitude. The digital logic analyzer flying leads differential probe should be connected to the LVDS output 3-pin headers for capturing the output data of the desired channel I/Q or both.

The results presented in Tables 6.7 and 6.8 are averages across the complete sample set of tested *Thames* ADCs (the quantity of ADCs under testing for each lot: 10 samples) for nominal corner (Lot 1) and extreme corner process (Lot 8 and 9).

Table 6.8: *Thames* Dynamic results summary - Q channel at Room temperature

| Freq | 10 MHz | | | 100 MHz | | | 200 MHz | | | 250 MHz | | | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Lot** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | **Lot 1** | **Lot 8** | **Lot 9** | |
| **ENOB** | 5.40 | 5.14 | 5.32 | 4.43 | 4.51 | 4.31 | 3.95 | 4.14 | 3.90 | 3.81 | 4.08 | 3.70 | [Bits] |
| **DNL** | 0.28 | 0.30 | 0.22 | 0.28 | 0.22 | 0.22 | 0.29 | 0.33 | 0.28 | 0.35 | 0.36 | 0.40 | [LSB] |
| **INL** | 0.88 | 1.18 | 0.94 | 0.98 | 1.16 | 1.14 | 1.33 | 1.04 | 1.57 | 1.76 | 1.19 | 2.16 | [LSB] |
| **SINAD** | 33.58 | 32.14 | 32.97 | 27.72 | 28.37 | 26.97 | 24.80 | 26.10 | 24.37 | 23.96 | 25.69 | 23.22 | [dB] |
| **THD** | -38.18 | -35.56 | -36.22 | -28.61 | -29.65 | -27.76 | -25.41 | -26.99 | -24.94 | -24.56 | -26.57 | -23.70 | [dB] |
| **SNR** | 35.81 | 35.14 | 35.95 | 34.91 | 34.27 | 34.85 | 33.72 | 33.42 | 33.63 | 32.95 | 33.12 | 33.02 | [dB] |
| $\mathbf{V}_{offset}$ | -1.00 | 0.20 | -0.60 | -0.90 | 0.30 | -0.40 | -0.30 | 0.50 | 0.20 | 0.30 | 0.70 | 1.00 | [LSB] |
| $\mathbf{HD}_2$ | -39.27 | -38.10 | -37.50 | -28.99 | -30.11 | -28.03 | -25.77 | -27.47 | -25.30 | -25.11 | -27.23 | -24.27 | [dB] |
| $\mathbf{HD}_3$ | -50.04 | -49.97 | -49.59 | -50.77 | -46.69 | -47.48 | -43.68 | -42.85 | -41.84 | -39.16 | -41.12 | -37.19 | [dB] |

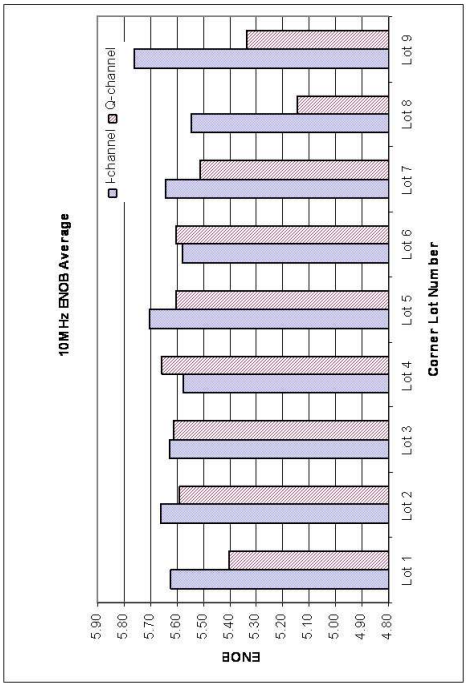
## 6.6 Test results and discussion

ADC dynamic specifications, such as effective-number-of-bits (ENOB), signal-to-noise-and-distortion ratio (SINAD), total-harmonic-distortion (THD), and spurious-free-dynamic-range (SFDR) are extracted from ADC dynamic performance test as addressed in Chapter 5. The performances of designed input buffers, track-and-hold amplifiers and comparators are based on differential bipolar junction transistor (BJT) amplifiers, which are dependant on the process variations of BJT-$\beta$ values and emitter areas. Poly resistor values for the ladder voltage references are also expected to depend on the corner process variations and contribute to quantize the input analog signals accurately.

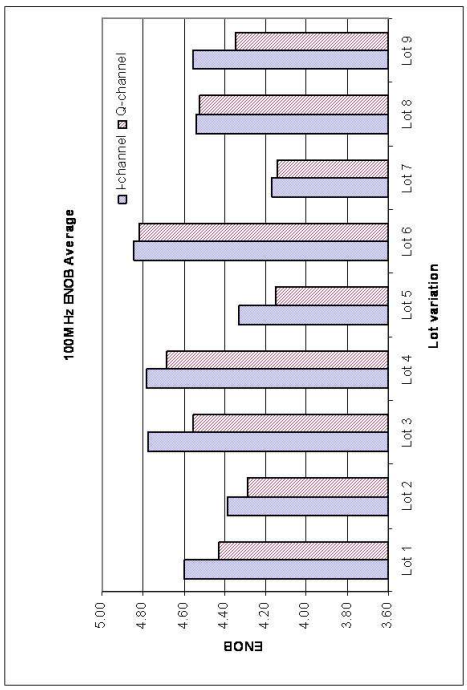
The complete corner lot splits were determined by skewing 4 process parameters: the poly resistor values (REpoly and RNpoly) and the BJT-$\beta$ values and the BJT emitter area size. The ADC corner lot evaluation is performed under ADC dynamic test conditions using input analog sine waves as addressed in Chapter 5. All tests were performed using our custom-designed evaluation board, socket, fix-

ture, and thermally enhanced thin quad flat packaged (TQFP) ADCs, which enable multiple samples to be tested in the same environment without the need to solder each sample to the board.

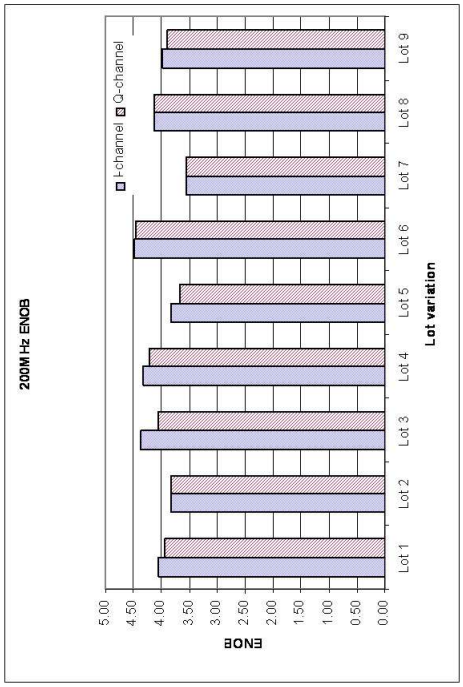
In Figure 6.4, Each corner lot split averaging ENOB results are plotted (over 5 samples) for 10, 100, 200 and 250 MHz sine wave input, respectively. The dynamic ADC parameters were extracted from the developed VTS suite based on Fast Fourier transform (FFT) in Chapter 5. By performing sine wave histogram tests [23, 13] with 10 MHz input sine wave, Figure 6.5 and Figure 6.6 were plotted the maximum differential nonlinearity (DNL) and integral nonlinearity (INL) values for each lot. The ADC offset values are also investigated for each corner process as shown in Figure 6.7. These process corners significantly improved circuit performance bounds in chip design, as compared to the overly pessimistic, conventional worst-case skew-corners.



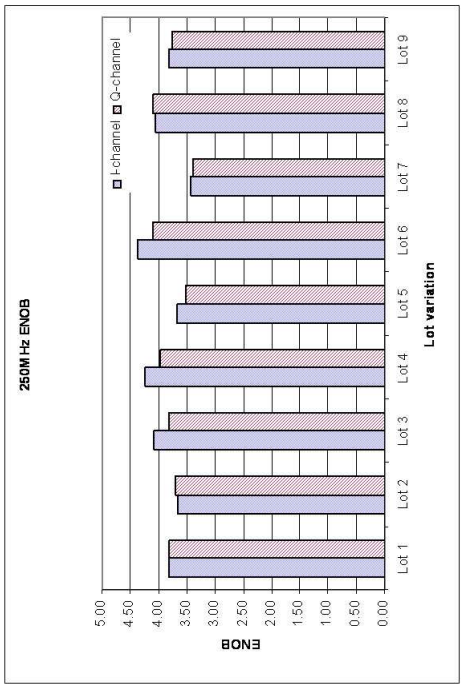

(a) 10 MHz




(b) 100 MHz

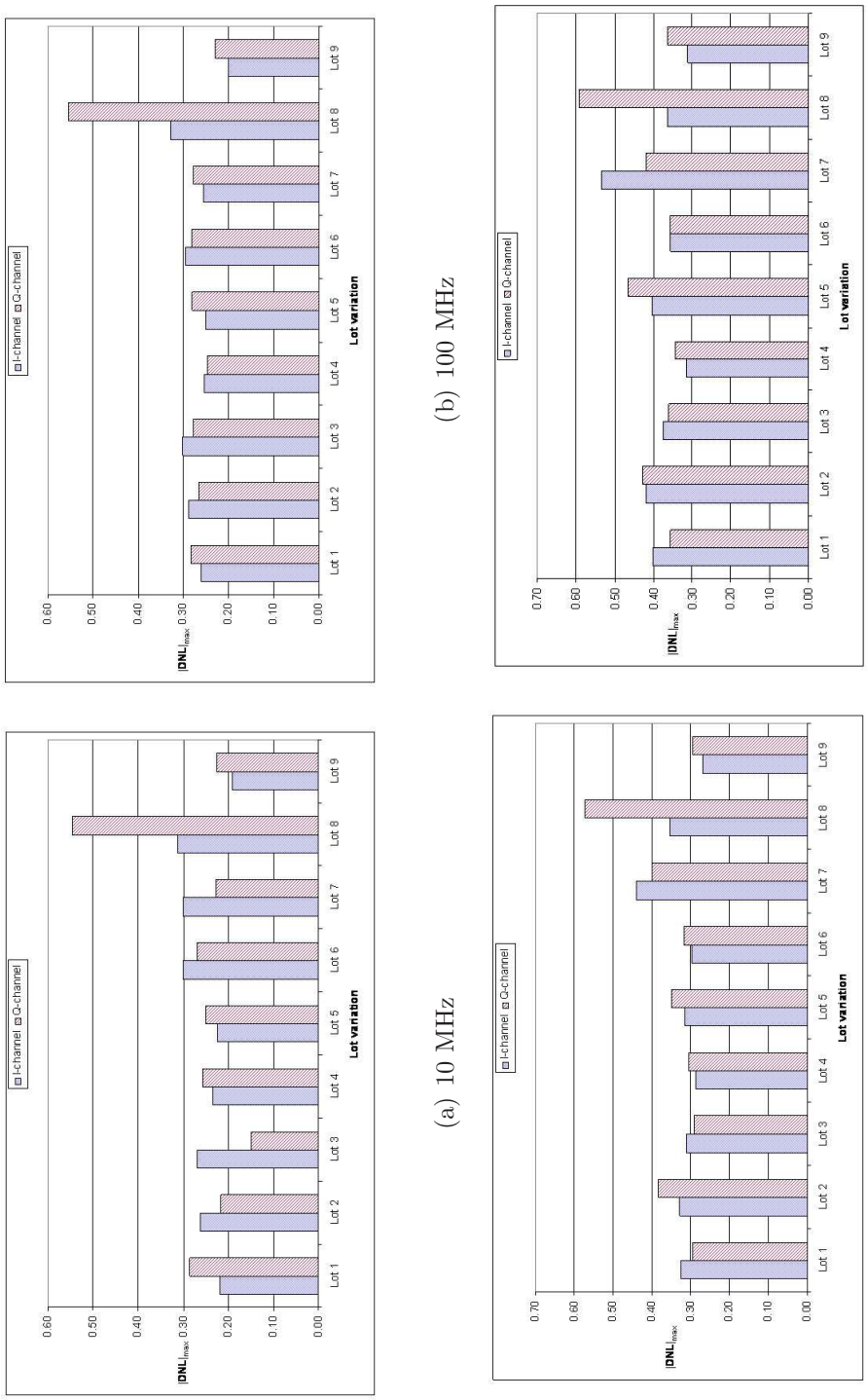



(c) 200 MHz




(d) 250 MHz

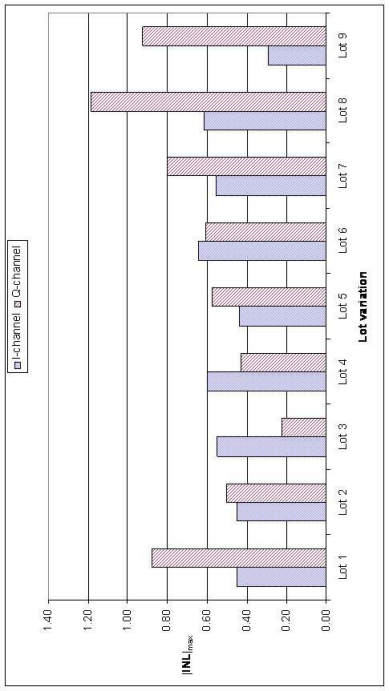
Figure 6.4: HNS *Thames* ASIC ADC ENOB for each corner lot split



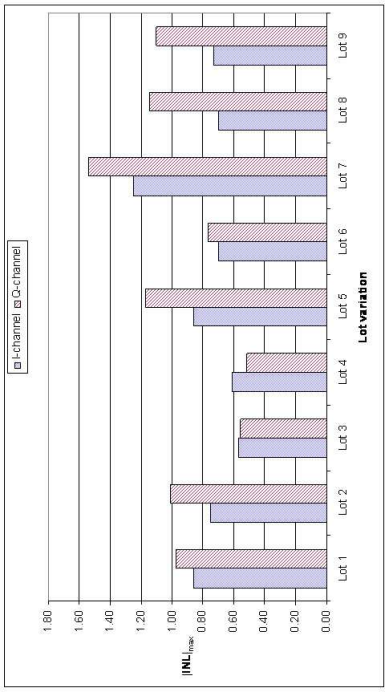

(a) 10 MHz (b) 100 MHz

(c) 200 MHz (d) 250 MHz

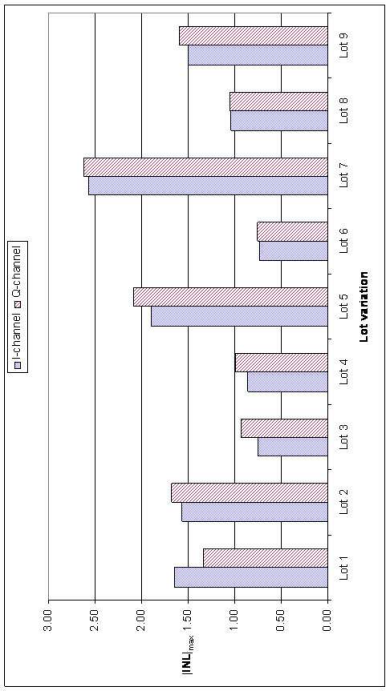
Figure 6.5: HNS *Thames* ASIC ADC DNL for each corner lot split



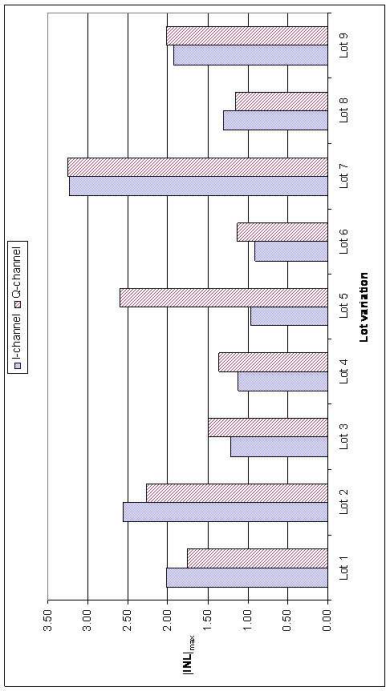

(a) 10 MHz




(b) 100 MHz

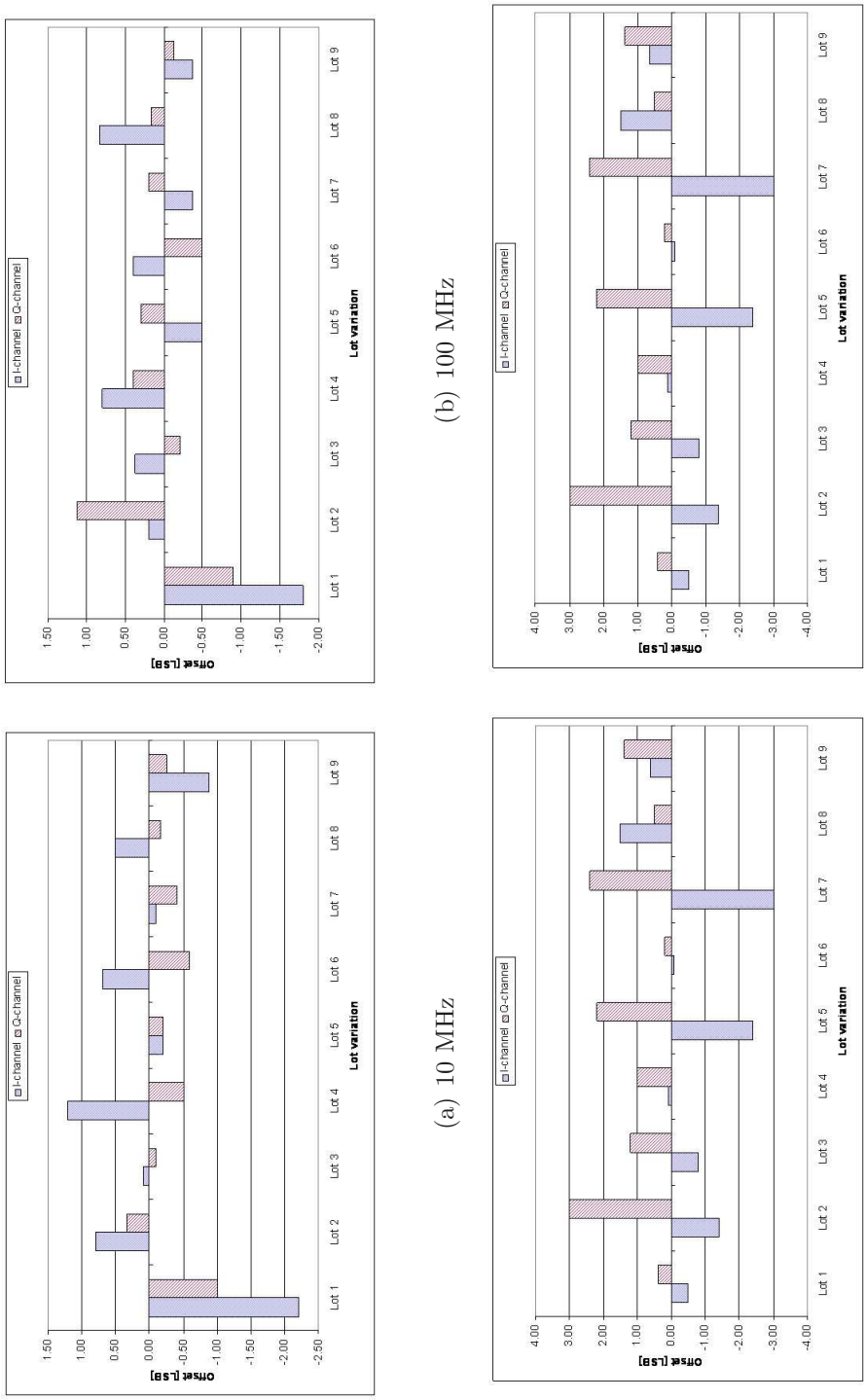



(c) 200 MHz




(d) 250 MHz

Figure 6.6: HNS *Thames* ASIC ADC INL for each corner lot split




(a) 10 MHz (b) 100 MHz

(c) 200 MHz (d) 250 MHz

Figure 6.7: HNS *Thames* ASIC ADC offset voltage for each corner lot split

## 6.7 Summary

Chapter 6 have demonstrated fully integrated high-speed ADC performance characteristics and the impact of process variations on these characteristics by skewing critical parameters in accordance with published and measured variance data [3]. Statistical process controlled corner variation methods allow us to evaluate the quality of the process, sufficiency of the test and measurement equipment, and which parameters dominate yield. The technique also informs us of the stability of a given process. This is why "corner-based"study can play an important role in product development. However, it has drawbacks. Corner lot study is slow and cumbersome since the study result is perceived by numerous testing and statistical data analysis.

As in previous chapters, DC testing is performed to monitor the ADC bias current and offsets. ADC dynamic parameters are all evaluated by using the VTS suite. In addition, the results of the ADC corner lot study confirmed that process variations such poly resistors and BJT-$\beta$ and emitter area size can affect the ADC dynamic performance. The study also puts these facts in a quantitative framework. Optimum ADC performance was achieved by setting the corner process at the Lot split-6 settings, which are maximum BJT-$\beta$ and minimum BJT emitter area, while keeping the poly resistors values as nominal and without changing the ADC chip design. Active circuit elements (as opposed to passive elements) are most dominant in defining ADC performance, primarily a circuit linearity.

Chapter 7

# Conclusions

## 7.1 Summary

High-speed ADC test methodology is presented. We have described a device verification software package that relies on FFTs for dynamic parameter evaluation. The software suite automatically applies optimal window functions and data set generators to guide the test through its duration. ADC performance is determined by operating conditions. ADC applications for modern satellite receivers and design-for-test (DfT) enhancing design approaches are also discussed. So, it is necessary to perform tests under a variety of input power levels and operating temperatures to verify the critical ADC parameters. As case study, 800 MS/s sampling rate HNS *Thames* high-speed dual channel 6-bit ADC is used and design-for-test methodologies are keys to success in all levels of ADC tests and verifications.

In addition, the proper testing set-up must consider high frequency effects at the device interfaces to the test equipment. Both input test tones, the sampling clock signal condition, a quiet power supply, and minimal ground noise must be ensured in the fixture design to achieve an optimum test result. This, in turn, imposes restrictions on the construction of the DIB fixtures and the ADC mounting socket. Many electrical interfacing problems are due to the ADC mounting socket on the DIB fixture. By increasing the thermal conduction from the electro-thermally packaged device to the heat sink, measured component performance can be improved. There is still a chance that the apparent performance can be degraded even if these steps are taken. This is due to the uncertainties in package design.

Fully integrated high-speed ADC performances for process variations are studied. ADC characteristics by skewing some critical parameters are monitored in-line and affect the circuit performance in a dominant manner. Statistical process controlled corner varied ADC study shows not only to evaluate the quality of the process, including the test and measurement equipment, but it tells us when the manufacturing process is not stable.

In this thesis, developed test fixture and VTS suite are able to qualify following *Thames*ADC specifications with DfT enhanced ADC design approaches:

1. DC tests: testing fixture can monitor and capture
    - Supply current
    - RF analog input DC bias

- Sampling clock input DC bias
- Temperature sensor DC voltage
- ADC internal reference DC voltage & Current

2. LVDS test: mostly performed in production testing phase and a basic foundry wafer probing tester can monitor

   - DC offset
   - Swing
   - Rise/fall time
   - Rise edge delay relative to 'data_ready'

3. Performance tests using the VTS suite: following parameters can be obtained:

   - voltage full-scale(VFS)
   - voltage offset
   - linearity: differential non-linearity(DNL) & integral non-linearity(INL)
   - effective-number-of-bits(ENOB)
   - signal-to-noise(SNR)
   - signal-to-noise-and-distortion(SINAD)
   - harmonic distortion(HD) & total harmonic distortion(THD)
   - spurious-free-dynamic-range(SFDR)

- inter-modulation-distortion(IMD)
- effective-resolution-bandwidth(ERB), and etc.

When a design is first released to production, the new product undergoes a characterization process to determine whether or not it meets the customer's requirements or the design specifications. The first-pass design often has problems that must be corrected before a final version of the design can be released to production. In order to produce a production-worthy design in a short time-frame, characterizing the design IC performance and diagnose internal circuit problems are concurrently managed and planned from the initial design process using proper DfT concept.

The following lists are summarizing this thesis research works:

- Important case study for a high-speed ADC and DfT enhancements
- Concurrent engineering for successful high-speed ADC design and test
- Verification tool development - VTS suite
- Cost-effective testing fixture development for a rack & stack production test
  - Socket design issue(s)
  - PCB design for high frequency
- ADC design parameters sensitivity analysis (corner lot study): to determine the impact of process variations and to analyze the sensitivity of the ADCs,

critical process parameter variant ADCs are fabricated and examined.

- Production test (approach to ATE)

## 7.2 Contributions

The high-speed ADC design verification and test methodologies are studied and the thesis provides a detail and generalized optimal high-speed ADC testing methodology. The methodology is suitable for duplicating the test method and the results for testing reproducibility. Improved methodology for dynamic performance testing of ADCs for satellite communications is employed with the device verification test software, VTS suite. To provide enough background for general high-speed mixed-signal system-on-chip device verification such as HNS *Thames* ASIC ADC, the methodology is also developed for someone who is not familiar with ADC or RF testing could understand. Design for Test (DfT) concept as a part of process from the design phase to the full productions are used to be successful in the high-speed ADC design verification tests (DVTs).

## 7.3 Future work

In the future, developing on-wafer level high speed ADC testing methodologies is sometimes considered for the next phase development of a high-speed ADC DVT. Unfortunately, wafer probe cards introduce unwanted signal crosstalk which is expensive to eliminate. The optimum test set-up for high speed ADCs would use

a packaged ADC designed with DfT methodologies and advanced RF packaging technology. More work must be done to estimate and eliminate from the package uncertainties.

The suggested test methodology and the VTS suite described in the thesis are fully compliant with IEEE test standards. They represent an extension of previously published work [77] through the integration of the IMD product and ERB testing options. Also automated window adjust for the FFT module of the VTS is included. These enhancements allow for the generation of a well-defined detailed sequence of testing operations. Automated test equipment (ATE) can be integrated with the VTS software suite to provide full control over the test minimizing test cost and effort.

# Appendix A:

# VLSI design procedure

To be successful in any of high-speed ADC ASIC project, it is a good idea to design functional procedure for ISO-9001:2000 compliance [100, 101]. The International Organization for Standardization (ISO) is a worldwide organization that develops many different kinds of Standards. ISO 9001 is a series of documents that define requirements for the Quality Management System Standard.

This chapter describes the *'what'* of ASIC designs [75] to carry on designing and testing a high-speed ADC for a modern satellite receiver. To be compliant with ISO 9001:2000, a design must proceed from phase to phase in the design process as described in this chapter. It should be noted that due to the rapid development of new technology in the VLSI design, divergence from the guideline is prone to be frequent. Clear demonstration and explanation for the design process is a key success factor to finish the ASIC project.

## A.1 Quality policy and objectives

The quality policy of Analog & Mixed-signal System Design Lab. in the University of Maryland, College Park is to develop state-of-the-art VLSI digital, analog, and RF/mixed-signal integrated circuits that optimize product value for their customers. This mission includes:

- management and design of program-critical integrated circuits
- industry leading design environment
- ASIC foundry relationships
- supporting software

To achieve the Analog & Mixed-signal System Design Lab. quality policy and objectives, the following metrics shall be considered for each project:

1. Actual schedule time, defined as the actual time between design specific report completion (signified by successful completion of the preliminary design report) and prototype delivery.
2. Promised schedule time, defined as the time promised to the customer between spec completion and prototype delivery.
3. Schedule time delta, defined as the difference between actual and promised schedule time

4. Number of critical defects (defects adversely affecting the product cost, features, or performance)

5. Number of major defects (defects requiring hardware or software workarounds)

6. Number of minor defects (defects not affecting operation and not requiring a work-around).

7. Production cost relative to initially planned cost

8. Total number of system problem reports filed during each phase

9. Total number of system problem reports filed after each phase for which the "phase injected" indicates the phase

10. Process phase effectiveness for the following stages of development: project planning, high level description (HLD), low level description (LLD), and top level verification.

    Process effectiveness is defined as the ratio of number of system problem reports (SPRs) filed after a phase is complete for which the "phase injected" indicates the phase divided by the number of SPRs filed during or before the phase. A phase is considered complete after the SPRs for the associated review are entered into defect and enhancement tracking systems (DETS). To summarize:

    $$\text{Process phase Effectiveness} = \frac{\text{No. of system problem reports filed after phase}}{\text{No. of system problem reports filed during phase}}$$

Analog & Mixed-signal System Design Lab. quarterly review shall be held amongst management and senior engineers to examine metrics collected and take corrective action if any objectives are not being met or the process is not being complied with.

Analog & Mixed-signal System Design Lab. quarterly review shall examine both process compliance and process effectiveness. During the review, all system problem reports written against the methodology shall be reviewed and an action determined. Additionally, any new customer feedback forms completed since the last review shall be examined and any actions determined.

## A.2 Project flow

Each ASIC design shall progress from phase to phase as illustrated in Figure A.1. Note that full custom analog and standard cell enhanced digital designs diverge after the high level design phase and converge at the fabrication phase. The project plan shall indicate which branch each particular project will follow.

The following sections describe each phase of an ASIC design. There are three subsections in each section. The Entry Criteria subsection describes what is necessary to begin the phase. The Activities subsection describes what activities take place in the phase. The Exit Criteria subsection describes what is necessary to exit the phase.

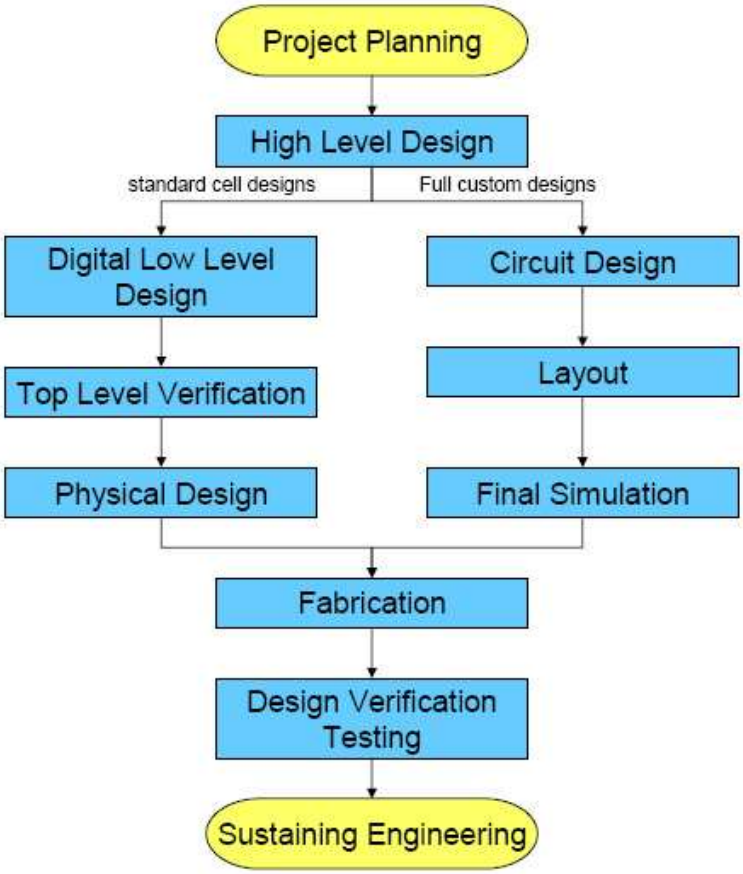



Figure A.1: VLSI Process Phase

### A.2.1 Project planning

A. *Entry criteria*

Generate a simple document which is indicating the requirement for ASIC/VLSI hardware. This stage is called an export compliance plan and it need to be documented the guidelines used by the project to determine if the project or specific components within the project are subject to export control. If found to be subject to export control, this plan specifies the type of controls that need to be applied.

B. *Activities*

Project planning involves determining the course of action for a particular ASIC design. This includes determining the required resources, developing an initial schedule, and understanding the basic requirements. Additionally, the project plan must state the projects quality objectives as well as any statutory and regulatory requirements.

C. *Exit criteria*

The project planning phase shall be considered complete when the design methodology review is completed and all associated action items.

### A.2.2 High level design

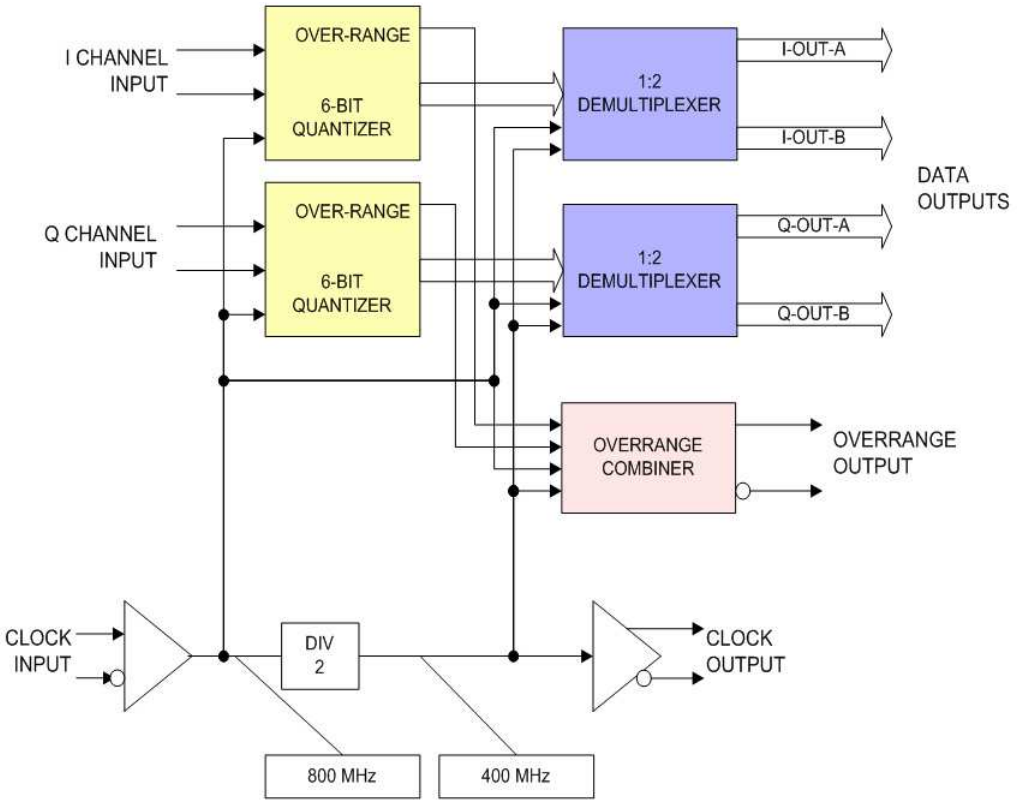



Figure A.2: Example of planning and design phase high level design functional block: high-speed ADC: the ADC is a dual 6-bit analog to digital converter at a sample rate of 800 MHz. The ADC is a two channel 6-bit device and samples from each converter are demultiplexed by a 6:12 demultiplexer. The output data from the converter is LVDS compliant with IEEE 1596.3-1996 [34]. The ADC provides an output clock signal at 1/2 of the input clock frequency and a mid-scale reference voltage output. The ADC also provides an over-range output signal, which is common for both converters and is active for one 400 MHz output clock cycle when triggered. The output saturates at positive or negative full scale when overdriven in the positive or negative directions, respectively. The ADC operates on positive supply voltages only.

A. *Entry criteria*

The high level design phase of an ASIC shall begin upon successful completion of the ASIC project plan.

B. *Activities*

High level design consists of design activities revolving around ASIC architecture and decisions affecting specific requirements for the design.

The high level design (HLD) phase should result in documentation with enough detail to begin low level design work. All requirements should be clear. When the high level design document is complete, a preliminary design review (PDR) shall be held. The document may be either the HLD section of the ASIC Design Specification or an ASIC Requirements Specification. If the ASIC Requirements Specification is created, the high level design (HLD) section of the ASIC Design Specification may be updated to reference this document and no further description is required in the design a specification. The PDR is a requirements review and successful completion of the PDR and all related action items shall indicate all parties agree on the requirements and scope of work.

Additionally, during the high level design phase, the first version of the ASIC procurement specification shall be created to facilitate communications through a vendor.

C. *Exit criteria*

The high level phase shall be considered complete when the following actions are completed:

- preliminary design review (PDR) completed and all associated action items closed.
- ASIC Procurement Specification checked in to document control under numerical revision
- ASIC Design Specification checked in to document control under numerical revision.
- If an ASIC Requirements Specification is used for the requirements document instead of the high level design (HLD) section of the ASIC Design Specification, this document shall be checked into document control under numerical revision.

As an example, Figure A.2

### A.2.3 Digital low level design

A. *Entry criteria*

Digital low level design of an ASIC shall commence after the preliminary design review is held.

B. *Activities*

The low level design phase involves detailed design and implementation of the design. Low level design occurs simultaneously for all blocks in the ASIC design. A low level description (LLD) shall be created for each block and incorporated into the ASIC design specification. ASIC management shall create a list of blocks that require a functional design review (FDR).

C. *Exit criteria*

The low level design phase shall be considered complete when the following actions are complete:

- ASIC Design Specification incorporating all low level description blocks (LLDs) checked in to document control under numerical revision
- All management required functional design reviews (FDRs) are completed and all action items closed
- All blocks are complete

### A.2.4 Top level verification

A. *Entry criteria*

The top level verification phase of digital ASIC designs shall commence when management determines a sufficient number of blocks are complete enough to obtain meaningful verification results.

B. *Activities*

Top level verification is the phase when the design is tested to prove correctness.

As a part of top level verification, the ASIC Design Specification must be updated with a complete verification section. This will include the design verification testing (DVT) tests for use when prototypes are available, as well as any required equipment. An ASIC DVT Plan document may be used as a separate document if desired (in place of listing DVT information in the ASIC Design Specification). If a separate ASIC DVT Plan document is used, the ASIC Design Specification shall be updated to reference this document and no further DVT information shall be listed.

Initial sign off (*ISO*) is the hand off of the complete design netlist. Before the netlist is considered signed off, the *ISO* review must be held.

C. *Exit criteria*

The top level verification phase shall be considered complete when the following actions are complete:

- All prior phases of digital ASIC design are complete.
- The *ISO* review is complete and all action items are closed.
- The ASIC Design Specification with updated verification information is checked in to document control under numerical revision.

– The ASIC DVT Plan document, if used in place of listing DVT information in the ASIC Design Specification, checked in to document control under numerical revision.

### A.2.5 Physical design

A. *Entry criteria*

Physical design shall commence after the ISO review is held and all ISO review action items are closed, for digital designs only.

B. *Activities*

The physical design phase is when the ASIC logical netlist is converted into physical information for the construction of the integrated circuit. During the physical design process the timing characteristics of the ASIC become clear. The ASIC Design Specification shall be updated with timing and other related physical information. The ASIC procurement specification shall be updated to reflect any relevant physical information as well. Final sign off (FSO) is the acknowledgement that the physical design meets all relevant criteria. Before this acknowledgement is given, the final sign off review shall be conducted.

C. *Exit criteria*

The top level verification phase shall be considered complete when the following actions are complete:

- The FSO review is held and all action items are closed.
- The ASIC Design Specification is updated with physical information and checked in to document control under numerical revision.
- The ASIC Procurement Specification is updated with physical information and checked in to document control under numerical revision.

### A.2.6 Circuit design

A. *Entry criteria*

Circuit design for analog ASICs shall begin upon completion of the preliminary design review.

B. *Activities*

The circuit design phase is when the ASIC is designed and implemented at the transistor level. Activities include circuit design and simulation. Simulations include block level, full chip, and full chip with package. Before the circuit design phase is considered complete, a review shall be held as specified.

C. *Exit criteria*

The circuit design phase of an analog ASIC design shall be considered complete when the following actions are complete:

- The circuit review is held and all actions items are closed.

- The ASIC Design Specification is updated with relevant low level design information and checked in to document control under numerical revision.

### A.2.7 Layout

A. *Entry criteria*

The layout phase of analog designs shall commence upon availability of circuit schematics and completion of the circuit design review.

B. *Activities*

During the Layout phase, floorplanning and layout are completed. Design rule checks and layout versus schematic checks must be performed to ensure correctness. Before Layout is considered complete, a layout review must be held. Guidelines for the Layout review may be found in [4].

C. *Exit criteria*

The Layout phase is considered complete when the Layout review is held and all action items are closed.

### A.2.8 Final simulation

A. *Entry criteria*

The final simulation phase of an analog ASIC design shall commence upon completion of the Layout review and closure of all Layout review action items.

B. *Activities*

Activities during Final Simulation include a full simulation of the entire ASIC including parasitics and the package. Once all simulations are passing and complete and the GDSII file is ready for handoff the design is ready for Final Sign Off (FSO).

As a part of the final simulation phase, the DVT plan shall be finalized and documented. Either the DVT Plan (if used) or the verification section of the design specification shall be updated to reflect the DVT test plan. Additionally, the design and procurement specifications shall be updated with final physical details.

Final sign off (FSO) is the acknowledgement that the physical design meets all relevant criteria. Before this acknowledgement is given, the final sign off review shall be conducted.

C. *Exit criteria*

The Final Simulation phase of analog ASICs shall be considered complete when the following actions are complete:

- FSO review held and all action items closed.
- All previous phases complete
- ASIC design specification checked in to document control under numeric revision.

- ASIC procurement specification checked in to document control under numeric revision

### A.2.9 Fabrication

A. *Entry criteria*

The fabrication phase of ASIC design shall begin after the FSO review has been held and all FSO review action items are closed. After the FSO review, a handoff of either a final netlist (for digital designs) or a DRC and LVS clean GDSII file (for analog designs) shall signify the start of the fabrication phase.

B. *Activities*

Although the activities associated with fabrication are not performed by the University of Maryland, College Park, the ASIC lead shall maintain contact with the foundry to assess progress and manage any difficulties that arise. As vendor management is critical to a success of the designs, frequent communication is encouraged.

C. *Exit criteria*

The fabrication phase shall be considered complete upon receipt of ASIC prototype parts.

### A.2.10 Design verification testing

A. *Entry criteria*

The design verification testing (DVT) phase of ASIC design shall begin when prototype parts are available.

B. *Activities*

The DVT phase is when the ASIC prototypes are tested in the lab. Results of the DVT shall be documented in the ASIC Design Specification verification chapter or in an ASIC DVT Plan document. The ASIC Procurement Specification shall be updated as well with any final adjustments.

Any device defects discovered shall be recorded in DETS. Although the data shall be summarized in the ASIC Design Specification, DETS is the official repository for ASIC defect information.

Before DVT is complete and the device declared production ready, the release to production checklist shall be completed by the ASIC manager or ASIC lead. Any action items resulting from completing this checklist must be tracked in DETS and closed before releasing the device to production by releasing the procurement and design specifications to alphabetic revision.

C. *Exit criteria*

The design verification testing phase shall be considered complete when the following actions are complete:

– The ASIC Design Specification shall be updated and checked in to doc-

ument control under alphabetic revision

- The ASIC Procurement Specification shall be updated and checked in to document control under alphabetic revision
- The ASIC DVT Plan document, if used in place of listing DVT information in the ASIC Design Specification, shall be updated and checked in to document control under numeric revision
- The release to production checklist is completed and placed in the project tracking folder and any action items are closed.

### A.2.11 Sustaining engineering

A. *Entry criteria*

The sustaining engineering phase of a digital ASIC design shall begin after the device is released to production by checking in the procurement and design specifications to alphabetic release.

B. *Activities*

The sustaining engineering phase of a project is when all remaining issues related to an ASIC are resolved.

Upon management creating a DETS SPR requesting design archiving, all of the design files and information shall be archived. The archiving checklist shall be completed by the ASIC lead. Any action items resulting from filling out

this checklist shall be tracked in DETS until completed.

Throughout the production lifetime of an ASIC issues may arise that require VLSI engineering support. ASIC management shall handle these issues by creating SPRs and assigning them to the appropriate engineering staff. The issues shall be tracked by ASIC management until they are closed. Until an ASIC completely goes out of production it is expected that some amount of support will be required.

Any documentation updates to the ASIC procurement or design specifications must be accompanied by an Engineering Change Notice (ECN). This is necessary to update documents under alphabetic revision. Additionally, any device re-spins after release to production require an ECN.

After release to production is achieved, the ASIC manager shall hold a lessons learned meeting with all engineering staff who worked on the project. The project shall be discussed openly including project success and failures. Future methodology recommendations should be made to help avoid problem. These shall be recorded at this meeting shall and entered into DETS as Methodology SPRs.

C. *Exit criteria*

The sustaining engineering phase of ASIC design shall be considered complete when the following actions are complete:

- The archiving checklist is completed and placed in the project tracking folder and any action items are closed
- All SPRs recorded in DETS are closed
- Lessons learned meeting held and Methodology SPRs filed
- The ASIC goes out of production

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