ABSTRACT

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                             COULOMB BLOCKADE DEVICES

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                             Department of Physics

In this thesis I describe the work performed in two different areas of research,

electrical breakdown of air for small electrode separations and measurements of

silicon (Si)-based tunable-barrier single electron transistors (SETs).

In this work, I describe a new method for measuring the breakdown of air for the

range of electrode separation of interest. This method has several advantages

compared to ones found in the literature, namely it allows for a measurement of

electrode separation before each breakdown measurement; it has a parallel plate

geometry and the surface roughness of the electrodes used is very small.

Using the results obtained with this method I have made a quantitative

comparison between the predictions of the standard theory of the field (field emission

of electrons) and our data, something that has not been done before. In this thesis I

describe analytically both the theory and the analysis of our data. I conclude that the

standard theory used in this field fails for the range of electrode separations of interest (400 nm to 45 μm).

Also, I describe electrical measurements performed on a Si-based tunable-barrier device fabricated in the group of Neil Zimmerman at the National Institute of Standards and Technology (NIST) using the fabrication facilities of Cornell University. I demonstrate that this device can be operated as an SET. I continue by describing measurements of the charge offset drift (Q_0(t)) for this device and show that it is almost 3 orders of magnitude smaller than in metal devices, and comparable to previously measured Si devices of this type. All of the previously measured devices originated from the same fabrication source, NTT, Japan. Our ability to demonstrate the same low drift in devices fabricated at Cornell, USA, indicates that the small values of Q_0(t) is a robust property of Si-based devices, and not sensitive to the details of fabrication.

ELECTRICAL MEASUREMENTS AT THE MICROSCALE: AIR BREAKDOWN
AND Si COULOMB BLOCKADE DEVICES

By

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Dedication

To my parents, Ada and Spyros.

Acknowledgements

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Chapter 1: Motivation

1.1: Two areas in materials beyond CMOS with open questions

In the past years, the need for smaller and faster electronic devices has pushed silicon (Si) technology to its limits. Even though Si devices have been getting smaller it is widely accepted that in the next few years the physical limitations of the size and speed of such devices will be reached. With that in mind, there is a large effort to discover and evaluate new possibilities for making computing possible in new ways [1]. Obtaining better measurement techniques and a better understanding of the physical processes in materials beyond the ones used in current complementary metal oxide semiconductor (CMOS) technology is very important.

In this work I have investigated two possible ways for creating better measurements techniques that would lead to a better understanding of physical processes in materials used for beyond CMOS technologies. I have used the idea of very sensitive charge electrometry as our probe into two questions that arise in terms of the operation of novel devices. As a first approach, I wished to investigate the physics of electron transport through a metal-molecule contact. The understanding of the properties of such a contact is clearly very important in predicting the behavior of a metal-molecule-metal device. The investigation of such a system involved making a capacitance measurement of a metal-self assembled monolayer (SAM)-air-metal capacitor. As a second approach, I wanted to build a better single electron transistor

(SET). This device, with improved characteristics, could be used as an ultra sensitive charge electrometer which would allow the investigation of charge transfer in materials used for beyond CMOS technologies. It would have potential use in a variety of different applications, such as a charge detector for charge based quantum computing.

In section 1.2, I will describe how the first approach led us to the examination of electrical breakdown of air for small electrode separations. In section 1.3, I will discuss the motivation behind building a better SET and its potential applications.

1.2: The capacitance experiment

I have measured the conditions for electrical breakdown between two electrodes separated by a gap of about 1 μm, a regime which has not been characterized adequately previously. Initially, as mentioned above, my desire was to better understand the energetics and transport through a SAM by measuring the capacitance of such a system of molecules as a function of applied voltage (more details are given below). However, during the course of this, I discovered that the breakdown phenomenon was preventing us from applying the necessary values for the voltage thus making the experiment impossible. Furthermore I found that the breakdown phenomenon was poorly characterized in the literature, for the range of electrode separations of interest in our experiment (400 nm to 45 μm). I thus chose to investigate further the topic of electrical breakdown at such small separations, which I report in chapters 2 and 3.

The original motivation for this experiment, as mentioned before, is the understanding of the electrical properties of molecules used in molecular electronics and their contact properties to metallic leads. Molecular electronics refers to the field that investigates the possibility of using molecules as the active components of a device [2]. In this field, much of the effort is concentrated on transport measurements of systems like the one shown in figure 1-1.
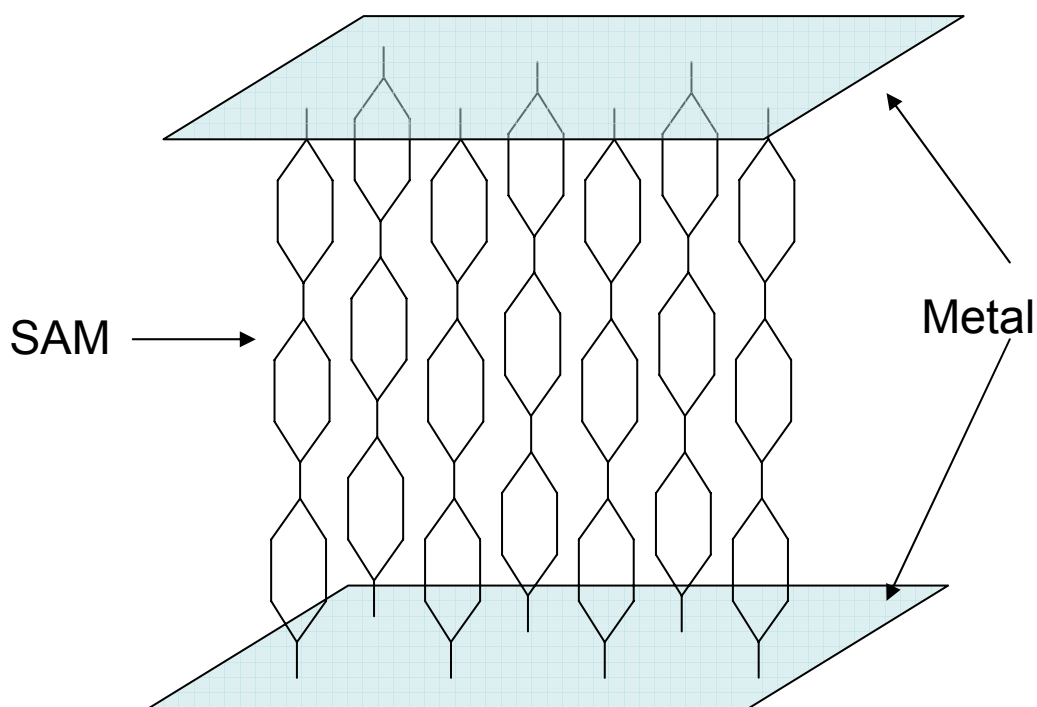
Figure 1-1 Schematic representation of a Self Assembled Monolayer contacted on both sides by metallic electrodes.

The techniques used to measure the current (I) as a function of applied voltage (V) of these molecules can be described by two main categories [2]. The first is measurement of conduction through a SAM of such molecules. In this case, a large

area of the SAM is used for conduction. The second is conduction through individual molecules (or a small number of them).

For the first case, a SAM is grown on an electrode (usually Au) of known size. A second electrode is either evaporated on top of the SAM [3], or is approached until it makes contact with the molecules. In both cases, the area of the metal-molecules-metal junction is very large compared to the size of the individual molecule, and so conduction through such junctions involves conduction through thousands, or even millions, of molecules.

For the second case, one common technique is to probe an individual molecule (or a small number of them) using a conducting AFM tip [4, 5]. A SAM is grown on an electrode and the molecule of interest is then inserted in holes, or imperfections, of the SAM. It is then located by the AFM and contacted by its tip. Other methods include forming a small junction either by a mechanical break junction [6], or by a break junction formed by electromigration [7]. In both cases, the small gap is then bridged with the molecule of interest.

Conduction through such metal-molecule-metal junctions is not well understood. Some of the questions that need to be addressed more carefully involve intrinsic properties of the molecules used, and some have to do with their contacts to metals. Examples of the first category of important questions are: what is the energy gap between the highest occupied molecular orbital (HOMO) and the lowest unoccupied molecular orbital (LUMO) [8], and what is the degree of delocalization of electrons in these orbitals [9]? As examples of questions about the contact properties I can ask: How does the Fermi energy of the metal line up with respect to the HOMO-LUMO

gap [9]? How does the HOMO-LUMO gap change because of the presence of the metallic contact [8]? What are the properties of the barrier between metal and molecule [9]? These questions are important since it is the HOMO and LUMO orbitals that are considered to be the ones that dominate the conduction [9].

In an effort to answer some of these questions, mainly ones that have to do with the metal-molecule contact, I propose the following experiment. Assume we have a system like in figure 1-2:
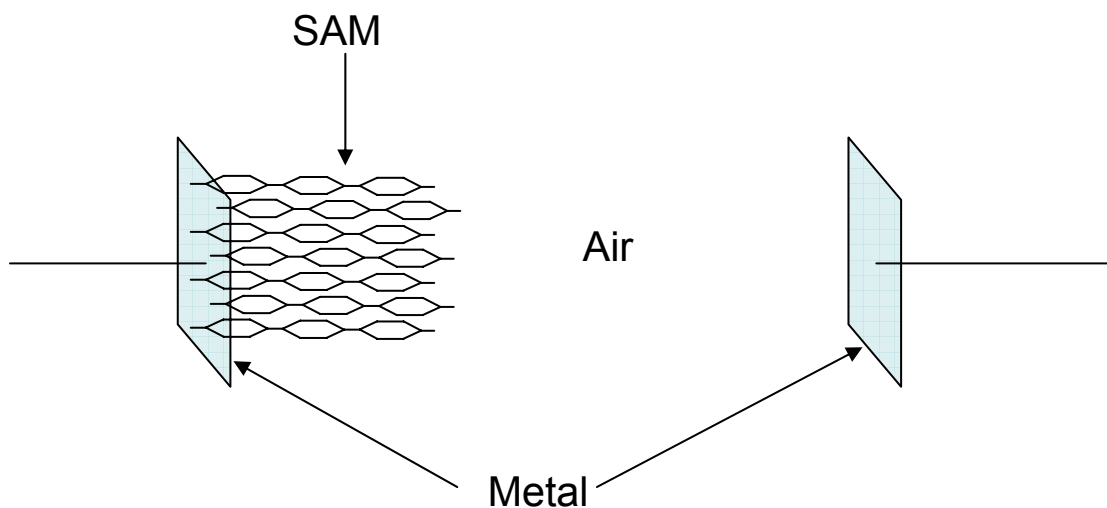
Figure 1-2 A drawing of a Metal-SAM-air-metal capacitor

I would like to apply a potential difference between the two electrodes, so that a potential difference builds across the molecules and the electrode they are attached to. By doing so, I want to force electrons to tunnel onto, or off of, the molecules from the metallic lead. This charge transfer would induce a change in the capacitance of the system, which I would detect. The details of the electronic structure of the system

would determine the qualitative and quantitative response of the capacitance (for a detailed discussion of the expected experimental observables, please see Appendix A).

The typical length of the molecules of interest is usually about 2 nm [6]. I would also like to be able to apply voltages across these molecules of the order of 1 V. This is a typical value of applied voltage across these molecules in the literature [6, 9]. This would mean that if the electrodes are spaced by a distance l, I would have to apply a voltage of roughly (l/2 nm) V between the two electrodes. Realistically I cannot expect that I will be able to approach macroscopic electrodes, in a parallel plate geometry, closer than a few hundred nanometers. That would mean that I would have to apply large voltages (hundreds of volts) across an air gap of a few hundred nanometers. So, I have established the fact that I need an applied electric field of approximately 1 V/nm, for our experiment.

The existence of the electric breakdown phenomenon limits the amount of electric field that can be applied between two electrodes for a given separation between them and a given dielectric in between them. In the case of our proposed experiment the knowledge of the exact value of this breakdown voltage is of great importance. If I were to exceed it, there would be a non-zero current flowing between the electrodes, making the measurement of capacitance impossible. In order to perform the capacitance experiment, I have to build a mechanical system with which I can change the separation between two metallic electrodes in air in the range below 1 μm. Also, it is important to understand how much voltage I can apply between these electrodes

before I reach electrical breakdown. By electrical breakdown I mean a sudden discharge between the two electrodes.

Electrical breakdown of an insulating material is the result of applying a large electric field across it. It represents a situation where the properties of an insulating material change and a path is created for electrons to pass through it. In many cases this is an irreversible effect and the properties of the material are permanently changed. In the case of air between two electrodes, breakdown can occur for either of the two following reasons. The electric field might be large enough to accelerate electrons enough that they can ionize air molecules through collisions. These ions can, in turn, produce more electrons by colliding with the electrode surfaces. This is known as an avalanche breakdown. The second possibility is that the electric field is high enough that it causes field emission of electrons from the electrodes. Both possibilities will be discussed in detail in Chapter 3.

In trying to design my system I have found that breakdown field of air for the electrode separations of interest to me is rarely discussed in the literature. Therefore, I decided to investigate this phenomenon in this regime. I have built a mechanical system that allows controlled variation of the distance between two electrodes in the regime of interest. I have measured the value of the breakdown voltage for air in my system for a range of electrode separations (400 nm to 45 μm). These measurements are described in chapter 2. I have also analyzed the standard theory of the field (field emission of electrons) and show that it fails to predict the breakdown voltages observed in our system. This part of the work is described in chapter 3. My results

also indicate that I would not be able to apply the necessary large electric fields needed for the capacitive measurement of molecular SAMs to work.

1.3: The silicon devices

A primary motivation for the second part of this thesis comes from the field of quantum computing. Quantum computing is a physically different approach to creating active elements for a specific computational need. Its strength comes from the fact that the active elements are not in a classically defined state that can take one of two or more possible values but rather that they are in a quantum mechanical superposition of all possible states. Furthermore, different elements can be entangled between each other (meaning that the quantum mechanical state of one depends on the others), a property that allows for types of interactions and speed of interactions between elements that would otherwise be impossible [10].

The building blocks for a quantum computer, the active elements, are called "qubits" which can be any two level quantum mechanical system. In all of the different implementations of qubits, there are great similarities. For example, in all cases gates are needed in order to initialize and control the individual qubits. Also a readout technique is needed in order to detect the final state of the qubit, after an operation. There are different ways for experimentally implementing a qubit. Some examples include ions [11] and some solid state qubits [11], to name a few. In the solid state qubit subcategory, there are flux based qubits (superconducting Josephson

junctions) [12], spin qubits [11], etc. The specific implementation we are most interested in is the charge qubit [11, 12]. In this case the observable is the position of a certain charge. There are different ways of making a charge qubit, using quantum dots of different materials. Lately there has been a demonstration of a charge qubit in a silicon device [13]. Silicon devices have the advantage of being well studied because of their use in conventional computing and fabrication processes are extremely well developed for this material.

In the case of the charge qubit, the logical candidate for a readout device which can detect the position of a single charge is the single electron transistor (SET). The SET is the world's most sensitive electrometer, with charge sensitivity that goes well below the charge of the electron (see section 4.6).

Besides quantum computing, the silicon devices that I will be using as my SETs have the potential of being useful in several different fields. As SETs, their robustness and reproducibility in terms of fabrication, combined with their very low charge offset drift and their higher temperature operation makes them good candidates for applications like current standards [14]. In this application, it is very useful to be able to operate several devices simultaneously, in parallel, to get a higher current value. Additionally, these devices operate as nano-field effect transistors (FETs) at room temperature. Even though these FETs have lower charge sensitivity than the SETs (100 to 1000 times less) they still have sub-electron sensitivity so they can still be used for charge electrometry experiments at room temperature. As an example, we have been working in using them to detect charge reconfigurations in bio molecules of interest.

The common feature of all these potential applications is the SET. The SET

consists of a piece of conducting material, called the island, connected to macroscopic

leads through tunnel junctions (see figure 1-3). The fact that the island is separated by

tunnel junctions means that the number of electrons on it is an integer number. It also

means that electrons can tunnel onto and off of it only in units of one. So, for current

to go through such a device electrons must tunnel on the island from one lead and

tunnel off through the other. If the total capacitance of this island is C_Σ, the amount of

energy needed to add an electron to the island will be $e^2/2C_\Sigma$. If, also, the thermal

energy is less than this value, it will be energetically unfavorable to add an electron,

for small bias voltages. Therefore there will be no current through the device; this

condition is called "Coulomb blockade". If we add a gate electrode, it turns out [15]

that the current through the device is a periodic function of the gate voltage. A single

period corresponds to adding one electron to the plate of the gate capacitor. We have,

then, a device that is very sensitive to charge redistributions that are capacitively

coupled to the SET island. A detailed description of the operation of an SET will be

given in chapter 4.
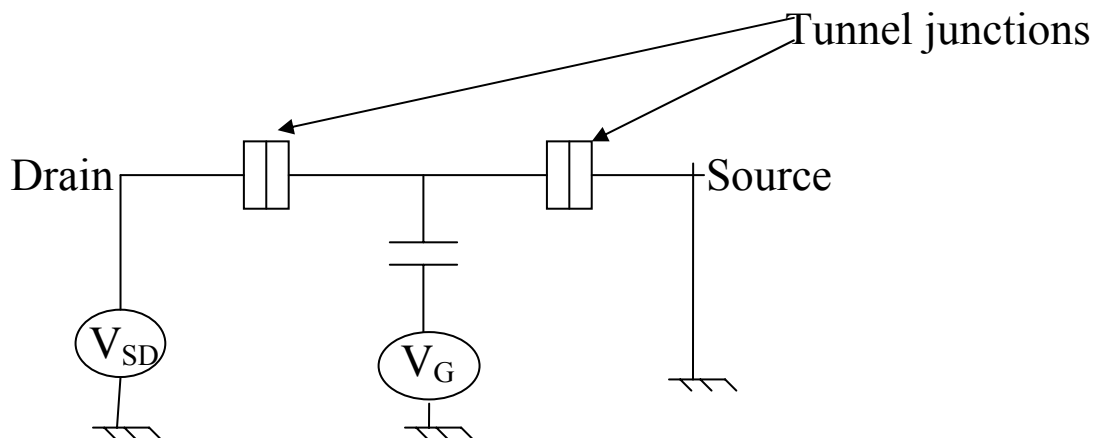
Figure 1-3 Circuit representation of an SET

Unfortunately SETs suffer from two major disadvantages. The first is that the temperature of operation is usually well below room temperature [16]. This is due to the fact that the total capacitance of the Coulomb island cannot take arbitrarily low values. The second one is called the charge offset Q_0 [16] and the charge offset drift $Q_0(t)$ [17]. It has to do with the fact that, due to the periodic characteristic curve and the excellent charge sensitivity, the phase of the characteristic curve shifts randomly from device to device and in time, due to charges moving around the device. The charge offset drift (Q_0) is a very low frequency phenomenon that affects the device operation in the time scale of hours and days and is different from the broadband noise of the device. Both these points will be discussed in some detail in chapter 4.

Our work focuses on the creation of SETs with better performance. We focus on silicon devices because we have found that they can be operated at higher temperatures and they have a much lower charge offset drift [18, 19]. They are less sensitive to electrostatic damage than metallic SETs. They can also readily be integrated in circuits including charge qubits based on silicon solid state devices. Our devices have been fabricated by our group (a new fabrication source) and have a novel design, incorporating tunable barriers. In chapter 5 I will demonstrate their operation as SETs, and reproduce the small charge offset drift observed previously in devices fabricated by the NTT group, indicating that this is, in fact, a robust characteristic of Si devices.

1.4: Summary of thesis

In chapter 2 of this thesis, I will present the problem of electrical breakdown of air for small electrode separations, along with a literature review of the subject. I will then describe our method for fabricating and controlling the distance between the electrodes of the capacitor used to take the measurements. Finally, there will be a presentation of the experimental results along with a discussion of them. The advantages of our method are: (1) the ability to measure the distance between the two conductors before each measurement and vary it in a range between 400 nm and 45 μm, (2) the use of a parallel plate geometry with a large plate area to distance ratio, which will produce nearly parallel field lines, and (3) the reduced surface roughness of the Au films used compared to typical bulk metal conductors commonly used in previous experiments. The results of this chapter have been published in ref. [20].

In chapter 3, there will be a presentation of the theory used to interpret electrical breakdown, which includes Paschen's law and field emission of electrons. Following that, there will be an analytical comparison between the predictions of this standard theory and our experimental results. The chapter will conclude with a detailed discussion of our results. From these I have concluded that the standard theory of this field cannot predict the results of our experiment. Therefore a new theory is needed in order to explain experimental results similar to ours. The work presented in this chapter has resulted in publication [21].

In chapter 4, the theory of SET devices will be discussed. The problem of the charge offset drift will be defined. A literature review of SETs generally, and specifically of silicon-based SETs, will be given.

Chapter 5 will introduce the silicon devices. The experimental setup will be described and the results of our measurements will be presented both for room and low temperatures. These results demonstrate our ability to fabricate and operate Si-based tunable barrier SETs. They also show that the charge offset drift $Q_0(t)$ is very small in these devices, fabricated in a different fabrication facility from previously demonstrated devices. I will conclude with a discussion on possible future directions for research with these devices. The experimental results presented in this chapter are being prepared for publication in [22].

Chapter 2: Breakdown of air: Experiment

2.1: Introduction

The value of the breakdown voltage of air for a specific range of electrode separations determines whether our capacitance experiment is feasible, as mentioned in the previous chapter. Besides this specific application, the understanding of electrical breakdown of air between electrodes that are separated by very small gaps is important for other technological reasons. In the microelectronics industry circuits are becoming increasingly dense. In micro electro-mechanical systems (MEMS), for example, spacing between conductors is of the order of a few micrometers, or below. In these types of devices, high voltages (100- 200 V) are usually applied across such small gaps (a few μm) of air [23, 24]. Electrical breakdown, which leads to leakage currents, can be detrimental to their operation. Clearly, the knowledge of the value of the breakdown voltage and the parameters that affect it will be an important consideration for their design, as well as their operation. The value of the breakdown voltage for small electrode gaps can also be of interest in areas such as automobile electrical systems, or even circuit breakers designed for household use [25, 26].

Traditionally the measurement of the value of breakdown voltage in air was done for electrode separations on the order of centimeters. For these values of separations Paschen's law can be used to interpret the data. It describes the avalanche mechanism responsible for electrical breakdown for macroscopic separations between the

electrodes [27]. The electrode configurations used to measure such voltages range from two parallel wires to a wire or a sphere over a flat electrode [27]. The most common configuration is that of two spherical electrodes. This is the configuration for which the American Institute of Electrical Engineers quotes their standards for breakdown voltage of air as a function of electrode separation [Appendix E in ref. 27]. These values are quoted, as mentioned before, for electrode separations and sphere diameters on the order of centimeters. This regime is far from being relevant for the applications discussed in the previous paragraph.

Recently a small number of studies have been done in the regime of small (order of micrometers) air gaps [28-30]. The main conclusions of these studies were that for small separations between conductors, Paschen's law no longer applies. Also, the studies found device geometry and surface roughness of conductors play an important role. Device geometry determines the shape of the electric field lines between the two conductors. Complicated geometries such as needle-like electrodes produce electric fields that are non-uniform on the surface of the electrodes. Surface roughness determines the amount of amplification of the electric field on the surface of the electrodes. This amplification is necessary in order to explain the experimental results [25]. The combination of these two effects makes the interpretation of experimental results challenging.

I now describe in detail the literature work for electrical breakdown of air at small electrode gaps. In reference [28], the authors have measured the breakdown of air between Cr electrodes separated by 0.9, 1.0, 1.5, 2.0, 3.0 and 4μm. These electrodes were thin films of 100nm thickness, deposited on a glass substrate. The measurement

consisted of applying a slowly increasing DC voltage across them and monitoring the current. The value of current would increase rapidly after a certain value of bias and damage to the device would occur. That value was chosen as the breakdown value. The disadvantages of this method include the fact that the device geometry is far from a parallel plate capacitor since the value of separation between the electrodes is about an order of magnitude larger than the size of the electrode. Also the existence of the glass substrate will alter the configuration of the electric field lines. Finally, with this method, for each value of the separation the authors had to make a new device.

In reference [29], the authors used a mechanical system driven by micrometers to approach one electrode to the other. In this case, one of the electrodes was a Ag plate, and the second was an iron needle. The separation between the two electrodes was varied between 0.1 and 40 μm with increments of 0.1 μm. The fact that a needle-like structure was used makes the analysis of the electric field on the electrodes complicated. The arc breakdown in this work caused a large crater to appear on the Ag plate. This means that after each breakdown the true distance between the two electrodes was hard to determine and that the surface roughness of the sample increases.

In reference [30], two macroscopic electrodes were brought together using a mechanical system controlled by micrometers. The two electrodes were a plate and a sphere of 2 cm diameter, each. The current through the electrodes was monitored and the value of breakdown voltage was determined to be the value of bias for which there was an observable current. The separation between the electrodes varied

between 0.5 and 25µm. This method suffers from the limitations described in the previous paragraph, as well.

In order to understand the mechanisms of breakdown better in the regime where Paschen's law no longer applies, more experiments with simpler geometries are needed. In contrast to previous experimental methods, our method for measuring the breakdown voltage of air has the following improvements: (1) it allows us to measure the distance between the two conductors before each measurement and vary it in a range between 400 nm and 45 µm, (2) it has a parallel plate geometry with a large plate area to distance ratio, which will produce nearly parallel field lines and (3) the reduced surface roughness of the Au films used compared to typical bulk metal conductors commonly used in previous experiments. The average surface roughness of our Au films, as deposited on a sapphire substrate polished to an optical finish, is 6 nm.

2.2: Sample fabrication and assembly

Our samples are Au lines, 80 µm wide, deposited on sapphire substrates. A picture of a sample is shown in Fig. 2-1, along with a profilometer scan across the Au line. All samples have the same "horseshoe" pattern with large contact pads on each end, so that the measurement of the electrical continuity of the line is possible at any time during the experiment. This is important because the lines often become electrically discontinuous as a result of the breakdown. The samples are designed so that the final air gap capacitor would have the desired plate spacing without the use of

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complicated mechanical systems. SiO_2 is used as a spacer between the samples. Sapphire is used as the substrate because of its hardness, which allows the application of forces without significant bending. In addition, its transparency proves useful in the alignment of the final device.

The process for creating the samples was as follows:

1) I start with commercially available sapphire substrates of 22.5 mm diameter and 3.3 mm thickness.

2) A thin film, usually 80 nm thick, of SiO_2 is deposited with a PE-CVD method.

3) I spin-coat the sample with photoresist (5,000 rpm, 30 sec), and with exposure and development I remove the resist from where I want the pattern to be.

4) The sample is then dipped in HF until the SiO_2 under the openings in the resist has been etched away (usually for ~3 min).

5) A thin layer of Cr (about 3 nm thick) followed by a layer of Au (of different thickness each time) is then evaporated on the sample. Cr was used to promote adhesion to the substrate.

6) Liftoff of the metal on top of the remaining resist is done by placing the samples in acetone and sonicating for ~10 min.

After liftoff, Cr and Au are left only in the previously defined trench. The thickness of the Au film determines how deep the final trench is (a schematic of the final result appears in fig. 2-1). In the profilometer scan in Fig. 2-1, for example, that value was chosen to be 70 nm. The surface roughness of the Au film, as measured by AFM scans, was 6 nm on average, with a maximum peak-to-trough height of about 60 nm. An example of such an AFM scan on a wide area is shown in Fig. 2-2. The

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samples are then mounted on plastic supports with electrical leads. For electrical

contact I used Al-Si wire bonds, shown in Fig. 2-1.
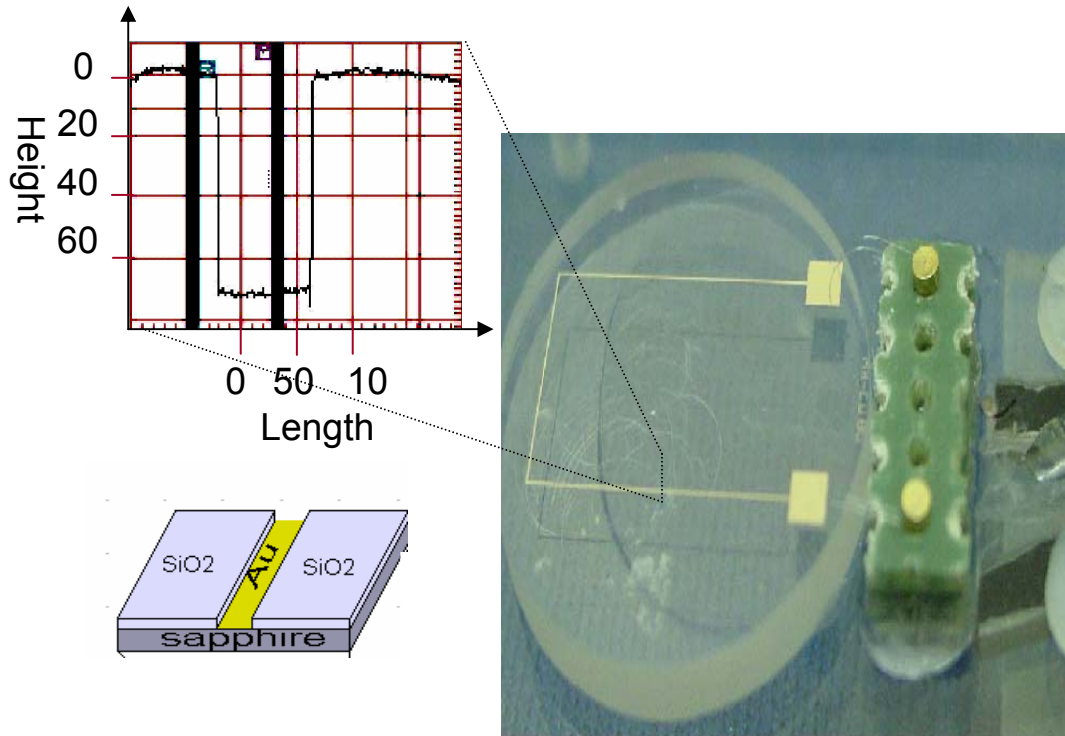
Figure 2-1 Picture of a sample. The Au line is 80 μm wide, with contact pads at each

end. There are wirebonds connecting the pads to Au posts on a plastic support. The

insert is a profilometer scan, perpendicular to the Au line. The depth of the trench was

chosen to be 70 nm for this sample. The schematic represents the structure across

which I scanned with the profilometer and is shown here for clarity.
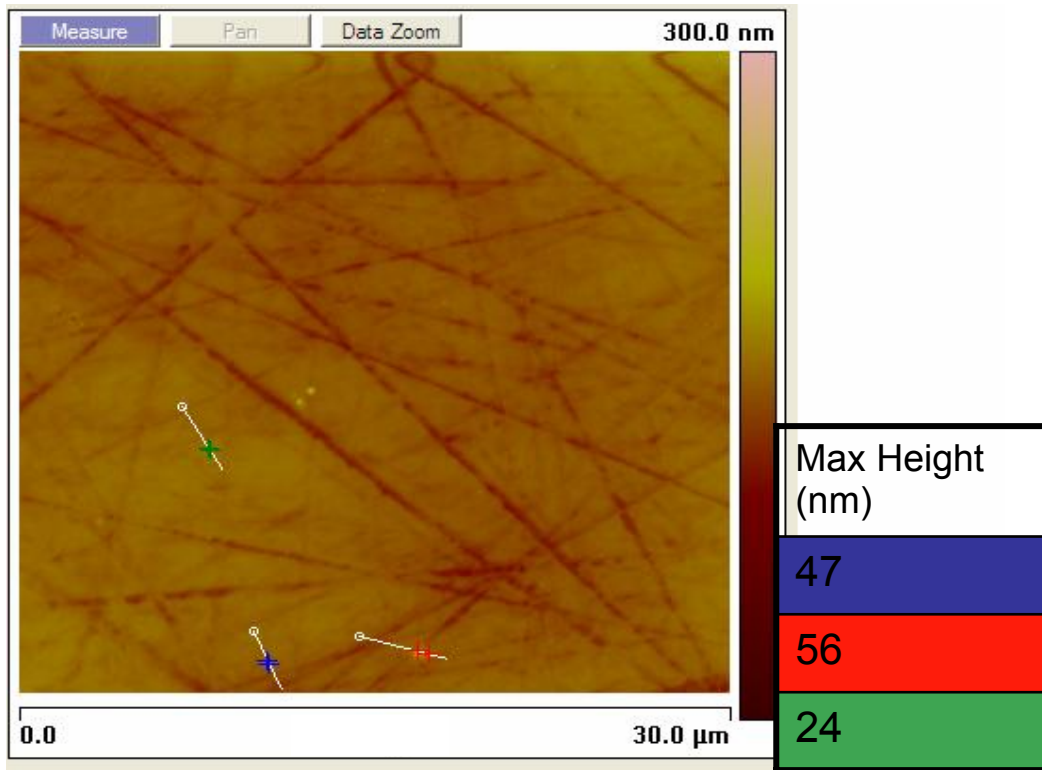
Figure 2-2 Example of an AFM scan of the Au surface. The line scans on the picture, which are indicated by white lines, were chosen to run over the spots of maximum height. The insert lists the values of the difference between the maximum and minimum height for each line scan.

To assemble the air gap capacitor I use two substrates. One substrate is flipped compared to the other and they are brought together so that the line on each one is perpendicular to the other. That creates two parallel plate capacitors for each device. A schematic of how the samples are brought together is shown in Fig. 2-3a. A picture of the final assembled device is shown in Fig. 2-3b. Because the sapphire substrates are not perfectly flat the ultimate goal of separation, which is defined by the thickness of the SiO_2, is never reached. Instead the separation between the two electrodes is

created by the substrates contacting each other close to the edges. So, the actual

separation between the Au lines is greater than the designed one. I used screws to

push down on the upper substrate in order to reduce this extra separation. It was this

fact that allowed me to vary the value of the separation between the electrodes. An

important consideration in this set up is the hardness of the sapphire substrate. It

allowed me to apply large forces without bending to the point where the Au lines

touched and the experiment became impossible. Finally, using this method, the

separation between the electrodes at the crossing points is different for the two

crossing points on the same device. This introduces errors that are discussed in

section 2.4.
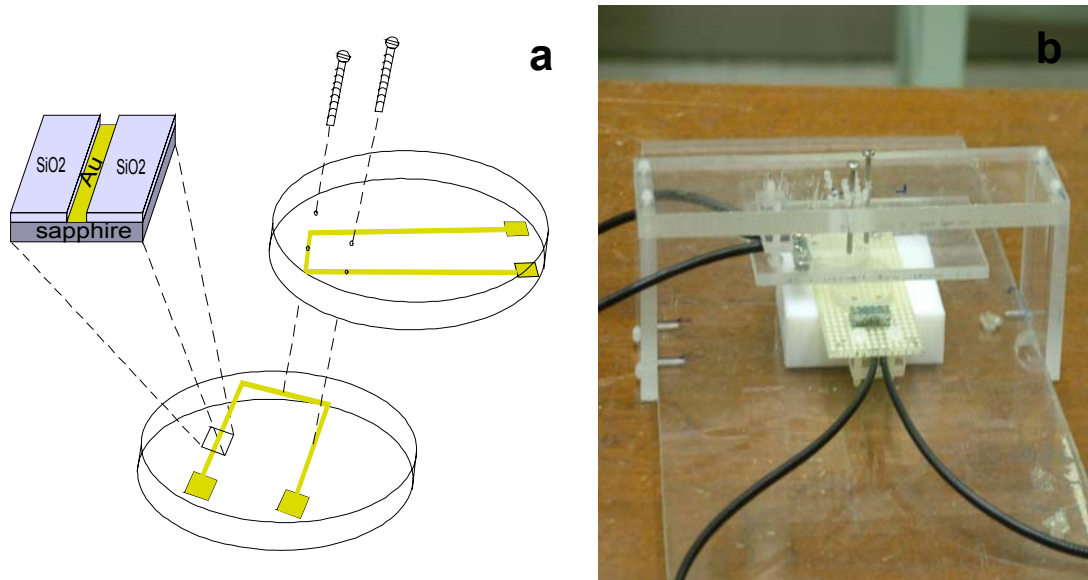
Figure 2-3 a) A schematic representation of two substrates coming together, forming

the air gap capacitors at each crossing point. b) A photograph of an assembled device.

Two substrates on plastic supports are brought together and pushed by metallic

screws.

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2.3: Using the value of the capacitance to ascertain the value of the plate separation

One weakness of all previous studies of air breakdown for small gaps is a lack of knowledge of the gap d between the electrodes before each measurement. I use a measurement of the capacitance between our electrodes to obtain a measurement of d.
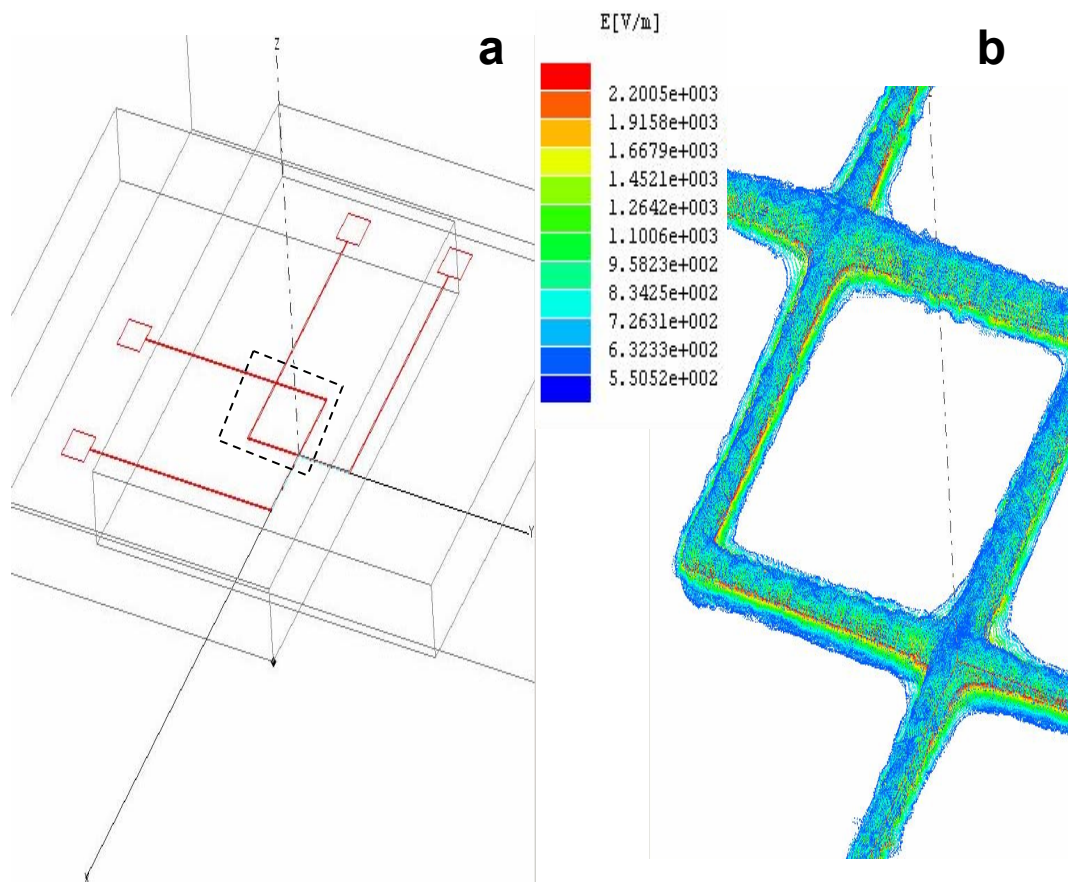
Figure 2-4 a) Simulated device structure. b) Example of results of simulation for electric field between the Au lines on the two substrates (blowup of dashed rectangle in a).

In order to understand how the capacitance between the two Au lines depends on the distance between them, I simulated the capacitance vs. separation using a commercial software package (Maxwell 3-D). In figure 2-4a, I show the structure I used to simulate our devices. Figure 2-4b is an example of the simulated electrical field between the Au lines for a given value of the separation. The results of the simulation for the capacitance are shown in Fig.2-5.
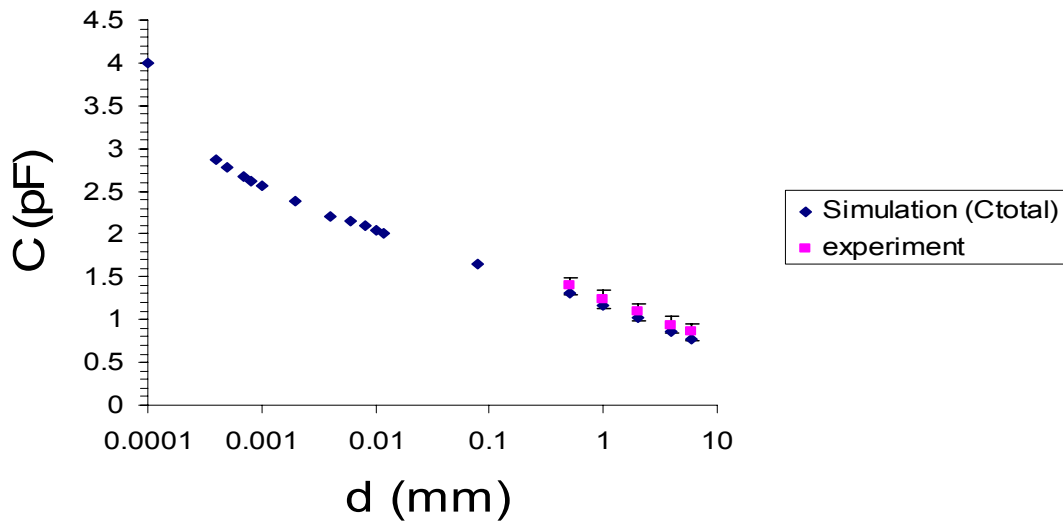
Figure 2-5 Capacitance (C) of the air gap capacitor as a function of electrode separation (d). The experimental data were taken by controlling the position of one of the electrodes with a x-y-z translator. The presence of the translator shifts the value of the capacitance and so an experimental uncertainty of ±0.1 pF is introduced. For spacings of 6 to 0.6 mm the experimental data agree with the simulation values, within the experimental uncertainties. I thus conclude that the simulation is an accurate description of the real capacitance down to 400 nm.

The capacitance of the device can be separated in two different parts. The first part is due to the parallel plate capacitor created by the crossing of the two Au wires. The second part is due to the capacitance between all other parts of each of the lines. For large separations the second part dominates. Below a separation on the order of the Au line width (80 μm), that part of the capacitance changes slowly with distance and the parallel plate part begins to contribute significantly to the total capacitance. For small separations, the parallel plate part dominates. The simulation shows that the electric field always has its maximum value in the area of the crossing between two Au lines.

I took two substrates that were brought together by the method described above and attached the top one to an x-y-z translator. I could thus control the distance between the two Au lines, the plates of the capacitor, with a precision of 1 μm. The capacitance of the system was measured using a capacitance bridge, which rejects stray capacitance caused by the wires. Special care was taken so that all cables used are electrically shielded. Also, all supports used were plastic, so that the value of the capacitance measured was not altered by stray fields. The capacitance vs. distance measurements are also shown in Fig. 2-5.

It is obvious that the data agrees with the simulation. From this, I conclude that by doing a capacitance measurement between the two Au lines, and using the simulation curve, I can accurately determine the distance between them. Furthermore, I can extrapolate this method to small values of separation, where a direct measurement of the distance is not possible. A capacitance measurement allows us to infer the

distance between the Au lines for all distances, in contrast to previous studies in the literature [28-30].

2.4: Measuring V_{break} as a function of d

Ideally, if two samples were brought in contact with the method described in section 2.2, the separation between the lines would be twice the distance between the upper surface of the SiO_2 and the Au film on the samples used. However, because the sapphire windows are not perfectly flat, that separation is, in reality, substantially larger. In order to bring the plates closer together, I bring the two samples in contact and then use screws to apply force over the regions where the lines cross.

For the determination of the value of the breakdown voltage, I want to measure the current through the capacitor as a function of the voltage applied to it. The circuit for the breakdown measurements consists of a DC voltage source, the capacitor and a 10 MΩ resistor in series. The specific choice for the value of the resistance was made as a compromise between having a resistance large enough to produce an easily measurable value of voltage across it for small currents and a value that is readily accessible in our laboratory. A voltmeter monitors the potential drop across the resistor in order to determine the current. A switch box allows us to change from a breakdown measurement to a capacitance measurement, which determines the value of the plate separation. A circuit diagram of this system is presented in figure 2-6.

Before each breakdown measurement, the substrates were taken apart and then put back together so that different parts of each of the two wires were used each time

as the plates of the capacitor. In addition, by changing the force on the screws the

separation between the plates of the capacitor was changed. No attempts were made

to control the humidity, temperature or composition of the air in the room, during this

experiment. As discussed at the end of chapter 3, this may be an important

consideration for future experiments.
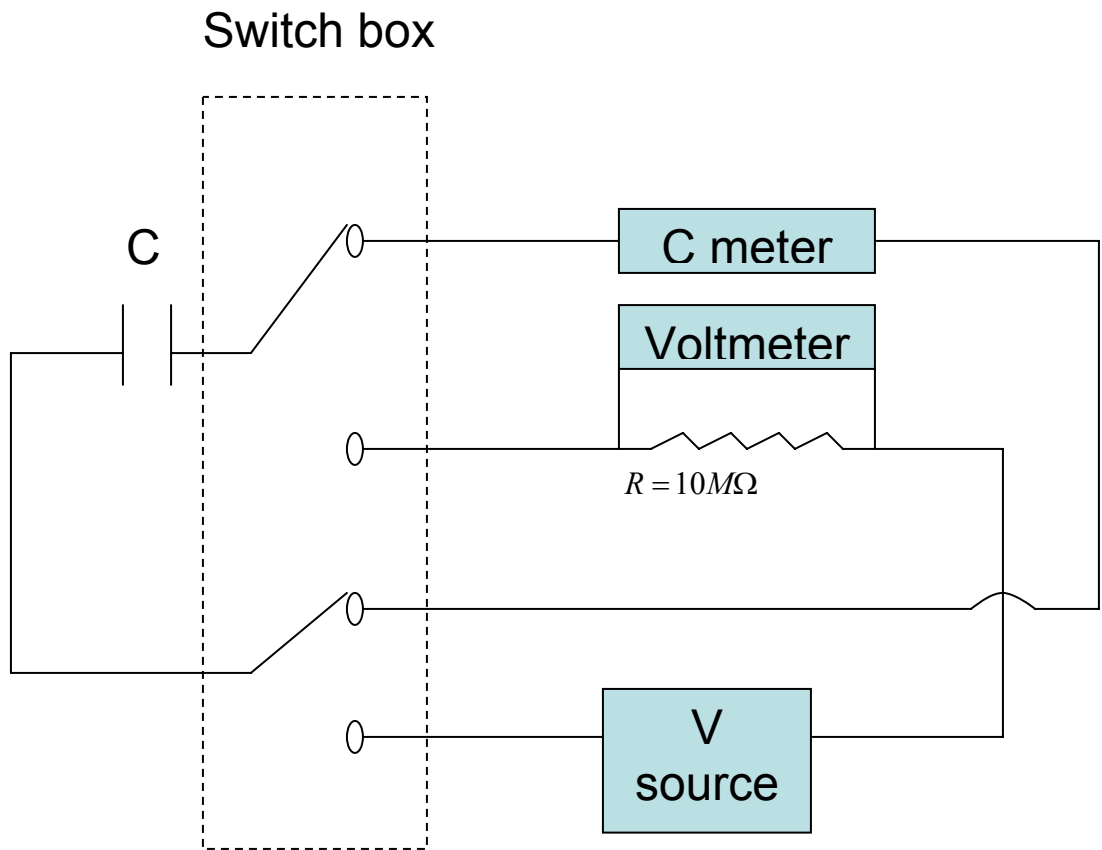
Figure 2-6 Circuit diagram of the measurement system. The switch box allows

changing the measurement from capacitance to breakdown.
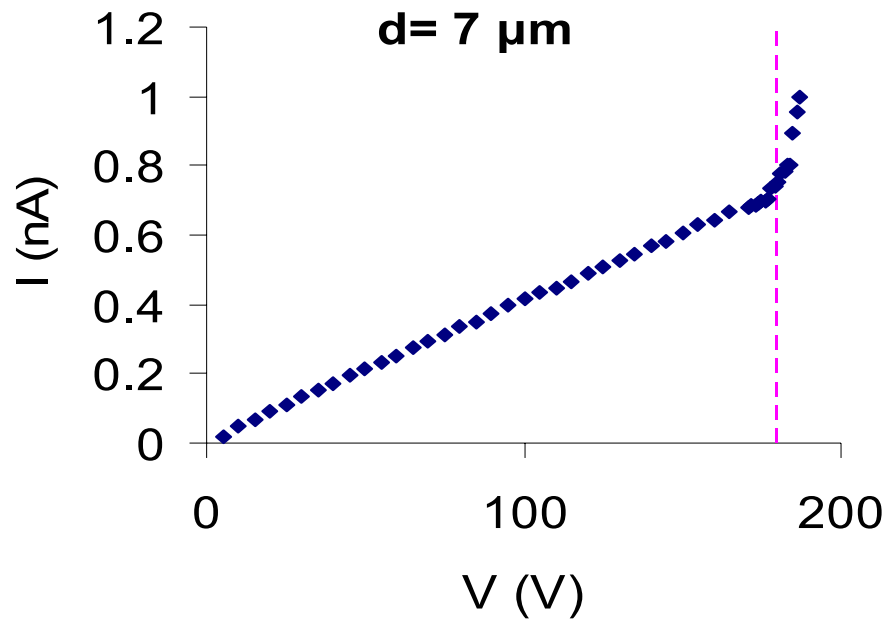
Figure 2-7 Current through the 10 MΩ resistor in series with the capacitor, as a function of the applied voltage from the DC voltage source. The value of the electrode separation is 7 μm. For this value of separation, the value of the breakdown voltage is taken to be 185 V. The linear part of the curve is due to a leakage of approximately 2.5×10^{11} Ω.

A measurement of potential drop across the resistor vs. applied voltage was made for each different spacing, so that the current through the capacitor vs. applied voltage is determined. An example of such a measurement is given in Fig. 2-7 for $d = 7$ μm. The value of applied voltage at which the current through the resistor becomes non-linear is chosen to be the value of the breakdown voltage. Clearly, it would be

preferable to have more data at larger voltages. However, the value of the current increased very rapidly for higher voltages resulting in the destruction of our electrodes.

The results from the capacitance measurement reflect an average separation between the two substrates used. This is due to the fact that for separations larger than 500 nm, the capacitance is not dominated by the capacitance of the two crossings. Various parts of the metallic lines contribute in significant measure to the total value of the capacitance. With that in mind, I have estimated the possible deviations of the two separations at the two crossings with respect to the average separation.

I estimate these deviations for a variety of possible geometries of the substrates and uncertainties due to photolithography and alignment. The geometries considered are the two substrates having positive and negative curvatures. I tried a variety of combinations of putting together two substrates with different curvatures. I also considered the possibility of the two substrates being put together with a relative angle. I assigned the uncertainty as the limits of the typical range of separations; these are represented in Fig. 2-8 as error bars. Finally, I note that uncertainties of this type seem unavoidable in planar geometries if I use a measurement of capacitance in order to determine d since, as mentioned before, the value of the capacitance of the leads play as important a role as the capacitance of the crossings, down to very small separations.

2.5: Results and discussion

I used the method described above to measure the breakdown voltage of air, in atmospheric pressure, for separations of the electrodes ranging from 400 nm to 45 μm.

Before taking the data, I measured the breakdown voltage at 4 μm of separation 4 times. The results were within 10 % of each other. I then took data for each different separation once. The results are shown in Fig. 2-8. The solid line in fig. 2-8 represents Paschen's curve which will be explained in the next chapter. It predicts that the absolute minimum value for the breakdown voltage of air, for uniform fields, is 360V [27]. It is shown here to clearly demonstrate that the results for $d < 10$ μm have a qualitatively different behavior.

In conclusion, I have developed a new method for measuring the breakdown voltage in air, for electrode separations of 400 nm to 45 μm. Our method enables us to monitor the actual value of the separation before each measurement. It also approaches the geometry of an idealized parallel plate capacitor, because of its very large aspect ratio (80 μm by 80 μm electrodes separated by as little as 400 nm) and because of the small surface roughness (avg. 6 nm).
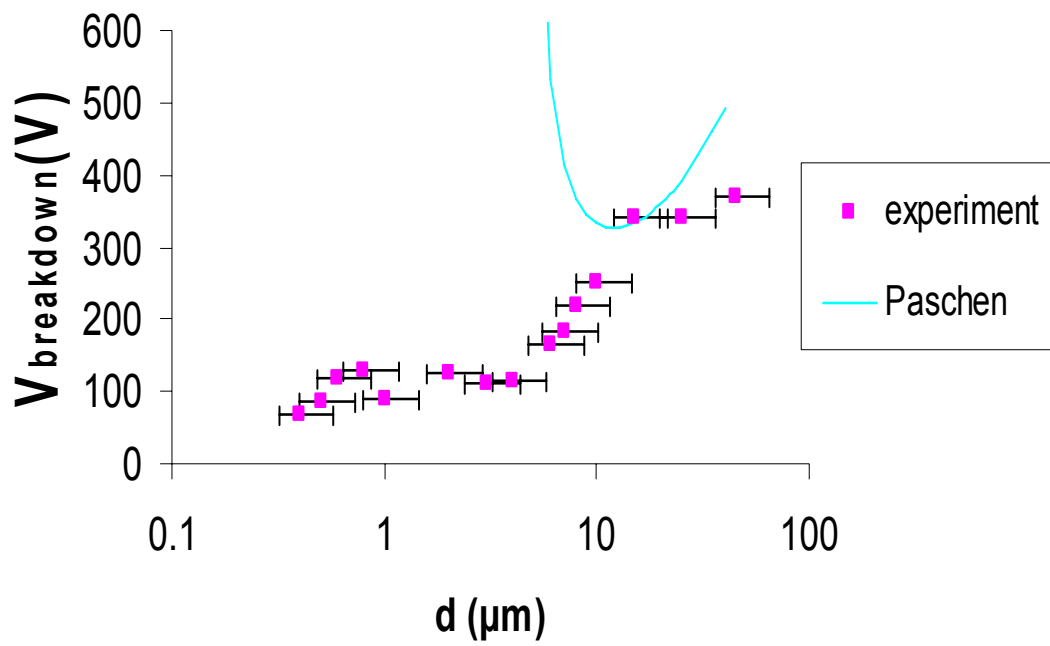
Figure 2-8 Data for breakdown voltage of air as a function of electrode separation. The error bars represent the statistical uncertainty due to geometrical factors (see text). The solid line is Paschen's curve.

Chapter 3: Breakdown of air: Comparison to standard theory

3.1: Introduction

As mentioned in the previous chapter, the results for the electrical breakdown of air deviate from Paschen's law for small electrode separations (see fig. 2-8). When the separation between the electrodes is decreased to a length scale comparable to the mean free path of an electron in air ($\sim$ 500 nm), Paschen's law is not expected to be applicable [25]. The experiments described in the introduction of the previous chapter show that the value of the breakdown voltage decreases almost linearly for values of electrode separations below a certain value. This is qualitatively different from Paschen's law which predicts a fast increase for the value of breakdown voltage for small electrode separations. In fact, in this regime breakdown values vs. separation are very similar to breakdown curves for vacuum [31-33]. These two facts, that the breakdown voltage decreases with gap and that its value is comparable to the value for vacuum breakdown (breakdown between two electrodes separated by vacuum), suggest that for d< 500 nm the process for air breakdown is most likely the same as for vacuum breakdown, which is field emission of electrons from the metallic electrodes. However, in typical experiments for both air and vacuum, the value of electric field at which the field emission is observed is as much as a factor of 100 smaller than the value predicted by theory [31-33]. That discrepancy is thought to be the result of local field amplification on the surface of the electrodes due to

roughness. In most published work in the field, researchers assume, but do not experimentally verify, the existence of features on the surface of the electrodes that would explain the observed results.

There are also a number of studies [34-40] that examine the surface roughness of the electrodes. In these publications the surface of the electrodes used for breakdown measurements are examined before and after breakdown. Unfortunately, the existence of surface roughness is considered evidence enough for field amplification and no quantitative measurement of surface features is made. No study makes a quantitative comparison between the predictions of the theory and the actual surface roughness observables.

In our experiment I measure the breakdown voltage in air for separations between 400 nm and 45 μm. For the range of $d< 10$ μm I observe large deviations from Paschen's curve and the data can be fit by the field emission theory. I focus on this range where I expect that field emission of electrons is the dominant effect. In this chapter, I first describe Paschen's law, and then the theory of field emission of electrons along with field amplification on the surface of the electrodes. I use the standard theory to predict the geometry of protrusions due to surface roughness that would enhance the electric field on the surface. I then use AFM measurements to try to locate such surface features and show that no such protrusions exist. I point out that such a comparison has not been done before. From our results I can show that there are 3 different reasons for coming to the conclusion that the field amplification theory does not explain our experiment.

3.2: Paschen's law

First I present a description of the theory used to describe air breakdown. Traditionally, experiments for air breakdown were done for separations of the electrodes in the cm range. For that range, the theory of Townsend discharges can explain experimental results adequately. By understanding this theory I can show why I would in fact expect that it would not hold for most of our results. The discussion in this section follows reference [27].

I start with a system of two parallel plate electrodes separated by a distance d filled with air. In this configuration, assuming a uniform electric field E everywhere, I want to calculate the current density that will result from the ionization of molecules due to electron collisions. Each electron leaving the cathode will produce a certain number of electron ion pairs due to collisions with air molecules on its way to the anode. The positive ions will return to the cathode where they will produce more electrons through collisions with the metal surface. If γ is the number of electrons emitted from the cathode for each of those arriving ions, when γ times the number of electrons arriving becomes one or greater, the process becomes self sustained. This is what is called avalanche breakdown.

The energy that an electron receives from the electric field is a function of the electric field strength E and of the distance it travels between collisions. If α designates the number of ionizing collisions per cm of path for one electron in the direction of E, then

$$\alpha = \frac{f(EL)}{L} \quad ,$$

where L is the mean free path of the electron. α is called the first Townsend coefficient.

If we have $n(x)$ electrons per second traverse a surface of 1 cm^2, then the number of new ions created through the ionization process along a path dx per second will be:

$$dn(x) = \alpha n(x) dx \Rightarrow n(x) = n_0 e^{\alpha x},$$

if n_0 electrons are emitted by the cathode per cm^2 per second. The number of electrons reaching the anode per cm^2 per second will be:

$$n = n_0 e^{\alpha d}.$$

Suppose the energy needed to ionize an air molecule is eV_i. Then an electron would have to be accelerated for a distance $x = \dfrac{V_i}{E}$ before gaining enough energy for an ionizing collision. For a mean free path L of the electron, it turns out [27] that the probable number of ionizing collisions per cm of path is

$$\alpha = \frac{1}{L} e^{-\frac{V_i}{EL}}$$

Also if we use the dependence of the mean free path on pressure p [27], we have:

$\dfrac{1}{L} = Kp$, where K is a constant. So

$$\alpha = Kp e^{-\frac{Bp}{E}} \tag{3.1}$$

where $B = KV_i$.

Each ionizing collision will produce an electron (as considered above) but also a positive ion. These ions will be accelerated by the electric field towards the cathode where they will cause electrons to be emitted from the metal through collisions. As mentioned before, γ is the number of electrons emitted from the cathode for each

arriving ion. Also, as shown before, one electron leaving the cathode will create e^{ad}

pairs of electrons and ions on its way to the anode. Then γe^{ad} is the number of

electrons produced from the cathode as a result of these ions colliding with it. If that

number becomes one or more the process is self sustained and spark breakdown

occurs. This situation corresponds to

$\gamma e^{ad} = 1$ or

$$\ln(\frac{1}{\gamma}) = \alpha d .$$

We have assumed that $e^{ad} \gg 1$, or that the electrodes are far enough apart so that the

electrons have a large number of collisions on their way to the anode. This

assumption limits the validity of this theory in terms of the electrode separation d ($d >$

$1/\alpha > L$).

The total number of electrons arriving at the anode per cm^2 per second will be

[27]:

$$n = \frac{n_0 e^{ad}}{1 - \gamma e^{ad}} \tag{3.2}$$

For the condition for breakdown described above we also see from eq. (3.2) that n,

which is equivalent to the current density J at the anode, goes to infinity.

Also, if we define the spark or breakdown potential, V_s, to be $E_s = V_s/d$, then from eq.

(3.1), we get

$$\alpha = Kpe^{-\frac{Bpd}{V_s}}$$

and solving for V_s,

$$V_s = \cfrac{Bpd}{\ln\left[\cfrac{Kpd}{\ln(1/\gamma)}\right]} \qquad (3.3)$$

The breakdown potential is only a function of pressure p and electrode separation d. The experimental curve that follows this law is usually called the Paschen curve and this theoretical relation is often referred to as Paschen's law.

One of the conclusions one can derive from examining the equation for the breakdown voltage is that V_s has a minimum value. In particular

$$V_{sm} = 2.718\frac{B}{K}\ln\frac{1}{\gamma}.$$

For $p=$ 1 atm $V_{sm}\approx$ 350 V. This means that according to this theory there can be no breakdown for values of voltage below this minimum value, no matter what the separation of the electrodes are. This is clearly contrary to our experimental results and those of other studies for small electrode separations.

Paschen's law assumes that the electron and ions have enough distance between the electrodes to be accelerated by the electric field in order for the statistics described above to be relevant. Clearly as one reduces the separation of electrodes so that it approaches the mean free path of an electron in air, the above equations can no longer predict the values of the breakdown voltage. For this range of separations, where Paschen's law no longer applies, the standard understanding of breakdown comes from the theory of field emission of electrons.

3.3: Field emission of electrons

In this section, I present the theoritical framework that underpins the standard understanding of breakdown at low separations between two planar surfaces. Electrons in a metal see a surface potential barrier due to the material's work function φ and their image charge. When a field exists, this barrier is deformed. If we consider z to be the direction perpendicular to the surface then the potential energy the electrons "see" is

$$E_e = E_F + \varphi - \frac{e^2}{4z} - eEz$$

for $z > z_C$ and

$$E_e = 0$$

for $z < z_C$, where $E_e(z_C) = 0$, E_F is the Fermi energy of the material and E is the applied electric field. A schematic representation of such a barrier appears in figure 3-1. For strong enough fields there is a finite probability of electrons tunneling through it. This is called field emission of electrons [41, 42].
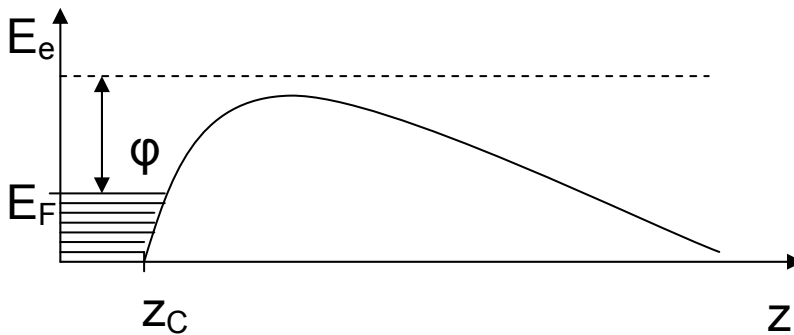
Figure 3-1 Electrostatic barrier on the surface of a conductor with an applied electric field perpendicular to its surface.

It is possible to calculate the tunneling probability for the electrons on the surface of the metal using the WKB approximation and the shape of the potential barrier and therefore calculate a current density. For field emission the current density (J) as a function of the applied electric field (E) is given by the Fowler-Nordheim equation [41]

$$J = DE^2 \exp(\frac{-B\varphi^{\frac{3}{2}}}{E})$$ (3.4)

where $D = \dfrac{e^3}{16\pi^2 \hbar \varphi t^2(y)}$, $B = \dfrac{4}{3e}(\dfrac{2m}{\hbar^2})^{\frac{1}{2}} \upsilon(y)$.

From [41]:

$$\upsilon(y) = 0.956 - 1.062y^2,$$

$$t(y) = 1.044,$$

$$y = 3.79 \times 10^{-4} E^{\frac{1}{2}} \Big/ \varphi ,$$

Where E is in V/cm and φ is the work function of the metal in eV.

Equation (3.4) shows that for current densities of 10^2-10^3 A/cm^2, which are typical in breakdown experiments, the electric field has to be 3-6$\times 10^7$ V/cm.

From experimental results of breakdown in vacuum [31-33] (where the breakdown mechanism is field emission of electrons) the value of the field required to cause breakdown is significantly lower (in some cases by more than a factor of 100) than the value predicted by the Fowler-Nordheim equation. In order to explain this phenomenon, a microscopic enhancement β of the local electric field is introduced. This enhancement is thought to be the result of the existence of protrusions on the surface of the metal. The value of the electric field will be

$$E = \beta \frac{V}{d}, \tag{3.5}$$

where d is the distance between the metallic surfaces between which V is applied. If

we write $J = \frac{I}{A}$, where I is the current and A is the area of the protrusion, we can

rewrite equation (3.4) as:

$$\frac{I}{V^2} = D \frac{A\beta^2}{d^2} \exp[\frac{-B\varphi^{\frac{3}{2}}d}{\beta V}] \tag{3.6}$$

Plotting $\ln(I/V^2)$ vs. $1/V$ is the common way of determining the value of β, assuming

the value of ϕ is known. The slope m of such a plot will be, from eq. (3.6):

$$m = \frac{-B\varphi^{\frac{3}{2}}d}{\beta} \tag{3.7}$$

and the y-intercept

$$y_{int} = \ln\left(\frac{DA\beta^2}{d^2}\right) \tag{3.8}$$

The quantities in the natural logarithms have been made uniteless by multiplying with

the appropriate units.

The local field enhancement factor β depends on the geometry of the protrusions

on the metallic surface. A protrusion will cause electric field to concentrate at its tip

in an effort to be perpendicular to the metallic surface. Solving Maxwell equations for

a hemispheroid protrusion (Fig. 3-2) and imposing the correct surface boundary

conditions (for a dc applied field) [43], the field amplification factor β as a function

of the height to base ratio (c/b) is shown in Fig. 3-2 (Note that for c/b~20, we have

β~100, which would allow for interpretation of previous experimental data [25]).
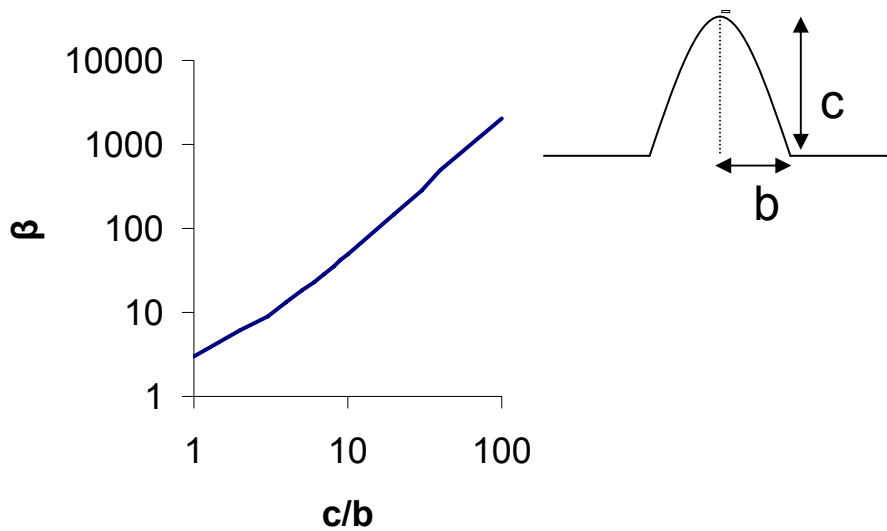
Figure 3-2 Graph of the dependence of the field amplification factor β on the height

to base ratio of a hemispheroid protrusion of height c and base length b. (see [43])

3.4: Breakdown results

I use the method I have described in the previous chapter to acquire the values of

breakdown voltage for different values of electrode separation. The separation range

is from 400 nm to 45 μm. The material used for the electrodes is thermally deposited

thin films of Au, for which ϕ = 5 eV [44]. The measurement consists of monitoring

the current through the air gap capacitor (area of plates is 80 μm by 80 μm) as the

applied voltage is increased. The value of the breakdown voltage is chosen to be

where the current starts increasing non-linearly (Fig. 3-3a). The linear part of this

curve can be attributed to leakage. When I take the two electrodes far apart, a

measurement of *I* vs. *V* shows the same linear behavior with no non-linear part. I can then define a leakage resistance *R* to account for this linear part that is independent of the breakdown part of the data. If I subtract the leakage current I_{leak}= *V*/*R* from the data in fig. 3-3a I get the results in fig. 3-3b which I will consider to be the current due to breakdown.

The data acquired with this method are shown in fig. 3-4. For separations below 10 μm the data deviate from Paschen's curve (Paschen's curve is drawn for reasonable values of its parameters). Below 10 μm the main cause of breakdown must be field emission of electrons since this is the only other possibility, given that the separation of the electrodes is large enough to assume that direct tunneling is negligible. This curve is typical of the field. Much of the work in the literature stops here, assuming surface roughness and β factors that would explain the experimental data (i.e. $\beta \sim 100$). In what follows I aim to explicitly test these assumptions.

In order to predict what ranges of β factors would satisfy the requirements of the observed current as well as the breakdown voltages, I plot $\ln(\dfrac{I-I_{leak}}{V^2}\dfrac{V_0^{\,2}}{I_0})$ as a function of 1/*V*, where $I_0 = 1$ nA, $V_0 = 1$ V. I then fit to get the value of the slope (two examples of this are shown in Fig. 3-5a and 3-5b). The fact that I can fit the data using the Fowler-Nordheim equation suggests that the cause for breakdown, in this regime, is, in fact, field emission (this is also a standard argument in the literature). Using equation (3.7) I get a value of β for each data point. Error bars represent the uncertainties in Fig. 3-6a. The big value of uncertainty in the calculation of areas *A* is the result of the fact that I am making a large extrapolation in Fig. 3-5 to 1/*V*=0.

41
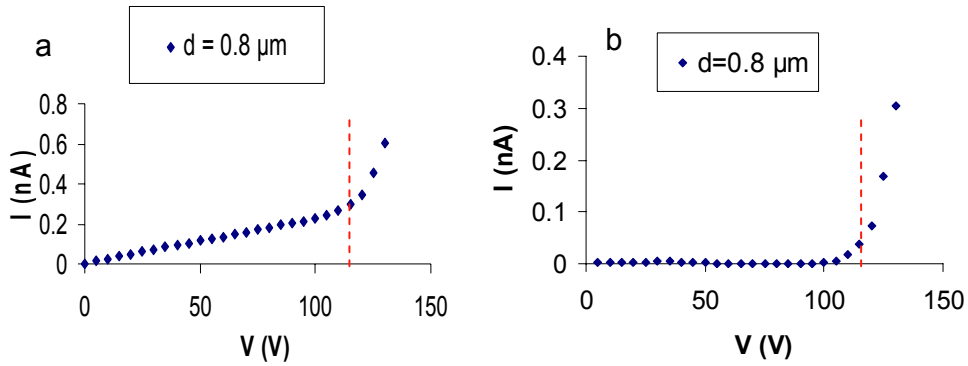
Figure 3-3 a) Current (I) vs applied voltage (V) through the capacitor used for breakdown measurements. The data are for d= 0.8 µm. V_{break} was chosen as 115 V (I vs. V becomes non-linear). b) I-I_{leak} vs. V for the same value of d.
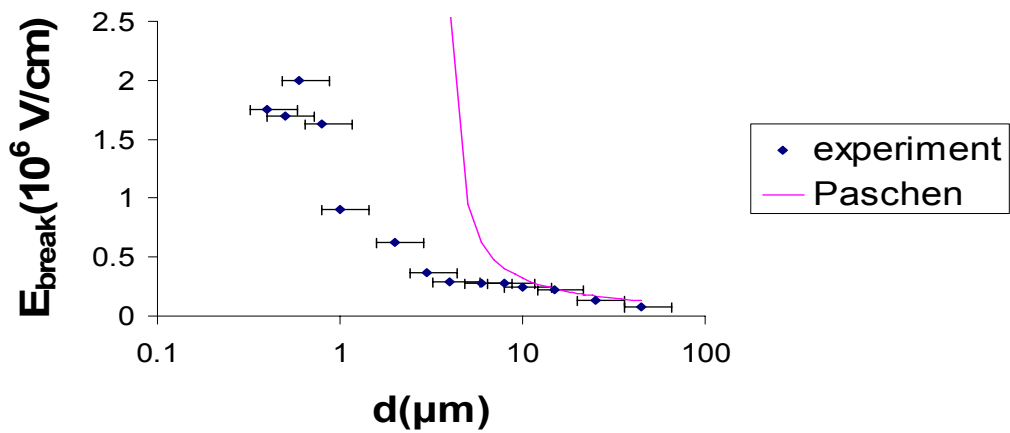
Figure 3-4 Breakdown electric field as a function of electrode separation (d). The points are experimental results. The red curve represents Paschen's law. Note that, as is standard in the field, E is 25-30 times smaller than 5×10^7 V/cm.

I then use the value of β to calculate the area A of the protrusion responsible for the observed current. I can do that by using the measured values of I and V and equation (3.6). The results of those calculations appear in fig. 3-6b. I note that some values of A (for d= 7 and 10 µm) are unphysical; they are larger than the area of the electrodes. This is our first piece of evidence that the theory does not explain our data.
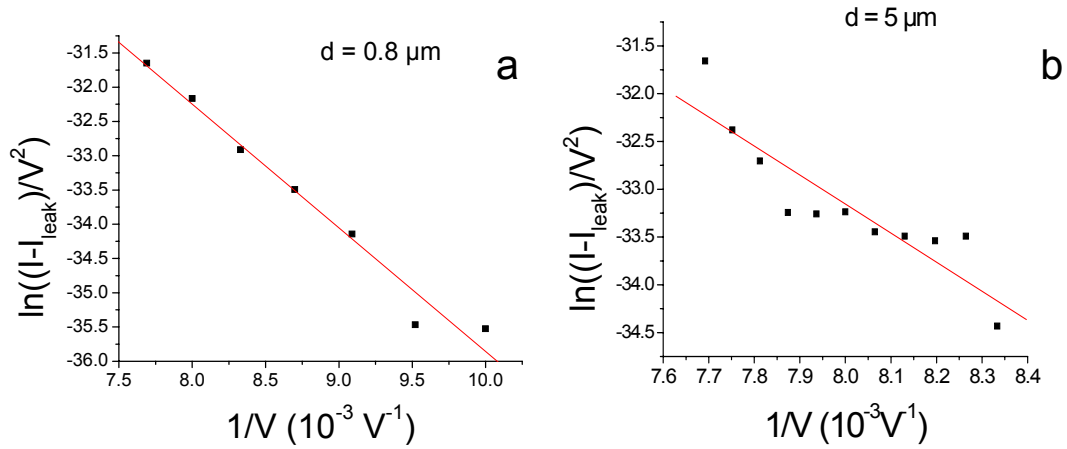
Figure 3-5 $\ln(\dfrac{I-I_{leak}}{V^2}\dfrac{V_0{}^2}{I_0})$ vs. $1/V$ for a. 0.8 µm of separation and b. 5 µm of separation. The red line is a linear fit with slope for a. -1800 V and for b. -3000 V.

43
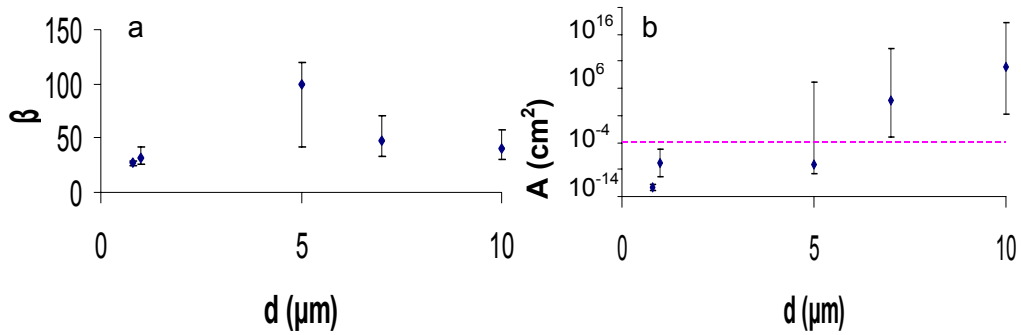
Figure 3-6 a) Roughness enhancement factor β as a function of electrode separation, b) emitting area A as a function of electrode separation. In b, the horizontal line represents the maximum area given the device geometry. Note that 2 sets are unphysical. This is our first piece of evidence against the theory.

3.5: Surface roughness results

Up to this point, I have followed the standard analysis in the literature of the experimental data. After the calculation of β and the area of the responsible feature, it is generally assumed in this field that such a feature in fact exists on the surface of the electrodes. The fact that I end up with unphysical calculated values of A suggests that further analysis is in order. Thus, I use the theory in order to get predictions of the actual sizes of the features thought to be responsible for the field amplification on the surface of our electrodes. In contrast to previous studies, I then try to locate

features of specific size, using an AFM. I can then directly compare the predictions of the theory with an experimental observable.

Knowing the values of β and the corresponding area of the protrusion, from the analysis in the previous section, I can use Fig. 3-2 to calculate the height of the protrusion, c, as a function of its base dimension, b. I am assuming $A = b^2$. I report this in Table 3-1, for values of area A, and so b, that are physically possible. I have excluded the data for d= 7 and 10 µm because for these cases the theory predicts unreasonable values of A (Fig. 3-6b).

d (µm)	0.8		1		5	
	Min	Max	Min	Max	Min	Max
Base b (nm)	1.1	20	65	22000	120	50×10^{12}
Height c (nm)	7.7	140	455	154000	1320	50×10^{13}

TABLE 3-1 Calculated minimum and maximum dimensions of protrusions necessary for observed currents at different electrode separations. The minimum and maximum values correspond to the range of areas A in fig. 3-6b. I note that the maximum values for d= 5 µm are also unphysical.

I have used the theory to predict the sizes of the protrusions necessary to explain our data. I use an AFM to look at the surface roughness of our metallic electrodes and to try to locate the protrusions with the predicted geometry. For this part an AFM with a 20 nm radius tip was used, in tapping mode. The AFM pictures were taken on samples before the breakdown measurements were performed. The results presented here (Fig. 3-7 and 3-8) are typical. In order to check reproducibility, I looked at electrodes after breakdown measurements, using a Scanning Electron Microscope (SEM). The electrodes are smooth, with no visible imperfections, except in discrete regions of size ~ $(100 \ \mu m)^2$. Since these regions are not coincident with the capacitor overlap regions where the electric field E is highest, so breakdown occurs, I can conclude that the capacitor electrode surfaces were not altered during the measurement.

Initially I take scans of large area as in Fig. 3-7. I then concentrate on areas where there are no visible protrusions (area inside dotted rectangle in Fig. 3-7). For this area, similar to almost all of the samples' total area, we see that the average roughness is 6 nm. The maximum deviation between low and high points for such areas is R_{max}= 69 nm. If protrusions exist in this area their height is not larger than 69 nm.

I then check visible protrusions individually. Three examples are given in fig. 3-8. I have done line scans over what seemed to be protrusions of large height. As is clear from fig. 3-8, the height to base ratio is much smaller than what is required by the theory. Table 3-1 gives the minimum and maximum base and height dimensions for the predictions of the theory not excluded by the value of A.

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All visible protrusions appear to have $c/b<1$. If there are any features with the appropriate c/b ratio, their base dimensions are so small that they are not individually discernible. Referring back to fig. 3-7, I see that the aggregate of all such protrusions would have a maximum height of 70 nm. That would mean that the only possible agreement with the theory can be for the data of 0.8 μm separation. In all other cases, the predictions of the theory are either unrealistic ($A> (80 \text{ μm})^2$), or the required dimensions of the protrusion responsible for the field amplification are outside the range of those found with the AFM scans. This is the second piece of evidence that the theory cannot explain our data.
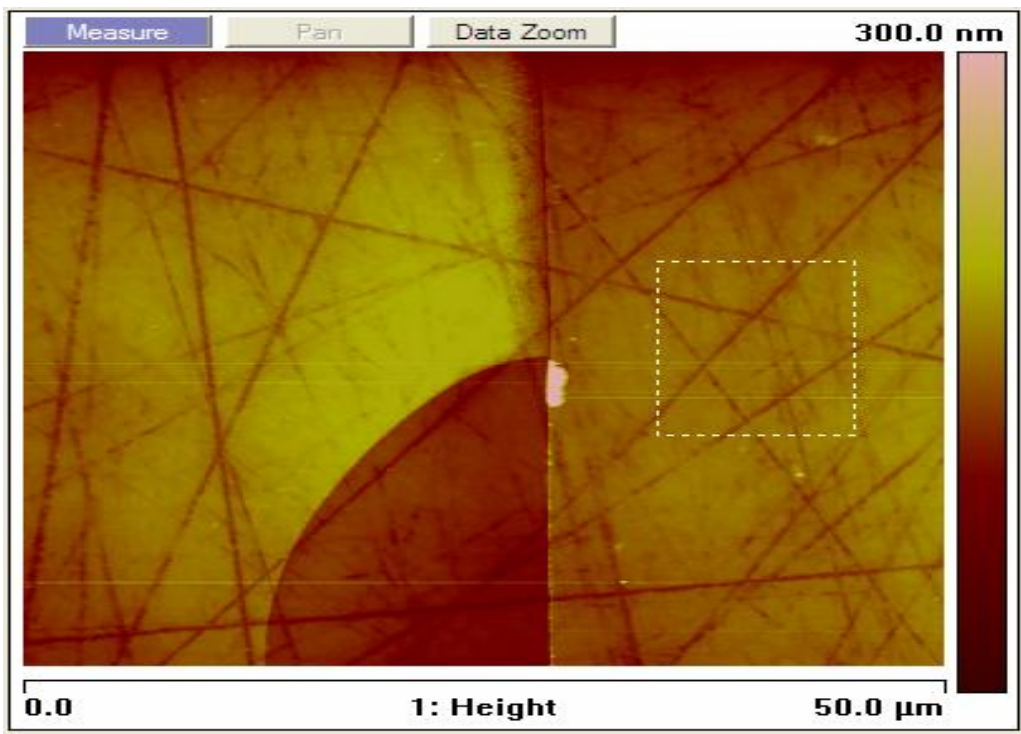
Figure 3-7 An AFM scan of the surface of one of our samples. For the region within the dotted rectangle, the average roughness is 6 nm. The maximum height of any feature in the dotted rectangle is 69 nm.
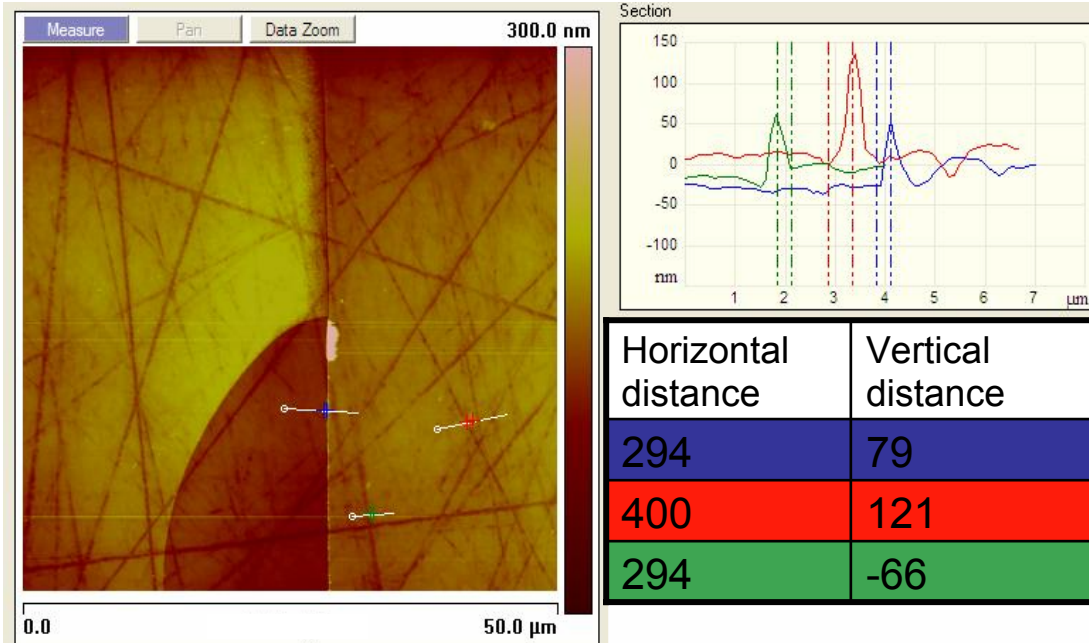
Figure 3-8 Line scans over three visible protrusions on the AFM image. For each scan I measure the height and base length of the protrusion using the upper right plot. The numbers for each scan appear in different color lines below the figures. Note $c/b<$ 1/3 for all 3.

3.6: Discussion

The analysis done for data in the regime where electrical breakdown is thought to be the result of field emission of electrodes assumes a field amplification factor on the surface of the electrodes. Any calculations made [eg. 43, 45] regarding the height or surface area of a surface feature responsible for such an amplification assumes that the current observed is due to emission from a single protrusion. This assumption

would seem valid if the emitted current depends strongly on the aspect ratio, so that for a variety of protrusions with a smooth distribution of aspect ratios, the single protrusion with the largest aspect ratio would dominate.

I have tested that assumption by calculating the amount of current as a function of applied voltage that would be produced by a variety of protrusions of different aspect ratios and shapes. The choice of shape does not appear to change our conclusions significantly. Here the shape of the features was chosen to be the one shown in the inset of Fig. 3-9. The results of our calculations are presented in fig. 3-9.

I have plotted $\ln(I/V^2)$ vs $1/V$, for consistency with the discussion of the previous sections. The current is the total current emitted by the protrusion due to the enhanced field at each point on the protrusion. The results represent currents induced from protrusions of aspect ratios 2, 4, 8, 10, and 20. It is evident from this figure that the differences in aspect ratios of an order of magnitude would produce currents that would differ by a factor of ~150 (a difference of less than 6 in the $\ln(I/V^2)$ vs. $1/V$ plot). That is, there is no reason to assume that a single protrusion dominates the current emission, especially when doing an analysis based on $\ln(I/V^2)$. In our opinion this means that a collection of non-interacting protrusions of different aspect ratios can produce a current that would appear to be caused by a single protrusion of larger aspect ratio.
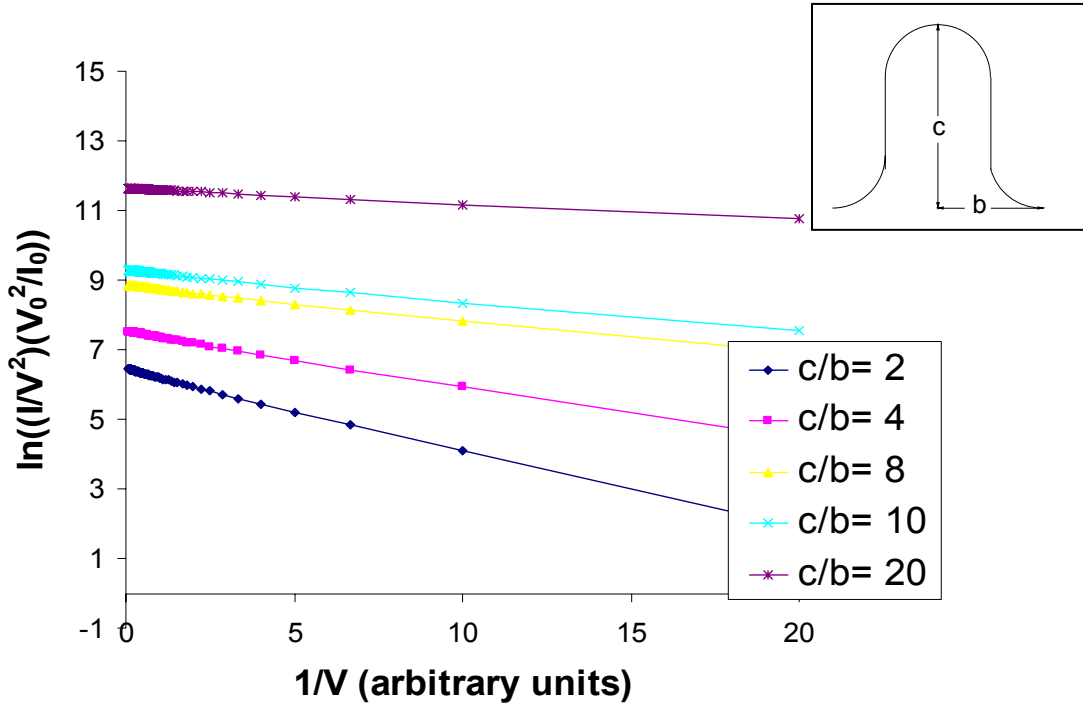
Figure 3-9 Simulations of $\ln(I/V^2(V_0^2/I_0))$ vs $1/V$ for protrusion of different aspect ratio.

The calculation of the emitting area A, then, would only be the sum of the areas of all the different protrusion involved in the measured current. In such a case, the calculations of the height for a single protrusion based on its base dimension, for values of calculated A as done in table 3-1, are not necessarily correct. For these cases the features responsible for the observed current may be a collection of smaller features, in height and base dimension, even of different aspect ratios between them. The standard theory is not helpful in predicting the characteristics of such features.

Although the above assumption of a large number of non-interacting protrusions provides a possible explanation as to why the standard theory breaks down in analyzing our data, it does not explain why in some cases the calculated emitting area

is much larger than the actual size of our electrodes. Also, having measured no visible

protrusion of aspect ratio more than 1 to our AFM precision, and knowing that

evaporated Au makes rather smooth films (typical size of features is 20-30 nm in

diameter, but only ~5 nm tall [46]), it seems rather unlikely that there would be

features of much smaller base dimensions and similar aspect ratios to those

calculated. The reasoning above leads us to the conclusion that even in the case of

$d=$ 0.8 μm it is unlikely that the data agree with the theory. In that case the theory

predicts values for the emitting area that are smaller than the precision of the AFM

measurement, but also predicts an aspect ratio of ~20 for the surface features. That

seems quite improbable given the typical surface characteristics of evaporated Au.

Finally, some of the reasons for enhanced local electric field on the surface of

electrodes, mentioned in studies such as ref. [34-40], do not seem to apply in our

case. For example, it is suggested that foreign element contamination of the

electrodes would locally enhance the electric field. The existence of foreign elements

refers to bulk metal electrodes and should not be possible in our thin film evaporated

electrodes.

3.7: Summary

I have presented data for breakdown of air for electrode separations between 400

nm and 45 μm. For the data below 10 μm, it appears that the mechanism responsible

for the breakdown is field emission of electrons, based on the good agreement

between the theory and our $\ln(I/V^2)$ vs. $1/V$ plots. This is the same mechanism that governs breakdown in vacuum. Using the standard Fowler-Nordheim equations for field emission we see that a large field magnification factor is needed to explain the data. It has been claimed previously that protrusions of a certain geometry on the surface of the conductors are responsible for such field amplification factors. I have used the Fowler-Nordheim theory to calculate the dimensions of such protrusions.

Using an AFM I have looked for such features on the surface of our electrodes. I have found 3 pieces of evidence that the theory does not explain our data. First, some of the calculated values of areas of surface features exceed the dimensions of our electrodes. Second, no protrusions with the correct height to base ratio exist on our electrodes that could explain our data (except, perhaps, for the data of 0.8 μm of separation). Third, the fact that I used evaporated Au seems to exclude the possibility of features of the correct aspect ratios that are smaller than our resolution. I have also shown that in some cases the assumption made by the theory that a single feature is responsible for the observed current is not valid.

I therefore must conclude that a different theory is needed for explaining the field amplification and field emission of electrons in our data. The fact that our data can be fitted with the field emission equations, like previous studies in the literature suggests that field emission is the reason for breakdown. It is the mechanism of field enhancement on the surface of the electrodes that requires further investigation.

In terms of trying to understand the origin of field enhancement in cases such as our samples, where the surface roughness is very small, it would be necessary to build a vacuum chamber in order to control the environment. Repeating the breakdown

measurements in a controlled environment would elucidate which environmental parameters affect the breakdown and why. For example, the effects of humidity could be eliminated by pumping such a vacuum chamber and backfilling with some inert gas. The effect of the gas on the value of the breakdown could then be examined by repeating the measurements in different gases and in vacuum. The difficulty of pursuing these types of measurement with our system is that the vacuum chamber has to be non-metallic in order to be able to perform a reliable capacitance measurement for our electrode separation.

If such measurements were to reveal that a more fundamental reason exists for local field amplification, the possible next steps would be harder to imagine. Perhaps a study of breakdown in a variety of different devices of different materials and geometries would help develop a practical guideline for estimating how much voltage can be applied between two electrodes of a certain separation.

In either case, a new theory should be developed that would explain the observed results. This theory should have definite predictions of experimental observables so that it can be checked against experimental results. It should also be applicable in a range of electrode separations that is relevant in most device geometries today, namely the submicron range. The final goal, in my opinion, should be to have a theory that would accurately predict the amount of potential that can be applied between two electrodes of a specific geometry, material and surface roughness as a function of their separation. Such a theory would be invaluable in designing, operating and understanding results of devices operated in voltage regimes close to the breakdown criteria.

Chapter 4: Introduction to Single-Electron Transistors

4.1: Introduction to Single-Electron Devices

In this chapter I will introduce the basic theory that governs electron transport through the single electron transistor (SET), a device whose behavior is dominated by the motion of single electrons. I will then describe the basic problems of SETs today and give a literature review of experimental implementations of the SET.

The SET is a device that consists of a conducting piece of material connected to macroscopic leads through tunnel junctions. I will call one of the macroscopic leads the source and the second one the drain. I will call the piece of material separated from the rest of the "world" by tunnel junctions the "island". In order to have current flowing from source to drain, electrons must go on and off of the island.

In addition, if the resistances of the tunnel junctions (R_T) connecting source and drain to the island are large compared to the resistance quantum $R_K = h/e^2 \approx 25.8$ kΩ, then the number of electrons on the island is an integer number [15]. The fact that the resistance is much larger than the resistance quantum guarantees that an electron that has tunneled onto the island is localized there. This, in turn, means that electrons can tunnel on and off the island only as units of one.

The conducting island has a total capacitance C_Σ, including the capacitances of the tunnel junctions, the self capacitance of the material itself and any capacitances between the island and nearby electrodes. We define the Coulomb charging energy

E_C as the energy needed to add or subtract an electron from the island; $E_C = e^2/2C_\Sigma$. If the temperature is such that the thermal energy (k_BT) is much smaller than the Coulomb charging energy, tunneling onto the island will be energetically controlled by the charging energy alone.

So, if we have a device that satisfies the conditions

$$R_T \gg R_K$$

and

$$E_C \gg k_BT,$$

transport through it will be governed by the Coulomb blockade due to the addition of an electron. The devices that satisfy these conditions I will refer to as single electron devices.

4.2: Coulomb blockade and the Single Electron Transistor

The single electron device of most interest to us is the SET. In the following, I roughly follow the description of an SET found in references [15, 47]. A circuit representation of an SET can be seen in figure 4-1. It consists of an island separated by the source and drain electrode through tunnel junctions of resistances and capacitances R_S, R_D, C_S and C_D respectively. The island is also capacitively coupled to an electrode called the gate. The drain electrode and the gate electrode are connected to voltage sources V_{SD} and V_G, while the source electrode is grounded. The voltage drop developed across C_D is V_1 while across C_S it is V_2. So, we have that

$V_1+V_2= V_{SD}$. I note that this situation is referred to as the asymmetrically biased

device.
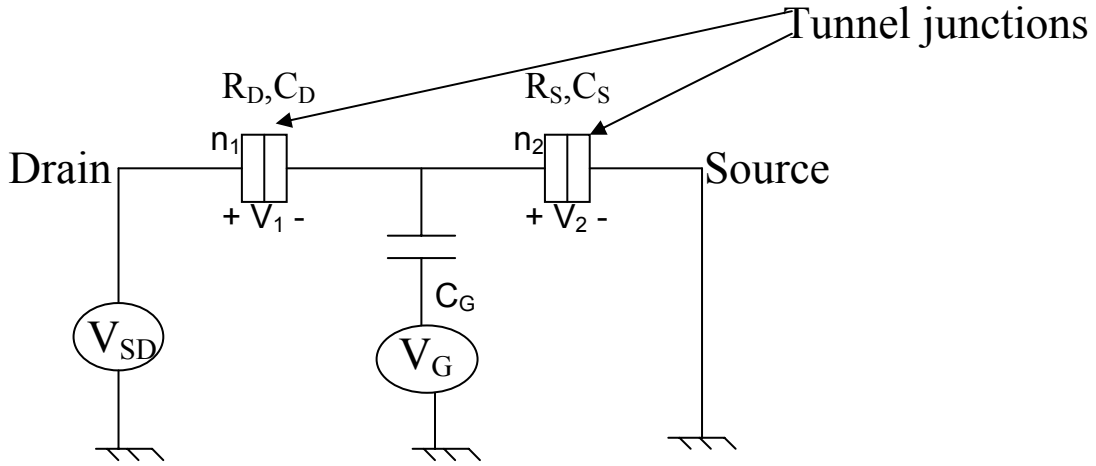
Figure 4-1 Circuit representation of an SET

Suppose that the island has n extra electrons on it. By extra electrons I mean

electrons that have tunneled on or off the island (I do not mean the electrons that are

intrinsic to the material and make it electrically neutral, when both V_{SD} and V_G are

zero). If n_1 is the number of electrons that tunneled onto the island through the drain

and n_2 is the number of electrons that tunneled out of the island to the source, then it

will be $n= n_1- n_2$. Also, suppose that the charges that develop across the capacitances

C_S, C_D and C_G are Q_S, Q_D and Q_G, respectively, while Q is the total charge of the

island. Then

$Q_D= C_DV_1$

$Q_S= C_SV_2$

$Q_G = C_G (V_G - V_2)$

and $Q = Q_S - Q_D - Q_G = -ne$ $\qquad\qquad$ (4.1)

In terms of the applied bias, we can rewrite the potentials across the junctions as

$$V_1 = \frac{(C_S + C_G)V_{SD} - C_G V_G + ne}{C_\Sigma}$$

$$V_2 = \frac{C_D V_{SD} + C_G V_G - ne}{C_\Sigma} \qquad\qquad (4.2)$$

where $C_\Sigma = C_D + C_S + C_G$. The electrostatic energy stored in the system is then

$$E = \frac{C_G C_D (V_{SD} - V_G)^2 + C_D C_S V_{SD}^2 + C_G C_S V_G^2 + Q^2}{2C_\Sigma} \qquad\qquad (4.3)$$

In order to calculate the total energy of the system we have to take into consideration

the work done by the voltage sources in delivering charge to the system. This work

will be:

$W = V_{SD}\Delta Q_{SD} + V_G \Delta Q_G,$

where ΔQ_{SD} and ΔQ_G are the total charges transferred from the voltage sources.

These charges include the continuous polarization charges induced across the

capacitors as the potential of the island changes, as well as the integer number of

electrons that tunnel on and off of the island. The total free energy is then

$E_e = E - W.$

With that in mind, we can calculate the change in total energy corresponding to an

electron tunneling across the two tunnel junctions:

$$\Delta E_{e1}^\pm = E(n_1 \pm 1, n_2) - E(n_1, n_2) = \frac{e}{C_\Sigma}(\frac{e}{2} \pm [(C_S + C_G)V_{SD} - C_G V_G + ne]) \qquad (4.4)$$

$$\Delta E_{e2}^\pm = E(n_1, n_2 \pm 1) - E(n_1, n_2) = \frac{e}{C_\Sigma}(\frac{e}{2} \pm [C_D V_{SD} + C_G V_G - ne]) \qquad (4.5)$$

The only events with high likelihood are those that lead to negative ΔE (at zero temperature).

For simplicity, let us assume that $C_G\, V_G \ll e$ and that $C_D = C_S = C$. If we start from a condition where $n = 0$, equations (4.4) and (4.5) tell us that for the total energy to be negative in each direction of tunneling, there is a minimum value of V_{SD} required. It is clear that for $-e/C_\Sigma < V_{SD} < e/C_\Sigma$, tunneling cannot occur. This phenomenon is referred to as "Coulomb blockade". It leads to a current vs. applied bias characteristic for the SET that looks like figure 4-2.
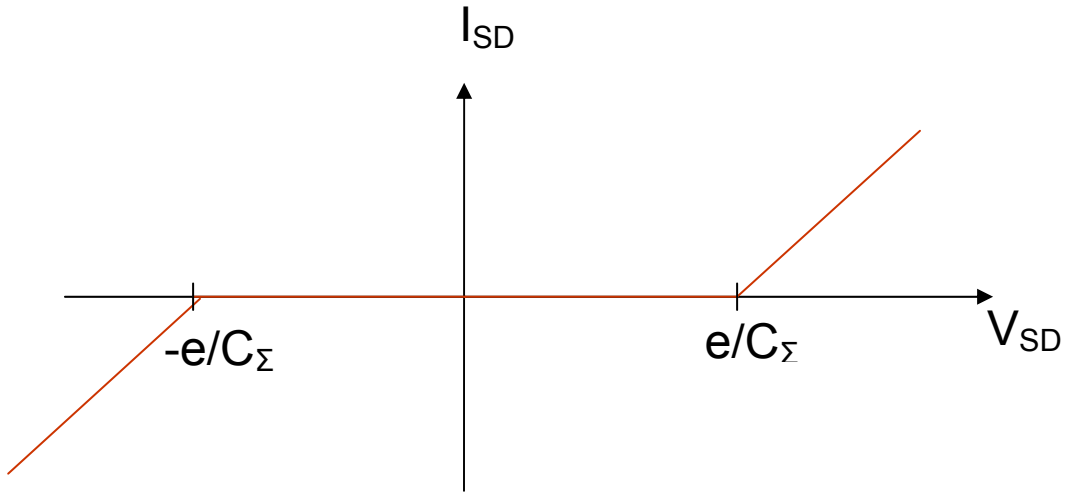
Figure 4-2 Current vs. applied bias characteristic of an SET.

4.3: Coulomb oscillations and the diamond diagram

In order to understand the dependence of the source-drain current on the gate voltage we have to consider the tunneling rates for each of the two junctions. These are given by [15]:

$$\Gamma_{1,2} = \frac{1}{e^2 R_{1,2}} \left[\frac{\Delta E_{1,2}}{e^{\frac{\Delta E_{1,2}}{k_B T}} - 1} \right] \tag{4.6}$$

where $\Delta E_{1,2}$ are given by (4.4) and (4.5). The current is then simply $I = e\Gamma_{1,2}$. It can be seen from (4.4) and (4.5) that there are combinations of values of V_{SD} and V_G for which the energy differences become negative. In such cases the Coulomb blockade is "lifted" and current can flow through the device. In the combinations where the energy differences are positive very little current will flow through the device. The current through the device then oscillates between the high and low values as a function of V_G [15]. I will refer to this phenomenon as "Coulomb oscillations" (figure 4-3a).

A convenient way to represent this behavior is through a stability diagram. Plotting the values of $V_{SD} C_\Sigma/e$ and $C_G V_G/e$ for which the energy differences are constant we get figure 4-3b (I have assumed that $C_S = C_D \gg C_G$, so $C_S = C_D = C_\Sigma/2$). Constant energy differences correspond to constant current through the device. Since current is the experimental observable, this is a natural choice for the stability diagram. The diamond like patterns of the stability diagram are usually referred to as "Coulomb diamonds".

The diamond diagram is a plot that contains a lot of information. As can be seen from figure 4-3b, the height of the diamonds corresponds to a bias voltage of e/C_Σ. It can therefore be used to determine the Coulomb energy of the island, which is $E_C = e^2/2C_\Sigma$. Also it can be seen that the period of the diamonds, in terms of the gate voltage, which also corresponds to the period of the Coulomb oscillations, is e/C_G.

Lastly, the slopes of the diamonds can be used to calculate the values of C_S and C_D. Starting from equations (4.4) and (4.5) and requiring that the energy differences remain constant for changing V_{SD} and V_G, we get:

$$\text{Positive slope} = \frac{C_G}{C_S + C_G} \tag{4.7}$$

$$\text{Negative slope} = -\frac{C_G}{C_D} \tag{4.8}$$

As mentioned before, constant energy differences for different tunneling events correspond to constant currents. Plotting constant current curves on a stability diagram is the experimentally convenient way of looking at the stability diagram.
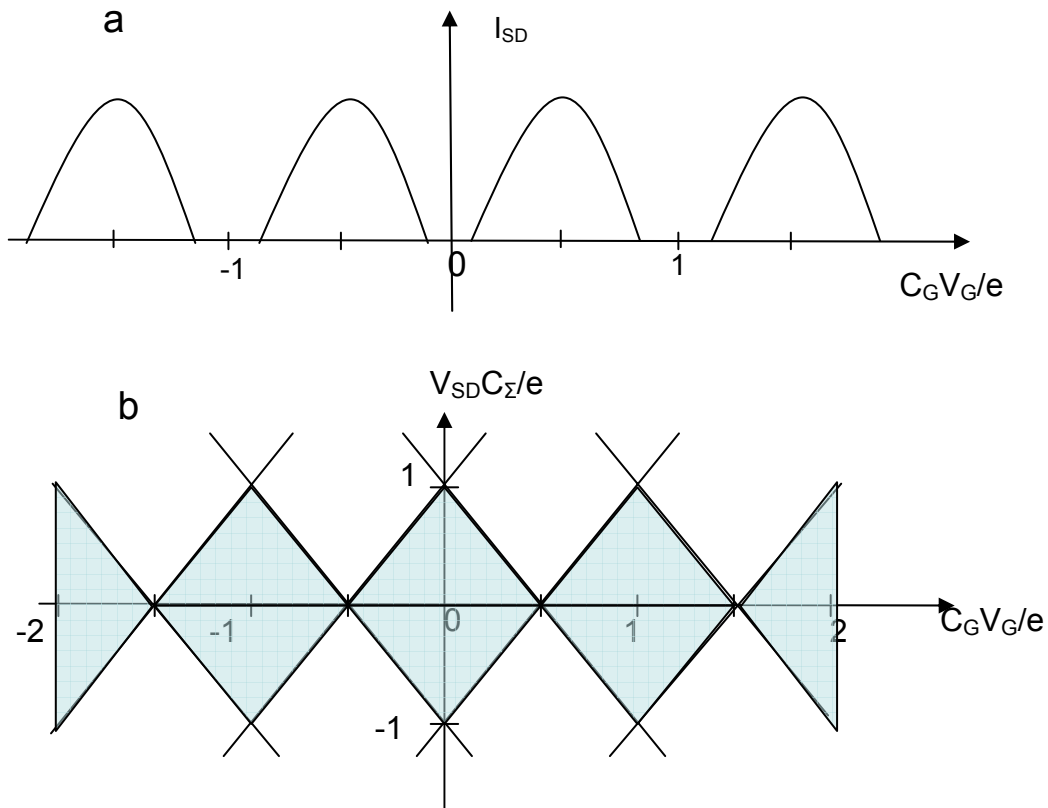
Figure 4-3 a) "Coulomb oscillations" of the source-drain current as a function of gate voltage. b) Stability diagram of an SET for $C_S = C_D = C_\Sigma/2 \gg C_G$. The shaded regions correspond to the existence of Coulomb blockade.

4.4: Temperature dependence of the source-drain current

The current flowing from source to drain (I_{SD}) in an SET undergoes oscillations as a function of gate voltage from a minimum value (I_{SDmin}) to a maximum one (I_{SDmax}), as was explained earlier. In order to understand the dependence of the ratio on the temperature (T) it is necessary to return to the tunneling rates of each individual tunnel junction in the presence of Coulomb blockade (equation 4.6). We can use this equation, along with equations (4.4) and (4.5), to calculate the tunneling rate of the two junctions for different values of the gate voltage V_G. For negative values of ΔE_e (which correspond to current flowing through the device) the smallest tunneling rate will be the one that limits I_{SD}. The smallest (in absolute value) negative ΔE_e will produce the smallest Γ. Also, from fig. 4-3a (assuming $V_{SD} \ll e/C_\Sigma$) we can see that we should expect the maximum current (I_{SDmax}) for $V_G = e/2$ where the Coulomb blockade is lifted, while for the minimum (I_{SDmin}) I will use $V_G = 0$.

If we want to consider the limiting rates for electrons tunneling from source to island to drain, for example, we can calculate $\Delta E_{e2}(n_1, n_2-1)$ for $V_G = e/2$ and $V_G = 0$. We can then repeat the process for $\Delta E_{e1}(n_1-1, n_2)$ and calculate which process is the limiting factor in each case. In our case, tunneling through to the source turns out to be the smallest negative value. We can then calculate the ratio:

$$\frac{I_{SD\,max}}{I_{SD\,min}} = \frac{\Gamma_2(V_G = {e}/{2})}{\Gamma_2(V_G = 0)} \quad .$$

We make some simplifying assumptions: $C_S = C_D = C$ and $C \gg C_G$ so $2C \approx C_\Sigma$, thus

$$\frac{I_{SD\,max}}{I_{SD\,min}} \propto e^{\frac{E_C}{k_B T}}$$ (4.9)

The ratio of the minimum and maximum current through the device as a function of temperature can be used to provide an independent estimate of the charging energy E_C.

4.5: Charge sensitivity

From figure 4-3a, it is clear that even for a change in gate voltage (δV_G) that would correspond to a sub-single-electron change $\delta Q_e = C_G \delta V_G$ the variations in current can be measurable. This is the basis of using the SET as an electrometer. The only thing limiting the charge sensitivity of a device is the noise. It has been shown [48, 49] that the absolute limit posed is that of the white noise of the SET, which is shot noise. For such a case, charge noise ($S_q^{0.5}$) levels of $< 10^{-5}\ e/\sqrt{Hz}$ are possible. In experimental implementations of SETs (eg. in metal devices) it has been shown that the noise follows a 1/f behavior [50]. This noise exceeds the fundamental limit of the white noise, for a wide range of frequencies. Even for such a case, though, charge noise levels on the order of $10^{-4}\ e/\sqrt{Hz}$ have been demonstrated for low frequencies of operation (~10 Hz) [51]. From the noise level of the device it is possible to calculate the charge sensitivity of the SET (ΔQ), given a specific bandwidth of operation. For example, a typical operation bandwidth of metal SETs in our lab would be between 0.1 Hz and 10 kHz. In such a case, we have

$$\Delta Q = \left(\int\limits_{0.1}^{10000} S_q(f)df \right)^{\frac{1}{2}}$$

Considering the 1/f behavior of the noise, we can see that it is possible to achieve

charge sensitivities of $\Delta Q = 10^{-3}$ e.

These values of charge sensitivity make the SET the world's most sensitive

electrometer. They are orders of magnitude better than commercially available

electrometers and are even better than specially designed low temperature

semiconductor devices [for example 52].

4.6: The problems of SETs

SETs as charge detectors suffer from two major problems [16]. These two

problems are the temperature of operation and the charge offset drift. The problem

with the temperature of operation can be understood starting from the discussion in

section 4.1. There, it was explained that in order for single electron effects to be

noticeable we must have $E_C \gg k_B T$. The charging energy E_C depends on the total

capacitance of the island (C_Σ), since $E_C = e^2/2C_\Sigma$. This total capacitance includes the

contributions from the capacitances of the tunnel junctions and the capacitances of the

gate, but also the value of the self capacitance of the island. Clearly, smaller

capacitance means greater charging energy, which, in turn, means larger temperature

of operation. But the capacitance of the island is limited by the self capacitance,

which for a case of a sphere of conducting material of radius R, in vacuum, would be

just $4\pi\varepsilon_0 R$, where ε_0, is the permittivity of free space. This would be the lowest

possible value of capacitance for an island of radius R. Even if we were to relax the requirement set earlier to $E_C \approx k_B T$, that would mean that in order to get $k_B T = 25$ meV, or room temperature, we would have to have a total capacitance of ~3 aF, or an island of radius $R \approx 25$ nm, which is hard to achieve lithographically. In reality the capacitances of devices are orders of magnitude larger than this limit due to the capacitances of the junctions and gate and so in order to satisfy the requirement, the temperature of operation must be low. In the case of metal devices it is usually below 1 K. The fact that these devices have to be operated at such low temperatures makes them impractical to use. They require special cooling equipment that is both expensive and hard to operate.

The second major problem of SETs is the charge offset Q_0 [16]. This problem is the result of the experimental implementation of SETs. The devices are fabricated using conducting materials as well as insulators. These insulators contain in them defects and impurities. Moreover, defects exist in the interfaces between different materials. These defects can carry charge and are randomly distributed. The existence of a charge impurity close to the SET will change the charge configuration of the island, in the same way as the gate does. This will cause a shift in the characteristic curve of the SET (for example fig. 4-4). This shift, or the charge offset (Q_0), as it is called, varies randomly from device to device. So, a collection of nominally identical devices (devices with the same design, even on the same substrate on the same fabrication run) will have a different value of current for the same value of gate voltage.

In fig. 4-4 I plot the current through the SET (I_{SD}) as a function of gate voltage (V_G) (Coulomb oscillations) for three nominally identical devices. The voltage offsets (x_1 and x_2) between the characteristic curves are the consequence of the charge offset Q_0. In such a case it will be

$Q_{01} = ex_1/\Delta V_G$ and $Q_{02} = ex_2/\Delta V_G$, where $Q_{01,2}$ are the charge offsets corresponding to x_1 and x_2, respectively, while ΔV_G is the period of the I_{SD} oscillations.
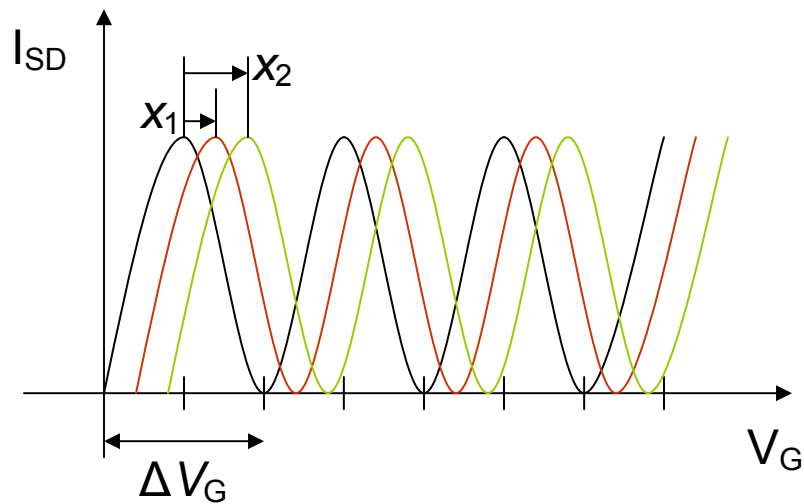
Figure 4-4 Characteristic curves (I_{SD} vs. V_G) for three nominally identical devices. ΔV_G is the period of the I_{SD} oscillations, while x_1 and x_2 are the values of voltage offset of the red and green curves from the blue one.

Moreover, this charge offset Q_0, caused by charged impurities around the device, drifts in time. I will refer to this as charge offset drift ($Q_0(t)$) [17,18]. This drift is random and happens over the timeframe of hours and days. It is therefore very low frequency. A typical value for this drift over the period of a few days can be as large as 1 e for metal devices [17]. It cannot be explained by the low frequency

extrapolation of the 1/f noise of the device, since typical amplitudes of this type of noise would integrate to 1 e only after many years [18]. Even if it were possible to somehow compensate for the charge offset Q_0, the fact that it drifts makes using SETs in parallel an extremely difficult task because of the random nature of the drift. We can imagine that we could start an experiment where we have compensated for the Q_0 of several devices running in parallel but returning to the uncompensated situation after Q_0 of one of the devices drifts.

4.7: Overview of SET implementations

Historically, the first experimental demonstration of an SET was in devices that used aluminum as the island and aluminum oxide for the tunnel junctions [53]. They were fabricated using a self aligned technique. Aluminum is deposited at an angle through a resist stencil, as a first step. Then, the aluminum is oxidized, by introducing a controlled oxygen pressure without breaking the vacuum. As the final step, a second layer of metal is deposited from a different angle through the same stencil, so that the relative angle of deposition determines the area of overlap between the two depositions. That way, tunnel junctions of controllable area can be easily created. This method has been widely used in fabricating metal devices.

Metal devices attracted a lot of attention in the early years of the SET research [15]. The ability to fabricate them "easily" (meaning few fabrication steps) has led to their use in a variety of applications like metrology [54] and scanning electric field

microscopy [55]. Nevertheless, they suffer from the two major problems that inhibit their use in widespread practical applications, as explained in the previous section.

There has been research in fabricating SETs with a variety of different materials. This effort has been an attempt to create "better" SETs that would not be limited by the issues common in metal devices. Examples include SETs fabricated using the two dimensional electron gas (2 DEG) at the interface of materials like GaAs/AlGaAs [56]. In such a case, metallic gates are used to deplete certain regions of the 2 DEG of electrons and so define the island. The tunnel junctions are just regions of space with a smaller electron concentration. Devices of this kind with electrostatically defined tunnel junctions offer the advantage of tunability of the resistance and capacitance of the junctions. Other examples include devices demonstrated in materials such as carbon nanotubes [57] and molecular systems [58].

In terms of creating an SET that would be best for a wide variety of practical applications, the natural choice of material is Si. Si-based SETs have the advantage of being compatible with the current complimentary metal oxide semiconductor (CMOS) technology. This means that Si SETs offer the possibility of integration with FET circuits [59]. Also, the Si process technology is more mature and the oxide used has a better quality than what is possible with other material fabrication processes. That is because Si processes have been widespread and commonly used in industry for decades. Finally with the use of silicon on insulator (SOI) technology there is a large flexibility in the possible designs of new devices [60]. This makes Si devices a much more attractive candidate than devices based on other materials.

The effort to built Si based SETs can be divided into two categories [59]. The first category uses chemical methods to produce an island. That island is then contacted by lithographically defined leads. These methods produce nanocrystals of semiconducting material that have sizes smaller than can be achieved with lithographic techniques. As an example of such a technique, in reference [61], Si nanocrystals are embedded in between the source and drain of a FET structure. The advantage of such methods is that because of the small size of the island its total capacitance is very small. As explained in a previous section, smaller total capacitance means that the device can operate at larger temperatures. The disadvantage is that the fabrication is not very well controlled, which creates reproducibility issues in these types of devices [59].

A different approach to making Si based SETs is to create a lithographically defined island. This technique allows for a better control over the island size and capacitance. It is considerably more difficult, though, to fabricate islands of the size possible with the nanocrystal method. Historically, the first lithographically defined Si based SET was made on a bulk Si substrate [62]. In more recent attempts, devices have been fabricated on SOI substrates. This allows for much smaller islands, since the oxide underneath the active Si layer limits the size of the island in one dimension. For further decreasing the size of the island it is possible to selectively remove the Si, using lithography and etching and so create a narrow channel in a FET configuration. Then by narrowing parts of that channel with the same techniques, tunnel barriers can be created [63]. The size of the island, then, is the size of the Si left in between those tunnel junctions. Another way to create the tunnel barriers is to include

lithographically defined regions of high stress that will produce barriers for conduction [64].

Recently, a new type of Si device on a SOI substrate has been demonstrated [65]. This type of device uses a standard FET configuration. Lithographically defined gates are used to deplete the FET channel of electrons and thus create tunnel barriers. This type of device combines all of the advantages of Si devices with the tunability of the parameters of the tunnel junctions usually found in the 2 DEG devices. I will call this type of device "tunable-barrier Si SET". It was shown in [65] that devices fabricated in this configuration showed excellent reproducibility of device parameters. The ability to independently control the junction parameters with electrostatic gates offers the possibility a large amount of flexibility in the device operation. It was shown, for example, that it is possible to have several gates on top of a channel and to use them to change the configuration of the device, going from a single island to a double island device. Finally, it was demonstrated that in these devices the charge offset drift (Q_0(t)) was very small (a factor of 100 better than in metal devices) [66]. They are thus almost free of one of the two major problems of SETs.

For the reasons described above, I feel that the tunable barrier Si devices are very interesting. They are interesting from a technology standpoint, since their reproducibility in parameters and lack of charge offset drift makes them excellent candidates for integration. They are also interesting from a science standpoint, since the flexibility of their operation allows for a possibility to investigate a device parameter space not previously possible. We have decided to fabricate such devices in our group and thoroughly investigate their properties.

Chapter 5: Measurements of tunable barrier Si single-electron transistor

5.1: Introduction

In this chapter I will describe the measurements of tunable barrier Si based SETs fabricated by our group. As mentioned in the previous chapter, I believe that this type of device is the most promising for both technological and scientific applications. Moreover, devices of similar architecture have been shown to be almost free of the charge offset drift (Q_0(t)) problem. All of the previous devices were fabricated in a single foundry, NTT in Japan.

We have fabricated tunable barrier Si SETs in a different foundry, the Cornell nanofabrication facility in USA. In what follows I demonstrate the operation of these devices as SETs and confirm the fact that they exhibit very small Q_0(t). From this I can conclude that this is a robust property of Si devices and can be reproduced under different fabrication conditions. I thus provide an additional argument in favor of the Si devices being the most promising for practical applications.

The devices were fabricated using conventional MOSFET processes. A schematic representation of the device appears in Figs. 5-1a (lateral) and 5-1b (vertical). A micrograph of a device, similar to the one used but without the upper gate, appears in Fig. 5-1c. We start with a silicon on insulator (SOI) substrate and etch a narrow channel, lightly p-doped, between heavily n-doped source and drain regions. Then a

layer of oxide is grown on top and a layer of localized in situ-doped polysilicon is deposited. Localized gates, the "lower" gates, are defined through electron beam lithography and etching of the polysilicon, followed by another layer of oxide. Finally, an upper polysilicon gate is deposited and is defined to cover the entire region between source and drain.
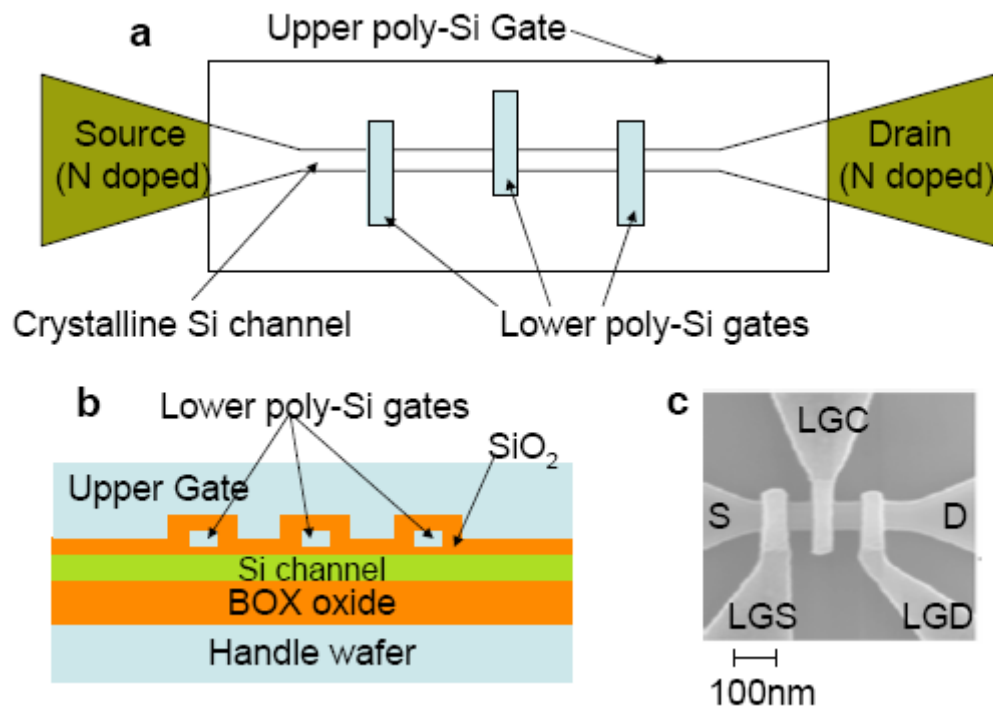
Figure 5-1 a) Lateral and b) vertical schematics of our device. c) A micrograph of a device with no upper gate.

The entire fabrication process followed for these devices is as follows:

Pattern alignment marks (process for creating the alignment marks)

E-beam lithography requires edges, rather than material contrast, for alignment. Generally, the alignment marks are etched as deeply as possible.

• Start with 6" SOI wafers: lightly p-doped, BOX=200 nm, device Si=100 nm

• Expose and develop thick photoresist with all alignment marks using a stepper

• Descum photoresist with 30 s oxygen plasma

• Etch into wafer using CF_4 plasma for the device Si, CHF_3/O_2 for the oxide and SF_6/O_2 for the substrate

• Remove photoresist using 2 min oxygen plasma for the skin of the resist and 1165 for the bulk

Pattern Si nano-wire (process for defining the channel)

The width of the nano-wires is adjusted in the CAD to account for the three oxidations and proximity effects.

• Expose and develop ~130 nm of XR-1541 using e-beam lithography

(4 min. 170 C pre-bake, 4 min. 170 C post-exposure bake and 4 min. dev. in 300 MIF)

• Etch Si using Cl_2, stopping on buried oxide

• Remove XR with a 100:1 DHF dip for 60 s

Si nano-wire etch cleanup (process for cleaning the etch damage from the channel)

Etch damage is removed by growing a thin oxide and then stripping it.

• Grow 4 nm of oxide at 800 C (10 min.)

• Strip oxide with a 2 min. 100:1 DHF dip

Source/Drain implant (process for doping the source and drain regions)

The source/drain implants need to be done before either gate formation. Use thick photoresist as the implant mask.

• Expose and develop thick photoresist with implant mask to open holes over S/D plus extensions, tips using a stepper

• Descum resist with 30 s oxygen plasma

• Implant phosphorus for n-type: 30 keV, 7 deg., 1×10^{15} cm-2 dose, 50 μA beam current, water cooling

• Remove photoresist using an oxygen plasma (5 min) for the skin followed by 1165

Lower gate stack formation (process for creating the lower gates)

• Grow oxide on Si nano-wire: 950 C, 82 min, ~ 40 nm

• Immediately deposit ~ 125 nm in situ phosphorus-doped polysilicon (620 C)

• Expose and develop > 250 nm XR with the "sleeved" lower gate pattern using e-beam lithography (4 min. 170 C pre-bake, 4 min. 170 C postexposure bake and 4 min. dev. in 300 MIF)

• Etch lower gate using Cl_2, stopping on buried oxide/gate oxide

• Remove XR with a 100:1 DHF dip for 2 min

Upper gate stack formation (process for creating the upper gate)

The UG will be exposed via photolithography in order to ensure coverage over the topography.

• Grow oxide on LG: thickness varied from device to device

• Immediately deposit ~ 125 nm in situ phosphorus-doped polysilicon (620 C)

• Deposit ~ 100 nm of PECVD oxide (400 C)

• Expose and develop thick photoresist with the upper gate pattern using image reversal

• Descum photoresist using 30 s oxygen plasma

• Etch PECVD oxide using 90 s 6:1 BOE dip

• Remove photoresist using 1165

• Etch upper gate using Cl_2, stopping on buried oxide/gate oxide

Form contact holes and metallize (process for contacting device through metal contact pads)

• Expose and develop photoresist with contact holes using photolithography

• Descum photoresist using 30 s oxygen plasma

• Etch oxide from above contacts using 90 s 6:1 BOE dip

• Remove photoresist using 1165

• Expose and develop photoresist with metal pads using photolithography

• Expose and develop photoresist with die numbers/scribe marks using contact lithography

• Descum photoresist using 30 s oxygen plasma

• Remove native oxide from above contacts using 2 min. 100:1 DHF dip

• Thermally evaporate ~ 800 nm of Al on front (one full slug)

• Lift-off photoresist using 1165

• Spin photoresist on front for protection

• Remove poly and oxide from back using CF_4

• Thermally evaporate ~ 800 nm of Al on back (one full slug)

• Remove photoresist using oxygen plasma and 1165

5.2: Room temperature results

5.2.1: Motivation and introduction

Before I attempt to measure these devices at low temperatures as SETs, I can make several room temperature measurements that will reveal whether the devices exhibit the expected characteristics. Measurements at room temperature provide a fast and convenient way of measuring the characteristics of the fabricated devices as a means of selecting which ones I will then cool to low enough temperatures to measure single electron effects.

Each gate of the devices presented in fig. 5-1 along with the section of Si channel directly underneath it acts as a FET at room temperature. An overview of FETs can be found in reference [67]. For our purposes I look at a certain set of characteristics that our devices need to exhibit in order for them to be considered candidates for further study at low temperatures.

The FETs are enhancement mode n-type transistor; the channel connecting source and drain in our devices is normally off. This means that for zero gate voltages the channel is non-conducting (there are few electrons in the conduction band). The upper gate can be used to electrostatically invert the channel (excite electrons to the conduction band) and thus make the channel conducting, or on. The lower gates can be used to locally repel these electrons and thus turn the regions underneath them to

non-conducting, or off. These non-conducting regions will act as the tunnel barriers in the SET operation.

I can test the operations described in the previous paragraph at room temperature. I can also check for leakage problems between the gates and the channel and between the gates themselves. When I find a device that exhibits the above characteristics and has no leakage problems I can hope that it will operate as a SET at low temperatures.

5.2.2: Results

The devices as fabricated come in an entire wafer. Each wafer includes 30 dies, each of which includes several devices. Each die is approximately 8 mm by 8 mm. Each device is connected to macroscopic leads that lead to contact pads. There are 24 pads per die. I cleave the wafer in order to get the individual dice. I then mount them to chip headers that allow us to connect to the measurement apparatus. I use wirebonds to connect from the contact pads to the chip header.

For the room temperature measurements I use a parameter analyzer (Agilent 4156C). The parameter analyzer allows us to apply voltages and monitor the current in four different leads simultaneously. The device is connected through a measurement box that has been specially designed to have a low level of leakage and noise between different leads ($\sim 10^{-14}$ A) for sensitive current measurements.

Using this method I can apply a voltage to the source, the drain, and one of the gates while ramping the voltage of a second gate and measuring the current through all four leads. During this measurement the rest of the gates are all grounded. An

example of this appears in fig. 5-2. In this case the drain voltage is 10 mV, the source is at 0 V the lower gate (LGS) is at 0 V, and I ramp the upper gate (UG). We can see that the UG is increasing the conduction of the channel between source and drain by almost five orders of magnitude. We can also see that I_{UG} and I_{LGS} are very small and that $I_D = - I_S$ (I have made all quantities positive in this graph in order to plot a logarithmic scale), which means that everything is as expected.
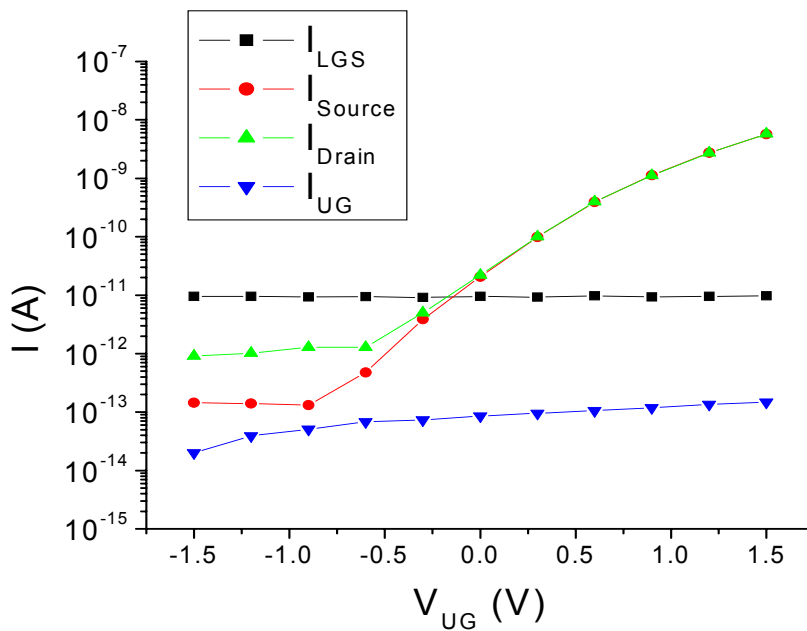
Figure 5-2 Current (*I*) through the source, drain, LGS and UG as a function of the UG voltage (V_{UG}).

Having tested the function of the UG I can set it to a value for which the conduction of the channel is most sensitive to changes in gate voltage (eg. 0.5 V, from fig. 5-3) and ramp LGS. The results appear in fig. 5-4. It is clear that in this case LGS is reducing the conductance of the channel by two orders of magnitude, as I apply a

more negative V_{LGS}. This is also consistent with the fact that I expect the lower gates to create local barriers of conduction. I also investigate the effects of LGD on the conduction of the channel. The results are similar.
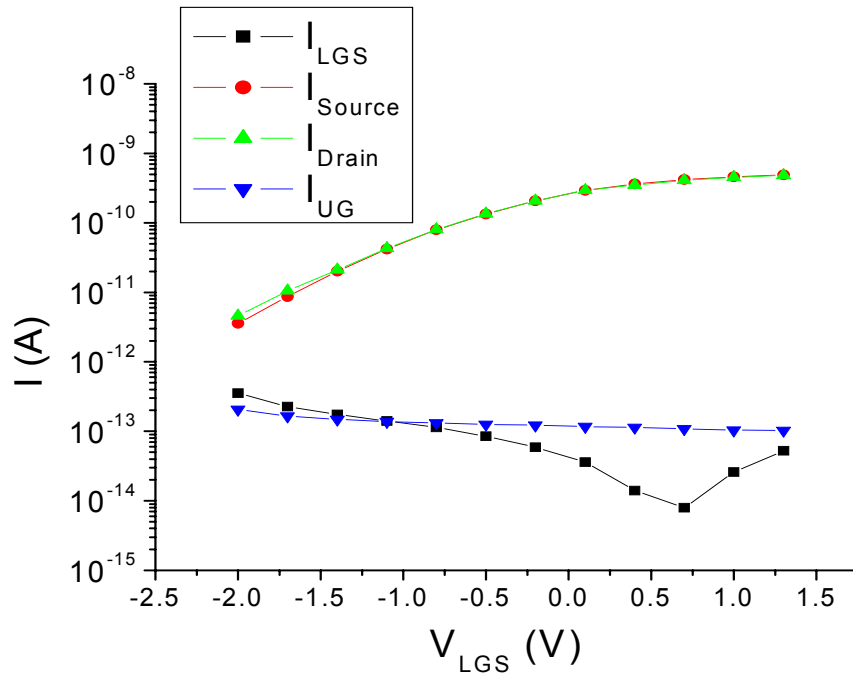
Figure 5-3 Current (*I*) through the source, drain, LGS and UG as a function of the LGS voltage (V_{LGS}).

Unfortunately some of the devices exhibited leakage problems as determined from measurements identical to the ones presented above. For example, I present in fig. 5-4 the results from a measurement identical to the one described in figure 5-3 for a different device. From the data in fig. 5-4 we can see that the gate LGS is leaking to another gate and possibly the drain. We can see that because LGS is nominally an open circuit and yet there is current flowing through it. Also, it is obvious that there is

more current flowing through the drain than the source for $V_{LGS} < -1$, which implies that at least part of that leakage is to the drain. The rest of the leaking current is going to one of the unused grounded gates. In order to understand between which leads the leakage exists, I continue making measurements as described above but changing one of the four leads each time. After I have measured all leads, I can find where the problem is.
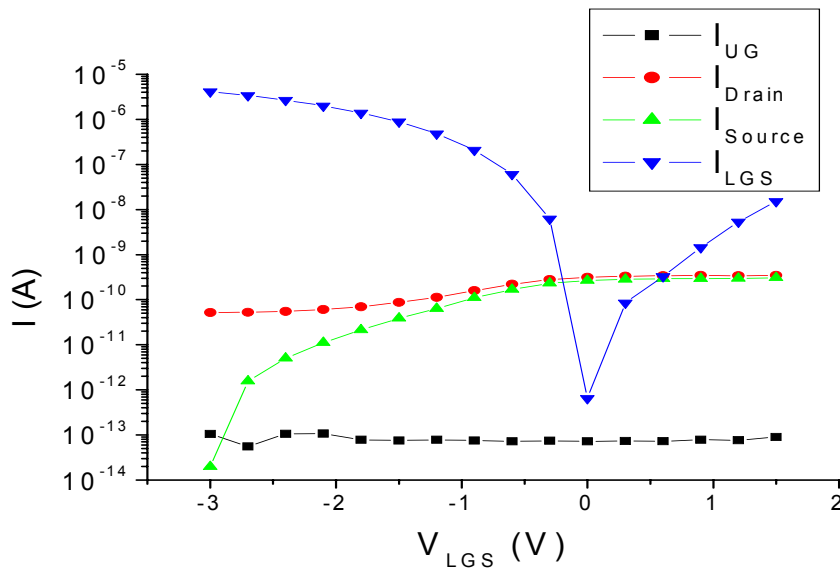
Figure 5-4 Current (*I*) through the source, drain, LGS and UG as a function of the LGS voltage (V_{LGS}) for a device with leakage.

Most of the leakage problems are a consequence of the BOE dip in the last section of the fabrication process (form contact holes and metallize). This step was too aggressive and ended up etching all the way through the BOX allowing the deposited metal to contact the handle wafer. Eliminating this problem should fix most of the leakage problems observed.

5.2.3: Conclusions

Using the measurements described above I can make useful observations about the operation of our devices (I measured a total of 24 devices):

1) In most devices the upper gate can turn the channel on and the lower gates can create a barrier for conduction (17 out of 24 devices).

2) In most cases there are serious leakage problems between different gates and the channel or between the gates themselves (22 out of 24 devices). This means that in the next fabrication runs, these problems must be addressed.

3) Because of the leakage problems, only a portion (2 out of 24) of the devices fabricated look promising enough to work as SETs at low temperatures. Future fabrication runs that have addressed the leakage issues will hopefully produce results of higher yield.

4) Some of the devices (2 out of 24) measured at room temperature exhibit the expected electrical characteristics and have very little leakage. So, despite the fabrication issues there are devices that can be used as SETs at low temperatures.

5.3: Low temperature results

5.3.1: Motivation

Having tested the devices at room temperature, I have identified the appropriate ones to cool to lower temperatures. Electrical measurements at low temperatures will

allow us to satisfy the criterion $E_C << k_B T$ set in chapter 4 as necessary to observe

single electron phenomena. I want to test the behavior of our devices as SETs. This is

the main motivation of the work described in this chapter as it was defined in chapter

1, namely to fabricate and demonstrate the operation of an SET of improved

characteristics. In this respect, I will demonstrate the basic SET characteristics of our

devices and measure the charge offset drift $Q_0(t)$ and compare it to previous results in

the literature.

5.3.2: Measurement set up

The measurements at low temperatures were taken in an Oxford dilution

refrigerator. The use of a dilution fridge allows us to cool the sample to temperatures

as low as 30 mK. It turned out that this was not necessary as these devices exhibited

SET behavior up to 40 K as will be shown later. Most of the measurements were

taken at temperatures ranging from 1 to 5 K, as these were low enough to observe

single electron phenomena clearly. This is an advantage of the Si devices as opposed

to metal ones, which I have to measure close to the base temperature of the dilution

fridge.

A schematic of the measurement circuit is shown in figure 5-5 (only the wiring of

the device is considered here. For more details on the cryostat wiring see appendix

B). Each of the lower gates is represented as a FET. The upper gate is also shown as a

FET that covers the entire region between source and drain. The SET island is

defined by the region between the FETs defined by the lower gates. So, the device

consists of the two FETs, the island and the UG capacitor, indicated in figure 5-5 by a dashed box. The gates are connected to voltage sources. The drain is connected to a voltage source through a resistive voltage divider (reduces the voltage applied to the device) and a resistor (limits the current noise injected in the device) and voltage and current amplifiers are used for the measurements of source to drain voltage and current, respectively. In figure 5-5 I have not included any of the capacitances of the leads to ground since they are not important in the considerations of the SET operation. The capacitance of the island to ground is also neglected since the total capacitance of the island is dominated by the capacitances of the two FETs and that of the upper gate. In the measurements described in this chapter I have left the third lower gate (named LGC in fig. 5-1) floating.
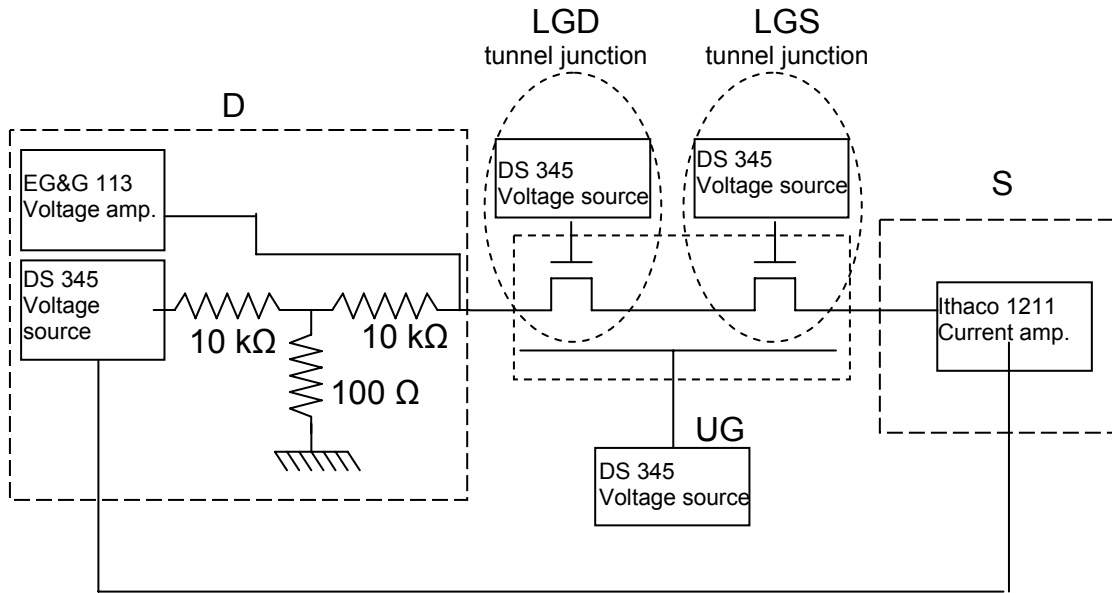

Figure 5-5 Measurement circuit of the tunable barrier SET. Gates and drain are connected to voltage sources, while the measurement of the bias voltage and the current through the device are made through amplifiers.

5.3.3: SET results

In the following I present results from a single device (JW2.4-23 EL). These results were confirmed in a second device (JW1.7-24 EL), the results of which will not be presented in this document. I start by confirming the operation of each individual gate at a temperature of 4 K. I do this to ensure that their electrical behavior does not change qualitatively from the room temperature results but also to quantitatively characterize their effect on the channel conduction at this temperature. In the case of the upper gate, for example, I set the drain voltage (V_{SD}) to 10 mV, with the source grounded and the lower gate voltages (V_{LGS} and V_{LGD}) to 1 V, to ensure that they will not be increasing the resistance of the channel underneath them. I then ramp the voltage of the upper gate (V_{UG}) and measure the current (I_{SD}) through the channel. The results appear in fig. 5-6. I then set V_{UG}= 3 V, to make the channel conducting and proceed by testing each of the lower gates. Fig. 5-7 shows the results for V_{LGD}. LGS exhibits similar behavior.

From fig. 5-6 we can see that the UG is turning the conduction on, as expected. From fig. 5-7 we see that LGD can control the conductance of the channel underneath it over four orders of magnitude. It can thus create a barrier of controllable resistance. In both cases I observe new features (marked with arrows in figures 5-6 and 5-7) on the current curve, that were not evident at room temperature. These features are completely reproducible upon sweeping the gate voltage again.
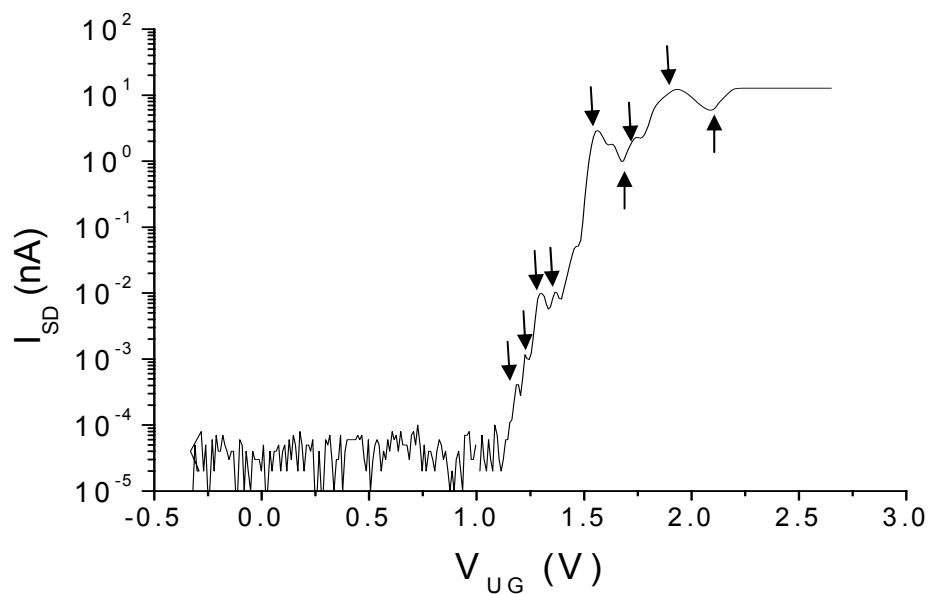
Figure 5-6 Current through the device (I_{SD}) as a function of V_{UG}. V_{SD}= 10 mV and V_{LGS}= V_{LGD}= 1 V. Arrows indicate new features at low temperatures.
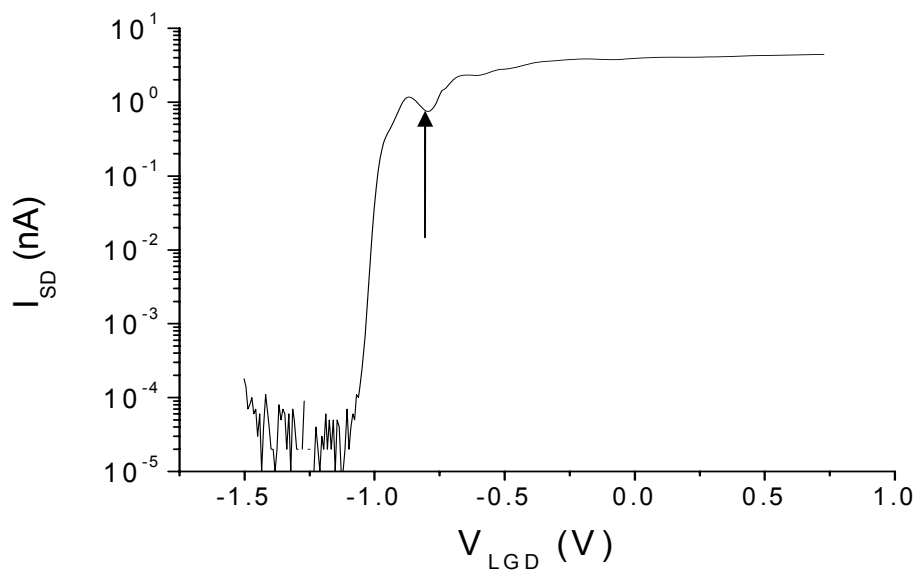

Figure 5-7 Current through the device (I_{SD}) as a function of V_{LGD}. V_{SD}= 10 mV, V_{LGS}= 1 V and V_{UG}= 3 V. Arrow indicates new features at low temperatures.

In order to understand these features we have to consider the possible origins of such "oscillatory" behavior. The fact that they are reproducible rules out noise effects. An obvious choice for an explanation, given our discussion of chapter 4, is single-electron effects. But from ref. [15] we know that single-electron effects are measurable only if at least one island is present in the device. In order to have one island we need to have at least two tunnel junctions. But in both cases considered above we do not have two intentional barriers. In the first case we do not have any intentional barriers and in the second we have only one. The only way we can attribute these to single-electron phenomena is by assuming that there are unintentional barriers in the Si channel. The existence of unintentional barriers is enough to explain these features on our current curves and is not unusual in the literature [15]. This clearly demonstrates uncontrollable effects which are not part of the nominal behavior of the device and should be addressed in future fabrication attempts.

I proceed by setting two barriers and operating the device as an SET. I set $V_{SD}=$ 10 mV and $V_{UG}=$ 3 V, so that the channel is conducting and I use fig. 5-7 to pick a value of V_{LGD} that gives a desired value of conductance for the barrier. For the data presented below I chose $V_{LGD}=$ -0.88 V which corresponds to $I_{SD}\approx$ 1 nA. I then ramp V_{LGS} which controls the conductance of the channel directly underneath it, but also modulates the potential of the island that is created between LGD and LGS through cross capacitance and measure the source drain current (I_{SD}). Using this method we can see clear Coulomb oscillations (fig. 5-8). Coulomb oscillations are supposed to be between a maximum current and a nominally zero one. In our case we have the

additional fact that the gate acts as a FET. Since we are looking at the subthreshold

region of the FET, where the current is increasing exponentially with gate voltage, we

see the Coulomb oscillations superimposed with the FET characteristic curve of LGS.

The fact that they are not periodic is attributed to the existence of unintentional tunnel

barriers in the channel.
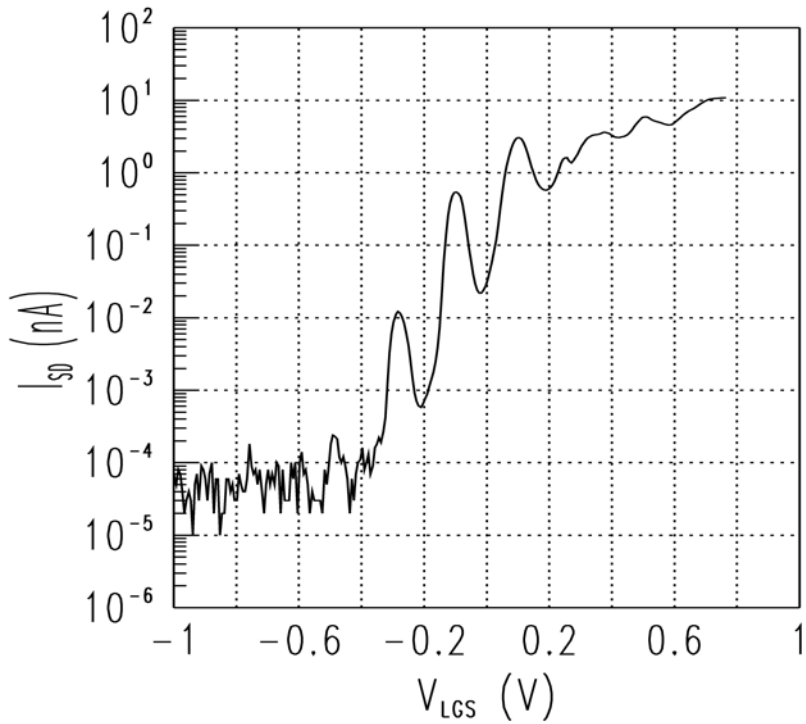
Figure 5-8 Coulomb blockade oscillations in I_{SD} as a function of V_{LGS}. V_{SD}= 10 mV, V_{UG}= 3 V and V_{LGD}= -0.88 V.

Despite the existence of unintentional barriers, the Coulomb oscillations are

dominated by the effect of a single island as can be seen from the contour plot in fig.

5-9. These data show clear Coulomb blockade "diamonds". The absence of additional

features is a strong indication that the conduction through the device is dominated by

a single island. In the case of multiple islands being involved in the conduction the stability diagram will change to demonstrate the fact that it has to be energetically favorable to tunnel through all islands in order to observe current through the device. In this case the areas of high conductance as the diamond closes at $V_{SD}= 0$ V would be removed. The value of I_{SD} increases rapidly with V_{LGS} because I am plotting values of V_{LGS} that correspond to the subthreshold region of the LGS FET: this can be seen from fig. 5-8.
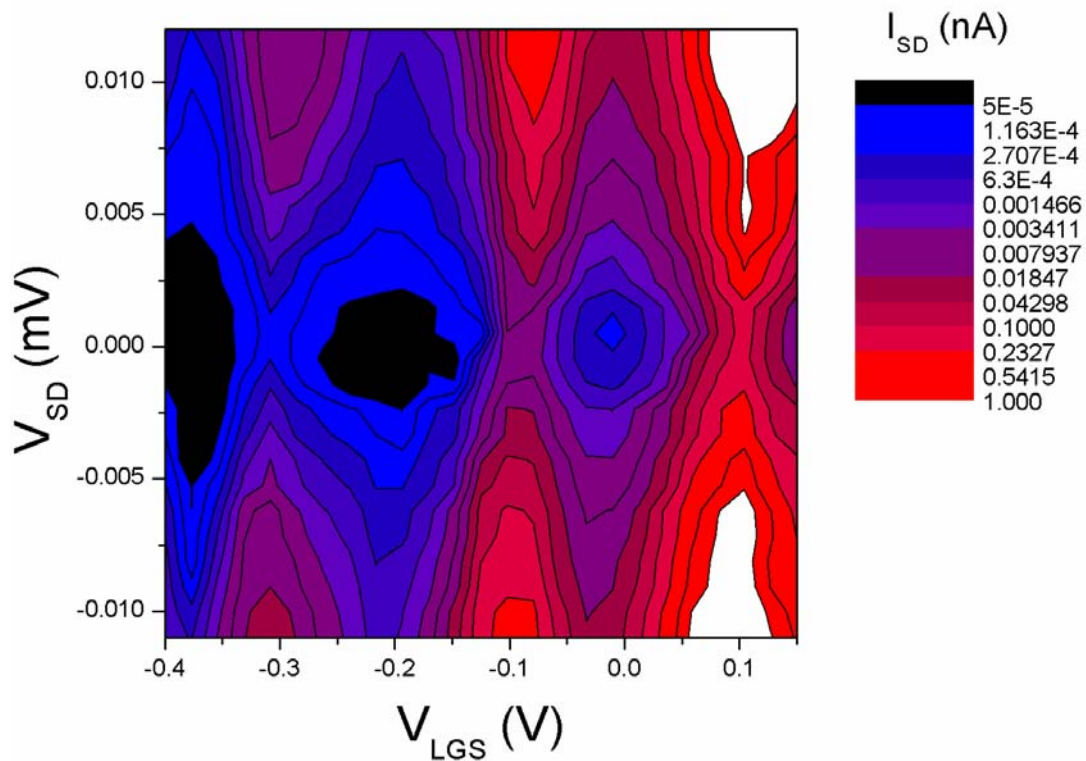
Figure 5-9 Contour plot of I_{SD} as a function of both V_{SD} and V_{LGS}. $V_{UG}= 3$ V and $V_{LGD}= -0.88$ V. Coulomb "diamonds" can be clearly seen.

As explained in chapter 4, the height of the diamond can be used to calculate the total charging energy of the island and thus the total capacitance C_Σ, and the slopes of the diamond give us the values of the barrier capacitances. In addition, from the period of the Coulomb blockade oscillations the gate capacitances can be calculated. The height of the diamond at V_{LGS}= 0 V is 3.5 meV which gives us C_Σ= 46 aF. I chose this value for the height based on the constant current curve of $I_{SD}\approx 0.002$ nA since it is the lowest value for which I get a clear diamond shape. The addition of the barrier capacitances (C_S= 17 aF and C_D= 27 aF) and the gate capacitances (C_{UG}= 1 aF and C_{LGS}= 1 aF) give us C_Σ> 46 aF. The inequality comes from the fact that I did not observe any oscillations due to the second lower gate, used as the fixed barrier, so I did not add the contribution of that gate capacitance to the total capacitance of the island. The fact that C_{LGS}= 1 aF and that for two other devices the capacitance of the lower gates to the island were all about 1 aF means that the true value of C_Σ is probably not more than a few aF larger than 46 aF. The fact that the values of total capacitance, calculated using two different methods, agree confirms that the effects we are seeing are due to a single dominant SET island. I note that the oscillations do not significantly die out for larger values of V_{SD}; this is common in devices where the properties of the barrier are controlled by the gate voltage [61, 68].

In figure 5-10 I present the results from measuring the Coulomb blockade oscillations as a function of temperature, at V_{SD}= 3 mV, V_{UG}= 3 V, V_{LGD}= -0.88 V. From this we can see that the oscillations persist to about 40 K. The inset in fig. 5-10 shows the temperature dependence of I_{SDmax}/I_{SDmin} near the peak at V_{LGS}= -0.1 V. Fitting these data to $I_{SDmax}/I_{SDmin} \propto e^{-\frac{e^2}{2C_\Sigma k_B T}}$, according to the discussion of section

4.4, I obtain C_Σ= 40 aF with uncertainty +10 aF, -15 aF, which agrees very well with

the two values determined by the methods described before. The uncertainty in the

calculated value comes from the uncertainty in the fitting of the data.
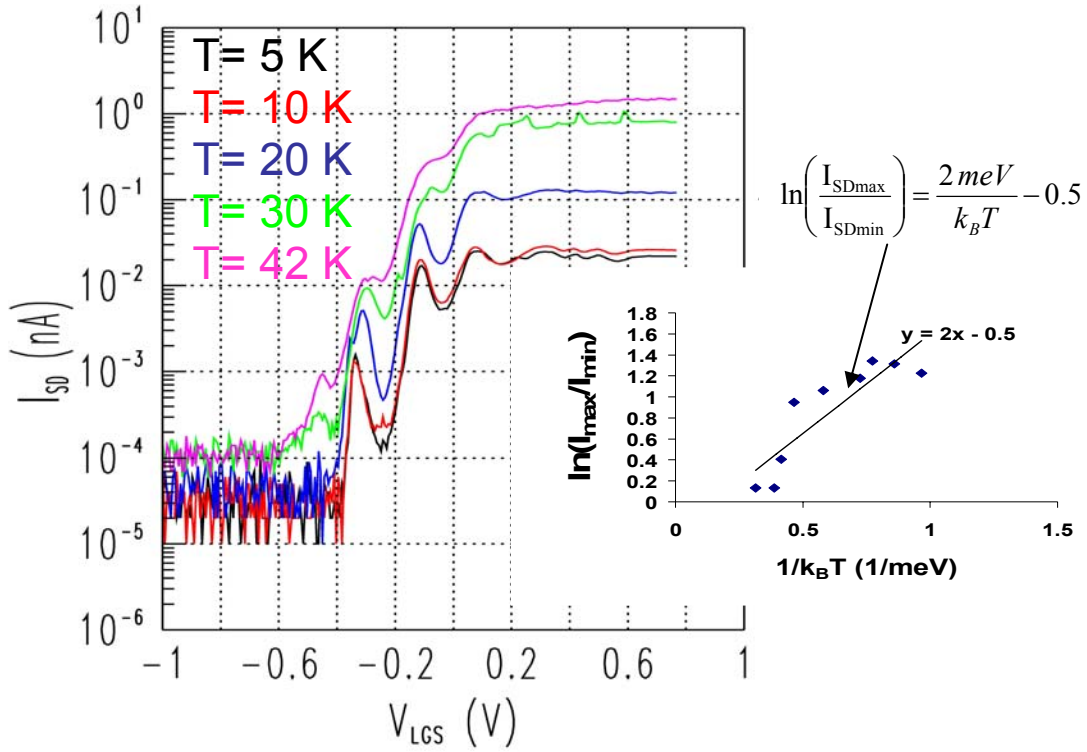
**Figure 5-10** I_{SD} vs V_{LGS} for temperatures of (5, 10, 20, 30, 42) K. The oscillations

persist to about 40 K. Inset: $\ln(I_{SDmax}/I_{SDmin})$ vs $1/k_B T$. The slope of the fitted line is

used in determining C_Σ.

5.3.4: $Q_0(t)$ results

Having demonstrated that these devices operate as single electron transistors, I

proceed to measure the charge offset drift ($Q_0(t)$). The method I use is as follows: I

take I_{SD} vs V_{LGD} curves over a period of several days. I pick a specific peak (near -0.1

V) in I_{SD} and measure the corresponding gate voltage $V_{LGS}(t)$. Then I obtain $Q_0(t)=$

$e[V_{LGS}(t)-V_{LGS}(t=0)]/\Delta V_{LGS}$, where ΔV_{LGS} is the value of voltage of an entire period,

which corresponds to one extra electron on the gate. The results appear in Fig. 5-11

where data is shown from May 18 to 31, 2007, for which the total $Q_0(t)$ range is about

0.1 e, with a drift of less than 0.01 e. The uncertainty in the reported value of $Q_0(t)$ is

0.01e, due to the fact that I could not measure the voltage corresponding to the peak

in question with a precision better than 2 mV. It is for this reason that the data appears

to be digitized. Also, the data seems to fluctuate mostly between $Q_0=$ -0.05 e and 0.

This indicates the possible existence of a two level fluctuator in our system. During

the measurement there were several liquid He transfers to the cryostat which cause

mechanical perturbations. The temperature of the device was 1K, while the rest of the

parameters were the same as the ones for the measurements presented in fig. 5-8.

These results show that the drift in $Q_0(t)$, for this type of device, is at least 100 times

better than in metal devices, where it typically changes by at least 1 e over a few days

[17]. They also show that our devices have comparable behavior to the previously

measured tunable barrier Si devices [66]. Finally, the robustness of this behavior is

demonstrated by the fact that even under mechanical perturbation (liquid He

transfers) the drift of $Q_0(t)$ remains orders of magnitude better than in metal devices.
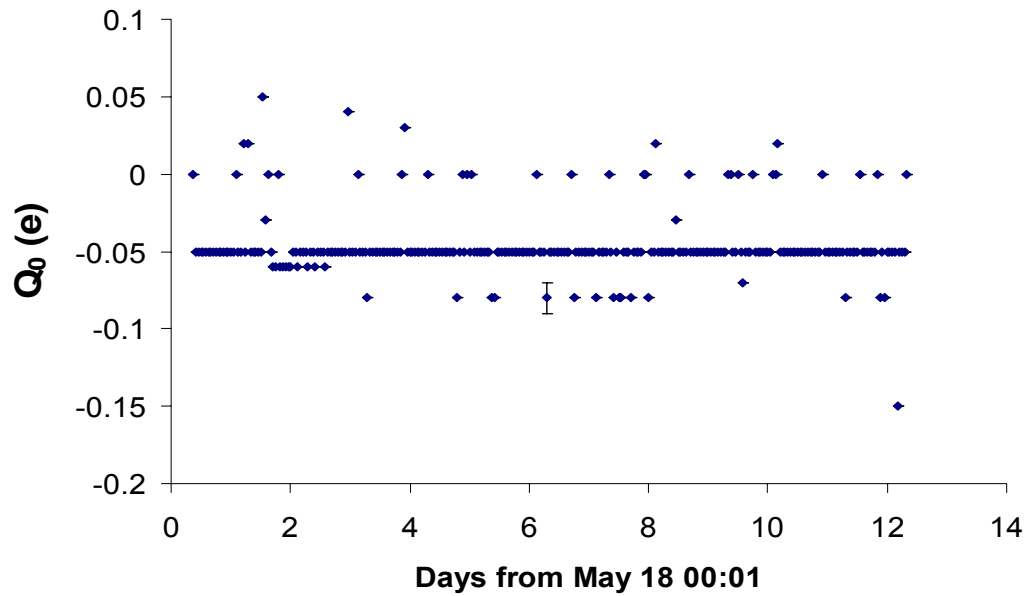
Figure 5-11 Charge offset drift Q_0 vs time. The uncertainty in $Q_0(t)$ is 0.01 e and is shown for one of the data points.

5.3.5: Conclusions

In conclusion, I have demonstrated the operation of tunable barrier Si single electron transistors. I have shown that, despite the existence of unintentional barriers, the device is dominated by a single Coulomb island. I have also confirmed the fact that the charge offset drift, $Q_0(t)$, in this type of devices is orders of magnitude less than in metal ones. This has been shown in the past by devices originating from a single fabrication source, NTT in Japan, and is confirmed by devices made at a different fabrication source, Cornell University in USA. I believe that this stability is a general characteristic of Si devices. Even though it is only demonstrated in terms of the charge offset drift, it is possible that other measurements that depend on the

stability in time of single-electron transistors will produce better results for these types of devices, compared to other materials. The difference in $Q_0(t)$ between metal and Si devices can be attributed to the difference in the quality of their fabrication processes. The microelectronics industry has invested huge efforts in perfecting the quality of the fabrication techniques used for Si devices. In particular the quality of the oxide used and the quality of the interface between the oxide and the Si have been extensively considered [69]. This has led to fabrication processes that produce more stable behavior than the ones used for any other material including metals, which in our case is demonstrated by the lower $Q_0(t)$. In particular, fewer and more stable charged traps and impurities in the oxide of interest will result in a smaller $Q_0(t)$. In the case of fewer traps it will be more unlikely that the trap exists close enough to the device to affect it. In the case of more stable ones, meaning traps that do not change their charge state over time, the effect will be a Q_0 with much less time dependence.

5.4: Future work

The results presented in this chapter are very promising in terms of our ability to fabricate and operate tunable barrier Si SETs. However, as was explained earlier, there are still problems associated with the fabrication of these devices, namely leakage issues and the existence of unintentional barriers in the Si channel. So, the next logical step in making "useful" devices must be an effort to correct these issues in fabrication. If future fabrication efforts yield devices closer to nominal, I can also start to examine different possibilities of putting them to practical use.

As an example, I can imagine trying to create a device where I use the lower gates to create an island of very small dimensions thus reducing the gate capacitance. Also by making the devices "thinner" and by trying to create wider barriers by pushing the lower gates to more negative values of voltage the barrier capacitances can be reduced. If I can do that, without increasing the resistance of the tunnel barriers to the point where the current is too small to measure, I can create a device that works in even higher temperatures than the one presented before. The ultimate goal would be operation at room temperature which is "only" a factor of seven higher than our current abilities. It might be a possible way to achieve reliable room temperature operation.

Finally, I would like to mention that the creation of better devices will enable their use in a variety of different applications, as explained in section 1.4. If we are able to fabricate devices without the current problems it will enable research into topics like metrology, quantum computing and even room temperature bio-detection. So, the creation of a Si-based tunable barrier SET is just the first step in a long list of research goals.

Appendix A

In this appendix I describe the predictions of the electrostatic response of a metal-SAM-air-metal capacitor to applied bias. As was explained in section 1.2, the measurement of the capacitance as a function of applied bias for such a system could be useful in answering some of the open questions in relation to the electrostatics os the metal-molecule contact.

Assume we have a system like in figure A-1:
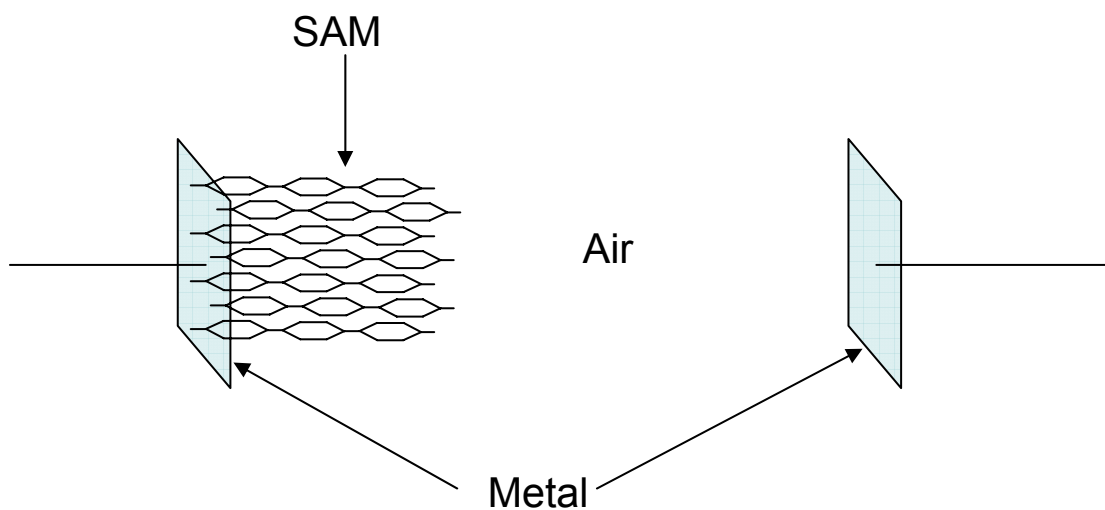
Figure A-1 A drawing of a Metal-SAM-air-metal capacitor

When no bias is applied the energy diagram of the system will look like:
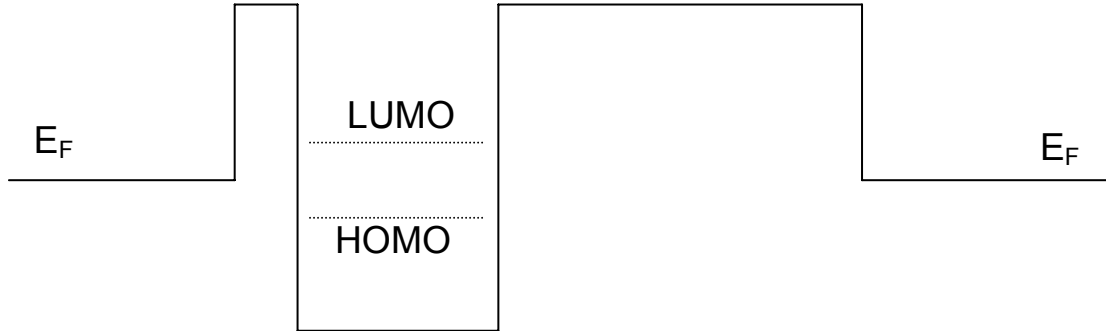
Figure A-2 Energy diagram of our capacitor under zero bias.

Applying a potential difference between the plates of the capacitor will cause the energy levels to change their relative positions. If at a voltage V_1, the Fermi energy of the metal plate in contact with the SAM crosses the HOMO or LUMO energy levels, there will be a transfer of charge from the metal onto the molecules or visa-versa.

If we assume that, up to that potential, the response of the SAM is that of a linear dielectric, the extra charge transfer will cause a change in the capacitance of the system. Further assuming that the LUMO (or HOMO) is delocalized and the molecules act like 'conductors', then we might expect to see a C-V curve like :
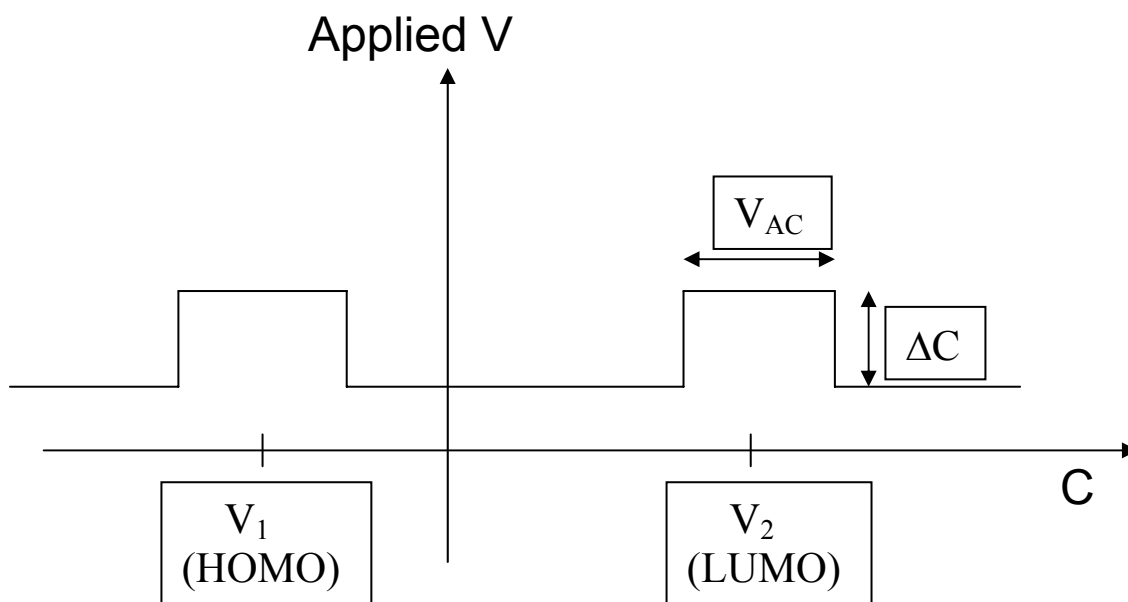
Figure A-3 Expected capacitance vs. applied voltage signal for our capacitor.

V_{AC} is the peak to peak voltage of the AC signal used to take the measurement.

For the following I assume that the molecules have length l, that the distance the extra charge "travels" on the molecule is Δx and that the area of the plates of the capacitor is A.
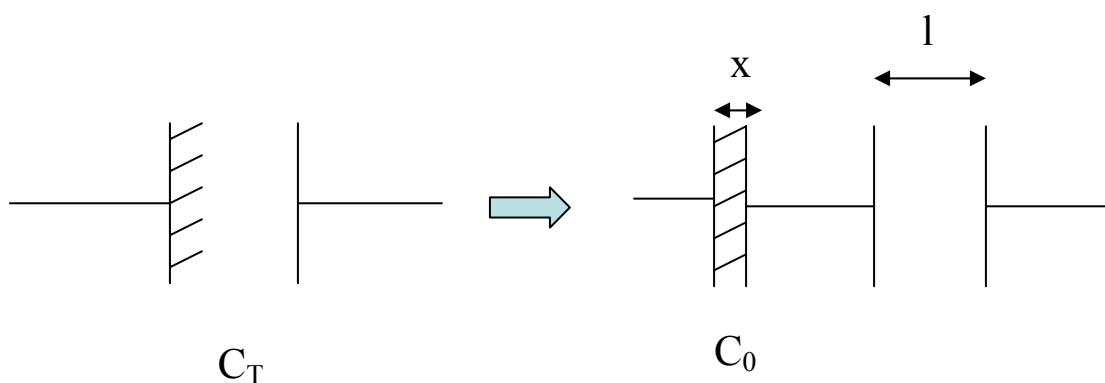
Figure A-4 Equivalent circuit for breaking the total capacitance in two different parts.

For the voltages where the SAM acts like a dielectric, it will be :

$C_0 = \varepsilon\varepsilon_0 A/x$

$C_T = (C_0\varepsilon_0 A/l)/((\varepsilon\varepsilon_0 A/x)+(\varepsilon_0 A/l))$

If $\varepsilon l/x \gg 1$, then (usually $\varepsilon \sim 2$, $l \sim \mu m$, $x \sim nm$) :

$C_T = C_0 x/\varepsilon l$ or

$C_T \approx \varepsilon_0 A/l$

When charge is transferred to the molecules, the change in the charge of the plates of the capacitor will be ΔQ_p. If there are N molecules in the SAM of length x and the extra charge on each of them, ΔQ_m, travels a distance Δx, then:

$\Delta Q_p = N\Delta Q_m \Delta x/(x+l) \approx N\Delta Q_m \Delta x/l$

If that happens when the voltage drop across molecules is V_m, then the voltage drop across the plates of the capacitor will be:

$V_p = (l/x)V_m$,

If we assume that the orbitals involved with the movement of the extra charge are "completely" delocalized and so the SAM acts like a metal, it will be:

$\Delta C = C(l-\Delta x)-C(l) = [\varepsilon_0 A/(l-\Delta x)]-\varepsilon_0 A/l$

so $\Delta C \approx \varepsilon_0 A\Delta x/l^2$

If we assume that $\Delta x = x = 2$ nm and $N \approx A/1nm^2$, then:

$\Delta C = (10^{-20}$ F $) A/l^2$

On the other hand :

$C_T = (10^{-11}$ F/m $) A/l$

So, for example, if $A = 1mm^2$ and $l = 1\mu m$:

$C_T = 10^{-11}$ F and $\Delta C = 10^{-14}$ F

The existence of the step on the C-V curve should give us a measure of the delocalization of the molecular orbital that lines up with the Fermi energy, since ΔC will be linearly related to Δx.

Complete delocalization would mean conductive behavior of the molecules ($\Delta x = x$), partial delocalization would mean that Δx is a fraction of x, while complete localization would mean dielectric behavior, $\Delta x = 0$, which would lead to a curve with a spike. So, defining Δx to be an "effective metallic length" for the molecules in question, we will have:

$$\Delta x = (l^2/\varepsilon_0 A)\Delta C$$

If the HOMO-LUMO stay fixed with respect to the Fermi energy of the metal plate that is far from the SAM, then the value of V_1 would be a direct electrical measurement of the energy difference between the Fermi energy of the metal plate connected to the SAM and the HOMO-LUMO.

If the HOMO-LUMO stay fixed with respect to the Fermi energy of the metal plate in contact with the SAM, there should be no step, or spike, feature in the C-V curve.

If the HOMO-LUMO levels move with respect to both Fermi energies (most likely situation), one could investigate how the capacitance between the molecules and the metal that is not in contact influences that relative motion. This could be done by changing the distance between the plates of the capacitor in steps and recording C-V curves for each step. For each distance the curves might look like figure 4.

In this case the values of V_1 and V_2 would not directly give us the energy difference between the fermi energy and the HOMO-LUMO. One can assume that, if V_{t1} and V_{t2} are the true energy differencies then it will be $V_1=\lambda V_{t1}$ and $V_2=\lambda V_{t2}$. We can assume that our system in this case will be equivalent to:
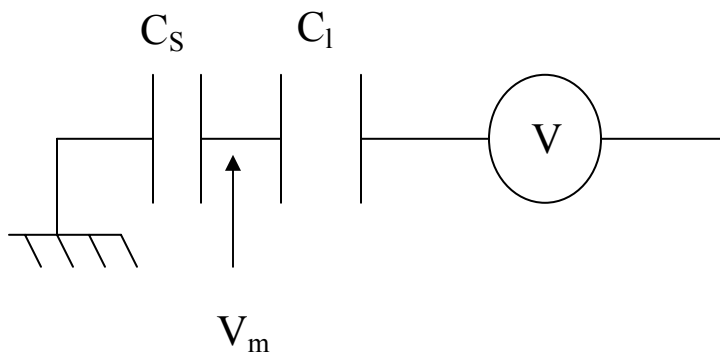
Figure A-5 Circuit representation of the metal-molecule-air-metal capacitor.

where C_s represents the capacitance of the Sulfur bond to Au, the SAM is represented by the metallic line connecting the capacitors and C_l is the capacitance between the SAM and the electrode that is not in contact. I am assuming that for $V<V_2$ or $V>V_1$ there is no charge transfer from the electrode to the SAM and so the S-Au bond acts like a capacitor. So we have:

$C_l V = V_m(C_s+C_l)$

Concentrating on V_2 (or V_1), we can say that as V goes to V_2 (or V_1), V_m goes to V_{t2} (or V_{t1}). So:

$V_{t2} = (C_l/(C_l+C_s))V_2$ or

$\lambda = (C_s/C_l)+1$ or

$\lambda = 2\varepsilon_1(l/x)+1$,

where ε_1 is the effective dielectric constant of the S-Au bond and I have assumed that the length of C_s is $x/2$. Then it is:

$V_2 = V_{t2} + 2\varepsilon_1 V_{t2}(l/x)$

Measuring V_2 for different values of C_l, and so for different values of l, would lead to a curve like the one shown in figure A-6, where $l_0 = -(x/2\varepsilon_1)$. From this curve one could find the value of V_{t2} (or V_{t1}). Of course, in order to observe a step in the C-V curve, and thus have values for V_2, λ has to be as small as possible. For example if $l =$ 1 μm and $\varepsilon_1 = 2$, then $\lambda = 2001$. If $V_{t2} = 0.5$ V then our step would happen for $V_2 =$ 1000 V, which is too high to observe. Also, in order for the V_2-l curve to give us useful information, we would to know l with great precision. A precision of the order of nm would be needed in order to get a sensible value for V_{t2} (or V_{t1}).

The hope is that this experiment can measure electrically the energy difference between the HOMO-LUMO of the SAM and the Fermi energy of the metal connected to it (**V_{t1}, V_{t2}**). Also it might be able to measure the delocalization of the orbitals involved (**Δx**).
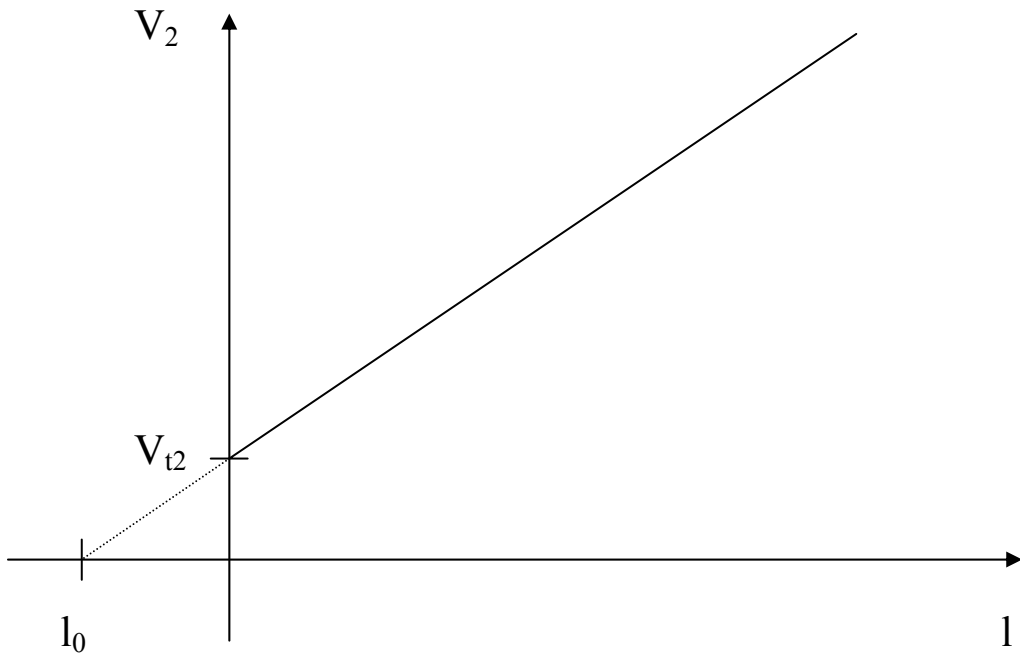
Figure A-6 Voltage for which a change in capacitance is observed (V_2) as a function of electrode separation.

Appendix B

The wiring of our cryostat was done with four main goals in mind:

1) The first one is that the wiring from room temperature to base temperature does not put too much of a heat load ($\dot{Q}$) on the system. If it were, it would be impossible to cool the samples to the desired low temperatures.

2) The second goal is to shield the sample from high frequency noise. High frequency noise will heat the device up and reduce our ability to observe single-electron phenomena. As an example of this I mention that a signal of 20 GHz corresponds to an equivalent temperature of 1 K or to an equivalent Coulomb energy of 0.1 meV or to a total capacitance of an SET island of $C_\Sigma = 1$ fF, which close to the typical values for metal SETs.

3) The third goal in wiring the cryostat is to keep the low frequency noise floor to a minimum. The signals measured in our experiments are very small (pA and nV) and so electrical noise can be detrimental to our measurements.

4) Finally, our system was designed to offer modularity or flexibility in terms of changing various aspects of the wiring.

For the measurements done in our dilution refrigerator we use a total of fourteen coaxial cables going from room temperature down to base temperature. Ten of them are designed to operate at low frequencies while the other four serve as leads for high frequency operation. A schematic representation of the system appears in figure B-1. The four high frequency cables have been further subdivided into two groups of two

(sets 11, 12 for intermediate frequency operation and 13, 14 for high frequency

operation), due to differences in their material. The set of ten low frequency cables

are represented by set 1-10.
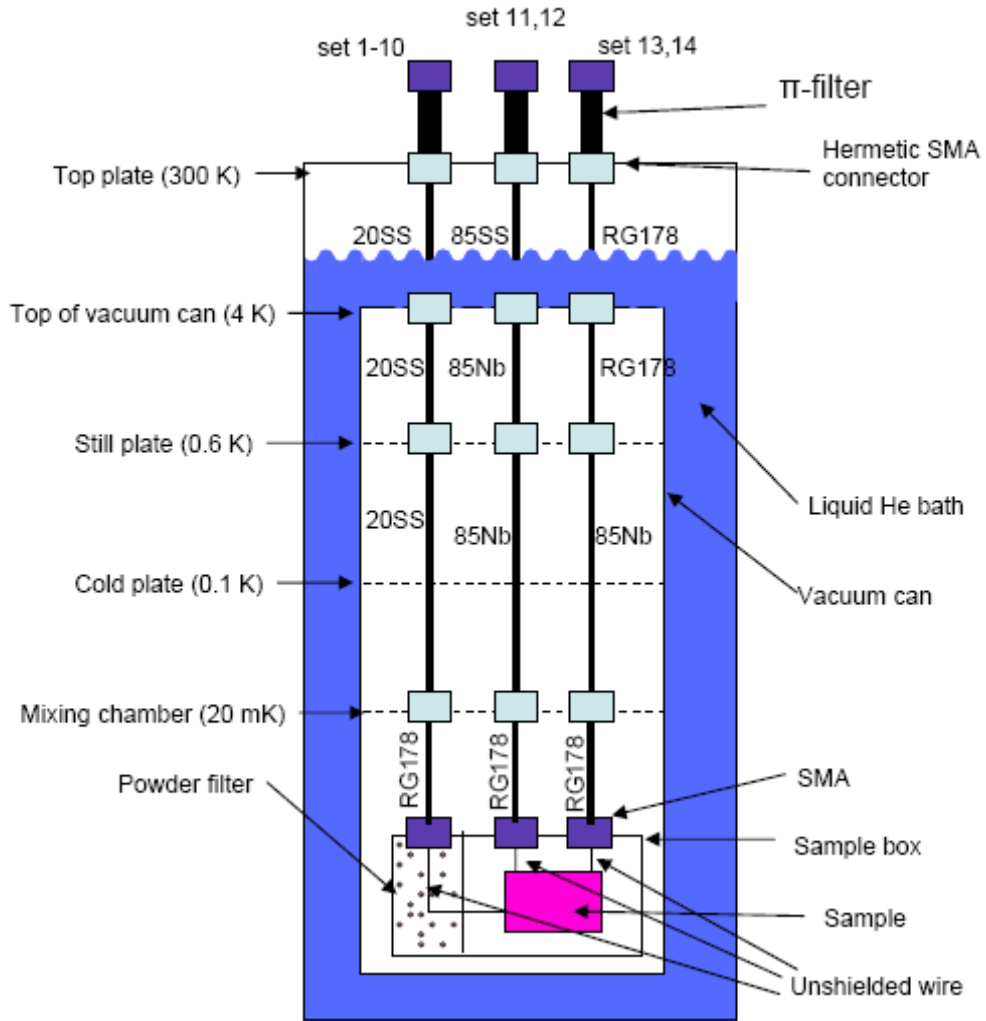
Figure B-1 Schematic representation of the cryostat wiring. Cable sets (1-10), (11,

12) and (13, 14) extend from the top plate to the sample box. The details of each set

are presented in the text.

We can see from figure B-1 that there are four different sections to each cable. The first is going from room temperature (the top plate of the cryostat) to the top of the vacuum can, which is at 4 K. There the cable is terminated to an SMA plug. This is connected to a hermetically sealed SMA (jack to jack) connector. This SMA serves a double purpose. It has a glass to metal hermetic seal which provides a vacuum tight connection but also provides a thermal link between the inner and outer conductors of the coaxial cables. The second section of the cable starts at the vacuum can SMA (with the same SMA plug connection to the cable as before) and ends at a hermetic SMA at the still plate, which is at 0.6 K. The third section starts at the SMA of the still plate and ends at the mixing chamber plate, which is at 20 mK or base temperature, terminated by a hermetic SMA. There is a thermal link between the cold plate (0.1 K) and the outer conductor of the coaxial cable (only in the case of set 1-10). After the mixing chamber plate, the fourth section is coaxial cables connecting to the sample box which is held at the same temperature as the mixing chamber. In the cases of sets 11, 12 and 13, 14 there is no link to the cold plate.

The material used for cables sets 1-10, 11, 12 and 13, 14 are as follows (also see figure B-1):

20SS: These are coaxial stainless steel with an outer diameter of 0.02 inches (Microcoax UT-20-SS-SS). Advantages include 1) small thermal conduction due to small size and poor conductivity of SS; 2) large low-pass filtering due to large inductance; 3) mechanical flexibility (ability to bend) due to small size.

85SS: Coaxial stainless steel semirigid cables terminated at both ends with SMAs (Microstock SMA-UT-85-SS-SS-SMA) with an outer diameter of 2.7 mm or 0.085 inches. Advantages include the small low-pass filtering for use in high frequency operation and the small thermal conduction.

85Nb: Coaxial Nb (with 1% Zr) semirigid cables (Microcoax UT-85-Nb-Nb) with an outer diameter of 0.085 inches. These are superconducting below ~ 9 K. Advantages include 1) small thermal conduction due to the fact that they are superconducting; 2) small low pass filtering for use in high frequency operation.

RG178: Coaxial Cu flexible cables terminated with SMAs (RF Connection SMA-RG178-SMA). Advantages include 1) mechanical flexibility (ability to bend); 2) small low pass filtering for use in high frequency operation.

1) Thermal load ($\dot{Q}$)

In terms of the thermal load of these cables, I can calculate it for each section of each wire, for the inner and outer conductors. The results of these calculations appear in table B-1, for set 1-10 and table B-2 for sets 11, 12 and 13, 14. The heat load on the mixing chamber can be compared with the stated cooling power of the mixing chamber by the manufacturer, which for a temperature of 20 mK is 2 μW, for example. I can also compare with the expected boiloff rate of the liquid He in the bath (1 L per hour for 1 W of load). I have used information of this kind to include the acceptable loads for each case in the two tables. It is clear that the thermal loads are within the acceptable range.

	300 K to 4 K (W)	4 K to 0.6 K (mW)	0.6 K to 0.1 K (µW)	0.1 K to 20 mK (µW)
$\dot{Q}_{acceptable}$	0.1	1	-	2
$\dot{Q}_{inner}$	2×10^{-4}	1×10^{-4}	-	2×10^{-2}
$\dot{Q}_{outer}$	2×10^{-3}	7×10^{-4}	2×10^{-1}	5×10^{-2}

TABLE B-1 Calculated heat load ($\dot{Q}$) of the cryostat cables (set 1-10) between the different heat sinking plates.

	300 K to 4 K (W)	4 K to 0.6 K (mW)	0.6 K to 20 mK (µW)
$\dot{Q}_{acceptable}$	0.1	1	2
$\dot{Q}_{inner}$ (set 11, 12)	2×10^{-3}	2×10^{-2}	2×10^{-1}
$\dot{Q}_{outer}$ (set 11, 12)	2×10^{-2}	1×10^{-1}	1.4
$\dot{Q}_{inner}$ (set 13, 14)	2×10^{-3}	2×10^{-2}	2×10^{-1}
$\dot{Q}_{outer}$ (set 13, 14)	4×10^{-2}	2×10^{-1}	1.4

TABLE B-2 Calculated heat load ($\dot{Q}$) of the cryostat cables (sets 11, 12 and 13, 14) between the different heat sinking plates.

2) High frequency performance

In terms of high frequency shielding of our sample I return to figure B-1. There we can see that commercial π-filters (Lark Engineering LR3000-3AA) are used on the top plate of the cryostat for all leads. These π-filters are low pass filters with a cutoff frequency of ~ 3 GHz (figure B-2). For the low frequency set of cable assemblies (set 1-10) the UT-20-SS-SS cable used is very lossy (high inductance and stray capacitance to ground), so it also acts as a low pass filter with a less sharp frequency dependence (figure B-3). The third place of filtering is in the sample box. There the inner of the coaxial cables goes through a powder filter before being connected to the sample. The powder filters act similarly to the lossy cables (figure B-4) and are placed as close to the sample as possible to attenuate high frequency signals picked up due to black body radiation from parts of the cable at higher temperatures. The combination of the above filters and cables accomplishes the goal of shielding the sample from high frequency noise. For signals above 6 GHz we have a nominal attenuation of ~ 200 bB.
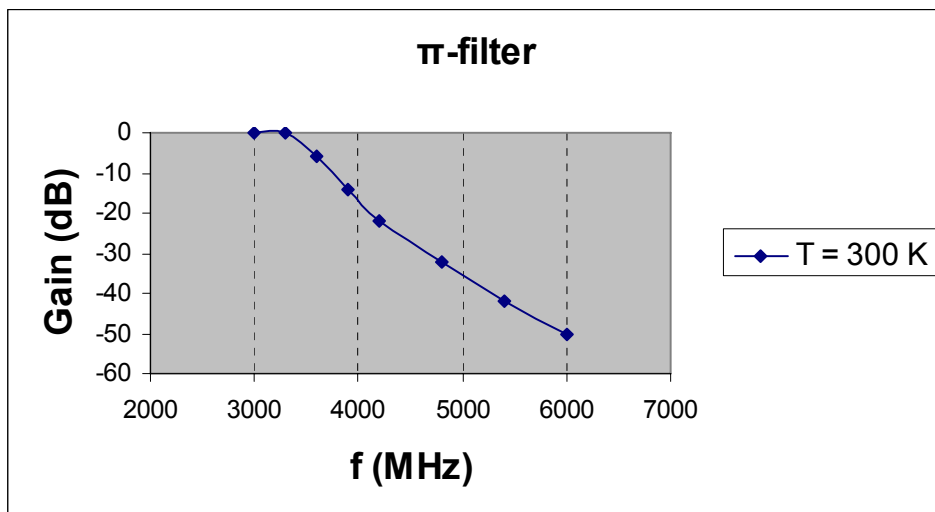
Figure B-2 Gain vs. frequency for the π-filters used in our system.

Figure B-3 Gain vs. frequency for the 20SS cable assembly used in our system.
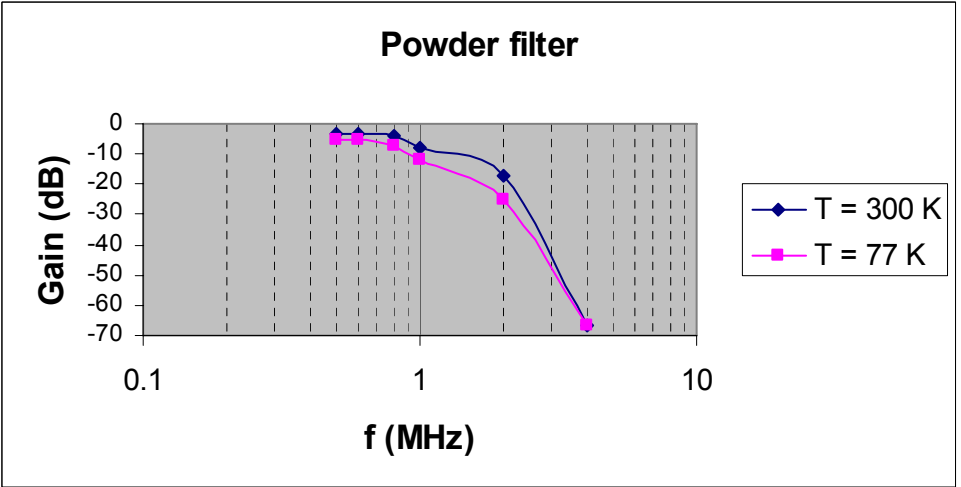
Figure B-4 Gain vs. frequency for powder filters used in our system.

For the high frequency cable assemblies of sets 11, 12 and 13, 14, the goal is to have minimum distortion and attenuation of the high frequency signals in contrast to the goal of set 1-10. The cables used in these sets attenuate significantly less than in the case of set 1-10. The gain vs. frequency characteristics of cable assemblies 85SS

(same as 85Nb) are shown in figure B-5. The characteristics of the RG178 assemblies appear in figure B-6. In figures B-5 and B-6 I plot the total insertion loss (attenuation including cables and SMAs). Furthermore, these cable assemblies do not go through powder filters before the sample. Finally, the π-filters on the top plate can be easily removed if the measurement requires frequencies higher than ~ 4 GHz. Without the filters, we can see that signals up to 400 MHz are attenuated by < 5 dB or less than a factor of two in voltage ratio. When dealing with very sensitive low frequency measurements, though, both sets 11, 12 and 13, 14 can be disconnected from the sample box, so as not to introduce high frequency noise.
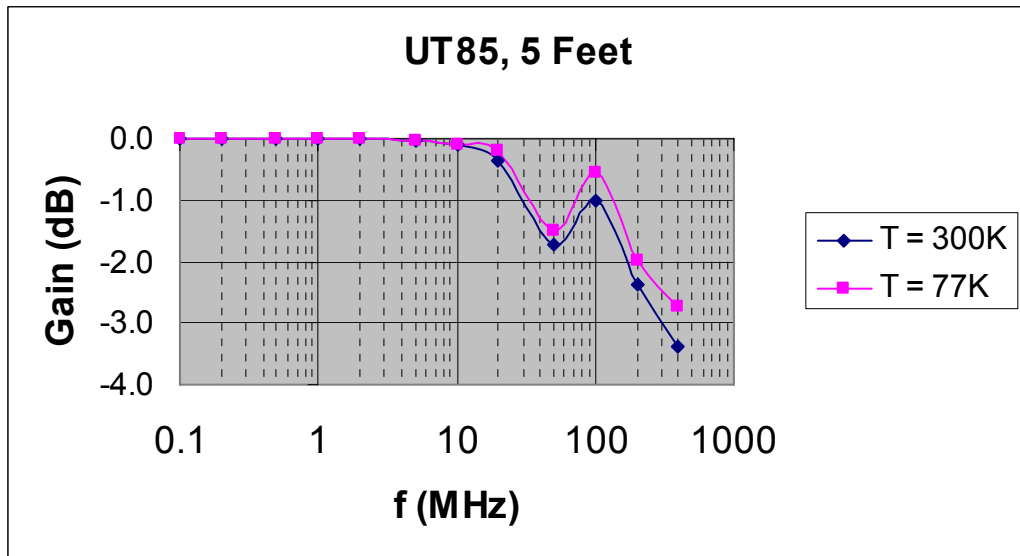
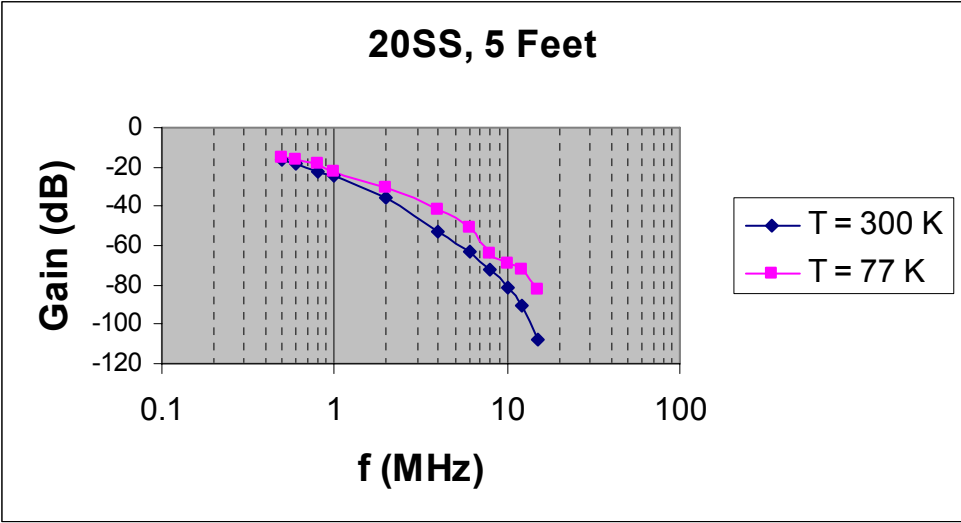**Figure B-5** Gain vs. frequency for the 85SS (and Nb) cable assemblies used in our system.

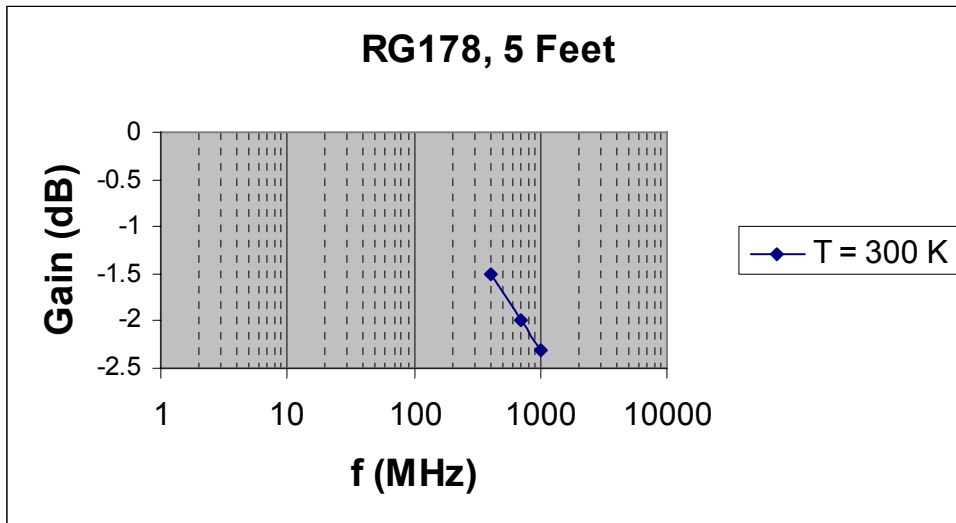**Figure B-6** Gain vs. frequency for the RG178 cable assemblies used in our system.

3) Low frequency noise

Keeping the low frequency noise of the cables to a minimum, which is the third

goal of the wiring, is a less straightforward task. The use of coaxial cable shields the

inner conductor from most capacitive pick-up of noise. The other major source of

noise is the inductive pick-up of 60 Hz signals due to ground loops. Our system is not

optimally designed to eliminate ground loops. On the contrary there exist several

ground loops since the outer of the coaxial cables used are grounded in many

different places. We have found, though, that the use of a 10 kΩ resistor in series with

the voltage divider connected to the source (see figure 5-5) reduces the injected noise

current to an acceptable level.

4) Modularity

Finally, the modularity or flexibility of the design of our system is demonstrated by the fact that we can remove and reattach any section of the cables in between the SMA connectors. The cables are broken into four different sections as can be seen from figure B-1. Each section is terminated in an SMA connector, as was mentioned earlier, and is not permanently soldered anywhere. I note that some sections are more complicated to remove than others. As an example, the most complicated section is from 4 K to 0.6 K: to replace one or more cables, one must a) unscrew all five at 0.6 K, b) unscrew the vacuum flange bolts, c) take off the vacuum flange and the five cables, d) unscrew and replace one or more cables, e) clean off, put a new In gasket on, and put back the vacuum flange, f) screw back all five cables to the 0.6 K plate. This introduces a slight complication, but overall the system can be modified more easily than in the case of soldered connections. Also, the fact that we can easily remove the π-filters from the top plate or disconnect the high frequency cables from the sample box is a demonstration of the modularity of the wiring design.

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