

ABSTRACT

Title of dissertation:

ELECTROMAGNETIC BANDGAP STRUCTURES FOR BROADBAND SWITCHING NOISE MITIGATION IN HIGH-SPEED PACKAGES

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For the past two decades, silicon-based complementary metal-oxide semiconductor (CMOS) technology and circuits have been advancing along an exponential path of shrinking device dimensions, increasing density, increasing speed, and decreasing cost. Electronic design complexity is in constant acceleration and new designs have to incorporate new features, which inevitably will require faster processing time. In recent years this acceleration rate has drastically decreased because of various constraints, such as static power dissipation due to leakage current, the effect of wires and interconnects and the decreased immunity of modern devices to noise, interference and voltage fluctuations on their Power Distribution Network (PDN).

Lowering the power supply voltages and hence the power consumption of a single transistor, has been possible due to the fact that these new technologies are able to provide smaller and faster transistors with lower threshold levels. The benefits associated with lowering the threshold levels of the transistors used in a given device comes at a high-price, specifically the decrease of immunity of such device to noise and fluctuations of the power supply voltage.

The research work carried out in this dissertation, addresses the concept of embedding Electromagnetic Bandgap (EBG) structures in conventional power distribution networks in order to increase the immunity of the circuits that feed from such networks to noise and voltage fluctuations. Underlying theories of Embedded EBG (EEBG) structures and design methodologies are presented. Various design concepts, based on simulations, measurements and different modeling techniques developed during this research work are presented. The accuracy of these methods is analyzed by comparing results of these techniques with experimental results.

Also, this work shows that EEBG structures are not only very effective in the suppression of switching noise in high-speed circuit but also they suppress Electromagnetic Interference (EMI) caused by such switching and they provide increased immunity for their PDN to external sources of noise.

Finally new EEBG configurations, topologies and miniaturized structures are introduced that overcome the limitations of current switching noise mitigation techniques, including initial EEBG designs to provide immunity against high-bandwidth noise, voltage fluctuations and radiation, new EEBG configurations, topologies and miniaturized structures are introduced and their efficacy is demonstrated. The novel designs developed

during this research provide noise mitigation over a wide range of frequencies, and also extends the suppression frequency range into the sub-gigahertz region, only using a single EBG design with smaller patches than those used in previous works.

ELECTROMAGNETIC BANDGAP
STRUCTURES FOR BROADBAND
SWITCHING NOISE MITIGATION
IN HIGH-SPEED PACKAGES

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2005

DEDICATION

To my family, especially my grandmother Sedighe, my uncle Shahpour, my aunt Shahin,
and my lovely wife Raha.

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Chapter 1. Introduction, Background and Objective of the Dissertation

1.1 Introduction

For the past two decades, silicon-based complementary metal-oxide semiconductor (CMOS) technology and circuits have been advancing along an exponential path of shrinking device dimensions, increasing density, increasing speed, and decreasing cost. Electronic design complexity is in constant acceleration and new designs have to incorporate new features, which inevitably will require faster processing time. In recent years this acceleration rate has drastically decreased because of various constraints, such as static power dissipation due to leakage current, the effect of wires and interconnects and the decreased immunity of modern devices to noise, interference and voltage fluctuations on their Power Distribution Network (PDN) [1]-[3].

Switching noise is known to be the main source of noise and voltage fluctuations on the power planes of the printed circuit boards (PCB) and packages that contain modern

CMOS-based devices [4]. The fundamental mechanism behind the generation of this type of noise is either high-speed time-varying current or the vias that pass through the parallel plate of a power distribution network, or a combination of both. The flow of high-speed time varying current through such vias, causes radiation. The radiated waves use the parallel plate wave guiding structure to propagate. At the edges of the PCB, a portion of these waves are reflected back and the rest is radiated. The radiated waves cause interference problems, and the reflected waves cause a resonance behavior in the cavity-like structure created by the parallel plates and the dielectric material between them [5]. The ratio of reflected waves to radiated waves is frequency dependent. Other vias that pass through the same parallel-plate structure act as receiving antennas. In this scenario, the devices connected to the receiving vias become victims of the radiating via. This scenario is worsened when multiple vias radiate at the same time. The type of noise caused in such scenario is known as simultaneous switching noise (SSN). The transient currents, drawn by the internal fast switching logic gates of an integrated circuit can be in the order of hundreds of milliamperes and can give rise to significant unwanted voltage fluctuations on the PDN of a PCB.

SSN, if uncontrolled, can cause logic circuits to switch state falsely. This false switching, in turn, can cause serious malfunctions in the subject circuits with catastrophic consequences. As a result, one of the key challenges for designers of modern high-speed circuits is to design a PDN capable of delivering large amounts of current at low voltage. Therefore it is absolutely necessary to reduce the power bus impedance as much as possible

while suppressing the propagation of waves generated by the consumption of that current by the switching devices.

Methods introduced in past works, in order to confront switching noise, all try to reduce the resonance effects of the cavity-like structure. The most widely used and effective of them include the use of decoupling capacitors [6],[7], embedded capacitances [8] and capacitors [9], the use of dissipative and lossy components along the PCB and at its edges [10][11], dividing power planes in power islands [12], and via stitching [13].

The use of decoupling capacitors is the most wide spread method and it consists of placing large capacitors around the sources of noise to disrupt high-frequency fluctuations on the power planes by creating a low-impedance path between the planes at these frequencies. This method, although very effective, is limited by the fact that capacitors have leads and connections to the PCB which at high-frequency become inductive, and therefore tend to create an open circuit rather than a short circuit. Other methods try to overcome this frequency limitation, in one way or another. Embedded capacitors and capacitances try to minimize the length of the problematic leads. Dissipative components and via stitching, try to damp down the radiated waves in order to avoid resonance (and radiation) effects. Their effectiveness requires materials which operate at high frequency. Power islanding is also widely used, but its applicability is limited to applications in which isolation is the goal such that the source of noise and the susceptible components are kept on different power islands.

In summary, all methods mentioned above have an effective range of at most few hundred megahertz and are expensive to implement, if not ineffective at high frequencies.

Recently the use of electromagnetic bandgap (EBG) structures has been introduced as an effective inexpensive method for SSN suppression in the GHz frequency band [14][15]. These earlier works, while introducing for the first time a realizable concept for SSN suppression in the GHz region, were somewhat less attractive to implement in the high-frequency PCBs used in the low-cost highly competitive consumer electronics industry. The first unattractive feature was the relatively narrow band of noise suppression. The second, the earlier introduced structures were relatively large in dimensions in comparison to the size of the PCB in which they are inserted.

This dissertation covers methods for design and analysis of EEBG structures. It describes the underlying theories of operation of EBG structures. In addition, advanced designs presented in this work eliminate the first critical drawback of early design by providing ultra-wide band suppression over a wide range of frequencies in which previous methods cannot be used or they provide only limited efficacy. Furthermore the miniaturization concepts and methodologies introduced in this work eliminate the second drawback transforming early designs into a viable and practical solution for broadband switching noise suppression in PCBs.

1.2 Anatomy of Switching Noise in Electronic Power Distribution Systems

As explained in the previous section, switching noise is usually caused by the high-speed time-varying currents needed by high-performance digital circuits. The flow of these currents through vias between layers of a printed circuit boards, causes radiation. The radiated waves use the parallel plates created by the power planes to propagate. Simultaneous Switching Noise (SSN) is a noise created while many outputs of a digital

circuit switch at the same time. SSN cannot be quantified in precise measure because of its dependence on the geometry of the board and current paths. Various studies have concentrated on modeling this phenomenon [16] [17] [18].

The continuous and rapid increase of clock frequency is another source for switching noise. In fact high-speed small currents have an equivalent impact on switching noise as switching of circuits that involve large amounts of current (simultaneous switching). Figure 1-1 shows a general schematic for generation of switching noise within a power bus of a PCB. A high-speed or high-power (or both) device that consumes power from two parallel power planes is the first type of noise. A via that passes through these plane and is not necessarily connected to any of them is another type of noise source. Electromagnetic waves generated by these sources of noise use the parallel plates to propagate and therefore induce noise on other signals passing through the power bus (vias), other devices that feed from the same power bus and eventually radiate from the edges of the board.

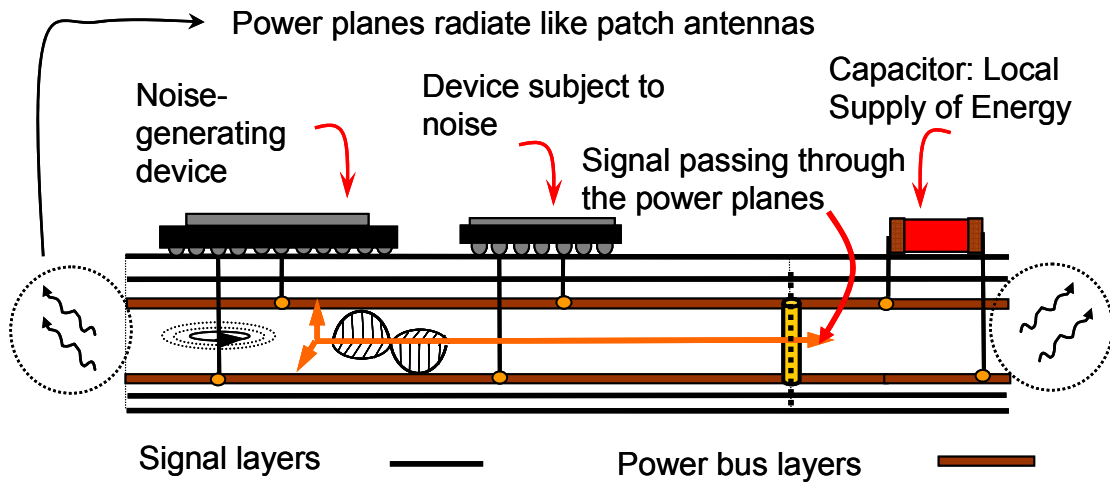


Figure 1-1 Switching noise generation mechanism in a PDN of a multilayer printed circuit board.

This section discusses the phenomenon of wave propagation and resonance in a parallel-plate structure and elaborates more on the theoretical fundamentals of such propagation and resonance.

1.2.1 Electromagnetic Wave Propagation and Resonance in an Infinite Parallel-plate Structure

The ground and supply voltage planes of the power distribution network constitute a parallel-plate waveguide. This type of structures can therefore support TE, TM and TEM modes [19]. The TEM waves correspond to the situation, where there are no electric or magnetic fields in the direction of propagation. TE and TM modes correspond to situations in which the fields have no electric or magnetic field in the direction of propagation, respectively. In the idealization of the parallel-plate waveguide illustrated in Figure 1-2, the

dimensions in the x -direction is assumed to be much larger than the thickness h of the waveguide such that all fringing fields and any variation in the x -direction can be neglected. For this type of analysis the wave propagation is one-dimensional and in the z -direction.

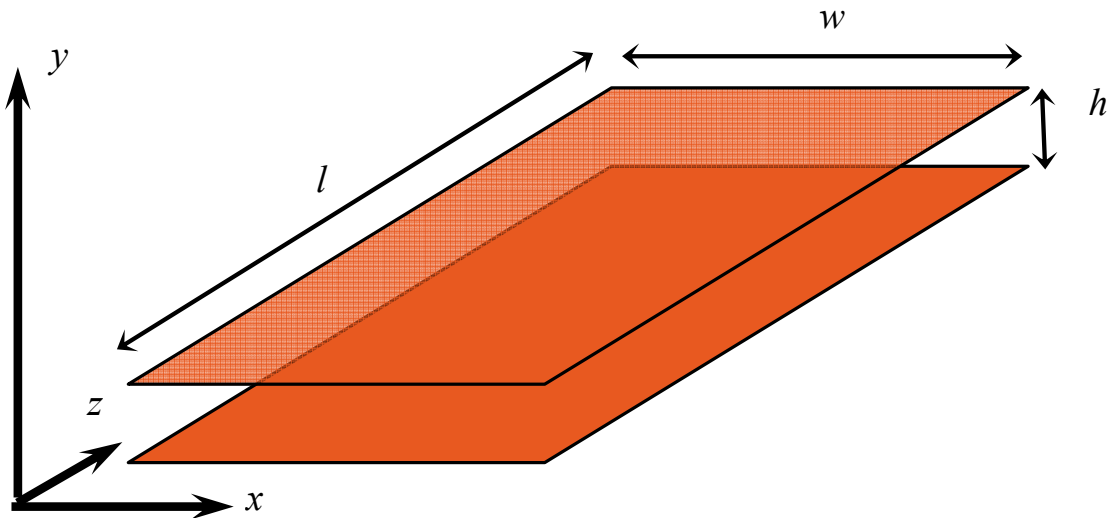


Figure 1-2 Diagram for an ideal parallel plate waveguide as a model for the power planes of a PCB.

The TEM waves correspond to the situation, where there are no electric or magnetic fields in the direction of propagation. TE and TM modes correspond to situations in which the fields have no electric or magnetic field in the direction of propagation, respectively. For all types of propagating waves,

$$k_c = \frac{n\pi}{h}, \beta = \sqrt{k^2 - k_c^2}, f_c = \frac{n}{2h\sqrt{\mu\epsilon}} \quad 1-1$$

In which k_c is the wave number, β is the propagation constant and f_c is the cutoff frequency. The constant n is the number of the propagating mode for which k_c , β and f_c are defined. k is the propagation constant of an equivalent wave in free space.

The first mode, which is a TEM mode is when n is equal to zero, hence:

$$\beta = k = \omega\sqrt{\mu\epsilon}, f_c = 0 \quad 1-2$$

Typical power planes have a thickness of less than 2 mm. This implies that the parallel-plate TE_n and TM_n modes have cut-off frequencies in the order of tens or hundreds of GHz and are not a major concern for systems operating at 20 GHz and below. The only modes of concerns are the TEM modes and the resonance modes induced by the finiteness of the power planes. In fact, in the calculation of the parallel-plate waveguide modes [19], it was assumed that the plates have infinite length in the z-direction. In practical power planes, the width (w) and length (l) of the plates are finite. In this case, waves propagating to the edge of the waveguide are reflected back and forth. Therefore, in addition to the parallel-plate modes, rectangular cavity modes are also excited. Both TE_{mnp} and TM_{mnp} modes are excited. Their cut off frequency is given by the same equation,

$$f_{res}(m, n, p) = \frac{1}{2\pi\sqrt{\mu\epsilon}} \sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{l}\right)^2 + \left(\frac{p\pi}{h}\right)^2} \quad 1-3$$

Since h is very small compared to l and w , only TE_{mn0} and TM_{mn0} modes have low enough resonance frequencies that fall into the frequency range of interest (below 20 GHz), hence:

$$f_{res}(m, n) = \frac{1}{2\pi\sqrt{\mu\epsilon}} \sqrt{\left(\frac{m\pi}{w}\right)^2 + \left(\frac{n\pi}{l}\right)^2} \quad 1-4$$

As an example a PCB with dimensions of 10 cm x 10 cm x 1.5 mm has resonance frequencies of 1.41 GHz, 2 GHz, 3.16 GHz, 4 GHz, 5.08 GHz, 6 GHz and so on.

More detail on the subject of power plane resonance the reader is referred to references [5] and [8].

Obviously, switching noise has its maximum impact if generated at the resonance frequencies of the PCB.

A very effective metric to characterize switching noise in PCBs is transfer impedance. Transfer impedance is defined as the ratio between the induced voltage at a victim location on the power bus and the injected current at a source location. The scattering parameter matrix $[S]$ can be transformed into the impedance matrix using [20]:

$$[Z] = Z_0 \frac{[I] + [S]}{[I] - [S]} \quad 1-5$$

Where $[I]$ is the identity matrix and $Z_0 = 50 \Omega$ is the characteristic impedance of the network analyzer. In $[Z]$, Z_{21} represents the open circuit voltage at a victim location on the power bus generated by the current injected at a source location; hence it is the transfer impedance.

From equation 1-5 the magnitude of Z_{21} is related to S_{21} measurements as:

$$Z_{21} = \frac{2Z_0 S_{21}}{4 - S_{21}^2} \quad 1-6$$

If $|S_{21}|, |S_{12}| \ll 1$ and $S_{11}, S_{22} \approx -1$ as it normally happens for power planes,

$$|Z_{21}|_{dB} \approx |S_{21}|_{dB} + 28dB \quad 1-7$$

As a result $|S_{21}|$ measurements can and they will be used directly to study the transfer impedance $|Z_{21}|$. Furthermore, attenuation in the S_{21} parameter as a result of employing noise suppression techniques will be directly associated with a decrease in transfer impedance, hence noise coupling.

1.3 Research Objectives and Thesis Structure

In summary, the objective of this research is to present a practical and very effective method for broadband switching noise suppression in high-speed CMOS based electronic packages.

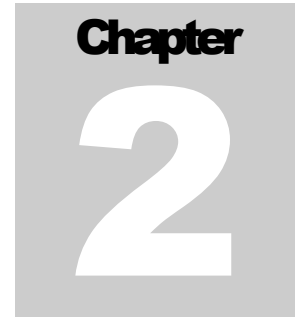
Chapter 2 covers theoretical and empirical modeling techniques as well as simulation and experimental methods for the study of SSN suppression using EEBG structures and practical considerations for their fabrication.

Chapter 3 introduces the first ever design concept for wideband noise suppression of SSN, based on classical filter theory and the similarities of EEBG structures to bandstop filters.

Radiation from PCBs caused by switching noise is studied in chapter 4 and mitigation techniques based on EEBG structures are presented. Finally, chapter 5 introduces the concept of combining EEBG structures with commercial high dielectric

constant material for the purpose of achieving a very large suppression bandwidth that extends to sub-gigahertz frequencies but at the same time reduces geometrical sizes of EEBG structures in a drastic manner, therefore achieving the last milestone required to transform early EEBG design into practical, matured and effective mitigation technique for switching noise suppression in PCBs of high speed circuits.

Conclusions, future works and potential extension to this thesis will be covered in chapter 6.



Chapter 2. Power Planes with Embedded Electromagnetic Bandgap (EEBG) Structures

2.1 EEBG Structures and the Switching Noise Suppression Concept

Electromagnetic Band-Gap structures introduced as High-Impedance Surfaces (HIS) in early stages of research in this field [21], belong to a broad family of engineered materials called meta-materials, which have been initially employed for antenna applications because of their unique behavior. In fact, HIS structures can satisfy a Perfect Magnetic Conductor (PMC) condition over a certain frequency band and impose a 0° reflection phase to normal incident waves, making them suitable for applications such as coupling reduction between antennas and antenna directivity improvement. Although EBG (HIS) structures have been extensively studied, these studies have focused on open structures (not enclosed in environments like PCBs) and normal incident waves, such as antenna application, therefore derived theories and models are only applicable to such

cases. For more information on open EBG structures the reader is referred to reference [21] and also the references mentioned in these references.

The use of EBG structures in PCB environments was first reported in [14], to suppress simultaneous switching noise in printed circuit boards. A similar concept was also introduced in [15].

When inserting an EEBG structure in the parallel-plate waveguide-like structure of the PDN of a PCB, a resonant circuit composed of the top plate, a single patch, the corresponding via and the plane that connects the vias together is created. In fact this circuit provides a low-impedance path to high-frequency currents in the power-planes therefore shorting the planes (resonance) at the physical location of the patches within the band-stop frequency range, thus suppressing propagation. The diagram of Figure 2-1 illustrates the generation of switching noise, the propagation of waves in the PDN, their suppression using EEBG structures and their radiation from the sides of the PCB.

In summary, each row of EEBG introduces transfer zeros. At the resonance frequencies of these transfer zeros a low-impedance path is created between the plates of the power bus shorting all the signals propagating at that frequency. When other rows of EEBG ribbons are added to the PDN, they shift the resonance frequency of the single row ribbon, creating multiple transfer zeros, therefore a band-stop region. The overall effect of this design is therefore to shorten and shield the power bus of the PCB within a range of frequencies.

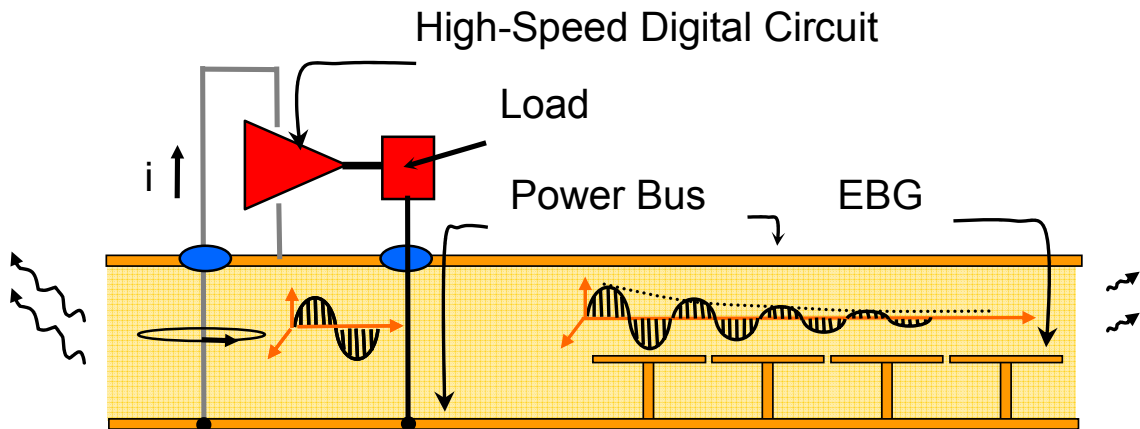


Figure 2-1 EBG structures embedded in PCBs: Switching noise generation, radiation and suppression mechanisms.

It is important to emphasize the fact that simple EEBG structures presented in this work are targeting the 0.5-20 GHz range, therefore pushing the limit of previous methodologies. Since simple EEBG structures have impractical geometrical sizes in the 500 MHz to 2 GHz frequency range, more complex EEBG structures need to be employed. In addition, in view of ongoing miniaturization of electronic systems the implementation of this method requires the availability of miniaturized EEBG structures with appropriate patch sizes, although the concept introduced in this paper can be generally applied regardless of the size of the EEBG structures. For wideband radiation reduction from hundreds of MHz to few GHz either a combination of different methods or use of advanced EEBG structures is the best solution. Such advanced EEBG structures are covered in chapter 3 and chapter 5.

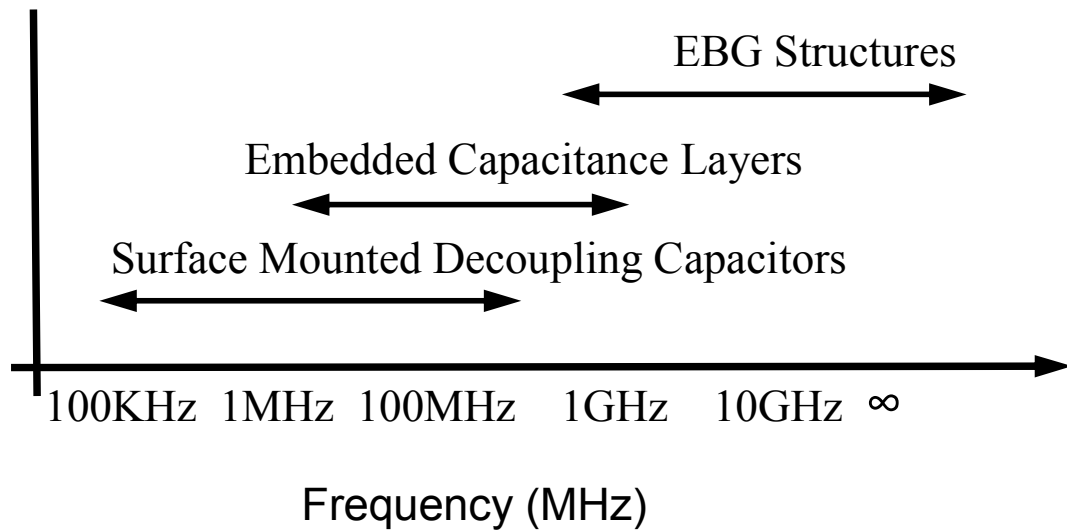


Figure 2-2 Efficacy range of different switching noise reduction methods.

Figure 2-2 shows the efficacy range of EEBG structures covered in this work in comparison to conventional switching noise suppression methodologies.

Early design for EEBG structures can also be applied to the same range of frequencies for which conventional methods are used (i.e. up to few hundred MHz). To provide noise suppression for the MHz range, the simple EEBG patches introduced earlier can be used, but the patch sizes will become possibly impractical. For practical purposes, to use the EEBG structures for noise suppression in the MHz range, more complex EEBG structures need to be considered. Alternatively, one can use a combination of the techniques introduced in this thesis with conventional methods.

2.2 Design Methodologies, Parameters and Issues

In the last few years, different methods have been utilized for the design and test of EEBG structures. Goals for all these methods include but are not limited to describing the

behavior of EEBG structures [22], studying the effect of various design parameters (e.g. patch shape, patch size, via diameter, gap diameter, dielectric constant of the substrate, etc.) [23] and deriving new EEBG structures for more effective noise suppression (e.g. higher bandwidth) [24].

Methods used so far for design and analysis of EEBG structures can be separated in six main categories based on direct experimentation, numerical wave analysis (frequency domain and time domain), circuit modeling and transmission line modeling. This section describes and compares different methods for designing EEBG structures.

2.2.1 Direct Experimentation

This method consists of fabricating PCBs with EEBG structures and performing S-parameter measurements in order to derive the band-stop region of the fabricated design. The major advantage of this method is the accuracy of the derived bandgap. The major drawback is when this method is used as a design method, a large design space needs to be explored. This can be costly and time consuming. For this scenario, approximate methods need to be developed to finalize the design by fabricating and testing a couple of possible configurations..

Figure 2-3 and Figure 2-4 show a typical experimental setup used for characterization of a sample EEBG structure. Figure 2-3 shows the patch layer of an EEBG structures placed in between two lateral pieces of PCB without any structure (i.e plain). A separate layer is mounted on top of this structure and pressed together as shown in Figure 2-4. For better clarity of the structure a lateral illustration of the final structure is shown in Figure 2-6. In this setup if port 1 is excited using a Vector Network Analyzer (VNA), waves can

propagate (and resonate) in the two lateral slabs of PCB (from port 1 to port 4) but propagation from port 1 to port 2 is suppressed by the presence of the EEBG structure. In this scenario a gap present in S_{21} represents the operating range of the EEBG structure under test. Figure 2-5 shows a typical S_{21} measurement using this technique.

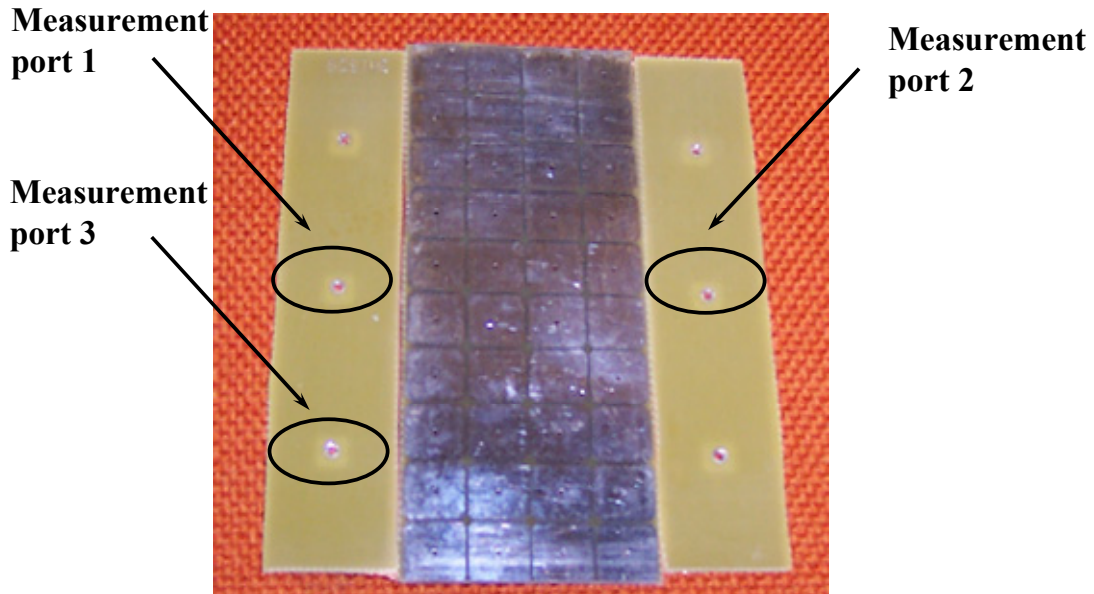


Figure 2-3 Test setup for EEBG structures with patches of 20 mm x 20 mm. A separate one layer board is mounted on top of this one as a second power plane.



Figure 2-4 Measurement setup using a Vector Network Analyzer (VNA). S_{21} is a representative for transfer impedance between port 1 and port 2.

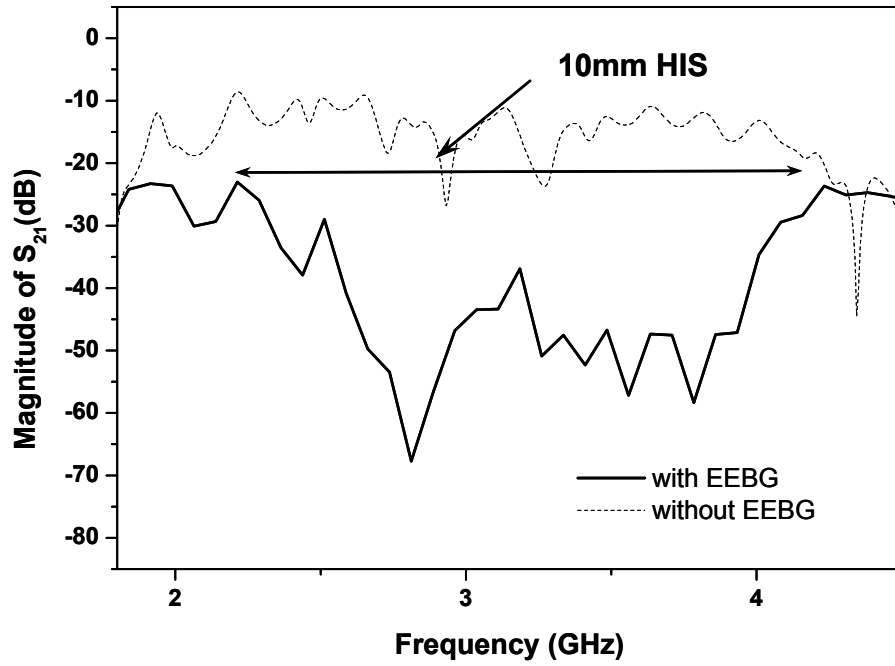


Figure 2-5 Sample measurement for the setup depicted in Figure 2-3

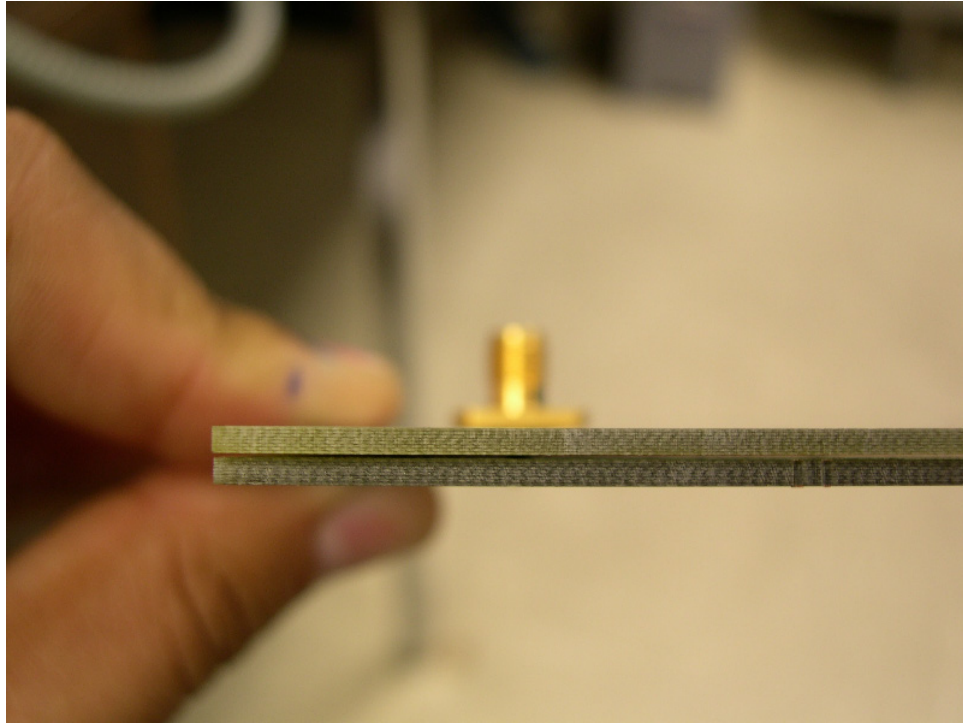


Figure 2-6 Lateral view of the PCB under test.

2.2.2 Full-wave Analysis of a Complete Structure

Full wave analysis of a complete EEBG structure consists of either analytically solve Maxwell's equations in the structure or simulation of the exact desired structure with all possible details using a numeric finite-element or finite-difference (time or frequency) method [25]. Analytical solutions of Maxwell's equations do not lead to a closed form equation.

On the other hand, simulations by numerical analysis can be achieved either by writing specific code for solving Maxwell's equations in EEBG structures or by using generic commercial tools. The performance (execution time and memory allocation) of this method is limited to the performance of those tools. Based on experience the real-size

models to be simulated become so large that even commercial tools take days to provide a fairly accurate result, assuming convergence happens.

2.2.3 Dispersion Diagram Extraction

A numerical indirect procedure that has proven to be very effective and fast consists of extracting the dispersion diagram of the EEBG structure. Such diagram describes the propagation characteristics of an infinitely periodic structure composed of EBG patches. In this work the dispersion diagram is extracted using the commercial finite element full wave solver HFSS [26], by considering only one patch (or a unit cell) and applying a periodic boundary condition on the sides of the cell (to mimic the presence of the cell in a periodic structure extending to infinity), and Perfect Electric Conductor (PEC) boundary condition on the top and bottom of the cell for the power planes, as shown in Figure 2-7 [27].

Dispersion diagrams show the relationship between wave numbers and frequency. These diagrams present propagating modes and band gaps that can potentially exist between such modes (in a periodic structure at a given frequency of operation, many modes in different directions may be excited). Brillouin, in his theory of wave propagation in periodic structures [28], states that for any periodic structure there are certain vectors (i.e., directions) in the unit cell of the periodic structure that constitute a boundary region of propagation called irreducible Brillouin zone. According to this theory, deriving the propagating modes in the direction of these vectors suffices to cover all the possible direction of propagation within the lattice. Hence the problem of deriving the propagating modes excited at a certain frequency reduces to finding such modes only in the directions of the vectors of the irreducible Brillouin zone. For the type of structure considered in this

work, the border of the irreducible zone is illustrated in Figure 2-7 and it consists of the direction pointing from Γ to X, from X to M and from M back to Γ .

Therefore, in light of Brillouin theory, a dispersion diagram for EEBG structures with rectangular patches will consist of three regions. In each region the wave vector β , translated into the phase shift between the sides of the unit cell shown in Figure 2-7 is considered. This translation allows the derivation of dispersion diagram using traditional eigenmode full-wave simulators. In these simulations, the unit cell structure and required phase shifts (shown as Phase 1 and Phase 2 in Figure 2-7) are given to the simulator. The simulator calculates the frequencies of propagating waves that would generate such phase shifts. For a wave propagating in the x direction with no variation in the y direction, phase 1 varies between 0° and 180° and phase 2 is kept constant at zero degree. This corresponds to the Γ to X direction. The X to M direction corresponds to phase 1 being constant and equal to 180° and phase 2 varying from 0° and 180° . This represents the second region in the dispersion diagram. The third region is represented by the M to Γ direction in which both phase are equal and changing from 180° back to zero. For the case of wave propagation in a space filled with only dielectric, as there is no dispersion, the diagram will constitute of a straight line in the first and third region. In the second region the relationship is quadratic. Equation 2-1 shows the frequency-phase relationship for a wave propagating in an infinite free space filled with dielectric,

$$f(\beta d) = \begin{cases} \frac{c}{2\pi d}(\beta d) & \Gamma - X \\ \frac{c}{2\pi d}\sqrt{\pi^2 + (\beta d)^2} & X - M \\ \frac{c\sqrt{2}}{2\pi d}(\beta d) & M - \Gamma \end{cases} \quad 2-1$$

In this equation d is the period of the structure, and c the speed of light in the dielectric.

With the presence of EBG structures, the surface becomes dispersive, therefore the frequency-phase relationship of propagating modes will not be the same as in free space. A gap between the upper limit of one propagating mode and the intersection of the free space propagation line with the next propagating mode represents a region in which the surfaces do not support any propagation.

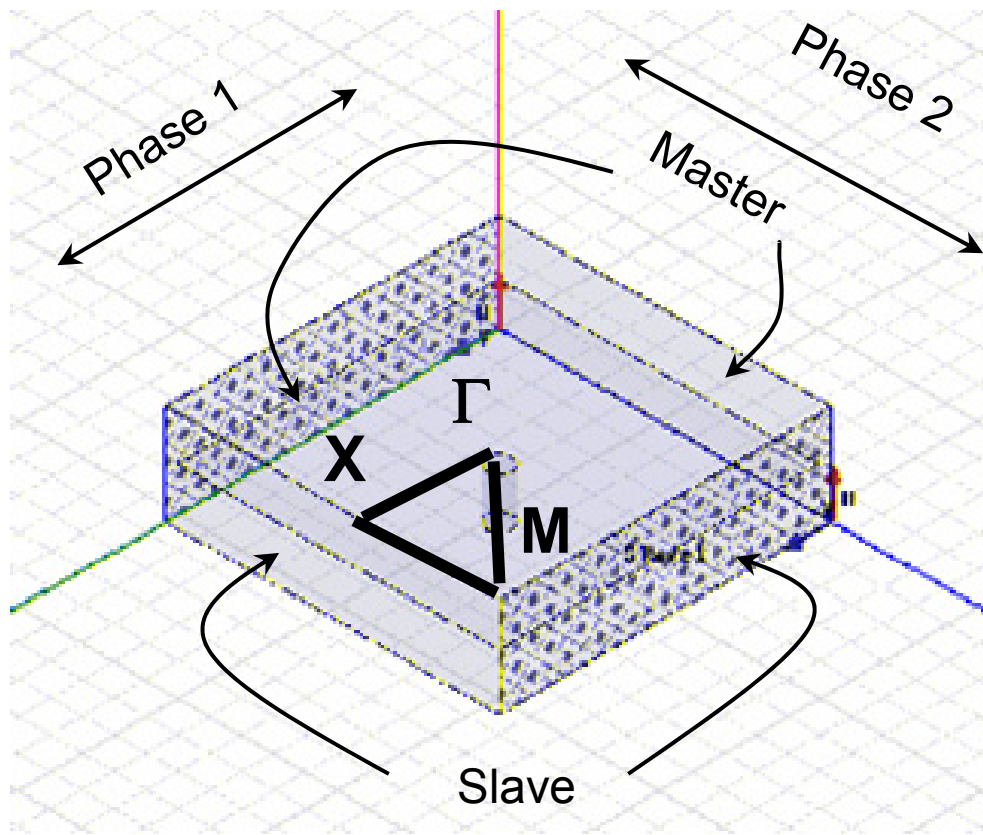


Figure 2-7 Diagram representing the simulation model used to extract the bandgap of an EEBG structure using dispersion diagrams. The computational domain includes a single cell. Periodic (Master/Slave) boundary conditions are placed in the x-z and y-z planes. The top and bottom planes of the cell are perfect electric conductors (PEC). The Brillouin triangle is shown above the top plane.

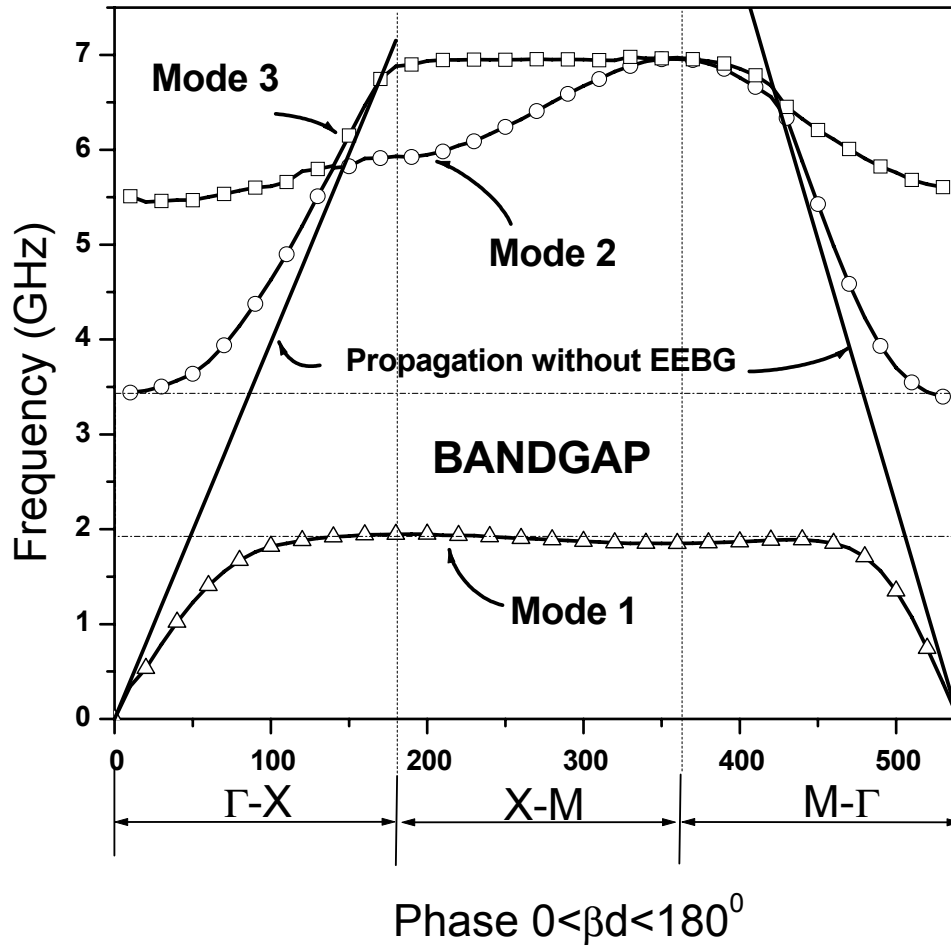


Figure 2-8 Dispersion diagram derived for an EEBG structure with dielectric material of dielectric constant of 4.1, via diameter of 0.8 mm, gap size of 0.4 mm and board thickness of 3.08 mm. Patches are located at equal distances from the power planes between them and their size is 12 mm x 12 mm.

2.2.4 Double-symmetric Model

Another numerical procedure that has proven to be very effective and it is the fastest method among full-wave simulations in terms of computational speed consists of creating a semi-infinite structure in between two ports as shown in Figure 2-9. The lateral sides of this model are “symmetry boundary conditions” that create a double-mirror-like structure in which the model would look infinite in the y-direction (both positive and negative).

This is a direct method whose output is the S-parameters (between port 1 and 2) and does not result in dispersion diagrams, therefore can be directly compared to experimental results (except for the fact that ideal material and metals with zero thickness are considered for the simulations). In addition, in reality the size of the board in the y direction is not infinite.

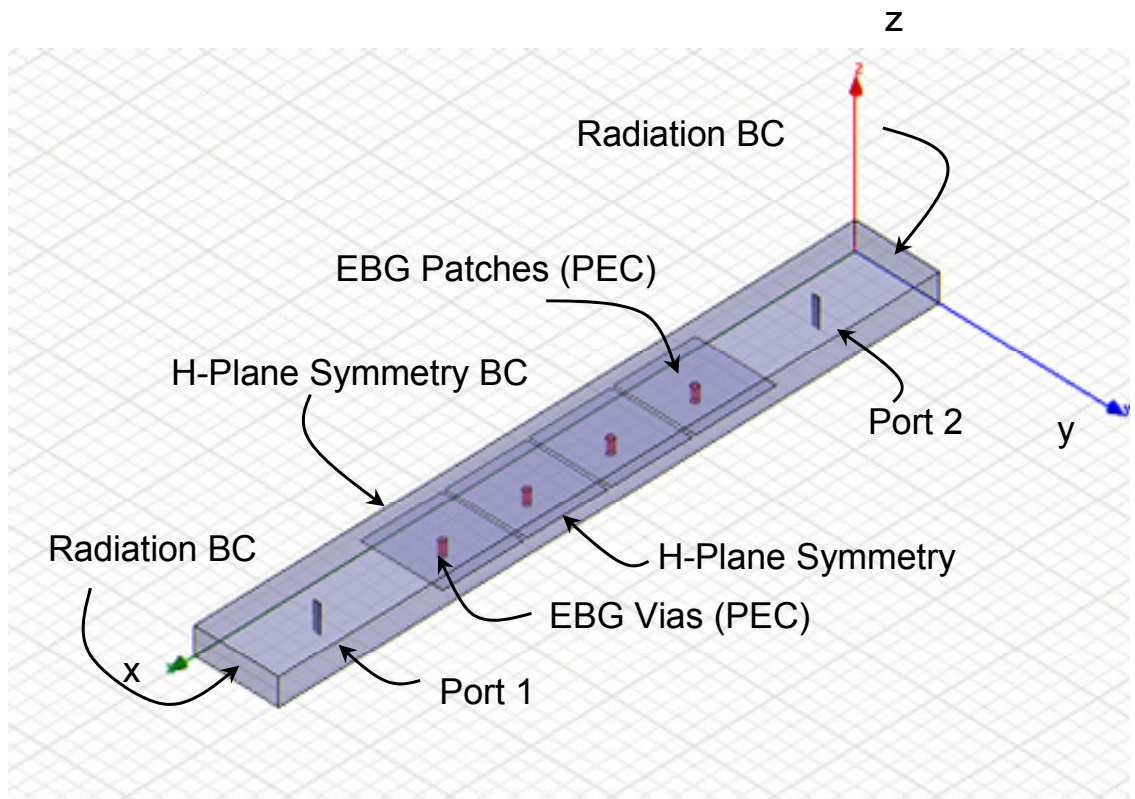


Figure 2-9 Diagram representing the simulation model used to derive the bandgap of an EEBG structure by extracting S-parameter. The computational domain includes a single cell. H-plane symmetry Boundary Conditions (BC) are placed in the x-z plane on the two sides of the structure to resemble an infinite structure in the y direction. The top and bottom planes of the cell are perfect electric conductors (PEC).

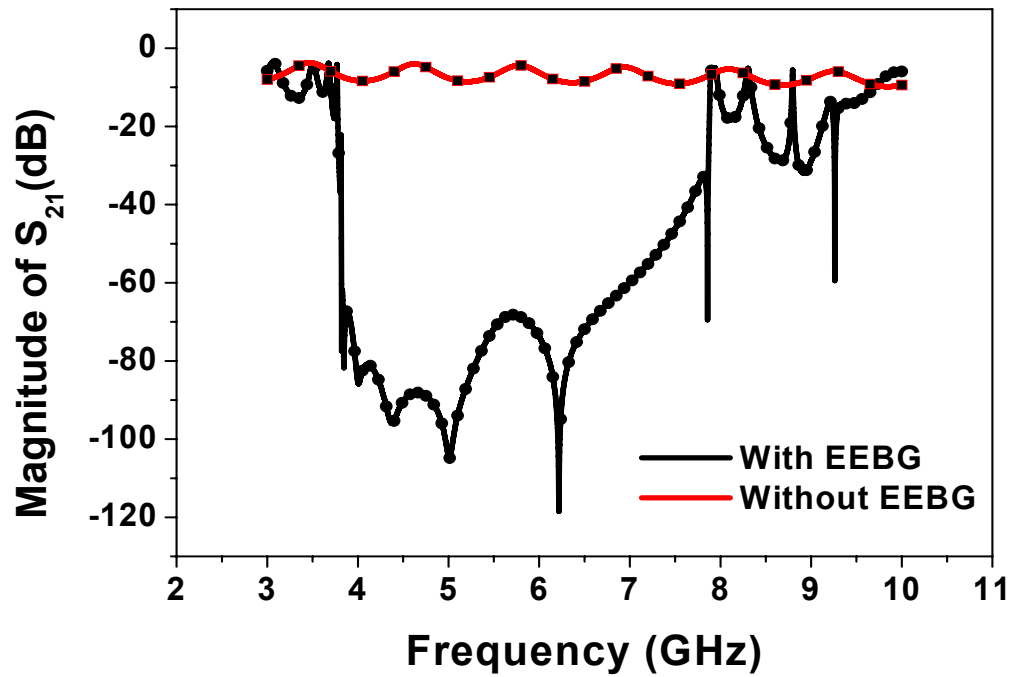


Figure 2-10 Typical result of double-symmetric simulations of the model in Figure 2-9.

2.2.5 Lumped Element Circuit Modeling

2.2.5.1 Simple Physics Based Model

As described throughout previous chapters, for EEBG structures full-wave simulation is the most widespread design method and includes design by using either S-parameter simulations or dispersion diagrams, or both.

Previous works, in their design stages, relied mainly on full-wave simulation or on circuit models originally developed assuming open structures for antenna applications (HIS

over a conductive plane) and normal incident waves. This model is illustrated in Figure 2-11.

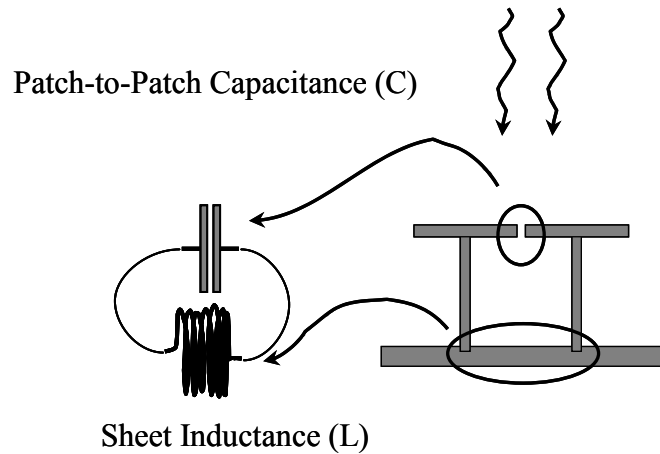


Figure 2-11 Model developed in previous studies for normal incident waves.

Although, full wave simulations are the best and most accurate method to design structures involving EBG structures, they are slow and cannot be easily integrated in iterative design processes, therefore new effective and accurate model needs to be defined. In addition they do not provide a mean to understand the effect of different design parameter on the suppression behavior of the structures.

In the model of Figure 2-11 that was initially introduced by Sievenpiper in [1] waves are normally incident to the HIS plane and therefore the circuit model for the resonance frequency would look like a parallel LC circuit with resonance frequency of:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad 2-2$$

Sievenpiper, in his work, applies these surfaces to low profile antennas. In such applications, HIS surfaces present high impedance within their operating frequency band(s), therefore acting like magnetic conductors and reflecting waves in phase with the incident waves (180° out of phase with a conventional metallic plane) [21]. The bandwidth of such antenna is proportional to:

$$BW \propto \sqrt{\frac{L}{C}} \quad 2-3$$

It should be noted that the bandwidth equation given in equation 2-3 is only applicable to low-profile antenna applications and it cannot be used for other applications such as HIS in PCB's (i.e. EEBG structures whose physics is more similar to a Low Impedance Surface (LIS) rather than a HIS).

Previous studies suggest modifications to the circuit model as they relate its error to the error of the available equations for the two components of the model [14]-[15]. These modifications include:

- Replacing the approximation for the capacitor with a better approximation value computed numerically by the method of moments.
- Modify the previous adjustment by adding the induction of the vias to the total inductance.

In order to evaluate these models, various LIS structures were analyzed using HFSS. The simulated structures were fabricated and tested to validate the simulation results. The results of the basic model are compared to results from the two suggested modified models. As the result of this analysis, no improvement in the accuracy of the predicting capabilities of the initial model (in order to predict the resonant frequency of the structure) was noticed.

This is mainly because the model (as a physics-based model) has not been developed for the physical phenomenon and wave propagation mechanism associated with parallel-plate structures.

In such structures, electromagnetic waves propagate in a radial fashion, therefore the incident waves are in the plane of the patches as illustrated in Figure 2-12, rather than being normal to the HIS structure.

Since, available circuit models are not applicable to the case of LIS structures and a new model needs to be introduced. To this end, the model in Figure 2-12 is presented.

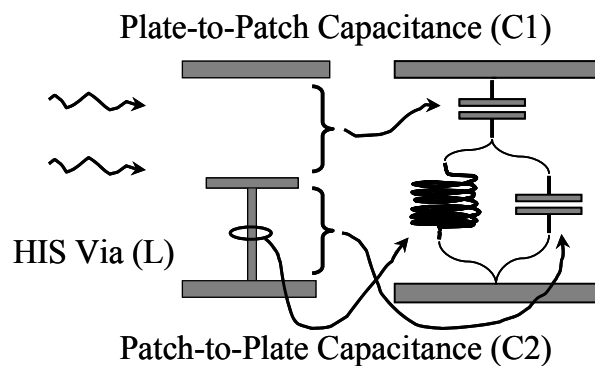


Figure 2-12 Proposed model developed for waves propagating in a plane parallel to the power bus and containing the patches of the EEBG structure.

The resonance frequency of the structure shown in Figure 2-12 is the transfer zero of the circuit. In fact, each unit cell provides high-frequency low-path impedance between the parallel-plates at this resonance frequency:

$$f_{res} = \frac{1}{2\pi\sqrt{L(C_1 + C_2)}} \quad 2-4$$

In this equation, capacitor C_1 denotes the capacitance between the metallic patch and the region of the top plate corresponding to such patch, inductor L is the inductance of the via and capacitor C_2 is the capacitance between the patch and the region of the bottom plate corresponding to the patch. Comparison of results from this model and full-wave analysis results shows the preciseness of the model in predicting the resonant frequency of the structure, provided accurate formulas or numerical approximations are used for the model components, especially the inductor. The effect of fringing capacitance, which is always neglected, is also a source of error.

Furthermore, unit cells when combined together to form a full LIS structure affect each other by shifting their individual resonant frequency, therefore creating a stop-band region [23]. Section 2.2.6.2 quantifies this bandwidth in details.

2.2.5.2 Complex Physics Based Model

Another method commonly used for the design and analysis of EEBG structures is circuit modeling. In this approach the whole structure is replaced by lumped components that reside between different points of the PDN. Two types of physics-based models have been considered so far.

The first type of approach consists of presenting an intuitive circuit that would describe the behavior of the EEBG structure as close as possible and derive the parameters (capacitance, inductance and resistance) of the circuit model by fitting the curves of the transfer function of the circuit model to the response extracted by full-wave finite element simulations of the structure.. The extracted circuit model can then be used to evaluate the performance of the PDN in the presence of other circuit elements such as decoupling capacitors and switching circuits [29]. Therefore the goal of this type of modeling is different than designing EEBG structures.

The second type of approach is aimed mostly at deriving a circuit model that can be used in the design phase of EEBG structures. Values for the components of this model are derived based on lumped element inductances and capacitances of the building blocks of the EEBG structure (e.g. power plane inductance, via inductance, patch to power plane capacitance, etc.) [30].

In order to derive this model, the model developed for EEBG unit cells can be incorporated into a physics-based model for power planes in printed circuit boards. In Figure 2-13, a three dimensional view of an EEBG unit cell is shown. The top and bottom planes represent the power bus and the plane in the middle is the EBG patch, connected to the bottom plane through a via. C_1 , C_2 and L_1 represent the model introduced in the previous section. Each of the capacitors C_3 - C_6 is twice the capacitance between adjacent patches, so that when the unit cell is connected to a neighboring cell the equivalent capacitance would be the capacitance between the two patches. This capacitance can be calculated using an approximate equation given in [21] assuming that the effective length

of the patch is equal to the gap size. This is due to the presence of the top plate. Inductors L_3 - L_6 are sheet inductances of half of the portion of the top plate located on the top of the patch. Therefore

$$C_{3-6} = \frac{2a\epsilon_r\epsilon_0}{\pi} \cosh^{-1}(3) \quad 2-5$$

$$L_{3-6} = \frac{\mu_0}{2} a \quad 2-6$$

In which a is the patch lateral size and ϵ_r is the dielectric constant of the material in between the power planes.

In order to validate this model, several cells of the compact 3D model are cascaded in a 2D fashion to build a model for the full power plane. Component values are derived by analytical and approximate equations. The result of simulating this circuit is then compared to full-wave simulations done using HFSS and measurement on a fabricated PCB with EEBG structure. Figure 2-14 illustrates such comparison for a structure with via length $h_2 = 1.54$ mm, board thickness minus via length $h_2 = 1.54$ mm, patch lateral size $a = 10$ mm, substrate material $\epsilon_r = 4.1$, gap size between patches $g = 0.4$ mm, via diameter $\nu d = 0.8$ mm.

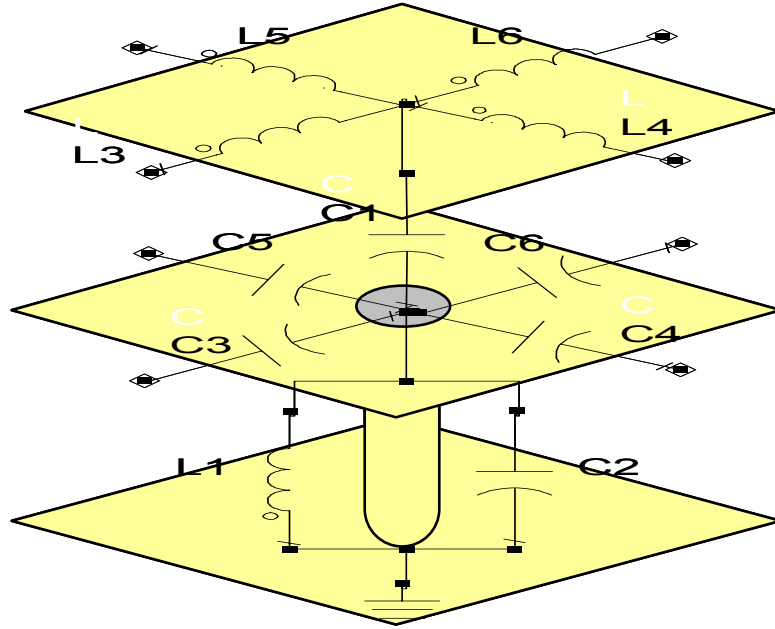


Figure 2-13 EEBG unit cell model merged with a conventional low frequency power bus circuit model. A 2D array of these cells represents the whole power bus.

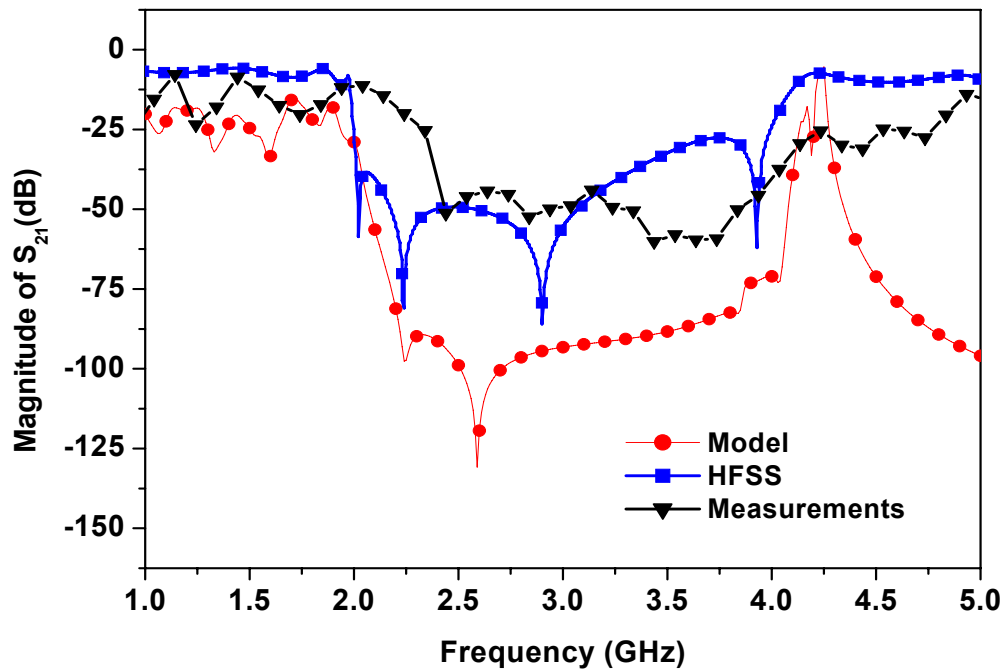


Figure 2-14 Comparison of the model shown in Figure 2-13, simulations using HFSS and experimental measurements.

A good agreement between simulation, experiments and results from the model show the high degree of reliability of the model to predict the gap of the structure.

It should be noted that, since the model used for the power bus is inherently a low-pass model, the resulting 3D compact model inherits this limitation and it is only valid in the range from DC to 4 GHz. Furthermore, the model for the unit cell presented in the previous section is not limited to this frequency range and it is able to have good predictions at far higher frequencies.

2.2.6 Periodically Loaded Transmission Line Modeling

2.2.6.1 Electromagnetic Wave Propagation in an Infinite Parallel-plate Structure Filled with Two Different Material

In order to derive a transmission line based model for EEBG structures a generic inhomogeneous-filled parallel-plate transmission line is considered. A thorough and detailed analysis of such structure is given in [32].

In other words, an EEBG structure can be modeled as a periodically loaded homogeneously or inhomogeneously-filled parallel-plate transmission line. The unit cell of this periodic structure is made of one single patch-via and a squared portion of the parallel-plate structure with lateral size of the patch size plus the size of the gap between patches (i.e. period of the structure), as shown in Figure 2-15.

2.2.6.2 Analysis of EEBG Structures Using Transmission Line and Periodic Structure Theory (TLPS)

The starting point for the EEBG model presented here is the generic form consisting of identical blocks of transmission lines, cascaded in a linear fashion, as shown in Figure 2-15. This generic form was first reported in [31] but for a different application (e.g. modeling high-impedance surfaces in the presence of surface waves). By studying the effect of cascading few unit cells, the propagation characteristics of the waves within the structure can be derived. In this model, each unit cell of the EEBG structure consists of a transmission line of length d with shunt admittance across the midpoint of the line, as shown in Figure 2-15.

The ABCD parameters of this unit cell are given by:

$$\begin{bmatrix} A & B \\ C & D \end{bmatrix} = \begin{bmatrix} \cos\left(\frac{\beta l}{2}\right) & jZ_w \sin\left(\frac{\beta l}{2}\right) \\ jY_w \sin\left(\frac{\beta l}{2}\right) & \cos\left(\frac{\beta l}{2}\right) \end{bmatrix} \begin{bmatrix} 1 & 0 \\ Y & 1 \end{bmatrix} \begin{bmatrix} \cos\left(\frac{\beta l}{2}\right) & jZ_w \sin\left(\frac{\beta l}{2}\right) \\ jY_w \sin\left(\frac{\beta l}{2}\right) & \cos\left(\frac{\beta l}{2}\right) \end{bmatrix} = \quad 2-7$$

$$\begin{bmatrix} \cos(\beta l) + j\frac{YZ_w}{2} \sin(\beta l) & jZ_w(\sin(\beta l) - j\frac{YZ_w}{2} \cos(\beta l) + j\frac{YZ_w}{2}) \\ jY_w(\sin(\beta l) - j\frac{YZ_w}{2} \cos(\beta l) - j\frac{YZ_w}{2}) & \cos(\beta l) + j\frac{YZ_w}{2} \sin(\beta l) \end{bmatrix}$$

In which Z_w and Y_w are the impedance and admittance of the propagating wave in an unloaded transmission line respectively, and β is the wave number of such wave.

The behavior of the EEBG structure at different frequencies can be estimated by multiplying the matrix derived in equation 2-7 by itself as many times as unit cells under consideration, and then plotting the absolute value of S_{21} given by,

$$S_{21} = \frac{2}{A_T + B_T Y_w + C_T Z_w + D_T} \quad 2-8$$

In which,

$$\begin{bmatrix} A_T & B_T \\ C_T & D_T \end{bmatrix} = \begin{bmatrix} A_1 & B_1 \\ C_1 & D_1 \end{bmatrix} \cdots \begin{bmatrix} A_n & B_n \\ C_n & D_n \end{bmatrix} \quad 2-9$$

At this point, parameters on the right hand side of equation 2-7 need to be defined. Part of the solution requires solving Maxwell's equations for a parallel-plate waveguide filled with two (possibly different) dielectric materials (i.e., making two different layers parallel to the power planes). Solution to Maxwell's equations in the described parallel-plate structure can be found in [32] and explained in section 2.2.6.1. The dominant mode is characterized as a TM mode (quasi-TEM). For a low frequency approximation, the wave impedance and the wave number are,

$$Z_w = \frac{\eta_0}{d} \sqrt{(h_1 + h_2) \left(\frac{h_1}{\epsilon_{r1}} + \frac{h_2}{\epsilon_{r2}} \right)} \quad 2-10$$

$$\beta = \frac{\omega}{c} \sqrt{(h_1 + h_2) \left(\frac{h_1}{\epsilon_{r1}} + \frac{h_2}{\epsilon_{r2}} \right)} \quad 2-11$$

Where c is the speed of light, ω is the operating frequency and η_0 is the free space wave impedance. The low frequency approximation is reasonable since the thickness of the EEBG structures under consideration is usually in the order of few hundred micrometers.

The second and final part of the solution is a lumped element model for the admittance Y as shown in Figure 2-15 (b) and (c). This model is inspired by the physical behavior of the fields in the patch. The admittance, Y , of the LC structure is given by

$$Y = \frac{j\omega C_1(1 - L_1 C_2 \omega^2)}{(1 - L_1(C_1 + C_2)\omega^2)} \quad 2-12$$

Where C_1 and C_2 are the parallel-plate to patch capacitances and L_1 is the inductance of the via. L_1 can be either calculated through numerical simulations or through approximate equations, such as in [33].

The frequency at which 2-12 becomes infinite, is the frequency of minimum propagation. This effect is equivalent to shorting the power planes, hence a series resonant effect. In addition, dispersion of waves with frequencies around the resonance frequency creates the bandgap of the structures. This model is also in accordance with a quasi-TEM assumption for the propagating waves [32]

Assuming that the structure is infinitely long or perfectly matched at the end (hence no reflections), invoking Floquet's theorem [34] for the n^{th} cell of the structure,

$$\begin{bmatrix} V_n \\ I_n \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} \quad 2-13$$

$$\begin{bmatrix} V_{n+1} \\ I_{n+1} \end{bmatrix} = e^{-\gamma d} \begin{bmatrix} V_n \\ I_n \end{bmatrix}, \quad (\gamma = \alpha_n + j\beta_n) \quad 2-14$$

After combining equation 2-13, equation 2-14 and equation 2-7, in order to have a feasible solution for the voltages and current along the structure,

$$\begin{vmatrix} A - e^{\gamma d} & B \\ C & A - e^{\gamma d} \end{vmatrix} = 0 \quad 2-15$$

Knowing that $\alpha_1 = \dots = \alpha_n$ and $\beta_1 = \dots = \beta_n$, (8) simplifies into,

$$\begin{aligned} \cosh(\alpha_1 d) \cos(\beta_1 d) + j \sinh(\alpha_1 d) \sin(\beta_1 d) \\ = \cos(\beta d) + j \frac{YZ_w}{2} \sin(\beta d) \end{aligned} \quad 2-16$$

All the parameters of equation 2-16 are defined in equations 2-10, 2-11 and 2-12. Notice that the right hand side of 2-16 is purely real, hence there are two possible solutions. The first solution is when $\alpha_1 = 0$. This case corresponds to propagating waves in the structure and defines the pass-band region of the structure. Hence equation 2-16 reduces to,

$$\cos(\beta_1 d) = \cos(\beta d) + j \frac{YZ_w}{2} \sin(\beta d) \quad 2-17$$

By plotting $\beta_1 d$ derived from equation 2-17 versus frequency, a first order dispersion diagram for the periodic structure can be derived.

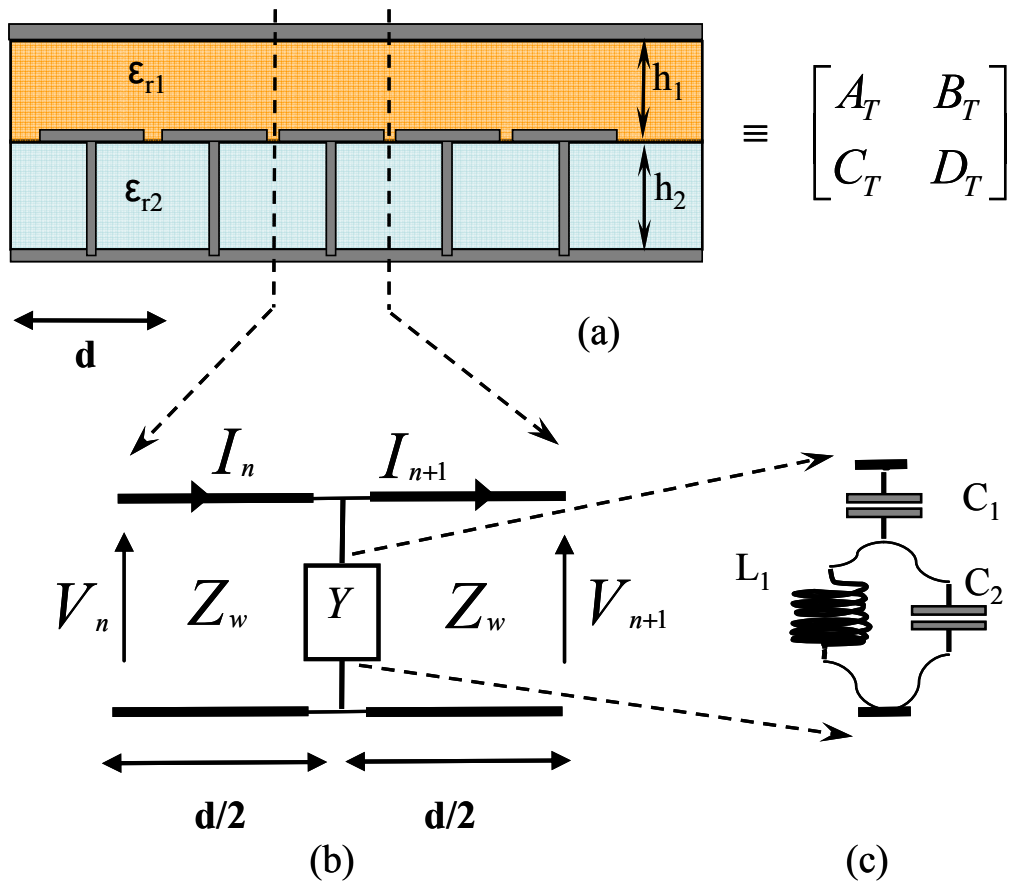


Figure 2-15 Lateral view of an EEBG structure. Each unit cell consists of a transmission line of length d with shunt admittance across the midpoint of the line. The admittance is a lumped element equivalent for the patch-via structure assuming square-patched EEBG structures.

The second solution occurs when $\alpha_l \neq 0$ and $\beta_l = 0$ or π . In this case waves do not propagate and they are attenuated along the structure defining the stop-band region of the structure. Since the transmission line is assumed to be lossless, power is not dissipated, but reflected back into the input of the line (S_{11} is 0 dB). In this type of solution, equation 2-16 needs to

be solved directly, resulting in a real and positive value for γ . Due to this real and positive γ , all the wave modes in the structure become evanescent, resulting in no propagation. The existence of this type of solution for equation 2-16 is the reason for the existence of the bandgaps in EEBG structures.

To validate the TLPS model, bandgaps predicted with the model are compared to finite element (FE) based analysis with various sizes and dielectric materials performed on EEBG structures.

Entry number	d (mm)	h ₁ (mm)	h ₂ (mm)	ϵ_{r1}	V _d (μm)	FE Gap (GHz)	Model Gap (GHz)
1	10.4	1.54	1.54	4.1	800	2.1- 4.0	2.5-4.0
2	10.4	1.54	1.54	8.2	800	1.6-3.7	1.8-3.7
3	10.4	1.54	1.54	12.3	800	1.3-3.1	1.5-3.5
4	10.4	1.54	1.54	16.4	800	1.2-2.9	1.3-3.4
5	2.2	0.016	0.1	30	125	2.3-13.2	2.3-13.5
6	2.2	0.016	0.1	4.1	125	6.0-18.1	6-14.7
7	5.2	0.016	0.1	4.1	125	2.2-6.5	2.2-4.82
8	5.2	0.016	0.1	16.4	125	1.1-6.4	1.1-4.45

Table 2-1 Comparison of periodically loaded transmission line model and Finite Element (FE) simulations: For all table entries ϵ_{r2} is equal to 4.1. Vd is the diameter of the vias of the EEBG cells. In both FE simulations and in the model four cascaded single cells have been considered.

Minor discrepancies between FE simulations and the results of the TLPS model are introduced by the fact that FE simulations, unlike the TLPS model, do not assume zero reflection as the ports defined in the FE model are terminated into 50Ω loads. Also the

TLPS model, unlike previous models such as in [9], does not include parasitic components such as changes in capacitances due to fringing fields, lateral patch-to-patch capacitances and the effect of the via on C_2 . The presence of parasitic components (capacitors and inductors) in the parallel-plate structure is equivalent to the presence of higher propagating modes (including TE, TM, hybrid, surface modes and evanescent). In order to further increase accuracy, the TLPS model may be refined with parasitic components, at the cost of increased complexity [36].

Figure 2-16 shows a sample result of calculations derived by calculating equation 2-17 using MatlabTM. According to Table 2-1, the minimum pass-band frequency and maximum stop-band frequency defined by a -20 dB criteria is 2.3 GHz to 13.5 GHz which are very close to the calculated 2.3 GHz to 13.2 GHz derived by FE simulations.

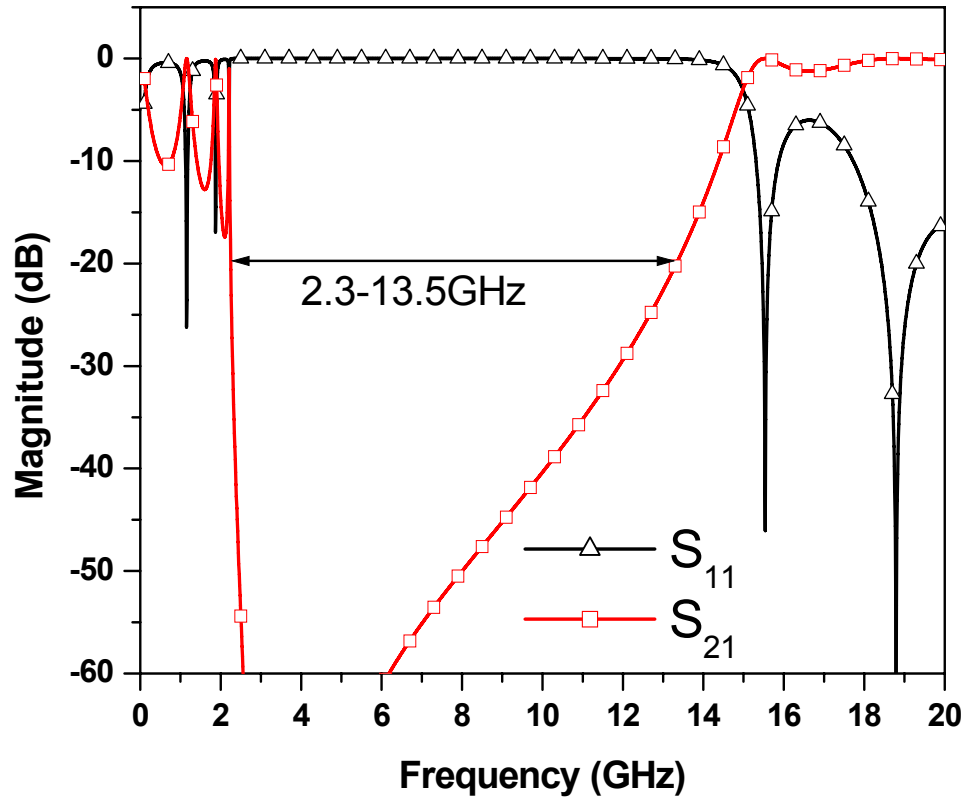


Figure 2-16 Scattering parameters for entry 5 of Table 2-1. The magnitude of S_{21} and S_{11} characterize the amount of power that propagates through the structure and the power that reflects back into the source respectively.

2.3 Implementation of EEBG Structures, Experiments and Results

2.3.1 Plain Structures

Using the direct experimentation technique described in section 2.2.1 various EEBG structures have been studied during early stages of this work. Fully populated

boards as shown in Figure 2-17 and a limited number of rows as shown in Figure 2-18 have been tested using the setups shown in Figure 2-3 and Figure 2-4.

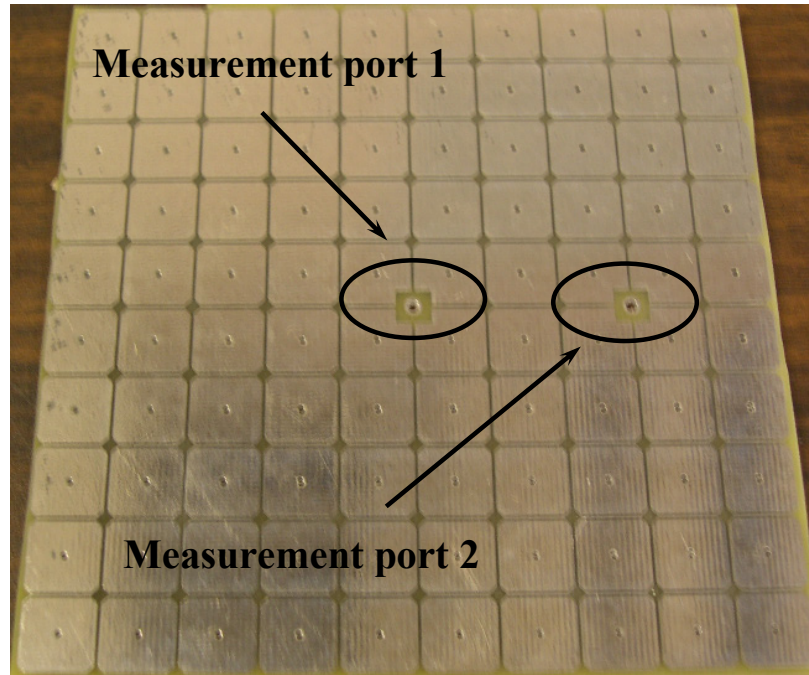


Figure 2-17 Mid-layer of a fully populated structure. Board size is 10 cm x 10 cm, patch size is 10 mm x 10 mm, $Vd = 0.8$ mm, $h_1 = h_2 = 1.54$ mm, $g = 0.4$ mm, $\epsilon_{r1} = \epsilon_{r2} = 4.1$.

Tests on fully populated boards are performed using a setup similar to the one shown in Figure 2-19. Result from experiments on the structure shown in Figure 2-18 are tabulated in Table 2-2. These experiments marked the end of early development of EEBG structures [37].

Patch Size	-20 dB Gap	
	Lower edge	Higher edge
2 mm	9 GHz	NA
3 mm	7.4 GHz	NA
5 mm	4.23 GHz	11 GHz
6 mm	3.93 GHz	8.2 GHz
10 mm	2.24 GHz	4.83 GHz
20 mm	0.8 GHz	1.2 GHz

Table 2-2 Results from experiments on sample EEBG structures shown in Figure 2-18. For 2 and 3 mm patches the attenuation of FR4 at the higher edge is more than 20 dB, therefore the gap never reaches the -20 dB line.

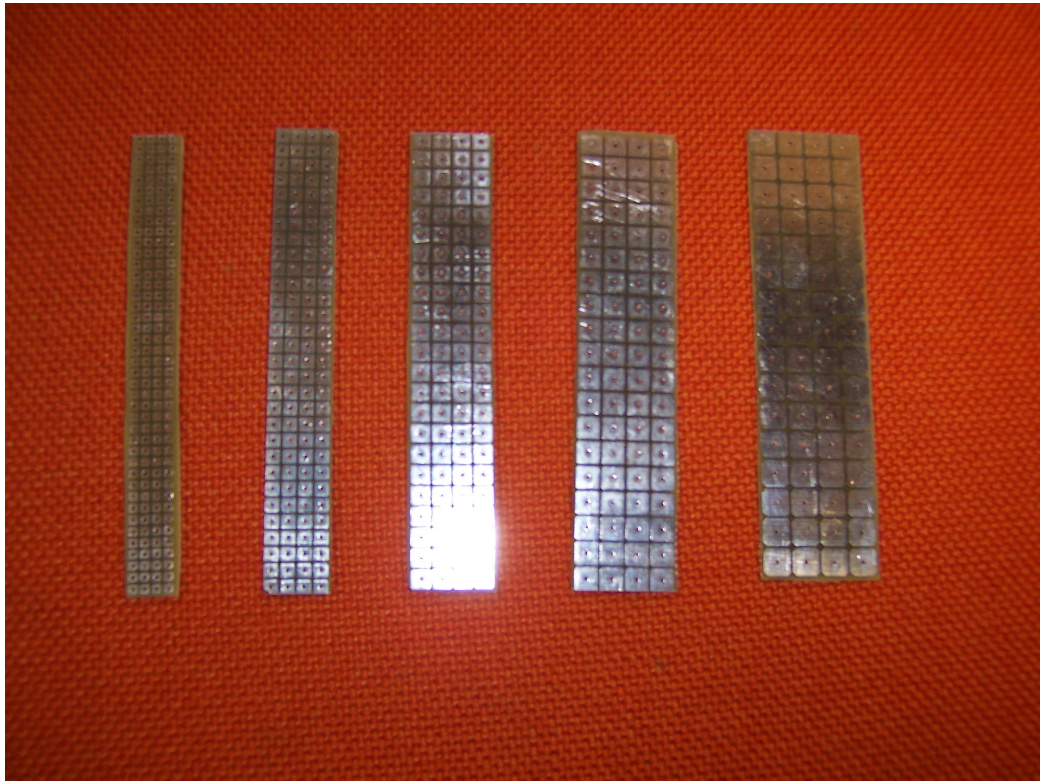


Figure 2-18 Implementation of EEBG structures with patch sizes of (from left to right) 2 mm x 2 mm, 3 mm x 3 mm, 5 mm x 5 mm, 6 mm x 6 mm and 10 mm x 10 mm. $Vd = 0.8$ mm, $h_1 = h_2 = 1.54$ mm, $g = 0.4$ mm, $\epsilon_{r1} = \epsilon_{r2} = 4.1$.

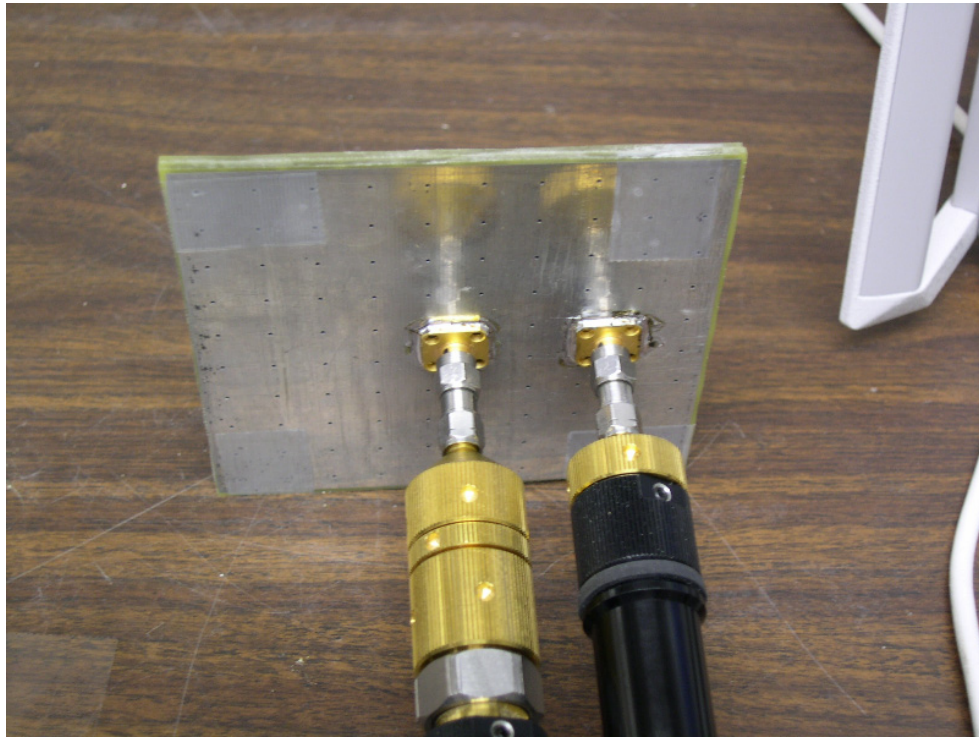


Figure 2-19 S-parameter measurement of a fully populated structure as shown in Figure 2-17.

2.3.2 Exotic Structures

As mentioned in section 2.2.5.1 initial development of EEBG structures were inspired by HIS structures, hence it was assumed that their bandwidth is proportional to the inductance of the patch-via structure (equations 2-2 and 2-3). With this concept in mind early designs such as the inductively tuned structures [37] were developed.

This family of design which includes designs such as the one shown in Figure 2-20 and Figure 2-21 aims at increasing the inductance of the patch via structure while affecting its capacitance minimally. The designs of Figure 2-20 and Figure 2-21 accomplish this goal in two layers while the inductively tuned design needs an additional layer for the inductor.

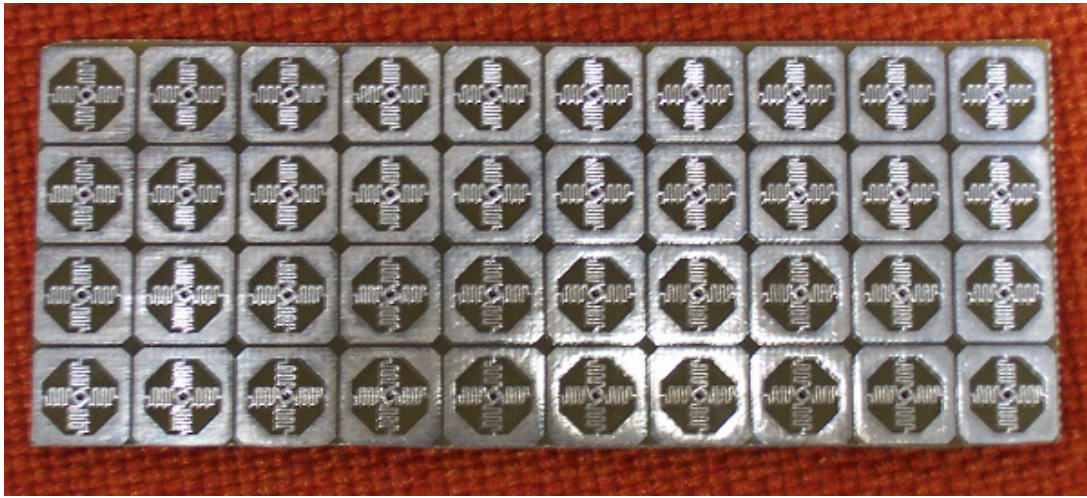


Figure 2-20 A sample design used to increase the inductance of a single cell of the structure by sacrificing some capacitance to study the overall effect.

Results from experiments using this family of structures, as shown in Figure 2-22, show that the increased inductance causes a downward shift in the frequencies of the bandstop region but affects the bandwidth minimally. This is due to the fact that equation 2-3 is indeed not applicable to EEBG structures. Instead more detailed and accurate models such as the models derived in section 2.2.6.2 need to be employed.

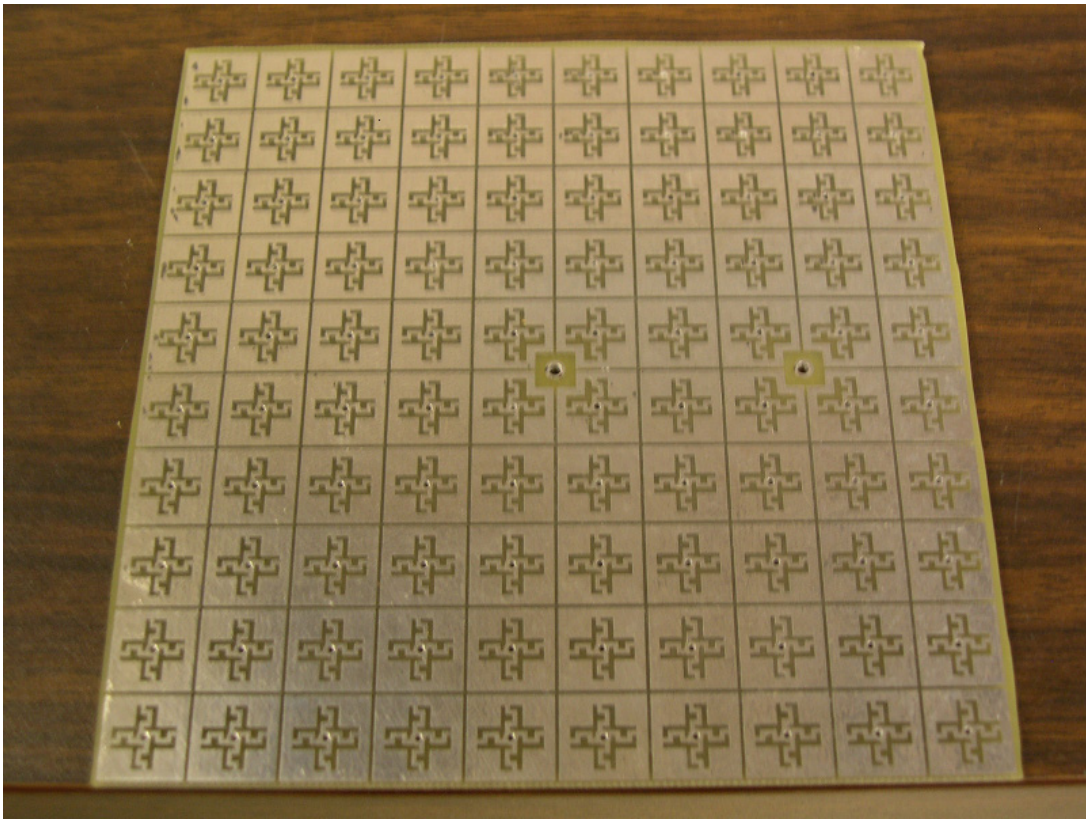


Figure 2-21 Another sample design used to increase the inductance of a single cell of the structure by sacrificing some capacitance to study the overall effect.

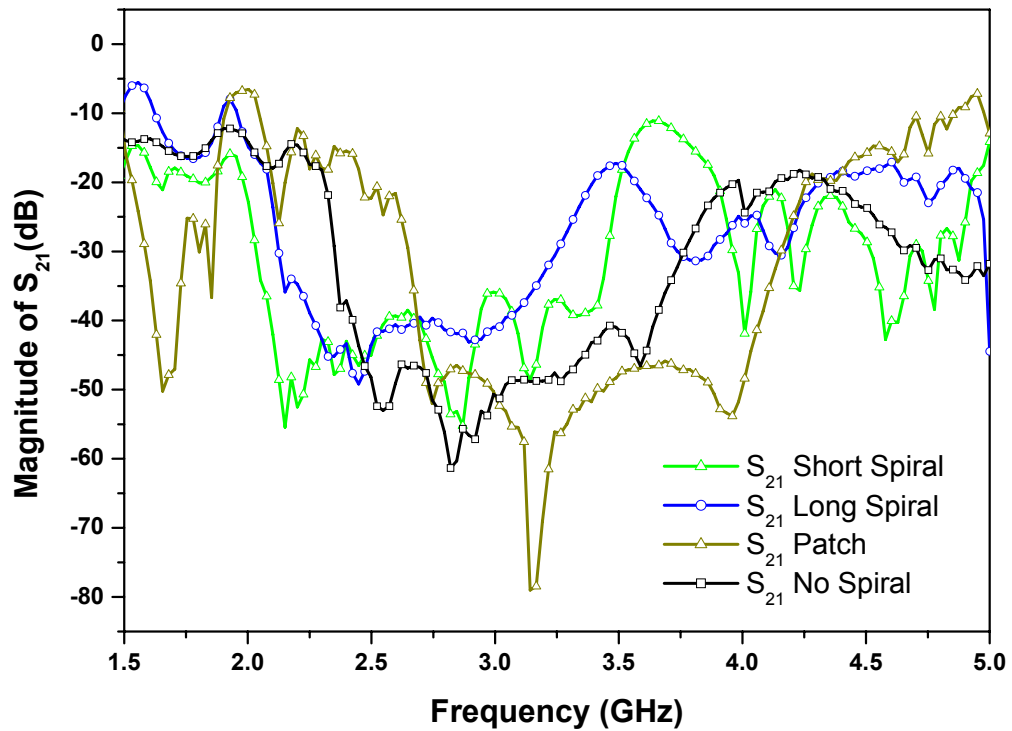


Figure 2-22 Results from experiments using exotic structures.

2.3.3 Design Considerations

Figure 2-23 shows a lateral cut of a typical multilayer PCB with three possible types of vias, buried blind and thru hole. A classical EEBG structure would require employment of blinded or buried vias which are more expensive to fabricate than through hole vias and in certain cases would also require a different fabrication technology than simple through hole vias.

The purpose of this part of the work is to replace the blinded or buried vias with thru hole vias and study how this change affects the stop-band of the designed bandgap structure. Figure 2-24 shows a modified version of the diagram of Figure 2-23 with vias extended to the outmost layers, therefore replacing the buried vias with thru hole vias. To avoid electrically shorting the power planes, the area around the EBG-vias on other layers is etched.

The structures of Figure 2-24 and Figure 2-25 were simulated using HFSS and the plot in Figure 2-26 shows the scattering parameters (S_{21} as a representative of transmitted power) between two ports located on two sides of such structures and connected between the power bus plates.

These plots clearly show that when the vias are extended through the PCB, there is only a minor and negligible difference in the suppressive behavior of the EEBG structure discussed so far. In summary, extending the vias of EEBG structures provides a cheap alternative for vias currently employed in the fabrication of a EEBG structures in parallel-plate environments.

On another front, practical multilayer PCBs have different thicknesses based on the amount of layers involved in their fabrication. An EEBG structure designed for a given layer-to-layer distance, may behave differently when the number of layers in use and therefore the thickness of the board changes. In addition, PCBs fabricated for past studies on high-impedance surfaces are beyond the practical range for layer-to-layer distance of the power-bus layers. In this part of the study, a specific designed EEBG structure located between two parallel-plates was simulated while the distance between these plates changes.

Figure 2-27 shows the simulation results. These plots demonstrate that by shrinking the thickness of the board, the center frequency of the bandgap does not change dramatically, but the band-stop region decreases. This is because the distance between the patches has not been reduced accordingly during simulation steps. Figure 2-28 illustrates how by decreasing this distance, the decrease in bandwidth due to the shrinking process can be compensated. To this end, other design parameters, such as the diameter of vias can also be used.

In summary, the effect of board thickness variation on the behavior of EEBG structures is minimal, hence extending already available design methodologies to practical applications.

By extending the vias to the other metallic power plane, and etching the area around it to avoid shorting the two planes (hence creating an anti-pad), EEBG structures can be implemented using cheap PCB technologies that support only through hole vias. Full-wave simulations using commercial finite-element by Ansoft Co. (HFSS) show that extending the vias used in an EEBG structure neither affects their band-stop behavior nor alters the properties of the designed bandgap. Shrinking the thickness of PCBs employing EBG structures reduces its bandwidth, but this collateral effect can be compensated by modifying other EEBG design parameters, such as the distance between EBG-patches or the via diameter, therefore achieving the same bandstop properties. Shrinking and via extension, provide a framework that makes the implementation of a EEBG structures in parallel-plate environments compliant with practical and cheap PCB technologies.

In fact, after this technique was first introduced by this work another research group successfully implemented this technique in a commercial prototype [38].

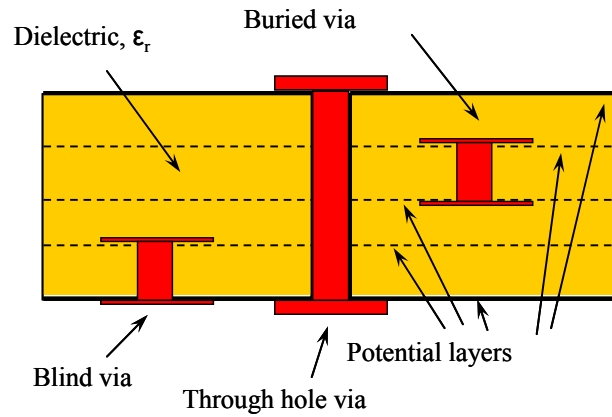


Figure 2-23 Diagram of the cross section through a 5-layer multilayer PCB produced by sequential lamination.

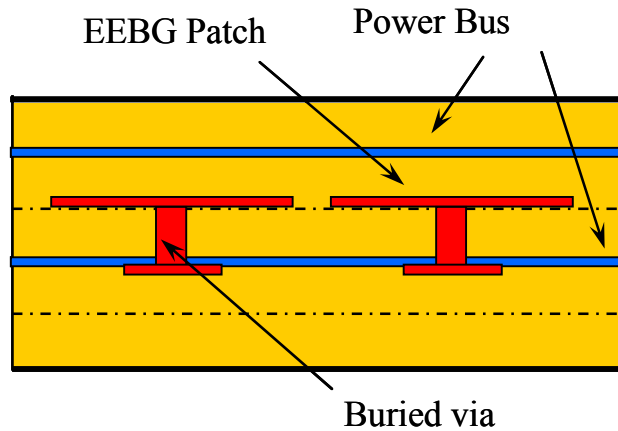


Figure 2-24 Lateral view of a multilayer PCB that uses an EEBG structure in between its power planes showing buried vias.

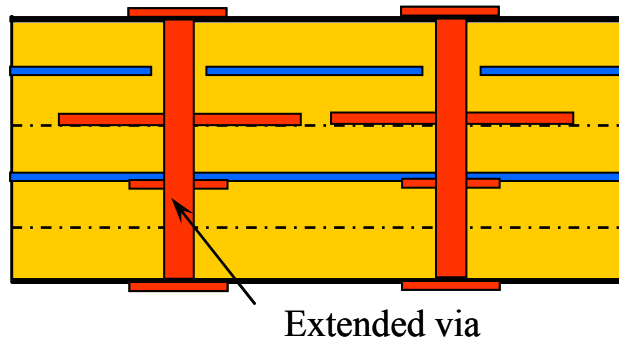


Figure 2-25 Lateral view of a multilayer PCB that uses an EEBG structure in between its power planes showing extended vias.

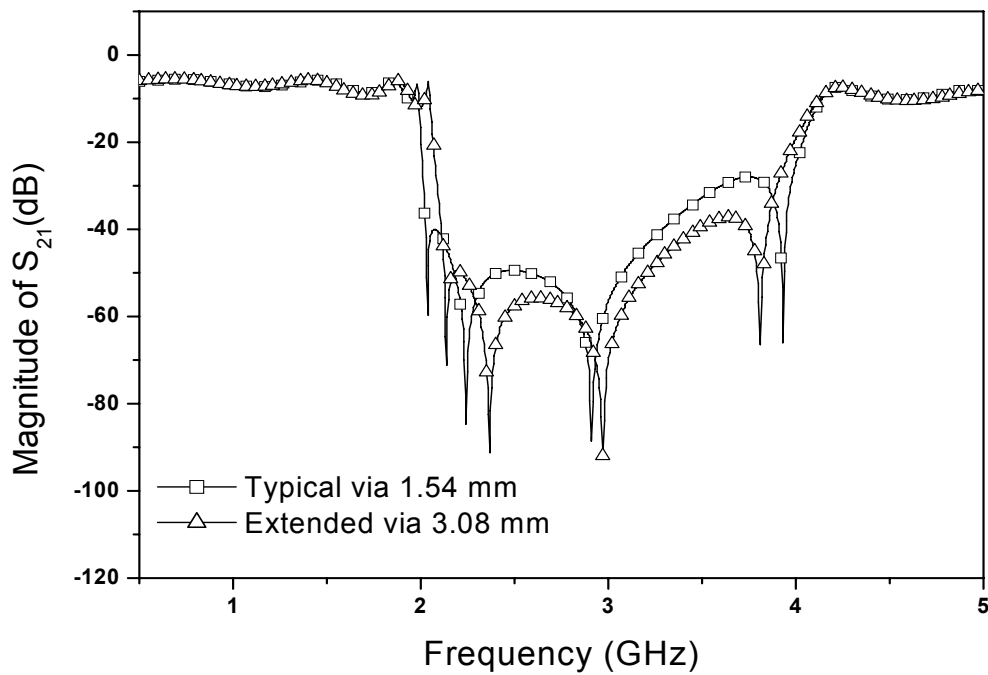


Figure 2-26 Effect of via height, h_2 , on the gap of an EEBG structure. The simulated structure has $a = 10$ mm, $g = 0.4$ mm, $Vd = 0.8$ mm, and $h_1 + h_2 = 3.08$ mm.

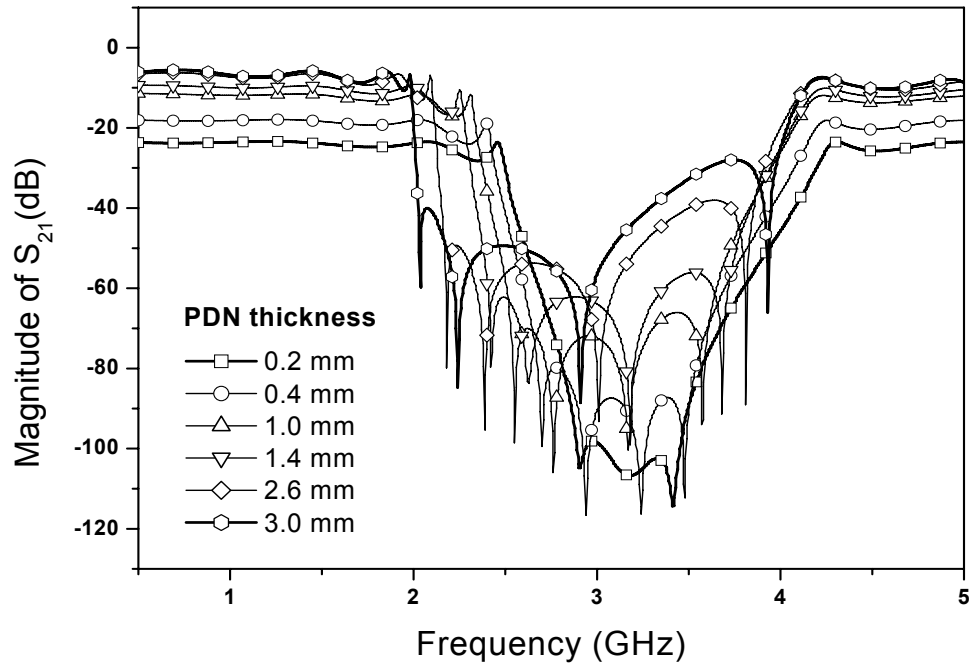


Figure 2-27 Effect of board thickness, $h_1 + h_2$, on the band-gap of an EEBG structure.

The simulated structure has $a = 10$ mm, $g = 0.4$ mm, $h_2 = (h_1 + h_2)/2$, and $Vd = 0.8$ mm.

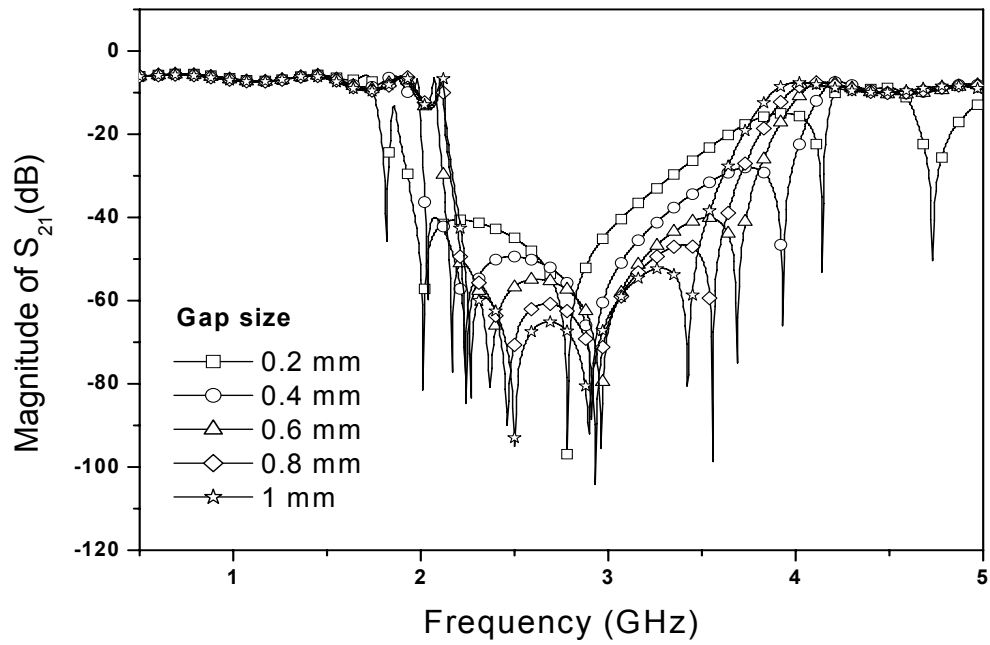


Figure 2-28 Effect of the size of the gap between patches, g , on the band-gap of an EEBG structure. The simulated structure has $a = 10$ mm, $Vd = 0.8$ mm, $h_1 + h_2 = 3.08$ mm, and $h_2 = 1.54$ mm.

Chapter 3. Ultra-wideband Noise Mitigation Using Cascaded EEBG Structures

3.1 Design Concept

Based on filter theory and the fact that EEBG structures behave like band-stop filters, it is expected that if several different designs of EEBG structures were cascaded, the overall effect would be a filter with a stop-band equivalent to the superposition of the original individual filters. Each stage of the filter is composed of an independent periodic structure. Figure 3-1 shows a diagram that illustrates this concept. In this study, as EEBG structures, the simplest structure that was originally proposed in [14] is used, which consists of a rectangular patch with a via post positioned in its center. On the left of the diagram of Figure 3-1 a switching Integrated Circuit (IC) generates noise and on the right of the diagram a second IC is a victim. If the source IC generates noise within the stop-band of the first EEBG structure (type 1), the noise is suppressed before arriving to the second structure. Likewise, if the noise frequency is within the stop-band of the second

structure (type 2), it is suppressed by the second structure. The overall effect is an EEBG structure with a band-stop region composed by the union of the two gaps. As a result, the overall band-stop region increases dramatically.

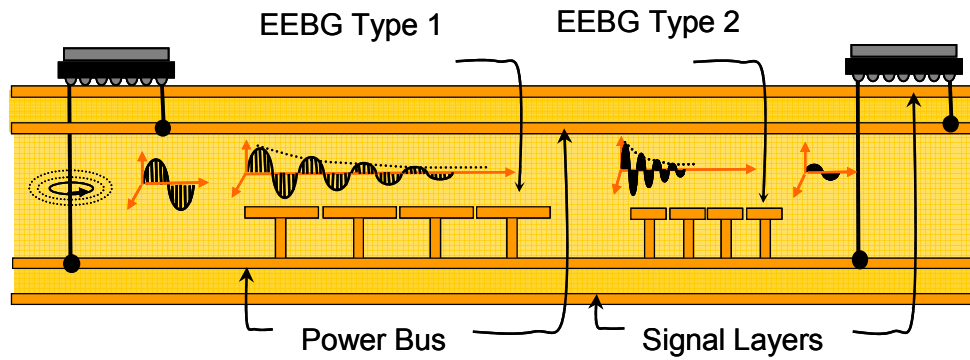


Figure 3-1 Lateral view of a multi-layer PCB with two designs of EEBG structures embedded in between a pair of power planes.

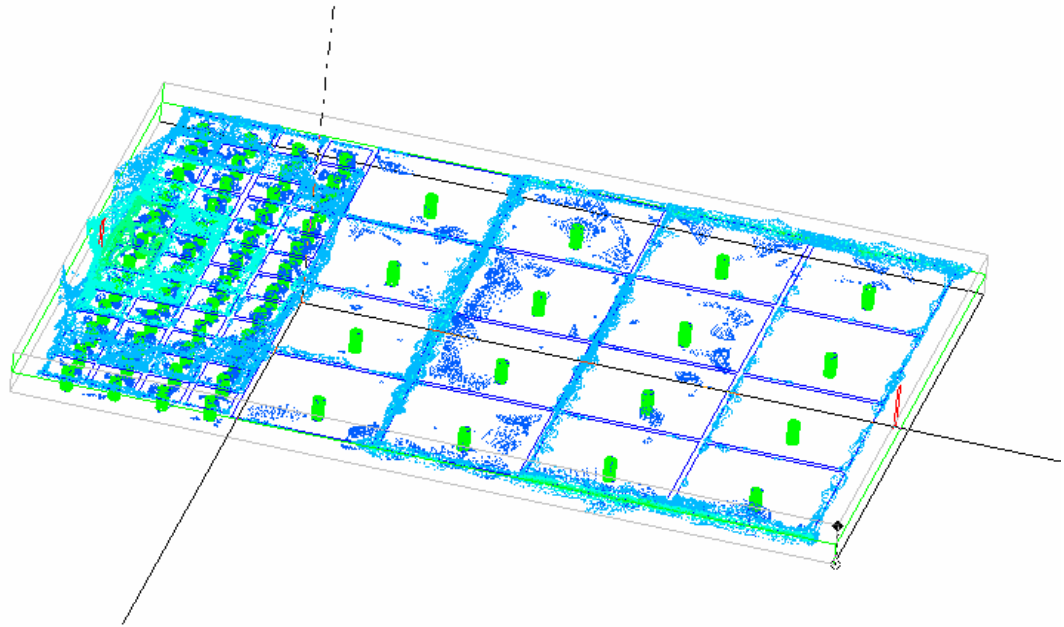


Figure 3-2 FE simulation of two cascaded structures. The excitation port is on the left of the structure and the frequency of excitation is in the stop-band of the structure on the right. The clouds represent the magnitude of the electric field which is strong in the first region (left) as expected.

3.2 Implementation, Measurements and Results

Approximate models were primarily used to have an initial estimate of the location of the bandgap. Full wave numerical simulations were used to validate the design before fabrication. Three structures were designed. Board thickness, board material, via and also gap sizes were kept constant among different structures. The only variable was patch size. Patches of 5 mm, 10 mm and 20 mm were considered.

After initial design using the simplified model, the cascaded structure was implemented with commercial PCB technology on FR4 laminates as a two-layer board. Figure 3-7 shows the fabricated two layer structure in details. A separate one layer boards was mounted to the top of the initial two layer board as a second power plane. Finally the whole structure is pressed to remove any air gaps between the boards. The overall dimension of the PCB was 10 cm x 30 cm. A top view of a schematic of the middle layer is shown in Figure 3-4, where each EBG section and the SMA connector locations are clearly indicated.

Figure 3-5 shows the experimental results from the fabricated boards. The three designed bandgaps are located at 0.8-1.8 GHz, 2.2-4.2 GHz and 4.5-10 GHz. They have been designed without overlap to show the flexibility of the superposition effect. Of course the design parameters can also be modified such that the suppression bands overlap, expanding the suppression region from 800 MHz to 10 GHz.

In summary, this chapter presents a novel design concept to mitigate simultaneous switching noise in printed circuit boards. This technique consists of cascading different configurations of EEBG structure with different stop bands, creating rejection over a wider frequency region. To demonstrate the validity of the proposed design, a prototype was fabricated and tested that consisted of three different EEBG designs (equivalent to three different stop band filters). Experimental measurements yielded highly satisfactory results confirming that the proposed technique can lead to significant SSN suppression over an ultra wide bandwidth. This bandwidth includes the dominant noise frequency and its subsequent harmonics [35].

In addition, cascading can be performed in series as demonstrated in this work, or in a variety of other arrangements such as concentric islands, where each island is a different EEBG with its unique stop band. Figure 3-7 shows this concept. In this design, three types of design have been arranged in a sketch board fashion. Results of this experiment were very similar to results of Figure 3-5, hence not reproduced here. Specifically, measurements from port 1 to port 2 of the structure in Figure 3-7 results in gap 1 and gap 2 of Figure 3-5. Measurement from port 2 to port 4 results in gap 1 and 3. Measurement from port 3 to port 4 results in gap 2 and 3. Measurement between ports in the same type of structure (port 1 and 5, port 2 and 6, port 6 and 4) results is single gap structures (gap 2, gap 1 and gap 3 in Figure 3-5 respectively). Figure 3-6 shows the close relationship between gaps in the S_{21} parameter and the low transfer impedance between the two points under measurement.

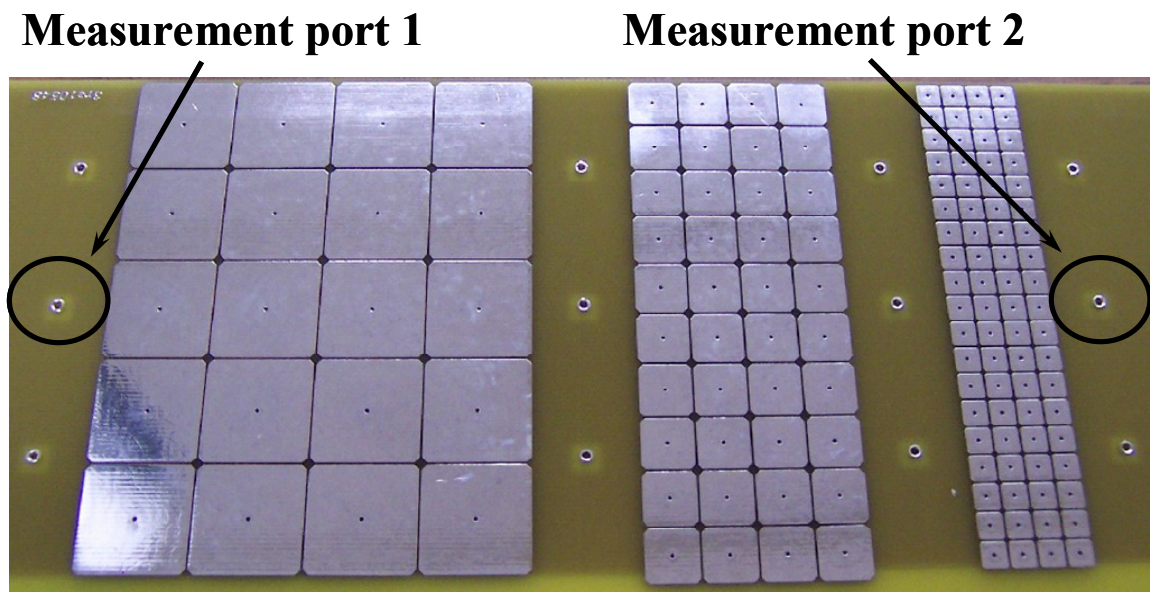


Figure 3-3 Proposed wideband/multiple band structure (gap size = 0.4, via diameter = 0.8 mm, board thickness = 1.54 mm and $\epsilon_r = 4.1$). Top view of the middle layer of the PCB and measurement points. Fabricated cascaded structures.

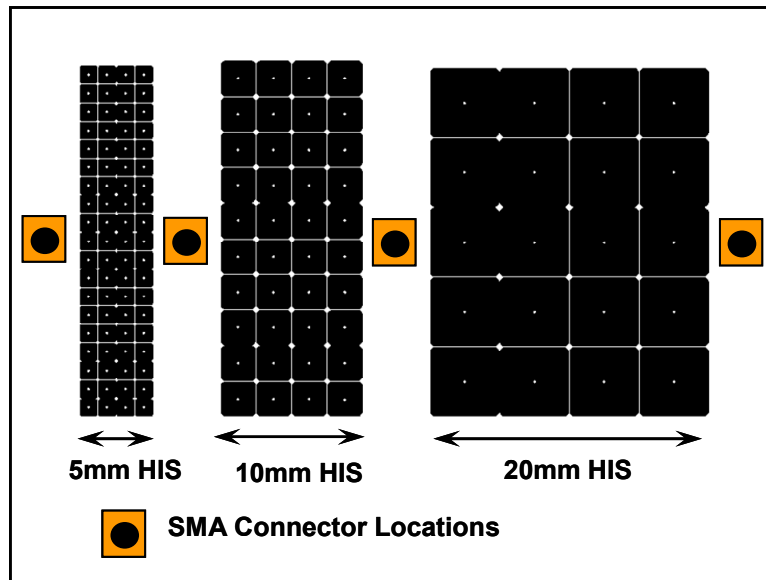


Figure 3-4 Proposed wideband/multiple band structure (gap size = 0.4, via diameter = 0.8 mm, board thickness = 1.54 mm and $\epsilon_r = 4.1$). Top view of the middle layer of the PCB and measurement points. Schematic of the overall filter.

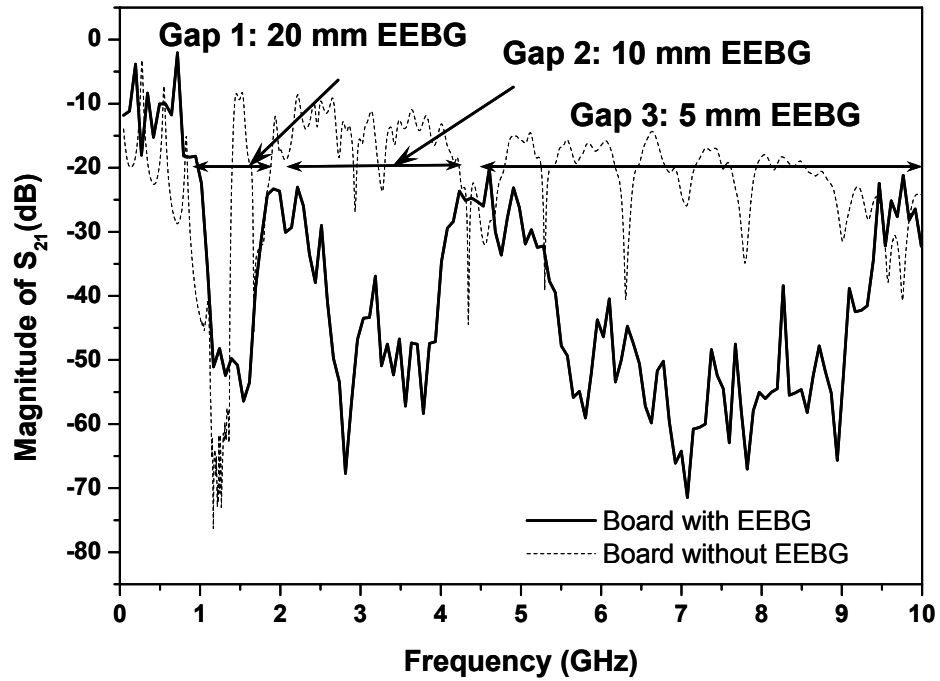


Figure 3-5 Measured S_{21} of the fabricated PCB shown in Figure 3-3 employing the cascaded EEBG structures. S_{21} is measured between the farthest SMA connectors (port 1 and port 2) as shown in Figure 3-3 using a Vector Network Analyzer.

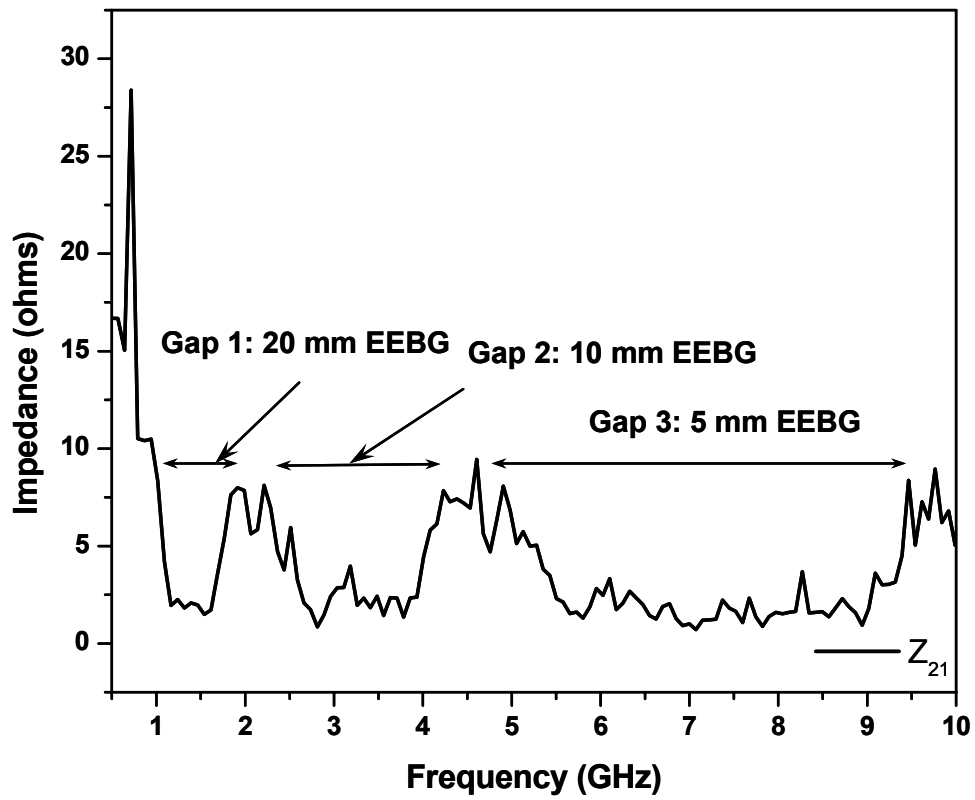


Figure 3-6 Plot of the impedance equivalent of the results of Figure 3-5 derived using equation 1-6.

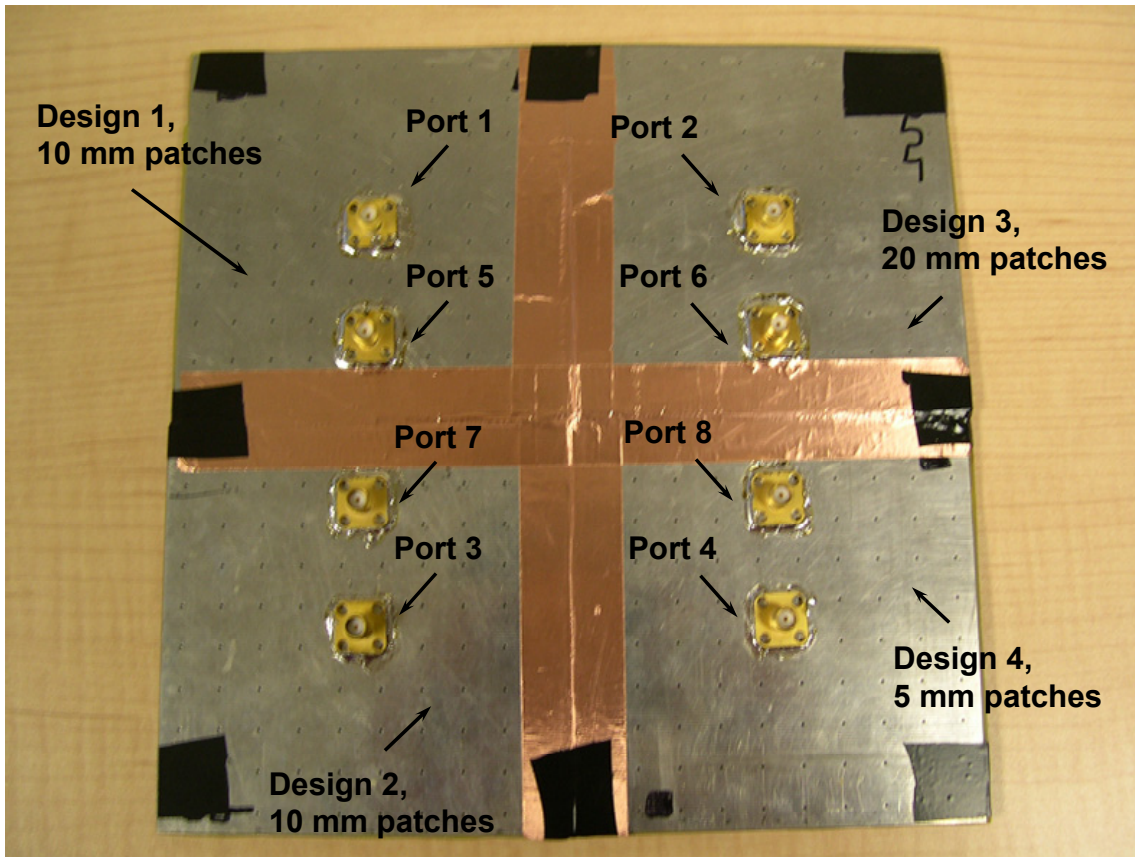


Figure 3-7 Test board used to test the sketch board design concept. Design 1 and design 2 are the same.



Chapter 4. Electromagnetic Interference (EMI) Suppression using EEBG Structures

4.1 Design Concept

Electromagnetic radiation of high-speed digital and analog circuits is considered one of the most critical challenges to the electromagnetic interference, compatibility and reliability of electronic systems. The continuous decrease in power supply and threshold voltage levels in CMOS based digital circuits increases their vulnerability to external electromagnetic interference. At the same time, the increase in clock and bus speed increases the potential of the circuit to radiate, thus compromising its compatibility potential and also increasing its security vulnerability. Switching noise is one of the major concerns for EMC engineers in modern designs [4] [39].

Electromagnetic interference is a complex mechanism that takes place at different levels including the chassis, board, component, and finally, the device level. Radiation sources typically include trace coupling, cables attached to the boards, components such as

chip packages and heat sinks, power busses and practically anything that can provide a low impedance current path. As the speed of modern high-performance digital circuits increases rapidly, their energy consumption increases as well. The required energy is provided by power planes embedded in the multilayer structure of the board. These power planes induce radiation in a manner highly analogous to the way microstrip antennas radiate. In microstrip patch antennas and in printed circuit boards (PCB), radiation is induced by a time-varying fringing electric field at the edges of the board. Recent studies describe this phenomenon [40] and others characterize this phenomenon analytically and through numerical simulations [5].

In previous works, several techniques were used to reduce this type of radiation. These methods include shielding, the placement of decoupling capacitors [6] [7], the use of embedded capacitance [8], the placement of resistive terminations on the edges of the board [9], employing lossy components throughout the board [10], dividing power planes in power islands [12], via stitching [13], or a combination of any of these techniques. Among these methods, via stitching is the most common method used in practice and its effectiveness has been quantified through rigorous Finite Difference Time Domain (FDTD) simulation as reported in [41]. All noise mitigation techniques, however, that employ discrete capacitor components have a fundamental limitation due to the inherent inductance arising from the leads of the capacitors (see [41] and references therein). For embedded capacitance, its relatively high cost and reliability considerations reduces its practical use at this time.

This study presents the first work on applying EEBG to reduce radiation from power busses of PCBs. It shows that for multilayer printed circuit boards, the presence of EBG structures between each pair of power planes can effectively shield the edges of the board and therefore decrease the level of radiation from such edges. The use of the EEBG structures is not limited to EMI radiation suppression from power busses and it can be extended to radiation suppression from signal layers as well.

4.2 Implementation, Measurements and Results

EEBG structures considered in this chapter are fabricated using commercial PCB manufacturing technology. In experimental stages, as described in chapter 2 and chapter 3, the printed circuit boards were constructed by compressing a double-sided PCB similar to the one shown in Figure 4-1 and a single-sided PCB involving one of the power planes together, to avoid the cost of blind vias.

As proved in chapter 2 using exhaustive full-wave simulations conducted on EEBG structures, extending the vias of the structures to the other plane (removing the copper around the hole on the other plane to avoid shorting of the two planes, therefore creating an anti-pad) and shrinking the thickness of the board to practical multilayer sizes (0.15 mm to 1 mm [42]) do not have appreciable effect on the bandgap. This concept is valid also for EEBG structures used for EMI suppression, therefore in practical applications, design parameters can be modified in order to achieve the same performance as thicker prototypes, with and without blind vias, making their fabrication inexpensive and practical.

Figure 4-1 shows a picture of a printed circuit board fabricated to test the proposed radiation suppression concept and Figure 4-2 is a diagram that shows the experimental

setup used to characterize such boards. The signal was fed to the parallel-plate environment through an SMA connector to the middle of the board using a vector network analyzer (VNA). The amount of radiation from the edges of the board is measured by measuring the scattering parameters (S_{21}) as a representative for the radiated power at various test points around the board, also shown in the diagram of Figure 4-3. These test points were chosen to show the omni directional suppression property of the proposed design. As shown in the diagram of Figure 4-2 a monopole probe (length 4 cm, diameter 3 mm made of copper) connected to the other cable of the analyzer through a SMA connector represents the receiver in this experimental set up. For details on the design of this monopole probe refer to Appendix A.

The area with no EBG structure in Figure 4-1 has been kept minimal in order to maximize the radiated energy received by the receiving antenna. In a practical scenario, a 5 mm patch EBG structure with four rows of EEBG resides in a 2 cm wide ribbon around the PCB. For a 20 cm x 10 cm board this is 28% of the PCB area. The presence of the EBG structure in this region implies some PCB design constraints for the PCB designers, in a similar way that placing decoupling capacitors on the board does. Considering the fact that components can reside on top of the structures and also that their power supply can be connected directly to the patches, it is most likely that for practical applications their impact is minimal. In fact, the assumption is that this technique does not impose an enlargement of the actual PCBs, but rather the EBG structures are being implanted into the border side of an already designed PCB with appropriate modifications. It should be emphasized that, although the concept of radiation suppression using EEBG structures is general, patch sizes

larger than 5 mm are not practical, thus more complex EBG structures need to be used for low frequencies. Chapter 5 introduces a novel conceptual design for such structures.

Figure 4-4 to Figure 4-8 show the results of these measurements. A wide gap from 4 GHz to 10 GHz shows an average suppression of 30 dB within this gap in comparison to the case without the EEBG structures. Higher attenuation than predicted by initial simulations at higher frequencies is highly likely due to dissipation in the FR4 substrate and to higher (but not significant) bandgaps created by the structure. The plot of measured S_{21} for a reference board without the EEBG structures is also included for comparison.

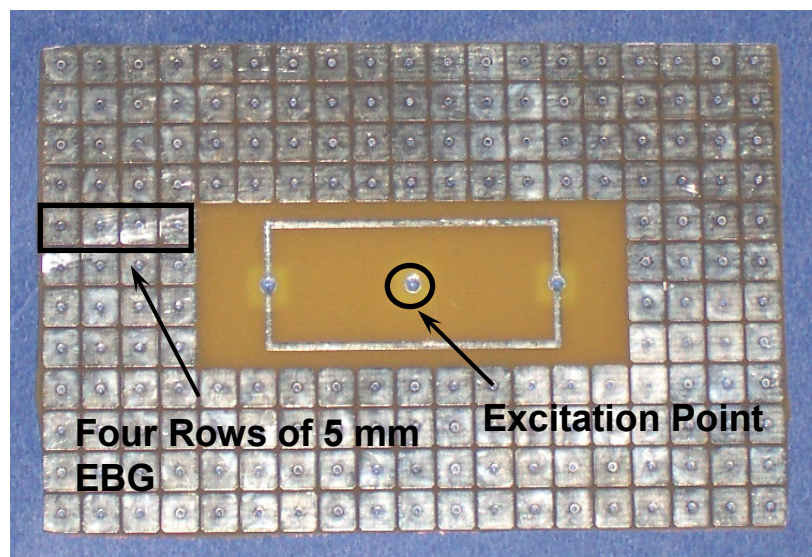


Figure 4-1 Test board (6.5 cm x 10 cm) fabricated on commercial FR4 in order to test the EMI suppression concept using EEBG structures. A ribbon of four rows of EEBG structures with patch size of 5 mm x 5 mm, $vd = 0.8$ mm, $g = 0.4$ mm and $h_1 = h_2 = 1.54$ mm. The source of noise (excitation point) is in the middle of the board.

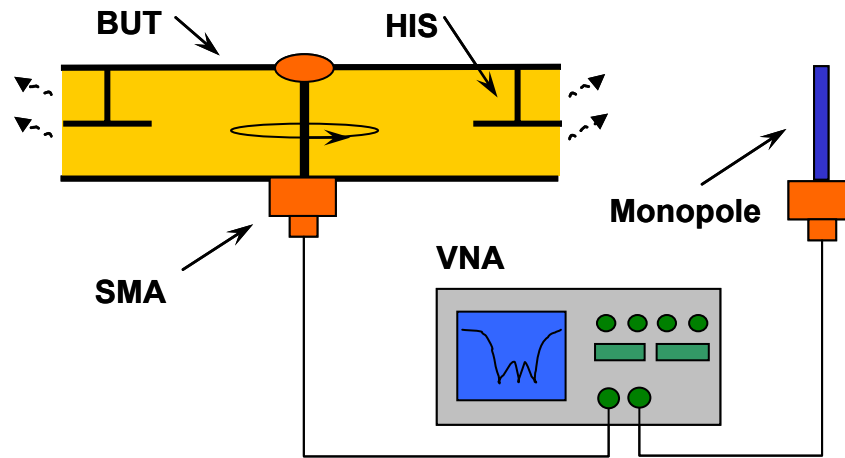


Figure 4-2 Experimental setup for S_{21} measurements for boards under test (BUT). One of the ports is connected to BUT and the other one to a monopole antenna.

4.3 Ultra Wide-Band EMI Reduction

Widening the suppression band-gap can be accomplished by using cascaded high-EEBG structures such as the structures described in chapter 3 around the board, creating an ultra wide-band stop band for the propagating wave. As an example, the configuration shown in Figure 4-9 with a board size of 20.6 cm x 16.6 cm is considered, and a signal source positioned at the center and connected to the board through an SMA connector. In this configuration an EEBG structure with a patch size of 10 mm is added to a structure with a patch size of 5 mm. Figure 4-4 shows the measured S_{21} response for this configuration, at test point 1 shown in Figure 4-3. Due to the omni directional suppression property of the EEBG structures already shown in Figure 4-4 to Figure 4-8 for a single stage structure measurements at other test points reflect the same radiation suppression

behavior. Experimental results in Figure 4-10 show that an additional gap between 2 GHz and 4 GHz is introduced by the added structure (with a period of 10.4 mm). This property is especially relevant to cases in which the suppression of a fundamental frequency is as important as the suppression of the harmonics of that frequency. As an example, as illustrated in Figure 4-10, the design in Figure 4-9 is capable of suppressing not only a noise at 3 GHz but also its second and third harmonics at 6 GHz and 9 GHz, creating ultra-wide band suppression radiation from printed circuit boards employing such design.

In summary, this study introduces the novel concept of using electromagnetic bandgap structures for the suppression of electromagnetic radiation generated by high-speed and high-current switching, also known as switching noise, from power busses of printed circuit boards. Simulation and experimental results prove the effectiveness of this method in suppressing radiation from printed circuit boards in a range of frequencies over which the conventional methods are not effective (0.5 GHz and up).

Ultra-wide band suppression of such radiation is achieved by cascading different configurations of high-impedance surfaces. The significance of ultra-wide band suppression lies in the fact that cascaded EEBG structures provide a practical way to suppress radiation not only at the fundamental frequency of noise but also its harmonics. PCB prototypes were designed, developed and tested showing unprecedented level of EMI reduction over an ultra-wide band of frequencies that can encompass the noise frequency and its immediate harmonics.

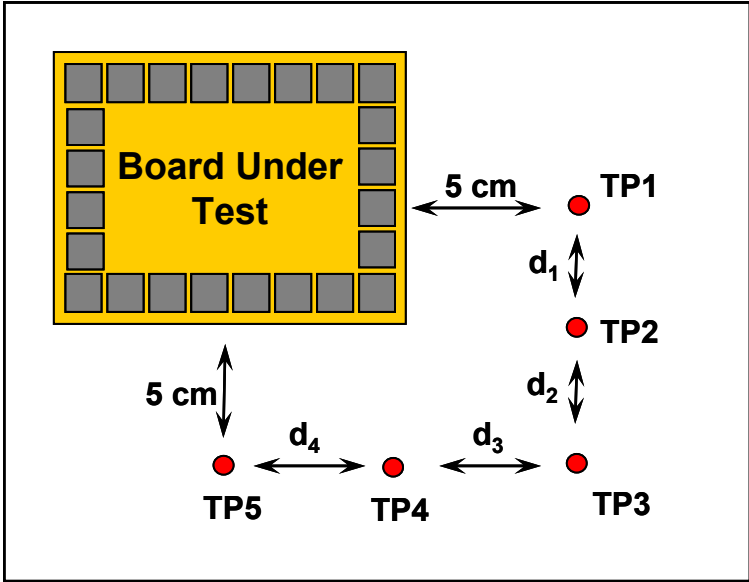


Figure 4-3 Location of different test points (TP) in all experiments.

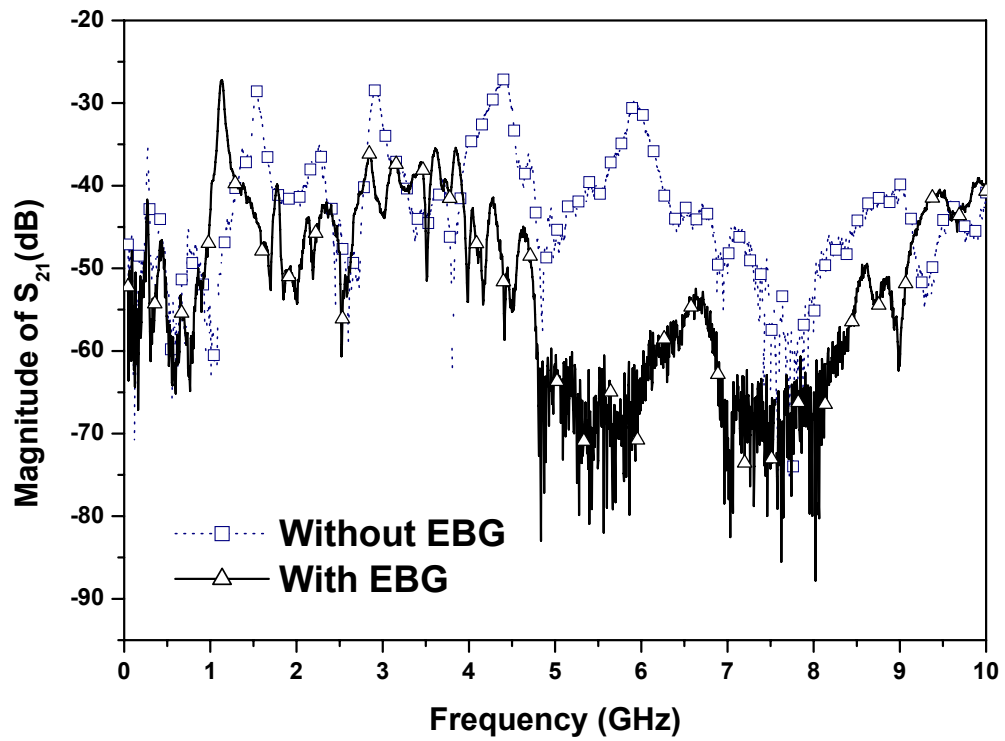


Figure 4-4 Measured S_{21} for the structure in Figure 4-1 within a power bus configuration, at test point TP1, with and without EBG structures.

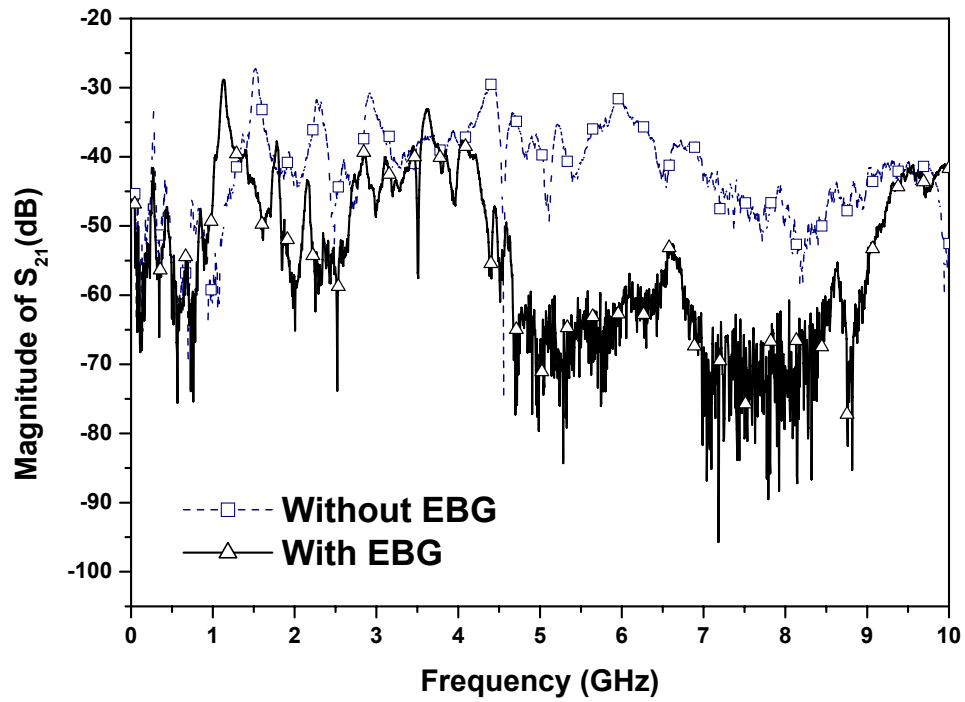


Figure 4-5 Measured S_{21} for the structure in Figure 4-1 within a power bus configuration, at test point TP2, $d_1 = 3.25$ cm, with and without EBG structures.

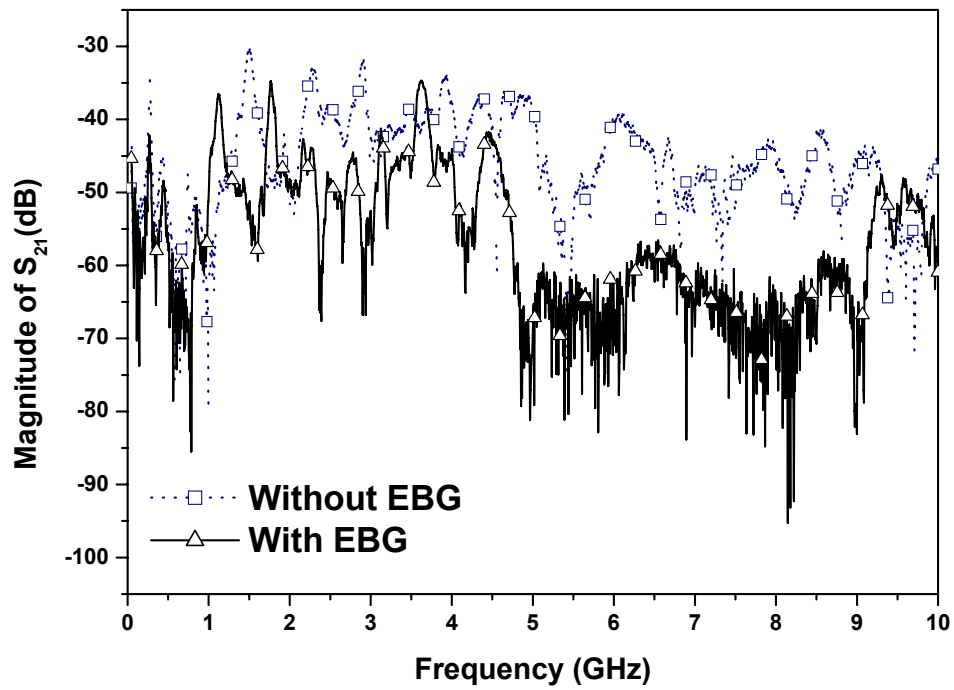


Figure 4-6 Measured S_{21} for the structure in Figure 4-1 within a power bus configuration, at test point TP3, $d_2 = 5$ cm, with and without EBG structures.

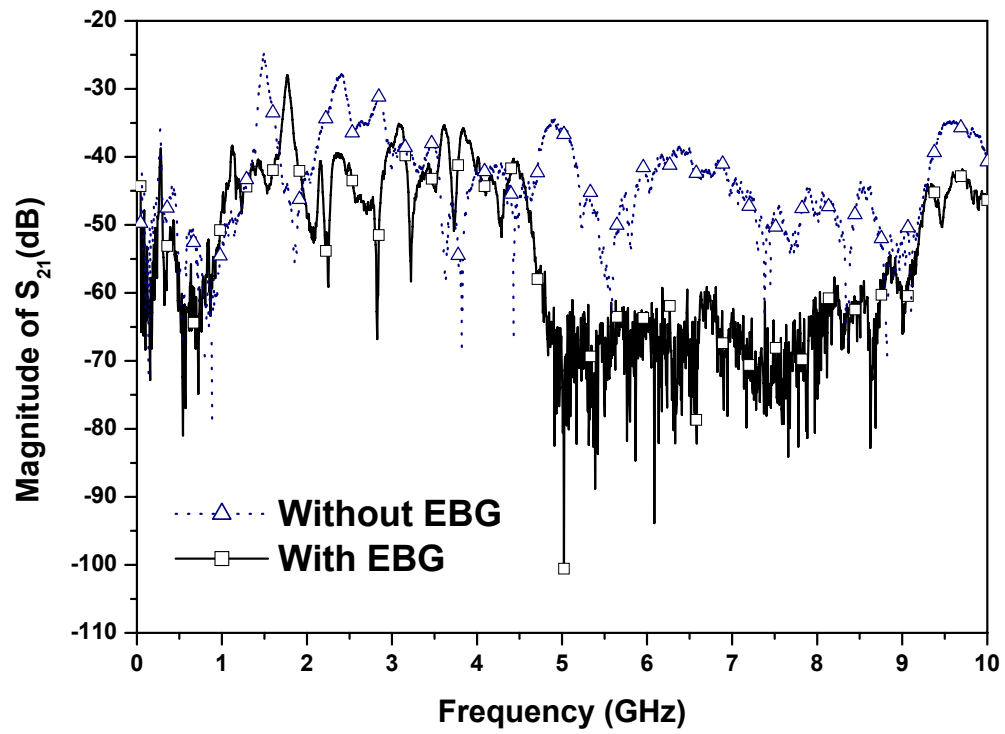


Figure 4-7 Measured S_{21} for the structure in Figure 4-1 within a power bus configuration, at test point TP4, $d_3 = 5$ cm, with and without EBG structures.

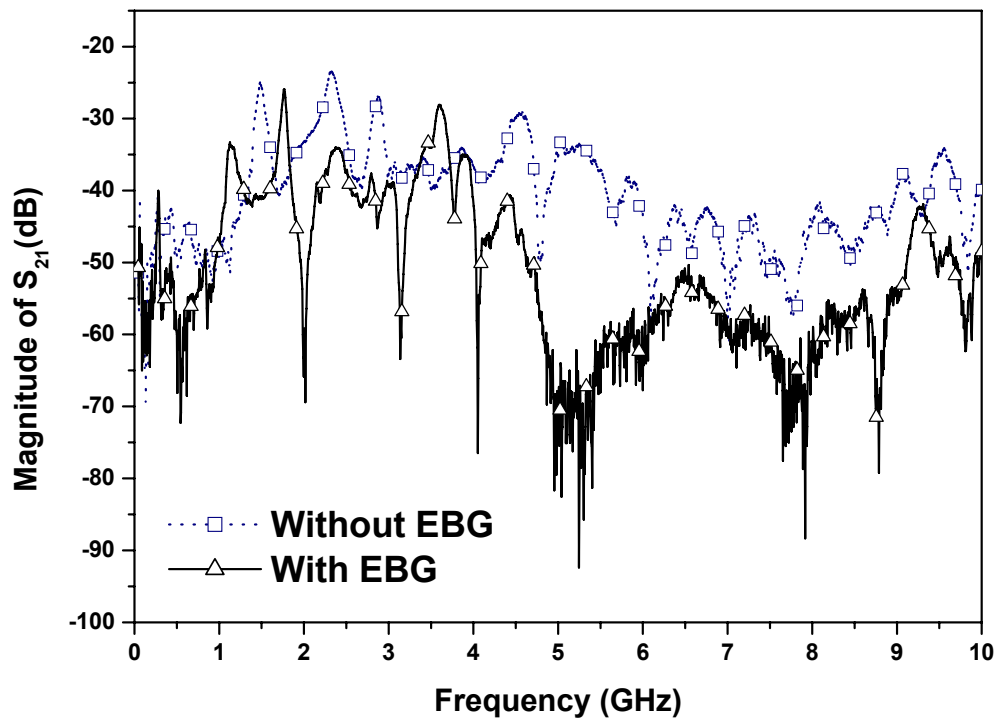


Figure 4-8 Measured S_{21} for the structure in Figure 4-1 within a power bus configuration, at test point TP5, $d_4 = 5.1$ cm, with and without EBG structures.

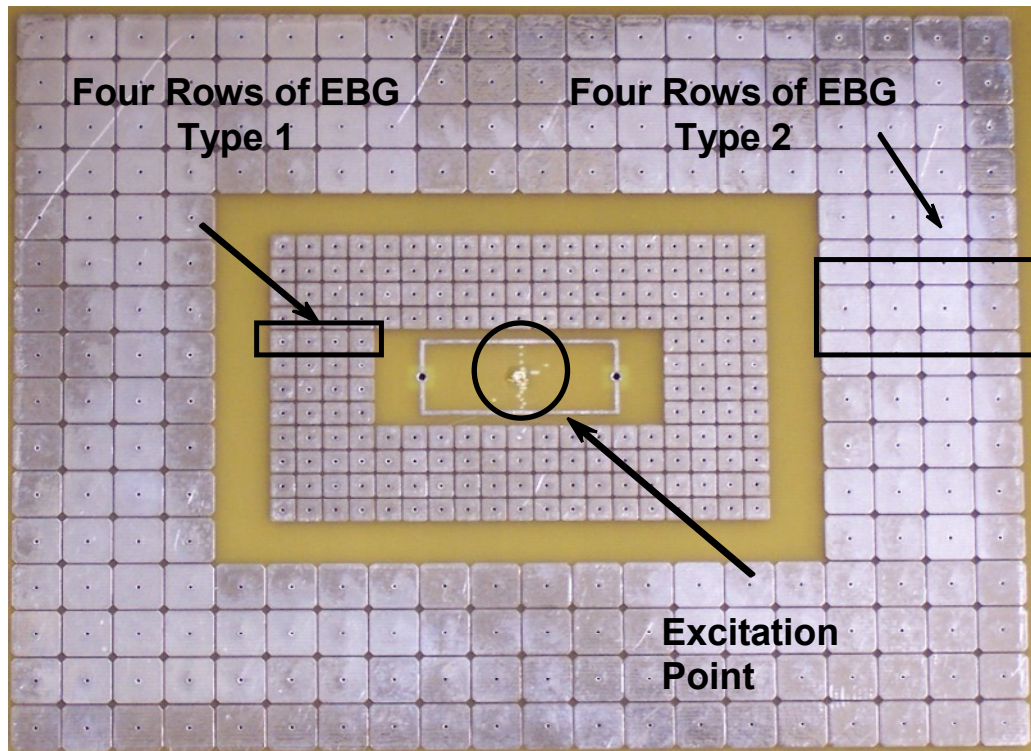


Figure 4-9 Cascading two EBG structures with different configurations (5 mm and 10 mm patches, 4 rows each, $g = 0.4$ mm, $vd = 0.8$ mm, $h_1 = h_2 = 1.54$ mm, $\epsilon_{r1} = \epsilon_{r2} = 4.1$, for an ultra wide-band suppression of radiation from the edges of the PCB.

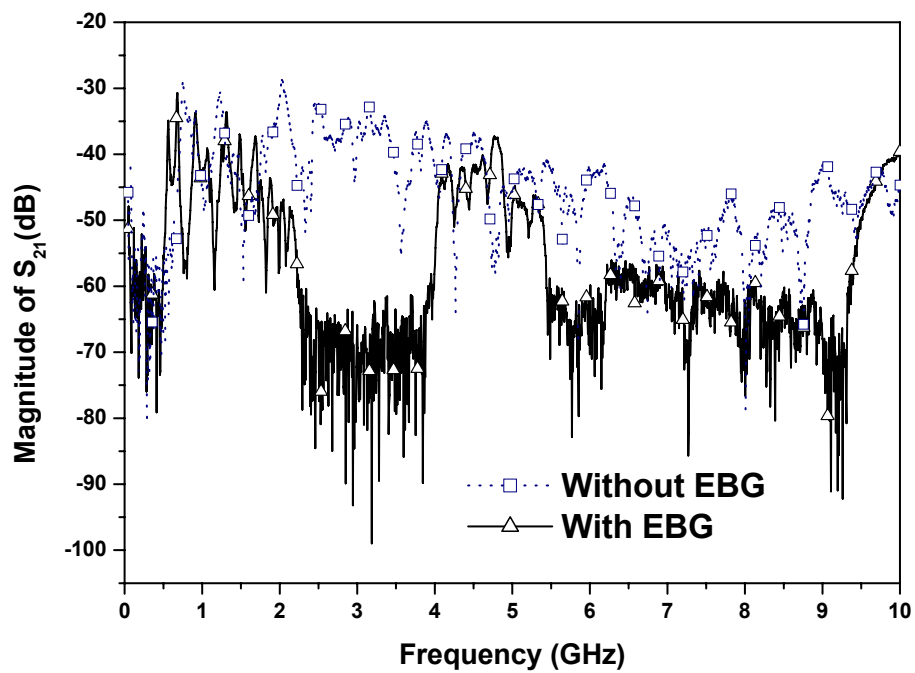
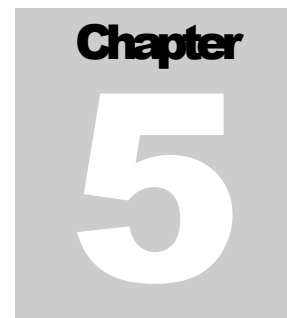


Figure 4-10 Measured S_{21} for the structure in Figure 4-9 within a power bus configuration, at test point TP1, with and without EBG structures.



Chapter 5. Broadband Noise Mitigation Using Miniaturized EEBG Structures on High-permittivity Material

5.1 Design Concept

For the past two decades, CMOS transistor technology has been advancing along an exponential path of shrinking device dimensions, increasing density, increasing speed, and decreasing cost. This advance may soon come to an end because of various constraints, such as static power dissipation due to leakage current, the effect of wires and interconnects and the decreased immunity of modern devices to noise, interference and voltage fluctuations on their power distribution network.

Switching noise is known to be the main source of noise and voltage fluctuations on the power planes of the printed circuit boards (PCB) and packages that contain modern CMOS-based devices. The main elements required for generation of this type of noise are a high-speed time-varying current and a via that passes through the parallel plate of a power distribution network. The flow of high-speed time varying current through such vias causes

radiation. The radiated waves use the parallel plate wave guiding structure to propagate. At the edges of the PCB, a portion of these waves are reflected back and the rest is radiated. The radiated waves cause interference problems, and the reflected waves cause a resonance behavior in the cavity-like structure created by the parallel plates and the dielectric material between them.

Other vias that pass through the same parallel-plate structure act as receiving antennas. In this scenario, the devices connected to the receiving vias become victims of the radiating via. This scenario is worsened when multiple vias radiate at the same time. The type of noise caused in such scenario is known as simultaneous switching noise (SSN). SSN, if uncontrolled, can cause logic circuits to switch state falsely. This false switching, in turn, can cause serious malfunctions in the subject circuits with catastrophic consequences.

To address this problem, methods introduced in past works, all intended to reduce the resonance effects of the cavity-like structure. The most widely used methods are use of decoupling capacitors, embedded capacitances and capacitors, use of dissipative and lossy components along the PCB and at its edges, dividing power planes in power islands, and finally via stitching. All these methods have an effective range of at most few hundred megahertz and are expensive to implement at high frequencies.

A novel concept for ultra-wideband suppression of switching noise in high-speed printed circuit boards (PCBs) is proposed, implemented and tested. This concept consists of using asymmetrical, Embedded Electromagnetic Bandgap (EEBG) Structures in conjunction with material with high dielectric constants. The proposed design modifies the

classical EEBG structures to achieve a high degree of miniaturization and an unprecedented broadband mitigation of switching noise.

The novel design presented in this chapter not only eliminates the drawback of previous designs by providing noise suppression over a wide range of frequencies but also extends the suppression frequency range into the sub GHz region.

A conventional EEBG design consists of structures in which the patches are located in a plane in the middle of the parallel-plates of the power distribution network (PDN) at equal distance from each plate with a uniform substrate material (constant and unique dielectric material such as FR4) in between these plates.

In this chapter two modifications to a conventional EEBG structure are proposed. In our design two dielectric materials are used. A different material with high dielectric constant is employed for the space above the patches and the thickness of this material is made to be very thin. This modification creates an asymmetrical structure in which the patches are far closer to one of the parallel-plates than the other [43].

Figure 5-1 shows a lateral cut of a PDN with EEBG structures in a general configuration in which the material of the region above the patch is not necessarily the same as the one below the patches.

Figure 5.2 is a diagram for a test setup that in conjunction with a VNA may be used to test the asymmetrical design concept mentioned above.

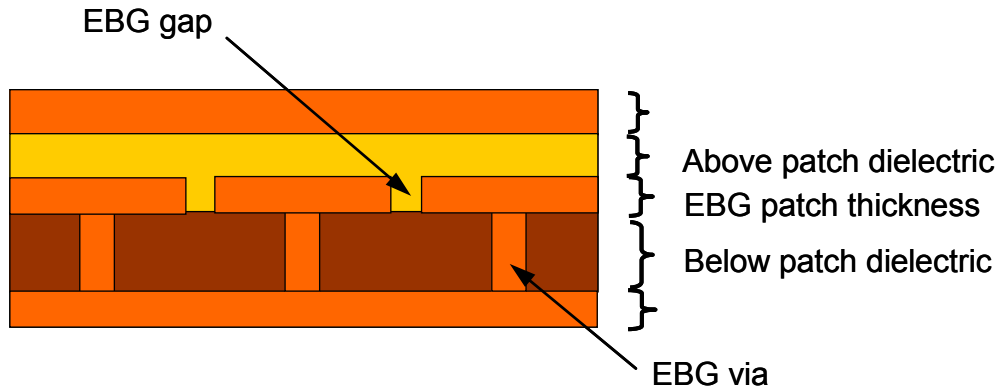


Figure 5-1 Lateral view of electromagnetic bandgap structures embedded between two power planes of a power distribution network. Thickness of the region above the patches is different from thickness and material of the region below the patches.

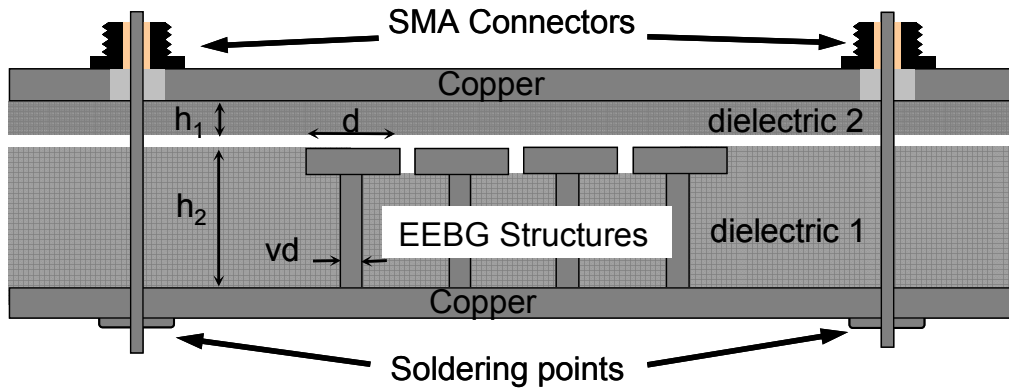


Figure 5-2 Lateral view of a typical simulation/experimental setup showing the application of the structures described in Figure 5-1. Specifically $h_1 \ll h_2$ and $\epsilon_{r1} \gg \epsilon_{r2}$. d is the period of the structure, g is the gap size and a is the lateral patch size: $d = a + g$.

This chapter has two claims. First, by using an asymmetrical design (i.e. a one in which the thickness of the dielectric material below the patch is greater than the thickness

of the material above the patch) and by using vias with very small diameter the equivalent inductance of the resonant circuit increases [14]]. In this scenario, therefore a given patch size has band-stops at a lower frequency compared to a symmetrical scenario. As an example as shown in chapter 2 and chapter 3 an EBG with 5 mm x 5 mm patch sizes has a band-stop region from 4 GHz to 8.2 GHz ($g = 0.4$ mm, $vd = 0.8$ mm, $h_1 = h_2 = 1.54$ mm, $\epsilon_{r1} = \epsilon_{r2} = 4.1$). By comparing this result to entry 8 of Table 2-1 an asymmetrical design has a 2 GHz downward shift without compromising the size of the stop region

Second, by increasing the dielectric permittivity of the material above the patch (that now is thinner than the dielectric below the patch because of the first modification), the equivalent resonance capacitance increases even further, without compromising the higher end of the band-stop region therefore creating a suppression over an ultra-wide band of frequencies. In the next section, simulation results and a detailed analysis are presented.

5.2 Simulation Results

Two main methodologies have been used to derive the band-stop region of the designs under investigation: dispersion relation derivation and scattering parameter extraction.

In the simulation setup for dispersion relation derivation, a single cell (top plate, bottom plate, patch, via and dielectric materials) is being analyzed. The simulator finds the possible propagating modes and their frequencies. The band in which there is no propagating mode is the band-stop region of the periodic structure composed by the single cell being analyzed.

In the second type of simulation setup four infinitely long rows of EBG cells are placed between two ports. The S_{21} parameter representing the received power at the second port due to an incident power at the first port, will show the band-stop region as a region where the received power is minimized. The precision and validity of these two methods has been described and widely proven throughout previous chapters.

Figure 5-3 shows the dispersion diagram of an EBG with parameters described in the first four entries of Table 5-1. This simulation has been done to show the effect of changing the permittivity of the dielectric material above the patch. As illustrated, the net effect is that the center frequency of the bandgap is being shifted down with a negligible impact on the bandwidth (second claim of the previous section). By applying the same concept to very small patch sizes that inherently produces gaps in higher frequencies one can observe a very wide-band stop-region that starts from the low-GHz region (i.e. Entry 5 of Table 5-1). The dispersion diagram for entry 5 of Table 5-1 is also shown in Figure 5-4. To compare the results of applying the first claim and the second claim of the previous section, two more simulations have been performed and the results are illustrated in Figure 5-4. These simulations are the results of entry 7 and 8 in Table 5-1. In other words, entry 5 can achieve an ultra-wide band gap using high-dielectric material. Cascading entries 7 and 8 can also achieve a wide band-region but at a lower cost. The trade off is size vs. cost. Entry 6 of Table 5-1 has been included to show that the impact of the patch thickness on the results is minimal.

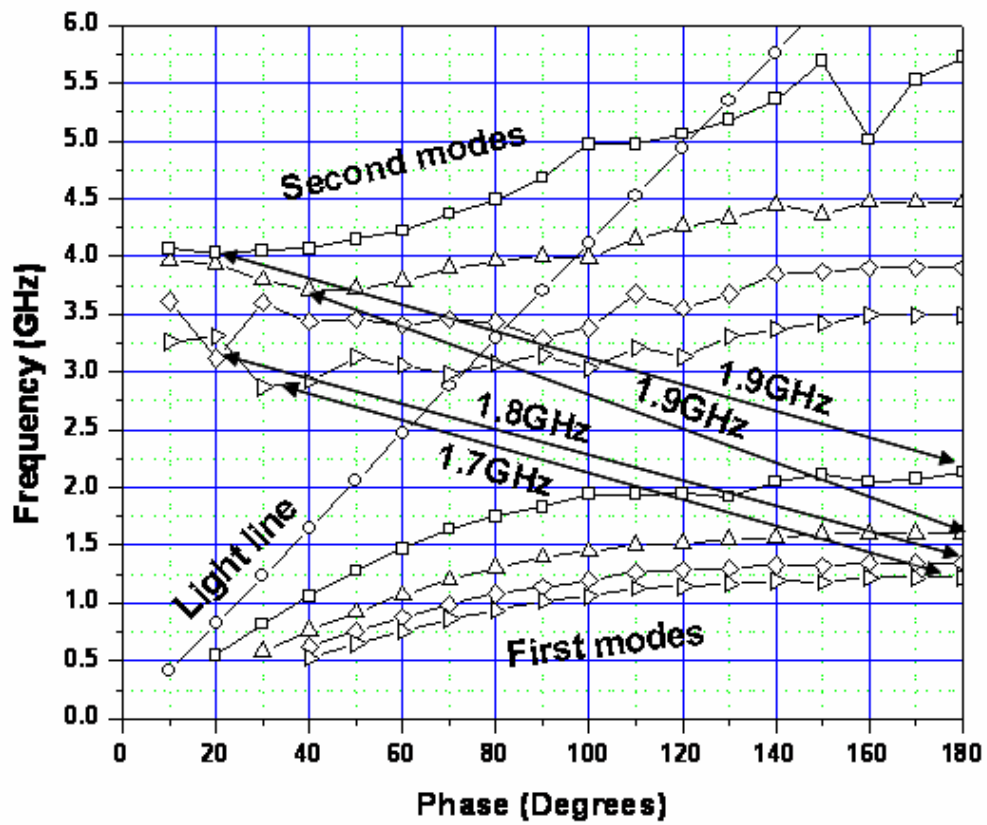


Figure 5-3 Dispersion diagram for a 10 mm x 10 mm patch structure while the permittivity of the dielectric above the patch changes (First four entries of Table 5-1). The distance between the first mode and the second mode for each structure (no propagation) is the band-stop region.

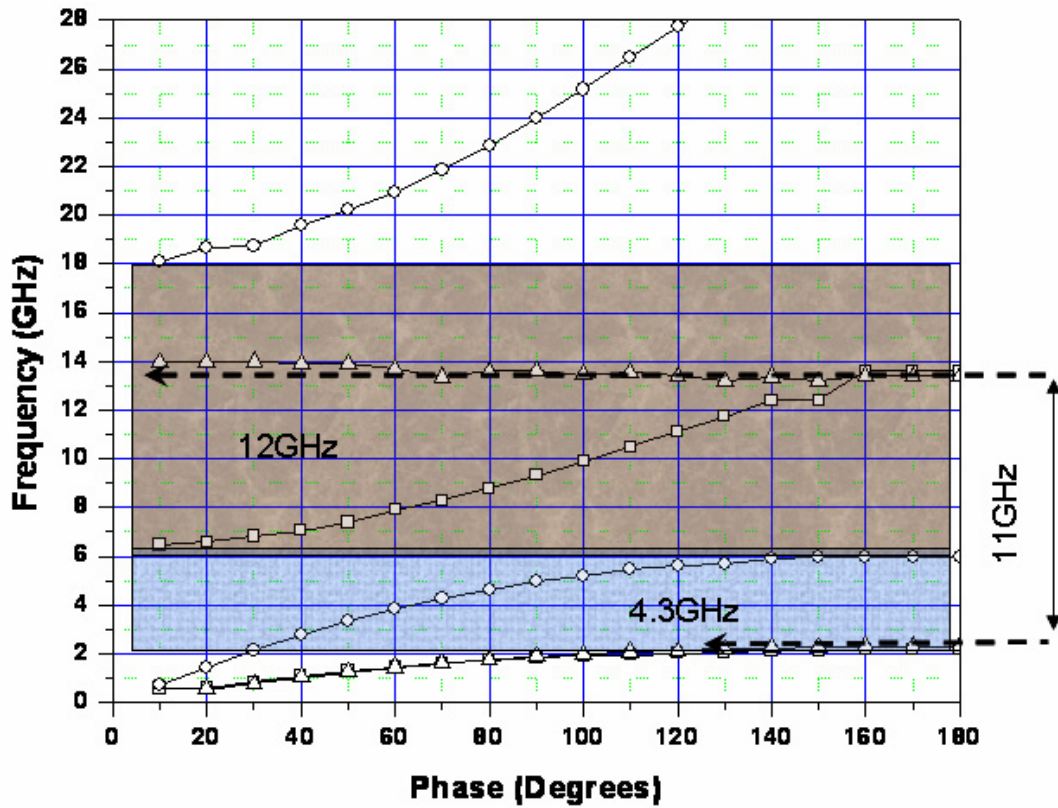


Figure 5-4 Dispersion diagram for entries 5, 7 and 8 in Table 5-1. Entry 5 can achieve and ultra-wide band gap (11 GHz) using high-dielectric material. Cascading entries 7 and 8 can also achieve a wide-band region (16 GHz) but at a far lower cost.

At last, one last design (entry 9 of Table 5-1) was simulated to demonstrate how a single and compact structure can provide noise suppression over a frequency range where the noise has much of its energy concentrated [15].

Figure 5-5 shows the S-parameter extraction for such design.

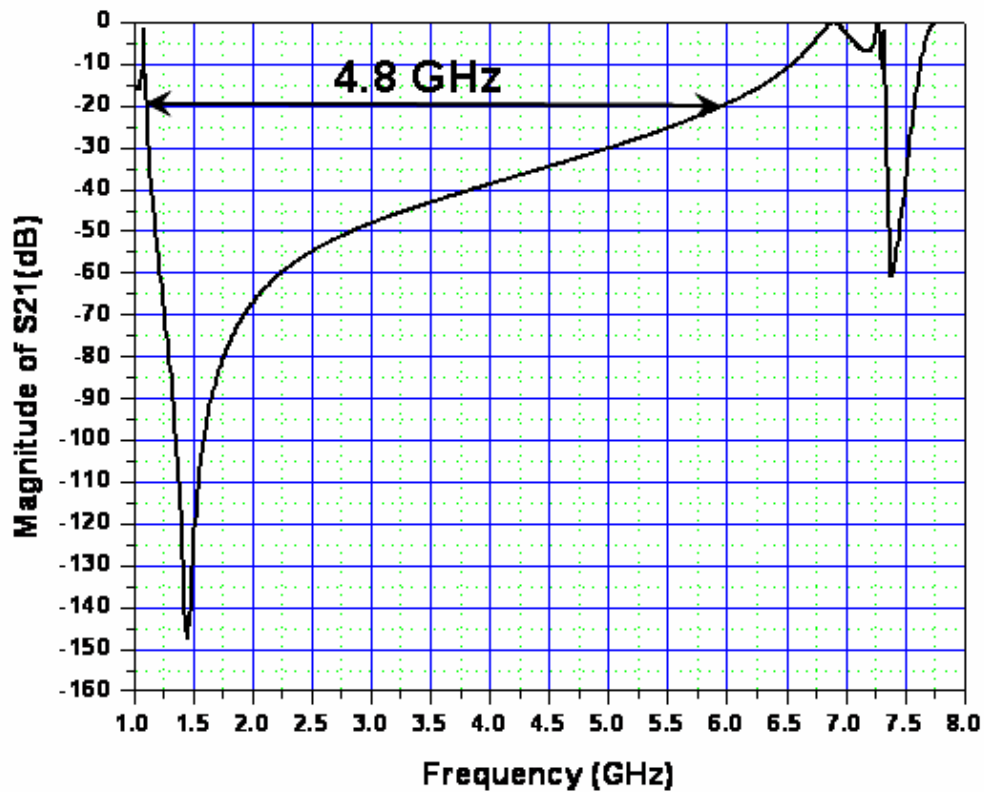


Figure 5-5 Simulation-derived (FE) attenuation for a power plane pair that employs EBG structures (entry 9 of Table 5-1).

A 4.8 GHz bandgap from 1.2 GHz up to 6 GHz is clearly visible. It should be noted that eigenmode simulations used to derive dispersion diagrams usually result in gaps consistent with the -10 dB bandwidth. In S-parameter extraction, especially in experimental analysis, it is safer to consider the -20 dB line since it stays away from the edge of the band, therefore resulting in a slightly more conservative and smaller bandwidth. At this point the initial claims of this chapter are analyzed again using the TLPS model introduced in

chapter 2, hence analyzing the s-parameters of the structure rather than dispersion diagrams.

Entry	Patch size (mm)	ϵ_{r1}	ϵ_{r2}	h1. (μm)	h2 (μm)	Patch th. (μm)	g (μm)	Vd (μm)	f_l	f_h
1	10x10	4.1	4.1	1540	1540	0	400	800	2.13	4.03
2	10x10	8.2	4.1	1540	1540	0	400	800	1.6	3.71
3	10x10	12.3	4.1	1540	1540	0	400	800	1.35	3.12
4	10x10	16.4	4.1	1540	1540	0	400	800	1.22	2.87
5	2x2	30	4.1	16	100	0	200	125	2.3	13.19
6	2x2	30	4.1	16	100	35	200	125	2.28	13.22
7	2x2	4.1	4.1	16	100	0	200	125	5.96	18.11
8	5x5	4.1	4.1	16	100	0	200	125	2.17	6.46
9	5x5	16.4	4.1	16	100	0	200	125	1.11	6.44

Table 5-1 Band-stop frequency range of various EBG structures derived by eigenmode simulation using a finite element full-wave solver. (th = thickness, f_l = lower frequency of the gap, f_h = higher frequency of the gap)

In summary, a revolutionary method that can be used to effectively suppress noise in a very wide range of frequencies consists of first, using an asymmetrical design (i.e. one in which the thickness of the dielectric material below the patch is greater than the thickness of the material above the patch) and by using vias with very small diameter the equivalent inductance of the resonant circuit increases.. In this scenario, therefore a given patch size has band-stops at a lower frequency compared to a symmetrical scenario. Second, by increasing the dielectric permittivity of the material above the patch (that now is thinner than the dielectric below the patch because of the first modification), the equivalent resonance capacitance increases even further, without compromising the higher end of the band-stop region therefore creating a suppression over an ultra-wide band of frequencies.

A conventional EEBG design consists of structures in which the patch is located in the middle of the parallel-plates of the PDN at equal distance from each plate with a uniform substrate material with constant and unique dielectric material (e.g. FR4).

By studying the effect of two parameters of structure on the scattering parameters, S_{21} in particular using the TLPS model and specifically equation 2-8, a novel EEBG design can be derived. Figure 5-6 shows the magnitude of S_{21} versus frequency for a structure with $d = 5.4$ mm, $g = 0.4$ mm, $Vd = 0.8$ mm, $h_1 = 100$ μm , $h_2 = 16$ μm , $\epsilon_{r1} = 4.5$ while ϵ_{r2} changes. h_1 , h_2 , ϵ_{r1} and ϵ_{r2} are the thickness of the material above the patch, the thickness of the material below the patch and their respective dielectric constant as described in Figure 5-2.

Figure 5-7 shows the magnitude of S_{21} versus frequency for a structure with $d = 5.4$ mm, $g = 0.4$ mm, $vd = 0.8$ mm, $h_1 = 100$ μm , $\epsilon_{r1} = 4.5$, $\epsilon_{r2} = 4.5$, while h_2 changes. In both cases four unit cells with the same parameters have been cascaded.

The first observation is that both of these modifications to a conventional EEBG design lead to a new design with wider noise suppression bandwidth than the conventional EEBG. The second observation is that, increasing the dielectric constant of the material above the patch has an additional advantage of extending the noise suppression capability of the EEBG structure to sub-GHz frequencies (Figure 5-6).

The third and final observation is that both these modifications to a given conventional EEBG design create a new EEBG structure with a band-stop region with cut-off edges lower in frequency than the original one. Therefore EEBG structures with smaller patch sizes which traditionally had a band-stop region at high frequencies can now be transformed into EEBG structures with band-stop regions with relatively lower frequencies. This in turn results in a very compact miniaturized design for EEBG structures.

Results from the model presented in this section are in agreement with results from detailed full wave analysis presented in Table 5-1. Next section, reports experiments on the EEBG structures introduced in this chapter.

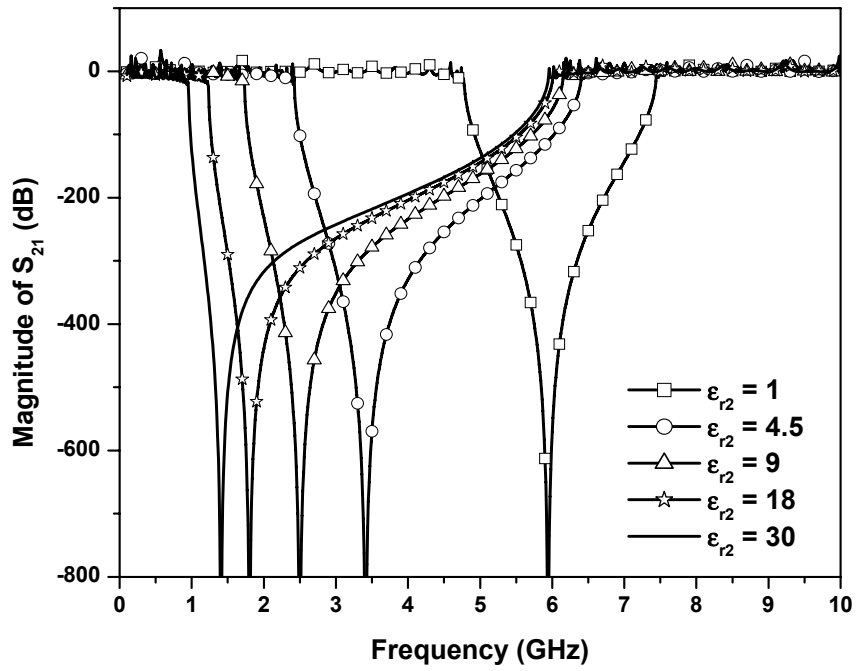


Figure 5-6 Magnitude of S_{21} versus frequency for a structure with $d = 5.4$ mm, $g = 0.4$ mm, $vd = 0.8$ mm, $h_2 = 100$ μm , $h_1 = 16$ μm , $\epsilon_{r2} = 4.5$ while ϵ_{r1} changes.

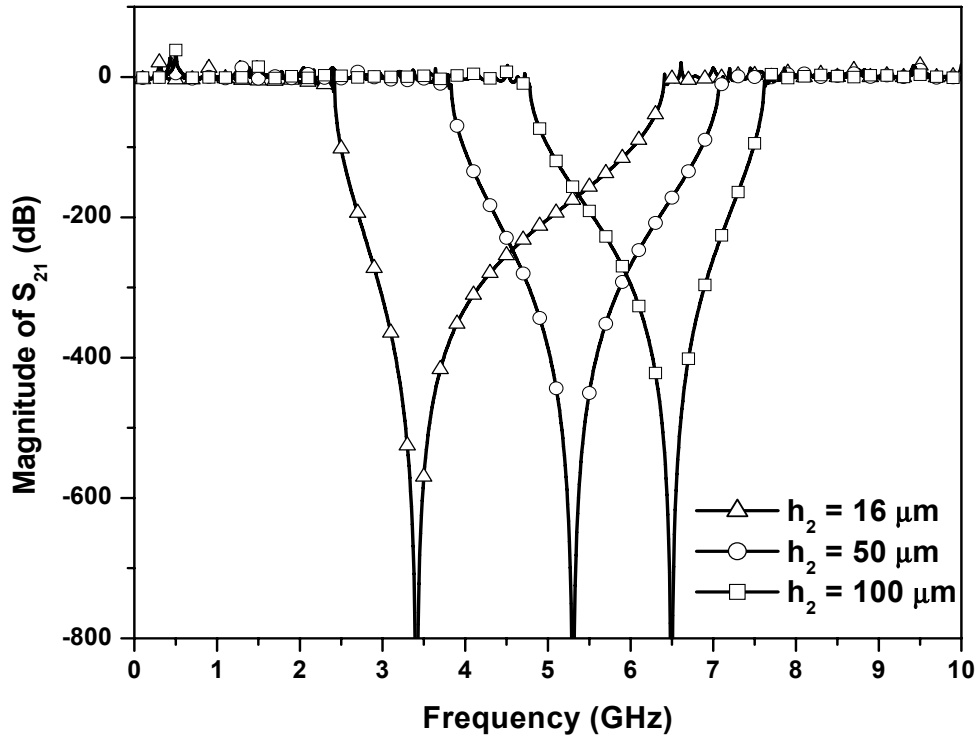


Figure 5-7 Magnitude of S_{21} versus frequency for a structure with $d = 5.4$ mm, $g = 0.4$ mm, $vd = 0.8$ mm, $h_2 = 100$ μm , $\epsilon_{r1} = 4.5$, $\epsilon_{r2} = 4.5$, while h_1 changes.

5.3 Implementation, Experiments and Results

At this point, experimental results performed on EEBG designs are presented to verify the effectiveness of this idea.

Figure 5-8 shows the experimental setup used for this experiment. SMA connectors are used to connect a Vector Network Analyzer (VNA) to the PCB in order to perform scattering parameter measurements. In this setup, the magnitude of S_{21} is proportional to the

noise power received from a victim located on port two while a noise source is switching at the location of port one.

The fabricated structure is composed of two main components: The bottom layer, with EBG structures implemented on commercial PCB technology (FR4 laminates) ($h_2 = 1540 \mu\text{m}$, $\epsilon_{r2} = 4.5$) and the top layer implemented using FaradflexTM [44] ($h_2 = 16 \mu\text{m}$, $\epsilon_{r1} = 30$) as dielectric material. The top layer was mounted on top of the fabricated bottom layer. Finally, as shown in Figure 5-8, the whole structure was pressed to remove any air gaps between the boards.

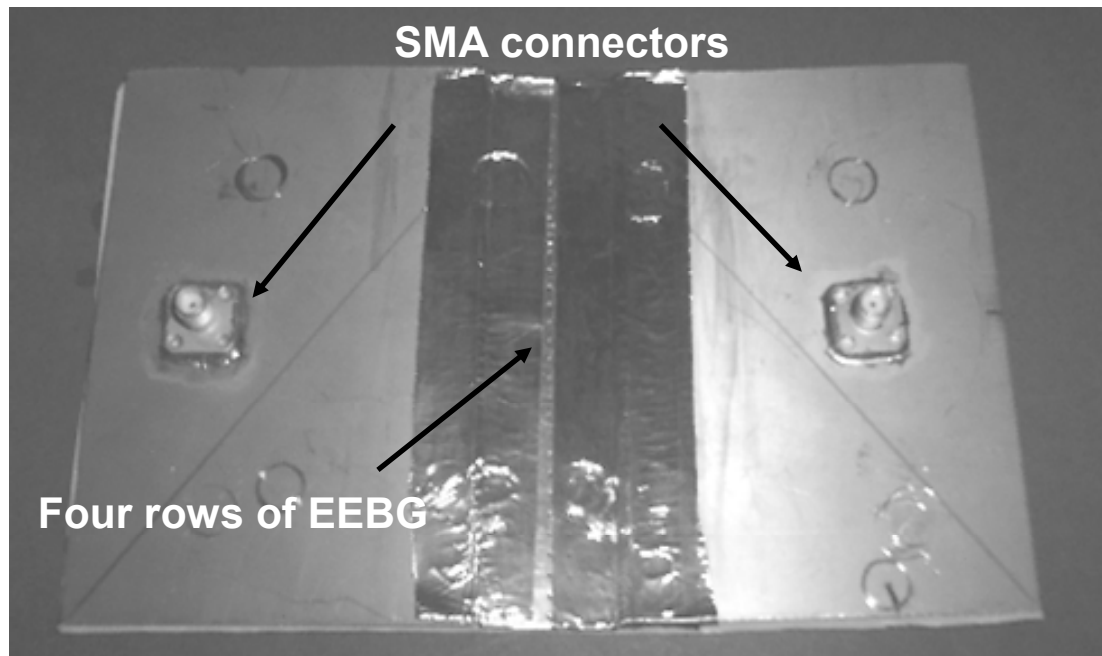


Figure 5-8 Top view of the fabricated PCB. This experimental setup is used to test the concept of broadband switching noise suppression using high-dielectric constant material.

Figure 5-9 illustrates the results of this experiment for a PCB with EEBG structure with a period of 3.4 mm and Figure 5-10 illustrates the results for a PCB with EEBG structure with a period of 5.4 mm. The results in Figure 5-9 illustrate the width of the suppression bandwidth of the new structures which extends from below 2 GHz to above 15 GHz. Figure 5-10 show how broadband suppression can be extended to sub-GHz frequencies. It should also be mentioned that pre-fabrication finite-element simulation predicted a far lower cut-off frequency for the lower edge of the gap for both experiments.

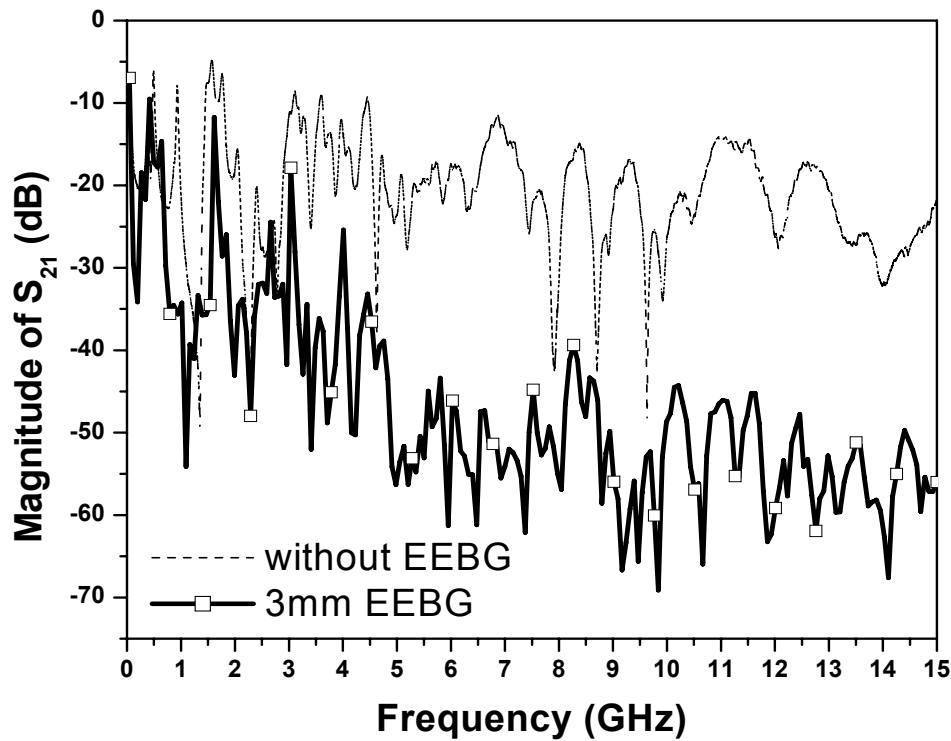


Figure 5-9 Measurement results for a structure with: $a = 3$ mm, $g = 0.4$ mm, $V_d = 0.8$ mm. Four rows of patches have been cascaded.

Minor discrepancies between simulated results and measured values, are mainly due to non-ideal conditions in the experimental setup. Specifically residual air gaps between adjacent patches and between the two boards that might be comparable to the thickness of the high-dielectric constant material. Another factor is that the thickness of the patches was neglected in the simulations.

Finally, from Figure 5-9 and Figure 5-10 two observations can be made. The first observation is that compared to a conventional EEBG design the new design has a substantial wider noise suppression band-width than the conventional EEBG structures.

The second observation is that new EEBG structures have a band-stop region with cut-off edges far lower in frequency than the original structures with the same patch sizes. Therefore EEBG structures with smaller patch sizes which traditionally had a band-stop region at high frequencies can now be transformed into EEBG structures with band-stop regions with relatively lower frequencies. This in turn results in a very compact miniaturized design for EEBG structures.

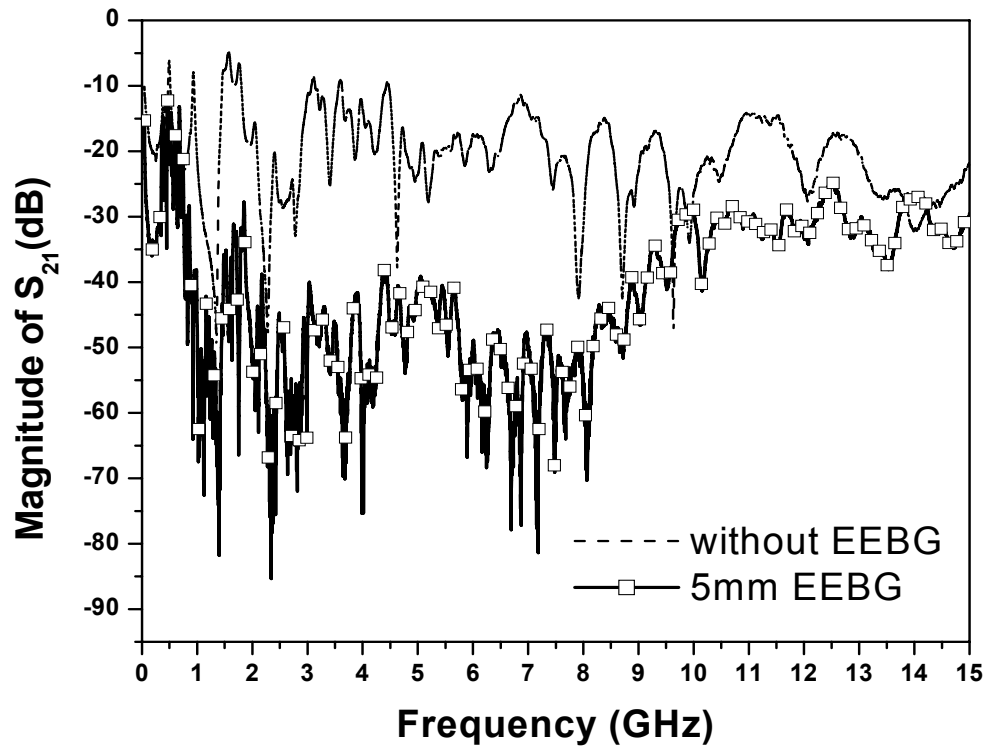
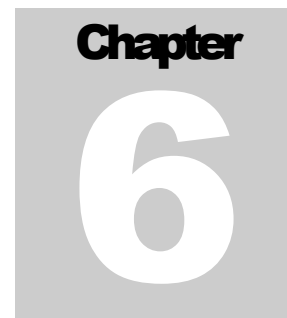


Figure 5-10 Measurement results for a structure with: EEBG period of 5.4 mm, a distance of 0.4 mm between patches, via diameter of 0.8 mm. Four rows of patches have been cascaded.



Chapter 6. Conclusions and Future Work

6.1 Conclusions

In this thesis, switching noise propagation and radiation in high-speed circuits and packages is mitigated through suppression of the propagating and resonant modes in a parallel-plane structure of a Power Distribution Network (PDN). The following results were obtained.

Simulation, experimental and analytical techniques for the design of EEBG structures were developed and matured.

Extensive tests and experiments were performed to validate the noise suppression capabilities of EEBG structures and also to quantify the accuracy of the simulation and analytical methods developed during this work.

The concept of wideband noise mitigation using cascaded structures is presented in details.

EEBG structures are shown to be a very effective tool for the suppression of Electromagnetic Interference (EMI) from PCBs. Due to the reciprocity theorem, EEBG

structures increase the immunity of the power distribution network of PCBs to high-frequency environmental noise and interference.

Finally, high permittivity-constant materials are combined with EEBG structures to create a very effective method for broadband switching noise mitigation whose effectiveness extend from sub-gigahertz frequencies to higher than ten gigahertz.

6.2 Future works

Consider two layer structures as an alternative to three layer EEBGs. In this type of structures filters are carved out one of the power planes.

It may be more convenient to fabricate the PDN in a two layer structure rather than three. The remaining issues that can be further investigated include radiation leakage from the PDN to adjacent layers and the fact that energy delivery to the local capacitors as local sources of energy may be disrupted by the increase of inductance on the power planes. Future studies on two layer structures need to address the issues mentioned above.

Consider EEBG structures that are not necessarily composed of patches parallel to the power planes and vias perpendicular to the patches (e.g. vias with a 45^0 angle and parallel patches). Fabrication processes at this time are not adequate for such designs, but in future this may change.

Consider time-domain analysis and experiments on EEBG structures. Most of the work has been done in frequency domain. Although recent works have started to look into time domain issues such as signal integrity in the presence of EEBG structures [45][46], further work needs to be done.

Finally, experiments and measurements on real-life circuits similar to the experiments mentioned in [38] and observations on immunity improvements will be definitely valuable.



Appendix A. Design of a monopole antenna over a ground plane using numerical codes

A quarter-wavelength monopole antenna is one of the simplest antennas to implement. They are tuned to specific frequencies (from tens of MHz to few GHz) and they have a narrow bandwidth. The performance of ideal monopole antennas over an infinite ground plane has been theoretically calculated [47][48]. Figure A-1 shows a diagram of the antenna under consideration.

The following section will cover the design of three ideal monopole antennas over an infinite ground plane and by using a commercial finite element simulator, HFSS [26] to simulate the effect of non-ideal characteristics on the antenna performance. These characteristics include the material used to fabricate the monopole, the finite area ground plane, and the presence of dielectric materials on the top of the ground plane (superstrate). The design is followed by comparison of simulation results (where possible) with experimental measurements, therefore validating implemented antennas.

A.1 Theoretical Designs

The theoretical directivity of a quarter-wavelength monopole over a ground plane is 5.16 dBi [47] and the direction of this maximum radiation is in the plane of the ground plane. The first resonant frequency of this antenna corresponds, approximately, to the frequency at which the length of the antenna is a one quarter wave-length:

$$f_0 = \frac{c}{4l} \quad (\text{Hz}) \quad \text{A-1}$$

In equation A-1, c is the speed of light and l is the length of the antenna above ground. As a result of equation A-1 antennas with resonance frequencies of 1 GHz, 2.45 GHz and 7 GHz will have lengths of 7.5 cm, 3.06 cm and 1.07 cm in free space, respectively.

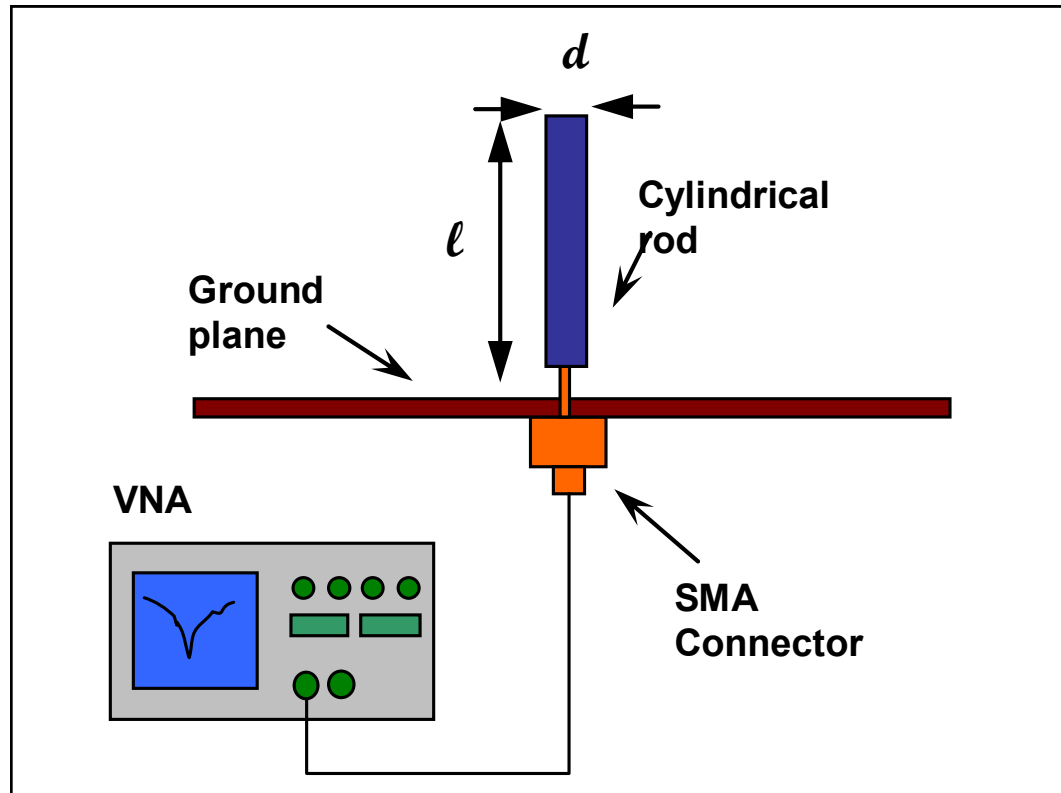


Figure A-1 Diagram of a monopole antenna over a ground plane (side view).

A.2 Design by Simulation

The three antennas considered in the previous section have been simulated using HFSS, with ideal conditions as well as non-ideal conditions. As suggested by HFSS manuals, the radiation boundaries have been kept at the distance of $\lambda/4$ from the body of the antenna. Also, the maximum mesh size on this boundary has been limited to $\lambda/6$. In the ideal case the antenna material is a perfect electric conductor (PEC) and the ground plane is infinite. In the non-ideal case, a limited ground plane of size 10 cm by 10 cm is considered. In addition the presence of dielectric materials on top of the ground plane is also considered. The antenna diameter (d) is considered to be 3 mm in all cases. Results from these simulations are tabulated in Tables A-1, A-1 and A-3.

For the ideal case, two types of excitation have been compared. In the first one, the 2.45 GHz antenna was excited using a 50 ohms coaxial cable and a wave port source. In the second case it was excited using a lumped gap source between the ground plane and the antenna. As expected, comparison of the simulations did not show any difference in the characteristic parameters of the antenna (gain, directivity, etc.).

Antenna	Center Frequency (GHz)	Bandwidth (GHz)
1 GHz	1.01	0.16
2.45 GHz	2.45	0.64
7 GHz	7.00	> 3

Table A-1 Monopole antenna characteristics from simulations

Antenna	Impedance Real part (ohms)	Impedance Imaginary Part (ohms)
1 GHz	36.25	6.25
2.45 GHz	42.94	7.13
7 GHz	46.42	6.23

Table A-2 Input impedance of the monopole antennas at resonance from simulations

Antenna	Impedance Real part (ohms)	Impedance Imaginary Part (ohms)
Impedance (ohms)	42.94+j7.13	38.77+j 7.90
Directivity	5.2dBi	4.2dBi
Radiation Pattern	For the non-ideal case, the maximum directivity is at $\theta < 90^0$ and it leans toward $\theta = 90^0$ as the size of the ground plane grows.	

Table A-3 Simulation results comparing ideal 2.45 GHz monopole vs. non-Ideal

Figure A-2 illustrates the radiation pattern of an ideal 1 GHz antenna, derived by HFSS simulation. From the legend of the diagram it is clear that maximum directivity is in the plane of the ground plane ($\theta = 90^0$) and it is equal to 5.2 dBi, which is very close to the value predicted by theoretical calculations.

A.3 Practical Considerations and Measurements

Three designed antennas are implemented using single side FR4 clad boards as ground planes as illustrated in Figure A-3. Each antenna is made of a brass rod, as it is easy to solder. Feeding is done through an SMA connector soldered to the ground plane as shown in Figure A-4. The size of the board is 10 cm by 10 cm. The length of the antenna was chosen to be longer than needed. Then it was sanded so that the antenna reached the required resonance frequency. The length of the antennas was then compared to the designed lengths, and they matched.

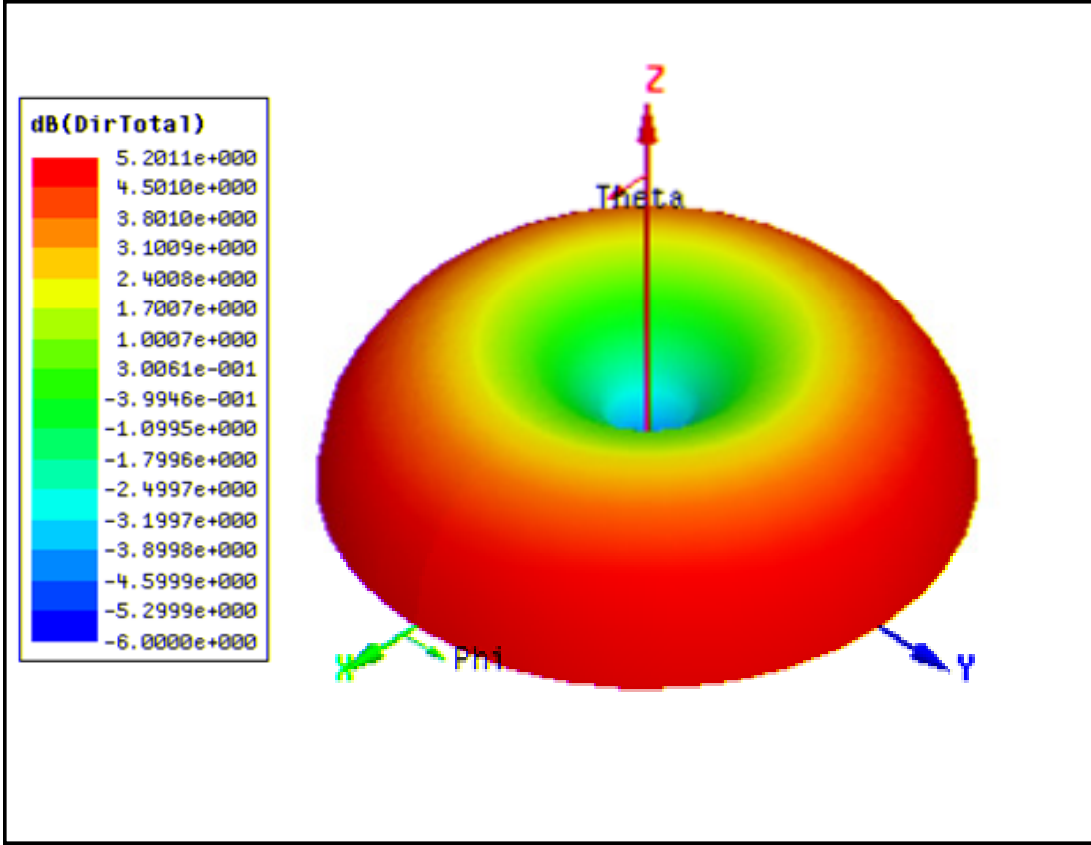


Figure A-2 Diagram of a 1 GHz monopole antenna pattern (3D view).

The center frequency was measured using a Vector Network Analyzer (VNA). This is because in a one port network, the measured scattering parameter, S_{11} , represents the reflection coefficient of that network. The bandwidth of the antenna was derived as the points at which S_{11} crosses the -10dB line. Results from these measurements are tabulated in Table A-4. Calculated values, simulation and measurement results show a great degree of agreement.

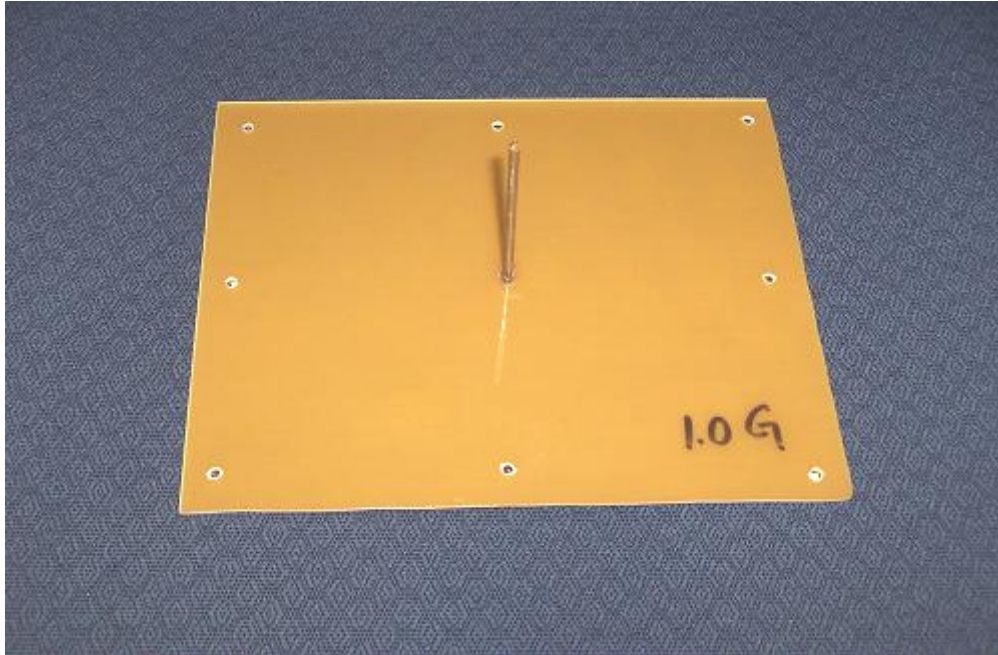


Figure A-3 Top view of the 1 GHz monopole.

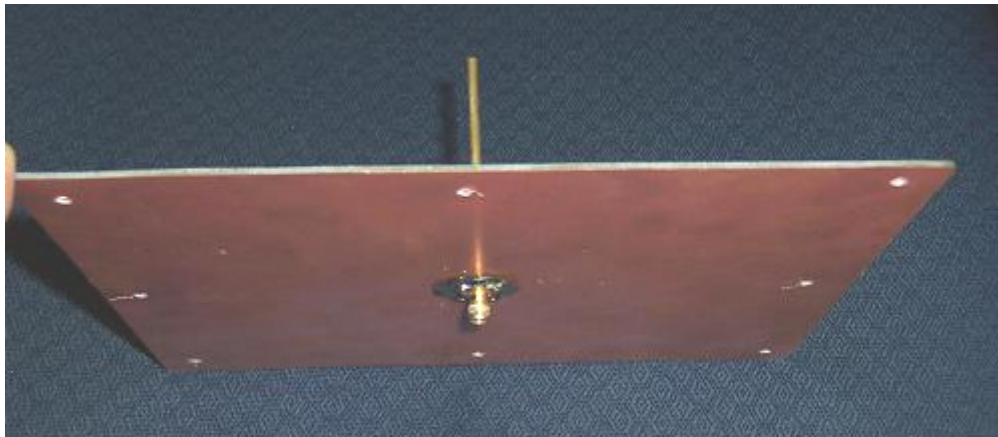


Figure A-4 Bottom view of the 1 GHz monopole showing the feed connection.

Antenna	Center Frequency (GHz)	Bandwidth (GHz)
1 GHz	1.01	0.11
2.45 GHz	2.46	0.77
7 GHz	7.01	2.96

Table A-4 Monopole antenna characteristics from measurements

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