

## ABSTRACT

Title of dissertation:           MODELS FOR RAPID ASSESSMENT OF LEADLESS  
  COMPONENT FAILURES DURING PRINTED WIRING  
  BOARD BENDING

Nathan John Blattau, Doctor of Philosophy, 2004

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The proliferation of leadless ceramic chip components has caused their failure to become a critical issue in the electronics industry. The majority of these failures are due to mechanical loads applied to the printed wiring board during assembly. The intentions of this dissertation are to demonstrate the relationship between printed wiring board flexure and the failure of leadless ceramic chip components and to develop a methodology for rapidly assessing the risk of these types of failures. To achieve this objective, closed form structural engineering based equations have been developed for calculating the loads at the critical location within the surface mount package when the underlying printed wiring board is subjected to bending. These loads are then used to calculate the stresses in the component. Validation of these stress results was done by comparing them to those of finite element models. Failure predictions using these stresses and a probabilistic failure model were then made and compared to published experimental results. The developed methodology was then physically validated with mechanical

testing and field case studies. This research identifies the physical mechanism that initiates failure in ceramic bodies attached to a glass fiber/epoxy matrix composite in a non-compliant manner, assesses the response of the mechanism to various geometries and mechanical loading conditions, and develops an analytical model that allows the user to assess risk during the design phase and to determine the root cause of field failures.

MODELS FOR RAPID ASSESSMENT OF LEADLESS COMPONENT  
FAILURES DURING PRINTED WIRING BOARD BENDING

By

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## LIST OF ABBREVIATIONS

$G$  = shear modulus

$h$  = solder joint height

$\delta$  = displacement

$\varepsilon$  = tensile strain

$\sigma$  = tensile stress

$y$  = deflection of the beam (length)

$\theta$  = slope of the beam (radian)

$M$  = bending moment of beam

$E$  = modulus of elasticity

$I$  = moment of inertia (length<sup>4</sup>)

$\nu$  = Poisson's ratio

$L$  = length of beam (length)

## CHAPTER 1 INTRODUCTION

### 1.1 Research scope and objectives

The purpose of this dissertation is to evaluate the response of the leadless surface mount structure and its interaction with the printed wiring board during a bending event.

Evaluating the response provides the stresses or strains that determine when the component structure will fail by overstress. To achieve this objective, this dissertation concentrates on analytical stress model development and the corresponding failure models. The output of the analysis will be the maximum stress and the probability of failure of a component, for a given applied printed wiring board moment. The models are developed and implemented so that a rapid analysis can be conducted.

As time to market and costs are forced to decrease, the ability to conduct complex analyses is greatly reduced and many companies are unwilling to invest the money or time necessary to conduct them. However, not doing anything can incur significant costs if problems occur. Rapid assessment of component durability will provide an inexpensive alternative. The following steps were taken to develop the rapid assessment model:

1. Develop a general analytical method to identify the forces and moments in the component due to the effects of printed wiring board bending.
2. Develop a methodology for converting these loads into the stresses present in the component
3. Determine the difference in values obtained from complex finite element analyses to values from the rapid closed form analytical equations

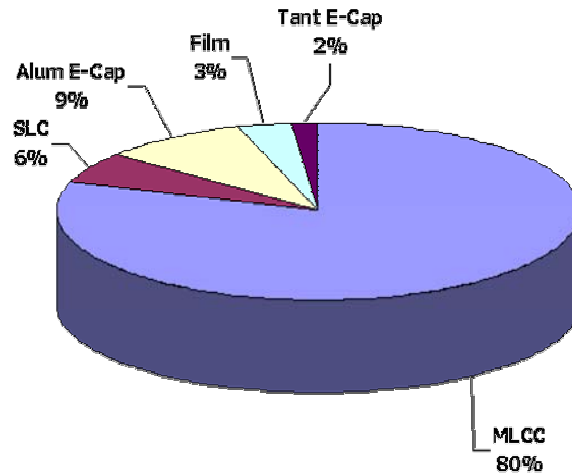
4. To provide parametric studies to determine the effect and relative severity of several parameters.
5. Predict the overstress limit for a component under a bending event and to compare the values obtained in the analytical methodology to experimental and field results.

## **1.2 Motivation**

Component failure due to the application of mechanical loads during board bending has become a critical issue in the electronics industry and is being driven by current and future trends in circuit design. The primary reason has been the proliferation of leadless ceramic components. As the demand for more complex and denser electronics increases, manufactures are forced to use small surface mount devices. Leaded components provide too large a footprint and cannot meet the input/output demands of most designs. These leads, which once served to facilitate manufacturing and accommodate thermally induced mismatches, are no longer present, yielding a much stiffer assembly. This added component stiffness has shifted some of the focus from thermo-mechanical induced degradation to failures of leadless devices due to pure mechanical loading or printed wiring board bending. The most common surface mount components are ceramic leadless capacitors and resistors.

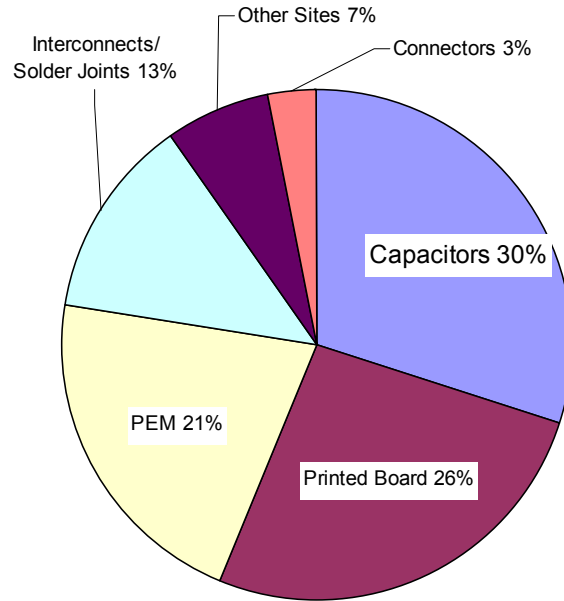
A typical cell phone can contain upward to 1000 surface mount components, with twenty times more surface mount passives (capacitors, resistors, etc...) than active components

[3]. Of the capacitors used, the multilayer leadless ceramic chip capacitor (MLCC) is by far the most common, as shown Figure 1-1.



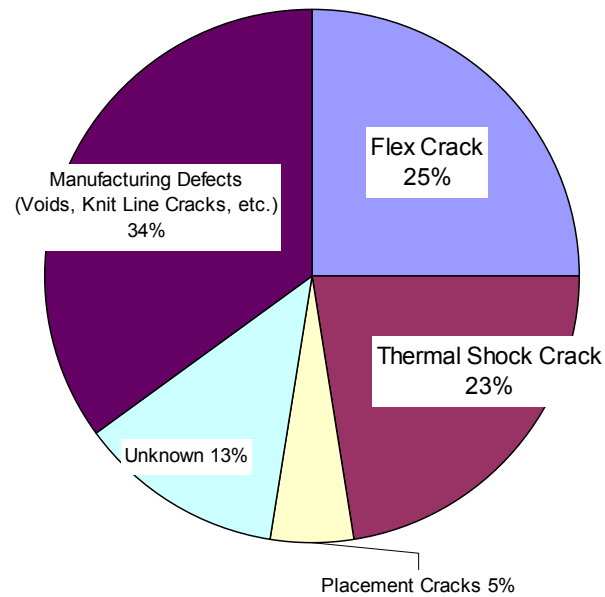
**Figure 1-1: Capacitor types used in electronics [4]**

The presence of such a large number of these components makes the reliability of most assemblies highly dependent on these devices. To better understand the influence of surface mount passives on failures in electronics, a review of 159 failure analyses performed by CALCE Laboratory Services, was conducted. These failures, representative of over 70 companies, were grouped by failure site and the results are shown in Figure 1-2. The most common reason for these failures was the non-functionality of a component (specifically, capacitors). Further review identified the overwhelming majority of failures as MLCCs. This is not unexpected because of the commonality of MLCCs, as displayed in Figure 1-1.



**Figure 1-2: Field failure occurrences by failure site [1]**

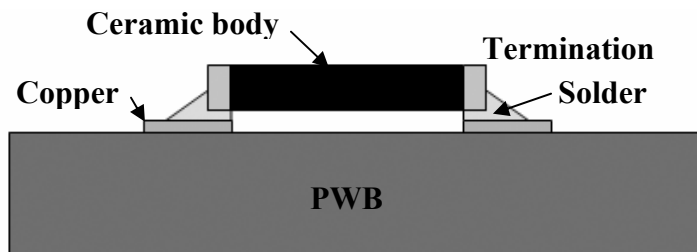
Failure studies of these ceramic capacitors were further broken down by root cause, or mechanism, by which the failures occurred. As shown in Figure 1-3, the majority of the failures were attributed to capacitor manufacturing defects. However, the second most common, which accounted for 25% of the failures, was cracking of the ceramic capacitor due to excessive flexure (or bending) of the printed wiring board. According to these results, the most common capacitor failures influenced by the designer or assembler were attributed to printed wiring board bending.



**Figure 1-3: Failure mechanisms in MLCCs [1]**

### 1.3 Background

A schematic of a typical surface mount passive is shown in Figure 1-4. The assembly consists of a leadless component on top of a printed wiring board with a solder joint attaching the component to the metallization on the board.

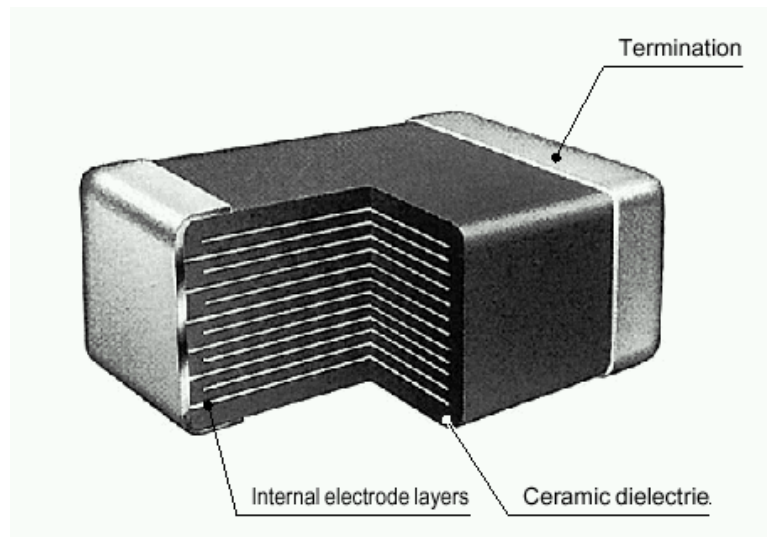


**Figure 1-4: A surface mount ceramic chip component**

Accurate failure assessments require a fundamental understanding of the architecture and materials of this structure, which includes the leadless ceramic component (capacitor and resistor), the printed wiring substrate, and the interconnect (solder).

### 1.3.1 Multilayer ceramic chip capacitor

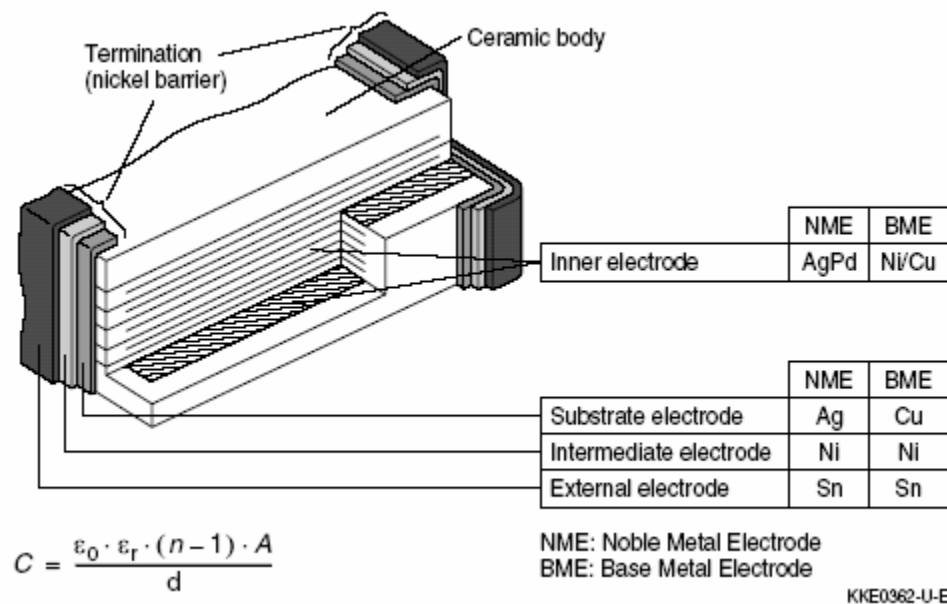
A typical multilayer ceramic chip capacitor (MLCC) is shown in Figure 1-5.



**Figure 1-5: Multilayer Ceramic Chip Capacitor**

The most common MLCCs are constructed of alternating layers of BaTiO<sub>3</sub> dielectric and metal electrodes. The internal electrodes come to the surface at the face ends of the ceramic block where an electrical contact is made to the end metal termination.

There are two general types of MLCCs based upon the metals used in their construction. The traditional noble metal electrode (NME) capacitor utilizes palladium-silver (AgPd) or palladium (Pd) for its inner electrodes. The more recent and rapidly accepted base metal electrode (BME) uses nickel (Ni) or copper (Cu) for its electrodes [5.b]. Other differences in the construction in the MLCC types are detailed in Figure 1-6.



**Figure 1-6: Detailed ceramic capacitor construction [5]**

There are different categories of dielectric that depend on the variation in capacitance as a function of temperature. Three of the most popular barium titanate based dielectrics are shown in Table 1.



**Table 1: Common capacitor dielectric designations [50]**

EIA designation	Class	Temperature range (°C)	Barium Titanate content (%)	Other dopants	Typical grain size (µm)
C0G (NPO)	1	-55 to 125	10-50	TiO <sub>2</sub> ,CaTiO <sub>3</sub> , Nd <sub>2</sub> Ti <sub>2</sub> O <sub>7</sub>	1
X7R (BX)	2	-55 to 125	90-98	MgO,MnO,Nb <sub>2</sub> O <sub>5</sub> , CoO Rare-earth	<1.5
Y5V	2	-30 to 85	80-90	CaZrO <sub>3</sub> , BaZrO <sub>3</sub>	3-10

### 1.3.2 Surface mount ceramic chip resistor

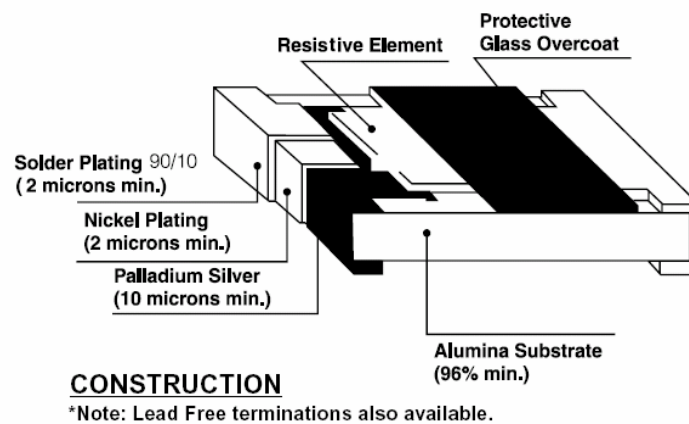
Resistors are typically the second most numerous parts used in electrical circuits. The surface mount ceramic chip resistor is a leadless device that is composed of a ceramic substrate supporting a resistive element. The substrate is a high purity alumina with the material properties shown in Table 2. The resistive element can either be a thick film or a thin film depending on the accuracy and power dissipation required.

**Table 2: Physical properties of alumina ceramic**

Physical Constant	Al <sub>2</sub> O <sub>3</sub> (99.8%)
Elastic Modulus	337000 MPa [10]
Tensile Strength	220 MPa [11]
Bending Strength	410 MPa [11]
Coefficient of Thermal Expansion	7.8 x 10 <sup>-6</sup> 1/°C [11]
Fracture Toughness	4.56 – 5.01 [10]

### 1.3.2.1 Thick film resistor

The thick film resistor uses a resistive paste that is screen printed onto the substrate and then fired. The paste is typically composed of metal oxides, glass and solvents. The resistance is varied by the composition of the paste, the amount of paste, and by limited laser trimming. This typically makes achieving high tolerances difficult (<0.5%). The basic construction of a thick film resistor is shown in Figure 1-7.

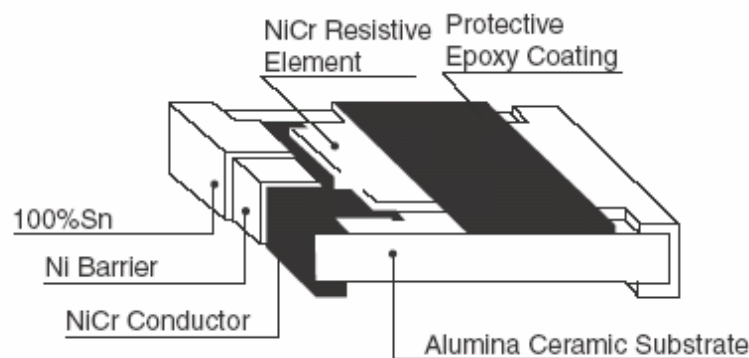


**Figure 1-7: Thick film resistor [6]**

### 1.3.2.2 Thin film resistor

The thin film resistor uses a metal film based resistive element that is deposited onto the substrate. The element is usually a nichrome (NiCr) or tantalum-nitride (TaN) film.

Resistance of the film is determined by patterning, thickness and laser trimming. The resistance can also be controlled by baking the element, which increases the oxide thickness and therefore the resistance [9]. The basic construction of a thin film resistor is shown Figure 1-8.



**Figure 1-8: Thin film resistor [7]**

### 1.3.3 Printed wiring board

The printed wiring board (PWB), also known as a printed circuit board (PCB) is the substrate to which the electronic components are mounted. The most common PWB is called FR-4<sup>1</sup>. FR-4 is composed of continuous glass fibers embedded in an epoxy resin matrix. The PWB supports the mechanical and electrical connections of the components

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<sup>1</sup> FR stands for flame retardant

and provides a thermal path for power dissipated by the components. Two distinct configurations of connections are predominant; thru-hole and surface mount. A through hole interconnect uses a hole in the PWB through which the lead of the component is passed and then attached. A surface mount interconnect does not require a hole in the PWB and the component is attached directly to a bond pad on the surface of the PWB. This allows for closer component spacing and does not disturb conductors that may be routed underneath the component in different layers. The most popular material used to attach the component to the PWB is solder.

#### 1.3.4 Solder

The most common solder used today is a eutectic combination of 63% tin and 37% lead. The melting temperature is around 183°C and tin-lead solders have good wetting characteristics and low cost. Solder is stencil printed onto the printed wiring board in a paste form. This paste is composed of the solder (in sphere form) and the flux. The flux is designed to remove organics, breakdown oxides and decreases the surface tension of the solder to insure good wetting. The material properties for 63Sn37Pb solder are shown in Appendix 10.2.1.

### **1.4 Literature review**

The work that relates the failures of ceramics due to printed wiring board bending coincides with the acceptance of using surface mount components on organic based substrates in the mid-eighties [15]. Before this, surface mount devices were typically only used on ceramic substrates and actual failures due to bending were quite rare.

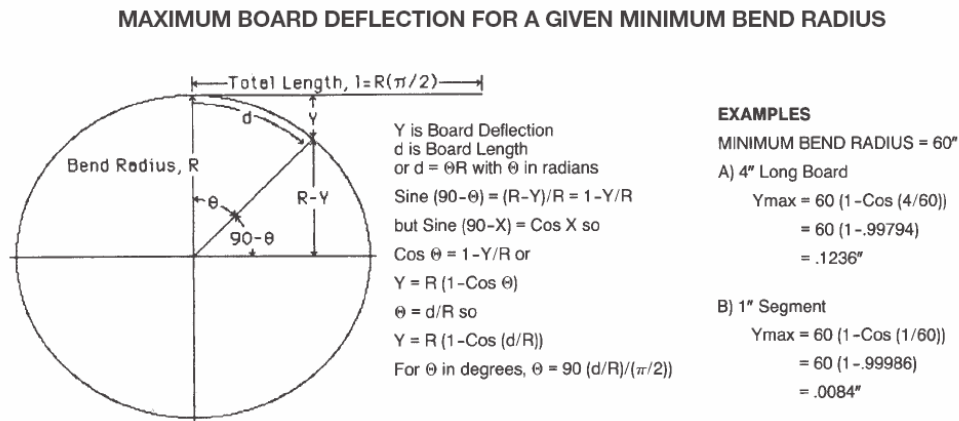
Instead most publications that evaluated cracking in capacitors tended to focus on those driven by thermal shock conditions. One of the first papers to address the structural reliability of leadless ceramic components on an organic substrate was written by Cozzolino and Ewell in 1980 [51].

The paper was the first to apply a physics of failure based approach to capacitor cracking. Critical material properties were measured through a variety of experimental techniques, including indentation to calculate fracture toughness, strain gages to measure residual strains, and ultrasonic methods to obtain elastic properties. Cozzolino also provided a basis for applying fracture mechanics through the use of finite element stress analysis and the calculation of stress intensity factors [54]. However, the paper did not directly address the relationship between substrate flexure and failures but instead focused on crack initiation and growth due to thermal shock.

Work by McKinney and Rice [17] in 1986 investigated the failure characteristics of surface mount capacitors. The study provided valuable data on the fracture behavior and mechanical properties of ceramic capacitors but did not extend the results to bending failures of capacitors on a substrate.

The paper “Cracks: The Hidden Defect” [16] written in 1988 by John Maxwell was one of the first to provide semiqualifiable guidelines to preventing capacitor failures due to substrate flexure. The study covered the morphology of cracks caused by thermal shock, pick and place, and board bending. It also provided guidelines on how components

should be located on a board to minimize failures to due board bending. However, the guidelines were relatively broad, based only on a geometric interpretation of bending. This interpretation is shown in Figure 1-9. Using this approach, Maxwell recommends that the minimum board radius of curvature should be greater than 60 inches to avoid flex cracking. The source of this recommendation was not provided.



**Figure 1-9: Geometric interpretation of board bending [16]**

Work done by Condra [23] in 1992 addressed the failures of ceramic chip capacitors on alumina substrates. Environmental issues such as vibration and thermal cycling were investigated as a possible cause of capacitor cracking. The study was limited to fractional factorial experimental testing that investigated the effects of various parameters on capacitor failures. These parameters included manufacturer, soldering technique, and conformal coating, as well as temperature, humidity and vibration. The testing indicated that vibration when combined with temperature cycling could increase the number of failed ceramic capacitors. However, due to the lack of failure analysis, cracking as the root cause of these failures could not be confirmed. In regards to flex cracking, no

guidelines were suggested, though the work did indicate that rework of the capacitors could greatly influence failure rates.

The next major study involving capacitor cracking was conducted by Prymak and Bergenthal of Kemet Electronics in 1995 [21]. They conducted numerous 3 point bend test experiments on ceramic capacitors and provided a statistical analysis of the results. The report contains data on the behavior of the capacitors during flex testing and the probability of failure for two sizes of capacitors, 0805 and 1206, on a 1.6 mm thick printed wiring board. This effort resulted in the first rudimentary attempt at a failure model, with the authors providing a probability of failure due to flex cracking as a function of displacement.

Panchwagh and McCluskey [22] investigated the internal stresses generated in ceramic capacitors during wave soldering. Using finite element analysis they investigated the effects of capacitor dimensions on the capacitor stresses incurred during wave soldering. The research did not extend into flexural cracking of the capacitors.

One of the first papers that focused on predicting component failures due to substrate bending using numerical modeling was written by Franken et al [18]. The study covered a series of experiments and the attempts to model the failure behavior using finite element analysis. The report contains data on the materials and properties that make up a ceramic capacitor, the effect that increased solder joint thickness has on the failure probability of the capacitor during bending and the potential effects that residual stresses

can have on the failure probability. Example, the authors did not correlate any other parameters to the failure probability of the device.

Literature on the behavior of ceramic surface mount resistors during printed wiring board bending does not seem to exist. Searches using INSPEC, IEEE Xplore and FirstSearch did not yield any articles with regards to mechanical failures of resistors. This is not surprising, due to their mechanical makeup, since the ceramic used in resistors has higher fracture strength than the ceramic used in capacitors. Therefore, more severe bending events are required for crack initiation. In addition, the functional aspect of the resistors is typically located on the top of the component, as opposed to the interior of the component, as with ceramic capacitors. With the classic morphology of flex cracks, this effectively removes the functional area of the component away from the crack path. Resistors with cracked substrates can be fully functional, unless the crack fully propagates through to the top of the device.

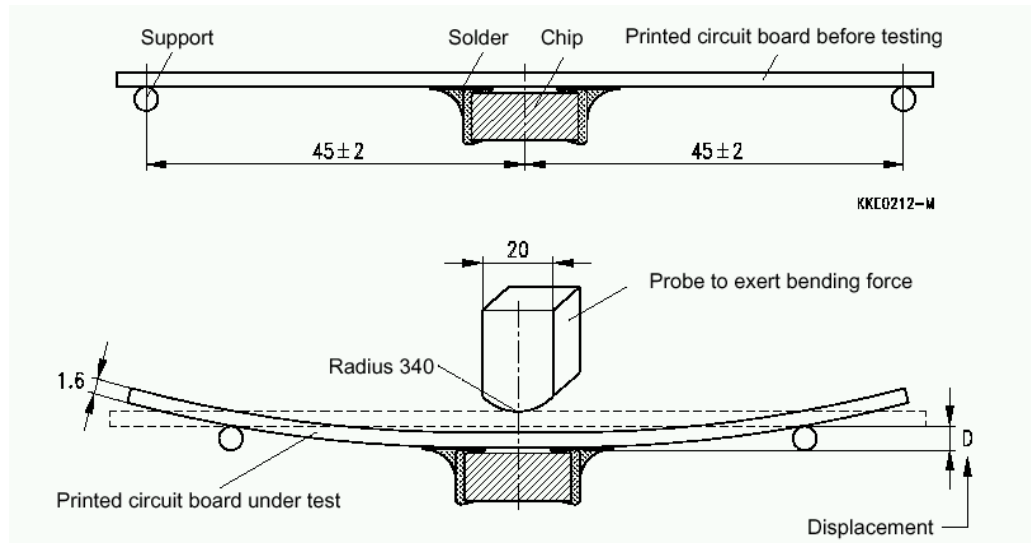
## **1.5 Industry response**

### **1.5.1 Capacitors**

Many ceramic capacitor manufacturers recognize the potential of failing ceramic capacitors when the printed wiring board is subjected to bending. The response from industry has involved numerous manufacturer publications to address the problem. Included in these papers are general guidelines with regard to placement and orientation of the capacitors on the board to minimize the potential of bending failures. There has also been industry sponsored standards developed to provide guidelines on how to assess



the robustness of capacitors during board flex events. The tests involve soldering a capacitor to a 90 mm x 40 mm x 1.6 mm thick FR-4 test coupon. The coupon is then subjected to a three point bend test as shown in Figure 1-10.



**Figure 1-10: EIA-J RC 3402 [22]**

This is a qualification type test and the board is deflected to the desired level and the capacitor is tested while the board is in the bent state. Passing of the test is accomplished if there are no visible cracks and the capacitance has not varied by more than a specified amount (classification dependent). Some standards for the test method are:

1. AEC-Q200, Automotive Electronics Council (2 mm deflection)
2. EIA-198D / PN-2271 (United States) (2 mm deflection)
3. IEC 384-10 4.35 (Europe)
4. EIA-J RC 3402 (Japan)

Unless noted, the tests do not specify the deflection of the device. This is left up to each manufacturer. Most manufacturers usually specify that their components can pass either a 1 mm or a 2 mm deflection limit. Some major manufacturers and their deflection limits are shown in Table 3. Manufacturers not listed do not publish a deflection limit.

**Table 3: Manufacturer deflection specifications**

Manufacturer	Deflection Specification		
	1 mm	2 mm	Other
AVX [30]		X	X <sup>2</sup>
Vishay [32]	X		
SAHA/Susco Components [26]		X	
Cal-Chip Electronics, Inc. [27]		X	
TDK [25]		X	
EPCOS [5]		X	
Kemet [34]		X	
MuRata [31]	X <sup>3</sup>		
Nippon Chemi-Con [28]	X <sup>4</sup>		
Samsung Electro-Mechanics [29]	X		

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<sup>2</sup> AVX offers a soft-termination capacitor with a deflection limit of 5 mm

<sup>3</sup> GRM03, GRM15 capacitors, PWB thickness 0.8 mm

<sup>4</sup> Printed wiring board thickness 1.0 mm (1.6 is the standard)

Syfer, Novacap [43]		X	X <sup>5</sup>
Johanson Dielectrics [43]	X <sup>6</sup>		X <sup>7</sup>
Panasonic [39]	X		
Philips, Phycomp, now Yageo [36]	X		
KOA Speer Electronics [35]		X	
Maruwa America [37]		X	X <sup>8</sup>
Taiyo Yuden [38]	X		
Walsin Technology Corp. [39]	X		

### 1.5.2 Resistors

The electronics industry has developed standards to verify the robustness of surface mount resistors. The common test for surface mount resistors is JIS-C-5202, Para.6.1.4 [42]. The test setup is identical to that shown in Figure 1-10 except that the specified deflection is 5 mm and the ram radius is 240 mm. The ram radius is decreased to allow for greater deflections to be applied to the board.

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<sup>5</sup> Syfer offers a polymer-termination capacitor with a deflection limit of 5 mm

<sup>6</sup> NPO class dielectrics

<sup>7</sup> X7R, Deflection specification 0.5 mm on FR-4

<sup>8</sup> Flexion termination, 8 mm deflection

## 1.6 Summary

A method for predicting the failure of ceramic chip capacitors and ceramic chip resistors is clearly needed. The number of failures of these devices is high when compared to other component level failures. Manufacturers have provided basic placement guidelines that may be used to minimize flex cracking. They have also typically provided the deflection limit at which their product can be safely used. This deflection limit may be a useful metric for comparing manufacturers, but it does not provide a designer with information on the flexure that the capacitor can survive in his application. Very few manufacturers publish the actual failure data and they also do not adequately address the effects of geometric parameters, such as board thicknesses, on the failures during printed wiring board bending.

The purpose of this study is to develop an analytical model to predict the failures of ceramic chip capacitors and resistors when they are subjected to a printed wiring board event. The analytical model can provide a rapid method by which:

1. The robustness of the an electronic design can be assessed with regard to the mechanical failures of resistors and capacitors
2. Root cause of failures can be conclusively identified based upon printed wiring board strain readings

## **CHAPTER 2 LEADLESS CHIP DEVICE STRESS MODELS**

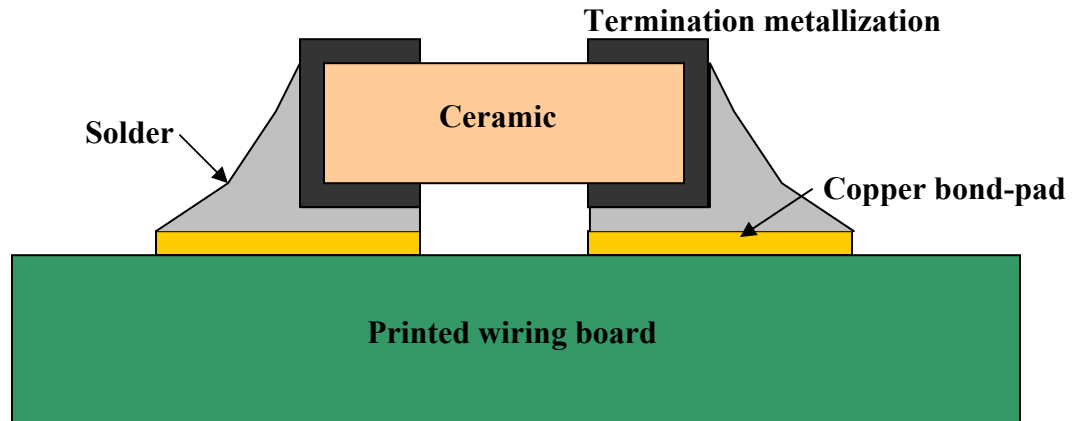
In this chapter, an analytical model is developed to predict the stresses developed in leadless ceramic chip capacitors and resistors (LCC/LCR) during board flexure. The model will convert printed wiring board deformation into the forces applied to the part.

Thus, the purposes of this chapter are:

- (1) To derive an analytical method for characterization of the forces and moments in terms of the geometric, material, and load parameters of the PWB
- (2) To determine the maximum loads and stresses within the leadless chip device

### **2.1 Analytical stress model for ceramic chip capacitors and resistors**

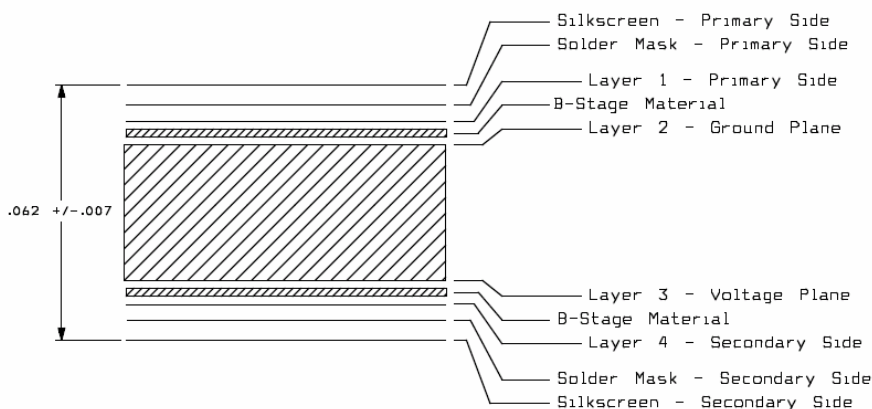
A structural engineering approach is used to develop the analytical model for determining the stresses in the device. As shown in Figure 1-5, Figure 1-7 and Figure 1-8 the structures of surface mount resistors and capacitors are similar. Therefore, one analytical stress model should be able to predict the stresses for either device. However, some simplification of the structure is necessary for modeling. This is shown in a two dimensional representation of the device in Figure 2-1.



**Figure 2-1: 2D representation of LCC/LCR structure**

### 2.1.1 Assumptions

There are some necessary assumptions that must be made in order to reduce the structure to the point that an analytical model can be developed. The component body is assumed to be homogenous. The printed wiring board will have effective properties based upon the number and location of full internal layers (voltage/ground planes). These calculations are based upon weighted averaging and the parallel axis theorem [74]. The stack up of the printed wiring board is assumed to be symmetric. an example of a board stack-up is shown in Figure 2-2. Therefore, the centroid of the pwb will always be assumed to be one half the thickness of the board.



### **Board Stack-Up** **4 Layer**

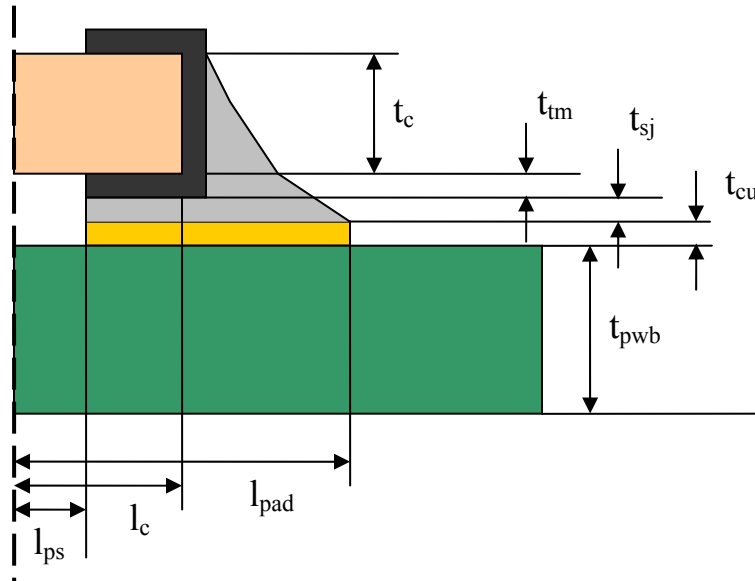
**Figure 2-2: Example board stack-up**

The initial assumption was that the members of the complete structure (component, solder, board) could be represented as beam type elements. This may introduce some error in the results as the elements are relatively short and their behavior may not be accurately predicted with simple beam equations because of excessive shear deformations. The accuracy can be increased by accounting for the shear, which is typically ignored in beams. The analytical stress model will also assume that the solder joint intersects the capacitor in the center of the capacitor termination (bandwidth<sup>9</sup>), which in this case reduces the capacitor length by 50% of the end metal termination. Furthermore, a 2-D planar representation is also assumed. This will cause some error to be introduced because any edge effects between the board and component will be

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<sup>9</sup> This is the length of the end metallization of the device

ignored. The amount of the error and necessary calibration factors will be determined using a finite element models. The geometric parameters shown in Figure 2-3 will be incorporated into the analytical model.



$t_c$  – thickness of the device

$t_{tm}$  – thickness of the device end metallization

$t_{sj}$  – solder joint thickness

$t_{tm}$  – copper bond pad thickness

$t_{cu}$  – thickness of the printed wiring board

$t_w$  – width of the device

$l_{ps}$  – bond pad separation

$l_c$  – length of the device

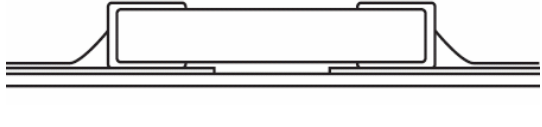
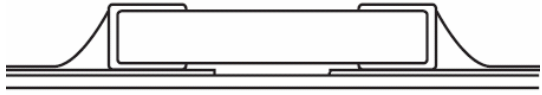
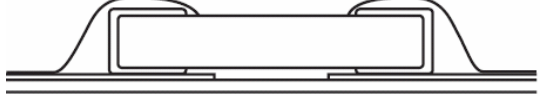
$l_{pad}$  – bond pad length

**Figure 2-3: Geometric parameters for analytical model**



Additionally, the model should account for the shape of the solder fillet. There are three general classifications of the solder joint, as shown in Table 4.

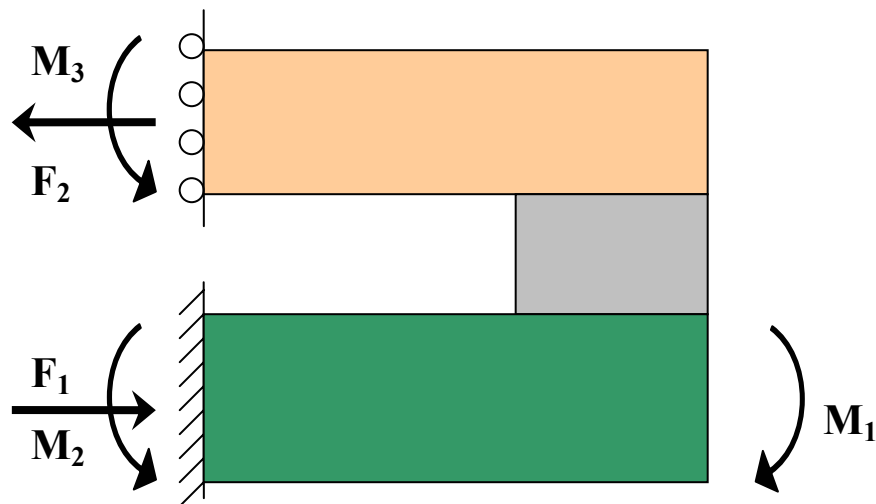
**Table 4: Solder joint shape classifications**

Starved	
Nominal	
Bulbous	

The main difference in the joints is the height at the end of the component. The starved joint will have this height assumed to be half the component thickness. The nominal joint will have this height set as 0.7 times the component thickness. The bulbous joint will have the height set as 1.0 times the component thickness. These three heights will be used to calculate a change in solder area that reflects the different stiffness of each type of joint.

### 2.1.2 Stress analysis technique, stiffness method

Based upon the assumptions, detailed previously, and the free body diagram in Figure 2-4, which indicates that the structure is over constrained and indeterminate, an appropriate analysis was chosen.



**Figure 2-4: Free Body Diagram**

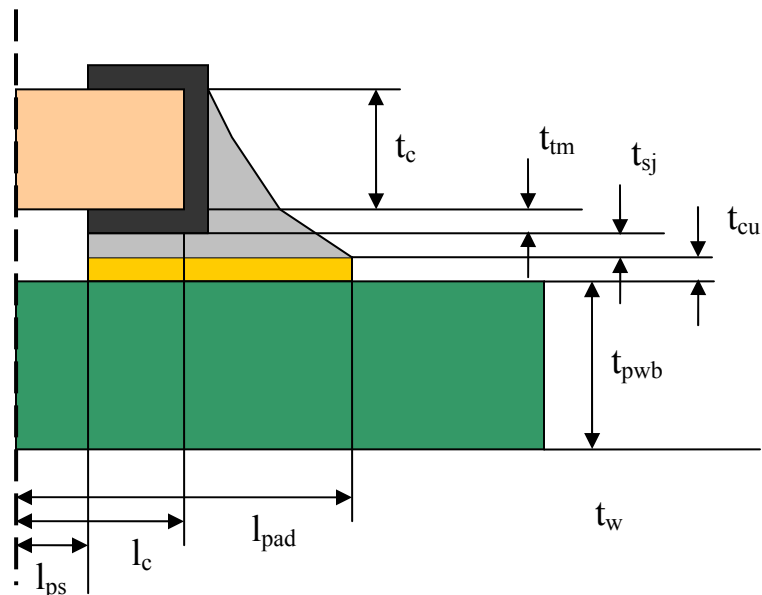
Many methods are available for solving such structures, most of which are variations of the stiffness method or displacement method. The stiffness method is well documented and is also known as the Finite Element Method. The stiffness method utilizes these basic steps [75]:

- Partitioning the structure into a series of discrete elements
- Formulating the stiffness matrix for each element
- Assembling the global matrix from the local stiffness matrices
- Applying the boundary conditions to obtain the reduced stiffness matrix

- Inverting the reduced stiffness matrix
- Multiplying this matrix with the force matrix to get the displacements of the nodes
- Post-processing to obtain the stresses and strains of each element

### 2.1.3 Stiffness method, Model development

The following example was used to demonstrate the development of the analytical stress model to predict LCC/LCR bending overstress failures. This example is of a 1206 size device that is soldered to an FR-4 printed wiring board with the parameters shown in Figure 2-5 and Table 5. The matrices and equations used can be found in Appendix 10.5.



$t_c$  – 0.68 mm (thickness of the device)

$t_{tm}$  – 0.010 mm (thickness of the device end metallization)

$t_{sj}$  – 0.065 mm (solder joint thickness)

$t_{tm}$  – 0.035 mm (copper bond pad thickness)

$t_{cu}$  – 1.575 mm (thickness of the printed wiring board)

$t_w$  – 1.524 mm (width of the device)

$l_{ps}$  – 1.024 mm (bond pad separation)

$l_c$  – 1.524 mm (length of the device)  $l_{pad}$  – 2.024 mm (bond pad length)

Solder joint type - nominal

**Figure 2-5: Example structure**

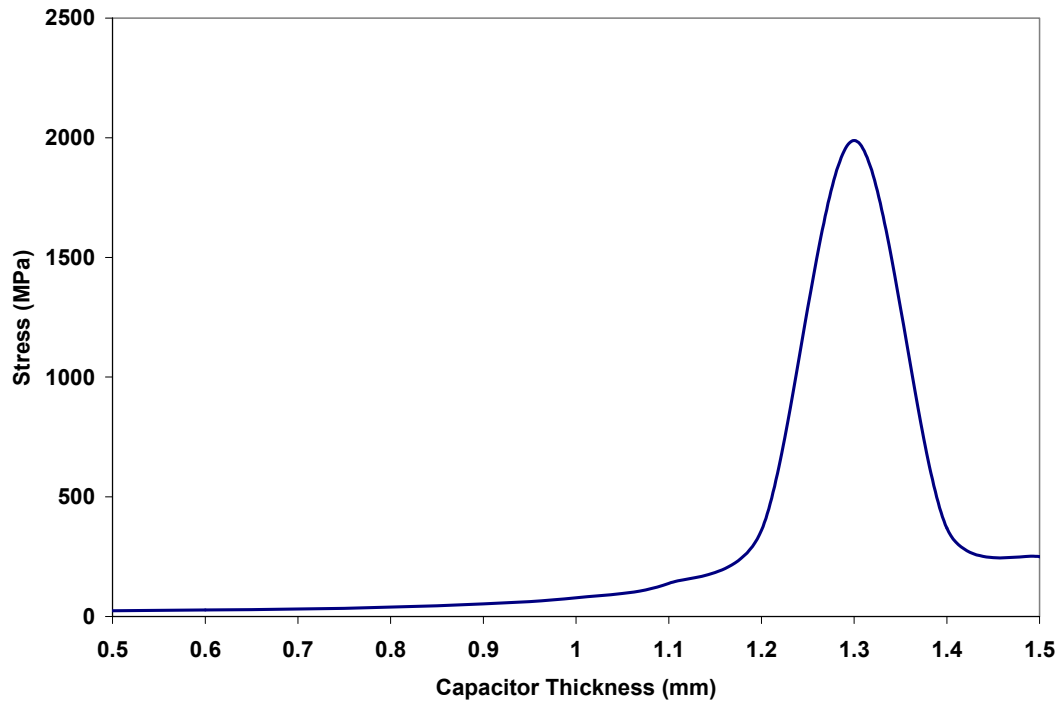
**Table 5: Material properties**

<b>Material</b>	<b>Description</b>	<b>E (GPa)</b>
Ceramic X7R	Capacitor Body	110[18]
FR-4	Board	17 [Appendix 10.2.2]
Solder PbSn	Attachment	26 [47]
Tin/Copper	End metallization	100 [18]
Copper	Bond pad	120 [18]

#### 2.1.4 Model performance

The analytical model was then exercised to characterize its behavior and performance for different sized devices. The first device investigated is a 0805 size ceramic capacitor.

The study involves plotting the stress output of the model as various geometric parameters of the device were changed. The first parameter modified is the capacitor thickness, which was varied between 0.5 and 1.5 mm. The results of the model with an applied moment of 100 N·mm are shown Figure 2-6.

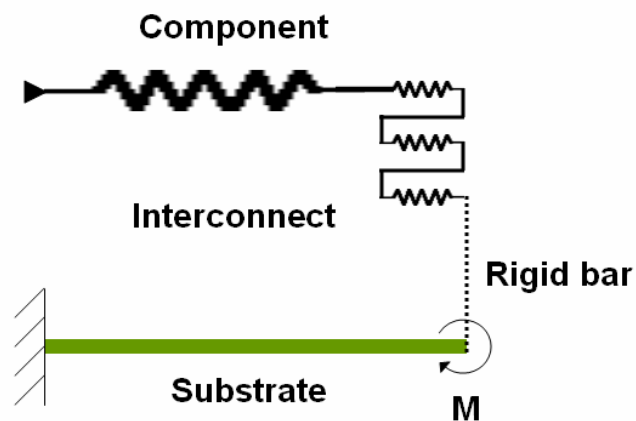


**Figure 2-6: Capacitor tensile stress as a function of capacitor thickness**

As shown in the graph, the model exhibits an unusual behavior over a specific range of device thickness. This behavior is inconsistent with FEA analyses conducted in a previous study of the same geometry [2]. The problem is that the stiffness of the device is calculated with beam equations and is therefore overly sensitive to any change in thickness, as the inertia increases as a cube of the thickness. Thus, the model required reformulation to more accurately reflect the behavior of the structure.

### 2.1.5 Reformulation of analytical model

The model was reformulated to ignore the bending stiffness of the component and attach. This assumption was made from observations from previous FEA models showing that the reaction moment on the component was quite small when compared to the moment generated by the reaction forces in the structure. As shown in Figure 2-7 the component and interconnect are now replaced with spring elements. The component interconnect is modeled as a rigid bar with a series of springs. The rigid bar provides an offset so that the component and interconnect have an apparent bending stiffness.



**Figure 2-7: Model representation**

The analytical model is effectively reduced and simple cantilever beam equations are used to calculate the behavior of the structure. The leadless device is assumed to only supply additional rotational stiffness to the printed wiring board at the end of the device.

The stiffnesses that need to be calculated are those of the printed wiring board, device body, copper bond pad, solder joint, and device metallization. The stiffness for the substrate is based upon the rotational stiffness of a cantilever beam, and is the amount of moment required to rotate the beam 1 radian. The equation for the rotational stiffness of a cantilever beam under pure bending is shown in Equation 2-1.

$$K_{\theta} = \frac{EI}{L}$$

**Equation 2-1: Bending stiffness of a cantilever under pure bending**

Where E is the modulus, I is the moment of inertia and L is the length. The stiffness of the copper bond pad, solder joint, and device metallization are assumed to be under pure shear with a stiffness calculated by Equation 2-2.

$$K_s = \frac{AG}{t}$$

**Equation 2-2: Shear stiffness**

Where A is the cross-sectional area, G is the shear modulus, and t is the thickness.

The stiffness of the device is assumed to be in pure tension with a stiffness calculated by Equation 2-3.



$$K_C = \frac{AE}{L}$$

**Equation 2-3: Tensile stiffness**

This results in four stiffnesses that must be combined as springs in series, as shown in Equation 2-4.

$$K_{CS} = \frac{1}{\frac{1}{K_{C1}} + \frac{1}{K_{S1}} + \frac{1}{K_{S2}} + \frac{1}{K_{S3}}}$$

**Equation 2-4: Combining series stiffnesses**

These combined stiffnesses must now be converted to an apparent rotational stiffness at the end of the printed wiring board. This is done by determining the moment required to rotate the rigid bar one radian. This rotation must be related to the axial deformation of the device (component and attach). The relationship between rotation and axial deformation is given by Equation 2-5.

$$\tan(\theta) = \frac{\delta}{t}$$

**Equation 2-5: Rotation - deformation relation**

Where  $\theta$  is the rotation,  $t$  is half the printed wiring board thickness, and  $\delta$  is the axial deformation of the component. Using this relationship and the small angle

approximation, the rotational stiffness due to the axial deformation of the component is Equation 2-6.

$$K_{C\theta} = K_{CS} \cdot t^2$$

**Equation 2-6: Apparent rotational stiffness**

Assuming compatibility, the rotation at the end of the printed wiring board due to the applied moment is calculated by dividing the moment by the sum of  $K_{\theta}$  and  $K_{C\theta}$ . Once the rotation is computed the axial force in the component can be computed by using Equation 2-7.

$$F = \frac{K_{C\theta} \cdot \theta}{t}$$

**Equation 2-7: Axial force in the component**

The axial force is then used to calculate the component stresses.

## CHAPTER 3 MODEL CALIBRATION

In this section, the numerical results from the analytical stress model derived in the previous section are calibrated using Finite Element Analysis (FEA). The mechanical properties used are shown in Table 5. The inputs to the analytical model were based upon a nominal solder pad and the ranges of industry specified dimensions as shown in Table 6.

**Table 6: Typical capacitor types and dimensions [5,18,25,26,27,28,29,30]**

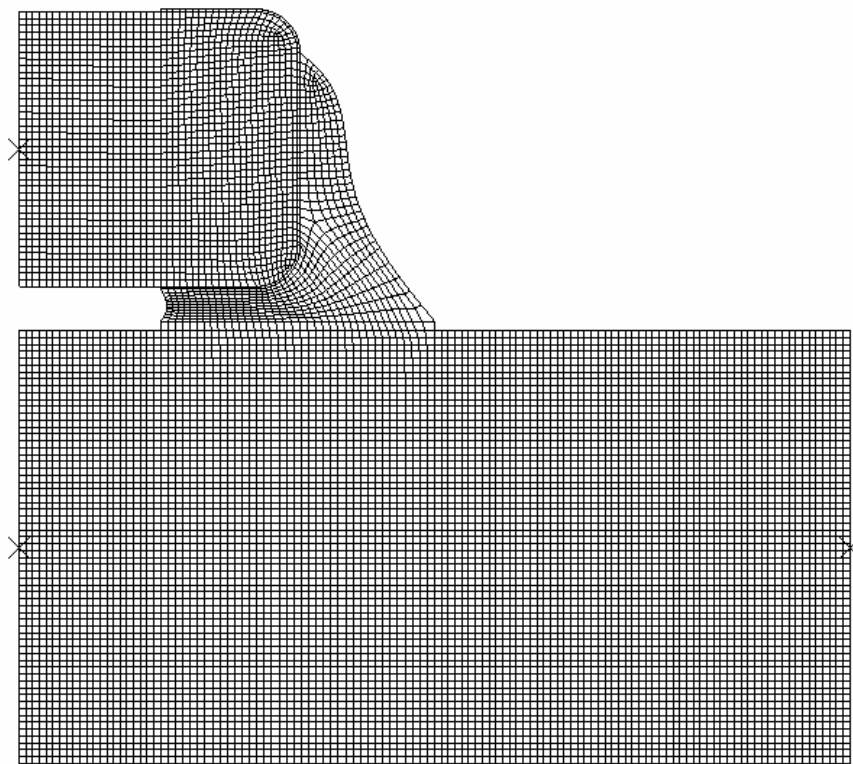
Capacitor	Length	Width	Thickness		
			Min	Nominal	Max
0805	2.01	1.27	0.50	1.00	1.27
1206	3.05	1.52	0.68	1.00	1.52
1812	4.57	3.05	0.90	1.50	1.85

The analytical stress model is calibrated using a 0805 device and will then be validated for a range of device sizes in the next section. However, before conducting a finite element analysis, a convergence study was conducted to determine the optimum element size.

### 3.1 Convergence study

One of the reasons for conducting a convergence study was to determine the largest element that could be used in a model that would still provide the desired accuracy. This

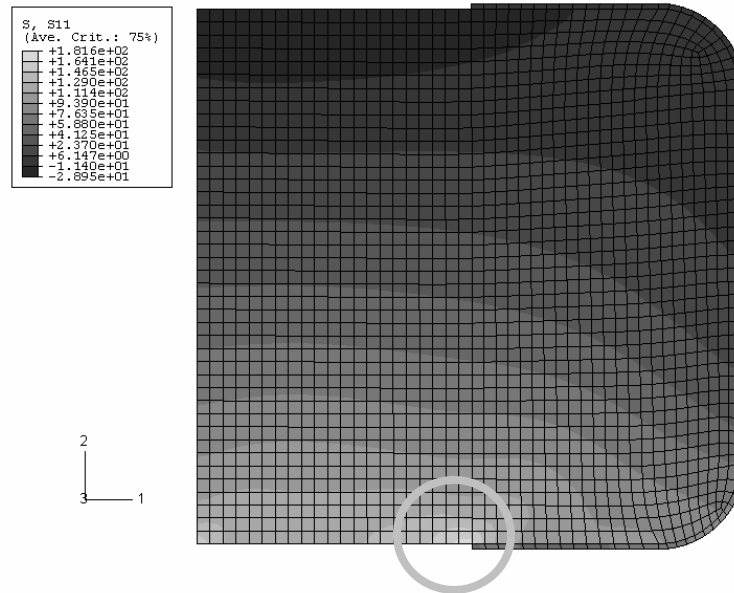
was done mainly to reduce the computational requirements of the model. As a general statement, today's computers far exceed the computational capabilities of computers just a couple of years ago and the need for conducting convergence studies has been reduced. However, they are still important in determining element size and should be conducted when doing a rigorous finite element study. The FEA model used for the convergence study was a 1.0 mm thick, 0805 size leadless device as shown in Figure 3-1.



**Figure 3-1: FEA, device model: 1.00 mm thick**

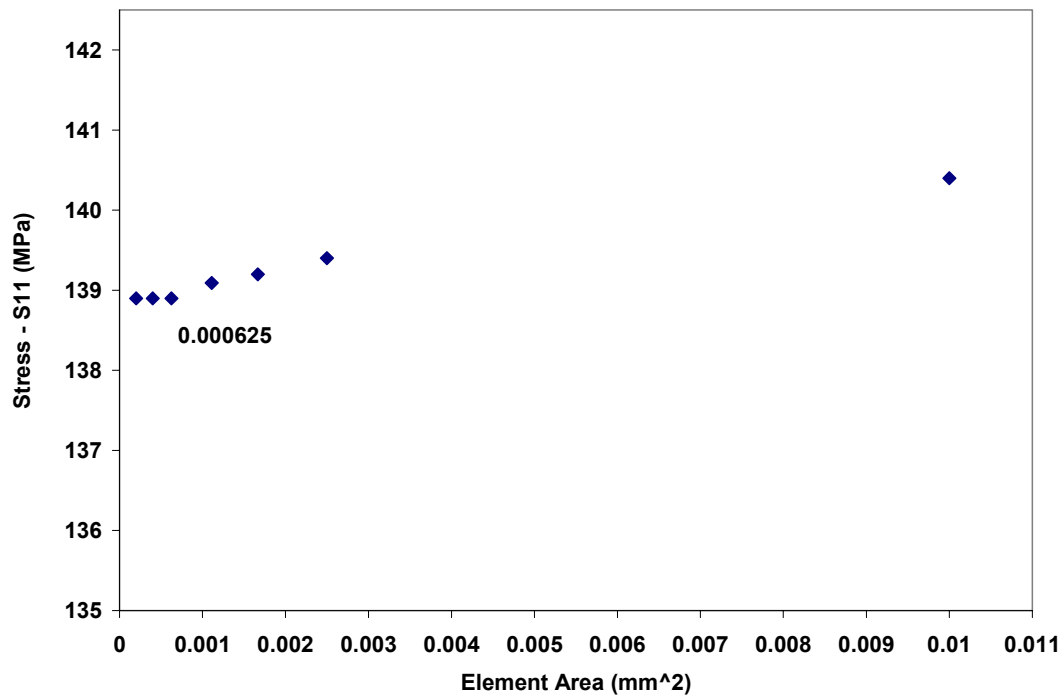
The mesh density was increased until the average stress values over the area of interest reached an asymptotic value. The region of interest is defined as the failure site. This

region is located where the end metallization terminates, as shown in Figure 3-2. A rectangular area of  $0.02 \text{ mm}^2$  is taken around this region for the stress averaging.



**Figure 3-2: Region of interest for convergence study**

Seven finite element analyses were conducted with consecutively smaller elements. The average stress in the convergence region as a function of element area is shown in Figure 3-3. The average stress decreased as the elements got smaller. This is expected as the smaller elements increase the compliance of the model. As the element area of decreased from  $0.00111 \text{ mm}^2$  to  $0.000625 \text{ mm}^2$  the changes in stress values decreased from 0.1% to less than 0.007%. Therefore convergence to less than 0.01% was determined to correlate with an element area of  $0.000625 \text{ mm}^2$  and 32 elements in the convergence region.



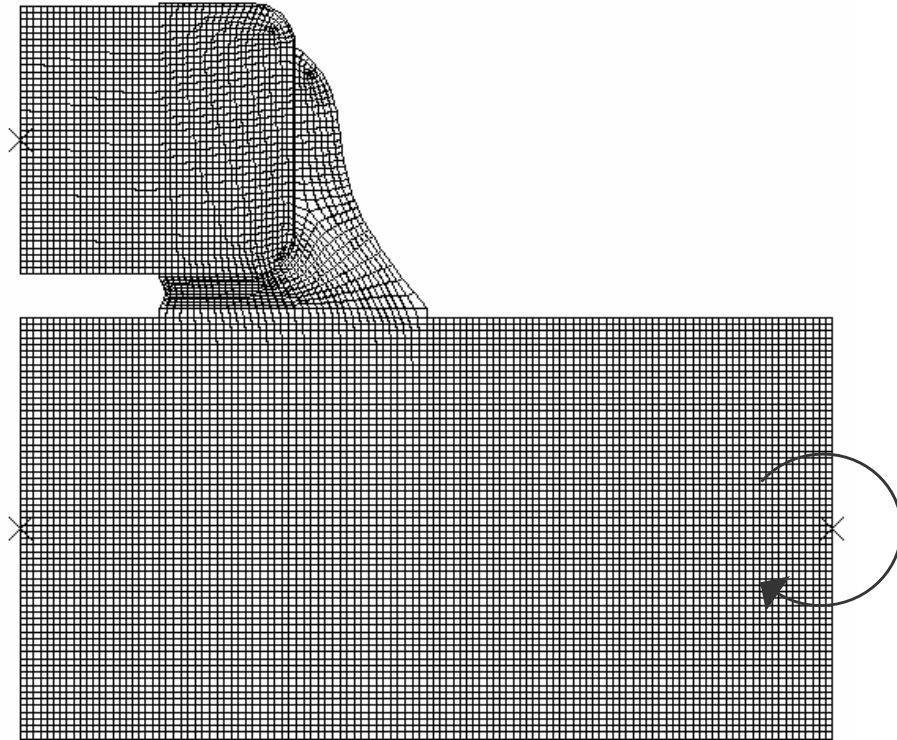
**Figure 3-3: Mesh convergence results**

Subsequent FEA models will use elements with an area equal to or less than 0.000625 mm<sup>2</sup> in the region of interest.

### 3.2 Model calibration

FEA models of a 0805 device were analyzed to develop the correction factors or modifications necessary to calibrate the analytical stress model. The nominal 0805 size capacitor is shown in Figure 3-4. This model has nominal dimensions as detailed in Table 6. The analysis assumes that all materials behave elastically. There are three rigid beams used in the model. One beam is used at the end of the board so that a moment can be applied, while the other two beams supply the symmetry boundary conditions at the

center of the device. The reference points for the rigid beams are designated by the x's in Figure 3-4. The deformed FEA model after application of the load is shown in Figure 3-6.

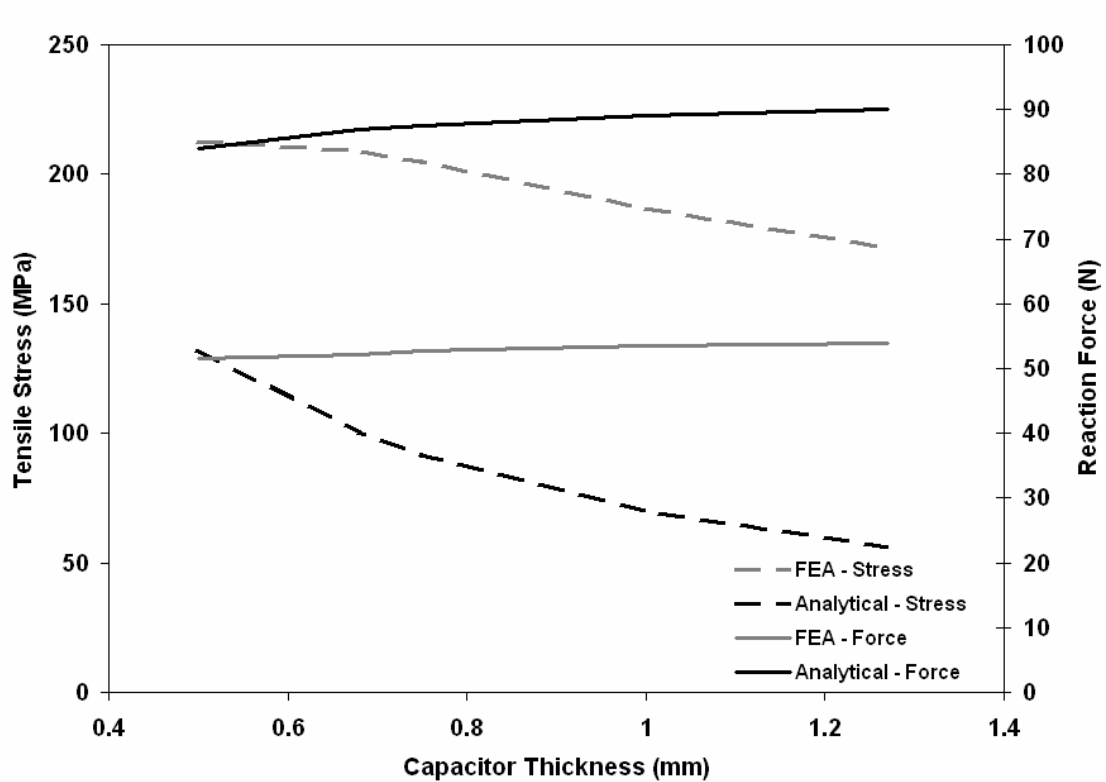


**Figure 3-4: FEA model of 0805 capacitor**

### 3.2.1 Effects of device thickness dimensions

The thickness of the capacitor in the FEA models was varied between the minimum and maximum values shown in Table 6. The maximum tensile stress for the 0805 capacitor is recorded in Table 7 at an applied moment of 100 N·mm along with the corresponding results from the analytical model. Additional thickness values were evaluated to ensure that the models did not exhibit the behavior shown in Figure 2-6.

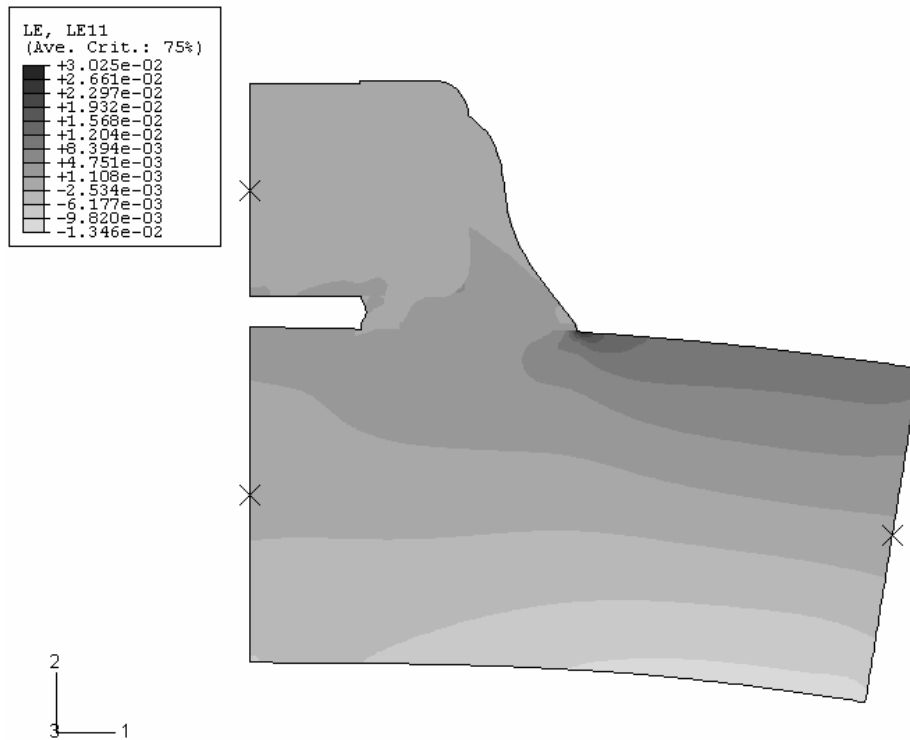
As shown in Figure 3-5, the analytical model is over predicting the reaction force of the capacitor. However, the behavior or response of the analytical model is similar to those of the FEA model.



**Figure 3-5: FEA and analytical model results**

This over prediction is due to the assumption that there is a perfectly rigid joint attaching the copper bond pad to the printed wiring board. In actuality, there is compliance in the joint because the bond pad is attached to the surface of the board. This allows shear deformation of the printed wiring board surface to reduce the forces transferred to the component.



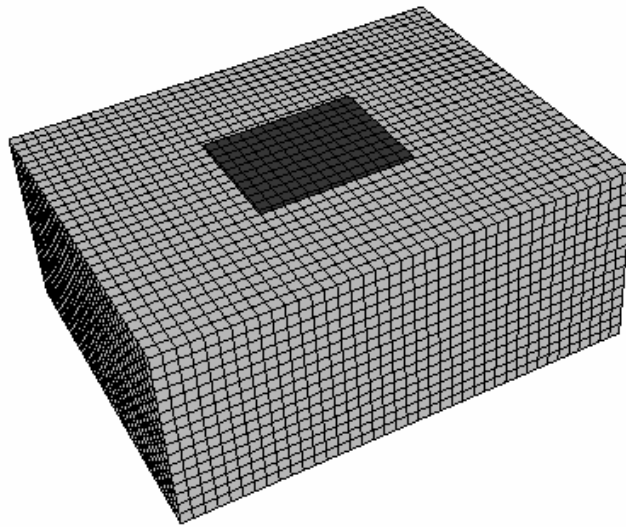


**Figure 3-6: LE11 – strain, deformation magnification 5X**

**Table 7: 0805 Analytical and FEA results**

Capacitor Thickness	FEA Reaction Force (N)	FEA (MPa)	Analytical Reaction Force (N)	Analytical (MPa)
0.5 mm	51.6	213	84	132.3
0.68 mm	52.1	209	87	100.5
0.75 mm	52.7	205	87.5	92
1.00 mm	53.5	187	89	70.3
1.27 mm	53.9	172	90	56

This shear deformation is better shown using a 3D FEA model of a shear loaded metal pad on the surface of a printed wiring board, as shown in Figure 3-7.



**Figure 3-7: 3D FEA model of pad on board (1.6 mm thick)**

Dividing the reaction force of the pad by the shear displacement will give the relative shear stiffness of the pad to board interface. An approximation of the stiffness of the board surface is the solution of a rigid disk founded on a halfspace. However, this assumes that the printed wiring board is infinitely thick, and will over predict the stiffness for thinner printed wiring boards. The basic equation for the translational stiffness of a rigid disk on a halfspace [58] is:

$$K_s = \frac{8}{2 - \nu} \cdot Gr_u$$

Where  $\nu$  is the Poisson's ratio and  $G$  is the shear modulus of the printed wiring board and  $r_u$  is the effective radius of the bond pad. This was modified by Gazetas [59] to approximate a square rigid pad.

$$K_s = \frac{9}{2 - \nu} \cdot Ga$$

Where the radius is replaced by "a" which is equal to half the pad side length. Five finite element models were analyzed to compare the effect of varying thicknesses on the stiffness. The stiffness was calculated by dividing the reaction force by the applied displacement. Comparison of this calculated stiffness with the 3D finite element model is shown in Table 8.

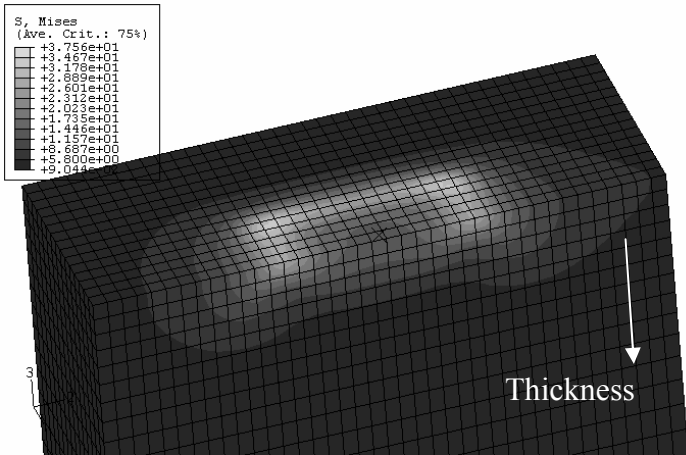
**Table 8: Rigid Square on a halfspace comparison (width 1.0 mm)**

PWB Thickness	FEA - Stiffness	Calculated Stiffness
0.8 mm	15040 N/mm <sup>2</sup>	21980 N/mm <sup>2</sup>
1.6 mm	18030 N/mm <sup>2</sup>	
3.2 mm	21190 N/mm <sup>2</sup>	
4.8 mm	22070 N/mm <sup>2</sup>	
6.4 mm	22090 N/mm <sup>2</sup>	

As shown by the table, the FEA model stiffness approaches the calculated value as the printed wiring board gets very thick. The board becomes less stiff as the thickness decreases because less board volume is available to resist the movement of the pad.

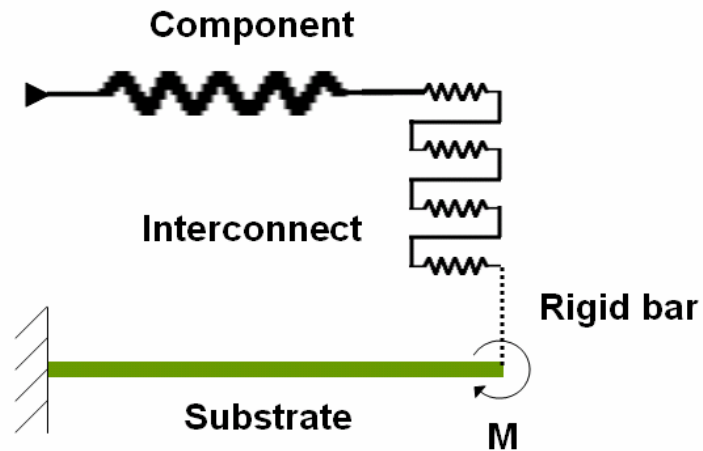
Figure 3-8 shows the stress fields generated in the printed wiring board after the pad has

translated 0.01 mm in the horizontal direction. As shown by the figure the stresses drop quite rapidly in the board thickness direction, about an order of magnitude at 0.7 mm.



**Figure 3-8: Stress distribution, 0.01 displacement**

The analytical model is modified to account for this by the addition of a spring offset by a rigid bar on the surface of the printed wiring board, as shown in Figure 3-9.



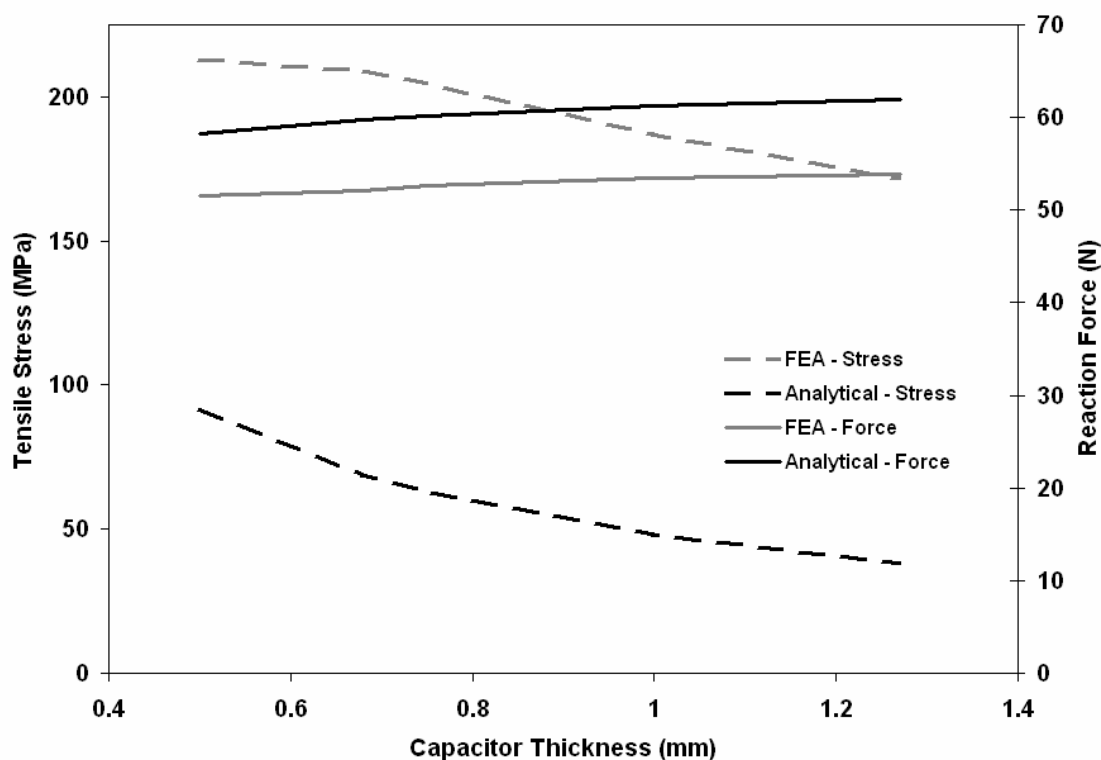
**Figure 3-9: Modified model representation**

The offset of the spring is set to one half the printed wiring board thickness. As a first order approximation, a printed wiring board surface shear stiffness that is not related to printed wiring board thickness will be used. Modifying and rerunning the model yields the results shown in Table 9

**Table 9: 0805 Analytical and FEA results**

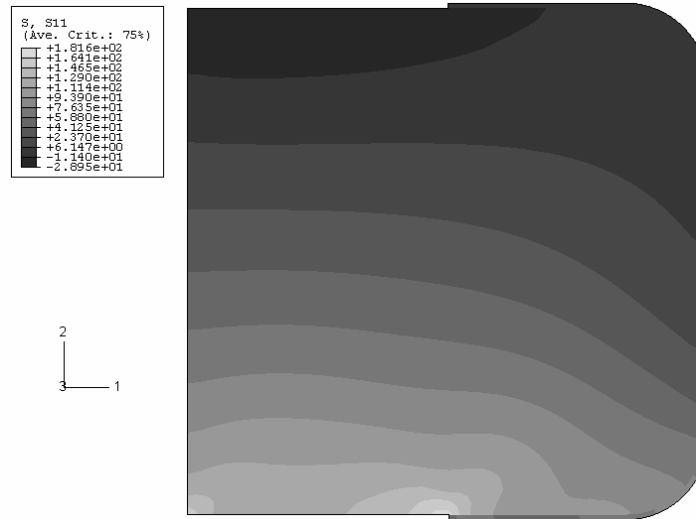
Capacitor Thickness	FEA Reaction Force (N)	FEA (MPa)	Analytical Reaction Force (N)	Analytical (MPa)
0.5 mm	51.6	213	58.2	91.7
0.68 mm	52.1	209	59.8	69.2
0.75 mm	52.7	205	60.2	63.2
1.00 mm	53.5	187	61.25	48.2
1.27 mm	53.9	172	61.9	38.4

The analytical model results are now within 15% of the FEA results. However, the stress values predicted by the analytical model are much lower than those predicted by the finite element models.



**Figure 3-10: FEA and analytical model results**

As shown in Figure 3-10 a simple stress calculation, such as force divided by area, is not adequate to represent the stress distribution in the capacitor. An example of the stress variations through the thickness of the capacitor are shown in Figure 3-11. The analytical stress is calculated assuming an axial application of the force. However, the device is loaded on an edge and therefore has an eccentric loading. Modification of the stress calculation to account for this eccentric loading is therefore necessary.

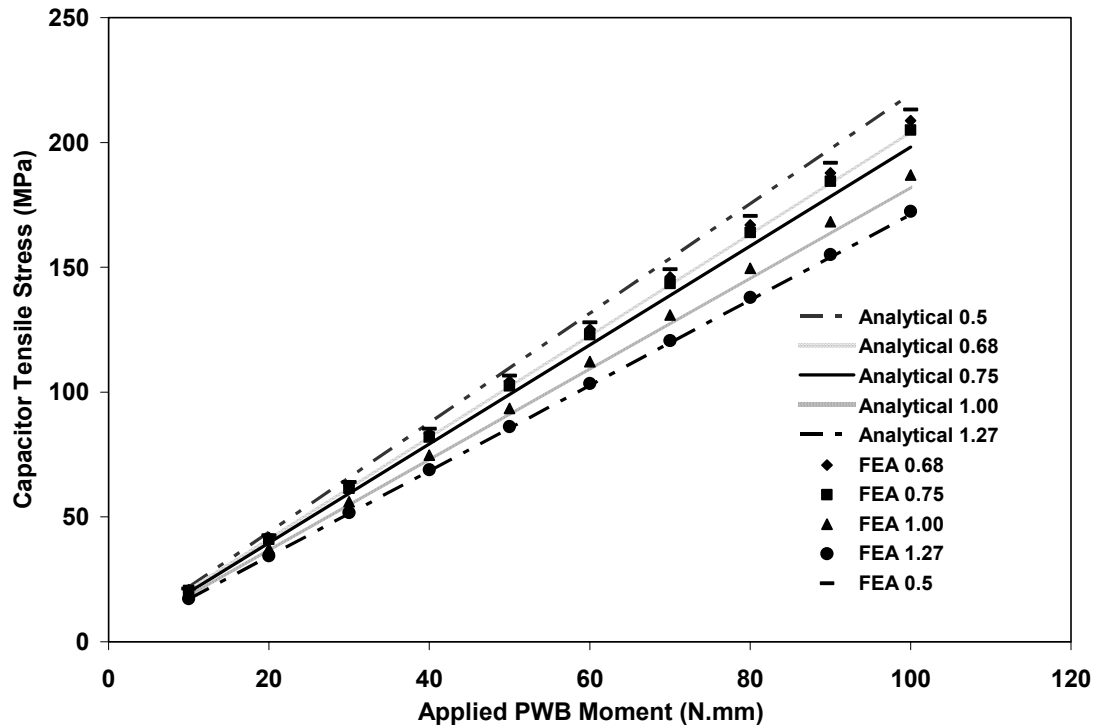


**Figure 3-11: Tensile stresses in the capacitor**

The results from the finite element analyses are used to develop a stress concentration factor that is dependent on the thickness of the device. The maximum stress will be divided by the average stress predicted by the finite element model and then plotted as a function of device thickness. This stress concentration factor is used in the analytical model to account for the edge loading effects of the actual device. The stress concentration factor calculated from the FEA results is:

$$S_f = 3.18 * t + 1.2$$

The results of the analytical model compared to the FEA results for a 0805 device using the stress concentration factor are shown in Figure 3-12. The difference between the FEA and analytical model stress values are less than 5% over the range of device thicknesses.



**Figure 3-12: Tensile stress comparison between FEA and analytical model**

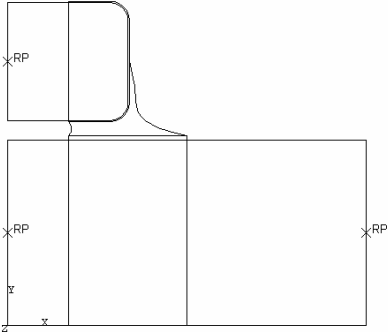
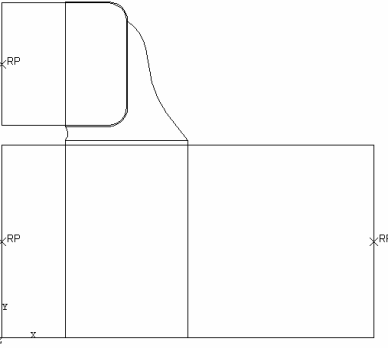
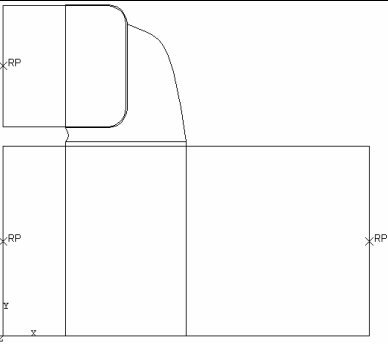
### 3.2.2 Effects of attach dimensions

#### 3.2.2.1 Shape

The device attach parameters were varied to determine the analytical models sensitivity to them. Three solder joint shapes were investigated, as shown in Table 4, while the standoff height of the component was held constant. The FEA models used to validate the analytical model are shown in Table 10 along with the factor used to modify the solder dimensions in the analytical model. This factor ( $J_f$ ) is a geometric interpretation of the solder joint shape and is roughly equal to the distance from the bondpad edge to the fillet meniscus and is used to modify the length of the solder joint to reflect the contribution of the fillet to the solder stiffness calculations.



**Table 10: FEA Models of different joint types and  $J_f$  factors**

<p style="text-align: center;"><b>Starved Solder Joint</b></p> <p>The fillet is ignored in the solder stiffness calculation, making the <math>J_f</math> equal to 0.5</p> $I_{sj} = (I_{pad} - I_{ps}) * 0.5$	
<p style="text-align: center;"><b>Nominal Solder Joint</b></p> <p>The fillet is accounted for in the solder stiffness calculation, making the <math>J_f</math> equal to 0.7</p> $I_{sj} = (I_{pad} - I_{ps}) * 0.7$	
<p style="text-align: center;"><b>Bulbous Solder Joint</b></p> <p>The fillet is accounted for in the solder stiffness calculation, making the <math>J_f</math> equal to 1.0</p> $I_{sj} = (I_{pad} - I_{ps}) * 1.0$	

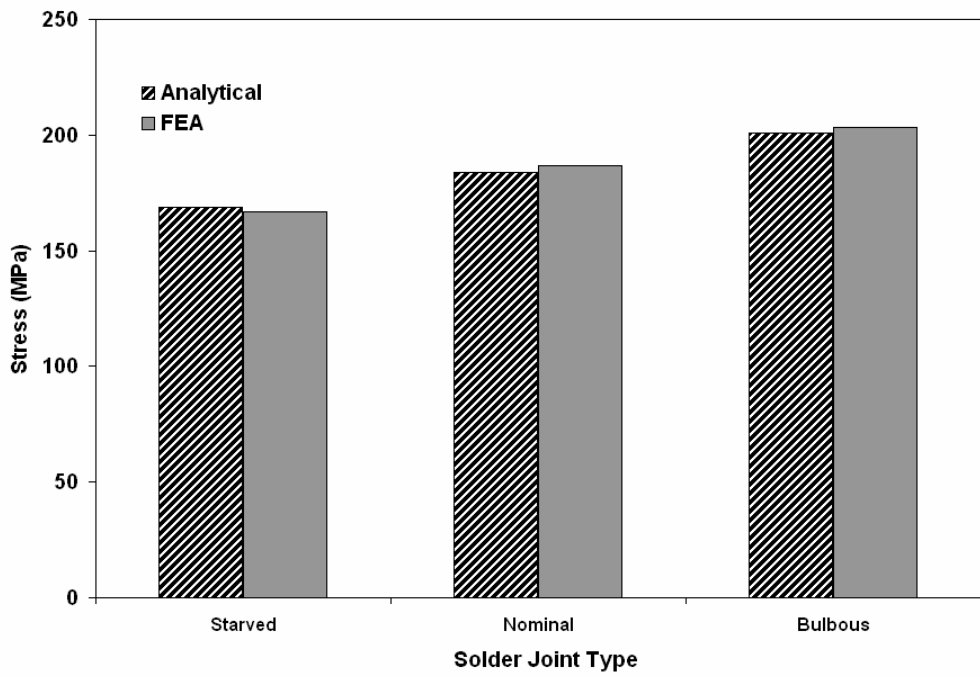
A comparison between the analytical model and the FEA models are shown in Table 11.

The results show that the analytical model agrees with the FEA results for the three fillet shapes.

**Table 11: Analytical and FEA results**

Solder Shape	FEA Reaction Force	FEA MPa	Analytical Reaction Force	Analytical MPa
Starved	52.3	166.8	52.2	169.5
Nominal	53.5	187	56.7	184.2
Bulbous	57.3	203.4	61.9	201.2

The results shown in Table 11 are displayed graphically in Figure 3-13.



**Figure 3-13: Analytical and FEA results**

As stated previously these results are based upon the solder shapes defined in Table 4.

The optimal joint shapes recommended by manufacturers vary. Many manufacturers are

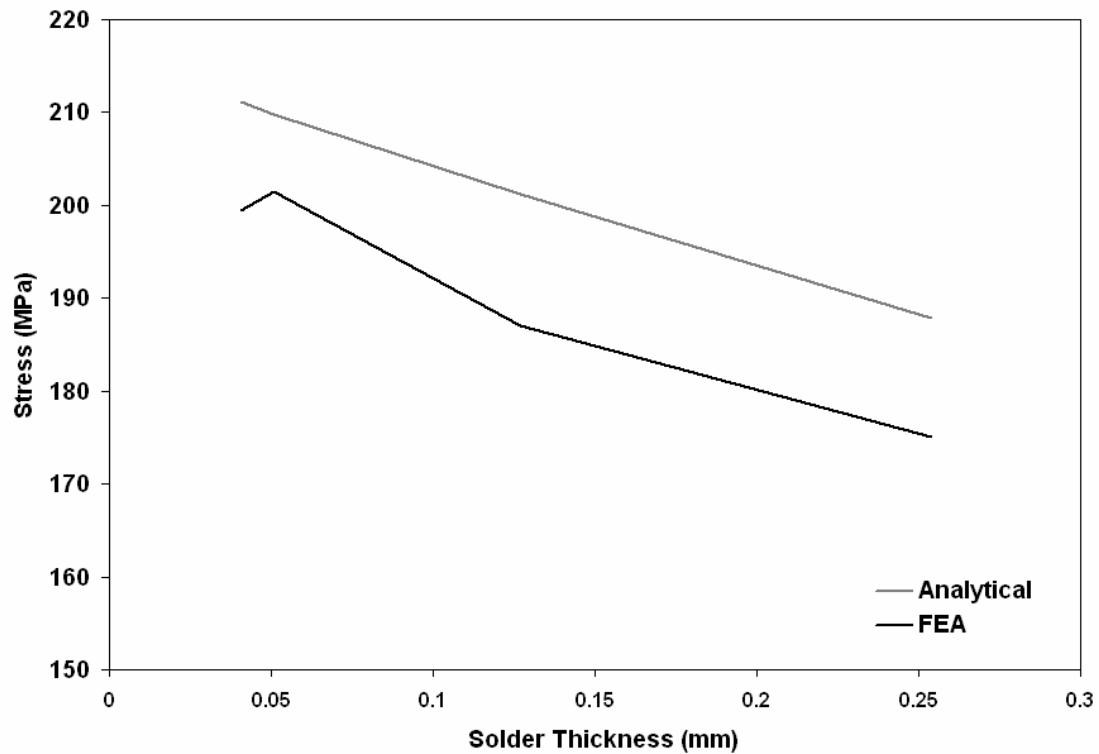
specifying smaller joints that would have been previously regarded as insufficient. This may be done to increase the joint compliance in an effort to minimize the potential for flex type failures.

### 3.2.2.2 Solder joint thickness

The FEA model was modified to investigate the effects of varying the thickness of the solder underneath the component. Four solder thicknesses representative of those seen on actual devices were studied, as shown in Table 12. The results show that the stresses in the device are not as sensitive to the solder thickness. Both the analytical model and the FEA predict the same behavior.

**Table 12: Analytical and FEA results**

Solder Thickness	FEA Reaction Force (N)	FEA (MPa)	Analytical Reaction Force (N)	Analytical (MPa)
0.0408 mm (1.6 mil)	58.8	199.5	65	211.2
0.0508 mm (2.0 mil)	58.1	201.5	64.6	209.8
0.127 mm (5 mil)	53.5	187	61.9	201.2
0.254 mm (10 mil)	51.2	175	57.9	187.9



**Figure 3-14: FEA and analytical model results**

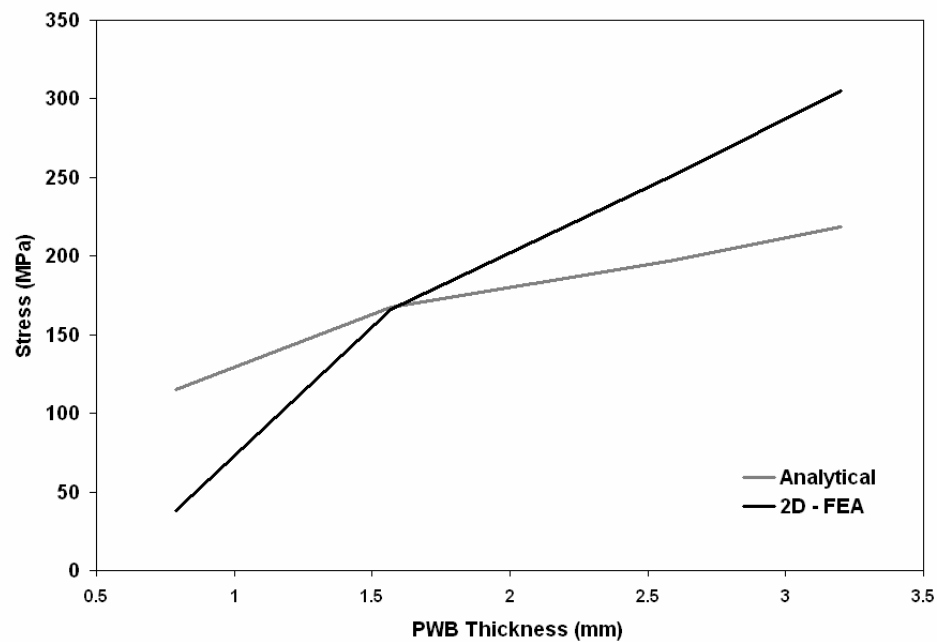
As shown by the figure the analytical results are within 10-15 MPa of the FEA results.

### 3.2.3 Effects of printed wiring board thickness

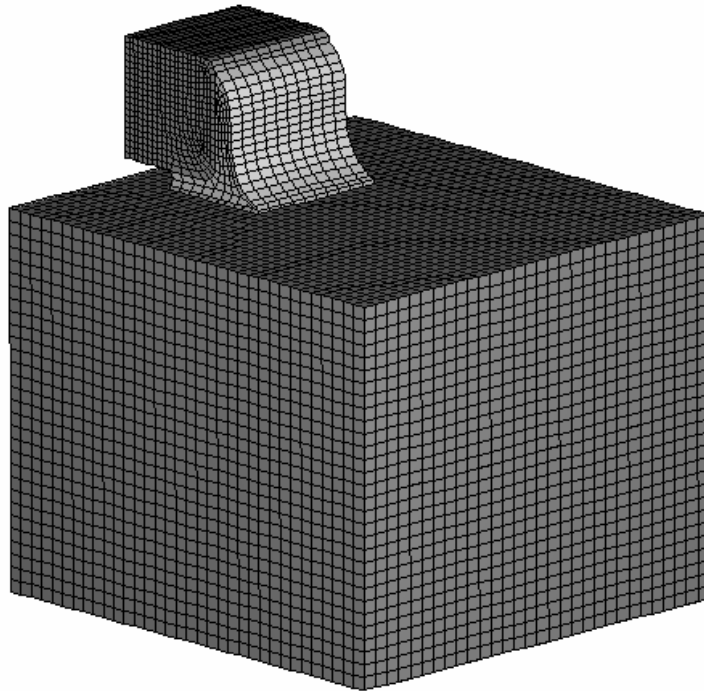
The FEA model was used to investigate the effects of varying the thickness of the printed wiring board. Four thicknesses were studied, as shown in Table 13. The previous studies were all conducted with a load of 100 N·mm. However, in this study the load will be adjusted so that the surface strain of the printed wiring board remains a constant one percent.

The results and the applied moments are shown in Table 13. The results plotted in Figure 3-15 show that the 2D finite element model has a large dependence on the printed wiring board thickness and may not reflect the actual response of the structure. The analytical model is less sensitive to changes in the thickness under a constant surface strain. The stress values predicted by the 2D FEA for the thinner boards did not appear to be realistic, and a 3D FEA model was constructed to verify the results.

The 3D model is used to verify the 2D FEA model and to investigate the effect of the thickness of the printed wiring board on the capacitor stress. The 3D model is shown in Figure 3-16, and utilizes symmetry about the center of the capacitor. The moment is applied by connecting a rigid surface to the end of the printed wiring board.



**Figure 3-15: 2D FEA and analytical model results**



**Figure 3-16: 3D FEA model, 3.15 thick PWB**

The deformed model shown in Figure 3-17 illustrates the bending behavior and the strains of the board. A comparison of the finite element analyses and the analytical model results are displayed in Figure 3-18. It can be seen that the 2D finite element and the analytical models do not agree with the results of the 3D models. This is mainly due to changes in the joint compliance as the thickness of the board increases. The initial assumption that the board shear stiffness does not change as a function of board thickness was not accurate and will be modified accordingly.

The equation  $K_s = \frac{9}{2-\nu} \cdot Ga$  is modified to include effects of the printed wiring board thickness as shown by the 3D finite element model. The modified equation for the board surface shear stiffness is:

$$K_s = \frac{9}{2-\nu} \cdot Ga \cdot 1.4 \cdot t^{0.5}$$

**Table 13: Analytical and FEA Results, 0.01 surface strain**

PWB Thickness	Applied Moment (N.mm)	2D - FEA (MPa)	3D - FEA (MPa)	Analytical (MPa)	Adjusted (MPa)
0.788 mm	22.34	37.8	114.8	115.3	121
1.57 mm	88.7	165.9	205.2	167.8	201
2.36 mm	200.4	252.1	275.6	197.8	262
3.2 mm	368.5	305.3	337.6	218.4	315

As shown by Figure 3-18 the analytical model results are within 5 -6 % of the 3D finite element results.

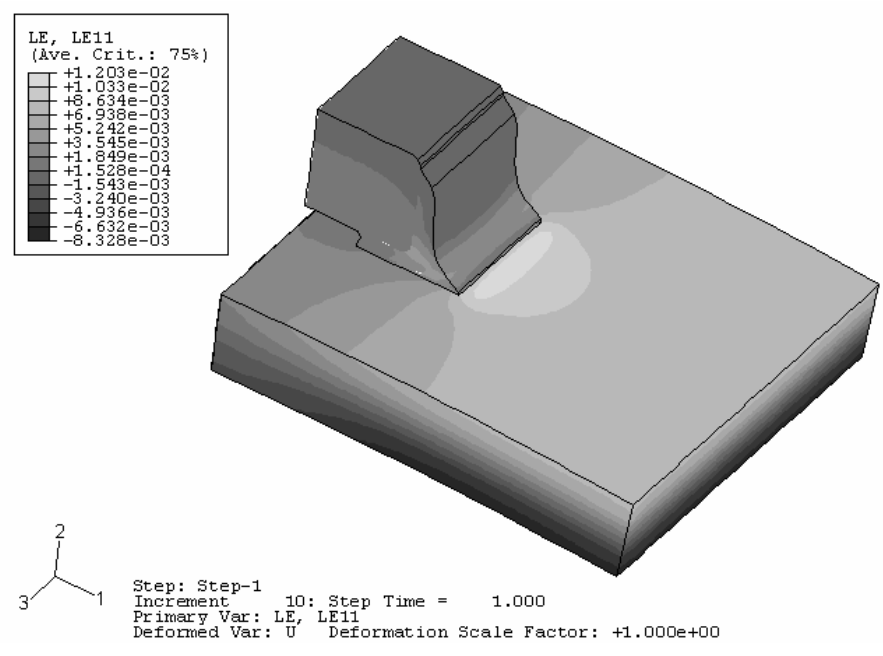


Figure 3-17: 3D FEA model, 0.788 thick PWB, LE11 strains

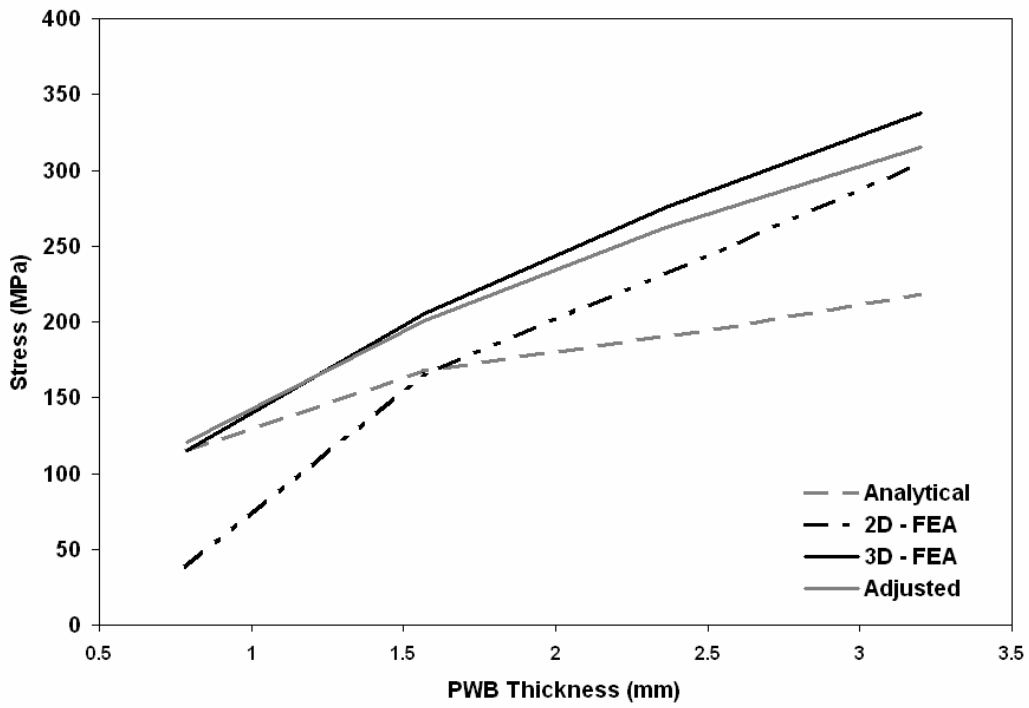


Figure 3-18: FEA and analytical results



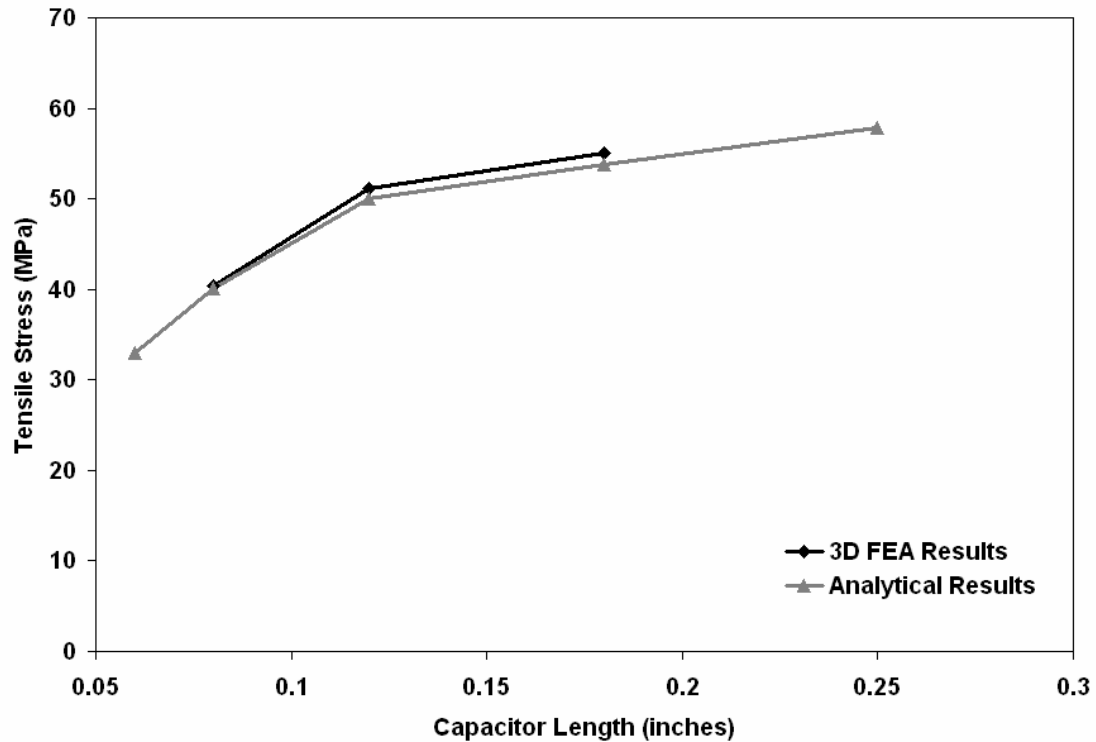
### 3.2.4 Effects of device length

Additional finite element models were used to compare the stresses of device of varying lengths to those predicted by the analytical model. Three lengths representative of 0805, 1206 and 1812 capacitors were investigated. The board and capacitor thicknesses were held constant and the end metallization was adjusted to reflect the dimensions shown in Table 6. The results under a constant board strain of 0.002, which is typical of strains encountered during capacitor failures, are shown in Table 14.

**Table 14: Analytical and FEA results, 0.002 surface strain**

Capacitor Size	Applied Moment (N.mm)	3D - FEA MPa	Analytical MPa
0603	10.7		33
0805	17.9	40.4	40.1
1206	21.4	52.6	50
1812	42.8	54.7	53.8
2512	42.8		57.8

As shown by Table 14 and Figure 3-19 the analytical model agrees within 5% of the 3D FEA results so that no adjustment is necessary.



**Figure 3-19: FEA and analytical results**

### 3.3 Summary

The analytical model has been compared to a combination of 2D and 3D finite element models. Several modifications factors have been introduced and implemented.

1. An additional spring to account for the surface shear stiffness of the printed wiring board. This is based upon a rigid disk on a halfspace and modified to account for varying board thicknesses
2. Modifier on the solder joint length to account for the effect of the fillet shape. In this case a starved solder joint (i.e. a small fillet) has the stiffness of the solder joint reduced by modifying the length of the solder joint, a bulbous solder joint has the solder length lengthened to increase the stiffness.

3. A stress concentration factor calculated from 2D finite element analyses. This is to account for the edge loading of the device

The analytical model has been shown to provide device stress values as a function of printed wiring board strain. The analytical model behaves in much of the same manner as finite element models and should be sufficient for making predictions on the failure of leadless chip devices.

## CHAPTER 4 MODEL VALIDATION

The calibrated analytical stress model is validated using 3D finite element models. The primary stress drivers as identified in the calibration section are:

1. Device length
2. Solder joint shape
3. Printed wiring board thickness

### 4.1 Test matrix

A partial factorial approach was taken and the test matrix is shown in Table 15. The loading will be an applied board level strain of  $2000 \mu\epsilon$ . This board level strain is more representative of those seen during printed wiring board bending events. Using this matrix means that nine FEA models must be constructed to validate the analytical stress model.

**Table 15: Test matrix for model validation**

		Solder Joint Shape		
		Starved	Nominal	Bulbous
PWB Thickness	Minimum (0.8 mm)	0805, 1812		0805, 1812
	Nominal (1.6 mm)		1206	
	Maximum (3.2 mm)	0805, 1812		0805, 1812

### 4.2 FEA results

An example of the FEA models run is shown in Figure 4-1. The models were half symmetric about the center of the capacitor. A moment was applied to a rigid surface tied to the end of the printed wiring board that generated a surface strain of 0.002.

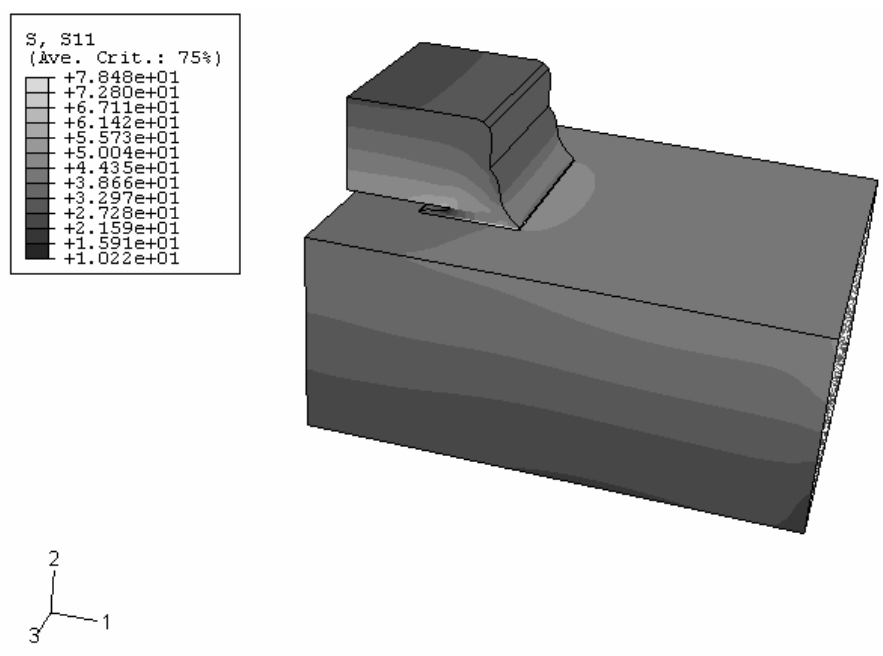


Figure 4-1: 3D FEA model, 1812 size device, with a starved solder joint

The results of the calibrated analytical model are shown in Table 16. As shown the analytical results vary between 85% and 112% of the FEA results. The average difference between the analytical and FEA are within 2%

**Table 16: Analytical and FEA results, 0.002 surface strain**

<b>Device Size</b>	<b>Solder Joint</b>	<b>PWB Thickness</b>	<b>3D – FEA (MPa)</b>	<b>Analytical (MPa)</b>	<b>Percent Difference</b>
<b>0805</b>	Starved	0.8 mm	21.3	24.5	-15.0%
<b>0805</b>	Bulbous	0.8 mm	26	26	0.0%
<b>0805</b>	Starved	3.2 mm	63	61.3	2.7%
<b>0805</b>	Bulbous	3.2 mm	75.2	70	6.9%
<b>1206</b>	Nominal	1.6 mm	52.6	49.5	5.9%
<b>1812</b>	Starved	0.8 mm	28.3	30	-6.0%
<b>1812</b>	Bulbous	0.8 mm	33.4	31	7.2%
<b>1812</b>	Starved	3.2 mm	96.5	92	4.7%
<b>1812</b>	Bulbous	3.2 mm	113.8	101	11.2%

As shown in Figure 4-2, the analytical model predicts stress relationships that agree with those shown by the FEA stress values. The analytical model typically provides predictions within -15% to 12% of those from FEA.

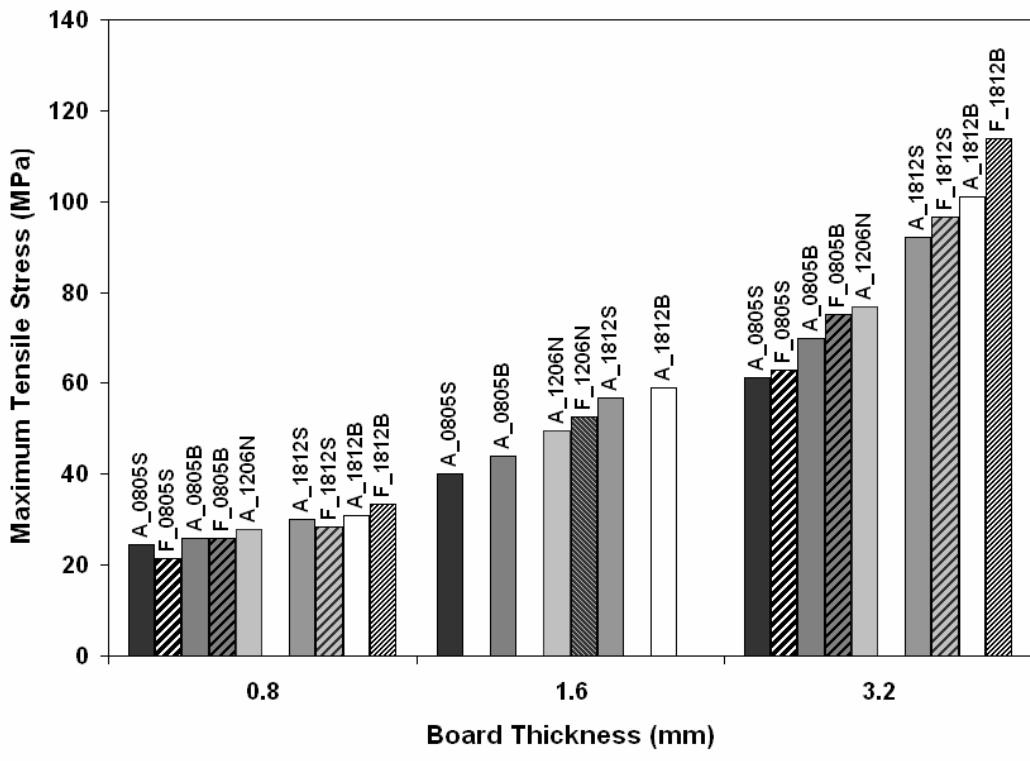


Figure 4-2: Analytical and FEA stress predictions

The analytical stress model provides results that are comparable to that of FEA. The relationships shown by the analytical model for capacitor length, printed wiring board thickness, and solder joint shape are very similar to those shown by the FEA models. The stress results should be sufficient to predict failures for these types of devices.

## CHAPTER 5 LEADLESS CHIP DEVICE FAILURE MODEL

The failure behavior of leadless chip devices when subjected to printed wiring board bending are typically specific to the device type and very dependent on the materials and geometry. This dependency can be used to limit the failure mechanisms and sites for the leadless chip device. For example, multilayer ceramic chip capacitors (MLCC) are known to fail during printed wiring board bending. The failure mode is cracking of the capacitor body. Therefore, solder joint failures are not typically associated with MLCCs and do not need to be assessed in regards to failure predictions. This is not unexpected as the fracture toughness of  $\text{BaTiO}_3$  is approximately  $1 \text{ MPa}\cdot\text{m}^{1/2}$  resulting in a relatively low fracture strength.

There are four potential failure sites associated with bending of leadless chip devices:

1. Component body
2. Component end metallization
3. Solder joint
4. Copper bond pad

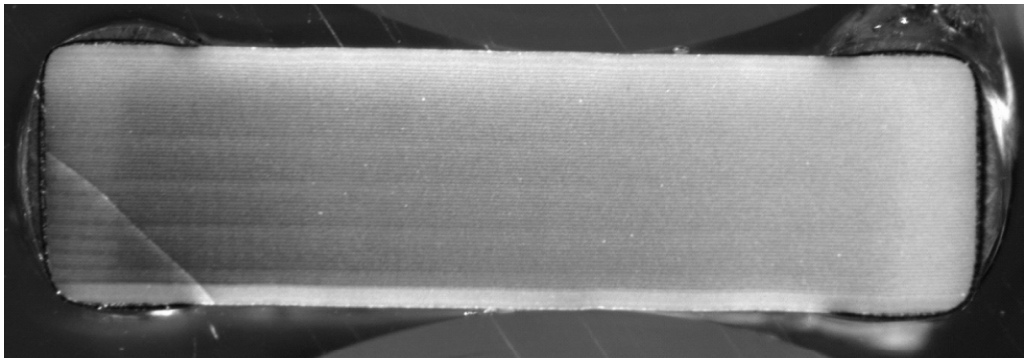
The component body can fail by cracking. The crack can intersect the resistive element or the electrodes of the component causing the resistance to increase or the capacitance to decrease. In brittle materials, the defects in the ceramic and the ceramic formulation will determine the stress at which the cracking will occur. The ceramic used for making capacitors has fracture properties that are highly dependent on the manufacturer.



## 5.1 Failure modes

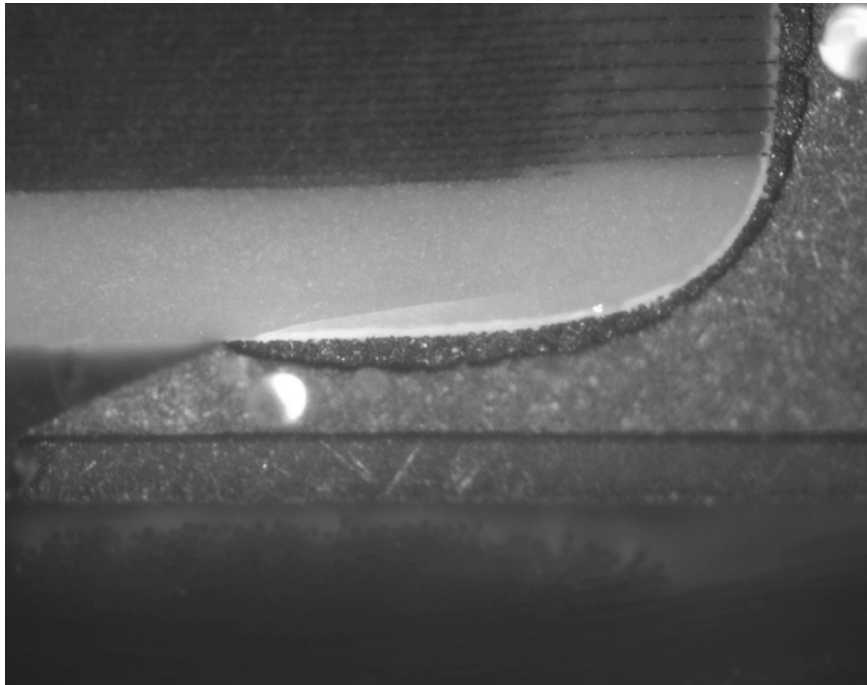
### 5.1.1 Capacitors

When a capacitor fractures the resulting crack may cause failure by intersecting the electrodes. This will cause a decrease in the capacitance or short the electrodes together causing a short to occur across the capacitor. A crack that intersects the electrodes is shown in Figure 5-1.



**Figure 5-1: Capacitor cracking (intersecting electrodes)**

Not all cracks will cause the capacitor to fail immediately. As shown in Figure 5-2, a crack limited to the margin of the capacitor does not intersect any functional aspect of the capacitor and is therefore not detectable, but still may represent a reliability concern due to the potential for long term crack growth.



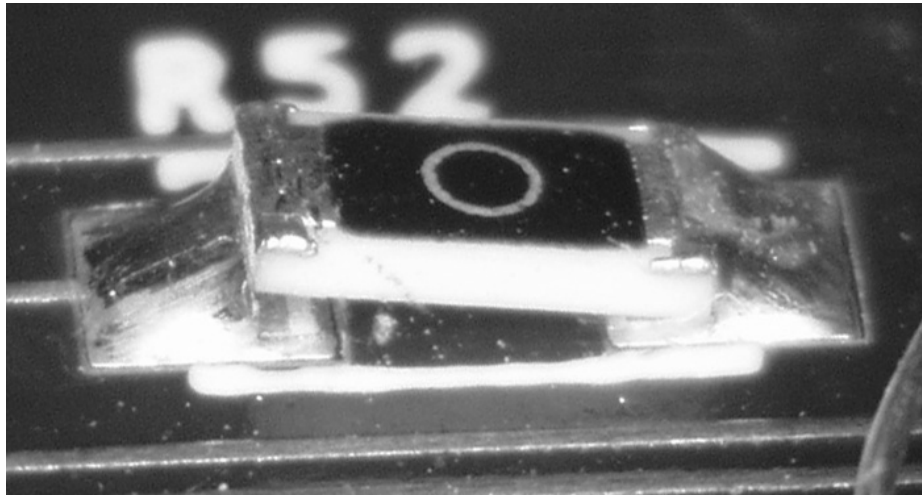
**Figure 5-2: Capacitor cracking (margin only)**

### 5.1.2 Resistors

The ceramic used for resistors, aluminum oxide ( $\text{Al}_2\text{O}_3$ ) has a higher fracture strength and higher stresses are therefore required to initiate cracking in the component body. Actual experimental failures of leadless chip resistors indicate two failure modes.

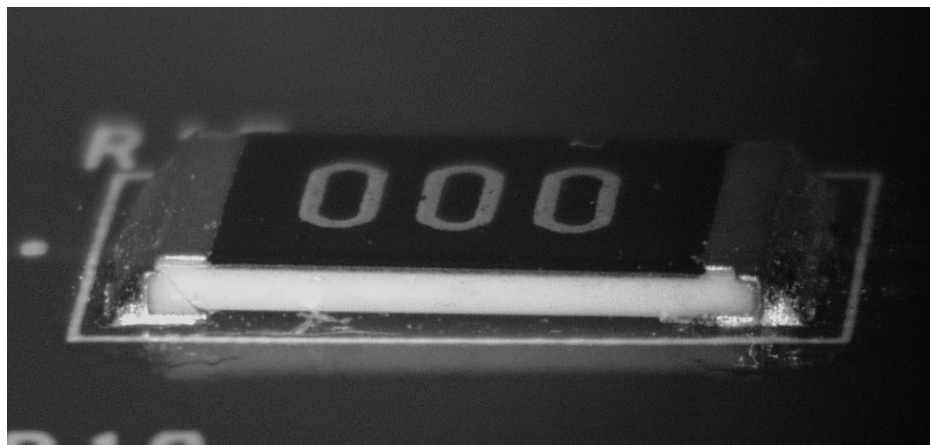
1. End metallization cracking
2. Body cracking

As shown in Figure 5-3, an end metallization failure occurs when the metal termination of the resistor separates from the ceramic substrate. Once separated, the resistor will no longer function properly.



**Figure 5-3: Resistor metallization failure [35]**

Resistor body cracking is the second failure mode of ceramic resistors. A resistor body crack, as shown in Figure 5-4 may cause failure if the crack intersects the resistive element or electrically separates the resistor from the board. Both failure modes share the same crack initiation site. The main difference is the path along which the crack propagates.



**Figure 5-4: Resistor body cracking**

Board bending failures of the bond pad and solder joint are very rare with regard to leadless chip devices and often require the presence of severe defects in the solder or printed wiring board (i.e. voiding, poor wetting, intermetallic formation, etc.). Typically, bond pad failures occur when the solder joint has a greater area than the pad, such as the case with non-soldermask defined (NSMD) ball grid array joints [72]. Experiments indicate that even under extreme bending conditions solder joint or bond pad failures do not occur [35].

## **5.2 Failure models, capacitors**

As stated previously, the dominant failure mode of multi-layer ceramic capacitors during printed wiring board deflection is cracking of the capacitor body. Manufacturers recognize resistance to cracking as critical measure of the durability of their capacitors and typically provide test data that reflects the capacitors durability. However, this data is extremely limited and typically only available for capacitors that are 0805 or smaller. Therefore, the applicability of a theoretical fracture mechanics failure model will be investigated and compared to an overstress based failure model derived from manufacturer test data.

### **5.2.1 Ceramic capacitor fracture mechanics failure model**

The ceramic used in capacitors is typically a doped barium titanate ( $\text{BaTiO}_3$ ). Manufacturers either formulate the ceramics themselves or acquire them from titanate vendors [50], depending on the complexity of the formulation. For example, ceramics such as Y5V are simple enough that manufacturers may formulate them in house. Large

ceramic vendors such as Murata, TDK and Kyocera do this. The formulations of the ceramics are typically proprietary and can vary from manufacturer to manufacturer. This means that the strength of the ceramic may also vary depending on the manufacturer.

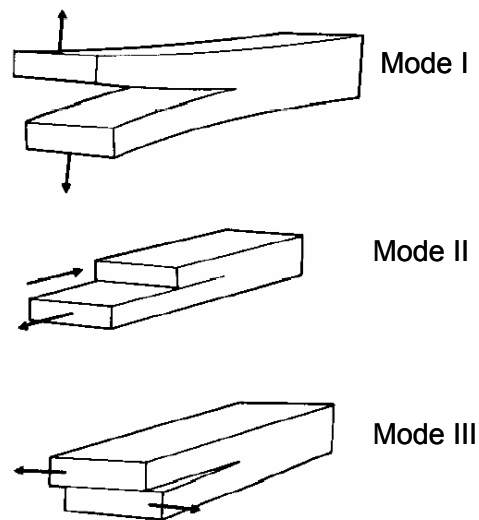
The variation in fracture strength will be dependent on [52]:

1. Fracture toughness  $K_{Ic}$
2. Flaw size (defects)
3. Residual stresses

The fracture toughness is typically dependent on the fracture mode. The three basic fracture modes are:

- I. Opening mode
- II. Sliding mode
- III. Tearing mode

The three modes of fracture are shown in Figure 5-5. The failure of brittle ceramics is typically dominated by Mode I [53]. The cracks shown in Figure 5-1 are typically associated with Mode I type fracture behavior.



**Figure 5-5: Three modes of fracture**

Assuming that a straight single ended crack initiates at the edge of the capacitor, Griffith [52] formulated an expression that states that the fracture stress ( $\sigma_F$ ) is defined by the equation:

$$\sigma_F = \left( \frac{2YE}{\pi c} \right)^{\frac{1}{2}}$$

Where  $Y$  is the Young's modulus,  $E$  is the surface energy and  $c$  is the half length of a crack. Further experimental work by Griffith determined that there was a relationship between the flaw size and the fracture stress. Work done by Griffith was expanded by Irwin and Kies [54] who developed the concept of stress intensity factors,  $K$  (after Kies). This was developed into the well known fracture equation, for mode 1, where the fracture toughness,  $K_{IC}$  [53] is defined as:

$$K_{IC} = \frac{\sqrt{2YE}}{\pi}$$

Converting the energy to applied stress and accounting for an edge crack yields the following equation [53]:

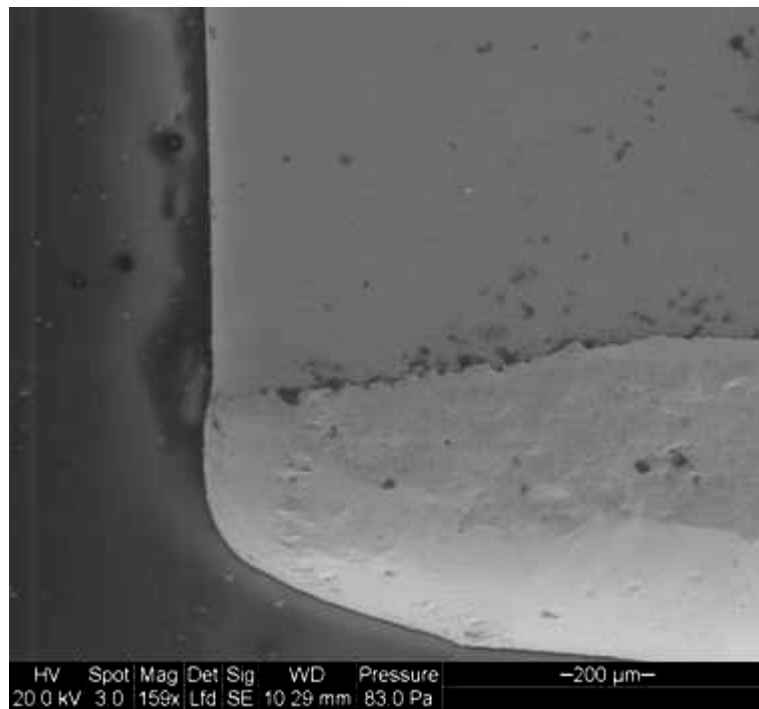
$$K_I = 1.12\sigma_f\sqrt{\pi a}$$

Typical published values of  $K_{IC}$  of X7R ceramics are usually between 0.9 and 1.3  $\text{MPa}\cdot\text{m}^{1/2}$  [56]. When  $K_I > K_{IC}$  then the crack will propagate through the ceramic and cause failure. Koripella [12] conducted experiments to characterize the fracture behavior of capacitor dielectrics C0G, X7R, and Z5U and reported the fracture stress, Weibull modulus and fracture toughness. The edge crack, flaw size (a) in Table 17, is computed from this data.

**Table 17: Computed flaw sizes from experimental data [12]**

Dielectric Type	Fracture Stress 50% Failure (MPa)	Weibull modulus	$K_{ic}$ ( $\text{MPa}\cdot\text{m}^{1/2}$ )	Flaw Size ( $\mu\text{m}$ )
C0G	175	4.8	1.5	18.6
X7R	166	6.5	1.03	9.8
Z5U	116	3.9	1.01	19.2

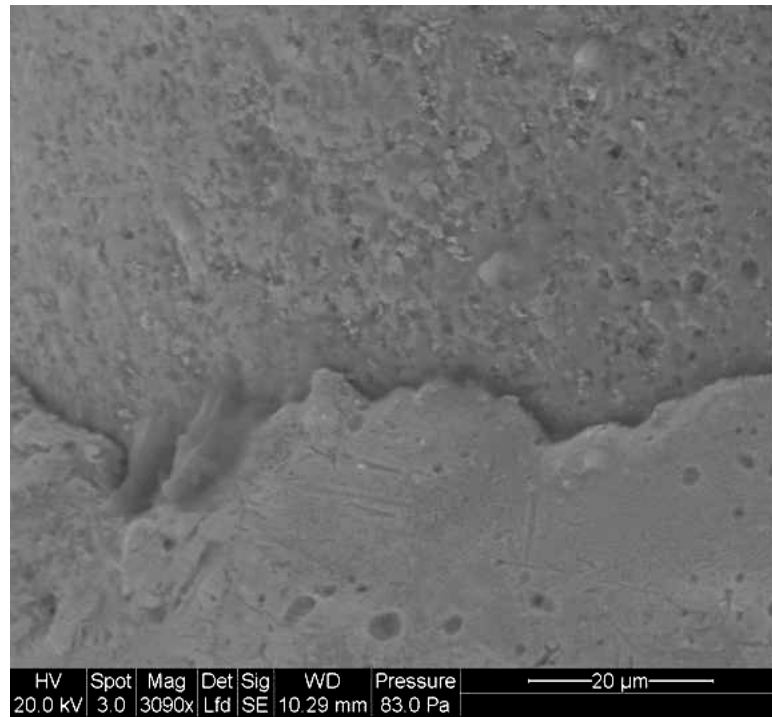
Actual identification of flaws of this size is possible. As an example, a 1206 size X7R capacitor was inspected using an environmental scanning electron microscope. A low magnification image of the capacitor is shown in Figure 5-6.



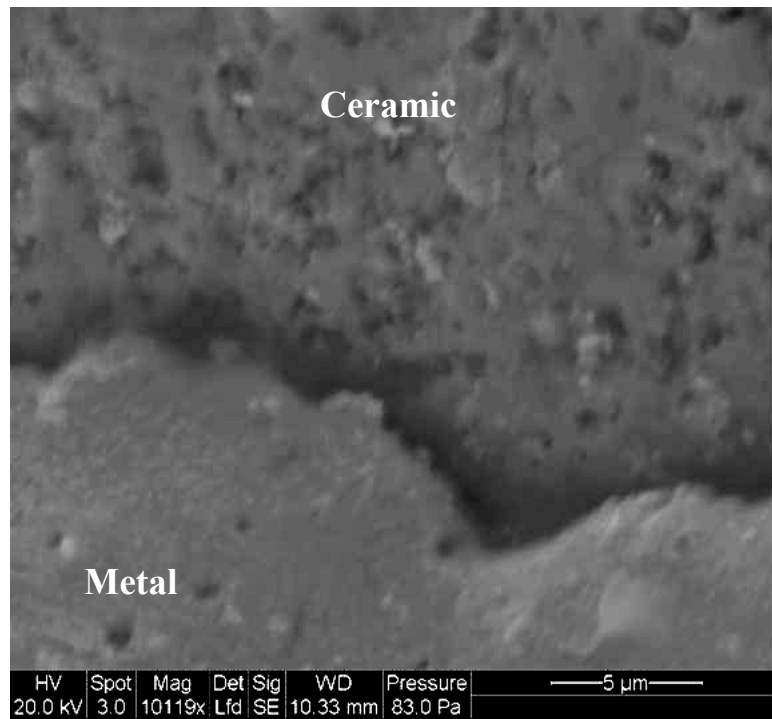
**Figure 5-6: ESEM image, 1206 capacitor, 159X magnification**

Magnification was further increased to identify flaws of the size calculated in Table 17. The areas inspected correspond to the areas where cracks are known to initiate, as shown in Figure 5-1 and Figure 5-2. A thorough inspection of the capacitor yielded no discernible defects at a magnification of 3090X, as shown in Figure 5-7. The magnification was increased to 10119X, and the capacitor was re-inspected. At this high magnification small pore like structures, on the order of 0.5 to 1.0  $\mu\text{m}$  were evident, as shown in Figure 5-8.





**Figure 5-7: ESEM image, 1206 capacitor, 3090X magnification**



**Figure 5-8: ESEM image, 1206 capacitor, 10119X magnification**

Assuming that these pores act as defects and are the initiation sites, the required fracture stress is computed and shown in Table 18. This fracture stress is around 509 MPa and is much higher than reported maximum fracture stress values for X7R type capacitors [18].

**Table 18: Computed fracture stress**

Dielectric Type	Fracture Stress 50% Failure (MPa)	$K_{ic}$ (MPa·m <sup>1/2</sup> )	Flaw Size (μm)
X7R	509	1.03	1.0

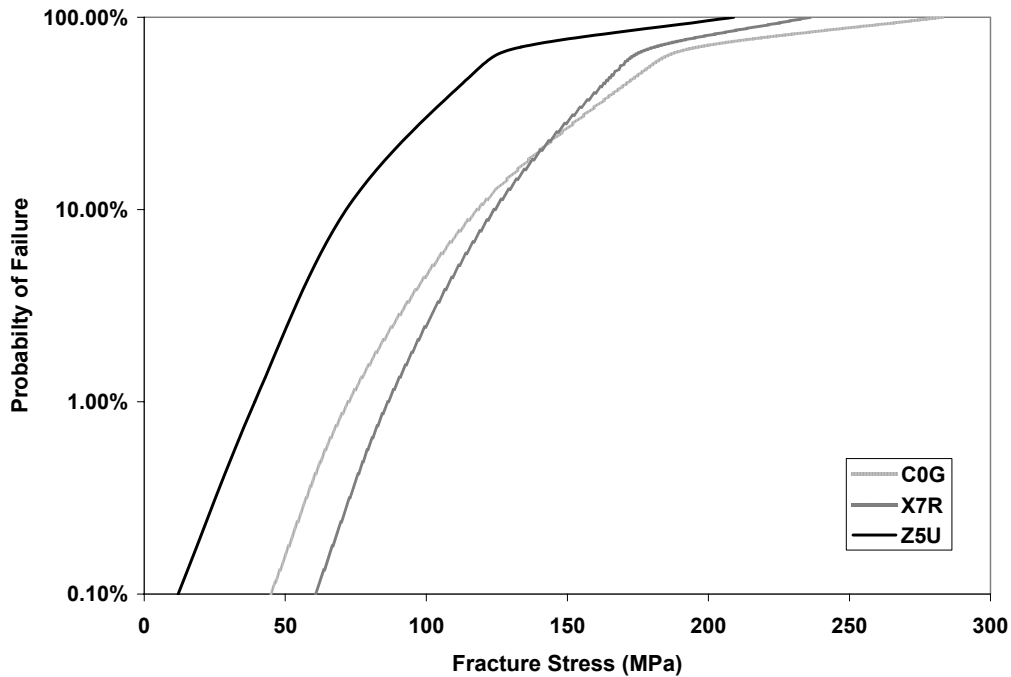
It has been hypothesized that the porous nature of the interface between the end metallization and the ceramic is actually providing the crack initiation sites [30]. As shown in Figure 5-8, a fairly large gap is present between the metallization and the ceramic, which could act a crack initiation site. However, the time required to characterize the fracture properties of this interface for the various capacitor manufacturers would defeat the purpose of a rapid analysis approach. A more realistic approach would be the utilization of a failure model that recognizes that there is a distribution of flaws that generate corresponding stresses at which fracture will occur.

This was first proposed by Weibull [55], and the resultant relationship has 2-parameters, the Weibull modulus and characteristic strength. This equation can also be modified to factor in the volume of the sample to reflect the flaw population at the crack initiation site. The equation for computing the survival probability of a sample (constant size, and shape) is shown in Equation 5-1.

$$\phi = \exp\left\{-\left(\frac{\sigma}{\sigma_o}\right)^m\right\}$$

**Equation 5-1: Failure distribution calculated using the Weibull modulus [53]**

Where  $\phi$  equals the survival probability,  $m$  is the Weibull modulus,  $\sigma$  is the applied stress, and  $\sigma_o$  is the stress at which 37% of the samples survived. Using this relationship the failure distribution for the data given in Table 17 can be calculated, as shown in Figure 5-9.



**Figure 5-9: Failure distributions from test data [12]**

### 5.2.2 Ceramic capacitor Weibull modulus failure model

The distribution for the fracture strength of the ceramic can be adjusted to account for the volume of the sample, as shown in Equation 5-2.

$$\phi = \exp\left\{-\frac{V}{V_o}\left(\frac{\sigma}{\sigma_o}\right)^m\right\}$$

**Equation 5-2: Failure distribution accounting for sample volume [53]**

Where  $V_o$  is the volume, or geometric parameter of the initial test specimen that describes the region where the crack may initiate.  $V$  is the geometric parameter of the sample for which the failure is to be calculated. Using the analytical stress model, the Weibull modulus, and characteristic strength can be determined from manufacturer test data. The failure initiation site will be assumed to be the area along the end termination. This means that the geometric parameter will be the width of the device. The manufacturer results are typically from three point bend tests and the given deflections must be converted to inputs suitable for the analytical model.

### 5.2.3 Failure Distributions

The failure of chip components under flexural loading is observed to be typically non-deterministic. The brittle nature of monolithic<sup>10</sup> ceramics and their sensitivity to flaw

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<sup>10</sup> While ceramic capacitors are a composite structure, the additional elements provide no reinforcement against flexure events and for all practical purposes can be ignored

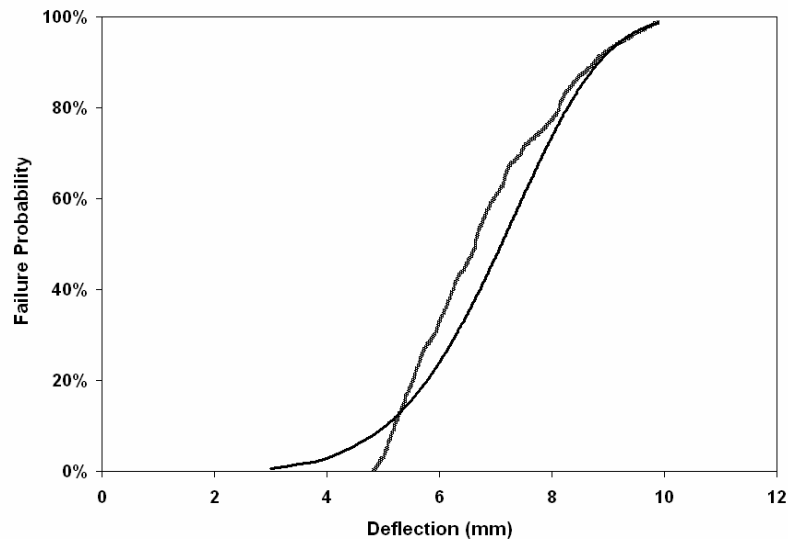
population triggers this probabilistic behavior. The analytical model therefore requires the selection of a distribution to describe this load-reliability relationship.

As mentioned in the previous chapters, the distribution selected was a Weibull distribution. While this distribution displayed an excellent fit to experimental measurements, the selection was based on the rationale that Weibull distribution is an extreme or lowest value distribution derived from weakest link theory [55]. This statistical approach (lends itself/maps) well to the physical mechanics that initiate chip component failure. As the application of the flexural load results in an overstress event, where initiation, rather than growth-dependent mechanisms, is the dominant factor, fracture results when the stress intensity factor evolving at the largest appropriate<sup>11</sup> flaw, i.e., the weakest link, exceeds the material fracture toughness.

A differentiation in Weibull distributions is provided by the use of two parameters or three parameters to describe the failure statistics. The criticality of this selection is inherent at the outer bounds of the distribution. This can be clearly be demonstrated in the tail ends of the distribution shown in Figure 5-10.

---

<sup>11</sup> Appropriate is defined as a flaw located in the volume subjected to Mode I tensile stress and oriented perpendicular to the applied load



**Figure 5-10: Two parameter Weibull distribution fit to data**

Numerous factors led to the selection of two-parameter Weibull as the appropriate distribution for predicting failure of chip components under flexural loads. While this deviates from the accepted method of fitting to three-parameter Weibull when describe the outlying behavior of solder joints subjected to thermo-mechanical fatigue [58,62] there are definitive rationales for the selection of two-parameter Weibull.

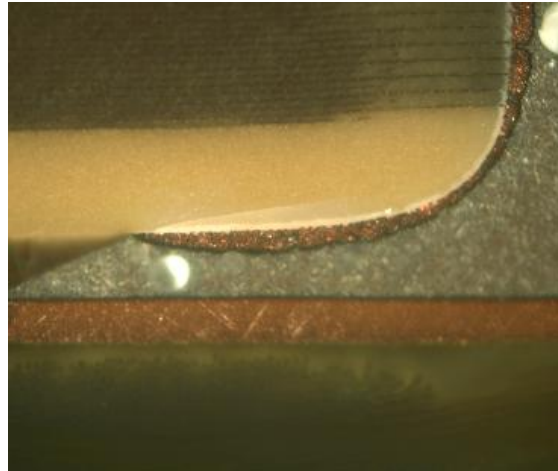
The primary driver is that three-parameter Weibull assumes a threshold stress or a failure free operating period (FFOP). This is appropriate for solder joint fatigue, as wear out requires the sequential evolution of deformation, microstructural coarsening, void formation and coalescence, and finally crack propagation [69]. Through this time-dependent failure threshold, solder joints of acceptable quality are expected to remain failure-free for some minimum amount of time and the Weibull distribution becomes more dependent upon solder geometry and variations in operating environments.

In fracture of monolithic ceramics subjected to uniaxial loading, there is limited evidence of a threshold stress. Numerous papers display two-parameter Weibull distribution when describing the fracture statistics of monolithic ceramics [63-68]. This approach is based upon the reality that the presence of large flaws, while of successively lower and lower probability, can never definitively be screened from the ceramic body. Transitioning from two-parameter to three-parameter Weibull distribution in describing the mechanical properties of brittle materials requires either a limitation in the criticality of the flaws present in the bulk material or an insensitivity to the flaw population in general. Examples of both can be found in the proof-testing of optical fibers [71] and the use of specialized processing techniques in the fabrication of high fracture toughness silicon nitride [70].

Neither case applies to the fracture of chip components under flexural loads. The use of powder processing to fabricate the bulk material (barium titanate, alumina) and the application of a metal termination provide avenues for the introduction of defects of significant size. Recent examinations of commercially available alumina identified pores exceeding 50 microns in diameter, even when investigating relatively small volumes [63].

An additional concern in the test data used to map the distribution behavior is the use of capacitance monitoring to identify fracture. While not definitively proven, personnel

observations (Figure 5-11 ) seem to suggest that capacitors that experience fracture at relatively low flexural loads display an acute angle of crack propagation.



**Figure 5-11: Capacitor fracture, no capacitance drop**

This can result in no loss of capacitance, as no electrodes are intersected by the fracture path. This would have the effect of obscuring the outer bound of the failure data, artificially creating three-parameter Weibull behavior.

The final justification for assuming two-parameter behavior is the unknown sample sizes available to fit these distributions. This provides insufficient data to provide any prediction of outer bound behavior, where two-parameter and three-parameter predictions begin to differentiate. Because of the need for a conservative prediction methodology, as under prediction has a severely limited value, three parameter should only be used when it demonstrates a significantly better fit to justify the need of an additional parameter, i.e. the threshold stress.



### 5.2.3.1 Deflection moment relationships

The input moment for the analytical stress model is calculated using the deflection relationships for three point bend tests. Initially beam equations were used and then verified with experimental results. If necessary, plate equations would be utilized.

During a three point bend test the maximum moment is developed at the center of the beam. The deflection for a three point bend test using simple beam equations is shown in Equation 5-3.

$$\delta = \frac{PL^3}{48EI}$$

**Equation 5-3**

Where  $\delta$  is the displacement at the center of the beam, P is the force applied, E is the elastic modulus, I is the second moment of inertia, and L is the length of the beam.

Given a displacement the force P can be determined. The moment in the beam can then be calculated using Equation 5-4.

$$M(x) = \frac{P}{2}(x) - P\left(x - \frac{L}{2}\right)$$

**Equation 5-4**

Where  $M$  is the moment,  $L$  is the length of the beam, and  $P$  is the applied force. Substituting Equation 5-3 into Equation 5-4 yields the following moment, and displacement relationship, shown in Equation 5-5.

$$M(x) = \frac{24\delta EI}{L^3}(x) - \frac{48\delta EI}{L^3}\left(x - \frac{L}{2}\right)$$

**Equation 5-5**

If necessary this moment can then be converted to the strain in the outer fiber of the printed wiring board by using the relationship shown in Equation 5-6

$$\varepsilon = \frac{My}{EI}$$

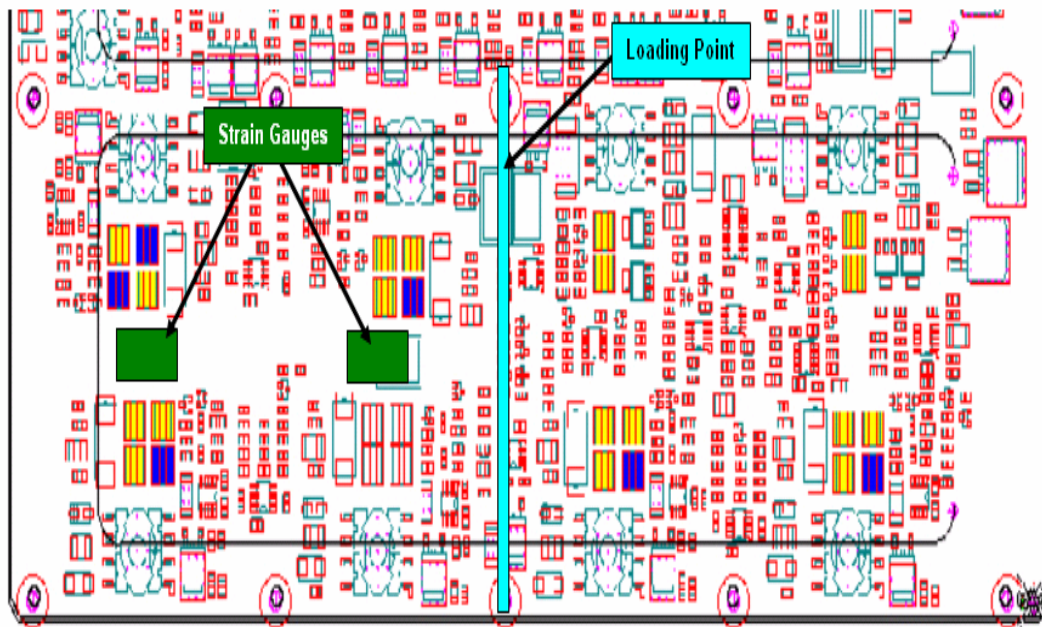
**Equation 5-6**

Where  $y$  is half the thickness of the printed wiring board,  $M$  is the moment,  $E$  is the Young's modulus, and  $I$  is the moment of inertia. The resulting strain is therefore directly proportional to the moment at that location in the board.

### 5.2.3.2 Validation of deflection moment relationships

The validity of beam type equations is verified by conducting a three point bend test on a printed wiring board assembly. Two strain gages were mounted to an actual printed wiring board, as shown in Figure 5-12, which was then tested in a three point bend test,

as shown in Figure 5-13. The center ram was pushed up into the board and strain readings were taken at 1 mm displacement intervals. Theoretical strain calculations were made for the strain gage locations using Equation 5-5 and Equation 5-6. The results of the calculations and experiment are shown in Figure 5-14.



**Figure 5-12: Test board section**

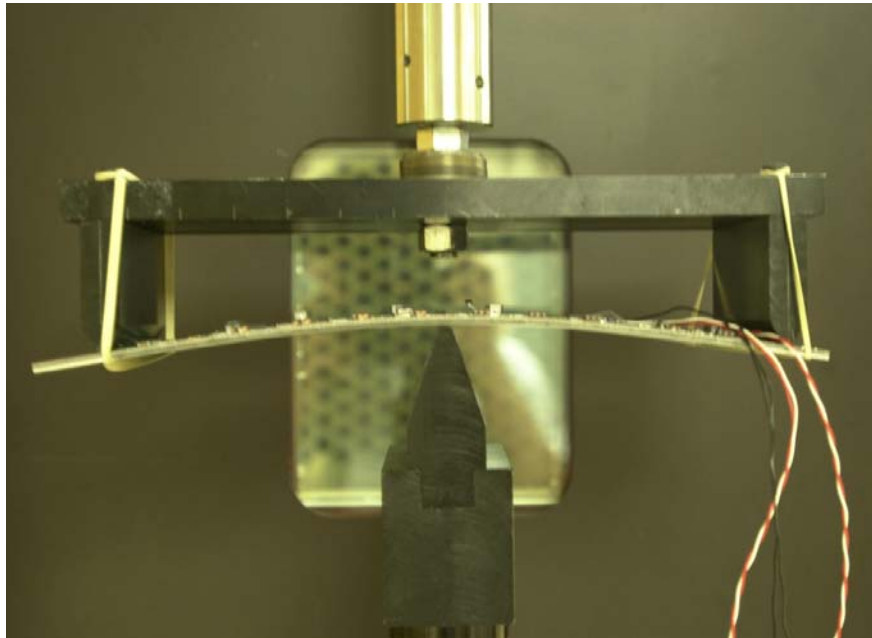


Figure 5-13: Board bending test setup

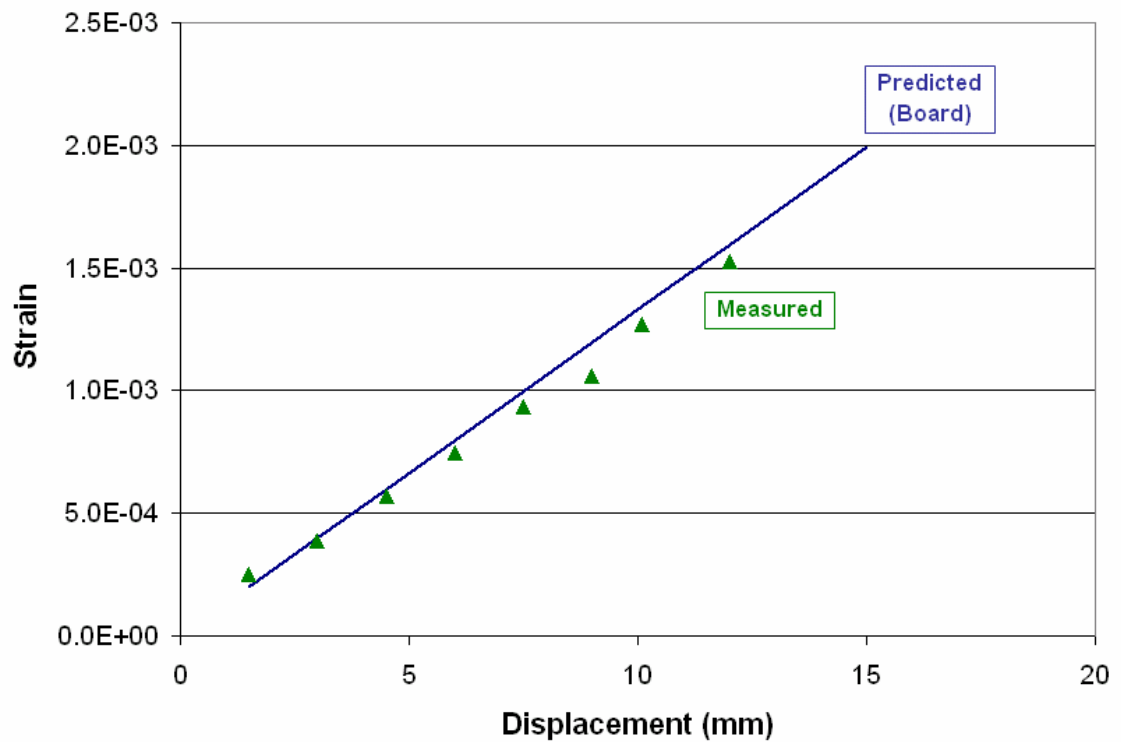


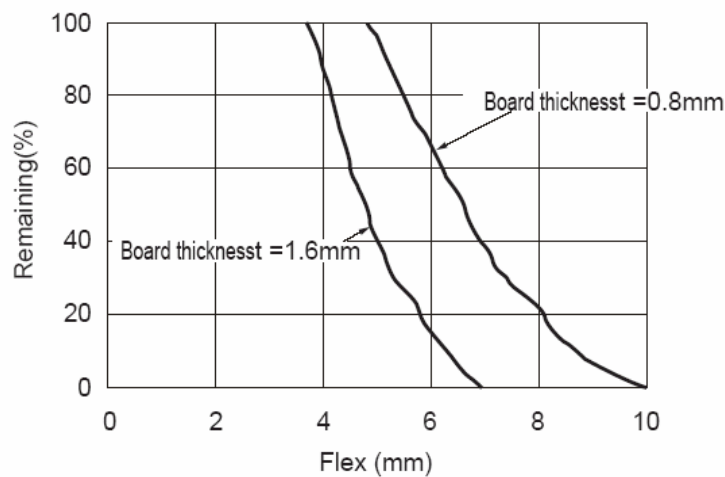
Figure 5-14: Board bending experimental and theoretical results

The theoretical calculations using beam equations showed very good correlation to the actual measured strain values.

#### 5.2.4 TDK failure parameters

The TDK Corporation has published failure data in their application manual for ceramic capacitors. The failure data from the TDK application manual for a 0805 capacitor is shown in Figure 5-15.

**Relation between board thickness and flex strength  
(C2012X7R1H103K)**



**Figure 5-15: TDK capacitor failure data 0805 size capacitor [25]**

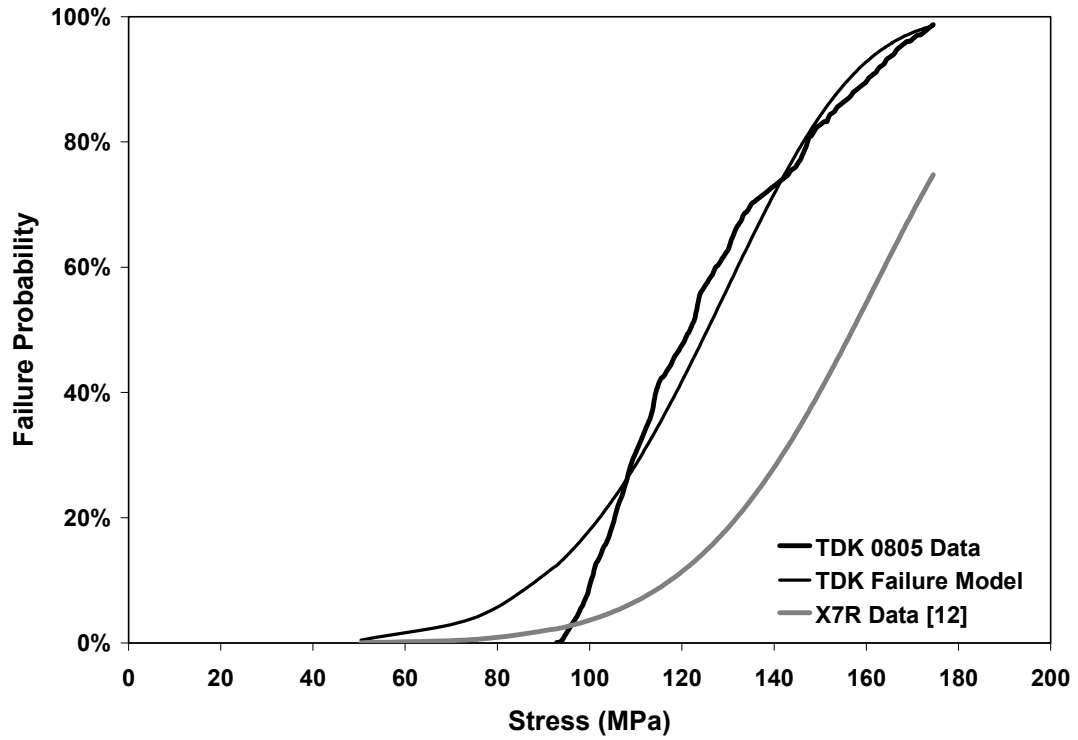
Converting the displacement data using the analytical model to the equivalent capacitor stress yields the survival probability as a function of stress. This then allows the computation of the parameters (Table 19) necessary to use the Weibull modulus as a

failure model. The failure data from the 1.6 mm board thickness was used to determine the Weibull modulus and characteristic strength values. The failure distributions are shown in Figure 5-16. Included in the graph are the failure predictions based upon parameters found in literature [12]. As shown, the literature failure parameters under-predict the probability of failure of the device. However, this is expected as these values were determined by three point bend testing on relatively short samples, which means that they may be failing in combined shear and bending.

The Weibull failure model provides a relatively good correlation with the failure data between failure probabilities of 30 to 99%. However, the error rapidly increases below 30%. The problem is that the test data does not include non-visible cracks in the capacitor that fail to intersect the electrodes. The standard capacitor flex test utilizes a drop in capacitance as its failure definition. Using this criterion excludes all cracks that are not visible or do not cause the required change in capacitance.

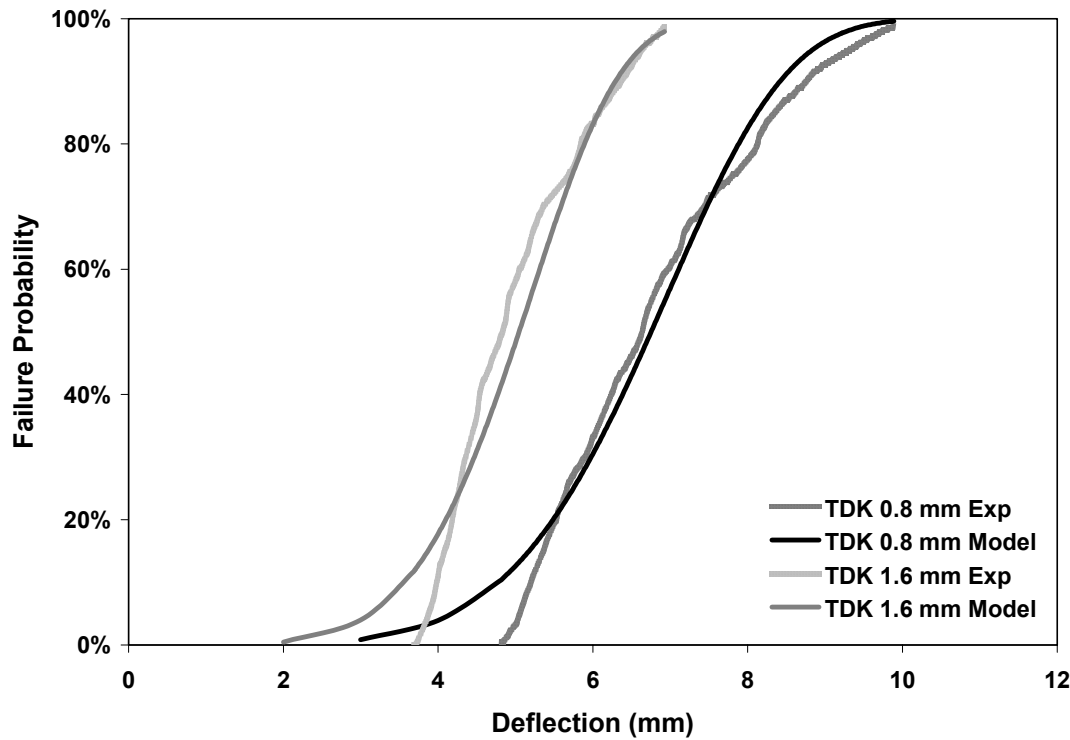
**Table 19: Computed Weibull modulus from experimental data**

Dielectric Type	Capacitor width	Characteristic Strength 67% Failure (MPa)	Weibull modulus
TDK 0805, X7R	1.27	134.2	5.5
X7R Dielectric [12]	4.83	166	6.5



**Figure 5-16: TDK failure probability, 0805 capacitor. 1.6 mm PWB**

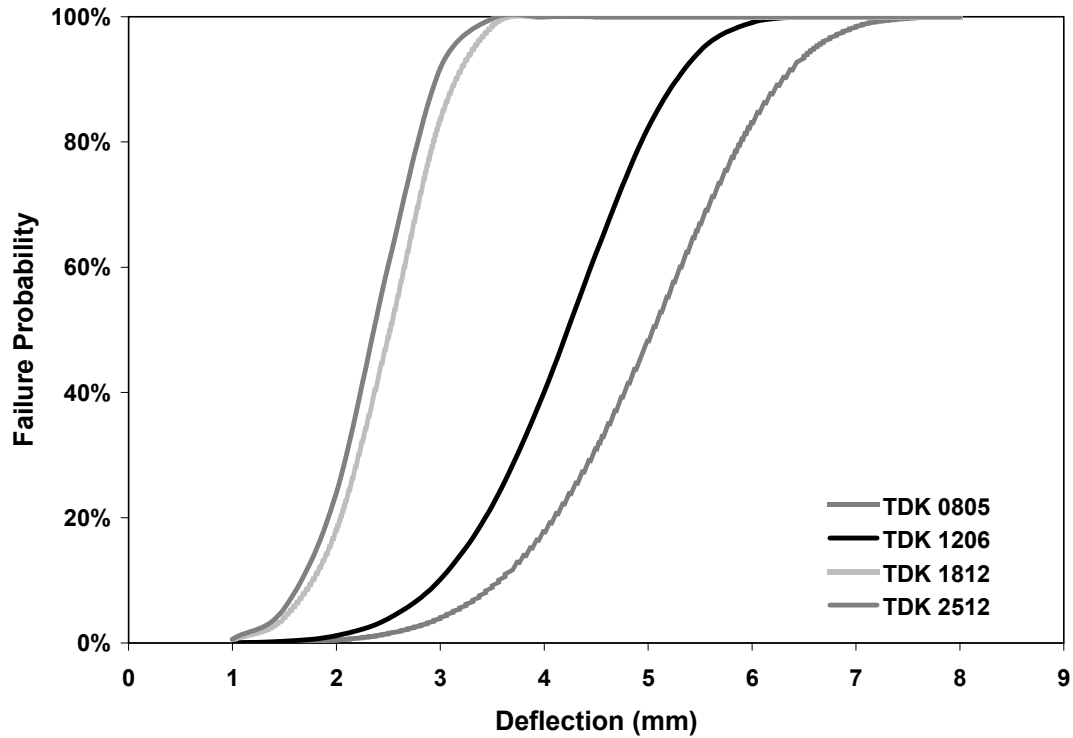
The TDK data also includes results from tests run on a 0.8 mm thick printed wiring board. Using the failure model with the calculated parameters, and the analytical stress model, the results as a function of board displacement are shown in Figure 5-17.



**Figure 5-17: TDK failure probability, 0805 capacitor, two PWB thicknesses**

The results show that the analytical model combined with a manufacturer specific failure results adequately predicts failures of capacitors during printed wiring board bending. A comparison of four TDK capacitor sizes and their predicted failure distributions is shown in Figure 5-18





**Figure 5-18: Capacitor size comparison**

### 5.2.5 MuRata failure parameters

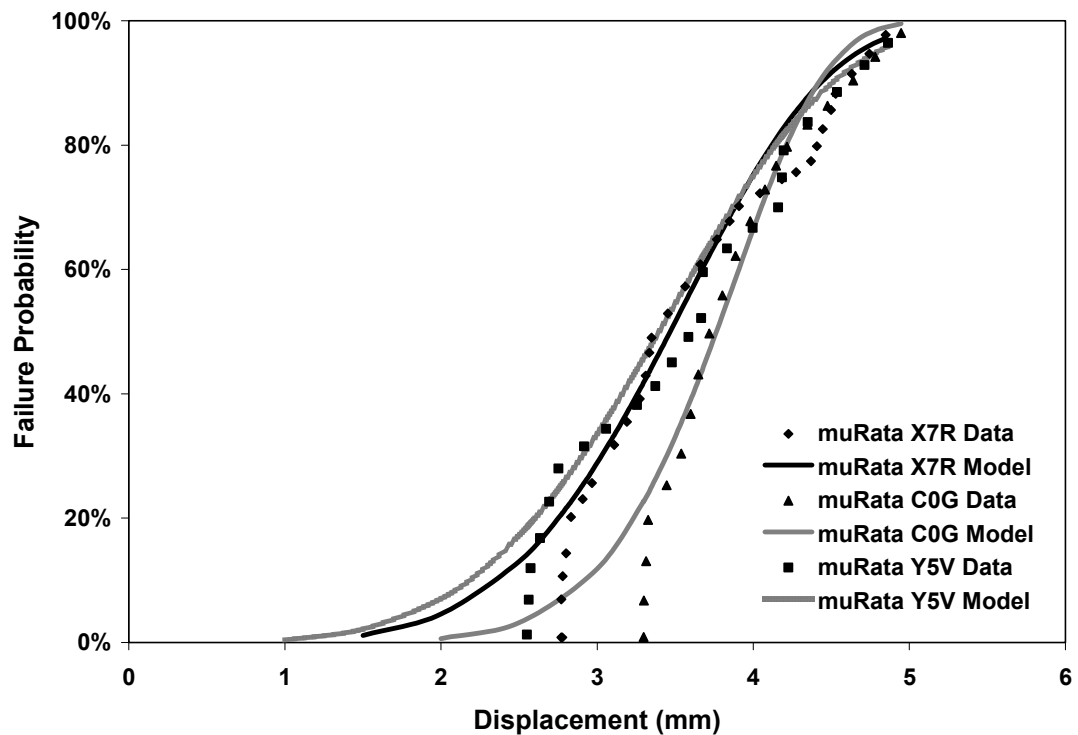
MuRata has published failure data in its application manual for MLCC capacitors [20].

MuRata did included data for three dielectric types. The failure parameters computed from this data are shown in Table 20. The experimental and analytical model results are shown in Figure 5-19.

**Table 20: Computed Weibull modulus from experimental data**

Dielectric Type	Capacitor width	Characteristic Strength 67% Failure (MPa)	Weibull modulus
muRata 0805, Y5V	1.27	100.3	4.47
muRata 0805, X7R	1.27	100.6	5.2
muRata 0805, C0G	1.27	106	13

The results clearly show the strengths of the various dielectrics and confirm that C0G is the strongest, followed by X7R and then Y5V.

**Figure 5-19: MuRata capacitor comparison, 0805**

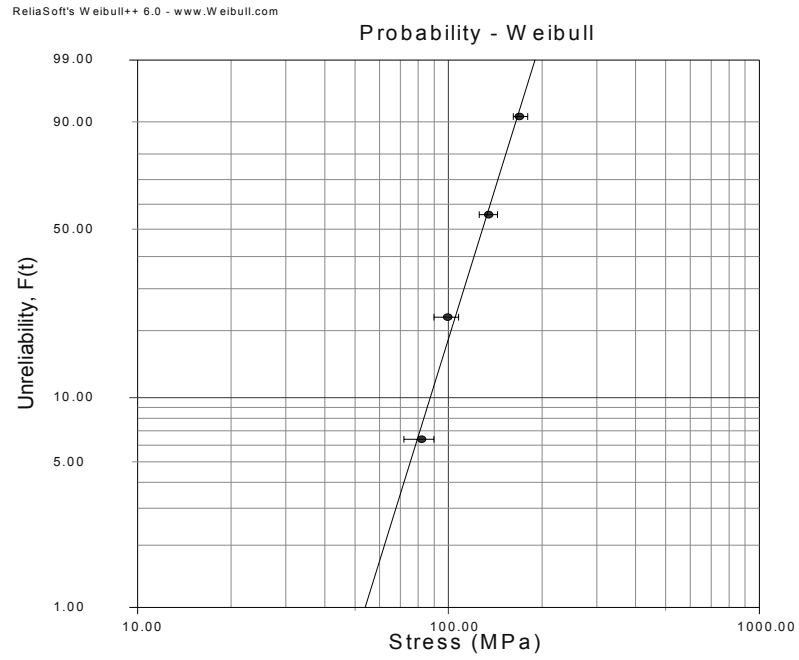
### 5.2.6 Syfer failure parameters

The data from Syfer is shown in Table 21. The failures are presented as interval data since they were collected at 0.5 mm displacement steps, as shown in Table 21.

**Table 21: Failure data from Syfer [44]**

Bend distance to Crack Capacitor	No. of Cracked Capacitors
2.5mm	31
3.0mm	79
4.0mm	158
5.0mm	171

This data was fitted to a Weibull distribution and plotted versus stress is shown in Figure 5-20.

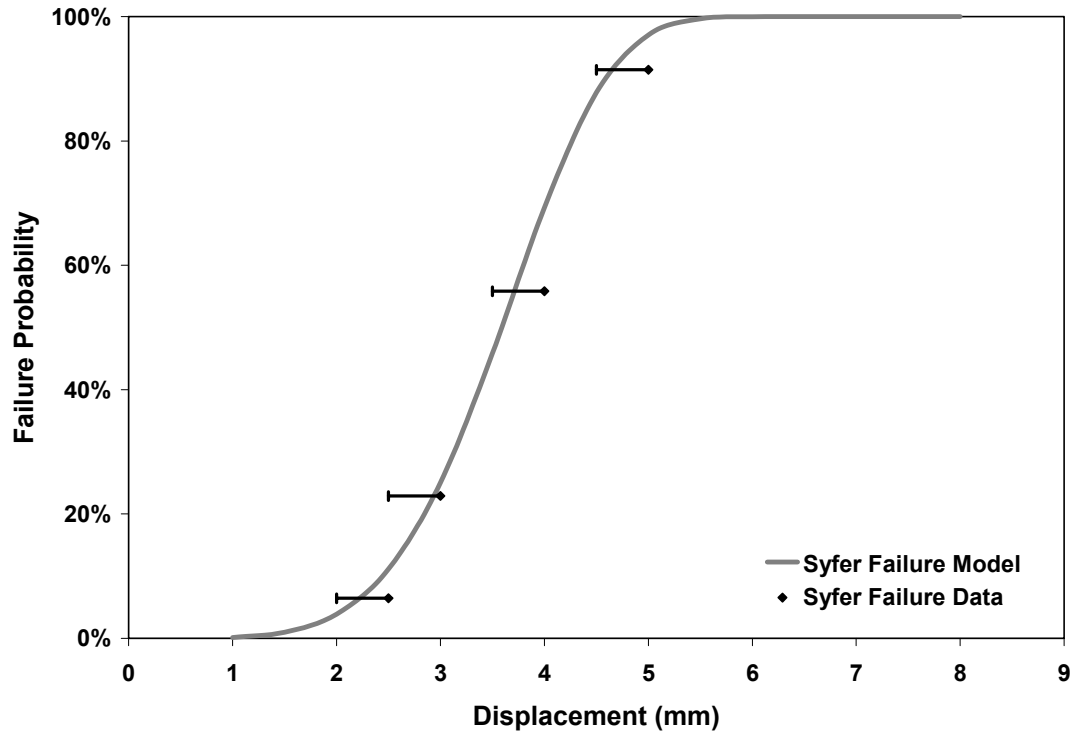


**Figure 5-20: Syfer failure data X7R 1206 capacitor**

The computed Weibull modulus for the Syfer X7R 1206 capacitor is shown in Table 22.

**Table 22: Computed Weibull modulus from experimental data**

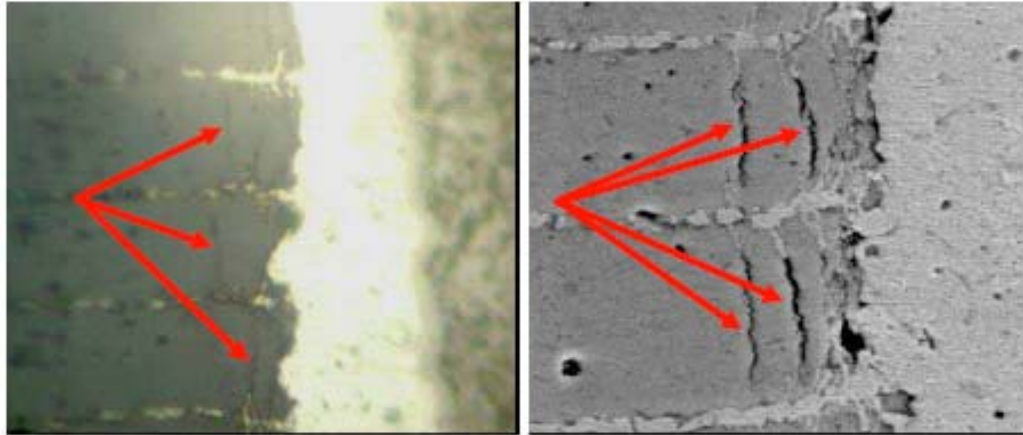
Dielectric Type	Capacitor width	Characteristic Strength 67% Failure (MPa)	Weibull modulus
Syfer 1206, X7R	1.524	117.5	5.12



**Figure 5-21: Failure model and experimental data**

### 5.2.7 Cal-Chip failure parameters

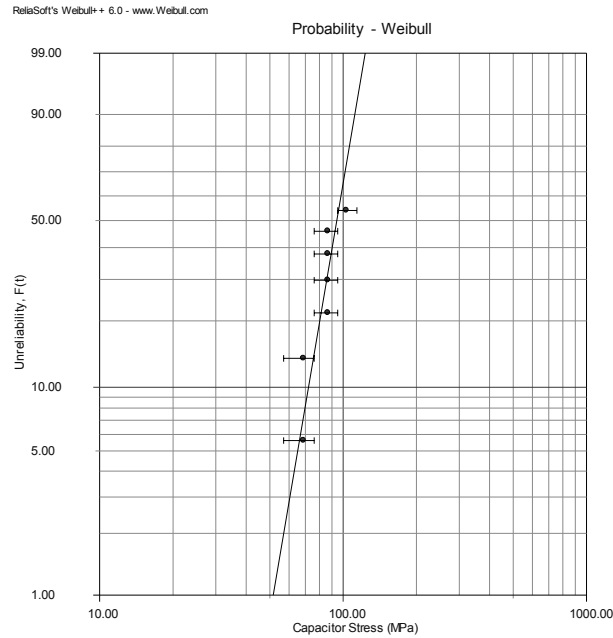
Four point bend tests were conducted on Cal-Chip Y5V capacitors. These capacitors had manufacturing defects present. The defect is known as micro-cracking, and it occurs near the end of the capacitor between the electrodes, as shown in Figure 5-22.



**Figure 5-22: Micro-cracking in Cal-Chip Y5V capacitor (optical and ESEM images)**

It was believed that the presence of these cracks could degrade the strength of the capacitors. Standard Cal-Chip capacitors are rated to a 2 mm deflection specification.

The failures were recorded at 500  $\mu\epsilon$  intervals. A Weibull plot verses stress is shown in Figure 5-20.

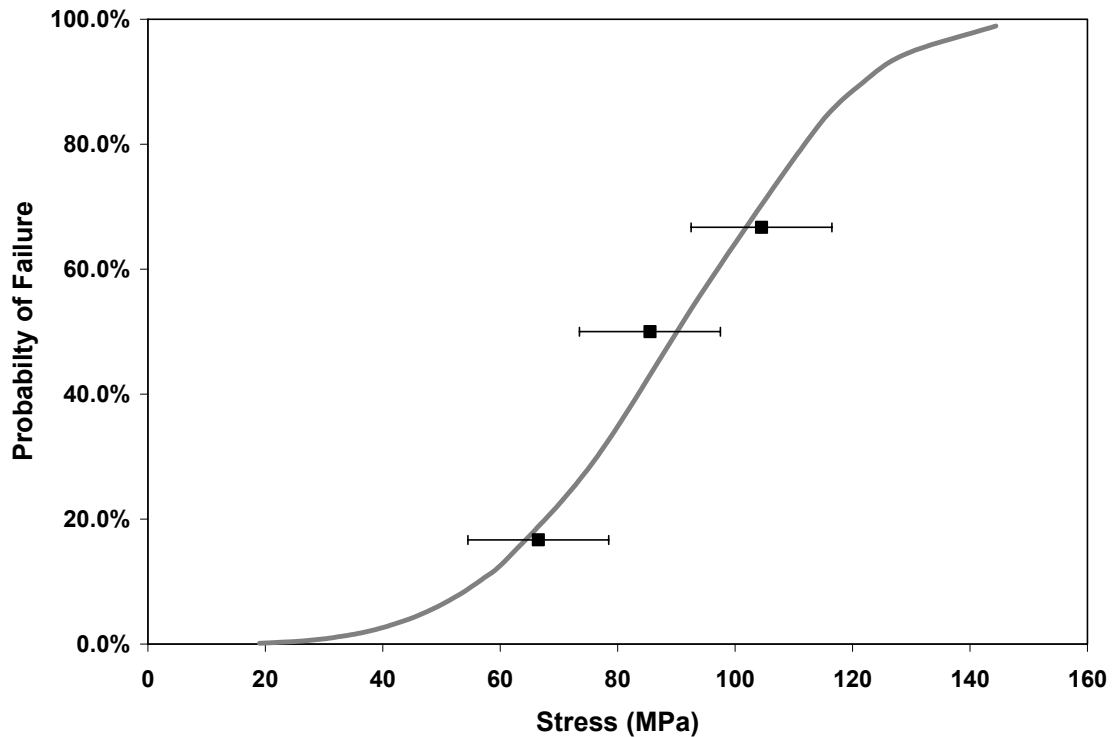


**Figure 5-23: Cal-Chip failure data Y5V 1206 capacitor**

The computed Weibull modulus for the defective Cal-Chip Y5V 1206 capacitors is shown in Table 22. These values are much lower and not reflective of a 2 mm deflection specified capacitor such as those from TDK. A plot of the failure model with the experimental results is shown in Figure 5-24.

**Table 23: Computed Weibull modulus from experimental data**

Dielectric Type	Capacitor width	Characteristic Strength 67% Failure (MPa)	Weibull modulus
Cal-Chip 1206, Y5V	1.524	75.2	3.9



**Figure 5-24: Cal-Chip Y5V failure model and experimental results**

### 5.2.8 Capacitor failure model summary

Experimental results from four major capacitor manufacturers have been used to develop manufacturer specific capacitor failure parameters and to demonstrate the technique for using the analytical stress model with a Weibull failure model. The steps for developing the failure parameters involved:

1. Converting printed wiring board deflections into equivalent pwb moments using basic beam equations
2. Converting these moments into capacitor stresses using the developed analytical model
3. Plotting the probability of capacitor failure as a function tensile stress

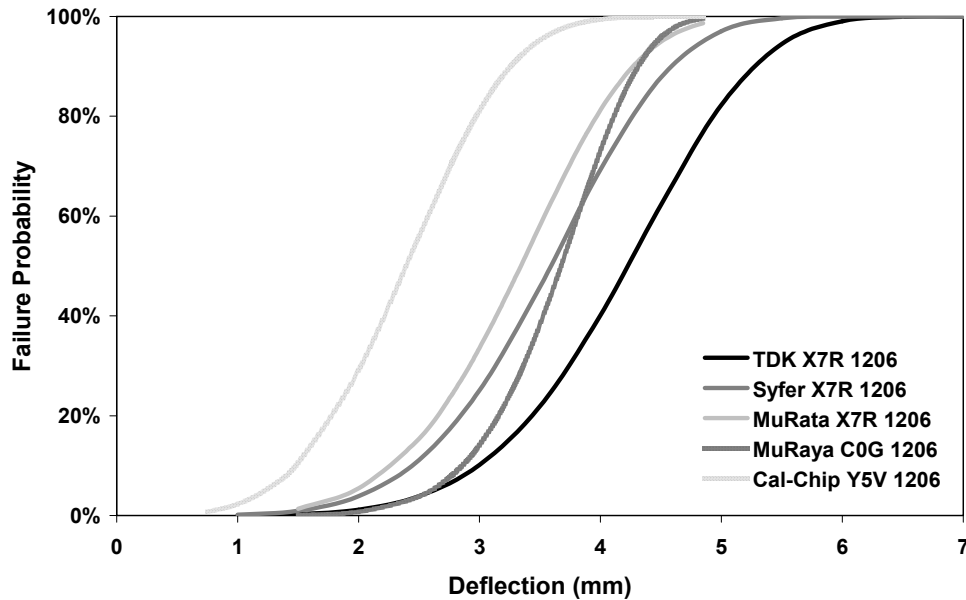


4. Fitting a Weibull distribution to the data and obtaining the Weibull modulus and characteristic strength at 67% failure, the capacitor width at which the values are taken must be retained in the failure model. This width is divided into the width of the capacitor for which failure is to be predicted.

A comparison of the failure behavior between five manufacturers for a 1206 size capacitor on a 1.6 mm thick FR-4 printed wiring board is shown in Figure 5-25.

Capacitors from TDK, Cal-Chip and Syfer are rated to 2 mm maximum deflection while the MuRata capacitors are only rated to a 1 mm maximum deflection limit (see Table 3 ).

The capacitors from Cal-Chip had defects present that may have compromised the strength of the capacitors. The results indicate that the capacitors from TDK are much stronger than the other X7R capacitors and that the presence of micro-cracking may have reduced the durability of the Cal-Chip capacitors.



**Figure 5-25: Manufacturer comparison, 1206 size capacitor**

### 5.3 Failure model, ceramic chip resistors

Flexural failure of ceramic chip resistors is far less common than ceramic capacitor failures because of the high strength of the alumina used in chip resistor construction. As stated previously there are two failure modes, resistor body cracking and end metallization separation. Experimental results indicate that these two failure modes can occur at the same stress levels [41]. These failure modes both have the same initiation sites with the difference being only in the direction of crack propagation. Therefore, this behavior suggests that only one failure model is necessary to cover both these modes. Thus, failure is defined as crack initiation and the subsequent direction of the crack is irrelevant. Experimental results for resistor failures are shown in Table 24. The stress values in column three are computed using the analytical model. These values agree with

published values for bulk alumina, which are typically around 380 MPa [48]. The characteristic strength and Weibull modulus from published data is shown in Table 25.

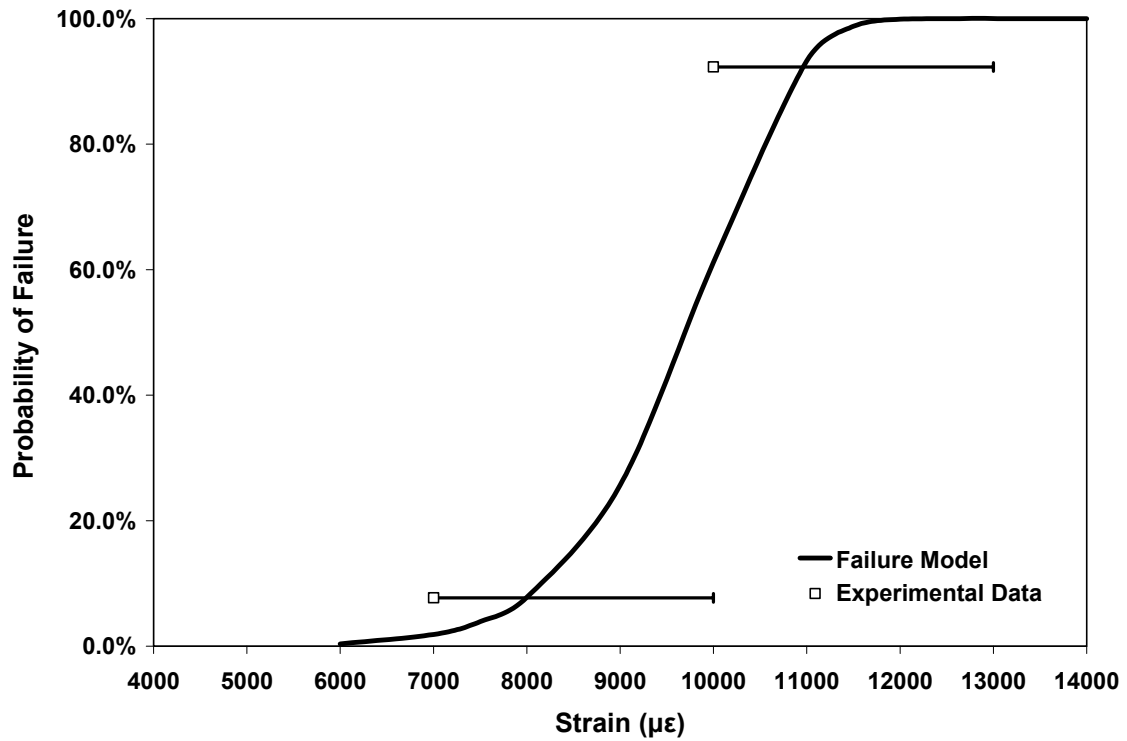
**Table 24: Failure Data, 1206 Size Resistor [35]**

Test Set	Number of Failures	Board Strain ( $\mu\epsilon$ )	Tensile Stress (MPa)
A	3	10,000 – 14,000	356 - 500
B	1	10,000 – 14,000	356 - 500
C	1	7,000 - 10,000	249 - 356
D	4	10,000 – 14,000	356 – 500
E	2	10,000 – 14,000	356 - 500
F	2	10,000 – 14,000	356 - 500

Using the provided Weibull modulus as the failure model the predictions for the failure of the chip resistor as a function of board level strain is shown in Figure 5-26.

**Table 25: Weibull modulus from published data [48]**

Material	Characteristic Strength 67% Failure (MPa)	Weibull modulus
Alumina	395	11



**Figure 5-26: Surface mount resistor failures. 1206 size**

The model predicts failure of the resistors in the measured intervals for the test data.

#### 5.4 Summary

The analytical model has been shown to provide stress values that can be used in a stress Weibull based failure model. This failure model can then be used to predict the failures various sized capacitors and resistors. Manufacturer dependent failure parameters have been developed for the analytical stress model but should be adequate for use in finite element analyses. The techniques used can be extended to other surface mount chip devices such as ferrite beads and varistors.

## **CHAPTER 6 SOFTWARE IMPLEMENTATION**

In this section, the analytical stress model and the failure models are implemented into an online web based calculator. The goal is to provide an engineer with a tool to rapidly assess the probability of failure for leadless chip capacitors and resistors. This will be accomplished by developing a straight forward, flexible, and intuitive interface that links to a software engine that handles the calculations. The calculator will consist of two parts.

1. HyperText Markup Language (HTML) and Javascript interface webpage
2. Java based analytical stress and failure model applet

### **6.1 Javascript, HTML interface**

The use of HTML and Javascript to construct the user interface allows for rapid development and platform portability. The inputs and results are displayed as text which makes printing the interface with the results very easy. The interface, which is shown in Figure 6-1 uses a variety of methods for inputting the necessary parameters for the analytical model.

Pull down menus are used to enter selections for which the parameters reside within the java calculator. These parameters are predefined as to speed up the data entry process and to control the inputs to ranges or values for which the model has been verified.

Capacitor Cracking Calculator (v2.0) - Microsoft Internet Explorer

File Edit View Favorites Tools Help

Address |

## Capacitor Cracking Calculator

### Probability of MLCC Cracking Due To Printed Wiring Board Bending

Version 2.0

---

This program calculates the probability of cracking an MLCC during PWB bending. Initially the form contains typical values for each entry, clicking on the Compute button at the bottom of the form will display the corresponding results. This allows the user to become familiar with the routine and see some typical results. The capacitor is assumed to be placed on the PWB at the point of greatest deflection.

---

<b>Reset The Form:</b>	<input type="button" value="Reset"/>
MLCC Manufacturer:	<input type="text" value="Generic, 2 - mm"/>
Dielectric Type:	<input type="text" value="X7R"/>
MLCC Size:	<input type="text" value="1206"/> Thickness: <input type="text" value="1.0"/> [mm]
Solder Fillet Shape:	<input type="text" value="nominal"/>
Solder Material:	<input type="text" value="PbSn"/>
Solder Pad Width:	<input type="text" value="100"/> [% of chip width (85-125)]
Solder Pad Length:	<input type="text" value="1.0"/> [mm]
Solder Thickness:	<input type="text" value="0.0635"/> [mm], Typically between 0.0254 and 0.127
PWB Thickness:	<input type="text" value="1.6"/> [mm]
PWB Modulus:	<input type="text" value="17000"/> [MPa]
Applied PWB :	<input type="text" value="0.002"/> <input type="text" value="strain [%"/>
<b>Compute Results:</b>	<input type="button" value="Compute"/>
<b>Capacitor Stress:</b>	<input type="text" value=""/> [MPa]
<b>Probability of Capacitor Failure:</b>	<input type="text" value=""/> %

---

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Applet started. My Computer

**Figure 6-1: Analytical model interface**

Selections that are predefined are:

1. MLCC manufacturer
2. Dielectric type
3. MLCC size
4. Solder fillet shape
5. Solder material
6. Applied PWB load type

The values for these selections reside within the java applet that implements the analytical calculations. The source code for the HTML interface can be found in Appendix 10.3.1. Once the variables are entered and selected a button is pressed that sends the values as strings to the java applet.

## **6.2 Java Applet, analytical model**

The JavaScript interface passes the variables as strings to the Java applet. In the case of inputted numbers, the strings are converted to actual floating point numbers and assigned to the corresponding variable. The results of the menu selections are also passed as strings. These strings are compared to strings in the applet that have predefined values associated with them.

### **6.2.1 Internally defined variables**

The first set of internally defined variables is associated with the capacitor manufacturer. The manufacturer has associated with it the variables that define the failure behavior of

the capacitor. Currently there are five different choices for the capacitor manufacturer as shown in Figure 6-2.

Reset The Form:	Reset
MLCC Manufacturer:	Generic, 1 - mm
Dielectric Type:	Generic, 1 - mm
	Generic, 2 - mm
MLCC Size:	Syfer
	muRata
	TDK
Solder Fillet Shape:	TDK
	1.0 [mm]

**Figure 6-2: Manufacturer selection**

Associated with these selections are the values of the Weibull modulus and characteristic strength of the capacitors that define the failure behavior, as detailed in chapter 5.

The next pull down menu selects the dielectric type, as shown in Figure 6-3.

Reset The Form:	Reset
MLCC Manufacturer:	Generic, 2 - mm
Dielectric Type:	X7R
	Y5V
	X7R
	NP0, COG
MLCC Size:	X7R
	Y5V
	NP0, COG
Solder Fillet Shape:	TDK
	1.0 [mm]

**Figure 6-3: Dielectric type selection**

The size selection for the capacitor involves two inputs. The pull down menu selects the industry standard size designation and the second is a numerical input for the thickness.



MLCC Size:	1206	Thickness:	1.0	[mm]
Solder Fillet Shape:	1206			
Solder Material:	0805			
Solder Pad Width:	0603			
Solder Pad Length:	1210			
Solder Thickness:	1808			% of chip width (85-125)]
PWB Thickness:	1812			
	1825			[mm]
	2220			
	2225			[mm], Typically between 0.0254 and 0.127
	3640			
	0000			[mm]

**Figure 6-4: Capacitor size and thickness entry**

The fillet shape selection has three choices, as shown in Figure 6-5.

Solder Fillet Shape:	nominal
Solder Material:	nominal
Solder Pad Width:	starved
	bulbous
	% of chip width (85-125)]

**Figure 6-5: Fillet shape selection**

These descriptors refer to the joint factor coefficient specified in section 3.2.2.1.

The solder material selection is fixed to PbSn until experimental data becomes available to validate the model for different solder, such as lead-free.

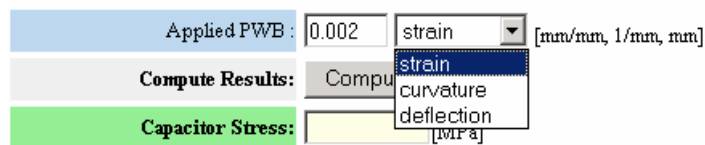
### 6.2.2 Externally defined variables

These variables are inputted into the fields of the interface. They are then passed as strings to the applet, converted and assigned to the appropriate variable. The following variables are passed to the applet.

1. Capacitor thickness
2. Solder pad width expressed as a percentage of capacitor width
3. Solder pad length
4. Solder thickness
5. Printed wiring board thickness
6. Printed wiring board modulus
7. Applied PWB strain, curvature or deflection

The applied PWB input has a pull down menu associated with it, shown in Figure 6-6.

This menu identifies the type of the input. These are percent strain, curvature or deflection. The deflection entry is based upon a simply supported beam with a length of 90 mm.



**Figure 6-6: PWB load type selection**

All the inputs or selections are passed as strings. An error message is displayed if no value is passed or if the values are outside the acceptable ranges.

### 6.2.3 Computations

After all the variables are assigned the applet implements the necessary equations to compute the capacitor stress and probability of failure, as detailed in chapters 2 through 4.

The java code for the model can be found in Appendix 10.3.2.

## CHAPTER 7 CASE STUDIES

To illustrate the use of the analytical model three case studies were conducted on industry sponsored failure analyses. Both case studies involve the failure of ceramic capacitors due to board bending. The first case study deals with failures due to printed wiring board assembly and the second involves the failures of capacitors that were later discovered to be defective.

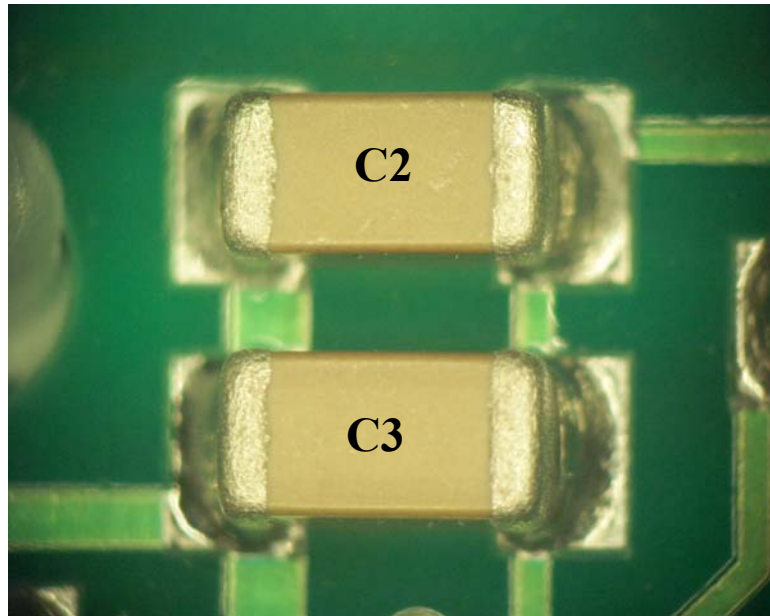
### 7.1 Ceramic chip capacitor cracking, medical product

The developed failure models for ceramic chip capacitors were applied to verify the failure of a medical product during testing. The manufacturer of the device began to experience an unacceptable reject rate of the product after a temperature/humidity screen of 40°C/90%RH for eight hours. When the failure rate increased, the company performed a failure analysis to determine root-cause. The failure mode of the rejects was described as high off-state current leakage. Electrical analysis traced the failure site to two multilayer ceramic capacitors (MLCCs), C2 and C3.

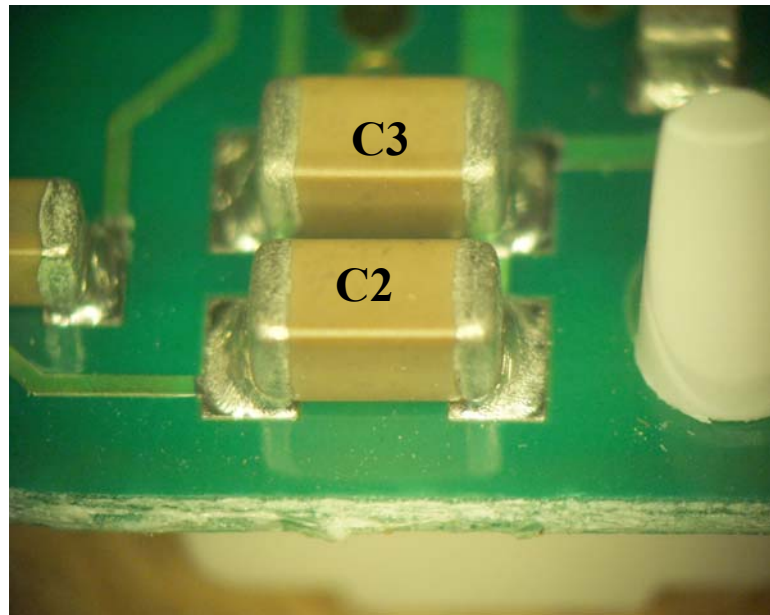
Investigation by the capacitor supplier Vishay Vitramon seemed to indicate that the failure mechanism of the ceramic capacitors was cracking due to excessive flexure of the board during the manufacturing process. The company then requested an independent analysis to review these findings.

### 7.1.1 Initial inspection

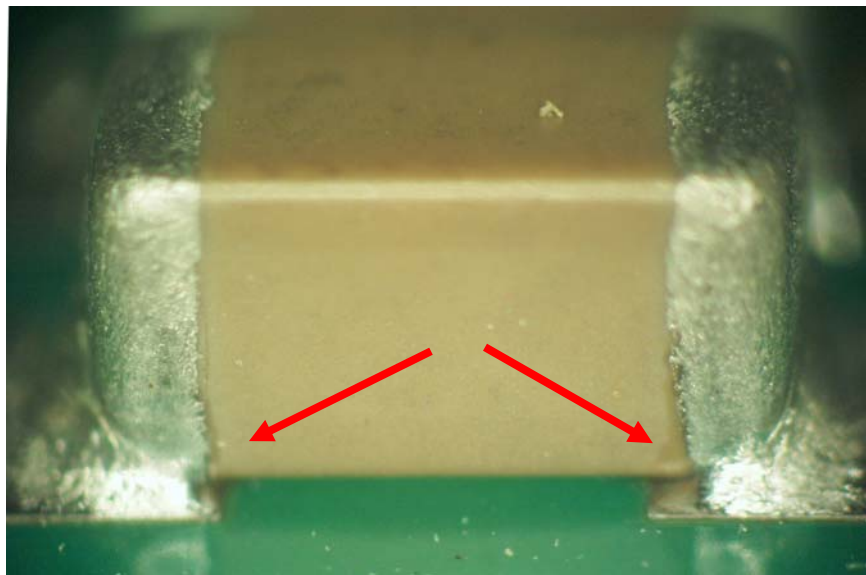
A systematic approach to the root-cause analysis was taken, proceeding from the least-destructive to the most-destructive until root-cause is conclusively identified. The first step in this process is visual inspection. Two samples were subjected to visual inspection with the unassisted eye. A more detailed inspection, performed at 20x using a Nikon stereoscope, was conducted to identify any gross defects. The results of visual inspection are displayed in Figure 7-1, Figure 7-2, Figure 7-3, and Figure 7-4.



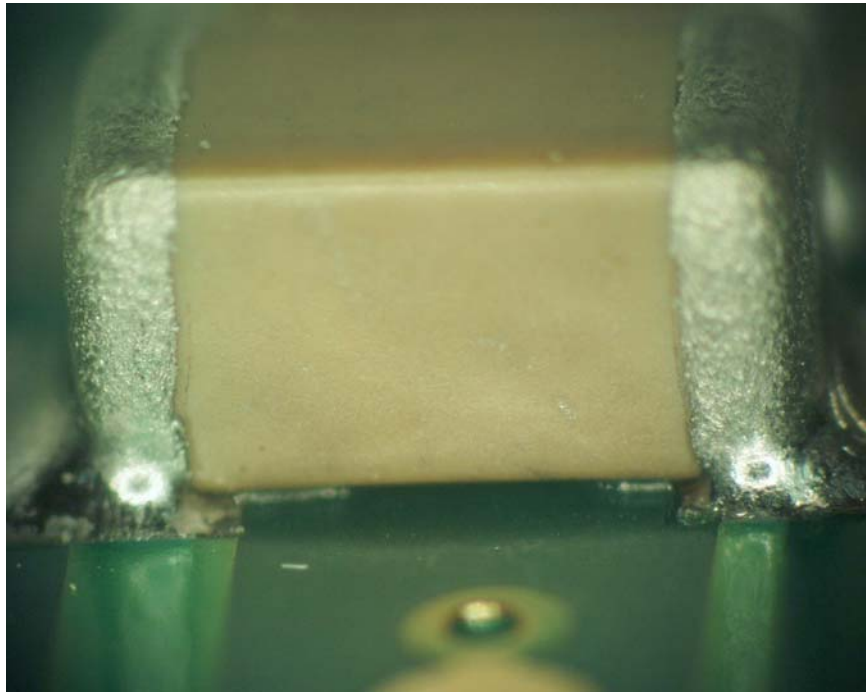
**Figure 7-1: (16.5x) Top view of capacitors C2 and C3**



**Figure 7-2: Low angle image of capacitors C2 and C3**



**Figure 7-3: Optical micrograph of C2, arrows mark the potential cracks**



**Figure 7-4: Optical micrograph of capacitor C3**

The capacitors C2 and C3 on two sample boards were then electrically isolated by severing traces leading to the capacitors. Capacitance and leakage current measurements were then performed using a Sencore Model LC53 Capacitance Meter. The results from electrical measurements are displayed in Table 26.

**Table 26: Electrical measurements of C2 and C3**

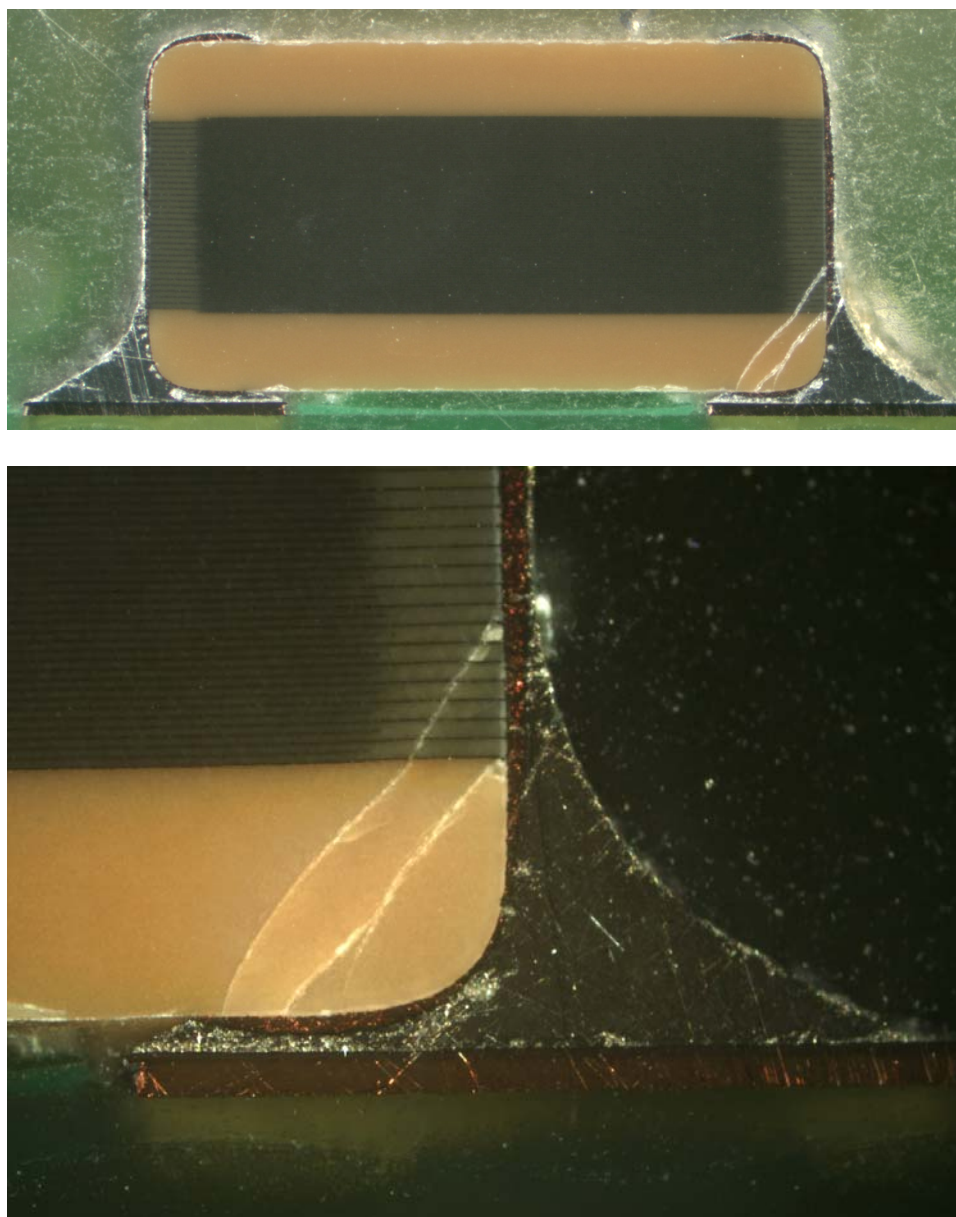
Sample	Capacitor	Capacitance ( $\mu$ farads)	Leakage Current ( $\mu$ amps)
Board 1	C2	0.475	0.00
	C3	0.477	0.00
Board 2	C2	0.492	0.00
	C3	0.479	0.00

While the visual inspection indicated that cracks might exist in at least one of the capacitors, the electrical measurements were inconclusive, with all measured capacitors showing nominal capacitance and no leakage current.

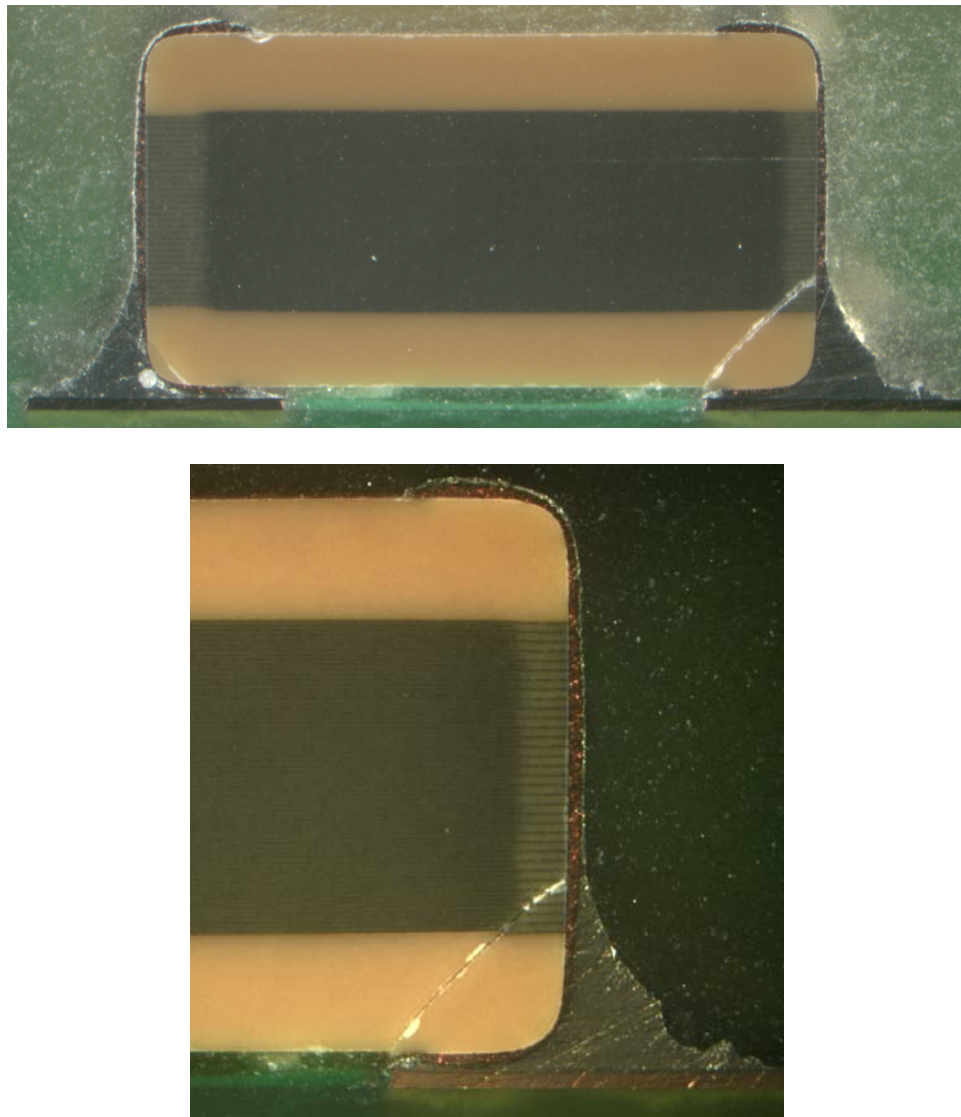
#### 7.1.2 Cross sectioning

Capacitor C1 and C2 on the devices were subjected to cross-sectioning. The capacitors were first mounted in a room-temperature cure epoxy. The additional rigidity prevents relative motion during material removal. The capacitors were ground to approximately one fourth the device width using 600 and 1200 grit silicon carbide paper. The results are displayed in Figure 7-5 and Figure 7-6.





**Figure 7-5: Optical micrographs of cross-sectioned capacitor C1**



**Figure 7-6: Optical micrographs of cross-sectioned capacitor C2**

The capacitors, while testing good showed evidence of cracks. The cracks were determined to be caused by excessive board flexure. This determination is based upon the morphology of the crack, which initiates at the metal termination and propagates at a 45 degree angle through the capacitor.

### 7.1.3 Root cause determination

To initiate effective corrective and preventative actions, it was necessary to identify the root-cause of the flex cracking. Since the products had not been shipped to the customer, reviews of the various stages of the assembly process were characterized to identify possible flex events. The manufacturer applied strain gauges to their assembly in the location of the faulty capacitors and the board was run through the manufacturing processes. A summary of the results of this set of measurements are displayed in Table 27.

**Table 27: Manufacturing Strain Measurements**

<b>Assembly Condition</b>	<b>Maximum strain (<math>\mu\epsilon</math>) measured</b>
In Circuit Test – series 1	947
In Circuit Test – series 2	977
In Circuit Test – series 3	1029
Depaneling	981
LCD Insertion	389

### 7.1.4 Analytical model, failure probability

The capacitors used were from Vishay and other manufacturers. The capacitors from Vishay were general purpose, X7R dielectric, and size 1206. These capacitors have a deflection rating of 1 mm. Since manufacturer failure data was unavailable the failure model for MuRata capacitors was used, as a conservative assumption, since MuRata

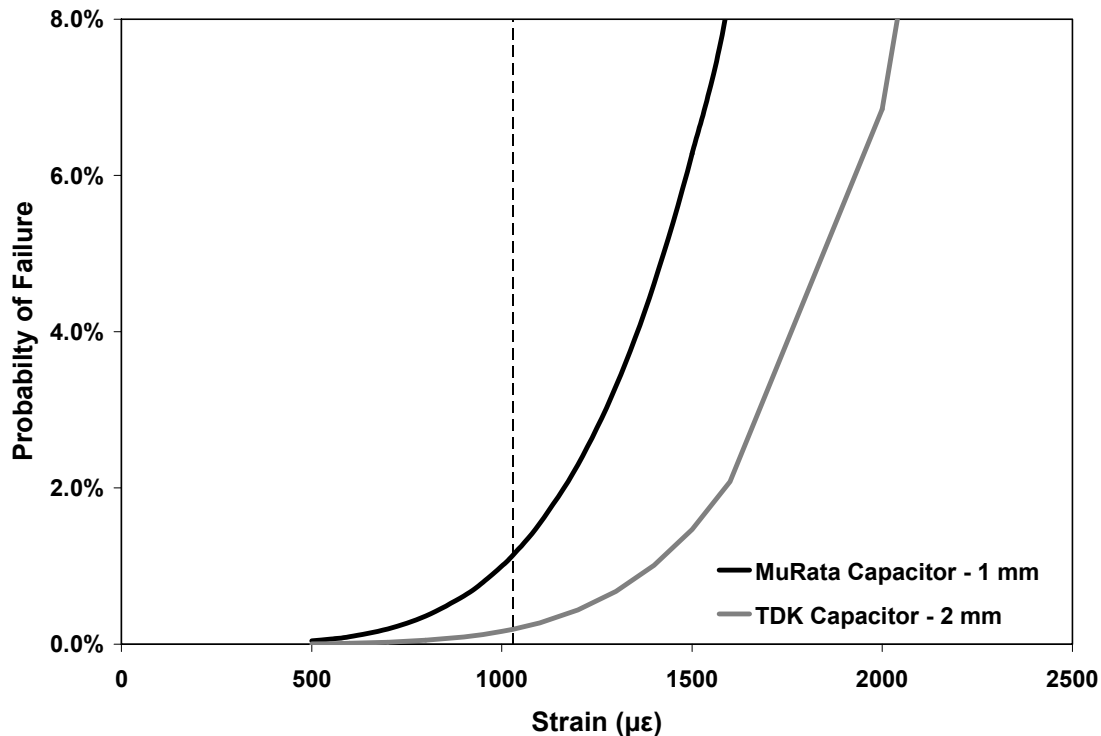
capacitors also feature a 1 mm deflection specification. The inputs to the analytical model are shown in Table 28.

**Table 28: Inputs to analytical model**

<b>Parameter</b>	<b>Value</b>
Capacitor Length	3.048 mm
Capacitor Width	1.524 mm
Capacitor Thickness	1.27 mm
PWB Thickness	0.8 mm
Solder Joint Thickness	0.03 mm
Solder Pad length	1.5 mm
Solder Fillet	0.7

The failure probability as a function of board level strain is shown in Figure 7-7.

As shown in the graph, the 1 mm deflection capacitors have a 1% chance of failing at a board level strain of 1029  $\mu\epsilon$ . The 2 mm deflection capacitors have a failure probability of less than 0.1% at the same strain level.



**Figure 7-7: Failure probability as a function of board strain**

#### 7.1.5 Corrective actions

A 1% probability of failure is unacceptable on a high volume product. As an example, the customer set the maximum fallout during screen, where the failures were detected, as 160 ppm (0.016%). Based upon the strain measurements and model predictions corrective actions were suggested to reach this level.

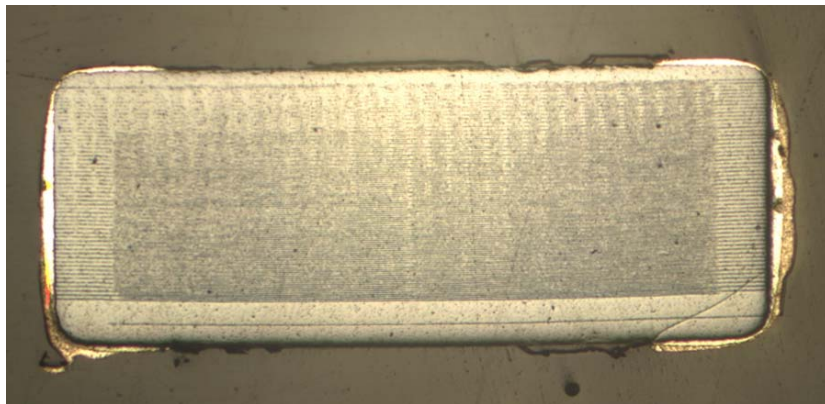
The first corrective action was to use capacitors that have a 2 mm deflection specification, such as those from TDK. Changing capacitors alone would reduce the failure probability by a factor of 10, to about 0.1 %. Additionally, it was recommended that the manufacturer find ways to limit board bending during assembly. The two critical

assembly steps were the in-circuit testing and the depaneling operation. If 1 mm capacitors are used these strain levels must not exceed  $450 \mu\epsilon$  to obtain a failure probability of 0.016%. The use of 2 mm capacitors increases the allowed board strain levels to around  $700 \mu\epsilon$ .

## 7.2 Ceramic chip capacitor cracking, military product

The manufacturer of a military product was experiencing an unacceptably high level of field returns. Root cause analysis identified capacitor cracking as the reason (see Figure 7-8).

The purpose of this exercise was to quantify the board-level strain that arose during depanelization and standoff attachment to confirm the root-cause of the failures. To initiate this investigation, the company provided printed wiring board panels. Each panel consisted of four boards each.

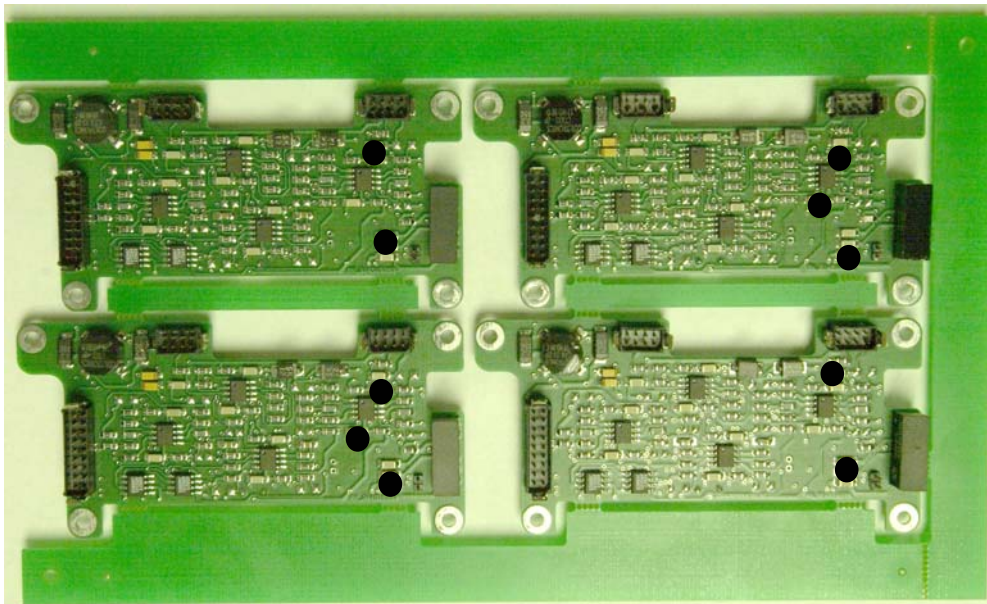


**Figure 7-8: Flex cracking in a capacitor**

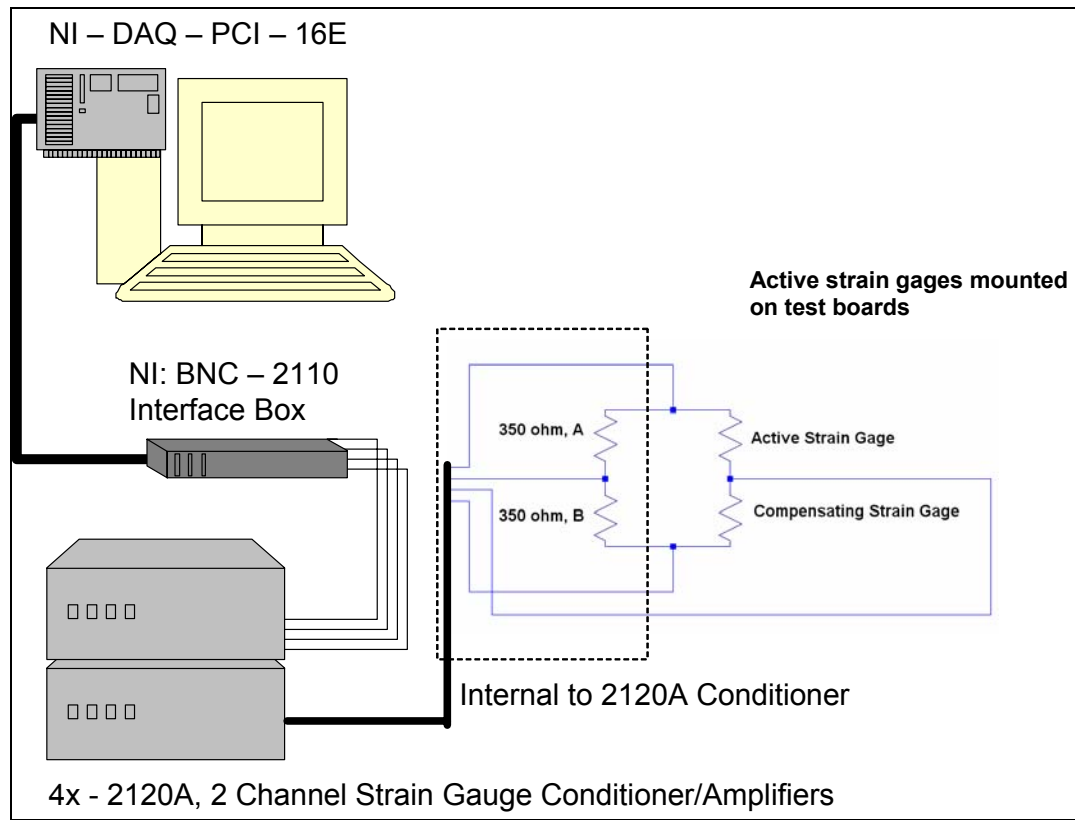
### 7.2.1 Experimental testing

The first step of the study was to investigate and identify the board-level strains present in the board during depaneling and chassis mounting. The measurement of board-level strain was performed by removing the capacitors of concern and applying a strain gauge to the board in the area of interest. The black dots in Figure 7-9 indicate the locations where the strain gauges were mounted. The data acquisition system diagrammed in Figure 7-10 was used to record the strain values.

After instrumentation, the panel was subjected to a manual depaneling process. An example is shown in Figure 7-11.



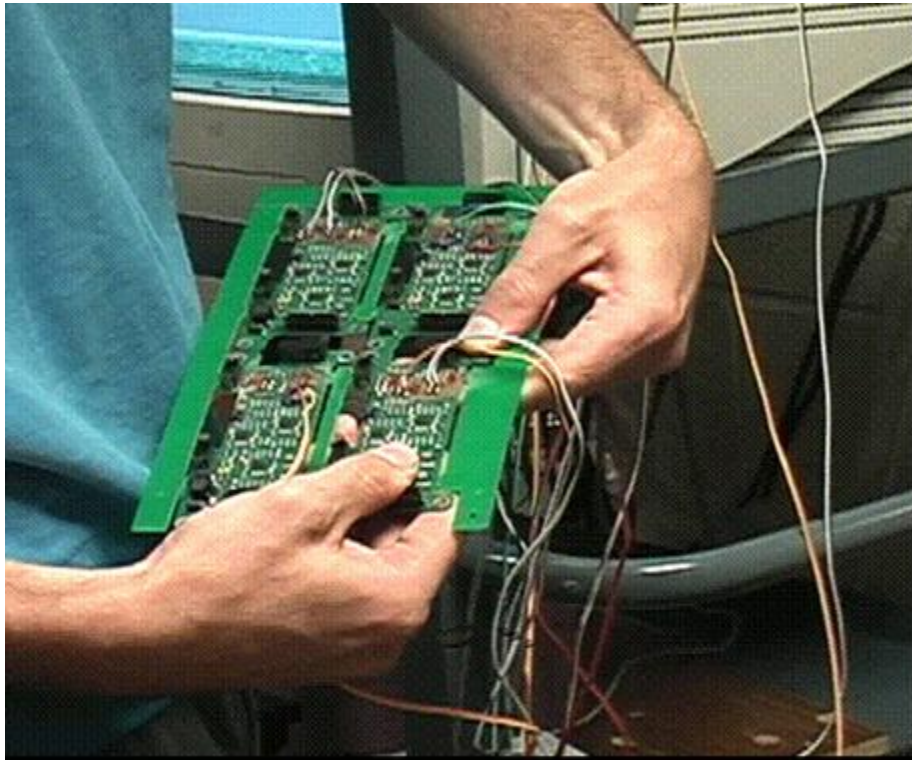
**Figure 7-9: Test panel with strain gauge locations marked as black dots**



**Figure 7-10: Data acquisition system**

The strain values recorded during the depaneling operation are displayed in Figure 7-12.

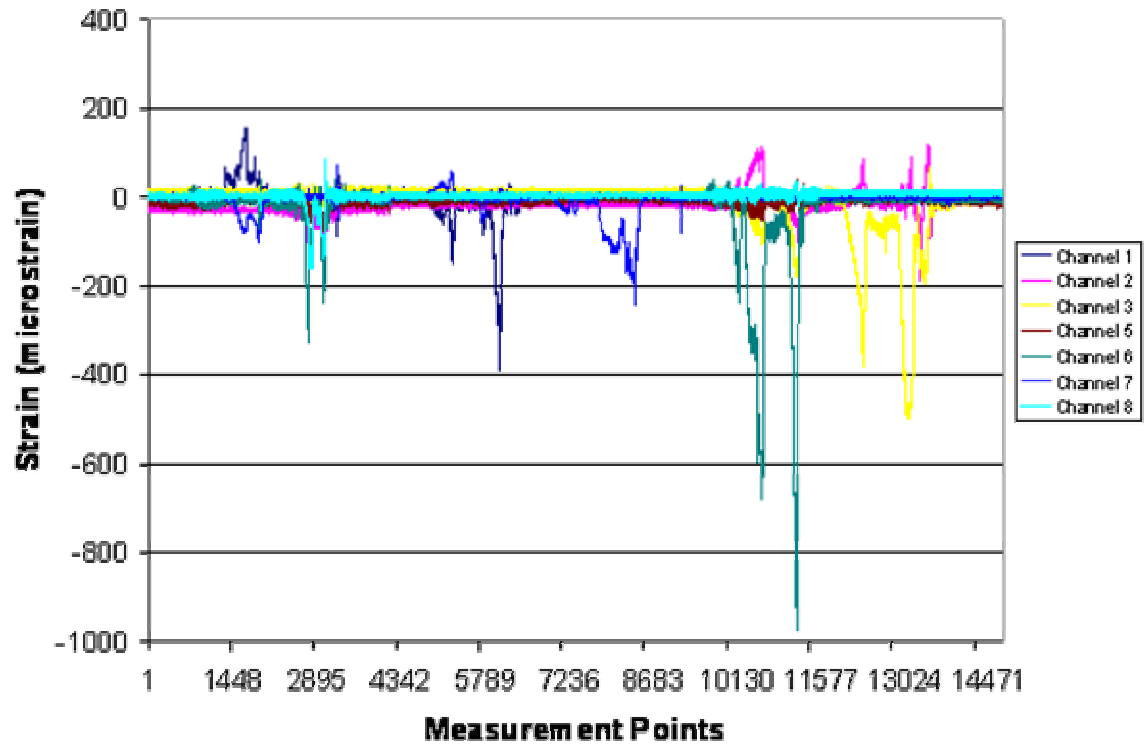




**Figure 7-11: Hand depaneling operation**

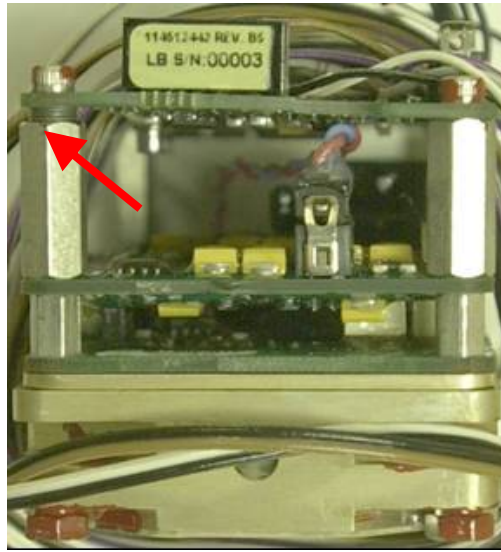
The maximum strain value recorded during the depaneling operation was approximately 980  $\mu\epsilon$ .

Next the board was subjected to chassis mounting with a shim added to one of the standoffs to simulate misalignment, as shown in Figure 7-13.

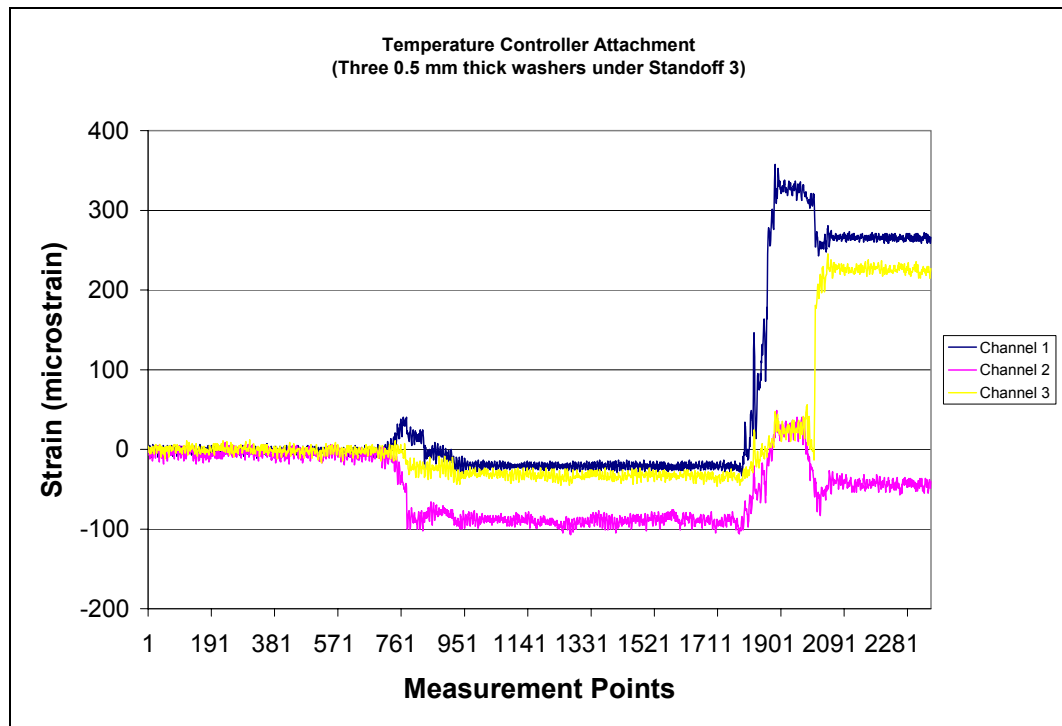


**Figure 7-12: Strain measurements during depaneling**

Three washers were used to achieve 1.5 mm of misalignment, based on tolerances on one standoff. The mounting screws of the board were then tightened to the manufacturers specified torque values. The recorded strain values are shown in Figure 7-14. The maximum strain value recorded during the chassis mounting operation was approximately 350  $\mu\epsilon$ .



**Figure 7-13: Chassis mounting with simulated misalignment**



**Figure 7-14: Strain measurements during mounting**

### 7.2.2 Analytical model, failure probability

The next step was to calculate the probability of failure for the maximum strains seen during the testing, which were approximately 940  $\mu\epsilon$ . The analytical model was used with the input shown in Table 29.

**Table 29: Inputs to analytical model**

<b>Parameter</b>	<b>Value</b>
Capacitor Length	3.048 mm
Capacitor Width	1.524 mm
Capacitor Thickness	1.00 mm
Capacitor End Margin	0.5 mm
PWB Thickness	1.6 mm
Solder Joint Thickness	0.035 mm
Solder Pad length	1.3 mm
Solder Fillet, Nominal	0.7

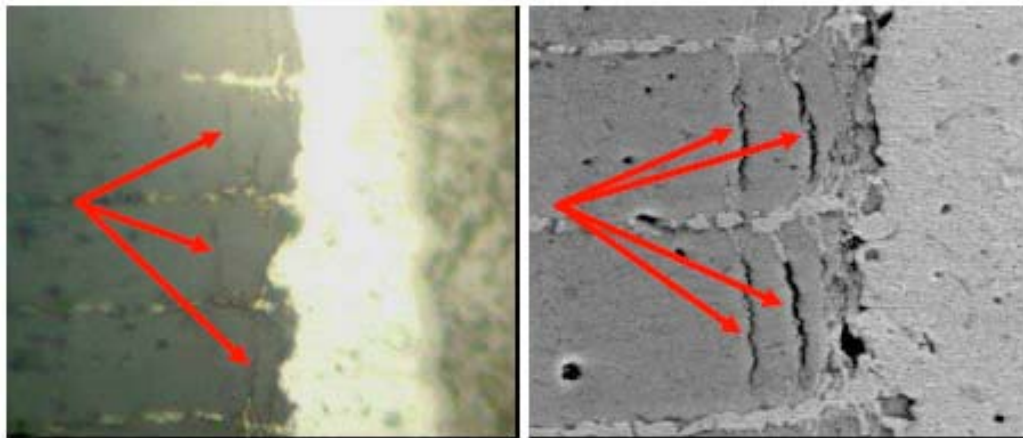
The failure model used was that for capacitors from Syfer, MuRata and TDK which are 1 and 2 mm spec capacitors, since no test data was available for the Cal-Chip capacitors used on the boards.

The results from the analytical and failure model are shown in Figure 7-17. According to these results the 2 mm spec capacitors should have between 0.01% and a 0.05% probability of failure and the 1 mm spec capacitors should have a failure probability

around 0.08%. This is much less than the observed field return percentages. Further investigation into the failure behavior of the Cal-Chip capacitors was needed.

### 7.2.3 Cal-Chip capacitor microscopy

To investigate the quality of the capacitors additional optical and electron microscopy was performed. Optical inspection revealed a manufacturing defect known as micro-cracking. Micro-cracks are typically a result of excess electrode material being deposited in the end margin. This excess metallization causes excessive residual stresses to develop in the ceramic near the end-cap which leads to the micro-cracking. The details of the micro-cracks observed are shown in Figure 7-15. Further experiments were conducted to assess the strength of these defective capacitors and to develop an appropriate failure model.

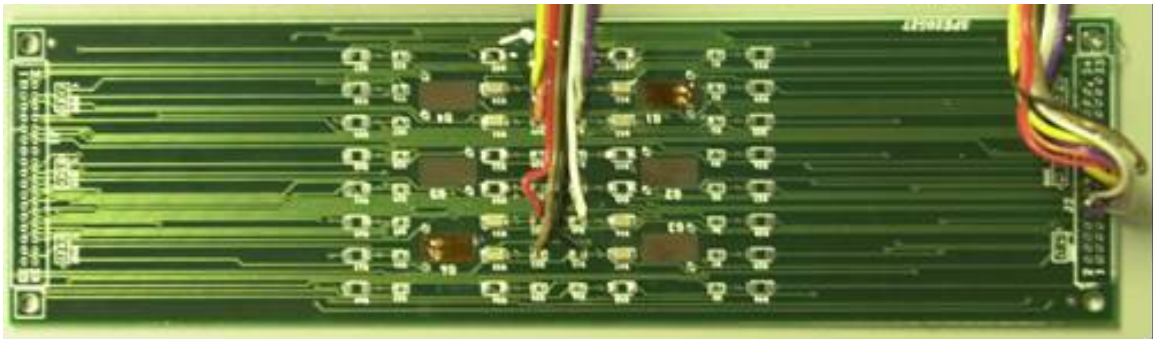


**Figure 7-15: Micro-cracking in Cal-Chip Y5V capacitor (optical and ESEM images)**

#### 7.2.4 Cal-Chip capacitor bend testing

The test coupon utilized is a custom design that was specifically developed for conducting four point bend tests on 1206 and 0603 sized components. It is a four layer FR4 board and is 0.062 inches thick and is shown in Figure 7-16 . Eight capacitors and two strain gauges were mounted on the test coupon.

The board was placed into the MTS machine and subjected to deflections that produced board surface strain values in 500  $\mu\epsilon$  increments. The results of the testing are shown in Table 30.



**Figure 7-16: Bend test coupon**

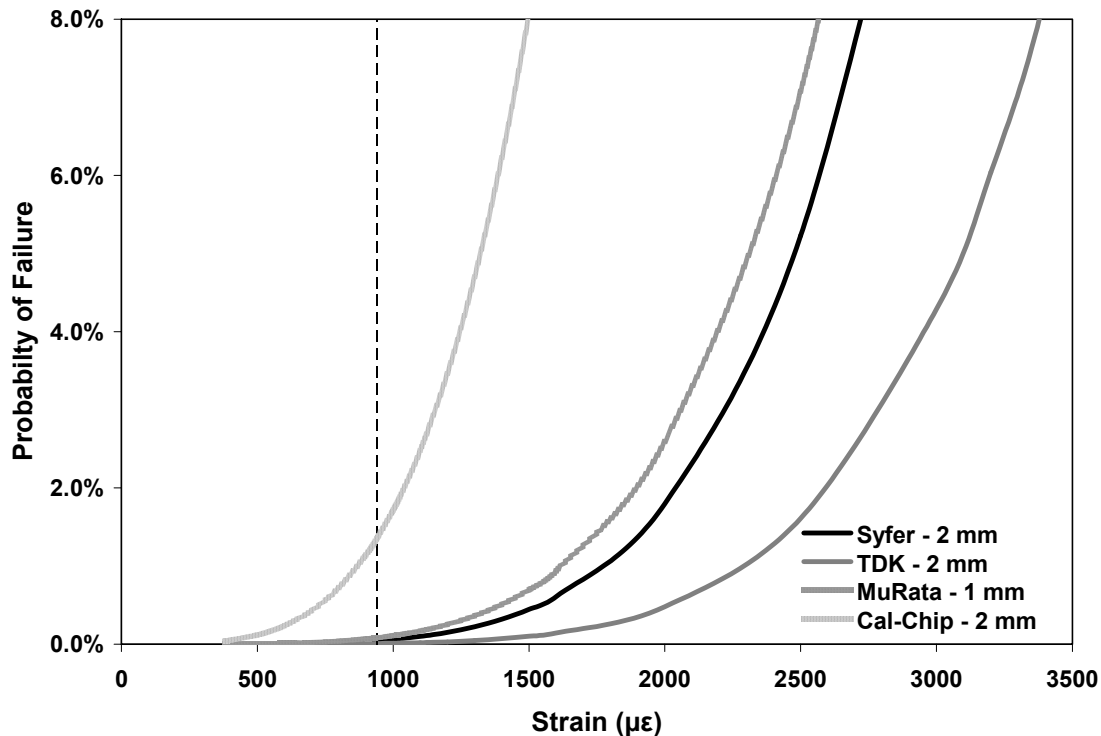
These results were used to develop the Cal-Chip capacitor failure model in section 5.2.7.

**Table 30: Bend testing results, Cal-Chip Capacitor**

<b>Identifier</b>	<b>Capacitance (<math>\mu\text{F}</math>)</b>		<b>Failure Strain (<math>\mu\epsilon</math>)</b>
	<b>Before Bend Testing</b>	<b>After Bend Testing</b>	
C1	1.07	0.21	2000 – 2500
C2	1.07	0.12	2000 – 2500
C3	1.07	0.12	2500 – 3000
C4	1.07	1.07	> 3000
C5	1.07	0.60	1500 – 2000
C6, C7, C8	1.07	1.08	> 3000

#### 7.2.5 Cal-Chip capacitor analytical results

Using the new failure model, the analytical model was exercised again to compare the Cal-Chip capacitors to other capacitors. The results are shown in Figure 7-17.



**Figure 7-17: Probability of failure, board depaneling with Cal-Chip capacitor**

The results show that at the observed strain levels the Cal-Chip capacitor has a probability of failure 17 times higher than capacitors from MuRata, 27 times higher than capacitors from Syfer, and 135 times higher than capacitors from TDK. Since the Cal-Chip capacitors are rated similarly to those from TDK and Syfer one would expect a similar failure behavior.

#### 7.2.6 Corrective actions

The failure probability of the defective capacitors was shown to be too high by the number of field returns and the analytical model. The main recommendation was to stop using the defective capacitors from Cal-Chip and to rework the boards to replace the

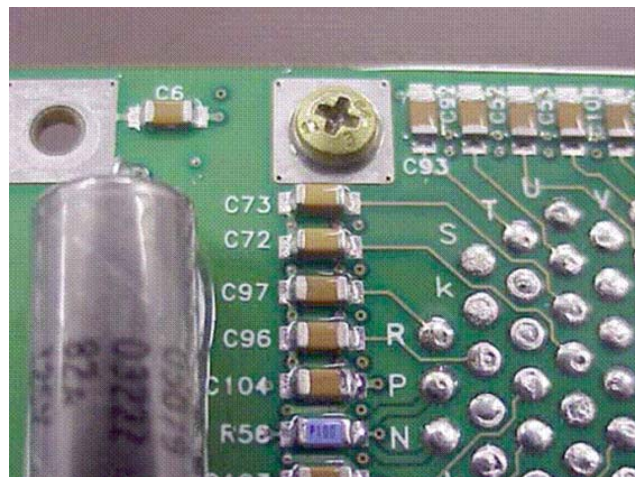


defective capacitors. As predicted by the model, normal capacitors of both 1 and 2 mm deflection should have very low failure probabilities under the applied printed wiring board bending. Additional robustness can be gained by using 2 mm specified capacitors from a well known manufacturer like TDK.

### 7.3 Ceramic chip capacitor cracking, defense product

The developed failure models for ceramic chip capacitors were applied to verify the failure of a defense product. This is a high reliability product and the manufacturer was experiencing a 5% failure rate during product qualification because of capacitor cracking.

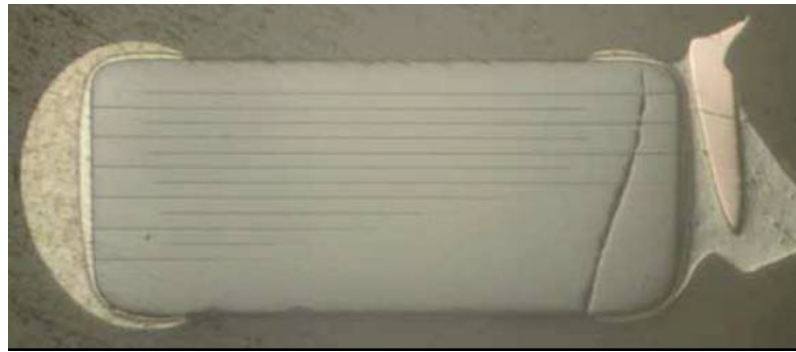
Root cause investigation identified capacitor C73, as shown in Figure 7-18, as the cause of the failure. Based upon the capacitors location, the cause of the failure was suspected to be cracking due the development of strain during tightening of standoffs to the board or standoffs to the housing mechanism.



**Figure 7-18: Failed capacitor C73, next to board standoff**

### 7.3.1 Cross-sectioning

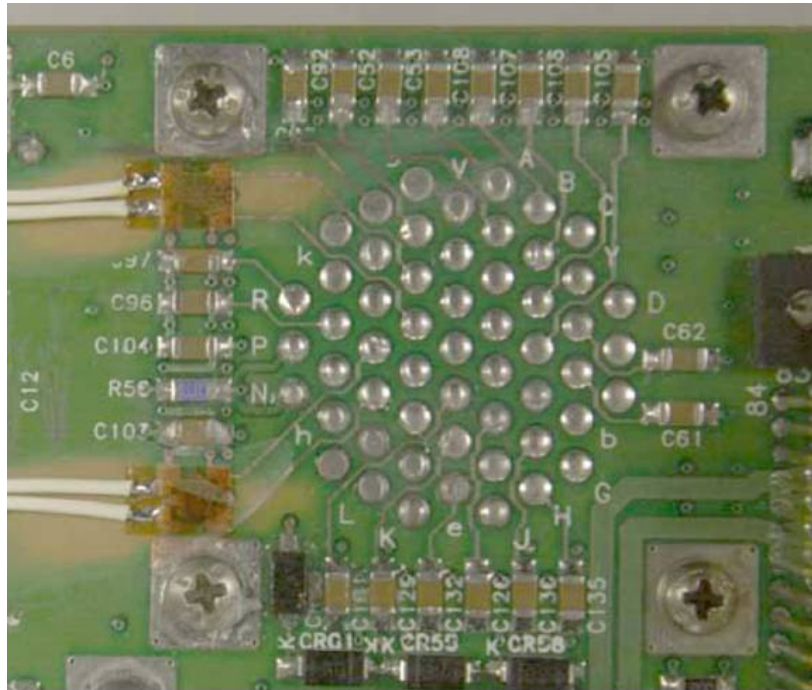
Capacitor C73 was removed and cross-sectioned to identify the failure. As shown in Figure 7-19, the capacitor had a crack present that was consistent with those associated with flexural failures.



**Figure 7-19: (32x) Optical micrograph of C73**

### 7.3.2 Experimental testing

Two capacitors were removed from the board at locations close to the standoffs. Strain gages were mounted in these locations, as shown in Figure 7-20, so that the strain values during board mounting and connector attachment could be monitored and recorded. The data was collected in two steps. Step one involved the mounting of the board to the chassis, as shown in Figure 7-21 and step two involved attaching the connectors to the chassis, as shown in Figure 7-22. The strain values were recorded as the mounting screws were tightened to specified torque amounts.



**Figure 7-20: Strain gage mounting locations, C73 and C63**



**Figure 7-21: Board to chassis mounting**



**Figure 7-22: Connector to chassis mounting**

The strains recorded at various torque levels are shown in Table 31 and Table 32.

**Table 31: Surface strain measured at location of capacitor C73**

Torque (cN-m)	Board Surface Strain (microstrain)		Comments
	Standoff to Board	Standoff to Housing	
20	-23	291	
40	-76	699	
60	-93	699	
80	-93	723	
100	-105	1026	Stripped one standoff

**Table 32: Surface strain measured at location of capacitor C63**

Torque (cN-m)	Board Surface Strain (microstrain)		Comments
	Standoff to Board	Standoff to Housing	
20	52	449	
40	76	425	
60	76	583	
80	117	723	
100	146	874	Stripped one standoff

As shown in the tables the higher strain corresponded to higher torque settings. The manufacturer had specified a torque setting of 80 cN·m and strain values of 723 were recorded at both locations at this setting.

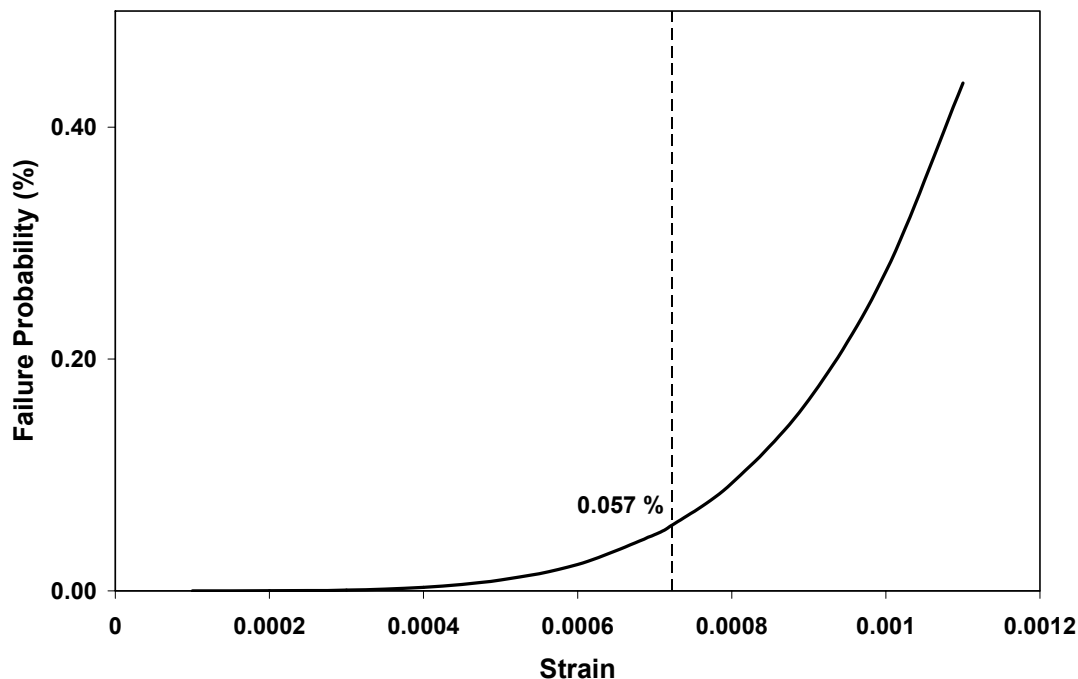
### 7.3.3 Capacitor analytical results

The values used in the analytical capacitor failure model are shown in Table 33. These values were determined by measurements taken from the actual device. The capacitors were reported to be manufactured by AVX with a 2 mm deflection specification. Since failure data for AVX capacitors was unavailable the failure parameters developed for Syfer capacitors was used.

**Table 33: Inputs to analytical model**

<b>Parameter</b>	<b>Value</b>
Capacitor Length	3.048 mm
Capacitor Width	1.524 mm
Capacitor Thickness	1 mm
Capacitor End Margin	0.5 mm
PWB Thickness	1.6 mm
Solder Joint Thickness	0.035 mm
Solder Pad length	1.7 mm
Solder Fillet, Nominal	0.7

As shown in Figure 7-23, at these strain levels the capacitor should have a failure probability of less than 0.06 %.



**Figure 7-23: Probability of capacitor failure as a function of PWB strain**

#### 7.3.4 Discussion

The analytical model did not predict flexural failures based upon the results of the tests. In a previous case study the discrepancy was experienced because of defective capacitors. In this case the capacitors did not appear to be defective. There are three other potential reasons for the discrepancy. One, the capacitors could be counterfeit and less robust to flex events than the capacitors from the intended supplier or the strain values measured may be lower than those actually present. There is also the possibility that the manufacturer was just extremely unlucky, based on the limited sample set (20

assemblies) this may be a possibility. The recommendations to the manufacturer were to verify the authenticity of the capacitors, limit the torque settings to 60 cN·m, and to consider applying strain relief between standoffs.

#### **7.4 Summary**

The analytical model has been employed in a series of case studies to illustrate its application and usefulness. The results of these studies confirmed the root cause of the failures and provided the companies the information required to facilitate corrective actions.

## CHAPTER 8 CONCLUDING REMARKS

The value of this research effort has been in identifying the physical mechanism that initiates failure in ceramic bodies attached to a glass fiber/epoxy matrix composite in a non-compliant manner, assessing the response of this mechanism to various geometries and mechanical loading conditions, and developing an analytical model that allows the user to assess risk during the design phase and to determine the root cause of field failures.

Previous attempts at resolution have failed to address the root-cause (Mode I stress condition in the ceramic capacitor). As a result, they are of limited value, especially to the end user, and prevent the designer the ability for a more nuanced assessment of risk (prior work focused on go/no-go)

Development of a closed form analytical model for rapidly assessing the failure of leadless ceramic chip components has been completed and applied to ceramic chip resistors and capacitors. The model utilizes classical approaches to structures and fracture to make failure predictions. The model is comprised of two sections, the stress analysis, and probability of failure analysis.

The stress analysis model has been verified and modified based upon the results of numerous 2D and 3D finite element models. Modification of the model utilizes a stress concentration factor and an additional shear spring to represent the surface behavior of

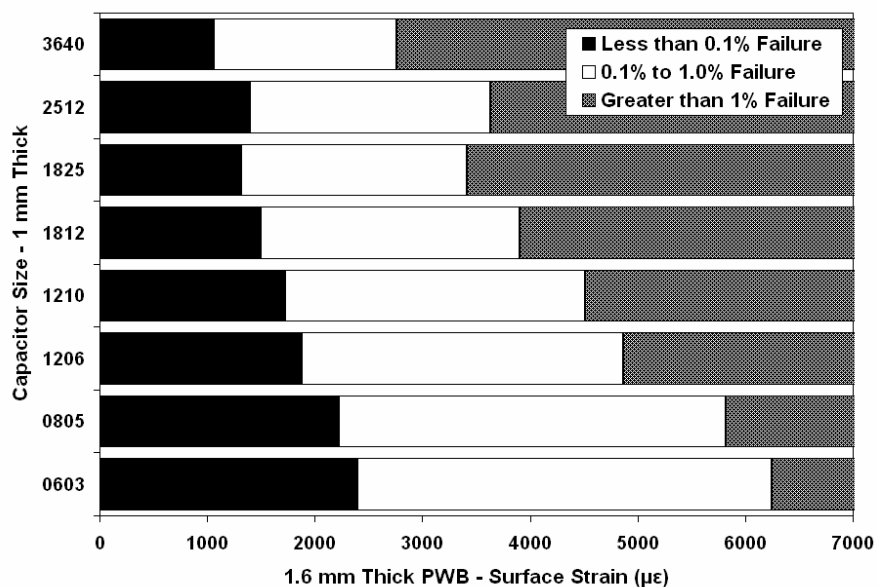


the printed wiring board. These are relatively simple equations that are easily explained. The resulting maximum stresses of the device are very close to those predicted by FEA.

These stresses are then used in Weibull based failure models to predict the probability of component failure with regards to printed wiring board bending. Failure parameters from literature for alumina have been shown to provide relatively good predictions of chip resistor failures with the stress values computed by the analytical stress model. Further accuracy can be obtained by using available manufacturer test data to develop manufacturer specific failure models.

The analytic model does deviate from the manufacturer test data with regard to low stress level failures. The reasons for this may reside in the test standards the manufacturers use for these tests. The standard specifies that a drop in capacitance or visual cracks indicate a failure. This criterion eliminates the capturing of two types of failures, non-visual cracks that do not intersect the electrodes, or non-visual cracks that do not drop the capacitance enough to be registered as a failure. The current standard therefore makes some cracking acceptable. This is not adequate because it fails to recognize that the crack may propagate under additional thermal or mechanical stresses. The analytical model assumes that any cracking is a reliability concern and should be avoided. In this regard the model actually seems to predict failures closer to those seen in the field and demonstrated by the case studies.

The analytical model can be used to generate part survivability plots that are functions of various part geometric parameters. Assuming an acceptable failure probability range between of 0.1% and 1% a plot can be generated for the use of various size components under board flexure type loads. An example graph for the acceptable surface strain values for 1 mm thick capacitors (2 mm deflection specification) of various sizes is shown in Figure 8-1.



**Figure 8-1: Acceptable strain values for various size capacitors**

Graphs such as these can be developed for a variety of geometric configurations and can greatly aid designers by allowing them to set strain limits for their designs.

## CHAPTER 9 FUTURE WORK

The closed form analytical model developed can be extended to handle a variety of leadless chip components. The failures of devices such as varistors, and ferrite beads could be predicted after suitable failure parameters are developed and validated.

Currently, the model is only validated for standard tin-lead eutectic solder. It could be extended to calculate the failure of leadless chip components that are connected with lead-free solders. There seems to be conflicting theories on the effects that solders such as tin silver copper (SnAgCu) will have on board flexing related failures. SnAgCu is the prime candidate solder in the United States to replace PbSn for lead-free soldering. Some tests indicate that the modulus may be lower than that of eutectic tin-lead. However, solder manufacturers categorize SnAgCu as a stiff solder, relative to tin-lead. Initial calculations using the analytical stress model using SnAgCu properties determined by Weise [47] indicate that the probability of failure may increase with this solder. Mechanical testing of SnAgCu and bend testing of soldered components must be carried out before this can be validated.

## CHAPTER 10 APPENDICES

### 10.1 Capacitor dimensions

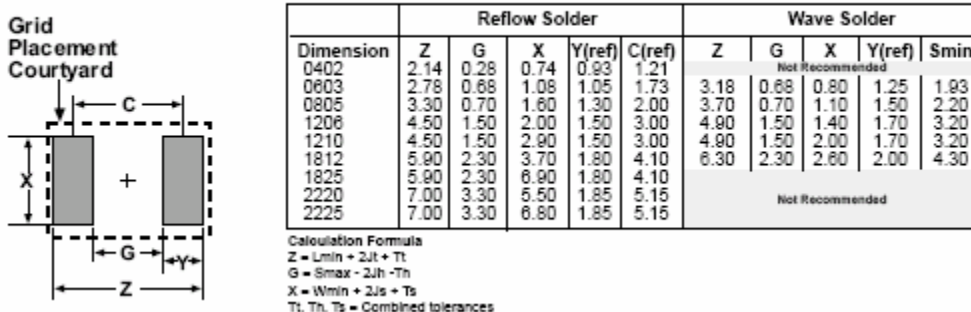
**THICKNESS CODE REFERENCE CHART**  
**PACKAGING QTY BASED ON FINISHED CHIP THICKNESS SPECIFICATIONS**

Thickness Code	Chip Size	Chip Thickness Range (mm)	Qty per Reel Plastic	Qty per Reel 7"	Qty per Reel 13" Plastic	Qty per Reel Paper	Qty per Reel 7"	Qty per Reel 13" Paper	Qty per Bulk Cassette
AA	0201	.30 ± .03	N/A	N/A	N/A	15,000	N/A	N/A	N/A
BB	0402	.50 ± .05	N/A	N/A	N/A	10,000	50,000	50,000	50,000
CB	0603	.80 ± .07	N/A	N/A	N/A	4,000	10,000	15,000	15,000
CC	0603	.80 ± .10	N/A	N/A	N/A	4,000	10,000	N/A	N/A
DB	0805	.60 ± .10	N/A	N/A	N/A	N/A	N/A	10,000	10,000
DC	0805	.78 ± .10	4,000	10,000	4,000	10,000	10,000	N/A	N/A
DD	0805	.90 ± .10	4,000	10,000	N/A	N/A	N/A	N/A	N/A
DE	0805	1.00 ± .10	2,500	10,000	N/A	N/A	N/A	N/A	N/A
DF	0805	1.10 ± .10	2,500	10,000	N/A	N/A	N/A	N/A	N/A
DG	0805	1.25 ± .15	2,500	10,000	N/A	N/A	N/A	N/A	N/A
DH	0805	1.25 ± .20	2,500	10,000	N/A	N/A	N/A	N/A	N/A
EB	1206	.78 ± .10	4,000	10,000	4,000	10,000	N/A	N/A	N/A
EC	1206	.90 ± .10	4,000	10,000	N/A	N/A	N/A	N/A	N/A
ED	1206	1.00 ± .10	2,500	10,000	N/A	N/A	N/A	N/A	N/A
EE	1206	1.10 ± .10	2,500	10,000	N/A	N/A	N/A	N/A	N/A
EF	1206	1.20 ± .15	2,500	10,000	N/A	N/A	N/A	N/A	N/A
EG	1206	1.60 ± .15	2,000	8,000	N/A	N/A	N/A	N/A	N/A
EH	1206	1.60 ± .20	2,000	8,000	N/A	N/A	N/A	N/A	N/A
EJ	1206	1.70 ± .20	2,000	8,000	N/A	N/A	N/A	N/A	N/A
FB	1210	.78 ± .10	4,000	10,000	N/A	N/A	N/A	N/A	N/A
FC	1210	.90 ± .10	4,000	10,000	N/A	N/A	N/A	N/A	N/A
FD	1210	.95 ± .10	4,000	10,000	N/A	N/A	N/A	N/A	N/A
FE	1210	1.00 ± .10	2,500	10,000	N/A	N/A	N/A	N/A	N/A
FF	1210	1.10 ± .10	2,500	10,000	N/A	N/A	N/A	N/A	N/A
FG	1210	1.25 ± .15	2,500	10,000	N/A	N/A	N/A	N/A	N/A
FH	1210	1.55 ± .15	2,000	8,000	N/A	N/A	N/A	N/A	N/A
FJ	1210	1.85 ± .15	2,000	8,000	N/A	N/A	N/A	N/A	N/A
FK	1210	2.10 ± .20	2,000	8,000	N/A	N/A	N/A	N/A	N/A
GB	1812	1.00 ± .10	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GC	1812	1.10 ± .10	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GD	1812	1.25 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GE	1812	1.30 ± .10	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GF	1812	1.50 ± .10	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GG	1812	1.55 ± .10	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GH	1812	1.40 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
GJ	1812	1.70 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
HB	1825	1.10 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
HD	1825	1.30 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
HE	1825	1.40 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
HF	1825	1.50 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
JB	2220	1.00 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
JC	2220	1.10 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
JD	2220	1.30 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
JE	2220	1.40 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
JF	2220	1.50 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
KB	2225	1.00 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
KC	2225	1.10 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
KD	2225	1.30 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A
KE	2225	1.40 ± .15	1,000	4,000	N/A	N/A	N/A	N/A	N/A

This chart refers to ceramic chip thickness codes on pages 50-53.

**Figure 10-1: Kemet capacitor thickness chart [34]**

**SURFACE MOUNT LAND DIMENSIONS - CERAMIC CHIP CAPACITORS - MM**



**Figure 10-2: Kemet capacitor solder pad dimensions [34]**

**X7R CAPACITANCE RANGE – 0402, 0603, 0805, 1206**

CAP PF	CAP CODE	CAP TOL	C0402*					C0603*					C0805*					C1206*										
			6.3V	10V	16V	25V	50V	6.3V	10V	16V	25V	50V	100V	200V	6.3V	10V	16V	25V	50V	100V	200V	6.3V	10V	16V	25V	50V	100V	200V
150	151	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
180	181	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
220	221	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
270	271	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
330	331	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
390	391	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
470	471	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
560	561	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
680	681	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
820	821	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
1000	102	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
1200	122	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
1500	152	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
1800	182	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
2200	222	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
2700	272	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
3300	332	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
3900	392	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
4700	472	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
5600	562	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
6800	682	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
8200	822	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
10,000	103	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
12,000	123	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
15,000	153	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
18,000	183	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
22,000	223	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
27,000	273	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
33,000	333	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
39,000	393	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
47,000	473	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
56,000	563	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
68,000	683	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
82,000	823	K,M,J	BB	BB	BB	BB	BB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB	CB
100,000	104	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
120,000	124	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
150,000	154	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
180,000	184	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
220,000	224	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
270,000	274	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
330,000	334	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
390,000	394	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
470,000	474	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
560,000	564	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
680,000	684	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
820,000	824	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
1,000,000	105	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
1,200,000	125	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
1,500,000	155	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
1,800,000	185	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#
2,200,000	225	K,M,J	BB	BB	BB	BB	BB	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#	CB#

\* Indicates EIA preferred chip sizes.  
 NOTE: For non-standard capacitance values or voltages, contact your local KEMET sales representative.  
 # X7R dielectric - Extended Range Values - Cap and DF measured @ 0.5 Vrms.

**Figure 10-3: Capacitor thickness codes [34]**

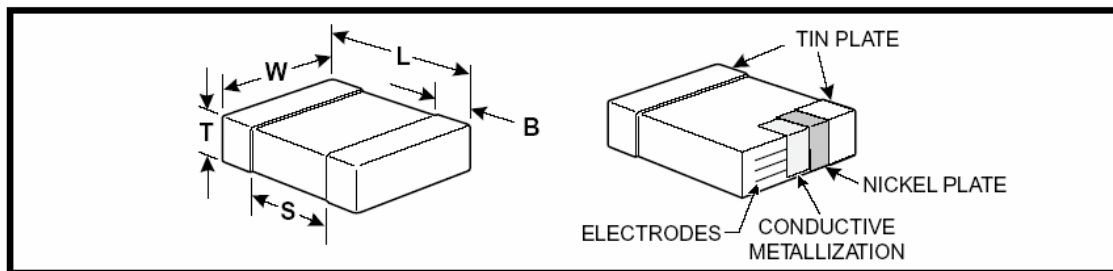
X7R CAPACITANCE RANGE – 1210, 1812, 1825, 2220, 2225

CAP. PF	CAP CODE	CAP. TOL.	C1210*							C1812*			C1825*			C2220			C2225		
			6.3V	10V	16V	25V	50V	100V	200V	50V	100V	200V	50V	100V	200V	50V	100V	200V	50V	100V	200V
2200	222	K,M,J	FB	FB	FB	FB	FB	FB	FB												
2700	272	K,M,J	FB	FB	FB	FB	FB	FB	FB												
3300	332	K,M,J	FB	FB	FB	FB	FB	FB	FB												
3900	392	K,M,J	FB	FB	FB	FB	FB	FB	FB												
4700	472	K,M,J	FB	FB	FB	FB	FB	FB	FB												
5600	562	K,M,J	FB	FB	FB	FB	FB	FB	FB												
6800	682	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB									
8200	822	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB									
10,000	103	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB									
12,000	123	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB									
15,000	153	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB									
18,000	183	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB									
22,000	223	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB						
27,000	273	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB						
33,000	333	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB						
39,000	393	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB						
47,000	473	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB						
56,000	563	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB					KC	KC
68,000	683	K,M,J	FB	FB	FB	FB	FB	FB	FB	GB	GB	GB	HB	HB	HB					KC	KC
82,000	823	K,M,J	FB	FB	FB	FB	FB	FC	FC	GB	GB	GB	HB	HB	HB					KC	KC
100,000	104	K,M,J	FB	FB	FB	FB	FB	FC	FC	GB	GB	GB	HB	HB	HB					KC	KC
120,000	124	K,M,J	FB	FB	FB	FB	FB	FC	FC	GB	GB	GB	HB	HB	HB					KC	KC
150,000	154	K,M,J	FC	FC	FC	FC	FC	FC	FC	GB	GB	GB	HB	HB	HB					KC	KC
180,000	184	K,M,J	FC	FC	FC	FC	FC	FC	FC	GB	GB	GB	HB	HB	HB					KC	KC
220,000	224	K,M,J	FC	FC	FC	FC	FC	FC	FC	GB	GB	GB	HB	HB	HB					KC	KC
270,000	274	K,M,J	FC	FC	FC	FC	FC	FC#	FD#	GB	GB	GB	HB	HB	HB					KC	KC
330,000	334	K,M,J	FD	FD	FD	FD	FD	FD#	FD#	GB	GB	GB	HB	HB	HB					KC	KC
390,000	394	K,M,J	FD	FD	FD	FD	FD	FD#	FD#	GB	GB	GB	HB	HB	HB					KC	KC
470,000	474	K,M,J	FD	FD	FD	FD	FD	FD#	FD#	GB	GB	GB	HB	HB	HB					KC	KC
560,000	564	K,M,J	FD	FD	FD	FD	FD	FD#	FD#	GC	GC	GC	HD	HD	HD					KC	KC
680,000	684	K,M,J	FD	FD	FD	FD	FD	FD#	FD#	GC	GC	GC	HD	HD	HD					KC	KC
820,000	824	K,M,J	FF	FF	FF	FF	FF	FF#		GE	GE	GE								KC	KC
1,000,000	105	K,M,J	FH	FH	FH	FH	FH	FH#												KD	KD
1,200,000	125	K,M,J	FH	FH	FH	FH	FH														
1,500,000	155	K,M,J	FH	FH	FH	FH	FH														
1,800,000	185	K,M,J	FH	FH	FH	FH	FH														
2,200,000	225	K,M,J	FJ	FJ	FJ	FJ	FJ														

\* Indicates EIA preferred chip sizes.  
 NOTE: For non-standard capacitance values or voltages, contact your local KEMET sales representative.  
 50 Volt Ceramic Chips can be used for 63 volt applications.  
 # Extended Range Values — Cap and DF measured @ 0.5 vms.

Figure 10-4: Capacitor thickness codes (continued) [34]

## CAPACITOR OUTLINE DRAWINGS



## DIMENSIONS—MILLIMETERS AND (INCHES)

EIA SIZE CODE	METRIC SIZE CODE (Ref only)	L # LENGTH	W # WIDTH	See pages 48-52 for thickness dimensions.	B BANDWIDTH	S MIN. SEPARATION	MOUNTING TECHNIQUE
0402*	1005	1.0 (.04) ± .05 (.002)	0.5 (.02) ± .05 (.002)		0.20 (0.008)-0.40 (0.016)	0.3 (.012)	Solder Reflow
0603*	1608	1.6 (.063) ± 0.15 (.006)	0.8 (.032) ± 0.15 (.006)		0.35 (.014) ± 0.15 (.006)	0.7 (.028)	Solder Wave † or Solder Reflow
0805*	2012	2.0 (.079) ± 0.2 (.008)	1.25 (.049) ± 0.2 (.008)		0.5 (.02) ± .25 (.010)	0.75 (.030)	
1206*	3216	3.2 (.126) ± 0.2 (.008)	1.6 (.063) ± 0.2 (.008)		0.5 (.02) ± .25 (.010)	N/A	Solder Reflow
1210*	3225	3.2 (.126) ± 0.2 (.008)	2.5 (.098) ± 0.2 (.008)		0.5 (.02) ± .25 (.010)	N/A	
1812	4532	4.5 (.177) ± 0.3 (.012)	3.2 (.126) ± 0.3 (.012)		0.6 (.024) ± .35 (.014)	N/A	
1825*	4564	4.5 (.177) ± 0.3 (.012)	6.4 (.252) ± 0.4 (.016)		0.6 (.024) ± .35 (.014)	N/A	
2220	5650	5.6 (.220) ± 0.4 (.016)	5.0 (.197) ± 0.4 (.016)		0.6 (.024) ± .35 (.014)	N/A	Solder Reflow
2225	5664	5.6 (.220) ± 0.4 (.016)	6.3 (.248) ± 0.4 (.016)		0.6 (.024) ± .35 (.014)	N/A	

\* Note: Indicates EIA Preferred Case Sizes (Tightened tolerances apply for 0402, 0603, and 0805 packaged in bulk cassette, see page 65.)

# Note: These thicknesses are EIA maximums. Most chips are considerably thinner. Consult factory for details. Also, some extended values may be slightly thicker than EIA maximums.

† For extended value 1210 case size - solder reflow only.

Figure 10-5: Typical capacitor dimensions [34]

## 10.2 Material properties

### 10.2.1 Solders

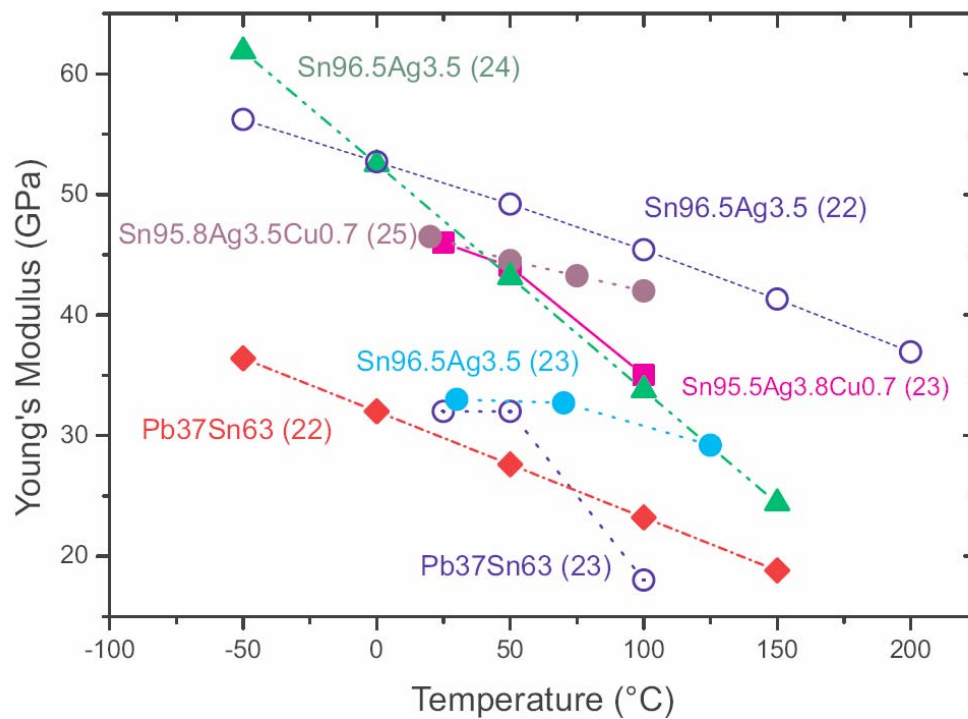
Elastic Modulus for Pb37Sn63 solder:

$$E = 27000 \text{ MPa [47]}$$

Elastic Modulus for AgCuSn solder:

$$E = 36000 \text{ to } 44000 \text{ MPa [47]}$$

Typical values compiled by Wiese of Young's Modulus from various sources.



**Figure 10-6: Solder properties [47]**



### 10.2.2 Printed wiring board

The flexural modulus for a 0.062 – 4 layer printed wiring board were determined using a 3 point bend DMA testing technique. Four boards were tested, three with metallization and one without, the results are shown in Table 34.

**Table 34: Flexural modulus of FR-4 at room temperature**

	<b>Board 44 4245544</b>	<b>Board 17 4245417</b>	<b>Board 26 4245426</b>	<b>Board No copper</b>
<b>Freq rad/sec</b>	<b>MPa</b>	<b>MPa</b>	<b>MPa</b>	<b>Baseline MPa</b>
<b>12.53</b>	20143	17542	19590	16369
<b>15.77</b>	20140	17538	19589	16383
<b>19.86</b>	20185	17567	19599	16400
<b>25.00</b>	20205	17598	19639	16419
<b>31.47</b>	20228	17642	19685	16436
<b>39.62</b>	20268	17708	19733	16474
<b>49.88</b>	20282	17773	19720	16490
<b>62.80</b>	20312	17772	19767	16525
<b>79.06</b>	20344	17856	19823	16563
<b>99.53</b>	20407	17938	19902	16622
<b>125.30</b>	20474	18049	19981	16696
<b>157.75</b>	20558	18156	20092	16772
<b>198.59</b>	20705	18315	20259	16904
<b>250.01</b>	20897	18513	20453	17071
<b>314.75</b>	21183	18822	20729	17335

10.2.3 Capacitors**Table 35: Capacitor dielectric properties**

Physical Constant	X7R	C0G (NPO)	Y5V
Elastic Modulus (MPa) [18]	110000 – 120000	120000 – 130000	90000 – 100000
Tensile Strength (MPa) [18]	62	103	43
Bending Strength (MPa) [18]	88	137	69
Coefficient of Thermal Expansion 1/°C [18]	$11 - 12 \times 10^{-6}$	$8 - 10 \times 10^{-6}$	$11 - 12 \times 10^{-6}$
Fracture Toughness (MPa.m <sup>1/2</sup> )	0.6 – 1.2 [18] 1.03 [12]	1.4 [18] 1.5 [12]	

**Table 36: Physical properties of metals used in capacitors [18]**

Physical Constant	Ag	Cu	AgPd	Sn	Ni
Elastic Modulus (Gpa)	82 [13]	110-120	150	42	210
Yield (MPa) 0.005	50-60 [13]		80		
CTE 1/°C	20 [13]				

**Table 37: Typical ceramic dielectric materials for MLCC [50]**

EIA designation	Class	Temperature range (°C)	Barium Titanate content (%)	Other dopants	Grain size (μm)
NPO (COG)	1	-55 to 125	10-50	TiO <sub>2</sub> , CaTiO <sub>3</sub> , Nd <sub>2</sub> Ti <sub>2</sub> O <sub>7</sub>	1
X7R (BX)	2	-55 to 125	90-98	MgO, MnO, Nb <sub>2</sub> O <sub>5</sub> , CoO Rare-earth	<1.5
Z5U	2	10 to 85	80-90	CaZrO <sub>3</sub> , BaZrO <sub>3</sub>	3-10
Y5V	2	-30 to 85	80-90	CaZrO <sub>3</sub> , BaZrO <sub>3</sub>	3-10

10.2.4 Capacitors**MECHANICAL & ENVIRONMENTAL CHARACTERISTICS**

	<b>SPECIFICATION</b>	<b>TEST PARAMETERS</b>
<b>SOLDERABILITY:</b>	Solder coverage 90% of metallized areas No termination degradation	Preheat chip to 120°-150°C for 60 sec., dip terminals in rosin flux then dip in Sn62 solder @ 240°±5°C for 5±1 sec
<b>RESISTANCE TO SOLDERING HEAT:</b>	No mechanical damage Capacitance change: ±2.5% or 0.25pF Q>500 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	Preheat device to 80°-100°C for 60 sec. followed by 150°-180°C for 60 sec. Dip in 260°±5°C solder for 10±1 sec. Measure after 24±2 hour cooling period
<b>TERMINAL ADHESION:</b>	Termination should not pull off. Ceramic should remain undamaged.	Linear pull force* exerted on axial leads soldered to each terminal. *0402 2.0lbs, 0603 2.0lbs (min.)
<b>PCB DEFLECTION:</b>	No mechanical damage. Capacitance change: 2% or 0.5pF Max	Glass epoxy PCB: 0.5 mm deflection
<b>LIFE TEST:</b>	No mechanical damage Capacitance change: ±3.0% or 0.3 pF Q>500 I.R. >1 G Ohms Breakdown voltage: 2.5 x WVDC	Applied voltage: 200% rated voltage, 50 mA max. Temperature: 125°±3°C Test time: 1000+48-0 hours
<b>THERMAL CYCLE:</b>	No mechanical damage. Capacitance change: ±2.5% or 0.25pF Q>2000 I.R. >10 G Ohms Breakdown voltage: 2.5 x WVDC	5 cycles of: 30±3 minutes @ -55°+0/-3°C, 2-3 min. @ 25°C, 30±3 min. @ +125°+3/-0°C, 2-3 min. @ 25°C Measure after 24±2 hour cooling period
<b>HUMIDITY, STEADY STATE:</b>	No mechanical damage. Capacitance change: ±5.0% or 0.50pF max. Q>300 I.R. = 1 G-Ohm Breakdown voltage: 2.5 x WVDC	Relative humidity: 90-95% Temperature: 40°±2°C Test time: 500 +12/-0 Hours Measure after 24±2 hour cooling period
<b>HUMIDITY, LOW VOLTAGE:</b>	No mechanical damage. Capacitance change: ±5.0% or 0.50pF max. Q>300 I.R. = 1 G-Ohm min. Breakdown voltage: 2.5 x WVDC	Applied voltage: 1.5 VDC, 50 mA max. Relative humidity: 85±2% Temperature: 40°±2°C Test time: 240 +12/-0 Hours Measure after 24±2 hour cooling period
<b>VIBRATION:</b>	No mechanical damage. Capacitance change: ±2.5% or 0.25pF Q>1000 I.R. 10 G-Ohm Breakdown voltage: 2.5 x WVDC	Cycle performed for 2 hours in each of three perpendicular directions Frequency range 10Hz to 55 Hz to 10 Hz traversed in 1 minute. Harmonic motion amplitude: 1.5mm

**Figure 10-7: Johanson Dielectrics specification page (0.5 mm) [43]**

## 10.3 Software implementation of analytical model

### 10.3.1 Interface

The HTML and Javascript code for the model interface:

[Start here]

```

<html>
<head>
<title>Capacitor Cracking Calculator (v2.0)</title>
</head>
<script language=JavaScript>
// Ceramic Chip Cracking Calculator
// by: Nathan Blattau
// CALCE University of Maryland at College Park
// Do not distribute
//
function select_item(name, value)
{
    this.name=name;
    this.value=value;
}
function get_selection(select_object)
{
    contents=new select_item();
    for (var i=0;i<select_object.options.length;i++)
    if (select_object.options[i].selected==true){
        contents.name=select_object.options[i].text;
        contents.value=select_object.options[i].value;
    }
    return contents;
}
function clearForm(form){
    form.pad_width.value="100";
    form.pwb_thick.value="1.6";
    form.pwb_deflect.value="2";
}
function computeForm(form){
    try {
        mlccMaker    = get_selection(form.cap_man).name;
        mlccSize     = get_selection(form.cap_type).name;
        solderJoint  = get_selection(form.solder_type).name;
        solderPad    = form.pad_width.value;
        pwbThickness = form.pwb_thick.value;
        pwbStrain    = form.pwb_strain.value;
        var app = document.CapCrackCalc;
    }
}

```

```

    if (app == null) {
        alert ("Java is not currently installed and/or enabled"
            + " on this browser,\nwhich means that you can't"
            + " use the best capacitor cracking\ncalculator"
            + " ever made. Sorry."
        );
        return;
    }
    app.computeResults (
        mlccMaker, mlccSize,
        solderJoint, solderPad,
        pwbThickness,
        pwbDeflection
    );
    form.cap_fail.value = app.getCapFailure();
    form.pwb_moment.value = app.getMoment();
    form.cap_stress.value = app.getStress();
} catch (ex) {
    form.cap_fail.value = "";
    msg = ex.message;
    if (msg.substring(0,21) == "java.lang.Exception: ")
        msg = msg.substring(21);
    alert (msg);
}
}
</SCRIPT><BODY vLink=#ff00ff aLink=#ffff00 link=#0000ff bgColor=#ffffff>
<CENTER>
<table border=0 cellpadding=0 cellspacing=0 width=600 style='margin:0'>
<tr><td><table border=0 cellpadding=0 cellspacing=0 width='100%'>
<tr><td align=left></td><td align=center>
<H2 style='margin:0; font-size=14pt'>Capacitor Cracking Calculator</H2>
<H3 style='margin:0; font-size=11pt'>
Probability of MLCC Cracking<br>Due To Printed Wiring Board Bending
</H3>Version 2.0</td></tr></table><HR noShade>
<p style='margin:0; font-size:10pt' align=justify>
This program calculates the probability of cracking an
MLCC during PWB bending. Initially the form contains typical values for
each entry, clicking on the Compute button at the bottom of the form
will display the corresponding results. This allows the user to become
familiar with the routine and see some typical results. The capacitor is
assumed to be placed on the PWB at the point of greatest deflection.
<HR noShade>
<style>TD { font-size: 10pt; } INPUT { font-size: 10pt; } SELECT { font-size: 10pt; }
</style><center><FORM name=form method=post style='margin:0'>
<TABLE cellSpacing=4 cellPadding=1 style='margin:0'>

```

```

<TBODY>
<TR>
<TD align=right bgcolor=#efefef><b>Reset The Form:</b></TD>
<TD><INPUT Onclick=clearForm(this.form) type=reset value=" Reset"> </TD></TR>
<TR>
<TD align=right bgcolor=#bdd6ef>MLCC Manufacturer:</TD>
<TD><SELECT name=cap_man>
  <OPTION selected>Generic, 1 - mm</option>
  <OPTION selected>Generic, 2 - mm</option>
  <OPTION>Syfer</option>
  <OPTION>muRata</option>
  <OPTION>TDK</option>
</SELECT></TD></TR>
<TR><TD align=right bgcolor=#bdd6ef>Dielectric Type:</TD>
<TD><SELECT name=diel_type>
  <OPTION selected>Y5V</option>
  <OPTION selected>X7R</option>
  <OPTION>NP0, C0G</option>
</SELECT></TD></TR>
<TR> <TD align=right bgcolor=#bdd6ef>MLCC Size:</TD>
<TD><SELECT name=cap_type>
  <OPTION selected>1206</option>
  <OPTION>0805</option>
  <OPTION>0603</option>
  <OPTION>1210</option>
  <OPTION>1808</option>
  <OPTION>1812</option>
  <OPTION>1825</option>
  <OPTION>2220</option>
  <OPTION>2225</option>
  <OPTION>3640</option>
  <OPTION>0000</option>
</SELECT> Thickness: <INPUT size=5 value=1.0 name=chip_thick>
[mm]</TD></TR>
<TR><TD align=right bgcolor=#bdd6ef>Solder Fillet Shape:</TD>
<TD><SELECT name=solder_type>
  <OPTION selected>nominal</option>
  <OPTION>starved</option>
  <OPTION>bulbous</OPTION>
</SELECT></TD></TR>
<TR><TD align=right bgcolor=#bdd6ef>Solder Material:</TD>
<TD><SELECT name=solder_mat>
  <OPTION selected>PbSn</option>
  <OPTION>SnAgCu</option>
</SELECT></TD></TR>

```

```

<TR><TD align=right bgcolor=#bdd6ef>Solder Pad Width:</TD>
<TD><INPUT size=5 value=100 name=pad_width>[% of chip width
(85-125)]</TD></TR>
<TR>
<TD align=right bgcolor=#bdd6ef>Solder Pad Length:</TD>
<TD><INPUT size=5 value=1.0 name=pad_length>[mm] </TD></TR>
<TR>
<TD align=right bgcolor=#bdd6ef>Solder Thickness:</TD>
<TD><INPUT size=5 value=0.0635 name=solder_thick> [mm], Typically between
0.0254 and 0.127</TD></TR>
<TR><TD align=right bgcolor=#bdd6ef>PWB Thickness:</TD>
<TD><INPUT size=5 value=1.6 name=pwb_thick> [mm]</TD></TR>
<TR><TD align=right bgcolor=#bdd6ef>PWB Modulus:</TD>
<TD><INPUT size=5 value=17000 name=pwb_mod> [MPa]</TD></TR>
<TR><TD align=right bgcolor=#bdd6ef>Applied PWB :</TD>
<TD><INPUT size=5 value=0.002 name=pwb_load> <SELECT name=load_type>
  <OPTION selected>strain [%]</option>
  <OPTION>curvature [1/mm]</option>
  <OPTION>deflection [mm]</OPTION>
</SELECT></TD></TR>
<TR><TD align=right bgcolor=#efefef><B>Compute Results:</B></TD>
<TD><INPUT Onclick=computeForm(this.form) type=button
value=Compute></TD></TR>
<TR><TD align=right bgcolor=lightgreen><b>Capacitor Stress:</b></TD>
<TD><INPUT size=8 name=cap_stress style='font-weight:bold; background:
lightyellow'>[MPa] </TD></TR>
<TR>
<TD align=right bgcolor=lightgreen><b>Probability of Capacitor Failure:</b></TD>
<TD><INPUT size=8 name=cap_fail style='font-weight:bold;
background: lightyellow'>% </TD></TR>
<TR><TD></TD></TR>
<TD></TD></TR><TR></TR></TBODY></TABLE></FORM></center>
<HR noShade><center>
<span style='font-size:8pt'>
Copyright &copy; 2004 by
<a href="http://www.calce.umd.edu/">Nathan Blattau</a> , All Rights Reserved
</span></center><center>
<applet name=CapCrackCalc code=CapCrackCalc.class width=0 height=0>
  <table border=1 cellpadding=5 cellspacing=0 width=400>
  <tr bgcolor=yellow><td><b>
Java is not currently installed and/or enabled on this browser, which
means that you can't use the best capacitor cracking calculator
ever made. Sorry.
  </b></td></tr></table></applet></center></td></tr></table></center>
</body></html>

```



### 10.3.2 Java based analytical model

```

import java.applet.*;
import java.io.*;
import java.awt.*;
import java.text.*;
import java.util.*;

public class CapCrackCalc extends Applet
{
//
//   Formatting the data passed from the applet to the webpage
//
    private DecimalFormat failureFmt = new DecimalFormat("000.00000");
    private DecimalFormat stressFmt = new DecimalFormat("000.00000");

//
//   Applet output variables
//
    private double cap_fail;
    private double cap_stress;
    private double pwb_moment;
    private double cap_force;

//
//   Throw an error
//
    private void error (String msg) throws Exception
    {
        throw new Exception (msg);
    }

//
//   Compute results
//
    public void computeResults (String mlccmaker, String dielect,
                                String mlccsize, String solderjoint,
                                String soldermat, String loadtype,
                                String capthickStr, String solderpadStr,
                                String solderlengthStr, String solderthickStr,
                                String pwbthicknessStr, String pwbmodStr,
                                String pwbloadStr) throws Exception

//
//   Check data passed from webpage to applet
//
    {
        if (capthickStr.length() == 0)

```

```

        error ("The Capacitor Thickness Field Is Empty");

    if (solderpadStr.length() == 0)
        error ("The Solder Pad Width Field Is Empty");

    if (solderlengthStr.length() == 0)
        error ("The Solder Pad length Field Is Empty");

    if (solderthickStr.length() == 0)
        error ("The Solder thickness Field Is Empty");

    if (pwbthicknessStr.length() == 0)
        error ("The PWB Thickness Field Is Empty");

    if (pwbmodStr.length() == 0)
        error ("The PWB Modulus Field Is Empty");

    if (pwbloadStr.length() == 0)
        error ("The PWB Load Field Is Empty");
//
// Convert passed strings to doubles and check for errors
//
// Capacitor Thickness
//
    double capthick = 0;
    try {
        capthick = Double.valueOf(capthickStr).doubleValue();
    } catch (Exception ex) {
        error ("Invalid Capacitor Thickness Value");
    }
//
// Solder Pad Width
//
    double solderpad = 0;
    try {
        solderpad = Double.valueOf(solderpadStr).doubleValue();
    } catch (Exception ex) {
        error ("Invalid Solder Pad Width Value");
    }

    if (solderpad < 85 || solderpad > 125)
        error ("Solder Pad Width Must Be Between 85 and 125");
//
// Solder Pad Length
//

```

```

    double solderlength = 0;
    try {
        solderlength = Double.valueOf(solderlengthStr).doubleValue();
    } catch (Exception ex) {
        error ("Invalid Solder Pad Length Value");
    }
//
// Solder Thickness
//
    double solderthick = 0;
    try {
        solderthick = Double.valueOf(solderthickStr).doubleValue();
    } catch (Exception ex) {
        error ("Invalid Solder Thickness Value");
    }

    if (solderthick < 0.010 || solderthick > 0.254)
        error ("Solder Thickness Must Be Between .010 and 0.254 mm");
//
// PWB Thickness
//
    double pwbthick = 0;
    try {
        pwbthick = Double.valueOf(pwbthicknessStr).doubleValue();
    } catch (Exception ex) {
        error ("Invalid PWB Thickness Value");
    }
    if (pwbthick < 0.7 || pwbthick > 3.4)
        error ("PWB Thickness Must Be Between 0.7 and 3.4 mm");
//
// PWB Modulus
//
    double pwbmod = 0;
    try {
        pwbmod = Double.valueOf(pwbmodStr).doubleValue();
    } catch (Exception ex) {
        error ("Invalid PWB Modulus Value");
    }

    if (pwbmod < 14000 || pwbmod > 22000)
        error ("PWB Modulus Must Be Between 14000 and 22000 MPa");
//
// Get PWB Load Value
//
    double pwb_load = 0;

```

```
try {
    pwb_load = Double.valueOf(pwbloadStr).doubleValue();
} catch (Exception ex) {
    error ("Invalid PWB Load Value");
}
//
// Set the size of the capacitor
//
double cap_length = 0;
double cap_width = 0;
double cap_term = 0;
double cap_thick = 0;
double str_x = 0;
double solder_mod = 0;

if (mlccsize.equals("0201")){
    cap_length=0.508;
    cap_width=0.254;
    cap_thick=0.254;
    cap_term=0.15;

} else if (mlccsize.equals("0402")){
    cap_length=1.016;
    cap_width=0.508;
    cap_thick=0.25;
    cap_term=0.15;

} else if (mlccsize.equals("0603")){
    cap_length=1.524;
    cap_width=0.762;
    cap_thick=0.762;
    cap_term=0.35;

} else if (mlccsize.equals("0805")){
    cap_length=2.032;
    cap_width=1.27;
    cap_thick=capthick;
    cap_term=0.5;

} else if (mlccsize.equals("1206")){
    cap_length=3.048;
    cap_width=1.524;
    cap_thick=capthick;
    cap_term=0.5;
```

```
} else if (mlccsize.equals("1210")){
    cap_length=3.048;
    cap_width=2.54;
    cap_thick=capthick;
    cap_term=0.5;

} else if (mlccsize.equals("1808")){
    cap_length=4.572;
    cap_width=2.032;
    cap_thick=capthick;
    cap_term=0.6;

} else if (mlccsize.equals("1812")){
    cap_length=4.572;
    cap_width=3.048;
    cap_thick=capthick;
    cap_term=0.6;

} else if (mlccsize.equals("1825")){
    cap_length=4.572;
    cap_width=6.35;
    cap_thick=capthick;
    cap_term=0.6;

} else if (mlccsize.equals("2220")){
    cap_length=5.588;
    cap_width=5.08;
    cap_thick=capthick;
    cap_term=0.85;

} else if (mlccsize.equals("2225")){
    cap_length=5.588;
    cap_width=6.35;
    cap_thick=capthick;
    cap_term=0.85;
} else if (mlccsize.equals("2512")){
    cap_length=6.35;
    cap_width=3.048;
    cap_thick=capthick;
    cap_term=0.85;

} else if (mlccsize.equals("3640")){
    cap_length=9.144;
    cap_width=10.16;
    cap_thick=capthick;
```

```

    cap_term=1.125;

} else {
    error ("Unsupported MLCC Size Value "+mlccsize+""");
}
//
//
//
double pwb_I = cap_width * Math.pow(pwbthick,3)/12;

if (loadtype.equals("strain")){
    pwb_moment = pwb_load * pwbmod * pwb_I / (pwbthick/2);
} else if (loadtype.equals("curvature")){
    pwb_moment = pwb_load * pwbmod * pwb_I;
} else if (loadtype.equals("deflection")){
    pwb_moment = pwb_load*12*pwb_I*pwbmod/Math.pow(90,2);
}

if (solderjoint.equals("nominal"))    { str_x = 0.7; }
else if (solderjoint.equals("starved")) { str_x = 0.5; }
else if (solderjoint.equals("bulbous"))    { str_x = 1.0; }
else { error ("Unsupported Solder Joint Type "+solderjoint+"""); }

double cap_I = cap_width * Math.pow(cap_thick,3)/12;
cap_length=cap_length/2;
if (soldermat.equals("PbSn")) { solder_mod = 27000; }
else if (soldermat.equals("SnAgCu"))    { solder_mod = 40000; }
else { error ("Unsupported Solder Material "+soldermat+"""); }

double solder_lgth = str_x * solderlength;
double solder_width = cap_width * solderpad/100;
double solder_A = solder_lgth * solder_width;
double cap_mod =0;
//
if (dielect.equals("Y5V"))    { cap_mod = 105000; }
else if (dielect.equals("X7R"))    { cap_mod = 110000; }
else if (dielect.equals("C0G"))    { cap_mod = 120000; }
else if (dielect.equals("AlO3"))    { cap_mod = 337000; }
else { error ("Unsupported Dielectric Material "+dielect+"""); }

double pwb_shear =
9*((pwbmod/2.6)*(solder_width+solderlength)/4)/1.82*1.4*Math.pow(pwbthick,
0.5);

```

```

double solder_stiff=1/(1/pwb_shear+1/(solder_A * (solder_mod / 2.6) /
solderthick));
double margin_stiff= cap_term * cap_width * (70000 / 2.6) / 0.010;
double pad_stiff= solder_A * (120000 / 2.6) / 0.035;
double cap_stiff= cap_thick * cap_width * cap_mod / cap_length;

double combine_stiff = 1/(1/solder_stiff+1/pad_stiff+1/cap_stiff);
double rot_stiff = combine_stiff * Math.pow(pwbthick/2,2);

double pwb_rot = pwbmod * pwb_I / (cap_length - cap_term/2);
double theta = pwb_moment/ (pwb_rot + rot_stiff);
cap_force = (pwbthick/2)* combine_stiff * theta;
cap_stress = cap_force/ (cap_width*cap_thick)*(3.18*cap_thick +
1.2)*Math.pow(1.575/pwbthick,1.2);
double w_mod = 0;
double chr_str = 0;
double width = 0;

if (mlccmaker.equals("Generic 1 mm")){
    w_mod=5.16;
    chr_str=100.6;
    width=1.27;}
else if (mlccmaker.equals("Generic 2 mm")){
    w_mod=4.87;
    chr_str=131.8;
    width=1.524;}
else if (mlccmaker.equals("Syfer")){
    w_mod=4.87;
    chr_str=131.8;
    width=1.524;}
else if (mlccmaker.equals("TDK")){
    w_mod=5.5;
    chr_str=134.2;
    width=1.27;}
else if (mlccmaker.equals("muRata")){
    w_mod=4.6;
    chr_str=100.6;
    width=5.16;}
else
    error ("Unsupported MLCC Manufacturer '"+mlccmaker+"'");

cap_fail=(1-Math.exp(-
1*cap_width/width*Math.pow((cap_stress/chr_str),w_mod)))*100;

}

```

```
public String getCapFailure ()
{
    if (Double.isNaN(cap_fail))
        return "NaN";
    return failureFmt.format(cap_fail);
}
public String getForce ()
{
    if (Double.isNaN(cap_force))
        return "NaN";
    return failureFmt.format(cap_force);
}

public String getStress ()
{
    if (Double.isNaN(cap_stress))
        return "NaN";
    return stressFmt.format(cap_stress);
}
public String getMoment ()
{
    if (Double.isNaN(pwb_moment))
        return "NaN";
    return stressFmt.format(pwb_moment);
}
}
```



## 10.4 Printed wiring board computations

### 10.4.1 Element 2, computations

Effective flexural modulus ( $E_f$ ) is computed as three rotational springs in parallel using the flexural stiffness ( $EI/L$ ) that is then normalized to just the solder dimensions. The length of the solder joint is assumed to be the length of the device end metallization plus an additional length based upon the fillet shape. This additional length is computed by equation using the variables defined in Figure 2-3 and the solder joint type.

$$L_{eff} = l_{pad} - (t_{sj}) \frac{(t_{sj} + j_c t_c)}{(l_{pad} - l_c)} - l_c$$

Where:

$L_{eff}$  is the new effective length of the solder

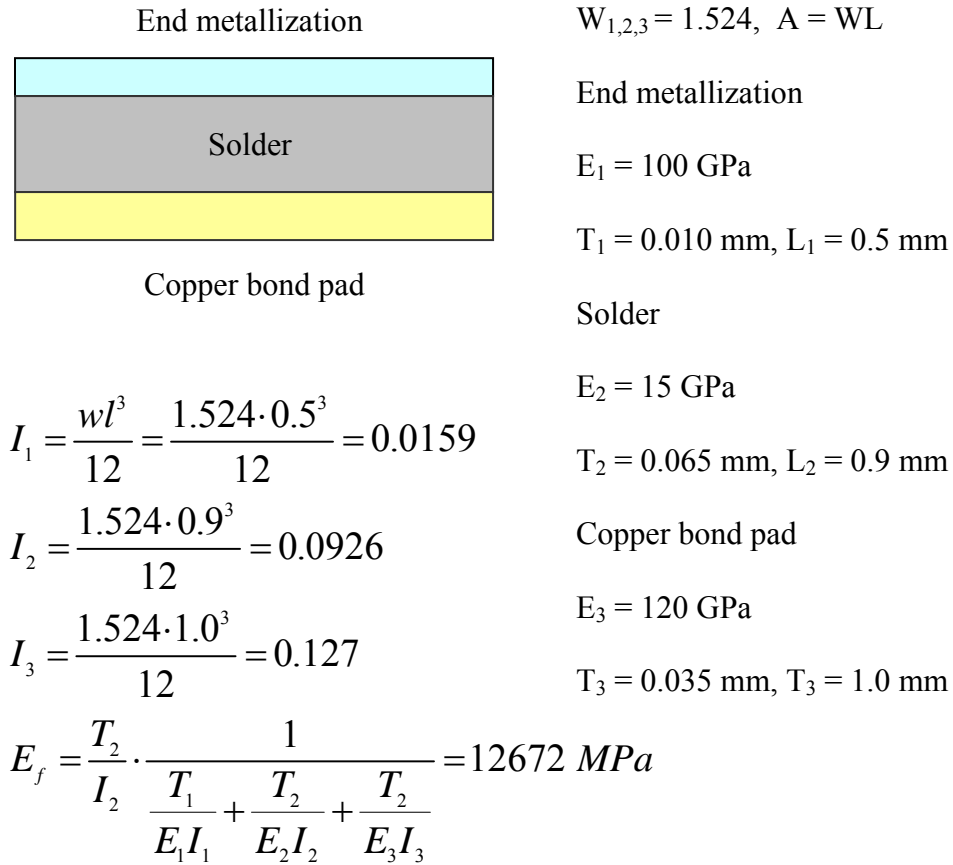
$j_c$  is the joint factor:

0.5 for starved joints

0.7 for nominal joints

1.0 for bulbous joints

For the example, this new computed solder length is 0.9 mm and the calculations for the flexural modulus are shown in Figure 10-8.



**Figure 10-8: Effective flexural modulus calculations**

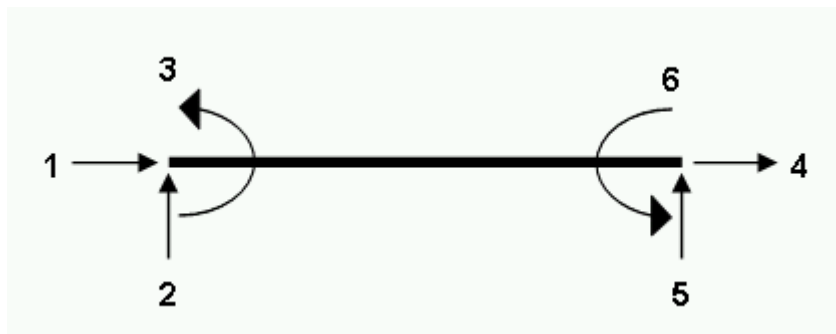
The tensile modulus is based upon the area and the thickness of each section. These are added up as springs in parallel and then normalized to the solder dimensions to calculate the effective tensile modulus of the element.

$$E_t = \frac{L_2}{A_2} \cdot \frac{1}{\frac{L_1}{E_1 A_1} + \frac{L_2}{E_2 A_2} + \frac{L_2}{E_3 A_3}} = 13610 \text{ MPa}$$

**Equation 10-1: Effective tensile modulus calculations**

### 10.5 Stiffness Method

Portions of the structure will be assumed to behave as beams even though the length to width ratio (aspect ratio) may not be suitable for a beam type approximation. Each beam element has six degrees of freedom as shown in Figure 10-9. Each number corresponds to either a force or displacement.



**Figure 10-9: Degrees of freedom for a beam element**

The stiffness of the beam to an applied unit displacement is shown in matrix form in Figure 10-10. The formation of this local stiffness matrix can be found in numerous references [74].

$$k' = \begin{bmatrix} \frac{AE}{L} & 0 & 0 & -\frac{AE}{L} & 0 & 0 \\ 0 & \frac{12EI}{L^3(1+4r)} & \frac{6EI}{L^2(1+4r)} & 0 & \frac{12EI}{L^3(1+4r)} & \frac{6EI}{L^2(1+4r)} \\ 0 & \frac{6EI}{L^2(1+4r)} & \frac{4EI}{L} \left( \frac{1+r}{1+4r} \right) & 0 & \frac{12EI}{L^3(1+4r)} & \frac{2EI}{L} \left( \frac{1-2r}{1+4r} \right) \\ -\frac{AE}{L} & 0 & 0 & \frac{AE}{L} & 0 & 0 \\ 0 & -\frac{12EI}{L^3(1+4r)} & -\frac{6EI}{L^2(1+4r)} & 0 & \frac{12EI}{L^3(1+4r)} & -\frac{6EI}{L^2(1+4r)} \\ 0 & \frac{6EI}{L^2(1+4r)} & \frac{2EI}{L} \left( \frac{1-2r}{1+4r} \right) & 0 & -\frac{6EI}{L^2(1+4r)} & \frac{4EI}{L} \left( \frac{1+r}{1+4r} \right) \end{bmatrix}$$

$$A_s = \frac{A}{K} : \text{Shear area}$$

$A$  = Cross sectional area

$K = 1.2$  : Rectangular cross section

$E$  = Modulus of Elasticity

$I$  = Moment of Inertia

$\nu$  = Poisson's ratio

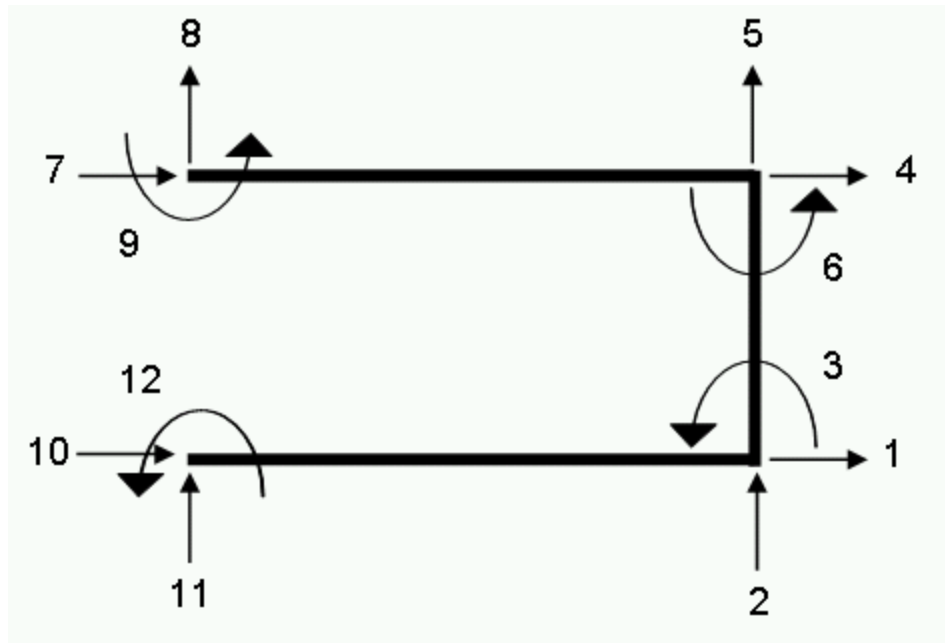
$L$  = Length of the beam

$$r = \frac{3EI}{GA_s L^2}$$

$$G = \frac{E}{2(1+\nu)}$$

**Figure 10-10: Beam stiffness matrix with shear compliance [74]**

The overall structure has three elements and four nodes and, as shown in Figure 10-11, has 12 degrees of freedom. The degrees of freedom are numbered starting with the unconstrained degrees of freedom first and continuing counter clockwise to the constrained degrees of freedom. The load and displacement matrices correspond to the boundary and loading conditions shown in Figure 2-4. These form the global displacement and the global load matrices as shown in Figure 10-12.



**Figure 10-11: Degree of freedom numbering**

Global Displacement Matrix

Global Load Matrix

$$\begin{bmatrix} D_1 \\ D_2 \\ D_3 \\ D_4 \\ D_5 \\ D_6 \\ 0 \\ D_8 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

$$\begin{bmatrix} 0 \\ 0 \\ M \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$$

**Figure 10-12: Global load and displacement matrices**

The local force matrix for each element is transformed from the local coordinates of the beam to the global coordinates of the structure. This is to align the local coordinates to those of the global structure and is done by multiplying the local matrix by a transformation matrix. The transformation matrix relates the local member to the global structure and can be expressed in geometric terms and in matrix form as shown in Figure 10-13, where  $\theta_x$  is the angle from the global structure x axis to the element and  $\theta_y$  is the angle from the global structure y axis to the element.

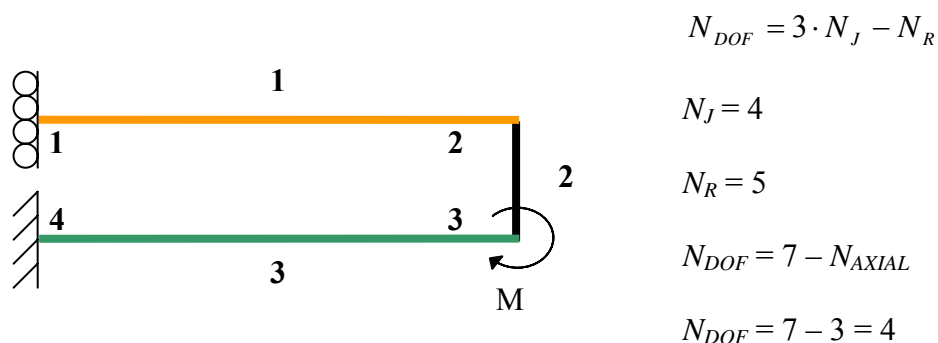
$$T = \begin{bmatrix} \cos\theta_x & \cos\theta_y & 0 & 0 & 0 & 0 \\ -\cos\theta_y & \cos\theta_x & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & \cos\theta_x & \cos\theta_y & 0 \\ 0 & 0 & 0 & -\cos\theta_y & \cos\theta_x & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \end{bmatrix}$$

**Figure 10-13: Displacement transformation matrix**

This transformation matrix also relates the global stiffness matrix to the local stiffness matrix through the following relationship  $[k] = [T]^T [k'] [T]$  where  $k'$  is the local member stiffness matrix,  $k$  is the global stiffness member matrix and  $T$  is the transformation matrix. The global stiffness matrix can then be assembled. The boundary conditions are then be applied to the global stiffness matrix to reduce the matrix.

The structure is assumed to be symmetric, and is discretized into three elements as shown in Table 38. Element 1 is the body of the device, element 2 is a combination of the solder, bond-pad, and end-metallization, and element 3 is the printed wiring board. The material properties used are shown in Table 5. There are four degrees of freedom for the symmetric structure of a LCC/LCR mounted to a printed wiring board.

**Table 38: Degrees of freedom, and node/element numbering**



The structure has the nodes labeled as shown in Table 38 and the load (M) at joint 3 is representative of the moment applied to structure due to printed wiring board bending. Using the degrees of freedom numbering shown in Table 38, the global stiffness matrix for element 1 is shown in Figure 10-14.

$$k_1 = \begin{bmatrix} \frac{A_1 E_1}{L_1} & 0 & 0 & -\frac{A_1 E_1}{L_1} & 0 & 0 \\ 0 & \frac{12E_1 I_1}{L_1^3(1+4r_1)} & \frac{6E_1 I_1}{L_1^2(1+4r_1)} & 0 & \frac{-12E_1 I_1}{L_1^3(1+4r_1)} & \frac{6E_1 I_1}{L_1^2(1+4r_1)} \\ 0 & \frac{6E_1 I_1}{L_1^2(1+4r_1)} & \frac{4E_1 I_1}{L_1} \left( \frac{1+r_1}{1+4r_1} \right) & 0 & \frac{-6E_1 I_1}{L_1^2(1+4r_1)} & \frac{2E_1 I_1}{L_1} \left( \frac{1-2r_1}{1+4r_1} \right) \\ -\frac{A_1 E_1}{L_1} & 0 & 0 & \frac{A_1 E_1}{L_1} & 0 & 0 \\ 0 & \frac{-12EI}{L_1^3(1+4r_1)} & \frac{-6E_1 I_1}{L_1^2(1+4r_1)} & 0 & \frac{12E_1 I_1}{L_1^3(1+4r_1)} & \frac{-6E_1 I_1}{L_1^2(1+4r_1)} \\ 0 & \frac{6E_1 I_1}{L_1^2(1+4r_1)} & \frac{2E_1 I_1}{L_1} \left( \frac{1-2r_1}{1+4r_1} \right) & 0 & \frac{-6E_1 I_1}{L_1^2(1+4r_1)} & \frac{4E_1 I_1}{L_1} \left( \frac{1+r_1}{1+4r_1} \right) \end{bmatrix}$$

**Figure 10-14: Global stiffness matrix for element 1**

The local stiffness matrix for element 2 must be rotated -90 degrees to align with the global coordinates. The resulting global stiffness matrix for element 2 is shown in Figure 10-15. The elastic modulus for element 2 is a combination of the materials that comprise the solder, bond pad, and end-metallization. The flexural modulus and tensile modulus for element 2 are computed as a set of three springs in series. The detailed computations are provided in Appendix 10.4.1. The local stiffness matrix for element 3 is transformed to align with the global coordinates. The resulting global stiffness matrix for element 3 is shown in Figure 10-16.



$$k_2 = \begin{bmatrix} \frac{12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{-6E_2I_2}{L_2^2(1+4r_2)} & \frac{-12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{-6E_2I_2}{L_2^2(1+4r_2)} \\ 0 & \frac{A_2E_2}{L_2} & 0 & 0 & \frac{-A_2E_2}{L_2} & 0 \\ \frac{-6E_2I_2}{L_2^2(1+4r_2)} & 0 & \frac{4E_2I_2}{L_2} \left( \frac{1+r_2}{1+4r_2} \right) & \frac{6E_2I_2}{L_2^2(1+4r_2)} & 0 & \frac{2E_2I_2}{L_2} \left( \frac{1-2r_2}{1+4r_2} \right) \\ \frac{-12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{6E_2I_2}{L_2^2(1+4r_2)} & \frac{12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{6E_2I_2}{L_2^2(1+4r_2)} \\ 0 & \frac{-A_2E_2}{L_2} & 0 & 0 & \frac{A_2E_2}{L_2} & 0 \\ \frac{-6E_2I_2}{L_2^2(1+4r_2)} & 0 & \frac{2E_2I_2}{L_2} \left( \frac{1-2r_2}{1+4r_2} \right) & \frac{6E_2I_2}{L_2^2(1+4r_2)} & 0 & \frac{4E_2I_2}{L_2} \left( \frac{1+r_2}{1+4r_2} \right) \end{bmatrix}$$

**Figure 10-15: Global stiffness matrix for element 2**

$$k_3 = \begin{bmatrix} \frac{A_3E_3}{L_3} & 0 & 0 & \frac{-A_3E_3}{L_3} & 0 & 0 \\ 0 & \frac{12E_3I_3}{L_3^3(1+4r_3)} & \frac{-6E_3I_3}{L_3^2(1+4r_3)} & 0 & \frac{-12E_3I_3}{L_3^3(1+4r_3)} & \frac{-6E_3I_3}{L_3^2(1+4r_3)} \\ 0 & \frac{-6E_3I_3}{L_3^2(1+4r_3)} & \frac{4E_3I_3}{L_3} \left( \frac{1+r_3}{1+4r_3} \right) & 0 & \frac{6E_3I_3}{L_3^2(1+4r_3)} & \frac{2E_3I_3}{L_3} \left( \frac{1-2r_3}{1+4r_3} \right) \\ \frac{-A_3E_3}{L_3} & 0 & 0 & \frac{A_3E_3}{L_3} & 0 & 0 \\ 0 & \frac{-12E_3I_3}{L_3^3(1+4r_3)} & \frac{6E_3I_3}{L_3^2(1+4r_3)} & 0 & \frac{12E_3I_3}{L_3^3(1+4r_3)} & \frac{6E_3I_3}{L_3^2(1+4r_3)} \\ 0 & \frac{-6E_3I_3}{L_3^2(1+4r_3)} & \frac{2E_3I_3}{L_3} \left( \frac{1-2r_3}{1+4r_3} \right) & 0 & \frac{6E_3I_3}{L_3^2(1+4r_3)} & \frac{4E_3I_3}{L_3} \left( \frac{1+r_3}{1+4r_3} \right) \end{bmatrix}$$

**Figure 10-16: Global stiffness matrix for element 3**

These global element matrices can now be assembled into the assembly global stiffness matrix. The global matrix, which is a 12 x 12 matrix, can be reduced to a 7 x 7 matrix by applying the boundary conditions. The reduced matrix is shown in Figure 10-17.

$$K = \begin{bmatrix} \frac{AE_1}{L_1} + \frac{12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{-6E_2I_2}{L_2^2(1+4r_2)} & \frac{-12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{-6E_2I_2}{L_2^2(1+4r_2)} & 0 \\ 0 & \frac{12E_1I_1}{L_1^3(1+4r_1)} + \frac{A_2E_2}{L_2} & \frac{-6E_1I_1}{L_1^2(1+4r_1)} & 0 & \frac{-A_2E_2}{L_2} & 0 & 0 \\ \frac{-6E_2I_2}{L_2^2(1+4r_2)} & \frac{-6E_1I_1}{L_1^2(1+4r_1)} & \frac{4E_1I_1}{L_1} \left( \frac{1+r_1}{1+4r_1} \right) + \frac{4E_2I_2}{L_2} \left( \frac{1+r_2}{1+4r_2} \right) & \frac{6E_2I_2}{L_2^2(1+4r_2)} & 0 & \frac{2E_2I_2}{L_2} \left( \frac{1-2r_2}{1+4r_2} \right) & 0 \\ \frac{-12E_2I_2}{L_2^3(1+4r_2)} & 0 & \frac{6E_2I_2}{L_2^2(1+4r_2)} & \frac{12E_2I_2}{L_2^3(1+4r_2)} + \frac{A_3E_3}{L_3} & 0 & \frac{6E_2I_2}{L_2^2(1+4r_2)} & 0 \\ 0 & \frac{-A_2E_2}{L_2} & 0 & 0 & \frac{A_2E_2}{L_2} + \frac{12E_3I_3}{L_3^3(1+4r_3)} & \frac{-6E_3I_3}{L_3^2(1+4r_3)} & \frac{-12E_3I_3}{L_3^3(1+4r_3)} \\ \frac{-6E_2I_2}{L_2^2(1+4r_2)} & 0 & \frac{2E_2I_2}{L_2} \left( \frac{1-2r_2}{1+4r_2} \right) & \frac{6E_2I_2}{L_2^2(1+4r_2)} & \frac{-6E_3I_3}{L_3^2(1+4r_3)} & \frac{4E_2I_2}{L_2} \left( \frac{1+r_2}{1+4r_2} \right) + \frac{4E_3I_3}{L_3} \left( \frac{1+r_3}{1+4r_3} \right) & \frac{6E_3I_3}{L_3^2(1+4r_3)} \\ 0 & 0 & 0 & 0 & \frac{-12E_3I_3}{L_3^3(1+4r_3)} & \frac{6E_3I_3}{L_3^2(1+4r_3)} & \frac{12E_3I_3}{L_3^3(1+4r_3)} \end{bmatrix}$$

Figure 10-17: Reduced global stiffness matrix

The displacements of the structure can now be determined by solving  $Q = K \cdot D$ . The reaction forces can then be determined multiplying the partitioned global stiffness matrix by the displacements.

Global Displacement	Global Load
Matrix [D]	Matrix [Q]
$\begin{bmatrix} D_1 \\ 0 \\ 0 \\ D_4 \\ D_5 \\ D_6 \\ D_7 \\ D_8 \\ D_9 \\ 0 \\ 0 \\ 0 \end{bmatrix}$	$\begin{bmatrix} 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ M \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \\ 0 \end{bmatrix}$

**Figure 10-18: Global load and displacement matrices**

The values of interest are the loads applied to the solder and the component. The matrix computations were conducted with Microsoft Excel. The loads are calculated by transforming the global displacements back to the local displacements for the component element. The local stiffness matrix is then multiplied by the local displacements with the result being the loads applied to the component. These loads are converted to the stresses in a rectangular body as shown in Figure 10-19, with the equations given in Table 39.

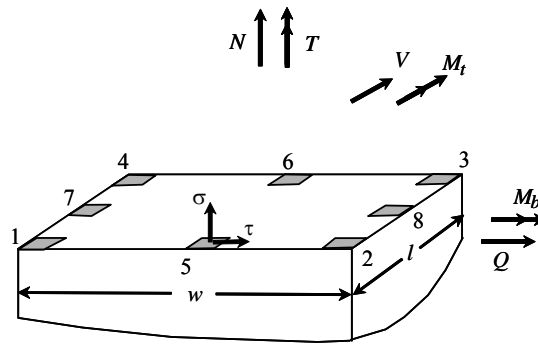


Figure 10-19: Critical stresses on a rectangular cross section [74]

Table 39: Equations for the critical stresses on a rectangular cross section [74]

Point	Normal stress $\sigma$	Shear stress $\tau$
1	$\frac{N}{wl} - \frac{6M_b}{wl^2} + \frac{6M_t}{w^2l}$	0
2	$\frac{N}{wl} - \frac{6M_b}{wl^2} - \frac{6M_t}{w^2l}$	0
3	$\frac{N}{wl} + \frac{6M_b}{wl^2} - \frac{6M_t}{w^2l}$	0
4	$\frac{N}{wl} + \frac{6M_b}{wl^2} + \frac{6M_t}{w^2l}$	0
5	$\frac{N}{wl} - \frac{6M_b}{wl^2}$	$\frac{3Q}{2wl} + \frac{kT}{wl^2}$
6	$\frac{N}{wl} + \frac{6M_b}{wl^2}$	$\frac{3Q}{2wl} - \frac{kT}{wl^2}$
7	$\frac{N}{wl} + \frac{6M_t}{w^2l}$	$\frac{3V}{2wl} - \frac{skT}{wl^2}$
8	$\frac{N}{wl} - \frac{6M_t}{w^2l}$	$\frac{3V}{2wl} + \frac{skT}{wl^2}$

The maximum stresses will be generated at point 5 with the given loads  $N$  and  $M_b$ . This tensile stress is used to conduct a rapid assessment of the probability of capacitor failure for a given printed wiring surface strain, curvature or applied moment.

## 10.6 Probability of failure comparison between PbSn and SnAgCu

**Capacitor Cracking Calculator**  
Probability of MLCC Cracking  
Due To Printed Wiring Board Bending  
Version 2.0

This program calculates the probability of cracking an MLCC during PWB bending. Initially the form contains typical values for each entry, clicking on the Compute button at the bottom of the form will display the corresponding results. This allows the user to become familiar with the routine and see some typical results. The capacitor is assumed to be placed on the PWB at the point of greatest deflection.

**Reset The Form:**

MLCC Manufacturer: TDK

Dielectric Type: X7R

MLCC Size: 1206 Thickness: 1.0 [mm]

Solder Fillet Shape: nominal

Solder Material: PbSn

Solder Pad Width: 100 [% of chip width (85-125)]

Solder Pad Length: 1.0 [mm]

Solder Thickness: 0.035 [mm], Typically between 0.0254 and 0.127

PWB Thickness: 1.6 [mm]

PWB Modulus: 17000 [MPa]

Applied PWB: 0.002 strain [mm/mm, 1/mm, mm]

**Compute Results:**

**Capacitor Stress:** 066.41748 [MPa]

**Board Moment:** 022.10816 [N.mm]

**Probability of Capacitor Failure:** 002.47550 %

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**Capacitor Cracking Calculator**  
Probability of MLCC Cracking  
Due To Printed Wiring Board Bending  
Version 2.0

This program calculates the probability of cracking an MLCC during PWB bending. Initially the form contains typical values for each entry, clicking on the Compute button at the bottom of the form will display the corresponding results. This allows the user to become familiar with the routine and see some typical results. The capacitor is assumed to be placed on the PWB at the point of greatest deflection.

**Reset The Form:**

MLCC Manufacturer: TDK

Dielectric Type: X7R

MLCC Size: 1206 Thickness: 1.0 [mm]

Solder Fillet Shape: nominal

Solder Material: SnAgCu

Solder Pad Width: 100 [% of chip width (85-125)]

Solder Pad Length: 1.0 [mm]

Solder Thickness: 0.035 [mm], Typically between 0.0254 and 0.127

PWB Thickness: 1.6 [mm]

PWB Modulus: 17000 [MPa]

Applied PWB: 0.002 strain [mm/mm, 1/mm, mm]

**Compute Results:**

**Capacitor Stress:** 081.63912 [MPa]

**Board Moment:** 022.10816 [N.mm]

**Probability of Capacitor Failure:** 007.50171 %

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