

ABSTRACT

Title of Thesis: LOW POWER AMPLIFIERS FOR RECORDING
ACTIVITY OF ELECTRICALLY ACTIVE CELLS

Makeswaran Loganathan, Master of Science, 2003

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Biological applications that require sensing individual cells have led to developments in the synthesis of large multielectrode arrays and single cell isolating microstructures. This in turn drives the need for the integration of low power electronic circuitry at or very close to the site of activity. We describe low voltage low power CMOS amplifiers that address this need by rejecting DC offsets, and have tunable bandwidths. They operate at 1.35V, with a power consumption of $37.8\mu\text{W}$ and have an input referred noise of $23\mu\text{V}$. We also describe the design of a wireless transmission system capable of transmitting the electrical signals sensed from cells. Integration of the amplifier array with the wireless link brings continuous monitoring of neurophysiologic activity of unanesthetized and freely moving animals closer to realization. The transmitter is

capable of generating an ASK modulated signal at a power level of -36 dBm at a frequency of 820 MHz.

LOW POWER AMPLIFIERS FOR RECORDING ACTIVITY OF
ELECTRICALLY ACTIVE CELLS

by

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Dedication

To my parents and my sister

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Chapter 1

Introduction

A major challenge in the field of biology is the study of the response of individual and single cells to different stimuli. Previous studies in cell biology have been performed on cell cultures, and results from them have been used to understand the behavior of single cells. The ability to observe the responses of individual cells will provide insight into variations among cells as well as statistical distributions. This knowledge will help understand better the mechanisms behind cell secretions, cell metabolism and coding of protein information [1, 2, 9, 10]. Interfacing of single cells to analyze different types of blood cells can be found in [2, 9, 10]. We are attempting to develop integrated microstructures and microelectronics that would help study the response of single cells, and also of groups of cells.

Various attempts have been made at developing microprobes [22, 23, 25, 30] and microelectronic structures [1] that are capable of localizing and studying the response of individual cells. Abshire et. al. [1] have reported the design of microstructures called “Cell Clinics” that have a vial to contain the cells, and a plastic lid that can be closed to contain the cells. By fabricating the cell clinics on silicon substrate and having electrodes at the base, it is possible to monitor electrical properties of cells. A diagram of the cell clinic is shown in Fig. 1.1.

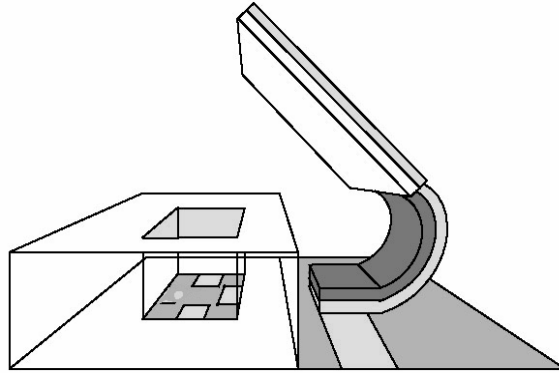


Fig. 1.1 Cell clinic capable of characterizing single cells [1]

The cells can be maneuvered towards the cell clinics by using techniques such as optical tweezing, micro fluidic manipulation, and dielectrophoresis [13, 17, 28]. We are conducting experiments to investigate optical tweezing and dielectrophoresis. Once the techniques to localize cells to these cell clinics have been perfected, we plan to conduct single cell experiments to understand responses from cells better. We also hope to modify the cell clinics to assist in experimental techniques like fluorescence probing, optical microscopy, and impedance analysis, chemical secretions of cells and recording of extra-cellular electrical activity.

In my dissertation, I aimed at recording the extra-cellular activity of electrically active cells like cardiac and nerve cells. To achieve this goal, I focused on designing VLSI amplifiers (bio-amplifiers) that could be used to record the signals from these cells at the site of activity. The cell clinics are currently being fabricated on silicon substrate and will have a gold electrode at the base to enable electrical measurements. The bio-amplifiers that I designed could later be integrated with the cell clinics to enable recording responses from cells very close to the site of electrical activity.

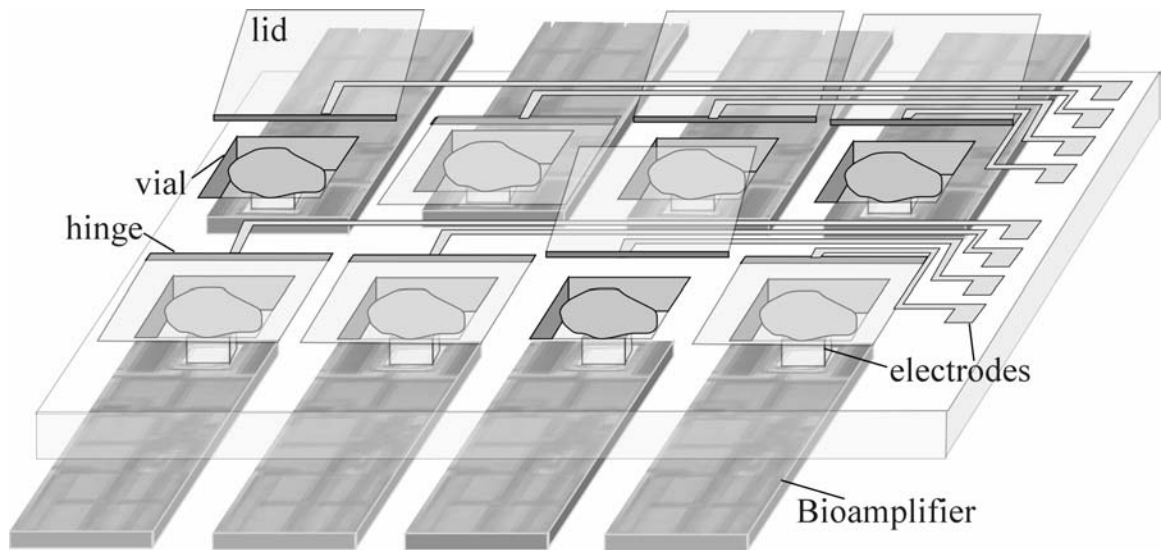


Fig. 1.2 Proposed integration of cell clinics and amplifiers for recording activity of cells

In the second part of my thesis, I aimed at designing a short range wireless transmitter to transmit the data from the bio-amplifiers. The integration of this transmitter with the bio-amplifiers would enable the realization of untethered recording units, and remote sensing recording applications. It would also bring closer the realization of continuous monitoring of cells in moving creatures in their natural habitats.

1.1. Design Specifications

The extra-cellular response of these electrically active cells has frequency content in the low kHz range (1-5 kHz) and amplitudes in the 100s of μV range. They also have huge DC offsets ($\sim 100\text{s}$ of mV) which usually contain no useful information. Amplifiers to record their activity should be designed for bandwidths

in the range of 1-5 kHz, provide high gain with a good signal to noise ratio (SNR). They should also have the capability of rejecting the DC offsets that occur across the membrane of the cell. Low power operation of these amplifiers helps prevent heating effects that may disrupt the functioning of the cells. On-chip area and input referred noise are also important considerations in the design of these amplifiers.

The wireless transmitter should be designed to operate at high frequencies in order to allow for multiplexing of data from many bio-amplifiers onto one transmitter. The data from the bio-amplifiers can either be scanned and transmitted serially or transmitted based on the presence of activity. The range of communication need not be very large, and the complexity of the transmitter should be minimal in order to allow for integration with the rest of the recording structures and electronics.

1.2. Overview

Keeping the above mentioned design specifications, we investigated and designed bio-amplifier schemes to record the extra-cellular activity of cells and a simple RF transmitter system to enable remote sensing of the bioelectric measurement setup. The rest of this document is organized as follows

Chapter 2: Review of Medical Instrumentation and Biological Recordings

presents a literature review of some of the amplifier schemes that have been implemented for recording and monitoring signals from biological applications. In this section, I discuss the different amplifier schemes, the different

microstructures and the techniques that have been used in the literature to record activity of cells.

Chapter 3: Bio-Amplifier Design discusses the design, implementation and the measurement results of a CMOS integrated bio-amplifier that could be used for recording activity from electrically active cells. It also identifies scope for improvement in the designs for low power operation.

Chapter 4: Low Voltage Techniques deals with some of the low voltage techniques applied to CMOS designs that are of particular interest to our design. In this chapter, we also discuss the design and experimental measurements of a low power filter from which the low power techniques can be used to our bio-amplifier.

Chapter 5: Low Voltage Low Power Bioamplifier discusses the implementation of low voltage low power bio-amplifiers from the basic design in chapter 3 and techniques from chapter 4. Different schemes are possible, and they are discussed in this chapter. We also present results and conclusions of our measurement in this chapter.

Chapter 6: Wireless Transmission System discusses the design of a short range wireless transmitter that implements a digital scheme of communication called Amplitude Shift Keying (ASK). The issues involved in the design and the parameters chosen are also discussed in detail.

Chapter 7: RF Test & measurement deals with the experimental procedure that was setup for measuring the output of our transmitter, and the results of our

measurement. We also placed a few test structures in our chips to help troubleshoot the system, and these are also discussed in this chapter.

Chapter 8: Conclusions and Future Work briefly summarizes this work, and presents techniques and suggestions for improving and integrating the designs developed here.

Chapter 2

Review of Medical Instrumentation and Biological

Recordings

2.1. Introduction

Understanding the metabolic activities of cells, chemical secretions from cells, the communication pattern, the overall functioning of the central nervous system and the muscular system on a single cell basis has been a major challenge and an active area of research in micro and cell biology in the past few years [7, 15, 28]. A better understanding of the protein patterns, metabolic activities and cell secretions will play an important role in the identification and cure of several diseases like cystic fibrosis, long QT syndrome [33]. The ability to identify and classify the spiking behavior of nerve cells will help in the realization of real-time direct interfaces between the brain and electronic and mechanical devices to help restore sensory and motor functions lost through injury or disease [31]. Another emerging field of research from the study of single cell behavior is bio-inspired circuits where neuronal systems are being implemented in silicon using adaptive algorithms and learning principles learned from biological cells.

Amplifiers and implantable microstructures capable of recording activity from cells have been a primary focus of research in the past few decades. In this chapter, we discuss a few amplifier schemes that have been developed for medical and instrumentation techniques, implantable micro probes with active circuitry,

hardware designs to sort the activity of neural signals, and the introduction of telemetry to bioelectric applications.

2.2. Amplifiers for Medical and Biological Purposes

One of the earliest micropower instrumentation amplifiers was designed by Degrauwe, et. al. [5]. Their design comprises a switched capacitor integrator structure that reduces the offset at the input and charge injection effects by an auto-zero technique. By using a single amplifier stage and a novel feedback method, they were able to achieve a stable configuration and a high CMRR amplifier operating from a voltage supply of 3V.

Staeyart et. al [38] describe the design of a micropower low noise amplifier for medical purposes. They designed a medical instrumentation amplifier of bandwidth 0.5 to 500 Hz and programmable bandwidths of 14/20/26/40 dB. The bandwidth is set by varying the values of resistors on chip. Their low frequency cut-off and their high frequency cut-off were selected by capacitors on chip. By sizing the transistors and choosing the bias current appropriately, they were able to obtain a low input equivalent noise voltage. They also introduced a term called the noise efficiency factor (NEF), which compares the input referred noise of any amplifier with that of a simple BJT amplifier with the same current drain and bandwidth. This gives a quantitative comparison between the performances of different amplifiers.

Implantable electrodes and multi-electrode arrays that enable on-site signal processing are key components for studying the nervous systems at the

cellular level. Najafi et. al. [30] have developed multi-channel multi-electrode recording arrays that could be used for recording of extra cellular neural biopotentials. Their active probes comprise on-chip circuitry for amplifying, multiplexing and buffering neural signals recorded from open electrodes present on the probe. The block diagram of their electrode is shown in Fig 2.1.

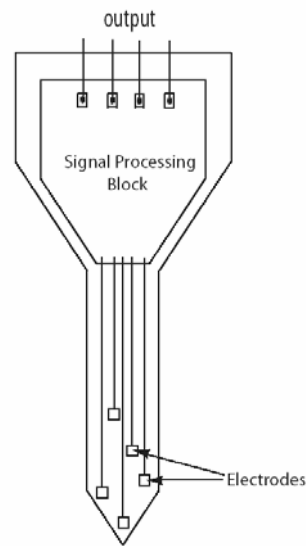


Fig. 2.1 Electrode used for probing neural cells [30]

By integrating the signal processing block at the site of activity, leakage and noise associated with the low amplitude neural signals are minimized. It also minimizes packaging issues that arise in the use of multiple probes and having a wire bonded to each of the pads. The important factors that have to be considered in designing these implantable probes is the minimization of tissue damage, and long term reliability of the probe in the cell medium.

Ji et. al. [22, 23] demonstrated the multiplexing of recordings from open pads in an implantable probe. Their probe had the same structure as shown in Fig.

2.2, and they incorporated CMOS circuitry that enabled the electronic positioning of the recording sites with respect to the active neurons. They also multiplexed the amplified output signals. This feature of selectively recording has a tradeoff with respect to the number of simultaneous recording sites, but enables possibility of recoding from those sites that are more crucial to the active neurons. They also used adaptive algorithms to move the recording sites if the probe's relative position changes in implants.

Signals from the cells have huge DC offsets, sometimes up to 100 times the magnitude of the signal. Chandran et. al. [3] introduced the addition of a very high resistor implemented using a saturated weak inversion MOSFET to the probe electrolyte interface to leak the DC offset. This resistance determines the low frequency cutoff of the measurement process. The schematic is shown in Fig. 2.2

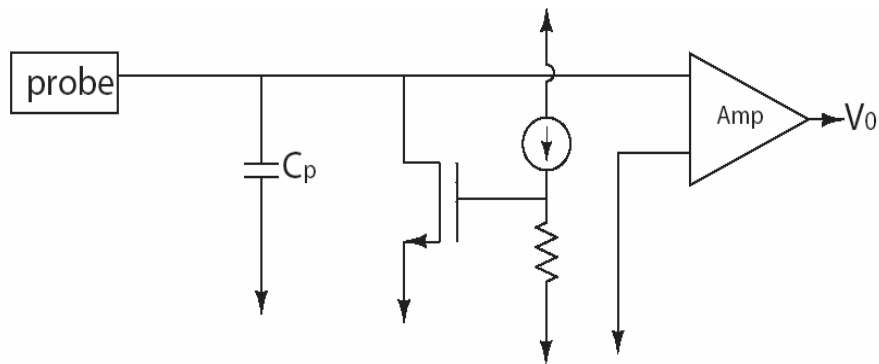


Fig. 2.2 Design to remove DC offsets at the membrane electrode interface [3]

Harrison et. al. [16] introduced the design of a low power low noise CMOS amplifier for neural recording applications. They implemented a high resistor to leak out the DC offset with a diode connected MOSFET as described in

[6]. The small size and the low power consumption enabled the integration of a large number of amplifiers on to one single chip. They also reported successful recording from neurons. Their schematic is shown in Fig. 2.3

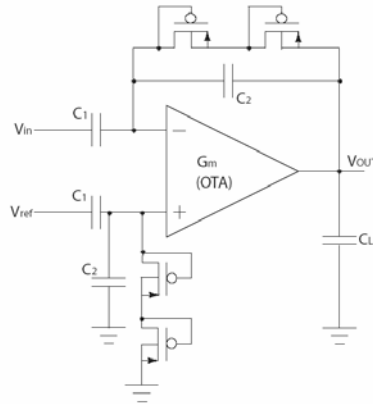


Fig. 2.3 Low power low noise amplifier for measuring extra-cellular activity [16]

Advancements in the field of neural recordings to understand the brain and the central nervous system better require the ability to simultaneously monitor densely packed neural arrays. Guillory et. al. [14] have presented and demonstrated multiplexing techniques that enable the continuous monitoring of activity from a 100-channel system. This system can be interfaced with the multi-electrode and probe arrays discussed above. Fig. 2.4 shows a block diagram of their setup.

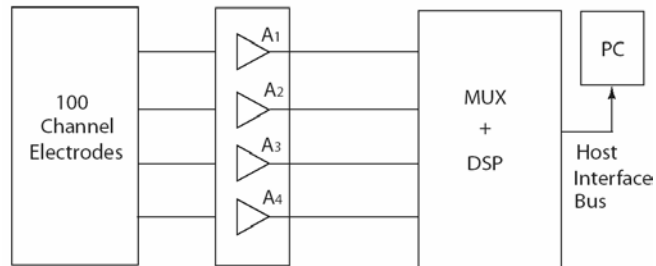


Fig. 2.4 Multiplexing signals and automation of recording process [14]

The integration of wireless telemetry to monitor and study the activity the behavior of neural cells enables long term neurophysiological studies of unanesthetized and freely moving animals. Dorman et. al. [7] developed a multiplexing system and a wireless telemetry system to record and transmit the activity of neural cells. They used low noise JFET input stages for their amplifiers and reverse biased diode connections and reverse biased configurations to remove the DC offsets. The output of the recording amplifiers are multiplexed and fed into an FM transmitter. Block diagram of their schematic is shown in Fig. 2.5

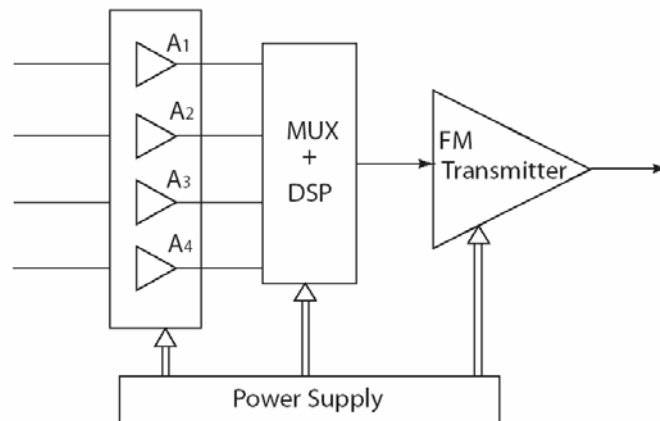


Fig. 2.5 Recording and wireless Telemetry of extra-cellular activity [7]

Irazoqui-Pastor et. al. [19, 20] have designed an implantable wireless neural recording device that frequency modulates and transmits neural signals. They use inductive power as replacement for batteries in their circuits. A wireless transmitter sends power to the inductive elements, which pick up the transmitted power and stores them in capacitors for the circuits to operate on. These circuits

amplify the neural recordings transmit the data through a wireless transmitter. Schematic of their design is shown in Fig. 2.6.

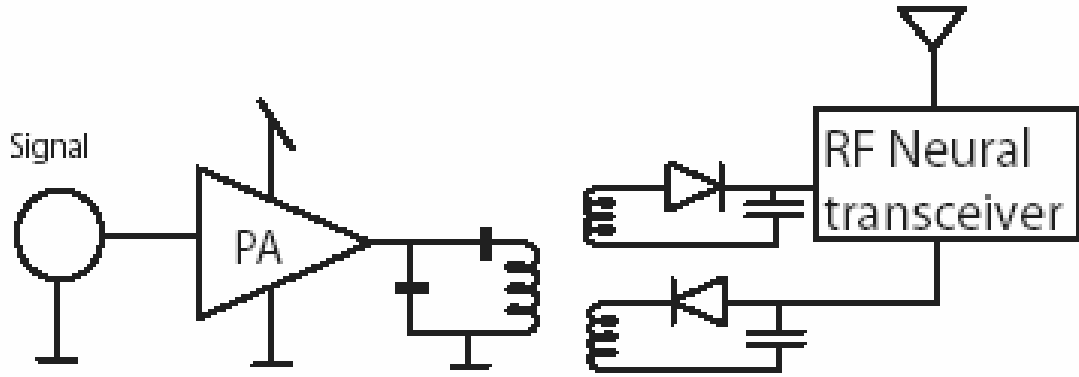


Fig. 2.6 RF Neural transceiver that uses inductive power [19]

Horiuchi et. al. [18] designed and implemented a technique that helps in pre-filtering, sorting and classifying the neural spikes before transmission. This would greatly reduce the load on the transmitter, and increase efficiency in recordings. They used an amplifier that rejects DC offsets using a MOSFET resistor and the amplifier's low frequency roll off is controlled by an external voltage. The spike sorting is done with peak and trough detector structures designed on the chip. The schematic of their design is shown in Fig. 2.7.

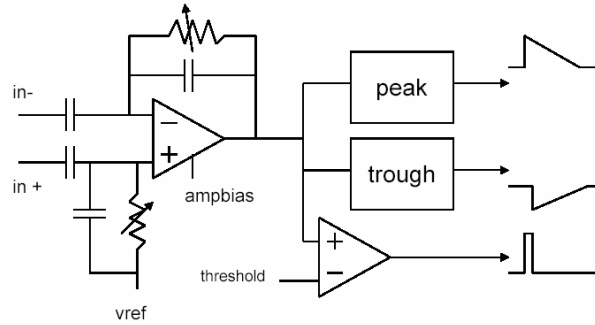


Fig. 2.7 Amplifiers to filter and sort neural spikes before transmission [18]

2.3. Microstructures and Micro-techniques

To remove leakage and noise for efficient recordings of biological activity of cells, progress towards the integration of recording pads and signal processing units are being investigated. One technique to study extra-cellular activity is the usage of patch clamps, as shown in Fig. 2.8. A small suction is applied through the glass pipette and this creates a high impedance seal and restricts leakage currents. Pederson et. al. [33] demonstrated the use of silicon based orifice that would help realize a giga-seal. A small suction mechanism from the backside of the chip would help push the cell into the orifice. This technique can be used in the realization of large scale integrated circuits as described by Han. et. al.[15].

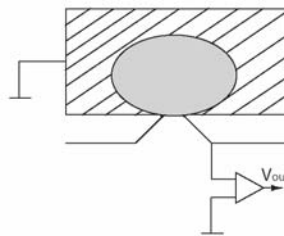
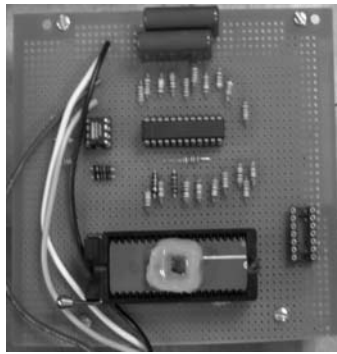
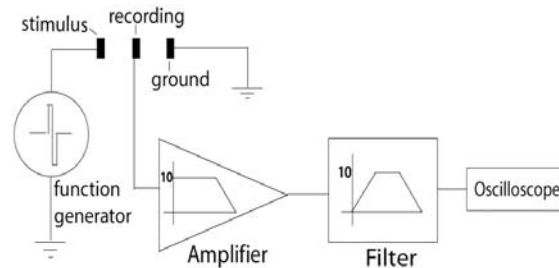


Fig. 2.8 High impedance seal technique using microstructures [33]

Another method to record activity of cells is to plate them on to electrodes, and realize amplifiers connected to these electrodes to record the extracellular activity of these cells. Reeves et. al. [37] have demonstrated extra cellular recordings from cells plated to electrodes and placed on a DIP package, and connected to external instrumentation filters and amplifiers. A block diagram of their schematic is shown in Fig. 2.9. Pancrazio et. al. [32] have also demonstrated activity from similar recording structures with the outputs being amplified, and multiplexed for interaction with PCs.



(a) The amplifier with epoxy for containing the electrolyte



(b) Block diagram of the measuring unit

Fig. 2.9 Setup for directly recording the activity of cells [37]

Jenkner et. al. [21] fabricated a silicon chip for two-way interfacing with neurons. The neurons were joined to each other by electrical synapse and to the chip by a capacitive stimulator and a recording transistor. The cells and the medium were contained in a perspex chamber made of glue, and the interfacing with the electronic circuitry was done by connecting the output pins to a standard DIP package.

Lorenzelli et. al. [25] reported the use of an ion sensitive field effect transistor (ISFET) for recording the pH variations of the medium due to cell metabolic activity. The changes in the pH cause a variation in the threshold voltage of the device and this shift is measured by sensor electronics. By integrating other sensing components like voltage regulators, multiplexers and band gap references, they automated the measurement and control process.

Abshire et. al. [1] describe integrated microstructures (cell clinics) and instrumentation for capture and characterization of individual cells. These cell clinics have a cell sized cavity and a closable lid that helps in the capture of cells. By placing gold electrodes at the base of the cell clinics, they enable the interfacing of electronic circuitry with cells. A block diagram of their cell clinic design is shown in Fig. 2.10.

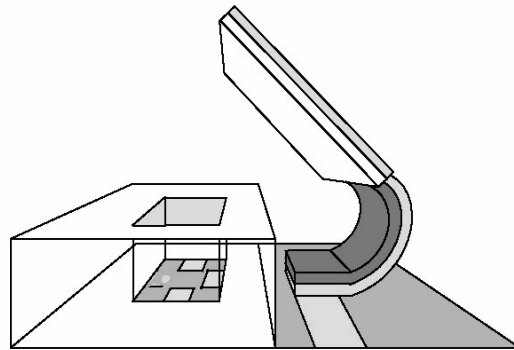


Fig. 2.10 Cell clinic for single cell sensing [1]

In the next chapter, we discuss the design of a suitable amplifier that could be used for recording the biological activity of cells

Chapter 3

Bio-amplifier Design

3.1. Introduction

We describe a bio-amplifier that is suitable for direct recording of signals from electrically active cells. The main constraints in the design are the requirement of low input referred noise, low power consumption, and a small area on chip. It should also have the capability of removing any DC offsets from the input. We describe a bio-amplifier that addresses the above issues [16]. It comprises an Operational Transconductance Amplifier (OTA) coupled in capacitive feedback configuration, as shown in Fig. 3.1.

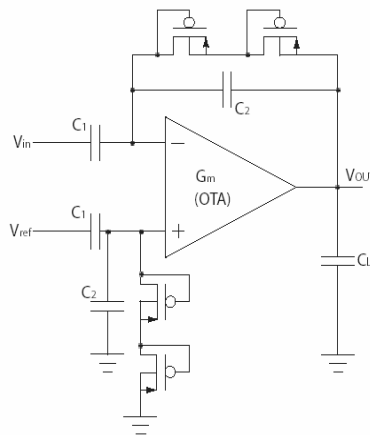
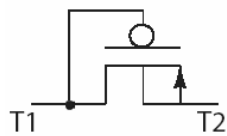


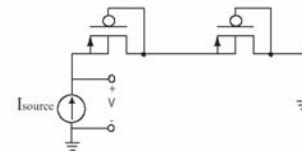
Fig 3.1 Schematic of the bio-amplifier [16]

To reduce DC offsets at the input and the output, a high resistance can be used in parallel with the feedback capacitor [16]. The resistor may not be easily realizable on chip due to area considerations. A high resistance can be implemented by a MOS transistor controlled by an external voltage, or by using a diode connected MOSFET [6] as shown in Fig. 3.1. When the terminal T_1 is

negative relative to T_2 (refer Fig. 3.2a), the gate source voltage is negative and the MOSFET channel is turned on. The MOSFET now has the gate connected to the drain and behaves like a diode. For low voltages, the current voltage relationship is exponential due to the sub-threshold region operation, and follows a square law relationship in the above threshold region. On the other hand, when the voltage of T_1 is greater than T_2 , the parasitic p-n-p transistor, with the source, the n-well, and the drain acting as the emitter, base and collector respectively is turned on. Since the base and the collector are shorted, the device behaves like a diode with exponential current voltage relationship.

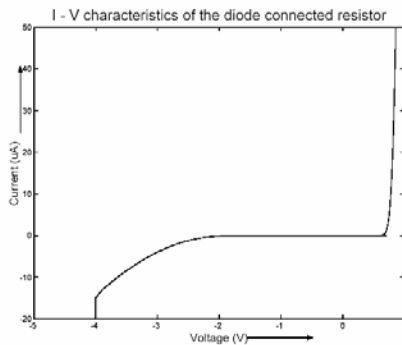


(a) Diode connected MOSFET [6]

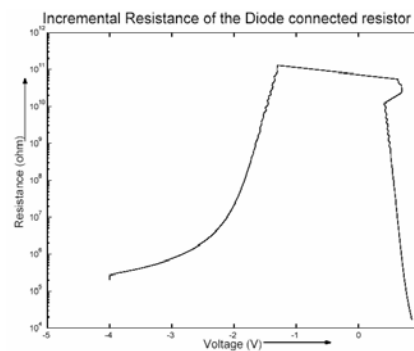


(b) Setup for measurement

Fig. 3.2 Diode connected MOSFET to implement high resistance



a. Current voltage characterisitic



b. Resistance as function of voltage

Fig. 3.3 Measured characteristics of two diode-connected MOSFETs (setup shown in Fig. 3.2 b)

The voltage current relationship across a series combination of two diode connected MOSFETs (setup shown in Fig. 3.2(b)) was measured. The reason for

using two of these devices in series is to reduce distortion for large input signals. The measurement was made by varying the bias current from the pico ampere to micro ampere using a current source unit (Keithley 216). The voltage drop across the device was measured, and the resistance was calculated from the readings. We notice that at very low currents, the back diode connected device has a very high incremental resistance (R_{inc}), and hence can be used as a high resistor which helps set the DC point. The kink at around 0.5V is because the voltage readings were fluctuating for bias currents in the 10 pA range. The reason for choosing a PMOS transistor is that the fabrication process is done on a p-substrate which will be connected to the most positive voltage of the circuit. Hence we would not be able to control the bulk voltage of the NMOS transistor as shown in Fig. 3.2(a). The PMOS transistor is fabricated in an N-well giving us the freedom to control the bulk voltage.

The midband gain of the amplifier is given by C_1/C_2 . The low frequency roll-off is given by the combination of C_2 and R_{inc} and is given by $1/2\pi R_{inc} C_2$. The high frequency roll off is determined by the output load capacitance and the equivalent resistance at output node. Cascodes are used at the output to increase the open loop gain of the OTA. The schematic of the OTA is shown in Fig. 3.4. Bias voltages for the cascade transistors were given from off chip potentiometer arrangements. M_{bias2} enables the control of amount of power supplied to bias the amplifier.

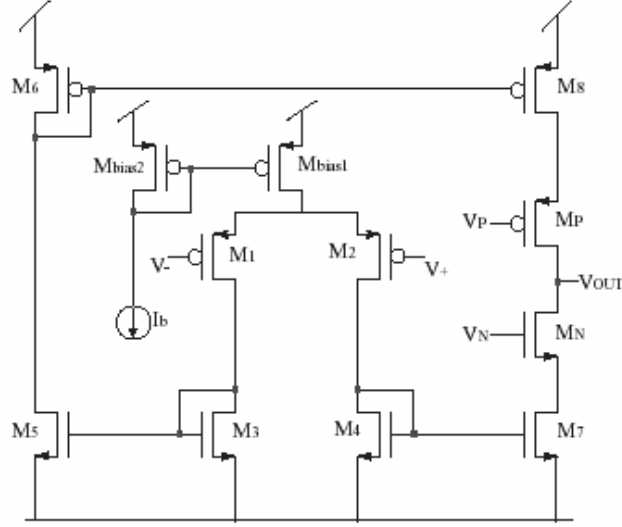


Fig 3.4 Operational Transconductance Amplifier

In designing the bio-amplifier, it is important to reduce the input referred noise voltage. The dominant noise sources in a MOSFET are the thermal and the flicker noise components [24]. The input referred noise voltage of a single MOSFET is given by [24].

$$\overline{V_n^2} = \left(\frac{4kT\gamma}{g_m} \right) + \left(\frac{KF * I_D^{AF}}{C_{ox} * f} \right) * \left(\frac{1}{g_m^2} \right) \quad (3.1)$$

where kT is the thermal voltage, γ is a constant equal to $\frac{1}{2}$ for subthreshold devices, and $\frac{2}{3}$ for transistors in the strong inversion region, g_m is the transconductance of the MOSFET, C_{ox} is the gate oxide capacitance, AF and KF are empirical constants equal to 1 and 10^{-25} respectively, and f is the frequency of operation. The first term corresponds to the thermal noise component (white noise), and the second component to the flicker noise component (colored noise).

We choose M_1 and M_2 to be identical, $M_3, M_4, M_5,$ and M_7 to be identical. The input referred noise of the OTA is calculated using transfer function analysis, and is given by (3.2).

$$\overline{V_{inOTA}^2} = 2\overline{V_{n1}^2} + 4\left(\frac{g_{m3}}{g_{m1}}\right)^2 \overline{V_{n3}^2} + 2\left(\frac{g_{m6}}{g_{m1}}\right)^2 \overline{V_{n6}^2} + \left(\frac{g_{mN}}{g_{m1}}\right)^2 \overline{V_{nN}^2} + \left(\frac{g_{mP}}{g_{m1}}\right)^2 \overline{V_{nP}^2} \quad (3.2)$$

where g_{mN} is the transconductance of transistor N and V_{nN} is the input referred noise of transistor N. From the above equation, we notice that the input referred noise can be reduced by increasing the g_m of the transistors $M_1, M_2,$ and reducing the g_m of M_3, M_4, M_5, M_6, M_N and M_P . We also notice that the OTA has three inherent poles, two at g_{m3}/C_3 and one at g_{m6}/C_6 . Hence, the reduction in the sizes of $M_3, M_4, M_5,$ and M_6 will lead to a reduction in the phase margin of the circuit. To maintain stability, they cannot be reduced arbitrarily. As described by Harrison [16], the input referred noise of the bio-amplifier can be calculated from (3.3).

$$\overline{V_{in-AMP}^2} = \overline{V_{in-OTA}^2} \left(\frac{C_1 + C_2 + C_{in}}{C_1} \right)^2 \quad (3.3)$$

For a typical gain of 100, the input referred noise of the bio-amplifier is almost the same as that of the OTA, and a reduction in the noise level of the OTA will lead to an equal reduction in the noise level of the bio-amplifier.

Another important figure of merit in the design of an amplifier is the Noise Efficiency Figure (NEF) [39] which is defined as the noise generated by the amplifier relative to the noise generated by a single bipolar junction transistor amplifier having the same total current and bandwidth. The lower the NEF, the better is the performance of the circuit, and the best possible NEF is by that of a single stage BJT amplifier and is equal to 1. The formula for calculating the NEF is given by [39] and is shown in (3.4).

$$NEF = V_{ni,rms} \sqrt{\frac{2I_{tot}}{\pi \cdot U_T \cdot 4kT \cdot BW}} \quad (3.4)$$

where $V_{ni,rms}$ is the input referred noise voltage, I_{tot} is the total current in the circuit, U_T is the thermal voltage, k is the Boltzmann constant, T is the absolute temperature, and BW is the bandwidth of the circuit. $V_{ni,rms}$ is the equivalent noise source and is calculated by integrating the input referred noise over the bandwidth of the circuit.

3.2. Device Specifications, Layouts, and Test Results

The circuits were designed using scalable CMOS design rules and fabricated through MOSIS in a commercially available 0.5μ CMOS process. We designed bio-amplifiers of gains 20, 40 and 100 for test purposes. In choosing the sizes of the transistors, we chose a high W/L for the input differential pair, a large enough L for the current mirror transistors in order to reduce the Early effect, and to increase the matching, and sufficiently long devices for the cascade transistors in order to boost the gain [38]. The device sizes of the individual transistors are

specified in Table 3.1 The value of C_2 was chosen to be greater than 200 pF so as to reduce the effect of fringing capacitances and the interconnect capacitances. C_1 was chosen to give the appropriate gain. C_1 and C_2 were placed on chip, and C_L was off chip, and included the loading of the measurement stage too. Their chosen values are listed in Table 3.2.

Transistor	Width	Length
M_1, M_2	$35\mu\text{m}$	$2.1\mu\text{m}$
M_3, M_4, M_5, M_7	$3.5\mu\text{m}$	$3.5\mu\text{m}$
M_6, M_8	$7\mu\text{m}$	$3.5\mu\text{m}$
M_N, M_P	$7\mu\text{m}$	$7\mu\text{m}$

Table 3.1 Dimensions of transistors used in the bio-amplifier

Amplifier Gain	C_1	C_2
26 dB	10pF	0.5pF
32 dB	20pF	0.5pF
40 dB	20pF	0.2pF

Table 3.2 On-chip capacitors used in the bio-amplifier

The output node is a high impedance node and is typically used for driving another on-chip stage. In designing the test fixture for characterizing the amplifier, we reduced the loading capacitance by using a commercially available op-amp in source follower configuration to buffer the output stage. The transfer functions of the amplifiers were measured using a Spectrum Analyzer (Agilent 4395A), and the bias current was supplied from a current source unit (Keithley 236). The transfer function measurements of the bio-amplifier are plotted in Fig. 3.5, and the characteristics of the amplifier are tabulated in Table 3.2.

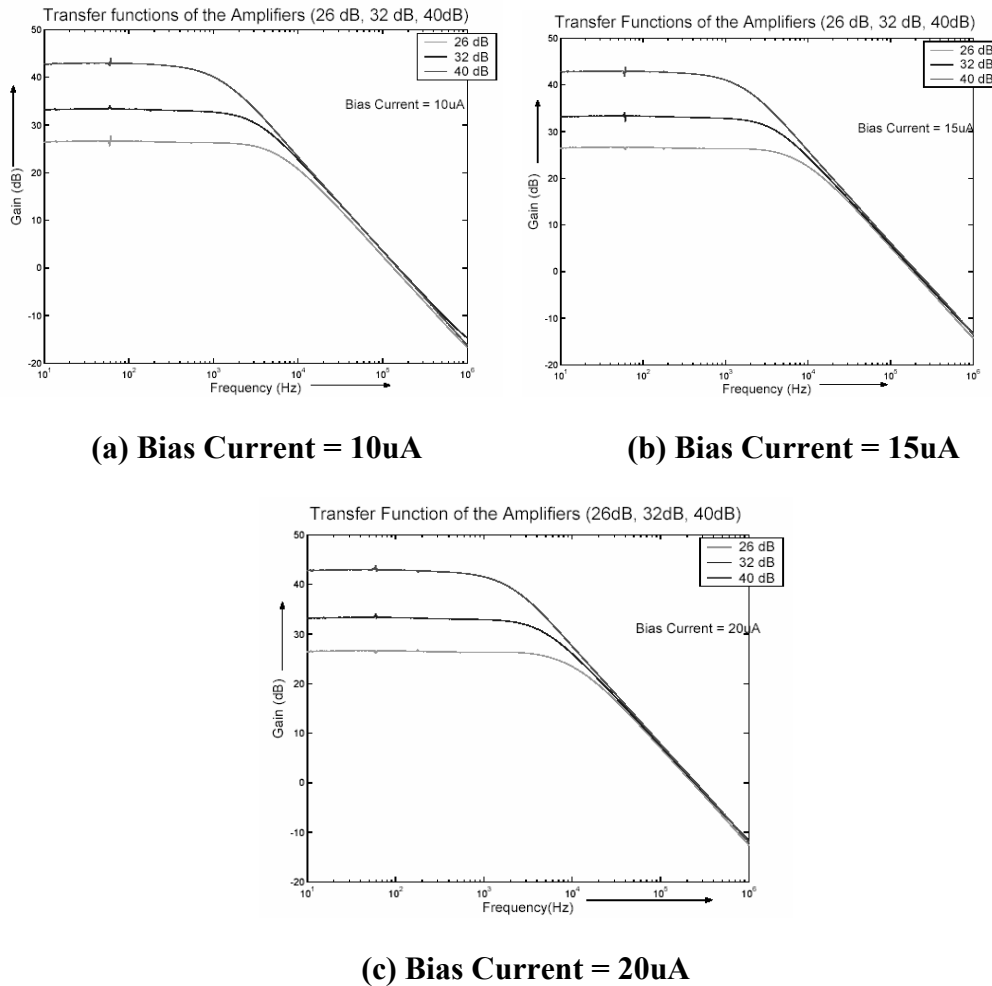


Fig. 3.5 Measured transfer functions of the amplifiers for different power dissipation

Bias Current	Power	Gain (dB)	Bandwidth	I/p referred noise	Phase Margin	NEF
10 μ A	60 μ W	42.29	1.16 kHz	1.167 μ V	85.69°	6.113
		32.84	3.55 kHz	2.6 μ V	82.6°	7.78
		26.36	6.15 kHz	9.7 μ V	86.7°	22.1
15 μ A	90 μ W	42.49	1.61 kHz	1.21 μ V	84.16°	6.588
		32.84	4.41 kHz	2.93 μ V	80.9°	9.64
		26.37	8.21 kHz	11.3 μ V	85.21°	27.25
20 μ A	120 μ W	42.36	1.96 kHz	1.303 μ V	82.92°	7.425
		32.88	5.188 kHz	3.23 μ V	79.43°	11.31
		26.36	10.21 kHz	11.4 μ V	83.70°	28.46

Table 3.3 Characteristics of the bio-amplifiers (Voltage Supply = 3V)

The designed gains were obtained, and these amplifiers appear to be suitable for integrating with the cell clinics microstructures. Their input referred noise levels in the 1.2 μ V - 11.5 μ V is also acceptable as extra-cellular signals have amplitudes of about 100 μ V. Flicker noise is the main component of noise for these amplifiers, and corner frequencies occur in the order of 100s of kHz. As expected, the noise levels increase with an increase in the total current level and

with an increase in the bandwidth. However, noise voltage levels do not vary as the square root of the bandwidth as the principal component is flicker noise. The use of PMOS transistors at the input stage has reduced the flicker noise, and hence the overall noise performance of the circuit.

The bandwidth is degraded because of the loading of the pins in the DIP package through which the output was recorded. An improvement in the bandwidth can be achieved by using on-chip loading and output driving stages to follow the amplifiers. NEF is inversely proportional to the square root of bandwidth, and hence an increase in the bandwidth would also lead to an improvement in the NEF of the bio-amplifiers.

3.3 Performance comparison with existing designs

A brief discussion of the designs and implementations of different schemes of instrumentation and neural recording amplifiers has been presented in Chapter 2. In this section, we discuss the performance metrics and characteristics designs listed in the literature. The characteristics of different amplifiers are presented in Table 3.4.

Some of the parameters for the table have not been reported by the authors, and are shown by a ‘-’ indicating missing data. All amplifiers reported here are capable of rejecting DC offsets at the input.

Authors	Voltage	Current	Power	Bandwidth	I/p referred noise	NEF
Degrauwe et. al. [5]	3 V	7 μ A	21 μ W	4 kHz	79 μ V	130
Staeysart et. al. [39]	5 V	31 μ A	155 μ W	0.570 kHz	8.2 μ V	74
Najafi et. al. [30]	3 V	44.3 μ A	133 μ W	6.5 kHz	-	-
Harrison et. al. [16]	5 V	16 μ A	80 μ W	7.2 kHz	2.2 μ V	4
Irazoqui-Pastor et. al. [20]	-	-	-	10 kHz	8 μ V	-
Horiuchi et. al. [18]	2 V	0.62 μ A	1.325 μ W	9 kHz	27 μ V	8.94
Bio-amplifier described here	3 V	20 μ A	60 μ W	1.16 kHz	1.17 μ V	6.11

Table 3.4 Performances of different instrumentation and neural amplifiers

The current and the power levels reported for our amplifier are in close agreement with other designs reported in the literature. The bandwidth of the bio-amplifier can be improved by using on-chip driving stages at the output. NEF varies inversely as the square root of the bandwidth, and hence an increase in the bandwidth would reduce the NEF of the bio-amplifier. The input referred noise of the amplifier is significantly low due to the use of PMOS input devices which have lower flicker noise than NMOS devices. The NMOS current mirrors have been sized much smaller than the input stage PMOS devices, and that reduces the noise contribution from the later stages.

Power consumption of our circuit can also be reduced by pushing the devices into sub-threshold region of operation. Horiuchi et. al. [18] achieves low power operation at $1.3 \mu\text{W}$ by operating the transistors in the sub-threshold region. In the next two chapters, we identify the limitations on voltage supply reduction to our amplifiers, and implement techniques to reduce the voltage supply and power consumption of the bio-amplifier.

3.4. Packaging for Direct Interaction with Cells

The bio-amplifier was then designed with provision for direct loading of cells. We designed an array of ten bio-amplifiers with bare aluminum pads as input. The design specifications and the layouts are exactly the same as discussed above. They were tested by applying an input signal through a passive probe and the output was observed on an oscilloscope. It gave a gain of 40 dB, and a bandwidth of 1.8 kHz as discussed in 3.2. The photograph of the array of bio-

amplifiers is shown in Fig. 3.6. These input pads to the amplifiers have to be plated with gold for bio-compatibility.

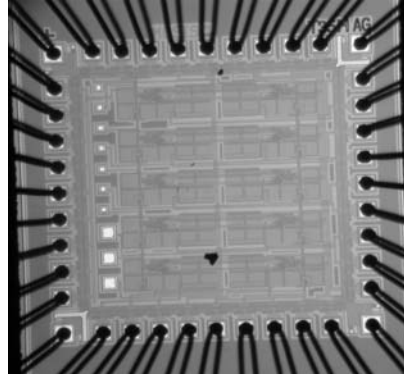


Fig. 3.6 Array of bio-amplifiers for direct recording from cells

Prior to plating of the amplifier directly with cells, we made measurements with a passive test fixture, where the cells were plated to the pads of an empty chip, and their activity was detected with discrete amplifiers and filters. The test fixture and the results of the measurement are shown in Fig. 3.7. This arrangement is more prone to noise and loss of signal strength due to the distances that the low power content signal has to travel before being amplified.

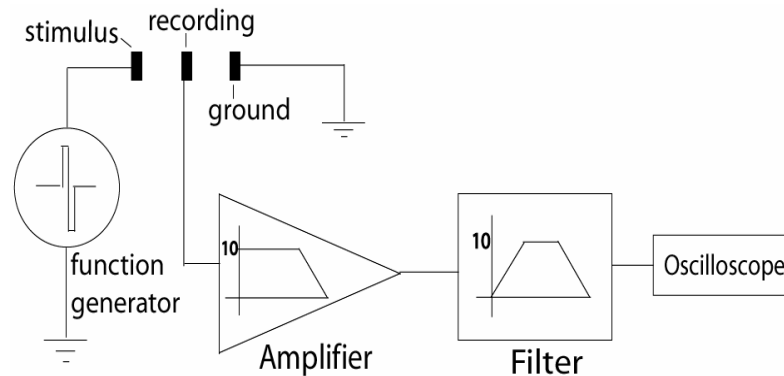


Fig. 3.7 Setup for recording from cells using discrete components

3.5. Power Supply Requirement of the Bio-amplifier

Voltage supply requirement is an important parameter in the design of the bio-amplifier, as we will be working with arrays of bio-amplifiers interfaced with cells. In this section, we identify the power supply requirements of the bio-amplifier. The above mentioned design works well with a power supply of 3V from V_{dd} to V_{ss} . The minimum required power supply for the entire circuit can be found out by tracing all the paths from V_{dd} to V_{ss} . They are listed in 3.5

$$V_{dd} - V_{SS} = V_{DSAT5} + V_{DSAT6} \quad (3.5a)$$

$$V_{dd} - V_{SS} = V_{GS3} + V_{OD3} + V_{DSAT1} + V_{DSATMbias1} \quad (3.5b)$$

$$V_{dd} - V_{SS} = V_{DSAT7} + V_{DSATN} + V_{DSATP} + V_{DSAT8} \quad (3.5c)$$

where V_{dd} and V_{SS} are upper and lower supply voltages, V_{DSATx} is the drain source saturation voltage of transistor x, V_{GSx} is the gate source voltage of transistor x, and V_{ODx} is the over-drive voltage of transistor x. Since the amplifier uses negative feedback, the output voltage V_{OUT} and the input voltages $V_{\{+,-\}}$ should be at the same potential. This introduces a new path which has to be considered while reducing the power supply. The power supply requirement for that path is given by (3.5d). If M1 and M2 are operated in weak inversion, then V_{OD1} may not be of concern in the design.

$$V_{dd} - V_{SS} = V_{DSAT7} + V_{DSATN} + V_{SG1} + V_{OD1} + V_{DSATMbias1} \quad (3.5d)$$

The voltage supply requirement given by 3.4c and 3.4d are significantly higher than the requirements given by 3.4a and 3.4b. These are the limiting factors in the reduction of the power supply of the OTA. In the next chapter, we analyze a few low voltage techniques that have been applied to CMOS circuit design. In chapter 5, we apply these methods to reduce the power supply requirement of our bio-amplifier.

Chapter 4

Low Power Techniques

4.1. Introduction

Low power techniques are important for integrated circuits as they enhance the level of integration by limiting heating effects and enable operation from single cell batteries. With processes scaling down to the submicron level and the voltage levels accordingly, and switching speeds of digital circuits reaching the GHz range, different techniques for the reduction of power supply and voltage levels are necessary and are being implemented. These low power techniques play an important role in the design of various portable devices like electronic watches, low power calculators, and hearing aids. They have also gained considerable importance in the design of implanted biomedical devices like cardiac pace setters and neural amplifiers.

Circuits described here are intended to directly record the activity of live cells. The need for low power circuits is important to prevent the evaporation of the electrolyte, and to prevent any temperature disturbance of the normal operation of these cells. The use of low power techniques also limits the temperature gradients from circuit power dissipation. Besides, the use of low power amplifiers will also enable integration of amplifiers with large arrays of recording microstructures and microelectrodes.

In the design of analog circuits, the reduction of voltage and current levels usually involves tradeoffs in dynamic range and speed. Most of these tradeoffs are

generally accepted and can be minimized by implementing different circuit techniques. In this chapter, we discuss some of the blocks used in our amplifier design, and the tradeoffs involved in low power operation.

4.2. Circuit Blocks

4.2.1. Transistor

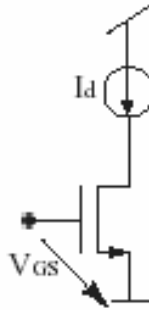


Fig. 4.1 Simple transistor

The transistor can be either in the strong inversion or the weak inversion region depending on whether its gate to source voltage is above or below its threshold voltage. The current and the transconductance (g_m) of the transistor are higher in strong inversion region. To enable power reduction techniques, the current levels are pushed down requiring the transistors to be biased in the weak inversion region. This reduces the g_m of the transistors. To compensate for the reduction in g_m , the aspect ratios (W/L) have to be increased.

The primarily dominant noise sources in a MOSFET are thermal and flicker noise. The input referred noise of the MOSFET M_1 shown in Fig. 1 is given by (3.1) Biasing the transistor in the subthreshold region enables low power operation by reducing the current levels. The saturation voltage of the transistors is also only about 80mV, and hence lower power supply levels can be reached.

The cost of operation in the subthreshold region is the reduced transconductance and increased input referred noise.

4.2.2. Current Mirror

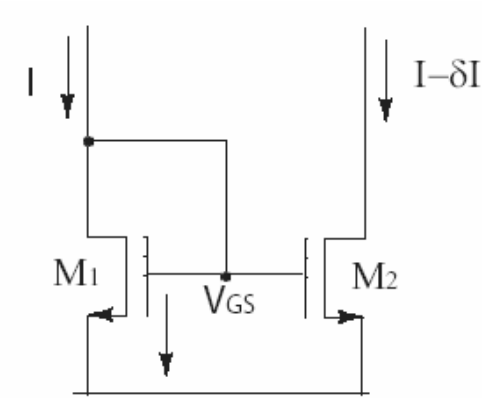


Fig. 4.2 Schematic of a current mirror

A simple current mirror schematic is shown in Fig. 4.2. It is widely used in the design of analog circuits [38], and its matching properties are very important. Mismatch in current mirrors has been studied and modeled by various research groups [34, 8]. The variation between the two drain currents arises mainly due to variations in the threshold voltages and the sizes of the two transistors in the fabrication processes. A simple first order derivation for the mismatch (ΔI_d) can be derived as follows [11, 34].

$$\begin{aligned}
 I_d &= \beta(V_{GS} - V_{T0})^2 \\
 \Rightarrow \Delta I_d &= (V_{GS} - V_{T0})^2 (\Delta\beta) + \beta \left(\Delta(V_{GS} - V_{T0})^2 \right) \\
 \Rightarrow \frac{\Delta I_d}{I_d} &= \frac{(\Delta\beta)}{\beta} - \left(\frac{2\Delta V_T}{(V_{GS} - V_{T0})} \right) \tag{4.1}
 \end{aligned}$$

where $\beta = \mu C_{ox} W/L$, and V_{T0} is the threshold voltage of the MOSFETs. The standard deviation $\sigma(I_d)$ of the current mismatch is given by (4.2)

$$\frac{\sigma^2(I_d)}{I_d^2} = \frac{4\sigma^2(V_{T0})}{(V_{GS} - V_{T0})^2} + \frac{\sigma^2(\beta)}{\beta^2} \quad (4.2)$$

where the σ_x is the standard deviation of x . At moderate and weak inversion operation, this mismatch term is given by (4.3)

$$\frac{\sigma^2(I_d)}{I_d^2} = \left(\frac{g_m}{I_d}\right)^2 \sigma^2(V_{T0}) + \frac{\sigma^2(\beta)}{\beta^2} \quad (4.3)$$

The first term models the mismatch effect due to variations in the threshold voltages, and the second term the effect due to the variations due to size mismatch. We observe that biasing the transistors in strong inversion can reduce the threshold voltage mismatch factor. Weak inversion topologies are generally not preferred for current mirrors as $\frac{g_m}{I_d}$ ratio is highest for a transistor at weak inversion.

The second term models the mismatch effect due to size variations. Increasing the width and the length of the transistors can reduce the size mismatch factor. Choice of minimum length transistors is not preferred for current mirrors also due to the Early voltage effect. For submicron processes, and short/narrow devices, this first order approximation cannot be used as fabrication parameters play an important role. A more rigorous analysis for submicron processes has been done in [8], and their results follow a similar trend to 4.1 for long and wide devices, and devices operating the strong inversion region.

In reducing the voltage supply of our amplifier, care should be taken to account for the strong inversion of the current mirror.

4.2.3. Transconductor

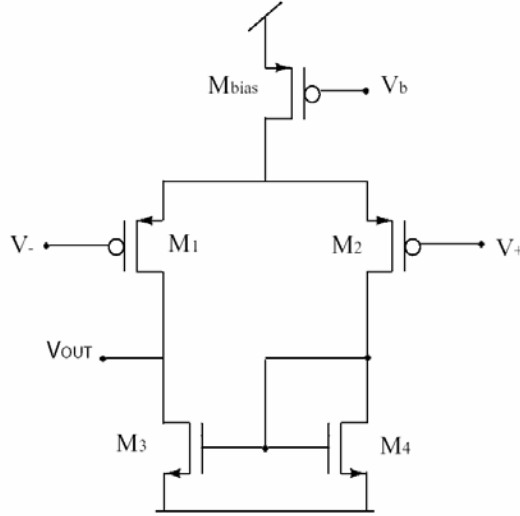


Fig. 4.3 Schematic of a basic transconductor

The basic transconductor shown in Fig. 4.3 is a building block in many analog amplifier configurations. It comprises a differential pair (M_1 and M_2), a current mirror (M_3 and M_4), and a current source (M_{bias}). The voltage supply requirement for this configuration is determined by the requirement that all transistors are saturated, and the current mirror transistors are in strong inversion. Assuming perfectly matched devices, the voltage requirement is given by (4.4)

$$V_{dd} - V_{ss} = V_{T3} + V_{OD3} + V_{DSAT1} + V_{DSATMbias} \quad (4.4)$$

where V_{T3} is the threshold voltage of M_3 , V_{OD3} is the overdrive voltage of M_3 to keep it in strong inversion, V_{DSATx} is the saturation voltage of transistor x .

Decreasing the current level can reduce the power consumption of this circuit. This can be achieved by operating the differential pair in the subthreshold region. To compensate the degradation in the transconductance due to the decrease in current levels, the aspect ratios of M_1 and M_2 have to be increased. The aspect ratio of the current mirror transistors should be small to reduce their gate source voltage. The current source M_{bias} can also be operated in the subthreshold region. Operating the transistors M_1 , M_2 and M_{bias} in subthreshold region also reduces their saturation voltage, and this reduces the V_{dsat} terms of 4.4.

The input referred noise of this circuit can be calculated using transfer function analysis [24], and is given by (4.5)

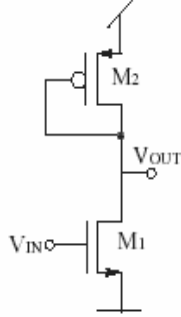
$$\overline{V_i^2} = \overline{V_1^2} + \left(\frac{g_{m3}}{g_{m1}} \right)^2 \overline{V_3^2} \quad (4.5)$$

Designing the aspect ratios of the transistors so as to keep $g_{m1} \gg g_{m3}$ reduces the input referred noise of the circuit.

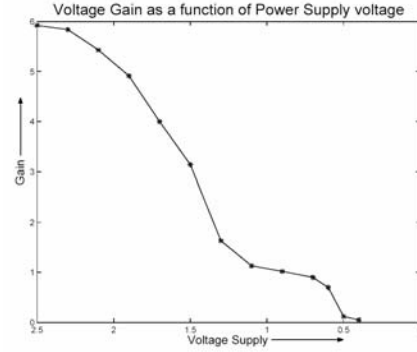
4.2.4. Voltage Gain Unit

Operating the transconductor in the subthreshold region with a very strict power budget will lead to a significant reduction in the transconductance and also the dynamic range. To compensate for this reduction, we used a voltage gain unit comprising a single stage common source transistor with a diode-connected load as shown in Fig.4.4a. Simulations for the gain of these units were made at different voltage supply levels using Cadence. The DC level of V_{in} was varied to

keep the two transistors in saturation. The results of simulation are plotted in Fig. 4.4b.



(a) Voltage gain units



(b) Simulated voltage gain as function of supply voltage

Fig. 4.4 Voltage gain units and their gain as function of supply voltage

The gain of this stage is maximum when the two transistors are in strong inversion [40]. As the voltage supply of this circuit is reduced, the two transistors leave strong inversion and enter into the weak inversion region, and the overall gain is reduced. The input referred noise of this circuit is given by (4.6)

$$\overline{V_{in}^2} = \overline{V_1^2} + \left(\frac{g_{m2}}{g_{m1}} \right)^2 \overline{V_2^2} \quad (4.6)$$

By increasing g_{m1} to be much greater than g_{m2} , we can minimize the input referred noise of the voltage gain units.

4.3. Voltage Follower Technique

The power supply requirement of the basic transconductor is given by (4.4). The dominant term is the gate to source voltage of the current mirror transistors. The direct connection between the gate and the drain is to ensure that

the gate voltage tracks the voltage changes in the drain, and also to maintain the output transistor in deep saturation. This connection can be removed and replaced with a voltage follower circuit [35] which drives the gate to track voltage changes in the drain as shown in Fig. 4.5

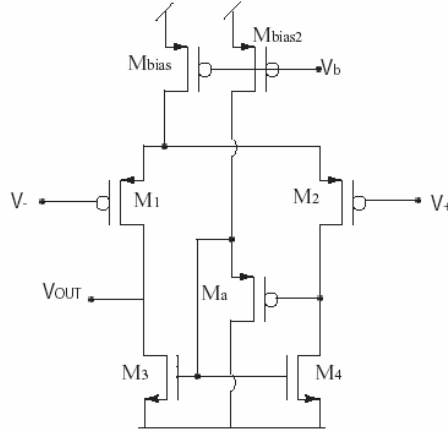


Fig. 4.5 Improved transconductor structure for low voltage operation [35]

It uses a PMOS current conveyor configuration as opposed to the more common NMOS current conveyor arrangement to drive the current mirror. The voltage supply requirement of the improved transconductor structure is given by

$$V_{dd} - V_{ss} = V_{T3} + V_{OD3} + V_{DSATMbias2} \quad (4.7)$$

The current source and the differential pair transistors are operated in the subthreshold region, and the current mirror is biased in the strong inversion. The transistor M_{bias2} need not support large currents and can be in weak inversion. By operating it in weak inversion, its saturation voltage can be reduced to about 80mV and the power supply requirement can be reduced. The differential pair transistors are made very large to improve the transconductance. The drain source saturation voltage of M_3 and M_4 is provided by the difference in the gate source voltages of M_4 and M_a . Hence the aspect ratio of M_a has to be large to keep the

current mirror in strong inversion and in deep saturation. The input referred noise of this circuit is the same as shown in (4.6).

Schematics of the NMOS and the PMOS current conveyor circuits are shown in Fig. 4.6. Their small signal circuit models are exactly identical.

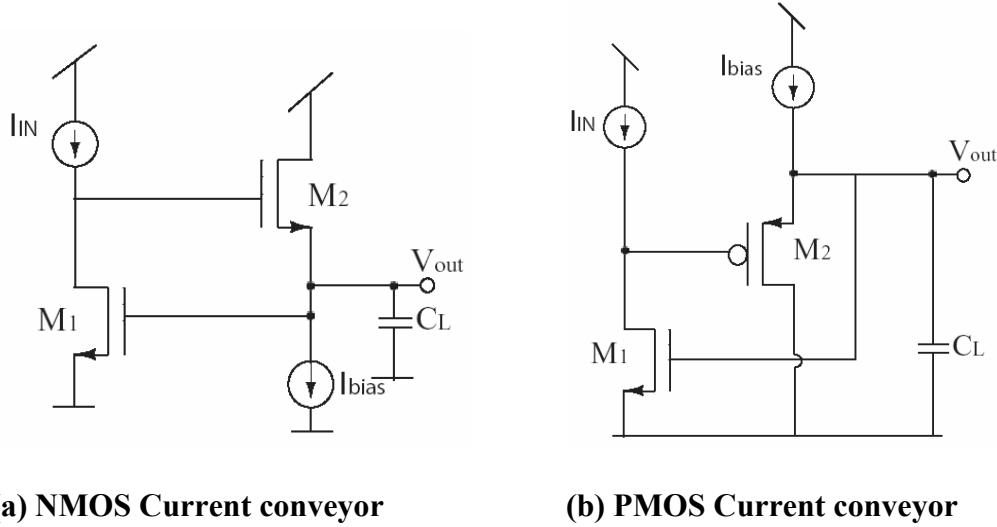


Fig. 4.6 Current conveyor configurations

The PMOS current conveyor was biased with a very small current to provide the saturation of the current mirror transistors at low supply voltages. This could potentially lead to a stability problem, and we performed a small signal analysis to analyze the same. The transfer function V_{out}/I_{in} is shown in (4.8).

$$\frac{V_o}{I_{in}} = \frac{g_{m2} + sC_2}{s^2 C_2 C_L + s \left(\frac{C_2}{r_{o2}} + \frac{C_2 + C_L}{r_{o1}} + g_{m1} C_2 \right) + \left(g_{m1} g_{m2} + \frac{g_{m2}}{r_{o1}} + \frac{1}{r_{o1} r_{o2}} \right)} \quad (4.8)$$

It is a second order response, and it has a peaking nature at high frequencies. The Q factor is given by (4.9)

$$Q = \frac{\sqrt{C_2 C_L \left(g_{m1} g_{m2} + \frac{g_{m2}}{r_{01}} + \frac{1}{r_{01} r_{02}} \right)}}{\frac{C_2}{r_{02}} + \frac{C_2 + C_L}{r_{01}} + g_{m1} C_L} \propto \sqrt{\frac{g_{m2}}{g_{m1}}} \quad (4.9)$$

where C_2 is the gate source capacitance of M_2 , r_{0x} is the output resistance of transistor x , g_{mx} is the transconductance of transistor x , and C_L is the loading capacitance of other transistors connected to that node. The results of simulations for different g_{m1} and g_{m2} are shown in Fig. 4.7.

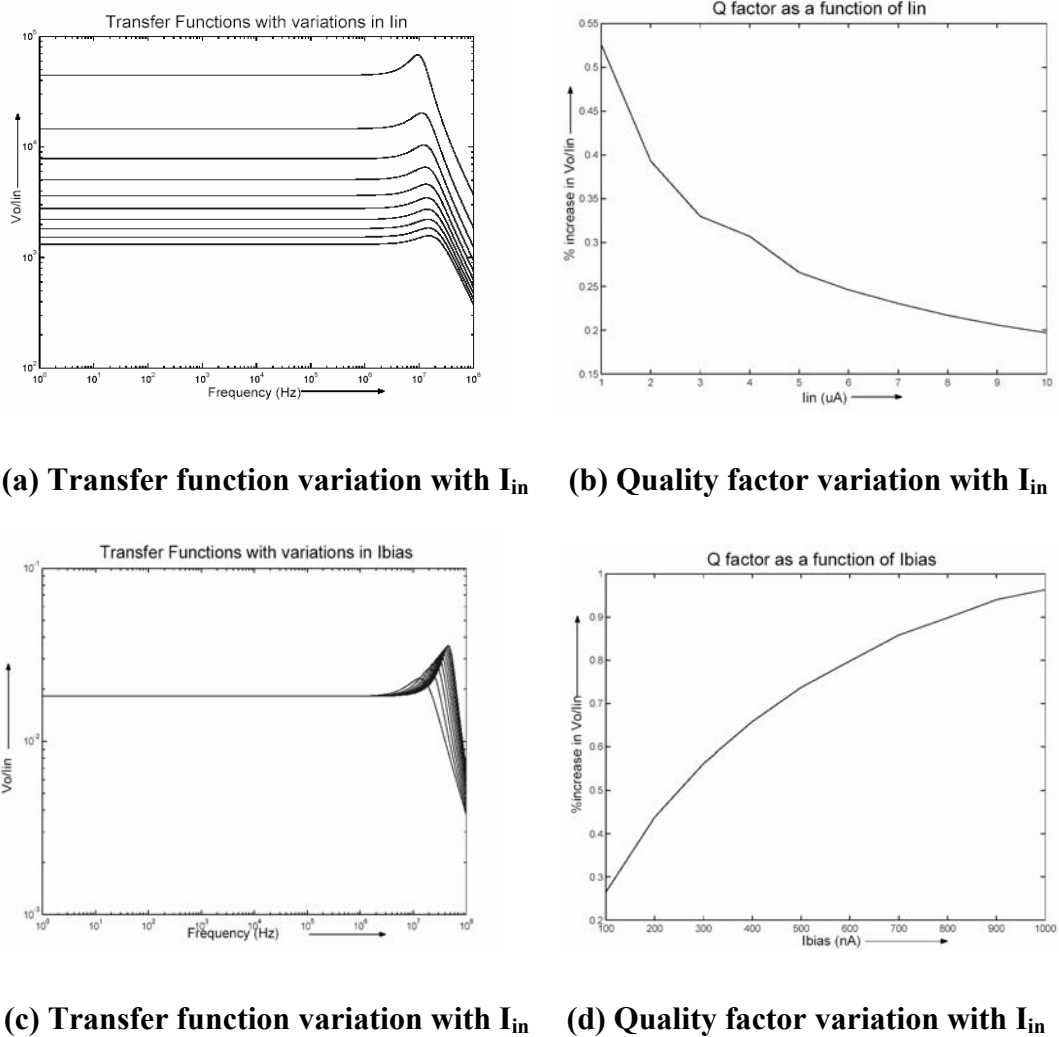


Fig. 4.7 Simulated transfer functions & Quality factors with variations in

$I_{in}(g_{m1})$ & $I_{bias}(g_{m2})$

Fig. 4.7(a) shows the variation of the quality factor for different values of g_{m1} with g_{m2} constant. There is a potential instability at frequency ranges of about 1 MHz, and is plotted in Fig. 4.7(b). This shows that for a given I_{bias} , it is better to have a higher I_{IN} . We chose I_{bias} to be 100nA, and I_{in} to vary from 1 μ A to 10 μ A for the simulations. Similarly, Fig. 4.7(c) shows the variation of the quality factor for different values of g_{m2} with g_{m1} fixed. For a given I_{IN} , it is better to have a lower I_{bias} to reduce the peaking nature of the response. The value of I_{in} was chosen to be 5 μ A and the bias current was varied from 100nA to 1 μ A for the simulations. These peaks occur at high frequencies of around 1 MHz, and can be avoided by operating the circuits at lower frequency ranges.

We designed a low voltage transconductor as described above. We tested the performance of the open loop gain of the transconductance amplifier at low voltage supplies of around 1V. A buffer was used while making measurements. The results of the measurement are shown in Fig. 4.8.

The open loop gain of these transconductance amplifiers showed gains of over 20dB at a voltage supply level of 1V, and gains of over 50dB at 1.16V. Threshold voltages of the PMOS and the NMOS devices are 0.75V and 0.93 V, and that limited the power supply reduction of our design. Sub-volt operation of this transconductor can be achieved by employing processes with lower threshold voltages.

Transfer Function Measurements of the modified Transconductor

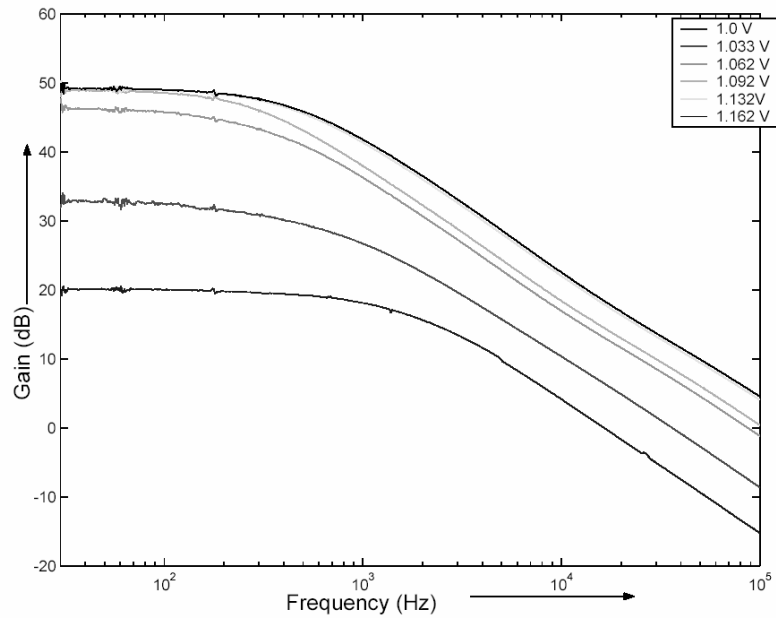


Fig. 4.8 Measured transfer function response of the improved transconductor at low voltage operation

Using this transconductance amplifier, a low pass filter was developed as described in [35], to test the functionality of these transconductors at near 1 V operation. This filter could also be later used in RF communication systems. It is a second Bessel filter realized using the repetitive $g_m C$ structures as shown in Fig. 4.9.

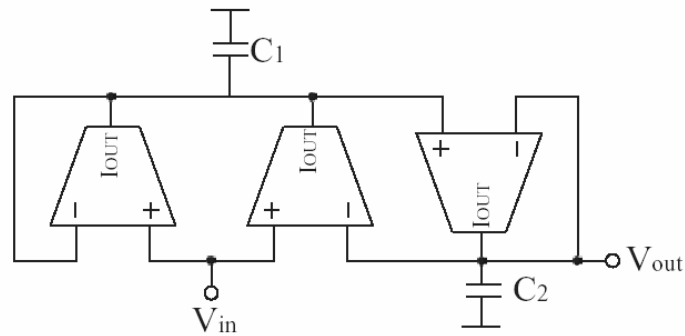
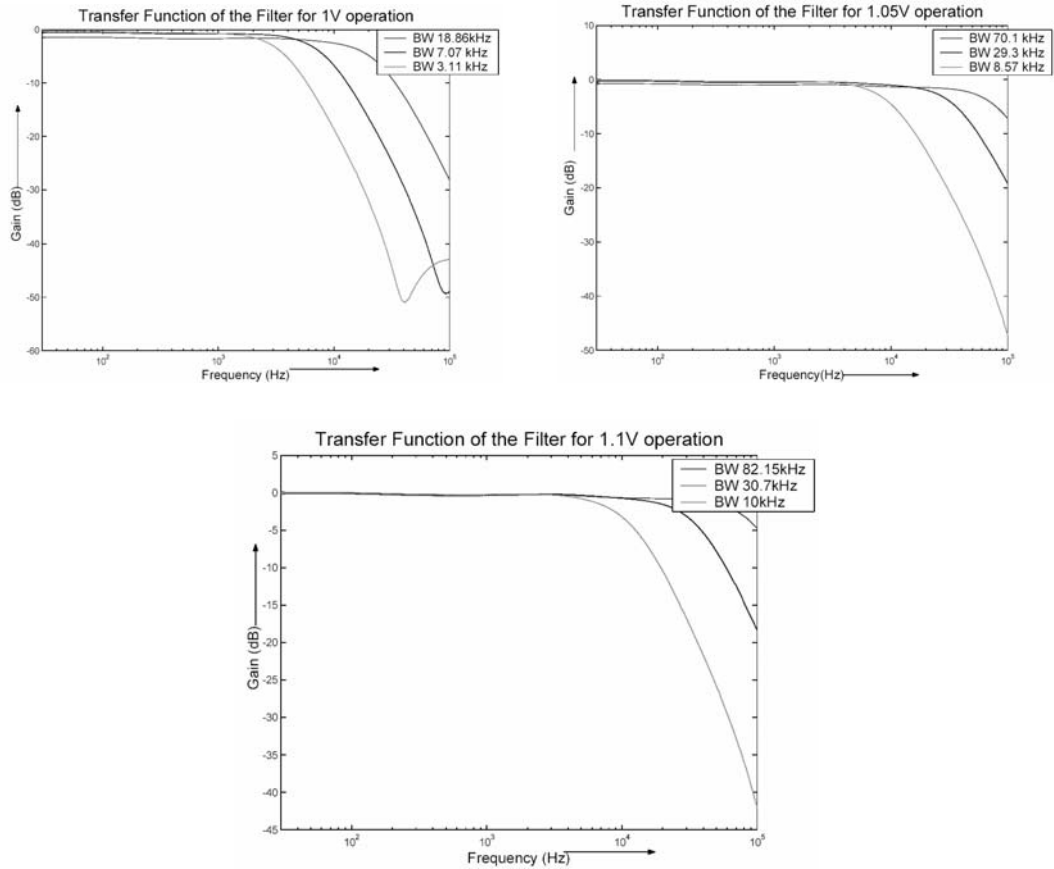


Fig. 4.9 2nd order low pass filter

Its transfer function is given by (4.10).

$$\frac{V_{out}}{V_{in}} = \frac{1}{1 + s \frac{C_1 + C_2}{2g_m} + s^2 \frac{C_1 C_2}{2g_m^2}} \quad (4.10)$$

Varying the g_m of the transconductance structures can control the cutoff frequency. This in turn can be achieved by tuning the bias current. The test results of our filter at very low voltages, and different control voltages are shown in Fig, 4.10 and tabulated in Table 4.1.



(c)

Fig. 4.10 Transfer functions of the 2nd order filter at different voltage levels. The transfer functions are measured for different values of the control voltage, showing the tunable range of operation.

Voltage Levels	Bandwidth	Gain
1 V	18.86 kHz	-1.5 dB
	7.07 kHz	-0.705 dB
	3.11 kHz	-0.3 dB
1.05 V	70.1 kHz	-1 dB
	29.3 kHz	-0.48 dB
	8.57 kHz	-0.37 dB
1.1 V	82.15 kHz	-0.29 dB
	30.7 kHz	-0.25 dB
	10 kHz	-0.226 dB

Table 4.1 Characteristics of 2nd order filter at different voltage supply levels.

The transfer function of the filter was measured at various low voltage levels. At each power supply level, the bandwidth of the filter was controlled by varying its g_m , which was achieved by tuning the bias voltage. The filter gave a unity gain, and a high range for the bandwidth at voltage supply levels of 1.05V, and gives encouraging results for operating OTA based structures at around 1V.

The low voltage and the low power techniques described in this chapter are very significant to the amplifier that is described in chapter 3. The building blocks of the bio-amplifier described in chapter 3 essentially comprise transistors, current mirrors and a transconductor. In the next chapter, I discuss the applications of these principles to modify the bio-amplifier for low voltage low power operation.

Chapter 5

Low Voltage Techniques applied to the Bio-amplifier

The two main limitations in reducing the power supply for the bio-amplifier is determined by the two paths given by 3.5c and 3.5d. In this chapter, we present methods that help us counteract these limitations.

5.1. Voltage Follower

The voltage requirement in 3.5c arises primarily from the gate source voltage of the current mirror transistor M_3 . This voltage cannot be reduced too much as that would lead to a degradation in the matching properties of the current mirror. We also note that the purposes of the drain source connections of M_3 and M_4 are to keep them in saturation and to make the voltage of the gate follow any changes in the drain voltage. This can be achieved by using the voltage follower circuit principle described in Section 4.3. The OTA modified with the voltage follower circuit is shown in Fig. 5.1

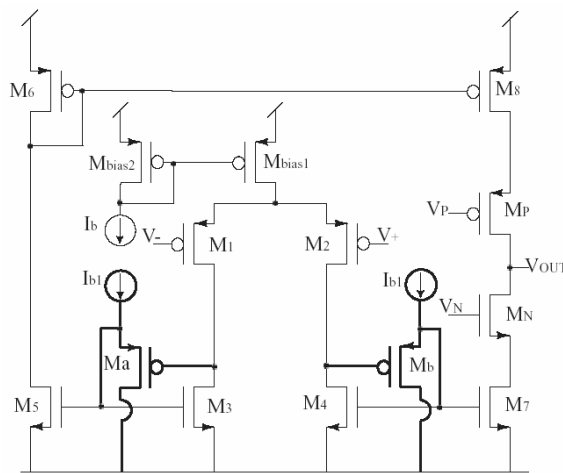


Fig. 5.1 OTA modified with voltage follower for low voltage operation

This arrangement echoes the current conveyor current mirror, using a PMOS rather than the more conventional NMOS source follower for an NMOS current mirror. M_a and M_b are connected in the source follower configuration which drives the gate of M_3 and M_4 to follow changes in their drain voltages. The drain source voltage of M_3 is given by the difference in the gate to source voltages of M_3 and M_a . By choosing a low value of I_{b1} and large aspect ratios for M_a and M_b , M_3 and M_4 can be kept in saturation. The power supply requirement in that path is now given by

$$V_{dd} - V_{SS} = V_{DSAT3} + V_{DSAT1} + V_{DSATMbias1} \quad (5.1)$$

The dominant term in the power supply requirement is

$$V_{dd} - V_{SS} = V_{T3} + V_{OD3} + V_{DSATMbias2} \quad (5.2)$$

where $V_{DSATMbias2}$ corresponds to the saturation voltage of the transistor used to realize the current source I_{b1} . By biasing the transistor M_a and M_{bias2} in weak inversion, the $V_{DSATMbias2}$ term can be reduced to 80 mV, thus reducing the power supply requirement in that path.

5.2. Level Shifting

The other factor that limits the reduction in power supply is the term that arises due to the feedback in the whole amplifier. The dominant term in 3.5d is the gate to source voltage of M_1 and M_2 . By introducing a level shifting circuit, we can enable a reduction in the power supply requirement. Simple level shifting circuits can be realized using single transistors biased in the common source configuration as shown in Fig. 5.2.

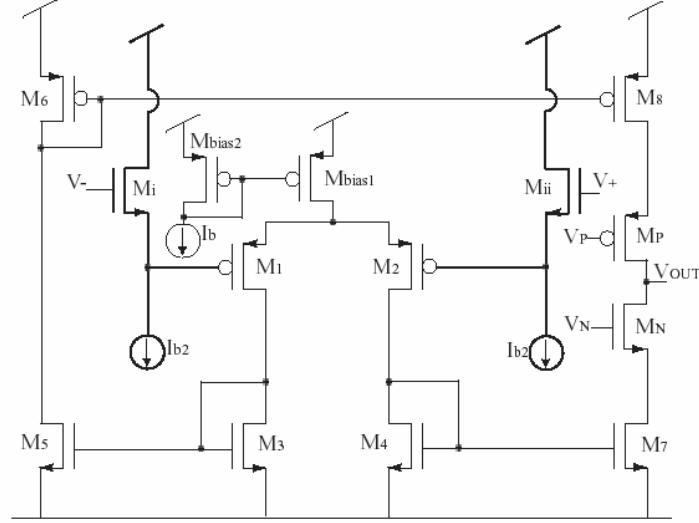


Fig. 5.2 OTA modified with level shifter for low voltage operation

The introduction of the level shifter removes the necessity for the output node and the gates of M_1 and M_2 to be at the same level. The input voltages are transferred to the differential pair by the source follower transistors. By choosing appropriate bias current I_{b2} and sizing the source follower transistors M_i and M_{ii} , M_{bias1} can be kept in saturation, and M_1 , M_2 can be operated either in the subthreshold or in the strong inversion regime. The power supply requirement in that path is now given by (5.3).

$$V_{dd} - V_{SS} = V_{DSAT7} + V_{DSATN} - V_{GSi} + V_{SGI} + V_{ODI} + V_{DSATMbias1} \quad (5.3)$$

By introducing a common source configuration transistor to provide the level shifting, we do not introduce any additional gain in the process of level shifting; thus making the cascodes at the output necessary. We could introduce a gain in the level shifting process by using a transistor in the common source configuration to perform the level shifting process as shown in Fig. 4.3. The open loop gain of the amplifier can be increased by providing sufficient gain in the

common source stage, and the cascades at the output stage can be removed. This would also give the amplifiers a higher bandwidth.

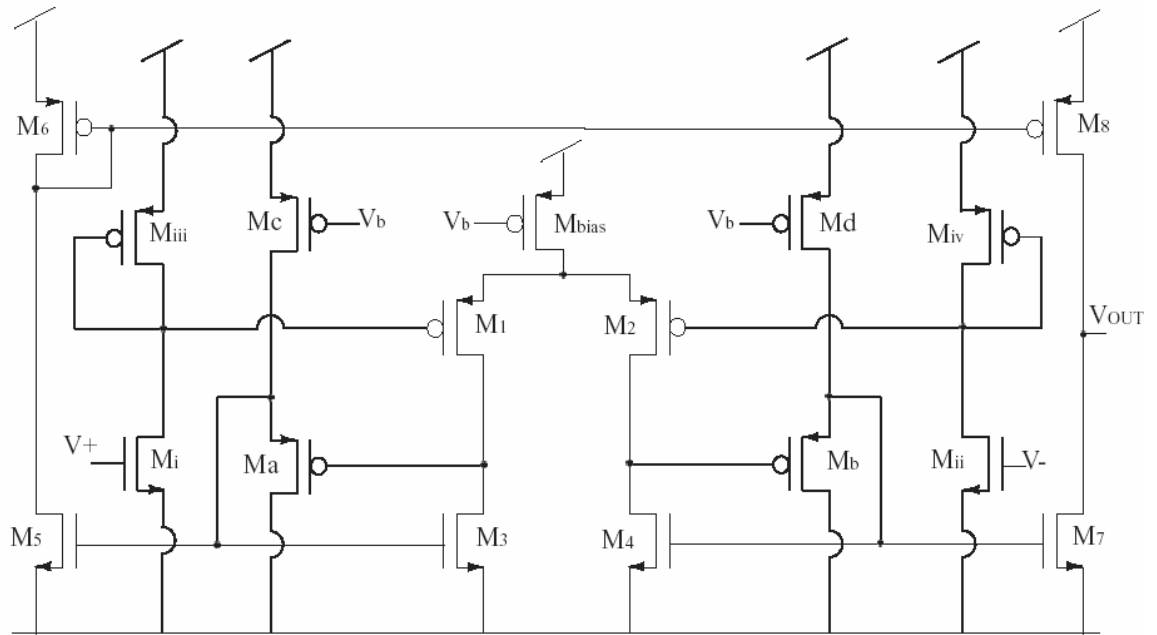


Fig. 5.3 OTA modified with voltage follower, and gain in the level shifter for low voltage operation

Transistors M_a and M_b act as the voltage follower, M_c and M_d are the biasing current sources for M_a and M_b . Transistors M_i and M_{ii} act as the level shifter transistors and are biased in the common source mode to provide additional gain. M_{iii} and M_{iv} are diode connected loads for M_i and M_{ii} . The design has also been realized with a NMOS differential pair.

5.3. Design Considerations

While designing the circuits, the aspect ratios of the transistors and the bias currents must be chosen in order to keep all the transistors saturated. In implementing the voltage follower configuration, we note that the drain to source voltage of the transistor M_3 is provided by the difference in the gate source

voltages of M_3 and the source gate voltage of M_a . Hence, to keep M_3 saturated, we reduce the source gate voltage of M_a by choosing a large W/L and a small current through it. The current cannot be made very small as that will degrade the voltage following capability of the transistors M_a and M_b .

The gate to source voltages of M_1 and M_2 and the saturation voltage of the bias transistor M_{bias} is provided by the gate to source voltages of M_{iii} and M_{iv} . Hence we choose small aspect ratios for them, and a sufficiently high bias current. Choosing a high bias current also increases the gain of the common source stages, but at the cost of increased power.

The modified OTA structure has three inherent poles given by $g_{m\text{-iii}}/C_{gs1}$, $g_{m\text{-6}}/(C_{gs6} + C_{gs8} + C_{ds8}(1 + A_8))$, and $1/C_{gsa-35}(r_{01} \parallel r_{03})$ where $g_{m\text{-n}}$ is the transconductance of transistor n , C_{gsn} is the gate to source capacitance of transistor n , A_8 is the gain at the output stage taken in order to account for the Miller effect, r_{0n} represents the output resistance of transistor n in the small signal approximation. C_{gsa-35} is the effective capacitance of C_{gsa} in series with C_{gs3} and C_{gs5} , given by (5.4).

$$C_{gsa-35} = \frac{C_{gsa}(C_{gs3} + C_{gs5})}{C_{gsa} + C_{gs3} + C_{gs5}} \quad (5.4)$$

By reducing the lengths of M_a and M_b , C_{gsa} is reduced and g_m is increased which enhances its voltage following capability. Minimum lengths were chosen for M_a and M_b . The value of the load capacitance should be chosen depending on

the required bandwidth, and should also ensure a safe phase margin. Higher open loop gains may be achieved by adding output cascodes to the circuit in Fig. 5.3, at the cost of reduced output swing. The sizes of all the transistors in the circuits are summarized in table 5.1. We also fabricated an amplifier with the level shifter being realized using a source follower transistor, and the gain being boosted with cascodes at the output. The sizes of the transistors in the circuit are summarized in table 5.1(c).

Transistor	Width	Length
M ₁ , M ₂	35μm	1.75μm
M ₃ , M ₄ , M ₅	3.5μm	3.5μm
M ₆	10.5μm	3.5μm
M ₇	7μm	3.5μm
M ₈	21μm	3.5μm
M _i , M _{ii}	17.5μm	1.75μm
M _{iii} , M _{iv}	3.5μm	7μm
M _a , M _b	35μm	0.7μm
M _c , M _d	1.75μm	7μm

(a) PMOS Ddifferential pair

Transistor	Width	Length
M ₁ , M ₂	21μm	1.75μm
M ₃ , M ₄ , M ₅	3.5μm	3.5μm
M ₆	10.5μm	3.5μm
M ₇	3.5μm	3.5μm
M ₈	10.5μm	3.5μm
M _i , M _{ii}	35μm	1.4μm
M _{iii} , M _{iv}	3.5μm	7μm
M _a , M _b	17.5μm	0.7μm
M _c , M _d	7μm	3.5μm

(b) NMOS Differential pair

Transistor	Width	Length
M_1, M_2	$35\mu\text{m}$	$1.75\mu\text{m}$
M_3, M_4, M_5	$3.5\mu\text{m}$	$3.5\mu\text{m}$
M_6	$10.5\mu\text{m}$	$3.5\mu\text{m}$
M_7	$7\mu\text{m}$	$3.5\mu\text{m}$
M_8	$21\mu\text{m}$	$3.5\mu\text{m}$
M_N	$7\mu\text{m}$	$7\mu\text{m}$
M_P	$21\mu\text{m}$	$7\mu\text{m}$
M_i, M_{ii}	$35\mu\text{m}$	$1.75\mu\text{m}$
M_{iii}, M_{iv}	$3.5\mu\text{m}$	$7\mu\text{m}$
M_a, M_b	$35\mu\text{m}$	$0.7\mu\text{m}$
M_c, M_d	$3.5\mu\text{m}$	$7\mu\text{m}$

(c) Source Follower as level shifter

Table 5.1 Sizes of transistors used in the amplifiers (a) Amplifier with the PMOS differential pair (b) Amplifier with the NMOS differential pair, (c) Amplifier with the source follower and cascodes

5.4. Noise Analysis

In this subsection, we calculate analytically the input referred noise for the amplifiers described in Section 5.2. We first calculate the input referred noise of the amplifiers with the common source level shifting stage. The transistors in the circuit are perfectly matched: $M_1 = M_2$, $M_3 = M_4 = M_5 = M_7$, $M_6 = M_8$, $M_a = M_b$, $M_c = M_d$, $M_i = M_{ii}$, $M_{iii} = M_{iv}$. Their input referred noise is given by (5.5)

$$\overline{V}_N^2 = 2 \left(\overline{V}_i^2 + \left(\frac{g_{m_{iii}}}{g_{m_i}} \right)^2 \left(\overline{V}_{iii}^2 + \overline{V}_1^2 + \left(\frac{1}{g_{m_l}(r_{01} \parallel r_{03})} \right)^2 \left(2\overline{V}_3^2 + \overline{V}_a^2 + \left(\frac{g_{m_b}}{g_{m_a}} \right)^2 \overline{V}_b^2 + \left(\frac{g_{m_6}}{g_{m_5}} \right)^2 \overline{V}_6^2 \right) \right) \right) \quad (5.5)$$

where V_x is the input referred noise of transistor x , g_{m_x} is the transconductance of transistor x , and r_{0x} is the output resistance of transistor x . The calculation has been performed based on small signal analysis as explained in [24]. It can be performed in a similar manner even for circuits that do not have completely matched devices. The maximum contribution of noise voltage is due to the input stage transistors M_i and M_{ii} . It can be reduced by increasing their g_m . The noise from the subsequent stages can be reduced by increasing $g_{m_i} \gg g_{m_{iii}}$. It is also important to keep the transistors in the differential pair saturated to reduce the noise from the current mirrors and the output stages.

The amplifier with the source follower stage as the level shifter also has matched devices. Its input referred noise is given by (5.6)

$$\overline{V}_N^2 = 2 \left(\overline{V}_i^2 + \left(\frac{g_{m_{iii}}}{g_{m_i}} \right)^2 \overline{V}_{iii}^2 + \overline{V}_1^2 + \left(\frac{1}{g_{m_l}(r_{01} \parallel r_{03})} \right)^2 \left(2\overline{V}_3^2 + \overline{V}_a^2 + \left(\frac{g_{m_b}}{g_{m_a}} \right)^2 \overline{V}_b^2 + \left(\frac{g_{m_6}}{g_{m_5}} \right)^2 \overline{V}_6^2 \right) \right) \quad (5.6)$$

The significant components to the input referred noise arise from the input stage, and from the differential pair. Hence their g_m should be increased, and the

differential pair should be biased so that it remains in saturation. Noise from the biasing transistors M_{iii} and M_{iv} are also dominant in the input referred noise, and can be reduced by making $g_{mi} \gg g_{miii}$.

5.5. Test and Measurement Results

5.5.1.1. Amplifier with PMOS differential pair and NMOS input stage

The amplifier was buffered with a source follower realized with a commercial IC during the testing process. The transfer function measurements were made for several low voltage supplies, and are plotted and tabulated below.

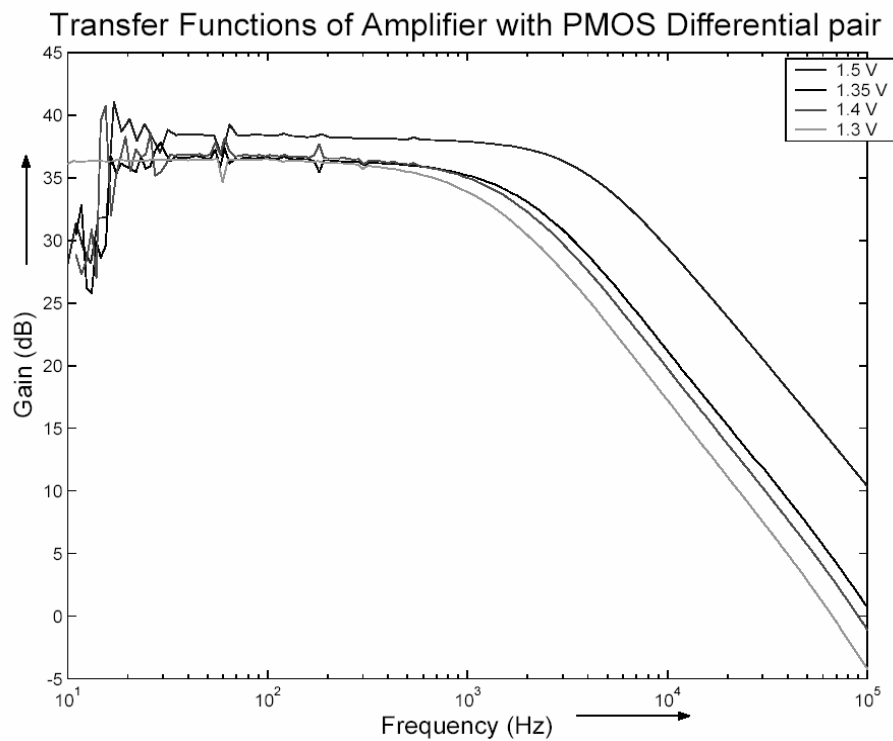


Fig. 5.4 Measured transfer functions of the amplifier with PMOS differential pair

Voltage Supply (V)	Power (μW)	Gain (dB)	Bandwidth (kHz)	Phase Margin	Input Referred Noise(μV)	NEF
1.5	48	38.23	3.94	50.77	22.74	81.74
1.4	35	36.49	1.80	50.14	26.55	124.81
1.35	24.7	36.27	1.622	50.68	25.09	106.3
1.3	18.7	36.54	1.14	51.86	22.74	101.94

Table 5.2 Characteristics of amplifier with PMOS differential pair

5.5.1.2. Discussion of the Measurement Results

The transfer function measurements were made for low voltage supplies ranging from 1.3V to 1.5V. Measured gain values ranging from 36.5 dB to 38.2 dB were obtained. These matched closely with the simulated results of 38.26 dB. Bandwidth of the amplifiers is limited by the loading of the pin capacitances of the DIP package. We would obtain a significant increase in the bandwidth by providing on chip loading and driving stages. Noise Efficiency Factors of these amplifiers are significantly higher than those of the previous amplifier configuration. This could be attributed to the presence of extra active devices, and also due to the degraded bandwidths. NEF could also be significantly improved by sizing the gain stages to have lower input referred noise voltages (5.5). The kink observed at low frequencies below 30 Hz is due to the resolution of the measuring instrumentation.

The output voltage of the amplifier was getting biased at V_{SS} during measurements. The reason for this behavior is as follows - The MOS diode connected devices have very low current when the drop across them is -0.2 to $-0.3V$; when it acts as a diode connected MOSFET, the current through it for very small voltage levels is very small. So a charge accumulated in the floating nodes could take a really long time to discharge. Hence in the low voltage design, where the most negative rail is only $0.75V$ below ground, the two diode connected MOSFETs and the NMOS at the output tend to reach an equilibrium state. In this state, the drain voltage of the NMOS goes down to $-0.75V$ and the resistors have a drop of about $-0.18V$ across each of them. So, an undesired common mode equilibrium state is reached by which the output stage of the amplifier is turned off. The node voltages and the entire circuit is shown in Fig. 5.5

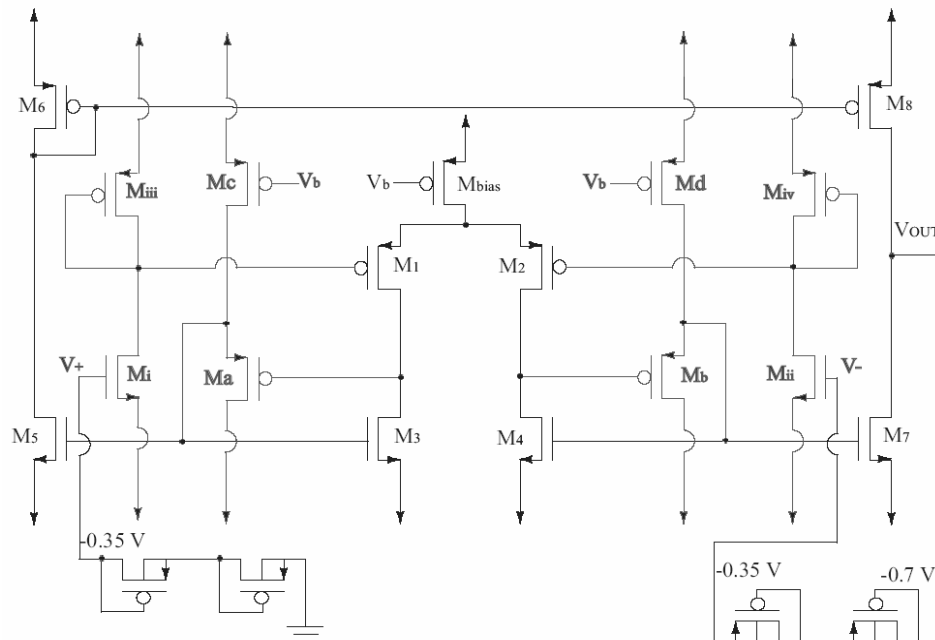


Fig. 5.5 Common mode equilibrium state with the output stage turned off

This problem does not exist at higher voltage supplies of about 2V. The equilibrium point can be avoided by using just one diode connected MOS resistor, or also by using a parallel connection of these devices in such a way as to have one of them as a diode connected MOS and the other as a diode connected BJT at all times. The schematic for this arrangement is shown in Fig. 5.6.

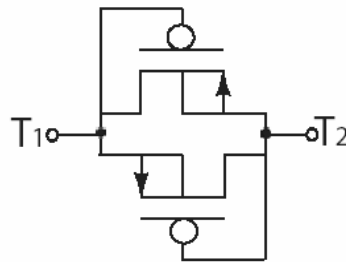


Fig. 5.6 Resistor arrangement to prevent common mode equilibrium state

This arrangement will have a low resistance even for voltage drops of 0.5V, and can leak out any accumulated charge with a small time constant. The drain voltage of the output NMOS would then increase and turn on the output stage. While making the measurement, we made the DC level at the output 0. This was done by tuning V_{ref} and accumulating charge at the positive node of the OTA till the output level swung to 0.

5.5.2.1. Amplifier with NMOS differential pair and PMOS input stage

This amplifier was buffered with a source follower stage, and tested at low voltage supplies. Measurement results are plotted in Fig. 5.7 and tabulated in Table 5.3

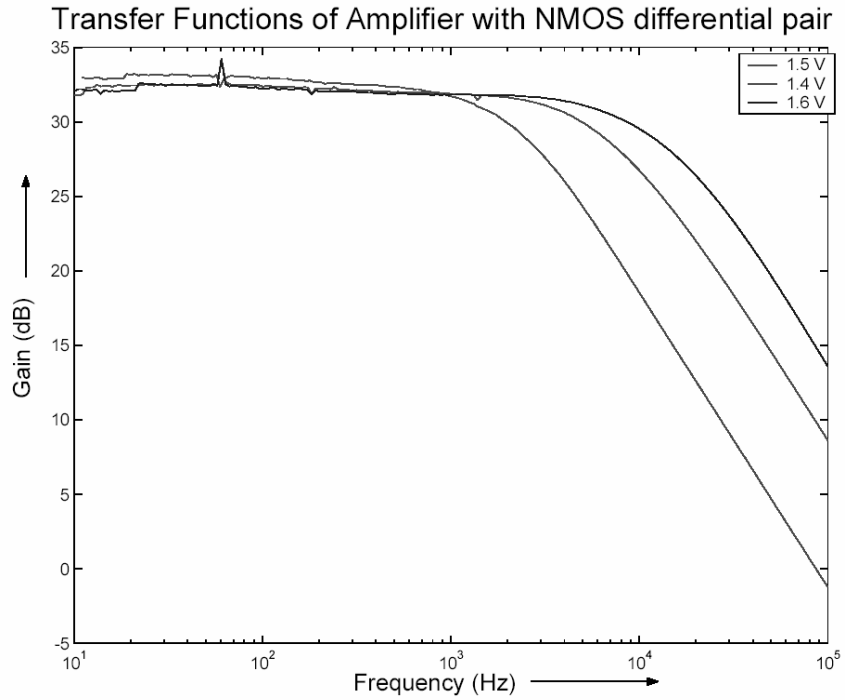


Fig. 5.7 Measured transfer functions of amplifier with NMOS differential pair

Voltage Supply(V)	Power (μW)	Gain (dB)	Bandwidth (kHz)	Phase Margin	Input Referred Noise (μV)	NEF
1.6	200	32.6	9.74	85	54.38	245.73
1.5	139.5	32.3	5.97	82	37.32	185.79
1.4	68.7	32.6	2.16	82	34.31	206.33

Table 5.3 Characteristics of amplifier with NMOS differential pair

5.5.2.2. Discussion of the Measurement Results

Output of this amplifier also tends to swing towards the negative supply voltage for low power supplies. We adjusted the value of the V_{ref} pin till the output swung to 0 mean before making the measurements. We could overcome this problem by using a single diode connected MOS or by using a parallel combination as discussed in 5.5.1.

Voltage gain using this configuration was only around 32 dB, though the amplifier has been designed for 40dB gain. The low g_m of the input stage PMOS transistors and the high threshold voltages of the PMOS devices reduce the loop gain of the entire structure. These amplifiers have a higher NEF than predicted due to the high current drain in the circuit, and a significantly higher input referred noise voltage. Input referred noise voltage can be reduced by sizing the transistors to have maximum gain in the initial stages. (5.5). Bandwidth of the amplifiers can also be increased by the use of on-chip loading and driving stages for these amplifiers.

5.5.3.1. Amplifier with Source Follower configuration

This amplifier was also tested with the source follower buffer stage. Transfer function measurements were made at low voltage supplies of 1.3 V to 1.6 V and are plotted in Fig. 5.8 and tabulated in Table 5.3

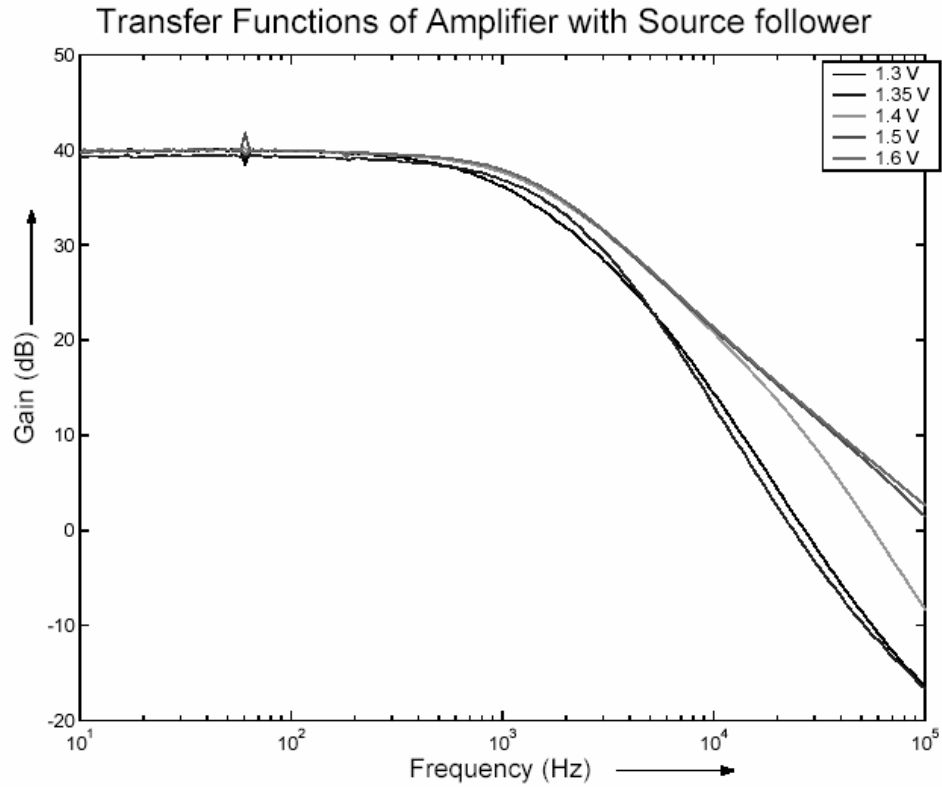


Fig. 5.8 Measured transfer functions of the amplifier with source follower and cascodes

Voltage Supply (V)	Power (μW)	Gain (dB)	Bandwidth (kHz)	Phase Margin	Input Referred Noise (μV)	NEF
1.6	80	39.9	1.3	82	23.94	187.27
1.5	61.5	39.8	1.28	65	18.3	130.64
1.4	44.8	39.8	1.23	43	18.78	120.82
1.35 V	37.8	39.4	1.13	44.7	23.06	144.79
1.3 V	29.3	39.8	0.85	43	17.9	116.16

Table 5.4 Characteristics of amplifier with source follower and cascodes

5.5.3.2. Discussion of Measurement Results

This amplifier configuration did not have the undesired common mode equilibrium state that the previous configurations had. This is because the gate voltages of the cascode transistors were controlled externally and that ensured a current through the output stage, and hence the equilibrium state is not reached.

Measured gains of 39.4 dB were obtained, and the amplifier shows encouraging results at low power supplies of 1.3V. The bandwidth of these amplifiers can be increased by adding on-chip loading and driving stages at the output. This would also reduce the NEF of the amplifier.

5.6. Conclusions

The low voltage techniques discussed in the previous chapter were applied to the bio-amplifier structure. Low voltage operation at 1.3V for gains of 40 dB was obtained from these amplifier configurations. At low voltage operations, the amplifiers with gain in the level shifting stage reach an undesired common mode equilibrium state which turns off the output stage. This equilibrium is not observed at higher voltage supply operation, and can be overcome by the use of a single diode connected MOS stage at the output, or by using a parallel combination of the diode connected resistors as discussed in 5.5.1.2.

The bandwidths of the amplifiers were degraded in the measurement as the loading provided by the DIP package and the measurement setup was significant. We could obtain an increase in the bandwidths and correspondingly a reduction in the NEF by incorporating on-chip driving and loading stages. The

limiting factor in the reduction of the voltage supply is the high threshold voltages of the transistors (0.75V for NMOS, 0.93V for PMOS), and could be pushed down with the use of a process with lower threshold voltages.

These amplifiers have provided positive results at low voltage and low power operations. Integration of Cell Clinics with these amplifiers can be considered.

Chapter 6

Wireless Transmission System

6.1. Introduction

The second part of the sensing system consists of a wireless transmission system that is capable of transmitting the data from the bio-amplifiers. In this chapter, we describe the design of an integrated wireless transmitting system that is capable of transmitting data over short ranges. We choose a digital scheme of communication called the Amplitude Shift Keying (ASK) technique. In this scheme, the binary values (one and zero) are represented by two different amplitudes of a carrier frequency, normally on and off, as shown in Fig 6.1.

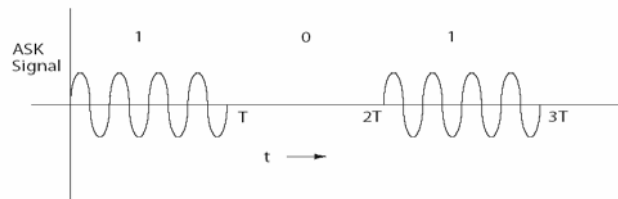


Fig. 6.1 ASK modulation scheme (1 => sine wave, 0 => no signal)

The advantage of the ASK scheme is that there is no power loss when the transmitted signal is 0. It is particularly ideal for short range communication because degradation of the transmitted signal due to noise is not very significant over short ranges, and the design is simpler. For long range communications, ASK is not suitable as noise corruption becomes significant and schemes like FSK (Frequency Shift Keying) and PSK (Phase Shift Keying) become more reliable.

The ASK transmitter comprises a Voltage Controlled Oscillator (VCO) which generates the carrier signal at 940 MHz (in accordance with the FCC rules), a switch which performs the ASK modulation of the carrier signal, a preamplifier to drive the power amplifier, and a power amplifier to boost the signal strength before delivering it to the antenna. The overall block diagram is shown in Fig. 6.2. These blocks are discussed in more detail in this chapter.

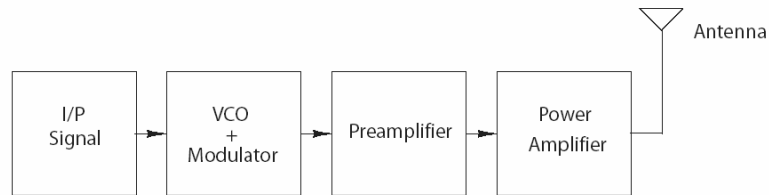


Fig. 6.2 Block diagram of the ASK transmitter

6.2. Voltage Controlled Oscillator (VCO)

The VCO is a current starved three stage ring oscillator [36], as shown in Fig. 6.3. This design is simple to realize and also has a wide frequency tuning range.

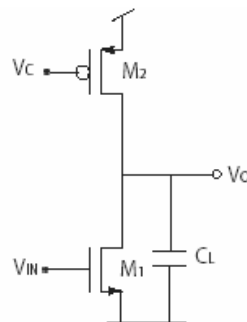


Fig. 6.3 Single stage of the VCO

The ring oscillator couldn't be implemented using a series of inverters as the carrier frequency is 940 MHz, and the rise time of the inverters has to be very

low in order to match that speed. The VCO described here is realized using a three stage ring oscillator with its time period being controlled by the time delay of each of the source follower stages. The time delay in the propagation (τ) from one stage to another is decided by the output resistance of the PMOS current source which is biased in the linear region, and the input capacitance of the following stage.

$$\tau = 2\pi R_{ON2} C \quad (6.1)$$

where R_{ON2} is the output resistance of the PMOS current source, and C is the loading of the subsequent stage. Substituting the value of R_{ON2} , the time delay (τ) can further be written as shown in 6.2 [38].

$$\tau = \frac{2\pi C}{\mu_p C_{ox} \left(\frac{W}{L}\right)_2 (V_{DD} - V_C - V_{ip})} \quad (6.2)$$

where μ_p is the mobility of holes, C_{ox} is the gate capacitance per unit length, W/L is the aspect ratio of M_2 , V_{DD} is the power supply voltage, V_C is the control voltage, and V_{ip} is the threshold voltage of M_2 . The frequency of oscillation (f) for the three stage oscillator is therefore given by

$$f = \frac{1}{6 * \tau} \quad (6.3)$$

Since the time delay is inversely proportional to the control voltage, we observe a direct relationship between the control voltage and the frequency of oscillation.

The VCO is followed by the ASK modulator, a switch which could either be on or off depending on the signal being transmitted. To remove its interference

(loading effect depending on the state) with the frequency of oscillation of the VCO, we provide a buffer stage between them. The schematic of the VCO, the buffer and the switch are shown in Fig. 6.4, and the sizes of all the transistors are tabulated in Table 6.1

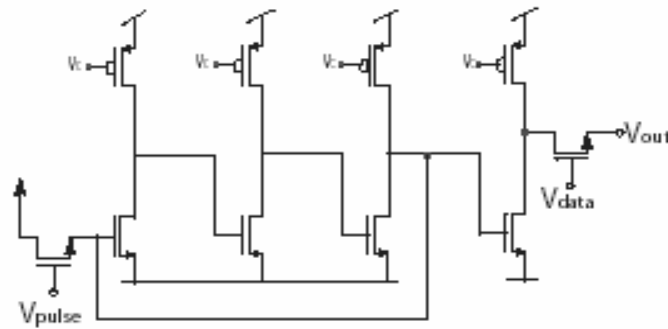


Fig. 6.4 VCO and the ASK modulator

6.3. Pre-amplifier

The pre-amplifier is used to drive the power amplifier. It is realized using transistors biased in the common source configuration, with increasing sizes of the transistors increasing from the VCO to the power amplifier. It also serves as an additional isolation stage between the VCO and the power amplifier. The schematic is shown in Fig. 6.5

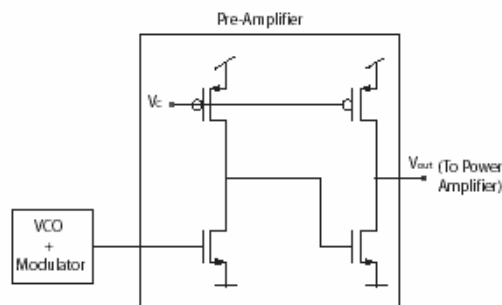


Fig. 6.5 VCO and the Pre-amplifier

6.4. Power Amplifier (PA)

The power amplifier (PA) is the last stage of the transmitter and drives the antenna. It is the block that consumes the maximum power in the transmitter. The important factors in the design of a PA are the maintenance of linearity, the power gain, and the efficiency. Power amplifiers can be broadly classified into two categories, *linear* and *constant envelope* operation. Linear amplifiers produce a replica of the input and are suitable for amplitude modulated signals, while constant envelope amplifiers do not contain any information in the amplitude and are more suitable for frequency and phase modulated signals. The most commonly used schemes of the PA are class A through F, with the first three being linear amplifiers, and the latter three being constant envelope amplifiers.

6.4.1. Choice of scheme for Power Amplifier

The PA [26, 36] essentially consists of a MOSFET which acts as a switch, and drives the load based on the input signal. The schematic of a generalized PA is shown in Fig. 6.6.

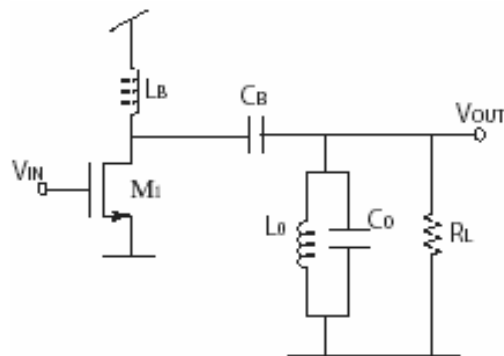


Fig. 6.6 Schematic of a general Power Amplifier

Inductance L_B , a big inductance, maintains the current through that path a constant, capacitance C_B blocks the DC level from entering the antenna, and L_0 and C_0 tuned at the carrier frequency increase the Q of the output circuit. The input signal to the PA is a large signal drives the MOSFET M_1 . Since the current through the inductance is constant, it either flows through the PA or through the output circuit depending on the state of M_1 . Power driven to the output can be increased by using a larger input signal that switches the MOSFET ‘on’ and ‘off’, and increasing the width of M_1 to reduce output resistance in the ‘on’ state.

Efficiency of a PA is defined as the ratio of the power delivered to the load to the power drawn from the supply. The theoretically possible maximum efficiencies of the different classes of PA are tabulated by Thomas Lee [26] in Table 6.1. We observe that the efficiency is higher for constant envelope amplifiers as compared to the linear amplifiers. For the ASK digital communication scheme, we chose a constant envelope amplifier. Another key parameter in the design of power amplifiers is the normalized power handling capability which is defined as the ratio of the actual power output to the product of the maximum device voltage and current. This is particularly important in the design of power amplifiers because the operation of the constant envelope amplifier relies on the switching property of the MOSFET which results in huge changes in voltage and current levels at the drain.

Class A through C are linear amplifiers, and do not give a high efficiency. [26] So we did not choose an amplifier from them. Class D, E and F are constant envelope amplifiers, and are more efficient in power. Class E amplifiers have a

poor power handling capability (0.098) as compared to class D amplifiers (0.32) and class F amplifiers (0.16). Class D amplifiers involve the design of mutually coupled inductors on chip, and on-chip inductors generally do not possess a high Q. Hence we chose a class F power amplifier for our scheme.

The schematic of a class F Power Amplifier is shown in Fig. 6.7. Its principle of operation is described in detail by Thomas Lee [26] and is outlined in Appendix A.

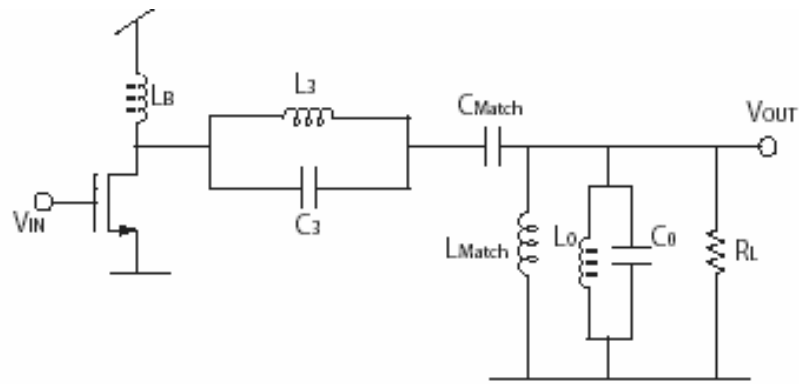


Fig. 6.7 Schematic of the class F Power Amplifier

6.4.2. Choice of Passive elements and transistor dimensions.

The purpose of the inductance L_B is to maintain a constant current through it, and hence it is desirable to choose a large inductor. If the inductance size is increased too much, then it would become difficult to integrate it owing to its size, and the possibility of the self resonant frequency being lower than the carrier frequency [41]. We chose a value of 10nH for L_B and it provides an impedance of 60Ω at the carrier frequency. To keep the drain current a constant within 10%, the input impedance from the passive circuits seen at the drain at the fundamental frequency should be less than 6Ω . We chose L_{match} and C_{match} to transform the antenna's 50Ω impedance to 4Ω at the carrier frequency.

If the drain of the PA were to swing from 0 to V_{DD} , then the power delivered to the power would be about 4.4W, which is very high for our application. Hence we chose a current limited design where the current supplied to the output would not swing from 0 to $8V_{DD}/\pi Z_{in}$. The current delivered to the load would swing only from 0 to the DC bias current of M_1 . We aimed at a power level of 2.5mW to be delivered to the output and the transistor M_1 was sized to provide a DC current level of 70mA. Minimum length was chosen for M_1 .

The values of L_3 and C_3 are chosen to resonate at the third harmonic of the carrier frequency ($3\omega_0$). To increase the Q factor, a small value of 0.5nH has been chosen for L_3 . Values below 0.5nH cannot be realized accurately on chip as a spiral inductor. The values of L_0 and C_0 have been chosen to provide a Q factor of 10 at the output.

6.4.3. Improvement of performance of the PA for ASK scheme

The gate of the switch M_1 should be ideally at ground level when the transmitted signal is 0. But there exists a possibility that the gate is not at ground level at this stage, and the power amplifier continues to dissipate power while not transmitting anything. To prevent this condition, a controlled MOSFET resistor is added at the input of the preamplifier as shown in Fig. 6.8. When the transmitted signal is 1, the MOSFET is in the ON state, and brings down the gate voltage of M_1 . When the transmitted signal is 0, the MOSFET is in the OFF state.

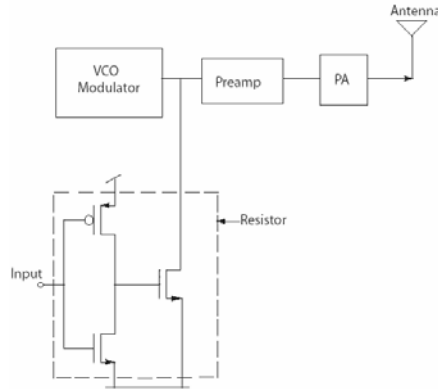


Fig. 6.8 Resistor to reduce power dissipation during ‘0’ transmission

At the ‘off’ state, the node at the junction of the modulator and the preamplifier is a floating node. Hence to remove the charge of that node, a relatively small MOS resistor would suffice. On the other hand, the node at the junction of the pre-amplifier and the power amplifier is an active node and is connected to the drains of the two MOSFETS of the pre-amplifier. If the resistor were placed at this node, then it should be realized by a MOSFET with a very high driving capability as the PMOS in the pre-amplifier is sized big and has a high driving capability.

6.4.4. Realization of On-Chip Inductors

The inductors in the transmitter circuit were realized as on-chip spiral inductors as shown in Fig. 6.9.

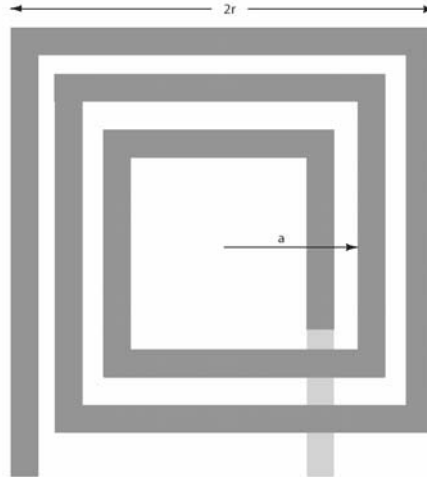


Fig. 6.9 Spiral Inductor

We used the top two metal layers available in our process and connected them using multiple contacts to reduce the parasitic resistance. The inductance of a planar spiral inductor can be obtained from [26], and is given by (6.4)

$$L = \frac{37.5\mu_0 n^2 a^2}{22r - 14a} \quad (6.4)$$

A more accurate modeling of the inductor and all its coupling effects is done in [9]. On-chip inductors do not have a high Q due to the various parasitic losses associated with it, and can be modeled as shown in Fig. 6.10. [41].

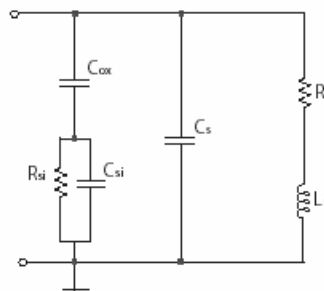


Fig. 6.10 Inductor's lumped model

where L_S is the spiral inductance, R_S is the series resistance, C_S is the overlap capacitance due to the overlap of the spiral with the underpass, C_{OX} is the

oxide capacitance between the spiral and the substrate, R_{Si} is the silicon substrate resistance and C_{Si} is the substrate capacitance. The capacitances in the equivalent lumped circuit give rise to a phenomenon called self resonance by which the inductance behaves like a capacitor after a certain frequency. The combined effect of the substrate loss terms and the self resonance give rise to a reduction in the Q at high frequencies. It has been shown in [41] that the Q factor can be improved by using a patterned ground shield under the inductance that removes the coupling of the inductance with the substrate, and also removes any currents that could be introduced by Lenz's law. This can be realized using a poly layer that is grounded to prevent coupling with substrate, and be etched and made discontinuous to prevent any eddy currents on it. We used a patterned ground shield, as shown in Fig. 6.11. The finger-like structures which point towards the center is the patterned ground shield realized with the poly layer available in the process.

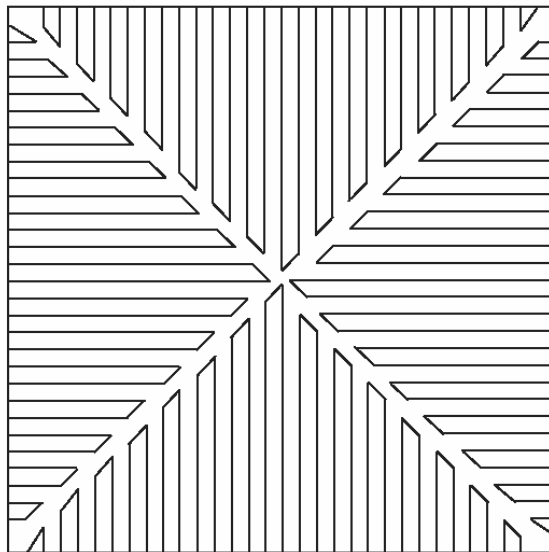


Fig. 6.11 Patterned Ground Shield to reduce substrate coupling [41]

Planar inductors of various geometries, sizes and no of sides have been characterized by [24]. We chose our inductance geometries from here, and also verified with the expression given by 6.5. We also placed a few inductors on our chip for testing purposes.

6.5. Layouts

The circuit has been designed for a 0.5 μm standard scalable CMOS process. The values, dimensions and the area consumption of the different elements are listed in this section.

Block	Transistor	Width	Length
VCO	M ₁ (NMOS)	105 μm	0.7 μm
	M ₂ (PMOS)	262.5 μm	0.7 μm
Buffer	M ₁ (NMOS)	210 μm	0.7 μm
	M ₂ (PMOS)	105 μm	0.7 μm
Modulator	NMOS	105 μm	0.7 μm
Preamplifier	M ₁ (NMOS)	210 μm	0.7 μm
	M ₂ (PMOS)	525 μm	0.7 μm
MOS resistor	M ₁ (NMOS)	2.8 μm	0.7 μm
	M _a (NMOS)	1.4 μm	0.7 μm
	M _b (PMOS)	2.8 μm	0.7 μm
PA	M ₁	1050 μm	0.7 μm

Table 6.1 Sizes of active devices on chip

Capacitor	Value	Area
C_{match}	6.72pF	8,994 μm^2
C_B	12.84pF	19,381 μm^2
C_0	34.78pF	46,801 μm^2

Table 6.2 On-chip capacitors realized with 2 poly layers

All the inductors are realized as On Chip Spiral planar inductors with the top two layers of metal strapped together to reduce the parasitic resistance.

Inductor	Value (nH)	Outer length	Inner length	No of turns	Thickness	Area on Chip (μm^2)
L_3	0.5	79.8 μm	20.3 μm	$2^{3/4}$	7.35 μm	13745
$L_{\text{match}} \parallel L_0$	0.65	91.7 μm	30.1 μm	$2^{3/4}$	7.7 μm	18437
L_B	10	381.5 μm	182 μm	5	15.75 μm	192627

Table 6.3 Characteristics of the different inductors in the Power Amplifier

The transmitter was fabricated in a commercially available 0.5 μm process. The photograph of the transmitter is shown in Fig. 6.12. We also placed a few test structures on the chip. The layouts are made in order to probe the test structure with an air-coplanar ground-signal-ground probe. The test and measurement results are presented in the next chapter.

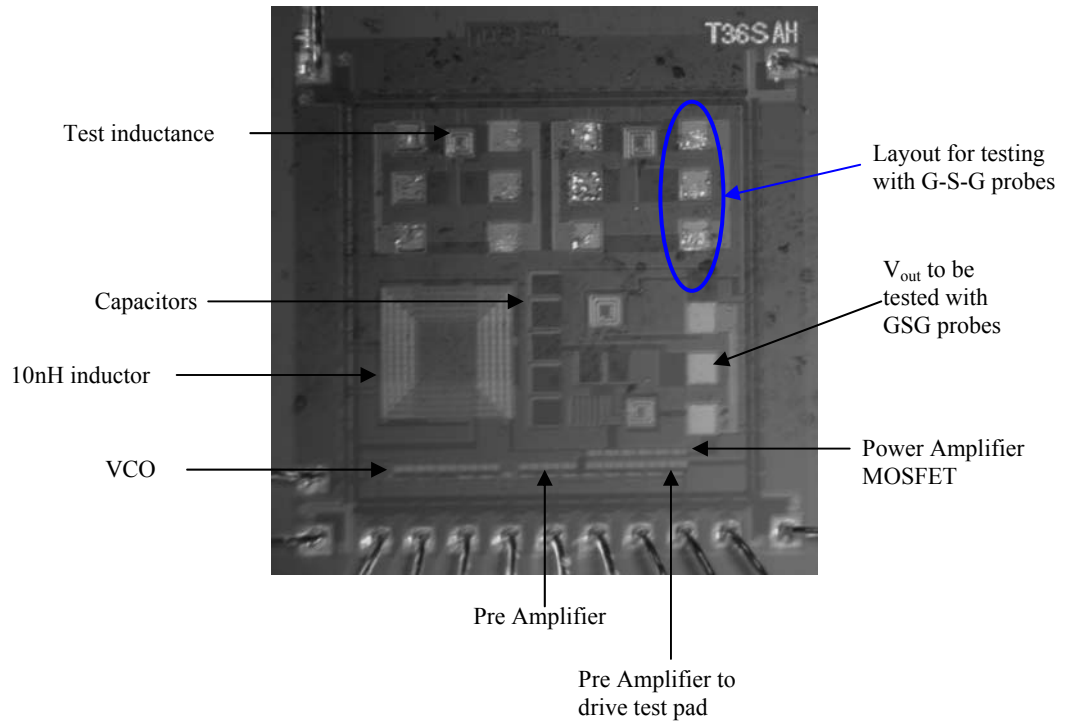


Fig. 6.12 Photograph of the ASK transmitter

Chapter 7

RF Test and Measurement

The ASK transmitter system is designed to operate at 940 MHz. The impedance transformation elements and the output tank circuit are chosen to operate at this frequency. We placed a VCO and a few inductors on the chip to be tested independently. In this chapter, we'll discuss the measurement results from the test structures, and that of the entire transmitter.

7.1. Inductance

The inductances have to be tested using an S-Parameter analysis at high frequencies. They cannot be measured using the standard Z or the Y parameters as it is difficult to provide a good short circuit or open circuit over a very broad frequency range. Reflections also play an important role in high frequency testing, thus reducing the accuracy of Z and Y parameter analysis. The inductances are measured from the S-parameters (scattering parameters) measurements. From the S-parameters, the Z-parameters can be obtained from a simple transformation.

We used the HP8568A Network analyzer, and a high frequency probe (cascade microtech air coplanar Ground-Signal-Ground probe) to perform the S-parameter analysis. To enable low loss high frequency testing, the probe has three tips: two of which connect to ground, and the center one to the signal (G-S-G) configuration. We designed our inductances based on the calculations in the previous chapter, and they were realized as on-chip spiral inductors. The test

structures were placed as shown in Fig. 7.1 in order to be tested using the cascade probes.

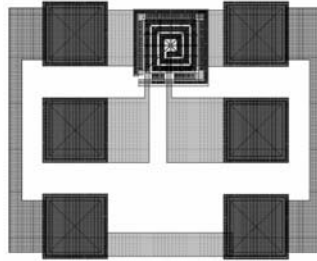
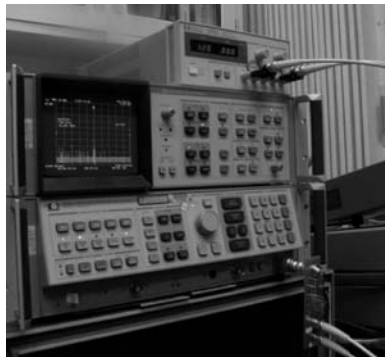


Fig. 7.1 Test inductance layout

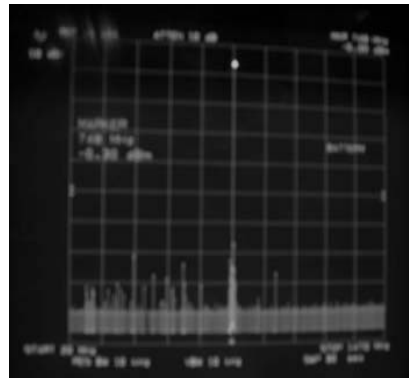
The layouts were designed for inductance values of 0.65nH and 0.50nH, and measured values were 0.8nH and 0.8nH respectively.

7.2. VCO

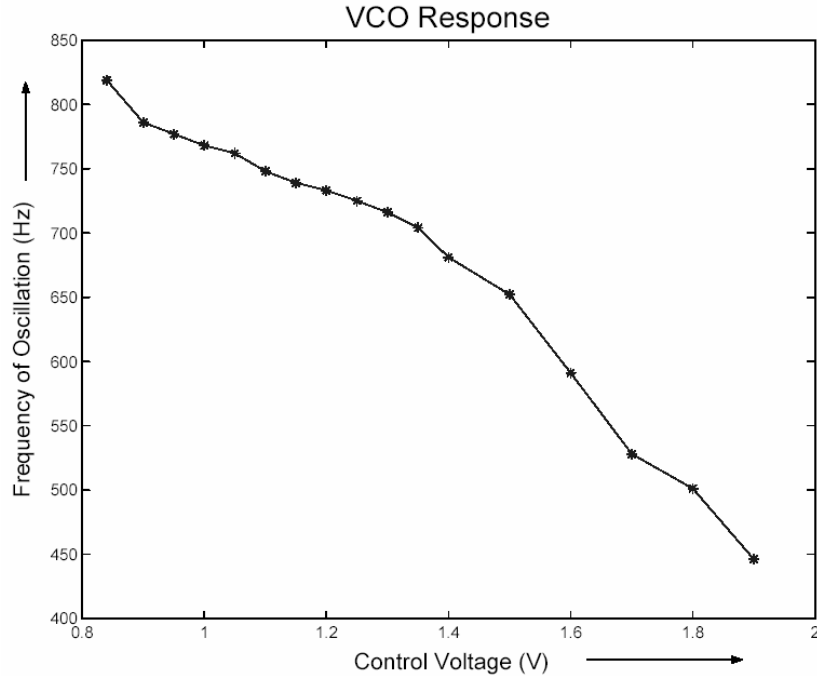
We placed a ring oscillator on the chip for testing purpose. The output of the ring oscillator was connected to a pin of the standard DIP package. We tested its performance using a spectrum analyzer (HP8568A) to find out the various tunable frequencies. The test fixture to reduce capacitive loading and the results of our measurement are shown in Fig. 7.2.



**(a) VCO at the input of
Spectrum Analyzer**



**(b) Output of VCO in the
Spectrum Analyzer**



(c) Variation of frequency with control voltage

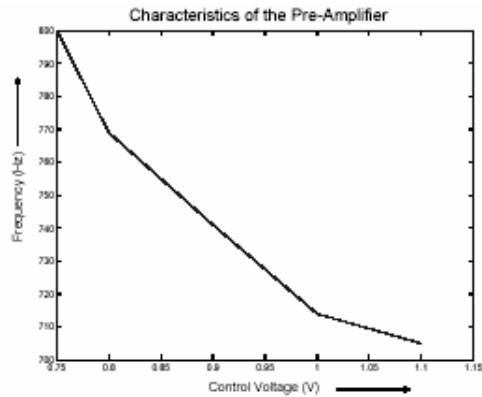
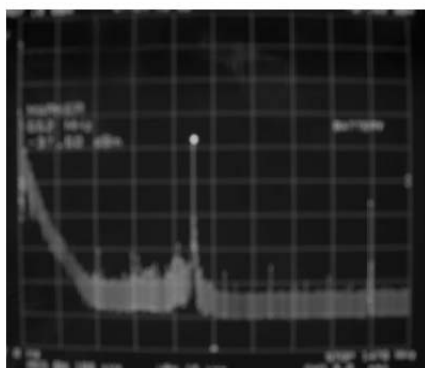
Fig. 7.2 Measurement results of the VCO (a) Test Fixture for VCO testing (b) Output of VCO for a control voltage, (c) Tunable range of the VCO

The frequency of oscillation of the VCO showed a wide tunable range from 450 MHz to 820 MHz. It did not oscillate at the designed 940 MHz because of the loading by the test stage, and also the loading due to the large sized devices. The output of the VCO had a swing magnitude of 2V in simulation, but has a lower magnitude during measurements. This is again due to the inability of the current starved common source stage at the output to drive the 50Ω input impedance of the test setup from rail to rail at high frequencies.

Future improvements in this design of the VCO would be to reduce the sizes of the transistors, and also to include an output matching stage for the 50Ω measurement setup.

7.3. Pre-Amplifier

The preamplifier that we used is very similar to the VCO in design, but bigger in size. To test its performance, we placed a preamplifier with input as VCO and its output connected to a DIP package. The variations in the frequency with control frequency were measured, and the results are as shown in Fig. 7.3. This output again drives a 50Ω , and hence does not swing from rail to rail.



(a) Output of Pre-amplifier (b) Frequency response of the Pre-amplifier

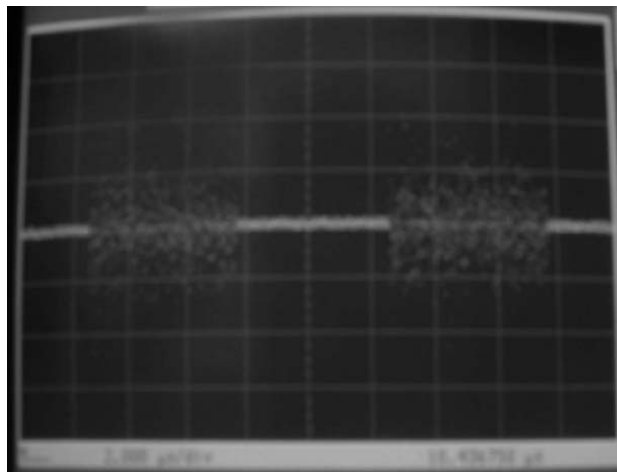
Fig. 7.3 Measured output of the Pre-amplifier

7.4. Transmitter

The output of the power amplifier is connected to a pin in the standard DIP package. We made a test structure similar to that as in Fig. 7.2a, and the entire transmitter was tested using the HP 83480A oscilloscope, and the HP 8568A spectrum analyzer. The input to the transmitter was given as a square wave from a signal generator. The output of the transmitter is measured across the oscilloscope in its 50Ω configuration. The measured results are plotted in Fig. 7.4



(a) Output of transmitter on Spectrum analyzer



(b) Output of transmitter on the oscilloscope for an input sequence of 01010

Fig. 7.4 Measured output response of the transmitter

The transmitter's output for an input sequence of 01010 is shown in Fig. 7.3(b). It shows the ASK modulated waveform of the input sequence. A square wave of 1MHz frequency was used as the input signal, and the output waveform had the same envelope frequency. The exact frequency of the carrier signal could not be accurately measured with our setup; the reason being that the measuring instrument required an input trigger signal of greater than 100mV amplitude, and our output amplitude was lower than that.

The power content of the output waveform when transmitting a '1' is -36 dBm, though it was designed for an output power of -0.4 dBm. This is because of the inability of the VCO to oscillate at a frequency of 940MHz, the frequency for which all the passive elements of the power amplifier have been designed. Hence the output of the VCO is significantly attenuated at the output. Simulations show an attenuation factor of about 200 from the output of the VCO to the output of the PA at a frequency of oscillation of 820 MHz of the VCO.

An improvement in the performance of the transmitter can be obtained by altering the design of the VCO to oscillate at higher frequencies.

7.5. Conclusions

The RF transmitter designed for the ASK modulation scheme has been tested. Test structures were also placed on the chip, and they were also tested. The test inductors were measured using S-parameter analysis, and the measurement results tally with the values that the layouts were made for. A test VCO structure was placed on the chip, and has been characterized using a Spectrum Analyzer. It showed a wide tunable frequency range from 450 MHz to 820MHz. It did not oscillate at the 940 MHz frequency that it was designed for.

The pre-amplifier also showed a peak in the frequency of oscillation of the VCO. The entire transmitter was tested for a switching waveform, and the ASK modulated waveform has been observed. The output power level is -36 dBm, and it shows a significant reduction from the designed values. This is due to the reduced frequency of oscillation of the VCO.

Improvements in the performance can be obtained by designing the VCO to reach higher frequencies.

Chapter 8

Conclusions

In this work, I present the design and measurement results of low power low voltage amplifiers and a transmitter that can be used for sensing the activity of single cells. This document starts with a brief introduction, and a literature review of the previous work that has been done in this field. We then discuss the design, and present test and measurement results of different amplifier configurations and a transmitter.

8.1. Amplifiers

We designed amplifiers for suitable gains of 40dB that can be used to detect extra-cellular activity of single cells. The measured gains of these amplifiers were 40 dB, and the bandwidths were limited by the loading capacitances of the package and the test setup. Future improvements in this design can be obtained by providing on-chip loading stages for these amplifiers.

We also investigated low voltage low power techniques that can be applied to our amplifier design. Transconductance amplifiers and filters capable of operating at 1V were designed, and tested. Measurements show that transconductance based structures can be operated at low voltage levels of 1V.

Based on the principles of low voltage low power techniques, we designed a few amplifier configurations that are capable of working at 1.5V. Measurement shows that these amplifiers are capable of providing gains of 40dB at low voltage.

supply levels of 1.3V. One of the configurations does not provide the designed gain of 40dB, and this is due to its low open loop gain. The bandwidth of all the configurations can be improved by providing on-chip driving stages at the output.

8.2. Wireless Transmission System

A wireless transmission system using the Amplitude Shift Keying (ASK) technique has been designed. The carrier frequency is chosen at 940 MHz. We also included inductance and VCO test structures on the chip for verification purposes. The inductances were measured using the s-parameter analysis and we obtained values close to the designed values. The VCO provided a wide tunable frequency range from 450 MHz to 820MHz. Its output was observed on a 50Ω oscilloscope, and hence the output did not swing from rail to rail.

The final output of the transmitter was measured using a spectrum analyzer and a oscilloscope. The ASK waveform was observed on the oscilloscope. The amplitude of the output was attenuated considerably due to the presence of matched elements in the PA tuned to 940MHz.

8.3. Future Work

The bio-amplifier discussed in Chapter 3 is suitable for integration with the Cell Clinics. Its bandwidth can be increased by providing on-chip output driving stages. Some of the amplifier configurations presented in Chapter 5 are also suitable for integration with Cell Clinics, while some of the configurations need some modifications in the sizing of the transistors used. The gain in the

amplification stages has to be designed in order to reduce the input referred noise of the circuit. The diode connected MOS element should be redesigned for compatibility with the low voltage designs.

The test structures should be matched to drive the $50\ \Omega$ measurement setup. We also plan to modify the design of the VCO, and the pre-Amplifier to operate at higher frequencies.

Appendix A

Class F Power Amplifier

The schematic and the principle of operation of a class F power amplifier is described in detail by Thomas Lee [26], and is briefly outlined here. The general schematic of a class F PA is shown in Fig. A1

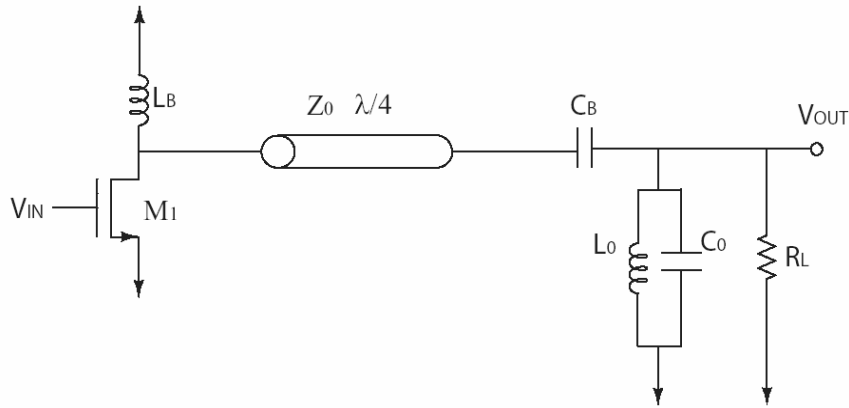


Fig. A1 Schematic of a class F Power Amplifier

A.1. Principle of Operation of a Class F Power Amplifier

The schematic of a class F PA [26] is shown in Fig.A1. It consists of a switch M_1 , a big inductance L_B to keep the current through it a constant, a quarter wavelength ($\lambda/4$) long transmission line, a blocking capacitance C_B which reduces DC dissipation in the load, and an LC tank circuit at the output comprised of L_0 and C_0 to increase the Q of the output circuit, and the antenna modeled as a resistance R_L . The LC tank at the output stage has very high Q, and its impedance is zero for out of band signals.

The input impedance of a transmission line is given by (A.1) [4]

$$Z_{in} = \left(\frac{Z_L \cos \beta d + jZ_0 \sin \beta d}{Z_0 \cos \beta d + jZ_L \sin \beta d} \right) Z_0 \quad (\text{A.1})$$

where Z_0 is the characteristic impedance of the line, Z_L is the load impedance, β is given as $\beta = 2\pi/\lambda$, and d is the length of the line. For a transmission line of length $\lambda/4$ the input impedance is given by (A.2)

$$Z_{in} = \frac{Z_0^2}{Z_L} \quad (\text{A.2})$$

At the fundamental frequency, the input impedance is an inverted version of the impedance at the output. By increasing the Q of the tank circuit, the input impedance of the transmission line can be made to approach zero at all frequencies outside the narrow band of interest. At twice the fundamental frequency, the transmission line behaves like a $\lambda/2$ line, and the input impedance is given by $Z_{in} = Z_L$. Since Z_L is zero at twice the fundamental frequency, the input impedance is zero. Thus there cannot be a voltage waveform having the twice fundamental frequency at the drain. At the third harmonic, the transmission line behaves like a $\lambda/4$ line again, and the input impedance is ∞ due to the zero impedance of the tank circuit at $3\omega_0$. Thus, the input impedance of the transmission line is finite at the fundamental frequency, zero at all even harmonics, and is infinite at all the odd harmonics [4].

Due to the nature of the input impedance waveform, the drain voltage can only have the odd harmonics and it ideally results in a square wave with 50% duty cycle. The current through the transmission line can have only the fundamental component. The voltage and current waveforms at the drain are shown in Fig. 6.8.

The high Q tank at the output ensures that the current through the load is sinusoidal.

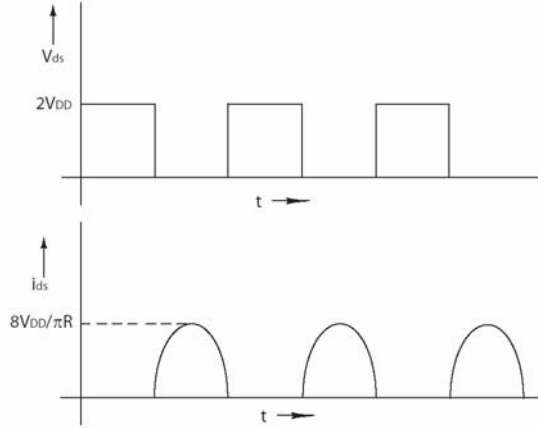


Fig. A.2 Voltage and current waveforms of an ideal class F PA

The non-overlapping nature of the drain voltage and current waveforms ensure that the switch does not dissipate any power theoretically resulting in 100% efficiency. The drain voltage swings from 0 to $2V_{DD}$. Its fundamental harmonic component has amplitude of $8V_{DD}/\pi$ and the drain current varies from 0 to $8V_{DD}/\pi Z_{in}$. The power delivered to the load is

$$P_0 = \frac{\left(4V_{DD}/\pi\right)^2}{Z_{in}} \quad (\text{A.3})$$

The maximum drain voltage is $2V_{DD}$ and the maximum drain current is $8V_{DD}/\pi Z_{in}$. Hence the power handling capability is given by

$$\frac{P_0}{v_{DS,peak} * i_{DS,peak}} = \frac{\frac{\left(4V_{DD}/\pi\right)^2}{Z_{in}}}{2V_{DD} \left(8V_{DD}/\pi Z_{in}\right)} = \frac{1}{2\pi} \quad (\text{A.4})$$

A.2. Realization of a Class F Power Amplifier

In practice, the $\lambda/4$ can be long and may not be integrated on a single chip. As described by Lee [26], the transmission line can be realized using lumped elements as shown in Fig. A.3. L_{match} and C_{match} are chosen such that they perform the impedance transformation at the fundamental frequency to realize the desired output power level. C_{match} also performs the role of the blocking capacitor. L_3 and C_3 are tuned to the third harmonic and have a high Q to implement the ∞ input impedance at $3\omega_0$. Thus the input impedance at the drain at the fundamental frequency is implemented with the matching circuit, is zero at the second and other even harmonics, and is ∞ at the third harmonic.

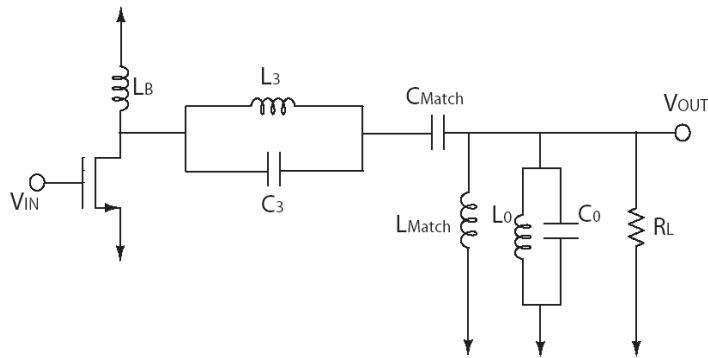


Fig. A.3 Realization of the class F Power Amplifier

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