ABSTRACT

Title of Document: NANOFABRICATION ON ENGINEERED SILICON (100) SURFACES USING SCANNING PROBE MICROSCOPY

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Fabricating and measuring sub-5 nanometer features brings to light several pressing issues in future semiconductor industry manufacturing and dimensional metrology. This dissertation presents a feasible process to create nanostructures using scanning probes with applications in dimensional metrology and nanomanufacturing processes. Using the lattice spacing of a crystal as the fundamental "ruler" or scale, sub 5 nm critical dimension reference standards can be created with atomic scale dimensional control.

This technique relies on atomically sharp tips to provide robust imaging and patterning (nanolithography) capabilities. We have developed a comprehensive process to routinely produce high quality scanning tunneling microscope (STM) tips. The quality of STM tips are a critical factor in achieving reproducible patterning. A modified electrochemical etching method has been used to create sharp tips with

preferred apex geometry. By using a field ion microscope (FIM), tip surfaces have been cleaned by field evaporation. Finally, a thermal ultra-high-vacuum (UHV) process is implemented to stabilize the atoms on the tip apex for improved performance. The process is also found to be capable of restructuring the apex to regain atomic resolution when tips fail during imaging or patterning.

Silicon (100) samples with pre-patterned micrometer-size fiducial marks are used as templates in this technique. The fiducial marks are used as 2D references to relocate the tip scanned area and the lithographic patterns. Large atomically-flat reconstructed (100) surfaces are obtained after a wet chemical cleaning process and a high temperature annealing process. After the high temperature annealing process, we observed reproducible step-terrace patterns formed on surfaces due to the fiducial marks. A kinetic Monte-Carlo simulation was used to study quantitatively the evolution of surface morphology under the influence of fiducial marks. Some of the key aspects, such as the electromigration effect and step permeability have been extensively studied.

Hydrogen-passivated silicon (100) reconstructed surfaces are used to create nanopatterns by selective depassivation lithography. Optimized depassivation procedures enable us to fabricate patterns from the microscale to the atomic scale consistently using an UHV STM. To preserve and later enhance the nanopatterns, SiO_2 hard etch mask marks are formed by oxidizing the patterns using ambient humidity or gaseous oxygen. A reactive ion etching (RIE) process is used to further enhance the aspect ratio of oxidized nanopatterns so that they can be served as 3D nanostructures on silicon surfaces.

NANOFABRICATION ON ENGINEERED SILICON (100) SURFACES USING SCANNING PROBE MICROSCOPY

By

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Dedication

To my parents, Jie Li and Ningjiang Jiao

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Chapter 1: Overview

1.1 Introduction

1.1.1 Development of Semiconductor Industry

During its short history, the semiconductor industry has gone through extraordinarily rapid development. The semiconductor industry can be traced back to 1904, the time when John Ambrose Fleming invented the diode. At that time, vacuum tubes were used to detect radio signals. Later on, these electronic devices drove the expansion of radio broadcasting, television, radar, telephone networks, analog and digital computers, and industrial process control. In 1947, William Shockley, John Bardeen, and Walter Brattain at Bell Labs created the first transistor, which boosted the development of semiconductor industry and soon became the key component in all modern electronics.

A transistor is a semiconductor device used to amplify and switch electronic signals. As one of the greatest inventions in 20th century, a transistor is the fundamental building block of modern electronic devices. The first transistor was made of germanium, but due to the germanium's impurity problem and its sensitivity to temperature, scientists started to use silicon to fabricate transistors. The first silicon transistor was produced by Texas Instruments in 1954.[1] In 1960, the first metal-oxide-semiconductor field-effect transistor (MOSFET) transistor was built by Kahng and Atalla at Bell Labs.[2] Compared with

vacuum tubes, transistors last much longer, consume less power, are smaller, more efficient, more reliable, and much cheaper.

For many years, transistors were made as individual electronic components and were connected to other electronic components (resistors, capacitors, inductors, diodes, etc.) on boards to make an electronic circuit. However, it did not take long before the limits of this circuit construction technique were reached. Circuits based on individual transistors became too large and too difficult to assemble. There were simply too many electronic components to deal with. To make the circuits cost less and provide better performance, one needed to pack the transistors closer and closer together.

In 1958 and 1959, Jack Kilby[3] at Texas Instruments and Robert Noyce[4] at Fairchild Camera, came up with a solution to the problem of large numbers of components, and the integrated circuit (IC) was developed. Instead of making transistors one-by-one, several transistors could be made at the same time, on the same piece of semiconductor. Not only transistors, but other electric components such as resistors, capacitors and diodes could be made by the same process with the same materials.

The integration of large numbers of tiny transistors into a small chip was an enormous improvement over the manual assembly of circuits using electronic components. The integrated circuit's mass production capability, reliability, and building-block approach to circuit design ensured the rapid adoption of standardized ICs in place of designs using discrete transistors.

In 1965 Gordon Moore observed that silicon transistors were undergoing a continual process of scaling downward, an observation which was later codified as Moore's law, which suggests that the number of transistors that can be fitted onto a chip doubles every

two years. Since his observation, transistor minimum feature sizes have decreased from 10 micrometers to the 32 nm range in 2010.

Nowadays with the development of nanofabrication techniques, a CPU chip with billions of transistors can be fabricated in a state-of-the-art fabrication facility. Complex fabrication techniques, such as immersion lithography[5] and extreme ultraviolet (EUV) lithography[6] have been utilized to produce devices with smaller features allowing individual chips to contain more transistors than ever before. On the other hand, there are also considerable efforts to make semiconductor devices such as FinFET[7] and 3D transistors[8] that consume less energy and become more effective. Also, new materials, such as Silicon on Insulator (SOI) wafers[9] and high-k materials[10] are being used in semiconductor industry to improve the performance. According to the trend targets listed by the International Technology Roadmap for Semiconductors (ITRS),[11] the feature size of a transistor will shrink to 16nm in 2016 by using conversional fabrication methods. However, after that there is no proven method to manufacture smaller devices.

Clearly, it becomes a pressing issue to develop a new fabrication method to shrink feature size further in the near future. Hence, the biggest challenge in the semiconductor device manufacturing is to develop entirely new fabrication techniques with sub 10 nm resolution on critical dimension to meet the requirements of the coming decade. Since most of these fabrications are applied in nanometer scale, one needs to understand the concept of nanotechnology and some other related subjects such as nanometrology before we go into this field.

1.1.2 History of Nanotechnology

The term "nanotechnology" was first defined by Norio Taniguchi[12] of the Tokyo Science University in 1974 as follows: "'Nano-technology' mainly consists of the processing of, separation, consolidation, and deformation of materials by one atom or one molecule." Since that time, the definition of nanotechnology has generally been extended to include features as large as 100 nm.

In history, the first mention of some of the distinguishing concepts in nanotechnology appeared in a letter in 1867 by James Clerk Maxwell. In Maxwell's 1871 book titled *Theory of Heat*, he conceived a thought experiment as a way of furthering the understanding of the second law, and that experiment was known as “Maxwell's Demon”. In 2007, David Leigh [13] created a nanodevice that successfully performed a real experiment based on the thought experiment by Maxwell.

During the 20th century, there have been many significant developments in characterizing nanomaterials and related phenomena in the field of interface and colloid science. Richard Adolf Zsigmondy used an ultramicroscope which applies the dark field method to observe and measure particles with sizes much less than the wavelength of light. He made a detailed study of colloidal gold and other nanomaterials with sizes down to 10 nm and less. Zsigmondy was the first who used nanometer explicitly for characterizing particle size. In his book,[14] he determined it as 1/1,000,000 of millimeter, and he developed the first system classification based on particle size in the nanometer range. In the 1920s, Irving Langmuir and Katharine B. Blodgett introduced the concept of a monolayer, a layer of material one molecule thick, which has been widely used in surface science and biology. Based on the concept of the monolayer, many applications,

such as anti-reflective glass and biological membranes, have been invented. In the early 1950s, Derjaguin and Abrikosova conducted the first measurement of surface forces.[15]

On December 29, 1959 at Caltech, Richard Feynman gave a talk "There's Plenty of Room at the Bottom" at an American Physical Society meeting.[16] Feynman described a process by which the ability to manipulate individual atoms and molecules might be developed, using one set of precise tools to build and operate another proportionally smaller set, so on down to the needed scale. In the course of this, he noted, scaling issues would arise from the changing magnitude of various physical phenomena: gravity would become less important, surface tension and Van der Waals attraction would become more important, etc. This basic idea appears feasible, and multiple assembly processes enhances it with parallelism to produce a useful quantity of end products.

Nanotechnology and nanoscience progressed in an unprecedented manner in the early 1980s with the birth of cluster science and the invention of the scanning tunneling microscope (STM). Introduction of cluster science led to the discovery of fullerenes in 1985 and the carbon nanotubes a few years later. The invention of STM made a major breakthrough in the understanding of the structural composition of various materials. IBM researcher Donald Eigler[17] was the first to manipulate atoms using an STM in 1989. In the experiment, he used 35 xenon atoms to spell out the IBM logo at ~ 4 degrees Kelvin.

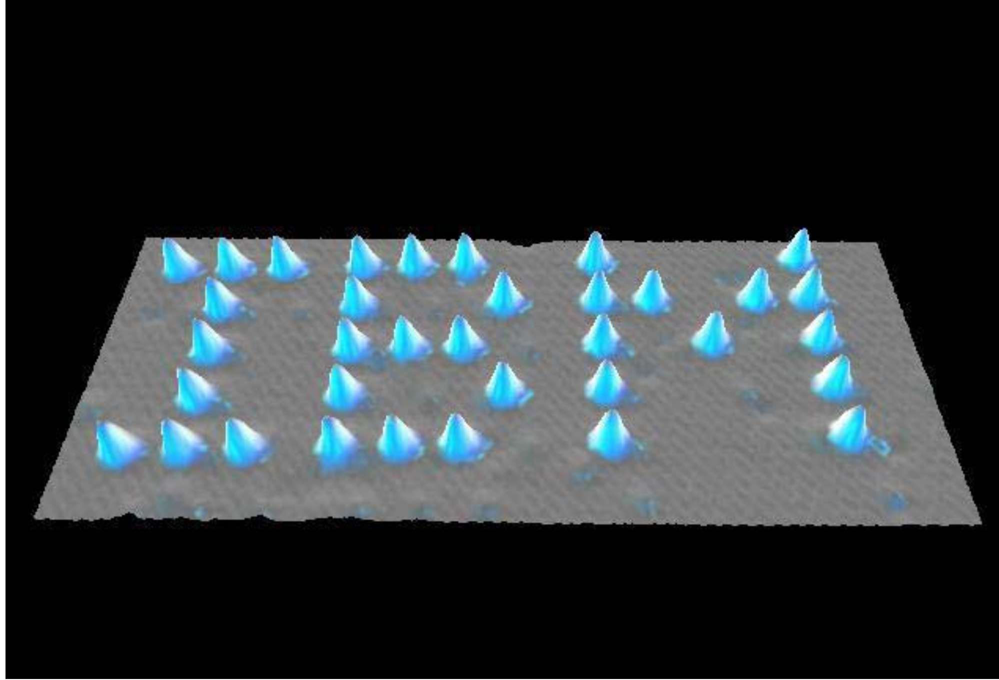


Figure 1.1: First successful atoms manipulation by using a low temperature UHV-STM. The "IBM" logo is made by 35 Xenon atoms (marked as blue dots in the image) on a nickel substrate. (From Don Eigler *et al.*[17])

Generally, two main approaches are used in nanotechnology to fabricate nanodevices namely the "top-down" and the "bottom-up". The "top-down" approach is the continuing reduction in the critical dimensions of current or conventional technology. In the semiconductor industry, experts invented many methods to approach the nanoscale, such as photo-lithography,[18] immersion lithography, and EUV lithography. Continued improvements in lithography have resulted in line widths as small as 15 nm.[19] On the other hand, the "bottom-up" approach, (also called molecular nanotechnology), is an attempt to reach the atomic limit of fabrication: to build devices such as nanowires[20] and molecular electronics[21] by directly assembling atoms. Although this approach is potentially suitable for producing devices in parallel and much cheaper than the top-down approach, it is still in its infancy. In the next decade, it is expected that advances in the top-down branch of nanotechnology will continue to lead the industry.

1.1.3 Dimensional Nanometrology

Control of the critical dimensions is one of the most important factors in nanotechnology. The dimensions of a typical nanosystem vary from 10 nm to a few hundred nm. The ability to measure feature positions or critical dimensions to sub-nanometer accuracy is a pressing issue in many cutting-edge manufacturing environments. In semiconductor manufacturing, the gate-length dimensions need to be measured accurately to 1 nm for devices that are of 40 nm in size, as stated in the ITRS.[22] The need for sub-100 nm reference standards and methods for making submicron measurements with tolerances approaching atomic size will become more and more demanding as the industry continues to reduce the dimensions of critical features.

Nanometrology is the science of measurement at the nanoscale. Nanometrology has a crucial role producing nanomaterials and devices with a high degree of accuracy and reliability in nanomanufacturing. Nanometrology includes length or size measurements (where dimensions are typically given in nanometers and the measurement uncertainty is often less than 1nm) as well as measurement of force, mass, electrical and other properties. Nanotechnologies, however defined, cannot progress independently of progress in nanometrology.

The challenge in dimensional nanometrology is to develop or create new measurement techniques and standards to meet the needs of next-generation advanced manufacturing, which will rely on nanometer scale materials and technologies. In order to build future devices atom by atom, it will first be necessary to measure devices atom by atom. To be able to measure or determine the parameters of nanostructures and

nanomaterials, various techniques and instruments, such as X-Ray Diffraction (XRD), Transmission Electron Microscopy (TEM), High Resolution Transmission Electron Microscopy (HRTEM), Atomic Force Microscopy (AFM), Scanning Electron Microscopy (SEM) and Scanning Tunneling Microscopy (STM), are used to measure and determine nanostructures with specific features.

1.2 Goals and Motivation

Because of the unprecedented development of nanotechnology in the last two decades, the need for metrology tools at the nanoscale and atomic scale has become increasingly clear. Length metrology tools are necessary to facilitate manufacturing of those new nanodevices by controlling the critical dimensions. The development of dimensional nanoscale and atomic scale metrology should also follow the pace of the nanotechnology.

To develop and promote measurement standards and technology to enhance productivity, facilitate trade and improve the quality of life, the National Institute of Standards and Technology (NIST) has launched the Atom-Based Dimensional Metrology (ABDM) Project[23] to develop a new, comprehensive approach to dimensional metrology using the atom spacing of a crystal as the fundamental "ruler" or scale. The 3D atomic scale structures will be made on hydrogen-terminated silicon substrates to meet the requirement of dimensional metrology. This work also represents an important advance in developing robust and repeatable processes for controlled patterning at the atomic scale, which can be combined with many current nanofabrication technologies, such as Atomically Precise Manufacturing (APM) and molecular imprinting.

The main motivation for this thesis is to address the issues at the sub 10 nm and atomic scale, and to develop next-generation tools for dimensional metrology at these length scales. In order to accomplish this task, it is necessary to develop methods to fabricate 3D nano-artifacts which can be measured and traced directly to the intrinsic crystal lattice. In order to use these artifacts as reference standards, it is necessary to develop a method which can transfer them to other measurement systems with dimensions known at the nanometer scale.

The methods developed as a part of this thesis will provide atomic precision in three dimensions with programmable top-down control. They could be utilized to solve the fundamental limitation of the manufacture of new devices such as quantum dots, qubits, Nanoelectromechanical Systems (NEMS) oscillators and biomedical devices with atomic precision. We are collaborating with Zyvex Labs (Dallas, Texas) and several universities in the Atomically Precise Manufacturing Consortium (APMC) to develop this revolutionary technique.

1.3 Methodology

There exist a wide range of techniques for fabrication on the sub-micrometer length scale, from sophisticated lithographic methods[5,6,18] that have their origins in the semiconductor industry to more recent materials and chemical advances that rely on self-organization.[24,25] However, for sub-10 nm length scales the technologies that are currently being used prove inadequate as there is new set of challenges. Hence, the area is still in its infancy, and there is a lot of room for researchers to test their techniques and optimize the conditions to be able to bring this to the manufacturing level. Atomic-level

lithography is expected to emerge and enable a new class of nanotechnology devices over time, but the nanofabrication techniques are expected to face integration and cost issues. The patterning at this scale is of great importance to attain higher integration density for semiconductor devices.

The major problem for all the conventional techniques, such as photo and electron-beam lithography, is that they do not have sufficient resolution at the length scale of sub 10 nm.[26,27] Perhaps the only alternative is to use an atomically sharp tip to pattern nano to atomic scale features by exploiting various probe-sample interactions. A method proposed in the early 1990's to achieve atomic resolution lithography in silicon by using an STM to pattern a resist layer on the silicon surface.[28] In this technique a Si (100) surface is passivated with a 1 atom thick hydrogen layer where the hydrogen atoms serve as a resist on the surface analogous to conventional lithography. Then a highly confined electron beam from an STM tip is used under certain bias/current conditions to selectively desorb, in ultra-high vacuum (UHV), hydrogen atoms from the resist, thereby exposing the silicon surface below.

Although the experiments were performed almost two decades ago, there has not been much progress in terms of technological applications. By following the concept of the experiments laid out in the 1990's, one can come up with ideas to fabricate atomic precision nanopatterns which can then be used for device fabrication. Developing stable and sharp STM probes (tips), which is essential to write and image patterns, and producing an atomically flat working template are two of the major challenges to realize a routine patterning and device fabrication. For atomically precise fabrication, these

challenges need to be addressed so that we gain atomic scale control on the probes as well as the sample surface.

1.3.1 Preparation of Atomically Sharp STM Probes

As a main component of STM, probes (sharp tips) play a major role in atomic resolution imaging and atomically precise manipulation.[29] STM relies on electron tunneling between the tip and a biased surface in very close proximity where the electronic orbitals overlap. The probe and the sample need to be conductive (at least semi-conducting). As the tip is raster-scanned over the sample, STM can generate images representing the electronic state density on the sample surface. With sharper probes, one can substantially improve the quality of the images, and hence, there has been considerable interest in the fabrication of sharp tips.

Tip fabrication includes the electrochemical etching and *in situ* cleaning procedures for making consistent atomically sharp tips and *in situ* regeneration of atomic sharpness after every process step. To achieve APM, STM tips have to be identical and invariant during the process. This is an issue that has never been comprehensively addressed before since the idea of APM itself did not exist until recently.

There are many factors that contribute to the performance of the STM tips for this particular application, such as the lifetime of the tip (how long can we keep the tunneling point), chemical properties, mechanical properties, etc. The material used for the tip must be very hard in order to avoid deformation and erosion of the tip during imaging and patterning. The shape and chemical composition of the tip apex are important factors that influence the STM image resolution and the quality of nanopatterns. All STM

measurements demand good electrical conductivity of the tip. Tungsten (W) wire is widely used to fabricate STM tips, and other materials, such as platinum (Pt), iridium (Ir), or even gold (Au), also can be used as STM tips.

For different tip materials, the preparation methods vary. Some of common methods for producing sharp tips are electrolytic polishing/etching, chemical polishing/etching,[30] ion milling,[31] cathode sputtering,[32] whisker growth,[33,34] vapor,[35] electro-[36] or electron-beam[37] deposited, flame polishing,[38] mechanical shaping methods such as oil-stone hand polishing,[39] cutting,[40] machining,[41] fragmenting,[42] bashing,[34] and combinations of the above methods.

The first step towards making a sharp probe for STM is by electrochemical etching. Electro-chemical etching is an etching process using chemicals, enhanced by a direct electric current to remove material layers from a metallic wire. The chemical process that takes place at the liquid-air interface removes the surface layers in a way to produce a conical shank with a sharp termination.[43]

Guise *et al.* have reported an electrochemical etching drop-off procedure to reproducibly fabricate W tips with ~ 5 nm radius.[44] The W wire is immersed in a droplet of KOH solution (etchant) held by an iridium loop (~ 1 cm diameter). A voltage is applied between the tip and the loop so that the tip is the anode and the loop is the cathode. The tungsten wire is etched in two steps. In the first step (coarse) etching, a DC voltage (typically 3V) is applied between the electrodes using 2M KOH etchant solution. In the second step (fine etching), a DC voltage of 0.5 V is applied using a 0.1 M KOH solution as the etchant.

Sharp W tips can easily be prepared *ex situ* by electrochemical etching but are naturally covered by a dense oxide layer. This will drastically change the conductivity of the tip and make it difficult to establish a stable tunneling current. The tunneling characteristics no longer correspond to vacuum junctions, but instead to the thin insulating layer which will change the quantum states involved in tunneling. Lisa *et al.*[45] suggested the tungsten oxide can be removed by treatment with hydrofluoric (HF) acid. Tungsten oxide is soluble in HF, whereas metal tungsten is inert to HF.

In situ methods that include sputtering, ion milling, electron bombardment, etc., can be used not only in tip surface cleaning but also tip sharpening. Swanson *et al.*[46], and Janssen and Jones,[47] have shown that an electro-polished tungsten tip can be sharpened by sputtering of the tip by neon ions. The tip radius was brought down from 100 nm to 20 nm using this process. Neon is considered ideally suitable for this process as it has an atomic mass which is large enough to produce an appreciable sputtering rate. They control the neon pressure and sputtering current to achieve a desired tip radius. The tip was briefly annealed at 2000°C before sputtering. Vasile *et al.*[48] have developed a novel technique to fabricate tips for STM high aspect ratio imaging applications. The technique involves focused ion beam milling on an etched tip.

Larson *et al.*[49,50] demonstrated sharpening of atom probe specimen tips by ion-beam milling. This process has a better control over the thermal field process in terms of the amount of material removed. Although there is a considerable sharpening of the specimens, artifacts occur during the ion milling process such as the introduction of defects, the production of irregular specimen shapes, and the production of slight ridges on the specimen surface. Zhang and Ivey[51] have also observed that, for an ion milling

time of 40 min, the tip radius is reduced from 250 nm to 20 nm, and the cone angle is reduced from 35° to 25°.

Other approaches have been tried to create atomically sharp tips. For example, carbon nanotubes attached to at tungsten tip are a very good candidate for STM use.[52,53,54,55,56] Depositing foreign atoms onto the tip surface can also fabricate single atom tips (SATs). Hans-Werner *et al.*[57] showed that a tip with a single atom termination can be formed with the deposition of an atom onto a W (111) trimer base tip. SATs can be produced by electroplating a thin layer of a noble metal on a W (111) surface and subsequent heat treatment in UHV.[58]

Rezeq *et al.*[59] used chemically etched polycrystalline tungsten tips to make single atoms tips by field assisted etching of the tip using nitrogen. Nitrogen is adsorbed on the tungsten surface, leading to the dissociation of N_2 on the tungsten surface followed by a diffusion of atomic nitrogen into the top atomic layer of W. This causes a protrusion of the W atoms from the surface, creating sites with increased field intensity so that atoms are removed spontaneously by field evaporation. This process takes place on the shank and proceeds with the removal of shank atoms. The tip gets sharper in the process, and single atom tips can be generated. Field ion microscopy observations clearly showed single atom termination at the apex.

We used the electrochemical etching method to create sharp tips (radii are about 50 nm) in the experiments. We assembled a field ion microscope (FIM) integrated into UHV system to provide *in situ* W (100) and W (111) tip cleaning and sharpening. We developed a tip fabrication process to create atomically sharp tips with robust imaging and writing (nanolithography) capabilities.

1.3.2 Atomically Flat Silicon Surface Preparation

Another challenge is to create atomically flat surfaces as the substrate. Silicon is widely used because it is a good semiconductor compared to other materials at high temperature. It can be easily patterned and forms a good semiconductor/dielectric interface when grown in a furnace. Because it has so many advantages, silicon replaced germanium and became the main material and substrate of most semiconductor devices such as transistors.

Highly pure (99.9999% purity) single-crystal silicon can be obtained by using the Czochralski process.[60] During the process, dopant elements such as boron, phosphorus, and arsenic can be added into it to create n-type or p-type semiconductors with different resistivities. Later the silicon crystal is sliced and polished to form wafers. Usually the silicon crystal is cut at certain angles, which are known as crystal orientations, to achieve wafers with special surface orientations. The most common orientations are (111) and (100) directions. Orientation is very important because silicon is a highly anisotropic material. Wafers with different orientations have different physical properties, such as electronic properties, Young's modulus, surface tension, and chemical properties such as crystal structural, atom diffusion rate, etching rate, etc.

As a metalloid element in group IVA, silicon has a structure similar to carbon and germanium. Silicon has a cubic lattice structure known as the diamond cubic crystal structure (shown in Figure 1.2), and the lattice constant of silicon is 0.543 nm. A bulk silicon atom is connected to four nearest neighbor atoms with covalent bonds. As for those surface atoms, since they could not form enough covalent bonds, there are several

dangling bonds left. Because of these dangling bonds, surface atoms become very reactive. Also, these dangling bonds become very important while we are dealing with the silicon surface and surface atoms.

Although an oriented Si wafer (i.e. (100) or (111)) has a nearly perfect flat surface, the surface is not actually flat at the atomic level. Because of the tolerance of the cutting tool, the wafer cannot be cut perfectly parallel to lower-index crystal planes (i.e. (100), (111), (110) planes); the small derivation from parallel is generally called the miscut angle. Because of the miscut angle, the surface cannot maintain the perfect lower-index crystal planes over long distance, leading to what is known as a 'vicinal surface' which is close to but not a flat low-index plane. On the microscopic scale, a vicinal surface is composed of a series of terraces and steps. Therefore, vicinal surfaces are also known as stepped surfaces.

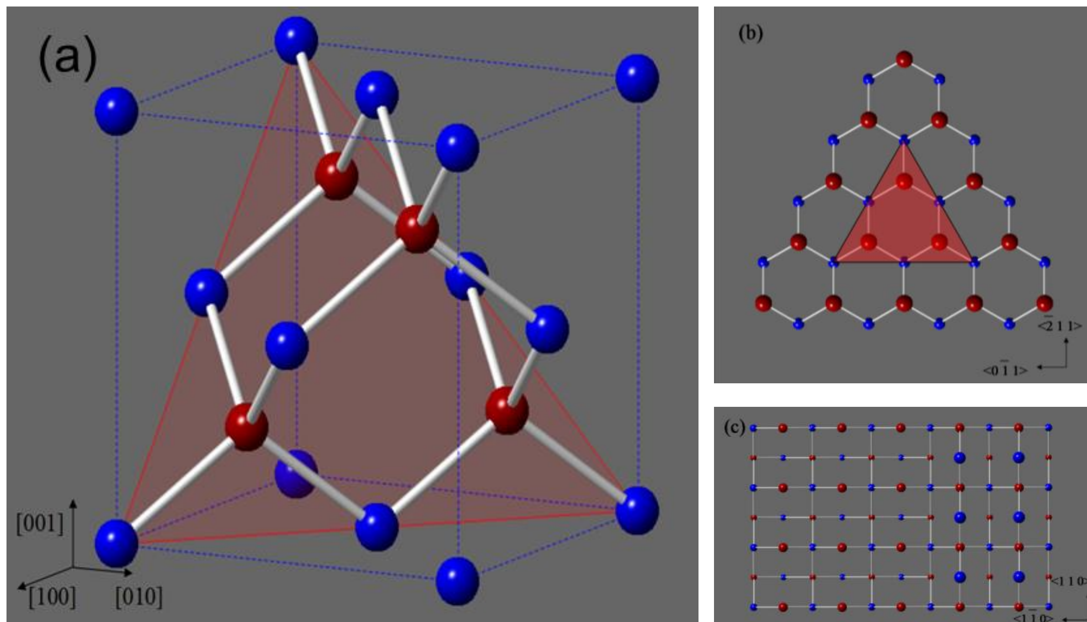


Figure 1.2: (a) The structure of a silicon unit cell. Every single Si atom (red) is connected four surrounding atoms with covalent bonds (white stick). The red triangle marked the (111) plane has shown in (b), and (c) represents the (100) plane.

The miscut angle of a wafer can be determined by x-ray diffraction. Figure 1.3 shows the miscut angle at the atomic scale. The average step width of terraces l can be estimated by the simple expression $\tan \theta = h/l$ once the miscut angle has been measured, where θ and h are the miscut angle and the step height, respectively. Vicinal surfaces play a very important role in surface reconstruction, step-step interaction, surface energy, kinks and defects. The effect of vicinal surfaces will be discussed later in this thesis.

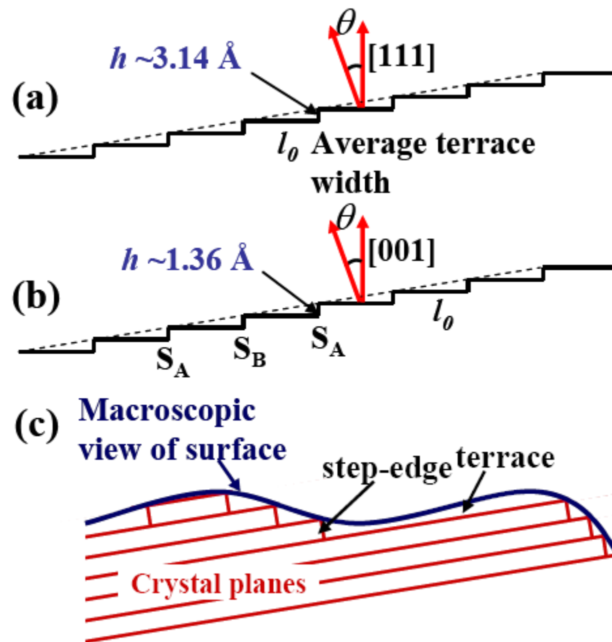


Figure 1.3: Schematic diagrams of the terrace and step structure of the Si (111) and Si (100) surfaces. (a) the Si (111) vicinal surface, (b) the Si (100) vicinal surface, and (c) the macroscopic view of surface. (From B. J. Gibbons[61])

For a macroscopic view, a silicon wafer surface is flat after undergoing polishing. However, the surface may contain small silicon fragments, trace metals, or even grease. Sometimes even microscopic cracks or defects are present. There are several methods reported in the literature, such as plasma cleaning or sputtering, wet chemical etching, and high temperature annealing to clean and fabricate silicon samples. A comprehensive

fabrication process needs to be developed to clean and fabricate silicon samples with atomically flat surface.

Plasma etching, which includes sputtering[62] and plasma cleaning,[63] is generally considered a good *in situ* cleaning method for many applications to remove contaminants from silicon surface. However, the surface roughness increases significantly after the process.[64] After cleaning, a thermal processing in UHV is required to produce a clean (contamination-free) and atomically smooth surface revealing the intrinsic lattice of silicon (100) surface.

Wet chemical etching, such as KOH or NH_4F etching, is very popular in silicon wafer cleaning and fabrication. Research and manufacturing related to silicon devices, circuits, and systems often rely on the wet-chemical etching of silicon wafers. Since silicon is a highly anisotropic material, the chemical etching speed on different orientations is different.[65] For example, the etching speeds of 55% KOH on the (110) surface is 500 times faster than on the (111) surface at 85°C.[66] Because of the preferential etching dynamics, we are able to create large atomically flat (111) terraces.[67] However, only pyramid structures are created after applied the KOH etchant on the (100) surface.[66] Hence we limit the *ex situ* chemical methods only to clean the surface of the thick oxide and other contamination layers that may be present.

The process of wet chemical etching contains several steps to remove organic contaminants, metallic particles, and oxide layers. Common acids, such as H_2SO_4, HCl and HNO_3, are used here to clean the surface and an HF or diluted HF or buffered HF has been applied to remove surface oxide. A hydrogen terminated surface can be obtained after treating by HF. Although a hydrogen layer can protect silicon in ambient conditions,

water molecules can penetrate it and oxidize the surface.[68] Also, the dissolved oxygen in solution can attack silicon immediately and roughen the surface.[69] After the etching process, some residue may still be on the surface as contaminants and cause surface defects at the atomic level. To reduce the effect of chemicals and provide a more controllable method to get repeatable and robust atomic flat surface, we combine the wet chemical etching and high temperature annealing method to modify silicon samples.

The high temperature annealing method[70,71,72] is not suitable for any semiconductor device fabrication currently because the device structure is expected to be destroyed beyond a certain temperature. Above that temperature, the structures atomic arrangement cannot be retained because of increased diffusion. However this method is suitable for our approach as there is no post annealing once the patterns are written on the surface. In fact, the initial UHV high temperature processing is necessary to reach our goal, because it leads to a complete desorption of the thermal oxide, diffusion of contaminants like carbon into the bulk, and to a completely flat surface (a few micrometers) due to the high mobility of the silicon atoms on the surface. The high-temperature annealing process can be carried out in various environments other than UHV. Inert gases such as nitrogen, argon, or hydrogen also can be used to smooth silicon wafer surface during high-temperature processing.[73] Around 500°C to 550°C, hydrocarbon contaminants can be desorbed from the sample,[74] and at 800°C silicon dioxide desorbed from the surface.[75] After flashing the sample to 1200°C, a flat silicon surface can be achieved.

At certain temperatures (800°C - 1000°C), silicon and carbon can form SiC,[76] which can pin on the surface and lead to a macroscopic roughness. It is necessary to take precautions during the high temperature processing to avoid the favorable temperatures

for SiC formation. Some metal ions, such as Fe, Ni, can also affect the reconstruction surface and induce lots of defects on the surface.[77]

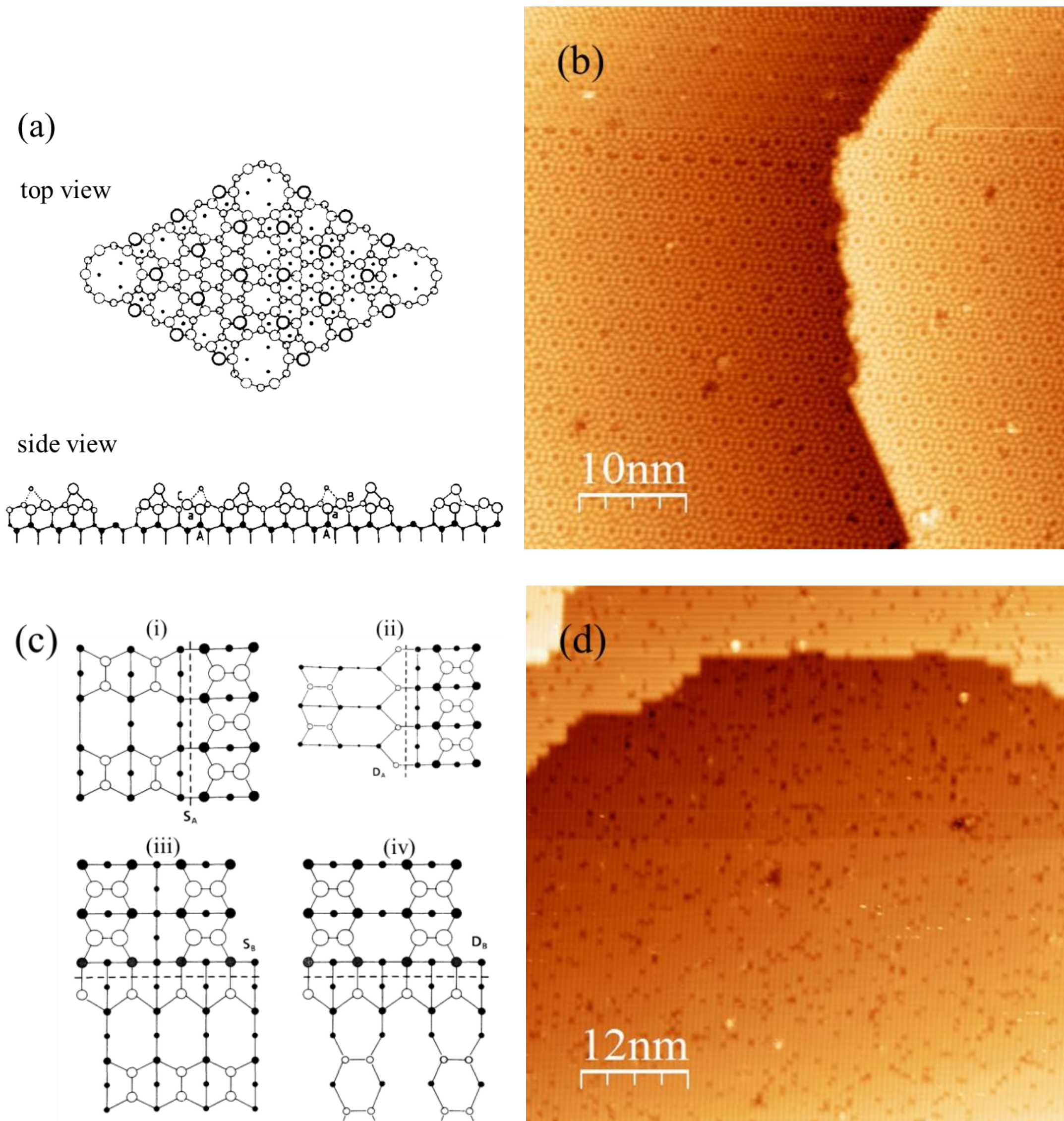


Figure 1.4: The Si (111) and (100) reconstructed surface. (a) A schematic picture of the Si (111) 7×7 reconstructed surface (From K. Takayanagi *et al.*[78]). (b) The corresponding STM image taken from our UHV STM. (c) The top view of the Si (100) 2×1 reconstructed surface. (i)-(iv) represent S_A, D_A, S_B and D_B steps, respectively. (From D. J. Chadi[79]) (d) An STM image of the Si (100) 2×1 reconstructed surface.

Atomically flat silicon reconstructed surfaces are verified by the STM after high-temperature processing. Due to the difference in the structures of Si (111) and (100) surfaces, the reconstruction patterns are different (as shown in Figure 1.4). The Si (100) surface forms alternating terraces with 1×2 and 2×1 dimer rows to reduce the surface

energy.[80] The formation of dimers also results in a surface of filled and empty rows. On the other hand the Si (111) surface, by comparison, exhibits a much more complex reconstruction. At low temperatures, the Si (111) surface forms a 2×1 reconstruction[81] (which is different from the (100)-2×1 reconstruction) and at temperatures above 400°C this structure converts irreversibly to a more complicated 7×7 dimer-adatom-stacking fault (DAS) reconstruction.[82] In addition, a disordered 1×1 structure is regained at temperatures above 850°C, which can be converted back to the 7×7 reconstruction by slow cooling. A number of similar DAS reconstructions have also been observed on Si (111) in non-equilibrium conditions in a (2n+1) × (2n+1) pattern, such as 5×5 and 9×9 reconstructions.[83]

1.3.3 Surface Modification/Patterning

Silicon reconstructed surface can be used as the template to perform nanofabrication after it has been properly treated. In the "top-down" approach, hydrogen-terminated silicon surfaces[84,85,86] can be used as a very good substrate. Not only can they provide long-range atomically ordered surface, but also they are found to be resistant to contamination and oxidation under ambient environmental conditions.[67,68] Under the protection of hydrogen atoms, silicon surfaces remain atomically flat after being exposed to ambient conditions for several hours.[87,88] That will be very useful when we transport samples outside UHV conditions.

Using atomic hydrogen, the surface can be passivated by filling in the dangling bonds. Atomically resolved patterns can be fabricated by selectively desorbing H atoms on silicon surface by breaking the Si-H bond under high energy electron beam. The exposed silicon atoms in the depassivated area have dangling bonds and are more

reactive compared to the rest of the surface atoms shielded by H atoms. As a next step, other materials, such as disilane (Si_2H_6),[89] oxygen (O_2),[28] can be introduced to enhance the nanopatterns or transfer them onto the substrate, as they are selectively reacting to the exposed atoms.

UHV-STM is the best tool to create hydrogen depassivated silicon nanopatterns. The UHV environment can maintain the surface clean for hours. STM is capable of sub-nanometer resolution of the surface and can be used to manipulate single atoms. Two different working modes are used to create patterns with different features. The high-voltage emission mode can depassivate large area with high writing speed.[90] Finer patterns down to the atomic scale can be achieved by applying the low-voltage resonance mode.[91]

The UHV-STM based fabrication does have drawbacks such as small scan size (usually smaller than 10 μm) and low writing speed (several nm/sec). Ambient scanning probe microscopes (SPM) can be a reasonable replacement. An ambient AFM can scan 100×100 μm^2 size and write patterns with 10 μm/s using a different technique. There is a water meniscus formed between the tip and the sample due to the moisture in air, with a bias voltage, oxide patterns can written on the sample.[92,93] Therefore, the feature size has been limited by the size of the water meniscus. Besides SPMs, focused laser beams have also been used to induce oxidation of the hydrogen passivated silicon surfaces.[94]

The silicon surface also forms an ideal substrate for nucleation and nanostructure formation due to its morphology. Ge ‘dots’ can be nucleated on Si (001) and are found to be are sensitive to the strain field of the substrate.[24] The strain distribution can be controlled on silicon surfaces.[95,96,97] By using molecular beam epitaxy (MBE) growth

equipment, the deposited materials can form 'dots' (up to about 100 nm) with self-ordering.[25]

In the "bottom-up" approach, self-assembly fabrication techniques are using on the modified silicon substrates. For example, the self-assembly block copolymer, PS-b-PMMA,[98] can be used to form nanometer-size patterns on silicon surfaces. By controlling the ratio of polymerized monomers and the copolymerization temperature, nanopatterns with different structures can be created. Some of these patterns have sub-10 nm features.

The Si (110)-16×2 surface can be used as the substrate on which to grow a highly integrated silicon nanowire mesh.[99] That silicon nanowire network can serve as a versatile nanotemplate for nanofabrication. The unique Si (111)-7×7 reconstruction surface can also be used as a template for deposition of Group III metals, such as Ga,[100] Tl,[101] and Al,[102] to form monodispersed nanostructures.

1.3.4 3D Nanostructures Fabrication

3D structures can be fabricated using different materials, such as O_2,[28] NH_3,[103] PH_3,[104] disilane and digermane.[89] The CVD process can also be used to pattern metals[105, 106] on silicon surface, too. After the fabrication, the height of those nanostructures is about 1 nm, which is not sufficient for the requirement of our project.

To increase the height of these nanostructures, a possible solution is to build materials on the nanopatterns. For example, nanopatterns can be filled by disilane or digermane on the sample surface at elevated temperature. The nanostructures are also covered by hydrogen atoms, which can be desorbed by STM. By alternately using hydrogen depassivation and disilane deposition processes on the surface, the height of the

nanostructures can be substantially increased. However, this method requires a lot of time to fabricate even one 3D structure; it also requires stringent stability to perform atomic precision lithography several times on exactly the same location.

At this time, it seems that the only feasible method which can enhance the nanostructures is the Reactive Ion Etching (RIE) process. The RIE process is an anisotropic etching technology which can be used to selectively etch different materials. After the nanopatterns have been oxidized and then formed into an oxide layer, they can be used as hard mask in RIE etching. After the RIE process, silicon will be etched away, and the nanopatterns will be remaining. By controlling the composition of etching gases, etching power and expose time, it is possible to create nanostructures with desired vertical dimension.

1.3.5 Preset Fiducial Marks

Once nanostructures have been fabricated, it becomes a realistic challenge to find those structures using different facilities. It's worse than 'finding a needle in a haystack' if no reference marks are on the sample surface. Preset references which recognize the nanopatterns need to be established on the surface.

Micrometer size features can be created on a Si surface using conventional optical lithography. These features cannot be considered as fiducial marks unless they survive after the annealing process. Nakamura *et al.*[107] investigated the evolution of 2-μm-deep gratings with different pitches ranging from 0.8 to 4.0 μm on Si (001) surfaces by annealing at 1100°C under UHV conditions. The results show that the gratings' collapse-

time increases with the grating period, and presumably the problem can be overcome by carefully designed fiducial marks.

S. Tanaka *et al.*[108] applied gratings on Si (001) surface to create large flat terrace during high-temperature annealing. Other patterns, such as holes,[109] stripes[96] and mesa,[110] etc. have also been added on the silicon surfaces to study the evolution of the surface morphology. But none of them have been successfully used as references.

The fiducial marks that we designed contain squares, circles, lines, etc., varying from 15 μm to 50 μm. After the annealing process, the fiducial marks can be recognized by a long-distance microscope (Infinity K2/SC) attached on the STM chamber. The STM tip location with respect to the fiducial marks can be recorded through a CCD camera. The pictures taken by the CCD camera can be used to identify the location of the nanostructures after the RIE process.

Besides locating the nanostructures, the fiducial marks are also found to influence the evolution of surface morphology during the annealing process. The surfaces of the cells in the patterned area transformed to nearly identical surface structures with large atomically flat surfaces (2 - 10 μm in width). Hence, the silicon surface with fiducial marks turned out to be an ideal place for the nanolithography.[111] A kinetic Monte-Carlo (KMC) simulation is introduced to understand the step flow and bunching process. The details will be discussed later in this thesis.

1.4 Outline of the Dissertation

This thesis describes the development of a new manufacturing method that can fabricate sub-10 nm size features by using STM, and also provides atomic-scale 3D structures which are suitable for dimensional metrology.

The outline of this thesis is as follows:

In chapter 2 the UHV system design will be described. Many UHV tools have been designed and built into the UHV system to meet the requirements of sample preparation and fabrication. A comprehensive transfer system has been established to facilitate the transfer of tips and samples across the chambers without compromising the UHV integrity.

Chapter 3 discusses the STM tips fabrication processes. The atomically sharp tips have been created after electrochemical etching, field ion microscopy (FIM) cleaning and thermal annealing. The fabrication details will be discussed, and the fabrication result will be compared with some other sharp-tip fabrication methods.

Chapter 4 deals with modification of the Si (100) substrate, fabrication of fiducial marks, and the high-temperature annealing process. The Si (100) substrate has been patterned with fiducial marks under E-beam lithography. A standard procedure has been developed to clean and fabricate the Si (100) reconstructed surface. Symmetric step-terrace patterns with wide atomically-flat regions created on the surface during the high temperature process. The effect of the fiducial marks will be discussed.

In chapter 5, a kinetic Monte-Carlo (KMC) simulation is used to simulate some of the aspects of the surface morphology after annealing. Surface morphology is strongly affected by fiducial marks in the experiments. The simulation may help us to understand

the surface evolution with the presence of fiducial marks which can help us to optimize the geometry and dimensions of the patterns for ideal step-terrace structure for our projects.

In chapter 6, we developed a procedure to fabricate the hydrogen passivated Si (100) reconstructed surface. The effect of hydrogen passivation will be discussed. Nanopatterns have been created by using two modes in UHV-STM. After oxidizing in ambient humidity and oxygen gas, nanopatterns transform to hard marks for the Reactive Ion Etching (RIE) process which will further enhance nanopatterns.

Chapter 2: System Design and Experiment Facilities Setup

To study the motion of silicon surface atoms and manipulate them requires a clean surface for a sufficiently long duration; it must be kept at extremely low pressures. An atomically flat, contamination-free silicon (100) surface is an essential requirement for atomically precise manufacturing. At a pressure of 10^{-6} Torr, approximately one monolayer of residual gas is formed on the sample surface every second.[112] A base pressure in the range 10^{-10} Torr is necessary to give a reasonable length of time for experiments before the surface is contaminated by adsorbates. An ultra-high-vacuum (UHV) system with the capability of processing samples and tips was used for atomic resolution imaging and fabricating nanometer sized patterns. The existing system was greatly modified by re-designing and adding several components to suit the experiments described in this thesis.

2.1 Ultra-high-vacuum (UHV) System

UHV is the vacuum range characterized by pressures lower than 1×10^{-9} Torr. To achieve that pressure level, multiple pumps need to be used in order to reduce the pressure from atmosphere to UHV. The system consists of different chambers connected by gate valves. The layout of the major UHV components of this system is shown in

Figure 2.1. The basic UHV system includes the load lock chamber, the transfer chamber and the main chamber. Besides these, two chambers, a custom field ion microscopy (FIM) chamber and a commercial scanning tunneling microscopy (STM) chamber, are attached to the main system to perform the analysis and fabrication of tips and samples. Tips can be imaged and cleaned in the FIM chamber and transferred *in situ* to the heating stage in the main chamber for further thermal processing. Some other devices, such as the low-energy electron diffraction (LEED), auger electron spectroscopy (AES), Hydrogen-flux cracker, pyrolytic boron nitride (PBN) heater, and oxygen heater are integrated into the system. Furthermore, a comprehensive transfer system, which includes multiple transfer rods, linear and rotary manipulators, and wobble sticks, has been established to facilitate the transfer of tips and sample across the chambers without compromising the UHV integrity. These components are critical to the projects and a considerable amount of time was spent for these modifications and hence they are described briefly in this chapter.

2.2 Components of the UHV System

Since my experiments are focused on atomic scale fabrication, it is essential that all the processing be carried out in a UHV environment. Hence, a UHV system with the ability of *in situ* fabrication and analysis is necessary for the experiments. For this purpose, the system is integrated with many analytical and processing tools to ensure the cleanliness and ultimately the performance for atomic scale imaging and lithography. Each of these tools used in the experiments will be described in this chapter.

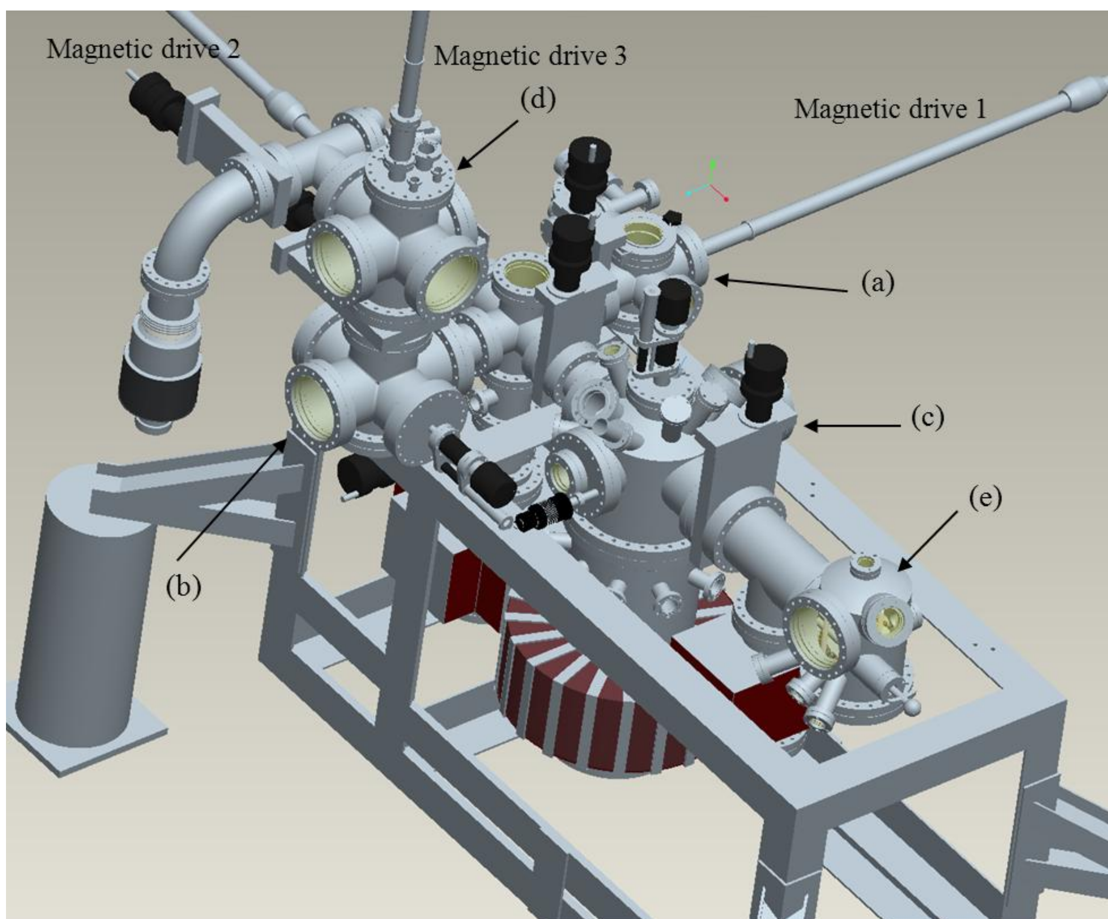


Figure 2.1: A diagram of the UHV system. (a) load lock chamber, (b) transfer chamber, (c) main chamber, (d) FIM chamber, and (e) STM chamber.

2.2.1 Load Lock Chamber

The load lock chamber is designed for quick and easy sample entry from atmosphere to vacuum and vice versa. Samples and tips are mounted onto the transporter in the load lock chamber via the quick-access door. The transporter is attached on magnetic drive 1 (as shown in Figure 2.1). Two pumps, a roughing pump and a turbo pump, are attached on the chamber, and the chamber's operating pressure is ~ 2×10^{-6} Torr. For compatibility purposes, the design of transfer section is based on the configuration of Omicron's devices, such as the sample holders and tip holders.

I have also used the load lock chamber for oxidation experiments by installing a custom, in-house fabricated temperature controlled oxidization set up. The oxidization set up is shown in Figure 2.2. This is used to oxidize the nanopatterns created in the STM in order to convert them into masks for further etching. The detailed oxidation process will be discussed in chapter 6.

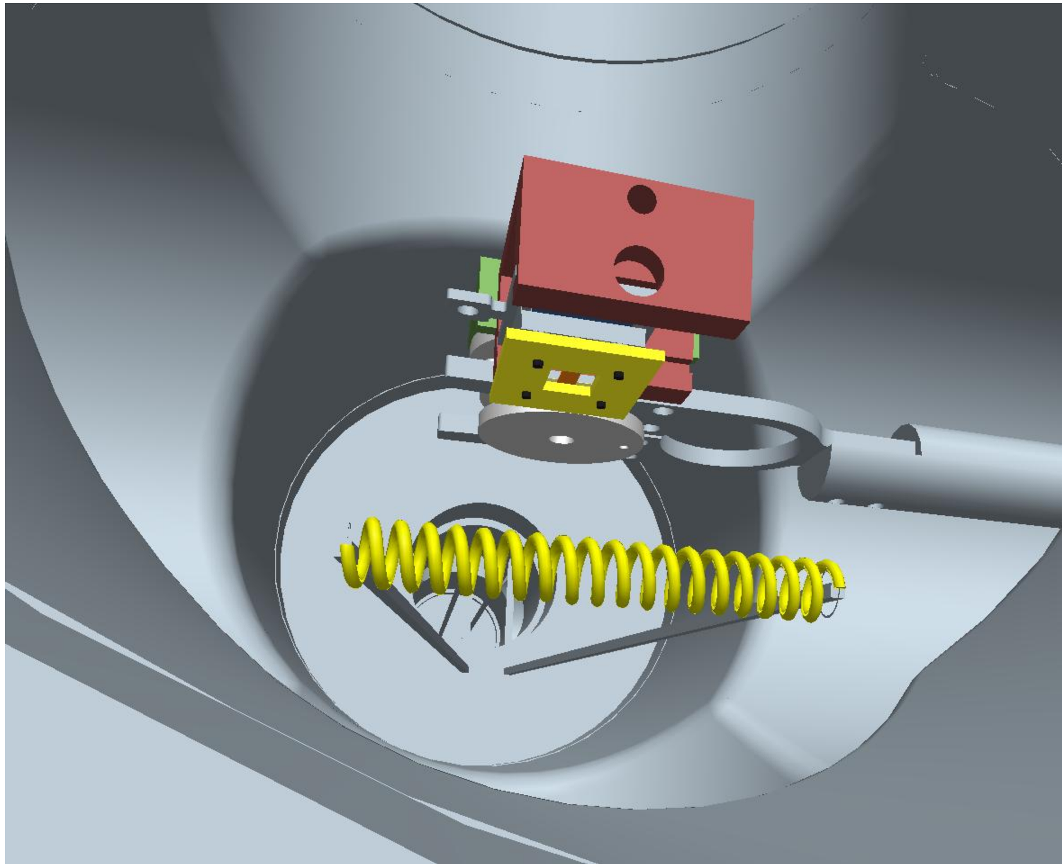


Figure 2.2: Sample oxidization in load lock chamber with a high-temperature quartz lamp. The yellow rectangular piece shown in the picture is the top side of the sample holder. The small orange piece within the sample holder is a Si sample. The quartz lamp appears as a big yellow coil in the picture.

2.2.2 The Transfer Chamber

Although the transfer chamber does not have any instrumentation and is not directly related to experiments, it is a very important part of the transfer system. The pressure of

the transfer chamber, as well as the FIM chamber, is controlled by an ion pump and an auxiliary titanium sublimation pump. The pressures in both chambers are maintained at 2×10^{-9} Torr and are monitored by two hot filament ion gauges.

When a sample holder arrives at the transfer chamber, the transporter is moved onto magnetic drive 2 (the sequence is shown in Figure 2.3). Once the pressure of the transfer chamber drops back to 2×10^{-9} Torr, the gate valve between the transfer chamber and the main chamber opens and the sample goes into the UHV environment

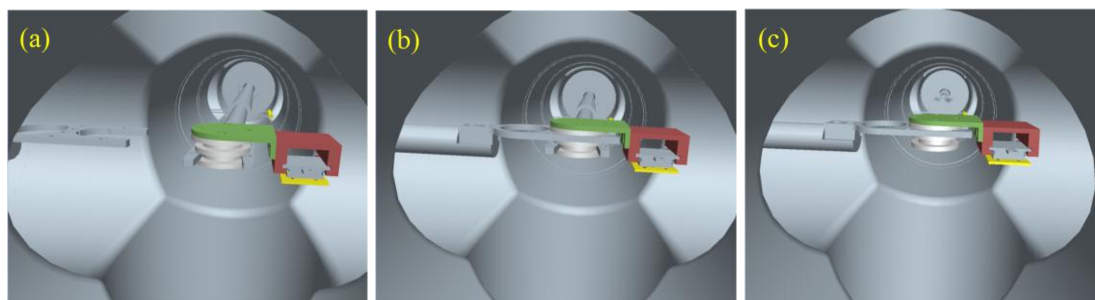


Figure 2.3: A set of diagrams showing how the transporter along with the sample holder is transferred from magnetic drive 1 to magnetic drive 2. (a) The sample holder is carried into the transfer chamber by a transfer fork attached at the end of magnetic drive 1; (b) the other fork approaches the sample holder and then locks onto it; (c) drive 1 is retracted after the transporter has been transferred.

As for tip transfer, it is accomplished in between the transfer and the FIM chambers. The topside of the tip holder has been changed from stainless steel to Kovar (a nickel-cobalt ferrous alloy), which is magnetic. Then the tip holder is taken out by a rotary-linear manipulator with small magnets after transfer it into this section (as shown in Figure 2.4). Then the manipulator will rotate 180 degrees to match the position of the magnetic drive 3. The magnet, which is attached at the end of the magnetic drive 3, can hold the tip and secure it (the sequence is shown in Figure 2.5). Later on, the tip will be transferred to the FIM chamber with magnetic drive 3.

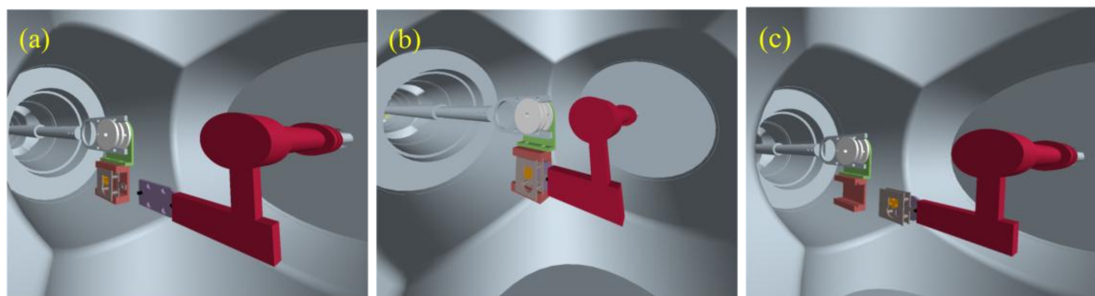


Figure 2.4: A rotary-linear manipulator with magnets grabs the tip holder and releases it from the transporter. (a) The tip holder is approaching to the grabber (in purple color). (b) The grabber attaches to the tip holder. (c) The drive 1 is retracted after the tip holder has been transferred.

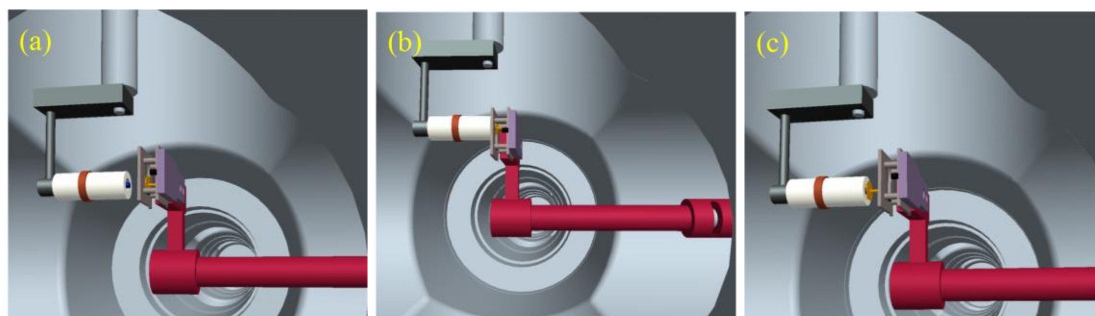


Figure 2.5: A set of diagrams showing the tip transferring between the manipulator and the magnetic drive 3. (a) The manipulator rotates 180° to match the position of the ceramic rode; (b) the tip is attracted by a magnet in the ceramic rode; (c) the tip is transferred to the rode.

2.2.3 The Main Chamber

The main chamber is equipped with a commercial heater (Omicron pyrolytic boron nitride (PBN) heater) which can perform direct (radiative) heating by using the PBN heating element and resistive heating (by passing current through the sample), for sample and tip processing. A low-energy electron diffraction (LEED)/auger electron spectroscopy (AES) system located in the chamber allows *in situ* analysis of the sample surface condition. A residual gas analyzer (RGA) is used to monitor the background gas species in the chamber. A water-cooled hydrogen cracker and a tungsten hot filament are also installed on the chamber with a hydrogen gas inlet. An ion pump and a titanium

sublimation pump maintain the base pressure at 1×10^{-10} Torr, which is monitored by a hot filament vacuum gauge and a cold cathode gauge.

PBN Heater

The PBN heater is a central element for sample preparation, tip annealing, and hydrogen passivation experiments. It is attached on a swing arm which can rotate 360 degrees inside the main chamber. With the swing arm, the sample can be rotated to certain angles to mate with other devices, such as LEED and the hydrogen cracker as required during experiments. A rotary-linear manipulator with a transfer head can grab the sample holder and tip holder from the magnetic drive 2. These holders (with samples or tip) will then be transferred onto the molybdenum annealing stage of the heater made for annealing. (The sequence is shown in Figure 2.6)

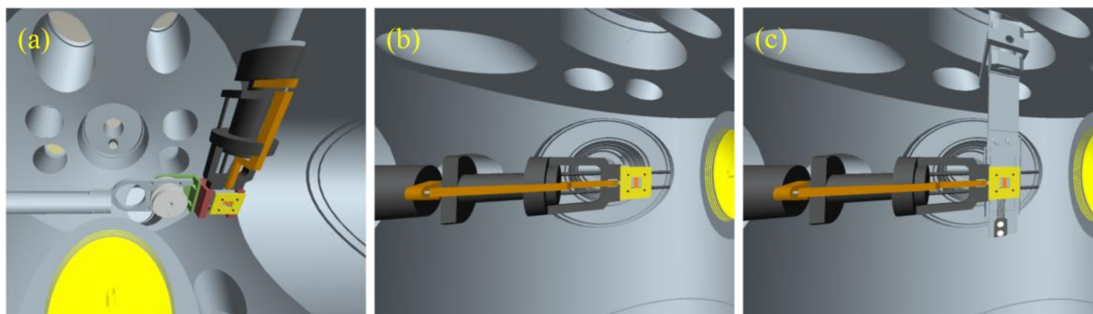


Figure 2.6: Illustration of sample holder transferring from the transporter to the PBN heater stage. (a) A transfer head (a black device with a golden-color jaw) grabs the sample holder on magnetic drive 2; (b) the transfer head rotates counter-clockwise 90° to match the position of the heater; (c) the sample holder after bing loaded on the heater.

A DC power supply can provide variable current through the sample after it has been loaded on the stage. The PBN heater can used to radiatively heat the sample holder or the tip holder as required. The temperature of the sample can be monitored after we rotate the heater to face the observation window by an infrared pyrometer. An infrared

optical pyrometer (range 500°C - 3000°C, ±10°C error) is used to monitor the sample temperature during the high temperature process. A second pyrometer (range 250°C - 1000°C, ±2°C error) is used to measure sample temperatures (~ 300°C) before the hydrogen passivation process.

LEED/AES System

A LEED/AES system was added to the main chamber to study the reconstruction of silicon surfaces and the procedure of hydrogen passivation. The SPECTRALEED system is a combination of LEED and AES. A surface analysis tool, LEED is a technique for the determination of the surface structure of crystalline materials by impingement of a collimated beam of low energy electrons (20-200 eV) and observation of diffracted electrons as spots on a fluorescent screen. It can be used to qualitatively determine the symmetry of surface structure by analyzing the diffraction patterns. I have used LEED to identify the surface structures of Si (100) and Si (100) 2×1 reconstruction, as they produce distinctly different LEED patters. It is also possible to use LEED to perform *in situ* diagnostics while the sample annealing procedure is processing. (See Figure 2.7 (a))

Hydrogen Cracker and Hot Tungsten Filament

After thermal annealing, the silicon surface needs to be passivated by atomic hydrogen. The traditional method is to fill hydrogen gas at a certain pressure and a red hot tungsten filament placed in front of the sample will crack hydrogen molecules and form atomic hydrogen. The sample is kept close to the filament, and highly reactive

atomic hydrogen forms Si-H bond and passivates the surface. This method is called the backfill method, and is shown in Figure 2.7 (b).

One can also get an H-flux from Atomic Hydrogen Source (provided by Tectra, http://www.tectra.de) by thermally dissociating hydrogen in a fine tungsten capillary heated by electron bombardment (thermal hydrogen cracker). The molecular hydrogen is cracked to atomic hydrogen after bouncing along the hot walls of the tungsten capillary. As opposed to the back filled method, this method can provide very high cracking efficiency, as the hydrogen is dissociated within the inlet capillary itself. An atomic hydrogen flux also can be used for *in situ*, damage free cleaning of residual oxygen prior to sample coating or analysis. (As shown in Figure 2.7 (c))

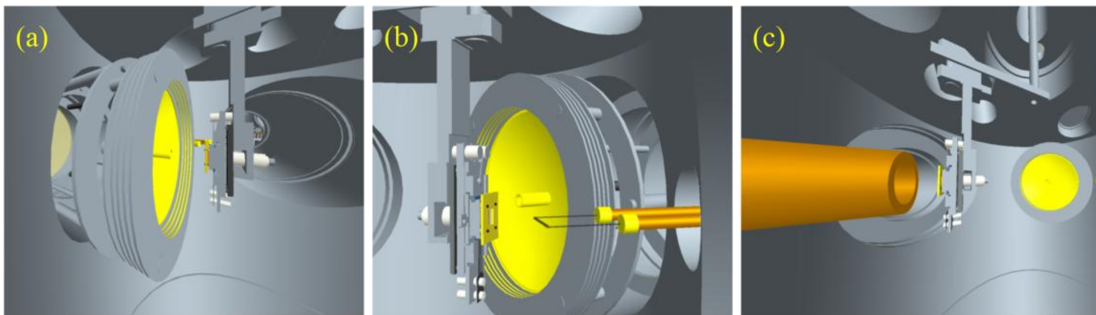


Figure 2.7: Illustration of the functioning of the rotary manipulator. (a) During the annealing process, the sample can be rotated toward to the LEED system before being analyzed; (b) the sample can be rotated toward a hot tungsten filament to perform the backfill hydrogen passivation experiment; (c) the sample can also be rotated toward the hydrogen cracker to perform the H-flux passivation experiment.

Residual Gas Analyzer (RGA)

During high temperature processing, many adsorbed gases, such as H_2O, CO_2 will be released from sample, thus increasing the total pressure. Some of them can react with silicon at certain temperatures and re-contaminate the surface. For example, hydrocarbons can react with silicon at 900°C - 1000°C to form SiC leaving the surface unusable. One should monitor the pressure of hydrocarbon during the experiment to

reduce the chance of forming SiC. The RGA system is used to monitor the quality of the vacuum and detect traces of impurities in vacuum systems.

2.2.4 The FIM Chamber

Field ion microscopy is a technique for imaging and modifying the apex of a tip with atomic resolution. In FIM, positively charged gas ions generated by the process of field ionization are used to produce images of the atoms on the surface of a solid specimen. The field ion image provides an atomic resolution view of the surface of the specimen and is used to characterize the features present in the microstructure. The image is a convolution of both crystallographic and microstructural information. Successive atomic layers of material may be ionized and removed from the specimen surface by the process of field evaporation. This enables the three-dimensional structure of the material to be imaged in atomic detail. (As shown in Figure 2.8)

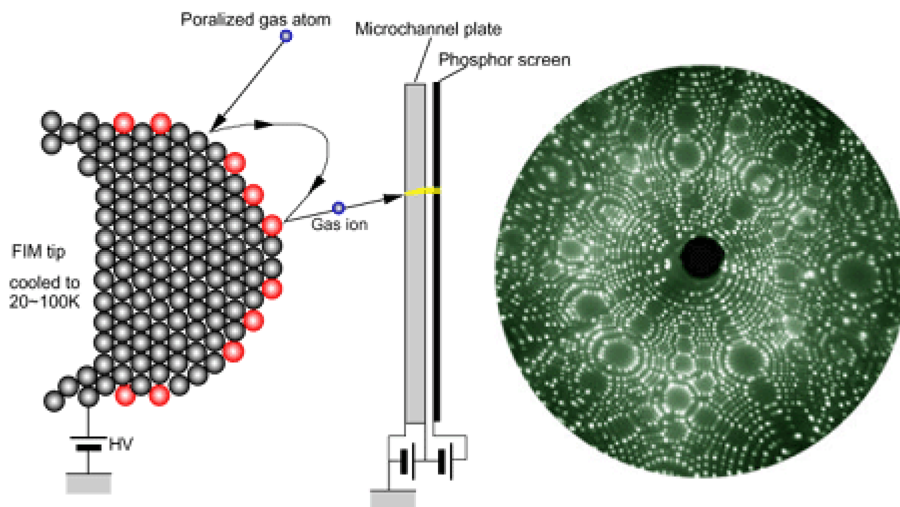


Figure 2.8: a schematic picture of an FIM (From NIMS/ Magnetic Materials Unit[113])

By using FIM, not only can we get information about the tip's apex, but the tip can also be cleaned under high electric field. The details of FIM application will be discussed in chapter 3.

2.2.5 The STM Chamber

The STM chamber is the heart of this system and is used not only for imaging silicon (100) 2×1 reconstructed surfaces and hydrogen passivated surfaces, but also for fabrication of atomic-scale nanostructures. We use a commercial variable-temperature scanning tunneling microscope (Omicron VT-STM) in the system. An ion pump is attached onto this chamber to maintain the UHV condition, and a metal gate valve isolates the STM chamber from the main chamber during the sample annealing process. The working pressure of this chamber is 1×10^{-10} - 2×10^{-10} Torr.

The components of the STM include scanning tip, sample, piezoelectric controlled height and x y scanner, coarse sample-to-tip control, vibration isolation system, and the control software and electronics. Figure 2.9 shows the schematic view of a STM. STM is based on quantum mechanical tunneling that occurs when the tip is sufficiently close to a biased sample surface (less than a nanometer). The tip is approached to the sample until it detects a preset tunneling current. This is done with the help of a feedback loop controlled by the SCALA PRO software supplied by the vendor. In the tunneling range, the scanning piezo is used to raster scan the surface always maintaining the preset tunneling current. While scanning, the piezo has to move the tip in the z-direction (perpendicular to the sample) to maintain constant tunneling current as a consequence of

the topography of the sample. The z-motion of the piezo can be recorded as a function of x and y coordinates and is a fair representation of the topography of the sample.

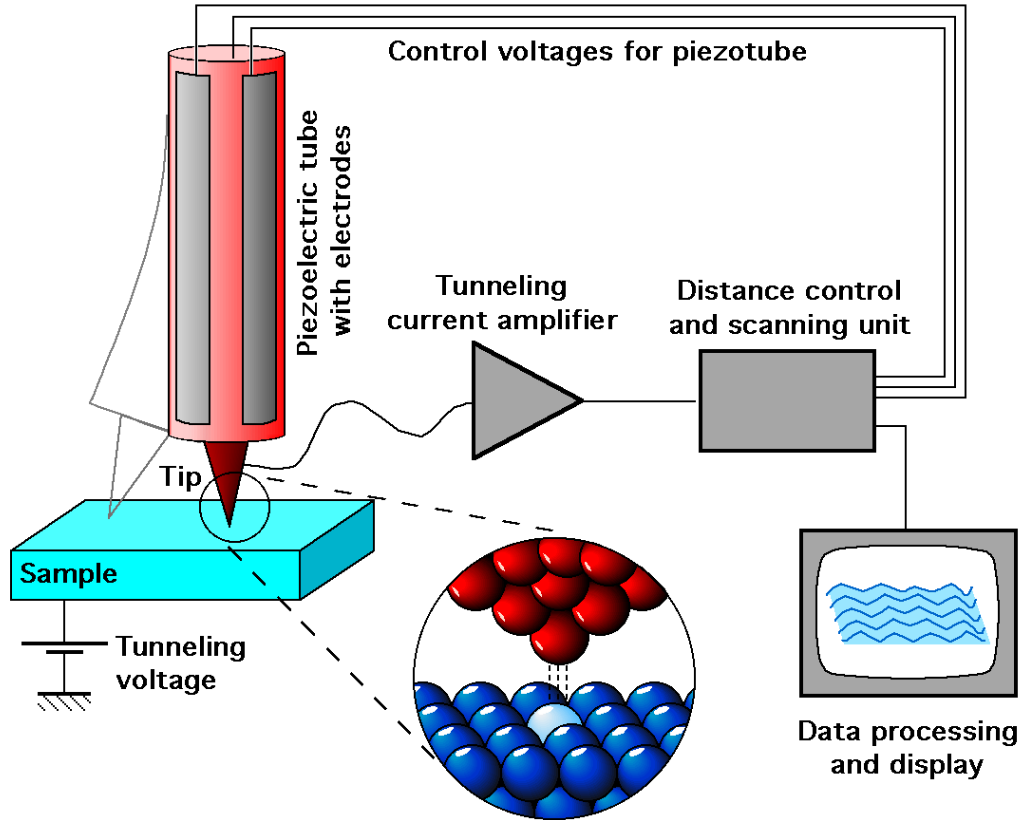


Figure 2.9: a schematic picture of an STM (From the IAP/TU Wien STM Gallery[114])

Maintaining the tip position with respect to the sample, scanning the sample and acquiring the data is computer controlled. The computer may also be used for enhancing the image with the help of image processing such as plane fit and 2-D FFT as well as performing quantitative measurements. More importantly, two modes, constant height mode and constant current mode, can be used for imaging the sample. In constant height mode, the vertical position of the tip is not changed, equivalent to a slow or disabled feedback. This leads to an image made of current changes over the surface, which can be related to charge density. In constant current mode, feedback electronics adjust the height

by a voltage to the piezoelectric height control mechanism. This leads to a height variation, and thus the image comes from the tip topography across the sample and gives a constant charge density surface. Thus, vertical displacement of the scanner (feedback signal) reflects surface topography.[115]

In addition to scanning across the sample, information on the electronic structure at a given location in the sample can be obtained by sweeping voltage and measuring current at a specific location. This type of measurement is called scanning tunneling spectroscopy (STS) and typically results in a plot of the local density of states as a function of energy within the sample.

As the tunnel current is extremely sensitive to the tip sample distance, proper vibration isolation is imperative for proper operation and obtaining reliable results. In our system, the whole system is supported by four pillars (as shown in Figure 2.1) which are standing on a concrete air table. The air table is located in the basement of the lab and is isolated (gas suspension) from the floor for maximum reduction of vibration effects. Additionally, an eddy current vibration isolation system is also utilized on our Omicron STM.

The Sample Holder

To avoid sample contamination, the sample holder is made of molybdenum and titanium. It can hold a sample with dimensions 9×2.5 mm^2 and pass variable current through the sample.

The Tip Holder

The tip holder is placed in the tip cage and secured by a key hole and a small magnet. A metal tip can be mounted into the center hole of a tip holder and secured by crimping the tip holder.

Chapter 3: STM Probes Fabrication

3.1 STM Probes

As a scanning probe, the tip is a central aspect of the whole project, because the performance of the tip directly influences the quality of imaging as well as lithography. Hence, one of the major focuses of the research effort was to develop a procedure that would improve the yield and the consistency of performance of the tips. Since tip performance was one of the top concerns, considerable time and effort was spent in optimizing tip fabrication and processing methods that can reliably provide quality atomic resolution images.

For atomic precision lithography, the tip radius should be on the order of atomic dimensions. An ideal tip for performing lithography on the sub-10 nm scale is a single atom tip (SAT) that can remain *invariant* throughout the experiment. It is well known that the final atomic-scale end form of the tip is extremely vulnerable and undergoes spontaneous changes, because of the high electric field and having to scan extremely close to sample surface. It has been observed from experience over the past few years that an *invariant* tip has remained more of a conceptual goal than a practical achievement. However, it was possible to develop a procedure that can reliably produce tips that provide atomic resolution images.

To create high quality STM tips with robust imaging and writing (nanolithography) capability, I developed a processing procedure for tips based on electrochemical etching

of polycrystalline tungsten. A tungsten wire (0.01" diameter) is chemically etched to produce a sharp tip of sufficiently small radius (less than 50 nm). Following electrochemical etching, scanning electron microscopy (SEM) was used to verify the tip's shape. Tips with optimum shape (short shank and small apex radii) are transferred into FIM to clean and sharpen by field evaporation and to produce the atomic structure of the tip apex. This is followed by thermal annealing of the tip which permits atoms at the apex to move around and settle down in the most stable positions. Details of the STM tip fabrication process will be presented in this chapter, along with fabrication results. At the chapter end, some novel SAT fabrication methods will be mentioned.

3.2 Tungsten (W) Atomic Sharp Tip Preparation Procedure

As an important component of the STM, tips play a major role in atomic resolution imaging and atomically precise manipulation.[29] STM performance relies on electron tunneling between the tip and a biased, atomically flat sample surface. The ABDM and APM projects are not viable without having robust atomically sharp tips. Therefore, reproducible preparation of atomically sharp tips is one of the key aspects to achieve our goals.

We developed a comprehensive method to routinely produce atomically sharp tips. First, a modified electrochemical etching method has been used to create sharp tips with preferred apex geometry. Instead of regular chemical cleaning, tip surfaces have been cleaned by field evaporation using an FIM. By carefully controlling the field evaporation process, the tip can be terminated by a single atom. Finally, a thermal process stabilizes the atoms on the tip apex, enhancing the performance of the tip.

3.2.1 Electrochemical Etching Process

The electrochemical etching method is one of the most popular methods to produce sharp tips. Most tip fabrication techniques use electrochemical etching as the first step to modify the metal wire to end up with a conical shank and a sharp point. One must keep in mind that, as has been reported,[44] one can fabricate atomically sharp tips by using only electrochemical etching. However, it is hard to routinely achieve atomic resolution imaging without adding an annealing process. The parameters and procedures, such as applied voltage (AC, DC or pulse) and etching steps (one-step or two-step etching) are optimized, to meet different requirements. For optimal use in STM, the tip requires a rapid decrease in diameter over a short distance. A robust protrusion (atomic) at the end of the tip is required to produce invariant, atomic resolution images.

The method developed for the work described here involves a two-step electro-chemical etching procedure, namely coarse electro-polishing and fine micro-polishing. By using a variable DC power supply the tip's etching rate can be controlled, and hence its shank shape. Different etchants are used for different tip materials. For W tip etching, KOH is used, while calcium chloride ($CaCl_2$) is used as an etchant for Pt/Ir wire.

Coarse Electro-polishing Process

The following procedure describes the coarse electro-polishing process.

1. Apply a high voltage (30 to 35 V) to the W or Pt/Ir wire, and then dip the wire into 3N KOH for few seconds to remove contamination from the wire surface.
2. Immerse one end of W wire, approximately 2 to 3 mm, into the 3 N KOH, then apply a sufficient DC voltage (7 V to 10 V depending on the concentration of etchants and the diameter of wire), and begin coarse polishing. The power applied voltage is automatically stopped by the power supply once the passing current is less than the set point value. (For Pt/Ir wire, the electrolyte is 35% saturated $CaCl_2$.)
3. Following the coarse etching process, the tip is dipped into distilled (DI) water and isopropanol alternately for a few seconds to remove contamination. The tip is then placed under an optical microscope for further evaluation.

Fine Micro-polishing Process

4. Use 0.5 N KOH solution for W tip fine etching (for Pt/Ir tip, use 1/3 saturated $CaCl_2$ solution). A loop of inert metal wire contains the electrolyte solution and serves as an electrode. A one-dimensional micromanipulator as shown in Figure 3.1 is used to manipulate the loop of liquid as the observer views the process through the optical microscope, at 750× magnification.
5. Immerse the etched tip in DI water for about 30 seconds, and then use an optical microscope to evaluate the sharpness of the tip.
6. Further evaluation of tip structure is then performed in an SEM before loading the tip into the vacuum chamber.

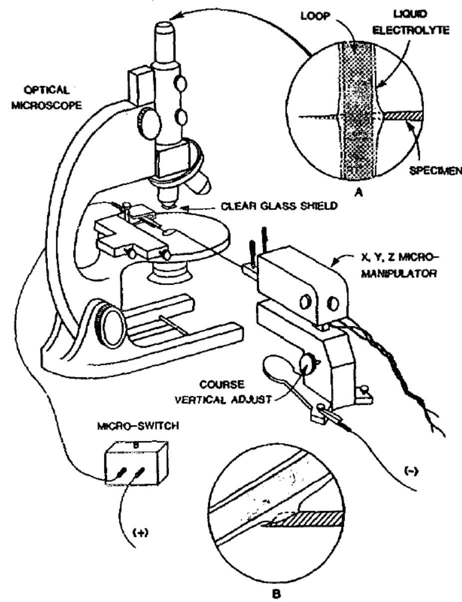


Figure 3.1: Fine micro-polishing apparatus for tip sharpening and resharpening. Insert A depicts longitudinal polishing and Insert B depicts side polishing. (From A. J. Melmed[43])

The fine electropolishing process can be used to modify the shape of tips with a micromanipulator. Figure 3.2 shows the mechanism of two fine polishing procedures: front polishing and rear polishing. Front polishing generally increases the tip cone angle and decreases the length; rear polishing can decrease the cone angle.

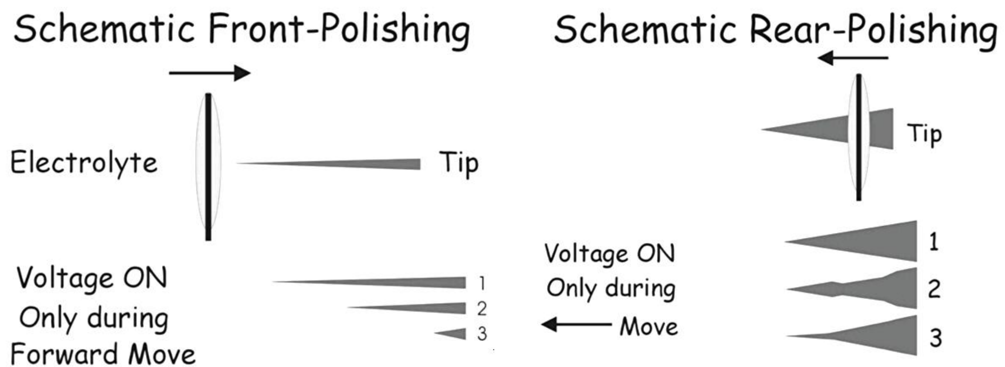


Figure 3.2: Schematic diagram of front-polishing and rear-polishing.

By using this method, the geometry at the end of the tip can be manipulated, and several tips may be produced within a short time. Following examination by SEM, the best tips are selected and used further in the fabrication process. (As shown in Figure 3.3)

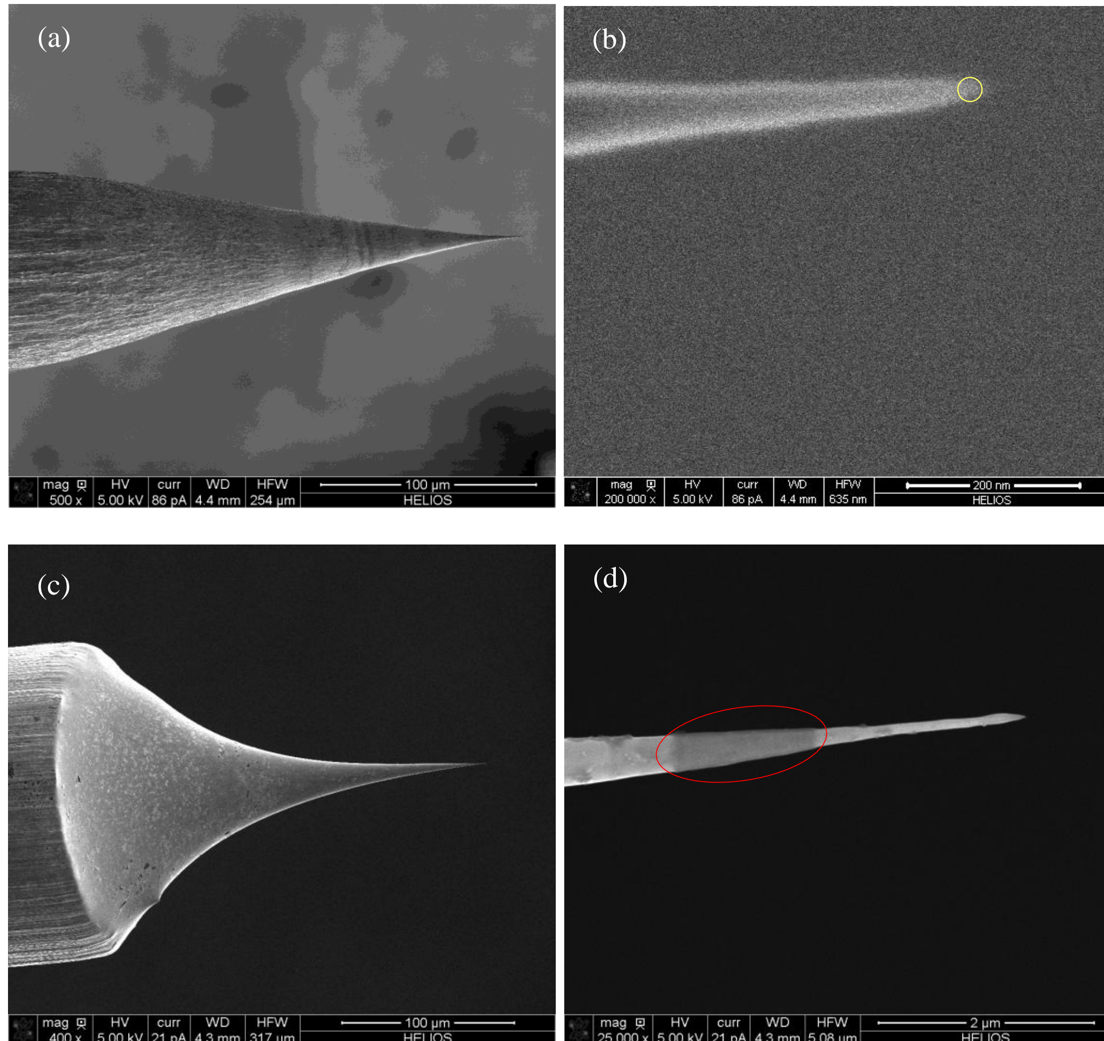


Figure 3.3: SEM images of etched W tips using (a) rear-polishing and (c) front-polishing processes. (b) and (d) are the high magnification images of these two tips, respectively. The diameter of the tip (a) apex is about 50 nm. The dark area (circled) shown on image (d) was due to the effect of high energy electron beam.

3.2.2 Tip Cleaning and Characterization with *in situ* Field Ion Microscopy (FIM)

In the FIM experiments, the end point of the specimen tip is crucial. Helium (He) gas is generally used for imaging in field ion microscopy. The tip's apex radius should be

as small as possible to create a high field (a few tens of volts per nanometer) to enable field desorption or field evaporation. The electrochemical etched tip as shown in Figure 3.3 is an ideal candidate for field evaporation for producing SAT. The FIM process can also be used to investigate the spatial structure of the tip apex. By carefully controlling the voltage on the tip, it is possible to create a tip apex with a trimer or even a single atom termination.

Polycrystalline W tips are primarily used as the specimens. The base pressure of the FIM chamber is 3×10^{-9} Torr.

1. Cool the tip to about -170°C with liquid nitrogen. Introduce helium gas until the pressure reaches 4×10^{-5} Torr.
2. Gradually increase the tip voltage until the FIM image appears (see Figure 3.5).
3. Slightly adjusting the tip voltage to remove central atoms one by one.
4. Check the structure of the tip apex by using field emission methods. (reverse bias voltage on tip)

As we have an FIM station integrated to the UHV system, the tip can be directly transferred into other chambers without recontamination. Also, a damaged tip can be re-sharpened using the same technique described above.

3.2.3 Tip Annealing Process

After FIM processing, the tip is transferred from the FIM chamber to the main chamber and loaded onto the PBN heating stage. The distance between the tip and the PBN heater is approximately 2 mm. During the annealing, the temperature of the PBN heater is about 1200°C, as monitored by an infrared pyrometer. Although there is no

direct means of measuring the temperature at the end of the tip, it is possible to estimate that the temperature during the 5-minute anneal could reach as high as 1000°C.

We found that the performance of the atomically sharp tips can be further improved by a subsequent annealing process. Although single-atom tips can be produced using the FIM, the lifetime of the tip is relatively short (few tens of hours) due to the unstable geometry of the tip apex. We have worked with one of our collaborators, H. Choi at University of Texas at Dallas by providing the experimental details for modeling the reconstruction of the tip apex atoms upon annealing. It suggested that thermal annealing can organize the apex atoms into electronically more stable configurations, which naturally extends the lifetime of the tip.[116] The effect of thermal annealing will be discussed later in this chapter.

3.3 Results and Discussion

3.3.1 Comparison between DC and AC Electrochemical Etching

By using electrochemical etching one can obtain tips with different shapes, ranging from a very thin shank, needle-like structure to a very wide conical structure. A tip with a long, gradual taper to the apex will be a very good candidate for FIM, but it will be very vulnerable during the process of STM imaging. The drop-off etching technique is therefore applied at this stage to make tips with short shanks so as to increase the lifetime of the tips.

DC voltage causes much less gas generation at the specimen surface compared to AC and thus enables more localization of the electropolishing activity. In comparison, AC

etching tends to perform a selective etching to remove material because of different local parameters, such as crystallographic orientation, composition and microstructure. However, AC etching can create numerous asperities on the tip surface, and those features may be very unstable and lead to spontaneous tip changes during the operation of the STM. Therefore, in our two-step etching technique, DC etching is employed as the first step to create desired tip structure with a smooth surface; and AC sweep is employed later to modify the very end of the tip to insure that it has an atomically sharp protrusion to serve as a stable tunneling point.

3.3.2 Tip Shape Examined Through SEM

Because the radii of well-etched tips are below the resolution limit of an optical microscope, an SEM is used to examine the quality of the tip. Since the SEM can provide highly magnified images with good depth of focus, the overall geometry of the tip shank can be checked with SEM. Often, tip shanks have either chemical contaminants, surface cracking, or an unstable end, those tips are discarded immediately. During its operation as an STM probe, the tip will pass back and forth thousands of times in extreme proximity to the sample surface. If the shank of a tip is too thin, it might cause mechanical noise during scanning. Also, a thin shank can increase the chance of fracturing the tip. Through experience, a tip with a shorter and wider shank is usually more stable and has a longer lifetime. By optimizing voltages and current cut-off values, tips with desired geometry can be produced.

After coarse observation of the sharpened tip apex using SEM, however, we found that the electron beam is often too powerful (see Figure 3.3 (d)). When a high energy

electron beam is focused directly onto the end of the tip, the tip will become deformed and even damaged. Therefore the radius of tips can only be estimated and further examination must be carried out using FIM. Following SEM analysis, the high quality tips (as shown in Figure 3.4) with a wide shank and small apex radius (less than 50 nm) are ready to go through the next process. Using these screened tips, one can routinely obtain atomically resolved Si (100) 2x1 reconstruction images.

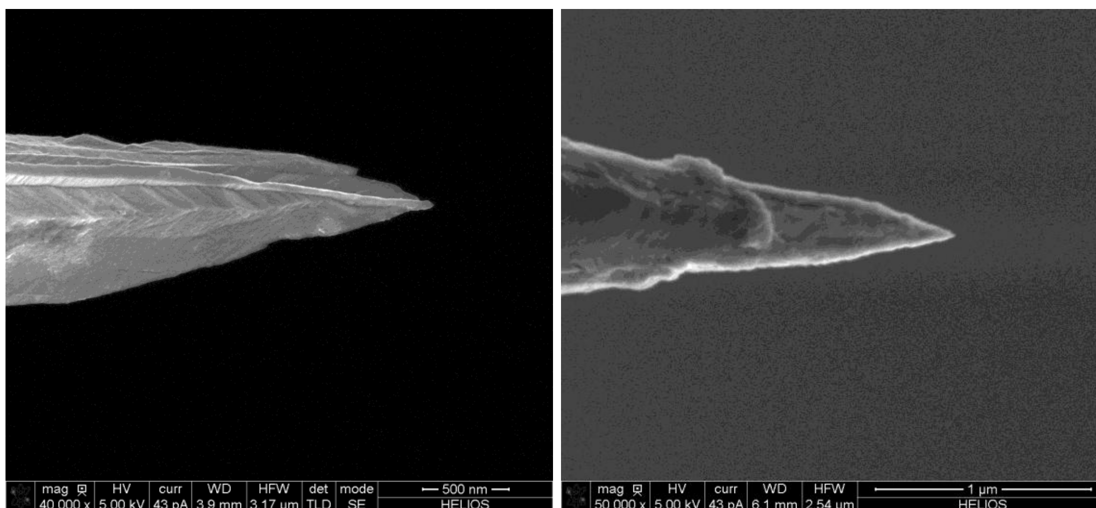


Figure 3.4: SEM images of electrochemical etched W (110) tip (left) and Pt/Ir tip (right).

3.3.3 Tip Characterization and Cleaning by FIM

FIM[117] is a very powerful tool to determine the spatial atomic structure of a test specimen. In FIM, at the very end of the tip, the electric field can be as strong as several tens of volts per nanometer. In this process, the tip is cooled down to liquid nitrogen temperature (78 K). Helium gas atoms contact the tip and lose their thermal energy in a series of collisions on the tip surface. At a critical distance from the tip, the gaseous atoms become ionized by the high positive field near the tip. The positively charged helium gas atoms have a trajectory away from the tip along the field lines, landing on an

imaging assembly consisting of a micro channel plate and a phosphor screen. There is a continuous beam of ions that originates from each of the atomic locations on the tip which produces bright spots on the phosphor screen that represent a true stereographic projection of the atomic arrangement of the tip apex. Through modeling,[118] the pattern typically reveals the spatial atomic structure of the apex.

FIM is used not only to determine spatial structure of the tip's apex but can also assist in the tip fabrication process in many ways as described next.

1. Ionization and removal of contamination, adsorbate layers, oxide, etc. from the apex region of the specimen, producing an atomically clean surface for examination.
2. Smoothing of protrusions and asperities, resulting in a regular, smoothly curved specimen end-form.
3. Controlled removal of successive atomic layers of material, allowing investigation of three-dimensional features of the specimen on the atomic scale.

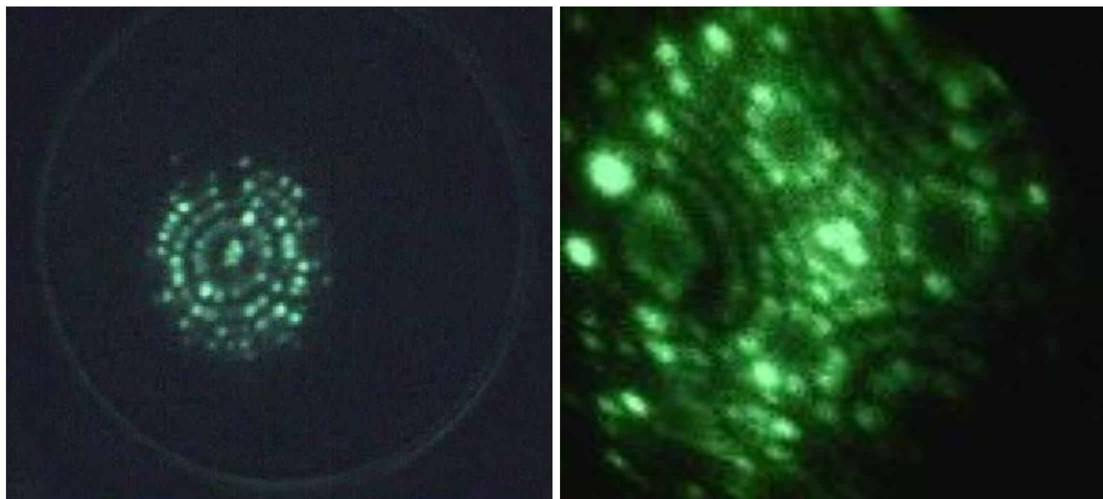


Figure 3.5: FIM image of a W (110) tip (left) and a W (111) tip (right)

By adjusting the voltage, the electric field can be controlled to remove the oxide layer and atomic-scale chemical residues from the surface. The result is a smoother surface and reduced number of undesired protrusions. By applying yet higher voltages, W atoms can be desorbed from the tip, and stable symmetric atomic patterns (as shown in Figure 3.5) are formed after a short time. With careful adjustment of the electric field on the tip's apex, it is possible to control the evaporation rate of W surface atoms. As shown in Figure 3.6, central atoms can be desorbed one by one, ultimately resulting in a single atom remaining on the apex.

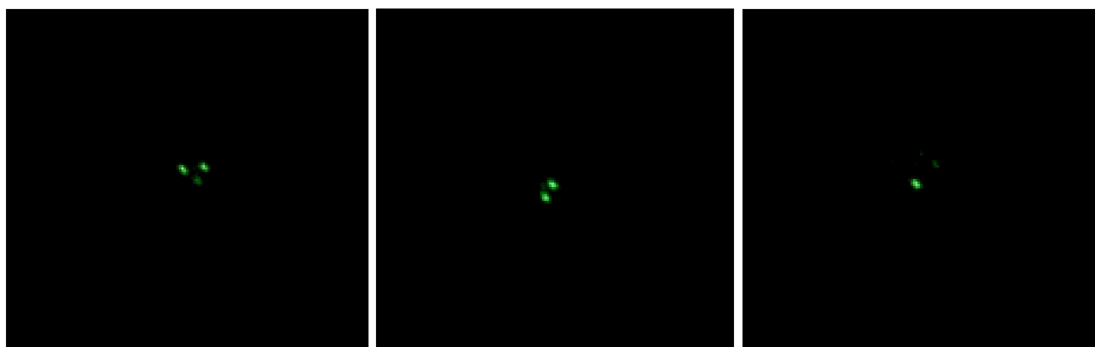


Figure 3.6: Sequence of atoms evaporation on a W (111) tip. Imaging voltage 1.7 kV, He pressure 1×10^{-5} Torr.

3.3.4 Thermal Annealing

Although FIM can produce an atomically sharp tip, the apex atoms can re-arrange during imaging, compromising the stability. From the feedback of the STM experiments, the lifetime and the stability of atomically sharp tips increased enormously after the thermal annealing. The idea of thermal annealing as implemented here was derived from similar experiments on noble metals.[119] H. Choi *et al.*[120] simulated the evolution of atomic configurations at the end of the tip. They demonstrated that thermal annealing can organize the atoms into electronically stable configurations, which naturally extends the lifetime of the tip. The results of the simulations are given in Figure 3.7.

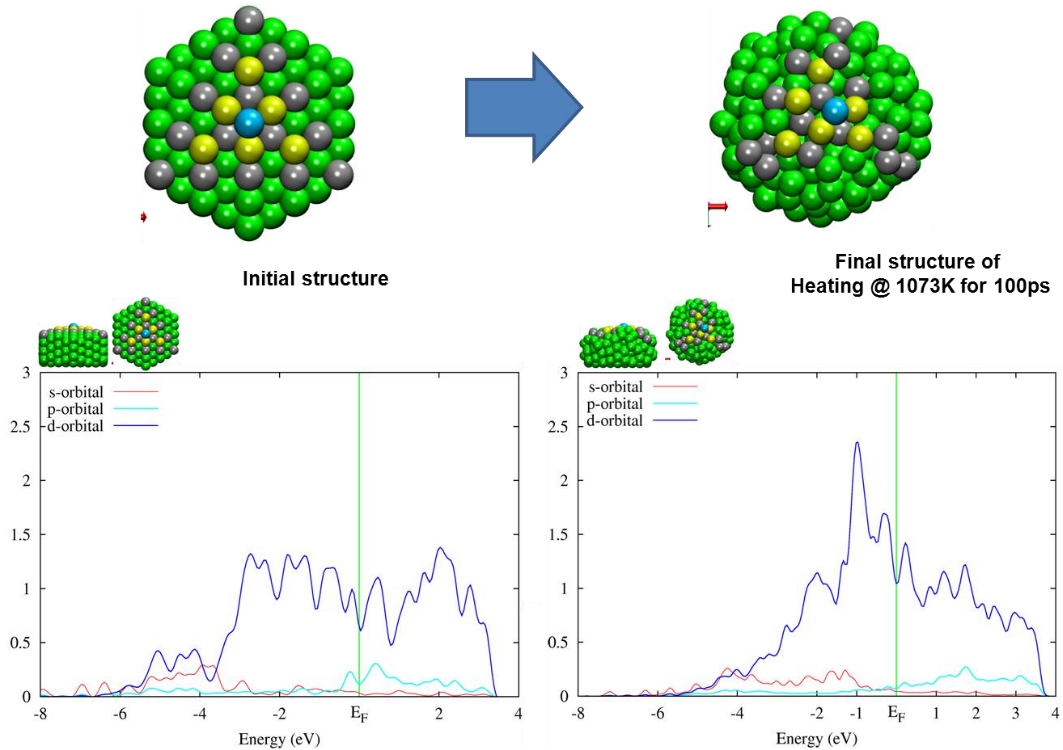


Figure 3.7: MD simulation of W tip apex structure before and after the annealing process. The d-orbital density of states for the apex W atoms configuration is calculated for both cases and plotted. It is seen that there is a strong d orbital peak after annealing. This could be very favorable for tunneling and improving the resolution of STM images. The 1st, 2nd and 3rd layers of the tip are marked as blue, yellow and gray dots, respectively. (From H. Choi *et al.*[120])

3.3.5 Tip Repairing (Rejuvenation)

Although the performance and lifetime of tips improved a lot after our fabrication process, tips become dull or blunt after several hundred hours of scanning and writing (nanopatterning). Repairing these blunt tips is a challenge in our project. By carefully operating the FIM to remove atoms at the end of the tip followed by the thermal annealing, tips can be repaired. Detailed repairing procedures can be found in 3.4.1.

3.4 Novel Fabrication Methods for Atomically Sharp Tip

There are several fabrication methods which may meet APM requirements.[121,122]

Field assisted N_2 tip[123] etching, noble atom deposition,[58] and Field-Directed Sputter Sharpening (FDSS)[124] can also create atomically sharp tips. In our laboratory, we only compared the fabrication methods for field assisted N_2 etched tips and noble-atom deposition tips in FIM experiments and compared the results with our previously-described results.

3.4.1 Field Assisted N_2 Etching Tip

Analogous to electrochemical etching, nitrogen etching can be used as an *in situ* FIM method to sharpen the tips. Previous studies of nitrogen (N_2) gas and tungsten tips show that nitrogen reactions occur in a low electric field, where it can penetrate the ionizing barrier.[125,126] After adsorption on the W surface, nitrogen molecules break under the electric field and form nitrogen atoms, and those atoms diffuse into the top atomic layer of the W tip. This causes protrusion of the W atoms and leads to an enhanced electric field around those protrusions, which is then adequate to ionize and evaporate the protruding W atoms.[123]

In our experiments, we applied the N_2 etching process on single crystal W (111) wires as well. For the N_2 etched tips, the initial shape of the tip is not very important. Because of the extremely high electric field at the tip apex, the shank of the tip will be slowly etched away by the nitrogen atoms. During the N_2 etching process, if the bias voltage on the tip is kept constant, the removal of atoms from the periphery of the apex sharpens the tip, which consequently enhances the field on the apex to a point where the apex atoms begin to field evaporate. To avoid the evaporation of central atoms, the bias voltage must be reduced to below the evaporation value. In this experiment, the N_2

etching lasted 30 minutes, and the N_2 pressure was maintained at $5x10^{-7}$ Torr. The bias voltage was slowly reduced to approximately 1 kV to protect the tip apex.

The shank etching effect can be verified by checking the tip structure before and after N_2 etching using SEM. By comparing SEM images (as shown in Figure 3.8), one finds that N_2 has etched a considerable amount of material away during the experiments, and the diameter of the shank had increased from about 100 nm to about 250 nm, which implied that the tip could be etched away several micrometers during the experiment. The subsequent FIM pattern (Figure 3.9) shows the spatial structure of the W (111) tip apex. Only a few W atoms remain at the very end of the tip. So even if a tip's initial condition is not excellent, by using this method the tip can be modified in an electric field to form a much improved structure.

Since the original tip structure is not a key concern, this method can be used to repair blunt W (111) tips. A blunt W (111) tip with a grain boundary was subjected to the N_2 etching process (Figure 3.10 left image). After one and a half hours, the apex of the tip becomes sharper and sharper, and there are fewer evaporated atoms. Finally, after careful control of the voltage, a very sharp tip (Figure 3.10 right) can be formed with a similar spatial structure to that shown in Figure 3.9.

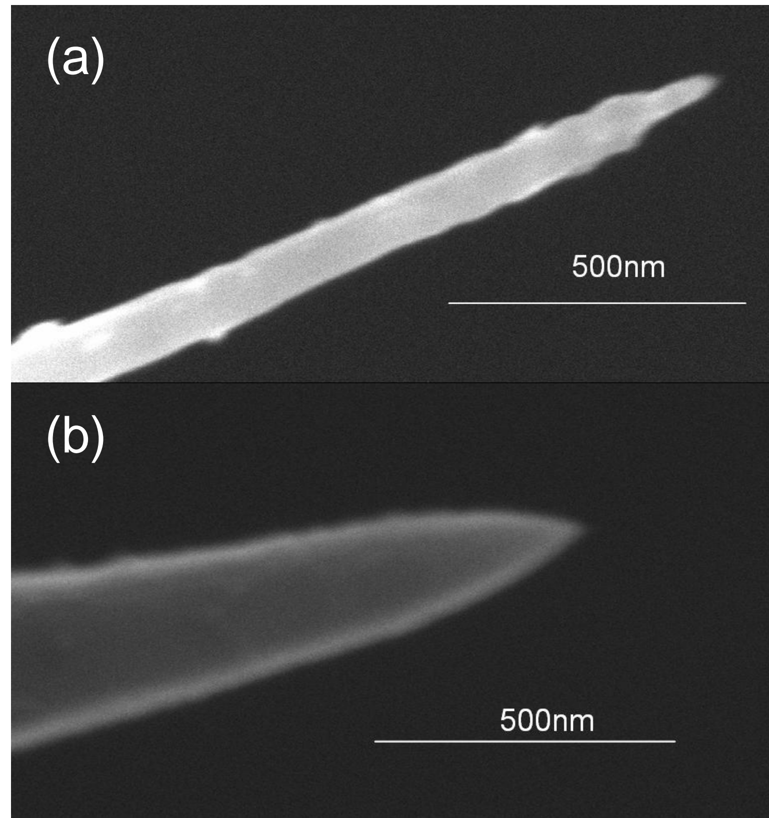


Figure 3.8: SEM image (a) before and (b) after etched by N_2 in FIM

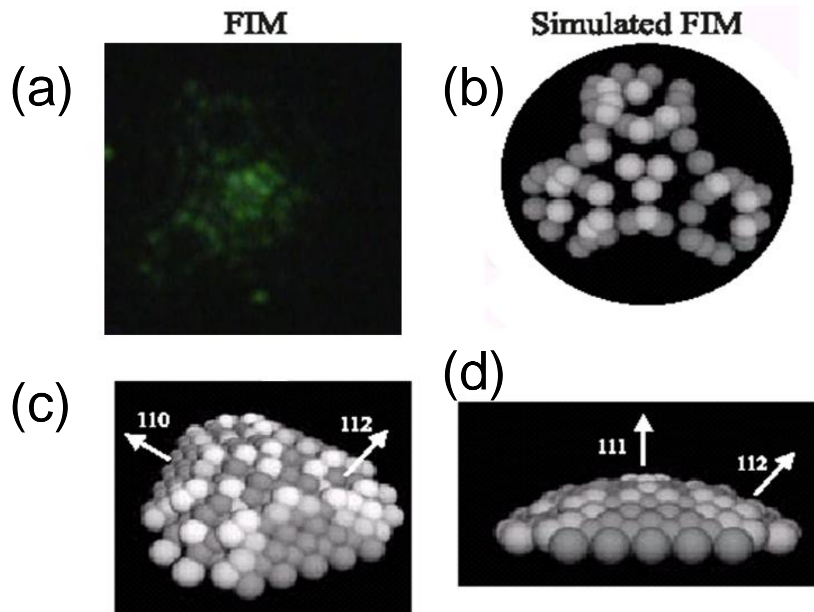


Figure 3.9: Comparison of simulated FIM images with experimental results. (a) W (111) FIM image obtained in our experiment; (b) simulated image of the tip apex; (c) and (d) are the geometry structrues in corresponding to the (a) pattern.

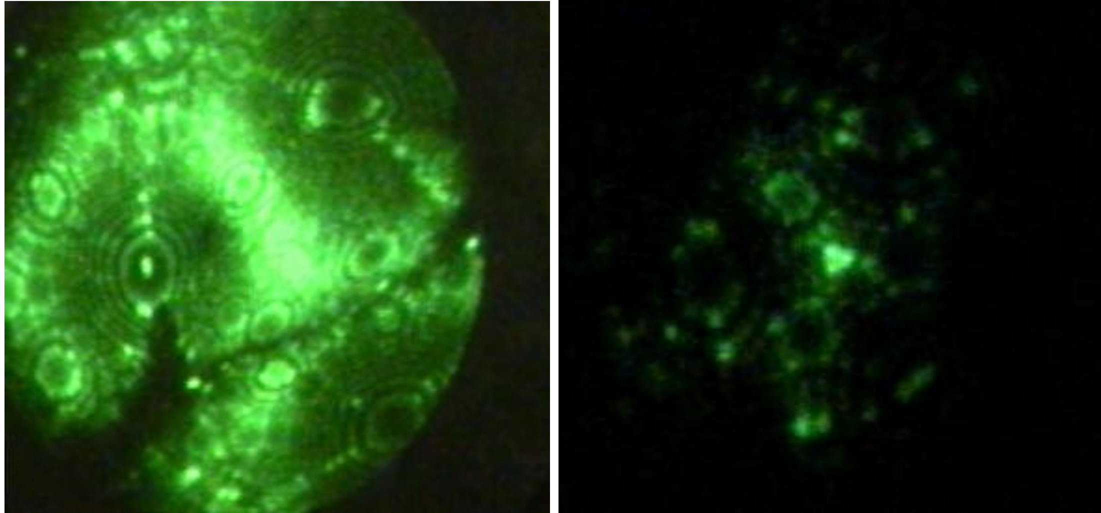


Figure 3.10: Left: before N_2 etching, imaging at 7.6 kV, He pressure 5×10^{-5} Torr. Right: after N_2 etching, imaging at 2.2 kV, He pressure 5×10^{-5} Torr, N_2 pressure 5×10^{-7} Torr. Etching voltage: 1.5 kV, etching time ~ 1 hour

N_2-etched W tips remain preserved in very good condition even after exposure to the ambient environment. An SAT was removed from the vacuum chamber and exposed to air for one day after N_2 etching. The tip apex was well preserved after exposure as can be seen from FIM images (see Figure 3.11).

Figure 3.11: FIM image after exposure to air, imaging voltage 1.9 kV.

However, N_2-tched W (111) tips do not perform consistently during STM operation. We suspected that after N_2 etching, a tungsten nitride (WN_2) layer formed at the tip apex, which could strongly affect tunneling conditions during STM operation. More experiments will need to be carried out to further investigate this method.

3.4.2 Noble Atom Deposited Tips

The concept of noble atom deposition is based on the finding of Madey *et al.*[127] An ultrathin Pd, Pt, Au, Ir or Rh film grown on a W (111) surface can undergo massive reconstruction upon annealing to form three-sided pyramids with (211) facets due to a decrease in surface energy anisotropy as the metal films are adsorbed on the W (111) surface. SATs can be produced by electroplating a thin layer of a noble metal on a W (111) surface and subsequent heat treatment in UHV.[58] The single-atom apex can be easily recovered by annealing the tip, thus the SAT can be regenerated with the same atomic stacking as the original pyramidal tip.

Although Pd/W and Ir/W tips from Zyvex Labs were examined, the FIM experiments were not considered successful. To examine the reconstruction of foreign atoms on W tips, we systematically heated tips from 600°C to 900°C with 50°C increments. FIM images were taken between every step, and we were extremely cautious not to field evaporate the Pd atoms off the tip while operating the FIM. Both FIM and field emission microscopy (FEM) images verified that no SATs were formed in the experiments. (As shown in Figure 3.12)

Figure 3.12: (left) Field Ion Image of a Pd/W tip, Imaging at 4.8 kV, He pressure 3×10^{-5} Torr. (right) Field Emission Image.

3.4.3 Field-Directed Sputter Sharpening (FDSS) Tips

Sputtering is commonly used for etching in semiconductor device fabrication. A focused ion beam (FIB), as an example, can be used to sharpen tips by bombarding inert gas atoms in a beam to remove material. Most of those sputtering techniques cannot provide atomically sharp tips due to the sputtering, anisotropic etching and damage of the surface. In the FDSS process, on the other hand, the tip itself is biased with positive bias voltage; a self-sputtering mechanism can effectively create atomically sharp tips. Analogous to the tip in FIM, the end of the tip is subjected to a strong electric field. When an ion beam bombards a tip which has high positive electric field at the apex, the ions are repelled from the apex and hit the shank of the tip. By adjusting the bias voltage of ion beam and the tip, the inhomogeneous electric field at the end of the tip will deflect ions from the apex regime, thus sharpening the tip. Figure 3.13 shows a schematic diagram of the FDSS process. Argon (Ar) plasma has been created and accelerated by an

electric field with a positive 1.8 kV bias. A positive bias voltage of 800 V is also applied on the tip to create an electric field to protect the end of the tip. After 20 - 30 minutes sputtering, the tip's apex has been shown to be smaller than 5 nm.

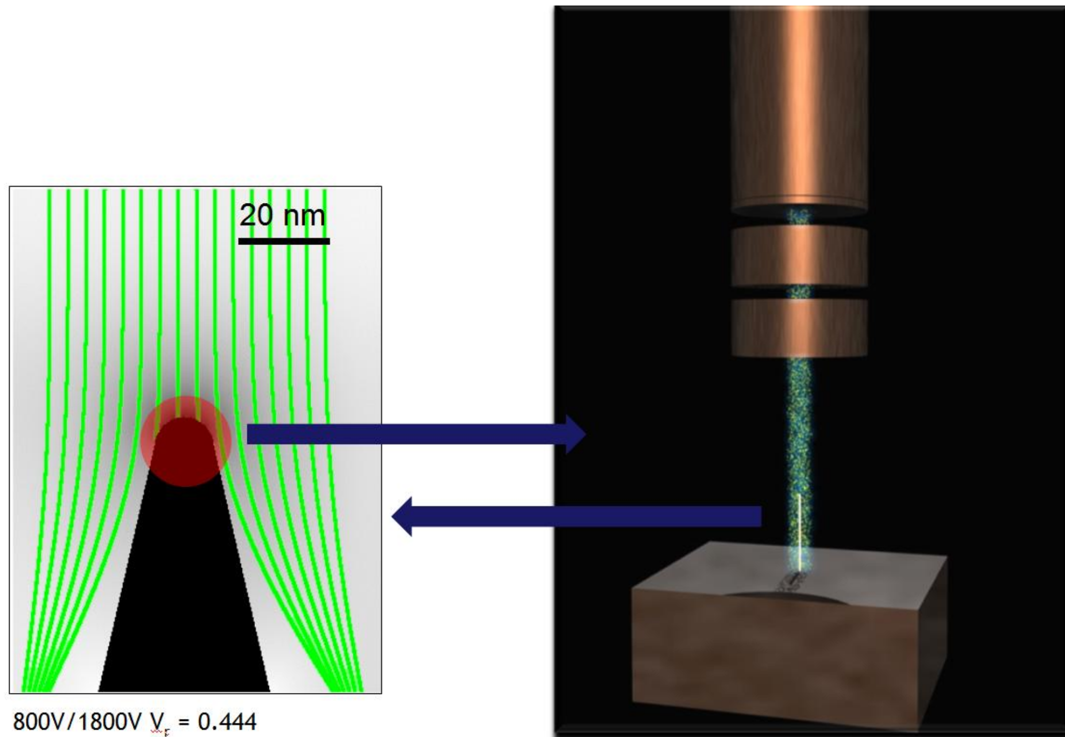


Figure 3.13: A schematic diagram of FDSS process (From S. W. Schmucher[124])

One of our collaborators, Joe Lyding, used this technique on W tips with a hafnium diboride (HfB_2) coating.[128] HfB_2 is an ultra-high temperature ceramic which has relatively high thermal and electrical conductivities. Because of its hardness, an HfB_2-coated W tip can last a long time in STM experiments. Those tips with radii less than 1nm are the ideal tips for tip-based nanofabrication.

3.5 Summary

Atomically sharp tips can be routinely obtained using our fabrication method. In the two-step electrochemical etching process, DC voltage has been applied during the coarse etching to create sharp tips with short and wide shanks; AC voltage is used to modify the tip apex and create a stable tunneling point in the fine etching.

The FIM process is used to remove the oxide layer on the tip apex and create atomically sharp tips. The following thermal annealing process allows the atoms on the apex to form a more stable geometry through reconstruction.

After our fabrication process, the tips may remain in good working condition for several hundred hours of scanning. Atomically sharp tip performance is validated by STM imaging, and the yield of atomically precise tips is over 80%.

Chapter 4: Controlled Formation of Atomically Flat Surface on Si (100) surfaces

4.1 Introduction

Preparing clean, atomically ordered, flat surfaces is a crucial requirement for atom based lithography, manufacturing and metrology. Controlling the dynamics of atomic steps on silicon surfaces and producing atomically flat wide terraces has gained unprecedented importance due to the demands in making finer 1D and 2D patterns over larger areas for the manufacturing of semiconductor devices. Wafer-scale integration of atomically controlled nanostructures is another main goal of Si-process technology which requires atomic scale control on step-terrace morphology at the wafer scale.[129,130] Self-assembly of step-terrace patterns with the ability to control the terrace width has become a necessity for atomically precise manufacturing needs to have nano-scale templates on which novel atomic structures can be built.[131,132] One common preparation process is wet chemical preparation plus annealing in UHV at high temperature to create silicon surfaces with atomically flat terraces and atomic steps, which can then be used for nano-lithography and nano-fabrication processes.

Although high temperature annealing is one of the methods to produce atomically flat terraces, this method could not provide surface with controlled step-terrace

morphology. As the formation of terraces by step dynamics at high temperatures is dictated by the energies of the surfaces and the miscut angle, there is almost no reproducibility reported in the step-terrace patterns obtained in such processes. Several parameters that play into the dynamics and evolution of atomic step patterns include: temperature[133], which gives mobility to the atoms, adsorption of Si atoms resulting from sublimation, and the influence of the electric field due to the voltage applied to drive the specimen heating current causing electro-migration of atoms. The mechanical surface stress due to sample clamping etc. has also been shown to influence the atomic step patterns on the sample.[134]

Fiducial Marks

It is possible to guide and control the self-organization of atomic scale steps by artificially patterning the surface with micro-scale patterns.[108, 135] These micro-scale patterns provide boundaries for atomic dynamic processes during high temperature processing; thus, ordered terraces can be formed within these patterns.

From a practical point of view, these micro-scale patterns are a central aspect of the sample and subsequent application since they serve as 2D references on surfaces. During the nanolithography process, it is very important to re-locate the lithographic patterns written on the surface using tools other than the STM where they were written. It is almost impossible to re-locate these patterns unless there are well organized co-ordinates on the sample. These fiducial marks (micro-scale patterns) are ideally suited for this purpose since they withstand high temperature processing and are still visible by optical microscopes. This is an important result of this thesis.

As shown in Figure 4.1, a photomask was designed and fabricated with 25 µm and 50 µm square patterns in two different orientations (regular square and 45 degree cross). After the patterns are transferred into the sample surface, the width of the trenches can be measured by an SEM. The average trench widths of the square patterns and 45 degree squares are 1.35 µm and 1.82 µm, respectively.

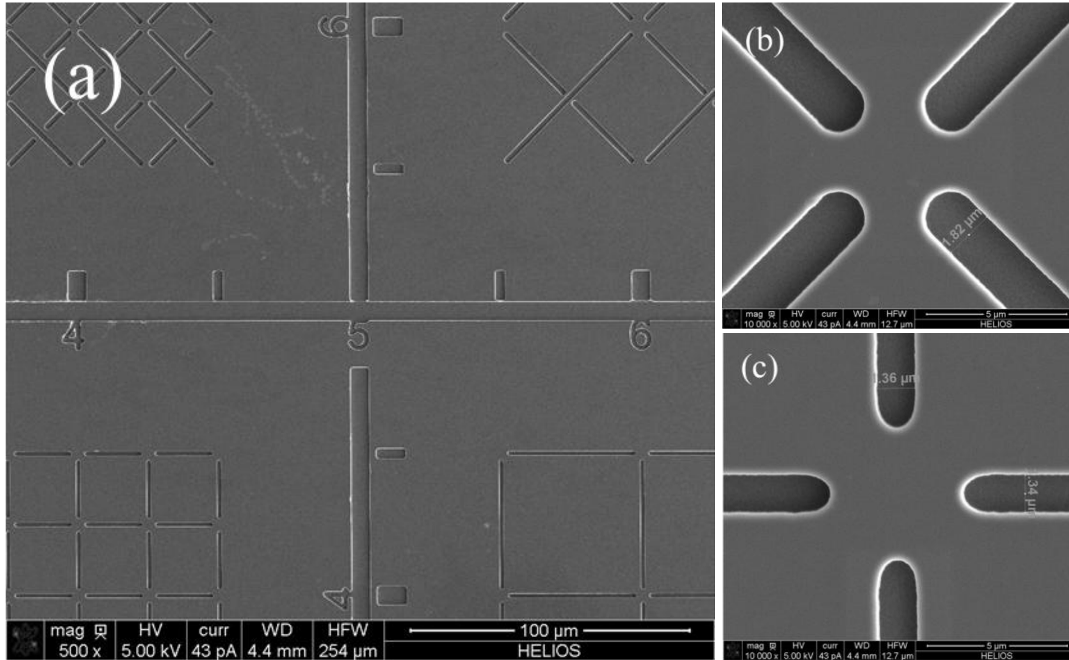


Figure 4.1: SEM images of the fiducial marks sample. (a) The overview of the surface; (b) a closer view of 25 µm cross (trench); (c) a closer view of 50 µm box (trench).

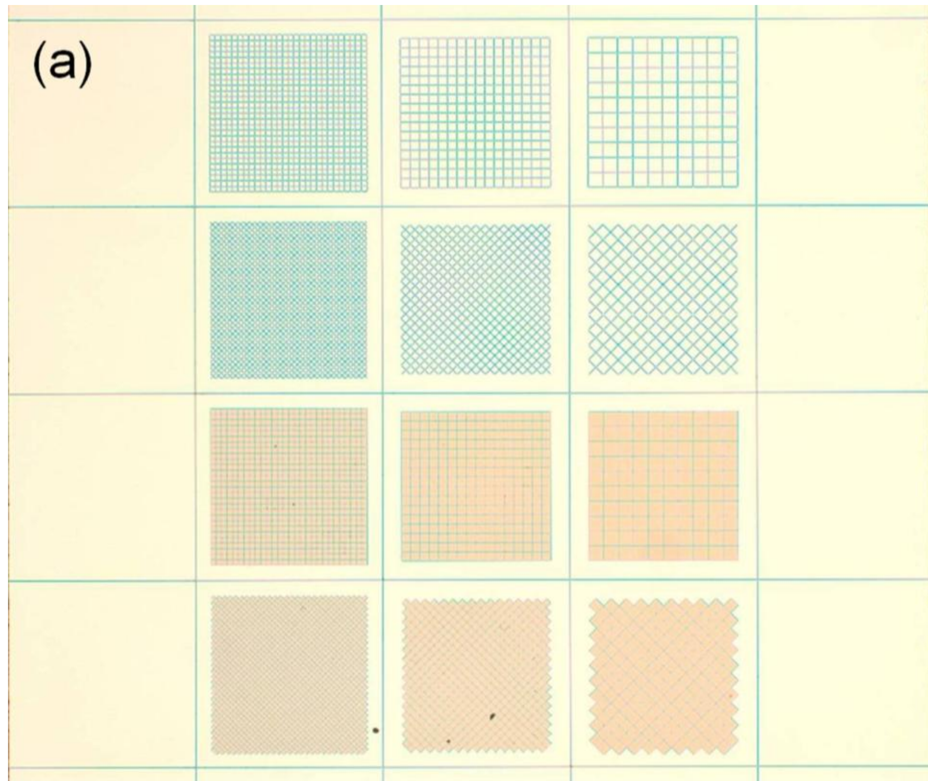
The work presented here describes the preparation of silicon surfaces via high temperature processing. This chapter is focused on the formation of reproducible step-terrace patterns by high temperature processing of Si (100) samples with microscopic etch patterns. During high temperature processing, silicon surfaces are known to display large mass transport due to sublimation, diffusion etc. Surfaces tend to evolve into steps and terraces. Atoms on the steps are more susceptible to thermal fluctuations and hence the step motion is a key to the nanostructure evolution. It is therefore necessary to find

the optimum parameters of annealing to produce atomically-ordered wide silicon surfaces.

4.2 Sample Preparation

Silicon wafers serve as the substrates for microelectronic devices and they undergo many process steps such as etching, deposition of various materials, and photolithographic patterning. In our experiments, silicon wafers were pre-patterned under the electron beam lithography process in order to create reproducible step-terrace patterns following high temperature annealing. Wafers were acquired from Virginia Semiconductor (http://www.virginiasemi.com), and the specifications are listed in the appendix A.

A photomask was designed and fabricated with 25 μm and 50 μm square patterns in two different orientations. The patterns were transferred on a boron doped P type Si (100) (±0.25’) substrate (0.01 ohm-cm to 0.02 ohm-cm) using a standard lithographic etching procedure. The resulting patterns contain two structures: one with plateaus separated by trenches; the other is the ‘reverse’ pattern, with flat areas separated by lines (walls). The dimensions of trenches and lines are about 1 μm in depth and height respectively, and about 2 μm wide as shown in Figure 4.2 (a). The samples are cut into rectangular pieces with dimensions 9×2.5 mm^2 and cleaned using chemical cleaning (modified RCA + Piranha) procedures before loading into the UHV chamber for high temperature annealing. The atomically flat reconstructed surface is formed after a procedure that includes flash heating and successive annealing. Figure 4.2 (b) shows an optical image of the sample with fiducial marks after the annealing process.



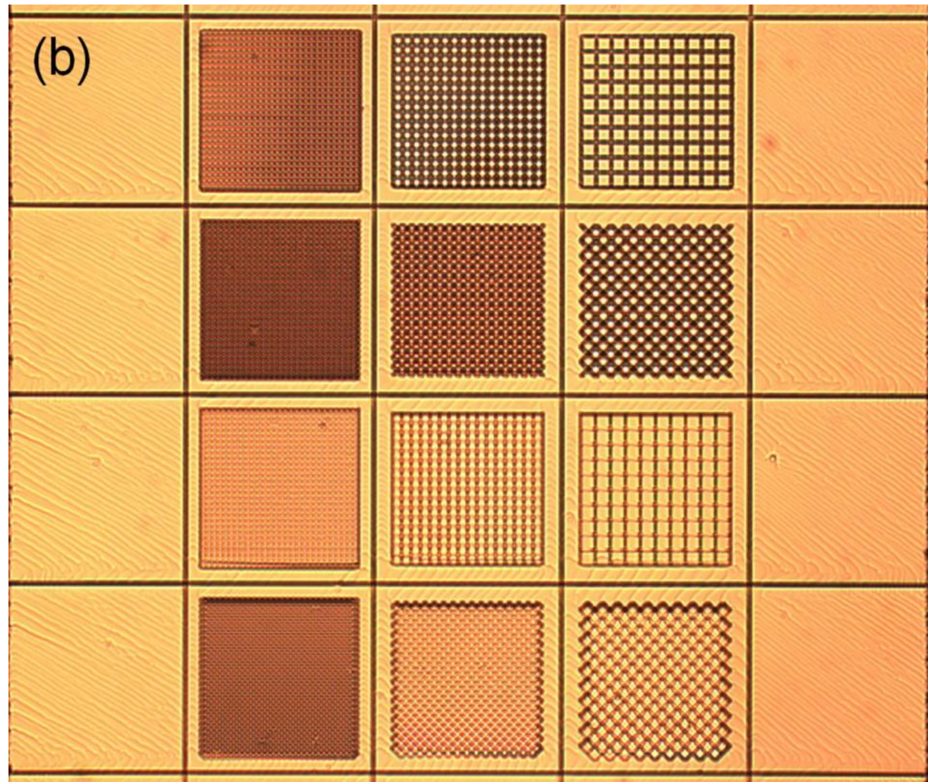


Figure 4.2: Optical images of Si sample with fiducial marks. (a) Before annealing, (b) After 24 hours annealing. The visible diagonal features on the outer cells on the left and the right are step bunches.

4.2.1 Silicon Sample Cleaning Procedure

A polished commercial silicon wafer has gone through many processes including melting, cutting, and polishing. It can contain small silicon fragments, trace metals, or even grease and sometimes even microscopic cracks or defects after having been cleaned and inspected by the manufacturer. In addition, the wafer surface may be covered by residual photo-resist material after the photolithography process. Therefore, it is necessary to meticulously clean silicon wafers before loading them into the UHV system for the annealing process.

The first step is to remove residual photo-resist, grease contamination etc. HPLC grade isopropanol is used here to dissolve those contaminants.

Cleaning Procedure:

Sample was rinsed with DI water (18.2 MΩ-cm resistivity) in an ultrasonic bath for 5 minutes. This was followed by a rinse in isopropanol in an ultrasonic bath for 10 minutes. The sample is then rinsed again using DI water in an ultrasonic bath for another 5 minutes.

A cleaning method developed by the Radio Corporation of America (RCA) in 1965 is widely used for silicon. The first part of this method (called SC-1, where SC stands for Standard Clean) is performed with 1:1:5 solution of NH_4OH (ammonium hydroxide) + H_2O_2 (hydrogen peroxide) + H_2O (DI water) at 75 or 80°C for 10 minutes. This treatment results in the formation of a thin silicon dioxide layer (about 1 nm) on the silicon surface, along with a certain degree of metallic contamination (notably Iron) that shall be removed in subsequent steps. This is followed by a DI water bath. The second step is a

short immersion in a 1:50 solution of HF (hydrogen fluoride) + H_2O at 25°C, in order to remove the thin oxide layer and some fraction of ionic contaminants. The third and last step (called SC-2) is performed with a 1:1:5 solution of HCl (hydrochloric acid) + H_2O_2 + H_2O at 75 or 80°C for 10 minutes. This treatment effectively removes the remaining traces of metallic (ionic) contaminants.

Aside from RCA cleaning, scientists have developed other methods such as the Caro clean, isopropyl alcohol (IPA) rinse, hydrofluoric acid (HF)/ammonium fluoride (NH_4F) clean, hydrochloric acid (HCl) clean, and combinations of the above methods for more effective cleaning.

The Piranha solution (a mixture of H_2SO_4 and H_2O_2) is used frequently in the microclectronics industry to clean photoresist residue from silicon wafers. The piranha solution is extremely effective in removing organic residues, especially carbohydrates. Also, because of the high acidity of sulfuric acid, the piranha solution can dissolve trace metals, metal oxides, and carbonates.

In a subsequent cleaning stage we combined both the Piranha cleaning with RCA cleaning in the following order.

1. Sample is immersed in a 2:1 solution of H_2SO_4 (concentrated sulfuric acid) and H_2O_2 (hydrogen peroxide) for 15 minutes.
2. Sample is rinsed with DI water in an ultrasonic bath for 5 minutes.
3. Sample is immersed in a 1:1:5 solution of NH_4OH (ammonium hydroxide) + H_2O_2 (hydrogen peroxide) + H_2O (DI water) at 75 or 80°C for 20 minutes.
4. Sample is rinsed with DI water in an ultrasonic bath for 5 minutes.
5. Sample is immersed in a 1:50 solution of HF (hydrogen fluoride) + H_2O at room

temperature for 5 minutes.

6. Sample is rinsed in DI water and blow dried with ultra-high purity nitrogen and loaded into the vacuum chamber.

Following the cleaning procedure, the sample is loaded into the vacuum system. Then we start the sample thermal annealing procedure.

4.2.2 Sample Annealing

The thermal annealing procedure is performed in an ultra-high-vacuum (UHV) environment where surface oxides can be dissociated and desorbed from the Si sample surface at 800 - 900°C. Moreover, contaminants diffuse into the bulk silicon and the sample surface reconstructs to a lower surface energy configuration. This process produces a flat, atomically ordered silicon (100) 2×1 reconstructed surface. This method requires a UHV environment with a pressure below 1×10^{-10} Torr. Experimental data show that the presence of Fe^{3+} and Ni^{2+} will induce a different kind of reconstruction and create defects on the sample surface.[77] Above 800°C, residual hydrocarbon can react with silicon and form silicon carbide (SiC), which will drastically increase surface roughness and change the surface morphology irreversibly.[74,76]

Procedure:

The annealing procedure was developed based on literature[76] and a series of experiments to optimize the parameters. We carried out elaborate experimental studies in order to optimize the parameters for samples with fiducial marks as there are only a few reports on similar topics. The following is a procedure that was developed in our

laboratory and was followed throughout for all the samples in all experiments presented in the thesis.

1. Sample is degassed by direct heating at ~ 650°C over 12 hours.
2. Sample is thermally flashed from 600°C to 1250°C. The temperature is lowered if the pressure inside the vacuum chamber exceeds 1×10^{-9} Torr. The procedure is repeated until the sample can be maintained at 1250°C over 30 seconds.
3. Sample is cooled rapidly from 1250°C to 1030°C in few seconds.
4. Sample is annealed at 1030°C for 24 hours.
5. The temperature is reduced rapidly from 1030°C to 900°C, and cooled down to room temperature at a rate of approximately 2 °C/sec.
6. After annealing, the sample is transferred into the STM to assess the surface reconstruction.

The sample temperature is measured with an infrared pyrometer (Minolta Cyclops 153) with an uncertainty of 30°C.

4.3 Results and Discussion

The summary analysis of the surface is accomplished with an ambient AFM, and detailed surface examination at the atomic scale is performed with our Omicron STM.

4.3.1 Evaluation of Surface Morphology after Annealing Using AFM

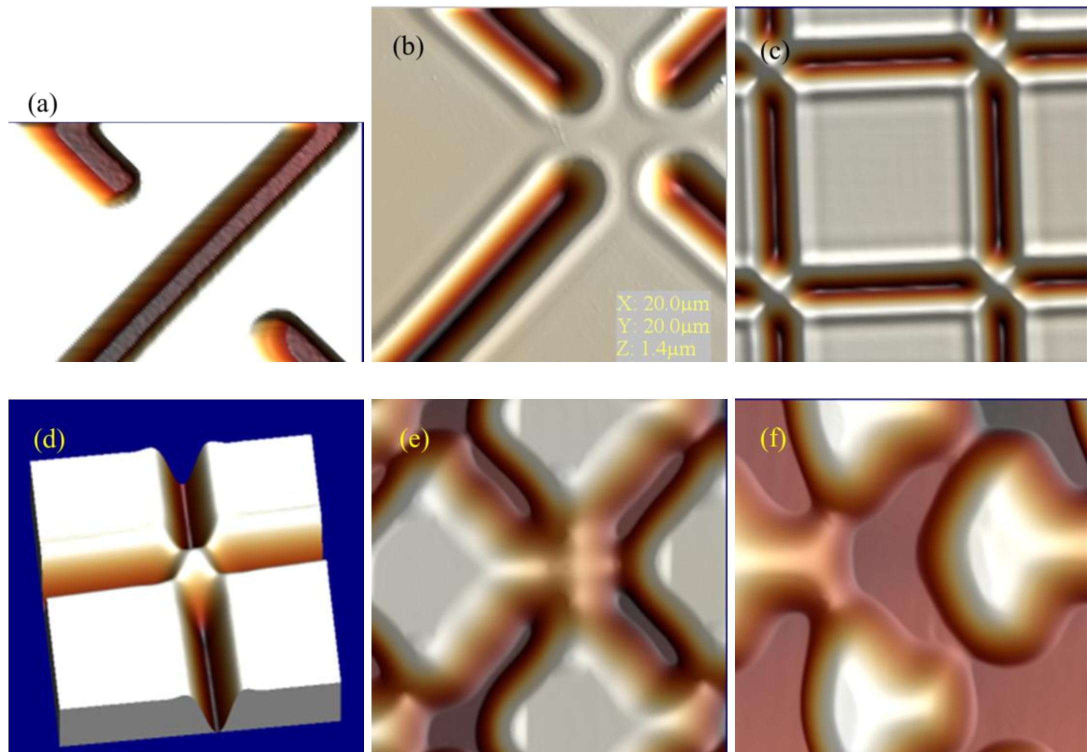
For samples with fiducial marks, the preparation procedure has been optimized by systematically varying the annealing temperature and duration (4 hours – 18 hours) after

the initial 1200°C flash heating. The samples were then examined *ex situ* using an intermittent-contact-mode ambient atomic force microscope (AFM) (Veeco Metrology) in a controlled temperature (21.0°C ± 0.1°C), humidity (45% ± 5%), and clean air (class 1000) environment. The samples were stored in a controlled environment while being transported from the UHV facility to the ambient AFM.

Figure 4.3 shows the change of depth of the trenches (fiducial marks) on the 25 μm patterns after the high temperature process. Figures 4.3 (a)-(f) show the change of the surface morphology, and the plot in Figure 4.3 (g) shows the accumulated heating effect. First, the sample was flashed at 1250°C for 10 to 15 seconds to remove oxide and other attachments. The flashing process was repeated three times for 15 seconds and 25 seconds, respectively. Finally, the sample was annealed at 1050°C for 6 hours and 24 hours, respectively. Even after 24 hours annealing, one could clearly recognize the fiducial marks clearly (Figure 4.2 (b)).

For the fiducial marks with lines, the features survive 48 hours of 1030°C annealing. As shown in Figure 4.4, the patterns separated with lines evolved into a nearly identical step-terrace structure after annealing.

During the flashing and annealing stages, the depth of trenches was significantly reduced from 1 μm to few hundred nanometers (as shown in Figure 4.3 (g)), which indicates a large mass transport during the high temperature process. After a careful examination of the surface morphology following a simple flash, versus a flash followed by prolonged annealing, we suggest two different mass transport mechanisms as directly resulting from the heating procedure.



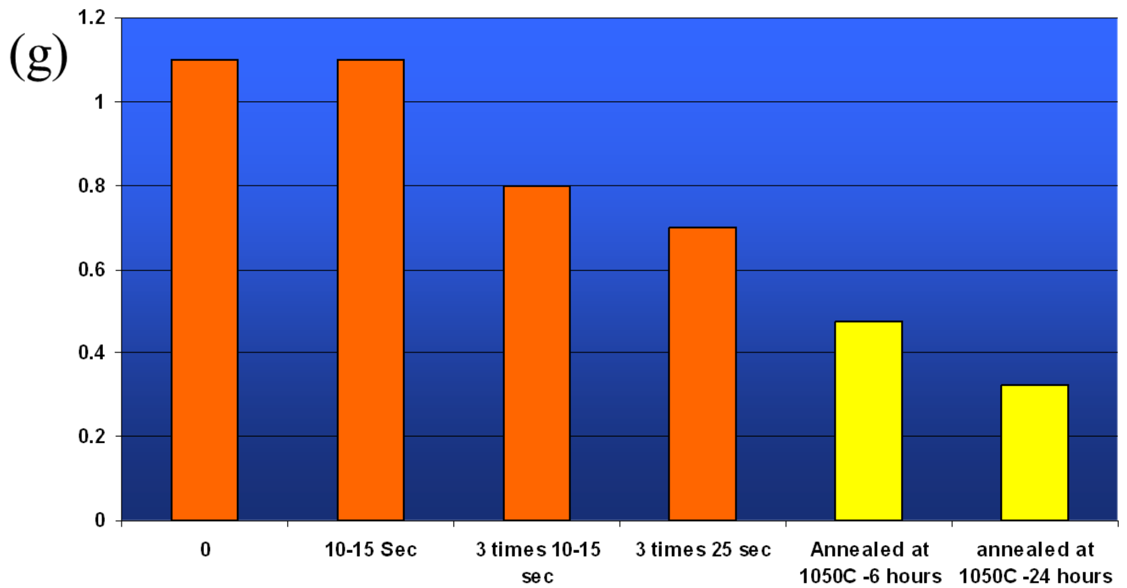


Figure 4.3: Sequence of the evolution of the depth of the fiducial marks under different annealing conditions. AFM images show the deforming of fiducial marks. (a) Initial structure of fiducial marks; (b) after 10 seconds flashing at 1250°C; (c) after 3 times 10 - 15 seconds flashing at 1250°C; (d) after 3 times 25 seconds flashing at 1250°C; (e) after 6 hours annealing at 1050°C; (f) after 24 hours annealing at 1050°C. (g) The average depth of fiducial marks measured by AFM at each condition shown above, unit in μm.

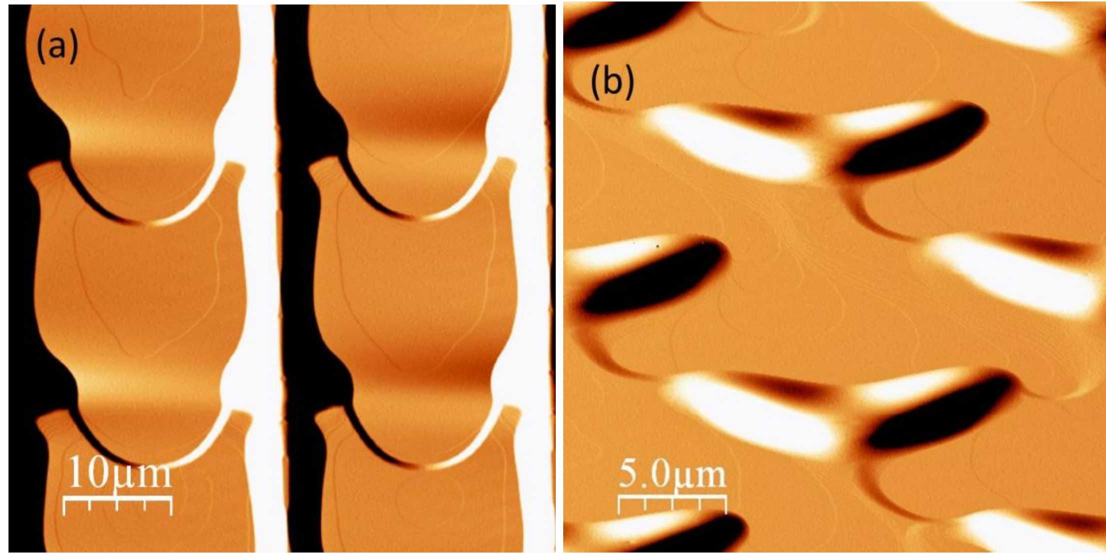


Figure 4.4: AFM images of post-annealing reversed patterns (lines), (a) 25 μm square patterns with identical step-terrace structures and (b) 25 μm cross patterns.

During the flashing stage, the decrease in the trench depth is due to sublimation effects. The area within the patterns has transformed into a symmetric formation of step-terrace patterns. The step-terrace morphology is very repeatable across various cells in the patterned area. The morphology achieved is an outcome of the kinetics that drives the surface to a minimum surface-energy configuration.[136] (As shown in Figure 4.5 (b))

On the other hand, the surface morphology is totally different after extended annealing (Figure 4.5 (e)), and the resulting decrease of trenches is caused by the adatoms filled into trenches. The driving force of those adatoms is the electromigration force due to the electric current used to resistively heat the sample. For short annealing times, on the order of minutes, the effect of electromigration is not very prominent; however, the effect becomes substantial with extended annealing times of several hours. In this case, the adatoms are supplied from the step edges of the lower terrace and the wide terraces tend to broaden further[137], and the growth of those terraces could be very similar to the step flow growth.

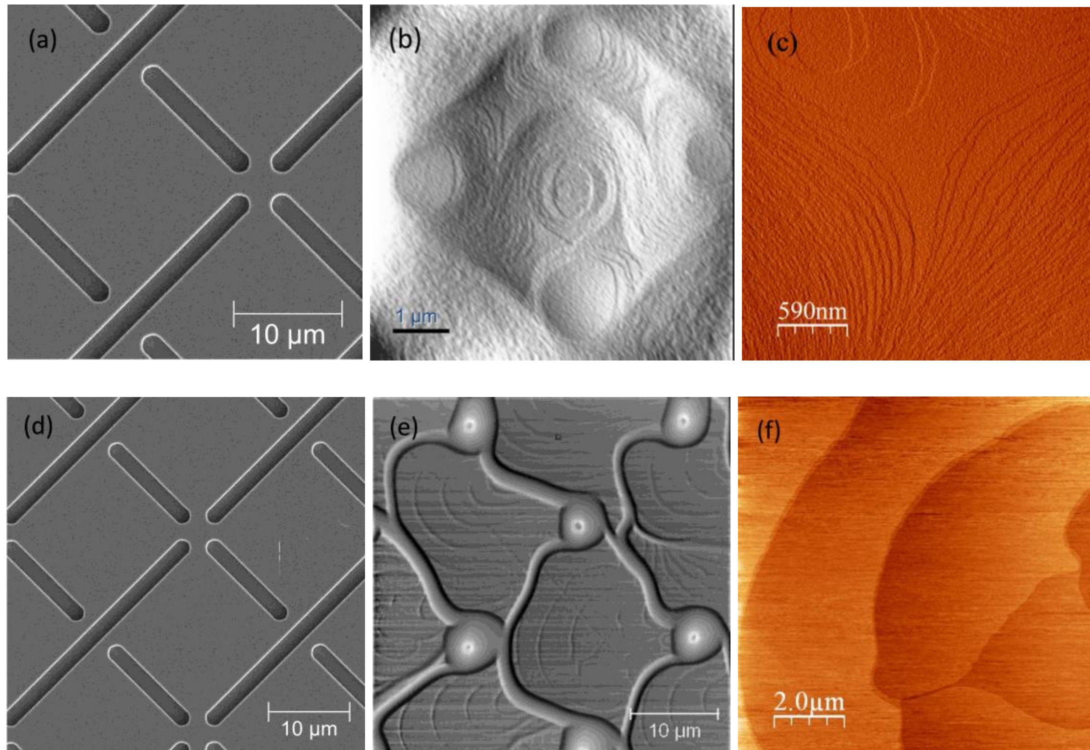


Figure 4.5: High temperature process of two samples with same 25 μm cross trench patterns. (a) and (d) are the SEM micrographs of two samples before annealing. The rest of the images were taken by an AFM; (b) surface morphology within a 25 μm cross after 3 times 10 - 15 seconds flashing at 1250°C; (c) shows mound and pit structures were formed after flash anneal; (e) is the surface morphology after 18 hours anneal. In comparison with (c), (f) shows large flat terraces formed within those boxes.

A series of experiments has been carried out to understand the effect of the electromigration on samples with fiducial marks where the sample has been subjected to the annealing process. After six hours of annealing, the sample was taken out and examined by an AFM to record the surface topography. The sample was subjected to another 18 hours anneal, followed by an AFM re-examination of the surface, and images are shown in Figure 4.6.

Figure 4.6 shows the time effect evolution of the trenches during growth. During the annealing process, the silicon material flows into trenches from plateaus, which “feeds” the trenches and reduces the trench height. In the meantime, the lateral size of the plateaus decreases. After a 6 hour anneal, flat terraces with step pairings[138,139] formed on

plateaus as well as on the bottom of trenches. After a 24 hour anneal, trenches which contain large atomically flat terraces become the dominant patterns on the surface, while the plateaus shrink or even disappeared in the 25 µm cross patterns. Step pairing is seen within the trenches. As for the fiducial marks with lines, large atomically flat terraces are found to form only at the base of the trenches (shown in Figure 4.4 (a)). Within this area, one can easily recognize large flat terraces; some of them could be as wide as 10 µm.

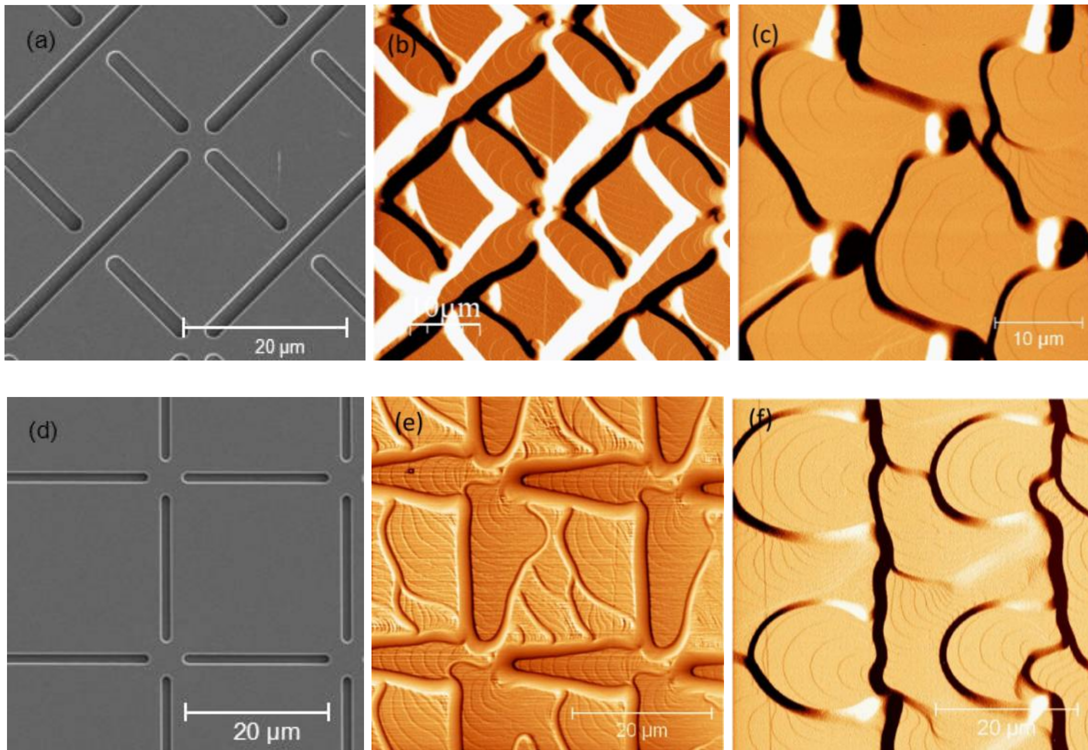


Figure 4.6: Evolution of the surface morphology under the influence of electromigration. (a) SEM micrograph of the 25 µm cross patterns, (b) and (c) are corresponding AFM images after 6 and 18 hours annealing, respectively. (d) SEM micrograph of the 25 µm square patterns, (e) and (f) are corresponding AFM images after 6 and 24 hours annealing, respectively.

We have been able to obtain large atomically flat terraces that are created on samples with fiducial marks by using a high temperature annealing process. We have also observed that it is possible to control the step and terrace patterns by optimizing the size

and shape of individual cells created by the fiducial marks. These identical atomically flat terraces are ideal templates for nanolithography.

We have found that the size of the pre-set patterns is another important parameter in the evolution of then surface morphology. Post annealing analysis (Figure 4.4 and 4.6) shows that the trenches and lines act as pinning sites and boundaries during the surface evolution. With increased size of cells beyond a threshold, the boundary conditions are observed not to be effective in organizing the step-terrace patterns. When the pattern size increases to 50 μm, the terraces become irregular (as shown in Figure 4.7 (a)) compare with the terraces in 25 μm patterns (Figure 4.6(c)). Although the surface formed large atomically flat terraces separated by step bunches due to electromigration, the shape of the terraces becomes irregular, and the surface structure looks similar to the area without fiducial marks (Figure 4.7(b)). This indicates that the fiducial marks become less effective in constraining the sample to small enough areas that create very similar step-terrace patterns.

We have observed that fiducial marks with smaller cells often disappear after the high temperature process. Elain *et al.*[140] studied the decay of individual 3 μm box shape structures after flashing. The decay rate of the structure at 1150°C - 1200°C is approximately one layer per second. Nakamura *et al.*[107] investigated the evolution of those lines (walls) with different pitch values annealed at 1100°C. The evolution of the surface morphology relies more on the mass transport mechanism than sublimation. Also, the collapse time of gratings will significantly increase with grating period. In our experiment, the 15 μm patterns lines partially disappeared after 24 hours anneal.

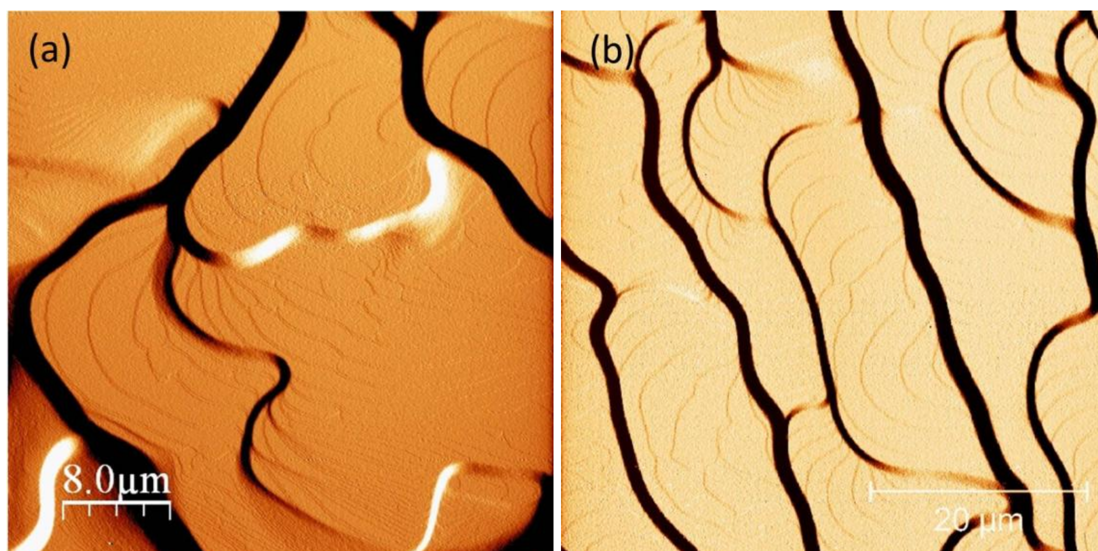


Figure 4.7: AFM images of (a) 50 µm cross patterns with trenches, and (b) step-terrace structures outside the fiducial marks after 24 hours annealing. In image (a), several step bunches formed within the cross box, which roughen the surface.

4.3.2 Evaluation of Surface Morphology after Annealing Using STM

After the annealing process sample surfaces can be quickly examined using LEED. A typical pattern corresponding to a 2×1 reconstructed surface is shown in Figure 4.8. The surface is further analyzed using STM. The surface atoms form 2×1 and 1×2 alternating dimers to reduce the number of dangling bonds, and the sequence of those dimers form orthogonal dimer rows on terraces.[139] The 2×1 dimer rows that are parallel to the step edges (S_A step) form the terraces T_A, and 1×2 dimer rows which are perpendicular to the step edges (S_B step) form the terraces T_B.

Defect density and the topography of reconstructed surface are two critical factors that determine the quality of the Si (100) reconstructed surface. The defects on dimer rows can directly affect the hydrogen passivation and depassivation process. Dimer row defects can be caused either by surface atom sublimation or contamination. Increasing the annealing time[72] and/or decreasing the cooling rate has been reported to reduce the defect

density on Si (100). As shown in Figure 4.9 (b), a lower surface defect density can be achieved by increasing the annealing time.

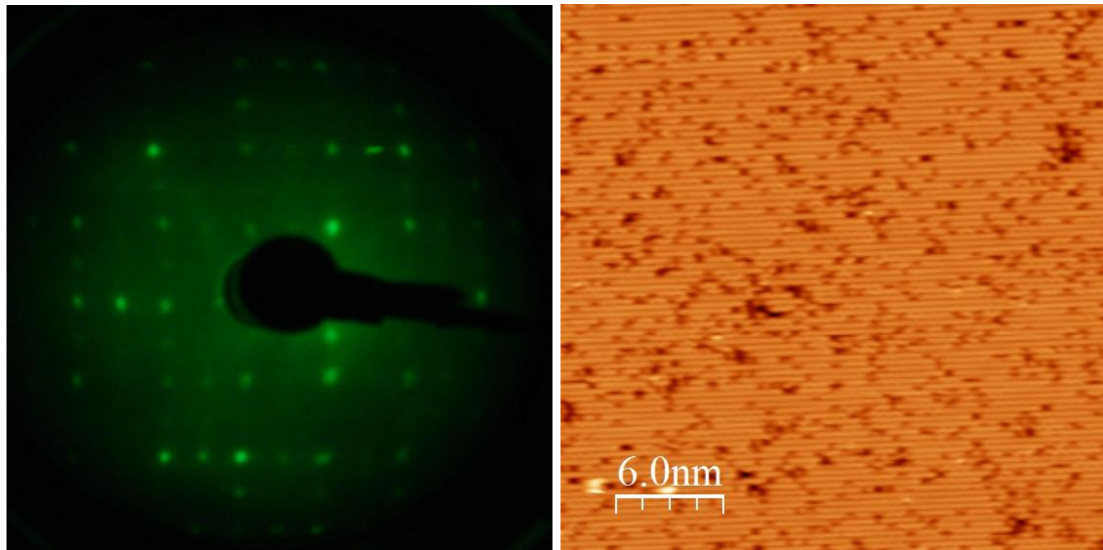


Figure 4.8: LEED pattern (left) and corresponding STM image (right) of the p-doped Si (100) sample.

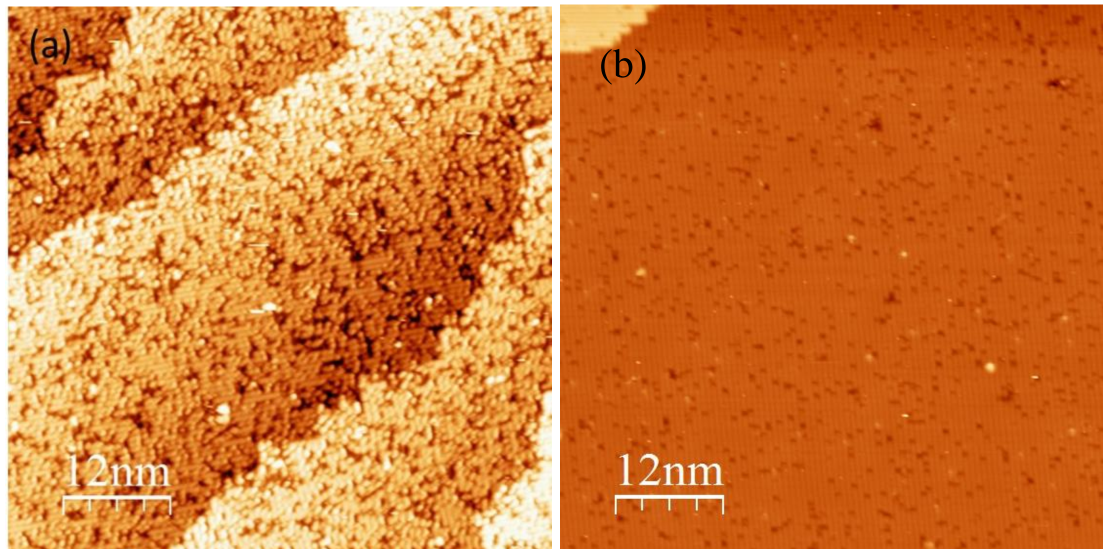


Figure 4.9: Si (100)-2×1 surface: (a) surface contains lots of defects after flashing process then cold down to room temperature; (b) defect density reduced after increase annealing time to 24 hours.

Surface topography on the micrometer scale is yet another critical factor that determines the suitability of a sample for atomic scale manufacturing. Although this does not directly affect the nanofabrication process locally, it becomes critically important if

one has to fabricate several such patterns over an extended area. Figure 4.10 shows two types of typical surface topography on the sample surfaces with fiducial marks, step pairing and step bunches, after high temperature processing.

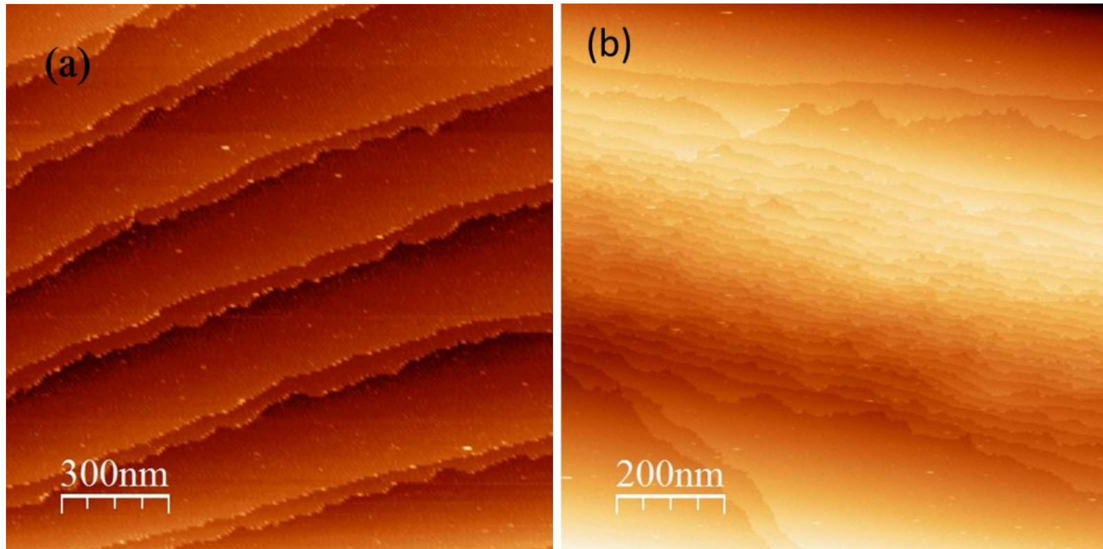


Figure 4.10: Si (100) surface topography. (a) Step pairing and (b) step bunching.

Previous studies have also demonstrated the possibility of producing step-free terraces up to several tens of microns by annealing patterned surfaces with micrometer scale features.[108] In comparison to the work by Tanaka *et al.*[108] our work is centered around preparing templates to realize the two essential requirements for building atomically-precise structures, namely, (1) the ability to control the step-terrace patterns at the atomic-scale and (2) the need to re-locate these structures /patterns in tools other than those used to fabricate them. The samples need to have dimensionally stable fiducial marks that can withstand high temperature UHV processing and should be optically visible after transferring to other measurement tools. The fiducial marks (prepared for re-location of the nanofabrication site) worked to our advantage also in organizing the step terrace patterns on the surface. Although it is not our main experimental goal, we have

obtained nominally 13 micrometers of step free terrace. However, the experimental efforts presented in the thesis are focused more on engineering steps and terraces in each cell defined by the fiducial marks to enable nearly identical patterns.

The ability to produce repeatable, large terrace patterns over the entire wafer in the presence of fiducial marks while maintaining the ability to control the terrace width presents new possibilities to meet atomically precise manufacturing needs.[111]

Surface Contamination

The sample goes through multiple annealing steps during the entire process. To get a high quality clean surface with fewer defects or vacancies, one needs to make sure that the vacuum level is better than 1×10^{-10} Torr. During the first instance of flash heating (1200°C), the pressure can increase to as high as 1×10^{-8} Torr due to the outgassing of various gas species into the chamber. At temperatures around 900°C, hydrocarbons can react with surface silicon atoms and form large pyramidal shaped SiC structures which will substantially increase the surface roughness in the micrometer size range (as shown in Figure 4.11 (a)). An RGA is used to detect those trace materials and monitor the partial pressure of them. Extreme precaution is taken to reduce the chance of system and sample contamination.

Another pontential contamination is nickel, which is a constituent of stainless steel. Usually it is a consequence of contacting the sample with stainless steel or of thermal diffusion of nickel from the sample holder to the sample surface during a annealing. A small amount of Ni contamination drastically changes the Si (100) reconstructed structure and creates split-off dimers (as shown in Figure 4.11 (b)).[141] After annealing, it produces

the 2×n reconstructed structure. Teflon tweezers must be used to handle silicon samples. In addition, the sample holder needs to be dissembled and cleaned in order to remove the deposited materials after it has been used every two or three times.

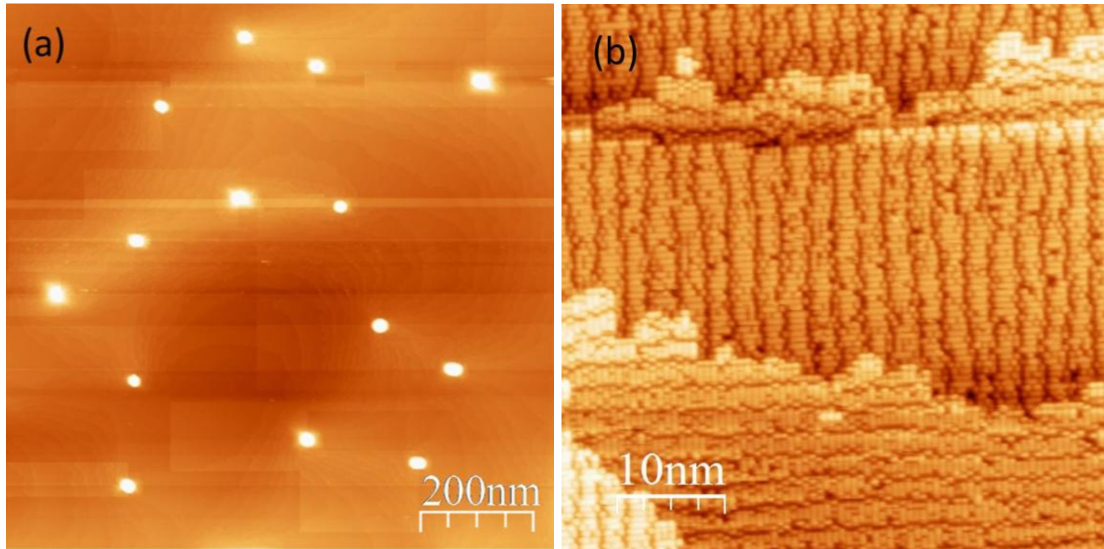


Figure 4.11: Si (100) surface morphology with varies contaminates. (a) Silicon surface with SiC (big bright dots); (b) Ni induced Si (100) reconstruction surface. After contaminated by Ni, 2×n reconstructed structure formed.

Effect of Bad Tips

Besides contamination that causes surface problems, STM tips can affect the quality of the images by providing false signals. For example, when the tunneling junction becomes unstable, the image resolution is compromised considerably. In some cases, two tunneling junctions can be active simultaneously, which is referred to as a “double tip”. Figure 4.12 is an extreme example of a “double tip” image. All the features near step edges, such as S_A and S_B steps, dimer rows and surface defects, have been doubled.

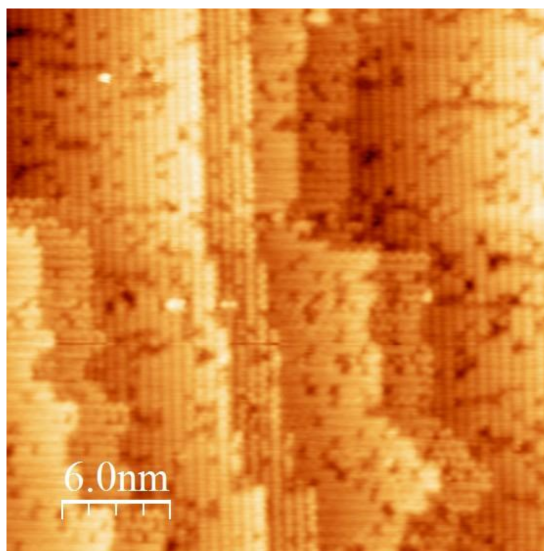


Figure 4.12: Si (100)-2×1 surface image under a “double tip”.

4.4 Summary

The custom designed fiducial marks (microscale patterns) have been fabricated on Si (100) wafers using the E-beam lithography process. AFM data showed that the fiducial marks survived after the high temperature process, and the average height of the fiducial marks reduced 200 to 300 nm in one minute 1200°C flashing. The height of the fiducial marks reduced another 400 to 500 nm in the following 24 hours 1050°C annealing. The fiducial marks are visible using a conventional optical microscope and can help to relocate nanoscale features fabricated on the atomically flat terraces.

During the prolonged annealing process, the evolution of the surface morphology is dominated by the electromigration effect caused by the direct-current resistive heating. By engineering the size of fiducial marks, nearly identical, large atomically flat, terraces separated by the fiducial marks are formed on the surface. To be able to control the

surface morphology and get the ideal template for nanofabrication, the pattern size should be 20 - 40 μm, and the depth needs to be at least 1 μm.

Chapter 5: Control of Surface Morphology: A Kinetic Monte-Carlo Simulation

The remarkable evolution of the Si (100) surface morphology at high annealing temperatures was observed using AFM as described in the previous chapter. With the presence of fiducial marks, the surface morphology is dramatically changed in comparison to those without fiducial marks. Over time, we have learned to control the evolution of step and terrace patterns by varying the geometries and the dimensions of the fiducial marks. In fact, nearly identical patterns with large (several microns) atomic flat terraces have been fabricated in our experiments.[111] The wide atomic flat terraces with fiducial marks are very important for nanopatterning and pattern location in the APM project.

To enable use as substrates for APM and future nanofabrication, it is necessary to engineer the fiducial marks to fabricate various patterns with distinct features which can be recognized by other instruments, such as an optical microscope or AFM. There are a multitude of parameters that determine the evolution of the step and terrace patterns, such as the geometry and dimension of the fiducial marks, etch depth of the lines and the trenches, and the annealing temperature and duration. A systematic experimental variation of these parameters to optimize the process parameters for the desired end result would be extremely time-consuming. To gain a better understanding of the sample surface morphology evolution after high temperature annealing in the presence of various

fiducial marks, it is essential to construct a model that can represent and simulate the experimental conditions.

In this chapter, a kinetic Monte Carlo (KMC) simulation has been developed using a solid-on-solid (SOS) model to represent the evolution of the surface with and without the fiducial marks. We then develop and discuss a quantitative explanation of the surface morphology. The simulation will help us to further our understanding of the surface evolution after high temperature processing. The data indicate that in the future we will be able to develop advanced fiducial marks which can evolve to more favorable patterns for the APM project and ABDM project.

5.1 Evolution of Si (100) Surface Morphology

At the microscale, crystalline silicon surfaces exhibit two distinct structures: a smooth or flat surface and a rough surface. At low temperature, silicon surface atoms are perfectly aligned in a smooth (atomically flat) plane. When the temperature exceeds a critical temperature T_R, which is known as the roughening transition temperature, the step free energy per length vanished and the surface roughens, crystalline surfaces become rough and undergo a roughening transition.[142,143] Above the roughening temperature, the surface fluctuates strongly and the notion of a crystalline plane becomes difficult to define. The transition is very gradual, so that locating T_R from images is not possible.

On a real crystal surface, due to the miscut angle, the surface cannot be maintained atomically flat over long distances and consequently a stepped surface is formed, which is also known as a vicinal surface. The boundaries between the terraces are steps. Such steps play an important role in allowing growth and sublimation processes to occur at

very small supersaturations.[144] The step density is related to the miscut angle, which is normally <0.5° in the experiments (detailed information on Si (100) wafers can be found in appendix A). During the manufacturing process, high step densities may occur during growth or as a result of nanofabrication processes, like the fiducial marks in our experiments.

Figure 5.1 shows the movement of adatoms on the surface. At zero temperature, all atoms are bound on the surface and form atomically flat planes. When the temperature rises, some of them detach from step edges, thus forming adatoms on the surface. A kink site is formed on the step edge during the detachment process. Kink sites are the corner sites on a non-straight single step, and they can also be created by cutting the surface with an azimuthal miscut angle. These adatoms can move on the surface and form different structures with different mass transport mechanisms. An adatom can diffuse from one site to another. Or it can attach to a step or cross over it. When two adatoms meet, they can potentially form a nucleus, which may either grow to a stable two-dimensional island by attachment of further diffusing adatoms or decay by detachment of atoms. Adatom evaporation may happen at high temperature, and condensation/deposition is possible in some processes such as molecular beam epitaxy (MBE) and chemical vapor deposition (CVD).

To be able to understand the evolution of silicon surface morphology, it is necessary to choose an appropriate approach to investigate the surface morphology. There are different levels of approach: microscopic, mesoscopic, and continuum approaches. Different theoretical models can be used for the study of the surface properties and evolution. The microscopic approach, such as molecular dynamics (MD) or kinetic

Monte Carlo (KMC), is focused on each possible atomic configuration on the surface. In this regime, structural evolution involves collective behavior strongly influenced by finite-size effects occurring at the atomic scale. The movements of single atoms can be combined to form some continuum phenomena, such as mass transport, surface evolution, etc. Therefore, it is possible to understand and predict such large structural changes after combining atomic scale transport behaviors.

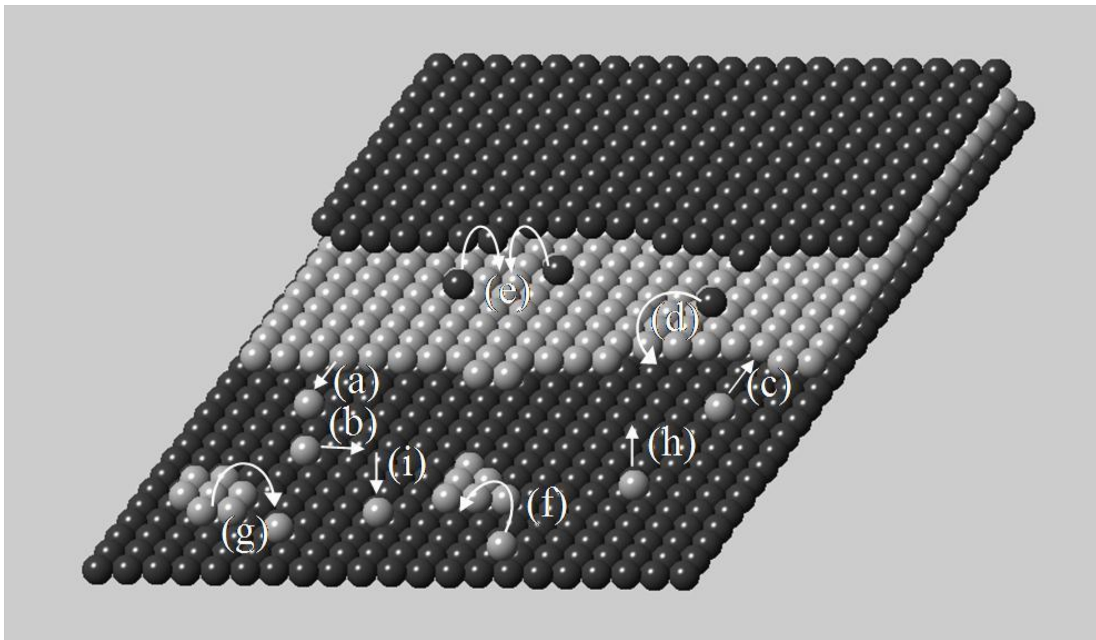


Figure 5.1: Schematic representation of different adatoms moving mechanism: an adatom can (a) form from a step, (b) diffuse on the terrace, (c) attach to a step, (d) cross over a step, (e) form a nucleus with another adatom, (f) attach to an island, (g) detach from an island, (h) evaporate from the surface, and (i) been deposited on the surface.

A major challenge of the microscopic approach is to describe every aspect of atomic motion with microscopic energies to fit with a real surface. A full and accurate understanding of all the relevant atomic interactions with steps remains a challenge. It requires a large computational effort to interpret and predict the large scale evolution of structures in a macroscopic system. Nonetheless, this approach is widely used and is a powerful source of physical insight.[145,146]

A mesoscopic approach, which is known as the "continuum step model", has been proven to be a very powerful approach.[147] Indeed, evolution of surface morphology can be recognized by the motion of the steps, which is implicitly connected to the atomic motion via the attachment and detachment of atoms at the edges of the steps. The motion of a step can be considered as a consequence of interactions between surface atoms, steps, and terraces; and the result of the step motions causes the evolution of the surface morphology from a macroscopic point of view.

The continuum approach has been a third powerful tool to describe the large scale evolution of the surface, especially above the roughening transition temperature. Instead of treating individual atomic configurations, this approach uses the surface slope or the step density as a variable. Hence, the continuum surface approach is not adequate for describing surface morphology in detail below the roughening temperature.

During high temperature annealing, the Si (111) surface undergoes mass transfer, and step pairing[148] and step bunching[149] appear on the surface. Step pairing and step bunching are current-induced instabilities during the evolution of surface during a resistive heating. Latyshev *et al.*[149] first recognized and quantified this effect on Si (111) in 1989. After resistively heating a Si (111) surface with small miscut angle (<1°), they observed the transition between closely packed step bunches and a uniform step train under different heating temperatures. In the case of step-up direction of DC current, step bunching occurs in the ranges 1050°C - 1200°C and >1320°C. In the case of step-down current direction, bunching occurs in temperature range 850°C - 1000°C and 1200°C - 1300°C (see Figure 5.2).

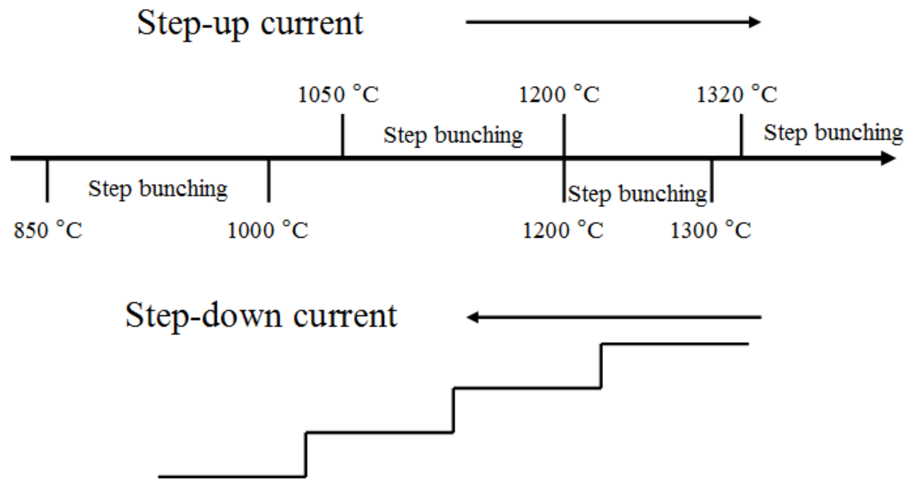


Figure 5.2: current-induced step bunching formation on Si (111) surfaces under different temperature ranges.

Although there are many interesting phenomena related to the Si (111) surface as well as many theoretical explanations about them, our experiments are focused on the Si (100) surface. Not only is the Si (100) surface technologically much more important in microelectronic device fabrication, but also its unique 2×1 dimer row reconstruction could be used in dimensional metrology as the fundamental "atomic ruler".

On the Si (100) surface, similar current-induced effects were found during resistive heating of the sample.[150] Later, a comprehensive investigation on Si (100) has been provided by T. Doi *et al.*[151] by using the reflection electron microscope (REM). The studies indicated that there are two domains with 2×1 and 1×2 dimer rows on the Si (100) surface. The direction of the heating current dictates the dominant terrace, either 2×1 terrace T_A (with a step-up current) or a 1×2 terrace T_B (with a step-down current). When the heating temperature is lower than 900°C, step pairing occurs for both step-up and step-down current direction. At temperature between 900°C and 1000°C, the steps accumulate and step bunches are formed on the surface. It is also shown that the width of

the majority domain becomes narrow due to the evaporation of Si atoms at temperature between 1000°C and 1100°C. At temperatures above 1150°C, mosaic domains are formed on the surface due to the evaporation of Si atoms.

There is much theoretical work regarding the domain conversion mechanism and step bunching formation. Stoyanov[152] first used the theory of Burton, Cabrera and Frank (BCF)[144] to explain the domain conversion phenomena in terms of two combined effects: the anisotropic diffusion rate of atoms on different domains and the effect of electromigration.[153] Silicon atoms were deposited[154] to analyze Si atom diffusion on the (100) surface. The experiments revealed that the adatom diffusion on the (100) surface along the direction of dimer rows is much faster than perpendicular to them. Other experiments[155,156] performed at elevated temperature showed that the diffusing species on the Si (100) surface is more likely to be an addimer, STM experiments clearly recorded the diffusion of Si surface addimers.[157] The anisotropic diffusion process has been observed through atom-tracking STM at temperatures of 128°C. Theoretical simulations[158,159] based on adatoms also confirmed the anisotropic diffusion effect.

The other effect is the electromigration effect. When a crystal is subjected to electric current, surface atoms drift due to the fact that either atoms carry a real charge (and so experience a force from the applied field) and/or they are pushed by transferred momentum from the charge carriers in the metal or semiconductor to the mobile atoms. This phenomenon is called electromigration. During thermal annealing, Si adatoms or addimers acquire a net charge and their motion is affected by the electric field which is applied across the sample.[153]

Besides those two effects mentioned above, many other transfer mechanisms, such

as adatom-step interaction and step-step interaction, can also affect the surface morphology. In some cases, atom evaporation or condensation needs to be taken into account to interpret the surface evolution. Some of these mechanisms will be introduced into the simulation program, and the effects of them will be discussed later.

5.2 KMC Simulation of the Evolution of Si (100) Surface Morphology

Before introducing the simulation model, I would like to quickly review our experimental observations of the evolution of the Si (100) surface. After a prolonged high temperature annealing process, identical micrometer sized atomically flat terraces are formed within the patterned fiducial marks area (as shown in Figure 4.6). Comparing with the regular Si (100) sample surface, it was concluded that the surface evolution is constrained within the boundaries defined by the pre-fabricated etch patterns. Due to the effect of electromigration, nearly identical atomic step-terrace patterns can be obtained across the large-scale cells defined by the fiducial marks (as shown in Figure 4.4).

In Figures 4.6 (c) and (f), C-shape patterns are formed on the surface. Under high magnification imaging of one of those patterns using STM, large atomically flat terraces can be recognized in Figure 5.3. The majority domain is covered with 2×1 dimer rows. Step pairing is clearly seen in the images shown in Figure 5.3. Small vacancy islands can also be seen on the flat terraces, which indicates that sublimation of Si atoms is also occurring during the annealing process. The growth of patterns within the fiducial marks (as shown in Figure 4.6) suggests a possible growth mechanism similar to step-flow growth. The important finding is that the shape of the step–terrace patterns is defined by the pattern and structure of fiducial marks.

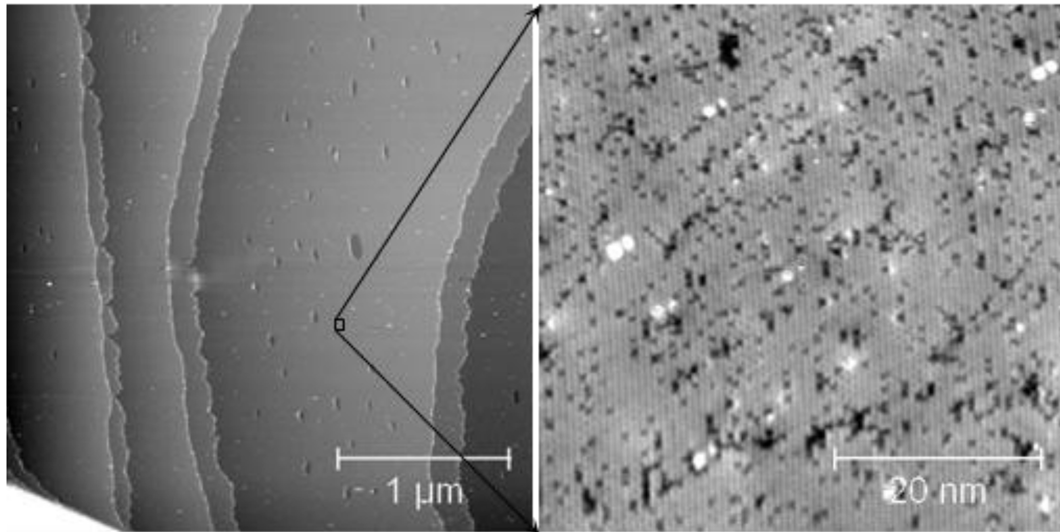


Figure 5.3: High resolution image of the samples acquired using STM. (a) shows a large area scan with coupling of adjacent steps. (b) is an atomic resolution image taken on a 50x50 nm^2 area shown in (a).

5.2.1 Surface Structure Representation

To be able to represent the surface morphology accurately, a well-thought-out comprehensive model needs to be established in the beginning. As was mentioned before, two types of models can be used here: a simple atomic model (solid-on-solid (SOS) model) and a step continuum model. Although the step continuum model has proved to be a very powerful model, it may not be suitable in our particular case. Since the fiducial marks on the surface constitute a very high step density at the etched part of the surface, it becomes very complicated to set up the initial conditions. Moreover, this method requires information such as step flow rates, which are difficult to measure from the experiments.

The simulation program in this thesis is similar to that of Sato.[160] An SOS model has been built in the KMC simulation algorithm. Details of the initial condition of the model and some key algorithms are discussed below. The Matlab code used for the simulation

itself is listed in the appendix B for reference.

Solid-on-Solid (SOS) Model

Silicon has an fcc atomic structure with (100) surface atoms packed in a square shape. On the (100) surface, an adatom has 4 nearest neighbors. When diffusion occurs, an atom can diffuse on the surface in four directions. Hence, it is very natural and convenient to create a square lattice SOS model to perform the simulation.

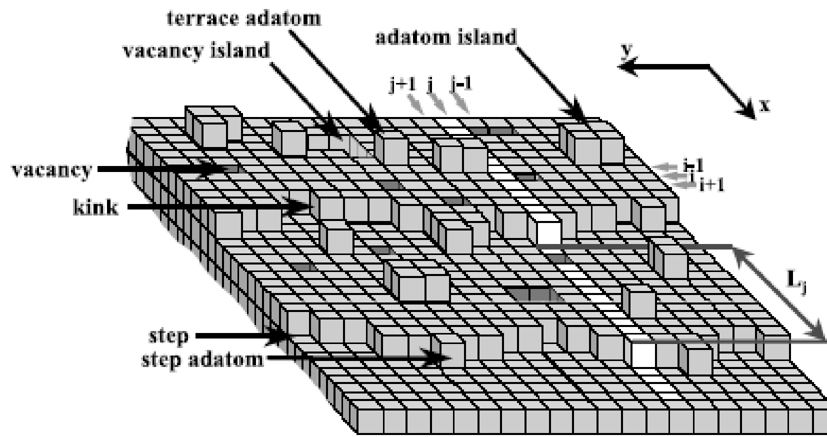


Figure 5.4: A schematic picture of the surface structure in SOS model. (From M. Giesen[161])

In the SOS model (as shown in Figure 5.4), the surface is represented by a square lattice of positions (x_i, y_j) spanned in the *x*-*y* plane, with atoms in lattice positions represented by cubes. The third dimension is measured by the height h_{ij} at each position (x_i, y_j). In the SOS model, only surface atoms are taken into account, i.e. there is only one h_{ij} value for each position (x_i, y_j), thus forbidding overhangs and bubbles.

Periodic Boundary Conditions

Periodic boundary conditions are often used in the KMC simulation to effectively represent a large system by modeling a small region. When an object (a cube in an SOS

model) crosses over one edge of the simulation area, it reappears on the opposite edge with the same properties. The boundary conditions in my model were chosen to accommodate surfaces of an arbitrary miscut angle. As illustrated in Figure 5.5, the model assumed that the surface is equally occupied by the A and B terraces (in gray and green lines), and gray vertical lines and green horizontal lines represent the 1×2 and 2×1 dimer rows. The terrace width W is given by the polar miscut angle, while the azimuthal miscut angle α determines the population of the kinks on each step. Both *x* and *y* direction are set to have helical boundary conditions so that the center square in Figure 5.5 can be used in the finite-size KMC simulation. The detailed boundary conditions can be found in appendix B.

Sampling in KMC Simulation

Qualitatively, there are two types of samplings in KMC simulations.[162] The first type (simple sampling) randomly visits all individual sites (cubes in my SOS model) based on the same probability of being chosen. After a site has been chosen, depending on the location of the site, a subsequent probability-based attempt is used to determine the occurrence of one of the events illustrated in Figure 5.1. The events include adatom diffusion, attachment, detachment, or none. The resulting state of that site is stored and used in later attempts. Instead of sampling all sites, the second sampling type is focused on those sites, such as adatoms and atoms on step edges, which might change state in the next attempt. Then a random number is used to calculate which site will be the next to activate and then changes that site's state after an attempt.

In general, the first algorithm is easy to implement, but it may not be very efficient

when dealing with a surface where majority components are inactivated sites (fewer step edges). Many attempts will be invalid. The second algorithm requires significantly more bookkeeping than the first, but is often much faster. In our simulation, the activate sites include step edges and adatoms. In the later stages of simulation, the number of adatoms can be surprisingly large. Based on these considerations the first algorithm is used in the simulations.

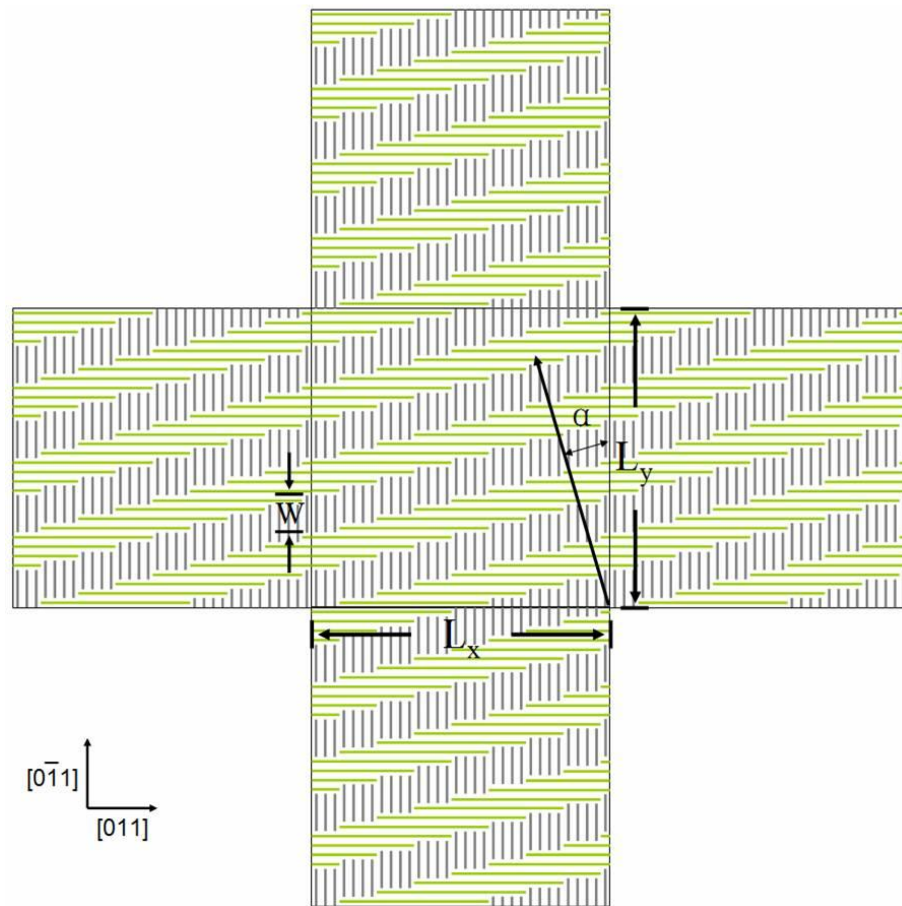


Figure 5.5: Illustration of the periodic boundary conditions used in the simulation. Gray vertical lines and green horizontal lines represent the 1×2 and 2×1 dimer rows. The terrace width W is given by the polar miscut angle, while the azimuthal miscut angle α determines the population of the kinks on each step. These identical squares can be used to represent the infinite surface.

5.2.2 Surface Atom Movement Algorithm

A square SOS model with the lattice constant (and the step height) $a = 1$ is used to interpret the Si (100) surface. Helical boundary conditions were used in the both *x*- and *y*-directions to accommodate surfaces of an arbitrary miscut angle. As shown in Figure 5.5, the lower right corner of the square is the highest position in this SOS model. Because of the negligible azimuthal miscut angle, we considered the step-down direction approximately parallel to the *y*-axis.

In the model, an adatom can only interact with the nearest four lateral neighbors, thus all long range interactions are neglected. We forbid two-dimensional nucleation in the simulation, i.e. there are no interactions (attraction or repulsion) between adatoms. To prevent step overlapping (or even touching), after every single attempt on a random position, the height difference between that position and its four nearest neighbors is less than 2. One needs to keep in mind that, this will not affect the initial step overlapping situation at the fiducial marks. We neglect long range step-step interaction; also there is no adatom evaporation or deposition in the simulation.

During the simulation, surface atoms are randomly detached from the step edges and become adatoms in accordance with predefined, site-specific detachment rates. Diffusion probabilities of adatoms along the *x*-axis and *y*-axis are calculated based on the diffusion barrier and electromigration effect. Adatoms can attach to step edges with the designated attachment rates, or they can cross over step edges when step edges become permeable (adatoms can pass through steps without been trapped).

A general statistical equation $P = (1+\exp(\Delta E / k_B T))^{-1}$ is used to generate the probabilities of all types of conditions mentioned above. We used several parameters to

determine the ΔE, thus to obtain the detachment rates and the diffusion probabilities. The kink effect is used to determine the attachment/detachment rates; the energy barrier of adatom anisotropic diffusion and the current-induced electromigration force are combined to give the adatoms diffusion rates; and the permeability factor (also related to the Ehrlich-Schwoebel barrier) is also used in the simulation to analyze the step instability. Some of these parameters such as the electromigration force and the permeability factor cannot be obtained explicitly from experiments. The model was designed with fully adjustable parameters by comparison to experiment. The details are discussed later in this section.

Anisotropic Diffusion Rate

Due to the 2×1 dimer-row reconstruction, the orientation of the dimer rows alternates from one terrace to the other, and the resulting vicinal surface shows anisotropic properties during atomic diffusion. It has been observed that at low temperature, instead of adatoms, addimers are diffusing on the surface.[157] At high temperature, there is no evidence of any particular species (adatoms or addimers) that undergo diffusion. However, an anisotropic diffusion phenomenon has been observed in both cases. Here, “adparticle”, which represents as a lattice position in SOS model, is used to represent an adatom, addimer or surface atom.

Roland and Gilmer used the empirical Stillinger-Weber potential to model the silicon atoms.[159] From the energy map, they calculated the energy barrier of $E_{//}$ = 0.67±0.04 eV for adatom diffusion along the dimer rows, and an energy barrier of $E_{\perp}$ = 0.76±0.04 eV for adatom diffusion across the dimer rows. The diffusion probability on

different terraces can be defined as

$$P_{//} = (1+\exp(E_{//} / k_B T))^{-1} \quad (5.1)$$

$$P_{\perp} = (1+\exp(E_{\perp} / k_B T))^{-1} \quad (5.2)$$

Current-induced Electromigration

During thermal annealing, surface particles become positively charged due to ionization, and their motion in all four directions is affected by the electric field. A compensation energy E_{curr} needs to be added to formula (5.1) and (5.2).

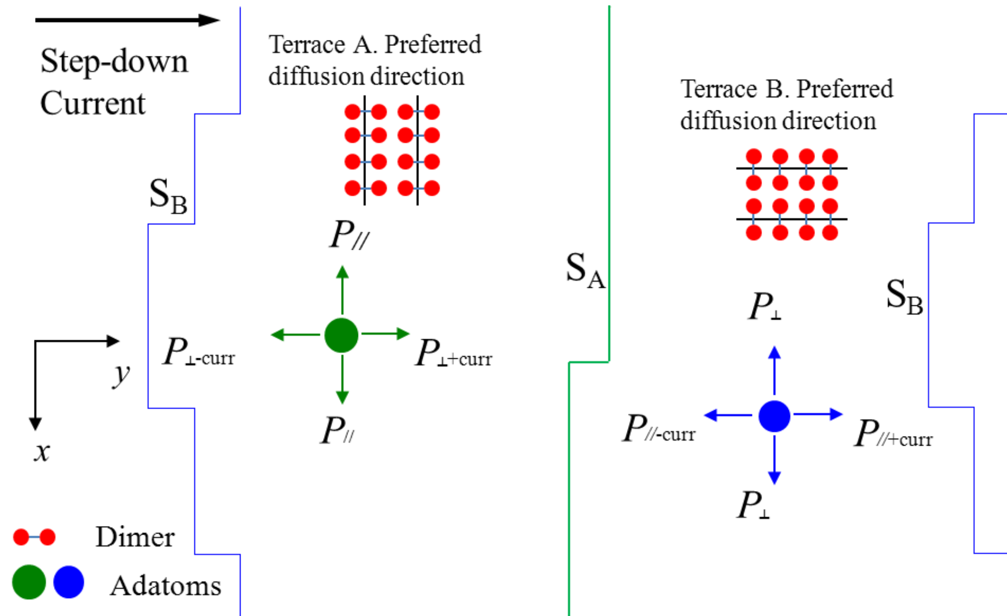


Figure 5.6: Definition of diffusion possibilities on different directions. X and y axes are labeled in the schematic picture, and a step-down current is passing through the surface. The big green dot appears on the terrace A (T_A), where dimer rows are parallel with the step (S_A). The big blue dot appears on the terrace B (T_B), where dimer rows are perpenticular with the step (S_B).

As shown in Figure 5.6, for the adparticles on terrace A (T_A), the diffusion rate is fast in x-direction. In the presence of an electric current (DC) on surface, the diffusion probabilities of the green dot in all four directions on T_A can be written as:

$$P_{y-} = P_{\perp}\text{-curr} = (1+\exp((E_{\perp} - E_{curr}) / k_B T))^{-1} \quad (5.3)$$

$$P_{x-} = P_{//} = (1+\exp(E_{//} / k_B T))^{-1} \quad (5.4)$$

$$P_{y+} = P_{\perp+curr} = (1+\exp((E_{\perp}+E_{curr}) / k_B T))^{-1} \quad (5.5)$$

$$P_{x+} = P_{//} = (1+\exp(E_{//} / k_B T))^{-1} \quad (5.6)$$

As for the blue dot, the diffusion rate is fast in the y-direction on terrace B (T_B). So the diffusion probabilities on T_B are:

$$P_{y-} = P_{//-curr} = (1+\exp((E_{//}-E_{curr}) / k_B T))^{-1} \quad (5.7)$$

$$P_{x-} = P_{\perp} = (1+\exp(E_{\perp} / k_B T))^{-1} \quad (5.8)$$

$$P_{y+} = P_{//+curr} = (1+\exp((E_{//}+E_{curr}) / k_B T))^{-1} \quad (5.9)$$

$$P_{x+} = P_{\perp} = (1+\exp(E_{\perp} / k_B T))^{-1} \quad (5.10)$$

The Effect of Step Permeability

While an adatom is moving on the surface, it may attach to a step. If the kink density along the step is high, the attachment to the step usually reaches a kink position to solidify. The adatoms crossing the step without solidification are negligibly few, thus the step is called impermeable (nontransparent). On the other hand, if the kink density along the step is low, adatoms attaching to a straight part of the step may not reach a kink position and will leave the step without solidification. If the number of the adatoms crossing the step without solidification is not negligible, the step is called permeable (partially transparent).

Figure 5.7 demonstrates the adatom-step processes when there is step permeability. An adatom can pass the permeable step without being incorporated, as shown in Figure 5.7(g) and (i). Otherwise, the adatom will stop and solidify on the step (Figure 5.7(h)).

In the SOS model, this incorporation process can be determined by the solidification

probability.

$$P_s = (1+\exp((E_{step} - E_s) / k_B T))^{-1}, \quad (5.11)$$

where E_{step} is the increment of the step energy and E_s is the energy gained by solidification (attachment). Following the calculation by Chadi[79], the step formation energies are E (S_A) = (0.01±0.01)/a (eV) and E (S_B) = (0.15±0.03)/a (eV), where a=3.85 Å is the 1x1 surface lattice constant.

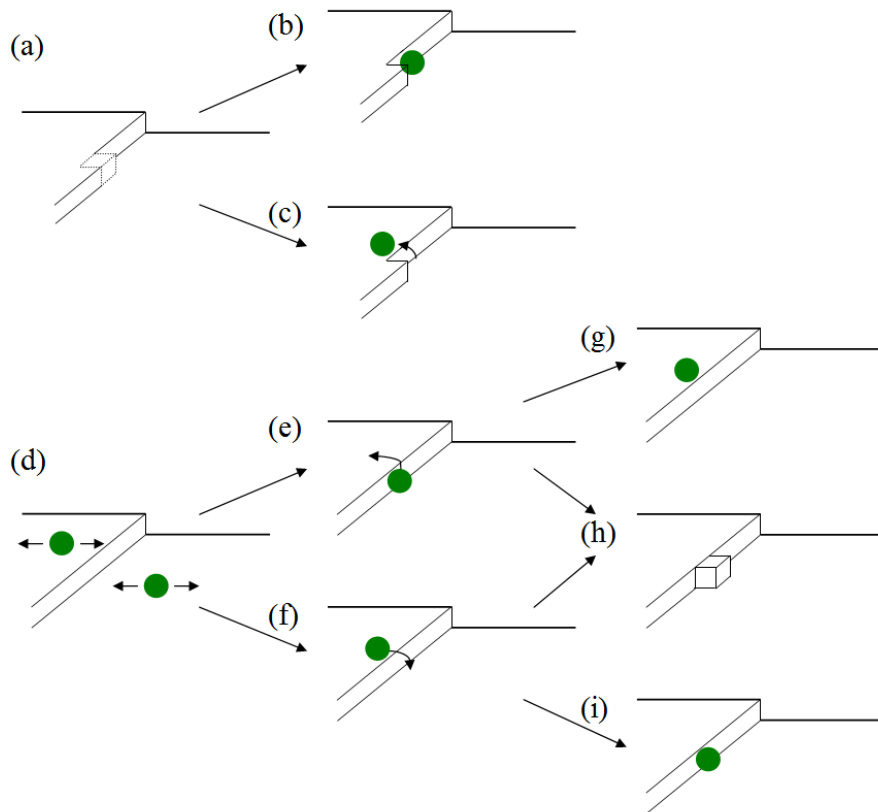


Figure 5.7: adatom-step interaction considered in the KMC simulation. (a) a atom melts from a kink to become an adatom, it can appear on the (b) lower terrace or (c) upper terrace. The adatom can (d) diffuse on the surface, or move toward a step from (e) lower terrace or (f) upper terrace. In the case of an impermeable step, the adatom will (h) solidify after it attaches on the step. In the case of step permeable, the adatom can (g) climb up to the upper terrace, or (i) move down to the lower terrace.

Ehrlich-Schwoebel (ES) Effect

When an adatom from an upper terrace jumps to a lower terrace, it requires more

energy to cross the step compare with the diffusion energy on the single terrace. The energy difference is known as the ES barrier.[163,164] Generally, due to the ES effect, the adatom on the upper terrace needs to overcome an additional energy barrier to reach the lower terrace (step down) because of the extra potential energy between the upper and lower terrace.

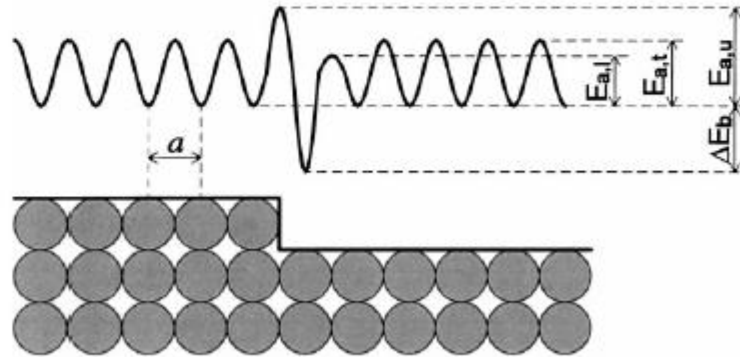


Figure 5.8: The ES barrier effect on the step edge. The energy barrier for adatoms diffusion is marked as $E_{a,t}$. When an adatom is moving to the step edge from upper terrace, it requires a higher energy $E_{a,u}$ to overcome the energy barrier at the step edge. The energy barrier $E_{a,u}$ could be less if the adatom is from lower terrace. (From H. C. Jeong *et al.*[165])

Roland and Gilmer[166] simulated the barrier energies when a silicon atom approaches a step edge. When an adatom approaches a step edge, the activation energies will be different depending on the diffusion direction (upper or lower terrace) and type of step (S_A or S_B step, shown in Figure 5.6). At the S_A step edge, the activation energy for moving from the upper terrace is 0.50 eV, while moving from the lower terrace is 0.38 eV. At the S_B step edge, the activation energy for moving from the upper terrace is 0.76 eV, while for moving from the lower terrace it is 1.0 eV.

Other Effects

In order to achieve reasonable computational times, two-dimensional nucleation and atom sublimation are neglected in the program. Steps overlapping are also forbidden.

A table lists all the parameters that I used in the KMC simulation. Some of those parameters values are from literatures, some values are from experimental observation or estimation. All values are adjustable in the program. (Please see appendix B for detailed information)

Table 5.1: Input parameters used in the KMC simulation.

Parameter	Value	Note [reference]
$E_{//}$	0.67 eV	[159]
$E_{\perp}$	0.76 eV	[159]
E_{curr}	-0.18 eV	Electromigration energy, estimated
T	1273 K	Annealing temperature
k_B	8.617343×10^{-5} eV/K	Boltzmann constant
Detachment coefficient [a]	$4^{(n-4)}$, n is the number of the nearest neighbors on the lower step.	Adatom formation probability, estimated
Attachment coefficient [b]	$4^{(n-4)}$, n is the number of the nearest neighbors on same level.	Adatom solidification probability, estimated
Permeability factor [c]	0.2	The probability of an adatom cross over a step edge without solidification, estimated

[a] The detachment coefficient C_{detach} depends on the number of adjacent atoms. $C_{detach} \propto \exp(-n)$, where n is the number of adjacent atoms. The base in C_{detach} can be adjusted to increase/decrease the effect of kink sites. In the simulation, the base is 4.

[b] The detachment coefficient C_{attach} depends on the number of adjacent atoms. $C_{attach} \propto \exp(n\text{-}4)$, where n is the number of adjacent atoms. In the simulation, the base is 4.

[c] The energies E_{step}, E_s and E_{ES} are not considered explicitly but their values will determine the permeability factor.

5.3 KMC Simulation Results on Si (100) Surface

The main goal of the simulation is to understand the surface morphology evolution with fiducial marks present during resistive heating.

5.3.1 Simulation without Fiducial Marks

After prolonged high temperature annealing, the Si (100) vicinal surface is composed of several step bunches and paired steps running between step bunches[167] (as shown in Figure 5.9 (b)). This effect is known as current-induced step bunching. The first step in developing the simulation is to reproduce the kinetic instabilities of the surface morphology observed experimentally after extended annealing. (As shown in Figure 5.9(a))

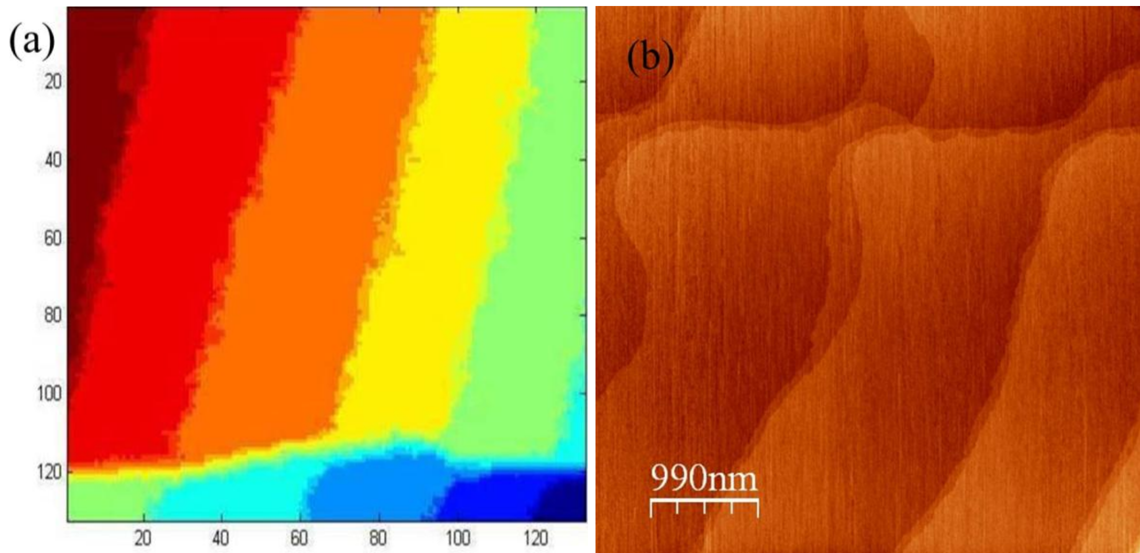


Figure 5.9: (a) a snap shot of the simulated surface morphology via KMC simulation (colors terraces indicate the height difference, the height of terraces increases from red to blue), (b) an image of Si (100) surface morphology taken by an ambient AFM after extended annealing.

We start from the basic model only with the assumption that the diffusion is anisotropic due to the combined effect of the structure of dimer rows and the electromigration effect. It is also assumed that the steps are permeable to atoms. The model is initiated with 128×128 pixels (atoms), and contains 16 uniform parallel steps, as shown in Figure 5.10. The total number of attempts is set at 5×10^8. Since the wafer that we are using has a very small azimuthal miscut angle (<1.5”), the effect of the azimuthal angle is very negligible and is not considered in the simulation. The electromigration

effect has been implemented in either the *y*+ (step-up diffusion) or the *y*- (step-down diffusion) direction. The diffusion coefficients in four directions are proportional to the adatom diffusion probabilities (calculated using equations (5.3) – (5.10)) in four directions. In order to increase the simulation efficiency, the total diffusion coefficients have been normalized so that the sum of diffusion coefficients of a fast-diffusing adatom is equal to one.

Within a few cycles of the simulation, individual steps get paired on the surface. Figure 5.10 (a) and (b) represent snap shots of the simulation result for anisotropic diffusion. The dotted green line represents the step corresponding to the B terrace, and the A terrace can be recognized by the steps with red dotted red lines. The surface is covered mainly by B terraces in the case of step-down drifting (due to the electromigration effect)[168] whereas for the step-up drifting the A terrace is the dominant terrace, as shown in Figures (a) and (b) respectively.

The computer code is written in a way such that, for the step-down diffusion direction (*y*-), adatoms on the B terrace can move faster in the *y*- direction. They will attach to the step edge B as they arrive. This results in a faster growth rate of the B terrace in comparison to the A terrace and hence, the B terrace will try to overgrow an A terrace. Since overhangs are forbidden in the SOS mode, one step cannot cross over the other.[169,170] Eventually, step B and A will be paired and the surface will be mainly comprised of B terraces, where the dimer rows are perpendicular to the step edge. For the case of the step-up diffusion, a similar argument can be applied. But in this case the surface will be primarily covered by the A terrace, where the dimer rows are parallel to the edge.

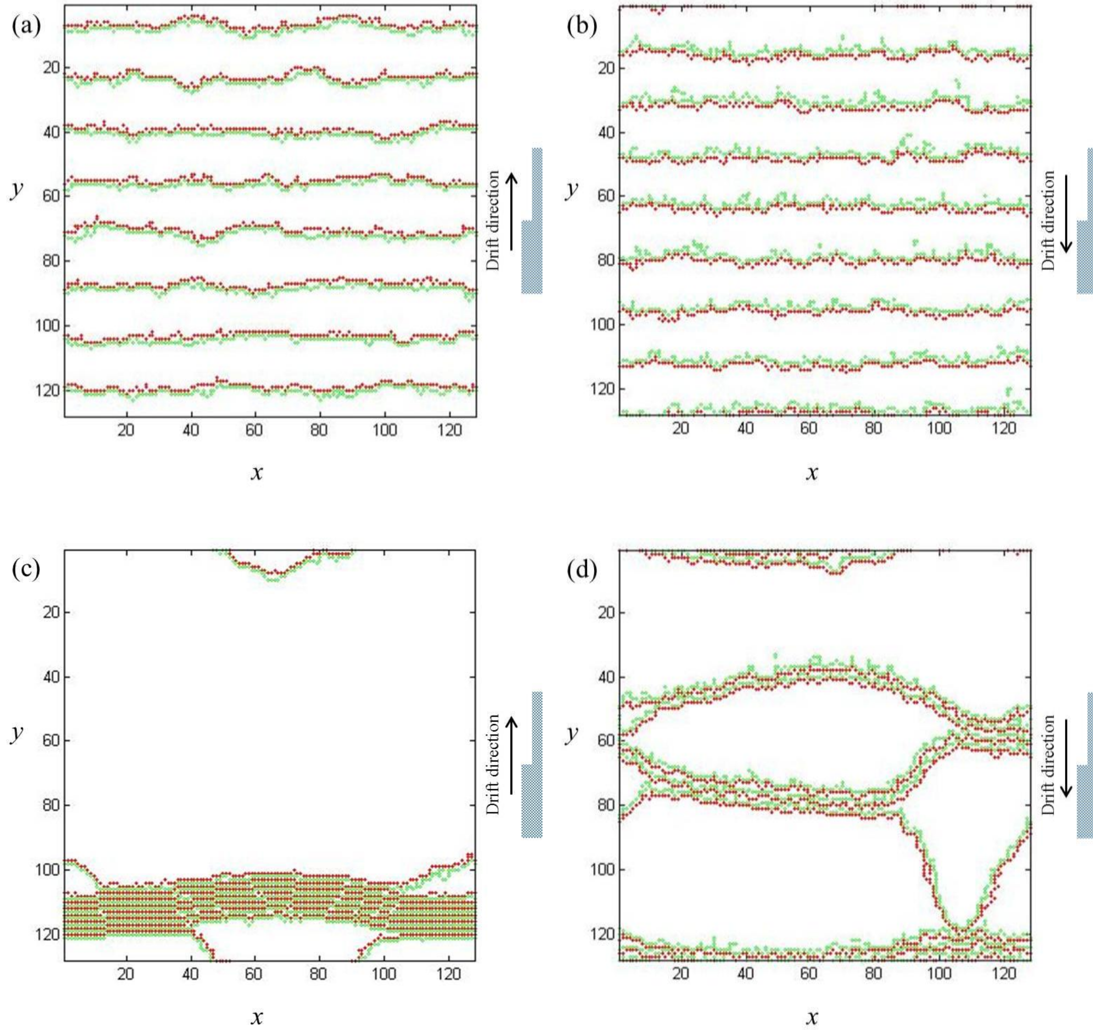


Figure 5.10: Snap shots of the surface structure with drift in the (a) step-down and the (b) step-up directions after a few cycles of the simulation. The dotted green line represents the step corresponding to the B terrace, and A terrace can be recognized by the step with red dotted red line. (c) and (d) represent the simulation results in the later stages with the step-down and the step-up directions, respectively.

In the later stages, as shown in Figure 5.10 (c) and (d), step bunching occurs on both step-up and step-down drifting directions. The density of step bunching is higher with the step-down simulation result (shown in Figure 5.10 (c)) compared with the step-up result (Figure 5.10 (d)).

The simulation results indicate the formation of step bunching is probably due to the step permeability rather than the ES effect. Natori *et al.* explained the formation of step bunches with step-down driving forces based on the extended BCF theory.[171] They

considered the drifting effect caused by the external driving force, the anisotropic diffusion coefficient, and the step-step repulsion to describe the surface evolution from step pairing to step bunching. With the step-up driving force the step bunches do not appear in their simulation results even with the ES effect. This does not agree with the experiments.

The classic BCF mode is established based on step-flow growth, where adatom detachment can be neglected; adatoms which appear on the surface are mainly from external material sources instead of the detachment from step edges. Such a high density flux of adatoms can strongly affect the rate of step motion. The adatom-step barrier (ES effect) becomes very important in this case. Figure 5.11 briefly explains the formation of step bunching under the ES effect. When the ES barrier is sufficiently high on the upper terrace (as shown in Figure 5.11 (a)), adatoms approaching from the upper terraces can be neglected; thus, the steps can only absorb adatoms from the lower terraces. The speed of step movement is proportional to the size of the lower terrace; the wider the terrace, the more adatoms present on the surface. Thus, the step moves faster due to more adatom attachment (Figure 5.11 (b)). After a period of time, no further step bunching can occur, as described in Figure 5.11 (c). However, another surface instability, named the meandering instability, can occur on the 2-D surface[172] for conditions opposite to that for bunching instability. On the other hand, for a negative ES barrier (as shown in Figure 5.11 (d)), the speed of step movement is proportional to the size of the upper terrace. Steps can stack up (Figure 5.11 (e)) and eventually form step bunches (Figure 5.11(f)).

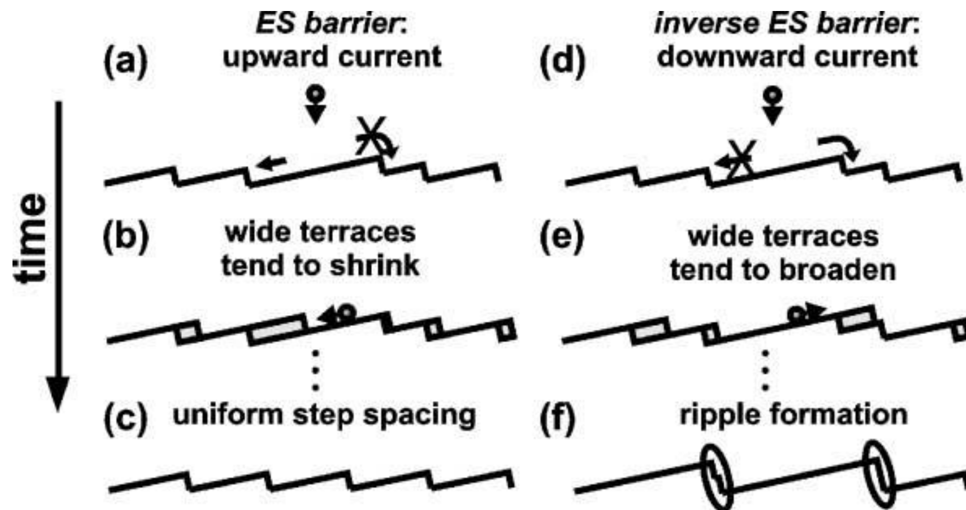


Figure 5.11: The development of the surface morphology during step-flow growth with an ES barrier. (a) ES barrier appears on the upper terrace, (d) ES barrier appears on the lower terrace. (From J. Myslivеček *et al.* [173])

In our experiments, because there are no external material sources, all the adatoms are from step edges. Since the total number of adatoms is much less as compared with the step-flow growth condition, the rate of step motion will be greatly reduced. Also, the rate is affected by the surface atom detachment rate, which can be very high due to the electromigration force.

Consider the case where an adatom approaches from a lower terrace and attaches to the step in two consecutive attempts. If the detachment rate is high enough due to the electromigration effect, or the geometrical location effect (attached on a flat step instead of a kink), this atom can escape from the step and become an adatom again. At this time, it can appear on either the lower or upper terrace, which purely depends on the probabilities. Eventually this adatom may move to an upper terrace. In this case, the adatom undergoes three processes, attachment, detachment, and then a move up, to cross over a step, which is very similar compared to the permeable step condition, but with a lower escape rate. Similar arguments can be applied with the presence of an ES barrier.

The higher the ES barrier, the lower the detachment rate; thus steps become less permeable.[174]

In the classical model the steps are impermeable, and the ES barrier is an important factor. However, instead of using ES barrier directly, we are using an empirical ‘permeability factor’ that depends on the ES barrier. Because of the step permeability, the density of adatoms around the steps will become higher. The high density of adatoms can accelerate (moving toward the step) or decelerate (moving away from the step) the rate of step motion. Eventually step bunches will be formed at places having high step densities. The results are shown in Figure 5.10 (c) and (d), which qualitatively agrees with our experimental results.

T. Zhao *et al.*[175] also considered the effect of electomigration and permeability on Si (100) surfaces using a 1D discrete-hopping model, and then derived the boundary conditions within a continuum sharp-step model. They found that both the kinetic coefficients and permeability rate can be negative when diffusion is faster near the step than on terraces. They also found that a step-bunching instability can happen with both step-down and step-up currents on impermeable steps.

5.3.2 Simulation with Fiducial Marks

Next, we introduced fiducial marks into the program by assigning h_{ij} values of positive 32 pixels (or negative 32 pixels) to create the wall pattern (or trench pattern). This can be recognized in Figures 5.12 (a) and (b). As illustrated in Figure 5.12 (a), a wall model contains 384×384 pixels and 32 steps. The green and red bands represent different terraces with 1×2 and 2×1 dimer rows. The width of the walls is initialized as

32. However, to satisfy the periodic boundary conditions, the width of the walls on the bottom and the top is set as 16. The size of basins between those walls is 160×160. A similar trench fiducial marks model is shown in Figure 5.12 (b) which contains 384×384 pixels, 32 steps, 32 pixels wide trenches, and size 160×160 plateaus. However, those trenches are discontinued and the length of them is 128 pixels.

Instead of directly using Figure 5.12 (a) and (b) to run KMC simulation, we used a quarter model based on these two figures to perform the simulation. First, it requires too much computation time if we simulate such a large model with too many pixels (384×384 pixels at here). Secondly, the Figure 5.12 (a) contains four basins, which is the smallest periodic element of the wall fiducial marks. We can shrink the simulation size while we maintain the periodic boundary conditions (also valid for the trench model).

As shown in Figure 5.12 (c) and (d), the simulation pixel counts are changed to 192×192 in order to evaluate the size effect of the fiducial marks. The model contains 16 uniform parallel steps, and one '工' shape wall (or one '+' shape trench) has been placed in the simulation region. The total number of attempts is set at 1×10^9.

As I mentioned above, the simulation results of Figures 5.12(c) and (d) can be used to interpret surface evolution on a larger scale due to the periodic boundary conditions. For instance, we can merge 4 identical 192×192 pixel simulation results into one 384×384 pixel-size structure to represent the evolution of the surface morphology on a bigger view that makes it easier to see the pattern. After merging the simulated results under various simulation conditions, we obtain the fiducial marks sample surface morphology, which are shown in Figure 5.13 (a) – (d).

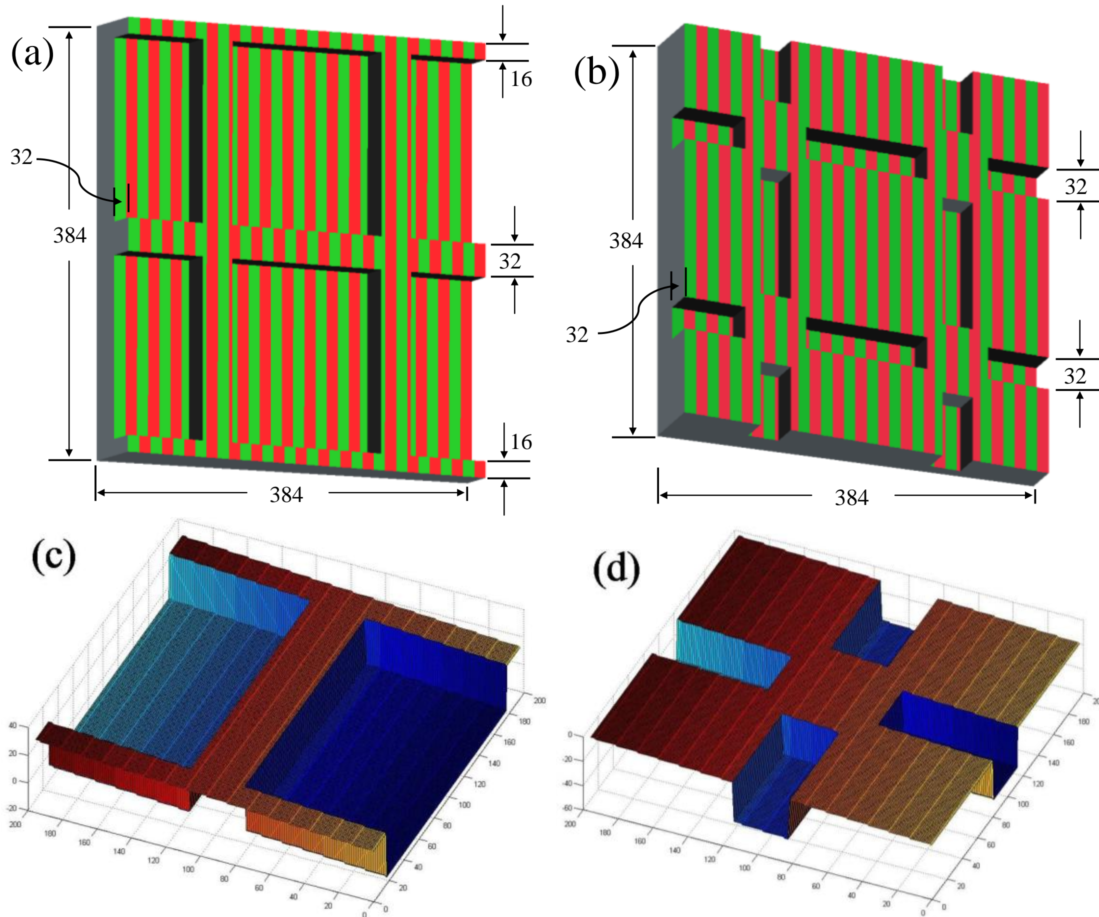
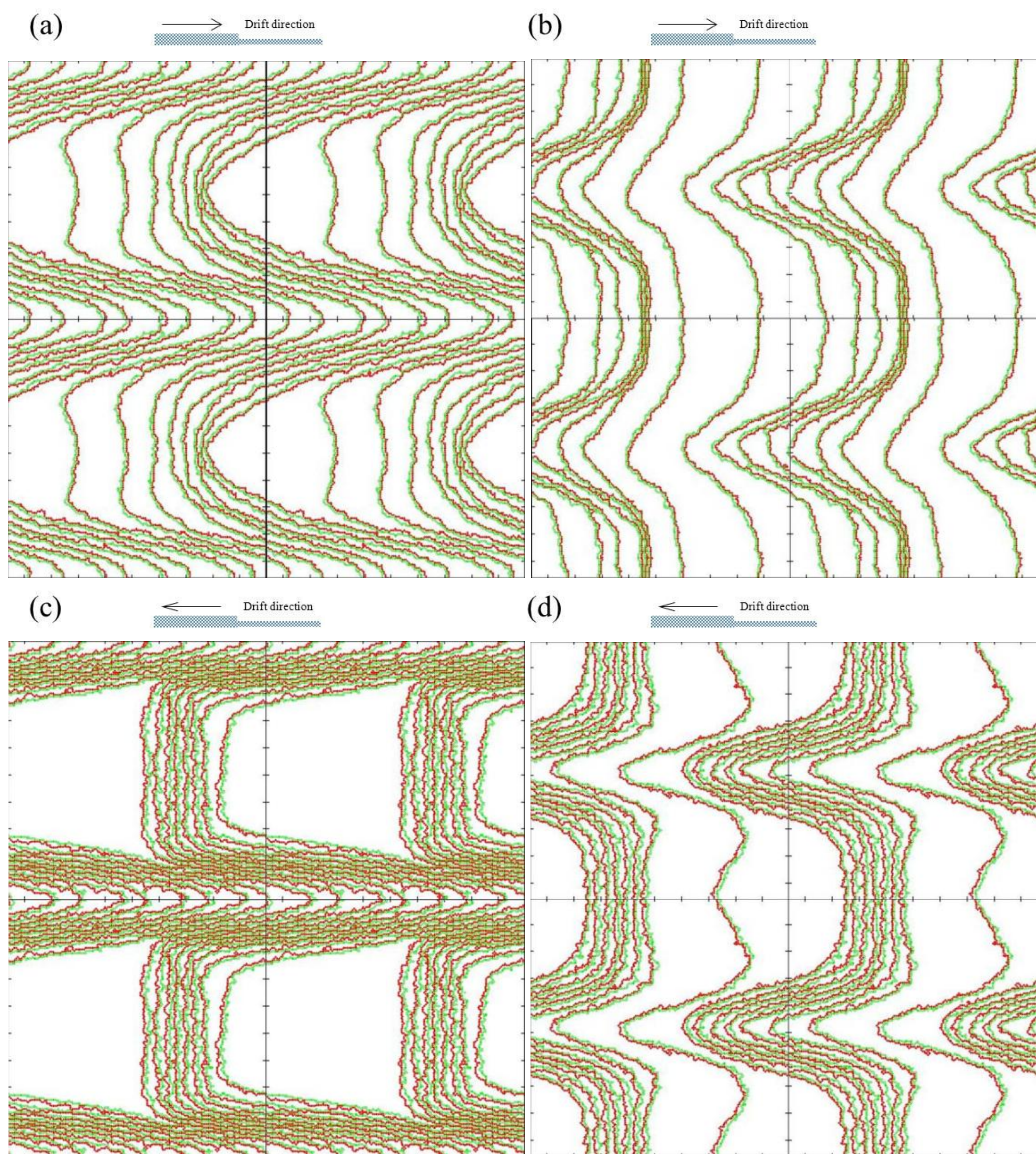


Figure 5.12: SOS models with fiducial marks (a) walls and (b) trenches. Model (a) contains 384×384 pixels and 32 steps. The green and red bands represent the different terraces with 1×2 and 2×1 dimer rows. The terrace on the left side is higher than the right side. The height of walls is 32, and the width is also 32, except the walls on the bottom and the top, which is 16. Model (b) has similar configurations, except with discontinued trenches. The length of these discontinued trenches is 128. Model (c) and (d) represent a quarter of (a) and (b), respectively.

Figures 5.13 (a) and (b) show the step-down drifting results with walls and trenches. Although step pairing is seen on the surface, there are no large flat terraces formed under these conditions. As for the step-up drifting shown in Figure 5.13 (c), these walls, which are perpendicular to the drifting direction, deformed and created step bunching after the simulation. Large flat terraces appeared between the step bunching and the side wall. In Figure 5.13 (d), ordered step pairing formed in the trenches during the simulation. The simulation results in Figures 5.13 (c) and (d) resemble very closely the experimental data (Figures 5.13 (e) and (f)). The snap-shot images from the simulation suggest a method to

form ordered terraces by applying a step up direction current, which will be verified in future experiments.



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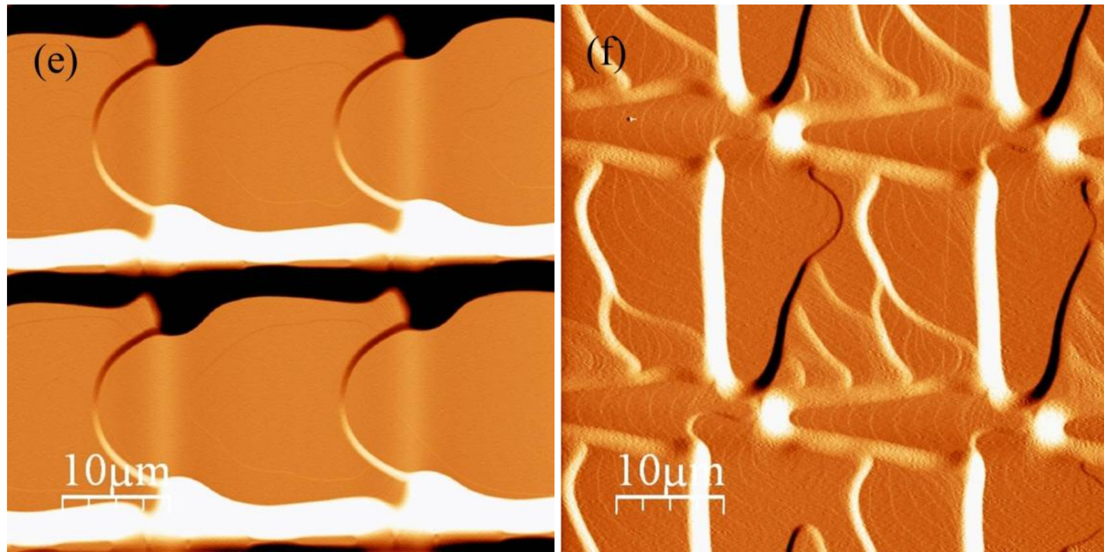


Figure 5.13: (a)-(d) show KMC simulation results with fiducial marks, and the simulation size is 384×384 pixels. (a) and (b) are the results of wall and trench patterns with the step-down drifting conditions. (c) and (d) are the results of wall and trench pattern with the step-up drifting conditions. The simulation results (c) and (d) are very close to the AFM data (e) wall and (f) trench patterns.

We also simulated the patterns shown in Figures 5.12 (a) and (b); however, many features shown in Figures 5.12 (a) and (b) are reduced to half scale (the size has been reduced to 192×192, the width of walls/trenches has been decreased to 16, and the size of basins/plateaus has been reduced to 80×80). As shown in Figure 5.14, it becomes quite difficult to recognize those patterns after 1×10^9 attempts.

This likely implies that the size of fiducial marks is also important, as we have confirmed with experiments (in 4.3.1). If the boxes (fiducial marks) are too small (<15×15 μm^2) or too thin (<1 μm), they may not survive the prolonged high temperature annealing.

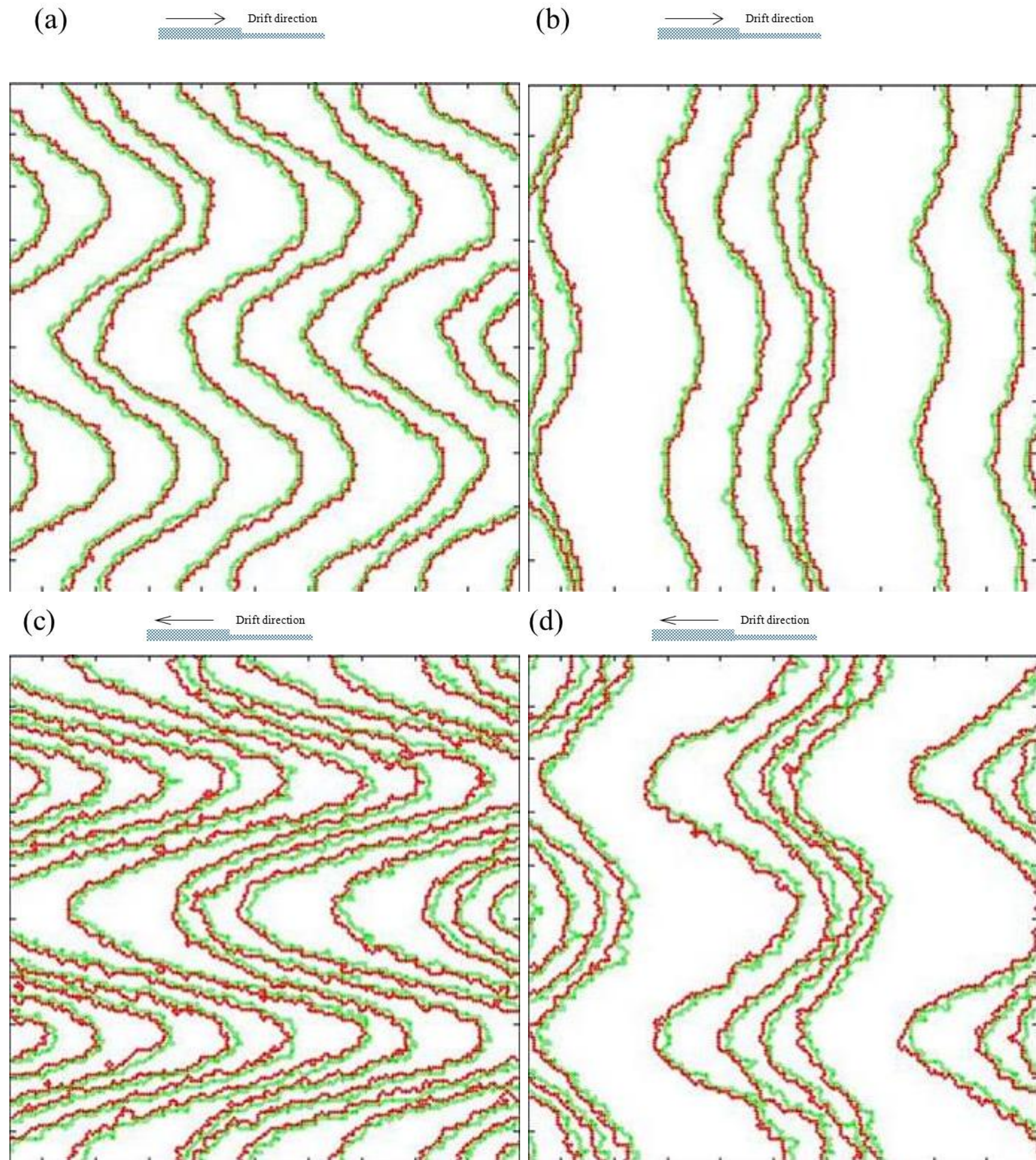


Figure 5.14: (a) and (b) are the results of wall and trench patterns with the step-down drifting conditions. (c) and (d) are the results of wall and trench pattern with the step-up drifting conditions. The simulation size is 192×192 pixels.

5.4 Summary and Discussion

By carrying out KMC simulations, we have studied the current-induced step instabilities on surfaces with fiducial marks. By introducing reasonable step permeability

along with an anisotropic diffusion coefficient due to the current-induced migration, step pairing and step bunching occur on both the step-up and step-down diffusion directions.

The computational time of the KMC simulation becomes a critical issue when we simulated the surface evolution with fiducial marks. To achieve reasonable computational time, many parameters have been either adjusted, or have not been considered by assumption, which may be important in determining the final surface morphology. For example, the number of pixels (atoms) has been compromised so that the computational time of one simulation can be accomplished within approximately 24 hours using a desktop (Inter® Core™ 2 Quad CPU Q6600 @ 2.40 GHz, 4.00GB RAM). If one wants to simulate the evolution of fiducial marks on a more realistic scale, the computational time will be enormously increased. Although the evaporation effect has been neglected in the simulation, one can recognize some vacancy islands in the experiment (see Figure 5.3), which are due to sublimation. These islands can keep growing if the sublimation effect is stronger, or they might disappear if the adatom density is high.

However, by choosing the primary parameters from our experiments, the simulation produced results that are in fairly good qualitative agreement with the experimental data. The simulation results suggested that relatively large boxes are better in terms of surviving the annealing process and creating wide, atomically flat terraces as confirmed by experimental observations. In summary, the results of the simulations are adequate and served the purpose for optimizing the geometry and dimensions of the fiducial patters for producing optimum templates for atomic scale lithography.

Chapter 6: Nanostructuring on Si (100) Surfaces

Nanostructuring on the Si (100) surface has potential applications in the area of nano manufacturing by providing standardized nanostructures with resolution extending down to sub-10 nm region. The key advantage of this lithographic technique is the ability to pattern sub-10 nm structures over a large area with a high-throughput and low-cost. Therefore, it can be pursued as a manufacturing technology at the nanoscale.

The process involves is passivation of Si (100) surface by atomic hydrogen and subsequent selective depassivation using an STM probe. The exposed silicon atoms in the depassivated area are then oxidized, and the sample is removed from the UHV chamber and subjected to RIE etching. The oxide patterns serve as masks during the RIE process. The aspect ratios can be considerably enhanced using this method. Details of these processes and results are discussed in the following sections.

6.1 Hydrogen Passivation

6.1.1 Procedure

The sample is transferred into the main chamber for hydrogen passivation after the reconstructed silicon surface has been analyzed by STM. Hydrogen molecules are cracked either by a commercial hydrogen cracker (H-flux) or by a hot W filament

(backfill) to form atomic hydrogen which is highly reactive. The atomic hydrogen will passivate the silicon (100) 2×1 surface by the formation of Si-H bonds (as shown in Figure 6.1).

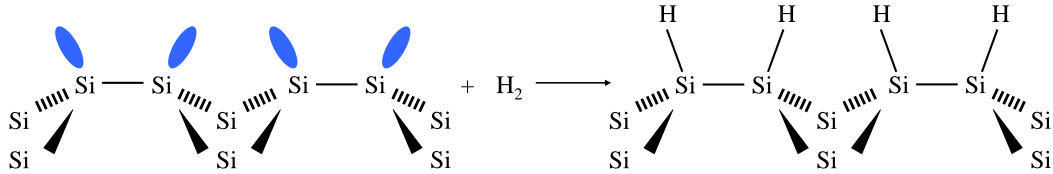


Figure 6.1: Schematic picture of hydrogen passivation process. After cracked by the hydrogen cracker or the hot W filament, atomic hydrogen can react with surface Si atoms and terminate those dangling bonds (shown as blue ellipses).

In this experiment, ultra high purity hydrogen gas (99.9999%) is used for passivation. A molecular sieve purifier and a liquid-nitrogen cold trap are used to further clean the hydrogen gas before it is introduced into the main chamber. A cold cathode vacuum gauge is used to measure the pressure because conventional Bayard-Alpert (BA) ion gauges do not function properly due to the high reactivity of hydrogen atoms. Separate experiments were carried out using a commercial hydrogen cracker and a hot W filament.

It is necessary to clean the sample surface before the passivation process. The sample is flash annealed at 1200°C to remove all the adsorbates or contaminations. Then the sample temperature is rapidly decreased to 900°C. After this, the temperature is dropped at a rate of approximately 2 °C/sec until the passivation temperature is reached. The hydrogen passivation temperatures for the hydrogen cracker and hot filament passivation are 370°C and 300°C, respectively.

The hydrogen cracker contains a fine tungsten capillary which is surrounded by a tungsten coil. The capillary is heated by electron bombardment and molecular hydrogen

is "cracked" to form atomic hydrogen after multiple collisions along the hot walls. A water-cooled copper jacket is attached at the end of the cracker to minimize radiated heat and outgassing during the operation. The ion pump is opened during the passivation process, and the fresh H-atom flux created by the cracker is pointed to the sample. The operation pressure is ~ 5×10^{-9} Torr, and it is monitored by the cold cathode gauge.

The hot W filament passivation procedure is as follows:

1. Close the gate valve between the main chamber and the ion pump.
2. Introduce the hydrogen gas into the chamber, and stop when the pressure gauge reading stabilizes at 1×10^{-6} Torr.
3. Turn off the vacuum gauge, and turn on the W filament; maintain the filament temperature at 1800°C - 2000°C for 10 minutes. In the meantime, rotate the heating stage to let the sample face the filament.
4. Pump out the hydrogen gas through the ion pump. Turn off the W filament, lower the sample temperature to room temperature, and then turn on the cold cathode vacuum gauge.
5. Transfer the sample to the STM chamber after the main chamber's vacuum has recovers.

Si (100) surface passivation results using the hydrogen cracker and the W filament are shown in Figure 6.2. Both are able to passivate the (100) surface with a small amount of defects and/or contamination.

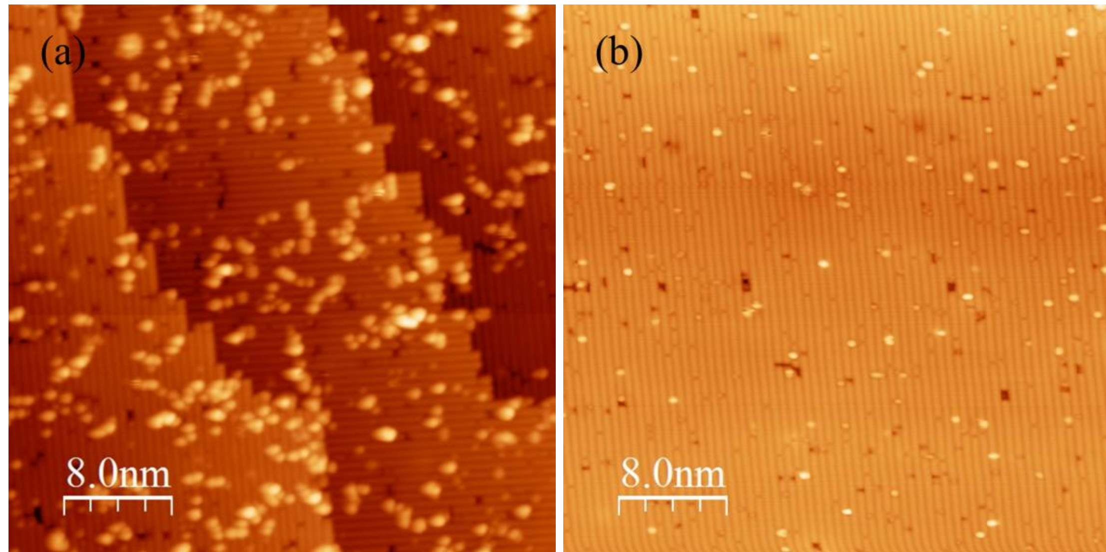


Figure 6.2: H-passivated Si (100)-2×1 surface obtained by two methods: (a) H-cracker and (b) W filament.

6.1.2 Results and Discussion

A Si (100)-2×1 surface atom has an exposed dangling bond which can be passivated by exposure to hydrogen atoms. A hydrogen-terminated silicon surface can be preserved reasonably clean (from residual gas adsorption) in UHV for a long time and serves as a main component or substrate in nanolithography. Thus the passivation quality of the Si (100) surface is a critical factor in the entire fabrication process. The passivation is affected by the sample temperature and the kinetic energy of hydrogen atoms. Hydrogen atoms may bounce several times after touching the silicon surface before they combine with silicon surface atoms. These bonded hydrogen atoms may even diffuse to nearby vacancies. Hence, it is necessary to adjust the passivation apparatus to optimize the quality of a passivated Si (100) surface.

The operating conditions and efficiencies of the H-cracker and W filament are different because of the difference in design and geometry. The commercial hydrogen

cracker is very efficient in creating H-atom flux at very low pressures (<1×10^{-8} Torr). To achieve good hydrogen passivation, the Si sample is heated to ~ 370°C and exposed to the atomic hydrogen beam for 3 minutes. The H-atom flux density and sample exposure time are critical parameters. The quality of passivation depends on the concentration of hydrogen atoms, sample temperature, sample exposure time, and vacuum conditions.

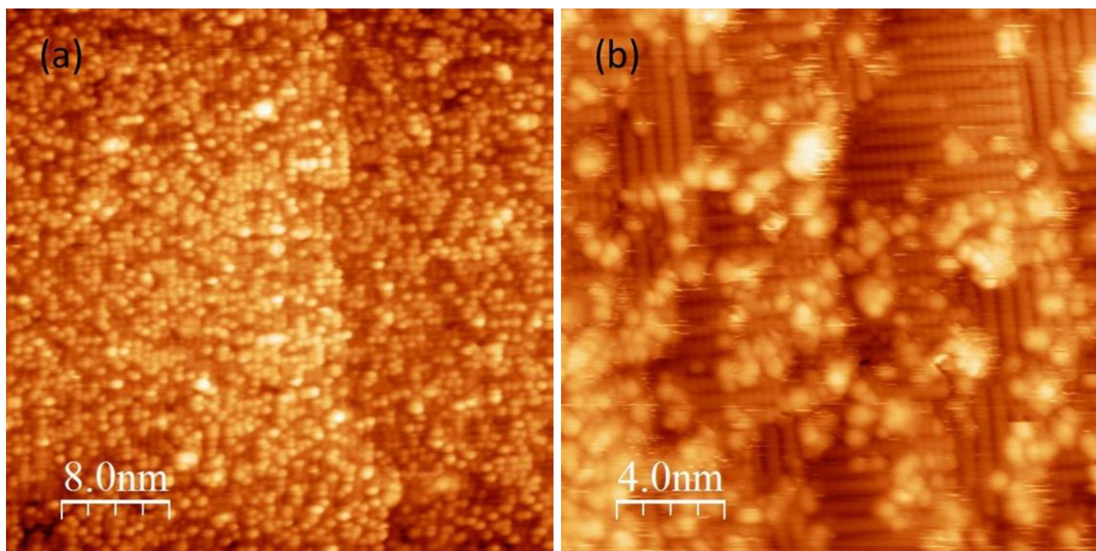


Figure 6.3: Unsuccessful passivation results taken from hydrogen cracker. In the STM image (a), the surface is full of dangling bonds, which are showing in STM as white dots. These white dots are small compare with bright dots in image (b), and they are not totally random. It is possible to see a short range order. In image (b), besides well passivated dimers, irregular bright dots also are sitting on the surface.

Insufficient exposure time or low hydrogen pressure results in failure to passivate, as shown in Figure 6.3 (a). In either case the Si (100) surface will be under-passivated, containing unsaturated dangling bonds. Compared with well-passivated surface atoms, the dangling bonds from unpassivated surface atoms can easily overlap with the electronic orbital of a close proximity STM tip. These are depicted in the STM image 6.3 (a) typically as bright dots. Contamination in the hydrogen supply line is another major problem. Those contaminants can go into the vacuum system with the hydrogen flux and then attach to the surface and interfere with the passivation process. The contaminants

can be observed after the passivation process, appearing as large white "blobs" in Figure 6.3 (b). In order to reduce this contamination, the hydrogen line is routinely pumped by a turbo molecular pump to ~ 5×10^{-8} Torr; then fresh hydrogen gas is filled and used in the experiment. This is repeated every time before the experiment.

In the case of the hot W filament, when the operating temperature is ~ 2000°C, it can automatically decompose nearby hydrogen molecules. The hot W filament produces a cloud of atomic hydrogen in contrast to the atomic hydrogen beam from the commercial cracker. Hence, the direction of the W filament is not important, while the distance between the sample and filament is critical. Also due to the lower efficiency of the filament, the operating pressure of hydrogen gas and the passivation times are higher. The passivation pressure is increased from ~ 5×10^{-8} Torr to ~ 5×10^{-6} Torr, and the passivation time is increased from 3 minutes to 10 minutes as compared with the H-cracker.

Figure 6.4 (a) shows an under-passivated surface with dangling bonds, which is very similar to the Figure 6.3 (a). During the operation, the filament temperature may be higher than 2000°C. If the distance between the sample and the filament is less than 1 inch, the sample temperature can significantly increase by 50°C to 100°C, which in turn will have a direct impact on the passivation efficiency. Figure 6.4 (b) shows the passivation results of a high temperature W filament (> 2000°C). The dimer rows are covered by relatively larger white "blobs" compared with the dangling bonds (smaller dots) suggesting that the surface is contaminated with some unknown species.

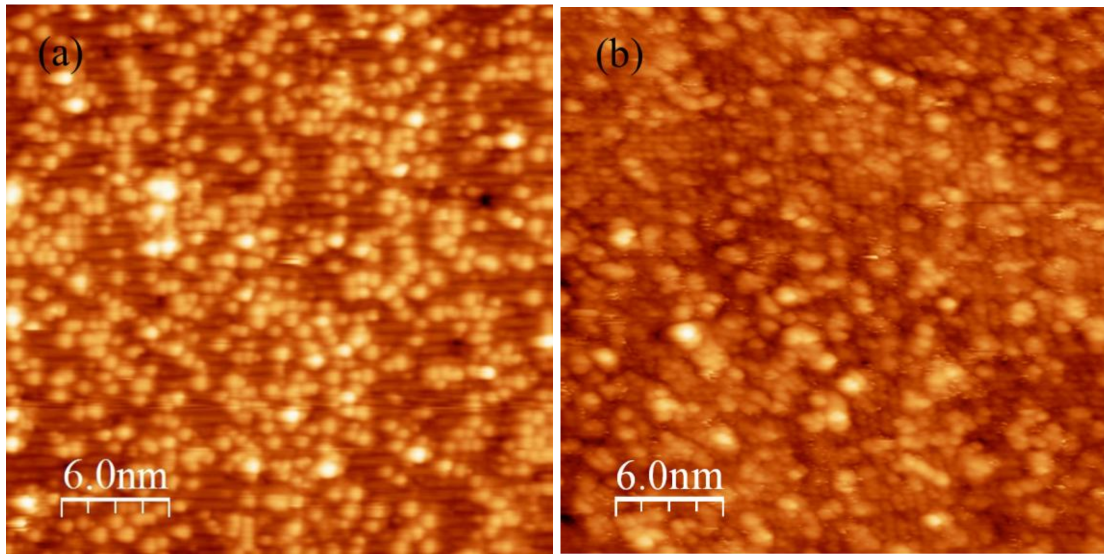


Figure 6.4: Unsuccessful passivation results taken from W filament. Dangling bonds can be recognized in the STM image (a). The bigger white blobs shown in image (b) could be some contaminates.

In order to reduce this heating effect, we lowered the sample temperature to 270°C for the W filament process. As a result, the passivation results improved substantially after reducing the sample temperature and additional work showed that flushing the hydrogen gas line for every individual passivation experiment helped as well (as shown in Figure 6.5).

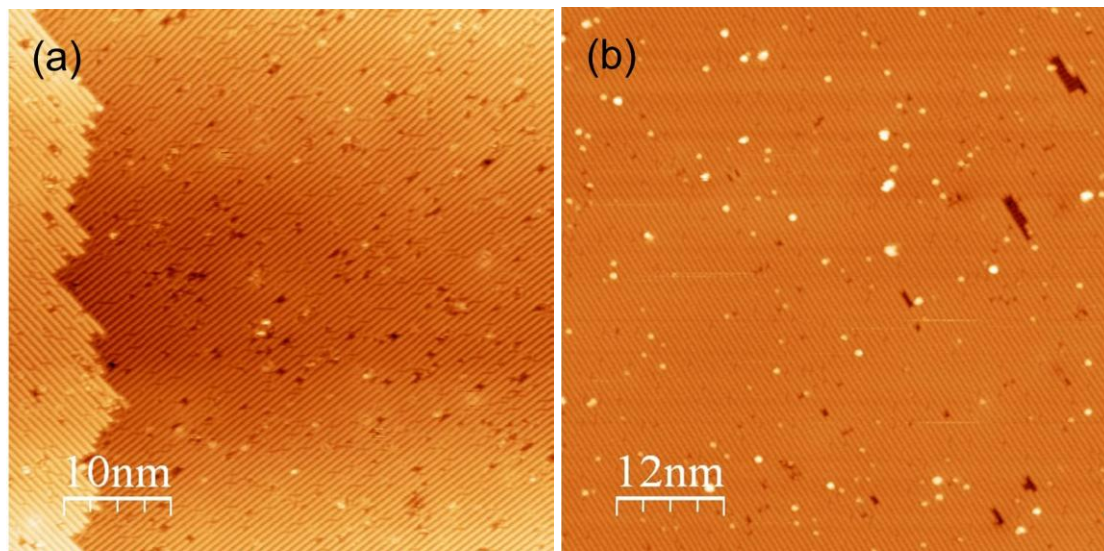


Figure 6.5: H-passivated Si (100)-2×1 surface using W filament after reduced the sample temperature to 270°C and flushed the hydrogen gas line. (a) and (b) are the STM images taken from different samples.

6.2 Nanopatterning by Hydrogen Depassivation

STM tip-based nanofabrication is a potential technique which has the capability to controllably manufacture nanostructures that approach the atomic scale. The first successful STM nanofabrication by oxidation was demonstrated by J. Dagata in 1990[93] where they demonstrated the patterning process in ambient conditions by an STM on a passivated Si (111) sample. With the presence of moisture, the oxide patterns were formed within the water meniscus between the tip and sample[92] and features with a few hundreds of nanometer size were fabricated on a Si surface. This method relies not only on the tunneling current and the bias voltage of the STM, but also on the ambient humidity. Although ambient SPM can manufacture nanopatterns on a hydrogen passivated silicon surface, it is not possible to create sub-10 nm size features or nanodevices without having detailed control of the ambient condition. To get better control of the environment and fabricate much finer patterns, it is suggested that STM nanolithography may be carried out in UHV environment, where the moisture layer on the surface can be controlled.

UHV-STM nanolithography has been established, and remarkable results have been achieved by J. Lyding *et al.*[28] They first demonstrated UHV-STM nanopatterning on a H-Si (100) reconstructed surfaces, and nanoscale features were obtained with various patterning conditions. Further investigation[86] revealed two hydrogen desorption mechanisms corresponding to two regimes of bias voltage. The direct electronic excitation mechanism can be applied in the high-bias regime (> 6.5 V), where the silicon-hydrogen bond can be excited from the σ bonding state to the σ* antibonding state (as

shown in Figure 6.6 (a)). In the low-bias regime (< 6.5 V), depassivation occurs via the multiple-electron vibrational heating mechanism, where the silicon-hydrogen bond is repeatedly excited by multiple low-energy electrons until it is ultimately breaks (as shown in Figure 6.6 (b)).

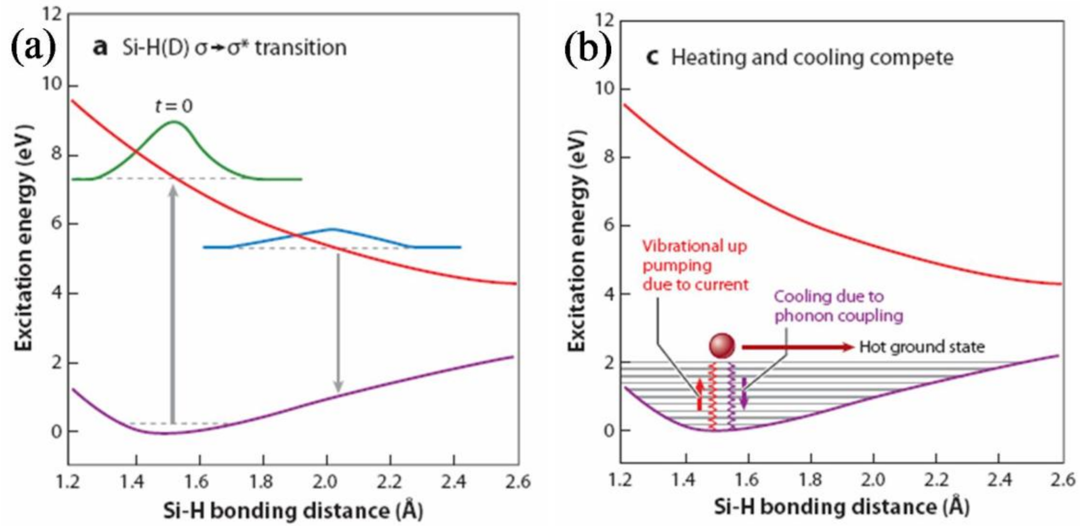


Figure 6.6: H-depassivation mechanisms. (a) demonstrates the direct electronic excitation mechanism. To excite Si-H bond from the σ state to the σ* state, a high voltage (> 6.5 V) need to be applied. The STM image (b) demonstrates the multiple-electron vibration mechanism. Multiple low-energy electrons can gradually excite the Si-H bond until it breaks. (Figure (a) from G. C. Abeln[90], and Figure (b) from M. C. Hersam[91].)

By varying the applied bias voltage in two different regimes, patterns with different sizes can be obtained to meet the requirements of APM. The hydrogen depassivation by the direct electronic excitation mechanism at high voltage depends only on the threshold voltage of 6.5 V. It is possible to depassivate a large area in a short time using this method. Hence, relatively larger structures such as reference lines, transistor bases, etc. can be fabricated by this mechanism. Figure 6.7 (a) shows a depassivated 200×200 nm^2 area created by raster scanning using this method. On the other hand, very fine patterns/structures can be created by taking advantage of the multiple-electron vibration mechanism, where the line width can be as small as 1 nm. Three parallel lines have been

fabricated using the multiple-electron vibration mechanism (Figure 6.7 (b)). The linewidth is about two dimer rows (about 1.5 nm). The linewidth can be as small as one dimer row, which is the smallest achievable definition for a line.

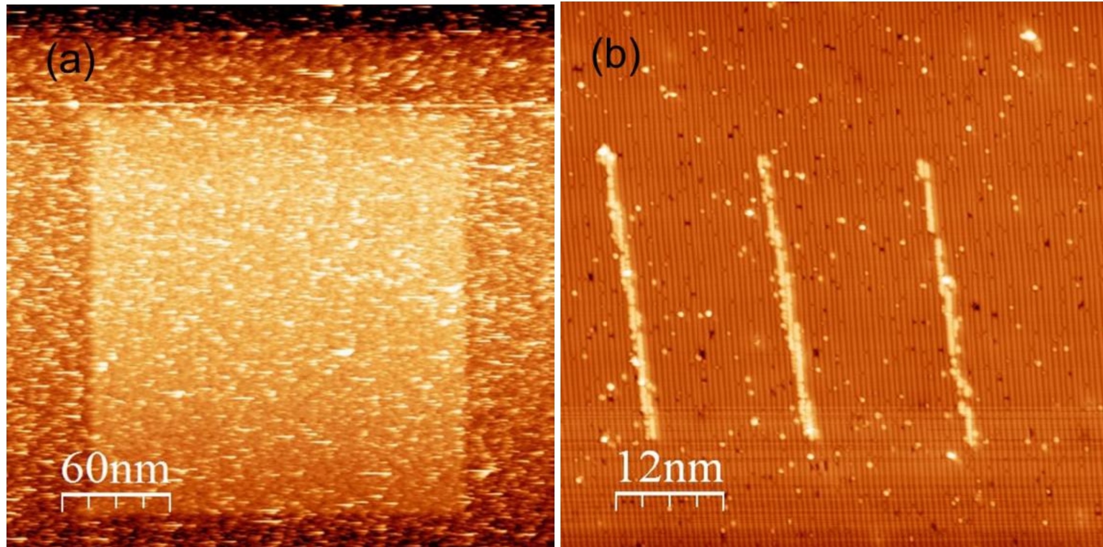


Figure 6.7: Nanopatterning results under different mechanisms. (a) shows the depassivation result using high-bias depassivation method. The STM was operated in the scanning mode with 7 V, 0.1 nA and 400nm/sec. In the STM image (b), the STM was programmed to create nanopatterns with 4.5 V, 2.5 nA and 10nm/sec.

6.2.1 Low-bias Voltage Depassivation

Hydrogen desorption in the low-bias regime is a very attractive and feasible method to fabricate nanodevices with features smaller than 10 nm. Not only it provide high precision desorption on Si surface, but also with programmable software nanometer size controllable patterns can be made. Under the threshold voltage, the hydrogen desorption yield mainly depends on two parameters: the tunneling current and the scanning speed. Needless to mention, it is always assumed that we use an atomically sharp tip which is crucial in this desorption process. In the multiple-electron vibrational heating mechanism, a large number of electrons hit the surface atoms to break Si-H bonds. So the desorption

yield is proportional to the dosage of electrons per unit area and is measured in units of C/cm.[28] This may be quantified by the following equation:

$$Q/L = (I \times t)/ (v \times t) = I/v \text{ (nA/nm/s)} = 10^{-2} * I/v \text{ (C/cm)} \quad (6.1)$$

I and v are the tunneling current in nA and writing speed in nm/s.

When we use the low-bias regime desorption process, the electron dosing rate is set between 10^{-3} - 10^{-2} C/cm to successfully desorb hydrogen atoms. When writing complicated nanopatterns with multiple features, such as a pattern array, the total writing length will be significantly increased. It makes the nanopatterning process very time consuming. Moreover, the creep of the piezo tube may cause distortions in the nanopatterns. Long writing times will also increase the chance of a 'tip change' due to the tip-surface interaction. According to equation (6.1), to keep the same dosing rate with faster writing speed, a possible alternative is to increase the bias current. But a higher bias current also increases the chance of a "tip change" because the distance between the tip and surface is closer. A very careful approach needs to be adopted to increase the hydrogen desorption yield for preserving the tip sharpness.

To find the stable working parameters of the STM tips, especially in the multiple-electron vibrational heating mechanism, nanopatterns need to be written under different writing parameters, so that we can compare the quality of the nanopatterns and choose the best working parameters. We programmed our STM so that it can write a series of test lines optimizing various writing parameters. In Figure 6.8 (a), ten test lines with different bias currents (from 1.5 nA to 2.4 nA, with 0.1 nA increment) are written on the surface. As can be seen from the desorption results (set of lines), depassivation parameters of 4 V, 2.2 nA and 2 nm/sec are the best and are used to create the parallel line pattern shown in

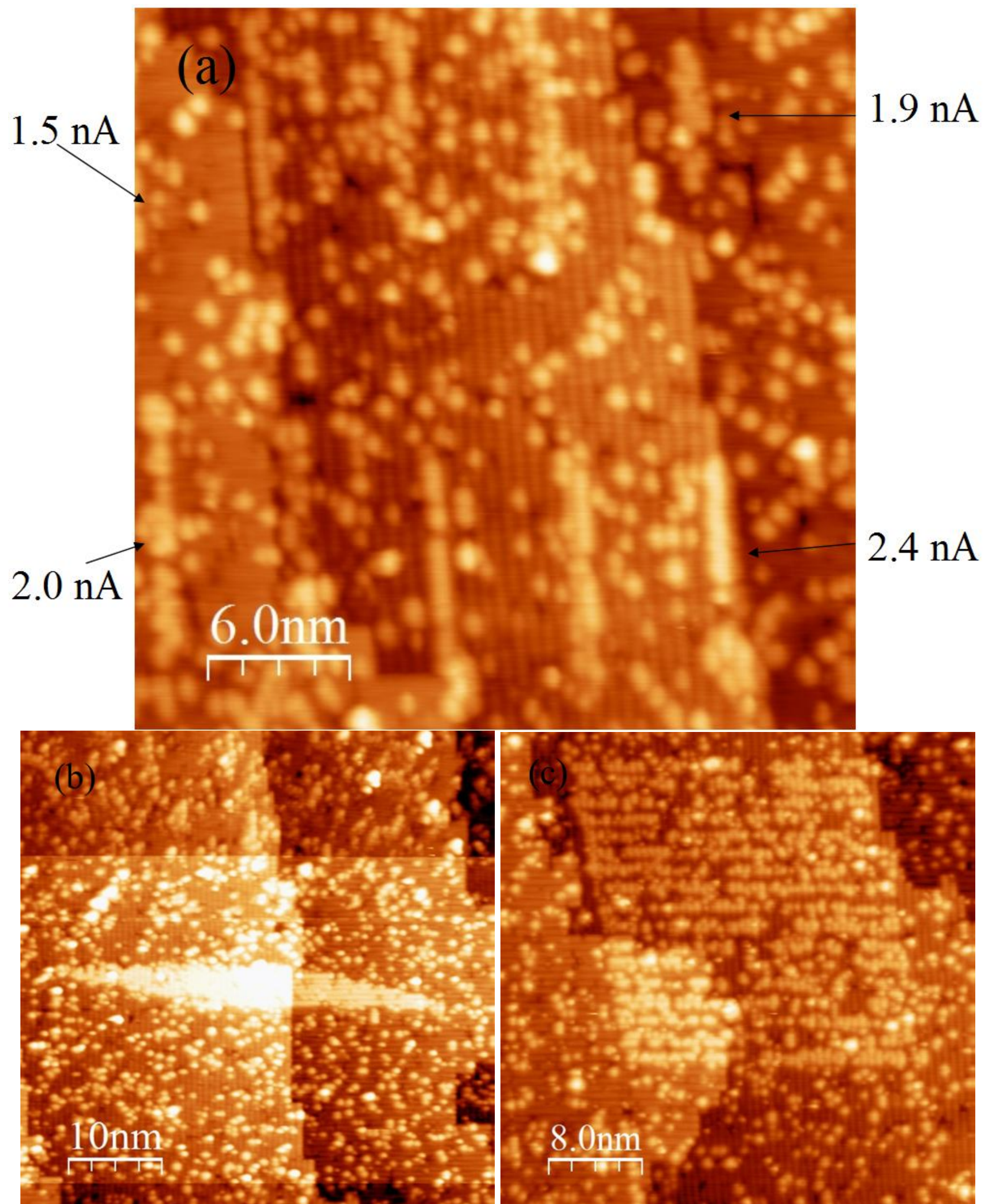


Figure 6.8: (a) Depassivated lines created at bias voltage 4 V, current 1.5-2.4 nA, writing speed 2 nm/sec. high quality lines are created under 2 nA to 2.4 nA. (b) Depassivated parallel lines with bias voltage 4 V, current 2.2 nA, writing speed 2 nm/sec. The bright area in the center is the result after depassivation. (c) same bias conditions, the writing speed has been increased to 5 nm/sec to reduce the piezotube effect. Individual lines can be recognized after depassivation.

Figure 6.8 (b). Because piezo-creep, the pattern was distorted and ultimately looked like a flat parallelogram with a bright area in the center. To offset the creeping effect, another patterning is attempted with a higher writing speed, 5 nm/sec. In this case, the parallel lines can be recognized individually (as shown in Figure 6.8 (c)).

Recently, another low-bias voltage hydrogen desorption model, referred to as the coherent resonant electron scattering model, has been used by Soukiassian *et al.*[176] to explain the low-bias depassivation mechanism. Instead of tens of electrons to vibrationally heat Si-H bond, the new model suggests a two-electron process to break the Si-H bond. Although the details of the low-bias depassivation process are not known, a large number of electrons (in both mechanisms) need to be dosed on every single Si-H bond to break the bond and create high quality nanopatterns. Nonetheless, we found that there is no significant change in depassivation for the bias voltages ranging from 4 V to 5.5 V. In the hydrogen depassivation process, the bias current and writing speed are the most important variables to determine the hydrogen desorption result.

After testing various writing conditions, we have found a set of parameters which provide us repeatable depassivation results. Figure 6.9 shows the depassivation results through two tips. These patterns were written under 4.5 V, 2.5 nA and 5 nm/sec conditions.

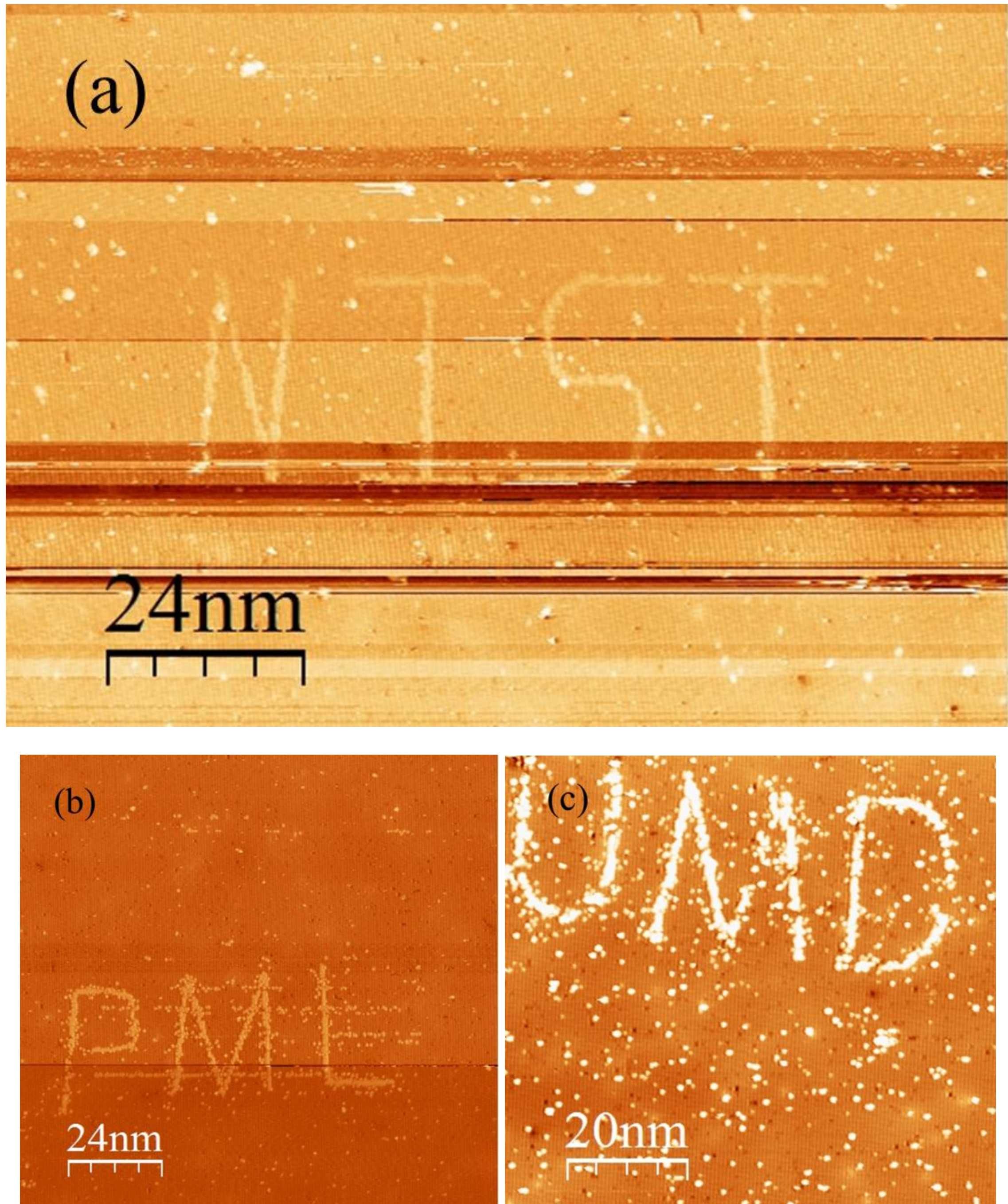


Figure 6.9: (a) 'NIST', (b) 'PML' and (c) 'UMD' have been written at bias voltage 4.5 V, current 2.5 nA, writing speed 5 nm/sec.

6.2.2 High-bias Voltage Depassivation

The high-bias depassivation process is equally important as the low-bias

depassivation and is extensively used in our experiments. The advantage of using this method is that wider lines can be fabricated in a shorter period of time. Figure 6.10 (a) shows high-bias depassivation of three 6 nm wide lines. Secondary lines (some partially broken) are also seen in the image. These are created by a secondary asperity on the tip apex. The effect of a secondary asperity becomes very prominent in the case of high voltage depassivation. This is because of the effect of field emission from the tip at a relatively large distance at high voltage. In low voltage depassivation only the closest asperity will form an active tunneling point. In the regular scanning condition, the protrusion which is the closest to the sample surface will be tunneling, and protrusions far from the very end will not contribute. On the other hand, in the high-bias voltage depassivation mode, the second closest protrusion may also field emit electrons and depassivate the surface. This double depassivation effect is not relevant for writing large patterns with multiple features, where the dimension of the patterns is relatively larger than the spacing between the multiple asperities. In Figure 6.10 (b), we demonstrate a set of large-area patterns created by using the high-bias voltage mode. The effect of a double tip cannot be seen even if there is one present.

This process can also be used to fabricate fine nanostructures (as shown in Figure 6.11 (a), (b)). In addition, various nanostructures such as zero dimensional dots (Figure 6.11 (c)), one dimensional lines and other patterns (Figure 6.11 (d)) can be fabricated within a short time.

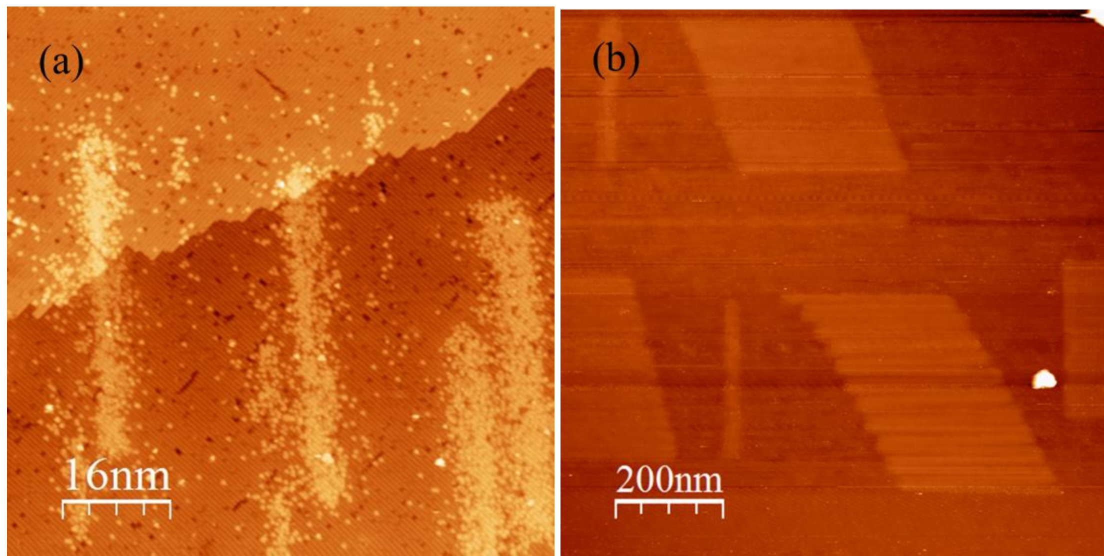
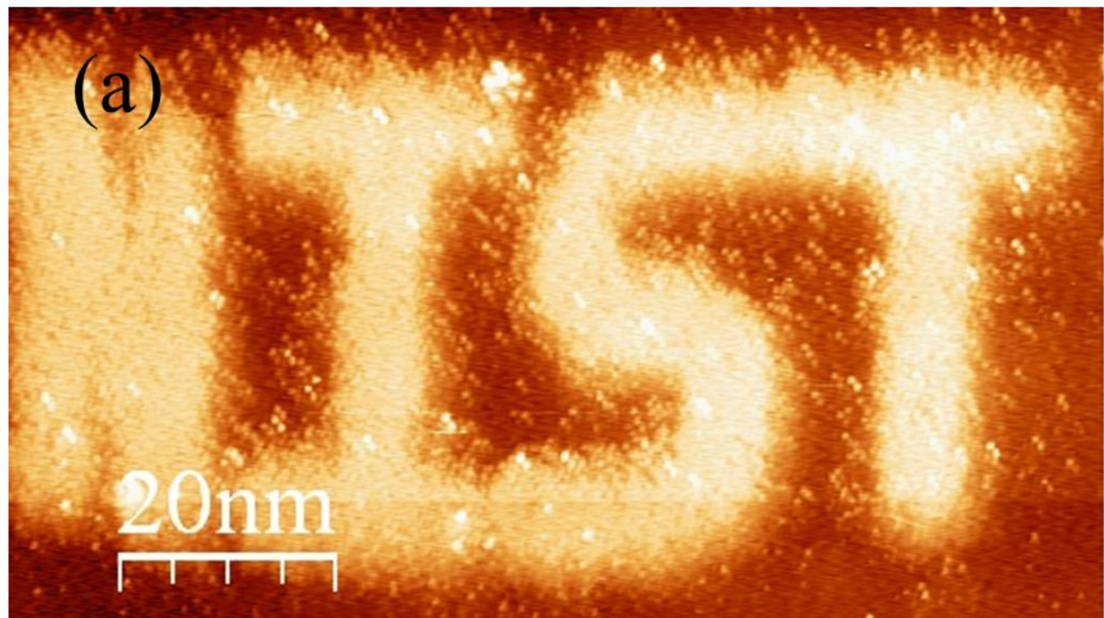


Figure 6.10: (a) fine lines litho using high-voltage mode. Writing parameters are 7 V, 0.1 nA and 10 nm/sec. Near the three continuous vertical lines, three small or disconnected lines can also be found. This is the effect of a multiple tip. (b) large pattern created under the parameters 7 V, 0.1 nA and 50 nm/sec.



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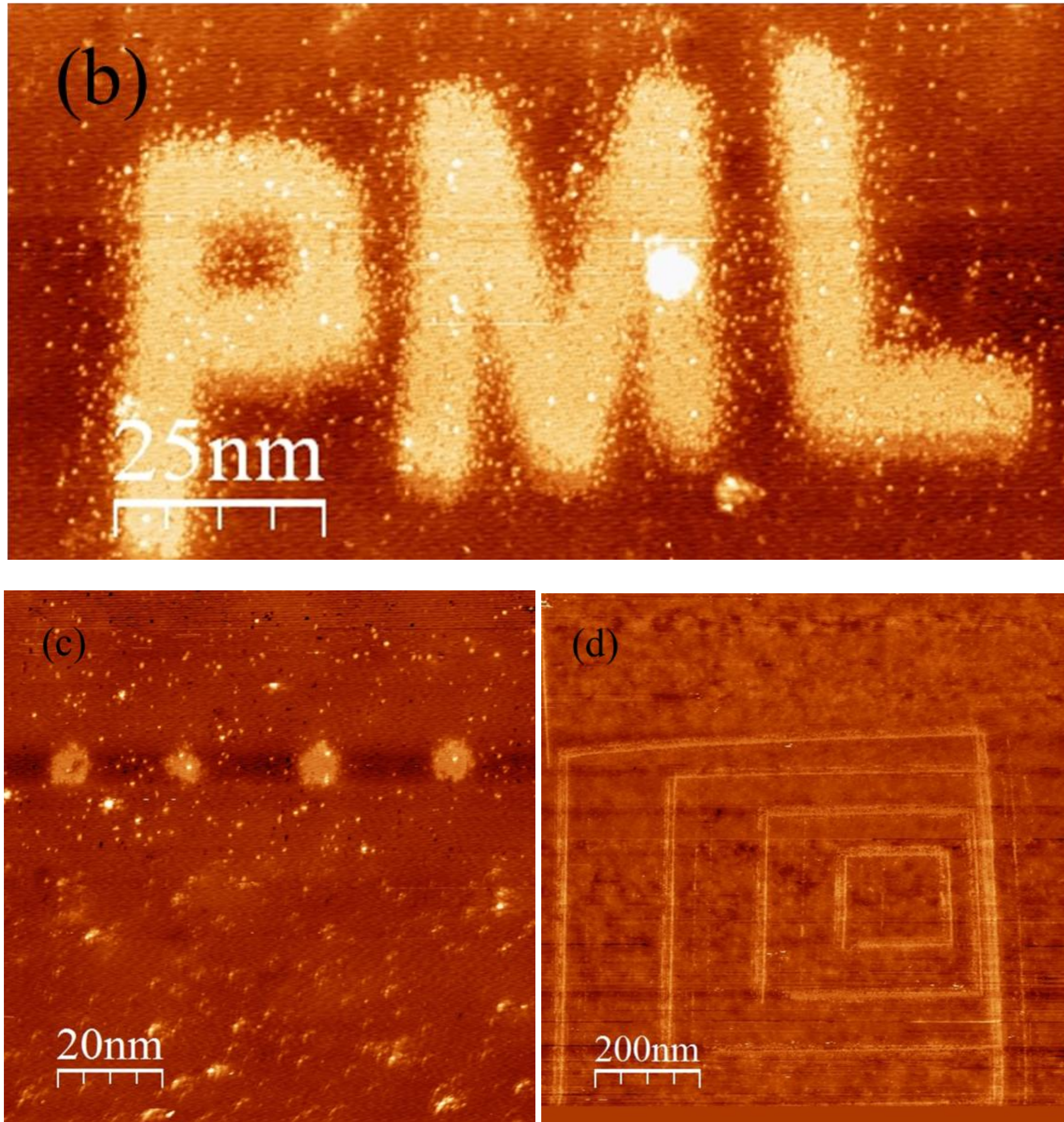


Figure 6.11: various nanopatterns fabricated by the high-bias voltage depassivation. (a) 'NIST', (b) 'PML', (c) nanodots, and (d) boxes.

6.2.3 Effect of Tips in Lithography

During the depassivation process, the stability of the tip is one of the most important factors. The structure of the STM tip can change during nanofabrication due to various tip–surface interactions. In particular, desorbed H atoms are expected to adsorb on the tip apex, thereby modifying its structure repeatedly during the fabrication of the nanopatterns.

Robust nanopatterning cannot be done without a stable, atomically sharp tip. A typical effect of the tip, namely a ‘double tip’ (multiple protrusions), is a double image or double depassivation. Typical examples are shown in Figures 4.12 and 6.10 (a).

Another observation of tip-surface interaction in our work is shown in Figure 6.12. During the depassivation process, the surface morphology can be altered. After the process, the surface became rough, and the surface roughness increased from a few angstroms to several tens of nanometers. This kind of surface damage is usually seen after the high-voltage depassivation process, and always appeared at the starting point of a pattern. We suggest that it is due to a rapid voltage change when the tip starts writing on the surface. In other words, the voltage applied on the tip changes so quickly that it can be considered as a voltage-pulse on the surface. This can largely affect the tip-surface interactions that eventually may deform the surface. To reduce this “V-pulse” effect, the voltage is ramped slowly to 7 V. As shown in Figure 6.12 (b), the depassivation results have been substantially improved after we modified the process.

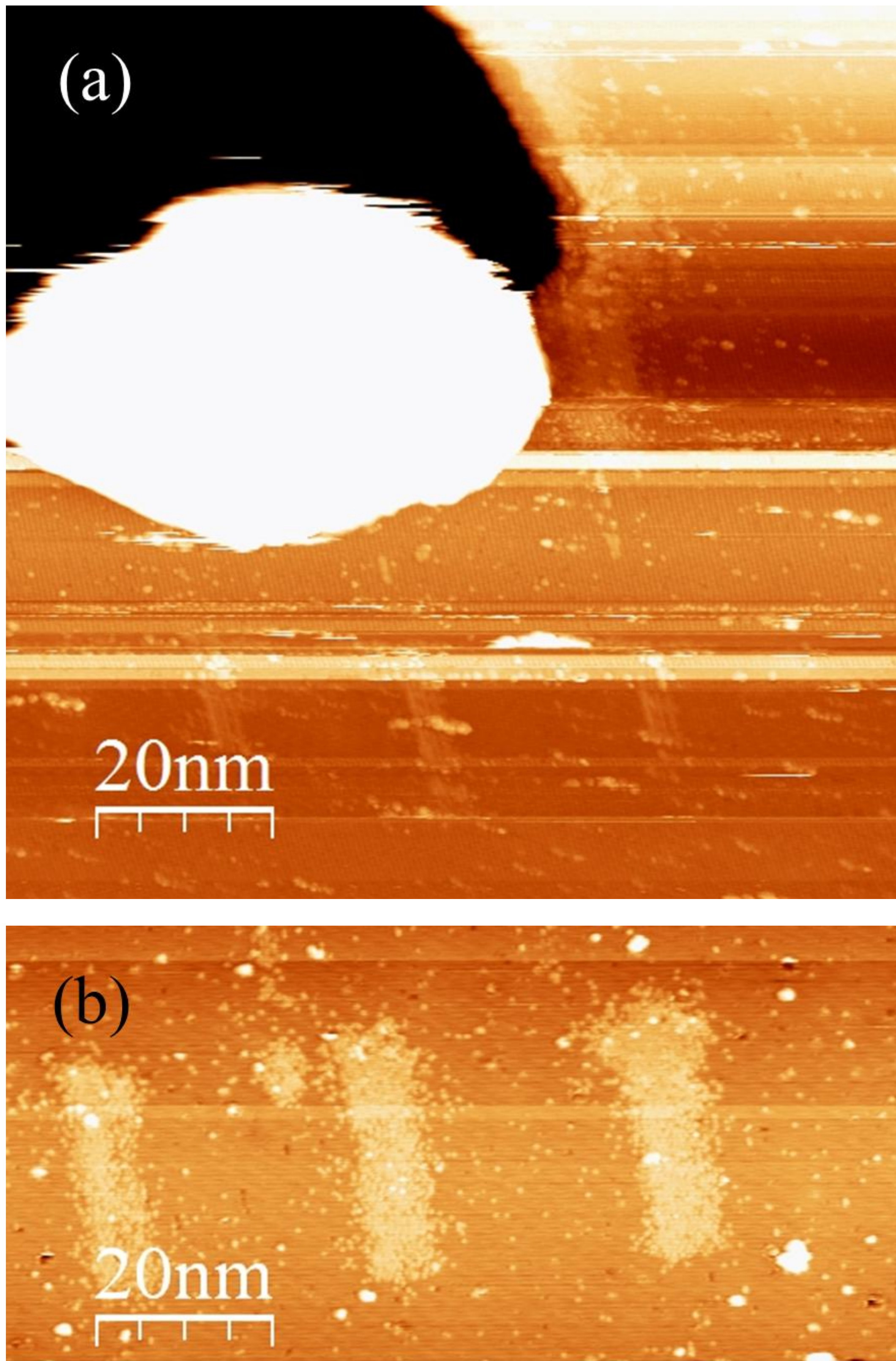


Figure 6.12: (a) Big bright "bump" appears on the surface after high-bias depassivation process. (b) Ordered depassivation lines created by the high-bias voltage process with ramped up voltage.

6.3 Locating Nanopatterns using AFM

Once nanopatterns have been fabricated, it becomes a significant practical problem to find them by using instruments other than STM where the patterns are written. The patterns written by depassivation do not produce any significant topography change. Only STM can clearly show the nanopatterns because of the variation in the electron density between the passivated and the depassivated area.

The hydrogen terminated Si (100) surface is well known as an inert surface. It is resistant to reaction and adsorption of many chemical species; it can also survive in a relatively clean state under ambient environments with humidity for several hours without being oxidized. After hydrogen atoms are desorbed, highly reactive silicon dangling bonds can easily react with inorganic or organic gas molecules and form stable structures on surface. Even metals can be deposited on the patterned areas. Following this idea, it is possible to increase the vertical dimensions (height) of the nanopatterns by such processes.

However, most of the pattern enhancement experimental images shown in the literature are *in situ* acquired by STM.[177,178,179] To be able to transfer those nanopatterns for further modification and facilitate nano-manufacturing, one needs to solve a practical problem of locating these nano-scale patterns outside the UHV-STM. The problem is so critical that it could be a “show-stopper” at the atomic scale for any nanomanufacturing that requires multiple processes using different tools. In general, without any references, patterns need to be high enough (at least 5 nm) and wide enough (few micrometer) that they can be detected by other instruments such as AFM and SEM. With the help of the fiducial marks pre-patterned on the sample surface, we are able to locate the patterns

using the AFM.

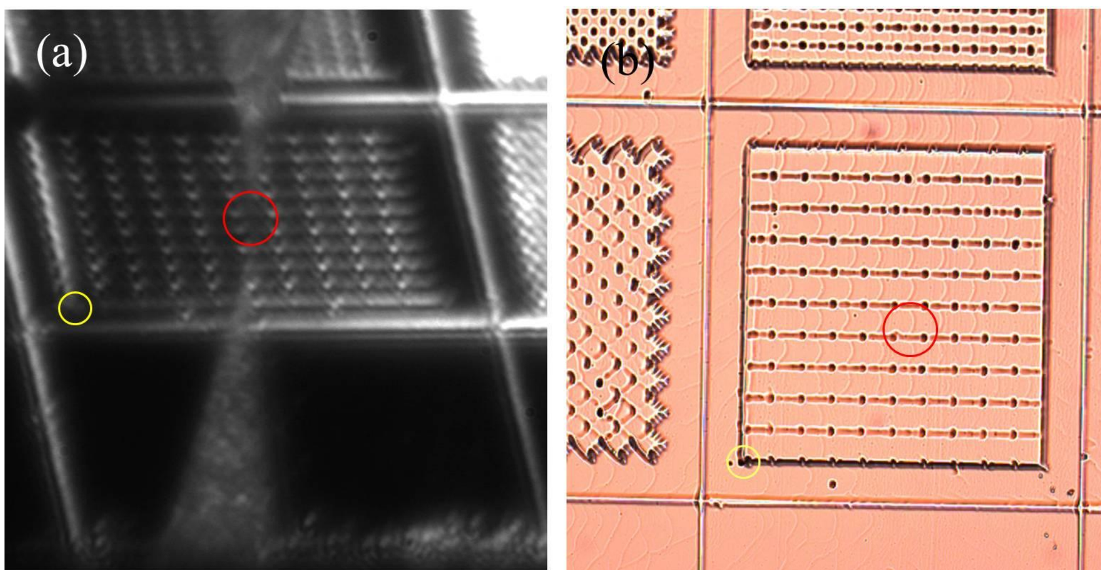
An experiment was performed to verify the idea of using the fiducial marks as references for pattern location, where an AFM was used to locate a particular area scanned using the STM. After imaging an area with an STM, the sample is taken out from the UHV system and exposed to air overnight and transferred to an ambient AFM. The microscopic tip-landing location within the fiducial patterns in terms of the fiducial mark numbering is recorded. This is done with the help of a long-distance microscope with a CCD camera. Comparing the CCD image of the *in situ* tip sample location with an *ex situ* optical image, the location can be estimated to be within two adjacent boxes (cells). Figure 6.13 (a) is taken by the long-distance microscope with the STM tip approached close to the sample surface. The STM tip can be recognized by the conical shaped feature in the upper half of the image, and the reflection of the tip can be identified in the bottom half. If we extrapolate both the tip and its reflection image, we are able to estimate the landing location, as marked by a red circle in Figs (a) and (b).

Comparing and correlating with the optical image taken *ex situ* (Figure 6.13 (b)), we can estimate the landing cell. We have used an AFM to obtain a high resolution surface image of the area (as shown in Figure 6.13 (c), (b)). Unique step-terrace patterns (step bunching and islands) from STM scans help us to identify unambiguously and compare the location during the AFM scan (Figure 6.13 (e), (f)). The location is identified to a nanometer level precision. It takes a few hours to identify and move to the exact location of the nano-scale patterns using the AFM.

Since we are at the optical limit of resolving 40 μm features at a working distance of about 30 cm, there is an uncertainty of about two 40 μm boxes (fiducials) at best

conditions using this optical microscope. The highest resolution of the long-distance microscope is 2.3 μm, which makes it impossible to focus on the end of STM tip (less than 100 nm) or its reflection on the Si surface. Because of the special design geometry of the Omicron STM chamber, the light source and the microscope can only access the sample at an angle, making it difficult to get a clear image of the approaching tip. We are currently using a highly focused light beam to enhance the quality of CCD images. We are in the process of designing and testing a new light source in combination with lenses.

In addition to this method, we have previously identified the tip landing location using the molecular measuring machine (M^3), designed and built by a different research group at NIST.[180] The M^3 is a UHV instrument with X- and Y-axis stages using interferometers. The interferometers can measure the displacement of the STM probe relative to the sample with 10 nm precision. The major challenge is to maintain UHV compatibility for all of the components. Since the typical base pressure of the M^3 is 1×10^{-7} Torr, the environment is not suitable for our sample preparation and nanopatterning processes.



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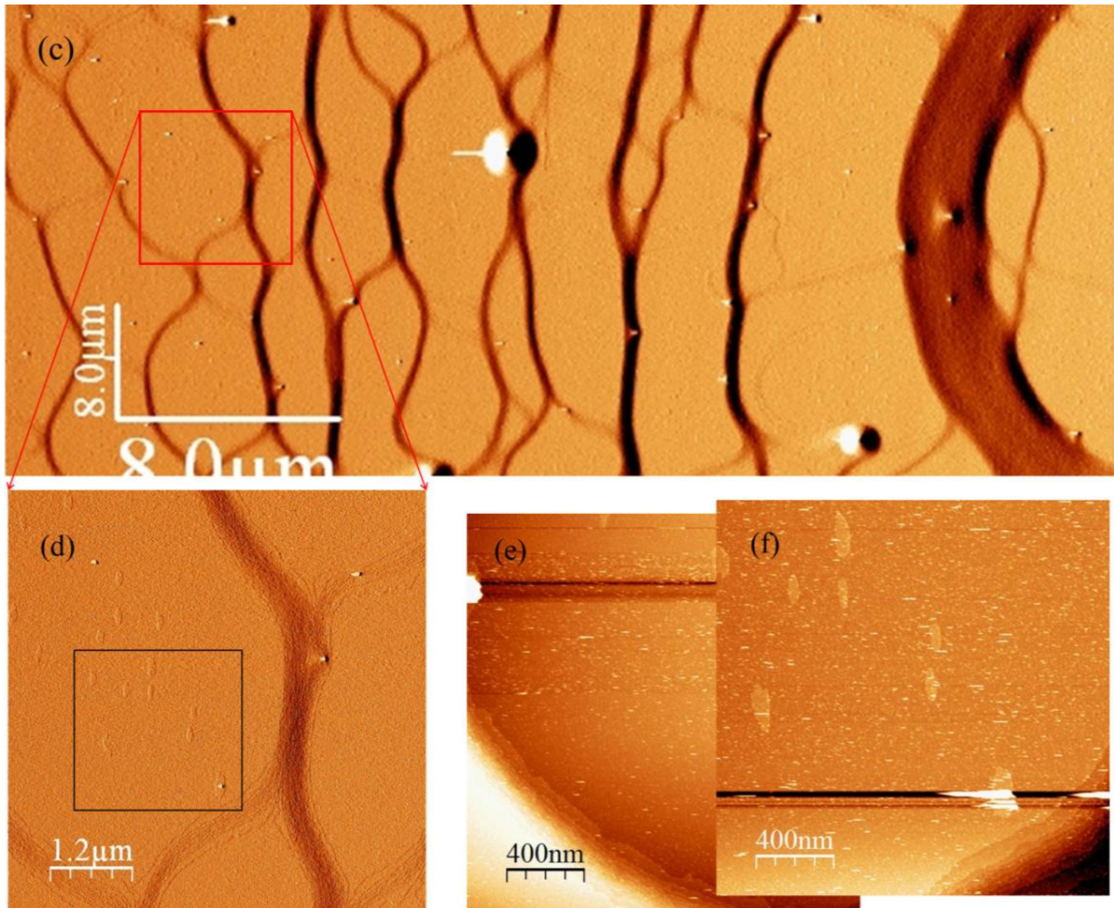


Figure 6.13: Locate tip working place via optical, AFM and STM images. (a) After the tip approached the surface, an optical image was taken by a CCD camera through the long-distance microscope, (b) optical image was *ex situ* after removing sample out of the UHV system. Yellow circles mark the zero point (reference) of the box (fiducial marks). Red circles indicate the landing location. (c) AFM image taken within the red circle marked area, and (d) an AFM image with a close up look at the red box in (c). The islands and step bunching patterns shown in STM images (e) and (f) are comparable with the patterns in image (d) (within the black box).

6.4 Nanopattern Enhancement using Oxidization Process

Since there is no hydrogen protection on the depassivated area (nanopatterns), a native oxide is formed on the silicon surface with a height of about 1 nm after several days of exposure[181] to ambient conditions. A patterned surface was exposed to ambient conditions and analyzed using an AFM. We did not observe adequate contrast in the topography to recognize the patterns. This is an indication that it is not sufficient to

depend only on the formation of a native oxide. In addition, the hydrogen passivated silicon surface may also start to degrade after two days of ambient exposure.[88] More radical methods need to be developed to enhance the oxidation of nanopatterns to produce a thicker oxide layer that can be detected by AFM.

After the patterns are oxidized, further RIE modification can be used to increase the aspect ratio of nanopatterns beyond several nanometers. During RIE etching, silicon will be etched at a relatively faster rate than the oxidized patterns (the etching ratio could be as high as 100:1[182]), leading to a formation of 3D nanostructure (pattern enhancement). These 3D nanostructures have vast applications. They can be integrated into nanoimprint technologies or can be fabricated as reference standards for dimensional nanometrology.

6.4.1 Oxidization Lithography using Ambient AFM

To optimize etching of small nanometer scale patterns, the first oxidization method we attempted is to oxidize the silicon surface concurrently while we are fabricating nanopatterns. Many reports[183, 184] show that an ambient SPM can be used for simultaneous hydrogen depassivation and the formation of oxide by utilizing the effect of ambient humidity. Oxidation occurs due to the dissociation of the water meniscus between the tip and sample.[185] Using this method, the oxide patterns can be established and then transferred into the sample using the RIE process. Although it has been reported that sub-20 nm linewidth can be achieved by varying the writing frequency and bias voltage,[186] this method heavily relies on the environmental conditions, especially the humidity level. Thus, it is very hard for us to reproduce the experiments in our lab. However, this method can be very useful for us to optimize our RIE process because it

has certain advantages over the STM patterning process. The method is relatively simpler and faster and hence it allows us to do several trials in a short period of time. Moreover, we can easily locate nanopatterns after writing because it directly writes oxide patterns having a height of ~ 2 nm.

We have used an AFM to write oxide patterns using this method and subsequently subjected it to RIE process. Figure 6.15 (a) shows an AFM topography image of an oxide pattern written by a diamond coated tip. The AFM image was obtained immediately after patterning using the same tip. Vertical lines have been written using the intermittent contact mode with bias 5 V applied to the tip, and the writing speed was 3 μm/sec. The dimensions of those oxidized lines are about 3 μm × 50 nm × 2 nm (L×W×H).

6.4.2 *In situ* Oxidization using UHV-STM

In order to achieve nanometer control of the size of the patterns and reduce the effects of the ambient environment, we are developing methods to perform *in situ* oxidization in the UHV-STM system. The challenge here is to use the right amount of number of monolayers of moisture on the sample surface without compromising the UHV system and atomic resolution. A water reservoir was connected to the transfer chamber via a leak valve to control the rate of water vapor entering the chamber. To optimize the moisture level, we performed the oxidization experiments on multiple samples with different exposure to moisture.

In the first experiment, the sample was exposed to water vapor for 1 minute at 5×10^{-8} Torr. Approximately 2 to 3 layers of H_2O molecules have been deposited. An STM image was taken after the exposure, as shown in Figure 6.14 (a). Atomic steps were still

observed. The box shown in Figure 6.14 (b) was created by the low-bias voltage process. The writing conditions are 4 V, 3 nA and 400 nm/sec. The writing voltage and current used for the vertical lines are the same as the box, 4 V and 3 nA, while we varied the writing speed (a closer view of these lines is shown in Figure 6.14 (c)).

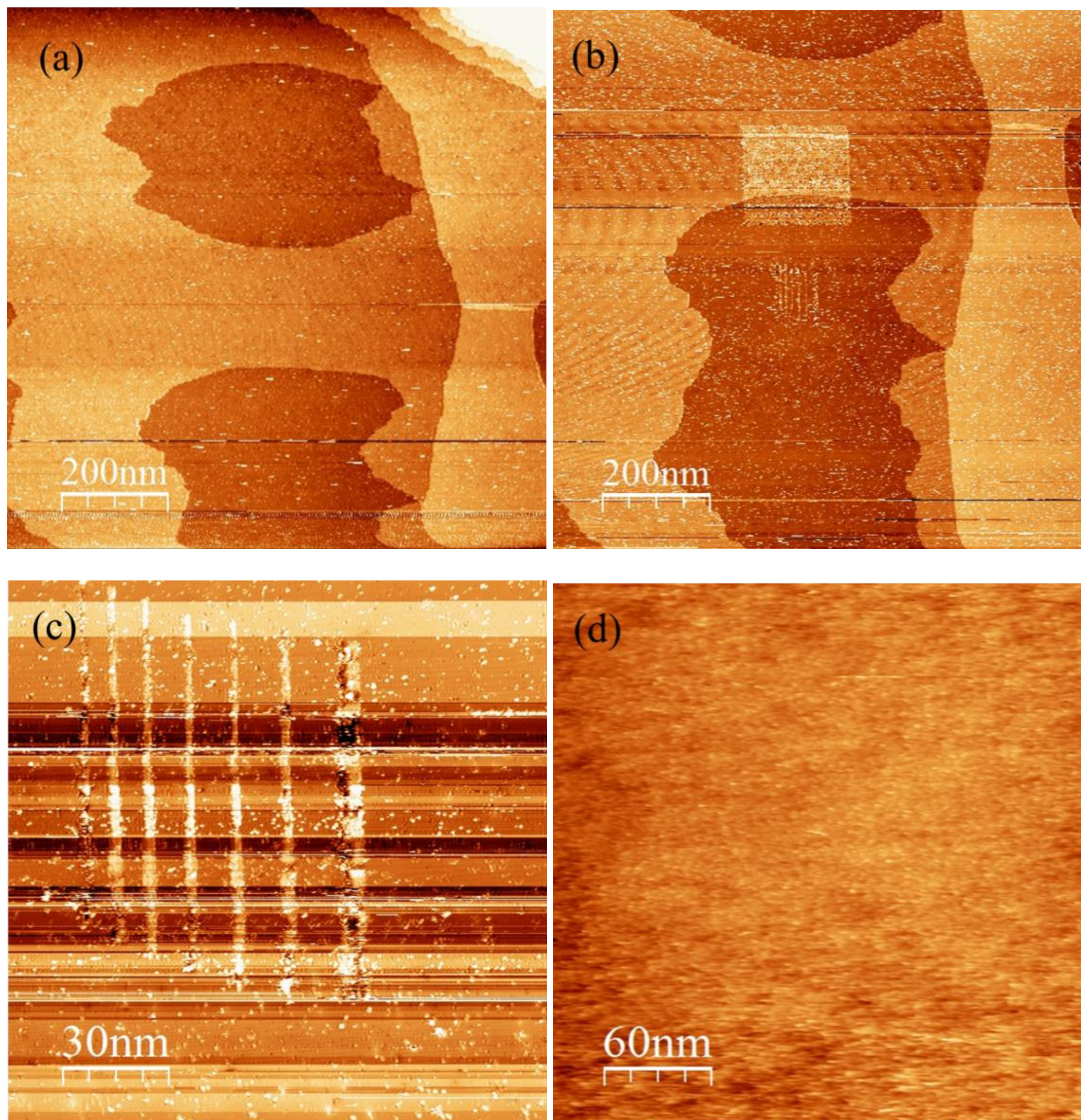


Figure 6.14: (a) an STM image is taken after the H_2O vapor exposure. (b) box and vertical lines are written on the surface. The writing conditions for the box are 4 V, 3 nA, 400 nm/s. In the image (c), the writing speeds for vertical lines are 100, 60, 80, 100, 80, 60 and 100 nm/s, respectively. (from left to right) (d) an STM image was taken after the sample was exposed to moisture at 5×10^{-7} Torr for 1 minute.

In another experiment, the water vapor pressure was set at 5×10^{-7} Torr. As shown in Figure 6.14 (d), after having been exposed for one minute, the surface became very rough,

and we were unable to recognize any steps or terraces. Additionally, it didn't form depassivated patterns after we used the depassivation processes on that place.

6.4.3 Nanopatterns *ex situ* Oxidization using Gaseous Oxygen

Another approach is to oxidize the patterns in the load lock at an elevated temperature. To accelerate the oxidation process, a halogen quartz lamp (Ushio J120V-500W) is used to radiatively heat the sample to 150°C in the load lock in the presence of an ultra-high purity oxygen gas. Because the dissociation temperature of an Si-H bond is 400°C,[187] care needs to be taken not to destroy the hydrogen-passivated area while oxidizing the nanopatterns. A thermocouple has been attached to a "dummy" sample to monitor the sample temperature with the heating lamp on. The voltage setting on the lamp was 55 V, and the sample temperature was measured to be about 150°C and 175°C after 10 minutes and 15 minutes exposure, respectively.

Nanopatterns were fabricated by the STM, as shown in Figure 6.16 (h), (i) and (j). After the elevated temperature oxidization process, an RIE process was used to oxidize the sample. After the RIE process, the nanopatterns were located by an ambient AFM (as shown in Figure 6.16 (a)).

6.4.4 Reactive Ion Etching (RIE) Process

According to our experiment results, the height of the oxidized nanopatterns is ~ 2 nm (Figure 6.15 (a)). The aspect ratio of nanopatterns needs to be increased further in order to transfer the patterns and utilize them in nanoimprint fabrication. RIE process,

being an anisotropic etching technology, can be used to further enhance the height of oxidized nanopatterns. The selectivity between Si and SiO_2 could be as high as 100:1.[182] By adjusting RIE etching parameters, we are able to create well-defined 3D nanostructures.

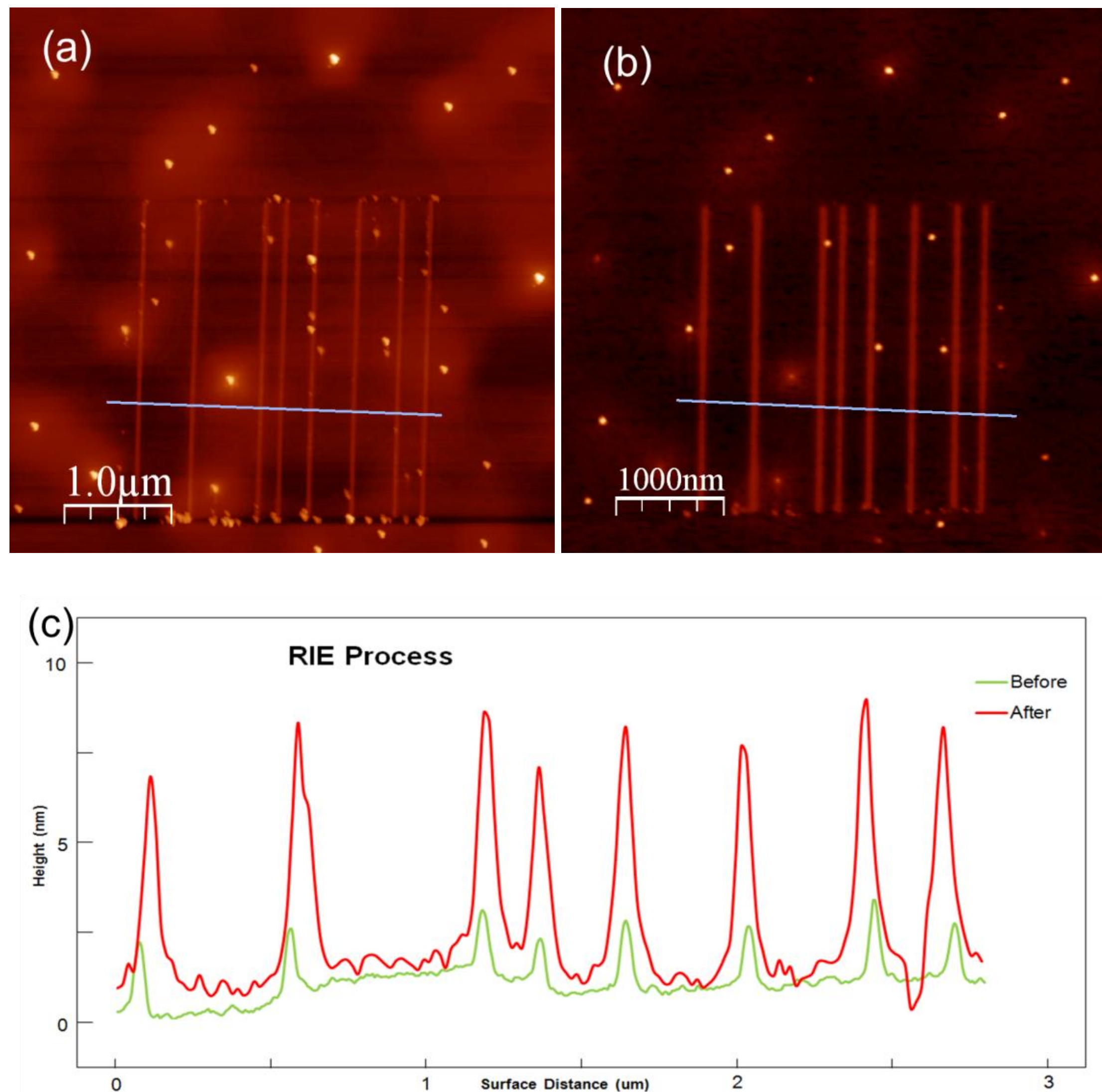


Figure 6.15: RIE experiment on oxidized lines. (a) and (b) are the AFM images taken before and after the RIE process, respectively. The line profiles in plot (c) show the height of the oxidized lines increased from 2 nm to 8 nm.

In an RIE experiment, the sample is grounded, and SF_6 is used to etch Si. A plasma is created in the system by applying a strong radio frequency (RF) electromagnetic field

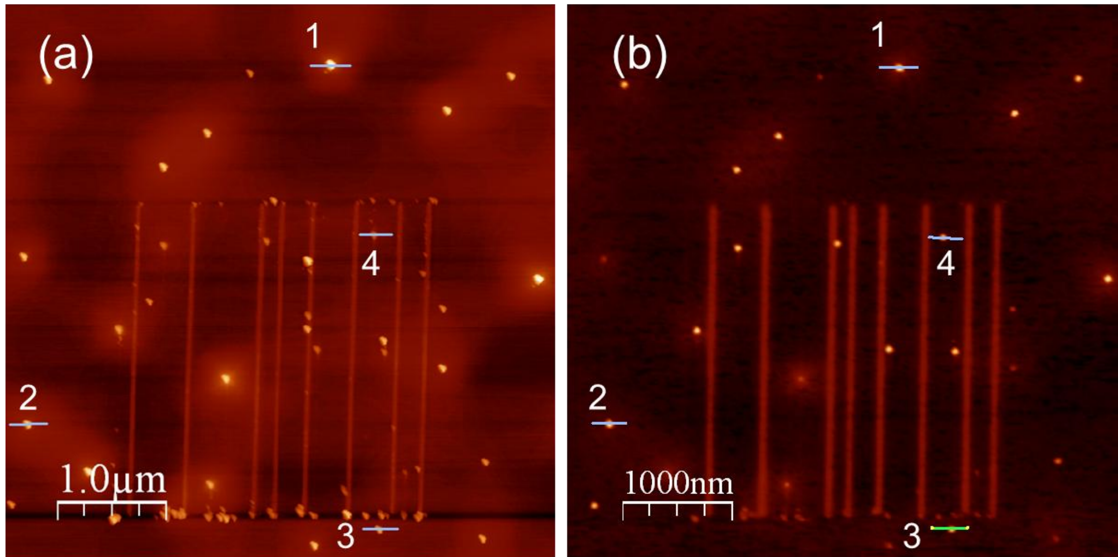
to the sample. The field is set to a frequency of 13.56 MHz, and a 500 W power setting is used. The composition of the gas used in the RIE process is mixed SF_6:O_2 in a 9:1 ratio. The sample exposure time can be varied from 5 seconds to a few minutes in the RIE process. After being exposed to the plasma for ~ 15 seconds, samples were taken out and examined by an ambient AFM.

6.5 RIE Enhancement Results and Discussion

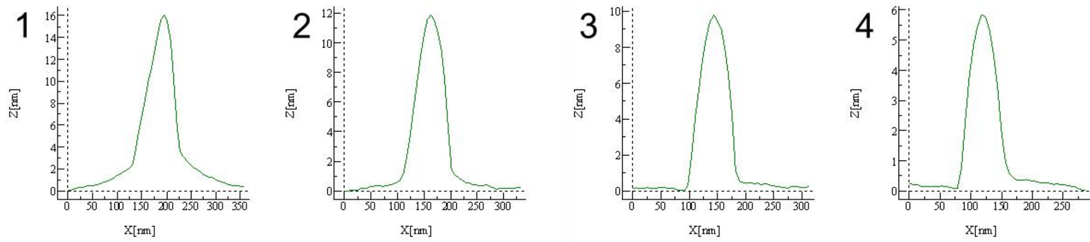
6.5.1 Enhancement of the Nanopatterns Created by AFM

The RIE is an etching technology process usually used to enhance micrometer size features in the field of nanofabrication. So far the process is not optimized for features below 100 nm and we need to test the etching capability of the features at this scale in order to take advantage of the technology for our project. An experiment was designed to verify the etching capability of the RIE process. We used an ambient AFM to create oxidized nanopatterns (method described in 6.4.1) on a Si sample with fiducial marks and subsequently subjected it to RIE process. Patterns were recognized after the RIE process with the help of fiducial marks.

Figure 6.15 (b) shows the results of the first RIE attempt on a sample with oxidized patterns. There are 8 vertical bright lines appearing in the image, which are oxide lines created by an ambient AFM. Comparing AFM data before and after RIE etching, it is clear that the height of the nanopatterns increased from 2 nm to almost 8 nm (as shown in Figure 6.15 (c)). However, due to tip convolution, it was not possible to get detailed information about the linewidth after etching.



(c) Height profile of bright dots before the RIE process



(d) Height profile of bright dots after the RIE process

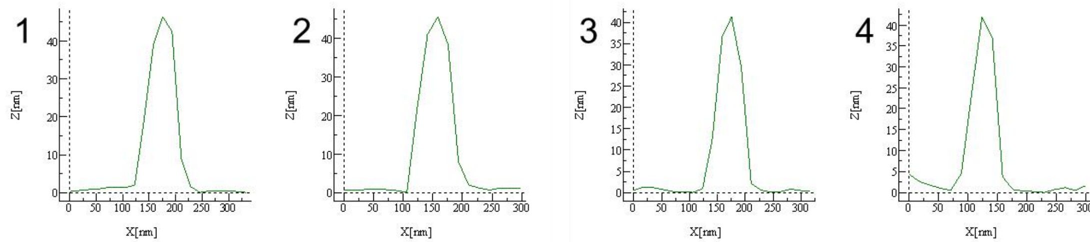


Figure 6.16: Height profiles of bright dots. (a) and (b) are the AFM images taken before and after the RIE process, respectively. The height profiles of some bright dots in plots (c) and (d) show the height of those dots increased from about 10 nm to about 50 nm.

Also we observed several bright dots on the images, which are presumably SiC because of their pyramid shape structure. After the RIE process, some of them disappeared. However, it is interesting to note the height change of the remaining dots. The average height of the brighter dots increased from about 10 nm to about 50 nm (as

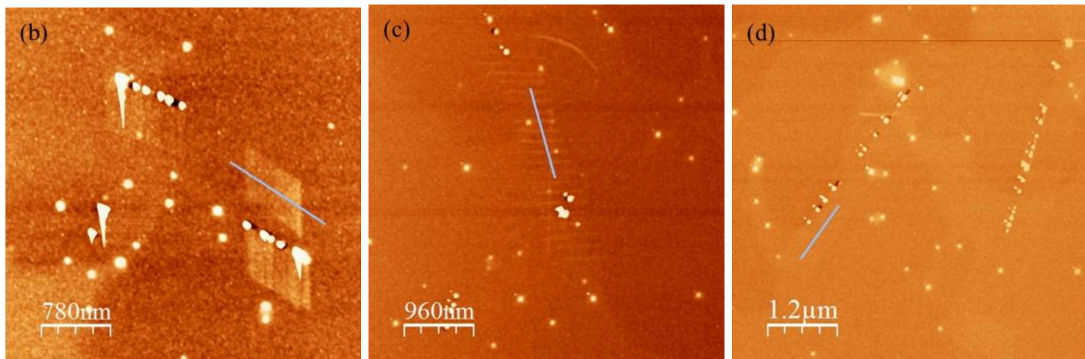
shown in Figure 6.16). As for the weaker dots that disappeared after the RIE, the initial height was about 5 nm.

It is evident from the experiments that at least 40 nm (height) of material was etched away during the etch process. Although SiO_2 is considered as a hard etch stop material compared with Si, and it last longer under plasma etching, the results show that it is in fact also etched away in the RIE process. This clearly indicates that the process parameters need to be refined in order to obtain material selectivity during the RIE process.

6.5.2 Enhancement of the Nanopatterns Created by STM

A sample patterned in the UHV-STM, oxidized in the load lock under the oxygen environment, was subjected to an RIE process. The RIE exposure time was increased to 18 seconds, while the remaining parameters were not changed. Figure 6.17 (a) shows the surface topography image using an AFM after RIE etching. Three color circles indicate the locations of the nanopatterns. A close up view of the nanopatterns is shown in Figure 6.17 (b), (c) and (d), which can be compared with the de passivated patterns fabricated by the STM in Figures 6.17 (h), (i) and (j), respectively.

The average height of the patterns after the RIE process is about 1 nm, which is much less than the result shown in Figure 6.15. A number of factors can potentially influence the etch depth in an RIE process, related either to the RIE process itself or to the oxidation process.



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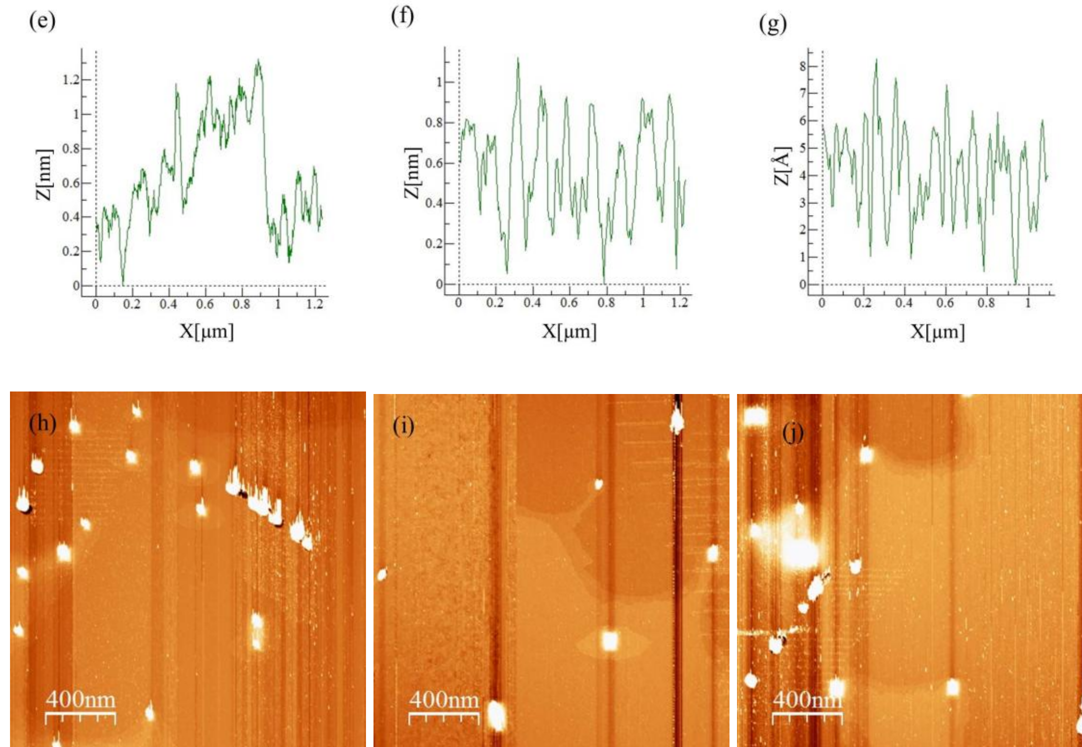

Figure 6.17: RIE experiment on the STM-based nanolithography. Image (a) is taken by an AFM. Several sets of patterns can be recognized, which are marked by color circles. (b), (c) and (d) are the AFM images zoomed into the red, blue and yellow circles, respectively. (h), (i) and (j) are the STM patterning images corresponding to (b), (c) and (d), respectively. The average height of the RIE treated patterns is 1 nm, which can be found in plots (e), (f) and (g).

With a very thin oxide layer (a few angstroms thick), we suspect that the SiO_2 hard mark can be also etched away, resulting in less height difference between the patterns and the background surface. We are now trying to optimize the oxidation temperature to improve the oxidation thickness and homogeneity and at the same time not desorb the hydrogen from the passivated surface. Previous data in the literature shows that hydrogen is desorbed from Si-H at about 700 K.[188,189] We believe that this temperature may not be the onset of desorption, but rather where the peak desorption is. Since we are trying to draw sub 5 nm patterns and oxidize them, this is a critical parameter to be optimized. Even a small amount of desorption could potentially compromise the quality

and the definition of the fine patterns. It remains unclear if we are at the optimum oxidation temperature (150°C) or oxidation pressure (~ 5 psi).

We do not yet have direct ways to measure the oxidation that results as a function of temperature for a realistic surface with some defects present. The pressure is important as well as potentially the addition of H_2O to enhance the oxidation process. A quantitative understanding would significantly speed the process development curve. We are collaborating with Prof. Wallace at the University of Texas at Dallas to simulate the Si (100) oxidization process and to optimize the oxide layer thickness on the patterns under different pressure and temperature conditions. We plan to vary the oxygen gas pressure from 1×10^{-4} Torr to 1 atm, and the oxidization temperature will be set between 150°C and 200°C.

These experiments are very time consuming and difficult as the entire multi-day process must be carried out to evaluate any given oxidation temperature or pressure. Further, any subtle variation in any of the key elements can offset those results. The process optimization is considerably slowed due to these reasons.

Although plasma etching (RIE) has been a well-established technology in the semiconductor industry for several years, it has never been optimized to the sub 10 nm scale. The effects of working pressure, gas flow ratio (SiF_6/O_2), and etching time on features with critical dimensions smaller than 10 nm needs to be investigated before they can be optimized. Since the patterns are small and delicate, we have used the RIE process at its lower limit of power and time. We have recently tested the RIE process with other samples that are patterned by AFM with oxidation lithography. Although the etching parameters were kept exactly the same, the results were considerably different. The

height of the nanopatterns did not increase significantly compared to the first RIE process on a similar sample. This clearly shows that the RIE process requires further optimization.

Another factor that can potentially influence the etching results is related to the environment during the sample transportation to the RIE station. During sample heating (for oxidization) and during exposure to air (for transportation to the RIE station), the quality of the hydrogen passivation can be degraded. The contrast in RIE depends purely on the material difference in the patterned and the non-patterned area. Even a single layer of amorphous oxide can substantially affect and even stop the RIE process.

The results obtained so far are encouraging as we have evidence from a couple of trials that the aspect ratio of the patterns can be enhanced. It is expected that parameters can be optimized within a few more experimental trials. We established a practical approach for fabrication of sub 5 nm robust features in the laboratory, that includes: 1) a high temperature UHV process to establish wide atomic terraces with few defects, 2) the hydrogen passivation process to selectively terminate silicon dangling bonds, 3) the patterning process to create features from nanometer to micrometer sizes, 4) the oxidation sequence to form a hard etch mask, and finally 5) the RIE process to enhance the aspect ratio of nanopatterns. Using this method, we will be able to create 3D features near atomic scale, which can be directly used as reference standards in dimensional metrology. This method can also be combined with the nanoimprint technology to fabricate nanodevices.

6.6 Summary and Conclusions

This chapter summarizes the efforts for developing techniques and methodology required for manufacturing at the near atomic domain. Hydrogen passivated Si (100) 2×1 samples have been used as substrates for the ABDM project and the APM. Hydrogen passivation capabilities were built into the UHV system, and a procedure was developed, tested and optimized for best results suitable for atomic precision lithography. Samples are chemically cleaned, degassed in UHV and annealed to produce surfaces suitable for passivation and lithography. The reconstructed Si surface is terminated by hydrogen atoms produced using a hydrogen cracker or a hot W-filament.

Hydrogen-passivated surfaces with a negligible number of dangling bonds were achieved on nearly perfect surfaces with minimum surface defects. These well-ordered surfaces can be used as substrates for atomic precision lithography and manufacturing. It also forms an excellent substrate for dimensional metrology applications, as the lithography patterns can be directly linked to the measurable lattice dimensions of the underlying silicon crystal lattice. A fully custom hot filament hydrogen cracker was successfully tested against a commercial atomic hydrogen source for optimum quality of passivation. The quality was checked through analysis the density of dangling bonds. These substrates could provide the basis for massively parallel nanoscale fabrication in the future.

Our optimized depassivation procedure shows that the surface can be patterned from the microscale to the atomic scale consistently. The parameters for depassivation have been optimized for various modes, particularly for the high voltage and the low voltage modes. The effects of tips on lithography have been investigated at length in order to

obtain consistency in depassivation lithography. Our tip preparation procedure needs to be modified, in order to avoid multiple asperities that compromise the quality of lithography at the sub 10 nm scale.

Fiducial marks that can be recognized by an optical microscope were introduced to enable nanopattern location outside the STM. We have also discovered that the fiducial marks facilitate a controlled surface evolution into large atomically flat terraces with well-ordered step-terrace patterns during a high-temperature annealing process. This result has turned out to be one of the important findings during the course of work for this thesis.[111]

Hard etch stop marks can be formed by oxidizing the patterns using ambient humidity or gaseous oxygen, which can help enhance the aspect ratio of the nanopatterns during an RIE process. The preliminary results indicate that the process is viable in reaching the end goal of the project. This process has never been attempted before and still requires a considerable amount of effort in fine tuning and optimization of the various process parameters that goes beyond the scope of this thesis. The study presented in the thesis, however, has clearly demonstrated a clear realizable and reliable pathway for the project to establish an innovative method in dimensional metrology as well as semiconductor device fabrication.

6.7 Future Work

Having demonstrated a method for making nanostructures, there remains a number of parameters to be optimized and improved in every step of the process. The oxidation of the patterns needs to be evaluated and optimized further to achieve thicker oxide

layers, without affecting the hydrogen passivated area. Experiments are also ongoing to improve the *in situ* oxidization process in the UHV-STM using adsorbed water molecules on the surface. The performance evaluation of the tips for patterning is also ongoing in order to achieve better control of the dimensions of the patterns in a consistent manner. It will be useful to develop a metric that can be used to evaluate the nanopatterning process and resulting nanostructures.

The process described in this thesis could be significantly improved with the use of alternative pattern enhancement techniques. Because of the exceptional etch selectivity between Al_2O_3 and Si, further work will be pursued using dimethylaluminum hydride as the precursor gas to develop Al_2O_3 masks.[105]

By creating nanostructures on silicon on insulator (SOI) wafers, one can create floating devices in nanometer scale. This will be very useful to understand some fundamental aspects of electrical conductivity of devices, such as single electron transistors.

The sub 5 nm nanopatterns eventually can be transferred and duplicated repeatedly onto other substrates using nanoimprint technology, which has vast applications in semiconductor industry. For instance, memory devices, such as dynamic random-access memory (DRAM) and static random-access memory (SRAM), contain multiple identical structures. Using the nanoimprint technology, one can reproduce identical nanostructures to be used as components in memory devices fabrication.

On the other hand, many complex structures can be created using a multiple-tip control system, which is being developed by one of our collaborators at NIST. We are

working on improving the tip fabrication process to produce ‘real’ invariant tips to achieve consistent patterning capability.

Fabrication of robust structures that are less than 5 nm are certainly within reach using the process demonstrated in this thesis based on the extensive amount of research completed. The results demonstrate that there is still a lot of room left for reducing the structure dimensions for real technological applications. Even if the process is not presently a current manufacturing solution, I hope that this thesis provides inspiration to develop a low-cost, high-efficiency tip-based nanomanufacturing process. There could be several new technologies on the horizon to take this process from the laboratory to a manufacturing level.

Appendix A

Si (100) wafer specifications

Customer:	NIST
WO #:	10-9440
Cust PO #:	515
Materials:	Cz
Surface:	Single side polished, backside etched
Orient:	<100>±0.25°
Dopant:	Boron
Diameter:	100.0 mm ± 0.3 mm
Thickness:	280 μm ± 25 μm
Resist:	0.01-0.02 ohm-cm
Pri. Flat:	32.5±2.5 mm@<100>±0.5°
Sec. Flat:	18.0±2.0 mm@90° cw±0.5°

Appendix B

The Kinetic Monte-Carlo Simulation Program

The Matlab program that was used to produce the simulation results in Chapter 5 is listed here for reference. The "run.m" is used to establish the initial conditions of the simulated surface, including simulation size, miscut angle value, fiducial marks sizes and positions, current directions, temperature, and the number of attempts. It is also used to save all the simulation data. The "checkAround.m" is used to define the position of the simulating site in one attempt. The "ProbFunction.m" determines a particular site's moving possibility to a certain direction. The algorithms of the simulation are implemented in the "move.m" file.

run.m

```
%%
clear;
clc;
%%

% area size LxL
L = 192;

% number of steps on the vertical edge of the square. W needs to be even, and L/W
should be an integer to match periodic conditions.
W = 16;

% number of steps on the horizontal edge of the square. C is even.
C = 0;
```

```
% The total number of steps.
N = W + C;

% Azimuthal miscut angle
alpha = atan(C/L);

% Polar miscut angle
beta = atan(W/L);
%%

locationAll = zeros(L + 4);

% create two vertical trenches in the center
locationAll(:, [1:18]) = -32;
locationAll(:, [179:196]) = -32;

% create one horizonal trench in the center
locationAll([83:114], :) = -32;

locationAll = locationAll + ceil(repmat(((L + 1):(-1):(-2))' * tan(beta), 1, L + 4) +
repmat(((L + 1):(-1):(-2)) * tan(alpha), L + 4, 1));
freeIndicatorAll = false(L + 4);
%%

% Temperature in Kelvin
Temperature = 1273;

% Current direction
NormalizedProbVector = ProbFunction(Temperature, 2);
locationData = zeros(L + 4, L + 4, T / frameStep + 1);
locationData(:,:,1) = locationAll;
freeIndicatorData = false(L + 4, L + 4, T / frameStep + 1);
freeIndicatorData(:,:,1) = freeIndicatorAll;

% Total number of attempts
t = 0;
T = 1000000000;

frameStep = 1000000;
imagesc(locationAll);
hold on;
[a1, a2] = find(freeIndicatorAll);
plot(a2, a1, '.k', 'MarkerSize', 3)
title(['t = ', num2str(t)])
hold off;
```

```
frameIdx = 1;
F = getframe;
F = repmat(F, 1, T / frameStep + 1);
%%

for t = 1:T
   i = randi(L);
   j = randi(L);
   [locationAll, freeIndicatorAll] = move (i, j, locationAll, freeIndicatorAll,
NormalizedProbVector);
   if(mod(t, frameStep) == 0)
      locationData(:,:,t/frameStep + 1) = locationAll;
      freeIndicatorData(:,:,t/frameStep + 1) = freeIndicatorAll;
      imagesc(locationAll);
      hold on;
      [a1, a2] = find(freeIndicatorAll);
      plot(a2, a1, '.k', 'MarkerSize', 3)
      title(['t = ', num2str(t)])
      hold off;
      frameIdx = t / frameStep + 1;
      F(frameIdx) = getframe;
   end
end
%%

imagesc(locationData(:,:,1));
hold off;
D = getframe;
D = repmat(D, 1, T/frameStep + 1);
for x = 1:T/frameStep
   imagesc(locationData(:,:,x + 1));
   hold off;
   D(x + 1) = getframe;
end
movie2avi(D, 'wall_cross_down.avi');
%%
```

---

checkAround.m

```
function [ifHigh, ifLow, nHigh, nLow, maxHigh, maxLow] = checkAround(location33)

nHigh = sum(location33([2, 4, 6, 8]) < location33(5));
nLow = sum(location33([2, 4, 6, 8]) > location33(5));
```

```
ifHigh = nHigh > 0;
ifLow = nLow > 0;
maxHigh = max(location33(5) - location33([2, 4, 6, 8]));
maxLow = min(location33(5) - location33([2, 4, 6, 8]));
end
```

ProbFunction.m

```
function NormalizedProbVector = ProbFunction(Temperature, CurrentDirection, Edrift,
Efastdiffusion, Eslowdiffusion)

% Boltzmann constant in eV/K units
k = 8.617343e-5;
if nargin < 2
% default current direction up
   CurrentDirection = 2;
end

if nargin < 3
% Moving energy induced by current, units in eV
   Edrift = -0.18;
end

if nargin < 4
% Diffusion energy alone dimer rows, units in eV
   Efastdiffusion = 0.67;

% Diffusion energy perpendicular to dimer rows, units in eV
   Eslowdiffusion = 0.76;
end

Prob1 = 1 / (1 + exp(Efastdiffusion / (k * Temperature)));
Prob2 = 1 / (1 + exp((Efastdiffusion + Edrift) / (k * Temperature)));
Prob3 = 1 / (1 + exp((Efastdiffusion - Edrift) / (k * Temperature)));
Prob4 = 1 / (1 + exp(Eslowdiffusion / (k * Temperature)));
Prob5 = 1 / (1 + exp((Eslowdiffusion + Edrift) / (k * Temperature)));
Prob6 = 1 / (1 + exp((Eslowdiffusion - Edrift) / (k * Temperature)));

switch CurrentDirection
   case 1
% current direction left
      ProbVector1 = [Prob2 Prob4 Prob3 Prob4];
```

```
        ProbVector2 = [Prob5 Prob1 Prob6 Prob1];
    case 2
% current direction up
        ProbVector1 = [Prob1 Prob5 Prob1 Prob6];
        ProbVector2 = [Prob4 Prob2 Prob4 Prob3];
    case 3
% current direction right
        ProbVector1 = [Prob3 Prob4 Prob2 Prob4];
        ProbVector2 = [Prob6 Prob1 Prob5 Prob1];
    case 4
% current direction down
        ProbVector1 = [Prob1 Prob6 Prob1 Prob5];
        ProbVector2 = [Prob4 Prob3 Prob4 Prob2];
    otherwise
        error('Invalid current direction!');
end

ProbMax = max([sum(ProbVector1), sum(ProbVector2)]);
NormalizedProbVector = [ProbVector1 / ProbMax; ProbVector2 / ProbMax];
end
```

---

move.m

```
function [locationAllNew, freeIndicatorAllNew] = move (i, j, locationAll,
freeIndicatorAll, NormalizedProbVector)

locationAllNew = locationAll;
freeIndicatorAllNew = freeIndicatorAll;
L = size(locationAllNew, 1) - 4;

if(i < 1 || i > L || j < 1 || j > L)
    error('Point coordinate out of bound!');
end

I = i + 2;
J = j + 2;
[ifHigh, ifLow, nHigh, nLow] = checkAround(locationAllNew((I - 1):(I + 1), (J - 1):(J +
1)));

% adatom formation
% detachment coefficient depends on number of adjacent atoms
if ~freeIndicatorAllNew(I, J) && ~ifHigh && ifLow && rand() < 4^(nLow - 4)
```

```
    locationAllNew = locationChange(I, J, locationAllNew, -1);
% climb over a step due to step-down drifting
    if ~freeIndicatorAllNew(I + 1, J) && rand() < 0.25
        freeIndicatorAllNew = freeIndicatorChange(I + 1, J, freeIndicatorAllNew);
    else freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
    end
    [ifHigh, ifLow] = checkAround(locationAllNew((I - 1):(I + 1), (J - 1):(J + 1)));
end

% adatom moving algorithm
% determine the moving direction
if freeIndicatorAllNew(I, J)
    moveDirection = movingPossbility(I, J, locationAll, NormalizedProbVector);
    switch moveDirection

% move left
        case 1
% adatom approaching a step from the lower terrace
            if locationAllNew(I, J - 1) < locationAllNew(I, J)
% impremeability factor is 0.8
                if rand() < 0.8
                    if ~ifLow
% adatom incorporate into a step
                        freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
                        locationAllNew = locationChange(I, J, locationAllNew, 1);
                    end
% adatom passes across a step
                elseif ~freeIndicatorAllNew(I, J - 1) && locationAllNew(I, J) ==
locationAllNew(I, J - 1) + 1
                    freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
                    freeIndicatorAllNew = freeIndicatorChange(I, J - 1, freeIndicatorAllNew);
                end
% adatom drifting
            elseif locationAllNew(I, J - 1) >= locationAllNew(I, J) &&
~freeIndicatorAllNew(I, J - 1)
                freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
                freeIndicatorAllNew = freeIndicatorChange(I, J - 1, freeIndicatorAllNew);
                [ifHigh, ifLow, nHigh, nLow, maxHigh, maxLow] =
checkAround(locationAllNew((I - 1):(I + 1), (J - 2):J));
% adatom approaching a step from the upper terrace
                if ifHigh && ~ifLow && rand() < 4^(nHigh - 4) || maxHigh >= 2
                    freeIndicatorAllNew = freeIndicatorChange(I, J - 1, freeIndicatorAllNew);
                    locationAllNew = locationChange(I, J - 1, locationAllNew, 1);
                end
            end
```

```
% move up
    case 2
      if locationAllNew(I - 1, J) < locationAllNew(I, J)
        if rand() < 0.8
          if ~ifLow
            freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
            locationAllNew = locationChange(I, J, locationAllNew, 1);
          end
        elseif ~freeIndicatorAllNew(I - 1, J) && locationAllNew(I, J) ==
locationAllNew(I - 1, J) + 1
          freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
          freeIndicatorAllNew = freeIndicatorChange(I - 1, J, freeIndicatorAllNew);
        end
      elseif locationAllNew(I - 1, J) >= locationAllNew(I, J) &&
~freeIndicatorAllNew(I - 1, J)
        freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
        freeIndicatorAllNew = freeIndicatorChange(I - 1, J, freeIndicatorAllNew);
        [ifHigh, ifLow, nHigh, nLow, maxHigh, maxLow] =
checkAround(locationAllNew((I - 2):I, (J - 1):(J + 1)));
        if ifHigh && ~ifLow && rand() < 4^(nHigh - 4) || maxHigh >= 2
          freeIndicatorAllNew = freeIndicatorChange(I - 1, J, freeIndicatorAllNew);
          locationAllNew = locationChange(I - 1, J, locationAllNew, 1);
        end
      end

% move right
    case 3
      if locationAllNew(I, J + 1) < locationAllNew(I, J)
        if rand() < 0.8
          if ~ifLow
            freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
            locationAllNew = locationChange(I, J, locationAllNew, 1);
          end
        elseif ~freeIndicatorAllNew(I, J + 1) && locationAllNew(I, J) ==
locationAllNew(I, J + 1) + 1
          freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
          freeIndicatorAllNew = freeIndicatorChange(I, J + 1, freeIndicatorAllNew);
        end
      elseif locationAllNew(I, J + 1) >= locationAllNew(I, J) &&
~freeIndicatorAllNew(I, J + 1)
        freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
        freeIndicatorAllNew = freeIndicatorChange(I, J + 1, freeIndicatorAllNew);
        [ifHigh, ifLow, nHigh, nLow, maxHigh, maxLow] =
checkAround(locationAllNew((I - 1):(I + 1), J:(J + 2)));
        if ifHigh && ~ifLow && rand() < 4^(nHigh - 4) || maxHigh >= 2
          freeIndicatorAllNew = freeIndicatorChange(I, J + 1, freeIndicatorAllNew);
```

```
                locationAllNew = locationChange(I, J + 1, locationAllNew, 1);
            end
        end

% move down
    case 4
        if locationAllNew(I + 1, J) < locationAllNew(I, J)
            if rand() < 0.8
                if ~ifLow
                    freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
                    locationAllNew = locationChange(I, J, locationAllNew, 1);
                end
            elseif ~freeIndicatorAllNew(I + 1, J) && locationAllNew(I, J) ==
locationAllNew(I + 1, J) + 1
                freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
                freeIndicatorAllNew = freeIndicatorChange(I + 1, J, freeIndicatorAllNew);
            end
        elseif locationAllNew(I + 1, J) >= locationAllNew(I, J) &&
~freeIndicatorAllNew(I + 1, J)
            freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAllNew);
            freeIndicatorAllNew = freeIndicatorChange(I + 1, J, freeIndicatorAllNew);
            [ifHigh, ifLow, nHigh, nLow, maxHigh, maxLow] =
checkAround(locationAllNew(I:(I + 2), (J - 1):(J + 1)));
            if ifHigh && ~ifLow && rand() < 4^(nHigh - 4) || maxHigh >= 2
                freeIndicatorAllNew = freeIndicatorChange(I + 1, J, freeIndicatorAllNew);
                locationAllNew = locationChange(I + 1, J, locationAllNew, 1);
            end
        end
  end
end
end


function freeIndicatorAllNew = freeIndicatorChange(I, J, freeIndicatorAll)
freeIndicatorAllNew = freeIndicatorAll;
L = size(freeIndicatorAllNew, 1) - 4;
for II = (I - L):L:(I + L)
  for JJ = (J - L):L:(J + L)
    if 1 <= II && II <= L + 4 && 1 <= JJ && JJ <= L + 4
      freeIndicatorAllNew(II, JJ) = ~freeIndicatorAllNew(II, JJ);
    end
  end
end
end

function locationAllNew = locationChange(I, J, locationAll, nStep)
```

```
locationAllNew = locationAll;
L = size(locationAllNew, 1) - 4;
for II = (I - L):L:(I + L)
   for JJ = (J - L):L:(J + L)
      if 1 <= II && II <= L + 4 && 1 <= JJ && JJ <= L + 4
         locationAllNew(II, JJ) = locationAllNew(II, JJ) - nStep;
      end
   end
end
end

function moveDirection = movingPossbility(I, J, locationAll, NormalizedProbVector)
R = rand();
locationAllNew = locationAll;
ProbVec = NormalizedProbVector(mod(locationAllNew(I, J), 2) + 1, :);
if R <= ProbVec(1)
   moveDirection = 1;
elseif R <= ProbVec(1) + ProbVec(2)
   moveDirection = 2;
elseif R <= ProbVec(1) + ProbVec(2) + ProbVec(3)
   moveDirection = 3;
elseif R <= ProbVec(1) + ProbVec(2) + ProbVec(3) + ProbVec(4)
   moveDirection = 4;
else moveDirection = 0;
end
end
```

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