

## ABSTRACT

Title of dissertation: INFORMATION POWER EFFICIENCY  
TRADEOFFS IN MIXED SIGNAL  
CMOS CIRCUITS

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Increasingly sensors for biological applications are implemented using mixed signal CMOS technologies. As feature sizes in modern technologies decrease with each generation, the power supply voltage also decreases, but the intrinsic noise level increases or remains the same. The performance of any sensor is quantified by the weakest detectable signal, and noise limits the ability of a sensor to detect the signal. In order to explore the trade-offs among incoming signal, the intrinsic physical noise of the circuit, and the available power resources, we apply basic concepts from information theory to CMOS circuits. In this work the circuits are modeled as communication channels with additive colored Gaussian noise and the signal transfer characteristics and noise properties are used to determine the classical Shannon capacity of the system. The waterfilling algorithm is applied to these circuits to obtain the information rate and the bit energy is subsequently calculated.

In this dissertation we restricted our attention to operational transconductance amplifiers, a basic building block for many circuits and sensors and oftentimes

a major source of noise in a sensor system. It is shown that for typical amplifiers the maximum information rate occurs at bandwidths above the dominant pole of the amplifier where the intrinsic physical circuit noise is diminished, but at the same time the output signal is attenuated. Thus these techniques suggest a methodology for the optimal use of the amplifier, but in many cases it is not practical to use an amplifier in this manner, that is at frequencies above its 3dB cutoff. Further, a direct consequence of applying the classic waterfilling algorithm leads to the idea of using modulation techniques to optimize system performance by shifting signals internally to higher frequencies, providing a practical means to achieve the information rates predicted by waterfilling and at the same time maintaining the real world application of these amplifiers. In addition, the information rates and bit energy for basic CMOS amplifier configurations are studied and compared across configurations and processes. Further the additional design constraints formed by adding the information rate and the bit energy to traditional design characteristics is explored.

INFORMATION POWER EFFICIENCY TRADEOFFS  
IN MIXED SIGNAL CMOS CIRCUITS

by

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# Chapter 1

## Introduction

### 1.1 Motivation

In recent years there has been a substantial amount of research into designing biosensors for particular applications. These sensors may include electrical activity sensors, such as to amplify weak extracellular signals of cells, capacitive sensors to monitor the motility and health of cells or fluorescence sensors which can be used for a wide variety of applications in biology including imaging and analyte detection and quantification. These sensors have general applicability in drug screening, explosives detection and clinical diagnosis just to name a few [1–8].

In these applications, however, one of the greatest concerns is with being able to detect signals that are very small. This implies that the power level of the input signal is an important factor to be considered. In addition each biosensor, particularly if implemented using integrated circuits, has a substantial intrinsic physical noise associated with it in addition to the environmental noise. This may change from process to process and is very much dependent on physical design parameters.

Finally many of these biosensors are meant to be used in portable and/or lab-on-a-chip applications. In these types of applications the available power resources are typically extremely limited. There therefore exists the need to consider these three factors (input signal level, noise and available power resources) when designing

biosensors. Studying the trade-offs between these three will give valuable insight into creating or improving design methodologies for more efficient sensors. To accomplish this the information rate was used to give a measure of trade-offs involved with the input signal power level and the physical noise of the channel, where the channel is the portion of the sensor that accomplishes the transduction of the signal of interest into a form that can be further analyzed or stored. Additionally the concept of bit energy, which is defined as the ratio of the system power to the information rate, is employed to incorporate a measure of the available power resources.

## 1.2 Impact of this work in Mixed Signal Design

In today's world many portable and lab-on-chip biosensors are implemented using a CMOS technology platform due to the low cost and the maturity of the technology. The trend in current CMOS processes is to scale down in size to get more transistors in a given area. This comes with a corresponding decrease in the power supply, but the intrinsic noise remains the same. This causes an increase in the overall signal to noise ratio. Understanding the trade-offs between the input signal of interest, the available power and the noise is the driving force of this work. When designing an application specific system, designers have many options to choose from to optimize a particular design. These options are typically specific to the application of the system, for example an amplifier which amplifies neural signal recordings has a different set of optimization goals than an imager whose task it is to perform signal processing on a captured image. A typical design cycle

progresses in such a way that a few parameters must be chosen at the outset, and these parameters are then used to find other parameters and system characteristics. The design is then simulated and manually adjusted to obtain what one hopes is the optimum design.

In pure digital design there are many optimization tools available which allow one to optimize for power, area and other factors. There also exists many synthesis tools which can aid the designer in the circuit design. No such tools currently exist in general analog design (at least for a wide range of applications), and designing analog and mixed signal circuits tend to be somewhat of an art rather than rigorous implementations of specific design rules that are can be repeatedly followed. There is also very little understanding of how to optimize for trade offs in mixed signal design, for example in OTA design one's goal may be to achieve the maximum open loop gain, while at the same time attempting to minimize noise, and also ensuring that the amplifier is stable. But while CMRR, CMR, PSRR and other constraints are usually calculated they are usually calculated after the design has already been chosen.

In order to bring the analog and mixed signal world closer to having a similar set of design tools as in pure digital design, this dissertation explores how to use principles of information theory and apply them to mixed signal circuits in order to optimize the energy efficiency of the design. As stated before, the mixed signal VLSI designer has many options and constraints while creating a design. Often they must critically consider power consumption and noise characteristics of the intended system. To date there is no standard figure of merit that considers an

optimum balance among input signal power level, power consumed by the circuit, and intrinsic noise characteristics, especially when considering different processes and topologies. It has been recently proposed that by applying the principles of information theory circuits can be treated as Gaussian channels with additive noise and a measure of signal power to noise level efficiency can be computed. By further considering the cost of using the circuit (power consumption) we can obtain a figure of merit which encompasses both noise sources and power considerations [9,10].

As fabrication processes allow the use of smaller and smaller transistors, intrinsic MOSFET noise becomes one of the most important limiting factors for circuit design. This can be especially important in sensor design. For any circuit, and for amplifiers in particular, noise places important limits on the input signal. This can be especially important in neural amplifier applications where the sensed input is in the  $\mu V$  range. In all circuits there are two classes of noise sources present. First there is noise due to physical processes such as thermal, shot and flicker noise, the second is the noise due to process variations. Both of these have an effect on the circuit. This work focuses on studying a specific class of amplifiers known as operational transconductance amplifiers (OTA) that are typical subcomponents used in sensor design.

Traditional analog design considerations include gain, bandwidth and stability. However optimizations of most of these factors are typically applied in a somewhat ad hoc manner. This means that there is some need for a rigorous methodology in mixed signal design.

Traditional design considerations for an OTA usually derive from wanting it



to be low noise and high open loop gain. There is not usually an area consideration for an OTA since it is usually relatively small. If feedback is used, however, then area can become a limiting factor for certain applications as passive components require significant area resources in most integrated circuit technologies.

In this work we consider the introduction of additional design considerations which are intended to allow the design to achieve higher energy efficiency. Capacity, measured in bits/s, is well known in the information theory field. In the following section a background summary on information capacity is given and the rationale for applying it to analog circuit design is explained.

### 1.3 Approach

Physically a transistor takes an input signal and through physical mechanisms of potential fields and current flow it gives rise to an output signal that is corrupted by the intrinsic noise of the transistor (figure 1.1). A passive noiseless resistor is assumed at the drain terminal. Assuming the input signal is noiseless, a MOSFET generates a field induced current between its source and drain terminals that can then be read either as a voltage (as shown at the drain terminal in the figure 1.1) or a current. The current in the channel is not a perfect replica of the input signal voltage as there will be an additional unwanted random signal due to extra charges being randomly *added* or *subtracted* to it due to the noise processes related to the operation of the device. This noise appears as fluctuations in the current through the device or fluctuation of the voltage or charge on a node. The parameters that determine

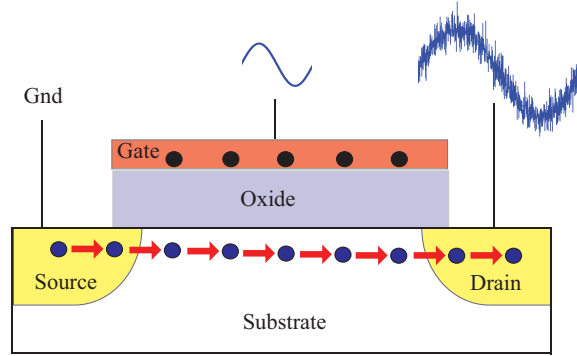


Figure 1.1: MOSFET transistor: output signal is corrupted by the physical noise sources which randomly affect the flow of charges from the source to drain terminals

the noise are derived from the physical structure. Therefore a reasonable model is that a transistor can be considered to be an information processing transformation channel in the presence of noise. [9]. This idea can be extended to circuits that are made up of multiple transistors such as amplifiers, analog to digital converters (ADC), digital to analog converters (DAC) and other practical systems. In many cases the noise sources are due to fundamental physical effects such as thermal, shot and  $1/f$  noise in continuous time channels such as an amplifier (see chapter 2), or the noise may be due to sources such as to switching and quantization effects in ADCs and DACs. Stationary noise may also be introduced because of process variations such as in an imager where fixed pattern noise exists. In this work the focus is on amplifiers used in sensor circuits which physically transform an input voltage to an amplified representation of itself. An interpretation of the maximum information rate in this context then is that it quantifies the ability of the channel to transduce the incoming input signal efficiently.

The mathematical framework to quantify information transmission in a channel has already been developed in the information theory field by Shannon [11, 12]. Entropy (similar in some ways to the entropy defined in classical thermodynamics taught in college physics and chemistry) is a measure of the average uncertainty in a random variable and is given by ([13])

$$h(X) = - \int_S f(x) \log_2 f(x) dx \quad (1.1)$$

where  $f(x)$  is a probability distribution function and  $S$  is the support set of the random variable  $X$ .  $X$  in this case represents the input signal to a sensor. Mutual information is defined as the reduction in uncertainty of one random variable due to another random variable, and is a measure of dependence between the two variables.

$$I(X; Y) = h(X) - h(X/Y) \quad (1.2)$$

A communication channel can be defined as an entity which takes an input and provides a correlated output which is probabilistically dependent on the input. The channel may be corrupted by noise, which can itself be a probabilistic process. A Gaussian channel is one which has an output that is corrupted by a noise source that is Gaussian in nature. A Gaussian channel is described by

$$Y_i = X_i + N_i \quad (1.3)$$

where  $X, Y$  and  $N$  are the input, output and noise of the channel, at time  $i$ , respectively (figure 1.2). The noise is considered to be independent of the input signal and is drawn i.i.d. (independently and identically distributed) from a Gaussian

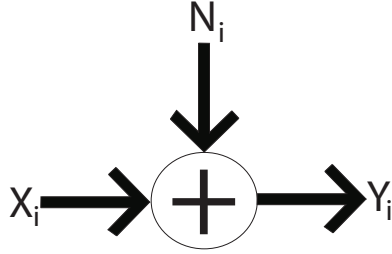


Figure 1.2: Gaussian channel: the output signal  $Y$  is composed of the original signal  $X$  as well as the noise associated with the channel.

distribution. The capacity of the channel is found by maximizing the mutual information which leads to an unlimited capacity when no constraints are specified. However under an average signal power constraint,  $P$ , the capacity of a Gaussian channel [11–13]

$$C = \frac{1}{2} \int \log_2 \left( 1 + \frac{(\nu - N(f))^+}{N(f)} \right) df \quad (1.4)$$

where

$$P = \int (\nu - N(f))^+ df \quad (1.5)$$

where  $\nu$  and  $N(f)$  are a constant and noise spectrum respectively. This solution is known as waterfilling, since the input signal power (assumed to be a Gaussian process) is allocated to spectral areas where the noise spectral density is lowest (figure 1.3).

Information theory has always been closely associated with digital circuits where bits are a natural unit of measure as there are only two states possible for any input or output signal. Within that framework the usual objective is to encode the input signal to achieve maximum information rate and to decode the signal after it has been transmitted through the channel (figure 1.4). Usual methods to

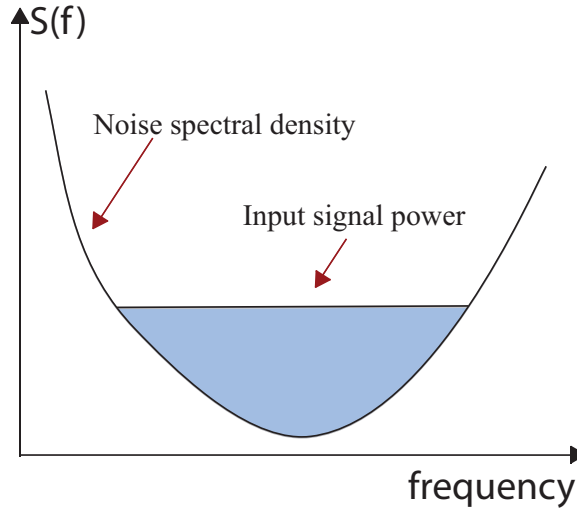


Figure 1.3: Waterfilling in the spectral domain: For maximum information rate the input signal power is placed at frequencies where the noise is lowest first before spilling over to the parts of the spectrum where the noise is higher.

incorporate this into the design of the digital communication system is to determine the best or most appropriate coding scheme to transmit a sequence of ones and zeroes over a noisy channel. In this case the noise is caused by clock jitter, thermal noise and interfering signals (crosstalk). In the analysis in this work we consider a continuous time signal where, for the purposes of the theoretical calculation, the signal is a sampled representation of itself. In this dissertation the implications of information theory and waterfilling in particular is taken as a guide to formulating a methodology for amplifier design and this work is not approached as a source coding or channel coding problem, but rather a problem of how to design a better circuit.

In this dissertation information rate is considered as an analogy of the circuit as a communication channel and information rates are determined because logically these sensory circuits essentially transmit information to the user about the input



Figure 1.4: A communications channel from the standard information theoretic point of view.

signal. In today's world of lab-on-chip applications the cost of transmitting this information is at a premium due to the weak signals and low power requirement of many sensors. In this sense the cost of using the channel is the energy to transmit the information (signal) over the channel. It is also worth noting that in the traditional sense capacity is the rate beyond which there exists some error in the received signal as it is impossible to transmit above this rate with arbitrarily small error. The actual capacity may not be achievable.

## 1.4 Research Contributions of this work

The capacity is defined as the maximum rate at which a channel can transmit information with arbitrarily small error. Information rate has been previously analyzed for silicon photoreceptors and systems with feedback [10,14]. However these results only assumed white noise processes, thermal noise for transistors or shot noise for photodiodes. In this work the implications of the maximum information rate and bit energy on analog circuits is more fully investigated by considering colored Gaussian noise sources in addition to the white noise sources. In addition, in order to better aid the mixed signal designer, the information efficiency trade-offs in analog and mixed signal circuits using the information rate and bit energy are

explored by studying different circuit topologies. We also focus on trade-offs for an example circuit in order to understand how they can affect existing design methodologies. Finally, the implications of the approach, including the suggestion for using chopper modulation to achieve information rate, are outlined.

## 1.5 Dissertation Outline

Background material on the physical sources of noise and their accompanying models for MOSFETs is outlined in chapter 2. Using simple models, a comparative analysis of the information rate and the energy required to transmit one bit of information with basic operational transconductance amplifiers was performed and experimentally verified in chapter 3. The information rate for circuits fabricated in two different technologies was also explored. Chapter 4 explores the accuracy of the models used and determines how the information rate and bit energy for amplifiers fit within an existing design methodology. As mentioned above, the natural conclusion of applying waterfilling to OTAs is chopper modulation, a technique that is explored in chapter 5. Finally, chapter 6 concludes this work with a summary of the findings and their possible impact on the world of analog design.

## Chapter 2

### Noise in CMOS Circuits

#### 2.1 Fundamental Noise Concepts

Noise is, in general, an undesirable random signal. Various sources of noise may be present in the output signals and these noise signals can severely distort the desired output signals. Before going into detail about specific noise models some fundamentals about stochastic processes are first briefly reviewed.

##### 2.1.1 Stochastic Process

As noise is usually random, it cannot be analyzed using standard signal processing techniques such as the Fourier transform and spectrograms. The analysis and theory of noise are dealt with using the concept of stochastic processes. A stochastic process is one in which a time function is assigned to every outcome in the sample space. The ensemble of all possible functions that can be realized is a stochastic process [15].

To start assume there is a stochastic process defined by  $X(t)$ . This stochastic process is considered stationary if it has time independent statistical properties and



is considered to be wide sense stationary if

$$E[X(t)] = \text{constant} \quad (2.1)$$

$$E[X(t)X(t + \tau)] = R_{XX}(\tau) \quad (2.2)$$

where  $R_{XX}$  is the autocorrelation function which is the expectation of the product of two random variables at times  $t_1 = t$  and  $t_2 = t + \tau$ . If a process is wide sense stationary and satisfies

$$A[X(t)] = E[X(t)] \quad (2.3)$$

$$A[X(t)X(t + \tau)] = R_{XX}(\tau) \quad (2.4)$$

where

$$A[X(t)] = \lim_{T \rightarrow \infty} \frac{1}{2T} \int_{-T}^T x(t) dt \quad (2.5)$$

then it is an ergodic process. If a process is ergodic, then it is possible to interpret what the parameters of the process mean in a physical sense. If a random signal can be modeled as an ergodic process, then its mean ( $E[X]$ ) is the DC component of the signal, the squared mean value is related to the DC component's power and the mean squared value is related to the signal's average power and the variance is proportional to the AC power. The variance is the difference between the squared mean and the mean squared that is  $\sigma_X^2 = E[X^2] - (E[X])^2$ .

Most noise processes are modeled as Gaussian processes. A Gaussian random variable has a probability density function given by

$$f_X(x) = \frac{1}{\sigma_X \sqrt{2\pi}} \exp \left[ -\frac{(x - \bar{X})^2}{2\sigma_X^2} \right]. \quad (2.6)$$

where  $\sigma^2$  is the variance and  $\bar{X}$  is the mean. Gaussian stochastic processes are completely described by their mean and auto-correlation function, that is no additional parameters are needed to completely specify the process.

### 2.1.2 Power Spectral Density

Noise is a random signal, therefore the Fourier transform does not exist. The power spectrum of the process is instead used to represent information about the frequency domain characteristics. The power spectrum is the Fourier transform of the autocorrelation function ( $R_{XX}$ ) which is defined as

$$R_{XX}(t, t + \tau) = E [X(t)X(t + \tau)] \quad (2.7)$$

$$S_{XX}(\omega) = \int_{-\infty}^{\infty} R_{XX}(\tau) \exp(-j\omega\tau) d\tau \quad (2.8)$$

This implies that the integral of  $S_{XX}$  over  $\omega$  is the expectation of the square of the random variable or the power of the process. It is then simple to move from the time domain to the frequency domain. If a process is modulated in the time domain this corresponds to a convolution in the frequency domain. If the process undergoes linear time invariant filtering this corresponds to multiplying the spectrum by the squared magnitude of the transfer function [15]. Use of the spectral density makes evaluation of noise in circuits using small signal analysis (for transistor circuits) possible. It allows placement of sources (either voltage or current) into the circuit to represent the noise source. The noise seen at various points in the circuit can then be evaluated using standard circuit techniques [15, 16].

### 2.1.3 System Models

Any noisy circuit may be modeled as a noise free multi-port network that is connected to independent noise sources that represent various noise sources from different components. They may also be equivalently modeled as a noise free circuit with equivalent sources at the input or the output. There are four basic transforms that may be used to manipulate each separate noise source within a circuit and turn it into the equivalent source at another node within the circuit (figure 2.1). The first way is a voltage source shift in which the noise voltage sources are moved through the circuit without changing the KVL (Kirchoff's Voltage Law) equations. The second way is a current source shift where the noise current sources are moved through the circuit without changing the KCL (Kirchoff's Current Law) equations. The third method is a Norton-Thevenin transformation where the noise current source is changed into a noise voltage source or the noise voltage source is transformed into a noise current source. The fourth method involves two-port shifts where the output noise and current sources are transformed into input current and noise sources via the equations

$$\begin{pmatrix} v_{it} \\ i_{it} \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} v_{ot} \\ i_{ot} \end{pmatrix}$$

where the noise voltages are as shown in figure 2.1. Note that the voltage and current noise sources are fully correlated [17]. It should also be noted that introducing feedback does not affect the equivalent input or output noise of the amplifier (assuming feedback elements are perfectly noiseless), thus noise generators may be moved outside of a feedback loop [18]. Noise is a fluctuation that can either be positive or

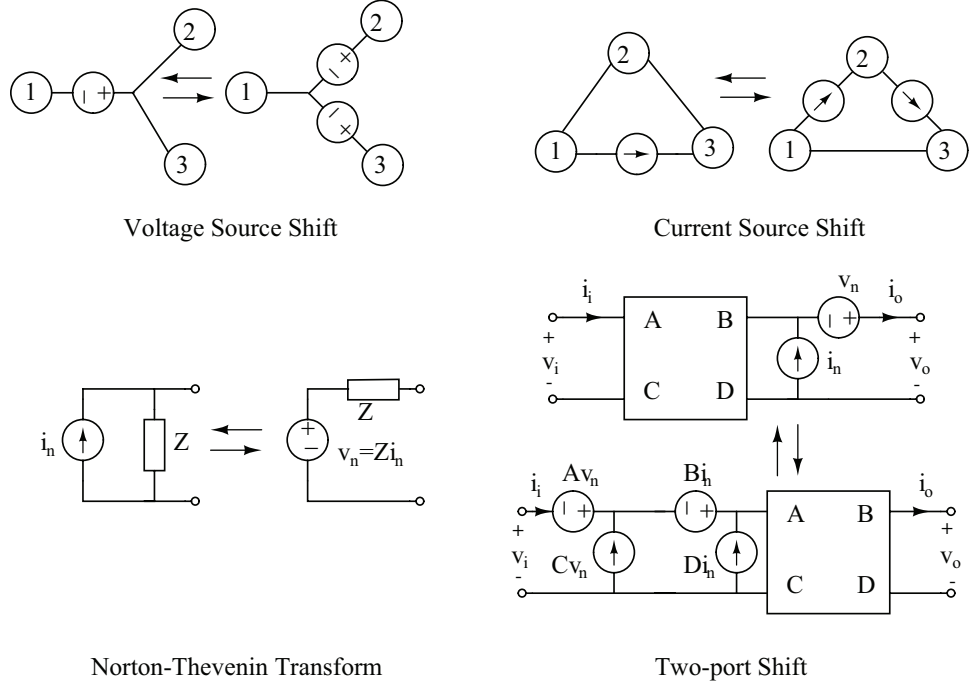
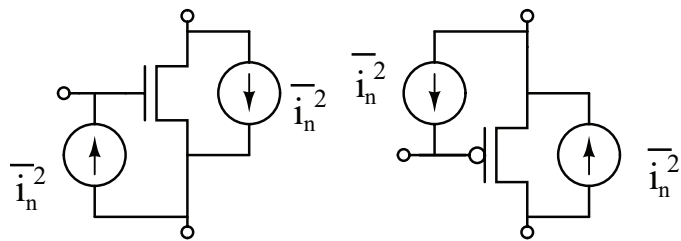


Figure 2.1: Transformations used to determine equivalent noise

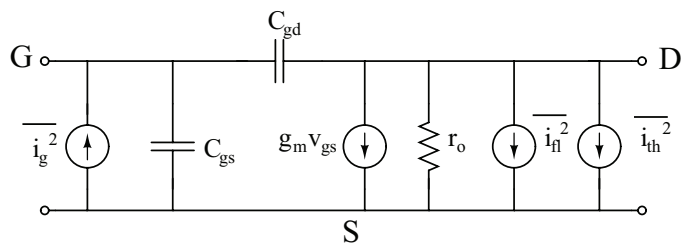
negative, therefore when drawing as a current or voltage source in a circuit diagram any direction may be chosen for the source. Typically the direction is chosen that makes any subsequent calculations or manipulations easier.

## 2.2 MOSFET Noise Models

There are four types main sources of noise in MOSFETs: flicker noise, thermal noise, gate leakage noise and shot noise. We consider each of these sources in detail in the following sections. In this work only flicker and thermal noise are considered to be dominant, and both are modeled as a noise current source across the source and drain (figure 2.2). As CMOS devices scale down we expect these noise sources to increase, thus noise considerations are critical to any design.



(a) Noise sources



(b) Small Signal Model

Figure 2.2: MOSFET Noise Sources. (a) NMOS and PMOS transistors showing noise current sources between the drain and source and into the gate (b) Flicker and thermal noise are modeled as current sources between the drain and the source. Gate current noise is modeled as a current source from the gate to the channel. Note that direction is shown on these figures to identify as the sources as current sources, the arrow may be drawn in the direction most suitable for the calculation.

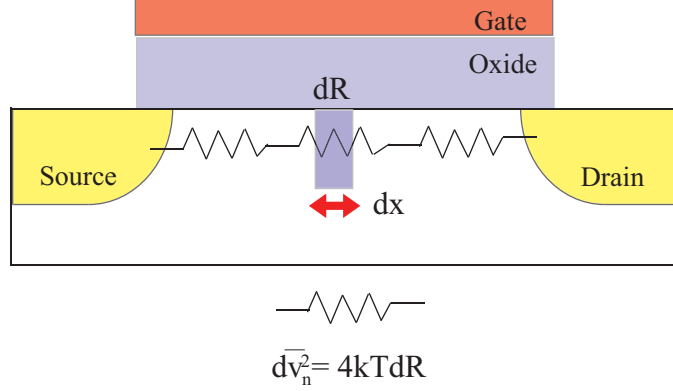


Figure 2.3: Channel is modeled as linear resistor for thermal noise calculations.

### 2.2.1 Thermal Noise

Thermal noise is present in a multitude of devices and is due to random thermal motion of electrons in the channel as depicted in figure 2.3. It is unaffected by direct current, as thermal electron velocities are much larger than drift current velocities.

A thermal noise model along with experimental results for conductors was first developed in papers by Nyquist and Johnson in 1928 [19, 20]. This model has since been applied to MOSFETs by assuming a linear channel resistance (figure 2.3) given by the transconductance,  $g_m$ . Van der Ziel derives the thermal noise for FETs as [21]

$$S_{I_D}(0) = \gamma 4kT g_{d0} \tag{2.9}$$

where  $\gamma$  is related to the drain and gate voltage, and thus the mode of operation of the device.  $\gamma$  has a value of  $2/3$  in the saturation region, and  $g_{d0}$  is the ratio of the conductance per unit length at the source (at zero drain bias) and the length of the device. For a MOSFET in above threshold saturation  $g_{d0} = g_m$  and the thermal

noise is more commonly written as:

$$S_{I_D}(0) = \gamma 4kT g_m \quad (2.10)$$

where

$$g_m = \frac{\mu W C_{ox}}{L} (V_{gs} - V_{th}). \quad (2.11)$$

Equation (2.10) is the noise at zero frequency, but is expected to be accurate up to relatively high frequencies. In weak inversion the value of  $\gamma$  is usually assumed to be 1/2. Van der Ziel's derivation for thermal noise at weak inversion arrives, after some manipulations, at the following expression

$$S_{I_d}(f) = 2qI_{sat}(1 + \exp(-\beta V_d)) \quad (2.12)$$

which is the accepted form of a shot noise model for  $I_{sat}$ . Sarpeshkar also makes the apparent connection between shot and thermal noise in subthreshold operation, however there is no doubt that the noise process is thermal in nature [22]. It was shown by Coram and Wyatt that the extended Nyquist-Johnson model is only thermodynamically valid for operating regions where the resistor is linear [23]. The form of the thermal noise as shot noise developed for subthreshold operation is thermodynamically valid and may thus be acceptable for use. In saturation clearly  $g_m$  is nonlinear and depends on the gate voltage, however for small ranges of the gate voltage it can be assumed that the transconductance does not change much. Thus equation (2.10) is widely used in practice for transistors operating in the saturation region despite the fact that it is inconsistent with thermodynamic principles. At best (2.10) is a bound on the thermal noise of the transistor.

In recent years thermal noise models have been improved, mainly for RF design where thermal noise is the most important noise source. Experiments have shown that the noise given by equation (2.10) is smaller than that experimentally measured in submicron devices [24]. It has been shown that previous models use a carrier temperature model that is inconsistent with the mobility model, leading to a wrong value for  $\gamma$  (hot electron effects) [24].

It has been assumed in most works that only the term  $\gamma$  changes in subthreshold operation, where it is assumed to be 1/2. However a more accurate thermal noise model for subthreshold is

$$S_{I_d}(f) = \frac{kT}{2\kappa} \quad (2.13)$$

where  $\kappa$  is the subthreshold slope [25]. Note that all these thermal noise equations are actually derived under equilibrium conditions.

## 2.2.2 Shot Noise

Shot noise arises each time current flows across a potential barrier, therefore there are a few possible sources for shot noise in a MOSFET, the source to drain current across the p-n junction in subthreshold, the current across the p-n junction to the substrate and the gate current in all regions of operation (figure 2.4). There is no shot noise for the source to drain current under strong inversion as the potential barrier which the current flows across is decreased. All shot noise is related to the direct current flow across the barrier and at any time instant the current can be thought of as comprising a number of random independent pulses. A current pulse



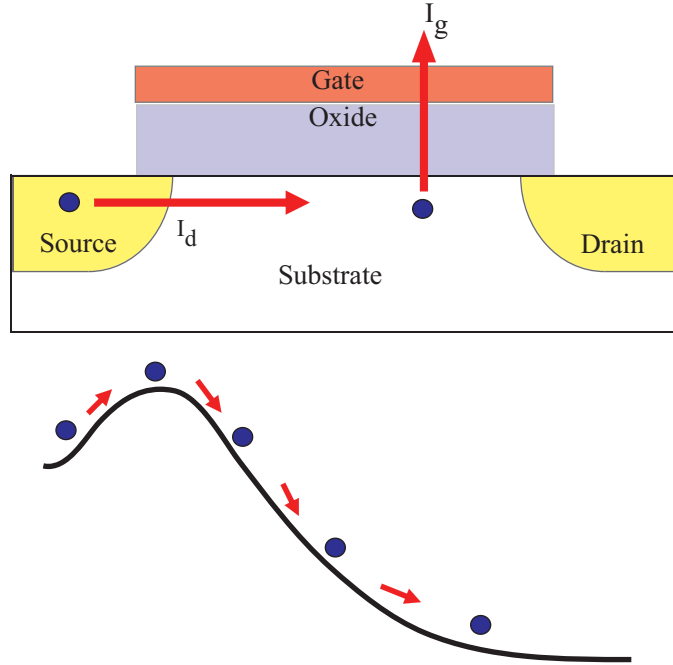


Figure 2.4: Sources of shot noise.

at any time  $\tau_k$  can be written as

$$X(t) = \sum_{k=-\infty}^{\infty} h(t + \tau_k). \quad (2.14)$$

For the drain current this leads to a noise spectral density of

$$S_{I_d} = 2qI_d \quad (2.15)$$

where the amplitude of this noise current has a Gaussian distribution.

The substrate current is typically assumed to be negligible and therefore this source of shot noise is ignored.

### 2.2.2.1 Shot Noise = Thermal Noise?

It has been proposed that in the subthreshold region that shot and thermal noise, traditionally thought to be separate processes, are actually the same process [22]. This was primarily achieved through a mathematical manipulation that assumes linearity of the conductance and that Einstein's relationship holds. This is not necessarily true and there is some debate about the validity of this approach. One method to prove or disprove this result would be to perform noise measurements at low temperatures in an attempt to separate the contributions due to thermal and shot noise. However the actual case may be that what we call shot noise and thermal noise are actually limiting cases for a more general noise mechanism with high temperature causing the thermal contribution to dominate and low temperature causing the shot noise to dominate. If the transmission of carriers is treated as a quantum mechanical phenomenon, it can be shown that both noise terms are limiting cases of the same physical model [21, 22, 26–28]. Therefore in this work shot noise is ignored as a source of significant MOSFET drain current noise.

### 2.2.2.2 Gate Leakage Noise due to Shot Noise

The shot noise due to gate leakage current can be written as

$$S_{I_g} = 2qI_g \tag{2.16}$$

Since  $I_g$  is typically very small, this term is usually insignificant, and is not considered in most calculations. The noise source is represented in the model as a noise current source at the gate of the transistor.

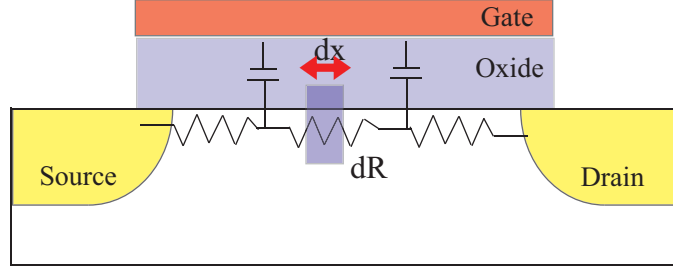


Figure 2.5: Induced Gate Current Noise.

### 2.2.3 Induced Gate Current Noise

The thermal noise in the channel induces fluctuations in the gate-channel voltage at arbitrary points along the channel. There exists a distributed RC network along the channel where the distributed resistance is the channel itself and there is a capacitance between the gate and the channel ( $C_{gs}$ ) (figure 2.5) [18, 21]. This gives rise to a corresponding gate current noise that is correlated with the channel thermal noise and is given by (for long channel transistors)

$$S_{I_g} = \frac{16}{15}kT\omega^2C_{gs}^2 \quad (2.17)$$

where  $C_{gs} = 2/3C_{ox}WL$ . The correlation factor between the induced gate noise and the thermal noise is 0.395 [18, 21]. For short channel transistors the noise is increased due to hot electrons (this is true for thermal noise as well). This noise source is more important at higher frequencies and for the purposes of this work it is ignored.

### 2.2.3.1 A Short Discussion of Shot Noise and Thermal Noise Physics

Shot noise and thermal noise in conductors were first referenced in papers by Johnson, Nyquist and Schottky [19, 20, 29]. Callegaro derives expressions for both thermal and shot noise [27]. Fundamentally thermal noise is typically understood to be fluctuations in the position of the charged carriers. This uncertainty in position gives rise to fluctuations around the mean of the current (voltage) measured. Shot noise on the other hand is related to the quantization of the carriers and thus the uncertainty is related to the exact energy of the carriers. This is therefore related to the number of carriers which contribute the direct current. As such both thermal and shot noise are classically thought to arise from two different physical processes and are usually considered to be independent. Based on the models for the two noise sources at absolute zero (or as close as one can get to it) there should be almost zero thermal noise, but the noise due to shot noise should still exist as long as there is a current flow. In addition as the temperature decreases the shot noise should remain the same. Note however that this explanation assumes that the device current is completely independent of temperature. It is also clear that the temperature will have some effect on the amount of uncertainty in the energy states. It is nevertheless widely accepted that one should not count both shot and thermal noise at the same time for MOSFETs. In addition in some quantum mechanical treatments both noise sources (thermal and shot) are attributed to the same physical mechanism [26, 30, 31].

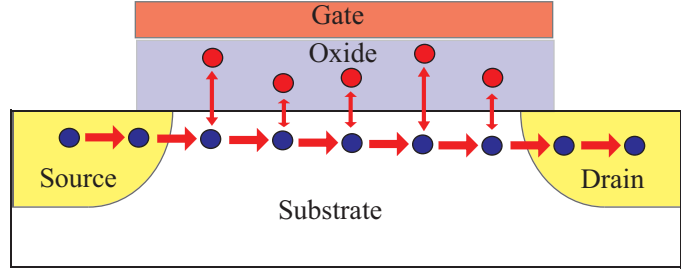


Figure 2.6: Flicker noise caused by traps at the Si-Oxide interface.

## 2.2.4 Flicker Noise

Flicker noise can be observed in many systems. This includes but is not limited to transistors, traffic flow rate, nerve membrane voltages and loudness and pitch of music. It is thus considered by some researchers to be ubiquitous [32]. It is the dominant noise source in transistors up to relatively high frequencies (process dependent). The most predominant theory on flicker noise holds that it is a superposition of several random telegraph signals (discrete modulation of the source to drain channel conductance, RTS) which are caused by single inversion carriers at the silicon - oxide interface being trapped and emitted from the interface traps (figure 2.6). This trapping-detrapping process results in fluctuations in the number of mobile carriers. Along with the carrier number fluctuation there is an associated channel mobility fluctuation due to the traps themselves being Coulombic scattering sites. Thus there is an associated fluctuation in the channel mobility. A single RTS is shown in figure 2.7; the times between the high and low current states are exponentially distributed, that is the switching is a Poisson process. By evaluating the autocorrelation function it is found that each RTS fluctuation has a Lorentzian

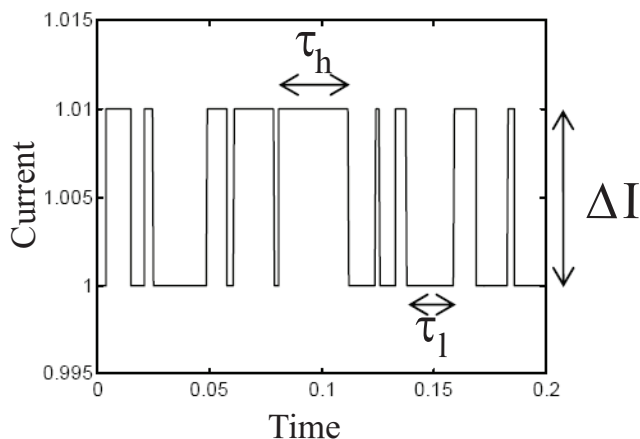


Figure 2.7: Random telegraph signal: change in current over time.

power spectral density. Superimposing a number of these RTS's gives rise to a  $1/f$  spectrum (figure 2.8). The trapping-detrapping process depends on the operating region of the transistor and can occur by thermally activated processes and tunneling. If an exponential relationship between the capture and release rates and the depth of the trap in the oxide is assumed and the traps are assumed to be uniformly distributed (spatially and energy wise), then the spectral density of the oxide traps is [33, 34]

$$S_{N'_{ot}} = \frac{N_{ot}}{WL} \frac{1}{f} \quad (2.18)$$

where  $N'_{ot}$  is the number of occupied traps,  $L$  and  $W$  are the length and width of the gate respectively and  $N_{ot}$  is the density of oxide traps per unit area. Under the assumption that the inversion charge and the gate voltage are linearly related for all operating regions, a physical model for flicker noise can be obtained and is given

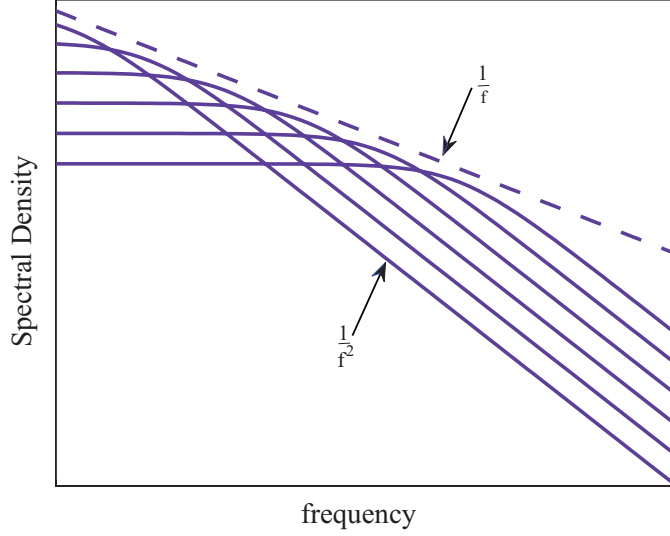


Figure 2.8: Superposition of all RTS gives rise to 1/f spectrum.

by [35,36]

$$S_{I_d} = \begin{cases} \frac{q^2}{C_{ox}^2} \left( \frac{I_d}{V_g - V_t} \right)^2 \frac{N_{ot}}{WL} \frac{1}{f}, & \text{strong inversion, linear} \\ \frac{q^2}{C_{ox}} \frac{N_{ot}}{L^2} \frac{I_d}{f}, & \text{strong inversion, saturation} \\ \frac{C_{inv}^2}{(C_{ox} + C_d)^4} \frac{q^4}{(kT)^2} I_d^2 \frac{N_{ot}}{WLf}, & \text{weak inversion, below threshold} \end{cases} \quad (2.19)$$

The above equations can be fitted to a generic semi-empirical form given by

$$S_{I_d} = \frac{K_f I_d^{A_f}}{C_{ox}^2 WL f^{E_f}} \quad (2.20)$$

where  $K_f$  is a constant that varies depending on the region of operation. However, for each operating region of the transistor, simple spice models can be derived,

$$S_{v_g} = \begin{cases} \frac{K_f I_d}{C_{ox}^2 L_{eff}^2 f}, & \text{strong inversion, saturation} \\ \frac{K_f I_d}{C_{ox}^2 WL f}, & \text{strong inversion, triode} \\ \frac{K_f I_d^2}{C_{ox}^2 WL f^{E_f}}, & \text{subthreshold} \end{cases} \quad (2.21)$$

where  $K_f$  is a process dependent parameter that is voltage dependent since it reflects the density of oxide traps.  $A_f$  and  $E_f$  are experimentally determined process

parameters which usually have a value of approximately 1. These are the simplest models that an analog designer can use and are generally considered to be extremely oversimplified; however they provide a bound on the expected noise of any circuit. Another simple model commonly used in practice, assumes the voltage noise source is independent of the bias current [18]

$$S_v = \frac{K}{WLC_{ox}f} \quad (2.22)$$

where  $K$  is a process dependent parameter.

More complex models are available (specifically the BSIM 3.3 or 4.0 model) which contains 4 different parameters which must be fitted experimentally. The equations given above are usually used for hand calculations and in most SPICE programs (HSPICE, PSPICE, TSPICE), although most implementations require the user to manually change the noise model as appropriate to the region of operation.

#### 2.2.4.1 Issues with Flicker Noise in the Literature

While the description described in the previous section is adequate for most designers, one should also be aware of the some of the controversy and misconceptions that surround flicker noise. One of the first questions asked is: “what is the flicker noise at zero frequency?” or “what is it’s cutoff frequency?” since the integral of  $1/f$  from zero to some frequency results in an infinite power. However this is easily resolved by considering that zero frequency means infinite time and hence infinite power, and that zero frequency does not really exist mathematically. Also



the autocorrelation function of flicker noise is constant, which implies that flicker noise arises from a process with time independent memory which is associated with the long occupation time constants of the interface traps [32, 37, 38].

The physical cause of flicker noise was also a subject for much controversy in the past, as it was thought that it could be caused by mobility fluctuations or carrier number fluctuations. It is now generally accepted that it is a fluctuation in the number of carriers, with each fluctuation having a Lorentzian spectra, which then gives rise to a mobility fluctuation. As already stated, the models given in the previous section are simplified models useful for hand calculations. The BSIM4 models do a slightly more accurate modeling of the noise parameters across different regions of operations but are still relatively inaccurate when compared to experimental data. This is because they do not take into account the bias history of the device which can affect the present noise data [33, 36, 39–43].

Another important question, particularly for this work given the approach outlined in Chapter 1, is whether flicker noise is Gaussian and also if it is stationary. Surprisingly, these are not always addressed in discussions about flicker noise. A survey of the literature shows that there are conflicting views. Some experimental results have shown that the amplitude distribution of flicker noise is Gaussian, however there are some view that oppose this. Brophy found that the process was stationary [44], while Brophy and Greenstein found it to be nonstationary [45]. Stoisiek and Wolf found that the statistical properties of flicker noise were consistent with the assumption of stationarity [46]. If the spectrum for  $1/f$  noise (band

pass filtered) is [47]

$$S_X = \begin{cases} \frac{C}{2\pi\omega} & \omega_1 < \omega < \omega_2 \\ 0 & \textit{otherwise} \end{cases}$$

then the autocorrelation function is

$$R_X = \frac{C}{2\pi} (C_i(\omega_2\tau) - C_i(\omega_1\tau)) \quad (2.23)$$

$$C_i(Z) = \int_{-\infty}^Z \frac{\cos y}{y} dy \quad (2.24)$$

This leads to

$$R_X(\tau \rightarrow 0) = \frac{C}{2\pi} \ln \frac{f_2}{f_1} \quad (2.25)$$

This is independent of the time and is thus stationary. However, as mentioned previously, there is some question as to whether this low frequency actually exists. Flicker noise has been measured down to  $10^{-6.3}\text{s}$  ([37]) and the spectrum keeps increasing. If this lower cutoff does not exist then the process is not stationary. Since this cutoff cannot be experimentally measured (such measurements would take an infinitely long time) [37], it may or may not exist. Therefore flicker noise may or may not be stationary. It is therefore assumed for this work that flicker noise is both stationary and Gaussian in nature.

### 2.3 Noise Parameter Extraction Methodology

The process dependent parameters for flicker noise ( $K_f, A_f, E_f$ ) were experimentally measured and extracted for a commercial  $0.5\mu\text{m}$  3-metal, 2-poly process. Figure 2.9 shows the experimental setup [48,49]. Measurements were performed in a Faraday cage to suppress environmental noise. The gate was biased using a battery

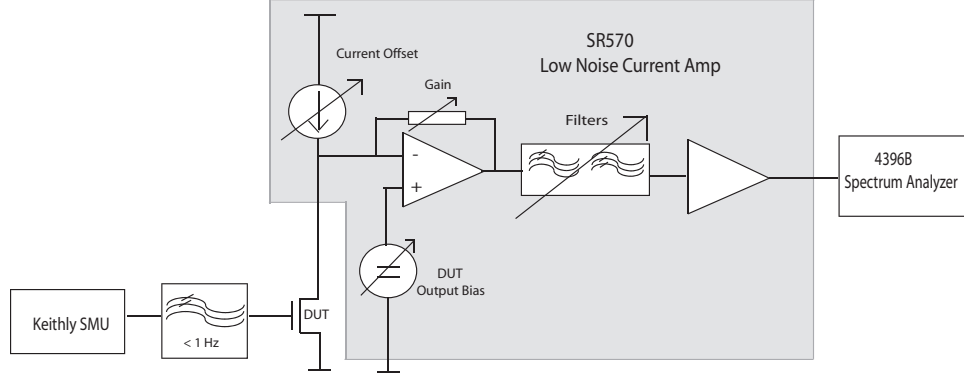


Figure 2.9: Noise parameter extraction setup.

and voltage regulator to provide a constant noiseless bias gate voltage. The SR570 is a low noise current preamplifier that can provide a bias current to the transistor, it also has the advantage of being battery powered. Keithley 236 source measure units were used to experimentally extract  $g_m$  and other parameters at varying bias currents. The output of the current preamp was connected to the input of the spectrum analyzer. Since the SR570 is a programmable transresistance amplifier, it allows the measurement of the noise voltage which can be easily converted back to the current noise. By using a log-log plot the parameter  $K_f$  can be extracted. Alternatively the noise voltage at the drain can be measured using a resistor to set the transistor drain current. In this configuration the noise of the resistor (assumed to be only thermal noise) needs to be taken into account.

For amplifier measurements, the output noise voltage is measured directly (through a low noise buffer). The output noise voltage is related to the output noise current by

$$S_{V_{out}} = Z_{out}^2 S_{I_{out}} \quad (2.26)$$

where  $Z_{out}$  is the output impedance of the amplifier together with its load, and may not be purely resistive.

### 2.3.1 Extracted Noise Parameters

Figure 2.10 shows the measured experimental noise for a 6/2 NMOS transistor in a standard 0.5  $\mu\text{m}$  process. Figure 2.11 shows the measured experimental noise at different bias currents (for above threshold saturation operation) for a 25/5 transistor in the same process. Here the aspect ratio is given in terms of lambda based designs where  $\lambda = 0.35\mu\text{m}$ . Using this noise spectrum measurement the noise parameter  $K_f$  is  $\approx 10^{-26}$ . The parameters  $A_f$  and  $E_f$  are extracted to be 1. It should be noted that although this is measured data, the actual  $K_f$  can vary from wafer to wafer and can also vary depending on which part of the wafer the chips have originated. This means that even though the parameters have been experimentally extracted they will not necessarily always match the experimental measurements for subsequent circuit designs, however they should be adequate to determine the noise before tape-out and are still useful as a design check.

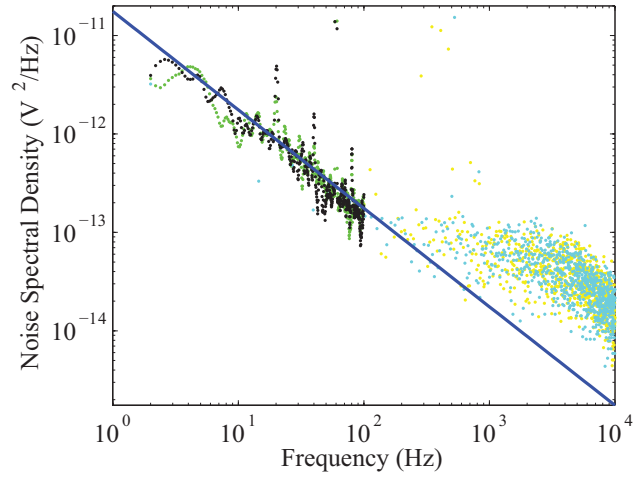


Figure 2.10: Experimental noise of 6/2 NMOS transistor: solid line is calculated noise with  $K_f = 10^{-26}$ . (Multiple lines reflect different measurement ranges during the same experiment).

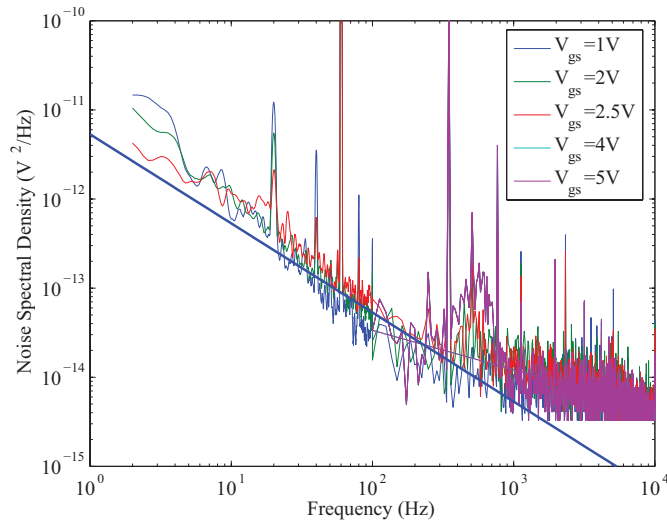


Figure 2.11: Experimental noise of 25/5 NMOS transistor: solid line is calculated noise with  $K_f = 10^{-26}$ . (The large peaks reflect 60Hz noise and its harmonics).

## Chapter 3

### Comparative Analysis of Amplifier Topologies

OTAs and single transistor amplifiers are ubiquitous components in analog and mixed signal design, we therefore choose to begin exploring the idea of information rates for circuits by focusing on how to determine the information rate for an amplifier and the implied characteristics of a particular design. Amplifiers are generally used to boost the absolute value of a signal. They are therefore used to amplify weak signals, in filter designs, in comparator designs, as buffers and are found in some form in almost any design which contains significant analog processing. In accordance with the theory outlined in the first chapter, each amplifier can be treated as a channel which transduces a weak signal into an amplified version of itself which can then be stored or further processed by other circuitry. To this end one of the first questions in investigating this approach is to ask the following: what does the information rate say about choosing a configuration for a particular task?

#### 3.1 Amplifier Configurations

For this study, we limit the choices to the basic configurations upon which more complicated designs are based. The configurations studied are: the single transistor amplifiers: common source, common gate and common drain, all with active loads. In addition the self biased transconductor, as well as a variety of OTA's are also

studied. The OTA's studied were the simple OTA, wide range OTA, wide swing OTA and folded cascode OTA (figure 3.1). Understanding the efficiency of these configurations will allow a designer to select the option most suited to the desired application.

These amplifiers reflect differences or improvements in gain, output resistance, common mode range, common mode rejection ratio and power supply rejection ratio. For a given fixed aspect ratio ( $W/L$ ), the folded cascode has the highest gain, while the source follower has the lowest (gain  $\approx 1$ ). The common gate is better suited to a current buffering application. Differential amplifiers are better suited to applications in which the environmental noise is expected to be high. There is an increase in gain from the simple to the wide range to the wide swing to the folded cascode. And of course the wide swing has the best common mode range of all the OTA's, while the folded cascode has the best power supply rejection ratio. The OTAs all have better power supply rejection and common mode rejection than the single transistor amplifiers. A fully differential amplifier (such as that to be seen in Chapter 5) would have improved noise immunity over the single ended versions, however we restrict this portion of the study to only single ended amplifiers.

The important properties of these amplifiers, specifically the low frequency gain, location of the dominant pole and power consumption, are summarized in Table 3.1. To apply the waterfilling approach, the noise spectrum of the channel is required and we start by determining the input referred noise of the amplifier. To begin a simplified noise model for the amplifier is assumed.

The noise for each transistor in an amplifier may be modeled according to

simple flicker noise and thermal models introduced in the Chapter 2. The output current noise spectral density for each transistor is given by

$$S_{I_d} = \gamma 4KTg_m + \frac{K_f I_d^{A_f}}{f^{E_f} C_{ox} L_{eff}^2} \quad (3.1)$$

where  $K_f \approx 10^{-26}$  (for NMOS),  $A_f \approx 1$  and  $E_f \approx 1$  are process dependent constants and  $\gamma$  depends on the region of operation ( $2/3$  for above threshold and  $1/2$  for subthreshold operation). The noise of the PMOS is an order of magnitude lower than the NMOS. The input referred noise of each amplifier is determined by first finding the output voltage noise, which can be related to the current noise (at low frequencies) as

$$S_{out_v} = S_{I_d} Z_{out}^2 \quad (3.2)$$

The input referred voltage noise is then the ratio of the output voltage noise and the differential gain of the amplifier. As stated in Chapter 2 while this is just one method to determine the input referred noise, and all valid methods should lead to the same answer. The noise of the current mirrors which provide the bias current are neglected in a simple model since ideally it adds into both sides of the differential amplifier equally and should not affect the output noise voltage. The noise of the current mirrors is considered in the single amp stages.

For more accurate noise modeling the full small signal model should be considered to properly take into account the frequency effects. The output voltage noise of each transistor is considered, and then the amplification of each noise source from its position in the circuit to the output is considered. The input referred noise is the sum of all these noise sources divided by the gain of the amplifier. This more



Table 3.1: Summary of Amplifier Configurations

Configuration	Low Frequency Gain	1/Dominant Pole	Power Dissipation
Common Source	$-g_{m1}(r_{o1}  r_{o2})$	$(r_{o1}  r_{o2})(C_{gd2}+C_L)$	$I_{bias}(V_{dd}+V_{ss})$
Common Drain	$\frac{r_{o1}  r_{o2}}{r_{o1}  r_{o2}+\frac{1}{g_{m1}}}$	$1/(1/(r_{o1}  r_{o2})+g_{m1})(C_{gs1}+C_{gd2}+C_L)$	$I_{bias}(V_{dd}+V_{ss})$
Common Gate	$r_{o1}  r_{o2}\left(\frac{1}{r_{o1}}+g_{m1}\right)$	$(r_{o1}  r_{o2})(C_{gd2}+C_{gd1}+C_L)$	$I_{bias}(V_{dd}+V_{ss})$
Self Biased Transconductor	$-(g_{m1}+g_{m2})(r_{o1}  r_{o2})$	$(r_{o1}  r_{o2})(C_{gd1}+C_{gd2}+C_L)$	$I_{bias}(V_{dd}+V_{ss})$
Simple OTA	$g_{m1}(r_{o2}  r_{o4})$	$(r_{o2}  r_{o4})(C_L+C_{gd2}+C_{gd4})$	$I_{bias}(V_{dd}+V_{ss})$
Wide Range	$g_{m1}[(R_{ocasn}  R_{ocasp})]$	$(R_{ocasn}  R_{ocasp})(C_L+C_{gd8cas}+C_{gd5cas})$	$2I_{bias}(V_{dd}+V_{ss})$
Wide Swing	$(g_{m1a}+g_{m1b})(r_{o6}  r_{o10})$	$(r_{o6}  r_{o10})(C_L+C_{gd6}+C_{gd10})$	$5I_{bias}(V_{dd}+V_{ss})$
Folded Cascode	$g_{m1}[(R_{ocasn}  R_{ocasp})]$	$(R_{ocasn}  R_{ocasp})(C_L+C_{gd6}+C_{gd10})$	$3I_{bias}(V_{dd}+V_{ss})$
Fully Differential Folded Cascode	$g_{m1}[(R_{ocasn}  R_{ocasp})]$	$(R_{ocasn}  R_{ocasp})(C_L+C_{gd6}+C_{gd10})$	$(5I_{bias})(V_{dd}+V_{ss})$

$$(R_{ocasn} = r_{o10}(1 + g_{m10}r_{o12}) \text{ and } R_{ocasp} = r_{o8}(1 + g_{m8}r_{o6}))$$

complicated model and whether it is necessary is discussed in more detail in Chapter 4.

Using the simple model and Table 3.1 we can look at trends for different topologies and determine bounds on the noise spectrum, information rate and bit energy.

## 3.2 Information Power Tradeoffs for Basic Topologies

In this section we theoretically and experimentally explore the trade-offs for basic amplifier topologies.

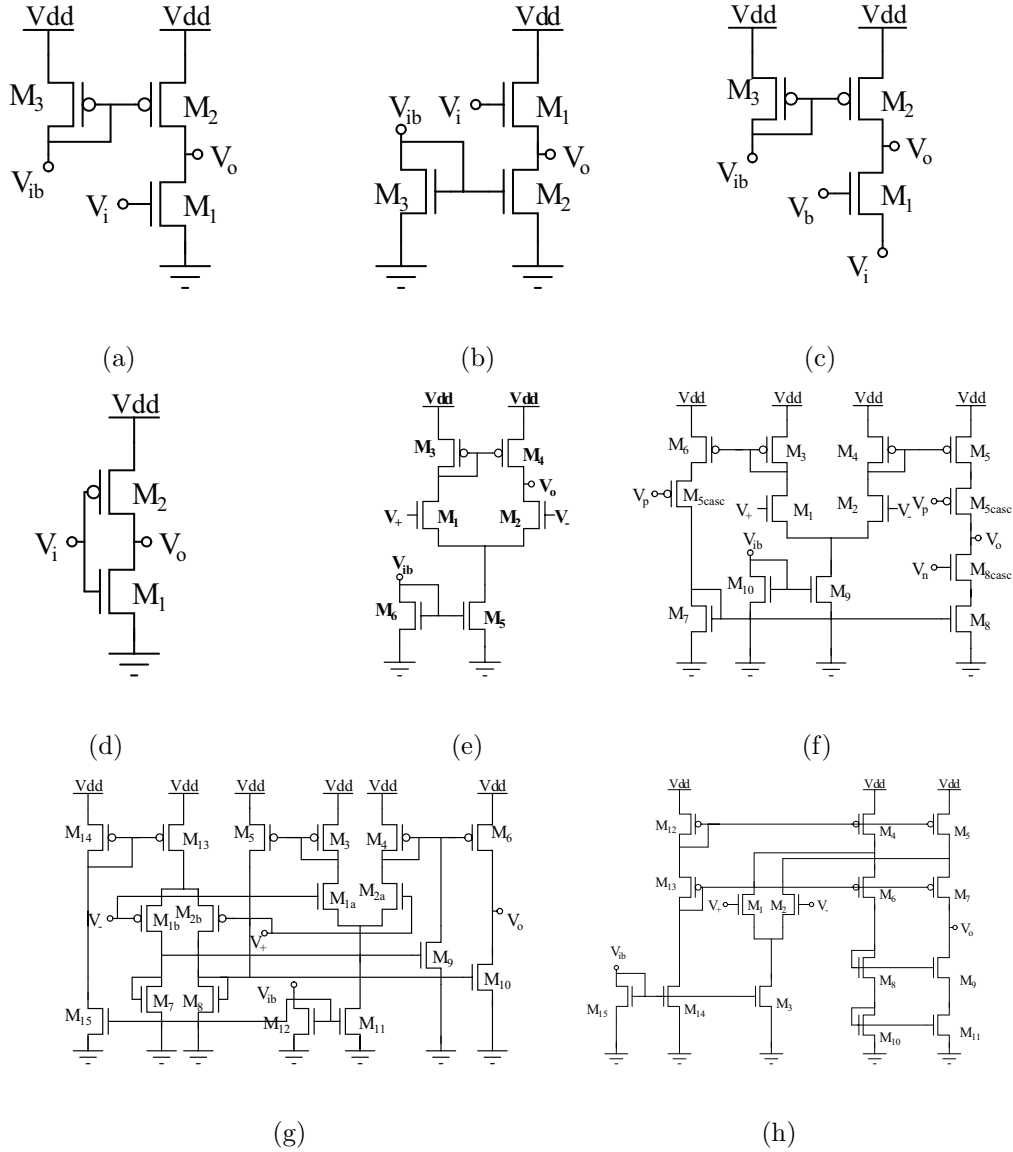


Figure 3.1: Amplifier configurations: (a) common source, (b) common drain, (c) common gate, (d) self biased transconductor, (e) simple OTA, (f) wide range OTA, (g) wide swing OTA and (h) folded cascode OTA.

### 3.2.1 Information Rate Using a First Order Model

The beginning of any design typically starts with “back of hand” calculations to get an idea of the basic performance before fine tuning with more complicated calculations and simulations. To this end we can consider the noise of only the input differential pairs for simplicity. This is motivated by the fact that most of the input referred noise in a multistage system originates from the first stage as well as the fact that we experimentally observe the output noise to have a form that goes as  $1/f^n$  plus some constant which is then shaped by the transfer function.

For a generic first order low pass amplifier with output noise given by equation (3.1), the input referred noise can be written in the form

$$S_{n_{in}} = \frac{S_0}{A_0^2} \left( 1 + \frac{f_k}{f} \right) \left( 1 + \left( \frac{f}{f_c} \right)^2 \right) \quad (3.3)$$

where  $f_k$  represents the corner frequency of the flicker and thermal noise components,  $S_0$  is the thermal noise level,  $A_0$  is the low frequency gain and  $f_c$  is the amplifier cut-off frequency or 3dB frequency. This formulation is a simplified case which reflects only the effect of the dominant pole of the amplifier and is assumed to be an input voltage noise. All parameters reflect physical characteristics of the transistors including noise parameters ( $K_f, A_f, E_f$ ), transconductance ( $g_m$ ) and aspect ratio (W/L) of the input differential pair, and output resistance ( $r_o$ ) as well as bias current ( $I_d$ ) flowing through the transistors. Depending on the amplifier topology, the output resistance may or may not be a property of the input transistors (that is, a single transistor is both the input and the output). These parameters are also the same design parameters used in standard amplifier design. We therefore model

our amplifiers using equation (3.3) as a first check at understanding how different design parameters may affect the information rates and available power resources for different topologies.

In line with our algorithm from information theory, the noise spectrum is further assumed to be colored Gaussian noise. This allows the amplifier to be modeled as a Gaussian channel where the input signal is corrupted by colored Gaussian noise. We restate the classical Shannon capacity of a Gaussian channel with colored noise as [10, 13]

$$C = \int_{f_1}^{f_2} \log_2 \left( \frac{\nu}{S_{n_{in}}(f)} \right) df \quad (3.4)$$

where  $\nu$  is the total spectral density of *signal + noise* over the signal bandwidth,  $\Delta f = f_2 - f_1$ , and is a constant. The signal power (assuming a cupshaped noise spectrum) is given by

$$\begin{aligned} P &= \int_{f_1}^{f_2} (\nu - S_{n_{in}}(f)) df \\ \nu &= S_{n_{in}}(f_1) = S_{n_{in}}(f_2) \end{aligned} \quad (3.5)$$

Combining the simple noise models and equation (3.4) an analytical expression for the information rate can be determined. Substituting equation (3.3) into equation

(3.4):

$$\begin{aligned}
I &= \int_{f_1}^{f_2} \log_2 \frac{\nu}{\frac{S_o}{A_o^2} \left(1 + \frac{f_k}{f}\right) \left(1 + \frac{f^2}{f_c^2}\right)} df \\
&= \int_{f_1}^{f_2} \log_2 \frac{\nu A_o^2}{S_o} - \log_2 \left(1 + \frac{f_k}{f}\right) - \log_2 \left(1 + \frac{f^2}{f_c^2}\right) df \\
&= \frac{1}{\ln 2} \int_{f_1}^{f_2} \ln \frac{\nu A_o^2}{S_o} - \ln \left(1 + \frac{f_k}{f}\right) - \ln \left(1 + \frac{f^2}{f_c^2}\right) df \\
&= I_1 + I_2 + I_3
\end{aligned}$$

with

$$I_1 = f \ln \frac{\nu A_o^2}{S_o}$$

and

$$\begin{aligned}
I_2 = \int \ln \left(1 + \frac{f_k}{f}\right) df &= \int \ln \frac{f + f_k}{f} df \\
&= \int [\ln(f + f_k) - \ln f] df \\
&= (f + f_k) \ln(f + f_k) - (f + f_k) - (f \ln f - f)
\end{aligned}$$

and

$$\begin{aligned}
I_3 = \int \ln \left(1 + \frac{f^2}{f_c^2}\right) df &= f \ln \left(1 + \frac{f^2}{f_c^2}\right) - 2 \int \frac{f^2/f_c^2}{1 + f^2/f_c^2} df \\
&= f \ln \left(1 + \frac{f^2}{f_c^2}\right) - 2 \int 1 - \frac{1}{1 + f/f_c} df \\
&= f \ln \left(1 + \frac{f^2}{f_c^2}\right) - 2 \left[ f - f_c \tan^{-1} \frac{f}{f_c} \right] \\
&= f \ln \left(1 + \frac{f^2}{f_c^2}\right) - 2f + 2f_c \tan^{-1} \frac{f}{f_c}
\end{aligned}$$

giving the information rate as

$$\begin{aligned}
I &= \frac{1}{\ln 2} \left[ f \ln \frac{\nu A_o^2}{S_o} \right. \\
&\quad - ((f + f_k) \ln(f + f_k) - (f + f_k) - (f \ln f - f)) \\
&\quad \left. - \left( f \ln \left( 1 + \frac{f^2}{f_c^2} \right) - 2f + 2f_c \tan^{-1} \frac{f}{f_c} \right) \right] \Big|_{f_1}^{f_2} \\
&= \frac{1}{\ln 2} \left[ 2f + f \ln \frac{\nu}{\frac{S_o}{A_o^2} \left( 1 + \frac{f_k}{f} \right) \left( 1 + \frac{f^2}{f_c^2} \right)} + f_k (1 - \ln(f + f_k)) - 2f_c \tan^{-1} \frac{f}{f_c} \right] \Big|_{f_1}^{f_2}
\end{aligned}$$

Using equation (3.5) we can write (in terms of the bandwidth  $\Delta f = f_2 - f_1$ )

$$I = \frac{1}{\ln 2} \left[ 2(f_2 - f_1) + f_k \ln \frac{f_1 + f_k}{f_2 + f_k} - 2f_c \left( \tan^{-1} \frac{f_2}{f_c} - \tan^{-1} \frac{f_1}{f_c} \right) \right] \quad (3.6)$$

If we instead consider the input signal to be filtered by an ideal low pass filter such that the 3dB frequency of the filter is the same as the 3dB frequency of the amplifier we can write the information rate of the amplifier as:

$$\begin{aligned}
\nu &= S_{n_{in}}(f_1) \text{ and } f_2 = f_c = f_{3dB} \\
I &= \frac{1}{\ln 2} \left[ 2(f_c - f_1) + f_c \ln \frac{\left( 1 + \frac{f_k}{f_1} \right) \left( 1 + \frac{f_1^2}{f_c^2} \right)}{\left( 1 + \frac{f_k}{f_c} \right) \left( 1 + \frac{f_c^2}{f_c^2} \right)} + f_k \ln \frac{f_1 + f_k}{f_c + f_k} \right. \\
&\quad \left. - 2f_c \left( \tan^{-1} \frac{f_c}{f_c} - \tan^{-1} \frac{f_1}{f_c} \right) \right] \\
I &= \frac{1}{\ln 2} \left[ 2(f_c - f_1) + f_c \ln \frac{\left( 1 + \frac{f_k}{f_1} \right) \left( 1 + \frac{f_1^2}{f_c^2} \right)}{\left( 1 + \frac{f_k}{f_c} \right) 2} \right. \\
&\quad \left. + f_k \ln \frac{f_1 + f_k}{f_c + f_k} - 2f_c \left( \frac{\pi}{4} - \tan^{-1} \frac{f_1}{f_c} \right) \right] \quad (3.7)
\end{aligned}$$

with the signal power being related to the bandwidth by the simultaneous equations

$$P_{sig} = \frac{S_0}{A_0^2} \left[ \frac{2}{3} \frac{f_2^3 - f_1^3}{f_c^2} + \frac{f_k}{2f_c^2} (f_2^2 - f_1^2) - f_k \ln \frac{f_1}{f_2} \right] \quad (3.8)$$

$$0 = \left( 1 + \frac{f_k}{f_2} \right) \left( 1 + \frac{f_2^2}{f_c^2} \right) - \left( 1 + \frac{f_k}{f_1} \right) \left( 1 + \frac{f_1^2}{f_c^2} \right) \quad (3.9)$$

Thus we obtain the familiar results of the waterfilling technique, where the information rate is a monotonically increasing function of signal power, with the signal allocated over an optimal frequency bandwidth. The actual results vary depending on the location of the noise corner frequency and 3 dB frequency. Assuming that the corner frequency occurs somewhere in the bandwidth  $\Delta f$ , the first two terms in equation (3.6) are dependent only on the bandwidth and the flicker noise corner frequency and thus are constant for a given noise spectrum and increasing the bandwidth or the noise corner frequency increases the information rate. The last two terms in equation depend on the cut-off frequency, typically  $f_1 \ll f_c$  and  $f_2 \approx f_c$ , so as  $f_c$  increases  $\tan^{-1}(f_2/f_c)$  remains almost constant while  $\tan^{-1}(f_1/f_c)$  increases linearly. For a constant  $f_k$ , amplifiers with higher 3dB frequencies have higher capacity. For large 3dB frequencies ( $f_c \gg f_{1,2}$ ), the last two terms in equation (3.6) tend to  $-f_c\pi$  and thus cancel. If  $f_c < f_{1,2}$ , that is at small corner frequencies, then the two terms together approach  $2(f_2 - f_1)$ . A plot of the typical input referred noise and the information rate inferred from it is shown in figure 3.2. A quick calculation shows that most of the input referred noise comes from the input differential pair. The input referred noise can be rewritten as follows:

$$\begin{aligned}
S_{Id} &= 4KT\gamma g_m + \frac{K_f}{WLC_{ox}f} \\
\Rightarrow S_{Vg} &= \frac{4KT\gamma}{g_m} + \frac{K_f}{WLC_{ox}fg_m^2} \\
&= S_o \left( 1 + \frac{f_k}{f} \right) \tag{3.10}
\end{aligned}$$

Therefore we can consider a simple hand calculation using real parameters for the

amplifiers given in Table 3.1 assuming a bias current of  $10 \mu\text{A}$  and fabrication in a standard  $0.5 \mu\text{m}$  process with

$$A_0 = g_m R_{out} \quad (3.11)$$

$$S_0 = 4kT\gamma g_m R_{out}^2 \quad (3.12)$$

$$f_k = \frac{K_f I_d^{A_f}}{W L C_{ox} 4K T \gamma g_m} \quad (3.13)$$

$$f_c = \frac{1}{2\pi R_{out} C_{out}} \quad (3.14)$$

where  $C_{out}$  is the dominant pole in this case approximated by the load capacitance.  $R_{out}$  is the total output resistance formed by the output resistances of the transistors at the output. This can allow one to optimize an amplifier for highest capacity or bit energy. The input referred noise and information rate was computed for the OTAs and single transistor amplifiers using equations (3.8), where n type transistors are assumed to be 25/5 and p type to be 75/5 for the OTAs and 200/5 for the single transistor configurations. These sizes are for lambda based designs where  $\lambda = 0.35 \mu\text{m}$ . Since noise scales as the inverse of the area, aspect ratios of the OTAs were chosen such that the noise level would be measurably high under experimental conditions. Figures 3.2 and 3.3 show that the wide swing, folded cascode and wide range OTAs have the lowest input referred noise. This translates into those OTAs having the highest capacity. Experimentally it might be expected that the folded cascode should have lower noise than the wide range OTA since the noise of the other transistors will be divided by a higher gain for the folded cascode than for the wide range. Based on these results one would want to go with the wide swing OTA as it seems that it would have the highest information rate for the differential amplifier.



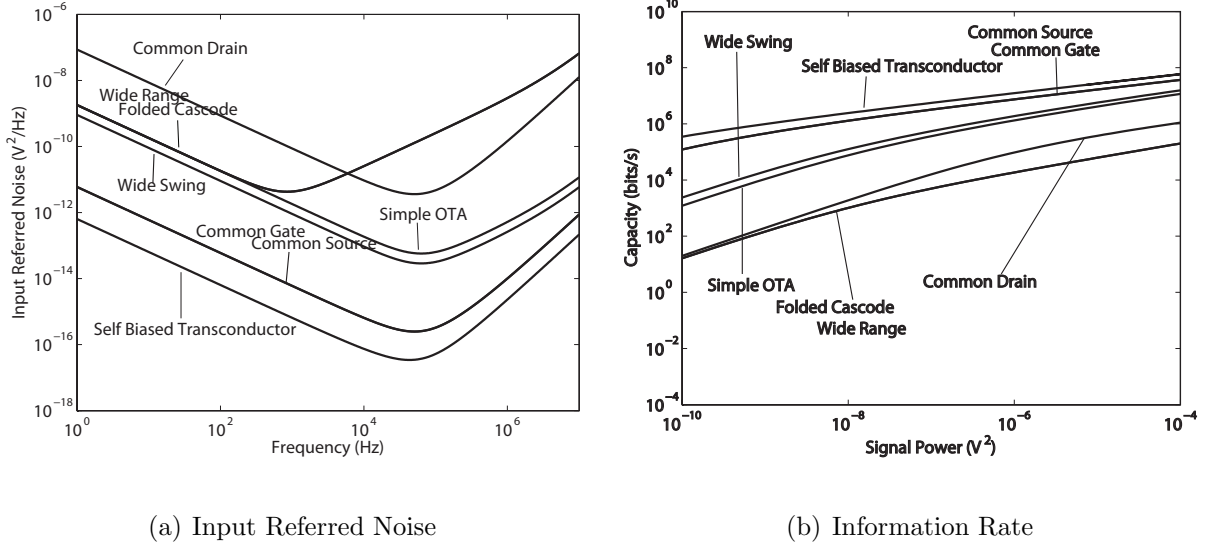


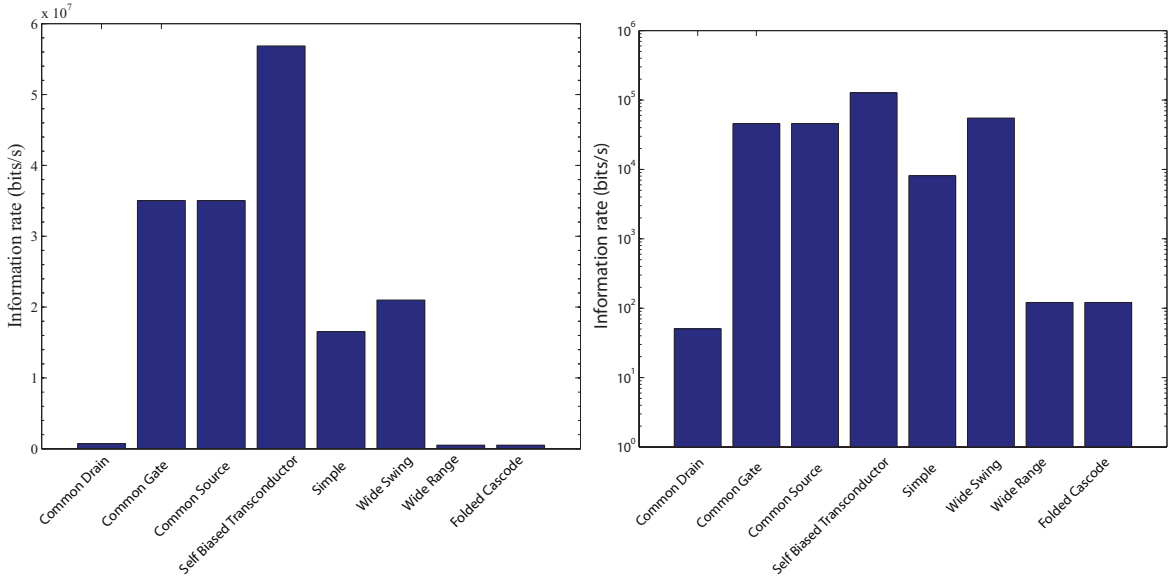
Figure 3.2: Input referred noise spectral density and information rate assuming first order characteristics.

These results may change when considering sizing and power budget constraints, but may be used as a first approximation for design exploration.

The above results are for the case of a single dominant pole. In many cases it may be desirable to use an typical amplifier transfer function with more than one pole or zero, but even in these cases a first order low pass approximation may suffice for hand calculations and design exploration. For an amplifier with  $n$  poles and  $m$  zeroes, the information rate can be found as

$$\begin{aligned}
 C = \frac{1}{\ln 2} & \left[ 2(f_2 - f_1) + f_k \ln \frac{f_1 + f_k}{f_2 + f_k} \right. \\
 & - \sum_{i=1}^n 2f_{pi} \left( \tan^{-1} \frac{f_2}{f_{pi}} - \tan^{-1} \frac{f_1}{f_{pi}} \right) \\
 & \left. + \sum_{j=1}^m 2f_{zj} \left( \tan^{-1} \frac{f_2}{f_{zj}} - \tan^{-1} \frac{f_1}{f_{zj}} \right) \right] \quad (3.15)
 \end{aligned}$$

with the bandwidth limits  $f_2$  and  $f_1$  being determined from the simultaneous equa-



(a) Information rate  $P_{sig} = 10^{-4}$

(b) Information rate  $P_{sig} = 10^{-10}$

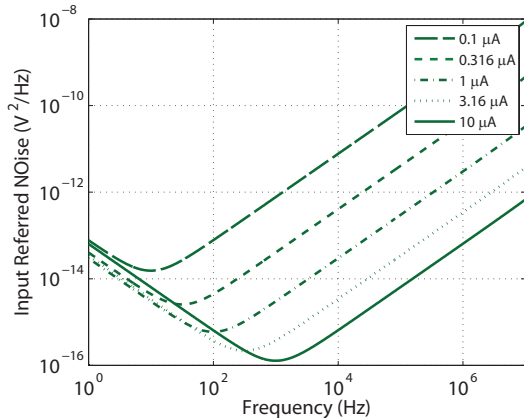
Figure 3.3: Theoretical information rate for power level of  $10^{-4}$  and  $10^{-10}$ .

tions described by equation (3.5). For large input signal power the bandwidth will be large. For every pole introduced the information rate generally decreases. Based on equation (3.15), for every zero introduced the information rate generally increases. As with the first order case the first two terms are constant. The highest pole will cause the most decrease in capacity, while the largest zero will cause the most increase. For typical amplifiers this implies that signal power is optimally allocated at frequencies above the dominant pole of the amplifier. This implies that optimal use of the amplifier is in regions where the signal is not actually amplified, more consideration of the implications of this will be given in chapter 5.

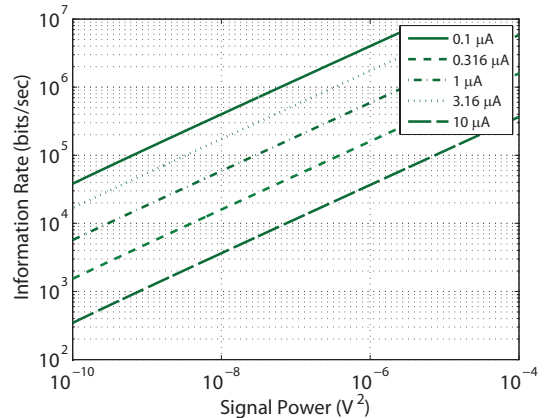
### 3.2.2 Information Rate as Function of Bias Current

We can look at how the information rate changes with the bias current. From equations (3.14), (3.3) and (3.1), it is obvious that the noise spectral density scales as the bias current (assuming  $A_f \approx 1$ ). However the transconductance scales as the square root of the bias current in above threshold operation and linearly with the drain current for subthreshold operation.

Figure 3.4 shows the theoretical results with the bias current logarithmically spaced from  $10 \mu\text{A}$  to  $0.1 \mu\text{A}$ , and with  $W/L$  of  $25/5$  for a standard  $0.5 \mu\text{m}$  process (with  $\lambda = 0.35 \mu\text{m}$ ). This assumes the very simplest model we can for an amplifier that is the noise only comes from the input differential pair and the midband gain is given by the transconductance and the output resistance. Decreasing bias current decreases the input referred noise level and also changes the frequency at which the noise minimum occurs. The latter is mainly due to the effect of the bias current on the dominant pole of the amplifier. We see that as the bias current decreases the information rate increases because the input referred noise is higher, note however that the frequency bands which are filled with the input signal power vary drastically for each bias point. Another thing to note is that for these results, figures 3.2 through 3.3, it has been assumed that the noise corner frequency is less than the 3dB bandwidth, that is  $f_k < f_c$ , so the input referred noise is cup shaped and the noise minimum occurs at relatively low frequencies. This is not necessarily true in general. In such cases particularly if the noise corner frequency approaches or exceeds the 3dB frequency, the noise minimum may occur at much higher frequencies and in



(a) Input Referred Noise



(b) Information Rate

Figure 3.4: Theoretical input referred noise assuming  $W/L=25/5$  and using the simple model. This would apply to a generic amplifier in a lambda based design.

addition the trough of the curve may be more flattened out. In general, however, most of the observed trends in figures 3.2 through 3.3 hold.

### 3.2.3 Noise Efficiency Factor

Other metrics have been introduced to characterize trade-offs between noise and power resources. In particular the noise efficiency factor ( $NEF$ ) [50] compares the amplifier noise to an ideal bipolar transistor with only thermal noise and no base resistance. The equivalent input noise for the bipolar transistor is given by [50]

$$V_{in,rms_{bjt}} = \sqrt{\Delta f \frac{\pi}{2} \frac{4kTV_T}{I_c}} \quad (3.16)$$

where  $\Delta f$  is the frequency bandwidth,  $V_T$  is the thermal voltage and  $I_c$  is the collector current.  $NEF$  is then defined as the ratio of the input noise of the ideal

BJT to the amplifier under consideration.

$$\text{NEF} = V_{in,rms_{amp}} \sqrt{\frac{2I_{tot}}{\pi 4kTV_T \Delta f}} \quad (3.17)$$

where  $I_{tot}$  is the total current drain in the amplifier. Note that since [50] and [8] only consider white noise the same is done for this analysis. For experimentally derived NEF however most authors clearly consider all noise sources measured, and the experimental noise should still track the theoretical trends. The higher the NEF the less efficient the amplifier is in terms of noise and power. By this definition NEF should always be greater than one, since a BJT is the best a designer can hope for in terms of noise. This means that lower NEF implies better noise characteristics. The NEF of all amplifier configurations is shown in Table 3.2. The NEF incorporates power considerations due to the inclusion of the transconductance factor which contains a current level. Figure 3.5 shows the calculated NEF for all the amplifier configurations. The folded cascode and wide range OTAs have the highest noise efficiency factors. The single transistor amplifiers all have the same NEF if they are assumed to have the same bias current. The self biased transconductor has the lowest NEF, which results from the lower bias current of this configuration. Clearly the values plotted can change drastically with the aspect ratios of the transistors. For similarly sized transistors the input referred noise is close in value. This means that a portion of the variation originates from the total bias current of the different topologies. It can be questioned whether figure 3.5 is a fair comparison between the single transistor amplifiers and the OTAs. While this is a valid point, a cursory look at the equations reveal that if the transconductance for each amplifier is held fixed,

Table 3.2: Noise Efficiency Factor of different configurations

Configuration	Noise Efficiency Factor
Common Source	$\sqrt{\left(\frac{g_{m2}}{g_{m1}}+1\right)\gamma\frac{I}{V_t g_{m1}}}$
Common Drain	$\sqrt{\gamma^2\frac{I}{V_t g_{m1}}}$
Common Gate	$\sqrt{(g_{m1}+g_{m2})\gamma\frac{I}{V_t g_{m1}^2}}$
Push Pull	$\sqrt{\gamma\frac{I}{V_t(g_{m1}+g_{m2})}}$
Simple OTA	$\sqrt{2\left(\frac{g_{m3}}{g_{m1}}+1\right)\gamma\frac{I}{V_t g_{m1}}}$
Wide Range	$\sqrt{\left(\frac{4g_{m3}}{g_{m1}}+2\frac{g_{m8}}{g_{m1}}+2\frac{g_{m5cas}}{g_{m1}}+\frac{g_{m8cas}}{g_{m1}}+2\right)\gamma\frac{2I}{V_t g_{m1}}}$
Wide Swing	$\sqrt{\left(4\frac{g_{m3}+g_{m7}}{g_{m1a}+g_{m1b}}+2\right)\gamma\frac{5I}{V_t(g_{m1a}+g_{m1b})}}$
Folded Cascode	$\sqrt{6\left(\frac{g_{m4}}{g_{m1}}+1\right)\gamma\frac{3I}{V_t g_{m1}}}$
Fully Differential Folded Cascode	$\sqrt{\left(2\frac{g_{m4}}{g_{m1}}+2\frac{g_{m6}}{g_{m1}}+6\right)\gamma\frac{5I}{V_t g_{m1}}}$

the single transistor amplifiers will still have a better NEF.

### 3.2.4 Bit Energy

Now recall we also want to incorporate the trade-offs between not only the input signal power and noise but also the power resources available for the applications. And unlike noise efficiency factor we want to include the effect of the supply rails. A likely measure that suggests itself is bit energy. Bit energy is a measure of amplifier efficiency and is defined as the ratio of the cost of using the amplifier to the performance of the amplifier, that is [9]

$$BE = \frac{P_{sys}}{C} \quad (3.18)$$

where  $P_{sys}$  is the power dissipated and  $C$  is the capacity or information rate as

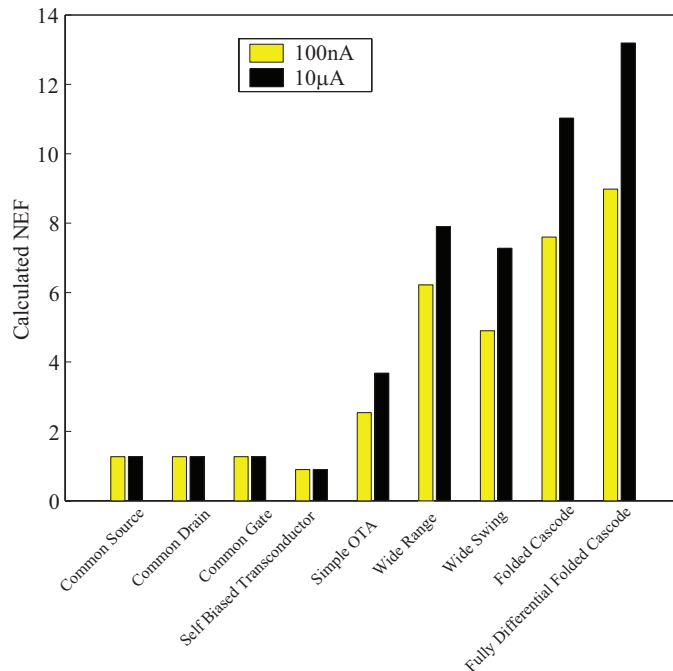


Figure 3.5: Noise efficiency factor of OTAs.

previously defined.  $BE$  defines the energy per bit of the amplifier and is used to compare the different amplifier configurations. It can be interpreted as the energy required by the amplifier to transmit one bit of information. The lower the  $BE$  the more efficient the amplifier is in terms of noise power trade-offs.

In general

$$P_{sys} = I_{tot} (V_{dd} - V_{ss}) \quad (3.19)$$

For a single pole amplifier as  $I_{tot}$  increases  $P_{sys}$  increases and the dominant pole decreases. This implies that the information rate decreases overall and the bit energy increases, implying less efficient operation.

Figure 3.6 shows the bit energy of the OTA's whose information rate was calculated in figure 3.2 for different input signal power levels. The trend is that for

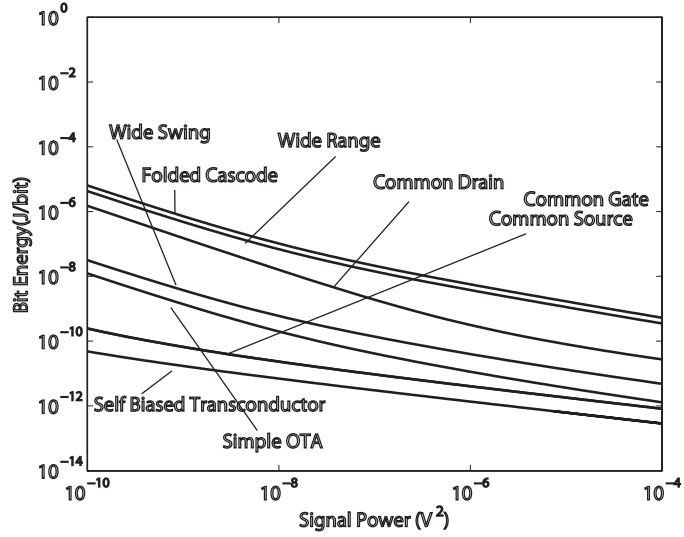
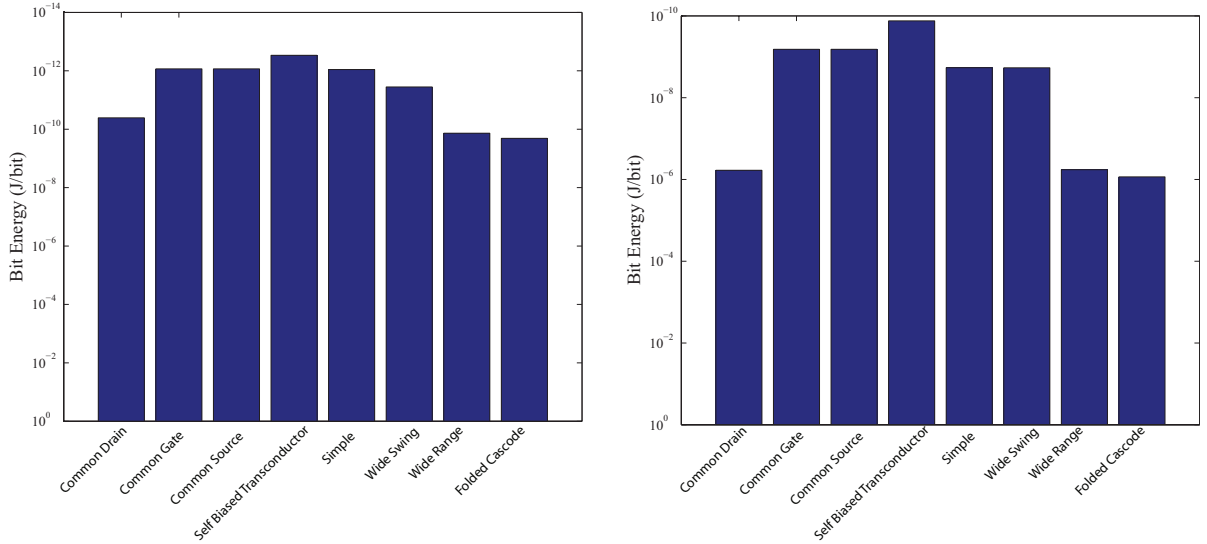


Figure 3.6: Bit energy assuming first order characteristics of amplifiers from Table 3.1

a particular amplifier configuration the bit energy decreases with increasing signal power. Figure 3.7 shows the bit energy at an input signal power of  $10^{-4} \text{ V}^2$ . These graphs show that the highest bit energy (and thus least power efficient operation) is the folded cascode OTA. The simple OTA is seen to be the most power efficient differential amplifier, while the self biased transconductor is the most power efficient amplifier overall. Most of this is explained by the fact that if one moves from the single ended to the OTAs, as the complexity is increased the total bias current flowing through the circuit increases and in some cases (for example the folded cascode) the total power supply may have to be increased so that there is enough head room to keep all transistors in saturation.





(a) Bit energy at  $10^{-4}$

(b) Bit energy at  $10^{-10}$

Figure 3.7: Theoretical bit energy for for two bias currents at a power level of  $10^{-4}$  and  $10^{-10}$ .

### 3.2.5 Other Considerations

All calculations and subsequent experimental measurements are performed in open loop configuration. The use of no feedback in these amplifiers means that experimentally the gain will vary from chip to chip due to mismatch. For OTA's without feedback, stability is easily accomplished by adding a load capacitance. It does however decrease the usable bandwidth (where usable bandwidth is defined, as usual, as that where significant amplification occurs). For experimental measurements there is a buffer located between the OTA and the analyzer. The DIP40 package's leads have a capacitance of 5 pF while the opamp has an input capacitance that is an order of magnitude less than the DIP40 (standard ceramic 40 in dual in-line package) package. The total load capacitance seen by the OTAs is therefore

approximately 5 pF and this number is used in all calculations.

Intuitively NEF is linearly related to the bit energy, however it is expected that bit energy would be a more accurate figure of merit for three reasons. One NEF only considers thermal noise, and no flicker noise (for theoretical calculations), two no frequency effects are considered. Thirdly, and most importantly, NEF does not take into account an input signal power level. It is expected that bit energy would give a more accurate bound for power-noise-signal trade-off considerations. It is also possible to normalize the bit energy by comparing to an ideal bipolar as was done for the NEF factor.

### 3.2.6 Experimental Measurements on Single Transistor Amplifiers

The input referred voltage noise has been experimentally derived and a single transistor configurations (figures 3.8, 3.9, 3.10, 3.11, 3.12, 3.13). The amplifiers were fabricated in a commercial 2-poly, 3-metal, 0.5  $\mu m$  process and the transfer function and output voltage noise were measured using an Agilent 4396B/4395A network/spectrum analyzer. Compared to the theoretical trends for comparing the amplifier topologies, it appears that the model is not quite good enough. Some of the trends such as the common gate and common source having similar input referred noise and therefore similar information rate did not hold experimentally. This is due in part to the transfer functions being further apart than predicted by the model as well as the difference in output referred noise. However the trends predicted for the information rate and bit energy still hold. The theoretical change

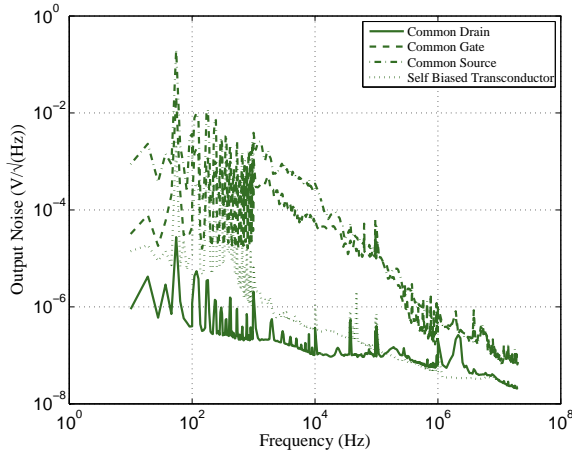
of the noise with bias current matches the experimental variation. Chapter 4 further explores using better models to match the experimental measurements.

### 3.2.7 Experimental Measurements on OTAs

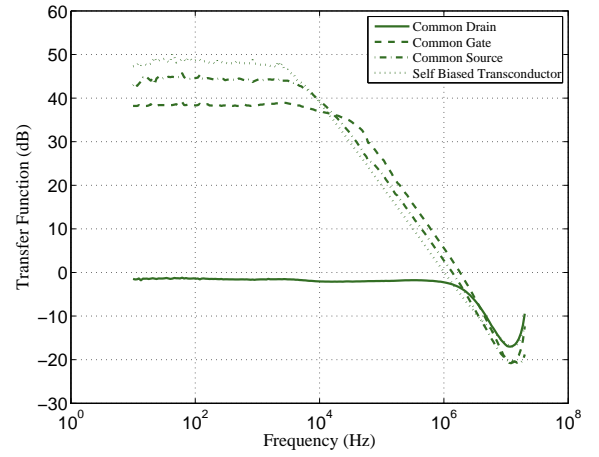
The input referred voltage noise has been experimentally derived and a preliminary comparative analysis has been performed for the OTAs (figures 3.14, 3.15, 3.16, 3.17, 3.18, 3.19, 3.20). The amplifiers were fabricated in a commercial 2-poly, 3-metal,  $0.5 \mu m$  process and the transfer function and output voltage noise were measured using an Agilent 4396B/4395A network/spectrum analyzer.

The OTA's differential pairs are all 25/5 and the PMOS are 75/5. Again these aspect ratios are lambda based and the numerator and denominator must be multiplied by  $\lambda = 0.35 \mu m$  to obtain the actual fabricated sizes. Decreasing the area increases the flicker noise contribution, however the gain goes as the transconductance,  $g_m$ , which is proportional to the aspect ratio of the transistor and is also inversely proportional to the drain current. The theoretical calculations of the input referred noise and capacity show a reasonable agreement with the experimental.

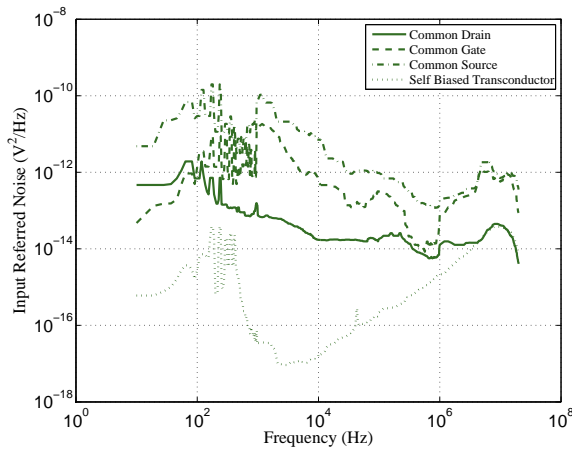
It is worthwhile to notice that the trends of the experimental results agree with the theoretical plots in Figures 3.2 and 3.6. This means that when designing an amplifier, while the first order approximation will not be the same value for the information rate or bit energy as the experimental, it can be used to accurately predict trends. Some of the differences in the experimental noise measurements for the different bias currents, particularly for some of the figures where the input



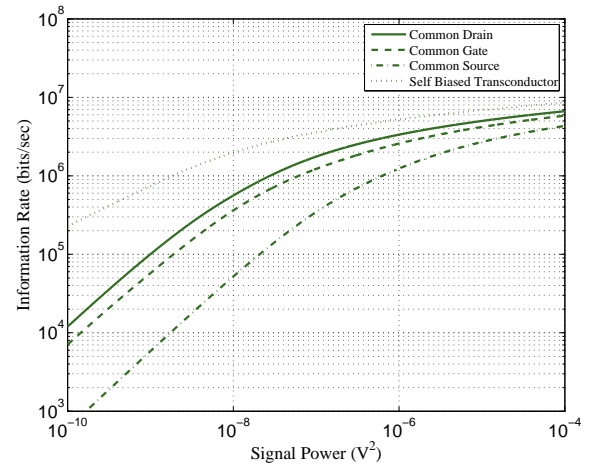
(a) Output Noise



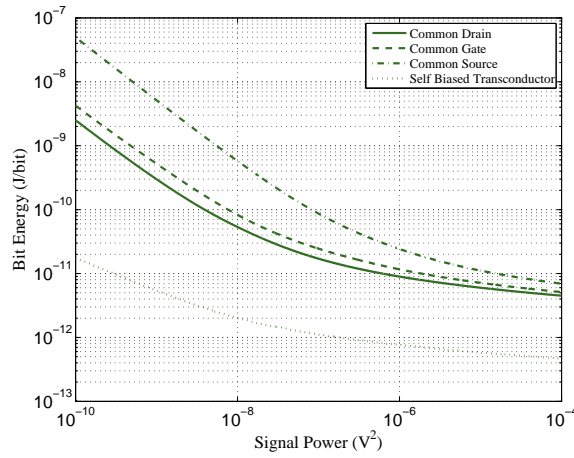
(b) Transfer Function



(c) Input Referred Noise

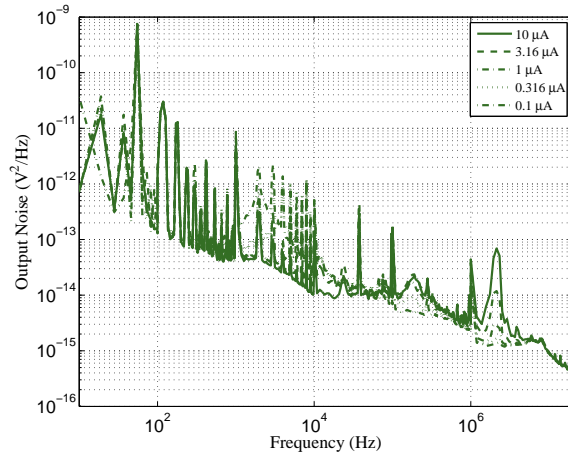


(d) Information Rate

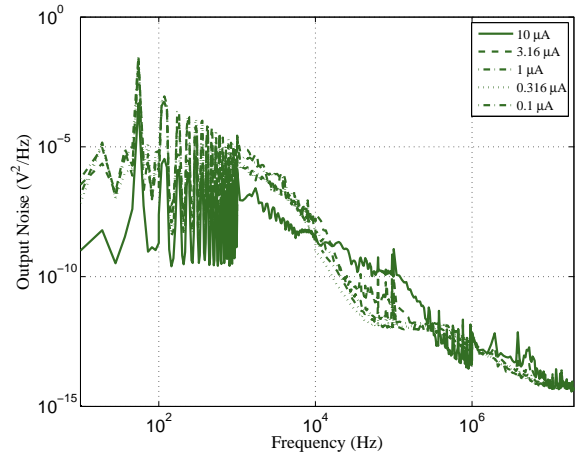


(e) IBit Energy

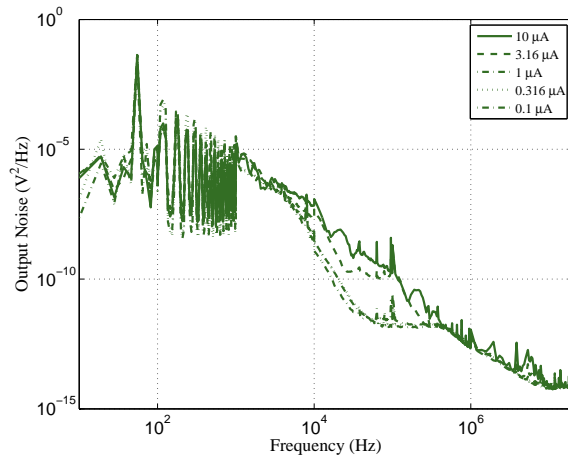
Figure 3.8: Experimental noise and transfer functions for single transistor configurations.



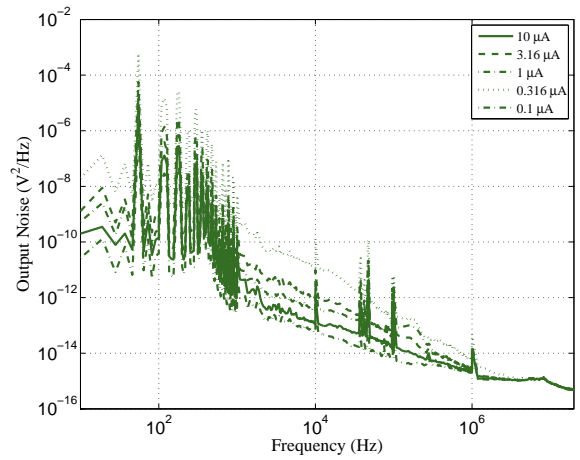
(a)  $S_{out}$  Common Drain



(b)  $S_{out}$  Common Gate

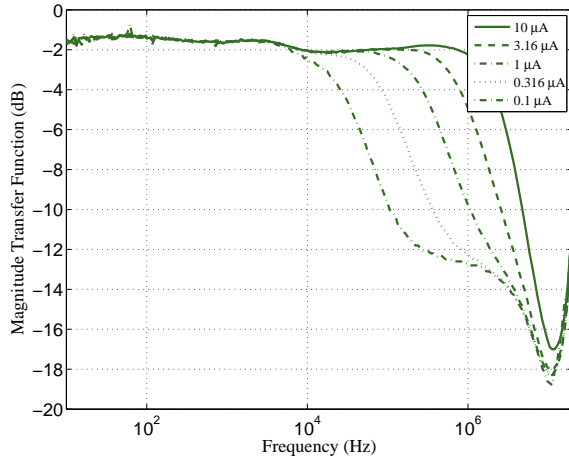


(c)  $S_{out}$  Common Source

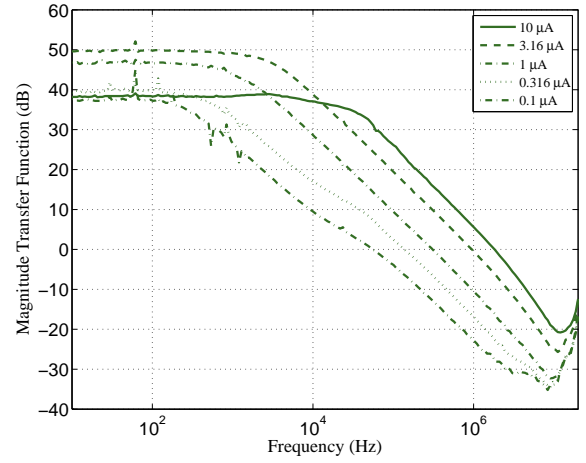


(d)  $S_{out}$  Self Biased Transconductor

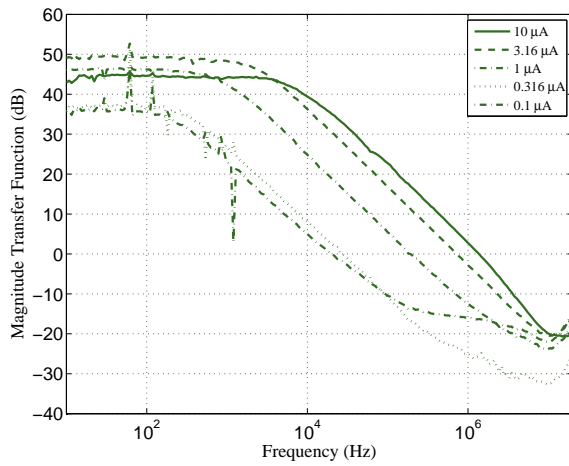
Figure 3.9: Measured output noise for different single transistor topologies at varying bias conditions.



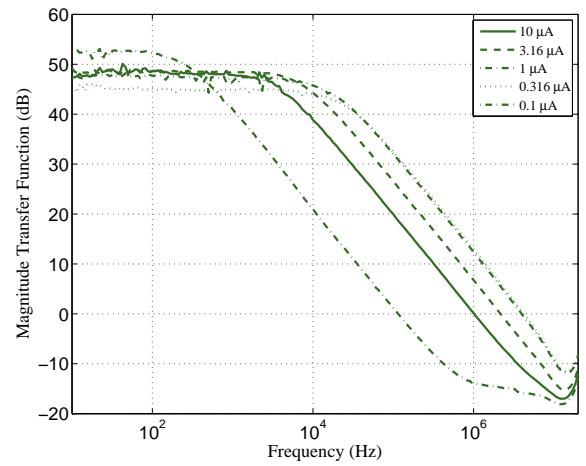
(a)  $|H(f)|$  Common Drain



(b)  $|H(f)|$  Common Gate

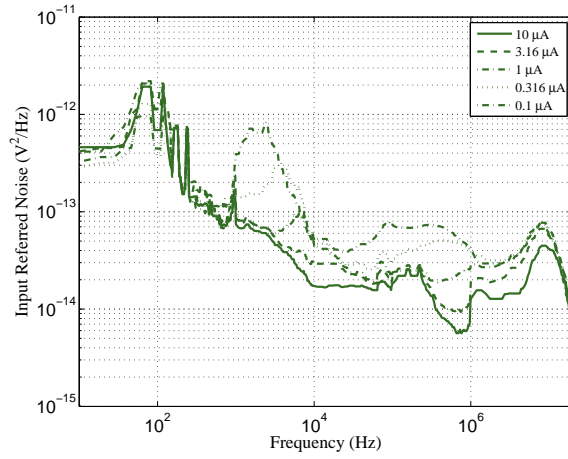


(c)  $|H(f)|$  Common Source

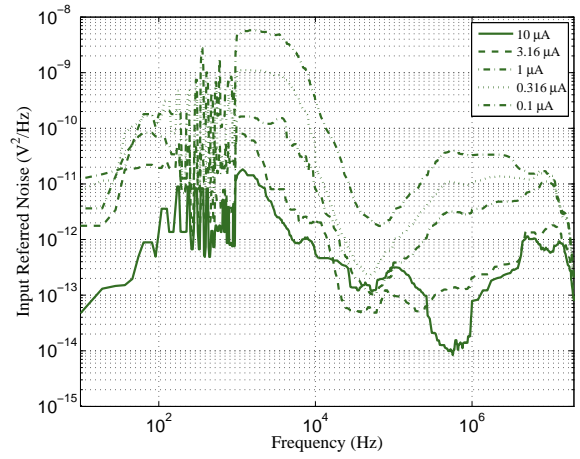


(d)  $|H(f)|$  Self Biased Transconductor

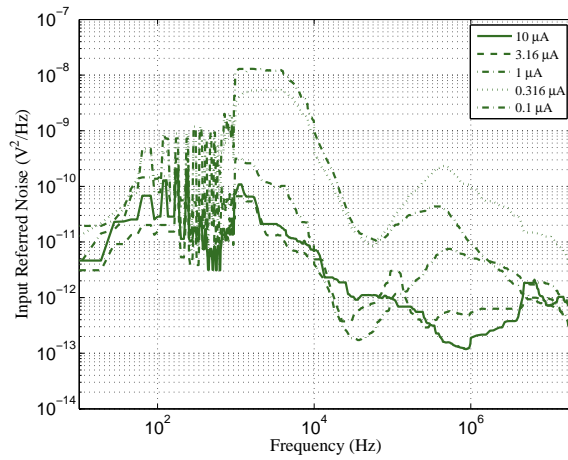
Figure 3.10: Transfer function for single transistor topologies at varying bias conditions.



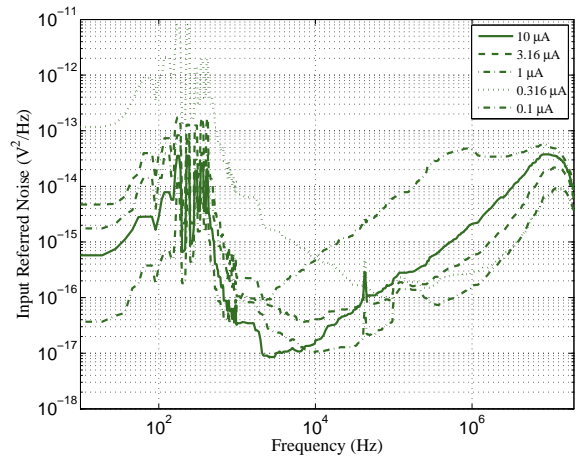
(a)  $S_{in}$  Common Drain



(b)  $S_{in}$  Common Gate

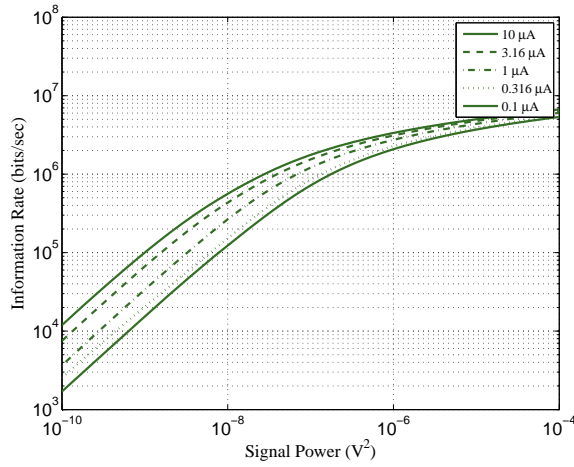


(c)  $S_{in}$  Common Source

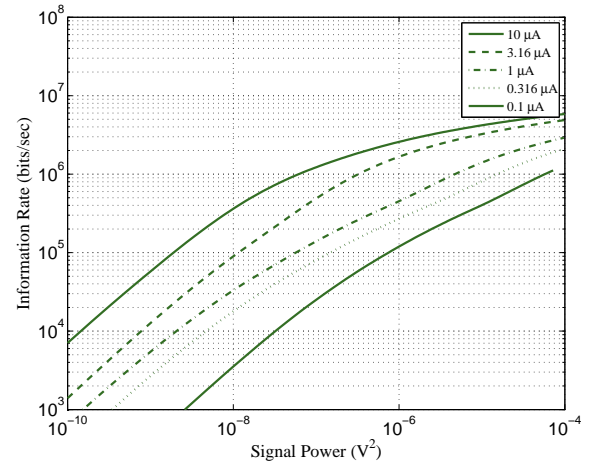


(d)  $S_{in}$  Self Biased Transconductor

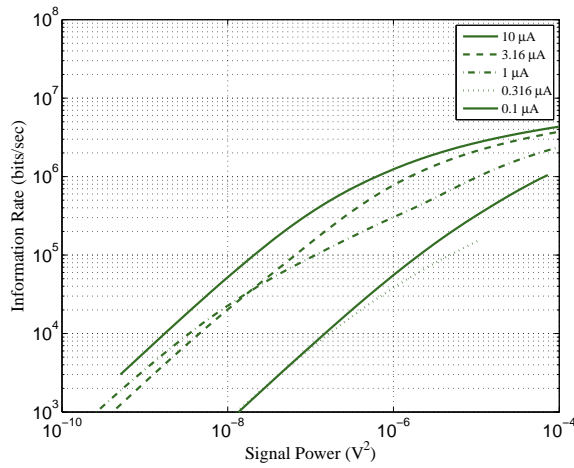
Figure 3.11: Experimentally derived input referred noise for single transistor topologies at varying bias current.



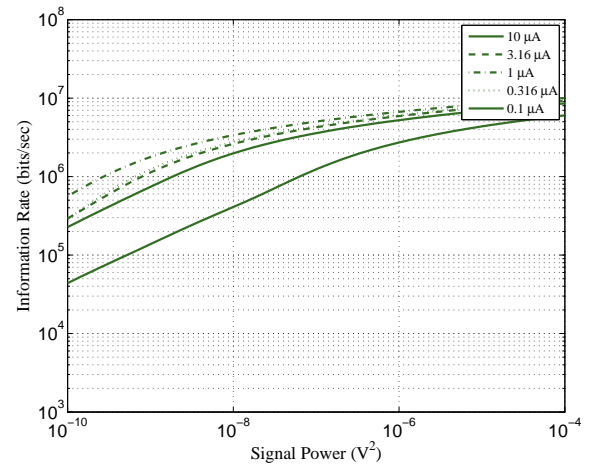
(a) Common Drain



(b) Common Gate



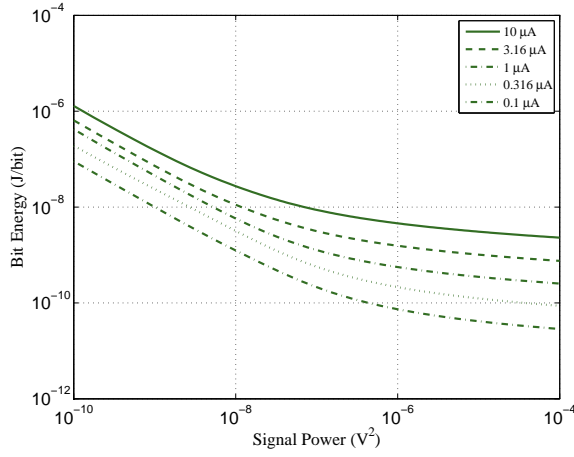
(c) Common Source



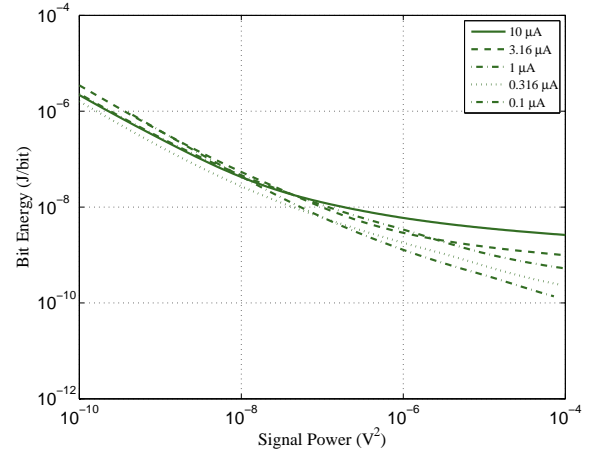
(d) Self Biased Transconductor

Figure 3.12: Experimentally derived information rate at different bias conditions for single transistor configurations.

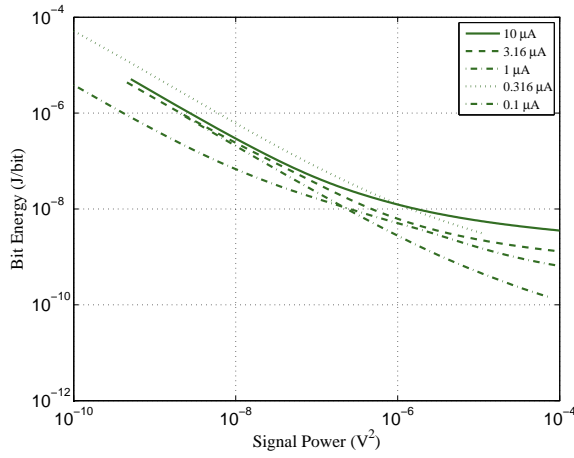




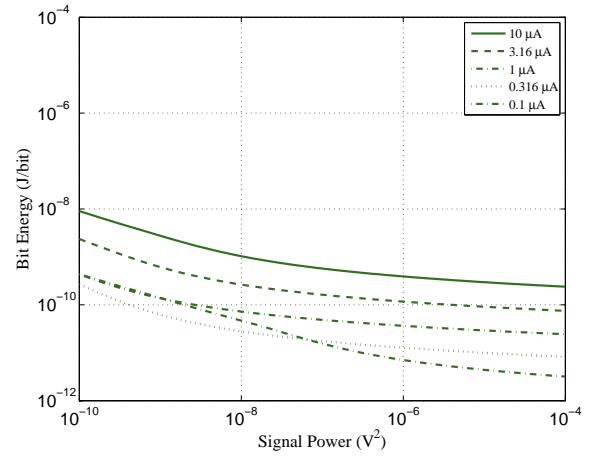
(a) Common Drain



(b) Common Gate



(c) Common Source



(d) Self Biased Transconductor

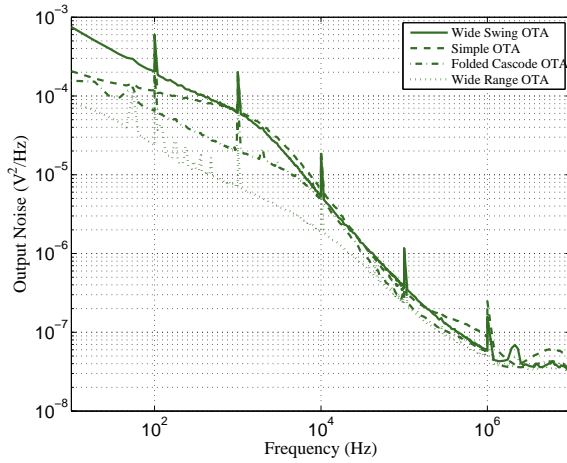
Figure 3.13: Experimentally derived bit energy at different bias conditions for single transistor configurations.

referred noise (and thus the resulting information rates and bit energy) are not spaced in the same manner as seen in the transfer function is mainly due to the higher than expected noise for some of the traces at higher frequencies.

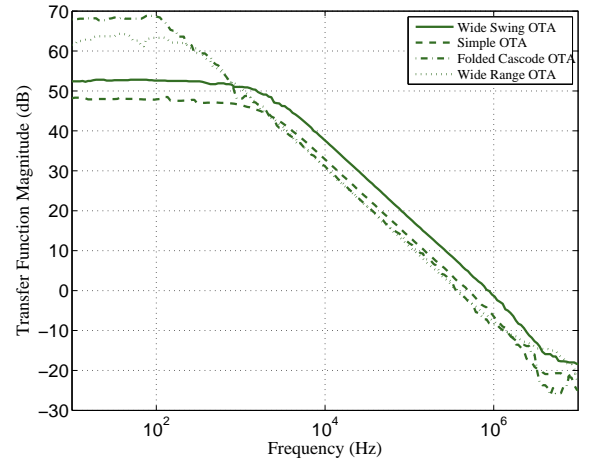
Figures 3.15 and 3.16 shows the measured output and transfer function for the different OTAs at bias conditions ranging from  $10 \mu\text{A}$  to  $0.1 \mu\text{A}$ . It can be seen, as predicted theoretically, that increasing bias current increases the output noise.

Figure 3.18 shows the calculated information rate for all the OTAs based on the measurements in figures 3.15,3.16 and 3.17 , while figure 3.19 shows the calculated bit energy for all the OTAs at different bias conditions and varying power levels. The graphs are summarized in the bar charts in figure 3.20. Clearly increasing bias current decreases the information rate and also increases the bit energy. This tracks well with the prediction of the simple model. However this should not be done arbitrarily as the other design constraints and goals also need to be considered. This is expounded upon in more detail in chapter 4.

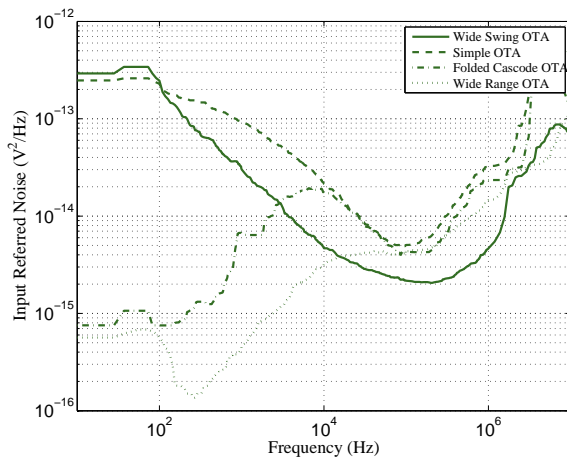
As a final word on the data presented thus far, the question could be asked why not compare amplifier topologies on the basis of having the same gain. This question does have some merit, and in Chapter 4, we examine the trade-offs involved when comparing information rate and bit energy to the other amplifier parameters and target characteristics. However, traditional design assumes the input differential pair gives rise to most of the noise, therefore choosing similar sizes, and then choosing the PMOS sizes based on the current flowing through them gives the amplifier transistor aspect ratios as explained in this section.



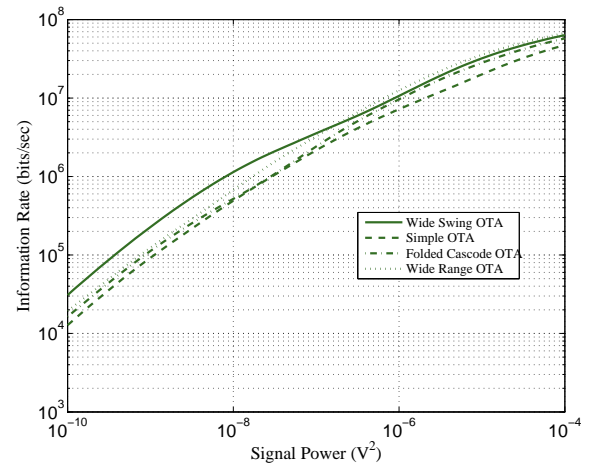
(a) Output Noise



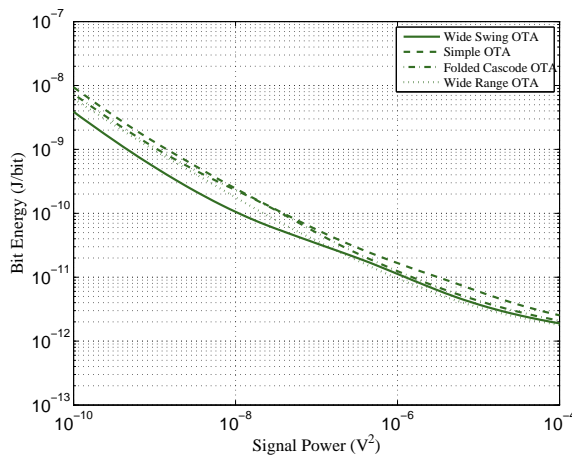
(b) Transfer Function



(c) Input Referred Noise

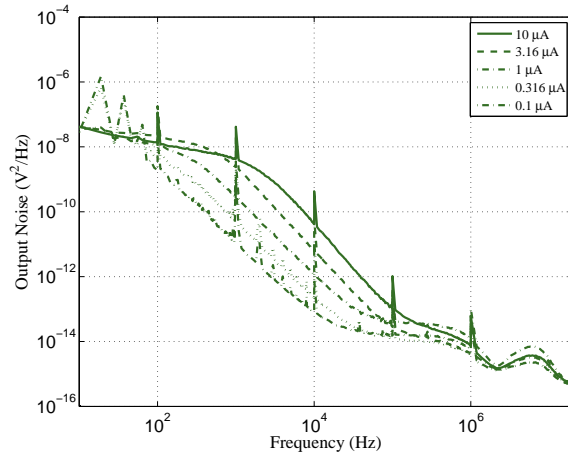


(d) Information Rate

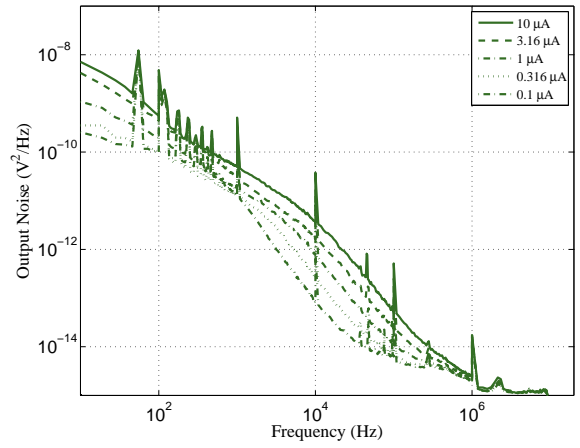


(e) Input Referred Noise

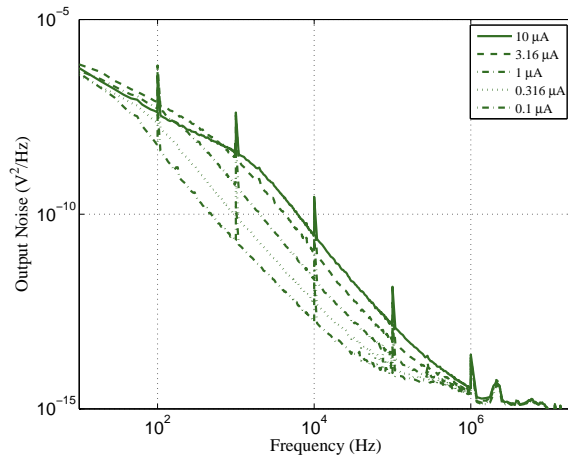
Figure 3.14: Experimental noise and transfer functions for all four OTAs with bias current of  $10 \mu A$ .



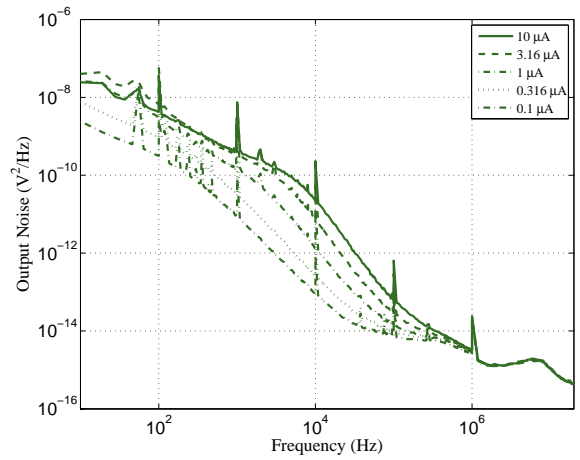
(a)  $S_{out}$  Simple OTA



(b)  $S_{out}$  Wide Range OTA

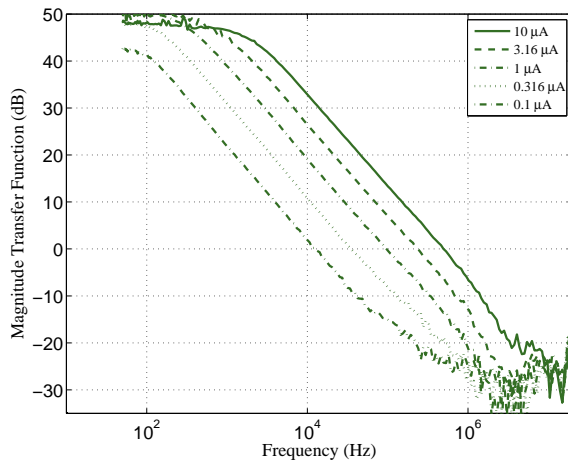


(c)  $S_{out}$  Wide Swing OTA

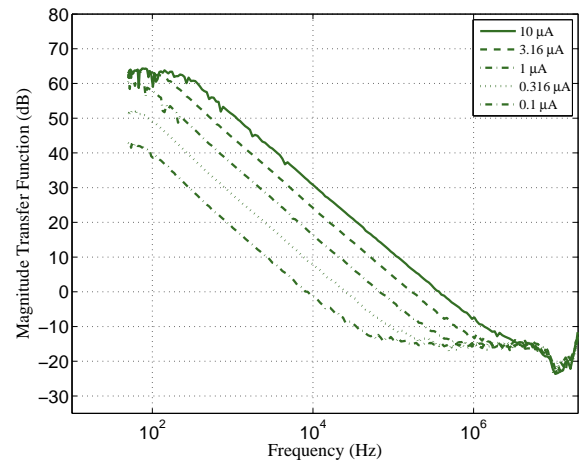


(d)  $S_{out}$  Folded Cascode OTA

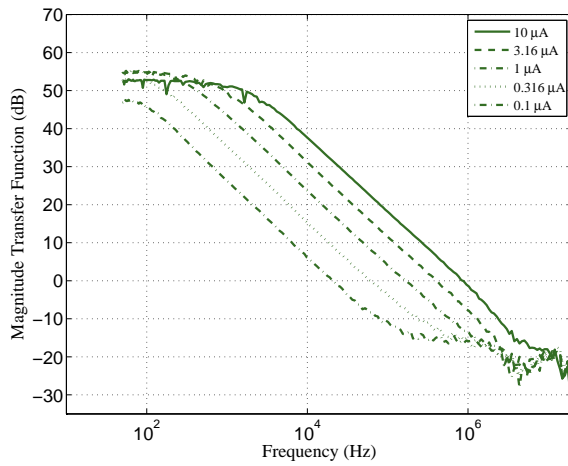
Figure 3.15: Measured output noise for different OTA topologies at varying bias conditions.



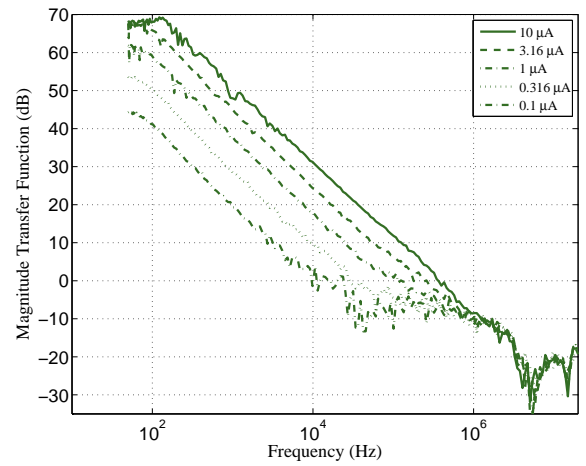
(a)  $|H(f)|$  Simple OTA



(b)  $|H(f)|$  Wide Range OTA

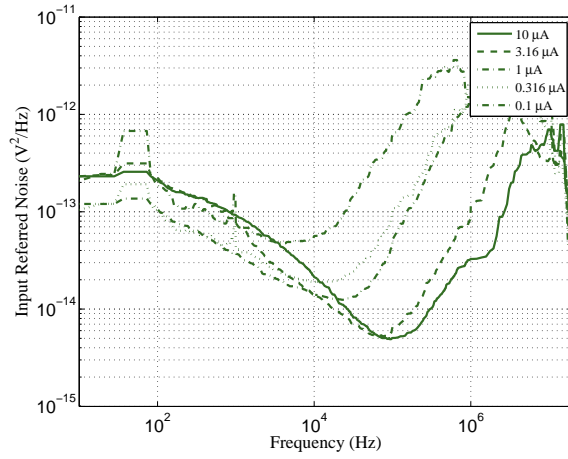


(c)  $|H(f)|$  Wide Swing OTA

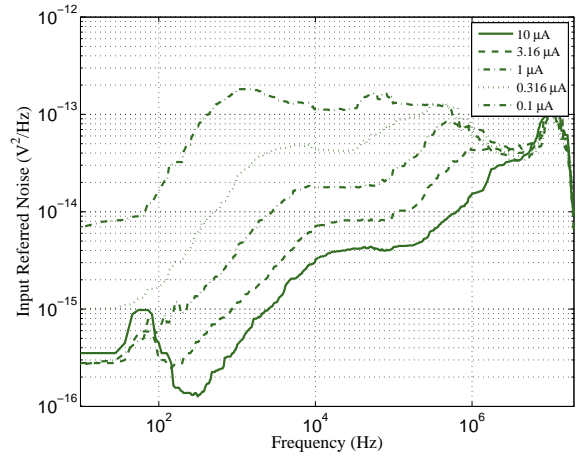


(d)  $|H(f)|$  Folded Cascode OTA

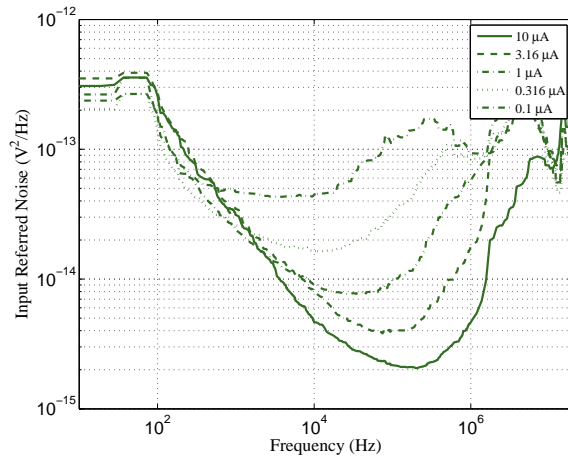
Figure 3.16: Transfer function for OTA topologies at varying bias conditions.



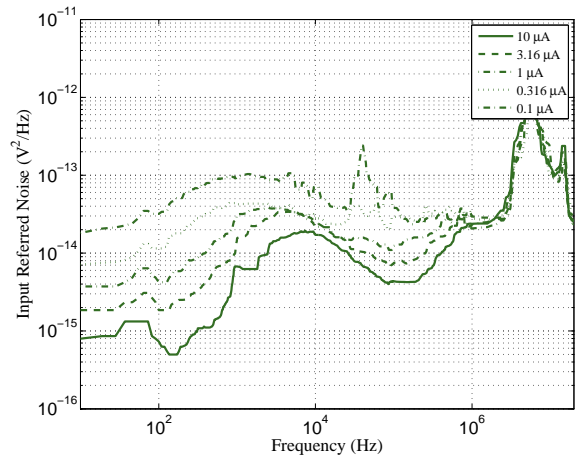
(a)  $S_{in}$  Simple OTA



(b)  $S_{in}$  Wide Range OTA

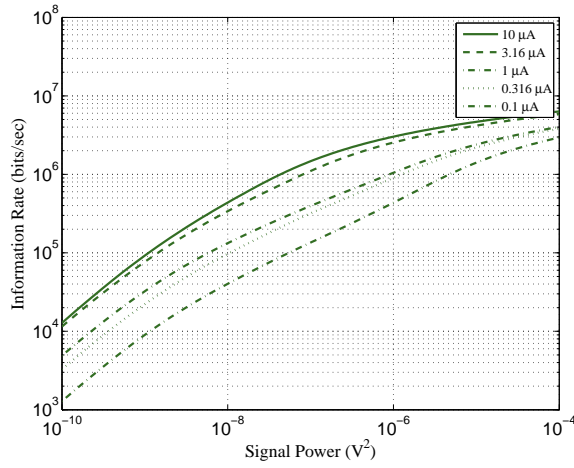


(c)  $S_{in}$  Wide Swing OTA

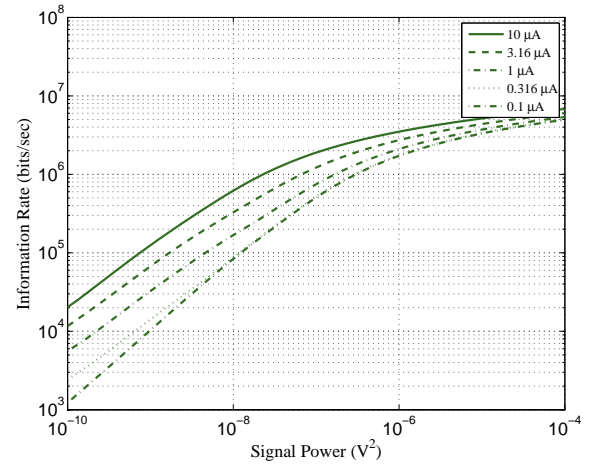


(d)  $S_{in}$  Folded Cascode OTA

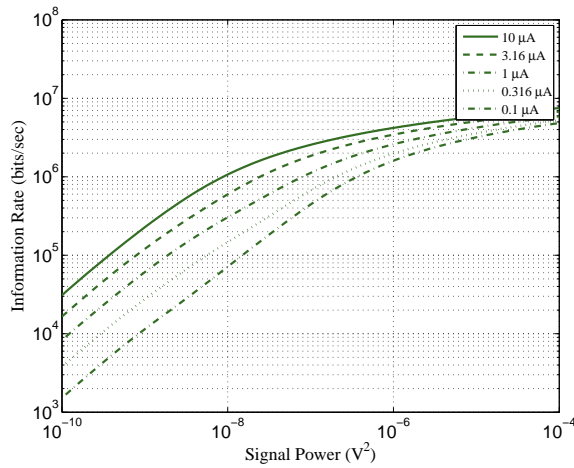
Figure 3.17: Experimentally derived input referred noise for OTA topologies at varying bias current.



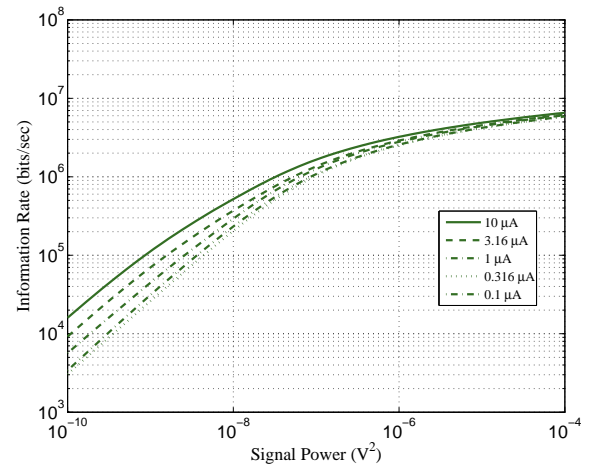
(a) Simple OTA



(b) Wide Range OTA

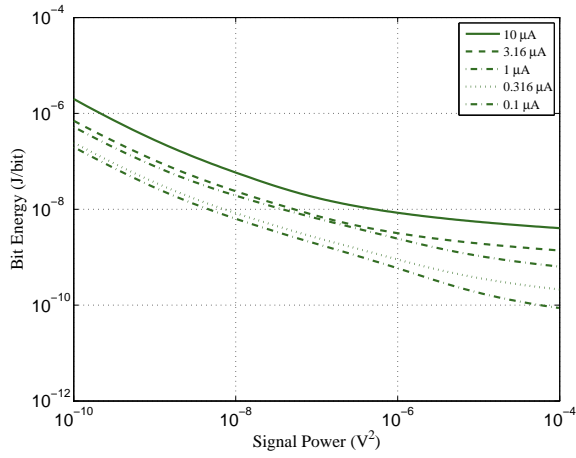


(c) Wide Swing OTA

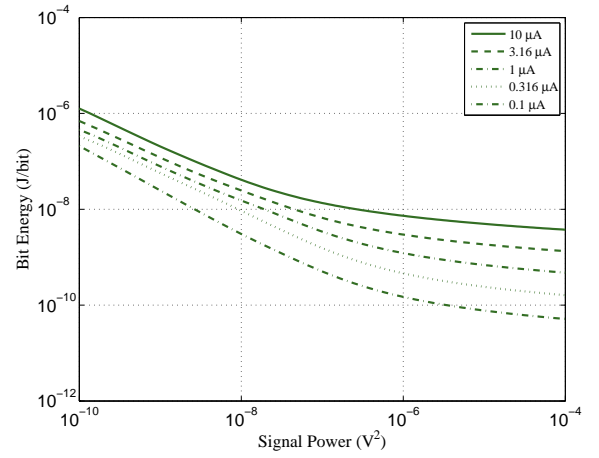


(d) Folded Cascode OTA

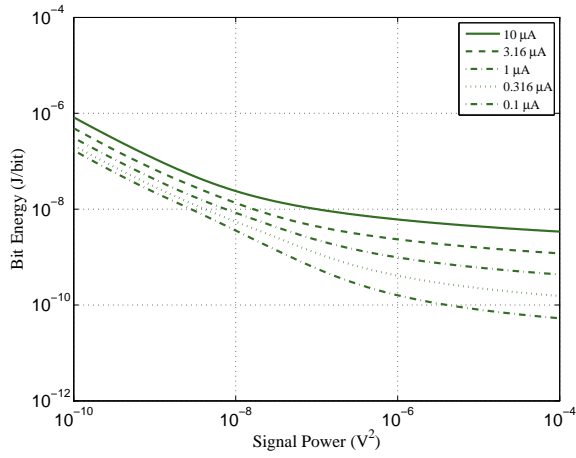
Figure 3.18: Experimentally derived information rate at different bias conditions.



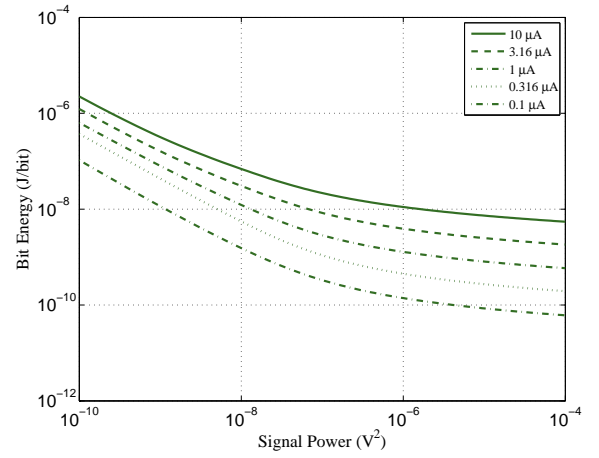
(a) Simple OTA



(b) Wide Range OTA



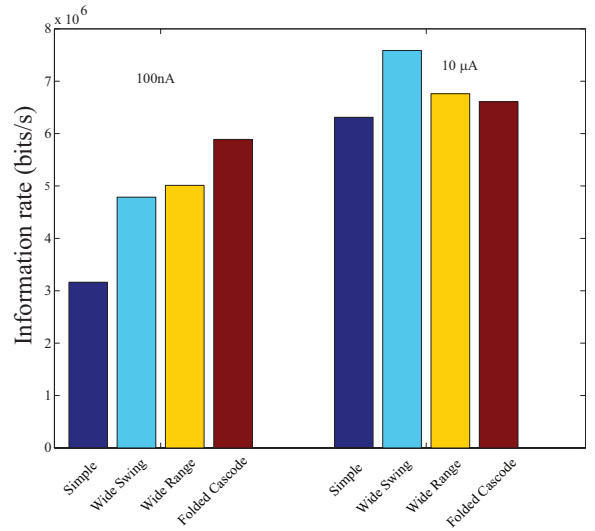
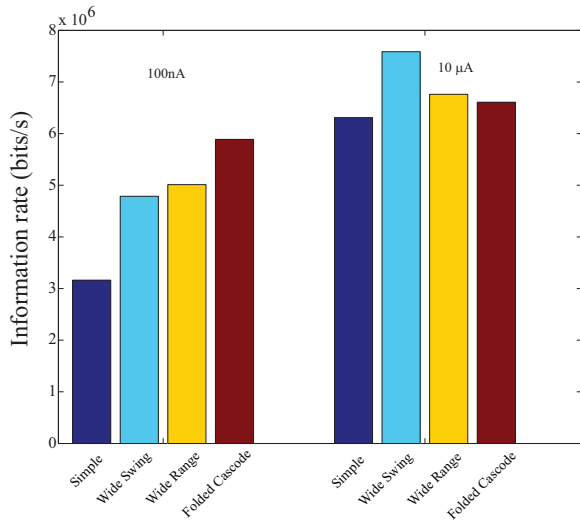
(c) Wide Swing OTA



(d) Folded Cascode OTA

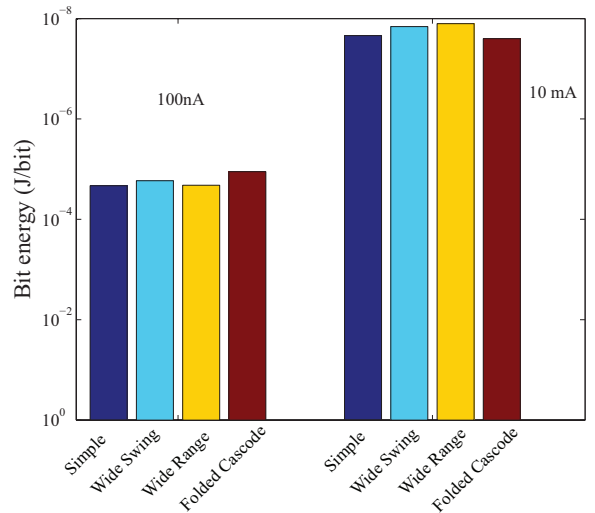
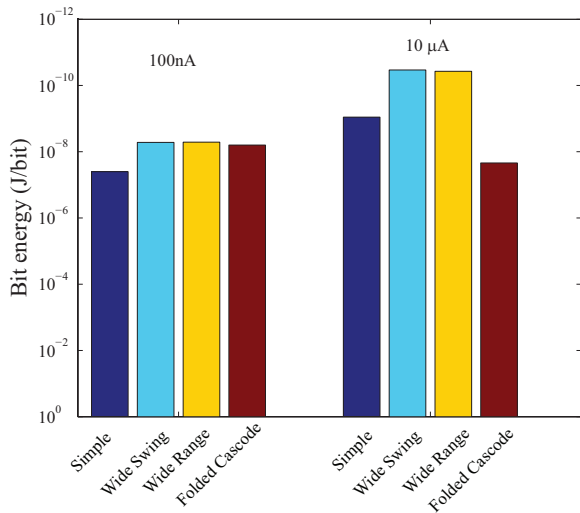
Figure 3.19: Experimentally derived bit energy at different bias conditions.





(a) Information Rate:  $P = 10^{-4}$

(b) Information Rate:  $P = 10^{-10}$



(c) Bit Energy:  $P = 10^{-4}$  Simple OTA

(d) Bit Energy:  $P = 10^{-10}$

Figure 3.20: Experimentally derived information rate for bias currents 10  $\mu$ A and 100  $\mu$ A for the OTA configurations.

### 3.2.8 Information Rate of Amplifiers Fabricated in Different Processes

In addition to investigating amplifiers in the same process, we may face a choice of processes in which to fabricate. Two such processes were used by the lab to implement a bioamplifier based on the popular Harrison design [4,8]. They were implemented in a  $0.5 \mu m$  process and in the  $0.13 \mu m$  8-metal, 1-poly process. The amplifier is shown in figure 3.21 where the OTA is a wide range OTA similar to that depicted in figure 3.1 with PMOS input differential pair. In the  $0.5 \mu m$  process the input PMOS are 100/6 and the NMOS are 10/10 with the rest of the transistors as 20/10,  $C_2 = 200$  fF and  $C_1 = 20$  pF ( $R=10/10$  and  $\lambda = 0.35 \mu m$ ). For the  $0.13 \mu m$  process the input PMOS are 24/1.2 and the NMOS are 2.4/2.4 with all other PMOS as 4.8/2.4,  $C_2=98.3$ fF and  $C_1 = 10$  pF (The resistors are  $0.5/20$  and sizes are in  $\mu m$ ). The input referred noise of the OTA can be calculated from the input referred noise of the amplifier as [8]

$$S_{amplifier} = \left( \frac{C_1 + C_2 + C_{in}}{C_1} \right)^2 S_{OTA} \quad (3.20)$$

where  $C_{in}$  is the input capacitance of the OTA.

The measured output noise and transfer function along with the experimentally derived information rate and bit energy is shown in figure 3.22. The designs are not necessarily going to be exactly the same as for the application under consideration (sensing action potentials) the gain need not be exactly the same, it just need to be known. It is noted that the  $0.5 \mu m$  process amplifier has a higher in-

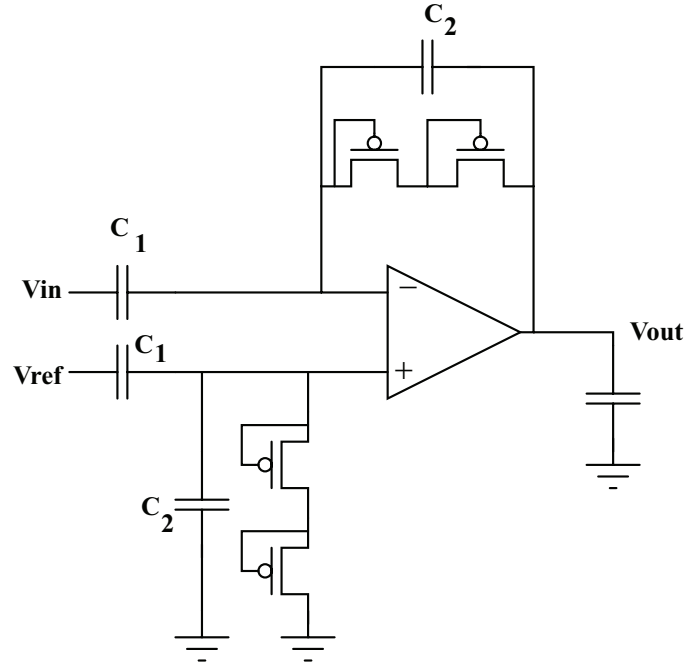
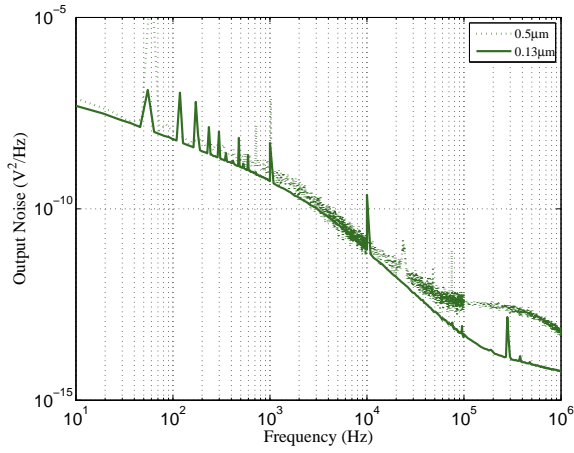


Figure 3.21: Bioamplifier based on Harrison design.

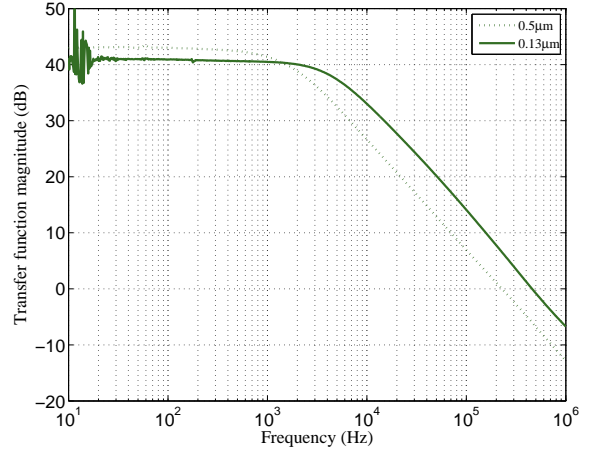
formation rate. It is theorized that this is most likely due to it having a slightly wider trough in its input referred noise spectrum to fill than the  $0.13 \mu\text{m}$  process. The power supply for the  $0.13 \mu\text{m}$  process is lower than the  $0.5 \mu\text{m}$  process ( $2.5 \text{ V}$  versus  $3 \text{ V}$ ), however the amplifiers modest decrease in voltage supply is not enough to compensate for the large difference in information rate.

### 3.3 Chapter Summary

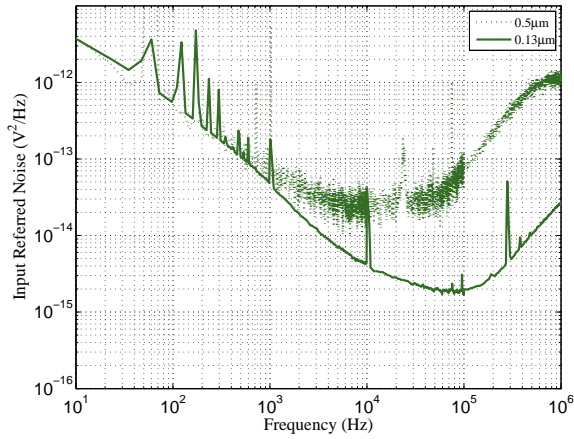
In this chapter a simple first order model was used to theoretically calculate the input referred noise power spectral density for an amplifier along with the information rate and bit energy. Varying the bias current (and thus the inversion level) changes the input referred noise and thus changes the information rate. The bit



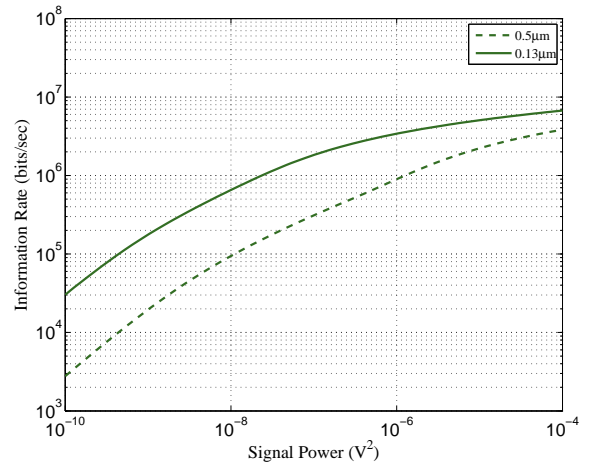
(a) Output Noise



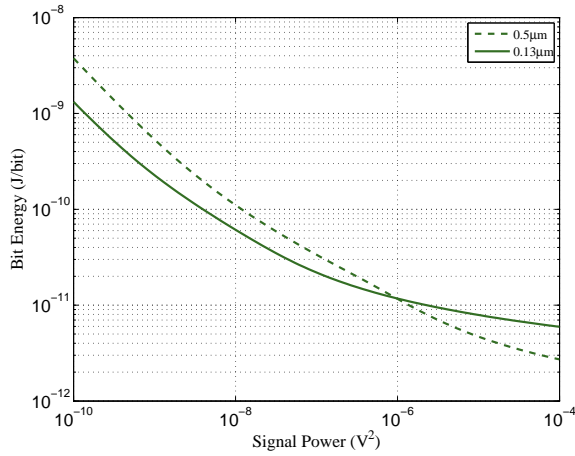
(b) Transfer Function



(c) Input Referred Noise



(d) Information Rate



(e) Bit Energy

Figure 3.22: Experimental  $0.5 \mu\text{m}$  and  $0.13 \mu\text{m}$  process. Sizes are different but characteristics are the same.

energy was defined as the ratio of the power required by the system to the information rate, and is especially useful when comparing different amplifier topologies. The input referred noise and transfer function was also experimentally measured for a standard  $0.5 \mu\text{m}$  and  $0.13 \mu\text{m}$  process and the the information rate and bit energy were determined from the experimental measurements. It was found that the trends predicted by the first order model for changing bias conditions, agreed with the trends that were displayed by the experimental results.

## Chapter 4

### Tradeoffs in a Single Amplifier Design

In the previous chapter different amplifier configurations were compared. In this chapter the research question is not just how does the information rate and bit energy for a particular amplifier topology vary in terms of the bias current,  $I_d$ , and the aspect ratio  $W$  and  $L$ , but how does it compare with the target gain, 3dB bandwidth and power supply requirements.

#### 4.1 Design Constraints on a Simple OTA Topology

We choose to optimise the simple OTA topology and examine how the use of information rate and bit energy fits with the standard amplifier design equations. For a simple OTA the DC equations can easily be written as

$$I_{D_1} = I_{D_2} = I_{D_3} = I_{D_4} = \frac{I_{D_5}}{2} = \frac{I_B}{2} \quad (4.1)$$

$$V_{DS_3} = V_{GS_3} = V_{DD} - V_X \quad (4.2)$$

$$V_{IN_1} = V_{IN_2} \quad (4.3)$$

$$V_S = V_{IN_1} - V_{GS_1} \quad (4.4)$$

$$V_M = V_{SS} + V_{GS_5} \quad (4.5)$$

$$V_{SB_{1,2}} = V_S - V_{SS} \quad (4.6)$$

$$V_{DS_1} = V_X - V_S \quad (4.7)$$

$$V_{DS_5} = V_S - V_{SS} \quad (4.8)$$

To facilitate hand calculations equations (3.14), (3.3) and (3.1) can be recast using the EKV model which is valid in all regions of operation.

Briefly the EKV model, named after Enz-Krummenacher-Vittoz, is a continuous model valid in all regions of MOSFET operation from subthreshold to above threshold [51, 52]. The MOSFET IV characteristics are:

$$I_D = \begin{cases} \frac{1}{2} \frac{\mu C_{ox}}{2} \frac{W}{L} (V_{gs} - V_T)^2 & \text{strong inversion} \\ \frac{2\mu C_{ox} U_T^2}{\kappa} \frac{W}{L} e^{\frac{V_{gs} - V_T}{nU_T}} & \text{weak inversion} \\ I_s \ln^2 \left( 1 + \exp \left( \frac{\kappa(V_{gs} - V_T)}{2U_T} \right) \right) & \text{valid in all regions} \end{cases}$$

where

$$I_s = \frac{W}{L} 2U_T^2 \frac{\mu C_{ox}}{\kappa} \quad (4.9)$$

and the transconductance is given by

$$\begin{aligned}
 g_m &= \frac{\kappa I_D}{U_T} G(I_D) \\
 G(I_D) &= \frac{1 - e^{-\sqrt{I_D/I_S}}}{\sqrt{I_D/I_S}} \text{ or } \frac{2}{1 + \sqrt{1 + 4I_D/I_S}}
 \end{aligned} \tag{4.10}$$

where  $I_d/I_s$  is the inversion coefficient (IC) and  $\kappa$  is the subthreshold slope where  $\kappa$  is  $\approx 0.7$ . Subthreshold saturation is for  $V_{ds} \geq 4U_T \approx 100$  mV and subthreshold ohmic is for  $V_{ds} \leq 4U_T$ . The inversion level is related to the gate voltage and the threshold voltage:

$$\begin{aligned}
 V_{gs} &\geq V_t + 100mV && \text{strong inversion} \\
 V_t + 100mV &\geq V_{gs} \geq V_t - 100mV && \text{moderate inversion} \\
 V_{gs} &\leq V_t - 100mV && \text{weak inversion}
 \end{aligned} \tag{4.11}$$

or alternatively it can be related in terms of the bias current and the  $I_s$  (the technology current times the aspect ratio  $W/L$ ).

$$\begin{aligned}
 I_D &\geq 10I_s && \text{strong inversion} \\
 10I_s &\geq I_D \geq 0.1I_s && \text{moderate inversion} \\
 I_D &\leq 0.1I_s && \text{weak inversion}
 \end{aligned} \tag{4.12}$$

This leads to a rewriting of the major design parameters and constraints, 3dB



frequency, mid band gain and noise corner frequency, in terms of IC as

$$\begin{aligned}
A_o &= \frac{\kappa}{U_T} \frac{1 - e^{-\sqrt{IC}}}{\sqrt{IC}} V_{A_{2,4}} \\
S_o &= \frac{4kT\gamma}{\frac{\kappa I_D}{U_T} \frac{1 - e^{-\sqrt{IC}}}{\sqrt{IC}}} \\
f_k &= \frac{K_f}{WLC_{ox} 4kT \frac{\kappa}{U_T} \frac{1 - e^{-\sqrt{IC}}}{\sqrt{IC}}} \\
f_{3dB} &= \frac{ICI_o W/L}{2\pi V_{A_{2,4}} C_{out}} \\
V_{A_{2,4}} &= \frac{V_{A_2} V_{A_4}}{V_{A_4} + V_{A_2}}
\end{aligned}$$

The information rate can then also be recast in terms of inversion level. The factor  $\gamma$  which has previously been identified as being 1/2 in weak inversion and 2/3 for strong inversion can be modeled across all operating regions as

$$\gamma = \frac{1}{1 + IC} \left( \frac{1}{2} + \frac{2}{3} IC \right) \quad (4.13)$$

to account for how it continuously changes smoothly from weak through the moderate and strong inversion regions [51].

The bias current flowing through transistor M5 is a design parameter as well as the aspect ratios of all transistors. The low frequency gain is traditionally written as:

$$A_0 = g_{m1} (r_{o2} \parallel r_{o4}) = \sqrt{\frac{\mu C_{ox} W/L}{I_{bias}}} \frac{1}{\lambda_2 + \lambda_4} \quad (4.14)$$

in saturation using the square law model. As mentioned in the previous chapter this can instead be written using the EKV model and now the design parameter is rather the inversion coefficient, IC. Recall that if IC is less than 0.1 the operation is in weak inversion and greater than 10 is in strong inversion, and an IC of 1 represents the

midpoint of moderate inversion. Figure 4.6 shows a plot of the low frequency gain vs the inversion coefficient for a standard 0.5  $\mu\text{m}$  process.

Minimum input is determined when the voltage at the gate of M1 starts to approach the lower rail voltage which causes the transistor to turn off and the minimum is found by looking at when  $M_5$  goes into triode (assuming above threshold behavior)

$$V_{DS5} \geq V_{GS5} - V_{th5} \quad (4.15)$$

$$V_{I_{min}} \geq V_{GS1} + V_{GS5} + V_{SS} - V_{th5} \quad (4.16)$$

$$\sqrt{\frac{I_B}{\beta_1}} + V_{th1} + \sqrt{\frac{2I_B}{\beta_5}} + V_{ss} \quad (4.17)$$

Maximum input is found as the input approached the top rail and  $M_2$  goes into triode  $\Rightarrow V_{DS1} = V_{GS1} - V_{THN}$ ,

$$V_{G1} = V_{I_{max}} = V_{D1} + V_{th1} \quad (4.18)$$

$$= V_{DD} - V_{DS3} + V_{th1} = V_{DD} - V_{GS3} + V_{th1} \quad (4.19)$$

$$= V_{DD} - \sqrt{\frac{I_b}{\mu C_{ox} W/L}} - V_{the3} + V_{th1} \quad (4.20)$$

The common mode gain and the common mode rejection ratio is:

$$V_C = V_{gs1,2} + 2i_d r_{o5} = i_d \left( \frac{1}{g_{m1}} + 2r_{o5} \right) \approx i_d 2r_{o5} \quad (4.21)$$

$$V_{out} = \frac{-i_d}{g_{m3}} = \frac{-i_d}{g_{m3}} \quad (4.22)$$

$$A_c = \frac{V_{out}}{V_c} = \frac{1}{2g_{m4}r_{o5}} = \frac{1}{\frac{4\kappa(1-e^{-\sqrt{IC}})}{U_T\sqrt{IC}} V_A} \quad (4.23)$$

$$CMRR = \left| \frac{A_v}{A_c} \right| \quad (4.24)$$

The slew rate is  $I/C_L$ , where  $C_L$  is the load capacitance assumed to be in the range of 0.2-10 pF. The value of the load capacitance is based on typical values for the ceramic package within which the die is contained.

## 4.2 Tradeoffs in a Simple OTA

For a standard 0.5  $\mu m$  process figures 4.1 through 4.11 show plots of the various amplifier characteristics verses the design parameters of inversion coefficient and transistor length. Transistor width is assumed to be fixed (at 100 times  $\lambda=0.35 \mu m$ ) and changes due to bias current is assumed to track changes due to the inversion level. This is a standard approach based on reference [53] as the width can be determined from the desired inversion level operation which is intrinsically linked to the system power level and therefore the bit energy. The inversion level was swept from 0.001 to 100 and the length was swept from  $2\lambda$  to  $25\lambda$ , where  $2\lambda$  is the minimum transistor length in this process.

The input referred noise is plotted assuming there is only noise from the differential pair and the transfer function is assumed to be ideal for the sake of simplicity. The trends observed with the model should be similar to that observed with full small signal models (see the following section). Recall that noise increases with  $I_{bias}$  and decreases with area. So it generally increases with the inversion coefficient (figure 4.1). Figure 4.2 shows the change of the input referred noise for varying length. The transconductance, noise corner frequency, 3dB frequency and bit energy all increase with inversion level (figures 4.3, 4.4, 4.5 and 4.10). The gain and thermal

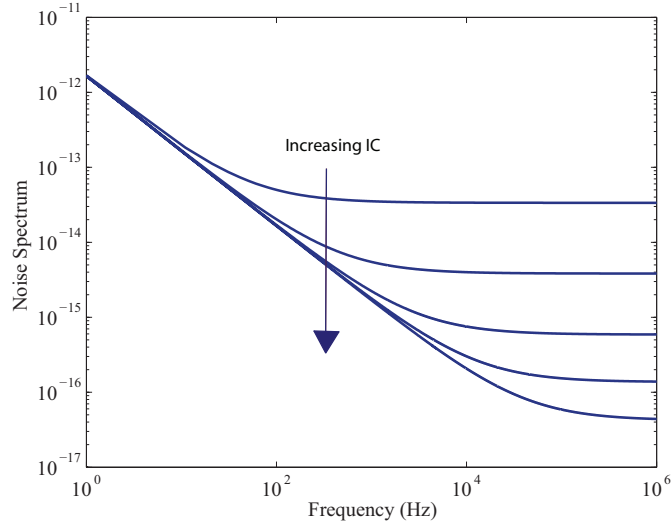


Figure 4.1: Input Referred Noise ( $S_{in}(f)$ ) for different inversion coefficients.

noise level decreases with increasing inversion level (figures 4.6, 4.8). The common mode gain increases for different inversion coefficients (figure 4.7). The information rate on the other hand shows an increase followed by a decrease, albeit within a relatively small range (less than an order of magnitude, figure 4.9). However for lower signal powers the spread between the information rates at different inversion levels may be more pronounced. Figure 4.11 shows the information rate and bit energy increasing with inversion level for different lengths. The trends are expected to remain the same for different topologies.

### 4.3 Model Accuracy

In the previous chapter we used a very simplified model which modeled only the noise of the input transistors to enable hand calculations in order to predict the experimental results. We were however predicting only trends and not the absolute

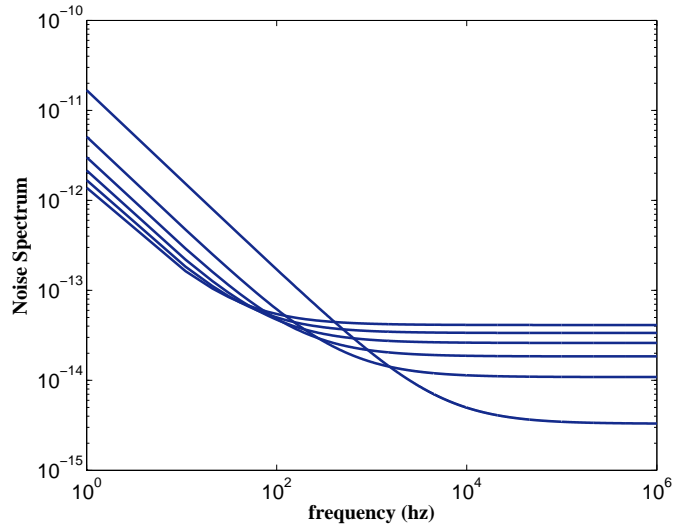


Figure 4.2: Input Referred Noise (Sin(f)) for different transistor lengths.

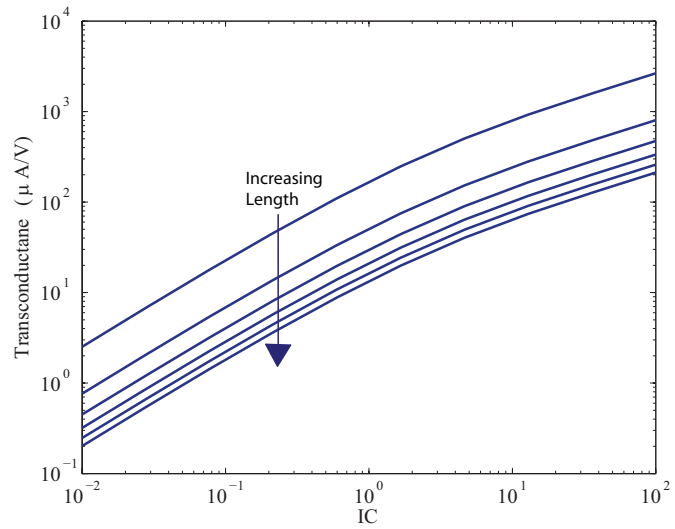


Figure 4.3: Transconductance for different inversion coefficients

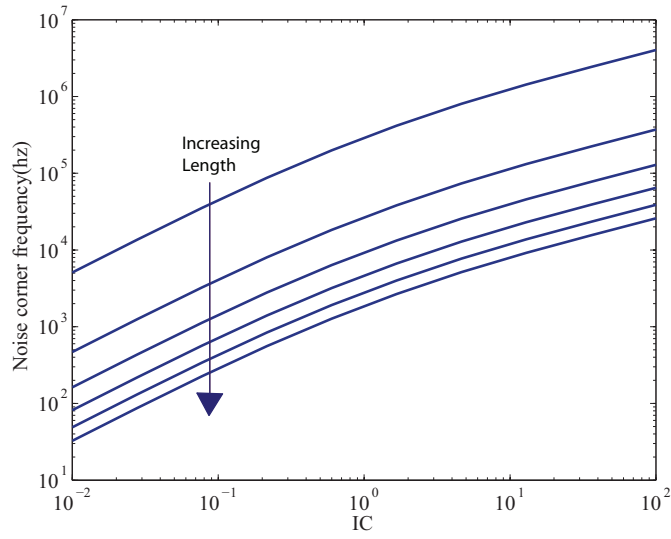


Figure 4.4: Noise corner frequency for different inversion coefficients

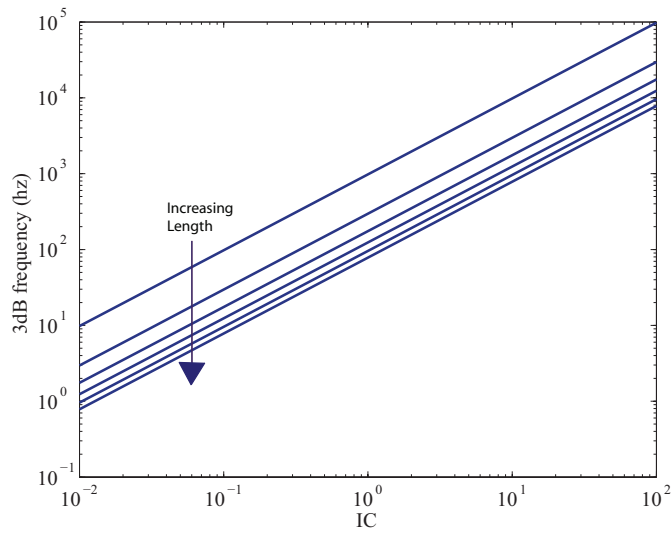


Figure 4.5: 3dB frequency for different inversion coefficients

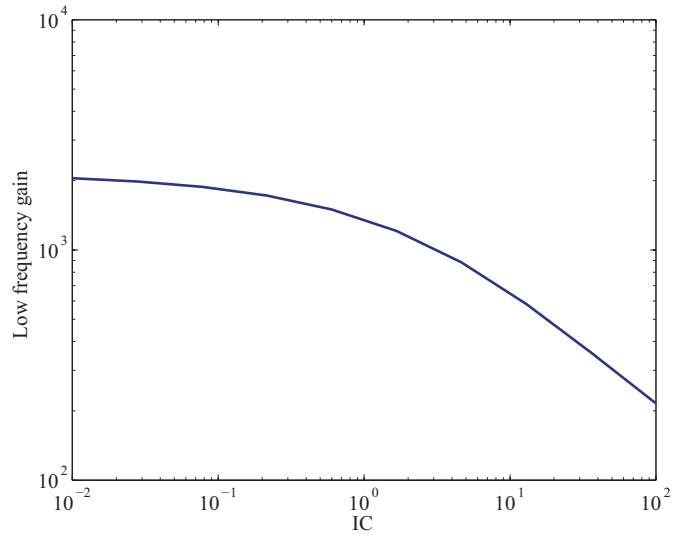


Figure 4.6: Low frequency gain for different inversion coefficients

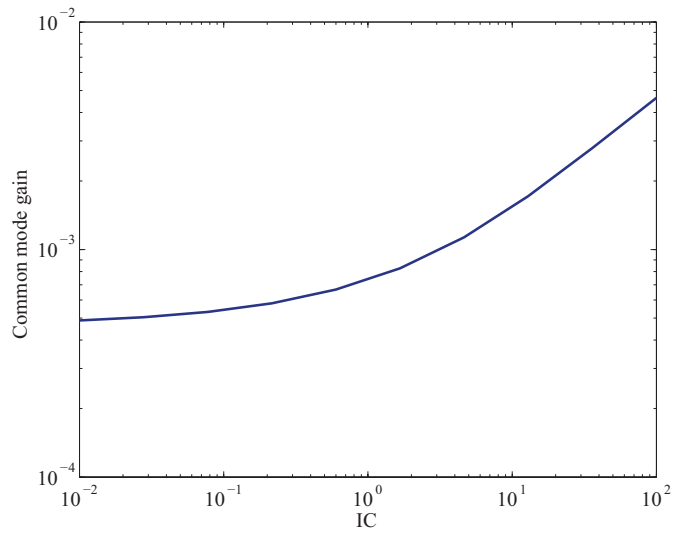


Figure 4.7: Common mode gain for different inversion coefficients

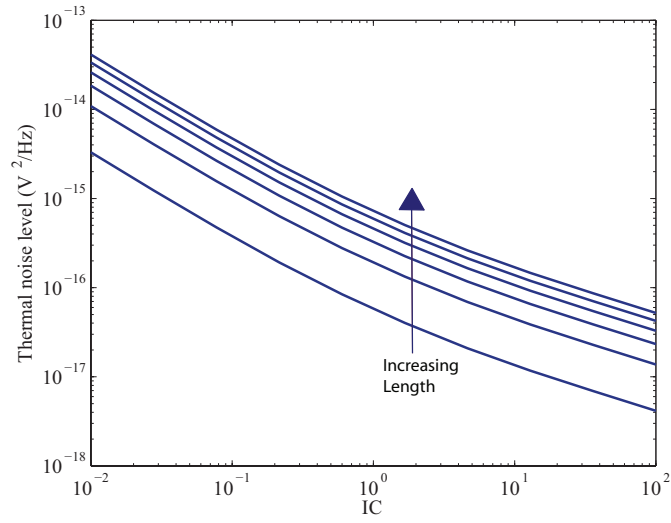


Figure 4.8: Thermal noise level for different inversion coefficients

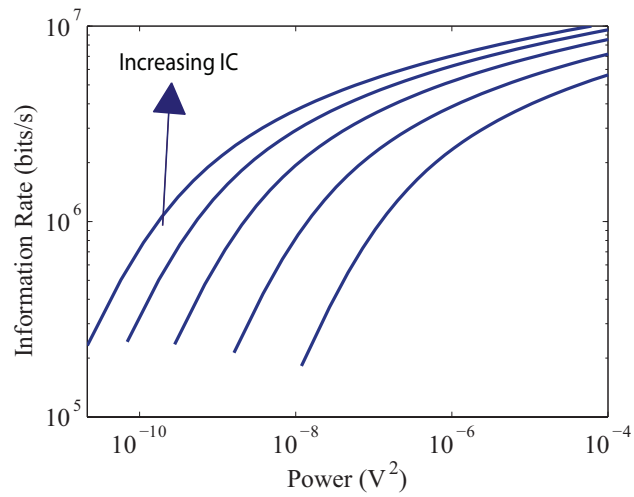


Figure 4.9: Information rate for different inversion coefficients.



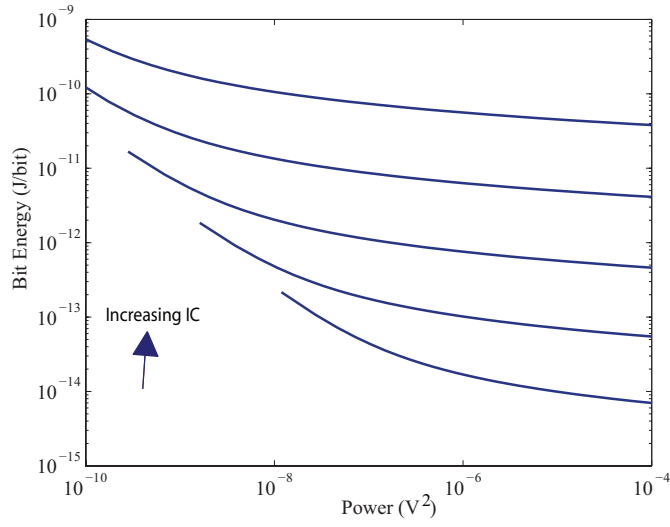
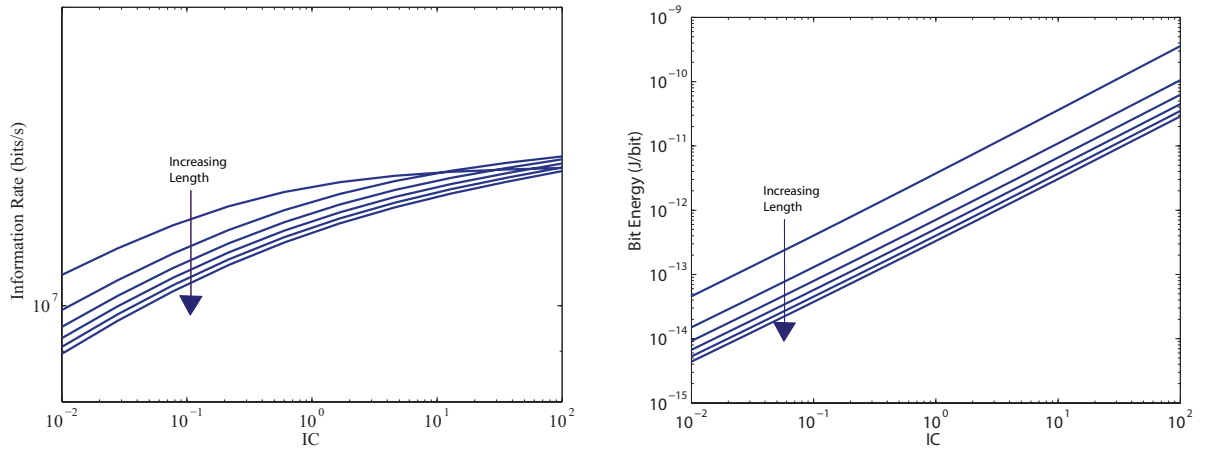


Figure 4.10: Bit Energy for different inversion coefficients.



(a) Information rate vs IC

(b) Bit energy vs IC

Figure 4.11: Information rate and bit energy vs IC for a power level of  $10^{-4}$ .

value of the information rate. In this section the noise, information rate is computed for the simple OTA as an example circuit and is compared to the experimentally measured noise and subsequent derived information rate and bit energy.

The simple model is easier for hand calculations purposes. Clearly the next research question is how accurate is the simple model, that is how far off is it from that predicted by a more complete model? How accurate of a model do we really need? That is, does the noise of all the transistors need to be considered, can low frequency transfer function model be considered only, do the gate source capacitances need to be included or do both gate source and the gate drain capacitance need to be included.

Intuitively if we want to accurately predict the information rate better models are necessary. To evaluate this we again look at a simple OTA. We assume  $g_{m1} = g_{m2}$  and  $g_{m3} = g_{m4}$ . In the low frequency model the input referred noise is [18]

$$\begin{aligned}
 v_{eq}^2 &= v_{n1}^2 + v_{n2}^2 + \left(\frac{g_{m3}}{g_{m1}}\right)^2 (v_{n3}^2 + v_{n4}^2) \\
 &= \frac{i_{n1}^2}{g_{m1}^2} + \frac{i_{n2}^2}{g_{m1}^2} + \left(\frac{g_{m3}}{g_{m1}}\right)^2 \left(\frac{i_{n3}^2}{g_{m3}^2} + \frac{i_{n4}^2}{g_{m3}^2}\right) \\
 &= \frac{i_{n1}^2 + i_{n2}^2 + i_{n3}^2 + i_{n4}^2}{g_{m1}^2} \tag{4.25}
 \end{aligned}$$

The important parasitic capacitances are shown in figure 4.3. These capacitances have effects at higher frequencies and are present between the gate-source and gate-drain terminals. There are additional parasitics associated with the substrate terminal which are ignored in this analysis. Assume that the gate-source and gate-drain capacitances of the PMOS pair and NMOS pair are the same. Further

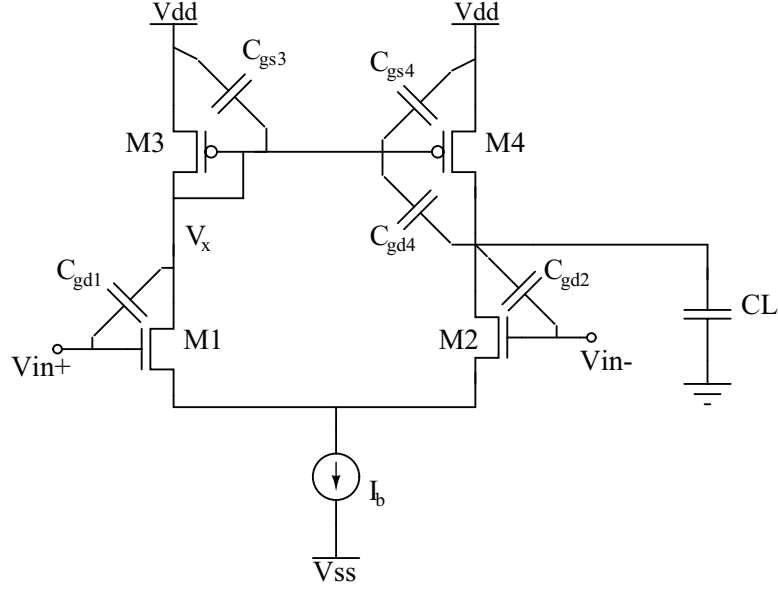


Figure 4.12: Simple OTA showing the parasitic capacitances

assume that the sources of M1 and M2 are at AC ground and that M5 does not contribute to the total noise. This allows the transfer function to be written as:

$$\begin{aligned}
 H(f) &= \frac{-1/2 (sC_{gd1} - g_{m1}) (sC_{gd1} + sC_1 + 1/R_1 + g_{m4})}{(sC_{out} + 1/R_{out}) (sC_{gd1} + 1/R_1 + sC_1 + sC_{gd4}) - sC_{gd4} (sC_{gd4} - g_{m4})} \\
 \frac{V_x}{V_{in}} &= \frac{1/2 (sC_{gd1} - g_{m1}) (sC_{gd4} + sC_{out} + 1/R_{out})}{sC_{gd4} (sC_{gd4} - g_{m4}) - (sC_{out} + 1/R_{out}) (sC_{gd1} + 1/R_1 + sC_1 + sC_{gd4})}
 \end{aligned}$$

where

$$\begin{aligned}
 C_1 &= C_{gs3} + C_{gs4} \\
 C_{out} &= C_L + C_{gd2} + C_{gd4} \\
 R_1 &= r_{o1} || r_{o3} || 1/g_{m3} \\
 R_{out} &= r_{o2} || r_{o4}
 \end{aligned} \tag{4.26}$$

If the parasitic gate drain capacitance of transistor M4 is assumed to be small

(which is usually the case in practice) the transfer functions may then be simplified as

$$\begin{aligned}
 H(f) &= -R_1 \left( \frac{1}{R_1} + g_{m4} \right) \frac{g_{m1} R_{out}}{2} \frac{\left( \frac{sC_{gd2}}{g_{m1}} - 1 \right) \left( 1 + \frac{s(C_1 + C_{gd1})}{1/R_1 + g_{m4}} \right)}{(1 + s(C_L + C_{gd2})R_o) (1 + s(C_1 + C_{gd1})R_1)} \\
 \frac{V_x}{V_{in}} &\approx \frac{1/2g_{m1}}{s(C_1 + C_{gd2}) + 1/R_1} \tag{4.27}
 \end{aligned}$$

The poles and zeroes of the transfer function, assuming the output resistance is much smaller than the transconductance are:

$$\begin{aligned}
 z_1 &= \frac{g_{m1}}{C_{gd2}} \approx 10^9 \\
 z_2 &= \frac{2g_{m4}}{C_1 + C_{gd1}} \approx 10^9 \\
 p_1 &= \frac{1}{R_o (C_L + C_{gd2})} \approx 10^5 \\
 p_2 &= \frac{g_{m4}}{C_1 + C_{gd1}} \approx 5 \times 10^8 \tag{4.28}
 \end{aligned}$$

The approximate locations of the poles and zeroes are given assuming aspect ratios quoted in the previous chapter. It will be noticed that other than the dominant pole the others are much further out in frequency. Therefore if we are only considering biological applications such as described in Chapter 1, it is clearly not a problem if the other parasitic poles and zeroes are ignored for design purposes. It also validates the use of the simple model in previous chapters.

The noise current can be reflected back to the gate as a noise voltage source, given that  $i = g_m v_{gs}$ , the noise voltage is usually represented as  $i_n^2/g_m^2$ . However if the gate drain capacitance is not ignored this can instead be written as  $i_n^2/(g_m + sC_{gd})^2$ . The complete expression for the input referred noise can be found using

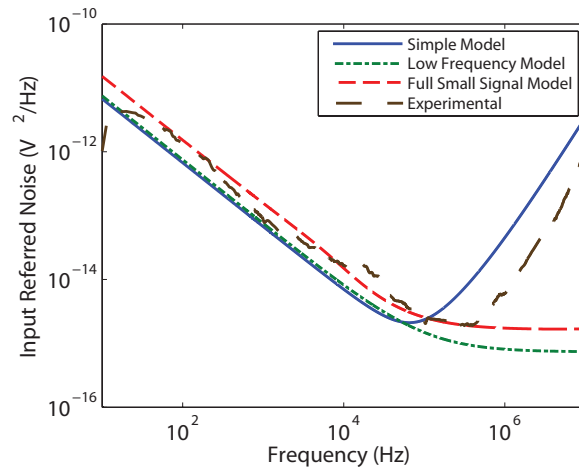
equation (4.26). That is, it is found by taking the current noise and transforming it to the voltage noise at the output node, and then dividing by the transfer function from the input to the noise voltage source.

The parasitic caps due to the substrate terminal are ignored. The effect of transistor M5 is also ignored as this can be considered to be common mode noise which would be negligible. Figure 4.13 shows the calculated noise and experimental noise along with the derived information rate.

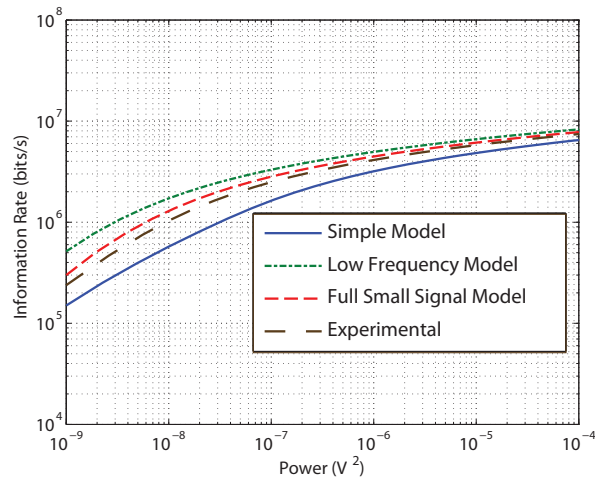
From figure 4.13 a number of things should be noticed, firstly all models are an overestimate on the experimental information rate. Secondly all the models give the same order of magnitude error. This means that the simple model is adequate for predictions.

#### 4.4 Fitting Information Rate and Bit Energy into Current Design Methodologies

If the inversion level, length and bias current are known then the width of the transistor is inherently known. The inversion level scales linearly with the bias current and gate length. In a design not only is the aspect ratio  $W/L$  important but also the area  $W \times L$ . It is therefore wise to be cognizant of the way both factors change with the inversion level. A typical design methodology based on  $g_m/I_d$  characteristic would start off by exploring the changes in amplifier characteristics with changing inversion coefficient, keeping other variables fixed [53]. Then the effect of transistor length and finally drain current on characteristics would be separately



(a) Input Referred Noise



(b) Information Rate

Figure 4.13: Input referred noise and information rate for the simple OTA

explored where the variation with bias current should track the variation with inversion coefficient since IC and  $I_d$  are linearly related. We add information rate and bit energy to the normally considered amplifier characteristics.

Looking at figures 4.11 both information rate and bit energy increase with increasing inversion coefficient (and therefore increasing bias current). This implies the optimum information rate for the amplifier is at higher inversion levels (and bias current) while the optimum bit energy is at low inversion levels (and bias current). This variation was explored assuming all the noise comes from the input differential pair and is summarized in Table 4.1.

It should be noted that in the plot for low frequency gain vs inversion coefficient there is no length variance because for this simple hand calculation the channel length modulation parameter ( $\lambda = 1/V_A$ ) is taken to be a constant. In reality this parameter has a  $1/L$  dependence. If this factor is taken into account the low frequency gain increases with increasing length.

#### 4.5 Information Rate assuming White Noise Only

A more detailed look may be taken if flicker noise is ignored so that only white noise shaped by a simple low pass filter exists. Then the input referred noise is of the form,

$$S(f) = \frac{S_o}{A_o} \left( 1 + \frac{f^2}{f_c^2} \right)$$

where the parameters are the same as that described in Chapter 3. We can write

Table 4.1: Summary of Trends with Design Parameters

Parameter	IC ↑	L ↑
$A_o$	↓	↑
$f_k$	↑	↓
$S_o$	↓	↑
$A_c$	↑	↓
$f_{3dB}$	↑	↓
$g_m$	↑	↓
Bit Energy	↑	↓
Information Rate	↑	↓

the power in terms of the bandwidth using the following:

$$P = \int_0^{f_2} \nu - \frac{S_o}{A_o} \left( 1 + \frac{f^2}{f_c^2} \right) df$$

$$\nu = \frac{S_o}{A_o} \left( 1 + \frac{f_2^2}{f_c^2} \right)$$

where  $f_2$  is the upper frequency limit defined by the waterfilling. Putting the above two equations together we get:

$$P = \nu f_2 - \int_0^{f_2} \frac{S_o}{A_o} \left( 1 + \frac{f^2}{f_c^2} \right) df$$

$$= \frac{S_o}{A_o} \left( 1 + \frac{f_2^2}{f_c^2} \right) f_2 - \frac{S_o}{A_o} \left( f_2 + \frac{f_2^3}{3f_c^2} \right)$$

$$= \frac{2 S_o f_2^3}{3 A_o^2 f_c^2}$$

So that the power level is strongly dependent on the bandwidth ( $f_2$ ) and inversely



proportional to the square of the 3dB bandwidth. We can now write the information rate as

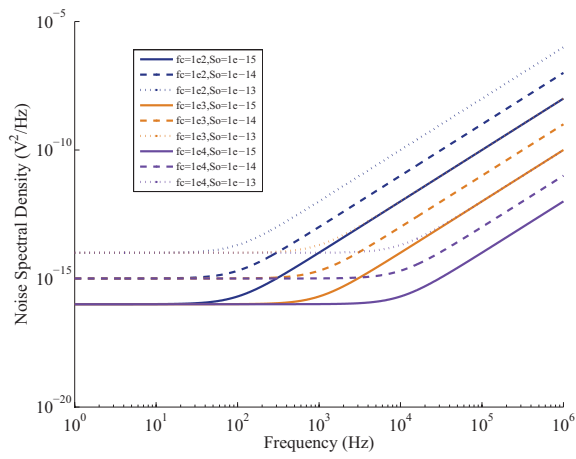
$$\begin{aligned}
 I &= \frac{1}{2} \frac{1}{\ln 2} \int_0^{f_2} \frac{\nu}{N(f)} df \\
 &= \frac{1}{2 \ln 2} \int_0^{f_2} \left( \ln \left( 1 + \frac{f_2^2}{f_c^2} \right) - \ln \left( 1 + \frac{f^2}{f_c^2} \right) \right) df \\
 &= \frac{1}{2 \ln 2} \left( 2f_2 - 2f_c \tan^{-1} \frac{f_2}{f_c} \right)
 \end{aligned}$$

Note that the information rate depends directly on the signal bandwidth and the 3dB cutoff frequency, but not on the thermal noise or low frequency gain. Using the above we can write the signal to noise ratio (SNR) as:

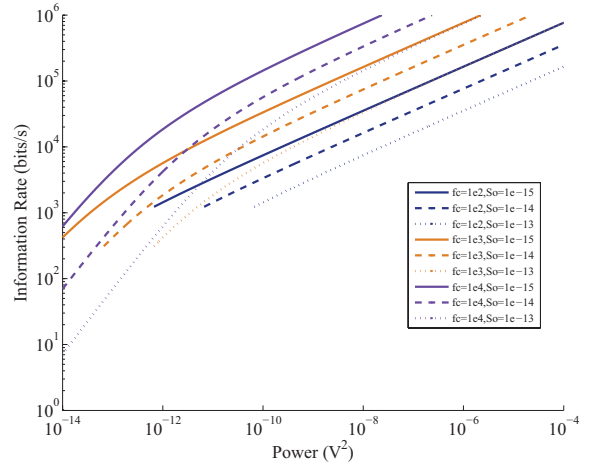
$$SNR = \frac{P}{N(f)} = \frac{\frac{2}{3} \frac{f_2^3}{f_c^2}}{\left( 1 + \frac{f_2^2}{f_c^2} \right)}$$

Figure 4.14 shows plots of the noise spectral density for different 3dB bandwidths and noise levels. The information rate is a function of three parameters which depend on each other and in some cases lower or higher signal to noise ratio do not mean lower or higher information rate (figures 4.14 (b), (c) and (d)). It is therefore important for any circuit under consideration to consider all of these parameters in detail.

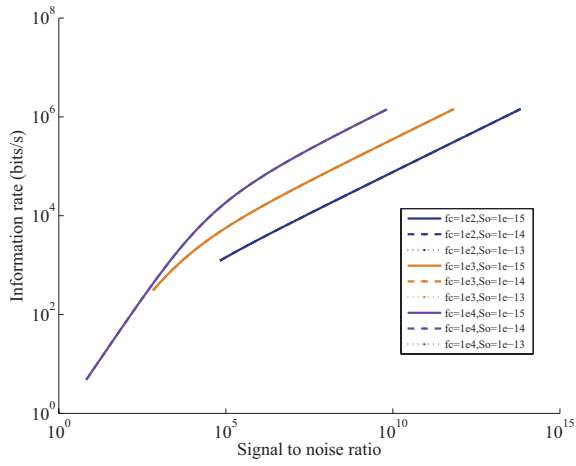
It can be asked for what values of system power is the bit energy,  $P_{sys}/C$ , optimum and is there an optimum fraction of noise power. If it is assumed that the sensor only has white noise for simplicity, then the bit energy can be written as,



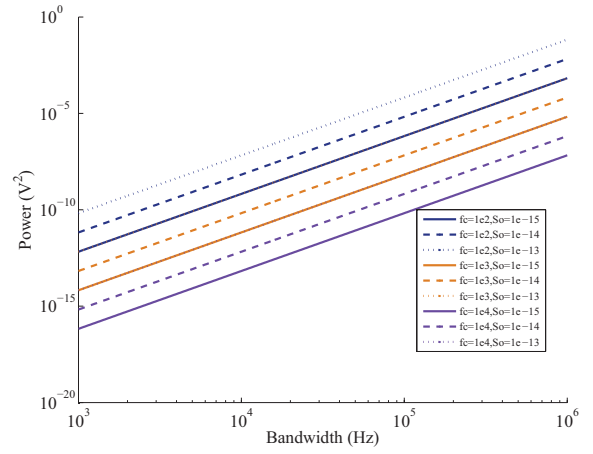
(a) Noise Spectral Density



(b) Information rate vs Power



(c) Information rate vs SNR at 0 frequency



(d) Signal power vs bandwidth

Figure 4.14: Theoretical results for information rate with white noise only with low pass filter.

$$\begin{aligned}
BE &= \frac{I_b(V_{dd} - V_{ss})}{\frac{1}{2 \ln 2} \left( 2f_2 - 2f_c \tan^{-1} \frac{f_2}{f_c} \right)} \\
&= \frac{I_b(V_{dd} - V_{ss})}{\frac{1}{2 \ln 2} \left( 2f_2 - \frac{\lambda I_b}{\pi C_{out}} \tan^{-1} \frac{2\pi C_{out} f_2}{\lambda I_b} \right)}
\end{aligned}$$

where  $C_{out}$  is the output capacitance dominated mostly by the load capacitance and  $\lambda$  in this case is the channel length modulation parameter and is related to the early voltage ( $V_A$ ).  $I_b$  is the bias current of the tail transistor. From this it is seen that the bit energy will increase linearly with the power supply rails, however its relationship with the bias current is more complex. Figure 4.15 shows the information rate and 3dB frequency vs the total system power for the same input signal power level. The power supply rail is kept constant for this plot. This plot demonstrates that for higher system powers the information rate decreases but is mostly due to the bias current changing. It is interesting to note that the information rate does not change for low system powers. It should be noted as well that in the expression for information rate the thermal noise level and the low frequency gain are absent. Those terms only appear in the expression that relates the signal noise power to the bandwidth. If the flicker noise is now taken into account, at low signal powers the bit energy will not remain flat as it does in the white noise case, simply because the expressions become considerably more complicated.

## 4.6 Chapter Summary

In this chapter the information rate and bit energy was incorporated into a design methodology based on [53, 54]. Using information rate and bit energy as

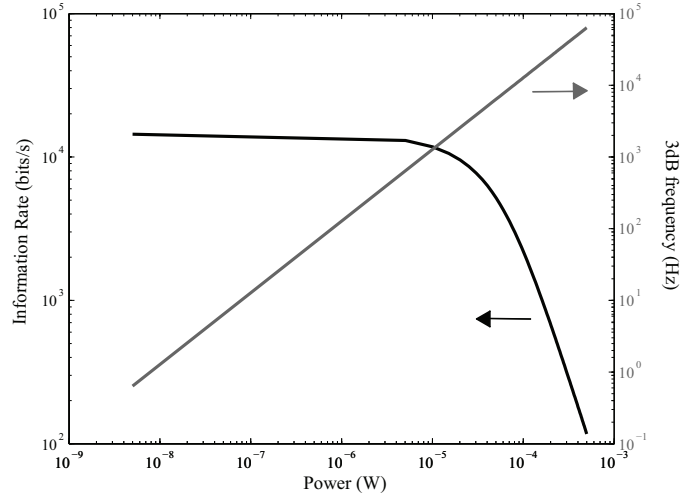


Figure 4.15: Theoretical results for information rate and 3dB frequency vs System Power with white noise only with low pass filter.

one of the design specifications the design space for the simple OTA was explored. This methodology can be repeated with any configuration. Ideally the results of the previous chapter and this one should be combined as a designer typically has to decide on both a *type* of configuration as well as the other design parameters. Work in this chapter related to accuracy of the model was also published in reference [55].

## Chapter 5

### Achieving Increased Information Rate

Figure 5.1 shows the input referred noise of two OTAs, a wide range and a simple OTA. In performing waterfilling notice that the bandwidths of the amplifiers are different, but also notice that the signal power is placed at *higher* frequencies where the noise is lowest. However, as alluded to before, this noise minimum can actually occur *above* the dominant pole of the amplifier, and if this occurs the input signal will in all likelihood be attenuated (Figure 5.2). While the amplifier may have the optimum signal to noise ratio (from optimizing the information rate) the amplifier is not performing as designed, it is not amplifying the signal and would thus be useless for the intended real world application.

The signals that are most interesting in biosensing and certain other applications tend to be relatively low frequency signals that occur where the noise is highest (for example a neural amplifier). Waterfilling implicitly requires that the input signal be moved to regions where the noise is lowest. Therefore any technique which moves the input signal from lower to higher frequencies should approximate the waterfilling algorithm and achieve increased information rate.

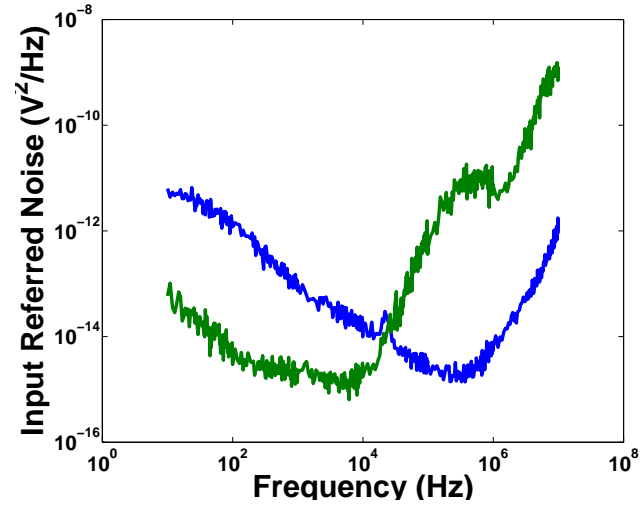


Figure 5.1: Input referred noise for two different OTAs

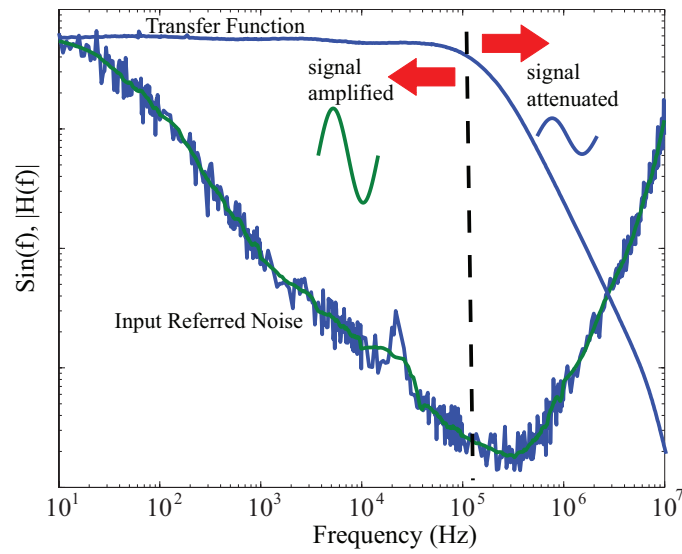


Figure 5.2: Input referred noise ( $Sin(f)$ ) and transfer function ( $H(f)$ ): placing signal at noise minimum may result in signal attenuation.

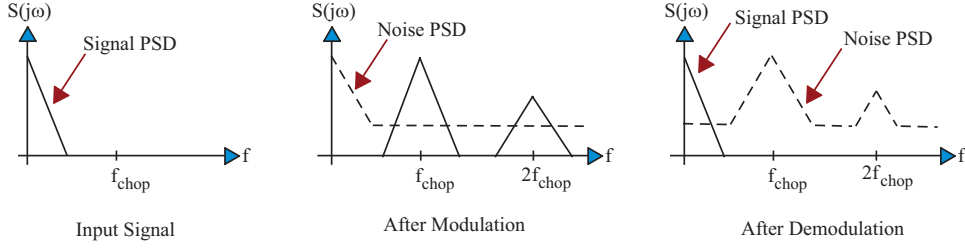


Figure 5.3: Basic principle of chopper modulation: the input signal is moved to higher frequencies where the noise is lower.

## 5.1 Standard Chopper Modulation

The chopper modulation technique is a technique which should approximate the waterfilling algorithm. The technique has been around for decades and was first introduced back in the era of vacuum tubes and was accomplished using mechanical choppers [56, 57]. The technique shifts the input signal to a higher frequency, amplifies it and then demodulates it back to the baseband. The overall effect at the output of the system is to shape the noise of the amplifier. The system performs a modulation operation and not a sampling operation. The principle of chopper modulation is outlined in figures 5.3 and 5.4 (a). From this system overview the output voltage is given by [56, 57]

$$V_{out} = (V_{in}Am(t) + v_n)m(t) \quad (5.1)$$

where  $m(t)$  is the modulating signal alternating between 1 and -1 with chopping frequency  $f_{chop}$ .  $v_n$  and  $A$  are the noise and gain of the amplifier respectively. The gain is a complex function of frequency that depends on the usual parameters of transconductance, output resistance, parasitic capacitances and load capacitances.

The noise is taken to be both flicker and thermal noise in accordance with the assumptions in Chapter 2. Figure 5.4 (b) shows an overview of the architecture required to implement chopper modulation. Modulation is easily accomplished using cross coupled MOS switches where the usual considerations for switching apply. Clearly the input signal is multiplied by  $(\pm 1)^2$  leaving it amplified but unchanged in the frequency spectrum at the output of the system. The equation for the voltage at the second modulator can therefore be simplified to

$$V_{out} = V_{in}A + v_n m(t) \quad (5.2)$$

As the modulating signal is a simple square wave, the Fourier representation of  $m(t)$  can be easily written as,

$$m(t) = \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{2}{jn\pi} e^{jn f_{chop} t} \quad (5.3)$$

The quantity of interest is the input referred noise. This is measured before the first modulator, as the system under consideration includes both the modulator and demodulator. The power spectral density of the input referred noise of the system can therefore be expressed as

$$S_{n_{in}} = \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \frac{S_{n_{out}}(|f - n f_{chop}|)}{|A(f - n f_{chop})|^2} \quad (5.4)$$

where  $S_{n_{out}}$  is the output noise spectral density of the amplifier only. Similar to Chapter 3, the simplified output noise of any amplifier can be written as consisting of two components. These two components are a white noise source and a flicker noise source of the form

$$S_{n_{out}}(f) = S_0 \left(1 + \frac{f_k}{f}\right) \quad (5.5)$$



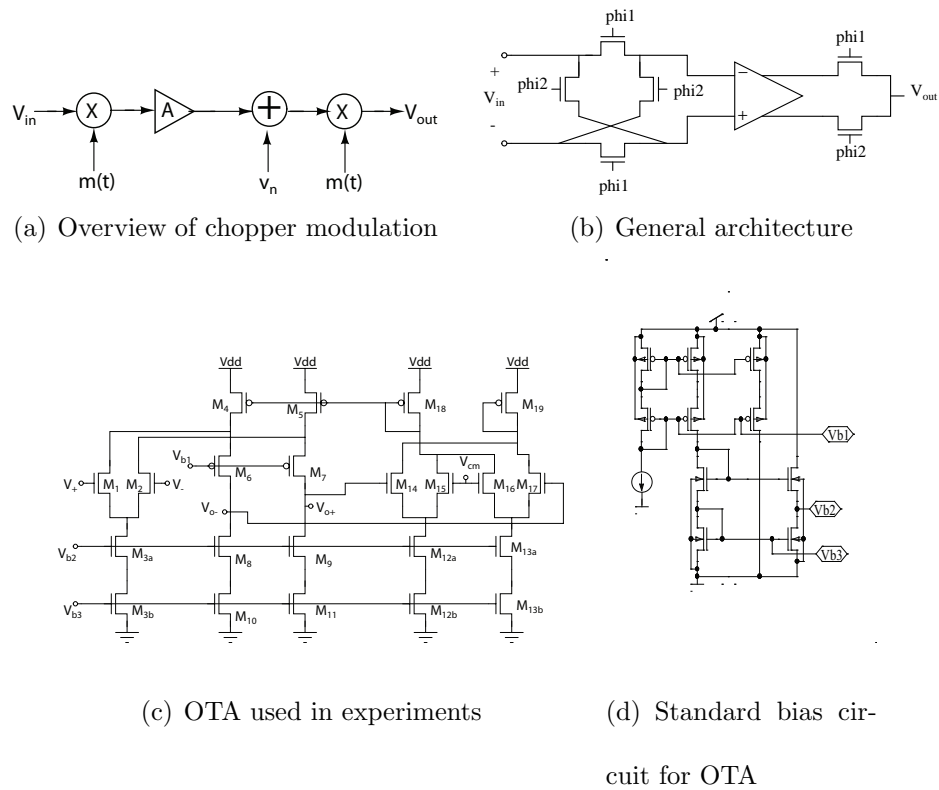


Figure 5.4: Chopper amplifier: (a) modulating  $v_{in}$  with a square wave moves the signal up to higher frequencies after signal is amplified both the amplifier noise  $v_n$  and the amplified signal are again modulated (b) modulation is easily accomplished by cross coupled switches at the input and a pair of switches at the output (c) fully differential folded cascode was chosen as the OTA for experimental measurements (d) bias circuit used for the OTA.

where  $f_k$  is the noise corner frequency and  $S_0$  is the thermal noise level. Again this form for the noise is motivated by the experimental noise measurements obtained throughout the course of this work. It is again further assumed that the gain of the amplifier can be modeled as a first order low pass transfer function as shown below:

$$A = \frac{A_0}{\sqrt{1 + \left(\frac{f}{f_c}\right)^2}} \quad (5.6)$$

where  $f_c$  is the 3dB corner frequency or bandwidth of the amplifier.  $A_0$  is the low frequency gain. Clearly this form of the transfer function takes into account only the dominant pole of the amplifier. An approximation for equation (5.4) can be obtained assuming the 3dB corner frequency is much greater than the chopping frequency ( $f_c \gg f_{chop}$ ). This implies that at relatively low frequencies below the 3dB bandwidth only  $A_0$  is necessary to obtain a valid circuit noise representation. Equation (5.4) can then be written as:

$$S_{n_{in}} = \frac{S_0}{A_0^2} \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} \left(1 + \frac{f_k}{|f - n f_{chop}|}\right) \quad (5.7)$$

It can be assumed that higher order terms in the taylor series for  $1/f$  are negligible (this is borne out by quick calculations). The input referred noise is then:

$$S_{n_{in}} = 2 \frac{S_0}{A_0^2} \left(\frac{2}{\pi}\right)^2 \sum_{\substack{n=1 \\ n=odd}}^{\infty} \frac{1}{n^2} \left(1 + \frac{f_k}{n f_{chop}}\right) \quad (5.8)$$

which at lower frequencies simplifies to

$$\begin{aligned} S_{n_{in}} &= 2 \frac{S_0}{A_0^2} \left(\frac{2}{\pi}\right)^2 \left(\frac{\pi^2}{8} + \frac{f_k}{f_{chop}} \frac{7}{8} \zeta(3)\right) \\ &= \frac{S_0}{A_0^2} \left(1 + 0.8526 \frac{f_k}{f_{chop}}\right) \end{aligned} \quad (5.9)$$

with  $\zeta(x)$  being the Riemann zeta function. This result is valid for frequencies that are less than twice the chopping frequencies. Note that the input signal frequency must be less than half the chopping frequency to avoid aliasing effects. In general, assuming the input signal is restricted to below the 3dB frequency,  $f_c$ , the gain is entirely given by the low frequency gain ( $A_0$ ). The input referred noise of the chopper amplifier can be then be approximated by taking the first term ( $n = 1$ ) in flicker noise portion of the series of equation (5.7).

$$S_{n_{in}} = \frac{S_0}{A_0^2} \left[ 1 + \frac{8}{\pi^2} \frac{f_k}{f_{chop} - f} \right] \quad (5.10)$$

Calculations shows that this is an underestimation of the input referred noise. It can however be useful for hand calculations. Note that this level depends only on the chopping frequency, noise corner frequency, thermal noise level and the AC gain. In general the input referred noise is given by a more complex form

$$S_{n_{in}} = S_0 \left( \frac{2}{\pi} \right)^2 \sum_{\substack{n=-\infty \\ n=odd}}^{\infty} \frac{1}{n^2} + \frac{\alpha}{n^3} + \beta + \frac{\lambda}{n} \quad (5.11)$$

At low frequencies the noise for the chopper amplifier is approximately white. However it starts to increase as the chopping frequency is approached. At the chopping frequency and odd harmonics the noise is infinite since  $1/f$  is transformed to  $1/(f - f_{chop})$ . The flicker noise is thus replicated at odd harmonics of the chopping frequency for square wave modulation. If modulation is implemented with just the fundamental sine wave, there would be no harmonics present. This is however a slightly more complicated circuit to implement. This circuit would also have strict design constraints to guarantee consistent and proper operation.

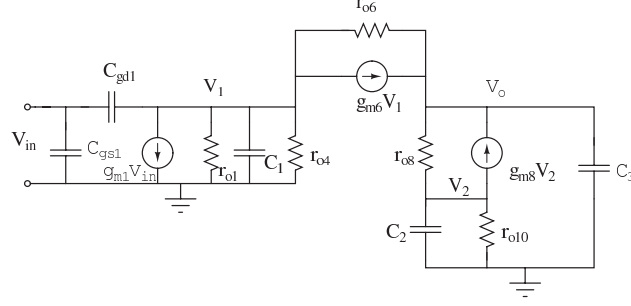


Figure 5.5: Simplified small signal model for the fully differential folded cascode [58].

The fully differential folded cascode amplifier within the chopper amplifier was implemented with the following transistor aspect ratios: all NMOS, 15/5; The PMOS transistors  $M_6$  and  $M_7$ : 70/5; and  $M_4$  and  $M_5$ : 105/5. Where again the width and length dimensions are given for a lambda based design, with  $\lambda = 0.3 \mu m$ . Figure 5.17 shows a photomicrograph of the implemented amplifier. The photomicrograph shows the OTA as well as the poly1-poly2 capacitors used to set the gain of the amplifier for the chosen application. The OTA is  $54.6 \mu m \times 80.4 \mu m$  and the power consumption is  $60 \mu W$ . For differential signals the small signal circuit model for this amplifier can be simplified to the form shown in figure 5.5 where the capacitors  $C_1$ ,  $C_2$  and  $C_3$  represent several parasitic capacitances within the circuit,

$$C_1 = C_{gd4} + C_{gs6} \quad (5.12)$$

$$C_2 = C_{gd10} + C_{gs8} \quad (5.13)$$

$$C_3 = C_{gd8} + C_{gd6} + C_{gs14} + C_{gs18} + C_L \quad (5.14)$$

Using nodal equations based on figure 5.5 the transfer function was determined. The

low frequency gain is given by  $g_{m1}R_o$  where  $R_o$  is the equivalent resistance looking into the drains of  $M_6$  and  $M_8$ .  $g_{m1}$  is the transconductance of the input differential pair [58]. The full transfer function contains higher poles as well as zeroes and has the general form:

$$\frac{V_{out}}{V_{in}} = A_o \frac{\left(1 - \frac{s}{z_1}\right) \left(1 - \frac{s}{z_2}\right)}{\left(1 - \frac{s}{p_1}\right) \left(1 - \frac{s}{p_2}\right) \left(1 - \frac{s}{p_3}\right)} \quad (5.15)$$

with the dominant pole given by  $1/R_oC_3$ . The first zero  $z_1$  is given by  $g_{m1}/C_{gd1}$ , the second zero  $z_2$  can be approximated as  $g_{m8}/C_2$ . The higher poles are approximated as  $g_{m8}/C_2$  and  $g_{m6}/C_1$  [58]. For the sizes and process utilized the higher poles and zeroes are much further out in frequency than the dominant pole, and can be ignored for simple calculations.

Figure 5.6 shows the theoretical and experimental input referred noise of a chopper modulated and unmodulated folded cascode amplifier. It can be seen that as the chopping frequency increases the low frequency noise decreases. The experimental input referred noise still shows some residual low frequency noise and is not completely flat as predicted by the ideal. The modulator/demodulator switches are implemented with dummy switches and transmission gates to minimize charge injection and clock feedthrough. However both of these phenomena, charge injection and clock feedthrough, still exist. The residual low frequency noise is therefore due to the noise of the modulators which are not taken into account in the theory and also due to charge injection and clock feedthrough of the first set of modulators.

Modulation introduces aliasing at signals above the chopping frequency and as seen from equation (5.11) the input referred noise does not converge in this region,

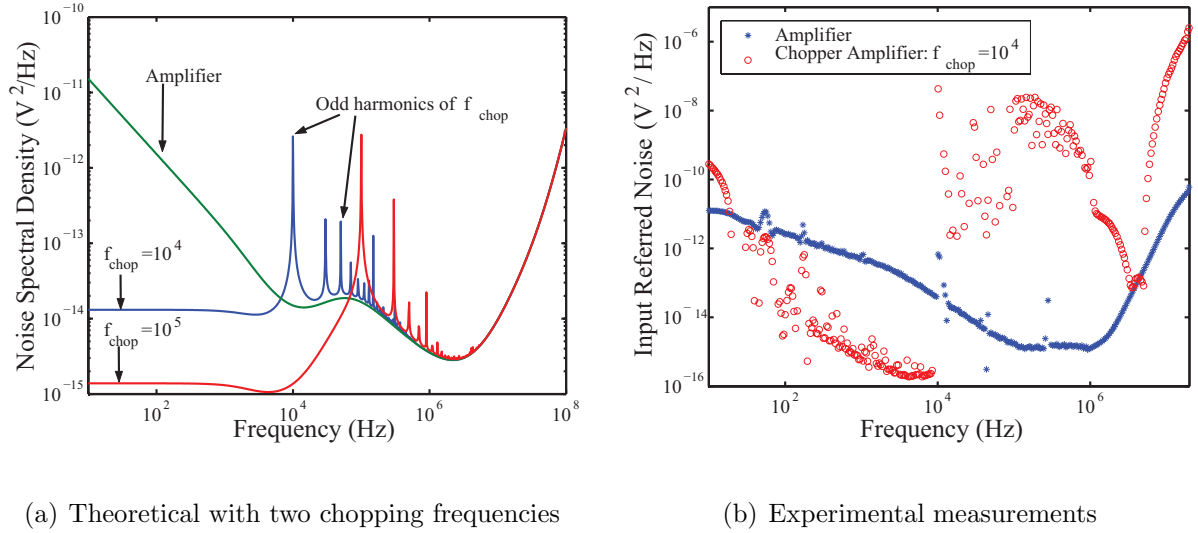


Figure 5.6: Input referred noise of OTA and chopper modulated OTA (a) theoretical and (b) experimental [58].

thus the bandwidth above the chopping frequency is unsuitable for signal transmission. The  $1/f$  spectrum is replicated around  $f_{chop}$  and odd harmonics. As the chopping frequency increases, the low frequency noise decreases. Charge injection and clock feedthrough of the modulators is ignored for the purpose of this analysis. The spectrum and input-referred noise is plotted in Figure 5.8. The bandwidth above the chopping frequency is unsuitable for signal transmission because any signal at frequencies outside the baseband will be aliased to baseband frequencies and thus will become indistinguishable from a baseband signal. For example, if a signal at some  $f$  higher than the chopping frequency is used, the signal after modulation will be modulated to either side of  $f_{chop}$  and amplified, then will subsequently show up as distortion in the baseband after demodulation. In practice a filter is usually implemented to remove higher frequency energy content after demodulation. The

filter would typically be implemented using an OTA-C configuration.

From equation (5.9) the noise may be modeled as a simple white noise for frequencies much smaller than the 3dB corner frequencies (that is for  $f_c \gg f$  or at low frequencies). Clearly a frequency bandwidth,  $\Delta f$ , must be chosen such that it lies between some lower limit  $f_1$  and upper cutoff  $f_2$ . Given that the shape of the noise below the chopping frequency,  $f_1$  will be at zero frequency. The upper cutoff will lie somewhere below the chopping frequency. Applying the waterfilling algorithm in this case gives

$$P(f) = (\nu - N_0) \Delta f \quad (5.16)$$

where  $\nu$  is a constant and  $N_0$  is the white noise level created by the choppers. This allows for the explicit solution for the information rate

$$I = \int_{f_1}^{f_2} \log_2 \left( 1 + \frac{(\nu - N_0) \Delta f}{N} \right) df \quad (5.17)$$

Since the term inside the logarithm is a constant, this expression can be easily simplified to

$$C = \Delta f \log_2 \left( 1 + \frac{P}{N_o \Delta f} \right) = \Delta f \log_2 \left( 1 + \frac{PA_0^2}{S_0 \left( 1 + 0.8526 \frac{f_k}{f_{chop}} \right)} \right) \quad (5.18)$$

where  $P$  is the total signal power and  $N_o$  is the total noise power in the operating range. As the chopping frequency,  $f_{chop}$ , increases, information rate increases, as the noise corner frequency,  $f_k$ , increases information rate decreases. Note that this expression is similar to that derived in chapter 4 for white noise only systems.

If, however, the noise is modeled as equation (5.10), an ever increasing function, the lower bound on bandwidth is zero. The information rate for this generalized

chopper noise model is

$$I = \frac{1}{\pi^2 \ln 2} \left[ (f_{chop}\pi^2 + 8f_k) \ln \left( 1 + \frac{8}{\pi^2} \frac{f_k}{f_{chop} - f_s} \right) - 24f_k \ln 2 - 8f_k \ln \left( \frac{f_k}{\pi^2 (f_{chop} - f_s)} \right) \right] \quad (5.19)$$

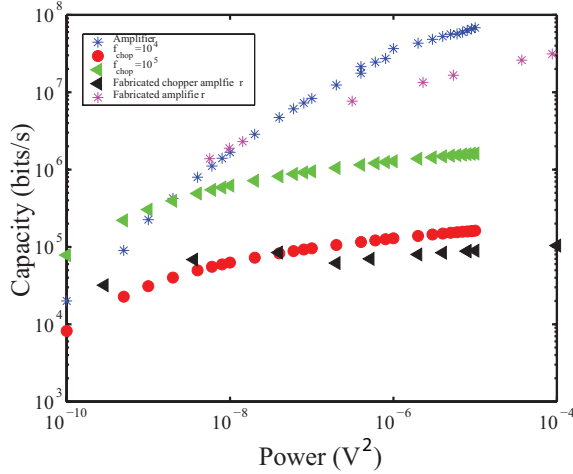
with the bandwidth,  $f_s$ , being determined from

$$P_{sig} = \frac{8}{\pi^2} \frac{S_0}{A_0^2} f_k \left[ \frac{f_s}{f_{chop} - f_s} - \ln ((f_{chop} - f_s) f_{chop}) \right] \quad (5.20)$$

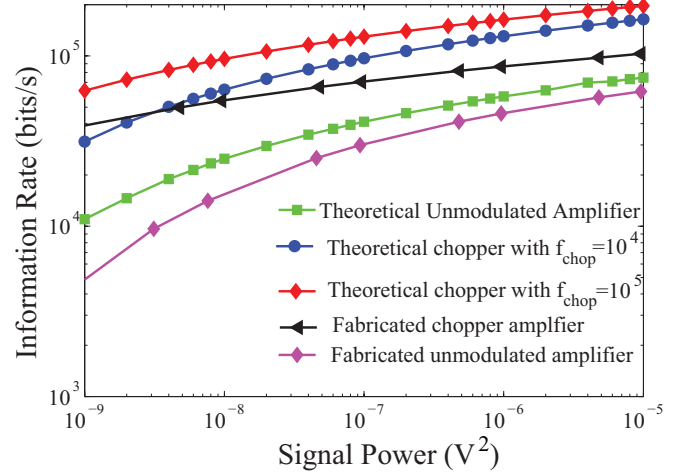
The capacity and information rate of the chopper modulated vs unmodulated amplifiers is shown in figure 5.7. The capacity of the chopper amplifier is higher than the capacity of the non-chopping version implying that it is more efficient at low signal powers. At high signal powers, the unmodulated amplifier actually has higher capacity. However if one looks at the information rate where the input signal bandwidth is limited to below the chopping frequency then the chopper modulated OTA always does better. Therefore the chopper modulated OTA performs waterfilling by moving the input signal to frequencies where the noise is lowest. It thus achieves the maximum information rate while ensuring the input signal is still amplified and not attenuated.

From this expression it can be seen that the lower the noise corner frequency, the higher the information rate. The effect of the 3dB cutoff frequency is negligible when it is much greater than the chopping frequency [56] and thus drops out of the expression. For lower 3dB cutoff frequencies the effect can be evaluated numerically if desired. Practical usage of a chopper amplifier typically places the chopping frequency at the 3dB cutoff frequency. It is easily observed that increasing the





(a) Capacity



(b) Information rate

Figure 5.7: Capacity and information rate chopper modulated and unmodulated folded cascode OTA [58].

chopping frequency increases the capacity for signals with frequency content lower than  $f_{chop}$ . No assumptions can be necessarily be made if the signal is constrained to be in bandwidths above the chopping frequency but contained strictly within the odd harmonics. This is evaluated numerically later in the dissertation.

## 5.2 Random Modulation

Now considering that the actual goal is to perform waterfilling, which inherently involves taking the input signal and allocating it to multiple frequencies, it can be noted that the standard chopping technique takes the input signal to a set of frequencies defined by  $f_{chop}$  and its harmonics. Waterfilling by definition should *smear* the input signal across multiple frequencies. This leads to the idea of randomly modulating instead of using a simple square wave. A random clock is assumed to

be generated from a clock operating at some frequency  $f_s (= f_{chop})$ . The clock can be generated as follows: in a period of time  $T$  a 1 or -1 is randomly generated for the half the period followed by a -1 for the other half of the period. The output spectrum of the clock can then be represented as [59]

$$S_{clk}(f) = \frac{1}{f_s} \left( \frac{\sin \frac{\pi f}{f_s}}{\frac{\pi f}{f_s}} \right)^2 \quad (5.21)$$

The input-referred noise is numerically determined from the convolution of the noise (equation (5.13)) and modulation signal (equation (5.21)) and is shown in Figure 5.8. The noise floor decreases as the clock period ( $1/f_s$ ) decreases. As a note random modulation has been previously proposed to reduce the spikes associated with standard modulation [60]. However the form of the clock spectrum derived is different from that already shown in this section. And although a circuit to generate the clock is shown in reference [60], all the work is simulated and most importantly the form of the random clock is different. In that work, the authors use an oscillator whose phase is randomly changed. In this dissertation we use a clock where the probability of obtaining a high or low value is a true random event driven by thermal noise events in a clocked comparator.

### 5.3 Theoretical and Experimental Results and Discussion

The theoretical information rate when the noise corner frequency ( $f_k$ ) and the 3dB cutoff frequency ( $f_c$ ) are varied is shown in figure 5.11. There are two trends which can easily be observed. First the information rate increases as the noise corner frequency decreases. Second the information rate increases with increasing

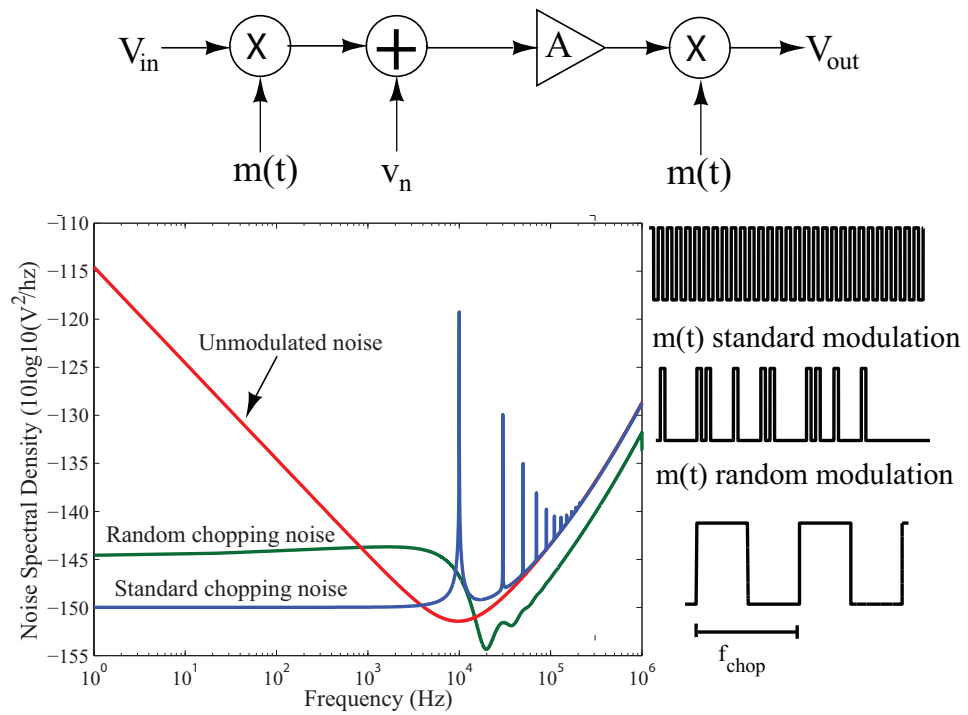


Figure 5.8: Overall system diagram, showing random and regular modulation signals, along with the input-referred noise for each modulation scheme [61].

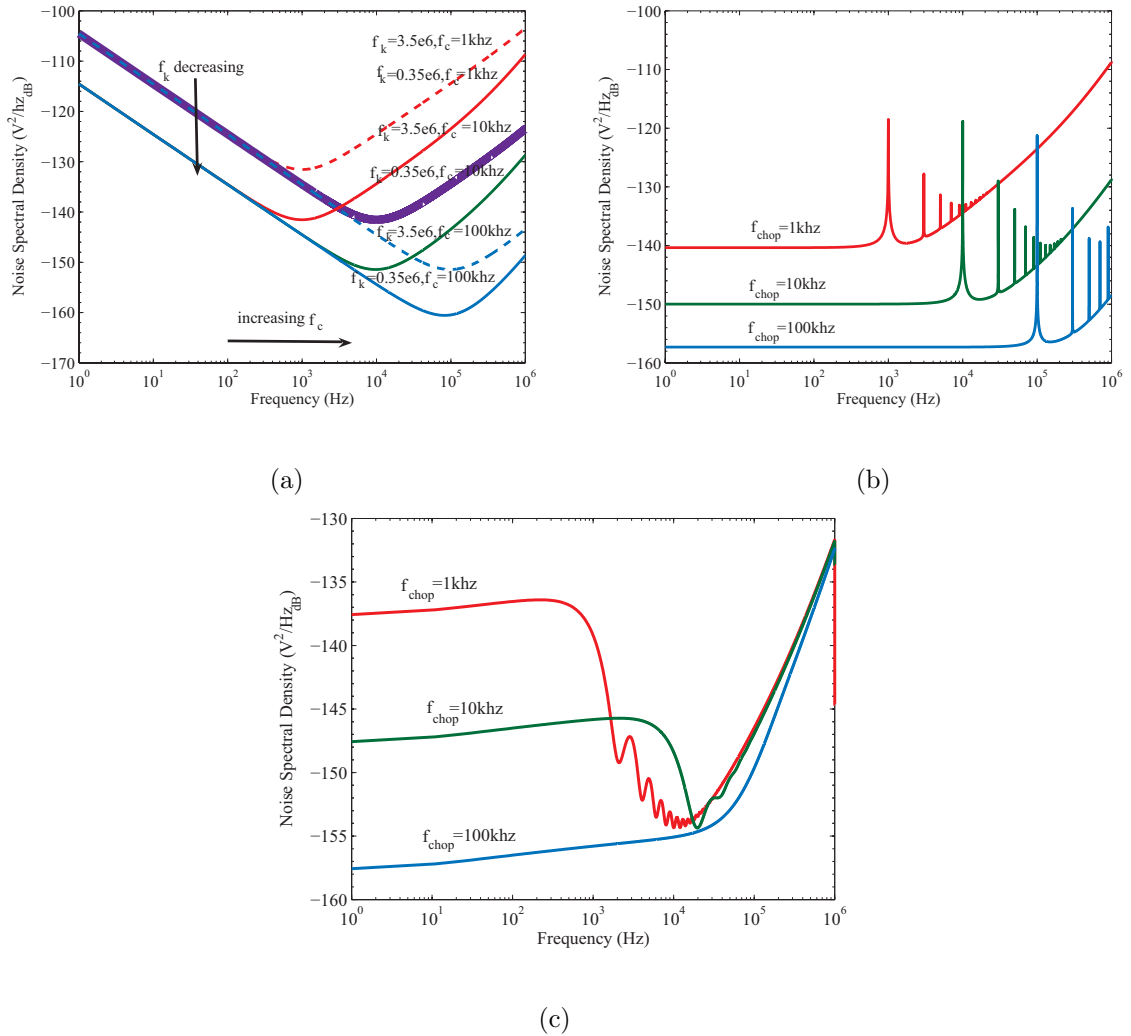
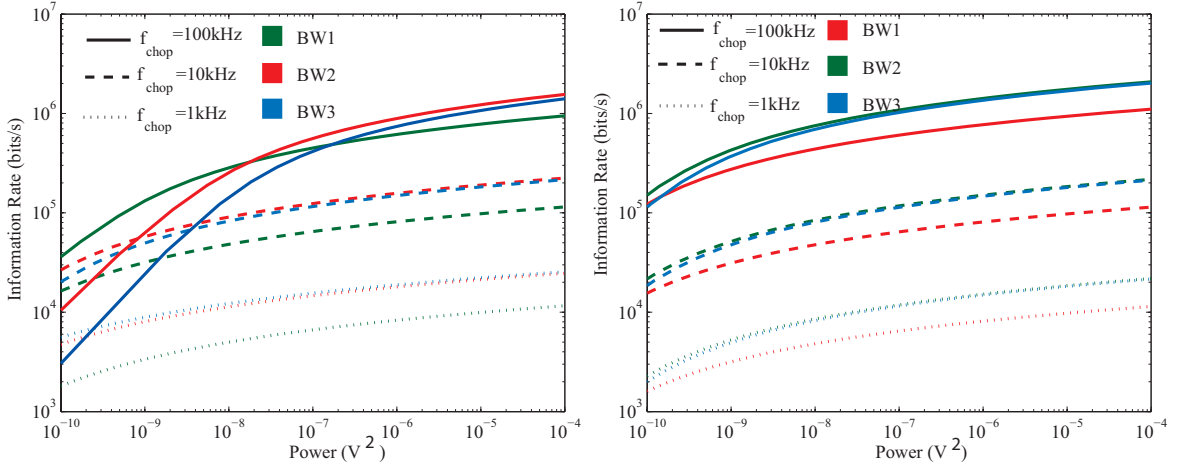
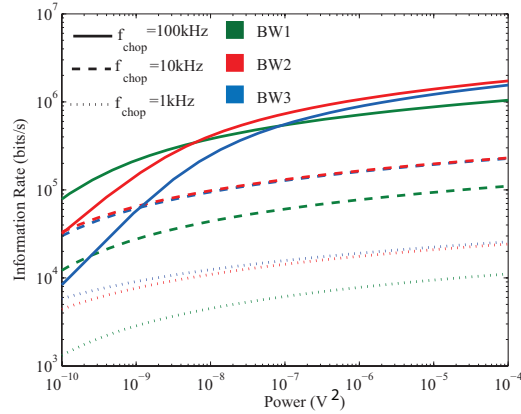


Figure 5.9: Input-referred noise for (a) unmodulated, with  $f_k = 3.5e6, 3.5e5$  and  $f_c = 1kHz, 10kHz, 100kHz$ . (b) Standard chopping and (c) random chopping schemes with  $f_{chop} = 1, 10$  and  $100 kHz$ .  $f_c = 10 kHz, f_k = 3.5e5 Hz$  [61].



(a)

(b)



(c)

Figure 5.10: Information rate for (a) unmodulated, (b) standard chopping and (c) random chopping schemes with  $f_k = 3.5e5$  and constraining the signal to be in three bandwidths, up to  $f_{chop}$  (BW1), from  $f_{chop}$  to  $2f_{chop}$  (BW2) and from  $3f_{chop}$  to  $4f_{chop}$  (BW3).  $f_c = 10\text{kHz}$ ,  $f_k = 3.5e5$ . For comparison purposes the signal limitation on the signal bandwidths are the same in all three cases [61].

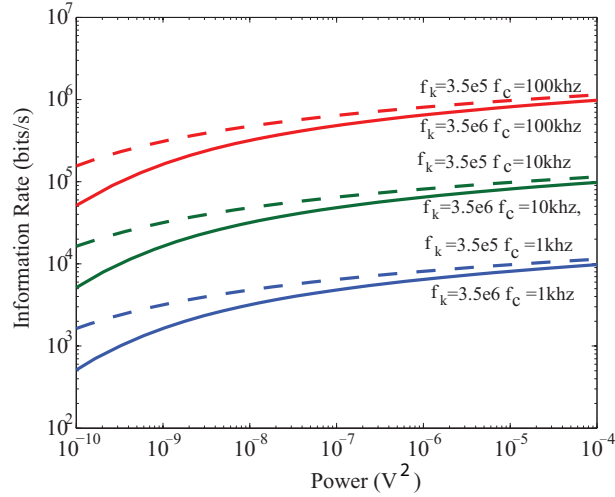


Figure 5.11: Information rate for the noise models shown in Figure 5.9(a) [61].

3dB cutoff frequency. This is clearly observed from the derived equations [61]. The results imply that increasing the bandwidth of an amplifier can improve the information efficiency of the amplifier [61]. Where information efficiency is measured in terms of the information rate. The effect of the amplifier parameters has already been studied in some detail in the previous chapter. It should be noted that the variation with the parameters shown here are very dependent on the assumption made about the manner in which these two parameters change with each other. In this portion of the work the two parameters were varied independently. However both parameters depend to some extent on the transconductance ( $g_m$ ) and the aspect ratios ( $W/L$ ) of the transistors. That is the variation of the two parameters are linked to some of the same amplifier fundamental characteristics of width, length and bias current. In certain applications more variation may need to be studied to obtain a full picture.

For the unmodulated amplifier the input signal power is intentionally allocated at the higher noise levels when introducing bandwidth limitations. This decreases the maximum information rate (Figure 5.10(a)). It is accomplished assuming an ideal brickwall filter of the the appropriate characteristic exists at the input of the system. This clearly goes against the idea of waterfilling, but is more representative of the real world use of the amplifier and is closer to the true information rate of the system. As the minimum noise level for this model is above the dominant pole, the best strategy would be to allocate the input signal power to higher bandwidths [61]. However note that this still requires allocating signals to frequency bands slightly above the dominant pole, where the attenuation may or may not be tolerable. It would be up to the designer to determine if the level of attenuation is acceptable to the application at hand.

The input-referred noise of the standard chopping modulation scheme is shown in figure 5.9(b). The noise floor is comparatively lower at the higher frequencies due the the particular chopping frequency chosen. Clearly it is possible that if the signal could be allocated at the higher frequencies that the information rate could be increased. This means placing the signal between the “peaks” in the noise spectrum. Note that this approach would have practical issues, such as aliasing, upon implementation. It is also not dissimilar to the unmodulated case. However it can be assumed that additional processing circuitry has been added to address this problem. Figure 3 examines this though of allocating the signals to these different frequency bands for all three modulation schemes. The input signal power is allocated to frequencies either below  $f_{chop}$ , or between  $f_{chop}$  and  $2f_{chop}$ , or between  $3f_{chop}$  and

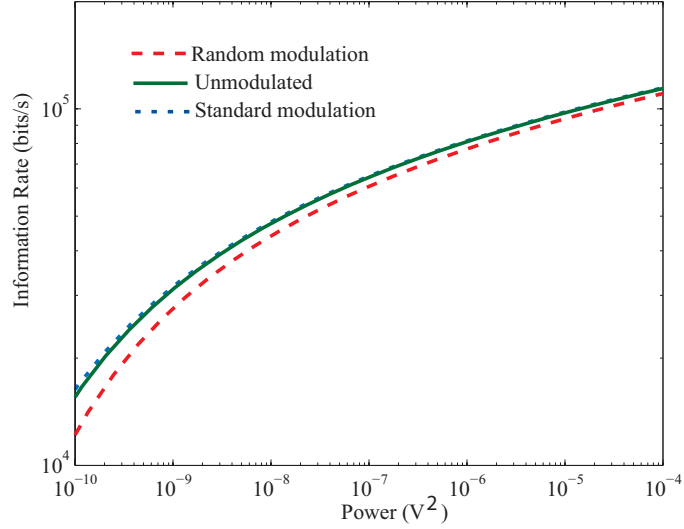


Figure 5.12: Theoretical information rate of amplifier using different modulation schemes with  $f_c, f_{chop} = 10\text{kHz}$  and  $f_k = 3.5e5$  [61].

$4f_{chop}$ . Clearly this could be continued for higher bands, however the first three are adequate for an initial consideration. For standard chopper modulation, increasing the chopping frequency increases the information rate if the signal is constrained to below the chopping frequency. Keeping the chopping frequency ( $f_{chop}$ ) constant, the information rate increases as the signal is constrained to higher (but possibly smaller range) bandwidths (Figure 5.10(b)). Figure 5.10(c) shows that the random chopper modulation is qualitatively similar to the standard chopper modulation. An important fact to recall when considering the three modulation schemes is that although the information rates may be the same and the bandwidth is constrained to be within a specific range, the actual signal band that achieves the maximum information rate is necessarily different for each scheme. This is due to the differences in the shape of the noise spectrum [61].



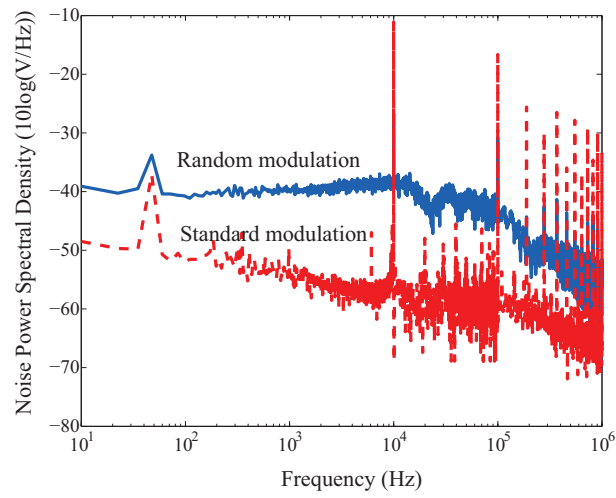


Figure 5.13: Measured output noise of circuit,  $f_{chop}=10$  kHz,  $f_c$  10 kHz [61].

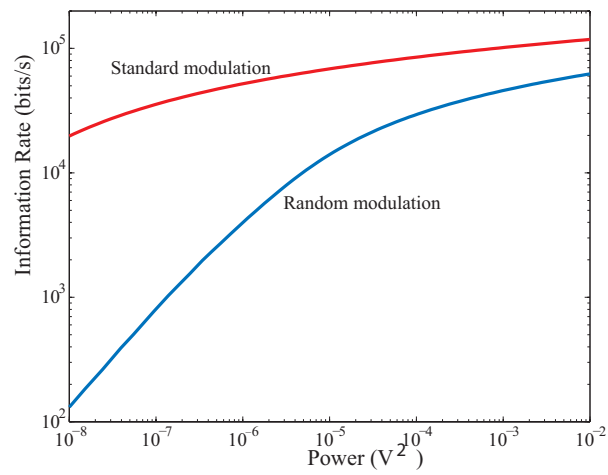


Figure 5.14: Experimentally derived capacity of noise in Figure 5.13 [61].

In the real world there is no choice as to whether the input signal may be placed in particular frequency bands. For example if the application is extracellular potential detection, the input signal will be in the range of tens of kilohertz. Therefore for all three modulation schemes, the input signal was considered to be in the frequency band 0 to  $f_c$ . That is the signal can only be placed up to the 3dB cutoff frequency of the main OTA. The information rate was then calculated assuming an ideal filter is placed in front of the system with cut-off frequency  $f_c$ . The information rate was computed using equation (3.5) where the cutoff frequency was  $f_k = 3.5 \times 10^5$  Hz, the thermal noise level was  $S_o = 10^{13}$  V<sup>2</sup>/Hz, the low frequency gain was  $A_o = 1$ , and the 3dB frequency was  $f_c = 10^4$  Hz [61]. The low frequency gain is assumed to be 1 for simplicity, different levels will scale the input referred noise and information rate accordingly. The trends of the results are not affected by the value chosen for the low frequency gain.

Since the noise is higher for the randomly modulated amplifier, its rate is lower than the standard modulation scheme (Figure 5.12). The noise is higher because the random modulation spreads the original noise spectrum over all frequencies. Compared to the standard case, the random modulation can be thought of as moving the energy at the odd harmonics of the standard chopping frequencies to the rest of the spectrum. This therefore means the standard modulation has very high energy within specific small frequency ranges, while the random modulation approaches a white noise. In order for the information rate using random modulation to approach that of standard modulation, the clock frequency used to generate the random signal must be increased. This causes the noise spectrum to be further spread out and the

overall noise floor to decrease, and thus there is an increase in the signal to noise ratio over the same bandwidth [61]. This increase in noise floor is easily decreased. Based on the circuit used to implement the random modulation there will be some maximum chopping frequency that is usable. Beyond this the circuit may have glitches that could affect the generation of the random signal. It may be possible to improve this by moving to a different process. It may also be possible, however, to implement a pseudo-random signal using software and a data acquisition card or a microprocessor it may be possible to generate much higher chopping frequencies.

Figure 5.13 shows the measured noise of a chopper modulated folded cascode OTA [58, 61] which utilized both modulation schemes. The modulation is accomplished using standard cross-coupled MOS switches, and a true random number generator developed by Xu *et al.* (and shown in figure 5.15 for reference) is used to provide the random clock in the case of random modulation [62]. Figure 5.16 shows the experimentally measured spectrum of the clock, which is driven by thermal noise. Experimentally the clock shows small energy content at the chopping frequency, however this is negligible. Figure 5.14 shows the information rate of both random and standard chopping. The information rate of the standard chopper amplifier is higher than that of random chopping due to the higher signal to noise ratio of the former. This is a direct consequence of the modulation frequency chosen.

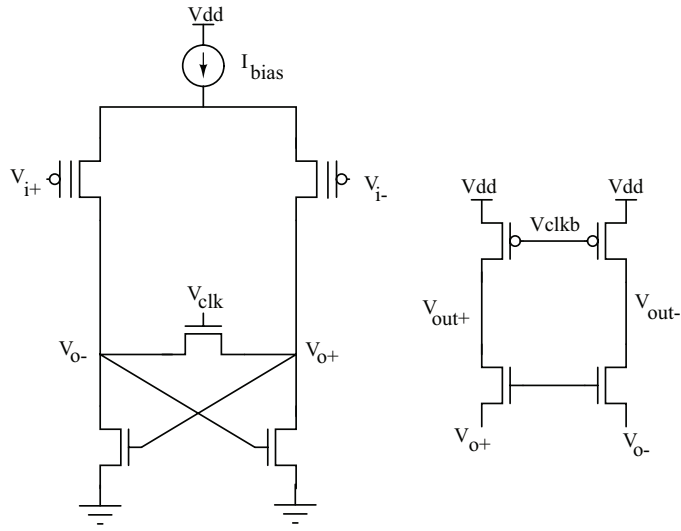


Figure 5.15: Random number generator used in experiments.

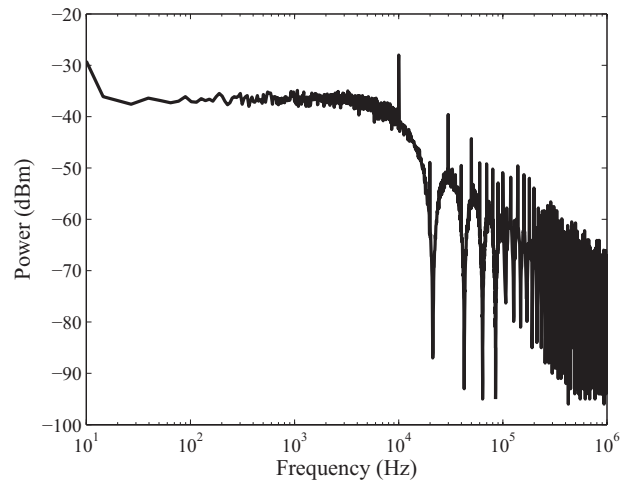


Figure 5.16: Experimentally measured clock spectrum with frequency of 10 kHz.

## 5.4 Bit Energy of Modulation Schemes

It should be noted that the chopper modulated and unmodulated OTAs have the same steady state power consumption as the switches which make up the modulators ideally draw no current once they are switched on. However there is some dynamic power dissipation governed by the intrinsic parasitic capacitances of the transistor as well as the resistance of the switch. If considering steady state switching however, then the chopper modulated amplifier will always have a lower bit energy, especially when considering the information rate. For higher signal powers there is possibly a trade off involved into which configuration has a higher cost. The standard configuration in practical uses requires a low pass filter to cleanly recover the signal. The random configuration does not. This is because in the simple square wave case large peaks are obtained at the chopping frequency and its odd harmonics. In the random case these peaks are smeared out over all frequencies, and thus the signal is much cleaner when viewed in the time domain. The low pass filter, if assumed to be a second order filter made with simple OTA's will add  $2I_{bias}(V_{dd} - V_{ss})$  to the power consumption previously calculated. Because it is in a later stage it will have negligible contribution to the input referred noise. In both cases the clocks will also add to the total power consumption of the system. The random clock is experimentally implemented as the same random number generator used in reference [62] based on a clocked cross coupled differential pair comparator. This clock will add  $2I_{bias}(V_{dd} - V_{ss})$  to the total power, the base clock was provided by a function generator. The standard clock was experimentally implemented using

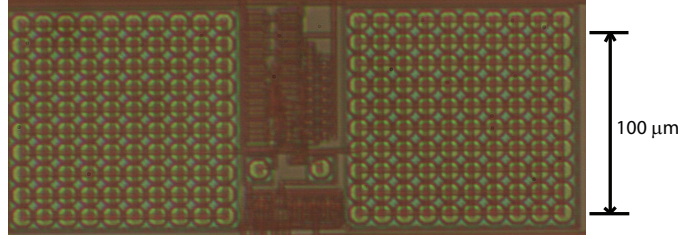


Figure 5.17: Photomicrograph of implemented chopper bioamp [58].

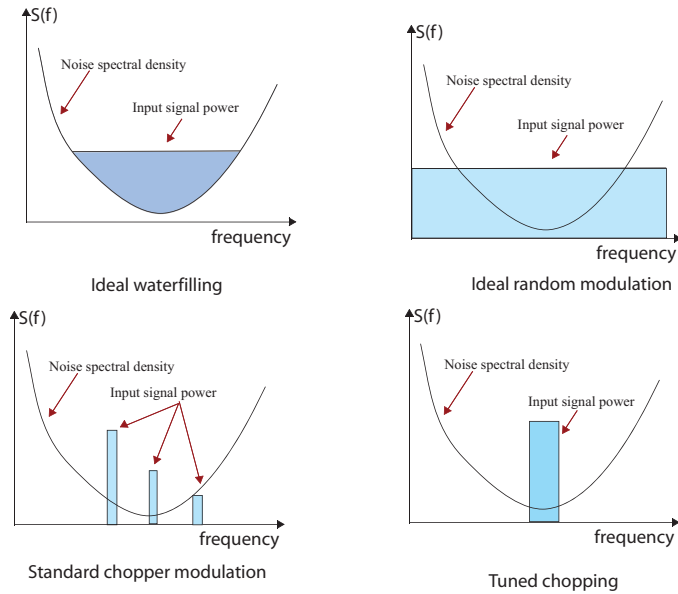


Figure 5.18: Different methods of frequency allocation of the input signal.

a function generator. In both cases the modulator and demodulator clocking signals must be in quadrature, and standard non-overlapping clock circuitry consisting of AND gates and inverters is implemented to accomplish this. The flicker noise contribution of the clocks in both cases is assumed to be negligible. There will however be  $kT/C$  noise due to the switching and the parasitic capacitances.

## 5.5 Modulation as an Optimisation Technique

In chapter 4 we explored the design space of amplifiers but in a practical setting this may not be useful as the signal will have to be in the right frequency range to achieve the maximum information rate. In an application such as detecting extracellular signals, the input signal frequency range is fixed. So let us consider a bioamplifier again, the input signal is at a narrow range of frequencies for any given application. Figure 5.18 shows possible applications of the input signal power. Ideal waterfilling can be seen as just filling up the cup. Standard chopping can be seen to place the signal at specific frequencies where only the fundamental block is the wanted signal. Ideal random modulation can be seen to spread out the signal over all frequencies regardless of where the noise is. However the design methodology indicated by using the information rate is most likely using a tuned chopping method. This can be thought of as taking the input signal (which is itself a relatively narrow band signal assuming we are sticking to action potential type signals) and placing it in a simple bucket that is narrowly defined by a sweep of frequencies. These modulation frequencies can be easily supplied by software implementations.

## 5.6 Chapter Summary and Discussion

Chopper modulation was seen as a method of increasing the information rate. Standard chopping modulation and random chopping modulation schemes were compared to each other and to the unmodulated case, and although random chopping has the effect of smoothing the spikes that occur at the odd harmonics of the chop-

ping signal, it does so at a slight increase in the noise floor over standard chopping (assuming the length of time for a 1 or -1 is the same). To achieve similar noise floors for both chopping schemes the fundamental clock frequency of the random signal must be higher than that of the square wave signal. The prediction of the simple noise model i.e. which scheme offers optimal transmission, corresponds with the measured experimental results. Both standard and random modulation may be used to achieve higher information in amplifiers, however modulation in general requires extra circuitry and the increase in capacity comes at a slight expense of area and power. Portions of the work reported in this chapter, particularly the results of the random modulation and standard modulation, are published in references [58,61].

It should be noted that all work thus far has not taken into account any further processing. The type of processing will greatly depend on the application. In the case of the example application, extracellular potential sensing, if the purpose is just to record data, then the job is complete as presented. However if there are multiple sensors on chip and there needs to some determination of where in space the signal is located then further processing is needed, specifically in this case spike sorting.

Waterfilling is an asymptotic result and one would have to wait a long time and therefore the question could be asked as to whether the experimental results are meaningful. The results presented are quite meaningful, thinking about waterfilling lead to reshaping the noise in such a way as to get the best signal to noise ratio and bandwidth trade-off. Experimental results are measured directly in the frequency domain using a spectrum analyzer. It can be thought of as sweeping across a range of frequencies with a narrow band pass filter, and then measuring the signal



power. Thus the length of time for measurements experimentally increases for higher frequencies and more narrow band pass filters. If one is concerned about the length of time for the actual signal, recall that the physical implementation places constraints on how high a chopping frequency may be chosen. In practice the chopping frequency is set to be at the 3dB corner frequency as if the chopping frequency is greater than the 3dB frequency there will not be sufficient gain as intended. If the chopping frequency is less than the 3dB frequency then any filter after the demodulator may be unable to reject enough of the spikes due to charge injection and parasitic coupling at the input modulator. If the time constant of the spikes are much smaller than the chopping period then most of the energy will remain at frequencies higher than the chopping frequency. In addition the offset of the chopper amplifier is limited by charge injection mismatch [57].

For time domain considerations, the amplifier needs to be designed to have the appropriate response time to an incoming signal in the frequency range of interest. That is the slew rate should be taken into account. If the input signal is a binary on/off signal, then the signal can be detected in the traditional way using a comparator. Note however as implemented that on/off in this case is  $\pm 1$  due to the use of bipolar rails. It should be noted that all the work outlined in this chapter

As a final note random modulation is similar in spirit to spread spectrum communications (figure 5.19 where the signal is deliberately spread over the frequency domain usually for security reasons to prevent detection, interference and jamming. It generally results in a signal that is of much wider bandwidth than the original. The spreading sequence,  $m(t)$ , is thought of as a noise signal in these applications

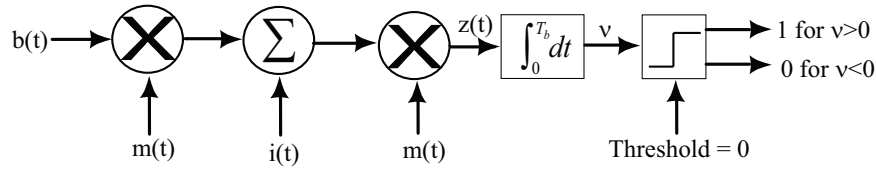


Figure 5.19: Ideal Spread Spectrum System.

and is usually implemented using pseudo random generators which generate maximum length sequences. This sequence is known both to the transmitter and the receiver. The pseudo random sequence is at a frequency much higher than the signal. The signal  $i(t)$  in this case is the interfering or jamming signal. The purpose of spread spectrum in this case is quite different from that outlined in this chapter. In this chapter it has been argued that modulation (be it random or standard) can be thought of as the physical analog to the water-filling algorithm for our chosen communication channel, the amplifier.

In the spread spectrum case note that there is a decision device, (which in the traditional circuit world would be implemented as a comparator). In fact in the typical system model the objective is to attain reliable communication over a noisy channel. The usual approach is to add communication systems to the noise channel such that one can detect and correct the errors caused by the channel. In this sense one may think of the modulator circuit as the encoder and the demodulator circuit as the decoder.

This is however quite different when compared to how the circuit is thought of in the traditional sense. In the traditional sense if we think of an analog spike (say from a biological cell) coming in then if we are only interested in when a spike occurs

and not its shape then a thresholding circuit may be implemented which will swing to the top supply rail if the spike is some appreciable amount above the noise level and will otherwise swing to the low supply rail. The waterfilling approach, however, allowed the noise level to be lowered which increased the probability of the circuit detecting the spikes accurately. It thus increased the sensitivity of the sensor.

Note that the argument for using standard or random modulation is entirely subject to the application at hand. It may be argued that a filter is still necessary after the demodulator in the standard case as there is still the same energy content from the noise and if it is large enough it may affect some applications. Certainly the requirements of the filter in the random case are less stringent than in the standard modulation case.

Experimentally the recovered signal was found to be a good representation of the test input signal in the random modulation case, albeit with a higher noise floor (figure 5.20). In the standard modulation case the higher order frequency content in the output signal must be filtered out to accurately recover the signal. Theoretically because we are simply multiplying the signal by  $(\pm 1)^2$ , the signal is able to be completely recovered.

Komae looked at a specific problem of trying to implement a method of a transmitter to predict the future position of a receiver [63,64]. This has applicability in satellite communications systems. In the scheme they use a photodetector to estimate where the center of the beam of interest lies and they develop a control law based on that. This is an inherently different problem to that being solved by this dissertation. In this dissertation the design of the amplifier is of paramount

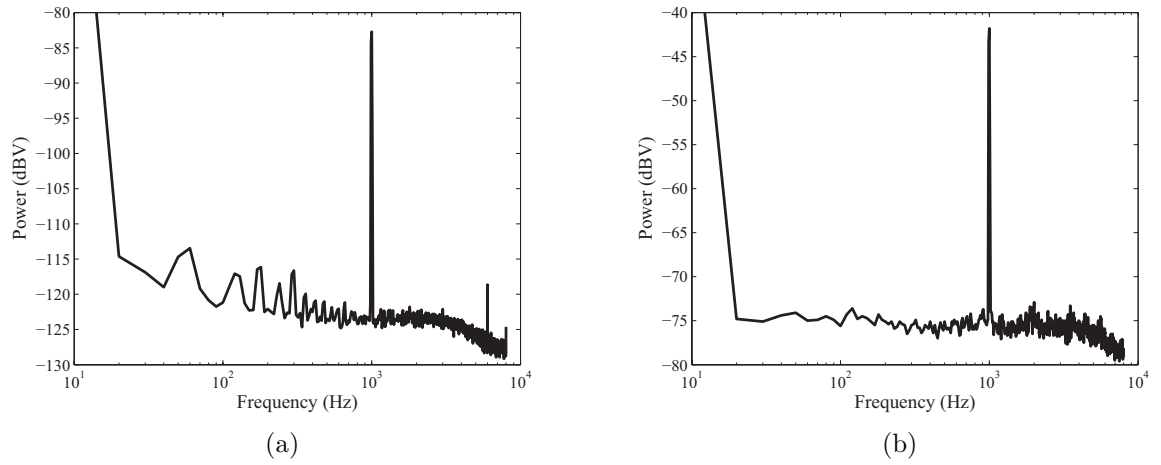


Figure 5.20: Experimental signal spectrum of a (a) 1 kHz sine wave before and (b) after being random modulated twice.

importance and as such issues other than that which pertains to the amplifier design itself are deemed irrelevant to the problem at hand.

## Chapter 6

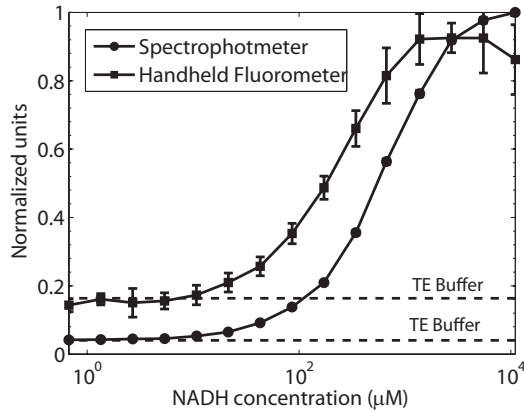
### Conclusions

This dissertation applied results from information theory to traditional circuit design. This involved modeling analog circuits as Gaussian channels corrupted by noise. This work was restricted to CMOS amplifier circuits as these are increasingly being used for sensor applications in the bioengineering field where the signal of interest is extremely weak and the power resources are limited. Although there are a variety of noise sources associated with CMOS transistors, at lower frequencies only two sources, flicker and thermal noise dominate. Thermal noise is a white noise source while flicker noise is larger at low frequencies and dies out at higher frequencies. As a result when determining the information rate using the input referred noise of the circuit, it was found that the optimum allocation of signal power tended to be at higher frequencies where the signal has a greater probability of being attenuated. In order to actually achieve optimum signal allocation, thinking about the waterfilling algorithm leads to considering modulation techniques. The first modulation technique explored was standard chopper modulation, wherein the input signal is modulated with a square wave, amplified and then demodulated with the same square wave. This has the effect of moving the signal up to frequencies where the noise is lower thus somewhat approximating the idea of waterfilling. It was however noticed that standard modulation places the signal at frequencies within a

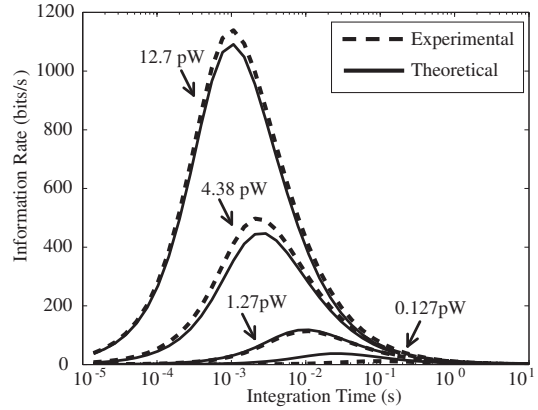
narrow band, a better approximation to waterfilling would be to spread the incoming signal out. This leads to implementing random modulation using a true random number generator to generate a random square wave in place of the standard one. The cost of using modulation is a slight increase in power, that is a increase in bit energy. The random modulation implementation has a lower bit energy than the standard implementation. An amplifier was designed and experimentally verified for this purpose.

In addition this work also compared the information rates and bit energies of various operational transconductor amplifier configurations. The amplifiers were fabricated in a  $0.5\mu m$  3-metal, 2-poly CMOS process. The information rates and bit energies vary depending on the bias current and the aspect ratios of the constituent transistors. Simple models were developed to allow a designer to perform “hand calculations” in order to use information rate and bit energy as a characteristic to be designed for. Additional consideration was taken to determine how accurate the noise models needed to be in order to predict trends and it was found that for most cases the simple model was adequate. Two amplifiers which had design specifications of low frequency gain and cut off frequency but designed in two different processes were also experimentally verified.

While this work has taken a detailed look into determining how to incorporate information theoretic ideas into mixed signal circuit design there are many avenues for future directions. These include applying the same algorithms to different classes of sensors. An example has already been started on for fluorescence detector where the input signal is the intensity of light and is detected by an active pixel sensor. A



(a) Typical calibration curve for a fluorescence detector [1]



(b) Information rate [65]

Figure 6.1: Information rate for a active pixel sensor

cursory look at an example experiment shown in figure 6 shows that the input signal has a large dynamic range. The amount of light detected by the detector is dependent on the integration time. The information rate for such a sensor implemented with a voltage mode pixel shows a relationship between the optimum integration time and the intensity of the light signal. This information can then be used while designing a sensor array for this type of application [1, 65]. The long term impact of this dissertation is that it demonstrates and explores in depth a new approach to circuit design for sensors based on information theoretic results, and has the promise of improving the sensitivity of biosensors.

In this dissertation the goal was to make the first stage of processing more efficient, as it is well known that most of the problems with intrinsic sensor noise is in the first stages (ignoring environmental noise). This dissertation thus focused

on the amplifiers which do the initial detection of the signal and not on the circuits that can be implemented further along the chain do perform specific mathematical functions on the acquired data.

Another note is that we assumed an average power constraint on the input signal, however in an analog setting our input signal is also constrained by the power supply rails so the that we can rework much of this assuming a peak signal power constraint. In which case

$$C \leq W \log_2 \frac{N + \frac{2}{\pi e} P}{N} \quad (6.1)$$

In this case the input signal is assumed to be evenly distributed between  $-\sqrt{P}$  and  $\sqrt{P}$ . Where  $P_{peak} = V^2/4$  if constrained from zero to V volts then the average power is  $V^2/12$ . For small signal to noise ratios the above tends to the average power result as displayed in Chapter 1. In our presumed application (amplification of cell signals) these signals tend to be in the tens to hundreds of microvolts range which are close to the noise levels and the assumption of average power constraint as opposed to peak power constraint is validated.

To conclude the applicability of considering waterfilling for general amplifier design has been demonstrated. Models have been introduced in order to accurately apply the algorithm. Considering the algorithm, amplifier efficiency, as measured by the information rate was improved by implementing random chopper modulation.



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## List of Publications

### Journal Publications

1. ***N. Nelson***, S. Prakash, D. Sander, M. Dandin, A. Sarje, H. Ji, P. A. Abshire, "Handheld Fluorometers for Lab-on-a-Chip Applications," IEEE Transactions of Biomedical Circuits and Systems Apr 2009

### Conference Publications

1. T. Hamilton, ***N. Nelson***, D. Sander and P. Abshire, "A Cell Impedance Sensor Based on a Silicon Cochlea," IEEE Biomedical Circuits and Systems, 2009
2. M. Dandin, J. Gallagher, M. Piyasena, ***N. Nelson***, I. D. Jung, M. Urdaneta, E Smela and P. Abshire, "Post-CMOS Packaging Methods for Integrated Biosensors," IEEE Sensors, 2009
3. ***N. Nelson***, P. Abshire, "Information Transmission Using a Generalized Chopper Amplifier: Comparison of Modulation Schemes," Conference on Information System and Sciences 2009
4. D. Sander, ***N. Nelson***, P. Abshire, "Noise model, analysis and characterization of a differential active pixel sensor," IEEE International Symposium on Circuits and Systems, 2008
5. D. Sander, ***N. Nelson***, P. Abshire, "Integration time optimization for integrating photosensors," IEEE International Symposium on Circuits and Systems, 2008
6. ***N. Nelson***, D. Sander, M. Dandin, A. Sarje, S. Prakash, H. Ji, P. A. Abshire, "A handheld fluorometer for measuring cellular metabolism," IEEE International Symposium on Circuits and Systems, 2008
7. ***N. Nelson***, S. Prakash, D. Sander, M. Dandin, A. Sarje, H. Ji, P. A. Abshire, "A Handheld Fluorometer for UV Excitable Fluorescence Assays," IEEE Biomedical Circuits and Systems Conference, 2007
8. M. P. Dandin, ***N. Nelson***, H. Ji and P. Abshire, "Single Photon Avalanche Detectors in Standard CMOS," IEEE Conference on Sensors, 2007
9. ***N. Nelson*** and P. Abshire, "Chopper Modulation Improves OTA Information Transmission," IEEE International Symposium on Circuits and Systems 2007
10. D. Sander, M. Dandin, H. Ji, ***N. Nelson***, P. Abshire, "Low-noise CMOS Fluorescence Sensor," IEEE International Symposium on Circuits and Systems 2007
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