ABSTRACT

Title of Document:	DETECTION OF INTERCONNECT FAILURE PRECURSORS USING RF IMPEDANCE ANALYSIS
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Many failures in electronics result from the loss of electrical continuity of common board-level interconnects such as solder joints. Measurement methods based on DC resistance such as event detectors and data-loggers have long been used by the electronics industry to monitor the reliability of interconnects during reliability testing. DC resistance is well-suited for characterizing electrical continuity, such as identifying an open circuit, but it is not useful for detecting a partially degraded interconnect. Degradation of interconnects, such as cracking of solder joints due to fatigue or shock loading, usually initiates at an exterior surface and propagates towards the interior. A partially degraded interconnect can cause the RF impedance to increase due to the skin effect, a phenomenon wherein signal propagation at frequencies above several hundred MHz is concentrated at the surface of a conductor. Therefore, RF impedance exhibits greater sensitivity compared to DC resistance in

detecting early stages of interconnect degradation and provides a means to prevent and predict an important cause of electronics failures.

This research identifies the applicability of RF impedance as a means of a failure precursor that allows for prognostics on interconnect degradation based on electrical measurement. It also compares the ability of RF impedance with that of DC resistance to detect early stages of interconnect degradation, and to predict the remaining life of an interconnect. To this end, RF impedance and DC resistance of a test circuit were simultaneously monitored during interconnect stress testing. The test vehicle included an impedance-controlled circuit board on which a surface mount component was soldered using two solder joints at the end terminations. During stress testing, the RF impedance exhibited a gradual non-linear increase in response to the early stages of solder joint cracking while the DC resistance remained constant. The gradual increase in RF impedance was trended using prognostic algorithms in order to predict the time to failure of solder joints. This prognostic approach successfully predicted solder joint remaining life with a prediction error of less than 3%. Furthermore, it was demonstrated both theoretically and experimentally that the RF impedance analysis was able to distinguish between two competing interconnect failure mechanisms: solder joint cracking and pad cratering.

These results indicate that RF impedance provides reliable interconnect failure precursors that can be used to predict interconnect failures. Since the performance of high speed devices is adversely affected by early stages of interconnect degradation, RF impedance analysis has the potential to provide improved reliability assessment

for these devices, as well as accurate failure prediction for current and future electronics.

DETECTION OF INTERCONNECT FAILURE PRECURSORS USING RF IMPEDANCE ANALYSIS

By

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Dedication

To my wife, Jiseon Shin,

my parents, and family.

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Chapter 1:

Introduction

As clock speeds and communication frequencies rise, the performance and reliability of electronic products are becoming increasingly sensitive to the integrity of the interconnects across which signals travel. Common board-level interconnects include solder joints, printed circuit board traces, component leads and connectors. These interconnects are susceptible to fatigue [1][2][3][4], creep [5], corrosion [6], and mechanical over-stress [7] failures, which are generally caused by cracks or chemical reactions that initiate in the circumferential area and propagate inward. Figure 1 summarizes the typical load conditions leading to interconnect failure and the corresponding failure mechanisms and damage initiation sites.

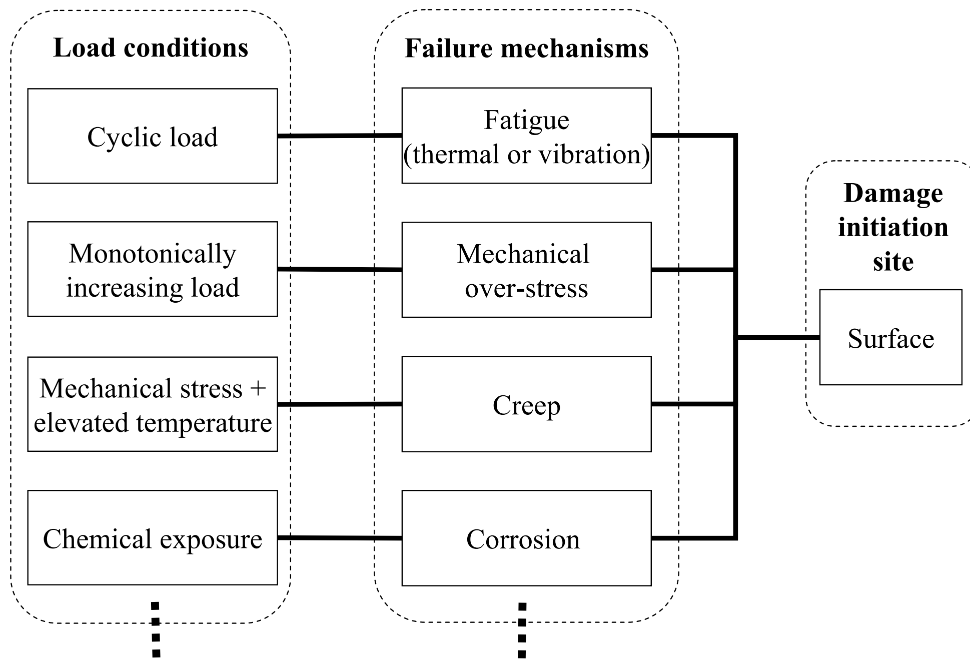


Figure 1 – Typical causes of interconnect failure

1. Problem Statement

The electronics industry has been traditionally using a measurement of DC resistance to monitor interconnect reliability. As a reliability monitoring tool, DC resistance often responds too late: for example, after a crack is large enough to result in a DC open circuit. Thus, when DC resistance is used to assess interconnect reliability, it may overestimate lifetime and preclude the opportunity to conduct preventive maintenance, allowing the probability of severe damage to the system. Successful detection of incipient degradation can provide a valuable basis for early prediction of interconnect failure of electronics systems. Therefore, an alternative means is required to detect early stages of interconnect degradation, and thus to predict the time to impending interconnect failure with an improved sensitivity compared to DC resistance.

2. Background and motivation

The skin effect is a phenomenon wherein signal propagation at high operating frequencies is concentrated at the surface of a conductor. Due to the skin effect, even a small crack at the surface of an interconnect can directly influence signal integrity, which can be measured by changes in the RF impedance. Therefore, RF impedance should be able to provide improved sensitivity to early stages of interconnect degradation. Figure 2 shows a conceptual representation of the increased sensitivity of RF impedance measurements to interconnect degradation compared to DC resistance.

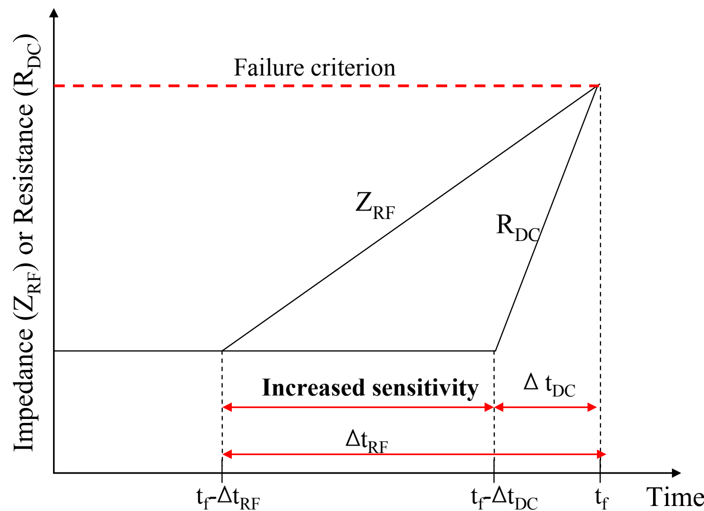


Figure 2 – Conceptual representation of increased sensitivity of RF impedance to interconnect degradation, t_f is the time to complete separation of the interconnect, Δt_{RF} and Δt_{DC} are the advanced warnings of failure provided by RF impedance and DC resistance, respectively

"Skin depth" refers to the thickness of the conductor within which approximately 63% of the current is contained [8]. As shown in Equation 1, the skin depth, δ, is directly related to the frequency, f, and the resistivity of the conductor, ρ:

$$\delta = \sqrt{\frac{\rho}{f \pi \mu}} \tag{1}$$

where μ denotes the material's permeability. In order for RF impedance to exhibit enhanced sensitivity to interconnect degradation, the skin depth should be much less than the interconnect thickness. Figure 3 describes the relationship between the frequency and the skin depth for some common interconnect materials, copper and eutectic tin-lead solder, compared to the typical dimensions of these two kinds of interconnects. According to Figure 3, the skin depth for both copper and eutectic tin-lead becomes less than about a tenth of the interconnect thickness above approximately 500 MHz. Therefore, it is possible for RF impedance over the frequency of 500 MHz to respond to interconnect degradation earlier than DC resistance. For eutectic tin-lead solder, the skin depth corresponding to this frequency is 8.5 micrometers.

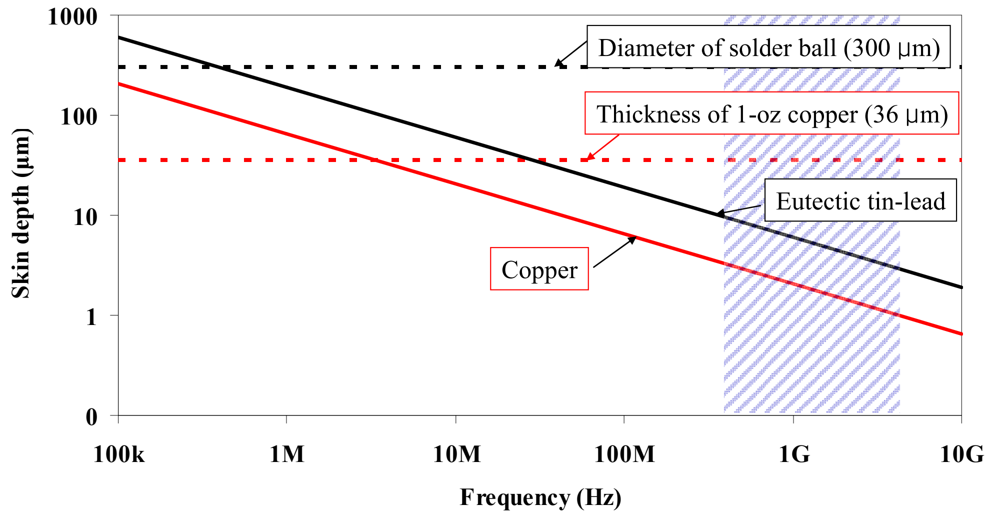


Figure 3 – Comparison between skin depth and interconnect dimensions

3. Detection methods using DC resistance

For reliability monitoring of electronic products, the electronics industry has been using either event detectors or data loggers, which are based on measurement of DC resistance [10][11][12]. Typically, DC resistance responds to a short or an open state of a conductor quite well; however, it is not well-suited to indicate intermediate stages such as a partially degraded interconnect. Several researches have endeavored to detect the degradation of an interconnect using DC resistance.

Qi, *et al.* [12] showed that measurement technique influences detection of solder joint failure. For instance when an event detector was chosen as a measurement instrument, failure should be defined as the first increase of an absolute DC resistance value, not as relative changes. Also, they pointed out shortcomings of the current detection methods based on DC resistance due to limited sampling rate and resistance characteristics during degradation.

Caers, *et al.* [13] observed an increase of the solder joint resistance in the range of milliohms as a crack propagated, which was too small to be detected by typical resistance monitoring techniques. Since these resistance changes during degradation are so small, DC resistance is not sensitive to the early stages of interconnect degradation, such as a partial crack of a solder joint, nor does it provide a sensitive and practical means of monitoring degradation.

4. Detection methods using high frequency signal parameters

The high frequency signal parameters, such as scattering parameters (or S-parameters), RF impedance, and time domain reflectometry have previously been used to characterize interconnect degradation.

Putaala, *et al.* [14] performed temperature cycling testing on BGA components in the range of -40 °C to 125 °C, and monitored the signal return loss (S_{11}), one of the S-parameters, and DC resistance during the test. They measured the signal parameters by taking the test assemblies out of the chamber at the intervals of 5-150 cycles during the test. The results showed qualitative changes in the S_{11} as the component degrades, while the DC resistance remained constant during the test.

Ghaffarian, *et al.* [15] also conducted temperature cycling testing on BGA packages in the range of -55 °C to 125 °C to characterize RF interconnects using S-parameters. They measured the signal return loss (S_{11}) and insertion loss (S_{21}) before the test and after 500 cycles for which only one solder joint of the BGA opened. Both the S_{11} and S_{21} changed qualitatively before and after the test. However, the signal

degradation of the S-parameter was not enough to indicate the increased sensitivity compared to DC resistance.

Foley, *et al.* [16] presented an approach for void detection in a transmission line by monitoring changes in the leakage conductance parameter calculated from the S-parameter measurements. While stressing the transmission line to induce voids, they measured the four transmission line parameters: the series resistance, the series inductance, the shunt capacitance and the leakage conductance. The results showed that the leakage conductance was the most sensitive parameter among the four transmission line parameters, including the measurements based on DC resistance.

Kruger, *et al.* [17] showed the improved sensitivity of the S-parameters compared to the DC resistance in response to physical distortion of a signal line. They simulated crack propagation by creating a controlled discontinuity on a signal line with monitoring the S-parameters, as well as the DC resistance. Both the FEA and the experimental result indicated that the changes in the S-parameters were greater than changes in the DC resistance, and increased as the crack propagated inward.

Most studies focused on either detection of defects and voids in a signal transmission line or simulation of changes in high frequency signals due to changes in physical geometry. However, this study focuses on quantification of the increased sensitivity of RF impedance compared to DC resistance in detecting early stages of interconnect degradation. In-situ monitoring of RF impedance during interconnect degradation allowed for investigation of the effect of physical degradation process of an interconnect on changes in RF impedance, and thus for prediction of interconnect remaining life.

5. Signal analysis techniques

In high frequency applications, S-parameters are commonly used to characterize electrical performance. S-parameters can be measured by using a network analyzer to send high speed signals through the circuit and measuring reflection (S_{11}, S_{22}) and transmission (S_{21}, S_{12}) coefficients over either the frequency or the time domain. A frequency domain measurement shows the effect of impedance discontinuities present in the circuit as the amplitude of the reflected (S_{11}) or transmitted (S_{21}) signal across the frequency spectrum, although this measurement does not directly provide spatial localization of the discontinuities. On the other hand, a time domain measurement shows any impedance discontinuities as discrete peaks with respect to their positions in the circuit. This is useful in identifying fault locations.

While a typical time domain measurement uses a sine wave to characterize the circuit, a time domain measurement using a network analyzer is a little more complicated. The network analyzer sweeps across the frequency range defined by the user and collects the S-parameters according to the frequencies. The network analyzer then applies an inverse fast Fourier transform to the frequency domain results, and obtains the time domain measurement results. Therefore, the time domain measurement using a network analyzer is a composite response of all the frequencies monitored. Figure 4 offers a comparison between frequency and time domain analysis. Since this study focuses on the solder joint degradation that occurs at specified locations in the circuit, a time domain analysis was conducted.

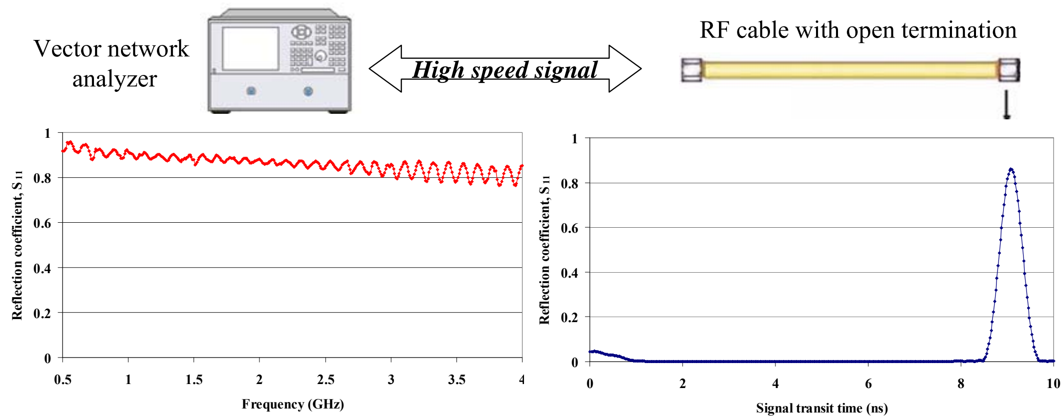


Figure 4 – Frequency domain analysis vs. time domain analysis

6. *Time domain reflectometry*

Time domain reflectometry (TDR) is a technique that characterizes impedance discontinuities within the circuit using signal reflection over the time domain. The independent variable, or x-axis, of the time domain plot is the round-trip transit time for electrical signals from the network analyzer port to a particular location on the circuit. The signal propagation speed, which is close to the speed of light, depends on the medium where the signal travels. The signal speed can be calculated from the signal transit time over a feature of known length, such as a wire. Therefore, the distance from a reference point (the end point where calibration has been conducted) to the location of an unknown impedance discontinuity may be calculated by multiplying the speed of the electrical signal by half the measured signal transit time. In this study, signal transit time values are reported directly because locations of features of interest, such as solder joints, are readily identifiable.

The dependent variable, or y-axis, of the time domain plot is the TDR reflection coefficient, which is essentially a ratio of the reflected voltage of the signal sent at a port to that of the transmitted signal from the same port. A solder joint can be characterized by monitoring the reflection coefficient at the solder joint location. As shown in Equation 2, the TDR reflection coefficient (Γ) can range from -1 to 1, which correspond to the impedance values of zero and infinity, respectively. It may be conveniently reported in milliunits (mU).

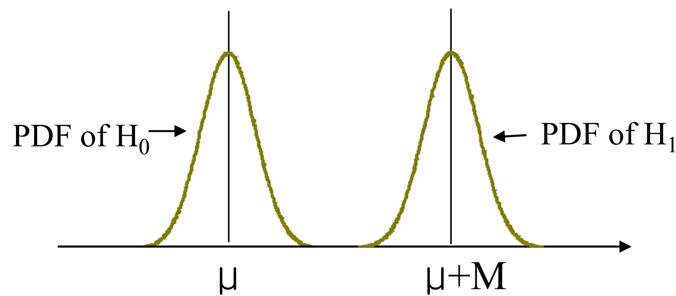
$$\Gamma = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{2}$$

where Z_L and Z_0 denote the impedance of device under test and the characteristic impedance of the circuit, respectively.

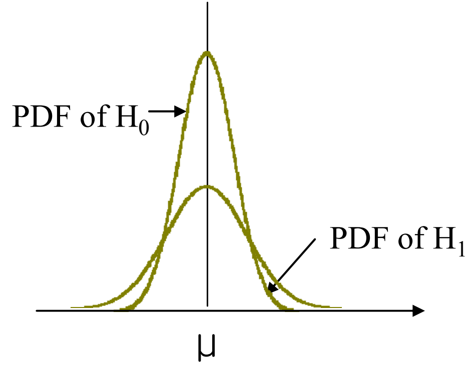
TDR has been found to be an effective method for evaluating impedance discontinuities in transmission lines [18][19], BGAs [20][21], QFPs [22], flip chips [23], and wiring systems [43]. TDR also offers the ability to detect degradation and isolate it at the level of individual solder joints in a daisy chain. For example, during system operation, solder joints in each location may experience different loading conditions, which could result in different levels of degradation. TDR reflection coefficient can be used to diagnose changes in such small structures. In this study, TDR reflection coefficient was used as a measure of RF impedance, and was continuously monitored during interconnect stress testing.

7. *Sequential Probability Ratio Test (SPRT)*

The sequential probability ratio test (SPRT) is a statistical hypothesis test that determines whether the test data falls into the probability density distribution of the training data that serves as a base line [24][25]. The SPRT detects changes in the test data by conducting a statistical test in which null and alternative hypotheses are compared with each other. The null hypothesis represents the normal test data in which the test data adheres to a Gaussian distribution with a mean of zero and a variance of σ^2 extracted from the training data. The following four tests are alternative hypotheses that represent abnormal test data: the positive mean test, the negative mean test, the normal variance test, and the inverse variance test. For the positive or negative mean test, the corresponding alternative hypotheses are that, as shown in Figure 5 (a), the test data adheres to a Gaussian distribution with a mean of $+M$ or $-M$ and a variance of σ^2, respectively, where M is a system disturbance level determined by the user. For the normal or inverse variance test, the corresponding hypotheses are that, as shown in Figure 5 (b), the test data adheres to a Gaussian distribution with a mean of zero and a variance of $V\sigma^2$ or σ^2/V, respectively, where V is a scalar factor related to the detection sensitivity.



(a)



(b)

Figure 5 – Alternative hypothesis tests of SPRT (a) positive mean test, and (b) normal variance test

The positive mean test, for example, evaluates whether the mean of the test data is shifted by *M* in the positive direction, which indicates the test system is degrading. An SPRT index is the logarithmical ratio of the probability that the alternative hypothesis is true to the probability that the null hypothesis is true. Given the null and alternative hypotheses, the SPRT index is

$$SPRT = \frac{M}{\sigma^2} \sum_{k=1}^{n} \left(x_k - \frac{M}{2} \right) \tag{3}$$

where x_k represents sequential observations of the test data.

During the experiment, the SPRT index is continuously calculated and compared to the lower and upper threshold limits, which are set by the user and related to the sensitivity of detection. When the SPRT index is less than the lower threshold, it can be concluded that the test data is normal; when the SPRT index is

greater than the upper threshold, the alternative hypothesis is accepted, which indicates that the test data has become abnormal. Thus, SPRT can help identify statistical anomalies in RF impedance and DC resistance data continuously collected during interconnect stress testing.

Chapter 2:

Early Detection of Interconnect Degradation by Continuous Monitoring of RF Impedance

This chapter describes the procedures to demonstrate the ability of RF impedance in detecting early stages of interconnect degradation, and to quantify the increased sensitivity of RF impedance compared to DC resistance.

1. Interconnect failure precursors under mechanical stress conditions

As shown in Figure 6, a simple test vehicle that contained two solder joints was designed in order to demonstrate the ability of RF impedance to detect early stages of interconnect degradation, and compare it with that of DC resistance measurements made using either a digital multimeter or an event detector. Cyclic mechanical stresses were applied to the solder joints to generate a fatigue failure. Simultaneous monitoring of RF impedance and DC resistance allowed a direct comparison of their respective sensitivities in detecting the physical degradation of solder joints. SPRT was used to quantify the differences in time between the detected failure precursor and the actual failure. Failure analysis of degraded solder joints was conducted to characterize the extent of physical degradation associated with the observed changes of both RF impedance and DC resistance at intermediate stages of solder joint degradation.

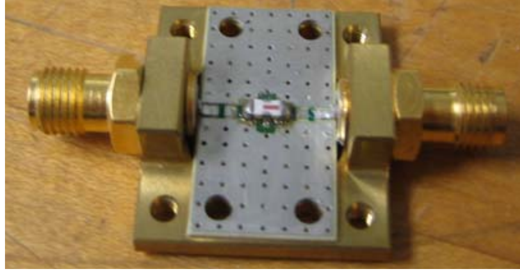


Figure 6 – Test vehicle

1.1 Experimental setup

A test circuit for simultaneous measurement of the RF impedance and the DC resistance was developed as shown in Figure 7. The test circuit consisted of the following: an impedance-controlled circuit board with a surface mount technology (SMT) low pass filter, two bias-tees, RF cables, and measurement instruments. The circuit board had a controlled characteristic impedance of 50 Ohms to match that of the test equipment, cables, and other components. An SMT low pass filter was soldered to this circuit board using eutectic tin-lead solder. The cut-off frequency of the low pass filter was 6.7 GHz. Since the frequency range used in this study was between 500 MHz and 6 GHz, the filter acted as a conductor with the same characteristic impedance of 50 Ohms.

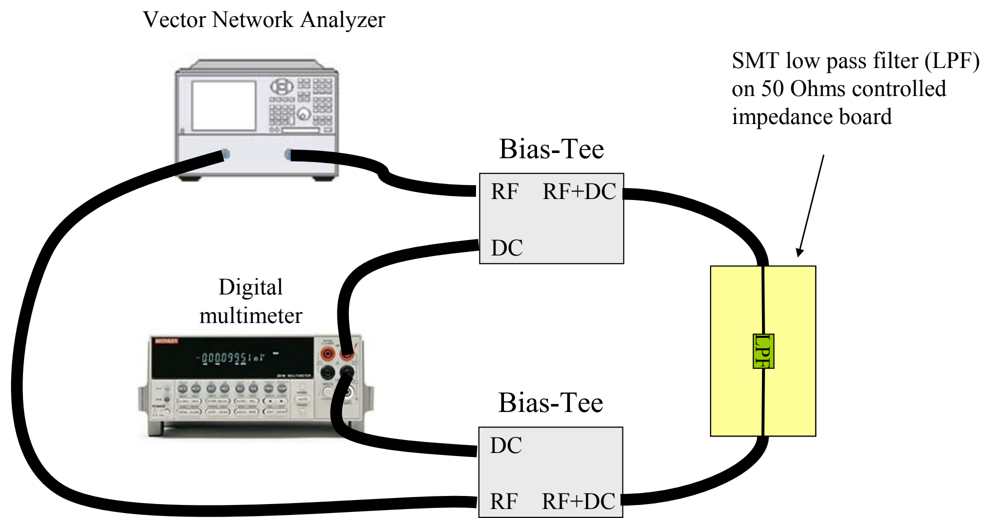


Figure 7 – Schematic of the circuit for simultaneous monitoring of the RF and DC responses

In order to allow simultaneous monitoring of the RF impedance and the DC resistance, bias-tees were incorporated into the test circuit. The bias-tees extracted or combined the RF and DC signals in order to allow for simultaneous monitoring of RF impedance and DC resistance. The DC and the RF measurement instruments were connected to the DC and RF ports of the bias-tees, respectively, while the composite ports were connected to both ends of the circuit board. All connections were made using RF cables which also had a characteristic impedance of 50 Ohms.

A Keithley 2010 7.5-digit multimeter and an Agilent E8364A vector network analyzer (VNA) were used to monitor the DC resistance and the RF impedance, respectively. The VNA had a frequency range of 45 MHz to 50 GHz and was configured with TDR functionality. Both instruments were externally monitored to allow automated data acquisition.

An MTS Tytron 250 was used to apply a cyclic shear force to the solder joint in order to generate fatigue failures. The MTS Tytron 250 is a uniaxial micro-tester that has a load capacity of 250 N and a load resolution of 0.001 N. According to the user's needs, various load profiles can be programmed, e.g., a cyclic shear force to generate fatigue failure or a monotonic increasing force to measure the strength of a material. The programmed force can be monitored along with the displacement, which provides the force and displacement profiles during stress testing. A strip of alumina was inserted between the metal tip of the force transducer and the component to avoid electrical connection at the contact.

1.2 Validation of electrical measurements during stress testing

RF impedance is sensitive to electromagnetic interference generated by electronic equipment around the device under test. In addition, the application of a mechanical load may affect the RF impedance measurements due to the mechanical contact between the load transducer and the component. Therefore, in order to evaluate the effect of any electromagnetic interference on the RF impedance and DC resistance measurements, the RF impedance and DC resistance were measured under three test conditions, as shown in Table 1. The three test conditions were the combinations of the operation status of the Tytron 250 and the application of load to the component. Three measurements for each condition were taken to ensure repeatability of the test results. The tests showed that the variations among the conditions were less than one percent, which verified that operation of the Tytron 250

did not introduce any measurable electrical noise into the RF impedance or DC resistance.

Table 1 – Test matrix to evaluate the effect of Tytron 250 operation

	Test conditions		
	1	2	3
Tytron 250 status	Off	Off	On
Application of load	No	Yes	Yes

1.3 Load profile design

In order to determine an appropriate force level for the fatigue tests, the shear strength of the solder joint was measured using the same test vehicles described earlier. A monotonically increasing shear force was applied to the component at a displacement rate of 0.5 mm/s until the solder joints failed. In the experiment, however, the failure mode was pad lifting from the circuit board, rather than cracking of the solder joints. In order to avoid pad lifting during the shear strength measurement, the SMT component was soldered to the ground plane of the same circuit board and the measurements were repeated. The shear strength of the solder joint was identified to be about 125 N, averaged over multiple trials.

Based on the shear strength measurement and several tests under various load levels, an offset force of 30 N and an oscillatory force of 10 N at a frequency of 0.25 Hz were chosen to produce fatigue cracking of the solder joints of the test vehicle. As a result, the cyclic shear force varied between 20 N and 40 N in a sinusoidal wave

form within a period of four seconds as shown in Figure 8. The offset force maintained the contact between the component and the force transducer throughout the entire fatigue cycle, and the oscillatory force corresponded to the amplitude of the sinusoidal force superimposed on the offset force.

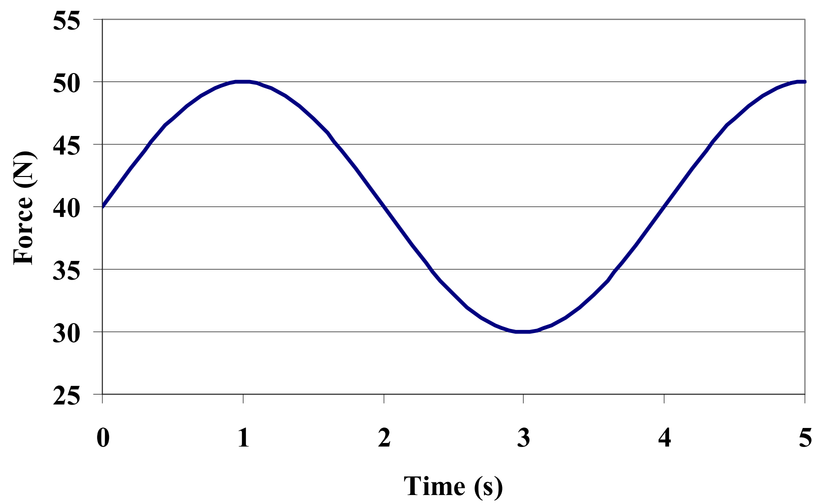


Figure 8 – Cyclic shear force profile

1.4 RF and DC data acquisition

Both the RF and the DC responses were collected every 30 seconds. Instrumental control software was used to instruct the multimeter to collect the DC resistance measurements periodically. At the same time, the TDR reflection coefficients over the entire time domain of the test circuit were collected as a measure of RF impedance. One set of TDR measurement data contained the multiple reflection coefficient values of the part of the signal path defined by the user. In order to compare to the DC resistance measurements, the TDR reflection coefficients at the

solder joint were extracted and displayed in one plot. Each experiment was conducted until it resulted in a DC open circuit or until the TDR reflection coefficient increased significantly.

1.5 TDR reflection coefficient measurement

The TDR reflection coefficients at particular locations of interest were extracted from the overall time domain plot. Figure 9 shows two measurements of the TDR reflection coefficients over the signal transit time domain: one taken prior to the application of the cyclic stress and the other after completion of a fatigue test. The physical locations corresponding to the peaks were identified experimentally through association with known features in the circuit. The change in amplitude of the peak was a result of an increase in impedance at the failure site, which was visually confirmed to be a cracked solder joint.

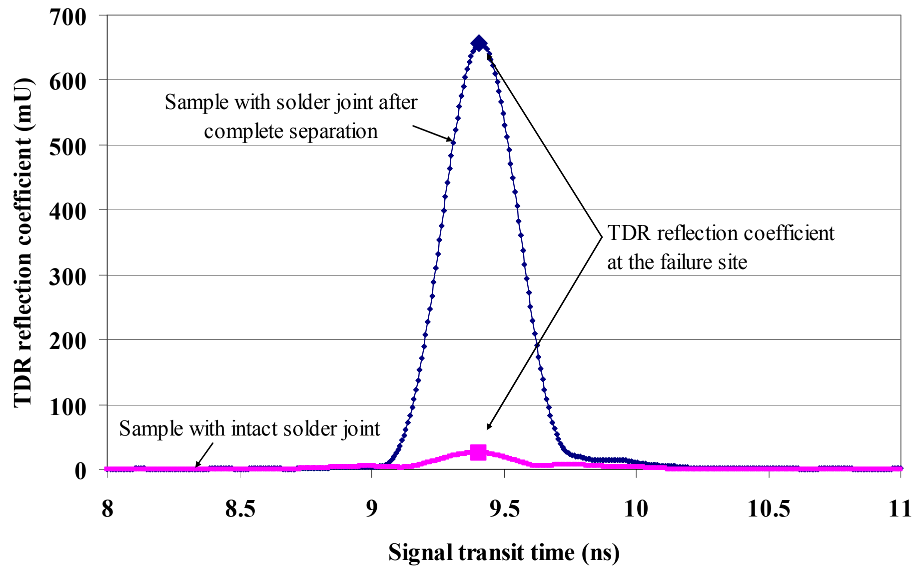


Figure 9 –TDR response before and after a fatigue test

1.6 Comparison between RF impedance and DC resistance

Figure 10 shows the results of one such fatigue test experiment, which compares the TDR reflection coefficient at the failure site with the DC resistance. The total duration of this test was about 1303 minutes. Both the TDR reflection coefficient and the DC resistance were collected every 30 seconds until the applied stress resulted in a DC open circuit. The SPRT was applied to both the TDR reflection coefficient and the DC resistance individually. The data points from 0 to 200 minutes of each parameter in a test were taken for the training data, respectively.

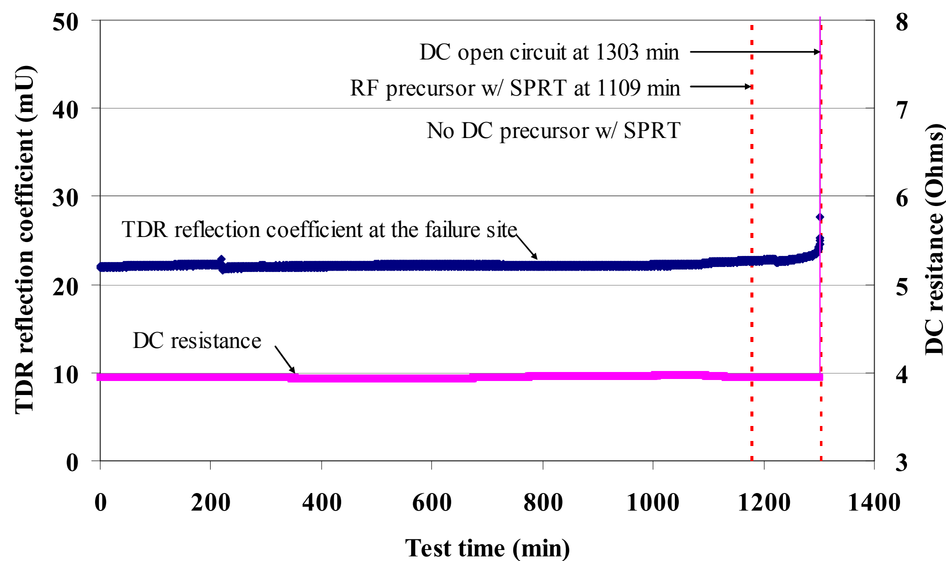


Figure 10 – Comparison between RF and DC responses with their failure precursor detections using SPRT during a fatigue test

At the beginning of the test, both measurements remained close to their initial values. SPRT detected an RF failure precursor, a gradual non-linear increase in the TDR reflection coefficient, at 1109 minutes, 194 minutes prior to the DC open circuit,

which signaled separation of the solder joint. This precursor corresponded to about 15% remaining life, considering the entire test time at which the solder joints were separated. On the other hand, the DC resistance remained almost constant until it exhibited a sudden increase, indicating a DC open circuit. However, SPRT triggered alarms between 718 and 1179 minutes. These were identified to be the effect of a diurnal variation that resulted from the changes in the ambient temperature. Analysis of the data showed that no DC failure precursors were observed by SPRT prior to failure of the solder joint.

Table 2 shows a summary of other test results with prognostic distance calculations. In every case, the SPRT detected RF failure precursors prior to the separation of the solder joints; while no DC failure precursors were observed. The prognostic distances show a little variation depending on a few test conditions that were not controlled such as the amount of solder and the solder fillet shape. These experiments confirm that the test results were qualitatively repeatable.

Table 2 – Summary of fatigue test results with prognostic distance calculations

Test	Time to DC open circuit (min)	RF failure precursor (min)	Prognostic distance	
			(min)	(%)
1	337	335	2	0.59
2	1303	1103	200	15.35
3	1210	1041	169	13.97
4	974	826	148	15.20
5	431	415	16	3.71

6	407	253	154	37.84
7	866	503	363	41.92
8	1557	1504	53	3.40
9	574	430	144	25.09
10	411	408	3	0.73
11	3633	3612	21	0.58

1.7 Failure analysis of degraded solder joint

Figure 11 shows the result of another fatigue test comparing the TDR reflection coefficient with the DC resistance. As observed in the previous result, both the DC and the RF responses remained around their initial values at the beginning of the test, but the TDR reflection coefficient began to increase as the solder joints were stressed. In order to investigate the physical degradation of the solder joint, which was responsible for the RF impedance changes, the test was stopped after 308 minutes of operation when the TDR reflection coefficient showed about a 4 milliunit (mU) increase from its initial value. This partially degraded solder joint sample was used to relate the failure mechanism and the extent of damage to the RF impedance changes.

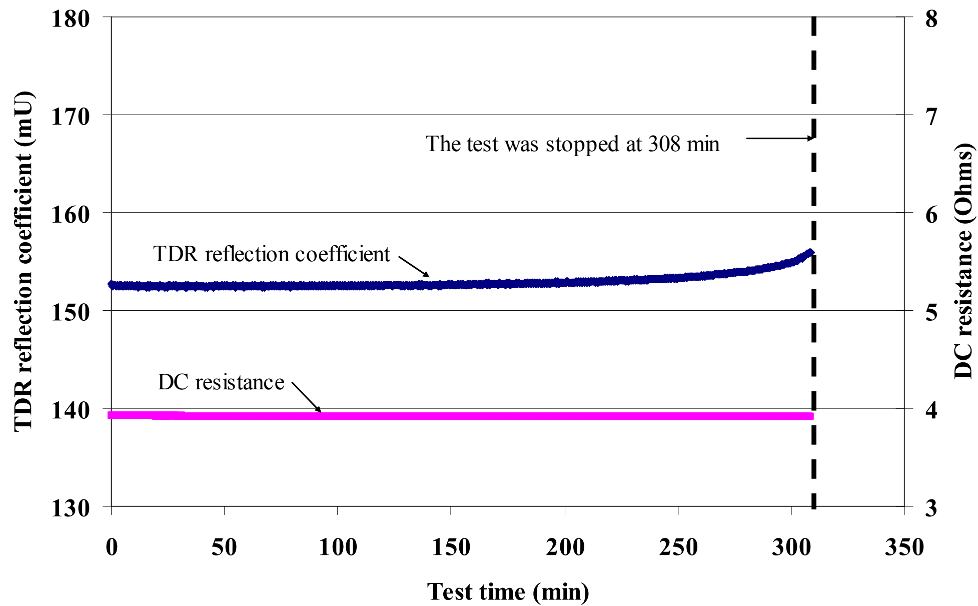


Figure 11 – Comparison between RF and DC responses during a fatigue test

After the test, the circuit board was initially inspected under the scanning electron microscope (SEM) to locate any damage to the solder joints. The SEM revealed an externally visible crack in the solder joint along the interface between the component and the copper pad on the circuit board. The sample was potted in epoxy and cross-sectioned to reveal the cracked solder joint on a plane orthogonal to the long axis of the filter, as shown in Figure 12.

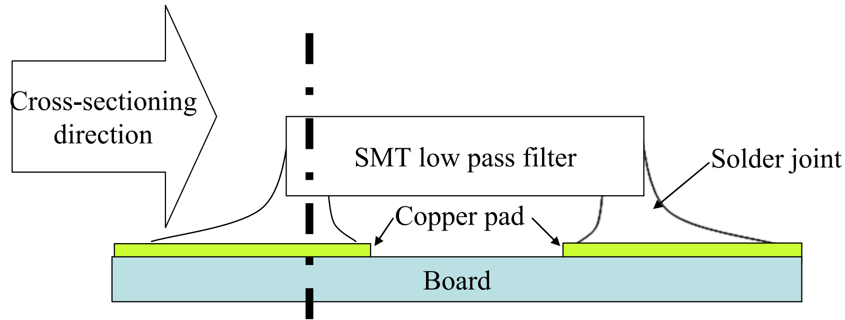
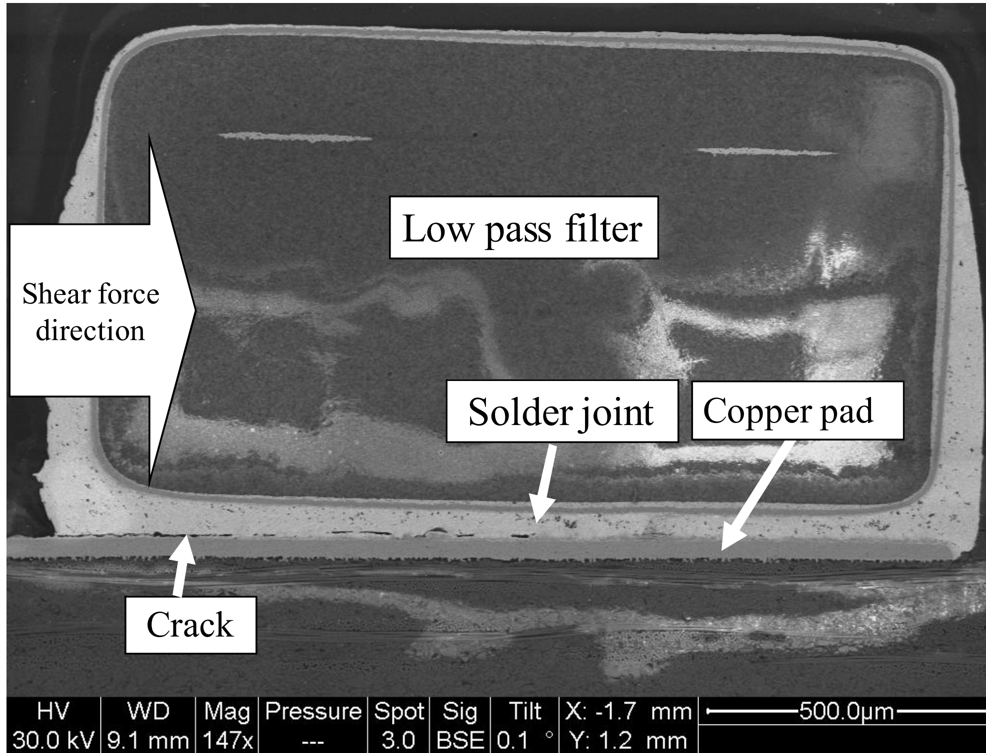
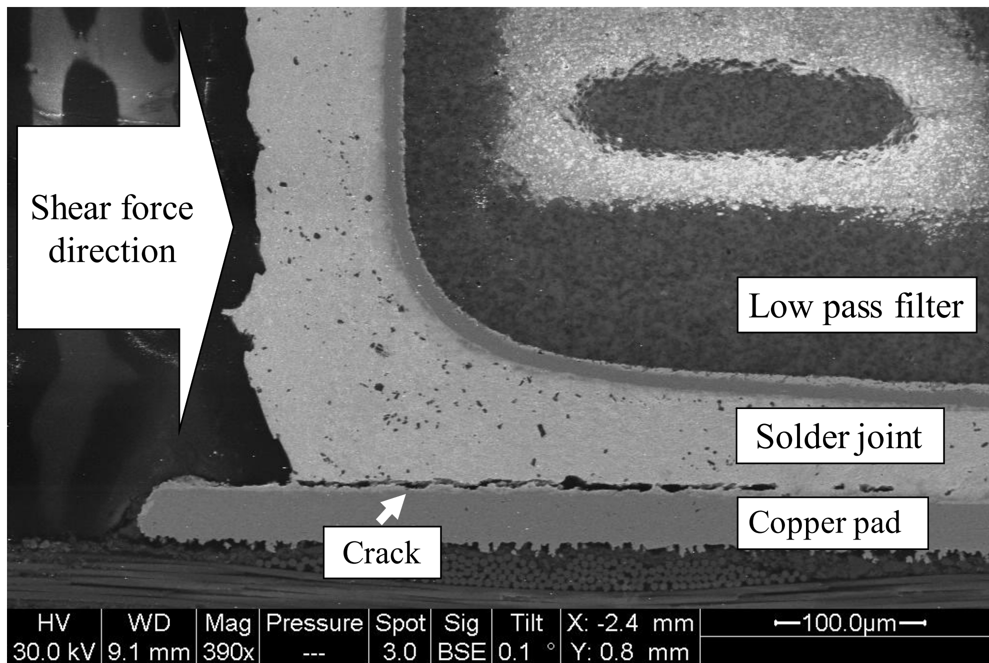


Figure 12 – Cross-sectioning direction and plane of observation

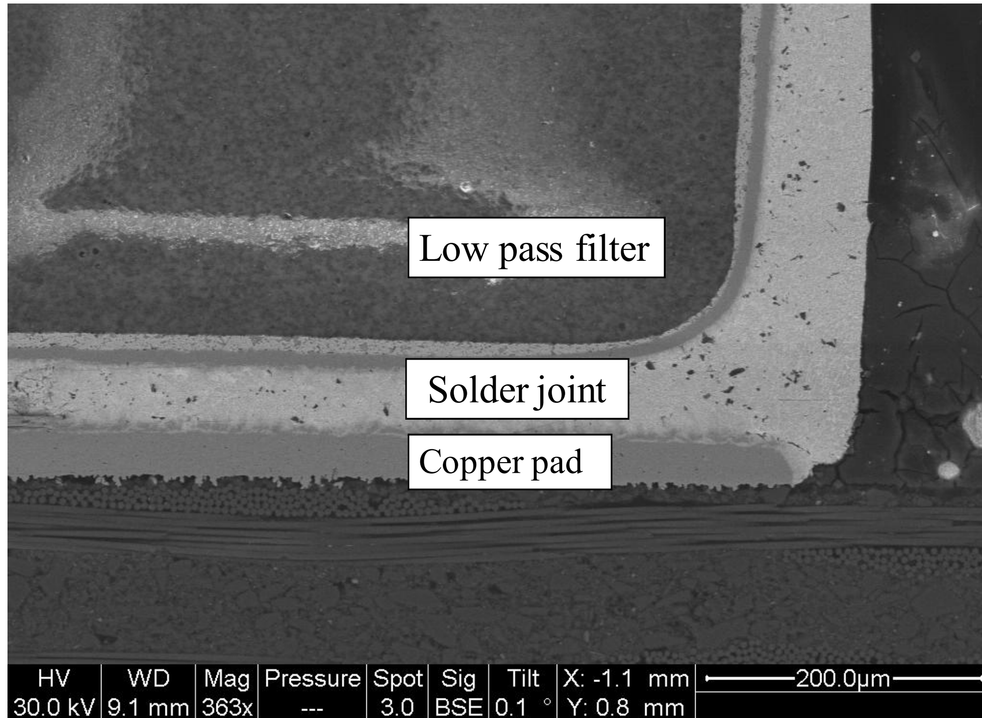
Figure 13 shows several cross-sectional SEM images of the degraded solder joint. A crack, which initiated at the surface and propagated inward, may be clearly observed in Figure 13 (a). The crack has opened on the side of the solder joint where the shear force was applied, and propagated towards the center, consistent with the direction of the applied shear force, as seen at higher magnification in Figure 13 (b). On the other hand, the opposite side of the solder joint was still intact, as shown in Figure 13 (c) with the possible exception of a micro-crack near the outside corner of the copper pad.



(a)



(b)



(c)

Figure 13 – Cross-sectional SEM images of component and solder joint (a) overview (b) left hand side close-up, and (c) right hand side close-up

Analysis of the figures revealed that the total crack length was about 700 micrometers, which is much greater than the skin depth under the given conditions. By this time in the fatigue test, the TDR reflection coefficient had increased by 4 mU, about 3% of the initial TDR reflection coefficient, but the DC resistance remained at its initial value. This provides clear evidence that RF impedance is more sensitive than DC resistance in detecting interconnect degradation due to the skin effect. Other experiments confirmed that these test results were qualitatively repeatable, though the

actual values of the initial TDR reflection coefficient and the DC resistance were slightly different, depending on the size and shape of the solder fillet.

1.8 Comparison with event detectors

The electronics industry has long been using event detectors and data loggers to detect intermittent behavior of solder joint resistance under loading conditions [26]. Paired with measurements taken using event detectors or data loggers, the IPC-SM-785 standard is widely used in the electronics industry to define the criteria for solder joint failure during reliability or qualification testing of electronics [10]. An event is defined to be a loss of electrical continuity where the resistance of the circuit exceeds a threshold resistance (R_{th}), which is also defined by the standard. The standard defines a failure as the first event (t_0) associated with the loss of electrical continuity, if it is followed by nine additional events within an additional 10% of the lifetime ($t_0+0.1t_0$) as shown in Figure 14. The loss of electrical continuity of a solder joint typically occurs when a crack within the solder joint is large enough to result in an instantaneous open circuit. Because of their rapid sampling rate, event detectors are also widely believed to be the best means of detecting a crack under cyclic or transient loading conditions. Nevertheless, event detectors may not be useful for detecting early stages of solder joint degradation, since the resistance increase associated with a partial crack would not be large enough to trigger an event.

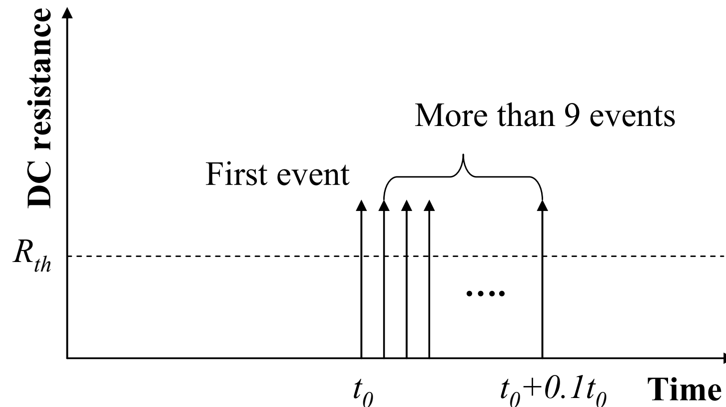


Figure 14 – Schematic representation of failure definition according to IPC-SM-785

In order to continuously monitor the DC resistance of the solder joints and compare it with the RF impedance, an event detector was incorporated into the test circuit in place of the digital multimeter as shown in Figure 15, and configured to have a threshold resistance of 300 ohms according to the IPC-SM-785 standard [10]. The effect of the high frequency signals and the RF components on the event detector measurement was evaluated to determine whether the event detector might be affected by the signals of a few gigahertz or the bias-tees. By introducing an electrical discontinuity into the test circuit, it was confirmed that the operation of the event detector was not influenced by the high frequency signals and components which had been used in the fatigue tests shown in the previous section.

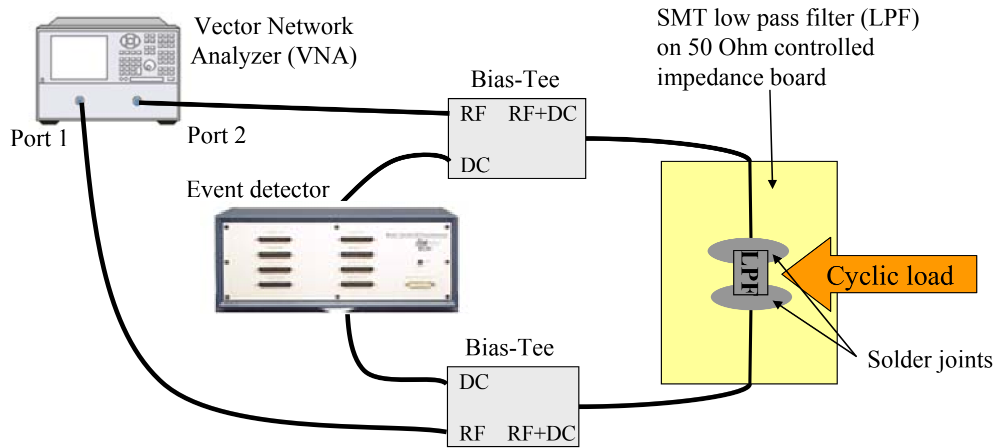


Figure 15 – Fatigue test schematic for comparison between RF impedance and event detectors

In a fatigue test, the event detector results were polled out once per second and displayed in a plot together with the TDR reflection coefficient. The output value from the event detector was either zero or one, which indicated a short or an open circuit, respectively. Figure 16 shows the result from a fatigue test conducted with an event detector. SPRT detected an RF failure precursor at 1599 minutes, providing early sensitivity of 535 minutes. The event detector did not catch any transitional DC open states until 2134 minutes at which time the test was stopped and the solder joint separation was observed.

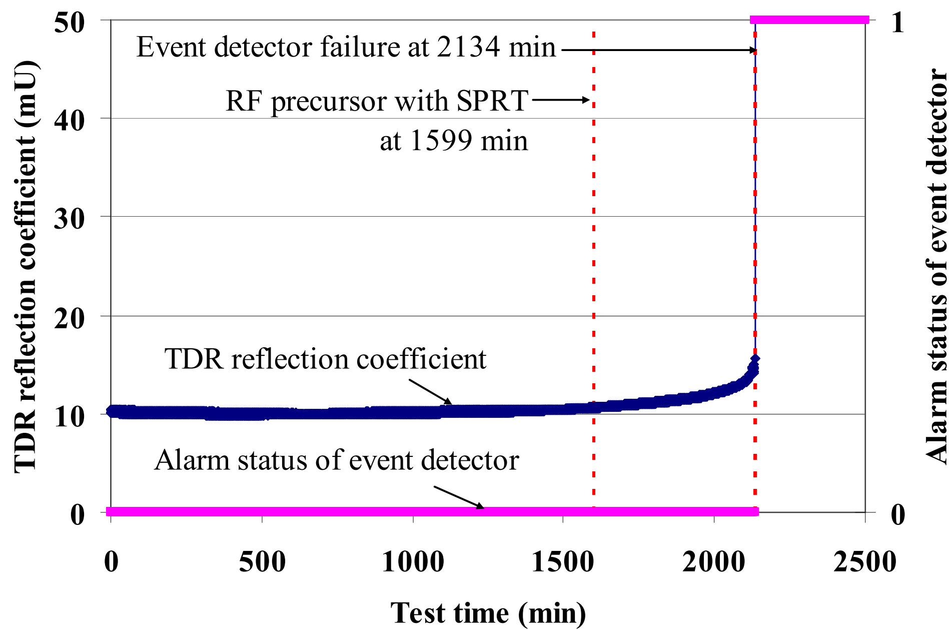


Figure 16 – Comparison between RF impedance and event detector during the fatigue test

This test result shows that, even at the relatively low monitoring frequency of once every 30 seconds, RF impedance detects interconnect degradation earlier than DC resistance. It also demonstrates that RF impedance can serve as a better reliability monitoring tool than an event detector. In spite of the continuous high speed sampling of the event detector, it failed to provide early warning prior to RF impedance. Although the time to TDR reflection coefficient increase and time to failure varied from sample to sample, the early sensitivity of RF impedance compared to event detectors was consistently observed over multiple trials.

1.9 Summary

The applicability of RF impedance in detecting early stages of interconnect degradation has been presented under mechanical loading conditions. A test vehicle was developed to allow direct comparison of RF and DC measurements during cyclic loading of a surface mount component. It was shown that the combination of an impedance controlled board with an SMT low pass filter and two bias tees was an appropriate test vehicle for monitoring RF and DC responses simultaneously. Also, the TDR reflection coefficient was found to be a useful parameter for monitoring circuit impedance changes in order to diagnose interconnect degradation. Since at high operating frequencies signal propagation is concentrated in the circumferential region of a conductor, a crack that initiates at the surface raises the RF impedance, thus causing an increase in the TDR reflection coefficient. As a result, the TDR reflection coefficient serves as a dependable indicator of interconnect degradation. It was shown that a 4 mU increase of the TDR reflection coefficient resulted from a crack extending about halfway across the solder joint of a 1206 component, when monitored using the frequency range of 0.5 to 6 GHz.

2. Interconnect failure precursors under thermo-mechanical stress conditions

This section demonstrates the ability of RF impedance in detecting early stages of interconnect degradation under thermo-mechanical loading conditions. The

reflection coefficient obtained from time domain reflectometry (TDR) as a measure of RF impedance was continuously monitored during degradation of the solder joints subjected to constant shear force at an elevated temperature. SPRT was used to detect failure precursors in the TDR reflection coefficient and thus to calculate the prognostic distance.

2.1 Experimental setup

A test circuit was prepared to simultaneously monitor the TDR reflection coefficient and DC resistance during creep testing, as shown in Figure 17. The test circuit consisted of an impedance-controlled circuit board, two bias-tees, a Wheatstone bridge, a vector network analyzer, and several RF cables that connected these elements to each other. The circuit board contained two eutectic tin-lead solder joints that provided both mechanical and electrical connections between the board and a surface mount technology (SMT) low pass filter. The bias-tees combined and extracted the RF and the DC signals in order to allow for simultaneous monitoring of TDR reflection coefficient and DC resistance. The Wheatstone bridge and the vector network analyzer were connected with the DC and the RF ports of the bias-tees, respectively, and thus, measured the DC resistance and the TDR reflection coefficient at the solder joint.

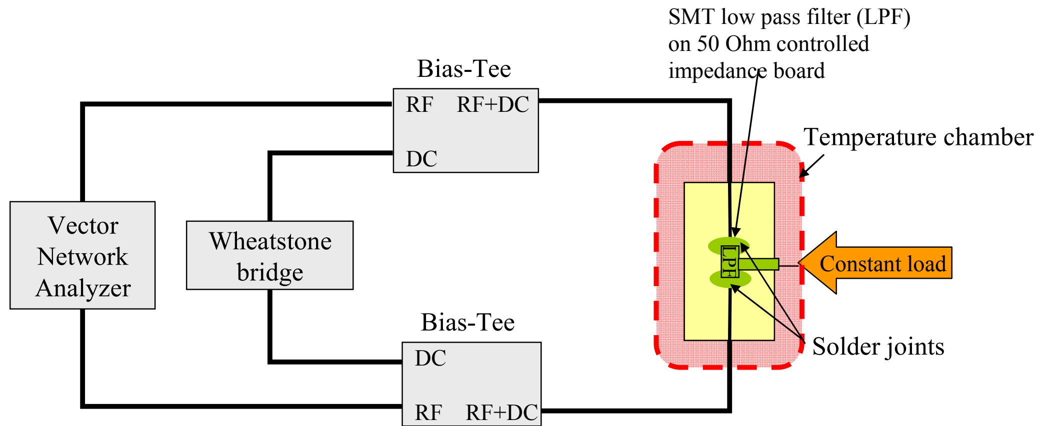


Figure 17 – Creep test schematic for comparison between RF impedance and DC resistance

In order to measure DC resistance, a Wheatstone bridge was used in this testing, as shown in Figure 18. Bridge circuits are commonly used to measure resistance, capacitance, and inductance [27]. The Wheatstone bridge is a resistive bridge that produces an output in the form of a voltage level that varies as the resistance changes. The Wheatstone bridge provides accurate resistance measurement, which enables the detection of small changes from a nominal value. The four arms of the bridge consist of three equal resistors, R_1, R_2, and R_3, and the DUT, R_u. As the resistance of the DUT changes, the output voltage between the nodes B and C, V_0, varies. Therefore, the resistance of the DUT can be measured with improved resolution by monitoring the output voltage, V_0, during creep testing.

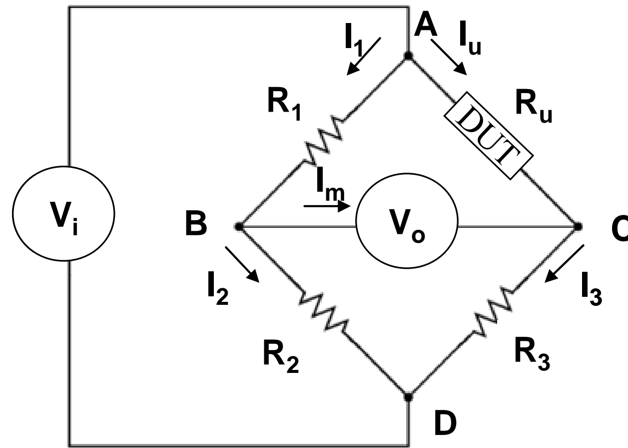


Figure 18 – Wheatstone bridge used to measure DC resistance

An MTS Tytron 250 was used to apply a constant load to the solder joints and to control the temperature of the chamber in which the test circuit board was placed during creep testing. A Keithley 2010 digital multimeter and an Agilent E8364A vector network analyzer were used to monitor the output voltage of the Wheatstone bridge and the TDR reflection coefficient, respectively. Both instruments were externally controlled to allow automated data acquisition.

2.2 Test conditions

A constant mechanical shear force of 10 N at an elevated temperature was applied to the low pass filter in order to generate creep failures of the solder joints. The test circuit board was put in a temperature chamber where the temperature was held at 125 °C during creep testing. The homologous temperature was calculated to be 0.87 for eutectic tin-lead, which was high enough to expect creep failures. The shear force maintained the contact between the force transducer and the low pass filter throughout the entire test until the solder joint was ruptured by creep. A ceramic

material was inserted to prevent electrical noise due to physical contact between the metal tip of the force transducer and the low pass filter.

The monitored frequency range for the TDR reflection coefficient was chosen to be 500 MHz to 6 GHz, which was consistent with the frequency range for mechanical stress testing. For the TDR reflection coefficient measurement, the network analyzer swept across the frequency range defined above and collected the reflection coefficients over the frequency domain. It then applied an inverse Fourier transform to the frequency domain measurement results and obtained the time domain measurement results.

Instrumental control software was used to instruct the multimeter and the vector network analyzer to collect the output voltage of the Wheatstone bridge and the TDR reflection coefficient, respectively, every 30 seconds. The collected output voltages were converted into DC resistances using the relationship among the bridge elements. Each set of TDR measurement data contained a set of reflection coefficient values over the partial signal path of the circuit board collected at a particular instant during a creep test. In order to monitor changes to the interconnect over time and allow comparison with DC resistance, the TDR reflection coefficients at the location of a specific solder joint were extracted and displayed in a plot as a function of test duration. During each experiment the TDR responses and the output voltages were simultaneously monitored until the thermo-mechanical stresses resulted in a DC open circuit.

In order to identify solder joint failure precursors, SPRT was applied to both the TDR reflection coefficient and the DC resistance, individually. It was assumed

that the data points from 0 to 200 minutes of each parameter in a test represented the responses from a non-degraded solder joint, and thus these data points were taken for the training data, respectively. In order to reduce the effect of measurement noise on the test data, at least five consecutive detections were considered as a real deviation due to degradation.

2.3 Comparison between RF impedance and DC resistance

Creep tests were conducted in order to identify solder joint failure precursors under thermo-mechanical stress conditions. Most tests were concluded when the DC resistance exhibited a sudden increase, indicating a complete separation of the solder joint. Until then, the TDR reflection coefficient and the DC resistance were simultaneously monitored and displayed together. Figure 19 shows the results of a creep test. The total duration of the test was 503 minutes, at which a DC open circuit was observed. In the beginning of the test, both the TDR reflection coefficient and the DC resistance remained around their initial values. However, as the test progressed, the TDR reflection coefficient gradually increased in response to the mechanical degradation of the solder joints, while the DC resistance remained constant despite the high sensitivity of the Wheatstone bridge.

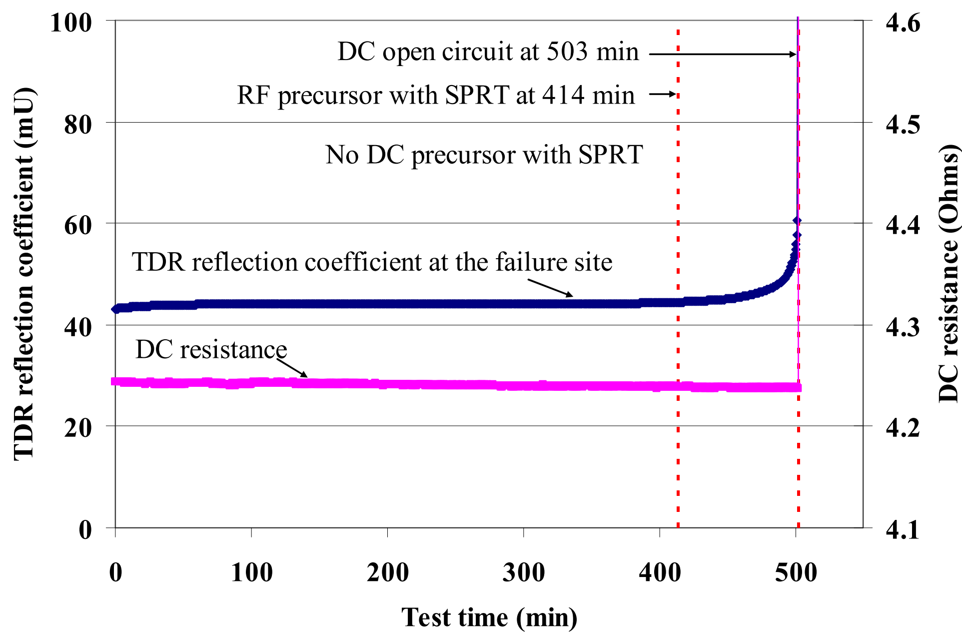


Figure 19 – Comparison between RF and DC responses with their failure precursor detections using SPRT during a creep test

The prognostic distances for the TDR reflection coefficient and the DC resistance were calculated in order to quantify their respective sensitivities in detecting early stages of solder joint failure. In the creep test shown in Figure 19, SPRT detected deviation of the TDR reflection coefficient at 414 minutes, which resulted in a prognostic distance of 89 minutes, equivalent to 18 % of the total lifetime. Meanwhile, SPRT did not detect any deviation in the DC resistance until the solder joint failed.

Table 3 shows a summary of several creep test results with prognostic distances of RF impedance. In every case, SPRT detected the failure precursors of the TDR reflection coefficients prior to the separation of the solder joints, while no failure precursors of the DC resistance were observed. The prognostic distances

showed a little variation depending on a few test conditions that were not controlled, such as the amount and shape of the solder fillets. These experiments confirm that the test results were qualitatively repeatable in general.

Table 3 – Summary of creep test results with prognostic distances calculations

Test	Time to DC open circuit (min)	RF failure precursor (min)	Prognostic distance	
			(min)	(%)
1	503	414	89	18
2	962	898	64	7
3	377	267	110	29
4	236	209	27	11
5	429	418	11	3

2.4 Failure analysis of degraded solder joint

Figure 20 shows another creep test result comparing the TDR reflection coefficient and the DC resistance over the test time. As described in the previous section, both responses remained around their initial values at the beginning of the test, but the TDR reflection coefficient showed a gradual increase as the solder joints were stressed. In order to examine whether this increase was caused by physical cracking within the solder joint, the creep test was stopped at 841 min when the TDR reflection coefficient showed an increase of approximately 16 mU from its initial value. This partially degraded sample was potted in epoxy and cross-sectioned on a plane orthogonal to the long axis of the filter, as shown in Figure 21.

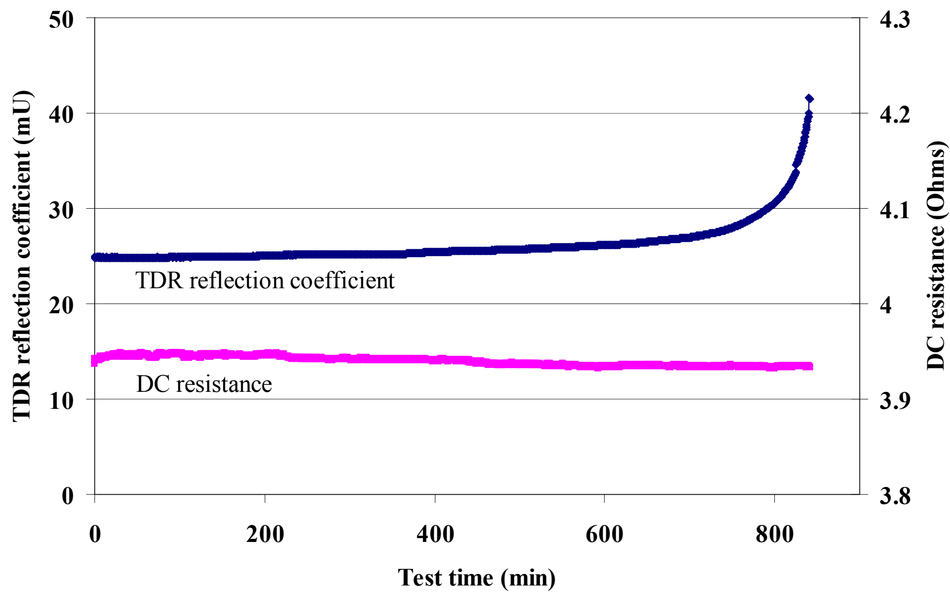


Figure 20 – Comparison between RF and DC responses during a creep test

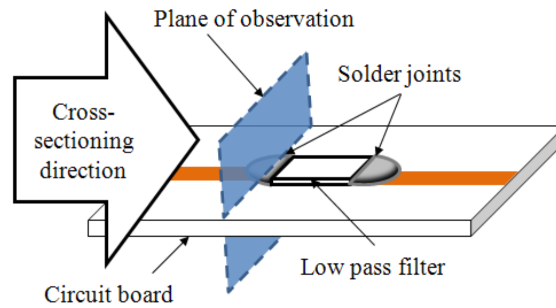


Figure 21 – Cross-sectioning direction and plane of observation

Figure 22 shows a scanning electron microscope (SEM) image taken after cross-sectioning. The image revealed that a partial crack initiated at the side where the shear force was applied and propagated towards the center, which coincided with the direction of the applied shear force. This partial crack was responsible for the changes in the TDR reflection coefficient, and, therefore, produced a gradual RF

impedance increase as the crack propagated further towards the interior. On the other hand, the opposite side of the solder joint was still intact, which provided an adequate signal path for the DC current to travel through. The change in the TDR reflection coefficient and the corresponding partial crack were observed from other degraded samples over multiple trials, though the actual values of the initial TDR reflection coefficient and the DC resistance varied depending on the size and shape of the solder fillet.

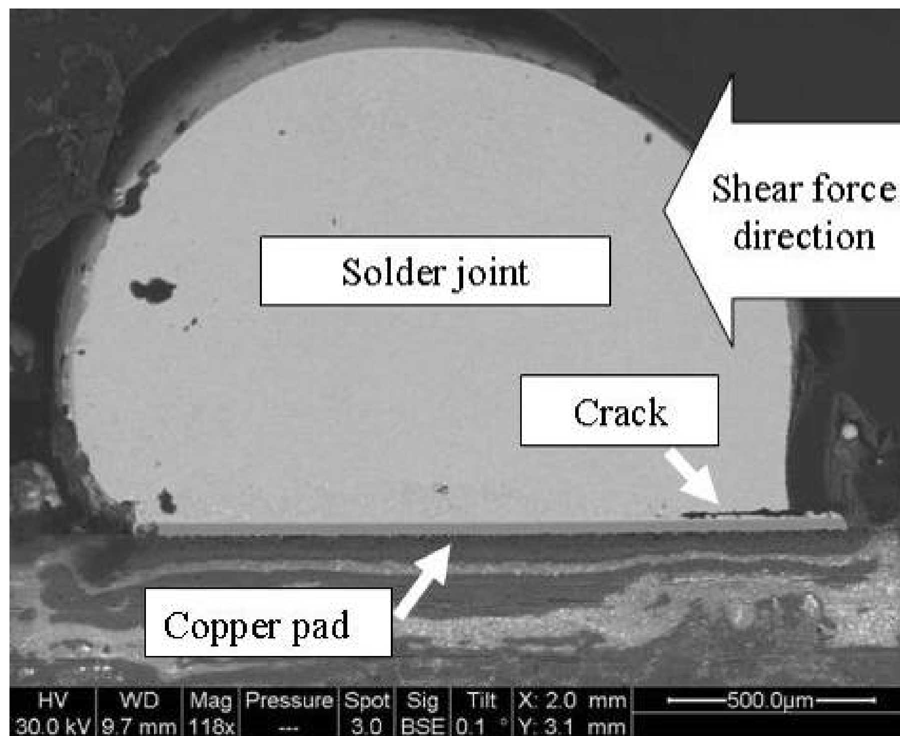


Figure 22 – Cross-sectional image of a partially degraded solder joint

2.5 Evaluation of the effect of different solder alloys

In order to examine the effect of different solder alloys on changes in RF impedance as the solder joint degraded, lead-free SAC305 (Sn3.0Ag0.5Cu) alloy,

which is widely used by the electronics industry, was used to solder the test board. The test boards were then subjected to creep testing with simultaneous monitoring of the TDR reflection coefficient and the DC resistance.

Using Equation 1, the skin depth for both eutectic tin-lead and SAC305 solder alloys can be calculated as shown in Figure 23. The monitored frequency range was chosen to be consistent with previous interconnect stress testing, 500 MHz to 6 GHz. The homologous temperature was calculated to be 0.81 for SAC305, which was high enough to expect creep failures. The shear force maintained the contact between the force transducer and the component throughout the entire test until the solder joint was ruptured by creep.

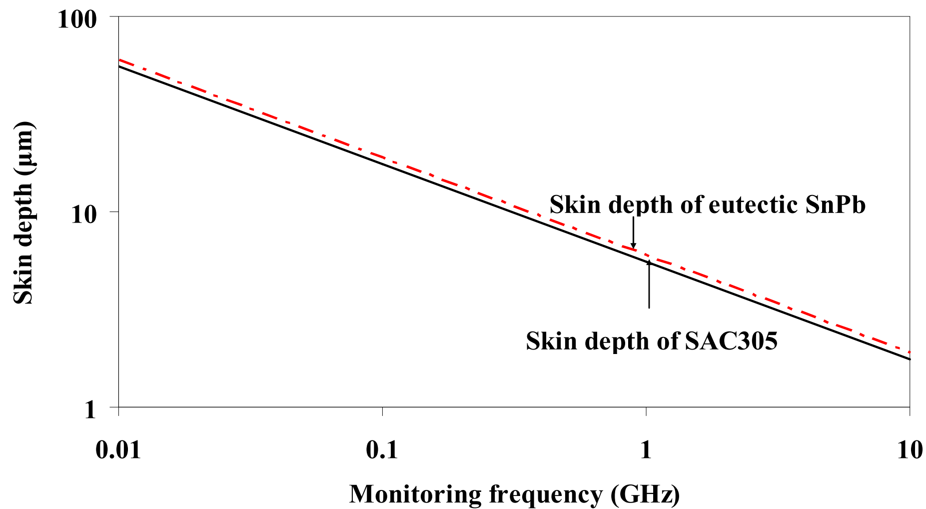


Figure 23 – Comparison between skin depths of eutectic SnPb and SAC305 over frequency

Figure 24 shows a creep test result conducted on SAC305 solder joints. Since the total duration of a test depended on the initial conditions such as the amount of solder, the responses during the last 500 minutes were provided to show the changes at the end of the test clearly. The gradual increase of the TDR reflection coefficient, which was observed towards the end of the test for the SAC305 solder joints, was similar to that observed in the tin-lead solder joint case. In general, the same behavior of the TDR reflection coefficient was observed from the creep tests with both solder joints, although the initial conditions varied from sample to sample. Thus, regardless of which solder is used, RF impedance consistently provides interconnect failure precursors under thermo-mechanical loading conditions.

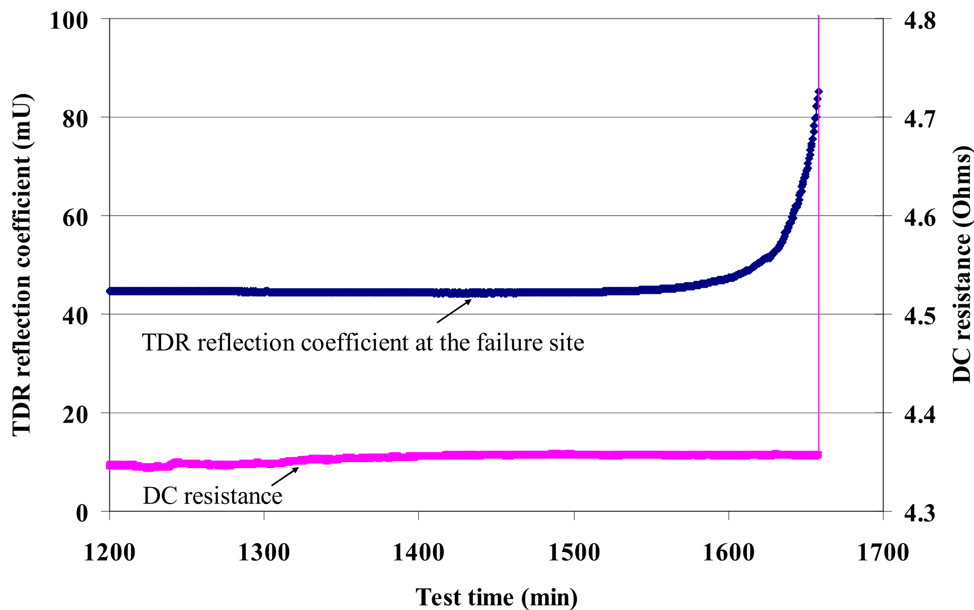


Figure 24 – TDR reflection coefficient and DC resistance during a creep test on a SAC305 solder joint

2.6 Summary

The ability of RF impedance analysis to provide interconnect failure precursors during thermo-mechanical loading has been demonstrated for two different solder alloys. The solder alloys investigated included eutectic tin-lead and SAC305 lead-free solder, which are widely used by the electronics industry. It was shown that regardless of the solder alloy, the TDR reflection coefficient provided interconnect failure precursors under thermo-mechanical loading conditions, while the DC resistance did not show any indications of degradation until complete solder joint separation. Failure analysis revealed that a partial crack within a degraded solder joint was responsible for the increase of the TDR reflection coefficient. Therefore, RF impedance can serve as a dependable indicator of interconnect degradation, allowing prediction of impending failure prior to loss of DC continuity.

3. Comparison of the relationship of changes in RF impedance to solder joint crack length

It has been shown that RF impedance responds early stages of interconnect degradation. This section analytically investigates the relationship between changes in RF impedance and DC resistance to crack length within a solder joint using the equivalent circuit model. The respective sensitivities of RF impedance and DC resistance were analytically compared by varying the length of a crack within a solder joint.

3.1 Transmission line model for a solder joint

The test circuit was considered as a transmission line, which is often represented schematically as a two-wire line. A transmission line can consist of a few lumped-element circuits with circuit elements of *L*, *C*, *R*, and *G*, where *L* represents the total self-inductance per unit length of the two conductors, *C* represents the shunt capacitance per unit length due to the close proximity of the two conductors, *R* represents the resistance per unit length due to the finite conductivity of the conductors, and *G* represents the shunt conductance per unit length due to the dielectric loss in the material. A solder joint can be modelled as a lumped-element circuit with circuit elements of L_1, R_1, and C_1 under an assumption that there is no dielectric loss between the signal and the ground plane, as shown in Figure 25.

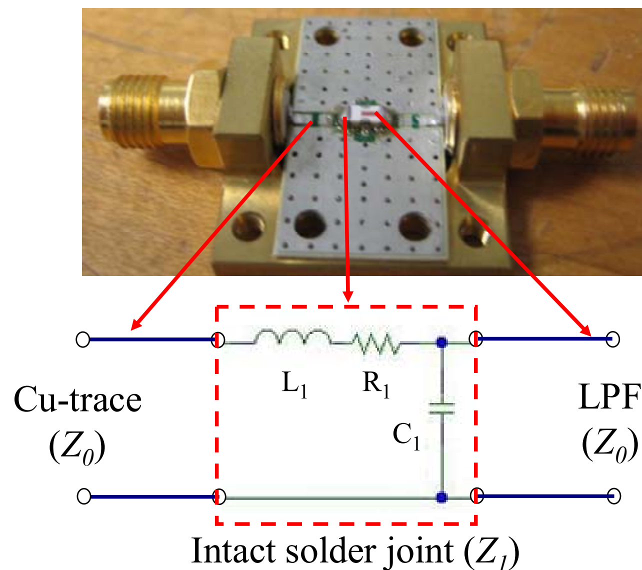


Figure 25 – Equivalent circuit of an intact solder joint

3.2 Equivalent circuit model for solder joint cracking simulation

Lando [28] developed an equivalent circuit model that can calculate changes in the RF impedance and the DC resistance of a solder joint as a function of crack length. Figure 26 shows a geometrical representation of a solder joint and a crack within the solder joint. Solder joint cracking was represented as reduction of the solder joint width (*d*) with a constant crack height (*h*) from the bottom. Solder joint cracking changes the impedance of the solder joint, and therefore the circuit elements of the transmission line. In order to simulate crack propagation, the crack length (*x*) varied from zero, corresponding to an intact solder joint, to the solder joint width (*d*, a full crack) and was proportional to the reduction of the cross-sectional area for signals to flow. According to the equivalent circuit model, the RF impedance and the DC resistance affected by the crack were expressed in the terms of the crack length as shown in Equation 4 and Equation 5, respectively.

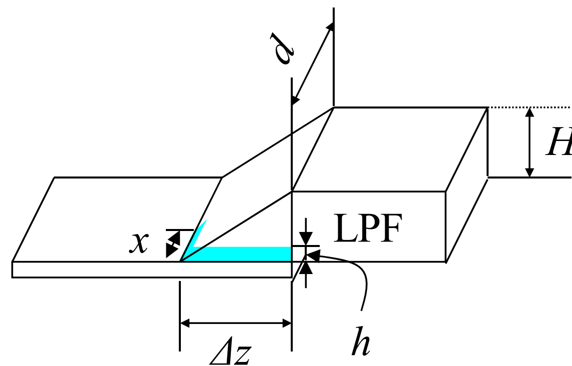


Figure 26 – Geometrical representation of solder joint cracking

$$Z_{eq}(x) = \left[\frac{L_1}{C_1 \Delta z} \left(\Delta z + \frac{hx^2}{dh - 4\pi^2 f^2 \varepsilon_r \varepsilon_0 \Delta z L_1 x^3} \right) \right]^{1/2} \tag{4}$$

where Δz is the length of the transmission line including the solder joint, f is the frequency of interest, ε_0 is the dielectric constant in vacuum, and ε_r is the relative dielectric constant.

$$R_{eq} = \rho_{sj} \left(\frac{\frac{H}{2} - h}{d\Delta z} + \frac{h}{(d - x)\Delta z} \right) = \frac{\rho_{sj}}{d\Delta z} \left(\left(\frac{H}{2} - h \right) + \frac{dh}{d - x} \right) \tag{5}$$

where ρ_{sj} is the resistivity of the solder alloy. The DC resistance was calculated by splitting the solder joint structure into two parts: an upper part that contributed the first term of Equation 5, and a bottom part that contributed the second term and was a function of the crack length, x.

3.3 Comparison between changes in RF impedance and DC resistance as crack propagates

Based on the actual dimension of the test vehicle, the parameters of the model can be determined. Table 4 summarizes the values of the model parameter values used in this study. After plugging these values into the model, the RF impedance and the DC resistance were calculated as the crack length, x, varied from 0 to d. Their relative changes with respect to their initial values were calculated and displayed over

relative crack length, representing the percent of the total crack length, as shown in Figure 27.

Table 4 – Summary of the model parameter values

Parameter	Value	Unit
L_1	263	nH
C_1	0.099	pF
Δz	1.04	mm
f	6	GHz
ε_0	8.85×10^{-12}	F/m
ε_r	1	
d	1.8	mm
h	10	μm
H	0.94	mm

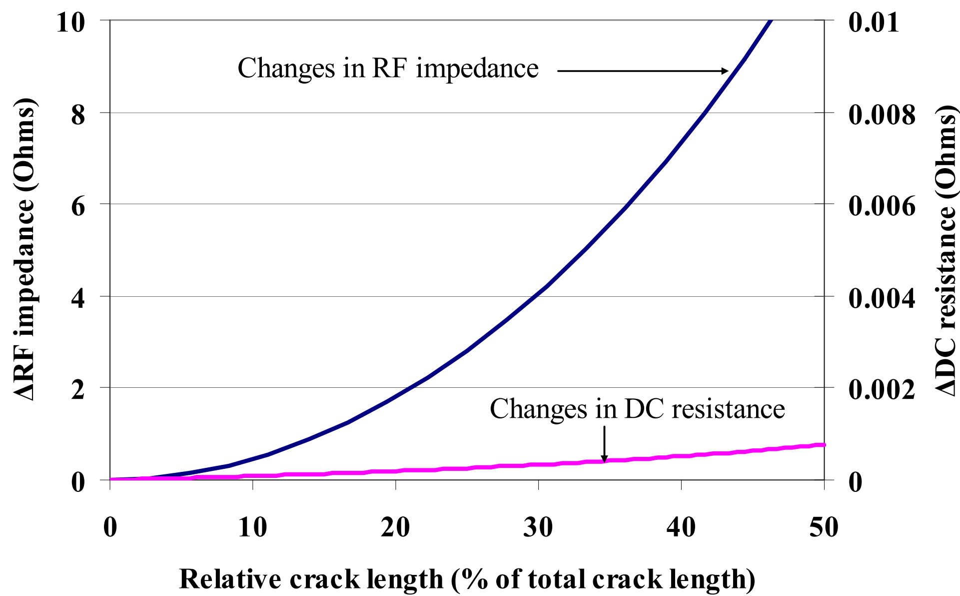


Figure 27 – Comparison between changes in RF impedance and DC resistance over relative crack length

The analytical investigation results matched with the experimental results, as expected. While a crack propagated within a solder joint up to 50% total solder joint width, the RF impedance was calculated to increase more than 10 Ohms, whereas the DC resistance was calculated to exhibit less than 1 milliOhm increase. The reported minimum measurement resolution of DC resistance was 0.1 milliOhm, and RF impedance was found to increase by 0.1 Ohms in response to the early stages of interconnect degradation. Considering these measurement resolutions, this investigation result indicates that RF impedance has improved sensitivity of an order of magnitude greater than DC resistance in detecting early stages of interconnect degradation.

3.4 Summary

It was confirmed that RF impedance responds to early stages of interconnect degradation with an order of magnitude greater sensitivity than DC resistance. Moreover, using the equivalent circuit model the relationship of changes in RF impedance to crack length within a solder joint was verified. These results coincide with the experimental results presented in the previous sections.

4. Conclusions

It was determined that RF impedance provides detectable interconnect failure precursors in response to early stages of interconnect degradation. During stress testing, the RF impedance exhibited a gradual non-linear increase in response to solder joint cracking, while the DC resistance remained constant. This increased sensitivity of RF impedance was quantified using prognostic distance. An analysis of experimental results showed that the results of this study are qualitatively repeatable and consistent.

These results imply that reliability assessment based on DC resistance measurements, using equipment such as event detectors, may overestimate the lifetime of high speed electronic assemblies. Currently, reliability data on printed circuit board assemblies are often obtained by monitoring the DC resistance of daisy-chained components using data loggers or event detectors. For products whose performance is dependent on the transmission of signals with a frequency of several hundred MHz or more, even a small crack may degrade the high speed signal

integrity, while it would not affect low speed signals such as DC resistance. Therefore, DC resistance may overestimate the time-to-failure and thus predict longer lifetimes than would be experienced during product use. RF impedance provides a more sensitive means of monitoring interconnects, which can provide more accurate assessment of the reliability of high speed electronic products in response to solder joint cracking.

Moreover, this technique offers advantages as a research tool for studying solder joint failure mechanisms at intermediate stages of progress prior to complete failure. As shown in the failure analysis of the degraded solder joint, an increase in RF impedance is associated with a physical crack in the solder joint. The continuous monitoring of RF impedance during a stress test provides a direct means of monitoring the health of an interconnect. Therefore, solder joint reliability tests halted upon observing specified increases in RF impedance provide an opportunity to perform detailed studies of defect generation and crack propagation prior to complete separation of the solder joint. Statistical techniques for anomaly detection can be paired with RF impedance to determine the earliest increase in RF impedance associated with the cracking of the solder joint. Studies such as this can lead to insights into the damage accumulation process under a variety of loading conditions.

RF impedance monitoring can be used not only for diagnostic purposes but also as a prognostic tool. In-situ measurements can be compared to an appropriate threshold that allows for the identification of the time at which the interconnect starts to degrade. This event can be a failure precursor, which can trigger an alarm to provide condition-based maintenance, thereby increasing product availability,

reducing unplanned down-time, and potentially bringing substantial savings in operational, repair, logistical and liability costs. This technique can also improve real-time reliability prediction of electronic products when incorporated into sensing circuitry that is either located on a circuit board in an assembly or in external diagnostic hardware.

Chapter 3:

Development of a Prognostics Approach to Predict Interconnect Remaining Life in Real-Time

Prognostics is the process of predicting the remaining useful life (RUL) of a product in its expected future use conditions [29][30]. A detectable event or series of events associated with the degradation of a product's performance is called a failure precursor [31]. Prognostics can be implemented by identifying failure precursors of a monitored product, trending the progress of failure precursors, and then predicting the RUL based on the trend [31].

The health of electronic products is affected to a great extent by the degradation of interconnects, which are vulnerable to failures by a variety of mechanisms such as fatigue, creep, corrosion, and mechanical over-stress. In the electronics industry, DC resistance–based methods have been traditionally used to assess the health of interconnects. However, DC resistance is not sensitive enough to detect early stages of interconnect degradation. In the previous chapter, the use of RF impedance as an improved means for monitoring the health of interconnects was demonstrated. The skin effect, a phenomenon wherein signal propagation at high frequencies is concentrated near the surface of a conductor, increases the sensitivity of RF impedance to small cracks initiated at the surface of an interconnect. The greater sensitivity of RF impedance compared with DC resistance was quantified

during interconnect degradation by simultaneously monitoring RF and DC parameters, and then combining these results with failure analyses on the degraded solder joints.

This chapter discusses an approach for real-time prediction of solder joint remaining lifetime. During stress testing, the reflection coefficient obtained from time domain reflectometry (TDR) exhibited a failure precursor in the form of a non-linear increase prior to the end of life. This failure precursor was trended using support vector regression in order to predict solder joint remaining life in real time. In the following sections, detailed prediction procedures and prediction results are presented.

1. Detection of solder joint failure precursors using RF impedance

In order to detect solder joint failure precursors using RF impedance, fatigue tests were conducted with the same test vehicles shown in the previous sections. Figure 28 shows a comparison between the TDR reflection coefficient at the failed solder joint and the DC resistance. At the beginning of the test, both responses remained near their initial values. Towards the end of the test, the TDR reflection coefficient exhibited a smooth non-linear increase, while the DC resistance showed an abrupt increase only when the solder joint became completely separated. Over multiple trials, it was confirmed that the TDR reflection coefficient repeatedly provided precursors of impending solder joint failure in the form of a non-linear increase near the end of life.

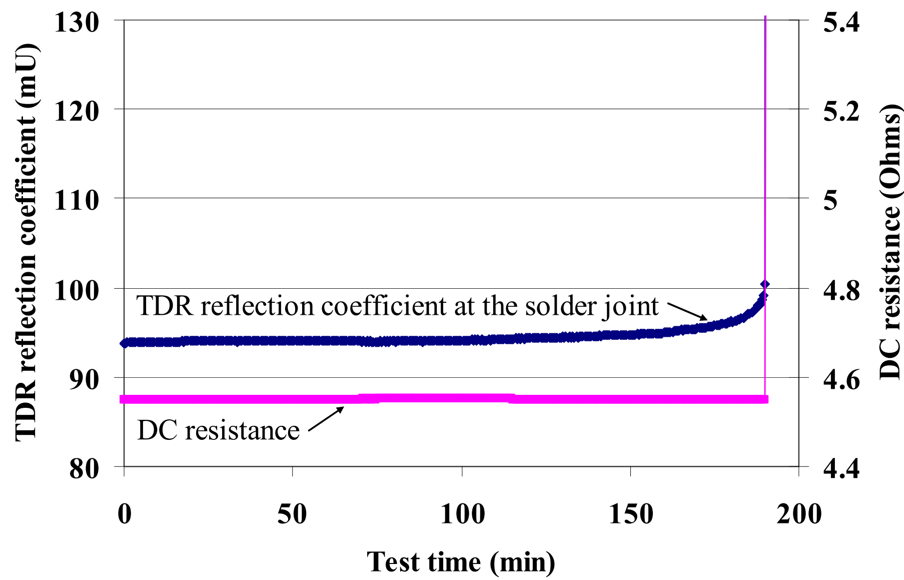


Figure 28 – TDR and DC responses during fatigue testing

2. *Remaining useful life prediction*

The non-linear increase of the TDR reflection coefficient was identified as a solder joint failure precursor. In order to predict the time to solder joint failure using a failure precursor, this non-linear behavior was trended using a support vector machine algorithm.

2.1 Training data and modified TDR response

For data trending, three fatigue tests were conducted to collect training data that represent the typical behavior of the TDR reflection coefficient during fatigue testing. Since the initial values of the TDR reflection coefficient and the test duration varied from sample to sample due to variations in the fillet shape and the amount of

solder in each solder joint, these parameters were modified as follows. The average value of the first 20 data points was subtracted from the TDR reflection coefficients, converting each measured value to the relative increase from the initial values (ΔΓ). The test time was converted to percent lifetime by dividing the test time by the total test time at which an open circuit was created due to solder joint separation. The modified TDR responses from the training data behaved similarly to each other, as shown in Figure 29.

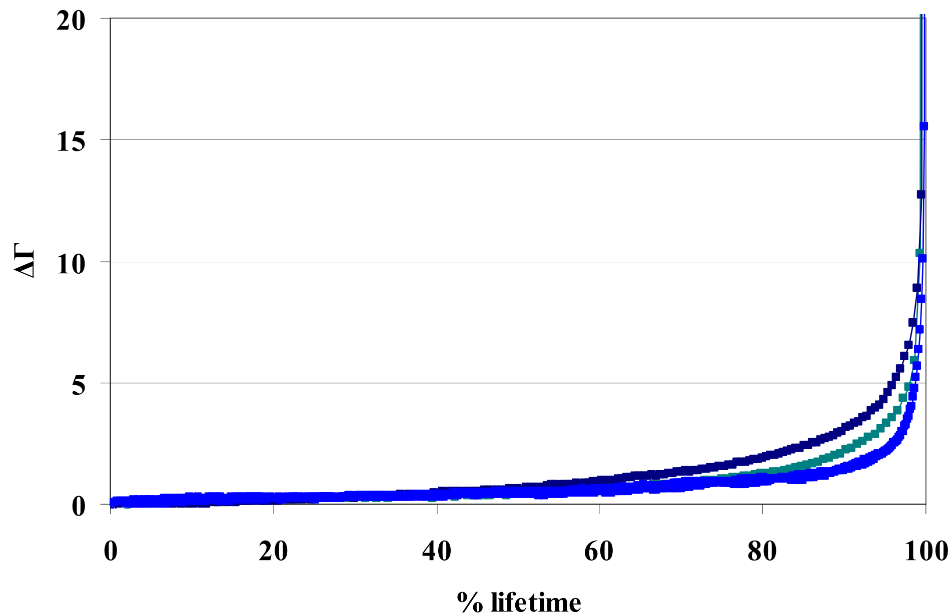


Figure 29 – Modified TDR responses using % lifetime and ΔΓ from three fatigue tests

2.2 Training data trending

Support vector machines (SVMs) were used to perform regression analysis on the modified TDR responses. SVMs were developed to solve classification problems

separating individual items into groups by producing a linear classifier in a high dimension space, and they were extended to the domain of regression problems [34]. SVMs have been useful for non-linear regression [35], as well as anomaly detection [36]. Regression problems using SVMs aim to find a function $f(x)$ that has the minimized loss function. A loss function, $L_e(y)$, which directly measures the deviation, is defined as an ε-insensitive function and can be expressed as in Equation 6:

$$L_{\varepsilon}(y)=\begin{cases} 0 & for \;\; |f(x)-y|<\varepsilon \\ |f(x)-y|-\varepsilon & otherwise \end{cases} \tag{6}$$

where y is the TDR reflection coefficient values for all the training data. According to Equation 6, errors greater than ε were only taken into account to minimize the loss function. In this study, ε was chosen to be 1 mU, which was the measurement resolution that could be obtained experimentally on a consistent basis. The training data was trended to obtain a regression curve using SVMs as shown in Figure 30.

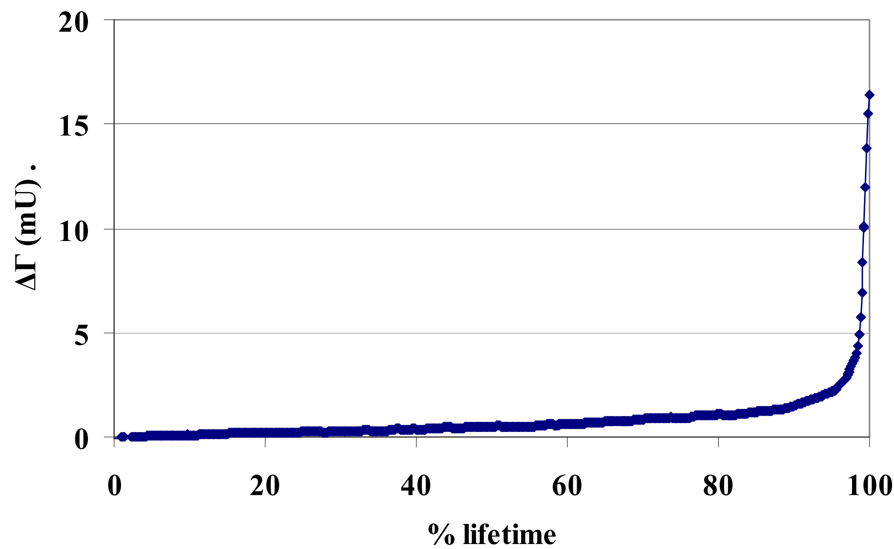


Figure 30 – The regression curve of the training data using SVM regression

As seen in the regression curve, two different increasing stages were observed during solder joint degradation: a linear increase up to about 70% of lifetime followed by a steeper non-linear increase with an ascending slope until a DC open circuit was observed. This non-linear increase continuously led up to the failure, a DC open circuit, and thus was used to predict the remaining life of the solder joints.

2.3 Prediction methodology

The failure precursor, which consisted of a non-linear increase in $\Delta\Gamma$, was obtained on the basis of percent lifetime. Thus, a time-to-failure could not be predicted without having a relationship between percent lifetime and actual test time. To overcome this, the coefficient of determination, which represents how well the regression curve represents the test data [37], was used to determine the relationship, and therefore to predict the time to solder joint failure.

In the following discussion, T_n is defined to be the time at which the system has consumed n% of its total life during a fatigue test. For example, T_0 and T_{100} indicate the beginning and the end of life; and the time interval between T_{70} and T_{100} is the period during which the non-linear increase of TDR reflection coefficient was observed.

In order to make a prediction at a particular time t_1, we make a trial assumption that t_1 corresponds to T_{98}. We also calculate a t_0 that corresponds to T_{70} to get the actual time interval during which the non-linear increase should be observed under the trial assumption. We then compare the values from the test data with the ones from the regression curve between t_0 and t_1. The comparison can be quantified using the coefficient of determination, which analyzes how closely the test data fits the regression curve. If the agreement is poor, the coefficient of determination would be close to zero, which would indicate that the current TDR response has not reached T_{98} yet. On the other hand, if the agreement is good, the coefficient would be close to 1, which would indicate that the current test time, t_1, could be converted into T_{98}, and vice versa. Thus, the time to solder joint failure, T_{100}, can be predicted in terms of test time.

Figure 31 shows the TDR reflection coefficient and the coefficient of determination during a fatigue test used as one of the training datasets. For the first 20 data points, the coefficient of determination values were assigned to be zero, since the coefficient of determination values fluctuated in the beginning of the test as a result of an insufficient amount of test data to compare with the regression curve. The fluctuation of the coefficient of determination decreased as the test time increased.

After about 53 minutes, the coefficient of determination began to increase gradually, indicating the current TDR response was showing a non-linear increase. Sensitivity analysis was performed in order to determine an appropriate threshold that could best predict the time to solder joint failure.

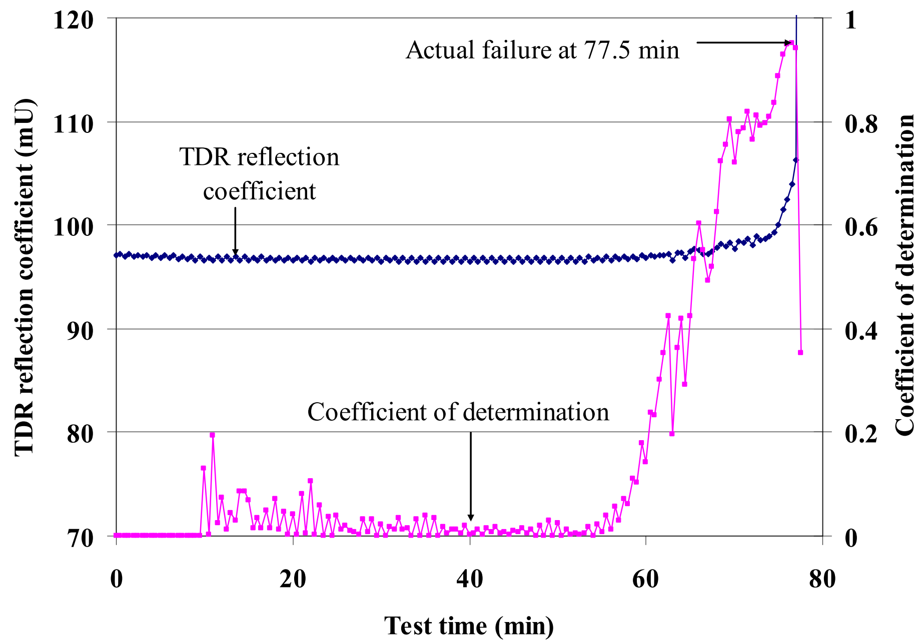


Figure 31 – TDR response and coefficient of determination during a fatigue test

2.4 Sensitivity analysis and prediction results using the regression curve

There is a trade-off between prediction accuracy and missed alarm probability. For example, when a threshold is set too low, T_{98} may be determined too early, which will reduce the prediction accuracy. On the other hand, when a threshold is set too high, it is possible to determine T_{98} too late resulting in over-prediction of the time to solder joint failure, or to predict nothing when the coefficient of determination does

not reach the threshold. In order to identify the optimal threshold, sensitivity analysis was conducted.

A set of possible threshold values of the coefficient of determination between 0.8 and 1, with increments of 0.01, were evaluated. In order to reduce the effect of measurement variation on the detection sensitivity, at least three consecutive events that violated the threshold were required. When this condition was satisfied, the time to the first event was used to predict the time to solder joint failure. The sensitivity analysis found that 0.94 was the optimal threshold value that provided neither too early nor too late prediction for all the training data.

The following section discusses the procedure to implement this prognostics approach using real-time monitoring of the TDR reflection coefficient during stress testing and provides the prediction results.

3. Evaluation – Real-time monitoring

Fatigue tests were conducted with real-time monitoring of the TDR reflection coefficient. The same test conditions and criteria were applied as discussed in the previous section. During fatigue testing, the TDR reflection coefficient was collected every 30 seconds. After 10 minutes of testing, the failure prediction was begun by determining whether the coefficient of determination violated the threshold at least three consecutive times to test the assumption that the time of the last measurement represented T_{98}. Three outcomes of the prediction were recorded for each of several

tests: the predicted time to failure calculated from the determined T_{98}, the actual time to failure, and their relative errors.

Figure 32 shows one result from the fatigue tests with the TDR reflection coefficient monitored in real time during the test and the determined T_{98}. The coefficient of determination remained less than about 0.2 until it began to increase at about 1400 minutes. Then it steeply increased as the TDR reflection coefficient rose. The coefficient of determination violated the threshold of 0.94 at 1936.5 minutes with more than three consecutive detections, and the predicted time to failure that corresponded to T_{100} was 1976 minutes. The test continued until the actual failure, an open circuit due to complete separation of the solder joint, occurred at 2002 minutes.

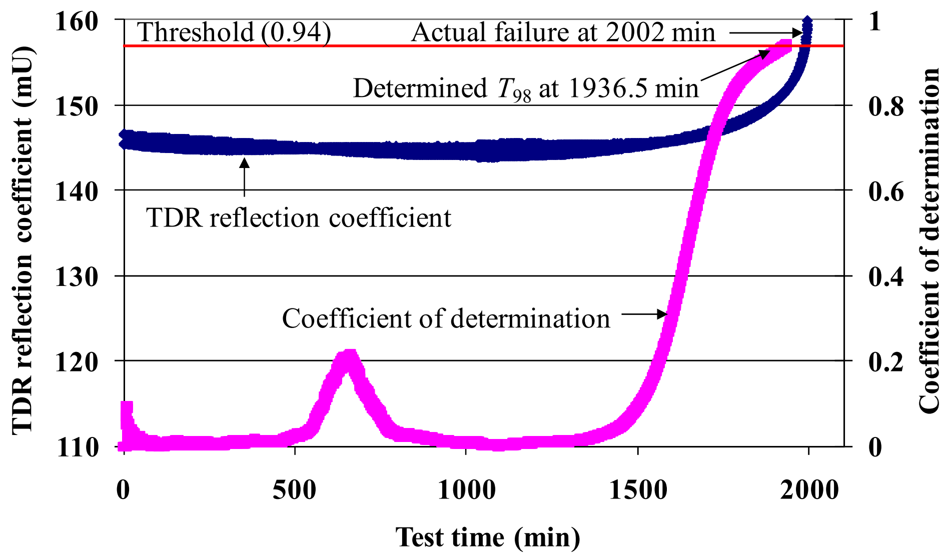


Figure 32 – TDR reflection coefficient and coefficient of determination during a fatigue test

Table 5 provides a summary of the failure prediction results using real-time monitoring of the TDR reflection coefficient over four more tests. Since the time to failure prediction was made after T_{98} was determined, a prediction error was calculated the difference in time between the predicted and the actual failure over the difference in time between the actual failure and the determined T_{98}. Although there was a wide range of variation in lifetimes from sample to sample, the prediction errors were less than 56 %. Moreover, the predicted times to failure were always prior to the actual times to failure, which indicates that this approach always provided conservative predictions in preparation for impending solder joint failure.

Table 5 – Summary of solder joint failure predictions from fatigue tests

Test no.	Predicted time to failure (min)	Actual time to failure (min)	Error (%)
1	1343	1360	39
2	188	190.5	40
3	70.5	72	52
4	1976	2002	40
5	284	291	55

This prognostic approach can be used to assure the user that the product under test should be healthy for the next a few percent of life. Although the time to failure can be predicted after the determination of T_{98}, until then it can be concluded that the system has not consumed 98% of its total life, indicating that for the remaining 2%

the system should be reliable. Based on this information, the user can make a decision whether the system can be used again until the next examination, or it should be taken out of the service. The remaining percent of its total life can be adjusted according to detection sensitivity and accuracy the system requires.

4. Conclusions

An approach to predicting solder joint remaining life in real time has been presented. During solder joint degradation, the TDR reflection coefficient exhibited failure precursors as a non-linear increase near the end of life. This behavior was consistently observed over multiple trials, and was trended using SVM regression to obtain a regression curve that represents the typical behavior of the TDR reflection coefficient during solder joint degradation. In real-time, the coefficient of determination between the regression curve and the test data was calculated to determine T_{98}, the time at which the system has consumed 98% of its total life, and thus to predict the time to failure corresponding to T_{100}. Over multiple tests, the time to failure was successfully predicted with an error of less than 3% and always prior to the actual failure. Thus, this prognostic approach can serve as a real-time means to predict and prevent importance prominent cause of failures in electronic products and systems.

These test results indicate that an early warning can be triggered with an appropriate prognostic distance from the actual interconnect failure. Prognostic distance is the distance in time between the failure precursor detection and the actual failure [31]. In this case, to obtain an adequate safety margin, the prognostic distance

can be defined as the time interval between the determined T_{98} and T_{100}, and any time within the prognostic distance can be chosen as the time when the system needs to be removed from operation in order to avoid failure. Since the experiment was conducted under an accelerated test condition, this prognostic distance could correspond to a few days, weeks, or months in field conditions. Also, the time of removal from service can be adjusted according to the safety margin required for any particular application.

Moreover, in order to improve the accuracy of these predictions, physics-of-failure (PoF) models can be incorporated into the TDR reflection coefficient regression curve. The PoF models associated with fatigue crack growth kinetics should allow the regression curve to effectively address the relationship between TDR reflection coefficient and physical changes in a solder joint, such as crack length. This would eventually provide a basis for implementing a fusion prognostics approach, which combines the model-based and the data-driven approaches [38], in order to further improve solder joint failure prediction.

The data trending in this paper was performed in a case where the loading conditions were controlled to be constant throughout the tests. However, in a real-life situation the loading conditions are not controlled and the rate and the amplitude of cyclic force can vary over time. These challenges should be addressed in order for this prognostic approach to be practically implemented in real-life applications. One possible solution might be to incorporate the rain-flow algorithm for normalization of randomness in cyclic loading conditions [39] and an incremental damage superposition approach [40][41] for combining the effects of various loading

conditions. It might be also possible to relate a latent variable such as solder joint crack length to changes in the TDR reflection coefficient by electromagnetic simulation modeling. In order to produce a more generally applicable prognostic approach, this strategy merits further investigation.

Chapter 4:

Development of a Method for Non-Destructive Identification of Interconnect Failure Mechanisms

Time domain reflectometry (TDR) is a measurement technique useful for characterizing and localizing changes in impedance of a transmission line or an interconnect. It has been used for a variety of sensing applications, such as for characterizing non-uniform transmission lines [42], locating faults within a wiring system [43], sensing liquid levels [44], and characterizing material properties [45]. The use of TDR to detect early stages of interconnect degradation was presented in the previous sections. Due to the skin effect, small physical changes, such as a crack initiated at the surface of an interconnect, provided a detectable increase in the TDR reflection coefficient, while DC resistance-based techniques, including event detectors, did not exhibit any early changes prior to the interconnect failure. Failure analysis on the partially degraded interconnects revealed that the early increase in the TDR reflection coefficient was due to a crack propagating within the interconnect. Thus, TDR can serve as an early indicator of interconnect degradation.

A TDR measurement is typically reported as a reflection coefficient (Γ) and is made by launching a pulse or a step into the circuit and observing the reflections caused by impedance mismatches with the characteristic impedance of the circuit [46][47]. The TDR reflection coefficient is a ratio of the incident to the reflected voltage. It is a function of the impedance of the device under test (DUT) and the characteristic impedance, as shown in Equation 7.

$$\Gamma = \frac{V_{reflected}}{V_{incident}} = \frac{Z_L - Z_0}{Z_L + Z_0} \tag{7}$$

where Z_L and Z_0 denote the impedance of the DUT and the characteristic impedance of the circuit, respectively.

The sensitivity of Γ to early stages of solder joint cracking stems from an increase in Z_L due to a crack near the periphery of the solder joint. This leads to an increase of the TDR reflection coefficient. If damage is localized at the solder joint, the characteristic impedance remains unchanged. However, printed circuit assemblies can also fail because of pad cratering. These phenomena can be associated with changes of the characteristic impedance, Z_0 in the equation. Thus, these physical changes can also be expected to alter the TDR reflection coefficient.

1. Non-destructive identification of interconnect failure mechanisms

Electronic products are exposed to various environmental and operational loading conditions, such as temperature cycling, vibration, and mechanical over-stress, that may result in the failure of interconnects or circuit boards. With any of the common loading conditions, interconnect degradation often initiates from the surface and propagates inward. Due to the skin effect, TDR can non-destructively detect the precursors of interconnect failure by monitoring the changes in impedance at the interconnect. Since the TDR reflection coefficient is also associated with changes in the characteristic impedance of the circuit, it should also be able to detect physical changes of the circuit such as pad cratering.

Figure 33 shows a circuit board with a coplanar waveguide structure composed of a signal strip line surrounded by two ground planes on the same surface on a dielectric. This type of transmission line is commonly used for board-level interconnects [9]. The characteristic impedance of a coplanar waveguide is a function of the effective dielectric constant (ε_e), the width of the signal trace (w), and the distance between the signal and the ground plane (s) as shown in Figure 34. The functional relationship between these quantities may be written as shown in Equation 8 [9][48]:

$$Z_0 = \frac{30\pi}{\sqrt{\varepsilon_e}}\left(\frac{1}{\pi}\ln\left(2\frac{1+\sqrt{k'}}{1-\sqrt{k'}}\right)\right) \tag{8}$$

where

$$k' = \frac{\sqrt{4sw + 4w^2}}{s + 2w} \tag{9}$$

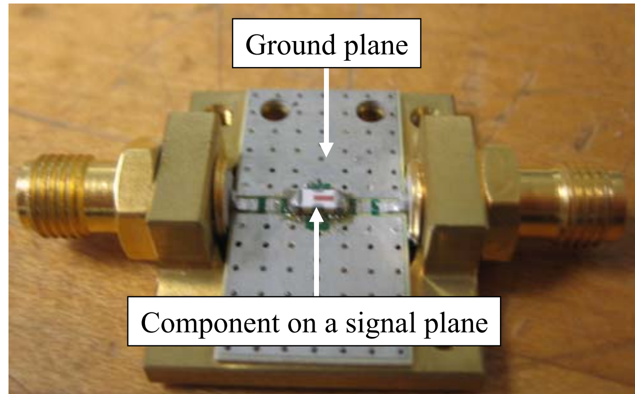


Figure 33 – Test vehicle with a component soldered on a signal plane

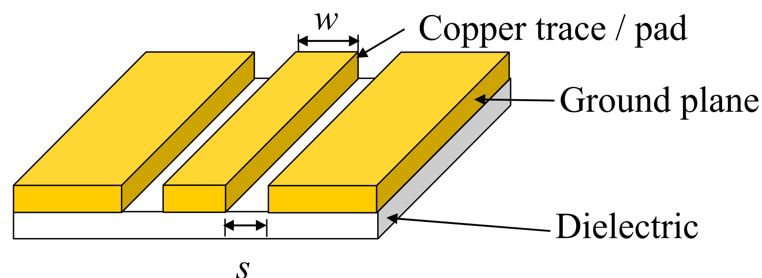


Figure 34 – Schematic of a simplified coplanar waveguide structure

Pad cratering results in both an increase of the effective distance between the signal and ground plane (s) and a decrease of the effective signal plane width (w) projected onto the circuit board, which raises the k' value and, consequently, the characteristic impedance (Z_0) of the circuit board. According to Equation 8, the TDR reflection coefficient decreases as the characteristic impedance increases. From this analysis, pad cratering is predicted to lead to a decrease in the TDR reflection

coefficient. Thus, the TDR reflection coefficient should be sensitive to pad cratering as well as solder joint cracking during degradation of a circuit board under stress, and the different changes in TDR reflection coefficient should allow for non-destructive identification of the relevant failure mechanisms.

2. *Experimental setup*

In order to examine the ability of TDR to distinguish between interconnect failure mechanisms, a test circuit was developed as shown in Figure 35. The test circuit included an impedance-controlled circuit board on which a low pass filter was soldered, two bias-tees for the simultaneous monitoring of the TDR reflection coefficient and DC resistance, a Wheatstone bridge for DC resistance measurement, and a vector network analyzer for the TDR reflection coefficient measurement. These components were connected using impedance-controlled RF cables in order to match the characteristic impedance of the test equipment.

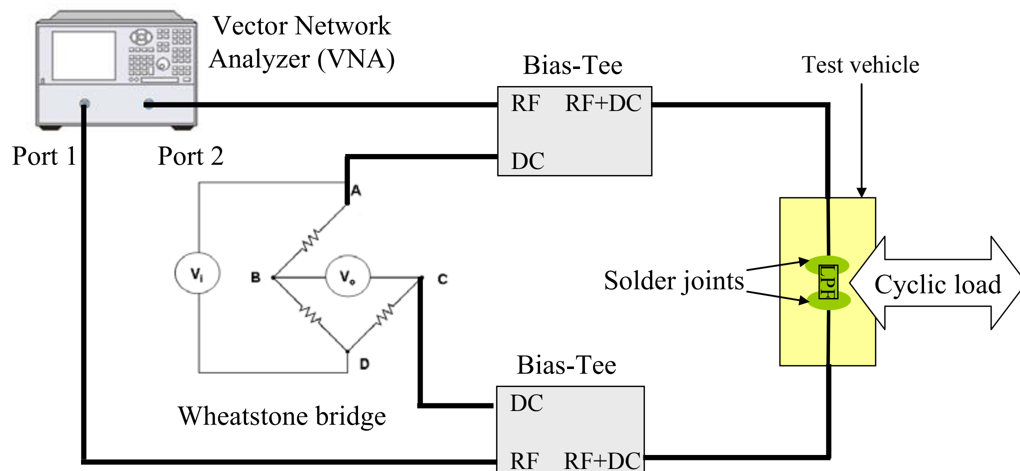


Figure 35 – Schematic of the test circuit

As shown in Figure 36, the test circuit board also had a controlled characteristic impedance of 50 Ohms with an SMA connector on each side. A surface mount technology (SMT) low pass filter (LPF) was soldered on this circuit board using eutectic tin-lead solder paste. The cut-off frequency of the low pass filter was 6.7 GHz, and the monitored frequency span for the TDR reflection coefficient was between 500 MHz and 6 GHz. Therefore, the low pass filter acted as a conductor to both the RF and DC signals.

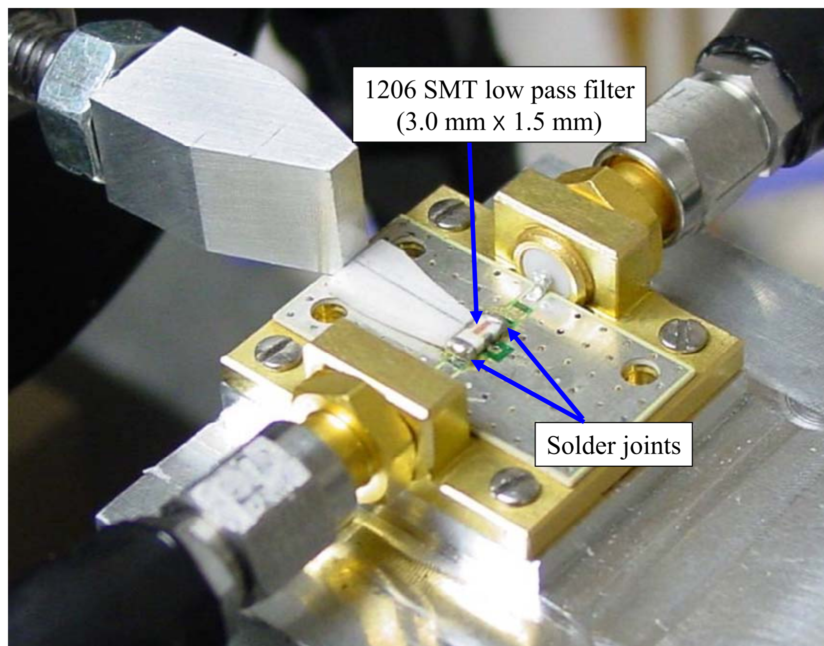


Figure 36 – Test circuit board soldered with a low pass filter

A Wheatstone bridge was incorporated into the test circuit for DC resistance measurement. It not only eliminated environmental influences such as fluctuations of

the ambient temperature, but also increased measurement resolution. A Keithley 2010 multimeter was used to monitor the voltage in the Wheatstone bridge circuit, which was converted into DC resistance. An Agilent E8364A vector network analyzer configured with TDR functionality was used to monitor the TDR reflection coefficient during fatigue testing. Each set of TDR measurement data contained a collection of reflection coefficient values over the partial signal path of the circuit board, collected at a particular instant during the fatigue test. In order to monitor changes in both the RF impedance and the DC resistance during interconnect degradation, the TDR reflection coefficients at each potential failure site were extracted and compared with the DC resistance by displaying them in a plot as a function of test duration.

An MTS Tytron 250 was used to apply mechanical load to the SMT filter in the form of a cyclic shear force. The shear force profile was programmed, applied to the body of the component, and monitored during fatigue testing. A strip of alumina was inserted between the metal tip of the force transducer and the component to avoid making electrical contact between the loading system and the circuit.

3. Test conditions

A cyclic mechanical shear force was directly applied to the low pass filter in order to produce fatigue failure of the interconnects. An offset force was used to maintain the contact between the component and the force transducer throughout the entire fatigue cycle, and the oscillatory force produced a cyclic loading condition

leading to fatigue failure. Preliminary fatigue tests were performed to identify the offset force levels that result in solder joint cracking and pad cratering, respectively, given an amplitude of 10 N and a frequency of 0.25 Hz in a sinusoidal waveform. It was observed that as the offset force increased above 40 N the interconnect failure mechanism shifted from solder joint cracking to pad cratering. Considering the fact that a higher offset force typically produced a shorter time to failure, the offset forces for solder joint cracking and pad cratering were chosen to be 30 N and 45 N, respectively. Thus, the final cyclic force profile was programmed as a sinusoidal waveform of 10 N amplitude and 0.25 Hz frequency superimposed on the offset force for each case, as shown in Figure 37.

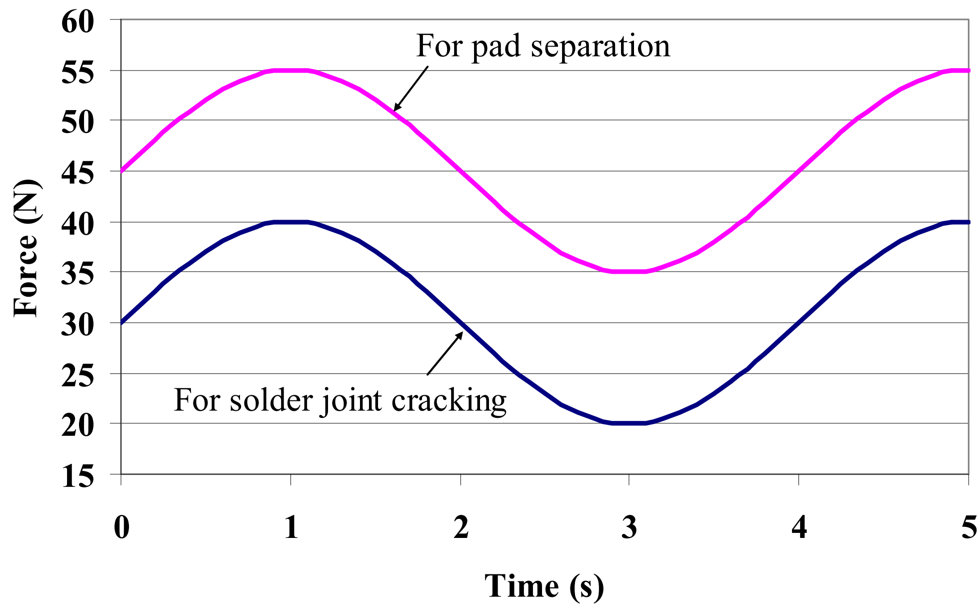


Figure 37 – Load profiles for solder joint cracking and pad cratering

During fatigue testing, instrumental control software was used to instruct the multimeter and the vector network analyzer to collect the DC resistance and the TDR reflection coefficient, respectively, every 30 second. During each experiment the TDR responses and the DC resistance were monitored until the cyclic stresses resulted in either a separation of the solder pad from the circuit board or a DC open circuit within the solder joint.

4. Results

Figure 38 shows a fatigue test result comparing the TDR reflection coefficient at the solder joint with the DC resistance while the applied cyclic shear force produced solder joint failure due to cracking within the solder. The test was concluded at 524 minutes, at which time a DC open circuit occurred due to solder joint cracking. During the test the TDR reflection coefficient and the DC resistance, calculated from a node voltage in the Wheatstone bridge, were collected every 30 seconds. Both the TDR reflection coefficient and the DC resistance stayed around their initial values during the first few hundred minutes of test time. As the test progressed, the TDR reflection coefficient gradually increased in response to the growth of cracks within the solder joint, while the DC resistance remained the same. At the end of the test, both the TDR reflection coefficient and the DC resistance showed a sudden increase indicating a DC open circuit of the solder joint, as shown in Figure 39. This behavior of the TDR reflection coefficient during solder joint cracking coincides with the observations described in [33]. Cross-sectional failure

analysis consistently confirmed that solder joint cracking was responsible for these failures.

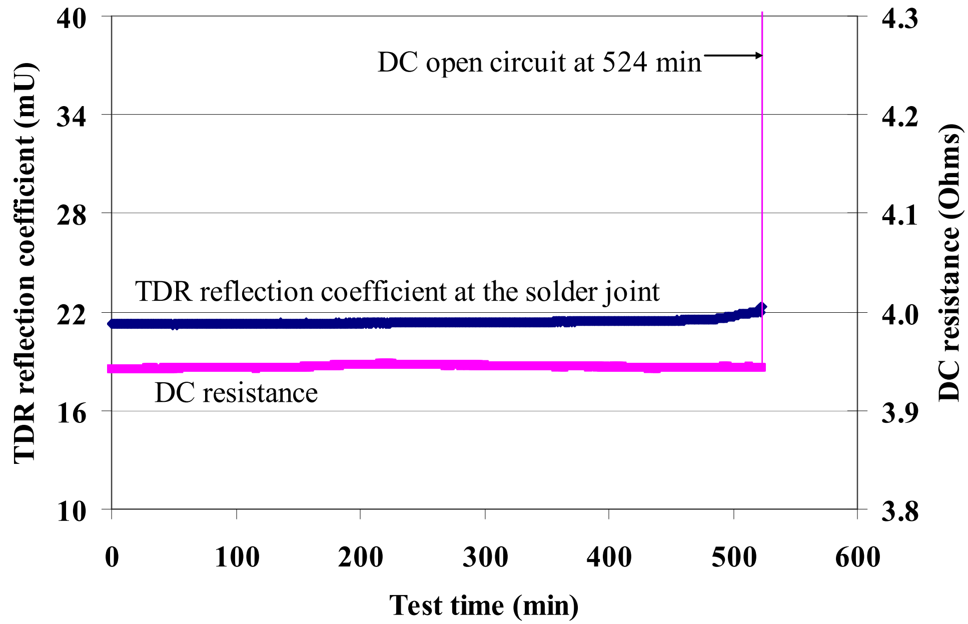


Figure 38 – Comparison between the TDR reflection coefficient and the DC resistance during solder joint cracking

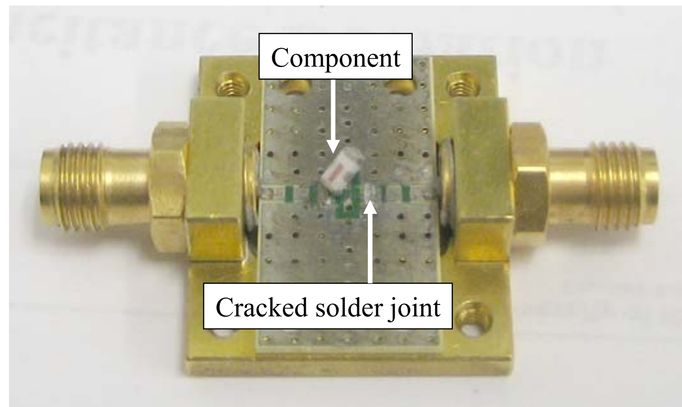


Figure 39 – DC open circuit as a result of solder joint cracking

Figure 40 shows the results of a fatigue test in which the failure occurred due to pad cratering. The total duration of the test was 194 min. The DC resistance remained around its initial value throughout the test, as observed during all but the last measurement of the solder joint cracking experiments. The TDR reflection coefficient, however, showed a gradual decrease towards the end of the test, which resulted from the separation of the solder pad from the circuit board. The test was stopped when contact between the force transducer and the component was lost due to pad cratering. In spite of the pad cratering, the solder joint still provided a mechanical and electrical connection between the component and the pads. Therefore, in this test neither measurement exhibited a sudden rise that would indicate a DC open circuit at the end of the test.

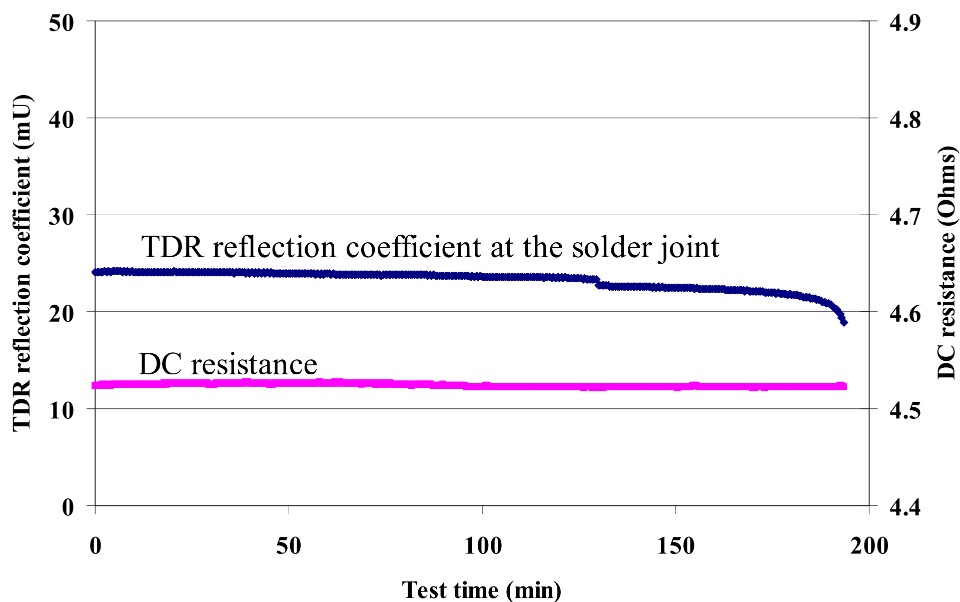


Figure 40 – Compasison between the TDR reflection coefficient and the DC resistance during pad cratering

After the fatigue test, the circuit board was inspected with a scanning electron microscope (SEM) to locate the physical damage that was responsible for the changes in the TDR reflection coefficient. As shown in Figure 41, the SEM revealed that the solder pad was torn off of the circuit board, a failure known as pad cratering. This phenomenon was responsible for the decrease of the TDR reflection coefficient near the end of the test. Also, the SEM showed that the solder joint on top of the separated pad remained intact, providing an electrical connection, which indicated that the decrease in the TDR reflection coefficient was caused by the increase in the characteristic impedance. The same response of the TDR reflection coefficient to pad cratering was observed over multiple trials.

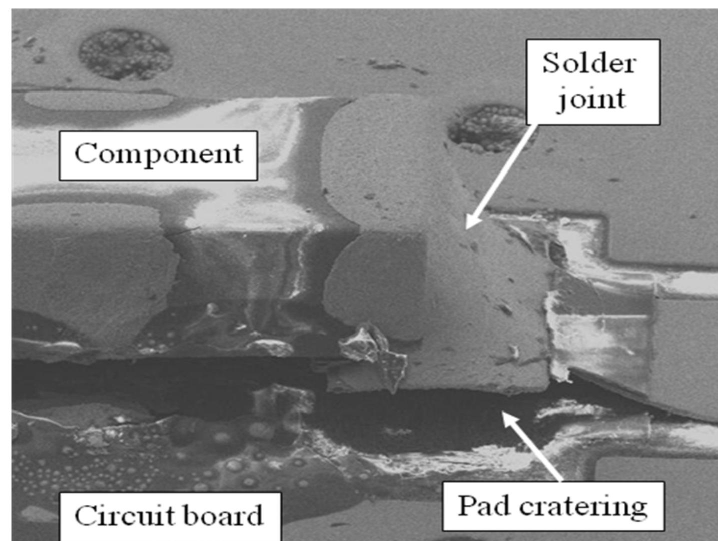


Figure 41 – SEM micrograph of the damaged sample

These results indicate that TDR can serve as a test method that can non-destructively sense interconnect failure mechanisms before the failure occurs. TDR

can also be used to identify interconnect failure mechanisms because the response over time of the TDR reflection coefficient differs for each interconnect failure mechanism: solder joint cracking increases the solder joint impedance, and thus increases the TDR reflection coefficient; pad cratering increases the characteristic impedance, and thus decreases the TDR reflection coefficient. TDR is also capable of predicting interconnect failure, because in both interconnect failure mechanisms changes in TDR reflection coefficient occur gradually, which allows the user to be prepared for the impending failure.

5. Conclusions

The ability of TDR to non-destructively identify interconnect failure mechanisms during cyclic loading has been demonstrated. Fatigue tests revealed that the TDR reflection coefficient gradually increased while the solder joint was degraded by physical cracking, whereas it gradually decreased as the solder pad was separated from the circuit board. This behavior was explained on the basis of a theoretical analysis of the effect of changes in characteristic impedance or impedance of the device under test on the TDR reflection coefficient. Meanwhile, the DC resistance, a traditional measure of interconnect reliability, did not provide early indications of interconnect degradation or allow identification of failure mechanisms during these tests. Therefore, TDR analysis can be used as a prognostic sensing technique to detect early stages of interconnect degradation on printed circuit boards and non-destructively identify interconnect failure mechanisms.

These results imply that analysis based on TDR can provide accurate reliability assessment of electronics exposed to cyclic loading conditions, such as vibration, repeated mechanical shocks or flexure, or thermal cycling. Regardless of interconnect failure mechanisms, the TDR reflection coefficient exhibited early and gradual changes in response to physical degradation of an interconnect. As clock speeds and communication frequencies rise, it may be expected that the performance of electronics will be adversely affected even by partially degraded interconnects due to the skin effect. Thus, the ability to detect physical changes such as small cracks or a small degree of pad cratering in the early stages of the degradation process should become increasingly valuable for accurate reliability assessment.

TDR can produce useful information for maintenance of electronics while they are still in service. Not only can TDR be used for early detection of interconnect degradation, but it also provides insight into the physical processes by which failures are being induced before the failure occurs. This application of TDR can eventually allow the user to initiate preventive actions prior to catastrophic failures and to have information about what is degrading.

Analysis based on TDR offers great promise for use in prognostics of electronic products. Since the changes in TDR reflection coefficient leading up to failure were gradual in nature, it should be possible to quantify the damage level associated with solder joint cracking or pad cratering. Prediction of interconnect failure can be made by trending the gradual changes of TDR reflection coefficient near the end of life. This approach has successfully predicted the remaining useful life of interconnects under controlled loading conditions as shown in previous chapter.

Eventually, this technique could enable condition-based maintenance, resulting in improved safety and economic advantages not only for manufacturers but also for users.

Chapter 5:

Degradation of Digital Signal Characteristics due to Intermediate Stages of Interconnect Failure

The performance of electronic products and systems is adversely affected by physical damage to interconnects across which signals travel. Common interconnects at the circuit board level include solder joints, printed circuit board traces, component leads, and connectors. Due to environmental and operational loading conditions during their life cycle, these interconnects are susceptible to failures due to wearout mechanisms such as fatigue and creep. Over time these mechanisms cause the gradual accumulation of damage, which eventually leads to the failure of the entire system. Even a small level of interconnect degradation, which could be neglected in low speed systems, becomes a major concern with the continued increase in the speeds of digital systems. In order to ensure proper functioning of current and future digital circuits throughout their intended lifetime, it is necessary to understand the effect of interconnect degradation on the characteristics of digital signals.

From previous chapters, it has been established that RF impedance as can serve as a sensitive means for detecting interconnect degradation. Due to the skin effect, RF impedance exhibits improved sensitivity compared to DC resistance for detecting early stages of interconnect degradation, which often initiates from the circumferential region of an interconnect. Moreover, RF impedance enables the non-

destructive identification of interconnect failure mechanisms associated with changes in the impedance of solder joints and the characteristic impedance of circuit boards.

This chapter investigates the practical implications of the skin effect using digital signals, which are widely used nowadays for information processing, communication, and control. Continuous monitoring of eye parameters such as eye height and jitter was conducted during mechanical fatigue testing in order to examine the relationship between solder joint degradation and changes in eye parameters. The contributors to digital signal degradation were further explored by decomposing jitter into its various constituent elements.

1. Digital signal characteristics

A digital signal is a waveform that switches between two voltage levels representing two states of a Boolean value. A digital signal waveform is continuous over time. Therefore, it can be analyzed in an analog fashion using an oscilloscope. An eye diagram is the superposition of multiple waveform samples over one unit interval, using a clock-based trigger to superimpose rising and falling transitions. An eye diagram is a common visualization method used for analyzing the characteristics of digital signal waveforms such as rise time, fall time, eye width, eye height, and jitter, as shown in Figure 42.

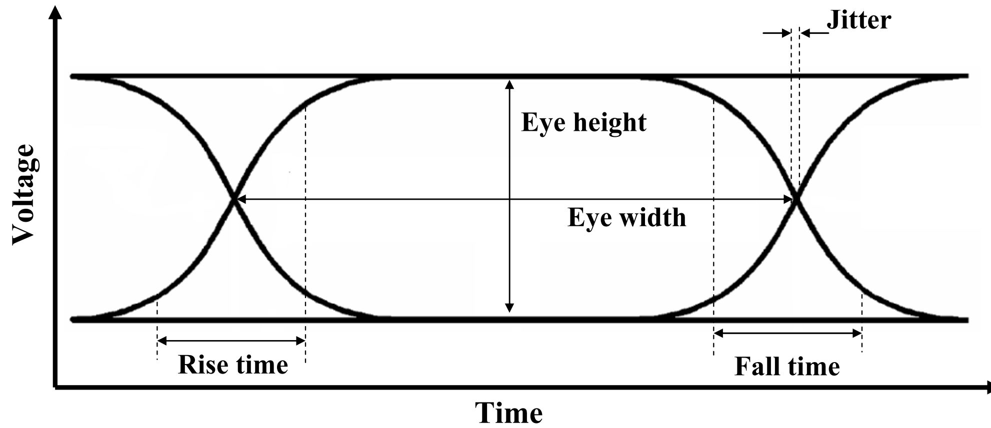


Figure 42 – Schematic of an eye diagram and eye parameters

Rise and fall time represent how quickly a signal can transition from a low to a high state, or a high to a low state. In this study they were obtained by identifying the mean locations of the high and the low states, calculating the corresponding 20% and 80% levels with respect to the low and the high, and taking the mean transition time between the two levels. Eye width and eye height are measures of the horizontal and the vertical opening of an eye diagram, respectively. Eye width was determined from the distribution in time of the 50% levels, as the difference between the +3 standard deviation point on the left of the eye and the -3 standard deviation point on the right of the eye. Eye height was measured as the difference in amplitude between the -3 standard deviation point of the 100% level and the +3 standard deviation point of the 0% level. Jitter is defined as the deviation of a signal transition from its ideal position in time, and it is measured in an eye diagram as the width in time at the eye crossing point where a rising edge and a falling edge meet each other [49]. These eye parameters quantify the performance of digital communication channels, whose

degradation could be manifested as an increase in rise time, fall time, and/or jitter, or a decrease in eye width and/or eye height.

Jitter can be further decomposed into its constituent elements to allow for precise analysis of contributors to signal degradation [50]. The first classification is between random jitter (RJ), which occurs randomly, and deterministic jitter (DJ), which does not. DJ is composed of periodic jitter (PJ), which is often affected by sources that have periodicity, and data-dependent jitter (DDJ), which is correlated to the data stream or pattern. DDJ can be further broken into two categories: inter-symbol interference (ISI) and duty-cycle distortion (DCD). ISI is degradation of a signal in which one transition within a data sequence interferes with a subsequent transition. Interconnect degradation may result in reduced or insufficient bandwidth, which does not allow the signal to reach its intended amplitude before it is required to make the subsequent transition from high to low or low to high. DCD is observed when the duration of the high state is different from the duration of the low state. Figure 43 shows the hierarchy of jitter as described.

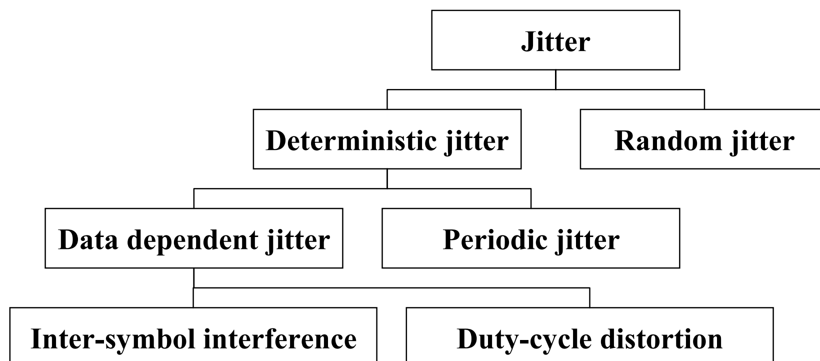


Figure 43 – Hierarchy of jitter

Intermediate stages of interconnect degradation have been shown previously to adversely affect signal integrity in the analog domain. An investigation of the sensitivity to solder joint cracking of the reflection coefficient obtained from time domain reflectometry (TDR) revealed that a crack with a length as little as 30 µm was detectable using frequencies of 0.5 to 6 GHz. It is therefore likely that changes should be observable in one or more of the jitter components, as well as the other eye parameters, prior to complete interconnect separation. The magnitude of the responses exhibited by each of the eye parameters cannot be readily predicted *a priori*. This chapter presents the results of an experimental investigation in which, while a solder joint was stressed by cyclic loading, the eye parameters were monitored in order to assess the impact of interconnect damage accumulation on digital signal characteristics and to identify possible interconnect failure precursors.

2. Experimental setup

A test circuit was developed to monitor the eye parameters while solder interconnects were subjected to cyclic loads, as shown in Figure 44. The test circuit included an impedance-controlled circuit board, a digital signal generator, and an oscilloscope for monitoring of the eye diagram and eye parameters. These components were connected using impedance-controlled RF cables in order to match the characteristic impedance of the test equipment and circuit board, which was 50 Ohms.

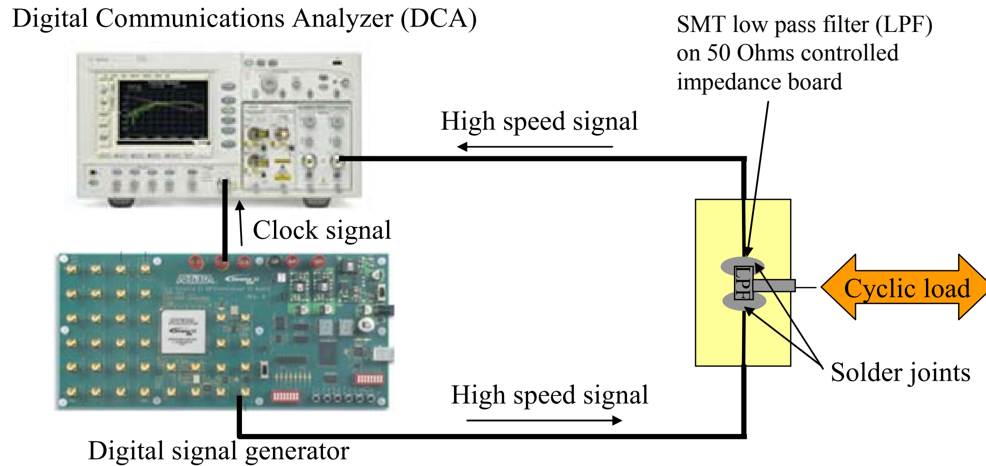


Figure 44 – Schematic of the test circuit

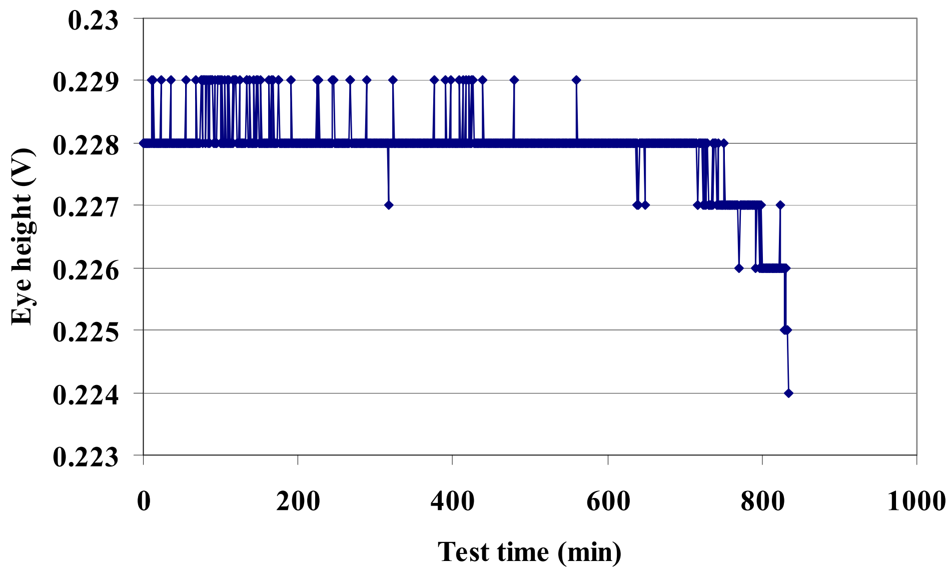
The test circuit board contained two SMA connectors and a surface mount technology (SMT) low pass filter, which was soldered to the board using eutectic SnPb solder paste. An MTS Tytron 250 was used to apply a cyclic shear force to the SMT component in order to generate fatigue failure of the solder joints. The applied cyclic force was in the form of a sinusoidal profile with an amplitude of 10 N and a frequency of 0.25 Hz, superimposed on an offset force of 30 N.

An Altera Stratix II GX signal integrity development kit was configured to generate a high speed digital bit sequence of PRBS 7 (Pseudo-Random Bit Sequence), which had a run length of 2^7-1 bits at 3.125 Gbps. This digital signal was transmitted through the solder joints on the test circuit, and an Agilent DCA 86100C oscilloscope was used to continuously monitor its eye diagram and measure the corresponding eye parameters such as rise time, eye height, and jitter during solder joint degradation. Jitter was further broken into its constituent elements using the jitter analysis software embedded in the oscilloscope.

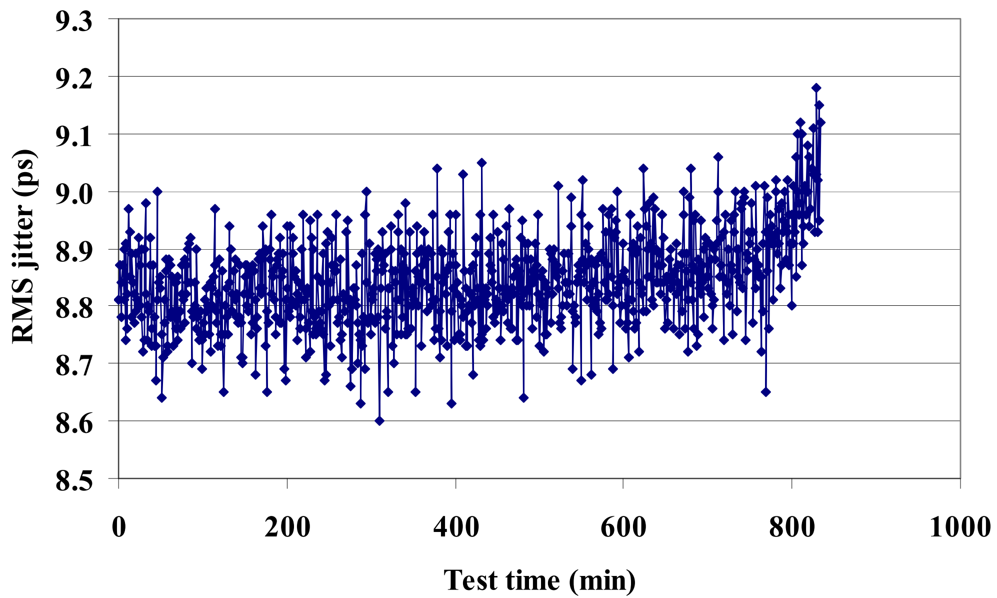
During fatigue testing, instrumental control software was used to instruct the oscilloscope to record the eye diagrams and the eye parameters once every minute. For each of these measurements about 150 waveforms were sampled and analyzed statistically. Each stress test was conducted until the cyclic stress resulted in the fatigue failure of one or both of the solder joints. The test results were displayed on a plot as a function of test duration in order to examine how each parameter changed during solder joint degradation.

3. Test results

Figure 45 shows the evolution of the selected eye parameters over the course of a fatigue test. The total duration of the test was 834 minutes, at which time one solder joint underwent complete separation. As shown in Figure 45, at the beginning of the test the eye height and the root mean squared (RMS) jitter values were observed to be about 0.228 V and 8.8 ps, respectively. However, starting from around 700 minutes both the eye height and the RMS jitter began to deviate from their initial values. The eye height decreased by 2% and the RMS jitter increased by 4% until there was complete separation of the solder joint. The remaining eye parameters—the rise time, the fall time, and the eye width—also showed a 5% increase, a 4% increase, and an 1% decrease, respectively, during solder joint degradation. Similar behavior was consistently observed over multiple trials using the same experimental conditions.



(a)



(b)

Figure 45 – Changes in (a) eye height and (b) RMS jitter during solder joint degradation

Figure 46 shows a photo of the partially separated solder joints taken after the conclusion of another fatigue test. In this test, the eye parameters were collected every two minutes in order to allow the jitter analysis software to decompose the jitter into its constituent elements. In spite of the partial separation, these solder joints were still capable of transmitting digital signals. This therefore represented an intermediate stage of solder joint degradation, after generation and propagation of cracks but prior to complete separation. The test was stopped at 54 minutes, which in this case was enough to generate partial separation of the solder joints. The overall test durations vary from test to test due to variations in the amount of solder and the fillet shape from sample to sample. Similarly to the results of the previous test, during solder joint degradation the eye parameters deviated from their initial values in response to physical cracking of the solder joints. Upon the partial separation of the solder joint, the ISI increased by 10 ps, as shown in Figure 47 (a). Although the DCD decreased by 3 ps, as shown in Figure 47 (b), this might be due to a minor re-allocation of jitter among the components precipitated by the step change in the jitter distribution. The net effect was an increase in the DDJ, the DJ, and the jitter by 7 ps. These test results indicate that physical degradation of an interconnect could adversely affect the performance of high speed electronics, even prior to the creation of an open circuit.

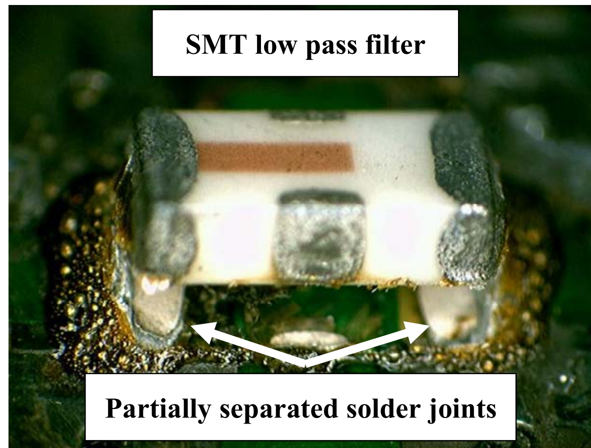
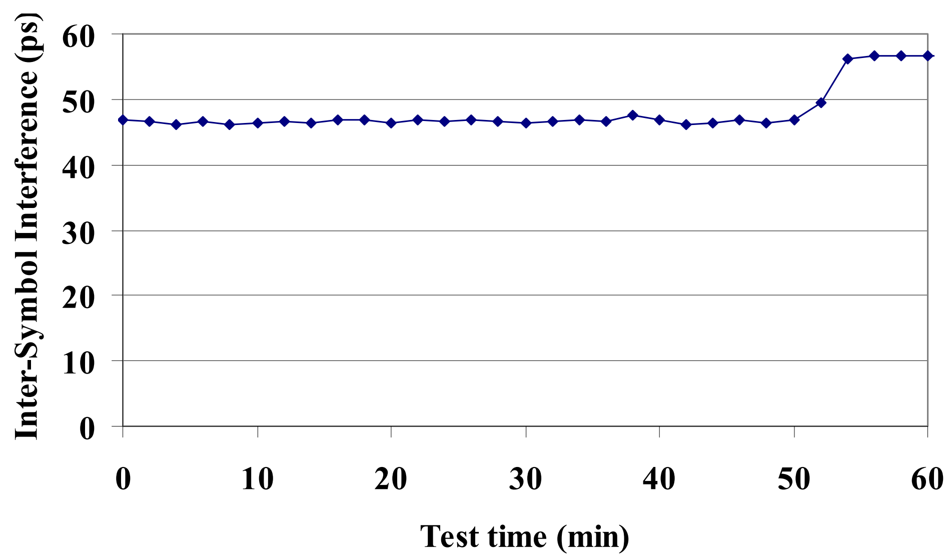
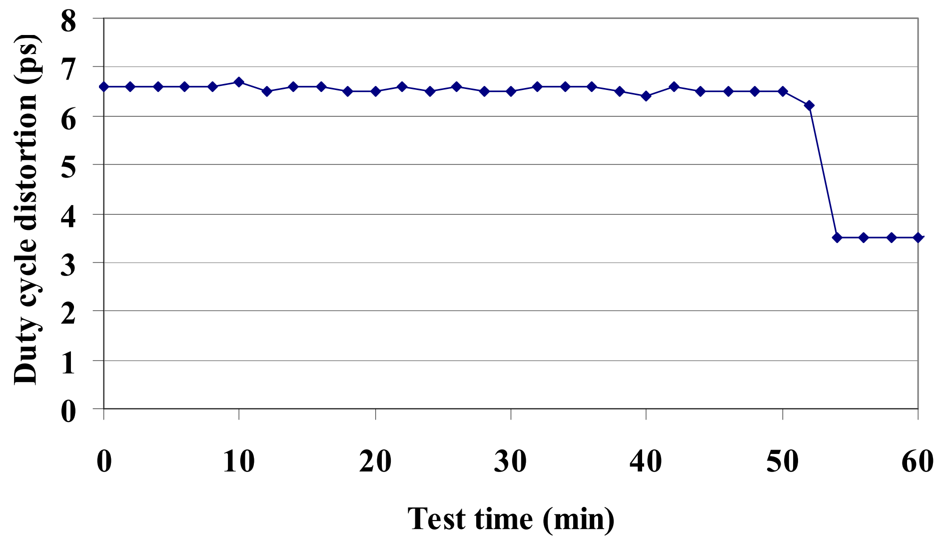


Figure 46 – Partially separated solder joint after fatigue testing



(a)



(b)

Figure 47 – (a) Inter-symbol interference and (b) duty-cycle distortion during solder joint degradation

4. Conclusions

It was demonstrated that digital signal characteristics exhibited measurable degradation due to intermediate stages of interconnect failure. Prior to complete separation, partial cracking of solder interconnects during cyclic loading led to changes in the eye parameters by 1% to 5% of their initial values. Eye height and eye width exhibited reductions near the lower end of this range, whereas rise time, fall time, and jitter all increased by 4 or 5%. The main contributor to jitter degradation was found to be inter-symbol interference. These test results were consistently observed over multiple trials, and support previous findings using analog signals; i.e., TDR reflection coefficient. Due to the skin effect, even a small crack initiating at the

surface of an interconnect raises the RF impedance and thus the TDR reflection coefficient. The skin effect also affects high speed digital signals. Therefore, physical damage accumulation in an interconnect deteriorates the signal integrity of digital signals.

The digital signal parameters responded to the accumulation of damage in the interconnect at about 87% of the total lifetime, defined as the time of creation of an open circuit. Considering the accelerated stress conditions of the experiment and typical expected lifetimes for electronic products, under normal operating conditions this early warning could occur a few days, weeks, or months before the system experiences total failure of the interconnect. With knowledge of these signal changes the user could have enough time to perform condition-based maintenance, which could increase the product safety and availability, and reduce operational and repair costs as well.

These results imply that traditional reliability monitoring methods may not be suitable for reliability assessment of high speed digital electronics. Interconnect reliability testing of electronic components and circuits is often performed by monitoring DC resistance of daisy chains. Whereas RF impedance and digital signal parameters have been found to change in response to damage accumulation prior to loss of continuity, DC resistance exhibits very poor sensitivity to such damage. For circuits whose performance is dependent on signal integrity, traditional DC-based methods may overestimate their lifetime. Digital signal parameters, on the other hand, are more closely related to system performance and thus may provide a better assessment of reliability. Detection sensitivity can be adjusted when the monitoring is

paired with statistical anomaly detection techniques. The discrepancies in predicted lifetime between DC and digital or RF reliability monitoring methods will only grow as data rates and signal frequencies increase.

Chapter 6:

Contributions and Future Work

1. Contributions

The contributions from this research are as follows:

- Developed a method for non-destructive electrical sensing of PWB interconnect failure mechanisms: solder joint cracking and pad cratering.
    - Demonstrated both theoretically and experimentally that TDR reflection coefficient can distinguish between two competing interconnect failure mechanisms during stress testing of interconnects.

- Determined and quantified the increased sensitivity of RF impedance compared to DC resistance in detecting early stages of PWB interconnect degradation by monitoring RF impedance and DC resistance in-situ.
    - Evaluated the effect of SAC305 and eutectic SnPb solders on changes in RF impedance and DC resistance due to solder joint degradation.

    - Demonstrated the ability of RF impedance to detect failure precursors as early as 53% of a solder joint total life.
    - Verified the relationship of changes in RF impedance to crack length within a solder joint using the equivalent circuit model.

- Developed a prognostic approach that can predict solder joint remaining life in real-time with a prediction error of less than 3% of total life.
    - Demonstrated a successful prediction of the time to failure of solder joints under cyclic mechanical stress conditions.

- Demonstrated adverse effect of PWB interconnect degradation on the performance of digital signal characteristics.

2. Potential impact

This study could be implemented to improve qualification of electronics. The main objective of qualification is to demonstrate that a product is capable of meeting or exceeding specified requirements. Accelerated testing often conducted to qualify the product by accelerating time-dependent failure mechanisms such as fatigue. In order to conduct an accelerated test, the following steps are commonly taken. First, all the possible failure mechanisms are identified. Based on the failure mechanisms, the load parameter that directly results in the time-dependent failure is chosen and its acceleration level is determined to generate the same failure mechanism that occurs

under the usage condition. According to the specified requirements for the product, accelerated tests are conducted, and the test results can then be quantitatively extrapolated to the usage condition to which the product might be exposed in the field. If the product meets the requirements according to the test results, it can be concluded that the product is qualified.

These steps for qualification take some time to be concluded. The current industry practice requires shorter time to market for a new product to be more competitive. Therefore, the industry should require a new approach in order to reduce the time for qualification. This study could provide an alternative approach to qualification. Using the detection capability of early stages of interconnect degradation, the health of the product under test can be estimated long before the failure. For example, in-situ monitoring of RF impedance during a qualification test can detect the presence of a partial crack, which eventually results in the failure of the product. Instead of waiting for the failure, the qualification test can be terminated upon observing changes in the RF impedance. The user then can make a decision whether the product is qualified or not before the product failure.

Also, this study can be used to uncover problems such as intermittent failure. Intermittent failure is the loss of function for a limited period of time. These failures are often reported to be a significant portion of warranty returns and field returns, resulting in economic losses in the industry. Under thermal cycling or vibration, the electrical continuity could exhibit intermittent behavior due to a partial crack on a solder joint. Appropriate detection of partial cracks during qualification could reduce the possibility to exhibit an intermittent behavior when the product is deployed in the

field. Also, detection of partial cracks during qualification could be used to improve the product design, which eventually reduce field failures, and thus increase the availability and reliability of the product.

3. Future work

Future work on this topic may involve an investigation of the challenges to take this approach from lab-controlled conditions to real-life conditions. The first challenge to be considered would be the effect of changes in the characteristic impedance of a circuit board. Many circuit boards in real-life are not designed for high speed applications, and therefore they are not impedance-controlled. In order to implement this study to non-impedance-controlled circuit boards, the detection sensitivity needs to be quantified using the metric such as signal-to-noise ratio. Since this approach is based on the relative changes of the RF impedance during interconnect degradation, it is required to evaluate if the changes exceed the noise floor in order to be detectable and measurable using a non-impedance-controlled circuit board.

Probing would be another challenge to be considered. In this study, SMA connectors were used to make both electrical and mechanical connection between a test vehicle and the RF cables for monitoring of the RF impedance, as well as the DC resistance. Alternatively, a probe may be used to make an electrical circuit, and a few probes for TDR measurement are already available commercially. For continuous monitoring, variation in contact resistance at the probing interface could become a factor that may adversely affect the RF impedance measurement. When a probe is

used to monitor the RF impedance during stress testing, repeatability in probing should be taken into account during experiment design process.

Similarly, repeatability in RF impedance measurement would be a factor to be considered. As pointed out previously, an RF impedance measurement can be affected due to bending of an RF cable or presence of an object that may interfere electromagnetic wave propagation. When this RF impedance approach is implemented for maintenance of a system where the health of an interconnect may not be continuously but occasionally monitored, the variation among the measurements should be taken into consideration. Taking an average measurement of a few consecutive measurements could be an option. It might be also desirable to have a post- processing algorithm that can filter out pre-defined environmental noises on the RF impedance measurement.

Another topic for future work may involve stress testing with components more representative of commercial products. Daisy-chained BGAs would be a good candidate to extend the feasibility of this approach toward real-life conditions. The RF impedance of a daisy-chain composed of a few corner balls can be monitored during stress testing and the responses at each solder ball can be extracted depending upon the design of the package such as pitch, solder ball diameter, and the monitored frequency range, which affects the measurement resolution. Under this setup, the analysis can be more challenging, because the reflection coefficient measurement of a solder ball in the back of the daisy-chain could be affected by that of a solder ball in the front. As the multiple solder balls are connected in series within a daisy-chain, the reflection coefficient at the solder ball in the back is not a function of the incident

voltage that the network analyzer generated, but a function of the transmitted (and reduced) voltage through the previous solder ball. This may reduce the detection sensitivity, as well as complicate the analysis.

A study on conductor size and shape would be also useful. The characteristic impedance depends on the geometry of a conductor, and the detection sensitivity may vary according to the relationship between the skin depth and the shape of a conductor. Moreover, according to the size and the shape of a conductor the characteristics of interconnect degradation such as crack propagation rate could differ from what has been observed in this study. These characteristics can be used to establish a physics-of-failure (PoF) model that can address the effect of physical properties of a conductor. This PoF model can be paired with the data-driven prognostics approach presented in this study in order to make this approach useful under a variation of interconnect characteristics. Thus, this approach can become a basis of fusion prognostics approach, and can be more generally applicable to various kinds of interconnects.

This study can be further studied to serve as a non-destructive indicator of physical damage within an interconnect by monitoring electrical signals. To this end, a direct correlation between changes in RF impedance and physical damage level such as crack size needs to be examined. This approach will allow the user to have an insight of the crack propagation process without applying destructive failure analysis to the device under test. In real-life more than one loading conditions are applied to the product simultaneously: for example, a product may be exposed to temperature cycling, vibration, and voltage bias conditions at the same time during its operation.

This condition can be hardly modeled, because it is very complicated to identify the interaction between each condition. However, the main contributor that leads up to interconnect failure is the physical damage accumulated to the interconnect. Therefore, with the relationship between physical damage and the electrical measurement, the RF impedance approach can provide a direct indication of the interconnect health, which could be also associated with the remaining life.

Appendices

1. *Journal Publications from Dissertation Work*

- Kwon, D., Azarian, M., and Pecht, M., “Early Detection of Interconnect Degradation by Continuous Monitoring of RF Impedance,” *IEEE Trans. on Device and Materials Reliability*, vol. 9, no.2, 2009, pp. 296-304.
- Kwon, D., Azarian, M., and Pecht, M., “Prognostics of Interconnect Degradation using RF Impedance Monitoring and Sequential Probability Ratio Test,” *International Journal of Performability Engineering*, vol. 6, no. 4, 2010, pp. 351-360.
- Kwon, D., Azarian, M., and Pecht, M., “Non-Destructive Sensing of Interconnect Failure Mechanisms Using Time Domain Reflectometry,” accepted to *IEEE Sensors Journal*.
- Kwon, D., Azarian, M., and Pecht, M., “A Method for Prognostics of Solder Joint Remaining Life in Real Time,” to be submitted to *IEEE Trans. on Industrial Electronics*.
- Kwon, D., Sotiris, V., Azarian, M., and Pecht, M., “Prognostics of Solder Joint Failure Using RF Impedance Analysis and Gaussian Process Regression,” to be submitted to *IEEE Trans. on Reliability*.

2. *Publications in Conference Proceedings from Dissertation Work*

- Kwon, D., Azarian, M., and Pecht, M., "Effect of Solder Joint Degradation on RF Impedance," *IEEE Workshop on Signal Propagation on Interconnect*, Avignon, France, May 2008.
- Kwon, D., Azarian, M., and Pecht, M., "Detection of Solder Joint Degradation Using RF Impedance Analysis," *IEEE Electronic Components and Technology Conference*, Lake Buena Vista, FL, May 2008.
- Kwon, D., Azarian, M., and Pecht, M., "Early Detection of Interconnect Degradation Using RF Impedance and SPRT," *IEEE International Conference on Prognostics and Health Management*, Denver, CO, Oct. 2008.
- Kwon, D., Azarian, M., and Pecht, M., "Identification of Interconnect Failure Mechanisms Using RF Impedance Analysis," *IEEE Workshop on Signal Propagation on Interconnect*, Strasbourg, France, May 2009.
- Kwon, D., Azarian, M., and Pecht, M., "Detection of Interconnect Failure Precursors on Tin-Lead and Lead-Free Assemblies Using RF Impedance Analysis," *IEEE Electronic Components and Technology Conference*, San Diego, CA, May 2009.
- Azarian, M., Kwon, D., and Pecht, M., "Use of Skin Effect for Detection of Interconnect Degradation," *International Symposium on Microelectronics and Electronics Packaging*, San Jose, CA, Nov. 2009.
- Kwon, D., Azarian, M., and Pecht, M., "Comparative Analysis of Interconnect Degradation Using RF Impedance and Event Detectors," *IPC APEX EXPO*, Las Vegas, NV, Apr. 2010.

- Kwon, D., Azarian, M., and Pecht, M., “Detection of Solder Joint Failure Precursors using Digital Signal Characteristics,” *IEEE Workshop on Signal Propagation on Interconnect*, Hildesheim, Germany, May 2010.

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