ABSTRACT

Title of Document: FABRICATION AND MODELING OF SILICON CARBIDE BIPOLAR JUNCTION TRANSISTORS

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The fabrication and modeling of Silicon Carbide (SiC) Bipolar Junction Transistors (BJT) and diodes for the development of high temperature power switches is presented. Silicon carbide processing including etching, implantation and ohmic contact fabrication are discussed. A 1-D computer model for SiC devices is developed that allows for temperature dependent calculations of current and potential in the device. The techniques that provide a unique ability to use either standard methods or the quasi Fermi method are provided. The modeled results are compared to experimental data and show very close correlation at room temperature but rapidly diverge at higher temperatures. Several temperature dependent variables that affect the model results are investigated to determine which calculations, if modified, would most improve the model accuracy. A perspective for future optimization of the model is given with an emphasis on the ability to calculate BJT currents.

FABRICATION AND MODELING OF SILICON CARBIDE BIPOLAR JUNCTION TRANSISTORS

By

Bruce Robert Geil

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Table of Contents

List of Tables

List of Figures

List of Equations

Chapter 1: Introduction

Silicon Carbide (SiC) has many advantages over silicon and is becoming the material of choice in power circuits and radiation hardened electronics. Due to its wide bandgap it can operate at high temperatures, high voltages, and high current. These advantages have not been fully realized due to challenges in material, and processing of SiC and circuit design challenges in the operation of SiC devices. This work will discuss the fabrication and modeling of silicon carbide devices, with an emphasis on the bipolar junction transistor (BJT).

Silicon carbide devices are being developed as a replacement for many of the devices currently produced in silicon. This includes vertical power devices, lateral logic and RF devices. This work will analyze power devices, which have special requirements since they need to operate at high voltages and current levels, and at temperatures in excess of 150 ºC. Many types of power devices will be discussed including the four that I have fabricated in silicon carbide.

1.1. Schottky and JBS Diodes

The simplest device that I have fabricated is the Schottky diode, which is just a metalized piece of silicon carbide. This design is not used in production due to poor reverse blocking characteristics and issues with reliability, but it is useful for process development. The next level of diode is the junction barrier Schottky (JBS) (Figure 1), which is used in applications up to 3000 V that do not require operational temperatures above 200 °C and is the current design used in commercial SiC diodes [1,2,3].

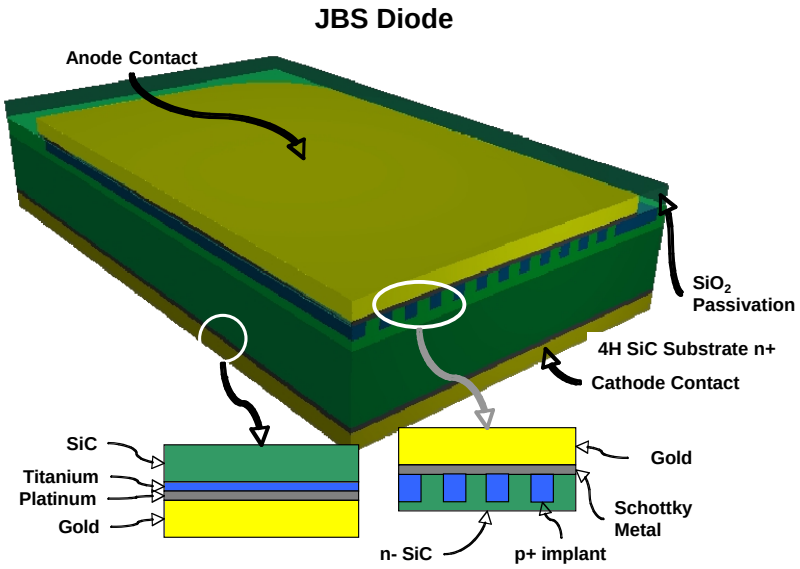


Figure 1 Junction Barrier Schottky Diode Cut-away

The JBS is a hybrid design that utilizes Schottky structures to provide low resistance in the forward direction and P-N diode structures to provide high reverse voltage. The JBS design has a lower forward drop allowing for more efficient operation.

1.2. PIN Diodes

Work has been done in SiC PN diodes but the JBS provides lower forward voltage drop for operation above 3000 V and when temperatures exceed 200 °C the P-I-N diode, shown in Figure 2, is the diode of choice [4].

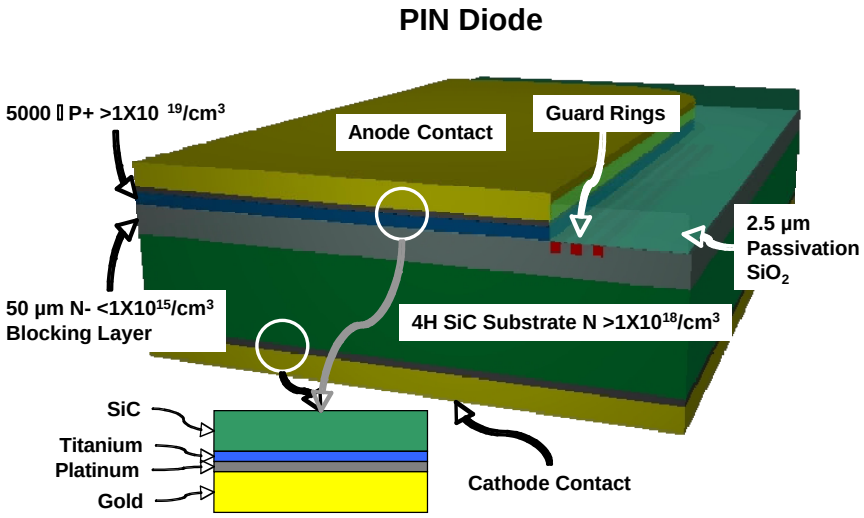


Figure 2 PIN Diode Cut-away

The P-I-N has a larger forward drop due to the thick epi layers required for operation at voltages above 3000 V. However, it is a minority carrier device which enables it to operate at higher temperatures then the JBS or Schottky diodes.

For power switching applications several different switches have been developed. Most of these are vertical power switching devices which include the junction field effect transistor (JFET) [5,6] and the vertical JFET or (VJFET), the insulated gate bipolar junction transistor (IGBT), the semiconductor controlled rectifier (SCR) or thyristor [7] and the metal-oxide-semiconductor field effect transistor (MOSFET).

1.3. Junction field effect transistors

The VJFET, shown in Figure 3, is the easiest to fabricate and is under development for low power switching applications such as gate drives [8]. The

VJFET is capable of handling higher current than the lateral JFET and is under development for power applications.

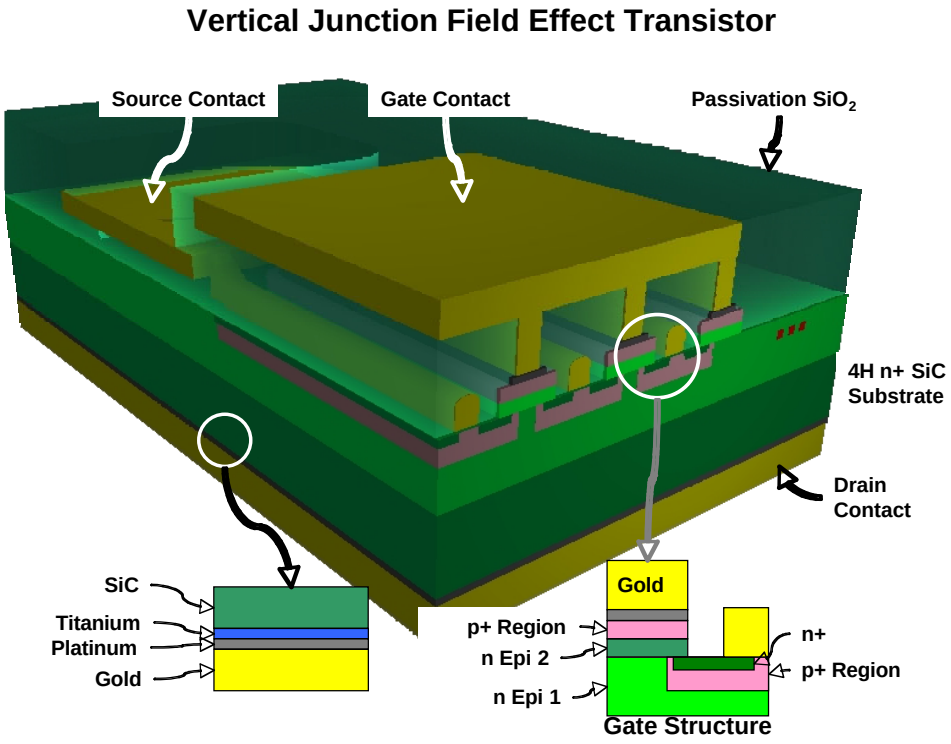


Figure 3 Vertical Junction Field Effect Transistor Cut-away

This is a normally on switch that utilizes a Schottky barrier contact to control the gate. These are simple devices with limited voltage capabilities that also require a holding voltage to turn the device off.

1.4. Bipolar junction transistor

Limitations in JFET devices are driving ongoing research which is being conducted to develop a BJT for power switching [9,10,11,12]. The modeling done for this work is focused on the bipolar junction transistor, which is a current controlled device. In silicon the BJT (Figure 4) the MOSFET and the related voltage

controlled IGBT make up the majority of switches used in power inverters and converters used for continuous power applications.

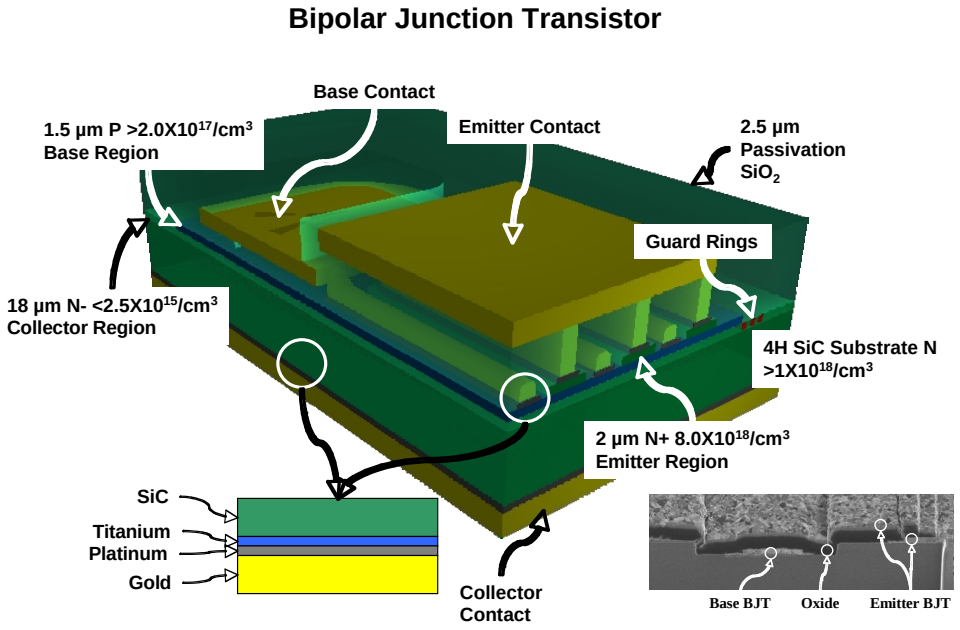


Figure 4 Bipolar Junction Transistor Cut-away

These three switches are non-latching devices that require current or voltage on the gate or base to remain on which makes them ideal for most inverters and converters for power conversion. BJT's provide very low forward drops of 2 volts or less and are well suited for power switching in both inverters and converters but the current controlled switching requires special drivers. IGBT's are a recent development, having been invented in 1982 [13], and are the preferred technology in silicon for most systems operating above a kilowatt. Limitations in the SiC oxidation process and drift issues in BJT's currently prevent fabrication of reliable IGBT's.

1.5. Thyristor

The other vertical switch studied is the thyristor shown in Figure 5, which is primarily used in pulsed power applications and high voltage applications. Thryistors are

current controlled devices like the BJT but differ in their ability to self-latch. The thyristor structure consists of 3 layers of epi material creating a 4-layer stack.

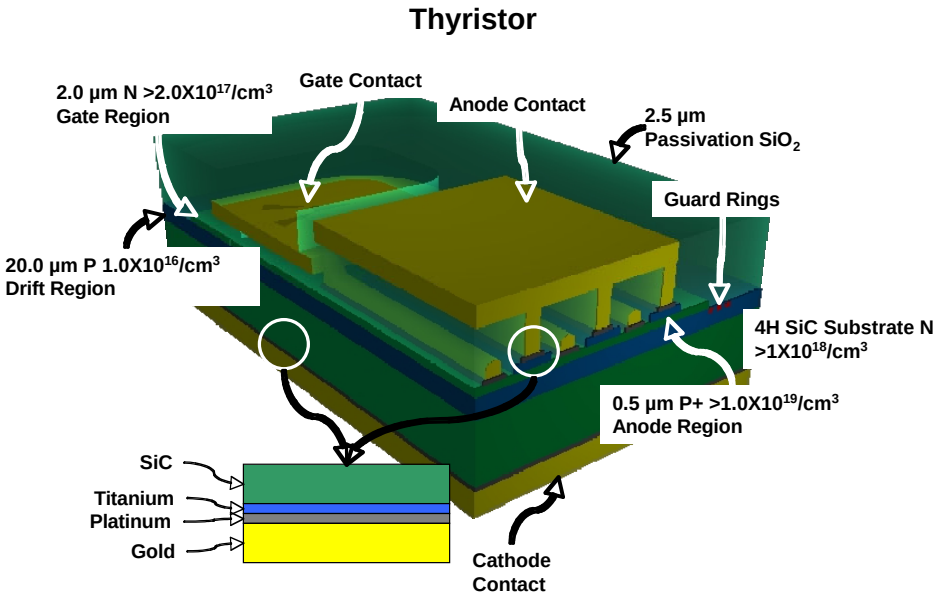


Figure 5 Thyristor Cut-away

This structure is the equivalent of two BJT's with a common connection between the base and emitter of one BJT and the base and collector of the second BJT. This creates a self-latching structure that once turned on will stay on until power is removed. This makes thyristors ideal for pulsed power applications that automatically remove power once switched. Some designs, including the ones that I fabricated, provide gate turn off capabilities with the ability to remove excess carriers through the gate turning the device off.

1.6. Metal oxide semiconductor field effect transistor

The MOSFET (Figure 6) [14,15,16], another device under development in SiC, provides a voltage controlled switching action making it much easier to control.

Most of the work in power MOSFET's in SiC has been in the development of double diffused MOSFET's (DMOSFET).

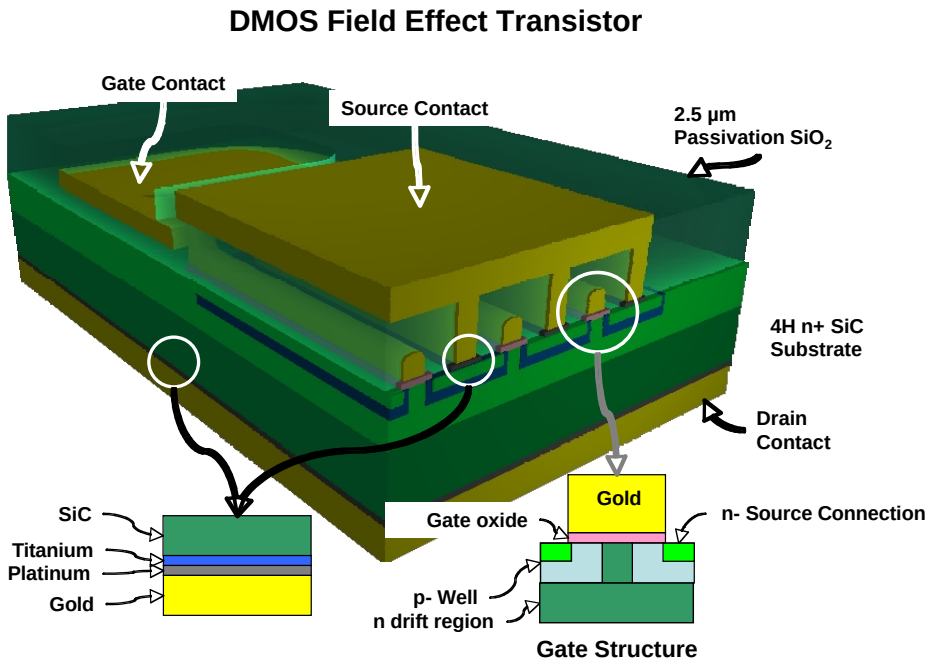


Figure 6 DMOS Field Effect Transistor Cut-away

Devices in this class include both the MOSFET and IGBT families of devices. These devices require an extremely clean oxide and for this reason they are very difficult to create in silicon carbide. Oxides for MOS structures need to be extremely pure, since contaminates trapped in the oxide or at the oxide semiconductor interface can cause shifts in the voltage characteristics of the device. These shifts reduce the reliability of the device and make the device difficult to control. These problems have been solved for silicon, allowing for the creation of everything from microprocessors with 100's of millions of transistors to IGBT's that can handle thousands of amps. The development of MOSFET's in silicon carbide presents a unique set of challenges in growing an oxide that has both a clean oxide/semiconductor interface and low levels

of trapped contaminates. During the oxide growth, carbon from the silicon carbide contaminates both the interface and the grown oxide creating charge centers located in the oxide and at the interface. Work is continuing in the development of processes that will remove the carbon from the oxide/interface. The current methods use oxygen and nitrogen post anneals at temperatures below the growth temperature to remove the carbon from the oxide. Currently, experimental MOSFET's have been produced using both lower power lateral designs and high power vertical DMOSFET's and the newest devices are close being put into production.

Chapter 2: Silicon Carbide Fabrication

2.1. Wafer Fabrication

SiC is a difficult material to work with and achieving low defect levels in large wafers has been a continuing challenge that has limited the availability of SiC devices. Several manufacturers, including Cree Research and Dow Corning semiconductor, are working on improved substrate materials and fabrication techniques. Silicon Carbide has over 200 different poly-types [17], which makes materials growth very difficult. Of these poly-types only 6-H, 4-H and 3-C are used in fabricating devices. To obtain wafers of a given poly-type requires a high quality seed crystal of the desired poly-type. Tight control of the growth process is required to prevent variations during the growth. Without this control, areas in the growth can have inclusions of varying poly-types thus limiting the size and quality of the boule. Due to this issue the first commercially available wafers were less then 1 inch in diameter and were produced using 6-H SiC. Improved processing has enabled 4-H SiC, currently used in most power devices, to be grown in diameters of up to 4 inches. 4-H SiC is preferred over 6-H SiC in power device work, due to its larger bandgap of 3.23 eV at 300 K [18]. There is some interest in using 3-C SiC as it can be grown on large area Si wafers because it is closely lattice matched to Si [19]. The use of the low cost silicon substrates and reductions in processing would reduce device cost. Constant improvement in the growth of large area SiC wafers has enabled commercially available 4 inch SiC wafers.

2.1.1. Substrate Defects

Better seed crystals have allowed economical growth of larger wafers and have continued to reduce the two killer defects that arise during growth [20]. The primary defects are micro pipes, caused by screw dislocations and inclusions that start at the seed crystal. These inclusions grow in the material and are generally killer defects in a device [21]. Through much work the major materials companies have reduced the micro pipe densities to below 15.0 per cm^2 and most of the remaining micro-pipes are at the edge of the wafer, allowing cost effective 1.0 cm^2 devices to be produced. While micro pipes have been the primary focus, work is now focusing on stacking faults, which cause long term reliability problems in bipolar devices. A stacking fault is a region in the device where the poly-type has changed from what was originally grown and occurs in devices fabricated from the hexagonal poly-types. Stacking faults occur at dislocations in the crystal and nucleate through the biased regions of the device [22]. In 4-H SiC power devices the stacking faults are comprised of 3-C SiC. Since 3-C has a lower band gap of 2.36 eV [18] the 3-C areas forward conduct at lower voltages under forward bias, which causes high current flow through this area. This current flow will then overheat the region due to resistive heating. Even if the heating doesn't destroy the device immediately, over time it can cause further nucleation of stacking faults thus changing the operational parameters of the device. The stacking faults also cause other instabilities in device operation including permanent reduction in BJT gain when operated under high voltage, temperature, or current. To reduce stacking fault effects most high temperature devices are specified for operation at reduced power and voltage.

2.1.2. Epitaxial Growth

While the base material is important for all SiC devices, vertical structure power devices require the growth of additional material layers with high levels of dopant activation. The preferred manufacturing method for these layers uses site-specific epitaxial growth. In this process, SiC epi-layers are formed using gases fed into a 2200 °C furnace. In most commercial processes the gases of choice are Silane to provide the Si and Propane to provide the carbon [23]. If no other gases are used, nitrogen in the air causes a light doped n-type material to be produced. To control the doping, gases containing aluminum for p-type and nitrogen for n-type are fed into the furnace. Dose control and activation are achieved by varying the silane and propane flow rates depending on the dopant type and amount required. For p-doped materials the aluminum replaces a Si atom in the lattice while nitrogen replaces a carbon atom for n type materials. This technique produces high quality layers with excellent activation of the Al. It can be difficult to obtain low level doping of n-type layers using this technique due to the limitation of the system vacuum levels allowing high ambient nitrogen levels in the furnace. It is possible to achieve doping concentrations below 5.0×10^{15} /cm^3 through compensation doping, better flow control, and improved sealing of the furnace [24]. The other challenge for high voltage devices is obtaining layers thick enough to provide the required voltage standoff. 4-H SiC has a breakdown field of between 3.0×10^6 V/cm and 5.0×10^6 V/cm [18], requiring thick layers of 100 (μm) or more to achieve the 10 kV hold off voltages necessary in many power applications.

2.1.2.1. Thick (> 100 µm) Epi Growth

The requirements for thick epitaxial layers cause further challenges in developing SiC devices. The fabrication of thick epi-layers is negatively impacted by particle contamination, which reduces layer quality and growth rate. This impacts the cost and layer quality of the material. Thick layers take many hours to grow and are dependant on accurate control of temperature and gas flow rates. To reduce cost and growth time the reaction rate can be increased through increasing the gas flow rate or through increased temperatures. Increasing the mass flow rate of the reaction gases increases the amount of reactants in the chamber. This increases the growth rate but can cause poor material quality and increased surface roughness through incomplete reactions that leave un-reacted materials and dangling bonds. If the temperature and mass flow rates are increased, the additional reactants will fully react which improves material quality. Increasing the temperature also increases the sublimation rate of the SiC which degrades the surface though loss of material. The surface morphology becomes worse with increasing layer thickness. To reduce roughness, while maintaining a reasonable growth rate, requires tight process control. Another challenge in epitaxial material growth is the ability to grow layers with doping concentrations greater then 1×10^{18} /cm^3. These highly doped layers are required to provide low resistance contacts and are particularly difficult to achieve in p-type materials. Do to the difficulty in activating implants, especially in p-type SiC, many device designs use an epitaxial deposited material to achieve reliable low resistance contacts to p-type material. Since the p-type dopant of choice in SiC is aluminum the size difference between the Si and aluminum causes the surface to get progressively

rougher as the layer thickness is increased. This problem can be minimized or eliminated by using a thin top layer of high doped material to create the contact or by progressively increasing the dopant levels during the deposition to create a gradient doping profile in the material.

2.1.2.2. Dislocation Reduction Methods

Until recently, the wafer was pulled from the furnace and checked after each layer was grown. This step caused additional defects and surface roughening, but was required since the furnace had to be cleaned between runs. Currently, processes have been developed that allow the continuous growth of layers even with changes in doping level and type. This has improved the performance and has been especially beneficial for the BJT and MOS-FET devices which need cleaner interfaces to prevent unwanted electron injection into the base and gates.

2.2. Device Fabrication:

2.2.1. Substrate and Epi Growth

The power devices developed at ARL are vertical devices for high current applications with the epi-layers designed to provide high reverse blocking voltages. All devices use an n type substrate with a doping concentration above 1 x 10^{19} /cm^3. The first epi layer is a buffer layer 0.5 to 5.0 μm thick grown directly on the substrate to provide a smooth surface for the epitaxial growth. The thickness of this layer is determined by a combination of substrate doping and carrier lifetime. The BJT requires a single buffer layer for the collector, but the thyristor design requires two different buffer layers. In the thyristor, the first layer is n doped to match the substrate while the second layer is p doped to provide a buffer for the following p

doped layer. Following the buffer layer, a thick layer is grown for the collector-base with the thickness based on the design requirement for the reverse bias voltage, which is graphically demonstrated in Figure 7.

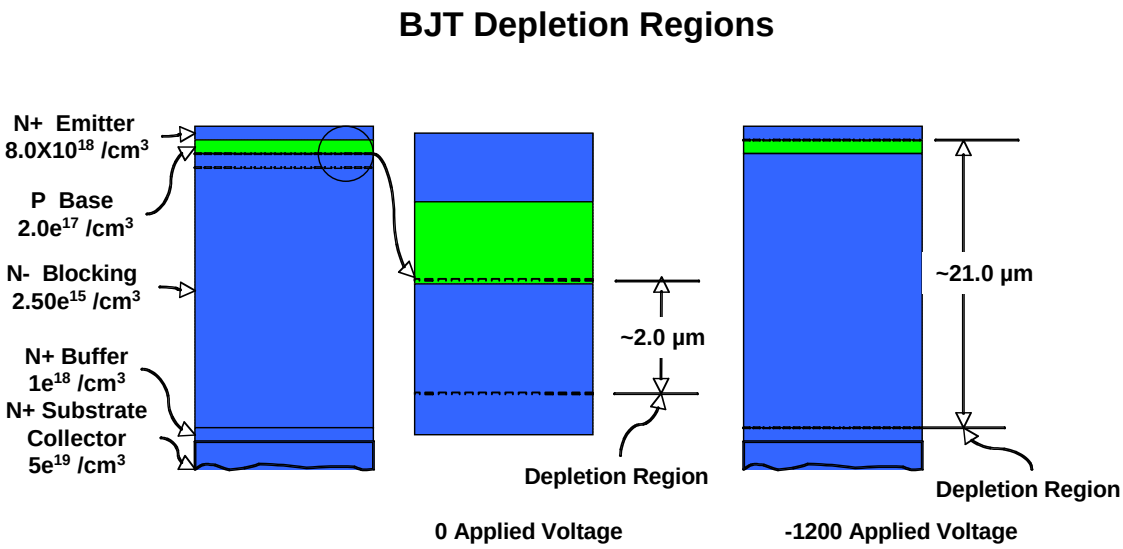


Figure 7 BJT Depletion Widths

To determine the required thickness for these layers standard calculations for depletion width are used [25].

$$Xn = \sqrt{2}\sqrt{\frac{E_{SiC}\,(V_{jct} - Va)}{q\,Na\,Nd\,(Nd + Na)}}\,Na$$

Equation 1 Diode depletion width N-side

and

$$Xp = \sqrt{2}\sqrt{\frac{E_{SiC}\,(V_{jct} - Va)}{q\,Na\,Nd\,(Nd + Na)}}\,Nd$$

Equation 2 Diode depletion width P-side

where

$$Junction\_Voltage = Vt\,\ln\left(\frac{Nd\,Na}{ni^2}\right)$$

Equation 3 Built in diode potential

The doping concentration of the blocking/collector region in the BJT's is kept low to provide proper blocking and to allow high efficient charge injection across the base/collector junction. In PIN devices, voltage blocking occurs in the n-type intrinsic layer with doping concentrations of 1 x 10^{15} /cm^3 or less. In the thyristor, the voltage blocking requirements determine the thickness and doping concentration of the p type first layer. The devices fabricated at ARL were designed to block 1200 V and required a thickness of 20 μm and a doping concentration of 2.5 x 10^{15} /cm^3. In the PIN device the second layer provides the top contact and is a p doped material on the order of 5000 to 7500 Å thick. To achieve low resistance contacts requires a graded doping profile to reduce roughness with the doping level increasing above the 1 x 10^{19} /cm^3 level as the layer is grown. In the BJT the base region consists of a p-doped layer 1.5 μm thick with a doping concentration of 2.5 x 10^{17} /cm^3. The thyristor has a similar 1.25 μm thick n-type 2.5 x 10^{17} /cm^3 layer used for the gating layer. Improvements in growing these layers have improved device operation and reliability. These advances have been realized through recent developments in epi growth that have enabled the ability to grow continuous layers with a thin transition between each layer. This reduces defects and stack faults that cause unwanted voltage shifts and premature device failure. A final layer is grown on top of the thyristor for the top anode connection and on top of the BJT for the emitter. In the thyristor this layer has the same specifications as the final layer used on the PIN devices since this layer will provide the high current, low resistance contacts. In the BJT, the top layer is 2.0 μm thick with a nitrogen doping concentration of 8.0 x 10^{18} /cm^3. All of these devices consist of 5 to 10 masking steps which include mesa

creation, gate or base contacts, guard ring fabrication, contact implants, oxide thinning, contact metalization, metal overcoats, via opening, and contact openings.

2.2.2. Initial Substrate Processing

Figure 8 shows the interdigitated design used for both the BJT's and thyristors. This design was chosen over other designs such as the involute due to its simplicity in layout and fabrication and its scalability. Simply adding additional fingers can enlarge the design and the bonding pads can be sized according to the size of the wire used for packaging.

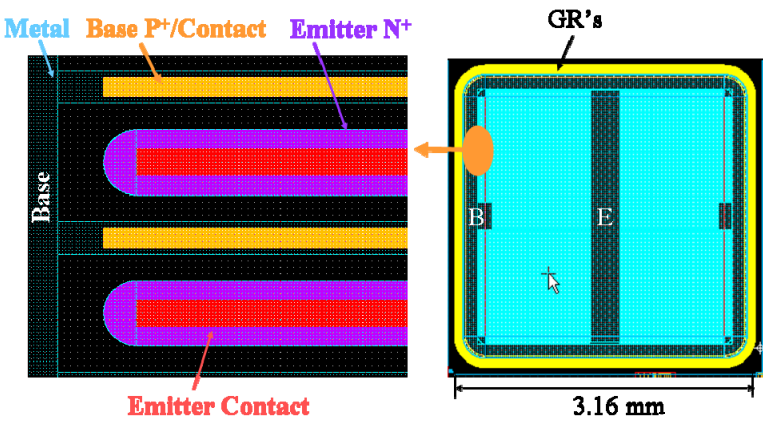


Figure 8 BJT Design

The process starts with the purchase of SiC wafers from Cree that have the required epitaxial layers already grown on the substrate. After receiving the wafers, each is visually inspected and then cleaned using a version of the RCA clean. This cleaning process was developed by RCA back in the 1960's to prepare wafers for gate oxide growth [26]. The purpose of this clean is to remove organics and trace metals from the surface of the wafer. The first step of this cleaning procedure consists of either a 7:1 buffered HF NH_3F:HF or a 10:1 Di:HF dip to remove the native oxide that forms on the wafers. Following this, the wafers are subjected to a 15 minute

piranha clean which is a 3:1 mixture of sulfuric acid and hydrogen peroxide used to remove the organics. The HF dip is then repeated after every process to remove any oxide that has grown on the wafer during the piranha clean. From here the wafer is moved into a 10:3:3 mixture of de-ionized water, hydrochloric acid, and hydrogen peroxide that is heated to 110 °C to remove surface heavy metals. The final two processes consist of a 10:3:3 mixture of de-ionized water, ammonium hydroxide, and hydrogen peroxide which is used to grow very thin layers of oxide on the wafer. The oxide etch removes this oxide, which removes any impurities with it and helps to smooth the surface. This oxide growth step is not as efficient at removing impurities in the silicon carbide when compared to silicon. This is due to the difficulty in converting the silicon carbide into silicon dioxide. This limitation requires a modified RCA clean, where the last step consists of a 20 minute clean in a bath of aqua regia made up of 3 parts hydrochloric acid and 1 part nitric acid that is heated to 120 °C. Most metals and organics are removed using this clean step and it is the last cleaning step done on the wafer before it is rinsed in de-ionized water.

2.2.3. Mesa Etch

The power devices fabricated here are based on a mesa isolation process. The first fabrication step is creating the mesa. For the PIN devices this is the only etch, while the BJT and thyristors require two etches: one to reach the contact region for the base or gate and the other to provide isolation. The most common etch technique for SiC is an inductively coupled plasma (ICP) etcher or, in the case of these devices, an older electron cyclotron resonance (ECR) etcher [27]. Both of these systems allow ion-enhanced etching where the plasma and substrate bias are independently

controlled. This decoupling of plasma and substrate bias is critical. Because SiC is such a tough material, much of the etching is accomplished through the kinetic ion etching action created through the biased substrate. This kinetic, or ion etching, process provides the highest etch rates, but also provides several challenges in developing a process. Since material removal is based on mechanical processes, masking materials are also removed at a high rate.

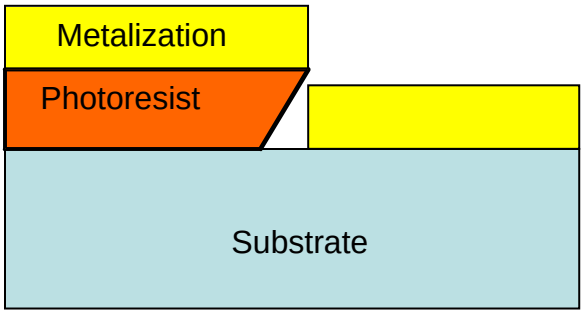
2.2.3.1. Masking

Process limitations on mask thickness and etch depth requirements limit mask materials to hard masks such as metals and nitrides. These masks have issues with re-deposition. This occurs when the where mask material that was removed through the sputter etch process re-deposits on the portion being etched. This re-deposition causes small areas to be masked resulting in roughening and blackening of the etched surface. This rough surface causes breakdown failure in the device due to high fields at the tips of the micro-masked areas when a bias voltage is applied to the device. Once micro masking has occurred, the wafer is destroyed and becomes unusable. The ECR used for these devices operates at 150 °C which further limits the choices of masking material. To overcome these limitations several masking materials were evaluated including aluminum and indium tin oxide (ITO). Early work was done using aluminum but problems with micro masking, temperature stability and mask damage could not be overcome. Aluminum is used for some thin etches in a couple of designs. To overcome these problems and allow the temperatures required for this etch, an ITO mask was used. ITO masks can be used at temperatures exceeding 200

°C and they etch at a rate 100 times slower than that of SiC. ITO does not sputter etch as badly as aluminum, reducing the amount of micro masking.

2.2.3.2. Liftoff Process

The ITO is patterned using a liftoff process, which uses a negative resist applied and patterned before the ITO is deposited. Negative resist is preferred for liftoff processes because it provides a reentrant profile.



Reentrant Profile

Figure 9 Re-entrant photoresist profile

This profile prevents the exposed sides of the resist from being coated by the ITO providing a cleaner liftoff through reduced tearing along the edge. The uncoated edge also provides a path for the solvents to attack the resist during the liftoff process.

2.2.3.3. ITO Application

The coating process starts with a 30 second oxygen plasma de-scum to remove any photoresist residue that could affect the adhesion of the ITO. The ITO is applied using an RF sputter system with a target thickness greater then 1000 Å. Most liftoff processes use evaporators for deposition since RF sputter deposition systems provide very good sidewall coverage, which hampers the liftoff process. Since ITO cannot be easily deposited using evaporation, special care was taken to achieve acceptable results with sputtered ITO. Keeping the ITO layer as thin as practical and

using an ultrasonic solvent bath kept edge roughness of the patterned ITO within acceptable limits. Once patterned, the SiC is ready for etching.

2.2.3.4. Mesa Etch Process

2.2.3.4.1. Process Chemistry

The etch processes for SiC utilize the same gases that are used to etch silicon. In processes using the ICP, sulfur hexafloride (SF_6) provides the fluorine ions used in removing the silicon. Since these devices are processed on the ECR system the gas of choice is carbon tetrafloride (CF_4), which provides the fluorine needed to etch the silicon. CF_4 provides a cleaner, less time consuming process through the elimination of sulfur deposits in the tool [28]. The disadvantage of using CF_4 is that it has recently been categorized as an ozone depleting material, which makes it more difficult to obtain, and it introduces additional carbon into the system. Etching of the SiC creates additional carbon when combined with the carbon supplied by the CF_4 can cause a layer of carbon to develop on the device reducing the etch rate. To prevent carbon buildup, 4.0 % O_2 is introduced into the etch process to convert the carbon to CO_2 and CO allowing it to be removed [29]. To achieve a clean, high rate etch requires careful control of the chemical and mechanical etch processes.

2.2.3.4.2. Smooth Sidewall Etch Process Gate/Base Etch

The mechanical etch process is important in SiC to provide fast etch rates and smooth sidewalls, but causes trenching to occur along the bottom edge of the mesa. This trenching is depth dependant and increases with increasing etch depth. The sputter yield of the ion causes increased ion scattering along the sidewall edge leading to faceting and trenching [30]. To eliminate the trenching caused by the mechanical

etching the etch process is accomplished through the use of multiple etch steps. The first utilizes high substrate bias to provide a smooth sidewall at the start of the process. After etching to a depth of 1000 Å, the process is switched to a lower substrate bias, which provides a slower etch rate but reduces the trenching affect. This slower etch continues to maintain the smooth sidewall that was started during the initial etch. Utilizing this process the ECR yielded an etch rate of approximately 2 µm per hour. The ITO mask is removed using a 120˚C 1:1 Di H_20:KOH bath. In the PIN, this etch provides the mesa isolation and in the BJT and thyristor it is used to uncover the base or gate contact region. The completed etch has a profile demonstrated in Figure 10.

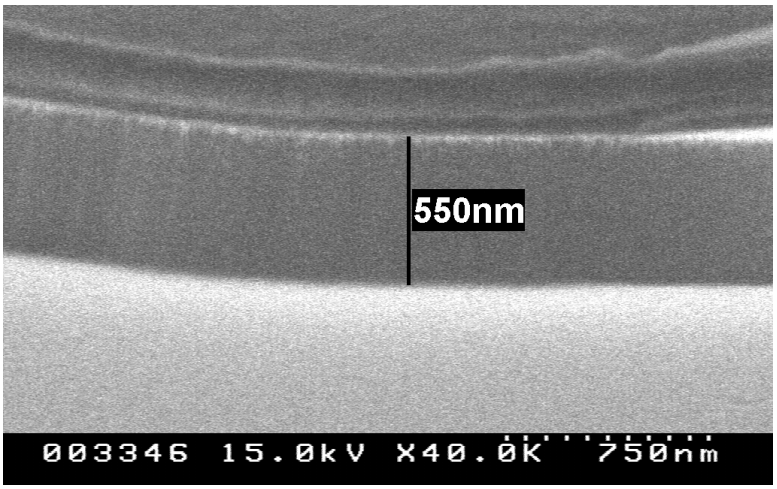


Figure 10 Profile of Gate/Base Mesa

2.2.3.5. Isolation Etch

The mesa isolation in the BJT and thyristors is achieved through a second etch that utilizes the same process with deeper etch depths and mask patterns. Figure 11 shows the results of the deeper isolation etch. The vertical ridges are caused by edge roughness in the photoresist and do not affect the performance.

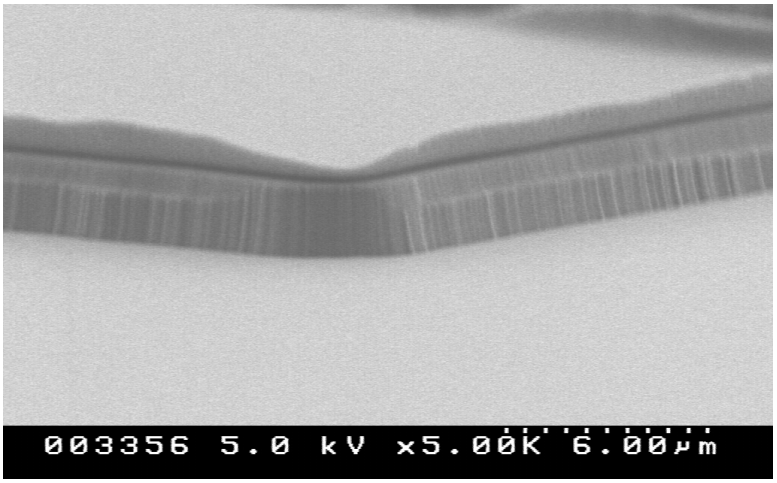


Figure 11 Post Etch Isolation Mesa with ITO Mask

2.2.4. Contact Implantation

Once the mesa etches are completed, the hard mask is removed and the sample is cleaned in preparation for the contact and junction termination implant [31]. In the BJT's and thyristors this implant increases the doping in the gate and base regions to provide good ohmic contacts. Since this implant is of the opposite type then that of the substrate material it can be used to terminate the fields at the bottom of the mesa.

2.2.4.1. Junction Termination Description

Several types of junction termination, including guard rings, junction termination etch and plate field termination methods, are available with each having advantages and disadvantages in performance and ease of processing [32]. The two techniques studied for these devices consisted of the guard ring and junction termination extensions. The guard rings consisted of implanted rings radiating out from the edge of the mesa [33]. The JTE utilizes a single large area implant that covers a similar region as the guard rings [34,35]. The JTE can be improved through

multiple smaller low dose implants over each previous implanted area. This technique provides very good termination, but requires multiple masks and implants steps, increasing time, cost and potential defects. The guard rings require a single implant but have smaller dimensions and tighter design tolerances than JTE's. Both of these techniques were computer modeled to determine the number of rings, ring spacing and implant dose. Guard rings were chosen for this work since the use of a single implant reduces process time, although this did lead to some challenges in patterning the guard rings due to the tighter design tolerances. The guard rings are at the bottom of the isolation mesa causing focus problems with the other areas being patterned. Changes in the pattern design and careful control of the aligner focus produced usable results. The 1200 V devices required 10 guard rings, 5 microns wide, on 3 micron spacing to provide adequate performance.

2.2.4.2. Dose and Energy Challenges in SiC

The implant energy and dose are calculated using SRIM [36] (Stopping and Range of Ions in Matter) from the implant profile and concentration provided by the guard ring models. SiC is difficult to implant due to the ion implant species used and the temperatures required to achieve activation of the dopants [37]. The implant process requires mask materials that can stop high-energy ions while dopant activation requires 800 °C implant temperatures.

2.2.4.3. Implant Mask Development

To meet these requirements a hard mask is necessary. The hard mask is created using a liftoff process similar to that used in the SiC mesa etch. Once the photo resist is patterned, the hard mask materials are applied to the wafer and the

photo resist is lifted off. The hard mask further reduces the accuracy of the pattern transfer due to the additional mask thickness and processing. The implant mask must be thick enough to stop the implant species while withstanding high implant temperatures. To achieve this, a stacked mask consisting of a 500 Å titanium glue layer, a 500 Å platinum barrier layer, and a 7500 Å gold overcoat was developed. The gold thickness was determined from the implant energy level through the use of SRIM. Gold provides good ion stopping due to its density and it has the ability to handle the high implant temperatures. However gold's high sputter etch rate, when subjected to bombardment by ions such as aluminum and nitrogen, causes mask thinning during the implant. To limit mask thinning and provide a visual confirmation that the mask survived the implant, a final 500 Å layer of platinum is applied. Due to the cost involved in operating a specialty implanter, all implants are done at a commercial facility. This process usually takes about two weeks and once the devices are returned the hard mask is removed.

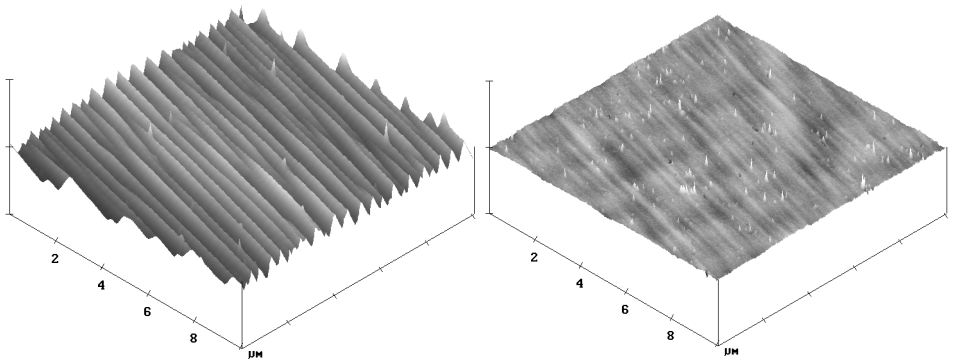
2.2.4.4. Mask Removal

Very few chemical etches will remove platinum but the same aqua regia process used in the RCA clean will completely remove both the gold and platinum. To remove the titanium a 30 sec submersion in 10:1 Di:HF is used. The wafer is then cleaned using the RCA clean in preparation for the implant anneal.

2.2.5. Anneal

The implant requires a high temperature anneal to complete the activation started during the implant process. The high temperature implant does not fully activate the dopants but does reduce the temperature needed for this anneal. The

activation anneal for nitrogen doped materials requires the wafer to be annealed at 1500 °C for 15 minutes. At these temperatures the silicon can start to sublimate out of the SiC leaving a rough surface (Figure 12).



Uncapped Anneal Capped Anneal

Figure 12 Post Anneal Comparison Uncapped versus Capped SiC

This also causes the dopants to evaporate out of the material.

2.2.5.1. Sublimation Reduction Methods

2.2.5.1.1. Basic Methods

Several techniques have been studied to reduce this problem. The earliest method used a blank SiC wafer placed face down on the sample being annealed. This causes excess silicon in the furnace, which increases the partial pressure of silicon in the area between the two wafers and provides a slight reduction in the roughening. To further reduce roughening, some groups, including the University of Mississippi and the University of South Florida, are introducing silane (SiH_4) into the anneal furnace to increase the partial pressure of silicon [38]. This method shows additional improvements over the wafer technique but does not prevent loss of dopant ions due to evaporation. Safety considerations prevented the use of this method in the ARL furnace.

2.2.5.1.2. Hard Cap

To overcome this limitation and the loss of dopant atoms additional research into other methods utilizing a capping layer was done [39]. The development of cap based processes require materials that can withstand the high temperatures without damage to it or the silicon carbide wafer while being easy to remove following the anneal. Aluminum nitride, while difficult to apply, was found to provide protection up to 1600 °C and could be removed using a hot Di:KOH etch. The use of carbonized photoresists has advantages over the AlN and is the current technique of choice for capping SiC. In this method, a layer of photoresist is applied to the wafer and then heated to 700 °C which produces the carbon cap. This carbon cap withstands temperatures in excess of 1700 °C but crystallization of the cap at high temperatures causes problems with the removal of the cap following the anneal process. Usually, standard oxygen plasma processing is used to remove the cap but crystallization of the cap prevents the plasma from removing the mask. The carbon is also oxidized in the presence of oxygen limiting this method to non-oxidizing atmospheres. Both the AlN and carbon masks were studied, but the AlN process was chosen for these devices due to problems with the carbon crystallizing. The AlN process uses either the laser deposition system or the RF sputtering system, located at the University of Maryland, to apply a 5000 Å layer of AlN to the wafer surface.

2.2.5.2. Annealing Process

Annealing was done in an RF induction furnace using an ambient of either argon or nitrogen. Nitrogen reduces damage to the AlN layer at higher temperatures, but argon is preferred to prevent damage to the furnace chamber. To further reduce

damage to the cap, the furnace is put under vacuum to remove excess moisture and reduce the ambient oxygen levels. After 5 minutes of vacuum purge the pressure is brought up to 400 Torr using the argon. The system is then ramped to 1500 °C over a 10 minute period to prevent thermal shock to the device. Once at 1500 °C the sample is annealed for 15 minutes and then slowly cooled back down to ambient over a 45 minute period. A quick visual check of the cap is performed before removal using a 110 °C 45% KOH solution.

2.2.6. Passivation Oxide

Following the anneal the devices are prepped for a passivation oxide. This oxide provides electrical passivation of the surface and protection from atmospheric contaminates. First, an RCA clean is performed to provide the extremely clean surface needed for the oxide growth. Samples are shipped to an outside firm, because ARL's oxide process is not clean enough.

2.2.6.1. Sacrificial Oxide Growth

Once the company receives the devices they go through another RCA clean followed by a sacrificial oxide grown using a pyrogenic steam process. The pyrogenic process uses hydrogen and oxygen which are introduced into a furnace operating at 1150-1200 °C [40]. The hydrogen and oxygen react with the silicon carbide surface to form the oxide. Approximately 8 hours is required for this process, and it yields an oxide thickness of 500 Å. This layer is then removed which reduces surface roughness and provides a clean surface.

2.2.6.2. Passivation Oxide Growth

A modified version of this oxide process is used for the passivation growth [41]. The modified process follows the standard oxide growth, which is then followed by an insitu 900 °C nitrous oxide NO_2 anneal [42]. This nitridation step removes the carbon trapped in the oxide during the growth, reducing both mobile and fixed oxide charges. Interface improvements are also realized through the reduction of carbon at the interface. Since the 500 Å oxide layer does not provide the 1200-1500 V hold off, a deposited oxide is used to increase the thickness [43].

2.2.6.3. Deposited Passivation Oxide

To achieve the 1200 V required, a standard thickness of 2.5 μm is used. Deposited oxides differ from grown oxides in that the silicon needed for the deposition is provided in gaseous form thru the introduction of silane (SiH_4) into the system [44]. In this process, a low pressure chemical vapor deposition (LPCVD) system is used to combine the silane and oxygen together to create the oxide [45]. This technique allows much thicker oxides to be deposited more rapidly, but with a much lower density and higher levels of hydrogen contamination from the breakup of the silane. Reduction of this hydrogen contamination is achieved by annealing the sample in an oxygen rich environment at 900-1100 °C increasing the density of the oxide and reducing the number of contaminants in the oxide. Finally, to help reduce post oxidation heavy metal contamination, a 1000 Å layer of silicon nitride is deposited on the top surface [46]. This layer is produced using silane and nitrous oxide in a LPCVD system.

2.2.7. Oxide Thinning

After 3-4 weeks of processing, the device is returned and photoresist is applied and patterned to thin the oxide over the active regions of the devices. This step is required since etching via openings and spinning resist over 2.5 μm thick structures is extremely difficult since the resist will remain in the via's after spinning and can not be properly exposed and developed. To thin the oxide, a photoresist mask is used to expose the top part of the mesa to an ICP etch that utilizes SF_6 or CF_4. Process time is determined by the amount of time it takes to thin the oxide to a thickness of 5000-6000 Å. Following the topside thinning, the device is placed in the ICP etcher upside down to remove any oxide grown on the bottom of the wafer.

2.2.8. Via Etch

The creation of via openings are required for the BJT and thyristor devices. The n-type contacts are done first due to the higher process temperatures required for the n-type contacts. These via's create the gate contact opening for the thyristor and the emitter contact in the BJT. The process is the same for both devices, with a photoresist mask used to define the regions and then an SF_6 based plasma oxide etch is used to remove the oxide down to the SiC [47]. If done correctly this etch allows the photoresist to be used as the liftoff mask for the metallization step. If problems occur, the mask is removed and a new mask is applied using the same mask and process. This causes misalignment between the via and contact metal which can increase contact resistance and increase the potential for shorted contacts.

2.2.9. N-Type Contact Formation

N-type contacts are formed using a nickel layer 1000 Å thick that is evaporated onto the sample and then patterned through the liftoff of the photoresist [48]. Once the front side contact is completed, the sample is inverted and the backside is also coated with 1000 Å of nickel. For the PIN devices only the backside is nickel coated. Once patterned the contacts are annealed using the implant anneal furnace since its vacuum atmosphere reduces oxidation of the contact metals. The nickel process varies from the implant anneal process and starts with a vacuum purge of the system for about 5 minutes. The pressure is then brought up to 400 torr for 5 minutes using argon to further purge any remaining oxygen from the system. While these steps help to reduce the oxygen in the system there is still moisture on the surface of the device. The moisture also oxidizes the sample and must be removed. This is achieved by heating the sample to 700 °C at a rate of 100 °C/min. The sample is held at 700 °C for 10 minutes and then the furnace is brought up to the anneal temperature of 900 °C using the same 100 °C/min ramp rate. The anneal requires 5 minutes and then the furnace is allowed to slowly cool back to ambient which requires 45 minutes since forced cooling is not possible with this furnace.

2.2.10. P-Type Contact Formation

Following the n-type contact formation on the thyristor gate and BJT emitter, the p-type contacts on the thyristor anode and the BJT base and PIN diode contacts are created using the same process. First, the via's are opened up using a photoresist mask and the oxide is removed down to the silicon carbide using a SF_6 based plasma etch. Once the via is opened, a 1000 Å thick layer of evaporated titanium is applied. For these devices titanium was used as the contact metal since the silicon carbide was

doped above 5.0 x 10^{19} /cm^3 [49]. For p-type contacts that are doped in the 5.0 x 10^{18} /cm^3 to 5.0 x 10^{19} /cm^3 range the preferred contact material is a combination of 90% aluminum and 10% titanium [50]. Aluminum/titanium provides more consistent contact resistance but the contact resistance is generally higher by a factor of 2. The improvement in resistance provided by the titanium is demonstrated by the reduction of forward drop shown in Figure 13. Titanium is more susceptible to oxidation then nickel so the process is modified to further reduce the moisture level in the furnace. Titanium is annealed at a lower temperature then the 900 ˚C used in the nickel process. To reduce the oxygen level, while preventing unwanted reactions, the furnace is brought up 400 °C following the standard pump down and argon purge. After holding at 400 °C for 15 minutes the furnace is brought up to the 600 °C for 5 minutes and then allowed to cool for 45 minutes.

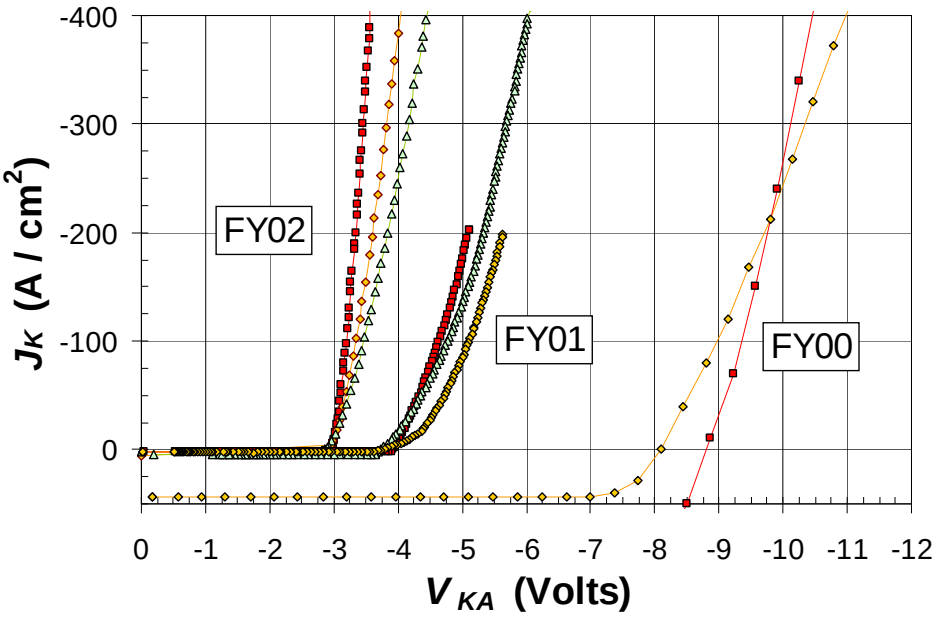


Figure 13 Contact Resistance Improvements on Forward Voltage Drop in a Thyristor

2.2.11. Gate/Base Overcoat Application

While contact metals provide a good ohmic contact to the material they cannot handle the design current of these devices, nor will wire bonds properly adhere to them. To achieve high current capability and provide a suitable surface for wire bonding an overcoat metal is applied to the contact metal. For the BJT and thyristor a photoresist mask is applied that opens up the gate or base fingers for overcoat application. Overcoat of these devices consists of a three-layer stack composed of titanium, platinum, and gold. Titanium provides good adhesion to oxides and metals which is critical in situations where the contact metals might be oxidized. Only 500 Å is required to achieve a good bond. Platinum bonds well to both nickel and gold, and provides a high temperature barrier between the titanium and the gold. As with the titanium, only 500 Å is required. For the BJT's and thyristors the gold is applied to a maximum thickness of 5000 Å, while the PIN diode is coated with 1 to 4 μm. The BJT and thyristor overcoat thickness is kept thin to reduce problems during the second overcoat over the anode and emitter. The layer thickness of the gold can be increased if high currents or large diameter wire bonds are used. Some groups replace the titanium/platinum stack with a chrome adhesion layer, which provides reasonable adhesion and operating temperature at a lower cost. This process requires additional processing to ensure the chrome is not oxidized during deposition. Oxidation of the chrome reduces adhesion and increases contact resistance. The stack materials are put down using an e-beam evaporator and are deposited without breaking chamber vacuum to improve the purity of the materials and reduce interlayer contamination. Following the overcoat application a liftoff procedure is used to

remove the photoresist leaving the stack over the gate or base fingers. In the case of the PIN the top metallization process is complete at this point. Figure 14 is a micrograph of the gate and anode finger region of a thyristor. The BJT finger region has an identical structure to that shown in Figure 14.

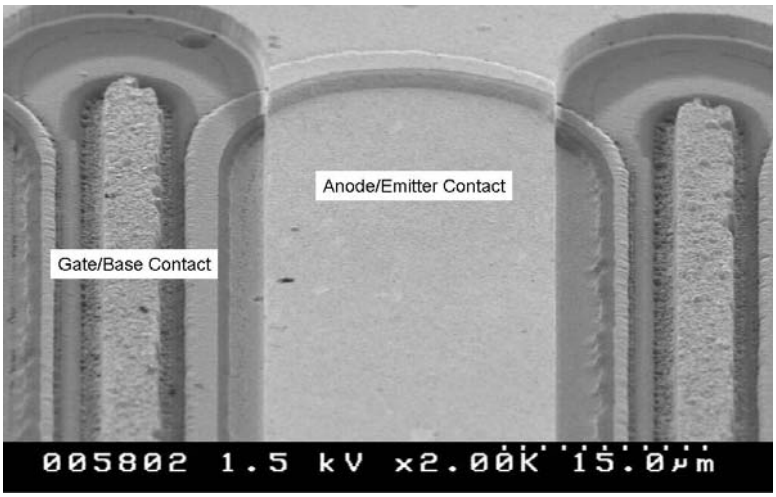


Figure 14 Gate and Anode Finger Micrograph

2.2.12. Emitter/Anode Overcoat Metallization

Thyrsitors and BJTs require a second metal process to provide contact to the anode or emitter and to further thicken up the gate/base contact pad. This second layer also connects the emitter or anode fingers together. To prevent shorting between the gate/base and anode/emitter layers, a layer of dielectric is applied to the device following the gate/base overcoat. Two of the most commonly used methods to achieve this are a deposited oxide process or a polyimide process. Some manufacturers utilize a polyimide layer for this step, which is cheaper and requires fewer process steps. The major disadvantages include reduced temperature operation, and problems with moisture absorption and swelling. The oxide method used in fabricating these devices uses a 1 μm thick layer of oxide deposited using a LPCVD

system. This layer is not densified as it was with the passivation oxide since the metals cannot handle the high temperatures and corrosive atmosphere needed for the densification process. Once the oxide is deposited, a photoresist mask is applied to expose both the emitter/anode fingers and the gate/base bonding pads. The same three-layer process is used, but a 2 μm and 4 μm layer of gold is used depending on the size of the device. This increased thickness requires a different negative resist to provide proper liftoff. This final topcoat is often fabricated using aluminum since many commercial packaging processes use aluminum wire, which can react with gold wires at high temperatures. Aluminum is also cheaper then gold, but can corrode when subjected to certain environmental conditions. Gold is the topcoat material of choice for these devices due to its oxidation resistance, low electrical resistance, high temperature stability and good wire bond adhesion.

2.2.13. Backside Metalization

The final metallization step is the backside coating. Several different materials can be used depending on the preferred die attach. For many commercial power devices silver is used for the backside metallization. Silver is cheaper than gold, and has better adhesion, wider process window, and improved reliability when used with lead based solders. Many low power devices are bonded using conductive epoxies, which allows for the use of low cost aluminum for the backside contact. For these devices gold is the preferred topcoat material, since the devices are bonded into the package using an 80% gold 20% tin eutectic. Gold does not adhere well to most materials, especially the nickel used on the backside, so the same three layer metal stack used in the overcoat processes is used again. The use of the 80:20 gold/tin

eutectic solder for the die attach reduces the final gold layer to be thinned to 1 μm thus reducing cost.

2.2.14. Final Passivation

For commercial devices a final passivation step is used to further protect the top of the device. This step consists of either a CVD oxidation coating or a polyimide coating. The polyimide process begins with the application of the polyimide through a three-step process starting with spin-on of the polyimide. The polyimide is then patterned and developed leaving open contacts. While the polyimide process is simple, the oxide process is better understood and does not suffer from swelling and moisture absorption so it was used for these devices. The oxide is deposited using the LPCVD and then photoresist is applied and patterned. The oxide is then removed from the base/gate and anode/emitter contract regions using the SF_6 plasma etcher.

2.2.15. Basic Packaging

Once completed, the devices are cut up and bonded into various types of packages depending on their applications. These devices were bonded to the substrates using either the 80/20 gold/tin, which has a melting point of 280 °C, or a polyimide based silver filled die attach [51,52]. The silver filled die attach can operate at temperatures as high as 500 °C and can bond materials other then gold. It does not provide high thermal conductivity so many devices are bonded using the gold/tin eutectic. The top contacts are wire bonded to the package using either aluminum or gold wire. Wire sizes vary but most power devices are bonded using a 10 mil wire to handle high currents. For lower power devices, and devices with odd shaped pads, a 1 or 3 mil wire is used.

Chapter 3: Modeling

3.1. Background

The development of state of the art semiconductor devices relies heavily on modeling the electrical and physical parameters of the device. There are several different types and levels of models used to model semiconductor devices. The most basic are the direct calculation of the parameters using the quasi Fermi, and intrinsic carrier concentration equations. The accuracy of these models is very poor due to the complexity of the devices and the number of assumptions required for calculation of the closed forms. Improved accuracy can be achieved through iteratively solving these equations. This method uses the most recent calculation to improve the accuracy of the following calculation. This requires reasonable computing power and a good first estimate. To further increase accuracy, the device can be broken into finite elements with the equation being solved for each element. This method allows for very accurate calculations if all of the parameters are known.

3.2. Model Complexity

Models are also based on the level of system complexity to be studied. At the lowest level are the Monte Carlo and similar models that will model the behavior of individual particles. These models track individual particles as they move through the material using random number generators to determine when and what types of collisions occur during particle collisions. The models will run the flight statistics including time between collisions and energy transfer in collisions for several thousand particles. This data can then be used in the higher-level carrier based models that use the drift-diffusion equations, or can be used with other methods such

as hydrodynamic modeling. The drift-diffusion and hydrodynamic modeling methods use equations that are based on averages, particularly the Fermi equations, to determine carrier and current flow through the doped regions of the device. These equations are best for calculating how individual devices will behave under different biasing conditions. The next level up is the circuit level model that uses equations such as the Ebers-Moll equations [53] or resistor models.

$$I_E = \alpha_1 I_C + I_{E0} e^{\left(\frac{q V_{EB}}{kt} - 1\right)}$$

Equation 4 Ebers-Moll equation for emitter current

$$I_C = \alpha_N I_E - I_{C0} e^{\left(\frac{q V_{CB}}{kt} - 1\right)}$$

Equation 5 Ebers-Moll equation for collector current

Using these equations the model can calculate circuit input and output values. Sophisticated models will combine multiple techniques, usually to achieve very high accuracy calculations at the cost of long calculation times. SiC uses the same techniques that are used in modeling silicon, but require additional calculations to handle issues related to its wide bandgap such as carrier ionization.

3.3. 1-D Model Description

The model developed here is a 1 dimensional model designed to provide carrier concentrations and potential values for a PN diode. Constants for both Si and SiC are provided and the model can solve for either type of material. This model utilizes the Poisson and drift-diffusion equations to find the potential and carrier concentrations. This technique utilizes 5 basic equations to describe the potential across the device and carrier flow into and out of the device.

3.4. Constants

Semiconductor models require many constants that are used throughout the calculations. The constant values used in this model are given in Table 1.

Variable		Value	Units
Boltzman's Constant	k=	8.62E-05	eV/K
Electron Charge	q=	1.61E-19	C
Permittivity of Free Space	ε0=	8.85E–14	F/cm
Electron Mass	m0=	9.11E-31	kg
Planck's Constant	h=	4.14E-15	eV s
	εSiC=	10.2	

Table 1 Constant Values

The thermal voltage (Vt) used in many of the equations is given by $Vt_i = \frac{k\,T}{q}$. Many other values used in this model are temperature dependant including the mobility (μ), the intrinsic carrier concentration (ni), bandgap (Eg), carrier lifetime (τ), and recombination and generation (RG). These values are discussed at the end of this section.

3.5. Poisson Equation

The Poisson equation relates the electric field gradient, or laplacian of the potential, to the space charge present in the semiconductor. The Poisson equation (Equation 6) [54] takes into account the electron, hole and ionized impurity concentrations present in the semiconductor.

$$\frac{d}{dx}\mathrm{E}(x) = \frac{q\,(p - n + N_d^{+} - N_a^{-})}{\varepsilon}$$

Equation 6 Poisson equation

3.6. Drift-diffusion Calculation

The drift-diffusion equations consist of two equations, one for electron based transport and one for hole based transport (Equation 7) [55].

$$J_n(x) = q\,\mu_n\,n_x\,\mathrm{E}(x) + q\,\mathrm{D}_n\left(\frac{d}{dx}\mathrm{n}(x)\right)$$

$$J_p(x) = q\,\mu_p\,p_x\,\mathrm{E}(x) - q\,\mathrm{D}_p\left(\frac{d}{dx}\mathrm{p}(x)\right)$$

drift diffusion

Equation 7 Drift-diffusion equations

These equations solve for the three primary methods of charge transport through the device. The drift current portion calculates the interaction between the electrons or holes, and the electric field generated by an externally applied potential. The diffusion current calculates the current that arises from variations in carrier concentration within the device. These equations also account for diffusion caused by carrier concentration gradients in the semiconductor at a constant temperature.

3.7. Carrier Balance Calculation

The final two equations needed to solve for the carriers and potential are the carrier balance equations (Equation 8).

$$\frac{\partial}{\partial t}n = \frac{\frac{\partial}{\partial x}Jn}{q} - R$$

$$\frac{\partial}{\partial t}p = -\frac{\frac{\partial}{\partial x}Jp}{q} - R$$

Equation 8 Carrier balance equations

These equations balance the carrier concentration caused by current flow into and out of the device with internal generation and recombination of carriers. As with the drift

and diffusion calculations two equations are required to balance out for both electrons and holes. These equations are solved self consistently to find the carrier concentrations n and p and the potential phi. The recombination, and generation value R used in Equation 8, is calculated using Equation 9.

$$R = \frac{p\,n - n_i^2}{(n + p + 2\,n_i)\,\tau}$$

Equation 9 Generation/Recombination equation

The model developed here uses only Schottky Read Hall recombination, which is adequate for the level of accuracy required, but other forms would increase accuracy especially when dealing with SiC materials [56].

3.8. Carrier Concentration

Solving for carrier concentration can be difficult due to the difference in magnitudes between the carrier concentration and the electric field. The doped carrier concentrations are in the range of 1.0 x 10^{15}/cm^3 to 1.0 x 10^{20}/cm^3 while the potential needs to be accurate to 3 or 4 decimal places and is usually held to -10 and 10 volts for most calculations. Actual concentrations of carrier in silicon differ by about 10 orders of magnitude while silicon carbide varies by as much as 52 orders of magnitude, causing both accuracy and rounding problems. To get around problems with rounding and accuracy several different calculation methods have been developed. The first is to calculate carrier values directly, here after referred to as the standard method, which can cause accuracy and rounding problems. To reduce the issues with rounding and accuracy when using the standard method, the carrier concentrations can be normalized by the maximum doping value. Another method

uses quasi Fermi potentials found using Equation 10 and Equation 11 to reduce the difference in magnitude.

$$n = n_i \, e^{\left(\frac{q(\phi - \phi_n)}{k T}\right)}$$

Equation 10 n Type Fermi equation

$$p = n_i \, e^{\left(\frac{q(\phi_p - \phi)}{k T}\right)}$$

Equation 11 p Type Fermi equation

These equations are solved for a potential value resulting in Equation 12 and Equation 13.

$$\phi_n = \phi - \frac{\ln\left(\frac{n}{n_i}\right) k T}{q}$$

Equation 12 n Type Fermi potential

$$\phi_p = \phi + \frac{\ln\left(\frac{p}{n_i}\right) k T}{q}$$

Equation 13 p Type Fermi potential

These variables have the same order of magnitude as the device potential but require more complex non-linear solvers due to the exponential function. The final method utilizes a linearization of the carrier calculations that allows the use of linear solvers. This approach makes use of the Slotbloom variables using potential (φ), and linear carrier concentrations (u) and (v). The values for u and v are found using Equation 14 and Equation 15.

$$n = n \, e^{\left(\frac{q\phi}{k T}\right)} e^{\left(-\frac{q\phi}{k T}\right)}$$

Equation 14 n Type Fermi equation for Slotbloom calculation

$$p = p\, e^{\left(-\frac{q\,\phi}{k\,T}\right)}\, e^{\left(\frac{q\,\phi}{k\,T}\right)}$$

Equation 15 p Type Fermi equation for Slotbloom calculation

These equations can now be rearranged to find the final carrier concentration values given by Equation 16 and Equation 17

$$n = n_i\, e^{\left(\frac{q\,\phi}{k\,T}\right)}\, u$$

Equation 16 n Type Slotbloom calculation

$$p = n_i\, e^{\left(-\frac{q\,\phi}{k\,T}\right)}\, v$$

Equation 17 p Type Slotbloom Calculation

where u and v are found from Equation 18 and Equation 19.

$$u = \frac{n\, e^{\left(-\frac{q\,\phi}{k\,T}\right)}}{n_i}$$

Equation 18 n Type Slotbloom variable

$$v = \frac{p\, e^{\left(\frac{q\,\phi}{k\,T}\right)}}{n_i}$$

Equation 19 p Type Slotbloom variable

Since Equation 16 and Equation 17 are linear with respect to u and v a linear solver can be used. The disadvantage to using this technique is rounding problems that occur when calculating applied biases above 10 volts. The Slotbloom method was not used in these modes. This work compared the results using the standard values to the results given by the quasi Fermi method.

3.9. Newton-Raphson Solver

3.9.1. Background

The basic solution method used in this model is based on the Newton-Raphson [57,58] method. In this method, N equations denoted by F_i can be used to find an equal number of unknowns. The basic Newton technique involves expanding an equation using a Taylor series approximation around the point x_j (Equation 20).

$$F_i(\bar{x}_j + \delta\bar{x}_j) = F_i(\bar{x}_j) + \left(\sum_{j=0}^{N}\left(\frac{\partial}{\partial x_j}F_i\right)\delta\bar{x}_j\right) + O(\delta\bar{x}_j^{\,2})$$

Equation 20 2nd order Taylor equation

The partial differentials in this equation are the Jacobian matrix of the equation F_i. To simplify the calculations the higher order terms $O(\delta x_j^2)$ can be neglected. Each of the N equations is solved for δx_j by setting $F_i\ (x_j + \delta x_j)$ to zero and rearranging the equation to $J_i * \delta x_j = -F_i$. The solution for δx_j is found to be $\delta x_j = -F_i/J_i$. The value of δx_j is then added to x_j to obtain a new value for x_j, $x_{j\ new} = x_j + \delta x_j$, which is used in the next solution iteration. The solver continues until the solution achieves a predetermined level of accuracy. While this method is one of the better general solvers for nonlinear equations it does require care to achieve accurate results.

3.9.2. Convergence methods

Convergence to a solution using the Newton method can be a challenge. To achieve quick and accurate convergence requires the initial values used to be close to the solution and the determination of reasonable damping values to control the convergence of the Newton method. Determining a good initial guess is problem

dependent and for these calculations requires a good starting value for ϕ. The second problem that can arise is the solution process being either over or under damped. In an over damped situation the solution is slow in converging to the required answer. In an under damped situation the iterative process converges too quickly and overshoots the answer. In this case the solver cannot obtain the answer without backtracking, which is not possible with the standard Newton method. This causes the algorithm to fail since it can't backtrack to find the correct solution. Several methods are available to prevent both under damped and over damped situations. The most basic method is to limit the magnitude of each step through a limiting weight value applied to the equations. This requires knowledge of the solution and can greatly increase the process time or prevent convergence. Methods are available that allow monitoring the solver to prevent an over damped situation [59] or allow the system to backtrack to the correct value in under damped situations. The method used here utilizes a weighted method that is discussed later in this section.

3.9.3. Discritization Method

The drift-diffusion method can be used to directly solve for values through a complete device but only in specific device cases. More general situations require solutions across small portions of the device. There are several techniques available for solving single and multi dimensional problems including finite difference, finite element and others. The finite element and finite difference techniques utilize an n dimensional grid of points to describe the device. A 1 dimensional, finite difference method was chosen due to its simplicity. This technique solves the equations at each nodal point based on information from the nearest neighbors. This requires each

equation to be discritized to fit on the mesh. The accuracy of this method relies on careful determination of the node-to-node spacing. Maximizing the node-to-node distance increases the speed of the model. Large nodal spacing reduces the number of calculations required but decreases the spatial accuracy of the results. Where spatial accuracy is important, reduced mesh spacing provides improved accuracy while increasing the solution time. In this model, the grid spacing is determined by calculating the minimum Debye length, Equation 21 and Equation 22, for each side of the junction.

$$X_{Debye_D} = \sqrt{\frac{E_{SiC}\, Vt}{Nd\, q}}$$

Equation 21 Debye length for donors

$$x_{Debye_A} = \sqrt{\frac{E_{SiC}\, Vt}{Na\, q}}$$

Equation 22 Debye length for acceptors

This step distance is applied to all steps that fall within the depletion width found by adding Equation 23 to Equation 24.

$$Xn = \sqrt{2}\sqrt{\frac{E_{SiC}\,(V_{jct} - Va)}{q\, Na\, Nd\,(Nd + Na)}}\, Na$$

Equation 23 Depletion width n side of pn junction

$$Xp = \sqrt{2}\sqrt{\frac{E_{SiC}\,(V_{jct} - Va)}{q\, Na\, Nd\,(Nd + Na)}}\, Nd$$

Equation 24 Depletion width p side of pn junction

where

$$V_{jct} = Vt \ln\left(\frac{Nd\, Na}{ni^2}\right)$$

Equation 25 Junction voltage

For regions outside the depletion region a step distance of 0.01 μm to 0.1 μm is used.

3.9.4. Taylor Expansion

The carrier concentration and potential equations are found at each mesh point through a Taylor's expansion of the functions around $x_{i-1/2}$ (Equation 26) and $x_{i+1/2}$ (Equation 27).

$$F_{i+1} = F_i + \left(\frac{d}{dx_i} \mathrm{F}(x_i)\right) Dx + \frac{\left(\frac{\partial^2}{\partial x^2} \mathrm{F}(x_i)\right) Dx^2}{2!} + \frac{\left(\frac{\partial^3}{\partial x^3} \mathrm{F}(x_i)\right) Dx^3}{3!} + \mathrm{O}(Dx^4)$$

Equation 26 Taylor expansion around (i+1)

$$F_{i-1} = F_i - \left(\frac{d}{dx_i} \mathrm{F}(x_i)\right) Dx + \frac{\left(\frac{\partial^2}{\partial x^2} \mathrm{F}(x_i)\right) Dx^2}{2!} - \frac{\left(\frac{\partial^3}{\partial x^3} \mathrm{F}(x_i)\right) Dx^3}{3!} + \mathrm{O}(Dx^4)$$

Equation 27 Taylor expansion around (i-1)

The spacing between the nodes is given by $x_i = a + i\,Dx$ where i is the step value. The difference of these two equations is found and solved for the second order value of F found in Equation 28.

$$F_{xx}(x_i) = \frac{F_{i+1} + F_{i-1} - 2F_i}{Dx^2}$$

Equation 28 2nd order finite difference

3.9.4.1. Taylor Expansion of the Poisson Equation

Using the Taylor method on the Poisson equation yields Equation 29.

$$F_{\phi_{k,i}} = \frac{-2\Phi_{k,i} + \Phi_{k,i+1} + \Phi_{k,i-1}}{Dx^2} + \frac{q\left(-n_{k,i} + p_{k,i} + Nd_i - Na_i\right)}{E_{SiC}}$$

Equation 29 Taylor expansion of the Poisson equation

Each equation is differentiated with respect to the 3 unknowns; ϕ, n and p to determine the Jacobian. A Jacobian calculation is performed for the 3 equations at node points i-1, i, and i+1, yielding 45 different equations. The Poisson equation is a straightforward calculation yielding Equation 30, Equation 31 and Equation 32.

$$\frac{\partial}{\partial \Phi_{i-1}} F_\phi = \frac{1}{Dx_i^{\,2}} \quad \text{eq a} \qquad \frac{\partial}{\partial \Phi_i} F_\phi = -\frac{2}{Dx_i^{\,2}} \quad \text{eq b} \qquad \frac{\partial}{\partial \Phi_{i+1}} F_\phi = \frac{1}{Dx_i^{\,2}} \quad \text{eq c}$$

Equation 30 Differentials of the Poisson equations with respect to φ

$$\frac{\partial}{\partial n_{i-1}} F_\phi = 0 \quad \text{eq a} \qquad \frac{\partial}{\partial n_i} F_\phi = -\frac{q}{E_{SiC}} \quad \text{eq b} \qquad \frac{\partial}{\partial n_{i+1}} F_\phi = 0 \quad \text{eq c}$$

Equation 31 Differentials of the Poisson equations with respect to n

$$\frac{\partial}{\partial p_{i-1}} F_\phi = 0 \quad \text{eq a} \qquad \frac{\partial}{\partial p_i} F_\phi = \frac{q}{E_{SiC}} \quad \text{eq b} \qquad \frac{\partial}{\partial n_{i+1}} F_\phi = 0 \quad \text{eq c}$$

Equation 32 Differentials of the Poisson equations with respect to p

3.9.4.2. Taylor Expansion of the Drift-diffusion calculation

The drift-diffusion calculations are more complex due to the hidden phi terms in n and p, and the use of both linear and exponential difference values. When the values a1 and a2 (Equation 33) and (Equation 34) are less then 1 x 10^{-3}, the linear Taylor approximation is used (Equation 37 and Equation 38).

$$a1 = \frac{\Phi_{k,\,i} - \Phi_{k,\,i-1}}{Vt_i}$$

Equation 33 Value of a1

$$a2 = \frac{\Phi_{k,\,i+1} - \Phi_{k,\,i}}{Vt_i}$$

Equation 34 Value of a2

$$f_{i-1_{Linear}} = \frac{2}{2 - \frac{\Phi_i - \Phi_{i-1}}{Vt_i}}$$

Equation 35 Linear function at location i-1

$$f_{i_{Linear}} = \frac{2}{2 + \frac{\Phi_{i+1} - \Phi_i}{Vt_i}}$$

Equation 36 Linear function at location i

Combining Equation 35 and Equation 36 with Equation 26 and Equation 27 yields the linear discritized drift-diffusion function (Equation 37 and Equation 38).

$$F_{n_{k,i}} = \frac{\mu_{n_i} Vt\left(\frac{2\,n_{k,i+1}}{2+a2} - n_{k,i}\left(\frac{2}{2-a2}+\frac{2}{2+a1}\right)+\frac{2\,n_{k,i-1}}{2-a1}\right)}{Dx^2} - RG\_F$$

Equation 37 Taylor expansion of the electron drift-diffusion equation for large values of a1 and a2

$$F_{p_{k,i}} = \frac{\mu_{p_i} Vt\left(\frac{2\,p_{k,i+1}}{2-a2} - p_{k,i}\left(\frac{2}{2+a2}+\frac{2}{2-a1}\right)+\frac{2\,p_{k,i-1}}{2+a1}\right)}{Dx^2} - RG\_F$$

Equation 38 Taylor expansion of the hole drift-diffusion equation for large values of a1 and a2

Equation 37 and Equation 38 provide high accuracy at the cost of slower convergence rate.

3.9.5. Scharfetter Gummel Approach

When the values of a1 and a2 are greater then 1 x 10^{-3}, an exponential approximation method developed by Scharfetter and Gummel [60] utilizing the Bernoulli equations (Equation 41 and Equation 42) provides faster convergence.

$$f_{i-1_{Bernoulli}} = \frac{\Phi_i - \Phi_{i-1}}{Vt_i\left(e^{\left(\frac{\Phi_i - \Phi_{i-1}}{Vt_i}\right)} - 1\right)}$$

Equation 39 Bernoulli function at location i-1

$$f_{i_{Bernoulli}} = \frac{\Phi_{i+1} - \Phi_i}{Vt_i\left(e^{\left(\frac{\Phi_{i+1} - \Phi_i}{Vt_i}\right)} - 1\right)}$$

Equation 40 Bernoulli function at location i

$$F_{n_{k,i}} = \frac{\mu_{n_i} Vt\left(\frac{a2\,n_{k,i+1}}{e^{a2}-1} - n_{k,i}\left(-\frac{a2}{e^{(-a2)}-1}+\frac{a1}{e^{a1}-1}\right)-\frac{a1\,n_{k,i-1}}{e^{(-a1)}-1}\right)}{Dx^2} - RG\_F$$

Equation 41 Taylor expansion of the electron drift-diffusion equation for small values of a1 and a2

$$F_{p_{k,i}} = \frac{\mu_{p_i} Vt \left(-\frac{a2\, p_{k,i+1}}{e^{(-a2)} - 1} - p_{k,i} \left(\frac{a2}{e^{a2} - 1} - \frac{a1}{e^{(-a1)} - 1} \right) + \frac{a1\, p_{k,i-1}}{e^{a1} - 1} \right)}{Dx^2} - RG\_F$$

Equation 42 Taylor expansion of the hole drift-diffusion equation for small values of a1 and a2

The generation/recombination rate RG_F is given by Equation 43.

$$RG\_F = \frac{p_{k,i}\, n_{k,i} - ni^2}{(n_{k,i} + p_{k,i} + 2\, ni)\, \tau}$$

Equation 43 Generation/Recombination rate

The linear Jacobian is found for Equation 37 and Equation 38 with respect to ϕ, n and p, and the results are given in Equation 44 through Equation 57.

$$\frac{\partial}{\partial \Phi_{i-1}} F_n = \frac{\mu_{n_i} Vt_i \left(-\frac{2\, n_{k,i}}{(2 + a1)^2\, Vt} - \frac{2\, n_{k,i-1}}{(2 - a1)^2\, Vt_i} \right)}{Dx_i^{\,2}}$$

Equation 44 dFn/dØ node n-1 linear difference calculation

$$\frac{\partial}{\partial \Phi_i} F_n = \frac{\mu_{n_i} Vt_i \left(\frac{2\, n_{k,i+1}}{(2 + a2)^2\, Vt} - n_{k,i} \left(-\frac{2}{(2 - a2)^2\, Vt} - \frac{2}{(2 + a1)^2\, Vt_i} \right) + \frac{2\, n_{k,i-1}}{(2 - a1)^2\, Vt_i} \right)}{Dx_i^{\,2}}$$

Equation 45 dFn/dØ node n linear difference calculation

$$\frac{\partial}{\partial \Phi_{i+1}} F_n = \frac{\mu_{n_i} Vt_i \left(-\frac{2\, n_{k,i+1}}{(2 + a2)^2\, Vt} - \frac{2\, n_{k,i}}{(2 - a2)^2\, Vt_i} \right)}{Dx_i^{\,2}}$$

Equation 46 dFn/dØ node n+1 linear difference calculation

$$\frac{\partial}{\partial n_{i-1}} F_n = \frac{2\, \mu_{n_i} Vt_i}{Dx_i^{\,2} (2 - a1)}$$

Equation 47 dFn/dn node n-1 linear difference calculation

$$\frac{\partial}{\partial n_i} F_n = \frac{\mu_{n_i} Vt_i \left(-\frac{2}{2 - a2} - \frac{2}{2 + a1} \right)}{Dx_i^{\,2}} - RG\_dN$$

Equation 48 dFn/dn node n linear difference calculation

Where $RG\_dN = \frac{p_{k,i}^{\,2} + 2\,p_{k,i}\,ni + ni^2}{(n_{k,i} + p_{k,i} + 2\,ni)^2\,\tau}$

$$\frac{\partial}{\partial n_{i+1}} F_n = \frac{2\,\mu_{n_i}\,Vt_i}{Dx_i^{\,2}\,(2 + a2)}$$

Equation 49 dFn/dn node n+1 linear difference calculation

$$\frac{\partial}{\partial p_{i-1}} F_n = 0 \quad \text{eq a} \qquad \frac{\partial}{\partial p_i} F_n = -RG\_dP \quad \text{eq b} \qquad \frac{\partial}{\partial p_{i+1}} F_n = 0 \quad \text{eq c}$$

Equation 50 dFn/dp nodes n-1, n and n+1 linear difference calculation

where

$$RG\_dP = \frac{n0^2 + n_{k,i}^{\,2} + 2\,n_{k,i}\,ni}{(n_{k,i} + p_{k,i} + 2\,ni)^2\,\tau}$$

$$\frac{\partial}{\partial \Phi_{i-1}} F_p = \frac{\mu_{p_i}\,Vt_i \left(\frac{2\,p_{k,i}}{(2 - a1)^2\,Vt_i} + \frac{2\,p_{k,i-1}}{(2 + a1)^2\,Vt_i} \right)}{Dx_i^{\,2}}$$

Equation 51 dFp/dØ node n-1 linear difference calculation

$$\frac{\partial}{\partial \Phi_i} F_p = \frac{\mu_{p_i}\,Vt_i \left(-\frac{2\,p_{k,i+1}}{(2 - a2)^2\,Vt} - p_{k,i} \left(\frac{2}{(2 + a2)^2\,Vt_i} + \frac{2}{(2 - a1)^2\,Vt_i} \right) - \frac{2\,p_{k,i-1}}{(2 + a1)^2\,Vt_i} \right)}{Dx_i^{\,2}}$$

Equation 52 dFp/dØ node n linear difference calculation

$$\frac{\partial}{\partial \Phi_{i+1}} F_p = \frac{\mu_{p_i}\,Vt_i \left(\frac{2\,p_{k,i+1}}{(2 - a2)^2\,Vt_i} + \frac{2\,p_{k,i}}{(2 + a2)^2\,Vt_i} \right)}{Dx_i^{\,2}}$$

Equation 53 dFp/dØ node n+1 linear difference calculation

$$\frac{\partial}{\partial n_{i-1}} F_p = 0 \quad \text{eq a} \qquad \frac{\partial}{\partial n_i} F_p = -RG\_dN \quad \text{eq b} \qquad \frac{\partial}{\partial n_{i+1}} F_p = 0 \quad \text{eq c}$$

Equation 54 dFp/dn nodes n-1, n and n+1 linear difference calculation

$$\frac{\partial}{\partial p_{i-1}} F_p = \frac{2\,\mu_{p_i}\,Vt_i}{Dx_i^{\,2}\,(2+a1)}$$

Equation 55 dFp/dp node n-1 linear difference calculation

$$\frac{\partial}{\partial p_i} F_p = \frac{\mu_{p_i}\,Vt_i\left(-\frac{2}{2+a2}-\frac{2}{2-a1}\right)}{Dx_i^{\,2}} - RG\_dP$$

Equation 56 dFp/dp node n linear difference calculation

$$\frac{\partial}{\partial p_{i+1}} F_p = \frac{2\,\mu_{p_i}\,Vt_i}{Dx_i^{\,2}\,(2-a2)}$$

Equation 57 dFp/dp node n+1 linear difference calculation

The Jacobian equations for small difference values found using the exponential are given in Equation 58 through Equation 69. The value for dFn/dp and dFp/dn are the same for both the exponential and linear difference calculations.

$$\frac{\partial}{\partial \Phi_{i-1}} F_n = \frac{\mu_{n_i}\,Vt_i\left(-n_{k,i}\left(-\frac{1}{Vt_i\,(e^{a1}-1)}+\frac{a1\,e^{a1}}{Vt_i\,(e^{a1}-1)^2}\right)+\frac{n_{k,i-1}}{Vt_i\,(e^{(-a1)}-1)}+\frac{a1\,n_{k,i-1}\,e^{(-a1)}}{Vt_i\,(e^{(-a1)}-1)^2}\right)}{Dx_i^{\,2}}$$

Equation 58 dFn/dØ node n-1 Bernoulli difference calculation

$$\frac{\partial}{\partial \Phi_i} F_n = \mu_{n_i}\,Vt_i\left(-\frac{n_{k,i+1}}{Vt_i\,(e^{a2}-1)}+\frac{a2\,n_{k,i+1}\,e^{a2}}{Vt_i\,(e^{a2}-1)^2}\right.$$
$$-n_{k,i}\left(\frac{1}{Vt_i\,(e^{(-a2)}-1)}+\frac{a2\,e^{(-a2)}}{Vt_i\,(e^{(-a2)}-1)^2}+\frac{1}{Vt_i\,(e^{a1}-1)}-\frac{a1\,e^{a1}}{Vt_i\,(e^{a1}-1)^2}\right)$$
$$\left.-\frac{n_{k,i-1}}{Vt_i\,(e^{(-a1)}-1)}-\frac{a1\,n_{k,i-1}\,e^{(-a1)}}{Vt_i\,(e^{(-a1)}-1)^2}\right) \Big/ Dx_i^{\,2}$$

Equation 59 dFn/dØ node n Bernoulli difference calculation

$$\frac{\partial}{\partial \Phi_{i+1}} F_n = \frac{\mu_{n_i} Vt_i \left(\frac{n_{k,i+1}}{Vt_i \left(e^{a2} - 1 \right)} - \frac{a2\, n_{k,i+1}\, e^{a2}}{Vt_i \left(e^{a2} - 1 \right)^2} - n_{k,i} \left(- \frac{1}{Vt_i \left(e^{(-a2)} - 1 \right)} - \frac{a2\, e^{(-a2)}}{Vt_i \left(e^{(-a2)} - 1 \right)^2} \right) \right)}{Dx_i^{\,2}}$$

Equation 60 dFn/dØ node n+1 Bernoulli difference calculation

$$\frac{\partial}{\partial n_{i-1}} F_n = - \frac{\mu_{n_i} Vt_i\, a1}{Dx_i^{\,2} \left(e^{(-a1)} - 1 \right)}$$

Equation 61 dFn/dn node n-1 Bernoulli difference calculation

$$\frac{\partial}{\partial n_i} F_n = \frac{\mu_{n_i} Vt_i \left(\frac{a2}{e^{(-a2)} - 1} - \frac{a1}{e^{a1} - 1} \right)}{Dx_i^{\,2}} - RG\_dN$$

Equation 62 dFn/dn node n Bernoulli difference calculation

$$\frac{\partial}{\partial n_{i+1}} F_n = \frac{\mu_{n_i} Vt_i\, a2}{Dx_i^{\,2} \left(e^{a2} - 1 \right)}$$

Equation 63 dFn/dn node n+1 Bernoulli difference calculation

$$\frac{\partial}{\partial \Phi_{i-1}} F_p = \frac{\mu_{p_i} Vt_i \left(-p_{k,i} \left(\frac{1}{Vt_i \left(e^{(-a1)} - 1 \right)} + \frac{a1\, e^{(-a1)}}{Vt_i \left(e^{(-a1)} - 1 \right)^2} \right) - \frac{p_{k,i-1}}{Vt_i \left(e^{a1} - 1 \right)} + \frac{a1\, p_{k,i-1}\, e^{a1}}{Vt_i \left(e^{a1} - 1 \right)^2} \right)}{Dx_i^{\,2}}$$

Equation 64 dFp/dØ node n-1 Bernoulli difference calculation

$$\frac{\partial}{\partial \Phi_i} F_p = \mu_{p_i} Vt_i \left(\frac{p_{k,i+1}}{Vt_i \left(e^{(-a2)} - 1 \right)} + \frac{a2\, p_{k,i+1}\, e^{(-a2)}}{Vt_i \left(e^{(-a2)} - 1 \right)^2} - p_{k,i} \left(- \frac{1}{Vt_i \left(e^{a2} - 1 \right)} + \frac{a2\, e^{a2}}{Vt_i \left(e^{a2} - 1 \right)^2} - \frac{1}{Vt_i \left(e^{(-a1)} - 1 \right)} - \frac{a1\, e^{(-a1)}}{Vt_i \left(e^{(-a1)} - 1 \right)^2} \right) + \frac{p_{k,i-1}}{Vt_i \left(e^{a1} - 1 \right)} - \frac{a1\, p_{k,i-1}\, e^{a1}}{Vt_i \left(e^{a1} - 1 \right)^2} \right) \Big/ Dx_i^{\,2}$$

Equation 65 dFp/dØ node n Bernoulli difference calculation

$$\frac{\partial}{\partial \Phi_{i+1}} F_p = \frac{\mu_{p_i} Vt_i \left(-\frac{p_{k,i+1}}{Vt_i \left(e^{(-a2)} - 1 \right)} - \frac{a2\, p_{k,i+1}\, e^{(-a2)}}{Vt_i \left(e^{(-a2)} - 1 \right)^2} - p_{k,i} \left(\frac{1}{Vt_i \left(e^{a2} - 1 \right)} - \frac{a2\, e^{a2}}{Vt_i \left(e^{a2} - 1 \right)^2} \right) \right)}{Dx_i^2}$$

Equation 66 dFp/dØ node n+1 Bernoulli difference calculation

$$\frac{\partial}{\partial p_{i-1}} F_p = \frac{\mu_{p_i} Vt_i\, a1}{Dx_i^2 \left(e^{a1} - 1 \right)}$$

Equation 67 dFp/dp node n-1 Bernoulli difference calculation

$$\frac{\partial}{\partial p_i} F_p = \frac{\mu_{p_i} Vt_i \left(-\frac{a2}{e^{a2} - 1} + \frac{a1}{e^{(-a1)} - 1} \right)}{Dx_i^2} - RG\_dP$$

Equation 68 dFp/dp node n Bernoulli difference calculation

$$\frac{\partial}{\partial p_{i+1}} F_p = -\frac{\mu_{p_i} Vt_i\, a2}{Dx_i^2 \left(e^{(-a2)} - 1 \right)}$$

Equation 69 dFp/dp node n+1 Bernoulli difference calculation

The solutions for the quasi Fermi values were found using the same techniques. In this case the values for n and p were replaced with values found by Equation 12 and Equation 13. The differentials in the Jacobian calculations are then based on the derivatives of $Ø_n$ and $Ø_p$.

3.9.6. Block Successive Over Relaxation (SOR) Method

Once the values of these equations are known, the equations are solved using the Newton method described previously. A Newton matrix (Equation 70) of these equations is generated to solve the nine nodal values.

$$\left(\begin{bmatrix} \frac{\partial}{\partial \phi} F_{\phi} & \frac{\partial}{\partial n} F_{\phi} & \frac{\partial}{\partial p} F_{\phi} \\ \frac{\partial}{\partial \phi} F_{n} & \frac{\partial}{\partial n} F_{n} & \frac{\partial}{\partial p} F_{n} \\ \frac{\partial}{\partial \phi} F_{p} & \frac{\partial}{\partial n} F_{p} & \frac{\partial}{\partial p} F_{p} \end{bmatrix}^{k}\right) \cdot \begin{bmatrix} \delta \phi \\ \delta n \\ \delta p \end{bmatrix} = \begin{bmatrix} -F_{\phi_{\phi^k, n^k, p^k}} \\ -F_{n_{\phi^k, n^k, p^k}} \\ -F_{p_{\phi^k, n^k, p^k}} \end{bmatrix}$$

Equation 70 Newton equation to solve for φ, n and p

In actual operation this method does not always converge. Other techniques that couple the equations are used to improve the convergence. This model uses a block successive over relaxation (SOR) method to improve convergence [61]. This method is based on the assumption that all main diagonal blocks in Equation 70 are non-singular and that the equations are a definite Jacobian matrix. Based on these two assumptions the matrix is split diagonally so that the solution for the k-th iteration is found through Equation 71

$$\left(\begin{bmatrix} \frac{\partial}{\partial \phi} F_{\phi} & 0 & 0 \\ \frac{\partial}{\partial \phi} F_{n} & \frac{\partial}{\partial n} F_{n} & 0 \\ \frac{\partial}{\partial \phi} F_{p} & \frac{\partial}{\partial n} F_{p} & \frac{\partial}{\partial p} F_{p} \end{bmatrix}^{k}\right) \cdot \left(\begin{bmatrix} \delta \phi^{k} \\ \delta n^{k} \\ \delta p^{k} \end{bmatrix}^{(m+1)}\right) = -\begin{bmatrix} F_{\phi_{\phi^k, n^k, p^k}} \\ F_{n_{\phi^k, n^k, p^k}} \\ F_{p_{\phi^k, n^k, p^k}} \end{bmatrix} - \left(\left(\begin{bmatrix} 0 & \frac{\partial}{\partial n} F_{\phi} & \frac{\partial}{\partial p} F_{\phi} \\ 0 & 0 & \frac{\partial}{\partial p} F_{n} \\ 0 & 0 & 0 \end{bmatrix}^{k}\right) \cdot \left(\begin{bmatrix} \delta \phi^{k} \\ \delta n^{k} \\ \delta p^{k} \end{bmatrix}^{m}\right)\right)$$

Equation 71 Block SOR solution method

This equation can now be broken down so that there are three systems of equations Equation 72, Equation 73, and Equation 74 that are solved sequentially.

$$\left(\frac{\partial}{\partial \phi} F_{\phi}^{\,k}\right) \delta \phi^{(km+1)} = -F_{\phi_{\phi^k, n^k, p^k}} - \left(\frac{\partial}{\partial n} F_{\phi}^{\,k}\right) \delta n^{km} - \left(\frac{\partial}{\partial p} F_{\phi}^{\,k}\right) \delta p^{km}$$

Equation 72 Block SOR solution for ϕ

$$\left(\frac{\partial}{\partial n} F_{n}^{\,k}\right) \delta n^{(km+1)} = -F_{n_{\phi^k, n^k, p^k}} - \left(\frac{\partial}{\partial \phi} F_{n}^{\,k}\right) \delta \phi^{(km+1)} - \left(\frac{\partial}{\partial p} F_{n}^{\,k}\right) \delta p^{km}$$

Equation 73 Block SOR solution for n

$$\left(\frac{\partial}{\partial p} F_p^{\,k}\right) \delta p^{\mathrm{k}(m+1)} = -F_{p_{\phi^k, n^k, p^k}} - \left(\frac{\partial}{\partial \phi} F_p^{\,k}\right) \delta \phi^{(km+1)} - \left(\frac{\partial}{\partial n} F_p^{\,k}\right) \delta n^{(km+1)}$$

Equation 74 Block SOR solution for p

This method should converge linearly, but methods are needed to prevent under or over damped conditions from occurring [62].

3.9.7. Convergence Damping

To reduce the probability of an under or over damped condition and to reduce convergence time, the initial solution estimate is critical. The estimate needs to be close to the final answer for the Newton method to converge. A possible initial guess for carrier values at equilibrium is the value of the potential found using the Fermi equations (Equation 12 and Equation 13). It was found that this value did not provide an adequate initial guess. To further refine this value it is run through a simplified single equation Newton solver that yields the Newton method ϕ curve in Figure 15. The initial carrier values are then found at each step by solving the Fermi equations using the potential at each spatial point.

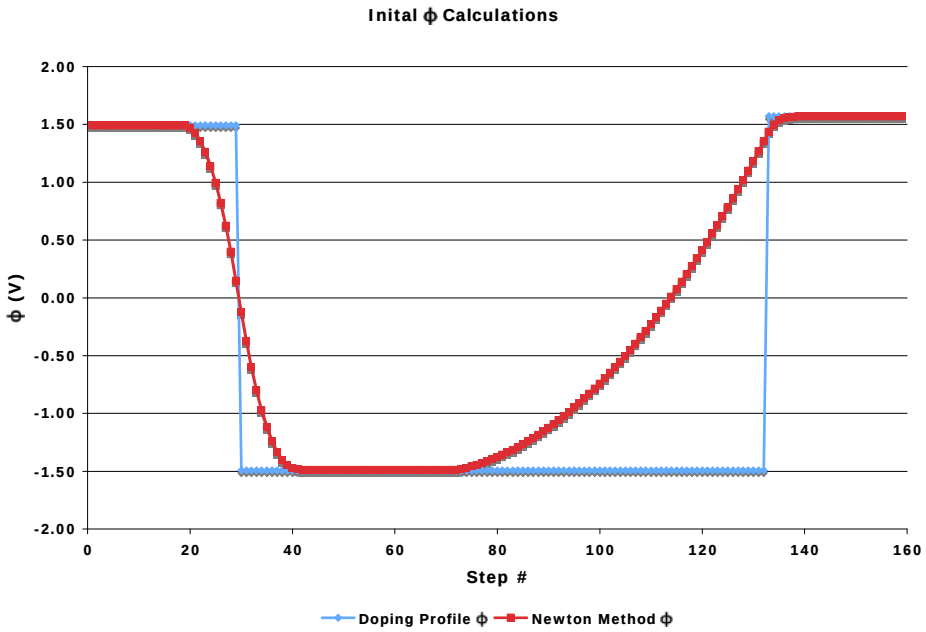


Figure 15 Initial potential calculations

To prevent problems with over or under damped situations in this model, a modified method of equation weighting is used. An initial weight value is used for the initial solution. If the calculation fails due to an under damped condition this weight value is increased. To prevent over damped situations, the iterative process is stopped after a preset number of loops and if the solution has not been found, a smaller weight value is calculated. This method works well, although it requires a large number of iterations to find a reasonable weight when the initial weight value is too large. Since the under damped mode is the most common methods of failure in this model the determination of a weight value is usually on the order of 1 to 2 minutes.

3.10. Temperature Dependant Values

3.10.1. Mobility

The solution of the Poisson and drift-diffusion equations can be performed with constant values for mobility, intrinsic carrier concentration and carrier lifetimes, but accuracy is improved when the calculation takes into account temperature affects. The mobility is affected by doping concentration, temperature, and high fields while carrier concentration is made up of several temperature dependant values. Mobility is reduced when increasing dopant concentrations increase local perturbations in the lattice. This effect is more dominant at low temperatures while at high temperature mobility is decreased due to lattice vibration affects becoming more dominate. To determine the values for the mobility at a given doping level and temperature, the Thomas Caughey equations are used [63]. These equations find the mobility based on both temperature and doping (Equation 75 through Equation 77).

$$\mu_{T,N} = \mu_0 \left(\frac{T}{300} \right)^{\gamma}$$

Equation 75 Dopant/Temperature dependant mobility

To find γ Equation 75 is used while μ_0 is found from Equation 77

$$\gamma = \beta_{min} + \frac{\beta_{max} - \beta_{min}}{1 + \left(\frac{N}{N_{beta\_ref}} \right)^{\alpha_0}}$$

Equation 76 Gamma value used to solve for mobility

$$\mu_0 = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + \left(\frac{N}{N_{ref}} \right)^{\alpha_\mu}}$$

Equation 77 Base mobility value for calculating mobility

The constants required for nitrogen and aluminum are given in Table 2.

Mobility Calculation Constants			
Constant	Nitrogen	Aluminum	
m_{min}	0.000	37.600	$cm^2/V\text{-}s$
m_{max}	977.000	106.000	$cm^2/V\text{-}s$
N_{ref}	1.17E+17	2.97E+18	$/cm^3$
a_m	0.490	0.356	
b_{min}	1.540	2.520	
b_{max}	2.620	3.040	
N_{beta_ref}	1.14E+17	8.67E+17	$/cm^3$
g	1.350	-0.456	

Table 2 Mobility constants

The mobility doping values differ from those used in the Poisson equation. Mobility requires the total doping value N_d+N_a, while the Poisson equation uses the difference between the majority and minority doping levels, N_d-N_a or N_a-N_d, in a region of the device. This model did not take into account field affects when calculating the mobility.

3.10.2. Intrinsic Carrier Concentration

The model uses the temperature dependant intrinsic carrier concentration (Equation 78) to more accurately determine carrier concentration at non standard temperature.

$$ni = \sqrt{Nc\ Nv}\ \mathbf{e}^{\left(-\frac{Eg}{2\,kT}\right)}$$

Equation 78 Intrinsic carrier concentration

The model also calculates the temperature dependent bandgap and effective density of states near the conduction band, Nc, and the valance band, Nv [64]. The bandgap, Eg, found using Equation 79, depends on experimentally determined constants to provide an accurate solution ($\alpha = \frac{0.00065\ \ eV}{K}$, $\beta = 1300\ \ K$ and $Eg0 = 3.2965625$ eV) [65].

$$Eg = Eg0 - \frac{\alpha\, T^2}{T + \beta}$$

Equation 79 Temperature dependent band gap

The effective density of states, Nc and Nv, are also temperature dependent and require the effective mass values for the electrons (Equation 80 and Equation 81).

$$Nc = 4\sqrt{2}\left(\frac{\pi\, me\, m0\, k\, T}{h^2}\right)^{(3/2)}$$

Equation 80 Conduction band effective density of states

$$Nv = 4\sqrt{2}\left(\frac{\pi\, mh\, m0\, k\, T}{h^2}\right)^{(3/2)}$$

Equation 81 Valence band effective density of states

where mh = 1, me = 0.6 and m0 = $9.11e^{-32}$ kg [66]

Plugging the values for Nc and Nv into Equation 78 yields the intrinsic carrier concentration. This value is then used to find the equilibrium carrier concentrations in a semiconductor using Equation 82.

$$p\, n = n_i^2$$

Equation 82 Equilibrium carrier concentration

3.10.3. Carrier Ionization

The assumption that carriers are fully ionized at room temperature, which is used when solving many problems in silicon, cannot be used when working with SiC. In silicon carbide most dopants have activation energies that are greater then k_B*T at room temperature causing less then 100 % ionization of the dopants. These non-ionized carrier values must be found to properly solve for the carrier concentrations and potential. First the donor/acceptor energies are found using the following equations.

$$\Delta E_d = E_c - E_d$$

$$\Delta E_a = E_a - E_v$$

Equation 83 Donor and acceptor energies

The ionization energy value E_d for nitrogen in 4H silicon carbide is 50 meV ±5 meV and the ionization energy value E_a for aluminum is 220 meV ±20 meV. When the device is in thermal equilibrium the Poisson Equation 6 is simplified to the results in Equation 84 and combined with Equation 82 to yield the equilibrium concentration for donors (Equation 85) and acceptors (Equation 86).

$$n + N_A^- = p + N_D^+$$

Equation 84 Equilibrium Poisson calculation

$$n = \frac{1}{2} N_{D-A} + \frac{1}{2}\sqrt{N_{D-A}^2 - 4\,ni^2} \qquad N_{D-A} = N_D^+ - N_A^-$$

where

Equation 85 Donor equilibrium concentration

$$p = \frac{1}{2} N_{D-A} + \frac{1}{2}\sqrt{N_{D-A}^2 - 4\,ni^2} \qquad N_{D-A} = N_D^+ - N_A^-$$

where

Equation 86 Acceptor equilibrium concentration

The concentration of ionized dopant atoms is found at steady state through a Gibbs distribution. For the donors and acceptors these values are found through the following equations

$$N_D^+ = \frac{N_D}{1 + \frac{g_D\, n}{n1}} \qquad n1 = N_c\, \mathbf{e}^{\left(-\frac{E_c - E_d}{kT}\right)}$$

where

Equation 87 Gibbs distribution for donors

and

$$N_A^- = \frac{N_A}{1 + \frac{g_D\, p}{p1}} \qquad p1 = N_v\, e^{\left(-\frac{E_a - E_v}{kT}\right)}$$

where

Equation 88 Gibbs distribution for acceptors

Combining Equation 83, Equation 85, and Equation 87 yields the non ionized carrier value (Equation 89) for the donors while the combination of Equation 83, Equation 86, and Equation 88 yields the value (Equation 90) for the acceptors.

$$\frac{N_D^+}{N_D} = -1 + \frac{1}{2}\,\frac{\sqrt{1 + \frac{4\, g_D\, N_D\, e^{\left(-\frac{E_c - E_d}{kT}\right)}}{N_c}\, N_c}}{g_D\, N_D\, e^{\left(-\frac{E_c - E_d}{kT}\right)}}$$

Equation 89 Non ionized carrier calculation for donors

.

$$\frac{N_A^-}{N_A} = -1 + \frac{1}{2}\,\frac{\sqrt{1 + \frac{4\, g_A\, N_A\, e^{\left(-\frac{E_a - E_v}{kT}\right)}}{N_v}\, N_v}}{g_A\, N_A\, e^{\left(-\frac{E_a - E_v}{kT}\right)}}$$

Equation 90 Non ionized carrier calculation for acceptors

The calculations for thermal dependence of carrier lifetime are straightforward and given by Equation 91 [67].

$$\tau_n = \tau_n\left(1 + \tau_a\left(\frac{T}{300} - 1\right)\right) \qquad \tau_a = 2.17$$

Equation 91 Temperature dependant carrier lifetime

This equation is used for both donors and acceptors.

3.11. Current Calculation

Once the potential and carrier concentration are found, the current can be calculated at each point. The two primary ways to solve for current are the drift-diffusion methods given in Equation 7, and the Scharfetter Gummel model discussed previously. The Scharfetter Gummel model provides more accurate potential values through the use of both Bernoulli and linear discretization methods (Equation 35, Equation 36, Equation 39, and Equation 40). These values are then applied to the discritized current yielding Equation 92 for Bernoulli based electron current and Equation 93 for linear calculations.

$$J_{n_i} = \frac{1}{2} \frac{q\,\mu_{n_i}\,Vt_i \left(\frac{\phi_{diff_i} n_{i+1}}{e^{\phi_{diff_i}} - 1} + \frac{\phi_{diff_i} n_i}{e^{\left(-\phi_{diff_i}\right)} - 1} + \frac{\phi_{diff_{i-1}} n_i}{e^{\phi_{diff_{i-1}}} - 1} + \frac{\phi_{diff_{i-1}} n_{i-1}}{e^{\left(-\phi_{diff_{i-1}}\right)} - 1} \right)}{\Delta_{x_i}}$$

Equation 92 Bernoulli based n current calculation

$$J_{n_i} = \frac{1}{2} \frac{q\,\mu_{n_i}\,Vt_i \left(\frac{2\,n_{i+1}}{2 + \phi_{diff_i}} - \frac{2\,n_i}{2 - \phi_{diff_i}} + \frac{2\,n_i}{2 + \phi_{diff_{i-1}}} - \frac{2\,n_{i-1}}{2 - \phi_{diff_{i-1}}} \right)}{\Delta_{x_i}}$$

Equation 93 Linear based n current calculation

The Bernoulli techniques yields Equation 94 for hole current while the linear method yields Equation 95.

$$J_{p_i} = -\frac{1}{2} \frac{q\,\mu_{p_i}\,Vt_i \left(\frac{\phi_{diff_i} p_{i+1}}{e^{\phi_{diff_i}} - 1} + \frac{\phi_{diff_i} p_i}{e^{\left(-\phi_{diff_i}\right)} - 1} + \frac{\phi_{diff_{i-1}} p_i}{e^{\phi_{diff_{i-1}}} - 1} + \frac{\phi_{diff_{i-1}} p_{i-1}}{e^{\left(-\phi_{diff_{i-1}}\right)} - 1} \right)}{\Delta_{x_i}}$$

Equation 94 Bernoulli based p current calculation

$$J_{p_i} = -\frac{1}{2}\frac{q\,\mu_{p_i}\,Vt_i\left(\frac{2\,p_{i+1}}{2+\phi_{diff_i}} - \frac{2\,p_i}{2-\phi_{diff_i}} + \frac{2\,p_i}{2+\phi_{diff_{i-1}}} - \frac{2\,p_{i-1}}{2-\phi_{diff_{i-1}}}\right)}{\Delta_{x_i}}$$

Equation 95 Linear based p current calculation

In these equations the values for $\emptyset_{diff}$ are found using $\phi_{diff_{i-1}} = \frac{\Phi_i - \Phi_{i-1}}{Vt_i}$ and $\phi_{diff_i} = \frac{\Phi_{i+1} - \Phi_i}{Vt_i}$ respectively. The currents are calculated at each voltage step to allow an IV curve to be generated for the structure. The model data is then scaled for comparison to the experimental data.

Chapter 4: Results and Analysis

4.1. Experimental Device

4.1.1. Device Design

Cree Research Inc provided the SiC bipolar junction transistors used for this work. The device chosen for analysis was based on a design that I provided them. This design is based on interdigitated structures that allow for either wire bonding or flip chip bump bonding of the device. This design provides large area emitter pads while smaller pads for the base connection are offset from the interdigitated base fingers.

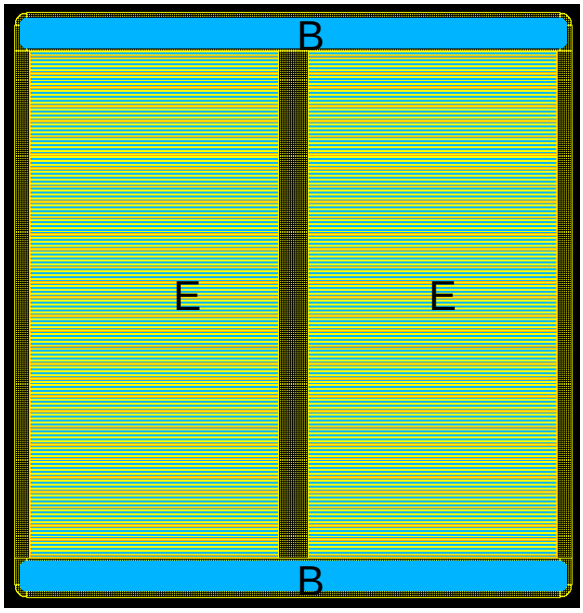


Figure 16 Device design

The interdigitiated design reduces current crowding and trace resistance in the emitter by providing large bonding pads directly over the emitter mesa.

4.1.2. Device Structure

The vertical structure consists of 5 layers of epitaxially grown SiC on a 4H SiC n-doped wafer. The wafer is approximately 400 μm thick and is doped to >1.0 x ^{19} /cm^3. Two different types of BJT's were studied for this work (Figure 17). The first is a lateral design that has very poor gain due to the number of implants required. The second is a vertical device structure that has much higher gain and provides better reverse blocking then the lateral device. This structure does have issues with low carrier lifetime at the base emitter junction, and at the implanted regions created for the base contacts. This work used the vertical structure devices which consisted of 4 epi layers. The initial layer is an n-doped buffer layer 0.5 μm thick used to achieve a smooth and consistent growth surface. Following the buffer layer the 18 μm thick collector region is deposited with a doping level of 2.5 x 10^{19} /cm^3. This region provides the reverse blocking in these devices and 18 μm can provide over 2000 V of blocking, which is reduced by the performance of the junction termination techniques. Following the collector region a p-doped base layer 1.5 μm thick and doped to 2.0 x 10^{17} /cm^3 is applied. The final two layers making up the emitter consist of an n-doped layer 1.5 μm thick doped to 8.0 x 10^{18} /cm^3 which provides emitter function and a 0.5 μm layer n-doped to >5.0 x 10^{19} /cm^3 to provide low contact resistance. The emitter and base contacts provide low contact resistance through the use of the highly doped epi layers. The base contacts require an implant to achieve a reasonable ohmic contact. To complete the connections and to provide decent bonding surfaces a Ti/Pt/Au stack is used on all bonded surfaces. To obtain high voltage blocking a guard ring junction termination is used around the mesa along

with a thermal/deposited oxide cap to passivate the surface. The devices were delivered to ARL for packaging using our standard process.

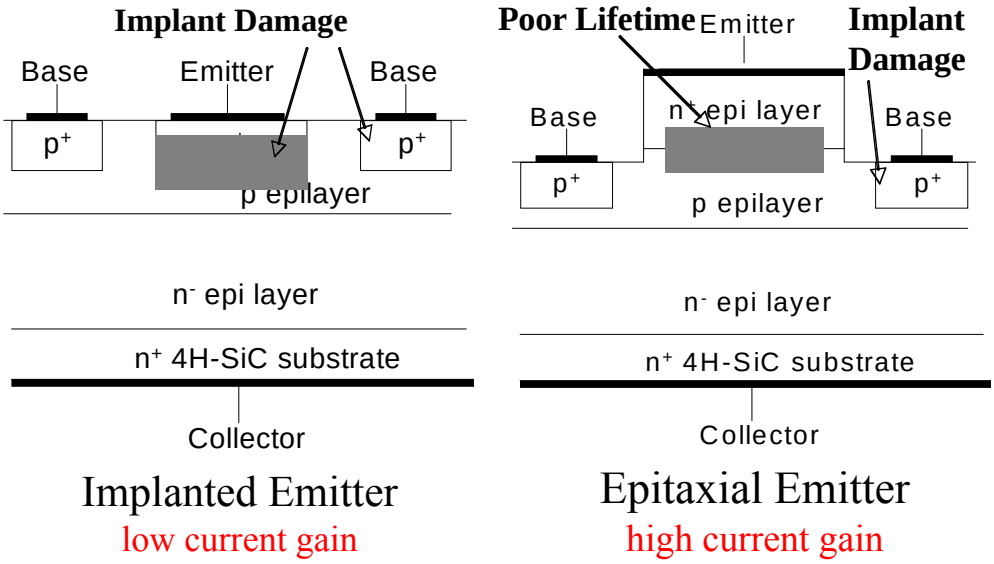


Figure 17 Lateral and Vertical BJT Structures

4.1.3. Device Packaging

The devices are mounted in a custom high voltage commercial package designed for ARL. This package consists of a base of copper 0.125 inches thick, electroplated with nickel/gold. An alumina ring is brazed to this base to provide isolation to the top connections. The two top connections fabricated from steel electroplated with nickel and gold, are brazed to this alumina ring (Figure 18).

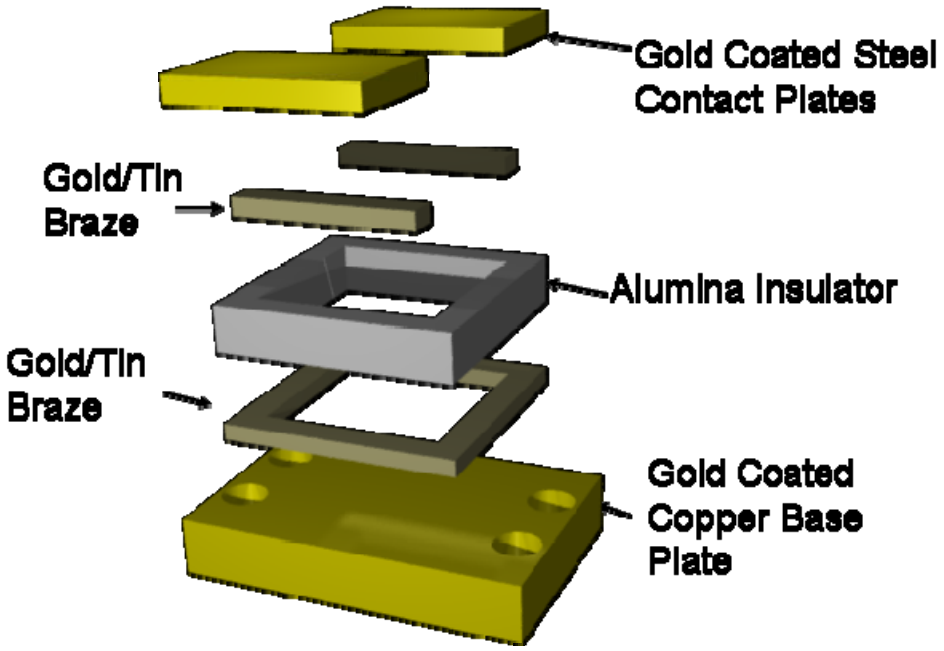


Figure 18 Exploded Package View

The devices were mounted to the base plate using an 80% gold – 20% tin paste 2 mils thick. The package is then heated in stages to 325 ºC to melt the solder and evaporate the flux. Once the remaining flux has been removed, 1 mil wire bonds are used to bond the emitter and base to the top package contacts. The emitter connection required several wire bonds to handle the current while the base connection required only 2 or 3 bonds due to the lower current requirements (Figure 19). Electrical testing was performed using a Tektronics 370B curve tracer while a digital hot plate was used to heat the devices.

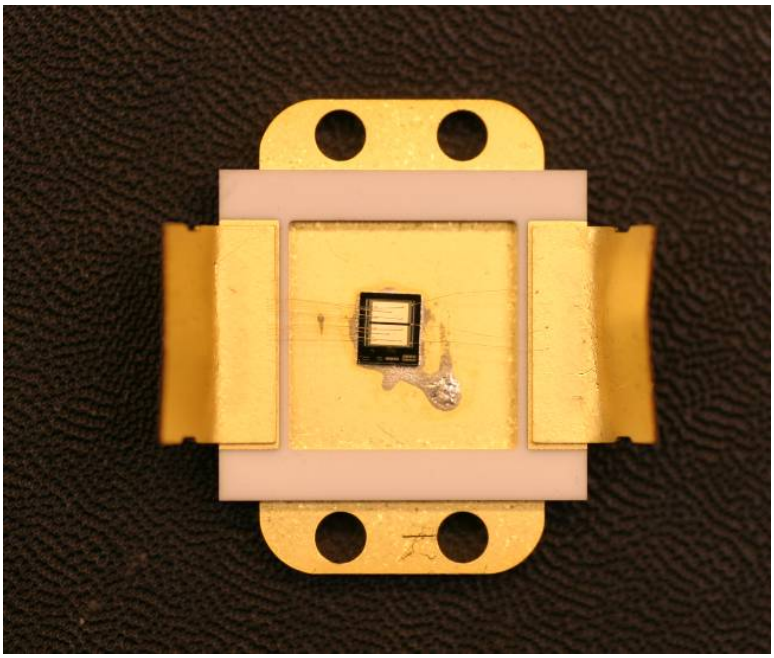


Figure 19 Packaged 3 X 3 mm BJT

4.2. Equipment Description

The device model was developed using Matlab 6.0 and all runs were done on an Apple MacBook Pro with a dual core 2.33 GHz Intel Core 2 Duo processor and 2 Gbytes of memory. The Matlab version used was designed for an IBM computer so it was run under Windows XP in a virtual machine using Parallels 3.0. Data was post processed using Microsoft Excel 2004 for the Macintosh.

4.3. I-V Description

The original goal of this work was to develop a BJT model that took into account heat generation caused by joule heating. This proved to be more difficult then planned due to limitations in modeling base current. The model was able to correctly generate the potential versus distance curve for the BJT at equilibrium (Figure 21). The model also produced a reasonable curve for a BJT in forward active mode (Figure 22). To generate these curves the potential was increased on the

collector while the emitter was held at a constant potential. This is similar to a device in forward active since the collector-base is being negatively biased while the emitter-base is being forward biased. The model uses linear voltage applied across the device to produce these curves. At each step a potential of -0.10 V was applied to the collector and at each node the voltage was reduced linearly such that the emitter had no potential applied to it.

Several different techniques to inject carriers into the base region were tried. These included applying a potential to the base, which prevented the model of converging. Other methods tried included adding and subtracting carriers at either a single point or across the base. The amount and timing of the additional carriers were also studied. In some runs the model was set to apply the total potential before adding carriers while in other runs carriers were added at each voltage step. In all cases the model either did not converge or it converged to the same results achieved without the additional carriers. The inability to inject base current prevented a full BJT analysis, so the model and experimental results are based on the PN junctions making up the emitter base diode and the collector base diode. The I-V curves were experimentally measured for both diodes from room temperature to 200 ºC. These curves were then compared with the data generated by the model. A scaling factor of 0.02 was used to convert the current density provided by the model to straight current provided by the curve tracer.

4.4. Model Performance Comparison

A unique capability of this model is the ability to use either the quasi Fermi method or the standard method to determine the values for potential and carrier

concentration. The standard method uses the values for potential and carrier concentrations directly while the quasi Fermi method replaces the values for n and p with a pseudo potential based on and n and p. Due to the challenges in modeling SiC most models utilize the quasi Fermi method. It was found that the standard method worked well in analyzing SiC as long as proper weighting values were used. This ability allows this model to provide a unique comparison between the performance and accuracy of the two techniques. Data from both techniques is compared to the experimental data to determine the accuracy and consistency of each method. Each junction is evaluated at 3 different temperatures using the two different modeling techniques. The two techniques are compared using the number of iterations, total run time, time per voltage step, iterations per voltage step, and time per iteration. The collector base performance (Figure 23) shows a large difference between the quasi Fermi method and the standard method. The standard method is over two times faster at all temperatures, and provides a 2 to 3 X reduction in the number of iterations required when compared with the quasi Fermi results. The average time per iteration is very similar for both methods so the difference between the two methods is caused by the quasi Fermi method not converging as quickly as the standard method. The emitter base evaluation (Figure 24) showed the standard method again out performed the quasi Fermi method. This junction was more difficult to accurately model using the standard method due to a large difference in carrier concentration between the two sides of the junction. To achieve convergence of the emitter base diode using the standard method required large scaling factors thus increasing the time to convergence. These scaling values had to be readjusted at several voltage steps

during the run further slowing the model. Even with large weight values and weight recalculations the standard method is more then 3 times faster then the quasi Fermi method. As was apparent in the collector base evaluation, the quasi Fermi method is 2 to 3 times slower in converging then the standard method. Part of the improved performance of the standard method is again caused by a lower number of iterations needed to reach convergence. Further performance improvement is due to the standard method calculating the results at each iteration more quickly. The iteration speed improvement is caused by a smaller emitter/base junction width reducing the number of spatial steps requiring calculation, which also reduces system overhead and further increases iteration speed. It was found that increasing the temperature caused both methods to converge more quickly. This affect was attributed to the reduction in the difference between the p and n type junction carrier concentrations, allowing the model to converge more quickly.

4.5. Collector-base Diode Comparison

4.5.1. Collector-base: Room Temperature

The accuracy of both methods was evaluated by comparing the model results with the experimental data obtained from the actual devices. The collector-base was initially analyzed using the standard method with a reduced collector thickness to reduce computation time. The scaled output (Figure 25) of the model did not match the measured data with the model producing much higher current then was actually measured. The shortened low-doped collector used in the model resulted in lower resistance then was actually measured so the model was modified to include the full 18 μm thickness of the collector. This hypothesis was tested using both the quasi

Fermi and standard methods. The results from both of these methods show very close correlation to the experimental results (Figure 26). While I expected improved accuracy, I did not expect the results to be so close in comparison with the experimental data because this model does not take into account resistance caused by the packaging and connections between the device and the curve tracer. The package only slightly increases the measured resistance limiting its affect on the accuracy of the model.

4.5.2. Collector-base: Elevated Temperature

4.5.2.1. Collector-base Evaluation of Results at 100 ˚C and 200 ˚C

Once the collector/base room temperature curves were generated several evaluations using both the standard and quasi Fermi methods were run at higher temperatures to determine model accuracy. The model run at 100 ºC (Figure 27) demonstrates a divergence from the experimental with the calculated results in both diode turn-on point and on resistance. This becomes progressively worse at 200 ºC (Figure 28). The modeled resistance and turn-on are both higher then the experimental results which is the result of two possible causes. The 1-D structure of the model does not solve for package resistance, so resistance was added to the modeled results to allow comparison with the experimental data (Figure 29). I found that increasing the resistance of the modeled data by 0.65 Ω brought the results into good correlation in resistance but, as expected, did not change the turn-on point. This level of additional resistance is quite high and packaging would not increase the resistance by this amount at 200 ˚C so limitations in the model were examined.

4.5.2.2. Collector-base Temperature Dependant Calculation Limitations

Several temperature dependant values are used in the model and limitations in these calculations reduce the model accuracy. To determine how these values affect the model, several model variations were run with modified values.

4.5.2.2.1. Collector-base Recombination at High Temperature

The first run looked at the affect that recombination had on the model results. With recombination turned off, the modeled resistance was lower then the experimental result (Figure 30) and the diode turn-on point was shifted higher. This result and the result with recombination turned on fall on either side of the experimental data in the linear region indicating that the recombination technique used in the model underestimates recombination at higher temperatures. Adding 0.1 Ω of resistance brought the model with recombination off into close approximation in the linear region but did not shift the turn-on point of the diode (Figure 31). The recombination calculations used in this model are limited to only trap-assisted recombination, which is the prevalent recombination mode in SiC due to the large number of defects. The inclusion of other forms of recombination and generation including surface recombination and impact ionization would improve the correlation between the model and experimental results at high temperatures.

4.5.2.2.2. Collector-base Carrier Ionization at High Temperature

The second evaluation turned carrier ionization off and also demonstrated a lower resistance and a higher turn-on voltage then the experimental results (Figure 32). As was the case with recombination turned off, an additional 0.1 Ω of resistance brought the modeled data into agreement with the experimental results in the linear

region (Figure 33). This is the same level of shift that was found when the recombination was turned off and indicates that carrier ionization and recombination calculations have a similar level of affect on the model. Based on this result the carrier ionization calculations are also underestimating the carrier concentration in the SiC at elevated temperatures resulting in lower current. Modifying the dopant ionization energy slightly would improve the resistance. Moreover, the use of more complex methods to solve the carrier concentration would improve the results. Two other temperature dependant values, mobility and carrier lifetimes, were not analyzed, but the addition of resistance is similar to changing the carrier lifetimes. Intrinsic carrier concentration is studied using the emitter-base diode.

4.6. Emitter-base Diode Comparison

4.6.1. Emitter-base Room Temperature

The emitter-base junction was analyzed using the same techniques as the collector-base junction. The experimental data was obtained from the same device used for the collector-base analysis at the same three temperatures. The model under calculates the current, which is expected due to the model not calculating the device resistance caused by device shape and package resistance (Figure 34). Figure 20 illustrates the problem areas in modeling the emitter-base diode with a 1-D model. The emitter-base diode is U shaped, which causes differences between the model and experimental data due to surface recombination, current crowding, base implant damage and an emitter area that is smaller then the collector area.

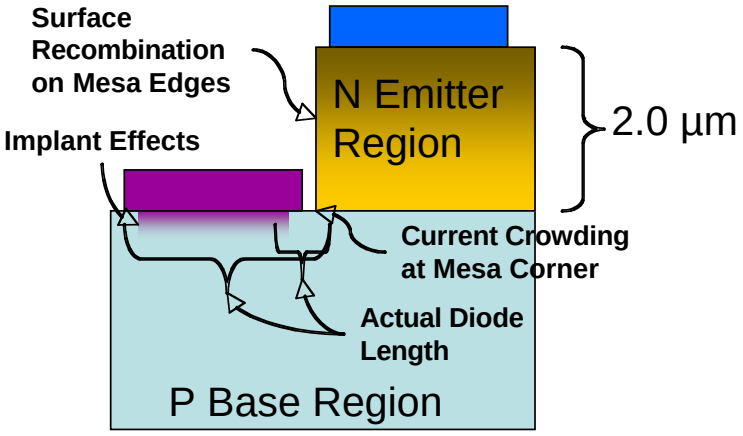


Figure 20 Problem areas in modeling emitter-base diode

To determine both turn-on point and the level of additional resistance caused by the non-modeled device affects, the model results were modified through the addition of resistance to match the linear region slope of the modeled data to the experimental data (Figure 35). It was found that .3 Ω of added resistance brought the curve into good correlation with the experimental data. In this evaluation the quasi Fermi method was slightly more accurate then the standard method. While the quasi Fermi improvement in accuracy was not analyzed it appears that reduced rounding errors improve the accuracy when analyzing junctions with a large difference between the junction doping levels.

4.6.2. Emitter-base Elevated Temperature

4.6.2.1. Emitter-base Evaluation of Results at 100 ˚C and 200 ˚C

The model was then run at 100 ºC and once again the model under calculated the resistance (Figure 36). To compensate for this, the same .3 Ω resistance was added to the modeled data to generate the data in Figure 37. The model was then compared with the experimental data obtained at 200 ºC and again the resistance was lower in the model (Figure 38). An additional .4 Ω brings the model into better

agreement with the experimental results (Figure 39). At this temperature, the .3 Ω resistance used at room temperature and 100 ºC did not work correctly so the resistance was increased to .4 Ω to provide better agreement with the experimental data. Again, this value is a much higher value then packaging would cause so additions to the model would be required to improve the accuracy.

4.6.2.2. Emitter-base Turn-on Point Evaluation

Increasing the temperature caused the turn-on point of both the emitter-base and collector-base junctions to shift from the experimental results. Many of the same calculations that affect the resistance also affect the turn-on point. As was noted before, the collector based junction model was modified by turning off recombination and assuming full ionization which resulted in both the output resistance and the turn-on point of the junction shifting from the experimental results (Figure 30, Figure 32). The emitter-base junction turn-on was also shifted but to a lesser degree then the collector-base. While several different calculations affect the turn-on point, the main one in this model is the intrinsic carrier concentration. To test this hypothesis the model was reprogrammed to allow varying carrier concentration values to be tested. The model normally calculates the intrinsic carrier concentration using several values, all of which are temperature dependant, using basic assumptions that are accurate at room temperature. At 200 ˚C the intrinsic carrier concentration calculated by the model is n_i= 159 /cm^3. To test the affect of varying concentration on the model, the intrinsic carrier concentration was set to values above and below this point, and the emitter-base junction was recalculated (Figure 40). Initially n_i was set to 100 /cm^3 and, as expected, the turn-on point shifted to a higher voltage. When n_i was set to

300 /cm^3 the turn-on point was close and when a resistance of 0.45 Ω was added the modeled results matched the experimental exactly. This resistance level is still high, but changes in the other temperature dependant values and the inclusion of effects that were not modeled would bring this value down.

4.6.3. Other Causes of Divergence at High Temperatures

There are two other variables that could cause the model to diverge from the experimental. The carrier mobility is a major factor in both the turn-on and resistance. The mobility calculations for silicon carbide are still being improved and improvements in the calculations used in this model would further improve the results. Due to the complexity in determining the actual values for the mobility the model generated values were not changed. Instead resistance was added to the results to bring them into correlation with the experimental data. The other temperature dependant parameter that was not looked at was the values calculated for carrier lifetime. These values have been experimentally determined but due to improvements in SiC materials the carrier lifetimes are constantly changing. Several of the other calculations including recombination use the carrier lifetime values making it difficult to determine how changes in the carrier lifetime modify the model results. Because of these multiple affects I did not analyze varying carrier lifetimes in the model.

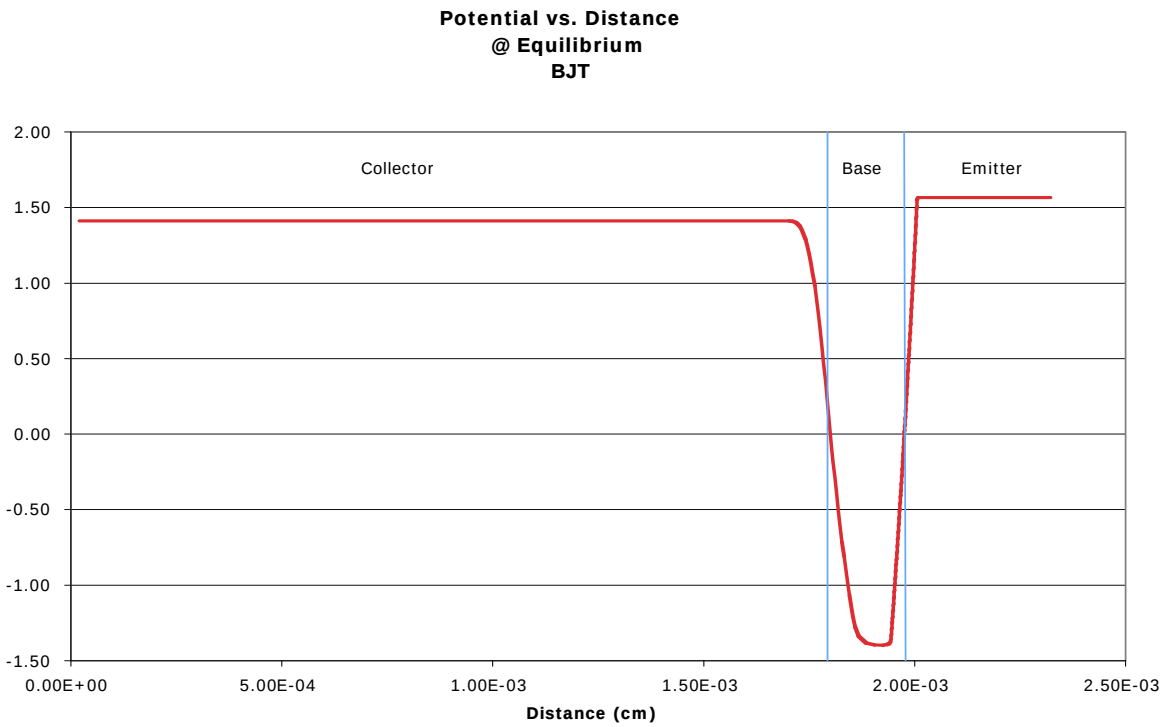


Figure 21 Potential versus Distance at Equilibrium 3 mm X 3 mm structure

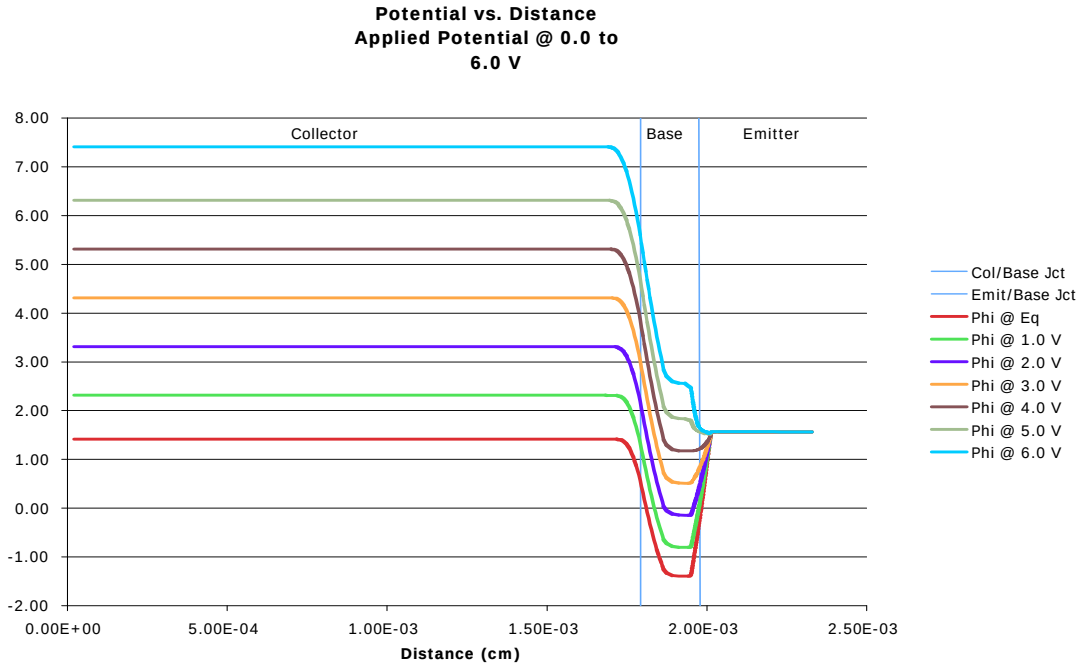
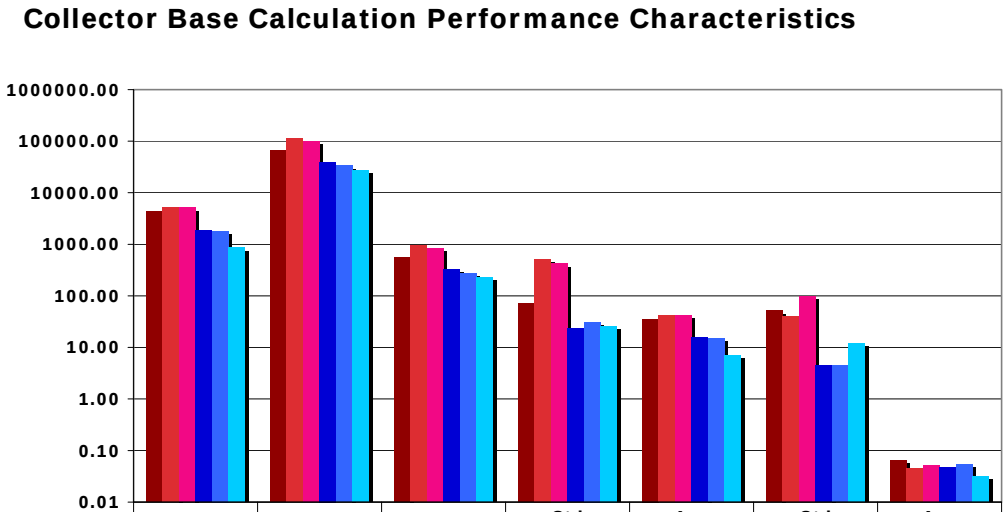
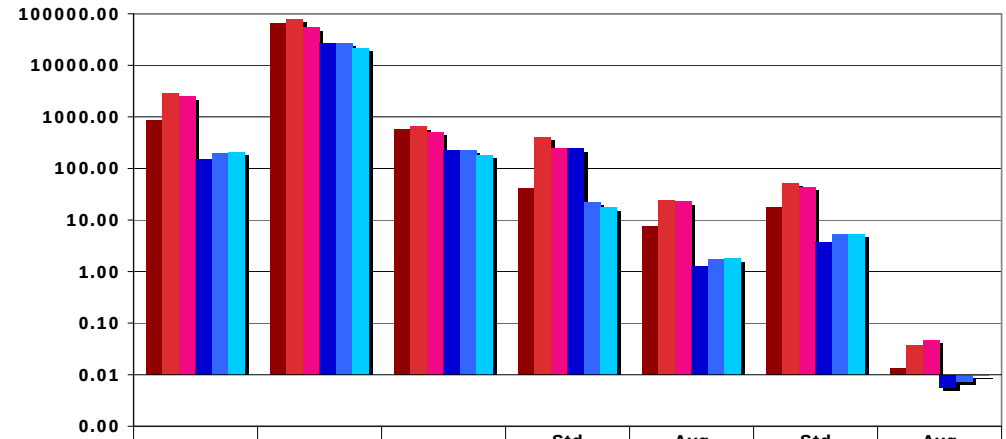


Figure 22 Potential versus Distance with Applied Potential 3 mm X 3mm Structure



	Total Time (sec)	Total Iter	Avg Iter/Step	Std Deviation (Iter/Step)	Avg Time/Step (sec/step)	Std Deviation (Time/Step	Avg Time/Iter (sec/step)
Quasi Method 23 °C	4317	66375	548.6	69.6	35.4	51.4	0.0650
Quasi Method 100 °C	5123	114609	947.2	521.5	42.0	39.5	0.0447
Quasi Method 200 °C	5115	99500	822.3	415.6	41.9	98.3	0.0514
Standard Method 23 °C	1850	39632	327.5	23.4	15.4	4.4	0.0467
Standard Method 100 °C	1810	33355	275.7	31.1	15.1	4.5	0.0543
Standard Method 200 °C	848	27261	225.3	25.9	7.1	11.9	0.0311

Figure 23 Collector base model performance



	Total Time (sec)	Total Iter	Avg Iter/Step	Std Deviation (Iter/Step)	Avg Time/Step (sec/step)	Std Deviation (Time/Step	Avg Time/Iter (sec/step)
Quasi Method 23 °C	867	64777	573.2	42.0	7.6	17.9	0.0134
Quasi Method 100 °C	2936	78819	651.4	401.9	24.1	52.4	0.0372
Quasi Method 200 °C	2471	53749	497.7	243.6	22.7	43.5	0.0460
Standard Method 23 °C	151	26801	229.1	242.7	1.3	3.7	0.0056
Standard Method 100 °C	199	26785	228.9	22.3	1.7	5.3	0.0074
Standard Method 200 °C	208	21588	184.5	17.5	1.8	5.3	0.0097

Figure 24 Emitter base model performance

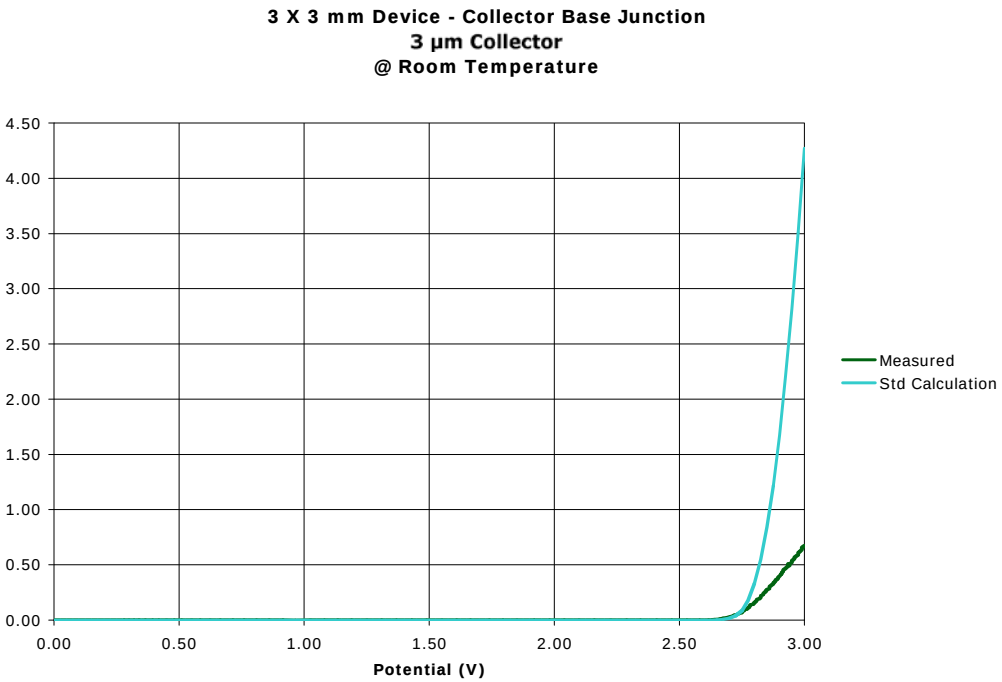


Figure 25 Collector-Base Junction I-V Curve with Collector Shortened to 3 µm

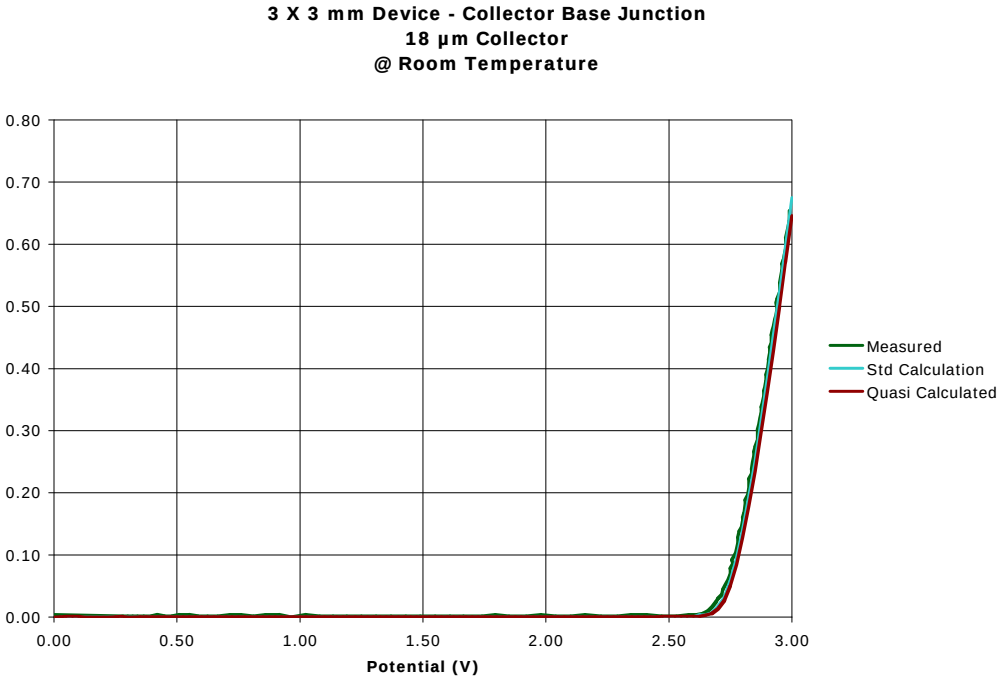


Figure 26 Collector-Base Junction I-V Curve with 18 µm Collector at Room Temperature

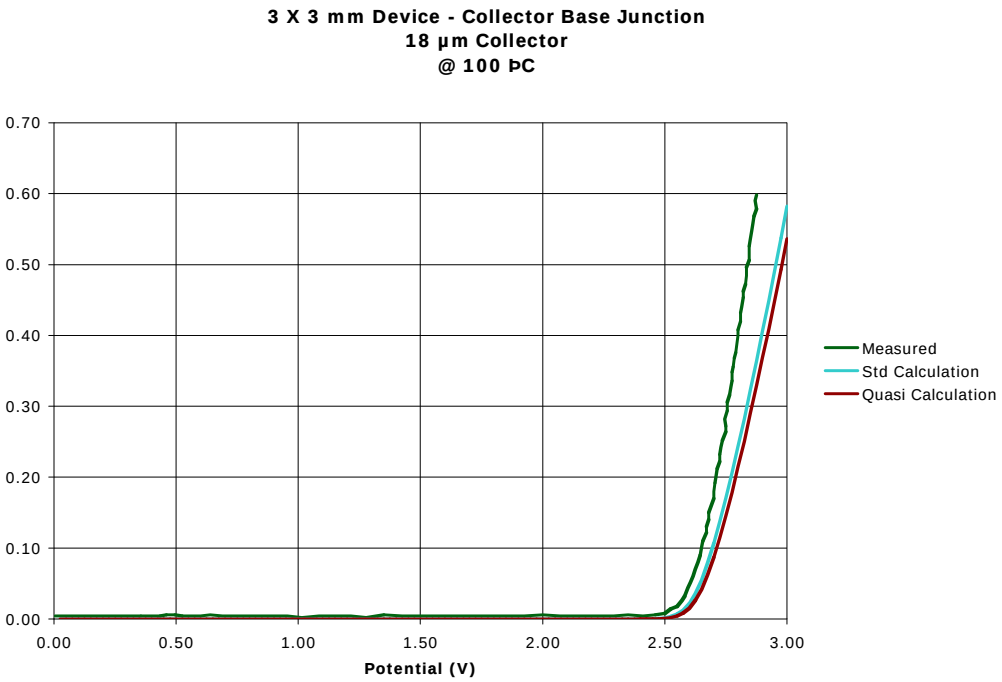


Figure 27 Collector-Base Junction I-V Curve at 100 ºC

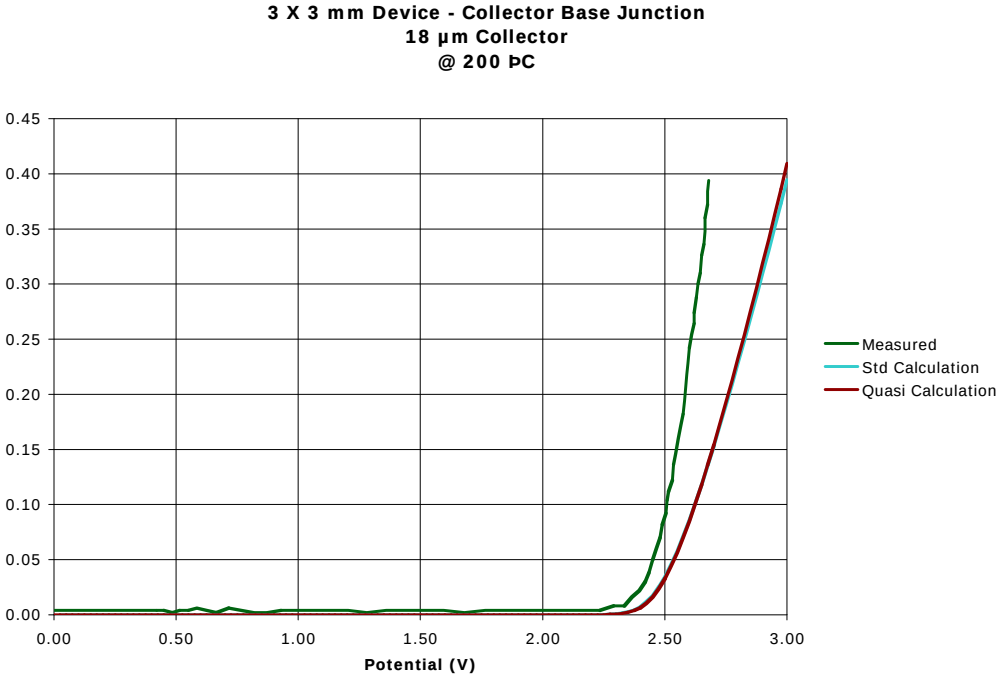


Figure 28 Collector-Base Junction I-V Curve at 200 ºC

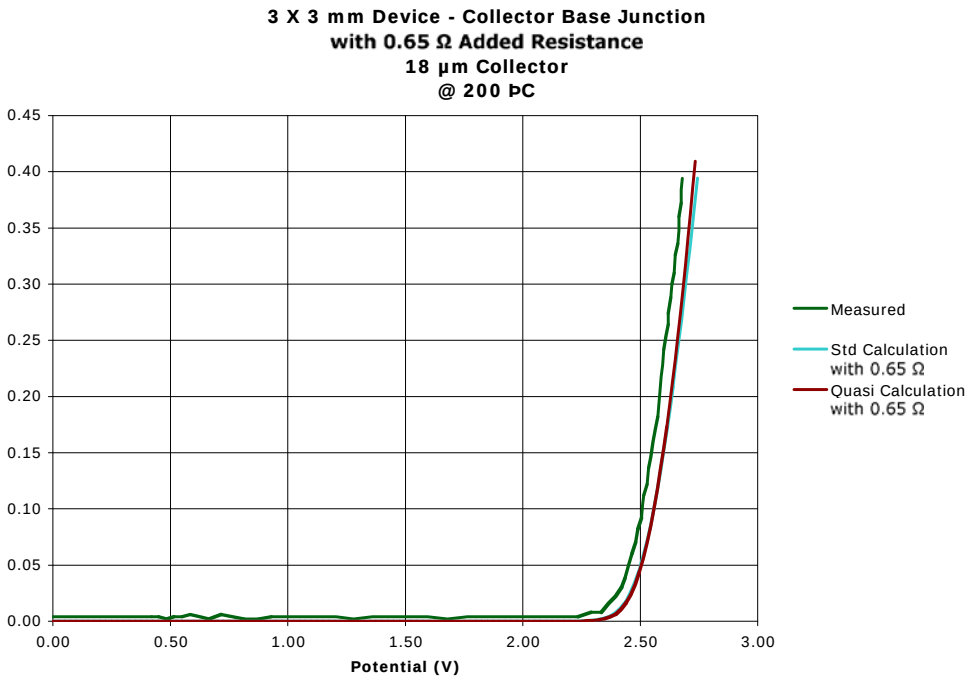


Figure 29 Collector-Base Junction I-V Curve at 200 ºC with 0.65 Ω added resistance

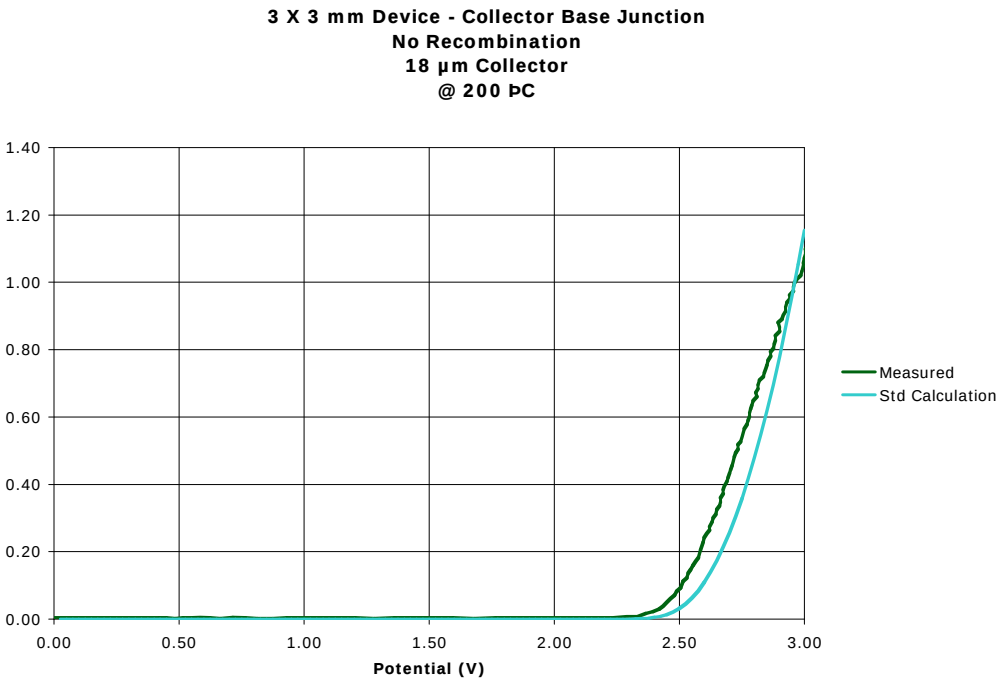


Figure 30 Collector-Base Junction I-V Curve at 200 ºC with No Recombination

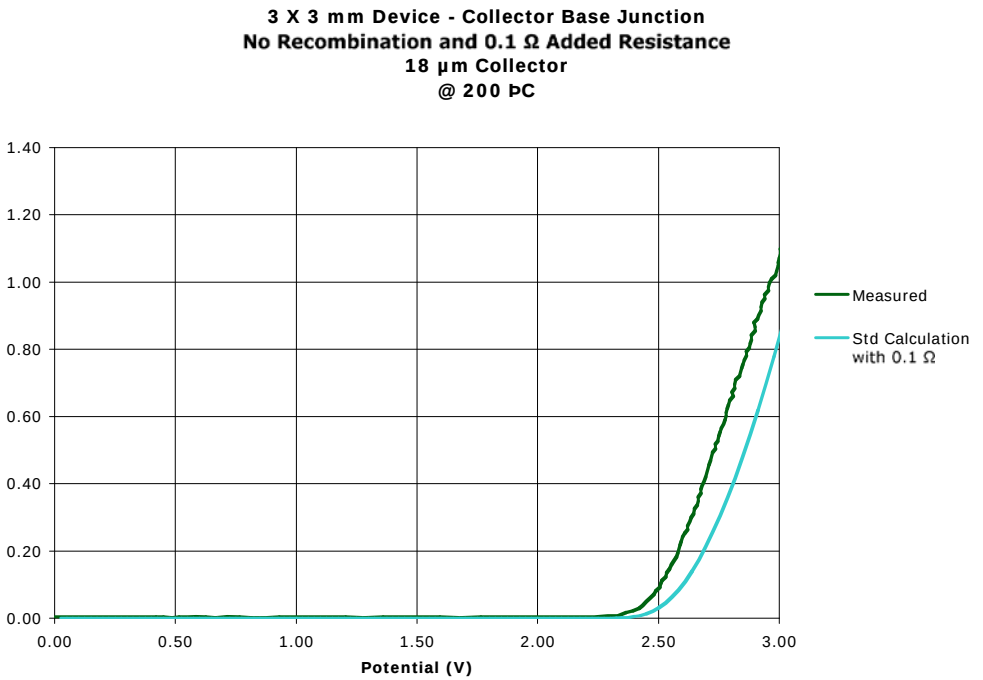


Figure 31 Collector-Base Junction I-V Curve at 200 ºC with No Recombination and 0.1 Ω of additional resistance

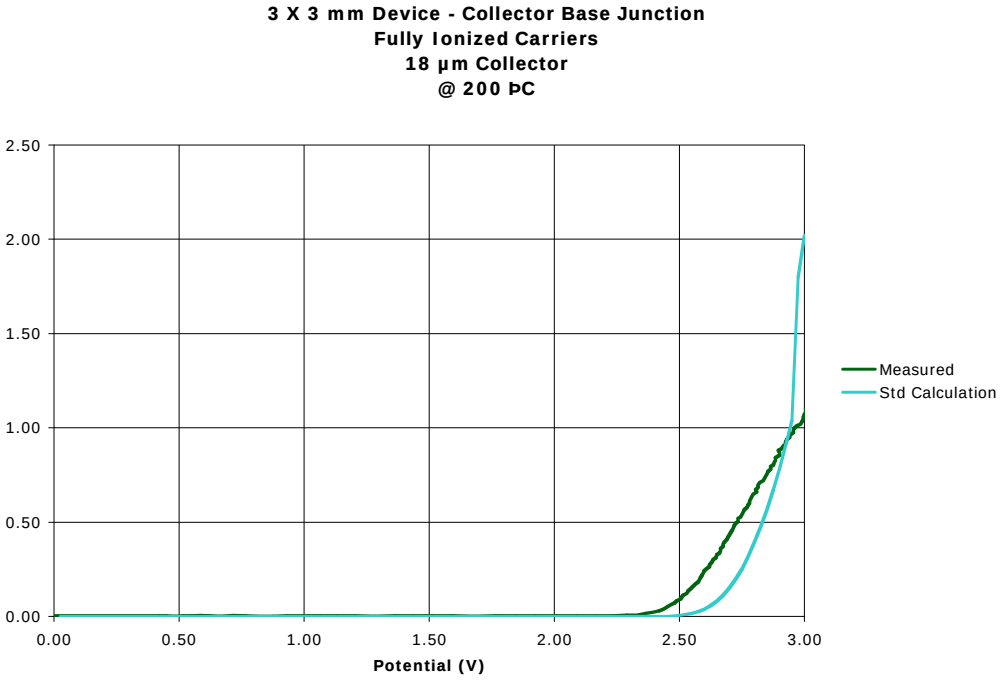


Figure 32 Collector-Base Junction I-V Curve at 200 ºC with Full Carrier Ionization

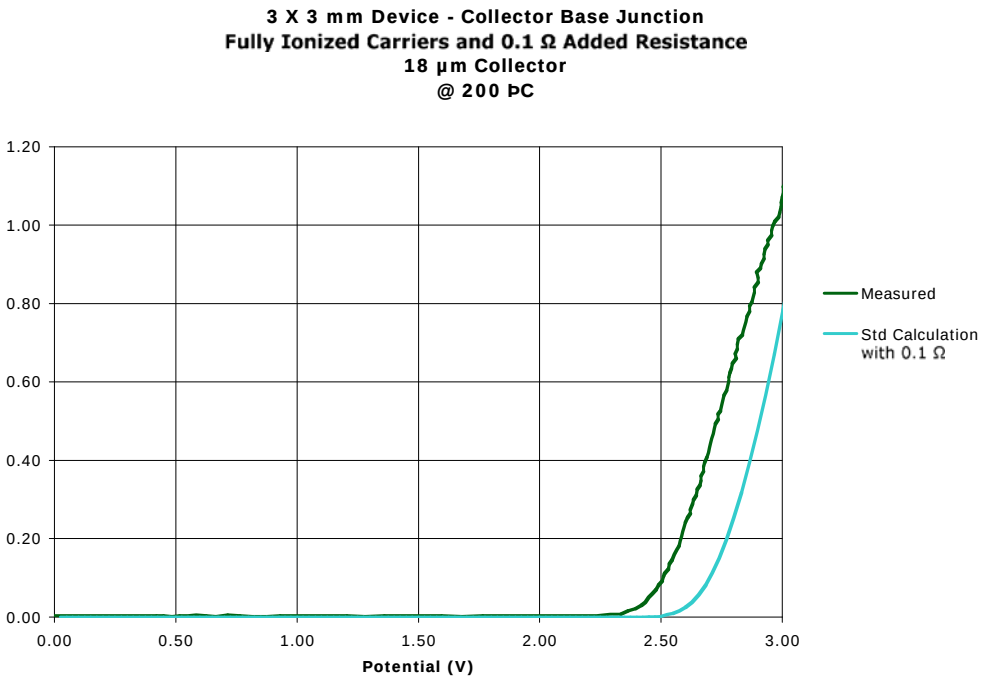


Figure 33 Collector-Base Junction I-V Curve at 200 ºC with Full Carrier Ionization and 0.1 Ω of additional resistance

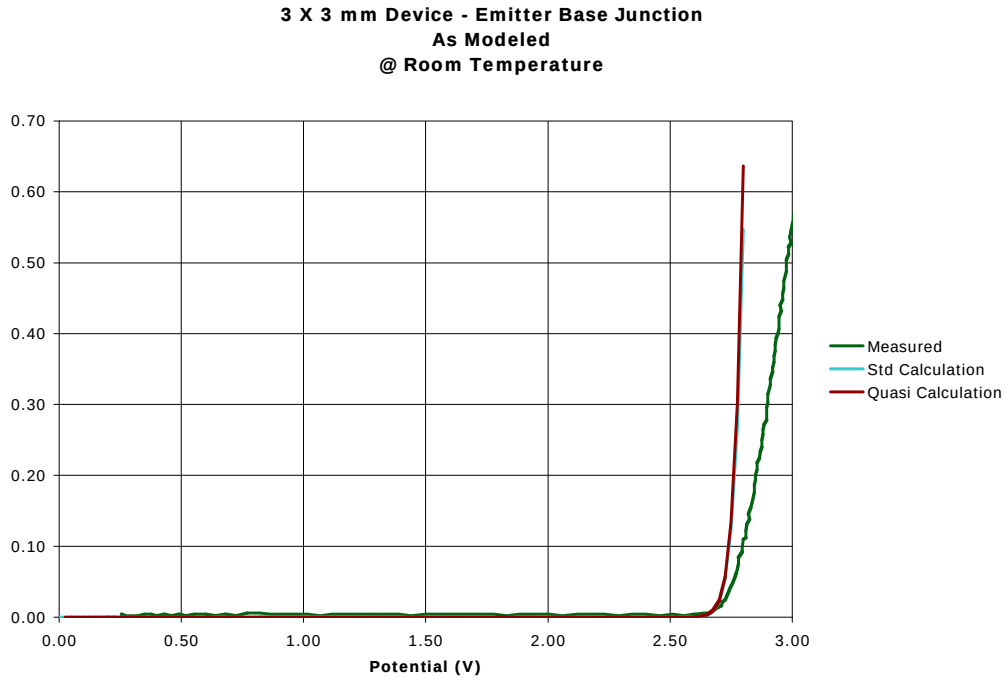


Figure 34 Emitter-Base Junction I-V Curve at Room Temperature

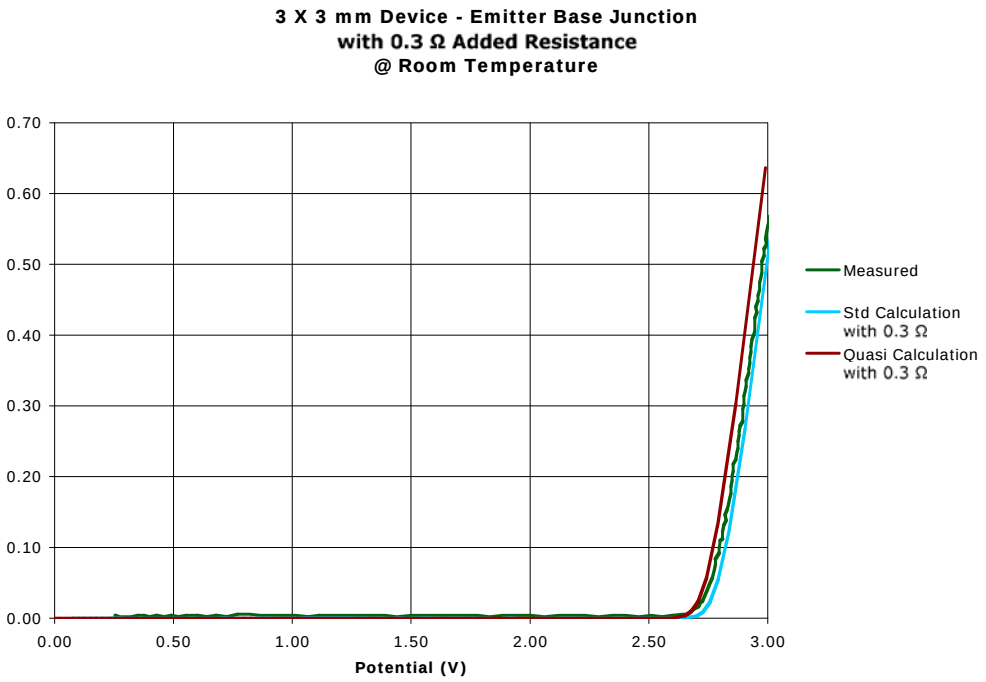


Figure 35 Emitter-Base Junction I-V Curve at Room Temperature with .3Ω of Added Resistance

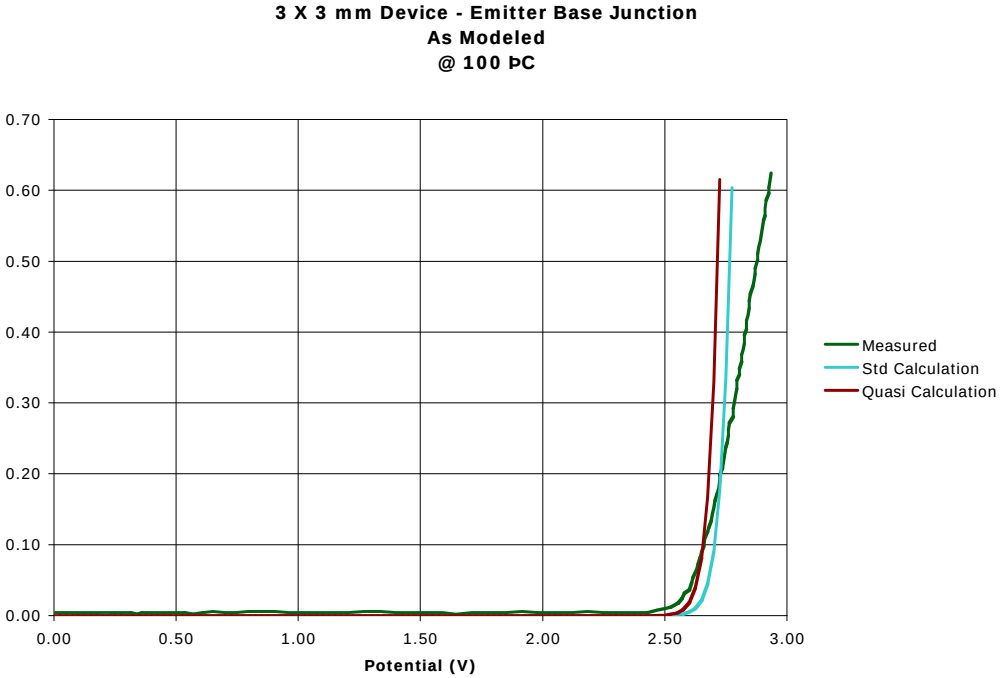


Figure 36 Emitter-Base Junction I-V Curve at 100 ºC

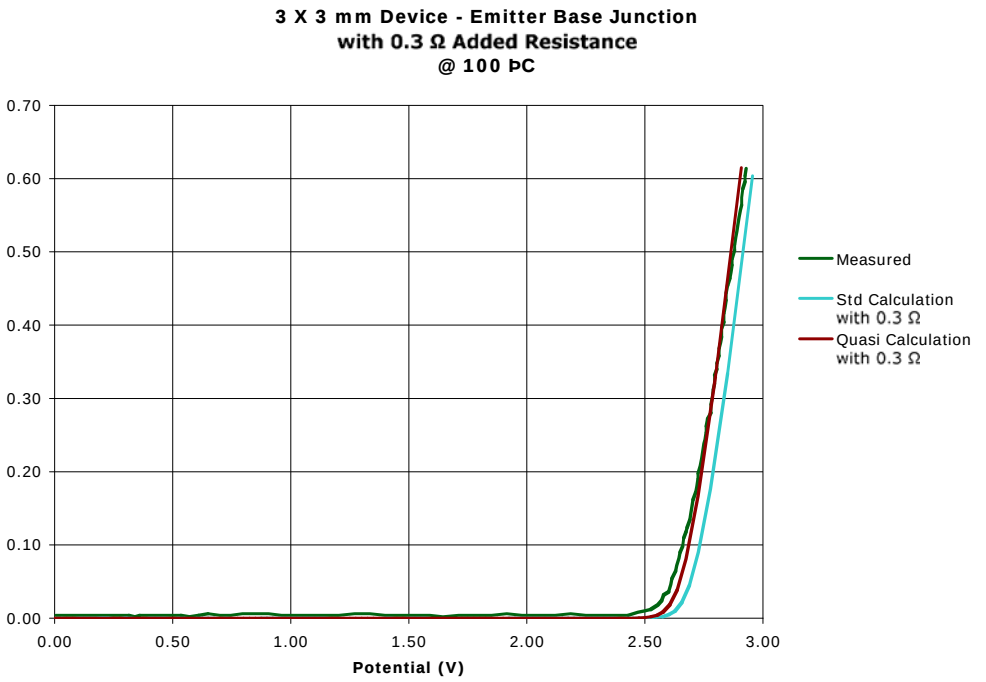


Figure 37 Emitter-Base Junction I-V Curve at 100 ºC with .3Ω of Added Resistance

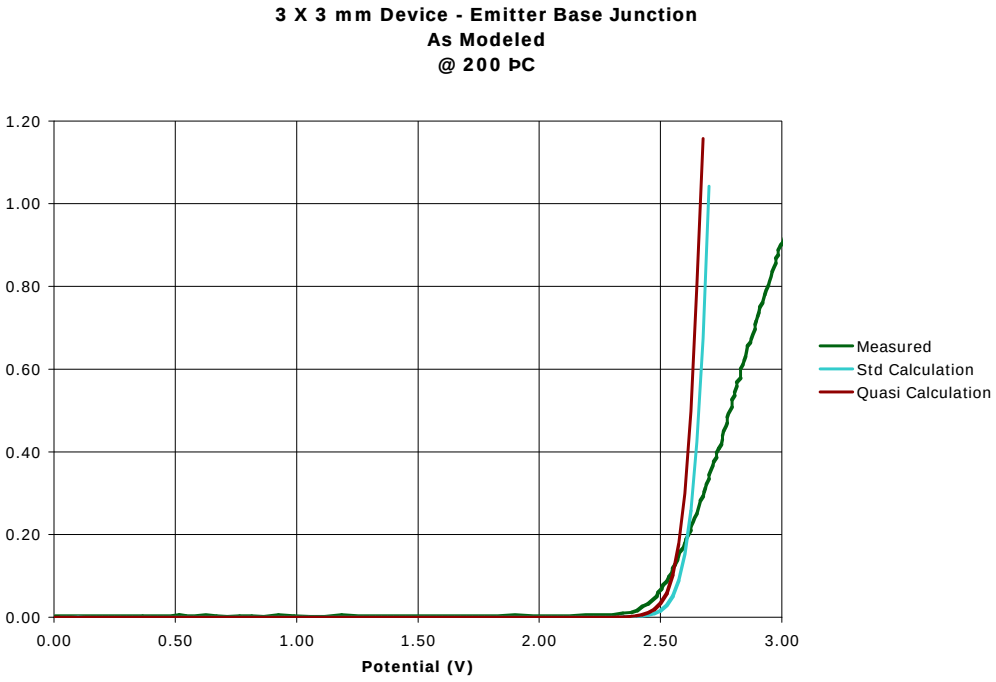


Figure 38 Emitter-Base Junction I-V Curve at 200 ºC

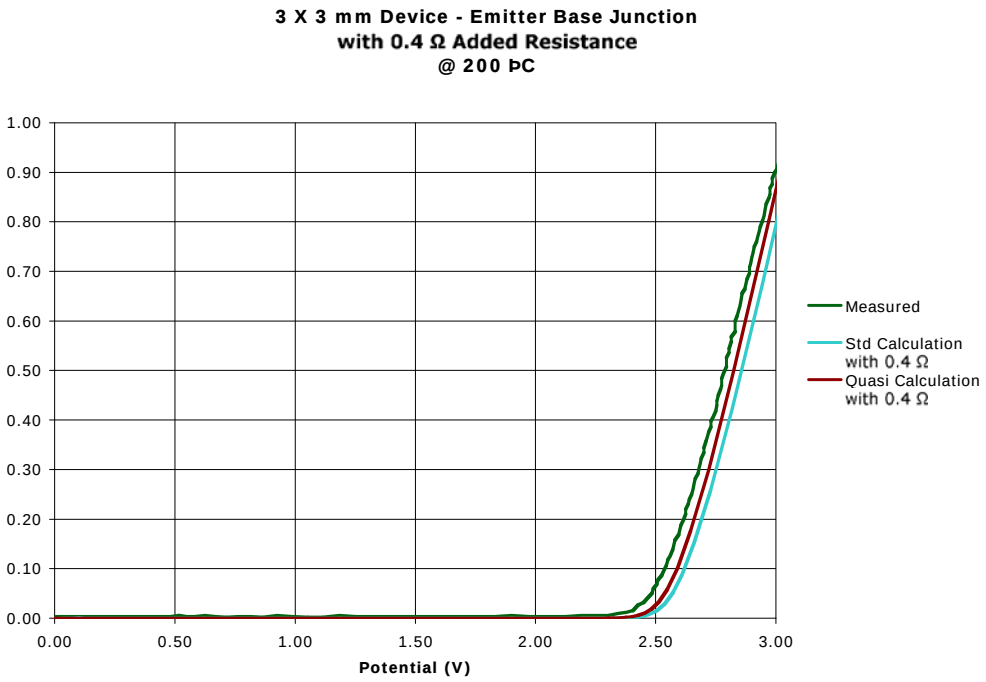


Figure 39 Emitter-Base Junction I-V Curve at 200 ºC with .4 Ω of Added Resistance

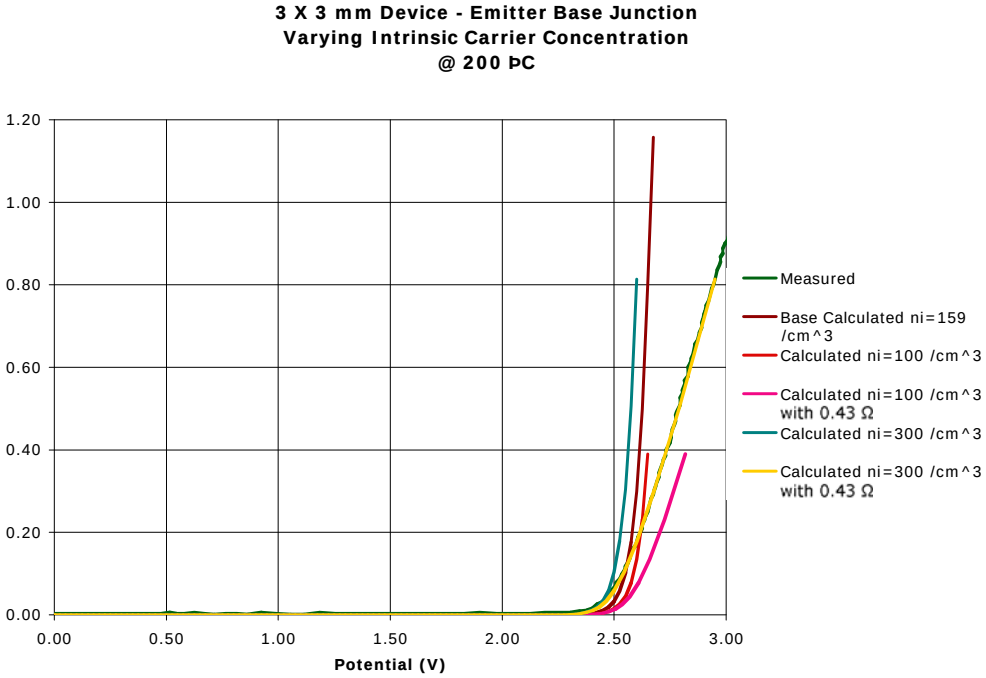


Figure 40 Emitter-Base Junction I-V Curve at 200 ºC with varying carrier concentration

Chapter 5: Summary and Future Work

The fabrication of silicon carbide devices is a challenge. Most of the fabrication discussed here involved the development of thyristors for power switching applications. The BJT design used similar techniques and a lot was started in support of the work discussed herein, but changes at the Army Research Laboratory prevented the completion of these devices. The devices used were fabricated by Cree using several of the processes developed at the Army Research Laboratory for the thyristor. The BJT was thought to be a simpler design than the MOS-FET because it is a normally off switch. This is preferred over the JFET's which are normal on switches. The challenges with gain drift in the BJT's turned out to be more difficult to solve than originally thought. As a result, the continued development of the BJT design is currently taking a back seat to the development of the MOS-FET. The SiC MOS-FET can replace a silicon IGBT while requiring smaller more efficient gate drives.

Several factors make silicon carbide a difficult material to model and thus reduce the accuracy of the model developed herein. Silicon carbide has been intensely studied for use in electronics only since the late 1980's. The process and materials fabrication capabilities continue to evolve improving device performance and reducing performance variations between devices. While the reduced spread in device performance improves model device convergence, many of the constants used in the models are changing as improved materials become available. As these constants converge, model accuracy is improved. In this work the most difficult constant values to obtain were the carrier lifetimes. Several different carrier lifetime

values were used during model development. The basic properties of silicon carbide also contributed to difficulties in developing the models. Silicon, and other narrow band semiconductors, can be modeled assuming full carrier ionization when at or above room temperature. For wide bandgap materials, such as silicon carbide, this assumption does not hold and additional calculations are required to determine carrier ionization levels. These calculations rely on thermally varying values, which further increase the computational complexity. This requires a large number of constants, some of which have only recently been experimentally determined. Mobility calculations for silicon carbide are very complex and the technique used in this model did not fully integrate all the solution methods available further reducing the models accuracy. Even with these limitations the model was very accurate when calculating room temperature performance of the device. The model accuracy decreased as the temperature increased demonstrating the limitations of the model at higher temperatures. This model was developed to provide a simple method to determine basic device performance and fabrication. Further development of the model through the use of more complex methods would improve the accuracy at the expense of simplicity.

Originally the model was intended to solve for the current in a BJT structure while calculating the resistive heating in the device. This proved to be extremely difficult due to the challenges in injecting carriers into the base region. To properly model the BJT required a method to inject current into the base region while forward biasing the emitter base diode and reverse biasing the collector base. The model demonstrated the ability to properly bias the two diodes but a technique to provide

current injection into the base proved to be difficult. Several methods were tried where extra charge was applied to the base regions of the model. Several additional attempts were made where new equilibrium values were found after additional holes were added to the base region. Many variations were tried that adjusted the level of carriers added, the methods used to apply the carriers across the base region, and the techniques used to arrive at a solution. The level of carriers added to the region ranged from a small percentage of the total excess carriers under bias to very large values approaching the background doping level. Very small values would converge but the large values did not converge. Several methods of applying the carriers to the base region including linear, and non linear were tried with the linear being the quickest to converge albeit to an incorrect answer. Both single and iterative methods were tried to improve convergence with no luck. The inclusion of the capability to solve for BJT structures using this model is important future work for providing a simple model to provide quick calculations necessary in developing basic structure and fabrication requirements.

The final model did solve the current and voltage for a silicon carbide diode and was used to analyze the diodes that make up the emitter-base and collector-base junctions of the BJT. These diodes are good choices for modeling with the emitter-base diode being a short diode, having a large dopant concentration difference between each side while the collector base diode is very deep on the collector side but the doping concentrations are similar. The emitter-base diode has 2 dimensional aspects that were more difficult to accurately model and required additional resistance to be added to the results. With this modification the model results compared

favorably with the experimental near room temperature but diverged as the temperature increased. Future work would include the addition of improved methods for handling higher temperatures.

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