ABSTRACT

Title of Document: FABRICATION AND PROCESS DEVELOPMENT FOR AN INTEGRATED OPTICAL MEMS MICROSYSTEM IN INDIUM PHOSPHIDE

Nathan Paul Siwak, Doctor of Philosophy, 2013

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This dissertation presents the design, fabrication, and evaluation of the first monolithically integrated MEMS resonant sensor system realized in the InP-InGaAs material family. The integration of a MEMS sensor along with the facilitating optical interrogation platform provides for increased manufacturing scalability, sensitivity, and reduced measurement noise and device cost. The MEMS device presented in this dissertation consists of an Indium Phosphide (InP) cantilever waveguide resonator whose displacement is measured optically via a vertically integrated laser diode and

waveguide photodetector. All three major components of the sensor were integrated in a single 7.1 µm thick molecular beam epitaxy (MBE) epitaxial growth, lattice matched to an InP substrate. Full fabrication of the integrated MEMS device utilizes 7 projection lithography masks, 4 nested inductively coupled plasma (ICP) etches, and over 60 discrete processing steps. This dissertation focuses on the integration design and the development of specific III-V semiconductor fabrication processes in order to completely fabricate and realize these devices, including specialized ICP etching steps and a MEMS undercutting release etch. The fabricated devices were tested and characterized by investigating the separate component subsystems as well as the total combined system performance. Investigation of device failure and performance degradation is performed and related to non-idealities in the device fabrication and design. A discussion of future work to improve the performance of the system is presented. The work in this dissertation describing the successful fabrication process and analysis of such a complex system is a milestone for III-V based optical MEMS research and will serve as the groundwork for future research in the area of optical MEMS microsystems.

FABRICATION AND PROCESS DEVELOPMENT FOR AN INTEGRATED OPTICAL MEMS MICROSYSTEM IN INDIUM PHOSPHIDE

By

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Dissertation submitted to the Faculty of the Graduate School of the
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Dedication

To my amazing friends and family for never growing tired of my ever receding “deadlines,” my wonderful wife Julie, who is not listed as an author in this work but should be, and last but not least the One who makes all of these things possible.

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Table of Contents

List of Tables

List of Figures

1 Introduction

Motivation

The need to monitor the environment and detect various chemicals is a critical task for industrial, military, and homeland defense applications. Recent developments around the world, such as terrorism and bioterrorism, beg the need for devices which can be used to screen and measure levels of toxins in a variety of situations. Biological hazards such as anthrax and the flu virus pose serious challenges for sensing technologies [1]. In addition to these biological hazards, chemical sensors are also sought for the detection and prevention of exposure to chemical warfare agents which have been common on the modern battlefield [2]. Additionally, chemical monitoring in industrial applications and emissions measurement have both continued to be areas of research requiring sensors that can be readily deployable and able to withstand severe operating conditions.

In each of these cases, detecting and identifying agents quickly and accurately while maintaining a system with low power, minimal infrastructure, high sensitivity, and portability is highly desired. Recent sensing methodologies which are common for these applications have been focused on technologies utilizing thermal sensors, capacitance sensors, and optical transmission [3-6]. These devices have the benefit of being readily fabricated and simple to implement and use. Integrating these components with electronics and other devices has been a major thrust in the development of these devices and has been the subject of much research in this area.

The integration of sensor systems can present a number of difficulties stemming from various packaging and interfacing schemes, which are often conflicting in their requirements. MEMS technology is ideal in terms of providing infrastructure and materials for systems-based approaches. With fabrication technologies and devices directly compatible with conventional silicon technology, MEMS has been a multi-disciplinary and diverse field in the study of systems engineering and integration. This makes MEMS technology ideal for the development of these future sensor systems, as the importance of portability and mass production become more important. Cantilever-based MEMS sensors are prime candidates to be used as portable chemical sensors due to their relative simplicity [7], flexibility [8, 9], and compatibility with conventional processes [10, 11].

III-V materials

III-V materials have long been studied for use in high performance electronic and optical systems. With the development of epitaxial growth, it has allowed researchers to grow compound semiconductors with nearly arbitrary composition, and thus exhibiting widely varied material characteristics. With the ability to dictate properties such as the bandgap, refractive index, and fabrication selectivity of each individual layer has come the broadened scope and vision for researchers and the expansion of the field of compound semiconductors into previously unexplored territories.

The initial push for the use of compound semiconductors stemmed from the very high electron mobilities, mean-free-paths and the direct-bandgap electronic

structure possessed by III-V semiconductors over traditional silicon based technology [12]. Many authors have highlighted the high speed transistor technologies made possible through the development of InP-GaAs compound semiconductor epitaxy. Devices such as HEMT's [13], MODFET's [14], and integrated optical receivers/HEMT's [15] are made possible through the unique electronic properties of III-V semiconductors.

A primary advantage of III-V materials is their tailorable direct bandgap via the growth process that enables growth of material exhibiting optical gain. GaAs was one of the frontrunners in this field of solid-state optics with a maximum bandgap wavelength of ~870nm, sufficient for early generation communication systems. With the transition to longer wavelength communications technologies, particularly 1.55 µm, InP soon emerged as an alternative material system to enable the fabrication of longer-wavelength active devices (1.660 µm – 0.925 µm) [16, 17]. The continued quest for high speed communications technologies combined with the ability to create active optical elements and high speed electronics in InP simultaneously brought about the first monolithic integration of these optical and electrical components; such as high speed optical receivers and modulators [15].

In recent years, microelectromechanical systems (MEMS) using InP-based materials have been investigated to augment these optical networks [18]. A number of examples have been reported in literature of optical modulators and demultiplexers [19-24], couplers [25, 26] all designed in III-V materials to facilitate monolithic integration of these optical components with photodetectors and sources.

Approach

The approach of this dissertation is to take advantage of the versatility of III-V semiconductors to facilitate the monolithic integration of a MEMS resonant sensor, as depicted below in Figure 1.1. A novel interrogation technique will be used to measure a MEMS resonant sensor that includes the use of an on-chip light source, and an on-chip photodiode. This work builds upon previous work [26-32] which served to develop each component of this system separately, with the culmination of ultimately integrating them on one chip.

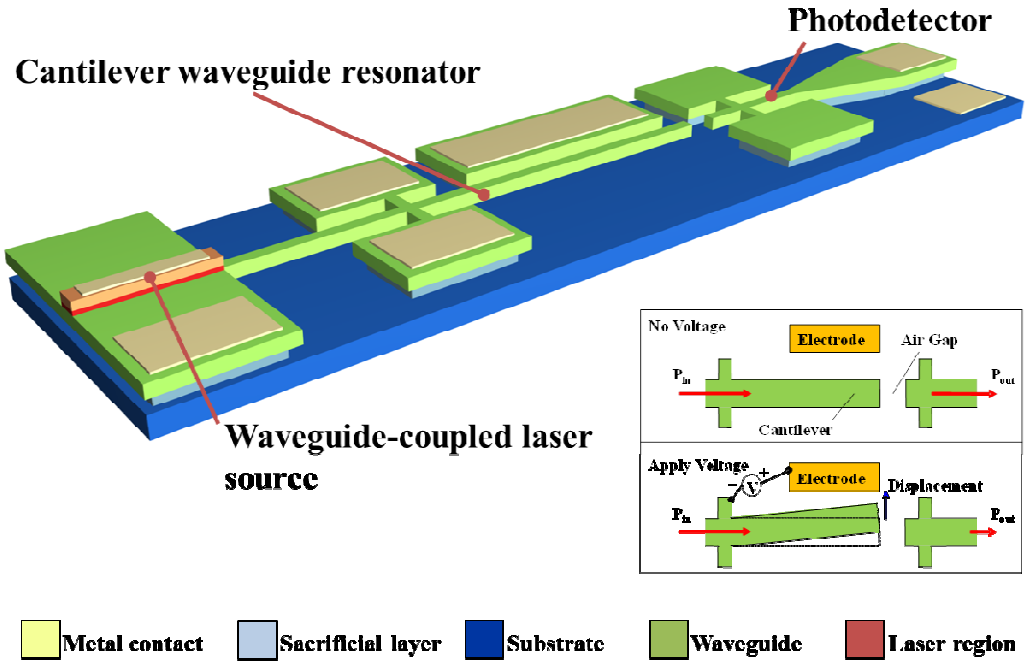


Figure 1.1. Conceptual schematic of monolithically integrated MEMS resonant sensor with device components notated.

Research Accomplishments

This dissertation seeks to explore the monolithic integration of optical sources and photodetectors with passive waveguides developed in the Indium Phosphide (InP) material system to establish a **single-chip** resonator sensor utilizing a novel readout

technique. These sensors are intended to be general-purpose, functioning as a microbalance sensor to measure chemical reactions, vapors, radiation, or fluid flow. The bulk of the research work performed for this project lies in the design of the integration scheme and the development of the fabrication procedures utilized to realize the integrated system.

1.1.1 Design of an epitaxial layer structure and optical MEMS devices

A vertically offset monolithic integration scheme was designed for the integration of a multiple quantum well laser source, an optical MEMS cantilever resonator sensor, and a waveguide integrated PIN photodiode within a single epitaxial growth. The system is designed to be implemented on one InP wafer with epitaxially grown layers to create each of the independent subsystems and also link them together into a functioning device. Multiple quantum well lasers were designed to emit at 1.55 μm wavelength, below the bandgap energy of the InGaAsP waveguide lying beneath this region. The InGaAsP-InP waveguide region is designed to function as a waveguide, as well as a cantilever resonator and is created with slight tensile strain. These waveguides are clad with an underlying InGaAs sacrificial material that can be removed to create released moveable structures. This sacrificial cladding has a lower bandgap energy than the emitted wavelength and thus is designed to be the intrinsic absorber region for the final photodiode component of the system. An epitaxial layer growth incorporating these elements was established and characterized in-house at the Laboratory for Physical Science (LPS). This design

provides a more simple alternative to more complex integration methodologies, both hybrid and monolithic.

1.1.2 Development of fabrication procedures

Fabrication processes were developed and established in order to realize the first physical implementation of a fully integrated optical MEMS microsystem. Dielectric deposition techniques, metallization, and other fabrication steps were all performed on an InP substrate first, and then on epitaxially grown substrates. A significant effort was made in establishing inductively coupled plasma (ICP) etching steps that were utilized for the definition of laser facets, waveguides and deep electrical isolation trenches. Each fabrication step needed to be carefully optimized in the perspective of being compatible with each section of the epitaxial growth and each additional fabrication step. This successful fabrication process with such a complex epitaxial growth is a milestone for III-V based optical MEMS research.

1.1.3 Testing of each component in the system

Each component of the fabricated microsystem was tested separately in an attempt to verify the operation of each subsystem. Characterization of each: laser, waveguide, and photodiode, was carried out with standard methods and procedures and compared with literature. The complete system was tested together in various environments ranging from cryogenic to ambient and the performance was analyzed and evaluated. Failure analysis was performed in order to better understand the critical parameters involved in the system-wide integration of these subsystems.

Dissertation structure

This dissertation is structured as follows: A literature review of optical MEMS technologies, monolithic optical integration, and sensor methodologies will be presented in section 2, meant to give a background of the current technologies available for monolithically integrated optical MEMS and sensor systems. The design of an epitaxial layer structure for this integrated system, cantilever waveguide resonators, and PIN photodiodes with relevant simulations and modeling will be presented in section 3. Section 4 covers the fabrication of the microsystem, with details covering each unit-process developed to enable the final structure. Testing elements such as setup and experimental procedures with the associated results of laser diodes, cantilever waveguides, and PIN diode results will be presented in the context of the two major fabrication runs accomplished with epitaxial growths in section 5. The data analysis and further discussion of the results from both of these fabrication runs will also be given in section 5. Finally section 6 will present a brief summary of the results, future work, and a final conclusion.

2 Literature Review

History of MEMS technologies

Micro-electro-mechanical Systems (MEMS) are traditionally described as the integration of mechanical elements with electronics on the microscale. Electronic components often are forced to interact with the environment through the use of external sensors and actuators. Combining these two separate functionalities via multi-chip packages or other interconnection and packaging techniques introduce unwanted parasitic effects, particularly as circuits and electronic equipment continue to be miniaturized. MEMS technology aims to address these shortcomings, which often lead to reduced sensitivity and increased power consumption, by miniaturizing external sensors to the point of integrating them directly alongside the IC control and readout circuitry [33, 34].

Arguably more important however, MEMS take advantage of the high volume and parallel fabrication which make the IC fabrication industry so cost effective for high volume production [33]. IT is the hope that this approach will greatly reduce the cost of sensors, increase sensor reliability, and decrease assembly complication. Due to their small size, a number of sensing or actuating functions can be integrated monolithically in the same device, further reducing cost, chip size, and increasing functionality [35]. All of these factors contribute to making MEMS sensors more attractive than many of their macro counterparts [36] and have continued to drive the continues investment in this technology both in academia and industry.

There have been a number of MEMS commercialization successes which capitalize on the aforementioned high volume production, most notably accelerometers, gyroscopes, projection systems, and pressure sensors [37]. The MEMS mechanical elements in these examples are generally fabricated using techniques common with standard IC fabrication such as lithography and dry etching. Certain cases however require more specialized tools and processes in order to realize. These techniques, generalized in the term "micromachining," consist of primarily two basic processes: bulk micromachining and surface micromachining.

Bulk micromachining indicates that the fabrication process involves removing large portions of the substrate, in most cases silicon, to fabricate a mechanical structure [38]. Most commonly, wet etching processes are used in bulk micromachining due to their high etch rates and ease of implementation. Examples such as the anisotropic etchants potassium hydroxide (KOH), tetramethylammonium hydroxide (TMAH), and ethylenediamene pyrocatecol (EDP) and the isotropic hydrofluoric, nitric, and acetic acid (HNA) etchant [35] are common in bulk removal. In addition to wet etching, some "dry" etching processes have been developed to perform the same tasks without the added complexity of drying fragile mechanical devices after wet processing. Xenon diflouride (XeF_2) gas is used to etch silicon isotropic ally, and other fluorine chemistries are used in conjunction with plasma etching systems to etch isotropically. Deep Reactive Ion Etching (DRIE) provides an anisotropic plasma etch, however is a special case of bulk removal as a cyclic etching technique.

Surface micromachining processes involve releasing thin layers of material that have been deposited and patterned on top of the substrate and tend to be more compatible with the traditional IC fabrication processes due to their smaller scale. An illustrative and common example of surface micromachining is associated with the fabrication of CVD polysilicon structures. A sacrificial layer such as silicon dioxide (SiO_2) is deposited on the substrate due to its high selectivity in a hydrofluoric acid (HF) etch compared to bulk silicon and polysilicon. On top of the SiO_2 sacrificial layer, a layer of polysilicon is deposited. Once it is deposited, the sacrificial layer is removed via a number of undercutting techniques, yielding a thin, released structure made from deposited films. Modern accelerometers utilize this fabrication method. Examples of silicon on insulator (SOI) substrates utilizing a similar fabrication scheme are very common, however with the added advantage of a single-crystal suspended mechanical layer as opposed to the amorphous polysilicon.

Optical MEMS

MEMS research has expanded greatly since the early 1980's and has generated a number of specializations, one of which is the field of micro-opto-mechanical systems (MOEMS). Optical MEMS are a subset of the MEMS research field which specifically deals with light generation and manipulation using microscale structures and elements. As mentioned in section 0, these devices are designed and intended to take advantage of the highly parallel fabrication methods inherent in IC fabrication technologies. Many different technological focuses lie in the scope of optical MEMS with current research focus on display technologies [39, 40], biomedical imaging [41, 42], miniaturized camera lenses [43], FTIR spectrometers

[44, 45], astronomy [46, 47], photonic integrated circuits (PIC's) [48, 49], free-space optical routing and beam steering [50-52], and tunable lasers [53-56] to name a few examples.

A large number of materials are used in the development of these devices, such as: silicon, polymers, or III-V direct bandgap semiconductors. The selection of the materials depends on the application and level of system integration desired. Optical MEMS can be generalized into two major categories of system architectures: free-space and guided.

2.1.1 Free-Space optical MEMS

As the name suggests, free-space optical MEMS devices process light by using mirrors and refractive elements. Common examples of free-space optical MEMS are optical switches and routers for fiber communications applications, laser scanning mirrors, micro lens technologies, and interferometers [57, 58]. Devices targeted for communications technologies are considered beneficial for very large scale applications such as backbone networks due to their flexibility and scalability with data format and port count, relative wavelength insensitivity, and also for their relative low power consumption compared to traditional macroscale counterparts [57]. Free-space switches also benefit from high throughput and protocol transparency for transport. These beam routing examples showcase designs which incorporate simple "on-off" mirrors which block or transmit light [59, 60]; however some work has concentrated more on beam steering devices [40, 50-52, 61, 62 2003, 2003, 2003, 63-65]. An elegant example of an optical MEMS free-space router was initially reported by Ford *et al* [66] and later finalized by Neilson *et al* [67], and

describes two arrays of 2-axis beam steering mirrors which utilize microlens arrays to help collimate the beams as they are propagated through the system (Figure 2.1).

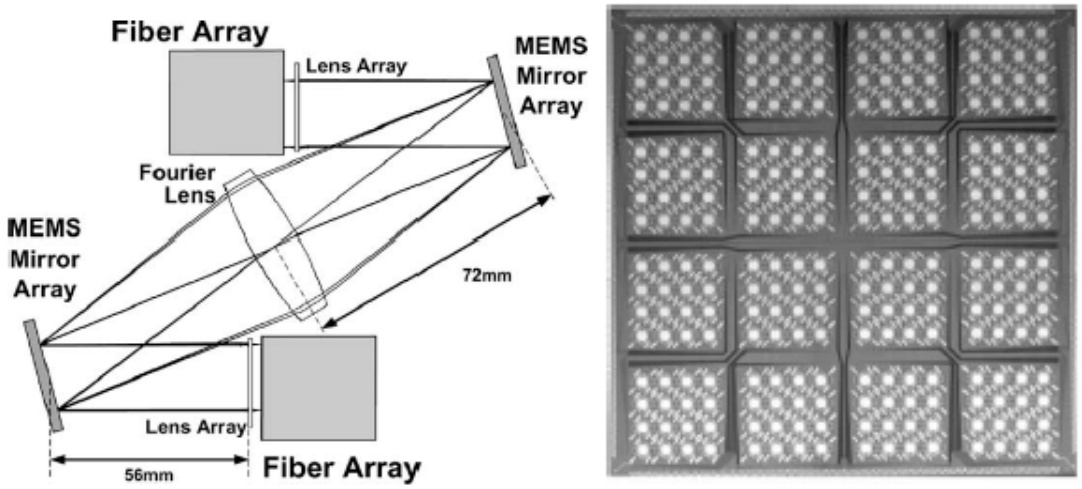


Figure 2.1 Schematic representation of and optical MEMS beam steering switch and a top down image [67].

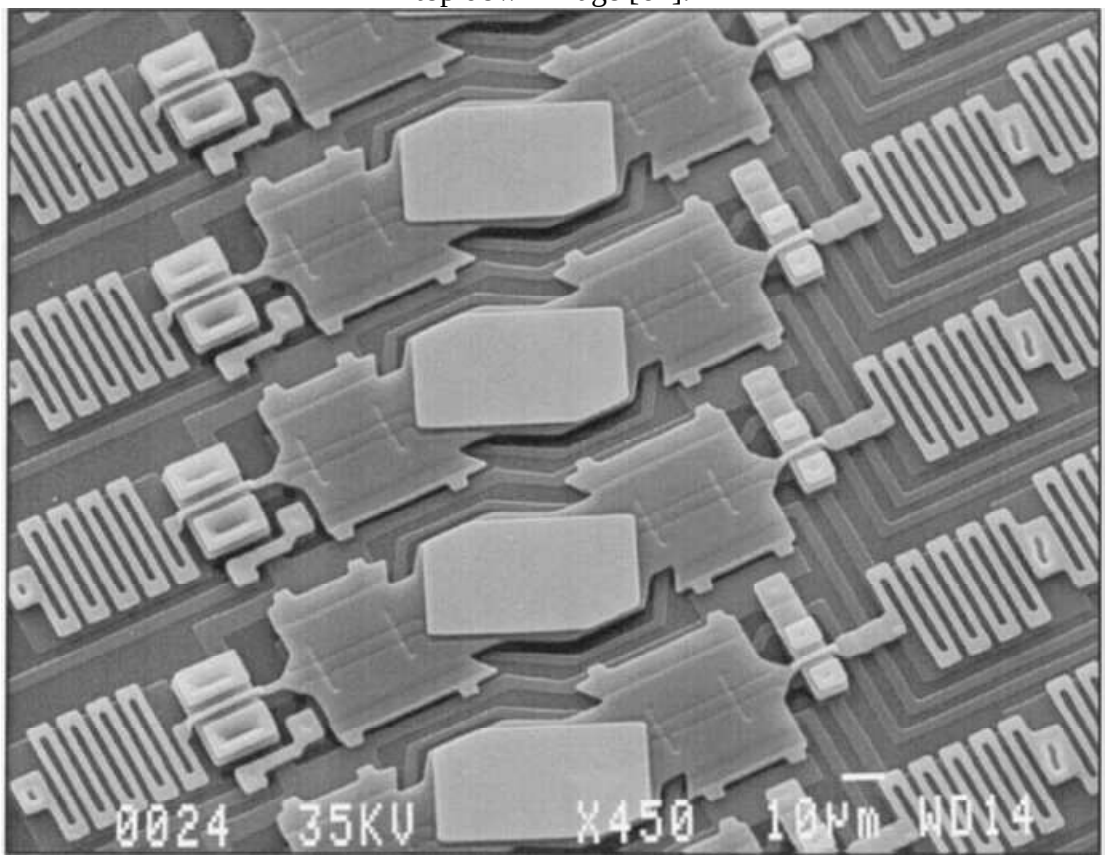


Figure 2.2. SEM image of tilt mirrors for and optical MEMS add/drop switch [66].

Other examples of multi axis tilt mirrors exist [68], however the importance of this specific device is that it was designed in the context of a complete system for use

with industry standard single mode fibers, at 1.55 µm wavelengths. When propagating single-mode beams for such a distance (257 mm), care must be taken to reduce beam divergence and loss from the mirrors and internal components. A microlens array and other free space optics are essential to achieving the low insertion loss in this system in preventing this excessive divergence in the propagating beams. Beyond costs associated with commercializing such a system, the major drawback to this configuration is slow switching speed and crosstalk and loss that can be experienced during beam switching. Notable examples of commercial free-space optical MEMS are the LambdaRouter™ [52], and the Texas Instruments Digital Mirror Device™ (DMD™) [40]. The LambdaRouter™ is a predecessor to the devices shown in [67] and in the same way uses arrays of analog, tilt-able, two axis micromirrors to perform non-blocking transmission through free space onto another array of positionable mirrors which then direct the beams to the output port. More recent versions of these multi-axis deflectable mirrors exist such as those reported by Kim *et al* [68].

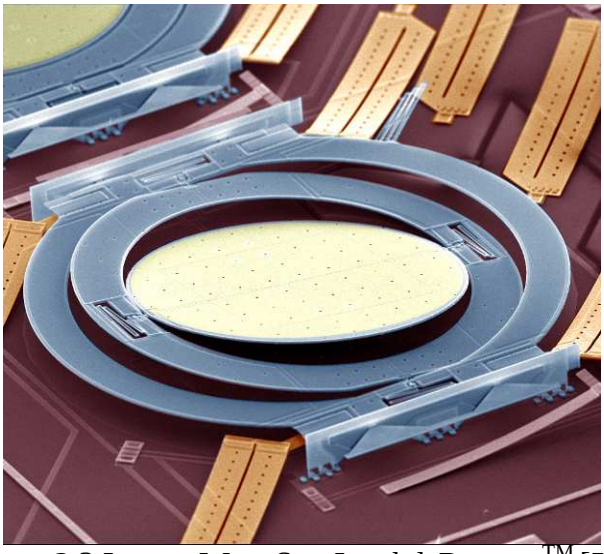


Figure 2.3 Lucent WaveStar LambdaRounter™ [52].

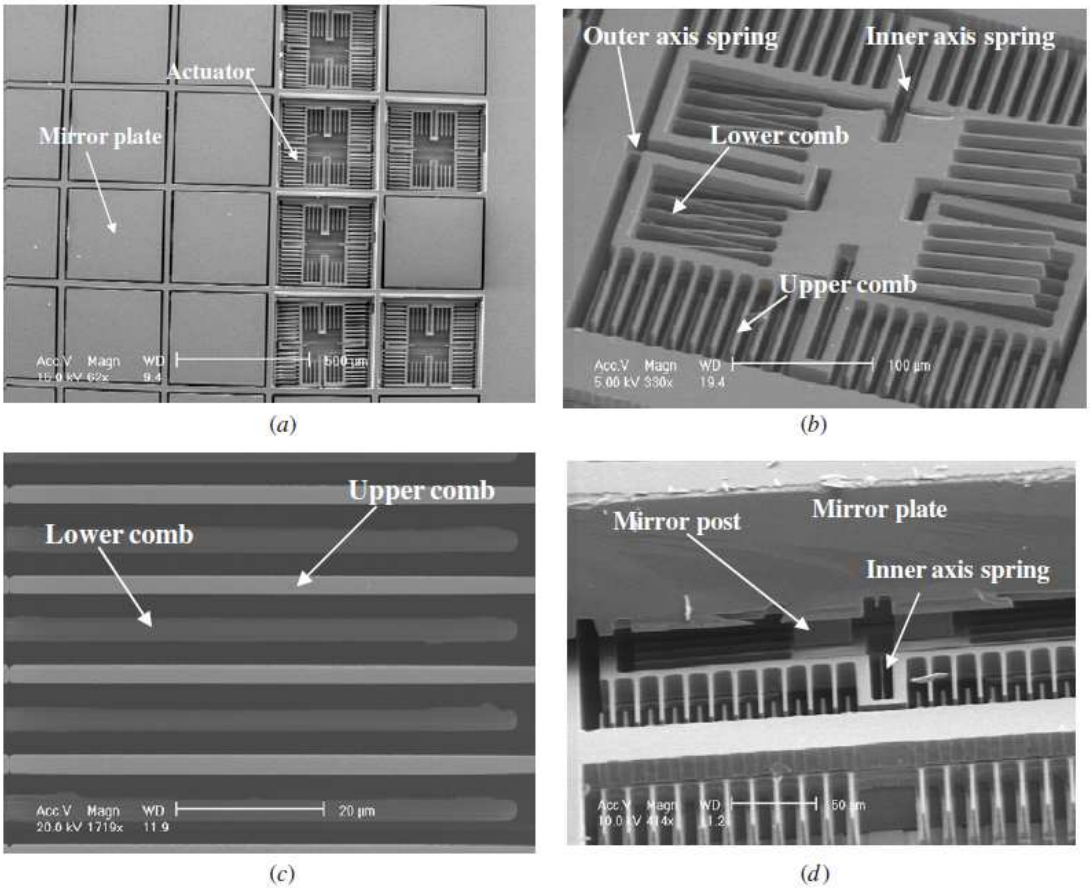


Figure 2.4. SEM images of multi axis high form factor micromirrors [68].

The Texas Instruments DMD^{TM} spatial light modulator (SLM) (Figure 2.5), possibly one of the most ubiquitous and successful examples of optical MEMS devices, is a projection device which uses an array of binary tilting micromirrors to reflect pixels to a screen or surface. These mirrors tilt in a way to generate an on/off pixel to a final projected image. In conjunction with a color wheel and via fast switching, colorized and moving images are projected onto a screen after reflecting from this dynamic pixel array through focusing optics. This technology has been used for everything from consumer electronics displays [69] to complex 3D maskless lithography tools [70] and benefits from its very simple operational principle.

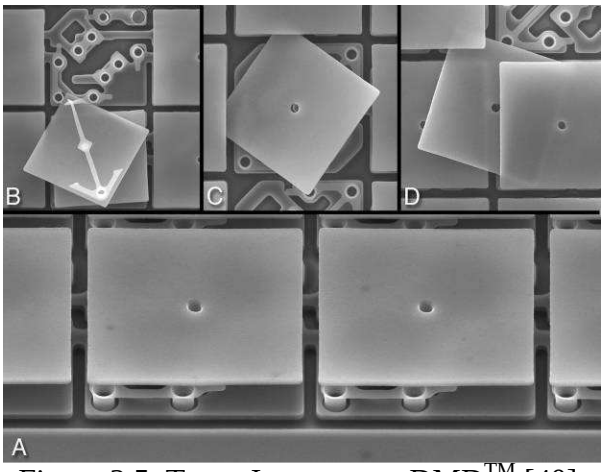


Figure 2.5 Texas Instruments DMD™ [40].

Scanning micromirrors are used to scan laser beams over surfaces for either display [71-73] or imaging technologies [44]. These devices typically utilize resonant structures in order to achieve high raster speeds and large mirror displacements. Biomedical applications are often targeted with these single scanning mirrors due to their small size and low power consumption, making them ideal for endoscopic and in-vivo imaging applications [74].

Although these devices have a number of applications and have seen commercial success, the eventual integration of these devices with external components can be difficult due to their out-of-plane operation. Intricate and custom packages are needed to fully implement real-world examples of these devices, particularly those intended for communications applications. This increase in packaging complexity increases future cost, decreases multi-device integration, and ultimately limits deployment possibilities.

2.1.2 Guided optical MEMS

Due to their out-of-plane operation, free-space optical MEMS do not lend themselves toward the integration of multiple components onto a single substrate

without extraneous post-processing (something which has proven to be a critical driver for the success of the IC industry). Utilizing a guided-optics architecture provides more control over light routing on chip, and opens up a number of additional technological applications such as refractive index sensing, and nonlinear optics. Free-space optical MEMS often experience less optical loss than the guided optical MEMS devices. This is due to the reduced surface roughness of planar surfaces compared to that of etched sidewalls or waveguides in most guided optical MEMS, which cause scattering losses. High throughput via multiple optical channels can be limited with guided optics due to the limited options for reconfiguring optical pathways and the wavelength dependent optical dispersion. When considering these technologies from a systems integration perspective however, these drawbacks are offset by the fact that in-plane guided optics are easier to combine with other optical elements, and allow for more control over the routing of light signals since their paths are lithographically defined, rather than straight-line propagation. This approach therefore leads to the potential for high levels of integration [75] due to this in-plane optical propagation which is easier to package with other components.

For communications applications, a large majority of waveguide optical MEMS are optical switch implementations. The basic switch architectures consists of an actuated moving waveguide or fiber cantilever which couples light from an input port into several output ports via the waveguide movement. Coupling between waveguides is usually achieved via butt coupled cantilever-like devices [26, 76-81] or evanescently coupled parallel waveguides and other resonant structures [82-87].

There have been a number of high throughput switches constructed and proposed using guided optical MEMS switches, but due to insertion losses, most require complex solutions like index matching fluids to allow for off and on-chip coupling. For example, Ollier *et al* [80] demonstrated seven 1×2 switches which have been cascaded into a 1×8 optical switch. The insertion loss of this device was measured to be 1.5 dB, and was achieved only after using index matching fluid in the gap region over which the light was traveling in free space. Other examples of 1×*n* optical waveguide switches are present in the field of optical MEMS [38, 57, 81, 88-90]; relevant examples of two of these devices are shown in Figure 2.6 and Figure 2.7. These two examples are particularly important because they utilize III-V compound semiconductors in their construction, which will be discussed in the next section.

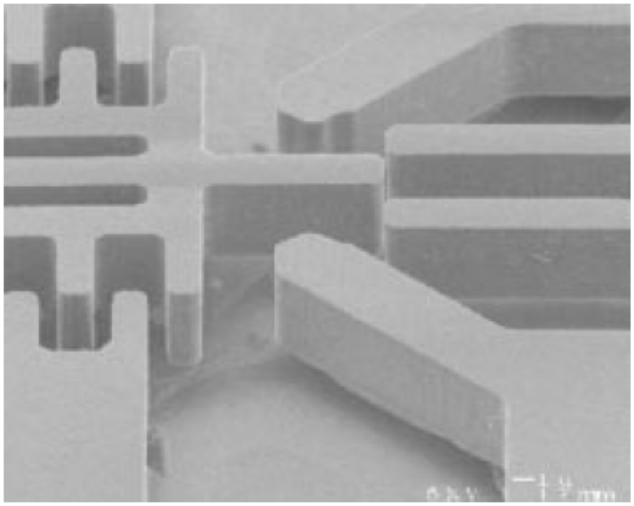


Figure 2.6 Example of waveguide switches in GaAs from [91]

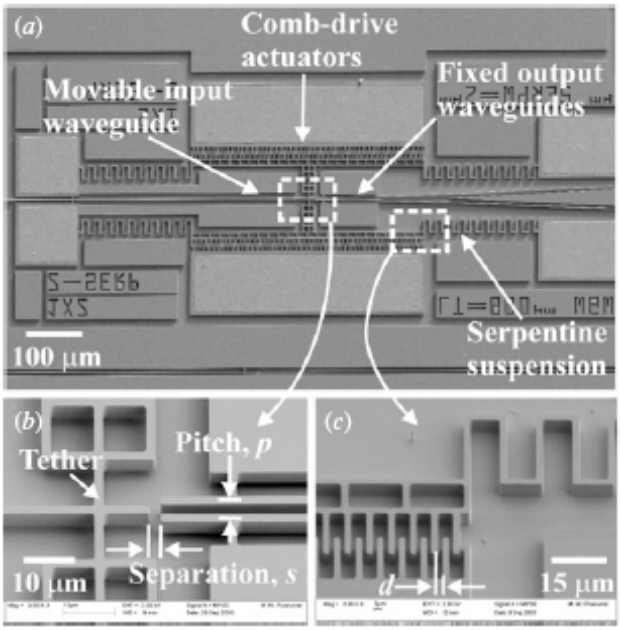


Figure 2.7 A waveguide switch fabricated in InP [26].

2.1.3 III-V optical MEMS

Integration of components is a common theme in the design and implementation of optical MEMS, as it was in standard MEMS technologies, and serves as the driving force behind much of the research development. The integration of optical components is often not as straightforward as the integration of electronic counterparts. Optical components often require a variety of different materials, interconnects, and strict alignment tolerances which increases the complexity of this task. Monolithic integration, which has been demonstrated repeatedly in MEMS [92-95], is even more difficult to achieve. Optical MEMS devices fabricated from III-V direct-bandgap semiconductors have the distinct advantage to allow for both passive and active optoelectronics within a single substrate. Many optical components rely on physically cleaved crystal planes to create optical quality reflectors and facets; promoting multi-chip integration solutions rather than a single chip. With improved fabrication methods and materials, systems can be constructed without the need for

cleaving and aligning multiple chips; creating new possibilities for monolithic fabrication of optical MEMS systems.

III-V materials for MEMS and optical MEMS have been pursued due to the control over specific material properties (stress, bandgap, lattice constant) when performing epitaxy of the compound semiconductors providing for the development of mechanical and active optical elements within the same substrate. Additionally, etch selectivity is easily achieved between different compositions of lattice matched materials allowing for the development of etch stops, sacrificial layers, and single crystal device layers. These properties are made possible through the growth of single-crystal substrates by way of molecular beam epitaxy (MBE) and metalorganic vapor phase epitaxy (MOVPE). Examples of materials that can be grown with varying bandgaps and lattice constants is illustrated in Figure 2.8. While there have been a many MEMS devices developed in these III-V material systems which take advantage of the piezoelectric properties [96-99], high electron mobility [100], or thermoelectric properties [101], the majority of examples take advantage of the configurable optical properties of these materials.

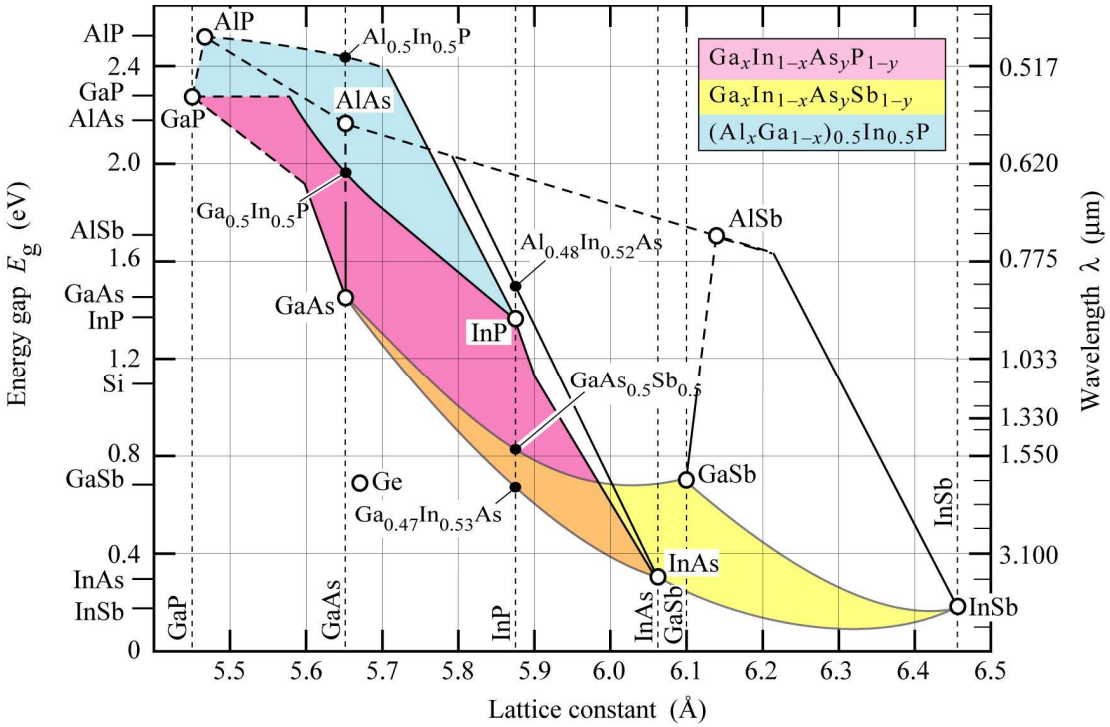


Figure 2.8 Diagram showing the relationship between material composition, lattice constant, and bandgap for some common III-V compound semiconductors [102].

A large number of III-V semiconductor compounds are direct-bandgap materials, making them suitable for the generation and detection of light. Furthermore these devices can be grown with variable bandgaps and compositions with the same lattice constant (see Figure 2.8), providing for optical, mechanical, and chemical tunability. Various devices can be created by growth of these materials.

The devices shown in Figure 2.6 and Figure 2.7 utilize the wet etch selectivity in order to fabricate suspended structures critical for optical MEMS devices by growing etch selective layers between a bottom substrate and top waveguide layer. Bakke *et al* and utilize GaAs/AlGaAs [79] while Pruessner *et al* and InP/InGaAs [26]. For each of these examples and others as well, the InP and GaAs layers are grown on the top of a single crystal sacrificial layer which is removed to facilitate suspended structures [103, 104]. Pruessner *et al* has created other devices such as evanescent

couplers using a similar material system [30]. High-quality, low loss, single crystal waveguides are created in this architecture by utilizing atomically smooth, lattice matched sacrificial layers.

Chemical etching selectivity, tight thickness control, and atomic-level surface roughness is exploited in the fabrication of optical filters and distributed Bragg reflectors (DBR). Tunable filters utilizing Fabry-Perot cavities have been widely implemented [103, 105-109]. Fabry-Perot filters are constructed in this architecture with distributed Bragg reflector (DBR) mirrors in the plane of the substrate in order to take advantage of the atomic smoothness and the tight control over layer thicknesses inherent in epitaxy. A sacrificial material can be grown between subsequent single-crystal semiconductor slabs, which allow for the creation of air cavities to facilitate DBRs and Fabry-Perot cavities. Irmer *et al* [106] demonstrates an example of one of these devices (Figure 2.9), and illustrates the wide tunability of these moveable mirror devices (142 nm).

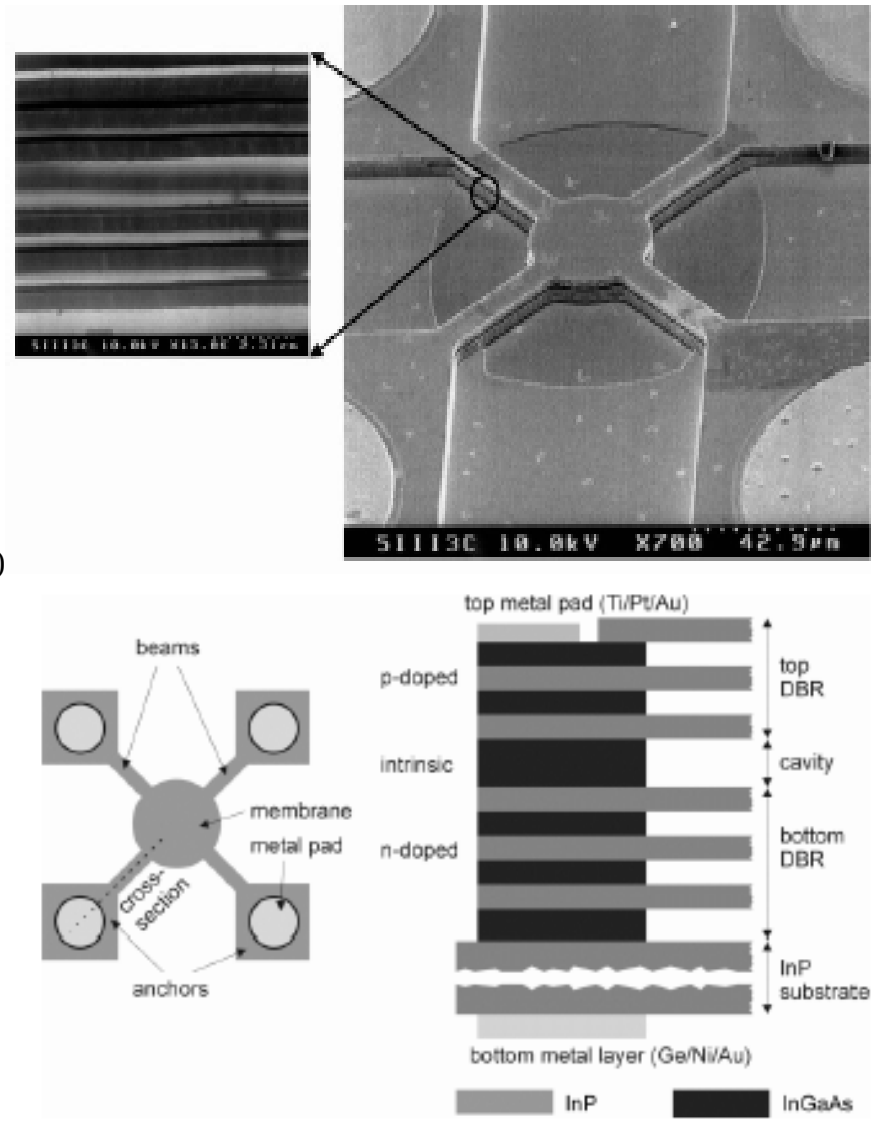


Figure 2.9 Out of plane electrostatically tuned Fabry-Perot filter in InP [106] with a) SEM showing a device, and b) Schematic design.

2.1.4 III-V integrated photodetectors

III-V semiconductors are traditionally used for opto-electronics applications due to their direct bandgap and high electron mobilities. Particularly, highly sensitive photodiodes are one of the many conventional applications of these materials. They are ideally suited for these devices because of the control over the material's direct bandgap, allowing for heterostructures with differing bandgaps to be grown in tandem, enhancing device applications.

Planar silicon photodetectors located at the surface of a substrate suffer from limited absorption volumes and only capture a fraction of the incident photon flux, as the depletion region created in this type of geometry is small. Buried diode configurations, which have larger depletion regions beneath the surface of the semiconductor, experience reduced incident flux due to the slight absorption in the top semiconductor layers before reaching the depletion region where recombination occurs. III-V semiconductors along with epitaxial growth allow for semiconductor regions with varying bandgaps and indices of refraction. This sort of control over the semiconductor properties allows one to make the top semiconductor layers of a planar photodiode to be transparent to the incident radiation, while maintaining absorption properties in some of the underlying material. Heterostructure surface illuminated PIN diodes are made in this configuration.

A major bandwidth limiting factor in normal incidence illuminated PIN photodiodes (see Figure 2.10) is the transit time of the photogenerated carriers through the intrinsically doped photon absorption region and to the *P* and *N* doped sides of the diode. Reducing the thickness of the absorption layer will clearly

decrease the time of transit from the *p* to the *n* type regions, but simultaneously reduces the absorption crossection encountered by incoming radiation, reducing the responsivity of the photodiode. This raises a clear disadvantage to obtaining high bandwidth and high quantum efficiency simultaneously [110, 111].

"Side illuminated" waveguide PIN photodiodes (see Figure 2.10) were introduced to combat this undesirable tradeoff between bandwidth and quantum efficiency [112]. By using a waveguide with an underlying absorption region as a portion of the cladding, the transit time across the absorbing region is controlled only by the thickness of the absorbing region, and the absorption length of the photodiode is directly controlled by the length of the photodiode. This provides a way to increase bandwidth and quantum efficiency nearly independent from each other. A number of diodes have been demonstrated with bandwidths in excess of 100 GHz by using this photodetector configuration [110, 111, 113, 114] and even higher bandwidths by using a traveling wave electrode configuration which exploit a distributed electrode configuration that supports traveling electrical waves impedance matched to the external measurement circuit [115, 116]. For the application intended, a side illuminated waveguide photodiode configuration is an ideal choice for in-plane integrated optical devices for the ease of alignment and coupling with other on-chip optical elements. Additionally, the frequency response of the device will not be a limitation as the operational frequencies are not expected to exceed 1GHz.

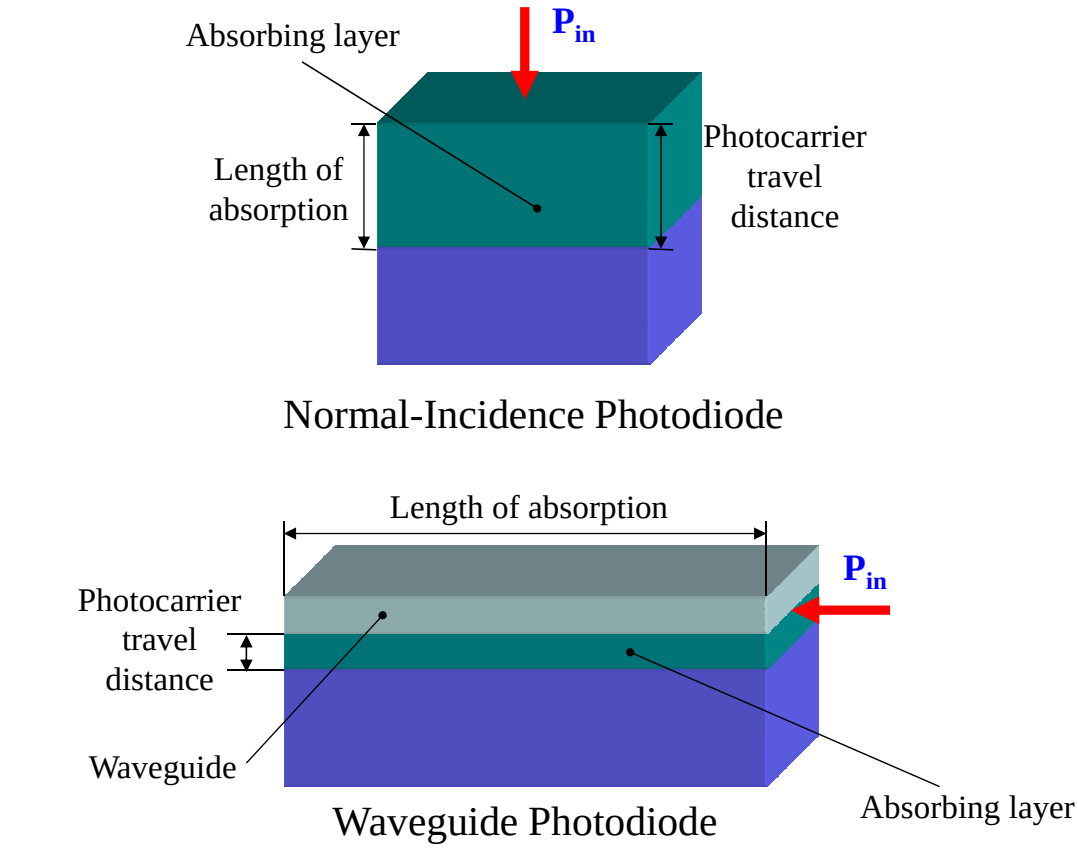


Figure 2.10 Illustration of differences between a standard surface illuminated photodiode and a side-illuminated PIN waveguide integrated photodiode.

2.1.5 III-V systems integration

The driving force behind the use of III-V semiconductor materials is the ability to create light generating materials in conjunction with absorbing and passive materials, all within a single substrate [117]. This integration has been particularly fueled by the communications industry which looks to improvements by reducing the number of separate components in an optical communications device, and ultimately, transitioning toward all-optical systems.

A critical component in the development of integrated systems such as the devices described in this proposal is the integration of optical gain regions (lasers) with waveguiding structures. A large body of work is present with a number of approaches to accomplish this task. There are a number of methods used to integrate active and passive electronics, the most common methods are simple vertically offset structures, regrowth structures, and quantum well intermixing (QWI) [118].

Vertically offset structures are devices built upon simple layer-by-layer construction, where quantum wells or other active regions are grown on top of passive waveguiding regions. The active portion of the layer structure is masked with a hard mask layer and then is selectively removed from the top of the intended passive regions through etching. This allows for the simultaneous creation of gain regions as well as passive regions in a single substrate growth. With this method one can integrate components in a simple way, requiring the least infrastructure and processing tools [118, 119]. These devices often suffer from the reduced optical mode overlap between the quantum well regions and the waveguide regions since they are physically separated from each other [120]. One can utilize a tapered

waveguide geometry to create passive active resonant coupling (PARC) structures that significantly increase the coupling between vertically integrated waveguides and layers as demonstrated by Vusirikala [121] and Dagenais *et al.* [122] as well as others [123, 124]. Another method used to achieve improved mode overlap and performance is the regrowth of waveguide regions [117, 125-127]. This is performed after the removal of the QW's and additional etching steps. This method will increase the modal overlap between the waveguide and the QW regions, but induce some unwanted reflections from finite index differences between growths [120]. More importantly, regrowth requires very precise control of growth parameters and the cleanliness of surfaces to have low-defect epitaxial layers grown on the processed samples.

QWI is another method used to fabricate both active and passive devices within a single growth. This method works by introducing impurities in the bulk of the QW epitaxial growth in selective areas, and then annealing the wafer to cause the QW's in the impurity laced areas to diffuse, changing the bandgap of these regions and causing them to be transparent at the active wavelength [118, 120, 128]. This creates regions of varying bandgap without the explicit need for re-growth or removal of material, allowing for the QW's to be directly in the center of the passive and active waveguide sections, maximizing modal gain. While this technique is very effective at creating complex designs with reduced optical coupling mismatch [120], it often will require the use of Ion implantation/x-ray irradiation and masking [128, 129] to perform. Depending on the method used, some additional layers must be grown on the top of the waveguide and QW regions to protect them from ion damage

during implantation. This layer will typically need to be removed, and thus there is still an additional etching step needed to finalize the devices.

For this system, maximum optical gain, single mode operation and efficiency are not the primary goals in the design of the laser source. Therefore, the vertically offset QW design is implemented. The ease of fabrication, no need for regrowth, the least amount of specialized equipment required (ion implantation beam lines), and the ability to increase optical coupling by incorporating PARC structures into the waveguide/laser/photodiode design make this technique the most attractive for the proposed devices with respect to the complexity required for a more simplistic non-communications application.

Sensors

This section reviews related work to establish the background knowledge related to these sensor devices. Examples of traditional sensors, MEMS sensors, cantilever microbalance sensors, and optical readout methods will be discussed.

2.1.6 Non-MEMS chemical sensors

There are a number of existing chemical sensors without micromechanical structures, using capacitive [130], resistive [131], bulk resonance [132], and optical methods [133] to transduce a chemical response into a useable signal [134]. The performance of these sensors is often limited by large required device sizes, power consumption, and supporting measurement equipment which can hamper mass production, large-scale integration, and portability.

Capacitive and resistive chemical sensors have been developed extensively in the past to detect chemicals in both gaseous and liquid forms [3, 4, 130, 134-138]. These types of sensors are generally comprised of a device which changes its capacitance or resistance due to a chemical reaction or environmental change. Demonstrations of ppb (parts per billion) sensitivities are common with these sensors [134, 139]. The sensitivity achieved with these sensors varies greatly based upon the materials and interrogation methods. Fabrication can be as simple as depositing an absorptive polymer on a set of microfabricated electrodes, however in many cases this is not compatible with standard microfabrication techniques. Furthermore, to provide for large changes in resistance or capacitance, devices are required to be large. Arraying a large number of sensors becomes more difficult with these two factors, particularly when looking at mass production. The sensitivity to humidity can also be troublesome in real-world deployment.

Surface acoustic wave (SAW) resonator sensors [132, 140] measure the resonant frequency changes of a surface/bulk resonator due to surface absorption of the target chemical analytes. Most SAWs are very sensitive due to high resonator quality factors and can be easier to fabricate since they use established fabrication techniques, however the absorption layers used are typically polymers which cannot be easily integrated into semiconductor fabrication techniques. The primary drawback of using SAWs lies in the difficulty of integrating them into multi-functional system. Single-chip arrays are difficult to realize due to the necessary size restraints of a SAW device, and the potential crosstalk between nearby adjacent SAW

resonators on the same substrate. This can cause problems when attempting to perform multiple chemical recognition studies on a single-chip sensor.

Optical sensors function differently in that they measure index of refraction changes, and in some cases molecular fluorescence, that occur due to chemical or gas exposure. Examples of discrete microfabricated waveguide devices, or even more simply, modified optical fibers are common representations of optics-based chemical sensors . These devices can be very sensitive to a target analyte but are also very sensitive to index of refraction and temperature changes in the surrounding environment. A significant drawback to a majority of these devices is the need for additional sample preparation or labeling in order to use the sensors. Many of the commercial and academic examples of these sensors require large external equipment such as lasers, spectrum analyzers, and photodetectors [143-147] which can be a hindrance to sensor deployment.

2.1.7 Micromechanical resonator sensors

In contrast to traditional designs, MEMS utilizing mechanical microstructures such as micromachined cantilevers provide promising sensor solutions which are small, scalable, low power, and due to these factors, ultimately portable. The ability to mass produce and to control and tailor device mechanical properties of such sensors provides an advantage over some of the aforementioned non-mechanical approaches.

First demonstrations by Nathanson and Howe [148, 149] using resonant microbridges for filtering and vapor sensing showed some initial demonstrations of

these MEMS sensors. MEMS resonant beam and cantilever sensing has since become a well-established method to detect various analytes in an environment. Many of these devices have the advantage of performing detection via label-free methods [133, 150] which can make sample detection and monitoring more streamlined. Being built upon the backbone of IC fabrication technologies, they are easier to fabricate in arrays in order to facilitate multiple sensing operations simultaneously. Examples of MEMS resonant sensors have reported detection of the attachment of single cells [151], DNA, viruses [152], and even attogram-level masses [153].

The most common examples of high sensitivity MEMS resonator sensors have been demonstrated while in a vacuum environment, rather than ambient, which can be a disadvantage when compared to other sensing methodologies. Operation of these resonators in ambient environments or liquids presents increased viscous dampening which reduces resonator quality factor making it more difficult to measure resonant frequency changes. While dampening due to ambient air can reduce the sensitivity of the resonator, there have been a large number of examples of micromechanical resonators achieving sufficient sensitivities for their intended applications [154-157]. An external feedback loop can be used in this case however to increase measurement resolution and artificially "increase" the quality factor of the resonator.

2.1.8 Cantilever readout

Traditionally, the most sensitive cantilever resonator sensors mentioned above have been measured using external optical methods [133, 152, 158, 159]. High displacement resolution allows for lower voltage resonant operation in

electrostatically actuated systems and even the possibility of ambient thermal excitation of resonant cantilevers if the quality factors are high enough. The most common measurement technique is similar to that employed in atomic force microscopy (AFM) where a laser is reflected off the cantilever surface onto a segmented position sensitive detector (PSD) [157]. Oscillations of the cantilever can be measured through the reflected beam angle changing, illuminating different parts of the segmented photodetector. Other optical methods, such as interferometry [160], are used to achieve ultra-sensitive displacement resolution; however, like traditional AFM techniques, they generally require costly and large equipment and infrastructure. Other more compact methods, such as piezoelectric [161], piezoresistive [162], and capacitive [155] readout are also used to measure cantilever response; however, they do not offer the same levels of high displacement sensitivity and relative electrical noise immunity that optical methods can exhibit [133] despite their smaller form factor and required infrastructure.

A significant drawback in using optical readout methods such as the typical AFM technique lies in the large free-space optical components (lasers, alignment mirrors, etc.) required, which limit the deployment of these sensors to laboratory use rather than to more portable systems. Furthermore, alignment tolerance and accuracy for these methods can be very stringent, as focusing a laser beam onto a microscale device is difficult. Due to these alignment challenges, cantilever device sizes are constrained to designs that are large enough to allow the beam to be focused onto the surface, potentially decreasing the sensor sensitivity and increasing device footprint. In these systems, obtaining high displacement resolution, component vibration

isolation, and photodetector and sample thermal stability become more critical due to the increased numbers of degrees of freedom introduced by components involved in the measurement setup [163].

One optics-based approach used to address these issues is a cantilever displacement readout scheme which relies on the variation of optical coupling between two waveguides, shown conceptually in the diagram Figure 2.11. An input waveguide directs light through a section of a waveguide that is separated and released from the substrate. This free end is allowed to then vibrate under excitation, ambient thermal or external actuation. As the cantilever waveguide oscillates, it misaligns with a fixed output waveguide, modulating the optical power coupled from the cantilever end of the waveguide into the fixed output waveguide. This output waveguide then guides the light to a photodiode to measure the change in optical coupling due to the cantilever's movement.

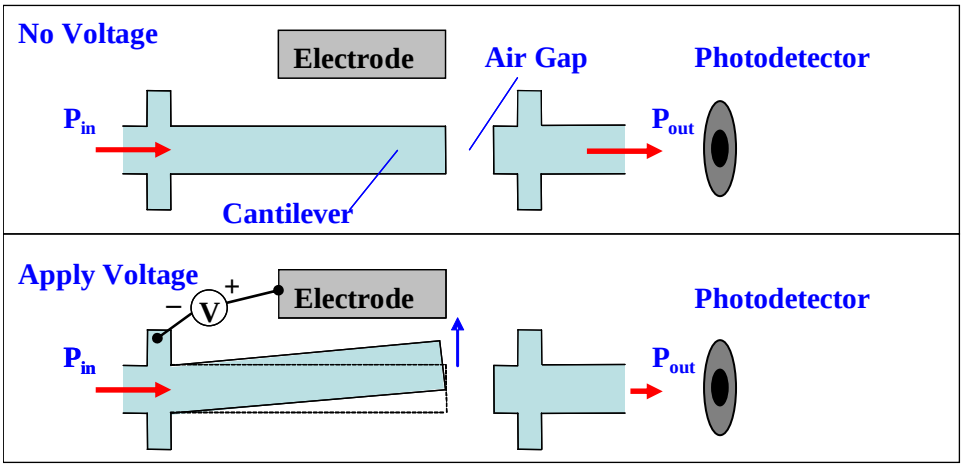


Figure 2.11 Cantilever waveguide principle of operation.

This measurement of optical coupling due to cantilever motion (misalignment) provides for a very sensitive displacement measurement, with reported resolutions comparable to traditional position sensitive detector (PSD) /

reflection readout systems (~20 fm / $\sqrt{Hz}$) [163]. The alignment tolerances of any external components, complexity of the readout system, and amount of external equipment required are reduced by using this method. This concept has been used with silicon dioxide SiO_2 cantilever waveguides for vibration measurements in high EM-interference background environments which electronic sensors were otherwise ill suited for [164] and as a replacement for traditional reflective AFM cantilevers in force and topography measurements [163]. The use of all in-plane optical components also increases the potential for single-chip integration of components since out of plane; off-chip coupling of light is not needed to perform the measurement of the cantilever.

This work will take this readout concept one step further toward a fully integrated sensor system. Through the use of III-V direct bandgap compound semiconductors, such as InP, the active optical components (light sources and detectors) needed for this readout scheme can be monolithically integrated into a single substrate. This system-on-a-chip methodology will take advantage of this readout method's simplicity and sensitivity and utilize the material flexibility that III-V semiconductors provide in order to combine all functions into one device and produce a more portable sensor system.

3 Theory & Design

This section covers the conceptual and theoretical design of the individual components and their integration into a complete sensor system.

System design overview

The complete system design has been introduced schematically in Figure 1.1; the figure is reproduced in this section as Figure 3.1 for convenience. A simplified version of the final layer structure is shown in Figure 3.2, detailing the crossection of the device schematic and the location of each device component in the layer stack.

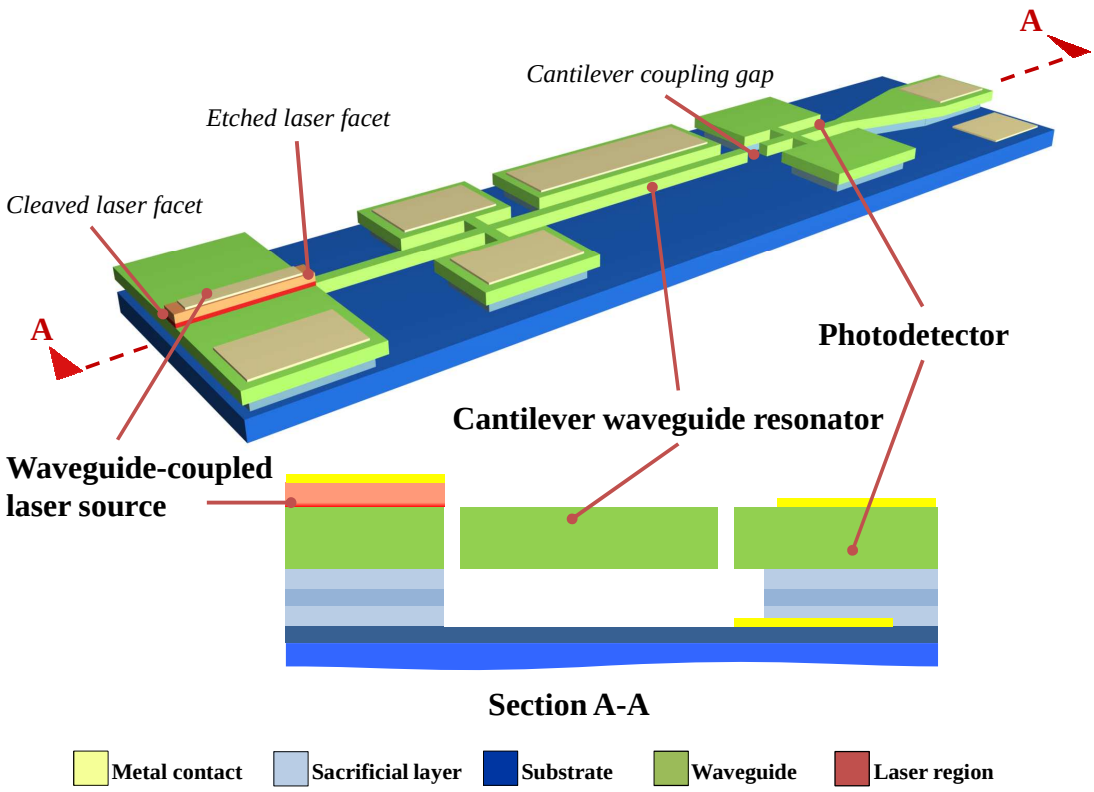


Figure 3.1. 3-D schematic of sensor system with included Cross-sectional representation.

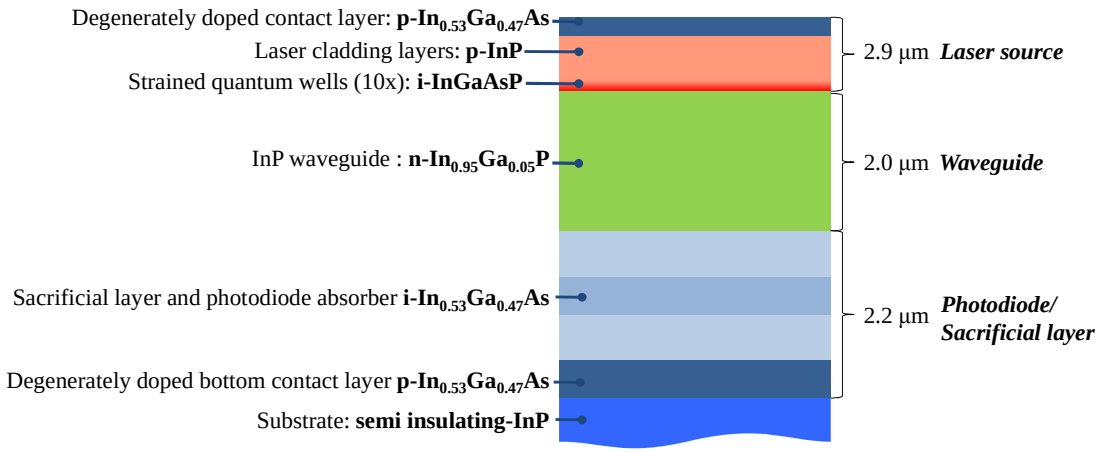


Figure 3.2. More detailed representation of layer structure cross-section.

The Indium phosphide (InP) material system is chosen here for this integration scheme as a matter of convenience to our group's previous work [26, 28, 30, 32, 165]. A large amount of test equipment and device fabrication recipes and procedures have also been acquired and developed for optical wavelengths of 1.55 µm, making this material system ideal for our purposes. This does not, however, restrict the extension of this design to using other III-V semiconductors. The design follows a vertically offset integration scheme in order to integrate the laser source, the waveguide, and the photodiode into one epitaxial growth. The three components in the above diagram will be summarized in this sub section, with more details in following sections:

Quantum well laser source

The quantum well laser source is designed to emit wavelengths in the range of 1.55 µm, below the bandgap energy of the InGaAsP quaternary alloy that is used for the passive waveguiding regions. The gain region of this laser diode consists of ten strained quantum wells that are clad by lower index confinement structures. An

operating wavelength of 1.55 µm is chosen out of convenience and in accordance with previously demonstrated laser designs that have been utilized for similar material compositions [122, 166]. The laser cavity is defined by a cleaved facet and an etched facet, with the etched facet coupling light to the suspended waveguides and photodiodes as indicated in Figure 3.1.

Cantilever waveguide resonator sensor

The cantilever waveguide resonator sensor is intended to function as a standard cantilever mass sensor [133, 159, 167, 168]. Measurement of the cantilever resonator will be performed with an optical waveguide readout principle introduced previously in section 2.1.8. This scheme utilizes suspended, moveable waveguides that become misaligned during the resonator movement. This misalignment causes a change in the optical coupling across a gap in the waveguide (see Figure 3.1) and is used as a means to directly measure cantilever displacement. This provides a method for measuring cantilever resonant behavior.

Waveguide integrated PIN photodiode

The output of the fixed waveguide will be measured by a waveguide PIN photodiode integrated directly below the passive waveguiding region (cantilever waveguide region). The optical absorption layer will be provided by a multi-layer InGaAsP - InGaAs sacrificial layer beneath the waveguide layer. $In_{0.53}Ga_{0.47}As$, the composition lattice matched to InP has a bandgap of 0.74 eV, making the band absorption edge lie at approximately 1675 nm and below. This makes $In_{0.53}Ga_{0.47}As$ an ideal material to absorb radiation at 1.55 µm. By growing the sacrificial layer as

undoped intrinsic material, *P* and *N* rich materials can be placed above and below in order to create a PIN waveguide photodiode [169].

Epitaxial layer structure growth

In order to facilitate all of these functions monolithically, they were implemented in a lattice matched epitaxial growth performed in-house at the LPS by Dr. Christopher Richardson and Laura Clinger. A table listing the entirety of the layer structure growth is presented in Table 3.1. Specification of each layer's function in this stack is also presented here, alongside the overall system purpose of sections of this layer growth (along the left side). Due to the relatively high thickness (7.1 μm) and strain variations throughout the layers, this final layer structure is a result of multiple growth iterations, the last being the only growth with high enough quality to be used for device fabrication. Throughout this section, ternary and quaternary layer compositions (InGaAs and InGaAsP) are all assumed to be grown with lattice matched compositions ($In_{0.53}Ga_{0.47}As$ and $In_{1-x}Ga_xAs_yP_{1-y}$ alloys) unless otherwise noted and will be referred to without mole fractions for brevity and convenience.

Table 3.1 Layer structure specification for entire growth, color coded for system-wide function (adapted from [166])

	Description	Composition	Thickness (Å)	Dopant	Doping Concentration	Repeat	Layer Number
Laser	Contact	p-Ga0.47In0.53As	2000	Be	p=1e19		36
	Cladding III	p-InP	6000	Be	p=2e18		35
	Cladding II	p-InP	4000	Be	p=9e17		34
	Cladding I	p-InP	2000	Be	p=3e17		33
	Etch stop	p-Ga0.175In0.825As0.38P0.62	1000	Be	p=3e17		32
	Dopant Transisiton	p-InP	1000	Be	p=3e17		31
	p-spacer	i-InP	500	-	undoped		30
	Upper SCH	i-Ga0.175In0.825As0.38P0.62	1500	-	undoped		29
	Barrier	i-Ga0.23In0.77As0.50P0.50	100	-	undoped	10x	28
	Quantum well	i-Ga0.23In0.77As0.75P0.25	100	-	undoped		9, 11, 13, 15, 17, 19, 21, 23, 25, 27
	Barrier	i-Ga0.23In0.77As0.50P0.50	100	-	undoped		
	Lower SCH	i-Ga0.175In0.825As0.38P0.62	1500	-	undoped		8
	Dopant Transition-contact	n-Inp	5000	Si	n=8e17		7
Waveguide	Waveguide	n-Ga0.05In0.95P	20000	Si	n=1e17		6
PIN Photodiode	Sacrificial cladding	i-Ga0.175In0.825As0.38P0.62	3750	-	undoped		5
	Sacrificial /aborbing layer	i-Ga0.47In0.53As	2500	-	undoped		4
	Sacrificial cladding	i-Ga0.175In0.825As0.38P0.62	3750	-	undoped		3
	Bottom contact	p-Ga0.47In0.53As	6000	Be	p=1e19		2
	Heavily doped Buffer	p-InP	7500	Be	p=1e19		1
	Substrate	Semi insulating InP	-	-	-		

3.1.1 Band structure

The band structure for these layers was calculated using a finite-difference solving iterative routine developed by Dr. Christopher Richardson at LPS. This routine uses iterative numerical methods to obtain the semiconductor band parameters starting from the raw material properties of the epitaxial layer structure. Specifically, multivariate interpolation is used to determine the initial material properties of arbitrary quaternary, ternary, and binary systems via empirical data available in literature [170]. The band structure and the effect of material strain on splitting of the valence bands is then determined via the k-p method. Quantum effects are accounted for in the quantum-well regions by solving Schrödinger's equation for the varying potential distributions in the finite barrier/well system. Finally, screening potentials are determined by relating electric potential to the localized charge distribution and

thus solving Poisson's equation. This allows one to calculate the equilibrium state of the conduction and valence bands of the epitaxial structure. This code is able to simulate arbitrary structures which may not have analytical solutions due to their complexity, and thus is a powerful tool in the development of a layer structure for many applications.

The plot shown below is the output from this program using the layer structure parameters listed in Table 3.1. In this plot, the primary direct conduction band is plotted, as well as the light and heavy-hole valence bands. All energies are presented in eV, with each being relative to the Fermi level (0). Visible in this plot is the expected light-heavy hole energy level splitting which occurs in the quantum well regions due to the material strain here, and is needed in order to reduce auger recombination and increase hole confinement. The PIN photodiode region also appears as expected, with a linear transition between the *P* and *N* type contact regions. The higher bandgap absorption layer cladding is clearly seen in this plot as well. Regions of contact (left and right extrema) show a Fermi level above the conduction band, which is expected for degenerately doped contact layers. For convenience the calculated band gap throughout the entire structure has been plotted separately. The complete band diagram is presented in Figure 3.3.

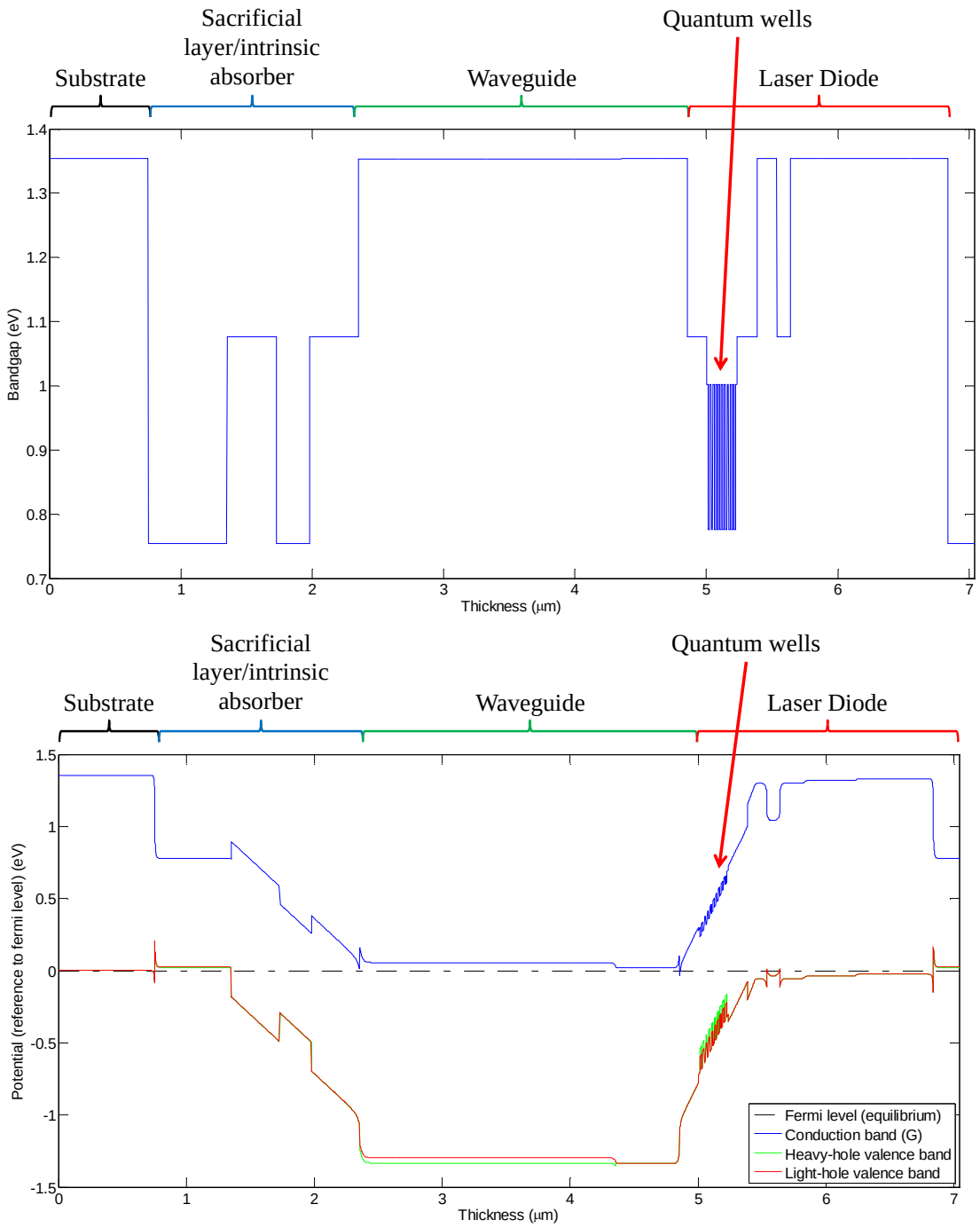


Figure 3.3. Top: Bandgap throughout structure. Bottom: Band diagrams of entire layer structure showing the Fermi level throughout the structure. Regions of interest are identified with labels.

3.1.2 Initial layer structure considerations

While it is true that a very large number of optical indices can be generated using the InGaAsP quaternary system, there is a limitation to the range of compositions that can be grown in a stable solid solution due to a phenomena known as spinodal decomposition [171]. Spinodal decomposition is characterized in InGaAsP by the formation of InP and GaAs rich regions instead of a homogeneous solid solution. This limits the largest index of refraction to be 3.206 for a composition of $In_{0.8314}Ga_{0.1866}As_{0.4059}P_{0.5941}$. With the effective index of the quantum wells being about 3.35; this creates a large discontinuity in the index profile with respect to the InP (n~3.1) waveguide core which increases confinement in the quantum wells. Initially a graded index waveguide scheme was pursued in order to better coupling into the underlying waveguide, however due to material growth difficulties, a simpler single-material composition within the limits of spinodal composition was implemented for this application.

Integrated laser source

The design of the Quantum well structure will follow the design laid out by Dagenais, Han, Saini, and Vusirikala *et al* [121, 122, 172-174] here at the University of Maryland and the Laboratory for Physical Sciences (LPS). Final refinements to the shown layer structure were performed by Richardson *et al* at LPS [166]. This well established design serves to provide an optical gain region that will be integrated onto the top of our waveguiding layer to create the laser cavity. The aim is to eliminate a number of the variables in the design, processing, and integration of this

laser with the additional structures (cantilever waveguides, PIN photodiodes, etc.) in the system.

This laser is a separate confined heterostructure (SCH) multiple quantum well (10 wells) (MQW) InP-InGaAsP laser diode. The relatively thick SCH layers are used to better confine the optical mode in the MQW active region where light amplification occurs and increase the modal gain. The quantum wells are designed with a bandgap of 0.765 eV, corresponding with a wavelength of 1.62 µm. The design is optimized to have maximum gain at approximately 1.55 µm in correspondence with the most commonly used communications wavelength. Literature also reports a comparable layer design which was used on the top of a passive waveguide layer, similar to the intended application [121-124], which reinforces the offset laser/waveguide/photodiode scheme utilized for these devices.

3.1.3 Laser diode design and layout

The indicated top section of the layer structure in Figure 3.2 contains contact, quantum well, and cladding layers for the ridge multiple quantum well laser. The design of the laser regions follows a standard buried contact electrically pumped ridge laser diode with a cleaved facet and an etched facet forming the laser cavity. The ridge depth is designed to be approximately 1.2 µm deep, but is not a critical dimension in the final device structure, and needs to only be less than the depth of the quantum wells. Quantum wells are removed from around the ridge region allowing for topside *n*-type contacts to be realized. A Si_3N_4 passivation coating of 7000-2000 Å is utilized to reduce surface current leakage as well as serve as electrical isolation for the ridge *p*-type contact (see Figure 3.4). Each laser has a fixed ridge width of 3

µm wide, intended to provide current and optical confinement, but still allow for lithography atop the ridge to realize the *p*-type contact; smaller than 3 µm becomes difficult to assure resolved patterns and good alignment. The 30 µm wide quantum well region is established to provide a via to expose the topside *n*-contact for the laser diode and minimize coupling of the guided laser mode with an etched sidewall. Having an etched surface in close proximity to the gain region can cause current leakage due to surface recombination, and any surface roughness from the etching process will cause optical scattering. This also removes the optical gain region from the remainder of die where there is no optical gain needed such as the waveguide and photodetector region. Mirror facets for the optical cavity are formed via a mechanical cleave and an etched facet (see Figure 3.4). The etching step for the facet also serves as a >7.1 µm deep electrically isolating trench that surrounds the laser structure (and photodiode/cantilever) and completely cuts through the epitaxially grown structure into the semi-insulating substrate. This etch not only establishes the facet, it creates the coupling gap between the laser and the suspended waveguides that are coupled to the cantilever resonator and photodiode. Three laser cavity lengths were designed and fabricated: 500, 1000, and 1500 µm.

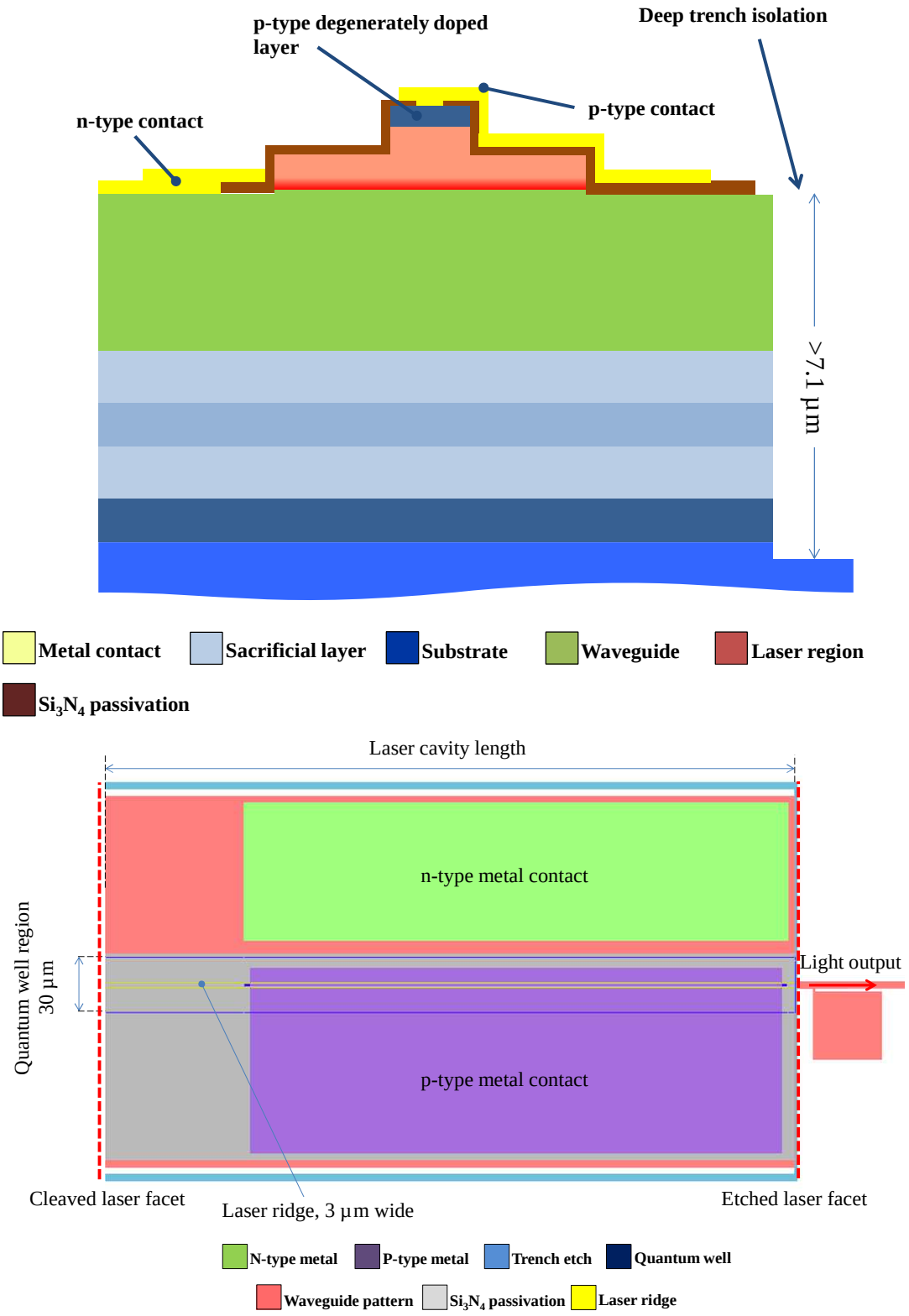


Figure 3.4 Laser crossection (top) and top-down mask layout (bottom) with fixed dimensions specified.

Waveguides

This section details all of the waveguiding components included in this integrated design, covering the theory and design of the suspended waveguide structures, and the cantilever waveguide resonators. A final design layout is presented showing device dimensions and important features of the structure.

3.1.4 Waveguide strain

Of note in this layer structure is the strained waveguiding layer. The waveguiding layer is chosen to be composed of semiconductor as close to InP as possible in order to be lattice matched and also transparent to the emission wavelength. These also serve as suspended mechanical structures and need to be designed with tensile strain introduced into it in order to prevent buckling of doubly-clamped waveguide sections [28]. A straightforward way to increase the tensile strain in the waveguiding layer is to change the material composition to reduce the lattice constant and create tensile strain in the layer. An equation relating the lattice constant (*a*) and the mole fractions, *x* and *y*, in $In_{1-x}Ga_xAs_yP_{1-y}$ is expressed as [175]:

$$a \approx 5.8688 - 0.4176 \cdot x + 0.1896 \cdot y + 0.0125 \cdot xy \quad (3\text{-}1)$$

Additionally, the lattice mismatch *f*, of a grown epitaxial layer upon the underlying substrate is defined as [176]:

$$f = \frac{a_s - a_f}{a_f} \quad (3\text{-}2)$$

Where a_s is the substrate lattice constant and a_f is the lattice constant of the grown film. With very small lattice mismatch, ($|f| \square 1\%$), the growth in question can

be assumed to be pseudomorphic and grow defect-free with this new lattice constant [176], exhibiting in-plan strain equal to the lattice mismatch.

It is clear from (3-1) that setting *y=0* and introducing a positive value of *x*, the lattice constant will shrink to a smaller value than intrinsic InP, establishing this layer as tensile strained compared to the InP-lattice matched material beneath. A very small amount of tensile strain is actually required for the suspended waveguide structures, and thus a very small perturbation of the Ga-concentration is needed. A minimal value of x, 0.05 is introduced, yielding ~ 0.36% in-plane tensile strain in this layer, sufficient for these structures. This step is critical in the realization of free standing waveguides as illustrated in Figure 3.5, showing the effect of both compressive and tensile strain on the final suspended structures.

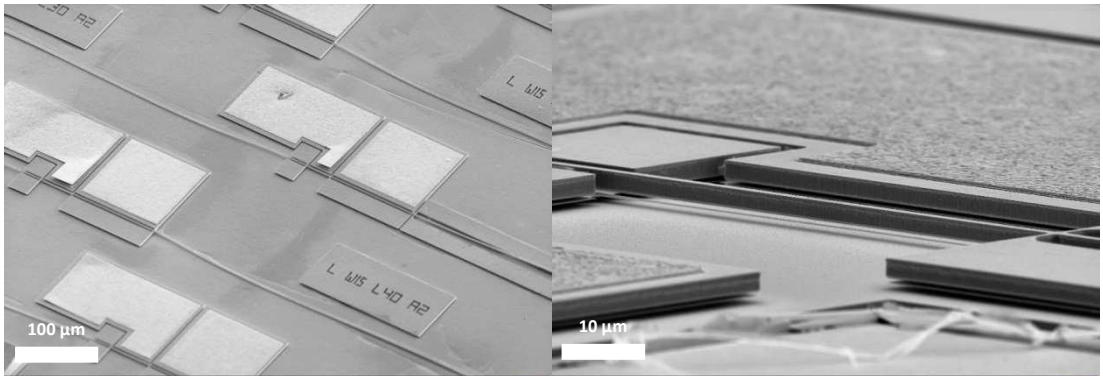


Figure 3.5. Left: Released waveguide structures appear buckled due to compressive stress. Right: tensile stress allows for fully suspended intact waveguide structures after release, as can be seen in this doubly clamped waveguide suspension.

3.1.5 Free carrier absorption

Doping concentrations and the optical properties of the layers within the structure must be considered in order to establish tradeoffs between free-carrier absorption and low device resistance in the contact layers.

The bottom contact layer for the laser structure (layer #6 as seen in Table 3.1) serves the purpose of a voltage contact for the laser structure, and therefore is usually doped highly so as to keep the resistance low in the total structure reducing joule heating. In our design, this structure will have a relatively large portion of the optical mode propagating through it as it is the upper portion of the underlying waveguide region. Free carrier absorption due to the high doping of this layer can be a problem, and needs to be considered in this case. A general equation which describes free carrier absorption in semiconductors is shown in equation (3-3) below (in MKS units) [177]:

$$\alpha = \frac{q^3 \lambda^{2.5} n}{4\pi^2 \varepsilon_o c^3 n m^{*2} \mu} \tag{3-3}$$

where λ = wavelength, n = density of free carriers, n = refractive index, m^* = effective mass, and μ = mobility. Additional experiments have also shown a linear dependence in the absorption coefficient (in cm^{-1}) on doping concentration (at 1.55 μm), yielding the empirical equation (3-4) [178]:

$$\alpha = 5 \times 10^{-20} \lambda^{2.5} \mathrm{n} \tag{3-4}$$

Each of these functions were plotted to establish an approximate range over which the free carrier absorption can be estimated for our intended doping level.

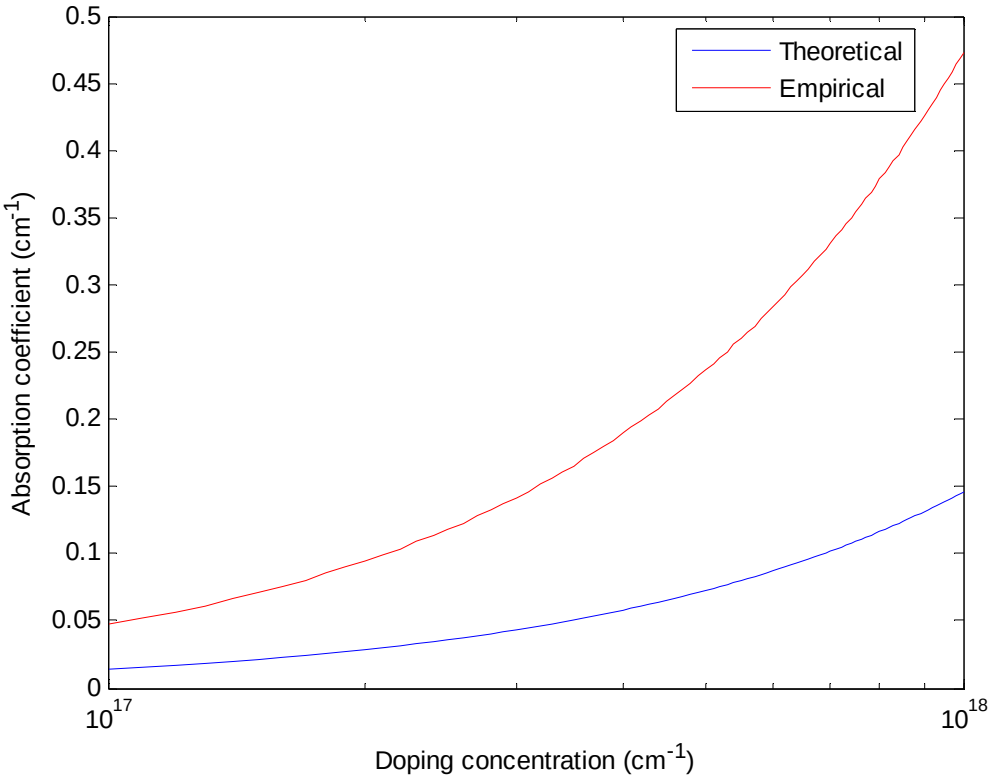


Figure 3.6. Absorption versus doping concentration comparing the empirical formula with theoretical calculations.

It is noted that in these calculations the entire waveguide is assumed to be homogeneous. The doping concentration is chosen according to both the sheet resistance and absorption values to effectively minimize each parameter's negative impact on the final device performance. Figure 3.6 shows that in the range of doping concentrations at 8×10^{17}, absorption losses are expected to be in the range of 0.1-0.3 $dB\cdot cm^{-1}$, and in this case, the InP sheet resistance for this layer will be approximately 70 mΩ/□. Since very little current is expected to pass through the capacitive actuation scheme of the cantilever waveguide structures and the contact area along the length of the laser diode ridge is large, this resistance has been perceived to be at an acceptable level. Choosing these values attempts to minimize the two factors, sheet resistance and free carrier absorption in such a way to provide relatively low loss and relatively

low resistance simultaneously. It is difficult to determine these values to absolute certainty via theoretical means as they depend on many other unknown factors such as film quality, exact doping density, system geometry, and the results of device processing.

3.1.6 Cantilever waveguides

3.1.6.1 Principle of operation

The cantilever sensor platform presented here operates based upon the optical misalignment principle discussed previously in section 2.1.8. In addition to this readout mechanism, these devices are designed in the InP III-V semiconductor material system to take advantage of the material flexibility and ultimate monolithic integration. The devices presented here aim to combine the advantages of integrated optical components with this highly sensitive readout mechanism. This section presents background on the specifics of the InP cantilever waveguide resonator which was studied for this dissertation. A schematic of the device and operation is shown in Figure 3.7.

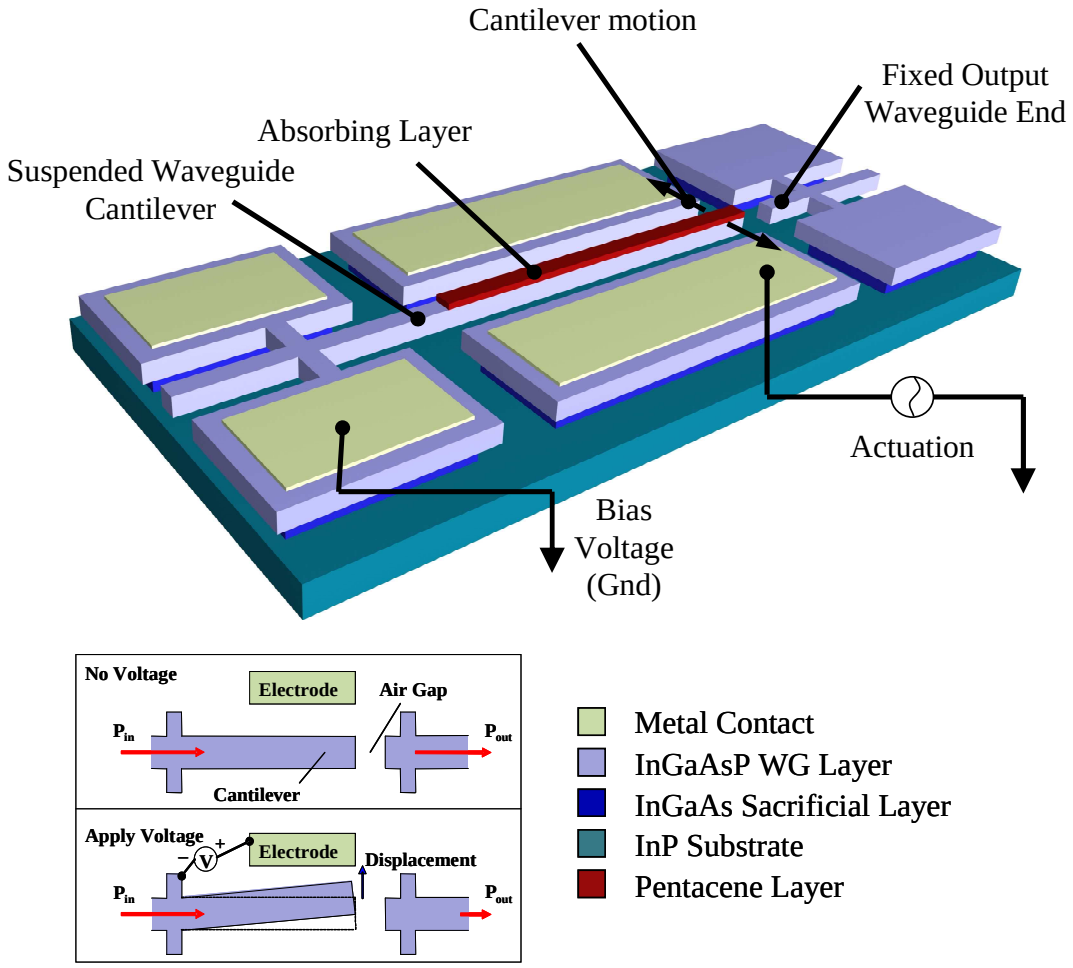


Figure 3.7 Schematic of device components. Inset: operational principle of the readout mechanism.

3.1.6.2 Electrostatic Actuation Modeling

The design of the cantilever waveguides concerned practical considerations of electrostatic actuation, such as the pull-in voltages of the cantilever and the maximum voltages to be applied the electrodes to actuate the device. This will fundamentally limit the stiffness of the cantilever to values that allow the cantilever to be actuated at this maximum voltage.

Static displacements due to this applied voltage were calculated assuming a uniform electrode and small displacements while assuming the parallel plate capacitor

model. Previous experiments using this material layer structure identified a maximum voltage of 26V which could be applied to the InP layer structure before breakdown occurred. This was used as an upper bound for actuation voltage.

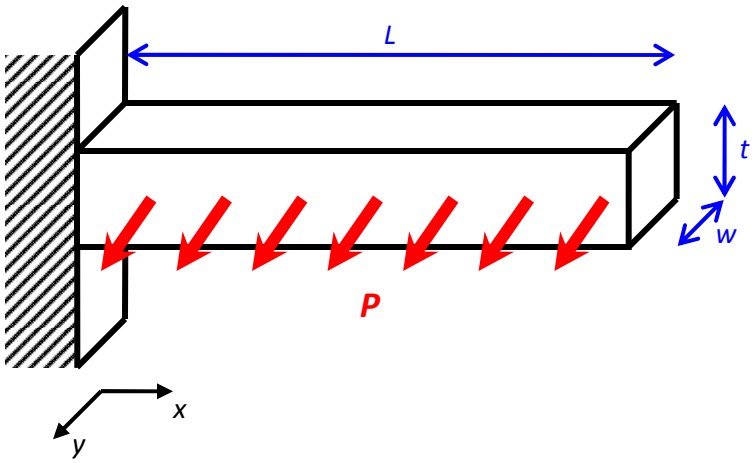


Figure 3.8 Diagram illustrating parameters relevant to the derivation using the Euler beam equation.

Solving the Euler beam equation (referring to Figure 3.8):

$$EI\frac{d^4d(x)}{dx^4} = P \tag{3-5}$$

where E is the Young's Modulus of the material, $d(x)$ is the displacement of the beam along the x direction, P is the electrostatic force acting in the y direction for small displacements (not a function of x or y), defined as:

$$P = \varepsilon_o \frac{V^2}{2g^2}t \tag{3-6}$$

where t is the cantilever thickness, V is the applied DC voltage between the electrode and cantilever, ε_o is the permittivity of free space, and g is the actuation gap of the cantilever. I is the moment of inertia of a cantilever defined as:

$$I = \frac{1}{12} t w^3 \tag{3-7}$$

with t as the cantilever thickness. Integrating equation (3-5), we obtain:

$$d(x) = \frac{P}{24EI} x^4 + C_1 x^3 + C_2 x^2 + C_3 x + C_4 \tag{3-8}$$

with C_1, C_2, C_3, C_4 all constants. Due to clamped end conditions $C_3 = C_4 = 0$, since $d(0) = d'(0) = 0$ for this case. The set of equations pertaining to the free end of the cantilever are similar $d''(L) = d'''(L) = 0$. Differentiating Equation (3-8) two and three times respectively and using $x = L$, gives the system of equations:

$$d''(L) = \frac{P}{2EI} L^2 + 6C_1 L + C_2 2 = 0 \tag{3-9}$$

$$d'''(L) = \frac{P}{EI} L + 6C_1 = 0 \tag{3-10}$$

which can be solved for both C_1 and C_2:

$$C_1 = -\frac{P}{6EI} L \tag{3-11}$$

$$C_2 = \frac{P}{4EI} L^2 \tag{3-12}$$

this result can then be used to express the displacement versus x of the cantilever:

$$d(x) = \frac{P}{2EI} \left(\frac{x^4}{12} - \frac{Lx^3}{3} + \frac{L^2 x^2}{2} \right) \tag{3-13}$$

The maximum displacement of the cantilever is the relevant design parameter, calculated by evaluating the value of $w(x)$ at $x = L$, which will give the maximum displacement of the beam:

$$d(L) = \frac{PL^4}{8EI} \tag{3-14}$$

Plugging in *P* and *I* as in equations (3-6) and (3-7), we come to the final result for maximum displacement:

$$d_{\max} = \frac{3\varepsilon_o V^2 L^4}{4g^2 w^3} \tag{3-15}$$

Using this expression (Equation (3-15)**)** to calculate maximum amplitudes for a variety of widths and lengths of the cantilevers produces curves such as Figure 3.9. After a displacement larger than the width of the cantilever, the above assumptions no longer hold, however these calculations were performed to estimate the smallest displacements of a cantilever with a given geometry which are well within these limits.

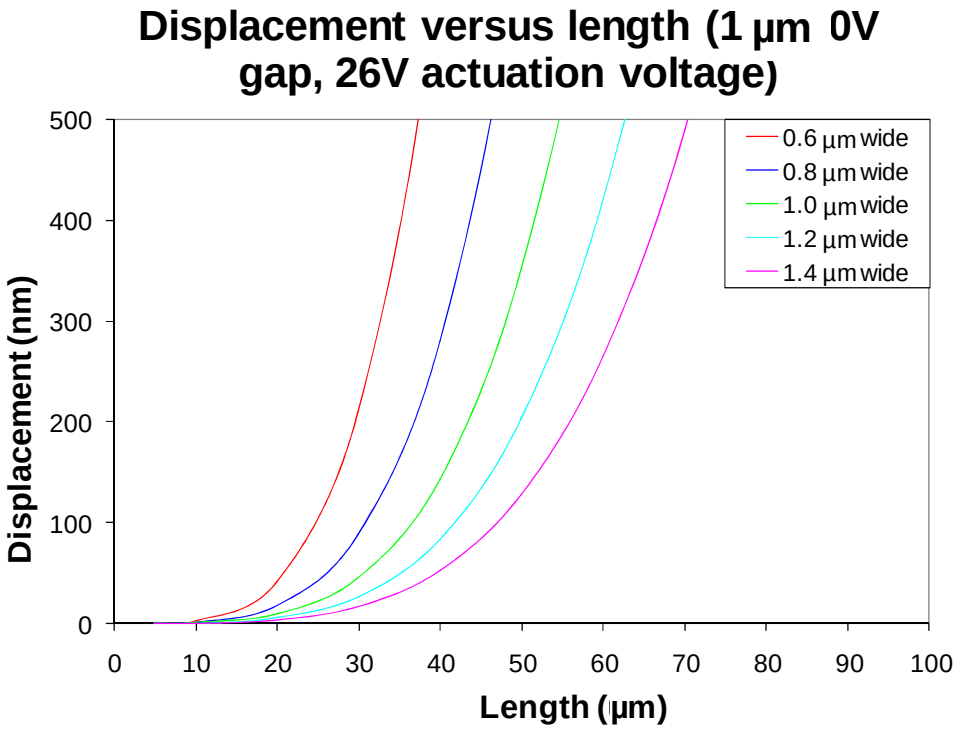


Figure 3.9 Plot of maximum displacement versus length of cantilever for a variety of cantilever widths, with a cantilever thickness of 2 µm.

In addition to the amplitude, pull-in voltages are calculated for the same lengths and widths of cantilevers. Pull-in is defined as the point at which the electrostatic force applied to the cantilever overcomes the spring restoring force. This causes instability, closing the gap between electrode and cantilever. Pull-in can cause permanent stiction, a destructive process with these devices.

The pull-in voltages are calculated using the model developed by [179] which accounts for cantilever bending, fringing field effects, and a number of other third order effects that change the cantilever pull-in voltage. This method is used to determine appropriate actuation gaps and feasible dimensions for the cantilevers. The simulation is performed for a range of widths, lengths, and actuation gaps. These calculations give an approximate maximum voltage before pull-in will occur. Figure

3.10 illustrates the pull in voltages versus the lengths of the cantilevers for an actuation gap of 1 µm and a number of cantilever widths.

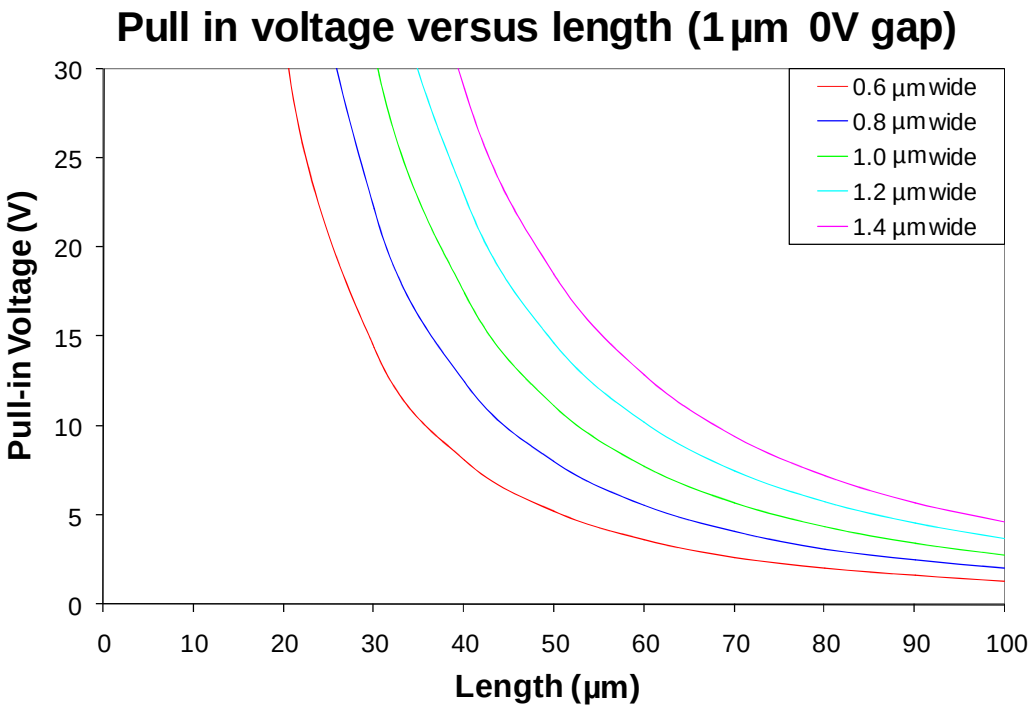


Figure 3.10 Pull in voltage versus length for two different actuation gap widths.

3.1.6.3 Coupled gap / free space propagation

Optical overlap integrals were calculated assuming free space Gaussian beam propagation in the axial (*z*) waveguide direction [180] in order to estimate the change in coupling due to cantilever waveguide displacement. A diagram in Figure 3.11 shows relevant parameters for this derivation.

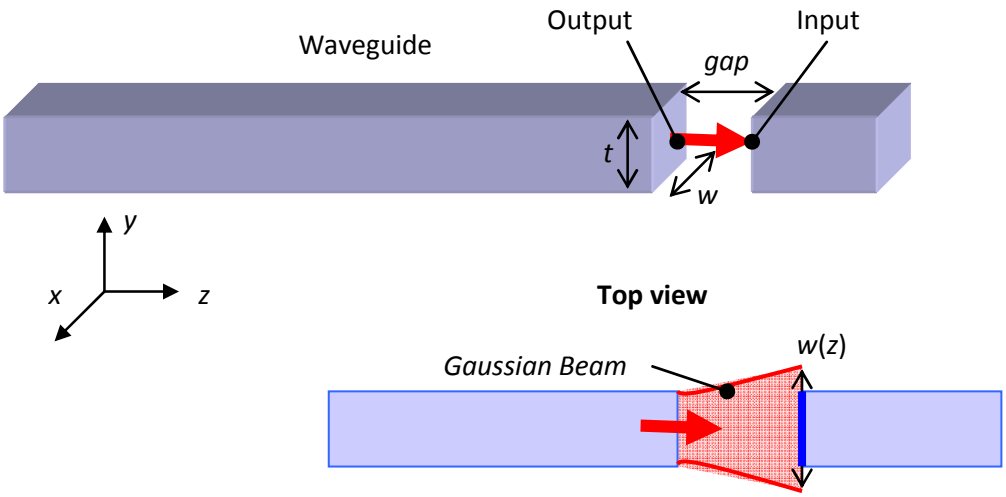


Figure 3.11 Diagram showing relevant dimensions and features for Gaussian beam propagation calculations.

The Gaussian beam equation of intensity as a function of *x* or *y* is shown in:

$$I(x,y,z) = \frac{2}{w(z)t(z)\pi} e^{\frac{-2y^2}{t(z)^2}} e^{\frac{-2x^2}{w(z)^2}} \tag{3-16}$$

with $w(z)$ and $t(z)$ the beam widths as a function of propagation distance:

$$w(z) = w\left[1+\left(\frac{\lambda z}{\pi w^2}\right)^2\right] \tag{3-17}$$

$$t(z) = t\left[1+\left(\frac{\lambda z}{\pi t^2}\right)^2\right] \tag{3-18}$$

with w and t the widths and thicknesses respectively. The mode overlap from the output facet to the input facet, T, is given by the following [180]:

$$T = \left|\iint I_{output}(x,y,gap) I_{input}(x,y,gap)\,dxdy\right|^2 \tag{3-19}$$

where z has been replaced with the gap length to simulate the propagation over this distance. From previous tests and projection lithography experience, the smallest consistently resolvable feature size with the available photolithography equipment has been found to be 0.6 µm, therefore all calculations use 0.6 µm gap lengths.

Considering a standard photodetector, an estimate of about 5% optical coupling change is the lower threshold for observing waveguide movement through the optical coupling loss. For the 0.6 µm wide cantilever scenario, this corresponds to approximately 200 nm of misalignment (see Figure 3.12).

Due to this limitation, devices below 20 µm long would not be measurable. Regardless of this 200 nm "limit," actuation at the resonant frequency can be as large as the quality factor (Q) times the DC static displacement, which for most devices the Q was estimated to be between 10-100, citing previous results [181], and thus the displacement calculated here may underestimate actual cantilever displacement.

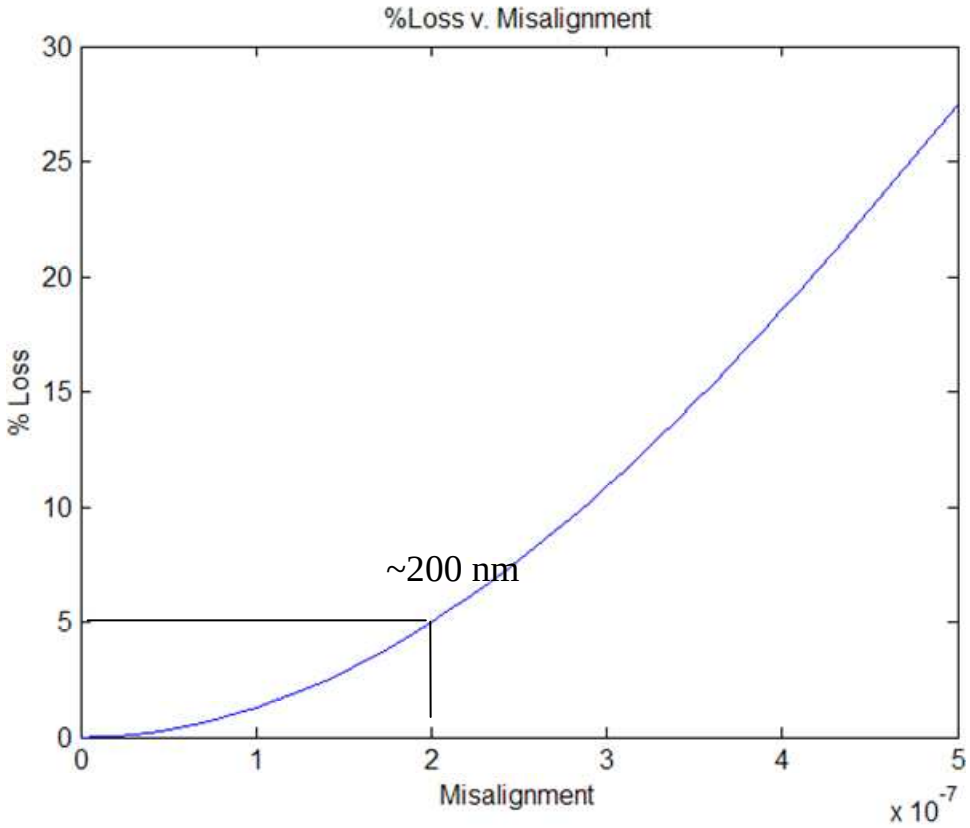


Figure 3.12 Percentage optical coupling loss versus cantilever misalignment (in meters). Superimposed is the 5% limitation, showing intersection at approximatley 200 nm.

3.1.7 Suspended waveguide design

The center of the epitaxial growth consists of a 2 µm $In_{0.95}Ga_{0.05}P$, moderately *n*-doped (1.0×10^{17} cm^{-1}) layer which is grown atop a sacrificial layer to be removed at the completion of device fabrication in order to prevent optical loss due to the underlying sacrificial region which absorbs at the operating wavelength as well as to facilitate a moveable MEMS cantilever structure. The introduction of a small mole fraction of Ga into the waveguide layers (see Figure 3.2) provides tensile strain in order to prevent the suspended structures from buckling after release (see section 3.1.4). The doping of the waveguide is performed in order to allow it to be electrostatically actuated via topside contacts. Suspended waveguides are established

in order to couple optical power from the laser source to the cantilever waveguide resonators and photodiodes. Empirically it has been found that waveguides smaller than 1 µm begin to experience significant loss due to sidewall imperfections due to the reduced optical mode confinement of reduced dimensions. In lieu of this, waveguide dimensions are fixed at 1.0 and 1.4 µm wide in order to obtain a range of dimensions for the final structures which are the least sensitive to variations in processing parameters and will produce the highest yield in suspended structures.

These waveguides are suspended above the substrate material by in-plane tethers anchored to larger un-released sections of waveguide material (see Figure 3.13). With the waveguide layers having tensile strain these suspended waveguide spans will not buckle. Each of these tethers have been found to have a loss of 0.1 dB/cm per tether for a tether width of 0.5 µm [182], and thus in comparison to estimated waveguide losses of over 2.5 dB/cm, minimal.

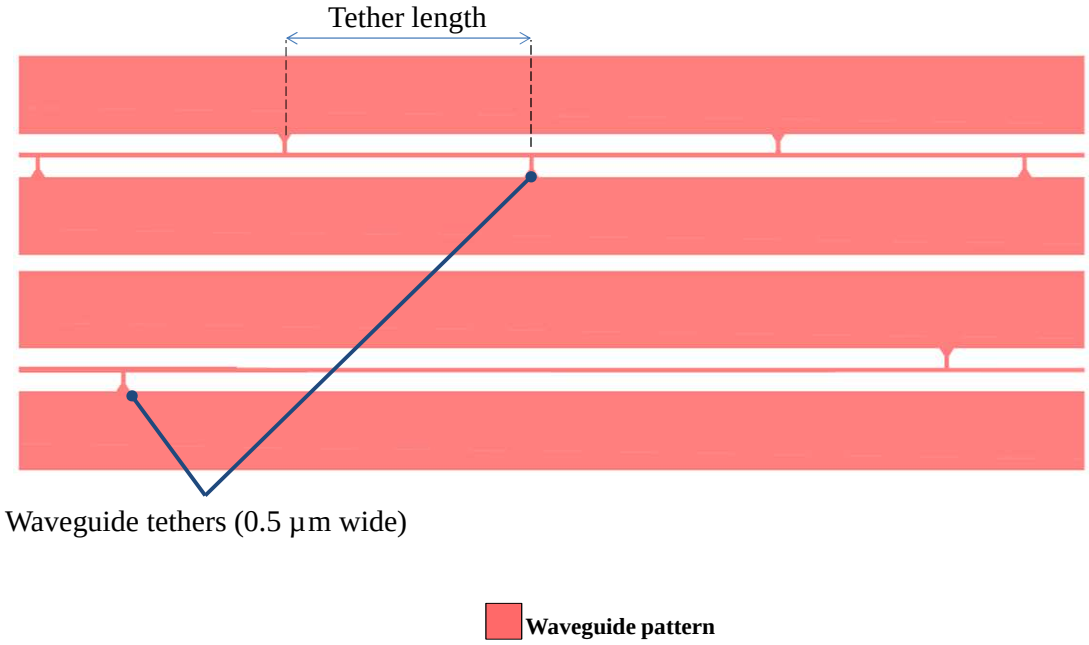


Figure 3.13. Top-down image of waveguides and tether locations.

Three designs are implemented for each waveguide width to span a variety of epitaxial growth conditions in case of material imperfections or errors in the strain of the waveguide layer so as to obtain higher yields without loss of devices due to waveguide buckling. Utilizing the Euler beam theory one can derive an expression for the critical length of a doubly clamped compressively-strained structure before buckling occurs:

$$L_{Critical} = \sqrt{\frac{\pi^2 E t^2}{3\sigma_{beam}}} \tag{3-20}$$

Where E is the young's modulus of the material (taken as 80 GPa from literature [183]), t is the smallest dimension of the beam crossection (the waveguide width in this case), and σ_{beam} is the compressive stress in the beam. For tensile stress, theoretically the critical length is infinite since tensile strain does not induce beam buckling.

Three variations on final material stress/strain are assumed in the designs from empirical data obtained through previous device implementations: tensile strained, 6 MPa compressive strain, 50 MPa compressive strain. Table 3.2 lists the values for final maximum tether spans calculated using equation (3-20).

Table 3.2. Final dimensions for tether suspensions given equation (3-20)

	1 µm wide waveguide			**1.5 µm waveguide**		
Assumed stress in beam (MPa)	tensile	6	50	tensile	6	50
Maximum tether spacing (µm)	1000	250	73.5	1000	400	110

3.1.8 Cantilever waveguide resonator design and layout

Cantilevers are formed from the suspended waveguides via the facet/electrical isolation etch also used for the laser diode. This etch "cuts" a doubly clamped waveguide and creates a single-clamped cantilever structure with a coupling gap to a stationary waveguide, as well as providing a deep etch for electrical isolation of the cantilever electrical actuation pads and the PIN photodiode structure. Electrostatic actuation of these beams is performed by applying a voltage between the bias electrode connected to the cantilever resonator, and an isolated actuation pad next to the device. Actuation direction is directed in-plane with the die surface. See section 3.1.6 for more details on operation.

Theoretical calculations covered in section 3.1.6 as well as previous demonstrations of this cantilever waveguide system were used to converge on a number of practically useful dimensions for device operation [31, 32]. Upper and lower bounds were placed on cantilever length at 70 and 25 µm respectively, the final cantilever lengths designed to be 70, 60, 50, 40, 30, 25 µm long. Each of these lengths is fabricated in the two waveguide widths (1, 1.5 µm) and with two actuation gap dimensions: 1 and 2 µm. Figure 3.14 presents the relevant dimensions for the design of the cantilever resonators.

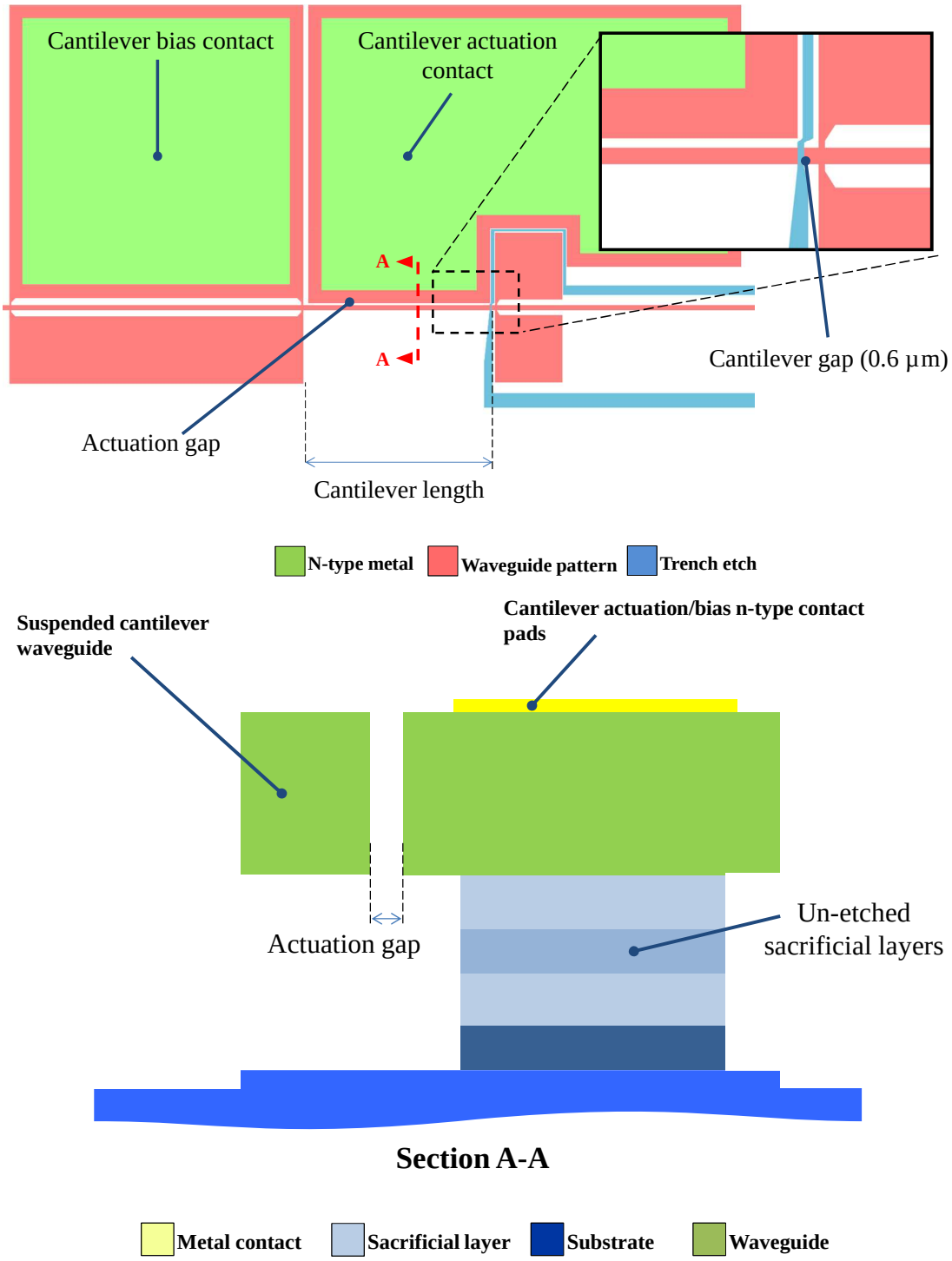


Figure 3.14. Top-down (top) and Cross-sectional view of cantilever waveguide resonator design with relevant dimensions specified.

Integrated PIN photodiode

The design of the photodiode region was kept as an underlying PIN photodiode region in accordance with previous work [31, 169] and following the scheme originally proposed. The reasoning behind using an waveguide-integrated PIN waveguide integrated diode configuration is motivated largely by the need for moveable and suspended structures; thus an underlying single-crystal sacrificial layer which is etch selective to InP material is utilized. This underlying layer was designed to be absorbing at the wavelength of light propagating through the waveguide, providing a built-in absorbing layer for the PIN photodiode. A novel core-geometry was introduced in order to decouple the thickness needed for the sacrificial layer from the optically absorbing layer thickness.

Previous designs also demonstrated that the 1.8 μm thickness of the underlying absorption region provided sufficient absorption for all variations of diode dimensions [31, 169] and thus the absorption layer thickness was optimized to achieve a sufficient cutoff frequency of operation rather than an optimal absorbing thickness. In addition to this parameter, reduction in overall absorbing intrinsic layer thickness was introduced in order to reduce the total thickness of the epitaxial growth and make deep trench isolation etching easier to acheive.

3.1.9 Core-absorber architecture

Previous experiments and design iterations in this material system [26, 28, 30, 32, 183] have found that very thin sacrificial layers become problematic in the release of the moveable waveguide structures. The reasoning for this is twofold: Wet etchant

effectiveness and stiction upon drying. Wet etchant diffusion underneath the mechanical waveguide structure is reduced for thin layers, increasing the time required to achieve the proper wet undercut. This in and of itself is not a significant problem when nearly 100% etch selectivity is maintained, however the metal pads on the structure as well as other layers in this more complex system do not have 100% etch selectivity with respect to the sacrificial layer; increased etching time often leads to unwanted material removal.

Stiction is an additional concern when dealing with MEMS devices. Stiction occurs during the wet etching process and is caused by the capillary forces due to surface tension forces at the air-liquid interface which occur during the drying process. To prevent this process, a specialized critical-point drying process is used (see section 4.1.6.2), however in practical processing conditions; there is some level of damage due to stiction which can occur. Having a very thin sacrificial region increases the possibility of encountering stiction resulting from accidental or localized drying.

Introducing a material which is optically transparent at 1.550 μm, and is also etch selective to InP just as the InGaAs material allows for the design of a thicker wet-etchable sacrificial layer, while being able to adjust the optically absorbing InGaAs material thickness independently. For this design, the PIN photodiode intrinsic region consists of two materials, comprised of 3 layers; a core absorbing region composed of InP lattice matched InGaAs, and cladding of $In_{0.825}Ga_{0.175}As_{0.38}P_{0.62}$. The bandgap of InGaAs is calculated to be 0.7451 eV, and for $In_{0.825}Ga_{0.175}As_{0.38}P_{0.62,}$ 1.076 eV. These values correspond to an absorption edge

of 1.664 µm and 1.154 µm respectively, indicating that the core region will absorb 1.55 µm wavelength light and the cladding layers will be transparent. InGaAs is chosen as the absorber primarily for its wet-etch selectivity when performing the undercut etch (detailed in sections 4.1.6 and 3.1.4). The particular transparent quaternary alloy of $In_{0.825}Ga_{0.175}As_{0.38}P_{0.62}$ is chosen because it reacts with acid:peroxide:water wet undercut etchants just like InGaAs, is optically transparent at 1.55 µm wavelengths, and for epitaxial growth convenience since it is used in the laser region and has thus will be already calibrated for precise growth.

In contrast with previous designs that utilized a 1.8-2 µm thick sacrificial layer [26, 30, 31, 169, 183], a reduced sacrificial layer thickness of 1 µm is chosen to provide significant thickness for release, as well as reduce the overall epitaxial growth thickness by approximately 1 µm. The thicknesses of the individual materials in this core-designed sacrificial layer are then chosen based upon the required photodiode response time.

3.1.10 Diode response time

A PIN photodiode's response time is dominated by two competing effects: RC time constant and the carrier transit time. The RC time constant is determined by the junction capacitance and circuit resistance (assuming standard 50 Ω termination), and increases with reduced intrinsic region thickness. The transit time refers to the time that a photo-generated charge takes to traverse the intrinsic region. This phenomena is dominated by the carrier saturation velocity and transit time is clearly reduced with the thickness of the intrinsic region. The 3 dB cutoff frequency of the PIN

photodiode will be dominated by one of these effects, with an optimal point that they intersect.

The PIN diode junction capacitance in reverse bias is the series combination of the capacitance in the depletion regions in the diode: *n*-type, *p*-type, and intrinsic. This follows from the standard expression for junction capacitance (C_j) and can be written as:

$$C_j = \frac{A}{\frac{x_n}{\varepsilon_n} + \frac{x_p}{\varepsilon_p} + \frac{d(t_{absorber})}{\varepsilon_{InGaAs}} + \frac{d(1 - t_{absorber})}{\varepsilon_{InGaAsP}}} \tag{3-21}$$

where A is the area of the photodiode, x_n and x_p are the depletion widths of the *n*-type and *p*-type regions of the PIN photodiode, d is the total width of the intrinsic region, $t_{absorber}$ is the percentage of the intrinsic region which serves as the absorber core (InGaAs material), and ε_n, ε_p, ε_{InGaAs}, $\varepsilon_{InGaAsP}$ are the relative permittivities of the *n*-type, *p*-type, InGaAs intrinsic core absorber, and the InGaAsP intrinsic cladding material, respectively.

Determining the values for the depletion widths follows the straightforward full-depletion approximation with an inserted intrinsic region between the *p* and *n* type materials. Assuming all charge density in the PIN junction can be attributed to the *p* and *n* type materials, the built-in potential, φ_i can be defined as:

$$\varphi_i = \frac{kT}{q} \ln \left[\frac{N_a N_d}{{n_i}^2}\right] \tag{3-22}$$

where k is the Boltzmann constant, T is the temperature, q is the elementary charge, N_a, N_d and n_i are the doping densities of the *p*, *n*, and intrinsic regions, respectively. The charge densities in the *p*-type and *n*-type regions are assumed to be constant in

the depletion region (qN_a and qN_d), and the charge density in the intrinsic region is assumed to be zero. Charge neutrality holds then that:

$$qN_a x_p = qN_d x_n \tag{3-23}$$

Additionally the potential in each of these regions can be determined by integrating over the charge density and equating to the built in potential (equation (3-22) minus any applied potential:

$$\varphi_p + \varphi_n + \varphi_{undoped} = \frac{qN_a {x_p}^2}{2\varepsilon_p} + \frac{qN_d {x_n}^2}{2\varepsilon_n} + \frac{qN_a x_p d}{\varepsilon_i} = \varphi_i - V_a \tag{3-24}$$

Equations (3-22), (3-23), and (3-24) can then be combined to find x_n and x_p expressed below:

$$x_n = \frac{\sqrt{\left(\frac{d\varepsilon_n}{\varepsilon_i}\right)^2 + \frac{2\varepsilon_n(\varphi_i - V_a)}{qN_a}\left(1 + \frac{N_d}{N_a}\right)} - \frac{d\varepsilon_n}{\varepsilon_i}}{\left(1 + \frac{N_d}{N_a}\right)} \tag{3-25}$$

$$x_p = x_n \frac{N_d}{N_a} \tag{3-26}$$

Equations (3-21), (3-25), and (3-26) are then utilized to establish the capacitance of the PIN diode for a constant applied bias voltage of 0 V. Device area is determined by the photodiode dimensions utilized in previous iterations [31, 169], shown below in Figure 3.15.

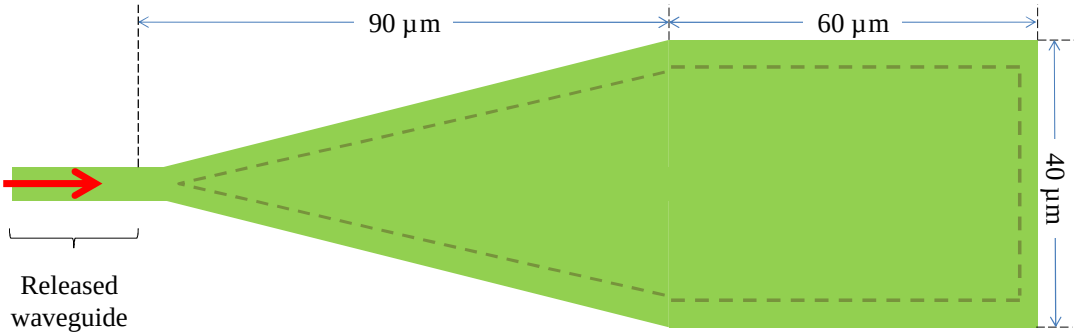


Figure 3.15 Top-down schematic view of waveguide photodiode. Red arrow indicates incident optical radiation; dotted line indicates the estimate for the extent of the undercut etch.

The 3 dB cutoff resulting from the junction capacitance can be approximated by considering the RC time constant of the circuit created. In this case, the 3 dB frequency can be expressed as:

$$f_{3dbRC} = \frac{1}{2\pi R_{ext} C_j} \tag{3-27}$$

where C_j is the junction capacitance and R_{ext} is the external circuit resistance, taken to be 50 ohms in this case.

The other competing effect in the PIN photodiode response time is the transit time of the carriers in the intrinsic region. This can be derived as in [184] by considering a varying current in the photodiode due to a periodic photon flux intensity:

$$photon\ flux = \varphi_1 e^{i\omega t} \tag{3-28}$$

The current density at V_a=0 then can be expressed as:

$$J_{sc} = \frac{q\varphi_1\left(1 - e^{i\omega t_r}\right)}{i\omega t_r} e^{i\omega t_r} \tag{3-29}$$

where t_r is the transit time of the carrier, which can be expressed as:

$$t_r = \frac{d}{v_s} \tag{3-30}$$

Where d is the thickness of the intrinsic region, and v_s is the saturation velocity of the generated carriers. The 3 dB cutoff can then be expressed as:

$$f_{3dbTT} = \frac{2.4}{2\pi t_r} \tag{3-31}$$

As both of these effects are present at all times in the PIN photodiode during operation, one will dominate over the other depending on intrinsic layer thickness. From equations (3-27) and (3-31), we see that 3 dB cutoff frequency due to the junction capacitance is directly proportional to the intrinsic layer thickness, and the transit-time of carriers is inversely proportional to the intrinsic layer thickness, indicating there is an optimal thickness for this system. Figure 3.16 shows a plot illustrating this for the case where the core InGaAs thickness is 25% of the total intrinsic layer thickness. For this particular case, the optimal intrinsic layer thickness is 0.677 µm thick, with a cutoff frequency of 5.65 GHz. From previous work, it has been found that measuring a cantilever resonator over 1 GHz is not practical, and can be set as an upper limit for the required response time of the PIN photodiode. This leads to a thickness range of 3.7 – 0.068 µm in order to achieve this metric. As a compromise on final thickness of the total layer structure thickness, 1 µm was chosen for the final intrinsic layer thickness, with a ¼ ratio of core InGaAs to InGaAsP, corresponding to a cutoff frequency, dominated by the carrier transit time, of 3.8 GHz.

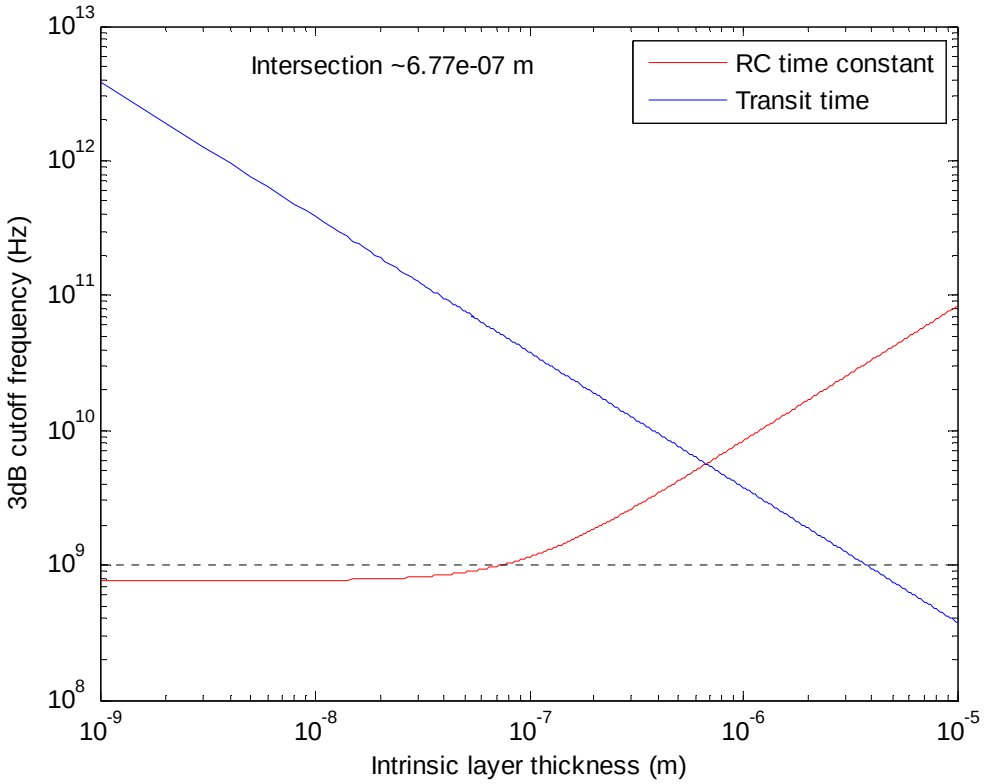


Figure 3.16. Plot of the 3dB cutoff frequency due to junction capacitance and carrier transit-time versus the intrinsic layer thickness. Dotted line provides a guide for the eye towards 1 GHz.

3.1.11 Core-absorber intrinsic region optical performance

Previous designs of this InP optical MEMS based system have included only the waveguiding regions and the optical absorption regions, addressing the separation of the two by physically removing the underlying absorptive region in passive waveguiding regions, serving the dual purpose of preventing absorption where intended and creating suspended structures. For this fully integrated design, complete removal of this underlying layer in all but the absorption region is not a viable solution due to the heat dissipation requirements of a laser source and due to the incompatible size scales of the geometries. To provide a larger surface area for heat transfer, the underlying layers must remain intact. These layers, however, are

designed to absorb at 1.550 μm as the absorbing region for the PIN photodiodes, and therefore have the potential to be lossy and reduce the efficiency of the laser source.

Fortunately, the thin absorber core design utilized in order to obtain sufficient cutoff frequency will potentially reduce the coupling from the laser region into this underlying sacrificial layer due to the reduced thickness. A tradeoff in coupling strength for photodiodes will obviously need to be made here since the introduction of a core layer reduces the efficiency of the PIN photodiodes.

To validate and to establish the impact of the core-absorber architecture on the optical modes supported in the laser region and photodiode regions, simulations have been performed using a MATLAB software package developed by Thomas Murphy's research group at the University of Maryland. This method uses a full vector finite difference algorithm to solve for mode profiles in dielectric waveguides comprised of materials that are symmetric in the *z* propagation direction [185]. The details of this method are beyond the scope of this dissertation, however the basic description of this discretization approach is as follows: the routine uses finite difference methods to compute the two transverse magnetic field components H_x and H_y for dielectric waveguides by applying the combined Maxwell's curl equation $\nabla \times (\boldsymbol{\varepsilon}^{-1} \nabla \times \mathrm{H}) - \omega^2 \mu_o \mathrm{H} = 0$ and the divergence relation $\nabla \times \mathrm{H} = 0$, and then using these values to compute E_x and E_y. The MATLAB routine has been used and modified to solve the mode profiles generated in the specific layer structure compositions illustrated in Table 3.1 and designed device geometries shown here in section 3. The primary goals are to estimate the loss experienced by the guided modes in the layer structure for both the core-based absorber structure and a simpler single-material intrinsic

region, and calculate the relative overlap of the electromagnetic fields in the absorber of the PIN photodiode. Only the primary TE mode is considered in the following calculations as this mode experiences the highest gain in quantum well ridge laser structures due to the larger density of states in the heavy-hole valence bands dominating radiative transitions [186, 187].

Output of this MATLAB code provides an effective index of propagation, which is generally a complex value, with the imaginary part indicating loss/gain. The following describes the calculation used to estimate the optical loss in the structure from the effective index of refraction.

For a propagating plane electromagnetic wave the electric field can be written as:

$$\vec{E} = Ae^{i(kz-\omega t)} \tag{3-32}$$

where A is a normalizing constant and *k* is defined as:

$$k = \frac{2\pi(n_{real} + in_{imaj})}{\lambda} \tag{3-33}$$

with n_{real} and n_{imaj} being the real and imaginary indices of refraction, respectively, and λ the free-space wavelength of the electromagnetic radiation. Knowing that the intensity (*I*) of the radiation is proportional to the square of the electric field magnitude, we can write:

$$I = |A|^2 e^{-\frac{4\pi\, n_{imaj}}{\lambda} z} = |A|^2 e^{-\alpha z} \tag{3-34}$$

for the intensity, and therefore α represents the absorption coefficient (in cm^{-1}). To calculate the loss (or gain) in dB/cm, we use the following:

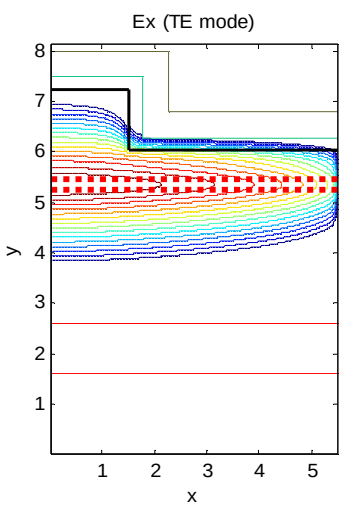
$$Gain\left(\frac{dB}{cm}\right) = \frac{10}{\ln\ 10} \times \frac{4\pi\ n_{imaj}}{\lambda} \tag{3-35}$$

where n_{imaj} is the imaginary part of the effective index yielded from the simulation results.

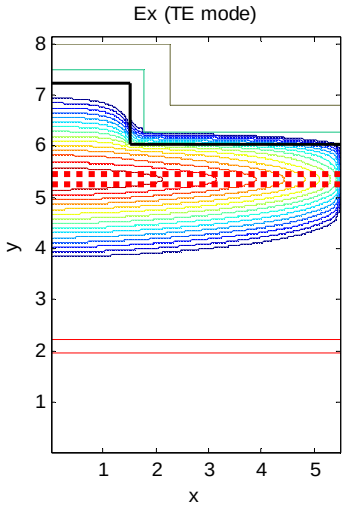
In addition to this loss estimation, the relative overlap of the electric field in the absorption region is calculated and expressed as a ratio with respect to the integral of the total field in the simulated mode.

$$Overlap\ ratio = \frac{\iint^{Absorber} \left|E_{xyTE}\right|^2}{\iint_{-\infty}^{\infty} \left|E_{xyTE}\right|^2} \tag{3-36}$$

In the following simulations of the layer structure, optical loss due to absorption of 2.3×10^3 cm^{-1} in the InGaAs sacrificial region is taken from values for attenuation coefficients in literature [188]. This simulation also takes into account the eventual surface coatings of Si_3N_4 and gold metal on the surfaces of the laser ridge (described in section 0). The calculated loss parameters are also presented in Table 3.3.

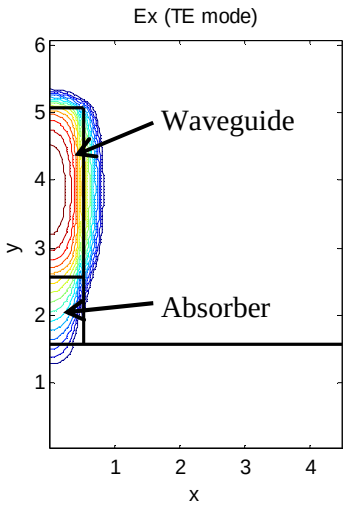


Loss TE mode: 1.1067 dB/cm
Overlap ratio: 8.1775×10^{-10}

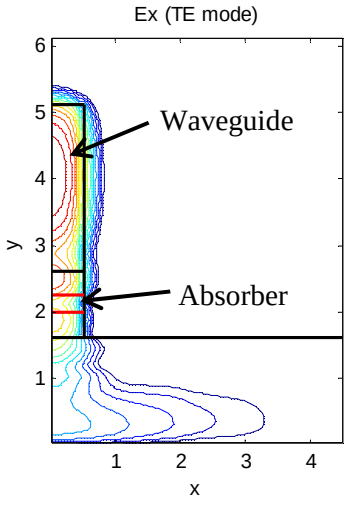


Loss TE mode: 1.106 dB/cm
Overlap ratio: 3.4197×10^{-10}

Figure 3.17. Simulations showing the effect of a single material (left) or a core (right) sacrificial region under the laser ridge of the optical source (indicated by the solid red lines on the plot). The quantum well optical gain region is indicated by the dotted red lines. The green and gray lines represent the passivation and metalization, respectivley. Loss of the fundamental mode is presented in caption and was calculated using equation (3-35).



Loss TE mode: 51.11 dB/cm
Overlap ratio: 0.0044



Loss TE mode: 104.63 dB/cm
Overlap ratio: 0.0078

Figure 3.18. Simulations showing the effect of a single material (left) or a core (right) sacrificial region in the waveguide-coupled PIN photodiode (indicated by the solid red lines on the plot). Loss of the fundamental mode is presented in caption and was calculated using equation (3-35).

Table 3.3. Calculated loss parameters from optical mode simulations.

	In laser region		In photodiode region	
	Single absorber	**Core-absorber**	**Single absorber**	**Core-absorber**
TE mode loss (dB/cm)	1.1067	1.106	51.11	104.63
Overlap	8.1775×10^{-10}	3.4197×10^{-10}	0.0044	0.0078

As can be seen in Figure 3.17 and Table 3.3, the introduction of a core sacrificial region does not significantly affect the losses experienced in the laser region; this is due to the small overlap of the mode in these regions which can be seen illustrated in the overlap ratio. This allows for a nearly arbitrary choice of a core thickness for the optical absorber and thicknesses for the quaternary cladding layers that are introduced in order to increase the sacrificial layer thickness without affecting the optical performance of the laser significantly.

Of note however, is the result of a core-waveguide structure on the PIN photodiode regions shown in Figure 3.18 and Table 3.3. Not surprisingly, the core-absorber architecture simulated here exhibited a higher overlap and therefore a higher estimated loss, increased by about 50%. This phenomena has been predicted and used for other waveguide-integrated photodiodes, particularly traveling-wave photodiodes [112]. The results of these simulations along with the response time considerations solidify the choice of layer structure dimensions as shown in Table 3.1.

3.1.12 PIN Photodiode design and layout

The final component in this microsystem to be defined is the PIN photodiodes which are used to transduct the movement of the cantilever waveguides. As described in section 3.1.6, the intrinsic absorbing region is formed by the sacrificial release layers. In order to keep the release layer intact in the photodiode region, an area with larger width is introduced so that during waveguide and cantilever release the sacrificial layer will remain. While reflections into a larger width such as the unreleased photodiode region from a narrow waveguide are expected to be very small [189], an adiabatic 90 µm long taper from waveguide width (1 or 1.2 µm wide) to 40 µm is introduced for convenience considering the practical required electrical contact pad dimensions which enlarge the structure. Figure 3.19 indicates this taper location. Topside contacts are made to the top waveguide *n*-type material at the same time as the cantilever actuation contacts and the laser *n*-type metallization. The *p*-type contacts are formed on the buried InGaAs layer which is reached after the waveguide mask is patterned to form the waveguide structures. This bottom contact is thus offset from the actual absorbing region of the photodiode. Dimensions of these structures were not varied, a fixed dimension of 40×60 µm was chosen with a 90 µm long taper from the waveguide width (1 µm or 1.5 µm) to the final photodiode width of 40 µm. Previous work had shown that very little practical advantage is gained in these waveguide PIN photodiodes by increasing or reducing the size of the structure [31], and thus a conservative design was chosen that had the sufficient frequency performance and fit within space constraints of the rest of the system components and maximized the number of devices to be included on the die.

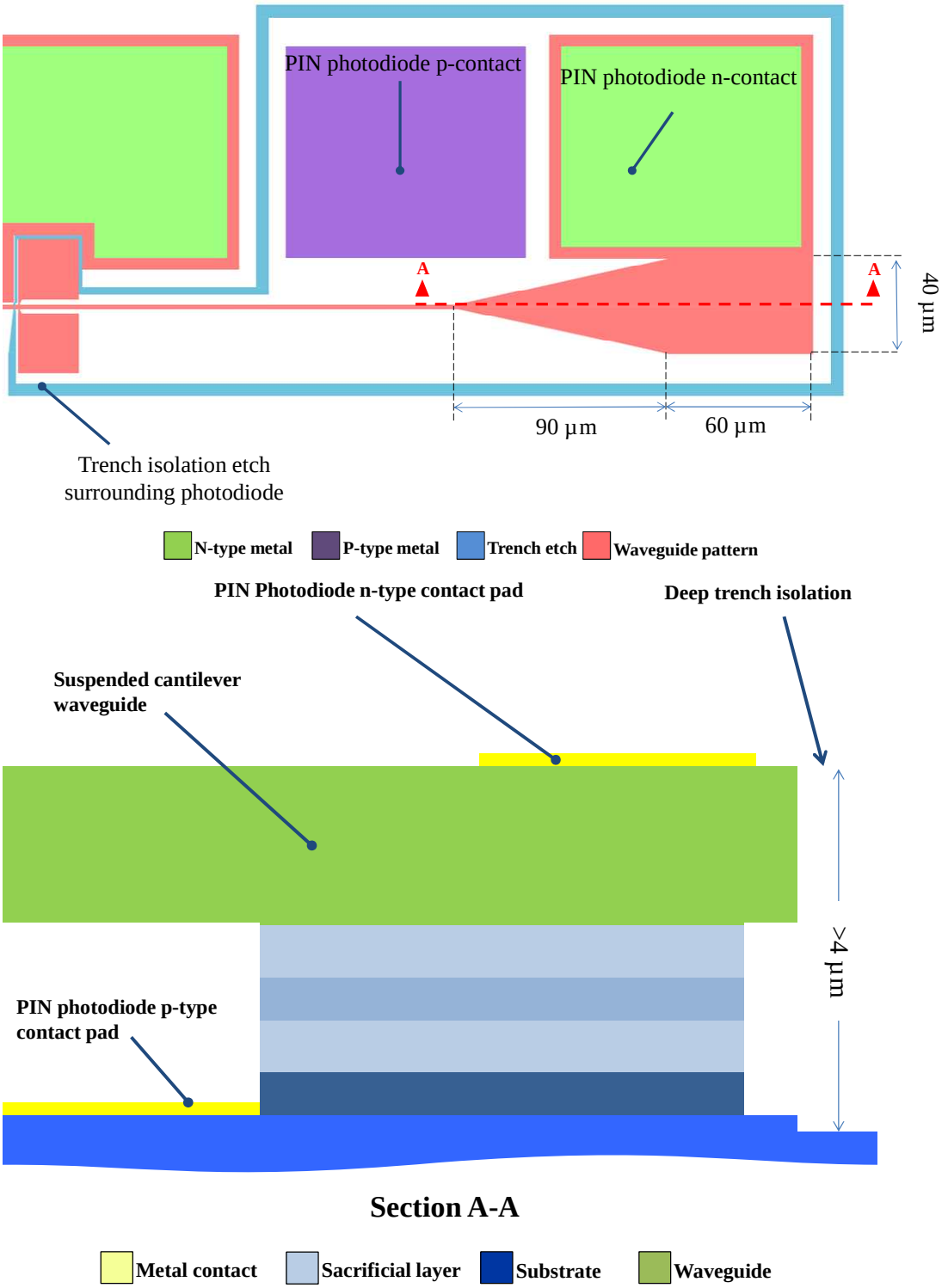


Figure 3.19. Top-down schematic of the photodiode region with relevant dimensions indicated (top) and a cross sectional view of the photodiode region (bottom)

Final device layout

Each of these components are ultimately integrated into a single device as illustrated in Figure 3.20. The laser region is separated from the cantilever waveguide resonator and PIN photodiode via a 530 µm long tapered waveguide designed to capture more light from the output etched facet of the laser. The 530 µm long separation was introduced to further electrically isolate the laser regions from the other components of the integrated system, as well as reduce the stray light that may be collected in the PIN photodiode, increasing the background signal measured. This waveguide starts with a width of 5 µm at the coupling gap near the etched laser facet in order to collect the maximum light emitted from the cleaved laser facet, and reduces to the cantilever waveguide width of the resonator, 1 or 1.5 µm.

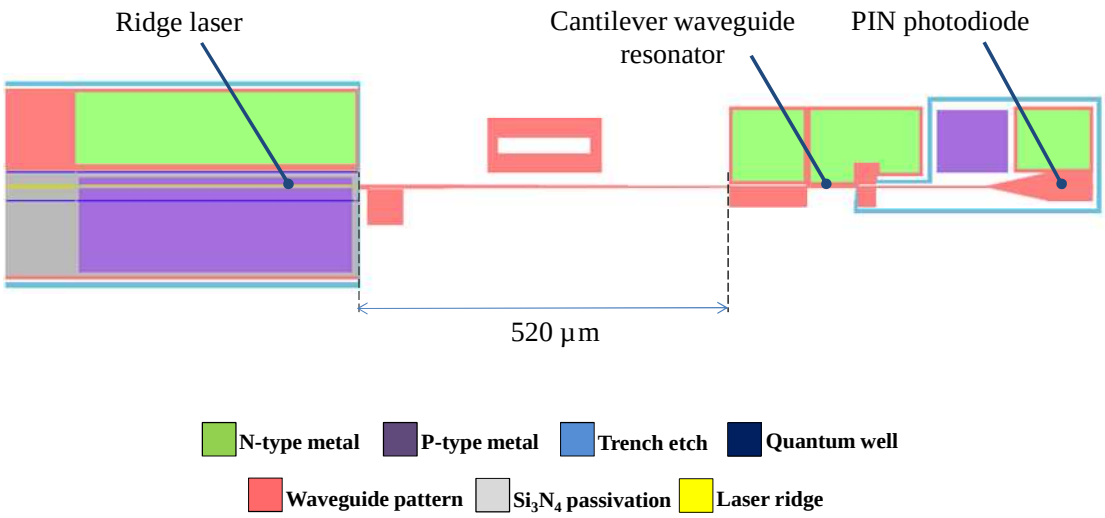


Figure 3.20. Top-down mask layout of the fully integrated laser-cantilever-and photodiode structure.

Slight variations on this fully integrated system shown in Figure 3.20 were included in the final mask design. Devices with only a laser component and a long tapered waveguide which could be coupled off-chip, devices which had no laser component, and instead allowed for an off-chip light source to be coupled to the

cantilever resonator and PIN photodiode, and devices with only cantilever waveguide resonators, requiring coupling of off-chip light sources and off-chip photodetectors. These variations were introduced in order to facilitate modular testing during device development.

The final 17×17 mm die design consists of seven 5x projection lithography masks, and comprises of 306 discrete devices. Devices which integrate all three components as in Figure 3.20 are placed in the center of the die in order to reduce processing imperfection due to edge-bead, mask misalignment, and other practical fabrication concerns. The top and bottom of the die contain test structures for measurement and process monitoring (release structures). The final die is split into three rectangular "chips," separated via cleave marks. These cleaves which separate the die into chips also form the cleaved laser facets and cleaved waveguide facets for coupling on and off chip. An overall image of the die layout is presented below in Figure 3.21.

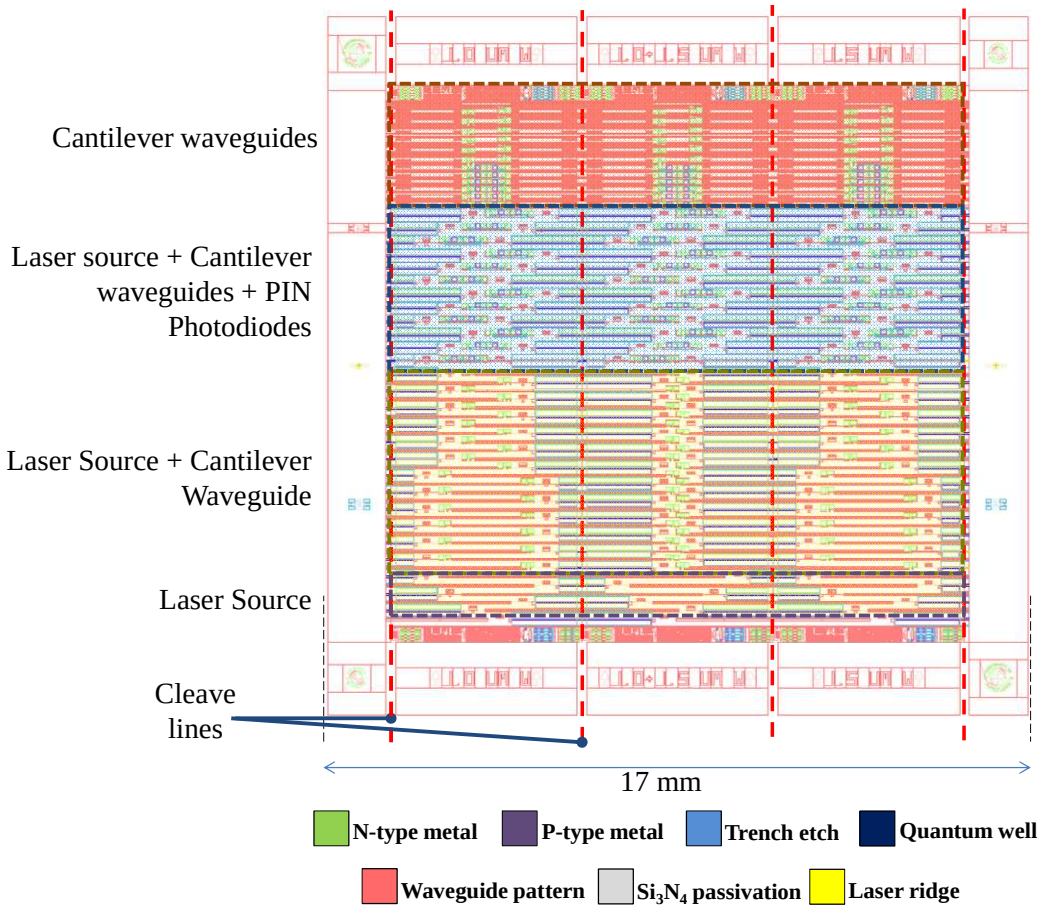


Figure 3.21. Full die layout with device variations labeled as well as cleave lines indicated.

4 Fabrication

Introduction

The bulk of fabrication of the III-V materials system-based devices was focused on the development of a number of unit-processes that are tailored for the geometries and materials utilized in the design. This chapter will outline a number of these processes employed and the critical aspects of the determined parameters. Additional data on the process recipes used is included in Appendix A.

Fabrication process flow

This section will describe the complete fabrication process flow of the integrated MEMS devices in more detail, specifics on fabrication processes follow in section 0. Full fabrication of the integrated MEMS device utilizes 7-projection lithography masks (see section 3.1.12), 4 nested inductively coupled plasma (ICP) etches, and over 60 discrete process steps. Figure 4.1-Figure 4.9 present diagrams in a simplified process flow outline covering the 9 major processing steps.

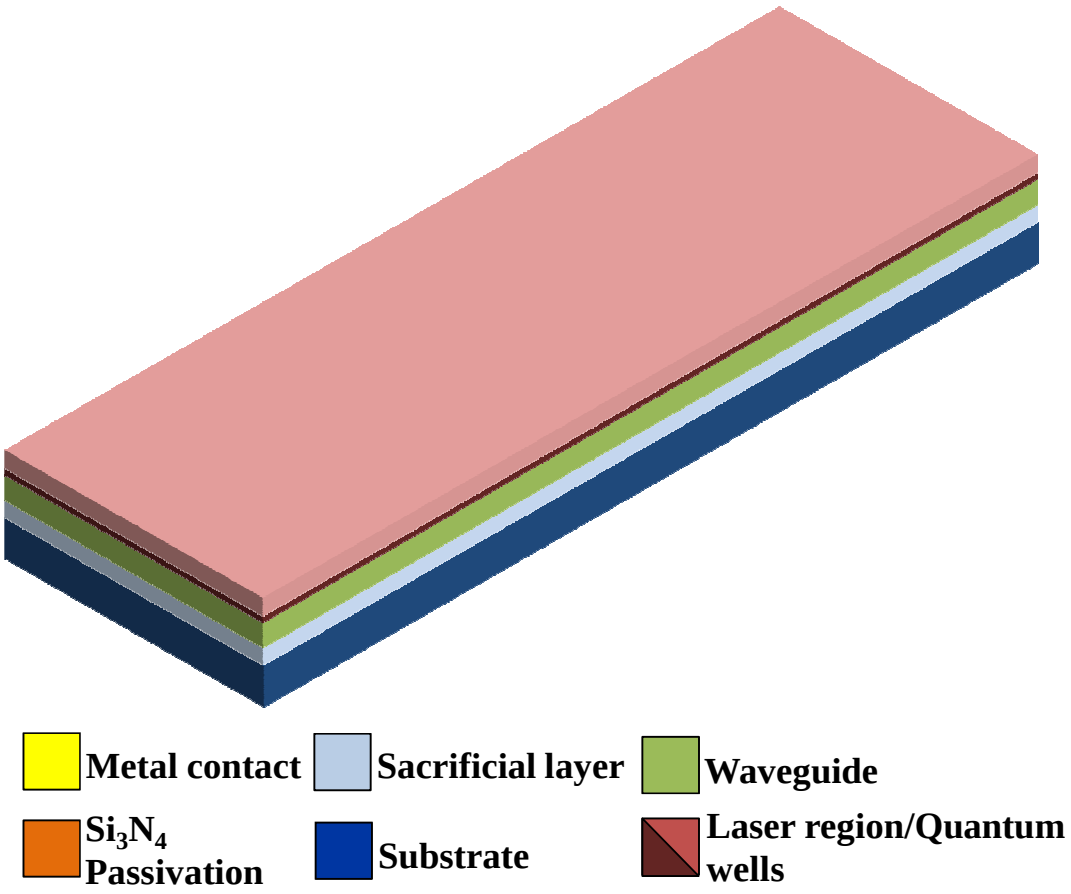


Figure 4.1. Step 1: Blank Substrate

Figure 4.1, Step 1: Fabrication begins with an epitaxially grown layer structure on a 625 µm thick InP wafer following the design in section 0 (Table 3.1). Due to limited material and process complexity, die-level fabrication is carried out on a cleaved 18×18 mm die. The die is coated with a 1.4 µm thick SiO_2 dielectric via plasma enhanced chemical vapor deposition (PECVD) in order to create a hardmask for ICP etching. A 1 µm thick positive photoresist layer is spun on the die and subsequently exposed and developed with the 1st mask level (trench) via projection lithography. This SiO_2 is patterned using a CHF_3-O_2 reactive ion etch (RIE).

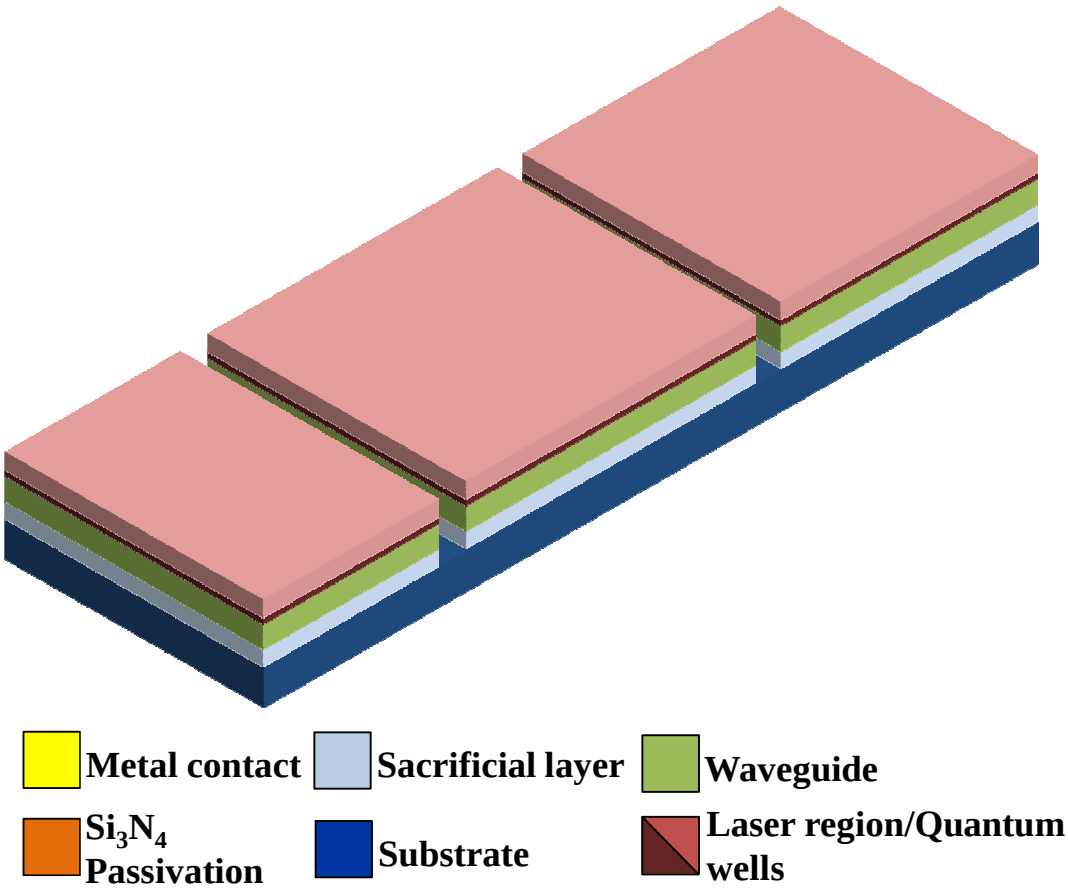


Figure 4.2. Step 2: Deep trench ICP etch which defines electrical isolation and laser facets.

Figure 4.2, Step 2: This SiO_2 pattern is then transferred into the underlying epitaxial substrate via an ICP etch, defining the deep isolation trenches, etched laser facets, and cantilever waveguide gaps simultaneously. The SiO_2 mask layer is removed via a wet 5-min buffered oxide etch (BOE).

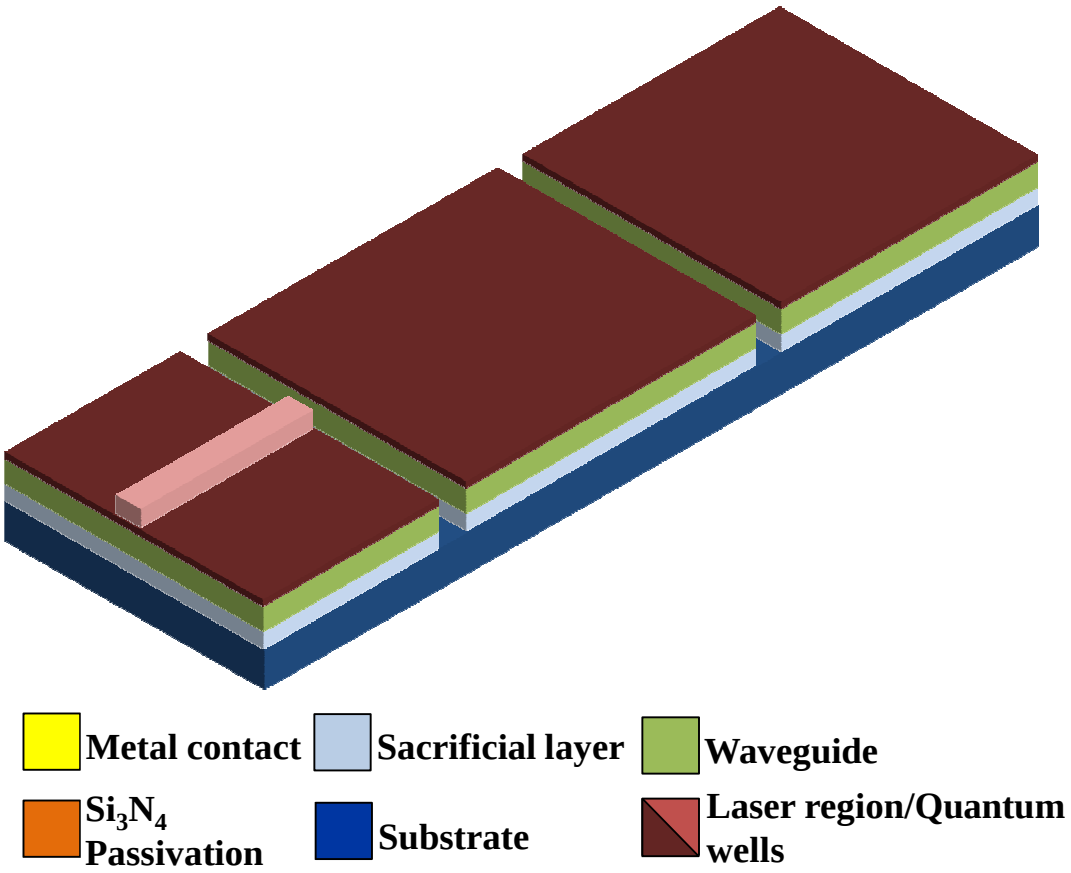


Figure 4.3. Step 3: Laser ridge ICP etch which defines the lateral confinement for the laser cavity.

Figure 4.3, Step 3: A second 1.0 µm SiO_2 hardmask is deposited via PECVD on the die. The die is coated with a 3.6 µm thick layer of positive photoresist in order to facilitate coverage over the very deep etched features. All subsequent photoresist thicknesses are ≥ 3.6 µm, due to the more complex and taller surface irregularities introduced through the remainder of processing steps. The laser ridge structure is then exposed and patterned into the photoresist layer, aligned to the underlying trench etch pattern. This photoresist mask is used to pattern the underlying SiO_2 hardmask material via the standard RIE etch. This SiO_2 mask is then used to define the shallow ridge etch via ICP. A 5 minute BOE dip is used to remove the hardmask.

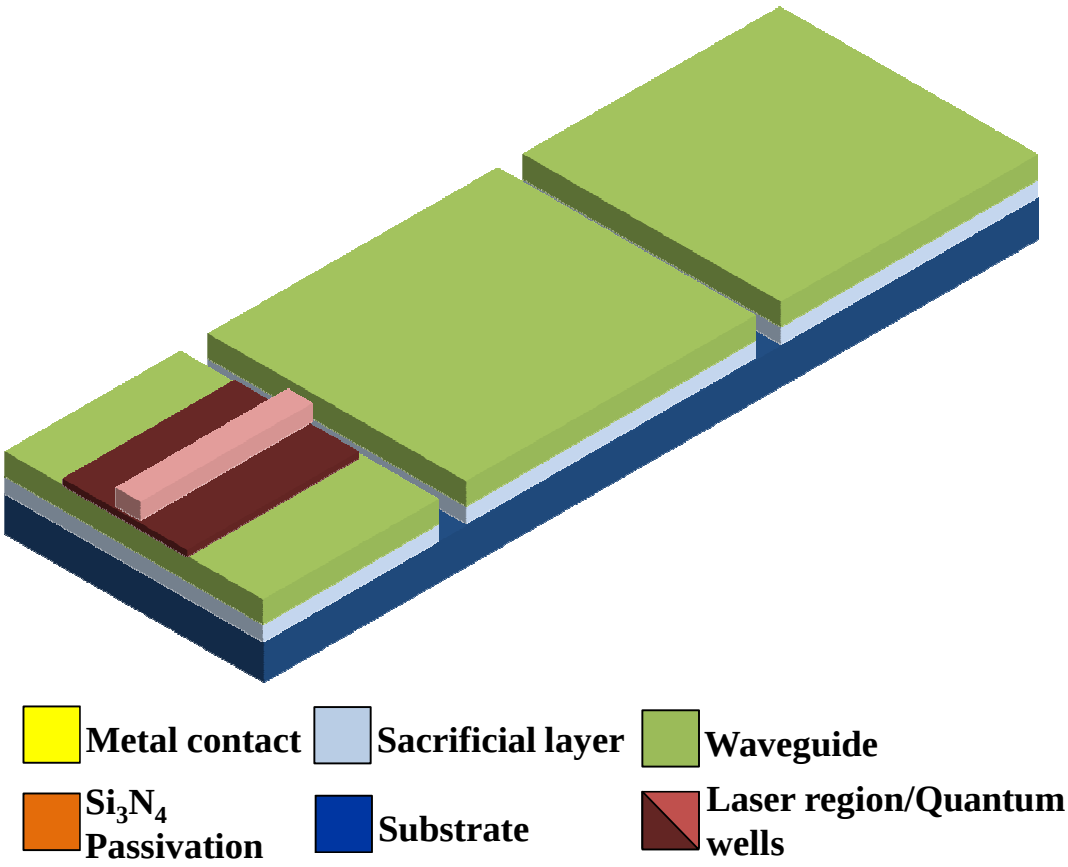


Figure 4.4. Step 4: Quantum well ICP etch which removes active region over the wafer where it is not needed and defines vias for topside *n*-type laser contact layers.

Figure 4.4, Step 4: A third 1.0 µm SiO_2 hardmask is deposited via PECVD on the die. The die is again coated with a 3.6 µm thick layer of positive photoresist in order to facilitate coverage over the additional etched features. This photoresist is patterned with the quantum well removal mask aligned to the laser ridge, all of which is designed to remove quantum wells over the die except 15 µm on either side of the laser ridge (see section 3.1.3 and Figure 3.4). RIE is used to transfer this photoresist pattern into the SiO_2 hardmask. ICP is used to etch through the quantum wells, exposing the *n*-type contact layer for the laser devices and removing the active region from the majority of the die. This step completes the etch component of the laser fabrication. BOE is used to remove this hardmask as with previous steps.

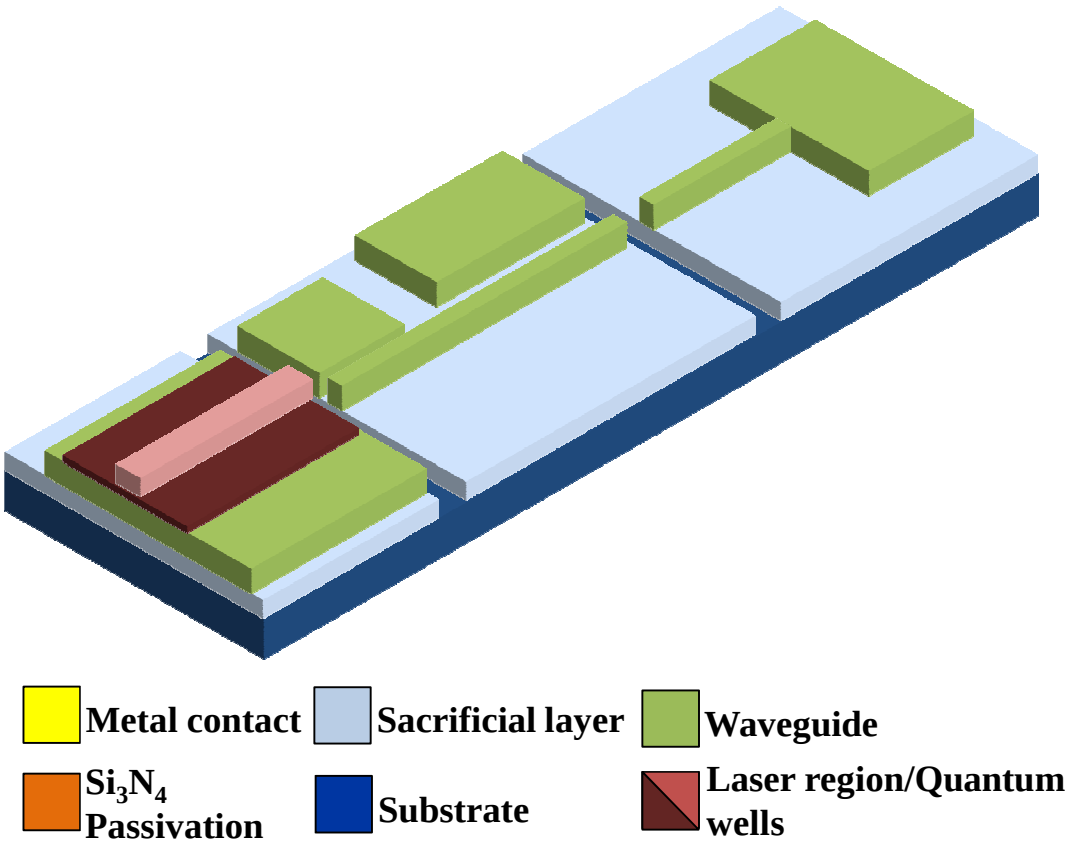


Figure 4.5. Step 5: Waveguide and photodiode ICP etch which creates the majority of the device layout and creates vias to buried *p*-contacts for photodiodes.

Figure 4.5, Step 5: A fourth 1.0 µm SiO_2 hardmask is deposited via the same PECVD methods. 3.6 µm thick photoresist is spin coated on the die and the pattern for the waveguides is exposed, aligned to the initial trench layer. This waveguide pattern defines the passive suspended waveguides, MEMS components, and the photodiodes. The photoresist pattern is once again transferred into the underlying SiO_2 via the standardized RIE etch. A timed ICP etch is used to etch through the underlying layers, stopping at the *p*-type bottom contact of the photodiodes. BOE is once again used to remove the hardmask.

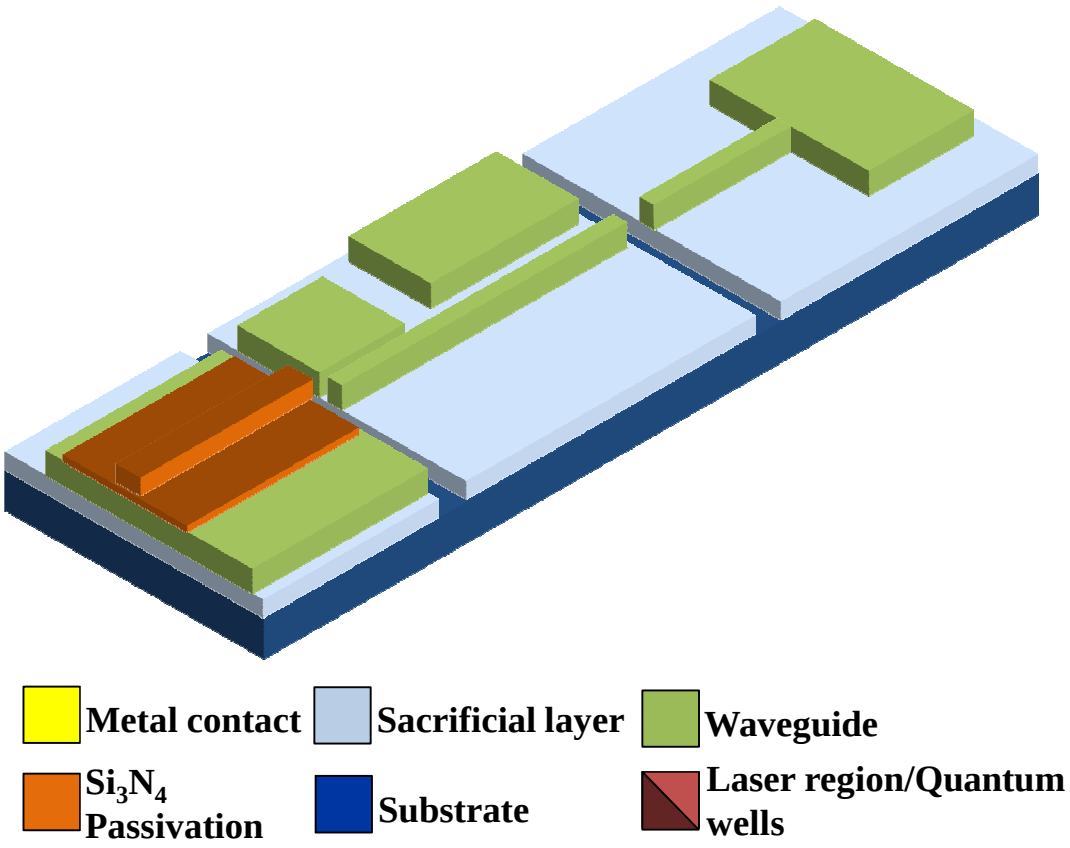


Figure 4.6. Step 6: Nitride passivation to protect and passivate laser region.

Figure 4.16, Step 6: 2000-7000 Angstroms of Si_3N_4 is deposited on the whole sample via PECVD in order to serve as a conformal laser-passivation region and as a protective coating for the metallization and undercutting steps. 3.6 µm thick photoresist is spin coated and exposed to define the laser passivation regions. A standardized SF_6 RIE etch is used to pattern this region and remove it across the majority of the die.

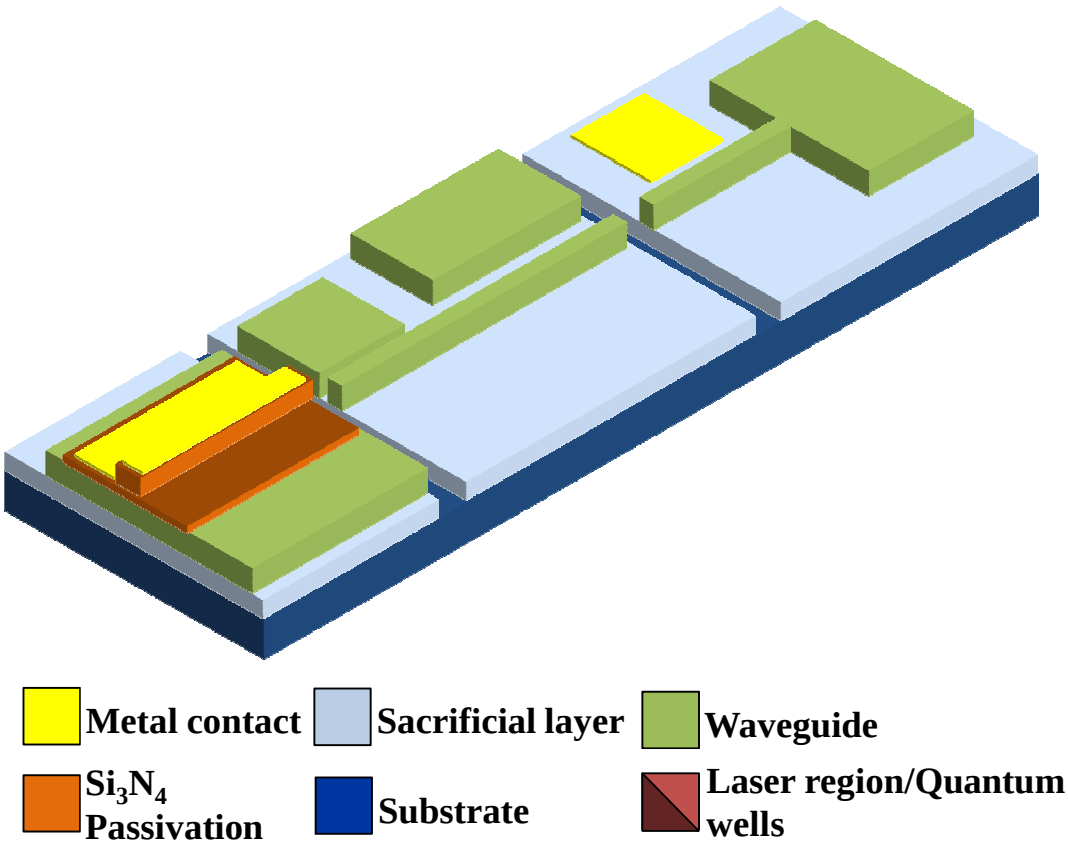


Figure 4.7. Step 7: *P*-type metal lift-off.

Figure 4.7, Step 7: 5 µm thick negative photoresist is spin coated on the sample to serve as the *p*-type metallization lift-off mask. The *p*-type metallization step needs to achieve continuity up a 1.2 µm tall laser ridge to create contact between the pad and the very top of this ridge structure. To achieve this, the standard *p*-type metallization (Ti-Pt-Au) is performed in an e-beam evaporation system with a planetary sample holder in order to obtain better sidewall coverage. To assure sufficient coverage, 1.2 µm of gold is deposited in the evaporation system. Lift-off is performed in 90°C resist stripper consisting of primarily the organic solvent N-Methylpyrrolidone (NMP). This step defines all of the *p*-type contacts, laser and photodiode.

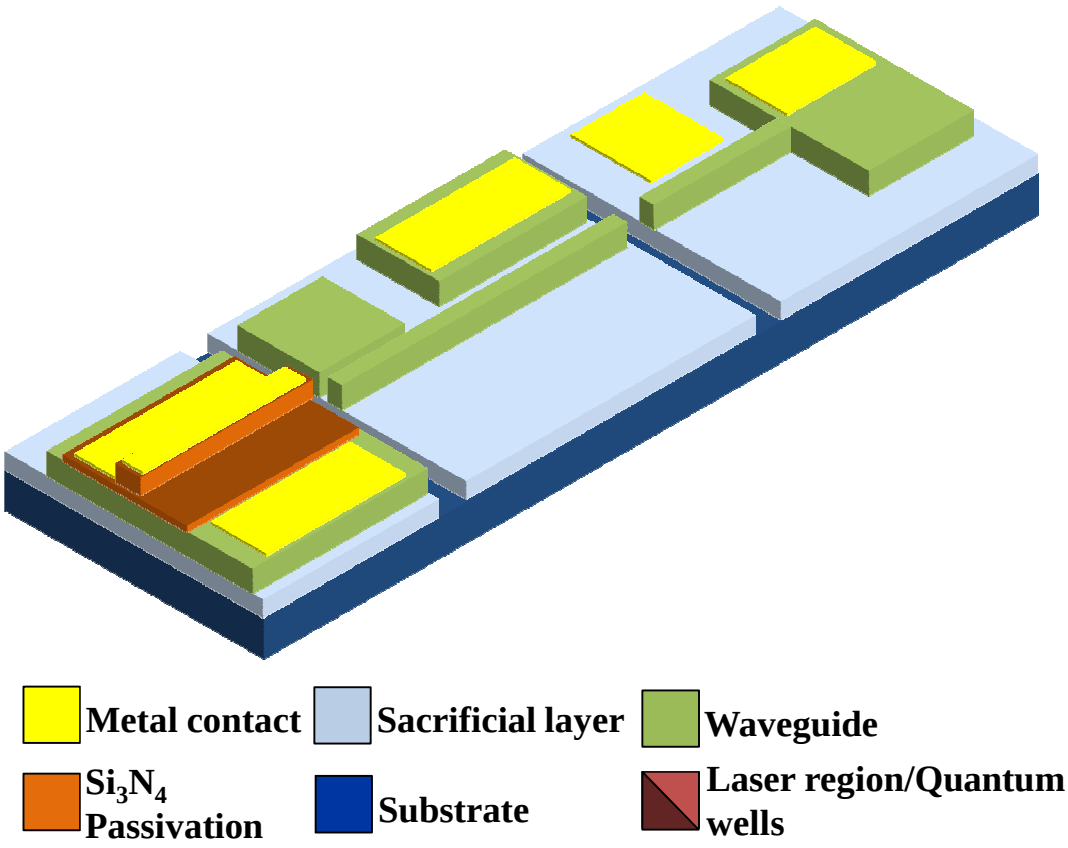


Figure 4.8. Step 8: *N*-type metal lift-off and anneal.

Figure 4.8, Step 8: 5 µm thick negative resist is spin coated on the die; along with subsequent alignment and exposure to define the *n*-type metal pads. No significant continuity over tall steps is needed for this step, so the deposition of the standard Ni-Ge-Au-Ni-Au *n*-type metallization is performed in the e-beam evaporation system with a standard mounted sample holder. Lift-off of the excess metal is performed in 90°C resist stripper (NMP). The *n*-type metallization is completed with a rapid thermal annealing (RTA) step of 60 seconds at 300°C and 40 seconds at 400°C. Annealing the structure alloys the *n*-type metal stack and reduces the Schottky barrier at the *n*-type semiconductor surface. This step defines all of the *n*-type contacts, laser, photodiode, and waveguide actuation.

A 6-7 µm thick photoresist layer is spin coated on the sample in order to protect the front of the die during the wafer thinning process. The die is mounted, via crystabond wax (acetone-soluble), un-processed side-up on a quartz plate which is fixture to a lapping monitor. A slurry of 9 µm alumina and deionized (DI) water is used to thin the die from 625 µm to 175 µm thick in order to facilitate more accurate cleaves when portioning the die into three chips. Acetone is used to de-bond the die from the quartz plate after lapping.

A precision scribe is used to create crystal defects at the edges of the thinned die, and a razor blade is used as a pressure point in order to cleave the die into 3 separate chips (see Figure 3.21 for cleave locations). These cleaves serve to separate devices from each other, and also create one of the laser facets for the laser components.

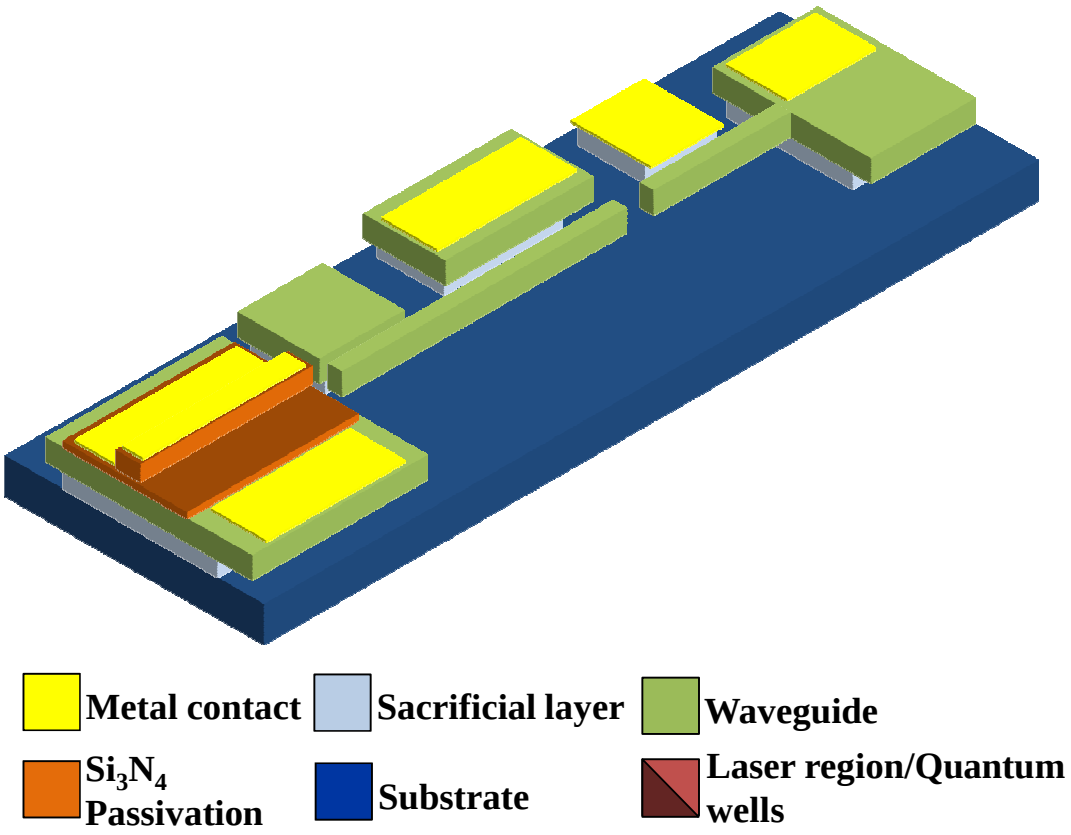


Figure 4.9. Step 9: Wafer thinning, cleaving and sacrificial layer removal.

Figure 4.9, Step 9: To create the moveable MEMS structure, a wet etch is needed to undercut the waveguide structures and create moveable devices. A selective etch of H_3PO_4:H_2O_2:H_2O is used to only etch InGaAs and InGaAsP, releasing the InP waveguides and cantilevers from the underlying substrate. The samples are dehydrated in subsequent baths of ultra-pure methanol and remain in this liquid until CO_2 critical point drying in order to prevent stiction.

The final step in the process flow utilizes CO_2 critical point drying to prevent premature stiction of the released materials. The CO_2 critical point dry process circumvents the gas-liquid phase transition, sublimating liquid CO_2 and drying the sample without the formation of a gas-liquid interface which would otherwise destroy

suspended portions of the sample due to surface tension forces. The completed samples are mounted to a copper sample holder using indium-containing solder in order to provide thermal contact to the underlying metal heat sink.

Unit process developments

As the above process flow indicates, there are a number of steps in the process which needed to be developed in order to realize these devices. Each unit step in the process was developed independently, and then in sequence with the rest of the fabrication process in order to verify compatibility of processing techniques. The following section outlines each of the fabrication processes in detail.

4.1.1 Photoresist processing

The processing of photoresist is one of the most critical aspects of the fabrication process due to its direct influence on the geometry of resulting masking patterns. Any imperfections in the photoresist will transfer into the underlying material. The bulk of the fabrication utilizes positive i-line resist (325 nm UV radiation) exposed using a 5X magnification stepper lithography tool (GCA). Negative resist was utilized for metal "lift-off" processes.

4.1.1.1 Photoresist background

Photolithography is the most common patterning method available for microfabrication. UV light is used to create a pattern of reacted and unreacted areas in a UV-sensitive polymer film called photoresist. The difference in reactivity is taken advantage of during subsequent development steps, where material is then either

added to or removed from these open areas. Negative photoresists cross-link when exposed to UV radiation and development removes unreacted (masked) regions. Conversely, positive photoresists become more reactive after UV exposure, and unmasked areas can be removed. To define various regions, photolithography processes use a patterned mask comprised of transparent and opaque regions. Using an optical projection system, this pattern is illuminated onto a photoresist coated substrate.

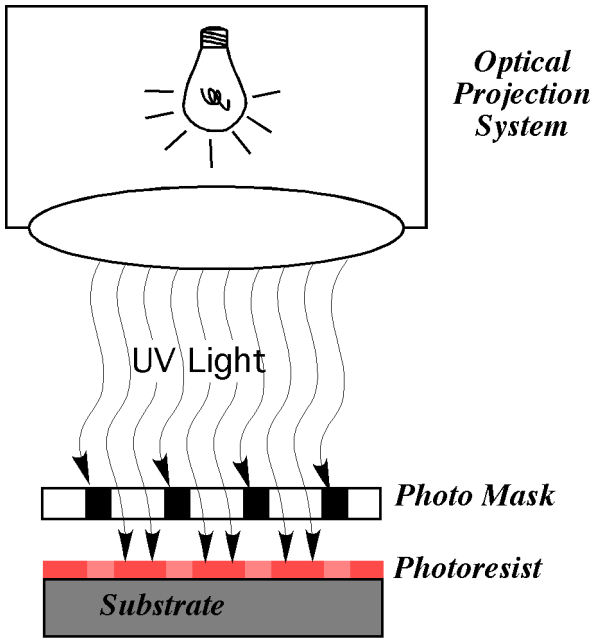


Figure 4.10. Typical components used in photolithography [190].

Photoresist coating is performed using a spin-coating tool which produces a thin, uniform film of the photoresist on the surface of the wafer. A particular spin speed is chosen to achieve the intended film thickness for a given photoresist viscosity. After the photoresist is spun onto a substrate, thermal energy is used to initiate the evaporation of solvents from the resist ("baking"). Each photoresist has a

tone (positive vs. negative), range of obtainable thicknesses, and specific baking profiles for optimal pattern transfer resolution and chemical resistivity.

The desired patterns are first designed as opaque and transparent regions on a glass plate called a photomask. In a simple contact lithography system, this photomask is placed into direct contact (or close proximity) to the photoresist-coated substrate. In projection lithography systems the photomask is mounted into an optical projection system where an image of the mask is reduced and focused via lenses or mirrors onto a semiconductor wafer coated with photoresist. Utilizing projection systems provides better pattern transfer due to the lack of physical contact with the photoresist surface and can obtain higher resolutions due to the reducing effect of the focusing optics.

After exposure, the photoresist coated substrate is submerged in a Tetramethylammonium hydroxide (TMAH) based solution to dissolve exposed (positive tone) or unexposed (negative tone) areas of the photoresist, revealing the photomask pattern that was exposed onto the surface. Both the optical projection system and photoresist chemistry are highly engineered to achieve high resolution and high repeatability within the photolithographic process.

4.1.1.2 Positive photoresist

Upon exposure to light, the solubility of a positive photoresist increases due to polymer chain scission. Common formulations of positive photoresists have included diazoquinone ester (DQ) as a sensitizer in a novalac resin (phenol formaldehyde resin) (N). Such formulations are referred to as DQN resists. The positive resists used were both variants of the DQN photoresist chemistry. These positive resists were

chosen because of the higher resolution capabilities than negative resists, the ease of stripping the material after processing, and tendency for vertical profiles as opposed to undercut. Positive photoresists require an additional coating treatment of hexamethyldisilazane HMDS solution when spinning on a silicon-containing substrate (such as the SiO_2 and Si_3N_4 hardmasks for this process flow) before the photoresist spin coating in order to promote adhesion.

4.1.1.3 Negative resist & Lift-off

Upon exposure to light, the solubility of negative photoresists decreases due either to cross-linking of the polymer chains or a photochemical reaction. Many polymers will cross-link when exposed to light. Common types of negative resist include chemically amplified epoxy or vinyl derivatives. The purpose for negative resists in this project are for performing lift-off of metalizations for contact pads.

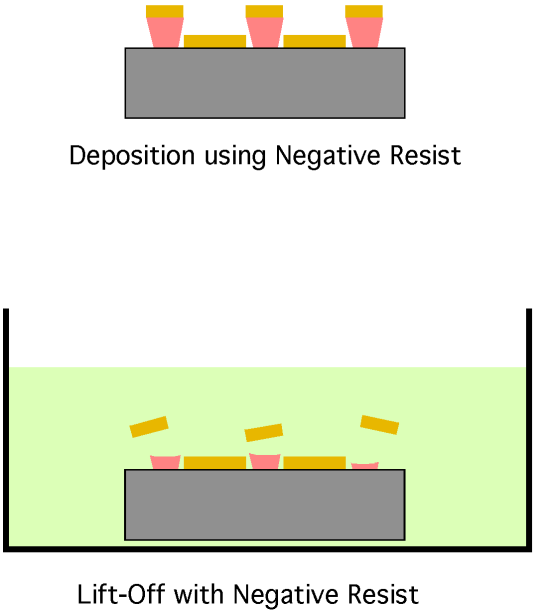


Figure 4.11. Diagram illustrating the lift-off procedure for negative photoresist (modified from [191]).

Lift-off is performed by submerging the substrate (covered with the exposed photoresist and deposited layers) into a solvent bath (see Figure 4.11). The solvent

dissolves the photoresist layer thus causing the deposited layer on the photoresist surface to float away. For this to work properly the deposited layer must be discontinuous at the edges of the opening in the patterned photoresist. Therefore the photoresist sidewall profile should be undercut. For this reason, negative photoresists work best for lift-off applications inasmuch as they inherently have undercut profiles. Some, like those used in this work include dyes which encourage exaggerated undercut profiles specifically designed for lift-off.

4.1.1.4 OiR 906-10 characterization

Fujifilm OiR 906-10 is a standard positive novalac resin-based i-line photoresist with a <0.34 µm resolution and a high resistance to wet chemical etching. The process designed for this work utilizes a nominally 1.2 µm thick film. This photoresist is used for only one step in the fabrication process: the first photolithography pattern which defines deep trenches for electrical isolation, etched laser facets, and waveguide coupling gaps in one step. Due to the very deep etch required for the ICP step that this photoresist pattern defines, the sidewall verticality is of utmost importance, more so than the resolved critical dimension. The impact of mask verticality is explained in more detail in sections 4.1.3.1 and 4.1.4.1.

Measurements of exposure dose-to-clear for 906-10 photoresist in the lithography system are performed as a part of routine process monitoring in order to determine the amount of energy required to cause all of the photoresist to develop away. This optimization procedure produces a sinusoidal “swing curve” where development time will be related to the photoresist thickness. This variation is directly related to the reflection of light from the substrate and photoresist surfaces,

causing potential standing wave and interference effects within the photoresist itself; an illustration of this is shown in Figure 4.12. The swing curve data reveal regimes where small variations in the photoresist thickness due to uncontrollable or random environmental effects will be least likely to impact final development time. Practically speaking this means that one aims to target their photoresist process to reside at the troughs or peaks of the swing curve.

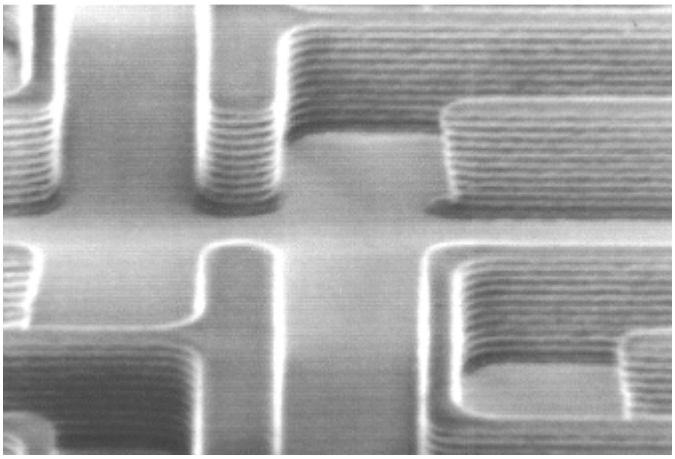


Figure 4.12. SEM image of corrugations in the photoresist sidewall due to standing waves [192].

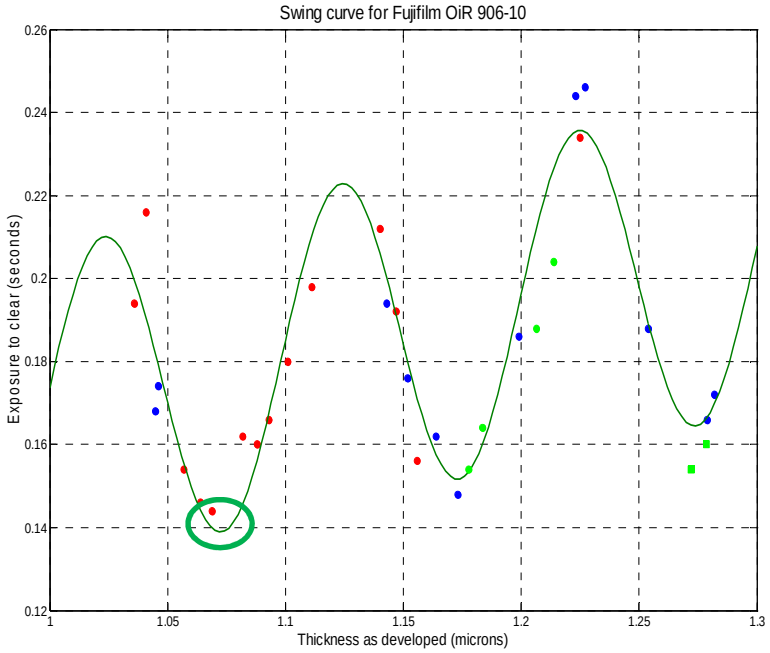


Figure 4.13. Swing curve of Fujifilm OiR 906-10 performed at LPS by J. Hryniewicz and P. Apiratikul. Green circle indicates thickness target chosen for this process.

Referring to the swing curve measurements performed in-house at LPS reproduced here in Figure 4.13, an optimal thickness of about 1.0-1.075 µm, corresponding to a spin speed of 3200 rpm, was chosen for this photoresist. The film thickness/spin speed relationship was determined empirically by measuring photoresist thickness as a function of spin speed. Consistency of film thickness is important for the final mask definition, however it was found that exposure time played the largest role in the final mask patterning, both in controlling critical dimension and sidewall angle. This parameter was varied due to the high level of control it provides during the lithography process compared to other factors. Control of critical dimensions was less of a concern in this step of the process and was deemed sufficient if the whole pattern was developed through and correctly transferred to the underlying material.

All experiments were performed on a substrate of InGaAs material coated with 1.4 µm of SiO_2 just as will be encountered in actual device fabrication. Using this substrate is important due to how the exposure of the resist is influenced by the material directly beneath the photoresist. Experiments varying the exposure time of the photoresist were performed, and cross-sectional SEM measurements of the exposed and developed photoresist were performed to assess the exposure time which yielded the most vertical resist profile (Table 4.1). Transfer of these profiles via RIE was also tested in parallel and was found to be relatively insensitive to the sidewall angle. These results will be detailed in section 4.1.3.1.

Table 4.1. Photoresist angle and resulting transferred SiO2 angle with respect to exposure time.

Exposure time	Photoresist angle	SiO2 mask angle
0.432	80.5	88.1
0.54	83.8	89.3
0.594	84.5	89.5
0.648	84.4	87.2
0.702	85.1	89.6

The final exposure time of 0.702 seconds with the projection lithography system at LPS was deemed as the most vertical profile. The results from this experiment were only partial to the complete development, and the final RIE transfer was used as a metric for the final parameters, not only the photoresist profile. The detailed photoresist recipe can be found in Appendix A.

4.1.1.5 OiR 908-35 characterization

Subsequent positive photoresist patterns after the first ICP etch process require a thicker formulation of the OiR 906-10 positive photoresist, and thus OiR 908-35 was used. OiR 908-35 is a more viscous formulation of the OiR 906-10

photoresist, and thus maintains the same photosensitive processes consistent with all novalac resin photoresists. Thicker photoresist is needed due to the large variations in surface topography; thinner photoresist will not cover the trenches and steps in the underlying substrate leading to insufficient protection during pattern transfer. A SEM of the consequences of this poor coverage is shown in Figure 4.14. Working with this thicker photoresist comes with another set of challenges, particularly in the resolving of critical dimensions and features. The mask design for two of the three layers utilizing this thicker photoresist are forgiving in terms of their large critical dimensions (laser ridge mask #2 – 3 µm, quantum well mask #3 – 30 µm), however waveguide mask #4 pushes the limits of the photoresist and the processing tools with critical dimensions of 1 µm lines and spaces. This coupled with the >3.6 µm topographical variation across the substrate make this step challenging.

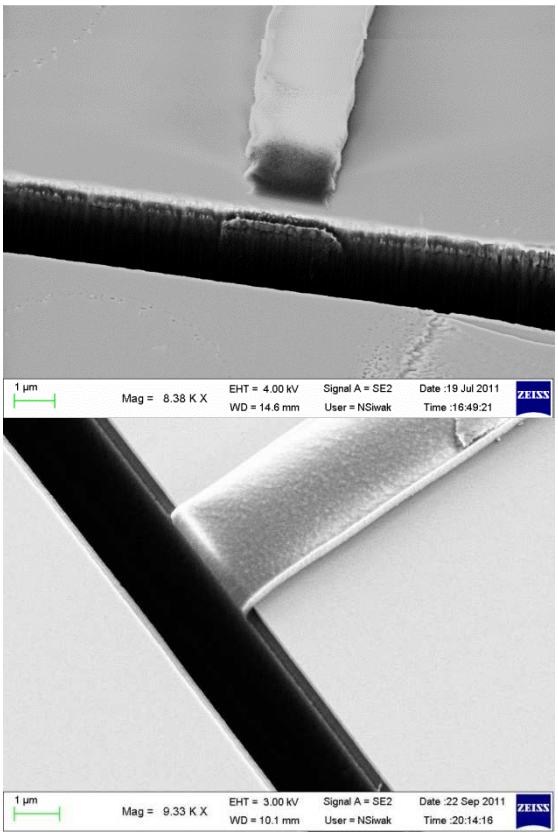


Figure 4.14. SEM showing the effect of poor photoresist coverage using OiR 906-10 (Left) and good photoresist coverage using OiR 908-35 (Right) on the resulting SiO_2 hardmask pattern. Notice the sloped profile of the poor coverage example.

Spin coating of this photoresist is performed using the same spin speed, 3200 RPM, corresponding to a 3.6 µm thick film. Cross-sectional SEM confirms that this thickness is sufficient to protect the critical features of the die; however some areas still suffer from less than perfect coverage due to the very large aspect ratios of the etched patterns (see Figure 4.15), particularly with the corners of wide and deep trenches. Since the locations of this incomplete coverage are non-critical, this aspect was not optimized. In order to achieve better coverage in the future, multiple spin-coats of the photoresist can be performed, spray-coating of the photoresist, or even thicker formulations of positive resists can be employed.

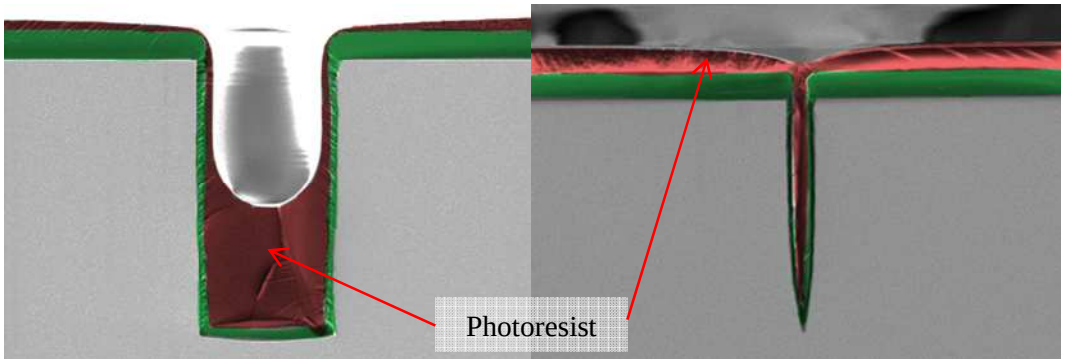


Figure 4.15. SEM images of OiR 908-35 spin coated over varying etched geometries (colored red), notice how the corner of some areas are still nearly unprotected. Green areas are SiO_2 coatings and grey areas are the underlying substrate.

As with the previous recipes, exposure time was varied to find the optimal recipe. Sidewall angle of the photoresist was investigated, however more importantly; the SiO_2 transferred pattern was used as a metric for an acceptable recipe. A final exposure time of 0.5 s was arrived at which balanced sidewall angle and resolved features in the final resulting SiO_2 hardmask.

4.1.1.6 AZ-nLOF 2035 characterization

Negative photoresist was used in this process in order to pattern the metal pads for electrical contacts. Both *n*-type and *p*-type metallization schemes require multiple metals, making wet etches impractical and the use of metal lift-off a necessity. Many lift-off photoresists exist which provide a negative undercut profile inherently. AZ-nLOF 2035 photoresist was chosen for this application due to the thickness of this formulation and its very large negative angle sidewall profile.

A spin speed of 3000 rpm was used during spin coating, corresponding to a 3.5 µm thick film. This thickness is important due to increased topographical variation and very thick metal deposition for *n*-type metals. Since this is one of the last photoresist steps carried out after all etching is completed, total height variation is approximately 7 µm across an 18×18 mm die and coverage is problematic with resist that is any thinner than 3.5 µm. Standard lift-off processing dictates that your photoresist layer is at least 2x the thickness of the intended metal layer to be lifted off. The metal deposition step for *n*-type metals includes a 1.2 µm thick gold deposition capping layer, necessitating this thick photoresist layer.

Exposure time of the photoresist was varied in order to obtain the best results. Nearly all exposures that developed cleanly yielded an undercut that was sufficient for clean lift-off, the best lift-off patterns resulted from the exposure times that just exceeded the exposure threshold for clean development; overexposure caused the photoresist to be more chemically resistant to the NMP-based resist stripper causing poor lift-off.

The lift-off procedure will be described in detail in section 4.1.5.3, and the detailed photoresist processing recipe can be found in Appendix A.

4.1.2 Dielectric deposition

Plasma enhanced chemical vapor deposition (PECVD) is a processing technique for the deposition of materials which utilizes high-energy plasmas of precursor gasses that react at a sample surface causing deposition of different dielectric films. The disassociation of gasses in the plasma chamber, the substrate material, substrate temperature, RF coil powers which create the plasmas, and the specific gas ratios used all affect the final material deposited. Due to the very complex interdependent relationship of the deposition parameters, material deposition parameters are determined empirically via deposition experiments and parameter variation rather than theoretically.

PECVD is important in this process as it allows for relatively low-temperature deposition of dielectric films, since the energy needed to drive the surface reactions which result in deposited films is provided via the RF source and not substrate/gas temperature. This is particularly critical for III-V devices which may intermix upon exposure to high temperatures such as quantum wells.

A number of dielectric depositions were performed throughout this fabrication process for hard plasma etch masks and device passivation coatings. All dielectric depositions were performed using a Novellus Concept One PECVD tool. This tool is unique in that there are two RF coils present which can couple into the plasma, providing more control over the density of the deposited dielectric films.

Additionally, the Novellus PECVD is a 5-station deposition tool which contains 5 separate gas-inlet areas that the sample is rotated into throughout the entire deposition process. This reduces film deposition non-uniformity and defects which may be introduced via a non-ideal plasma chamber geometry. For all etch masks 1.4 µm thick SiO_2 was used, and 2000-7000 angstroms of Si_3N_4 was deposited for device passivation.

4.1.2.1 SiO_2 Deposition

The PECVD process for depositing SiO_2 disassociates silicon and oxygen from silane and nitrous oxide constituent gasses in order to allow them to recombine into SiO_2. This specific recipe also introduces additional nitrogen into the gas mixture to increase the surface energy of the substrate due to ionic bombardment, promoting the growth of SiO_2 here. This precise mixture of gasses at an established plasma energy will cause the deposition of non-stoichiometric SiO_2 upon the surface of the die within the chamber to occur. A well-tuned deposition PECVD recipe utilizing these three gasses was used to deposit the SiO_2 materials (See Appendix A) at a thickness of 1.4 µm.

Planar dielectric coverage is not the only aspect of the dielectric that needs to be measured for these devices, but due to the large topographical variations, coverage of the dielectric inside of trenches and on the sidewalls of ridges is important to control and measure. The deposition thickness along sidewalls was measured to be anywhere from 100-75% of the planar deposition thickness, with close to 50% reduced deposition only seen at the bottom of high aspect ratio trenches (7 µm deep, 1 µm wide). These values were measured using test depositions along various points

in the fabrication process and performing SEM crossection measurements. For every hard-mask step, only coverage near the upper corners of the etched surfaces are essential, and are well protected with this deposition thickness.

4.1.2.2 Si_3N_4 Deposition

The PECVD process for depositing Si_3N_4 disassociates silicon and nitrogen from silane and ammonia constituent gasses in order to allow them to recombine into the intended Si_3N_4. As with the recipe for SiO_2, nitrogen is introduced into the gas mixture to increase the surface energy of the substrate and facilitate the growth of Si_3N_4 at the substrate surface. This precise mixture of gasses at an established plasma energy will cause the deposition of non-stoichiometric, low-stress Si_3N_4 at the die surface. A standardized deposition recipe (detailed parameters available in Appendix A) is used in order to deposit Si_3N_4 for the laser passivation step.

A similar determination of sidewall coverage is performed for Si_3N_4 deposition as with the SiO_2 process, however only the ridge sidewall coverage is necessary to consider for this step since the function of the Si_3N_4 deposition is to passivate the laser ridge of the device. Cross-sectional measurements of samples with this material deposited after etches were performed showing a 70% reduction along the ridge height, with a smaller deviation for more shallow ridges. A SEM crossection showing the Si_3N_4 passivation coating a laser ridge is shown in Figure 4.16.

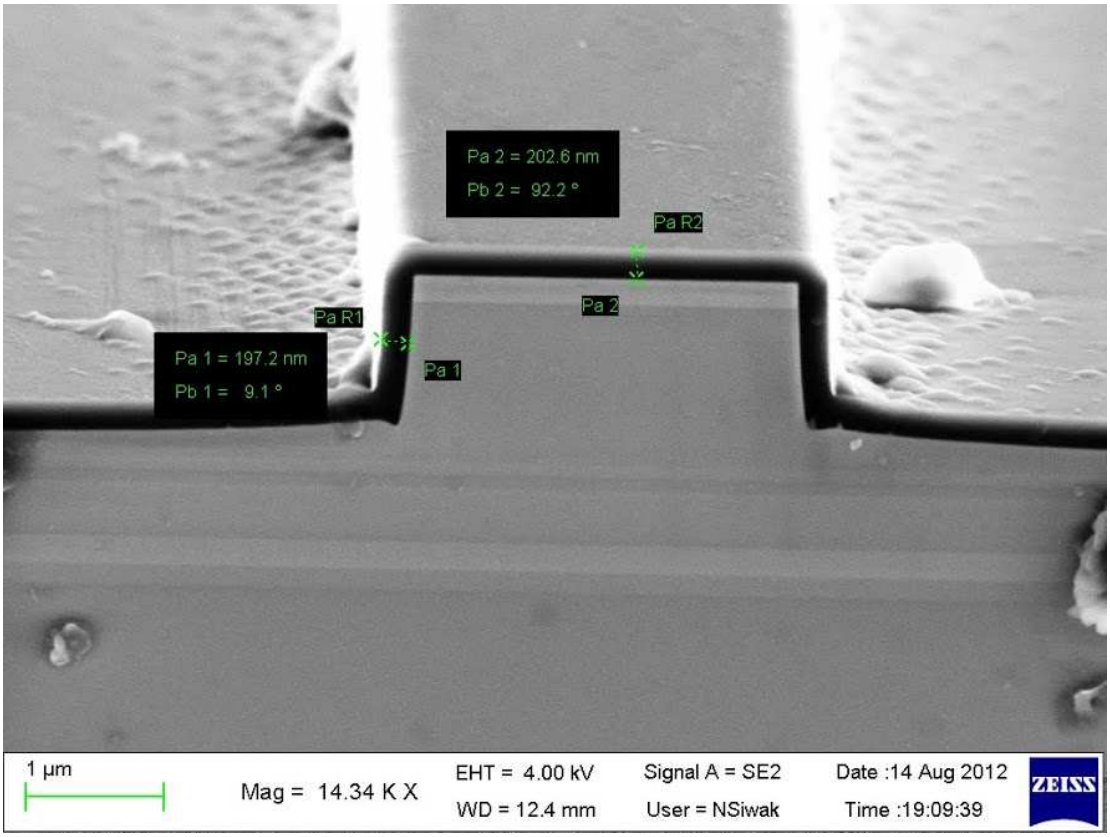


Figure 4.16. SEM crossection of laser ridge, showing Si_3N_4 passivation coating.

4.1.3 Reactive Ion Etching (RIE)

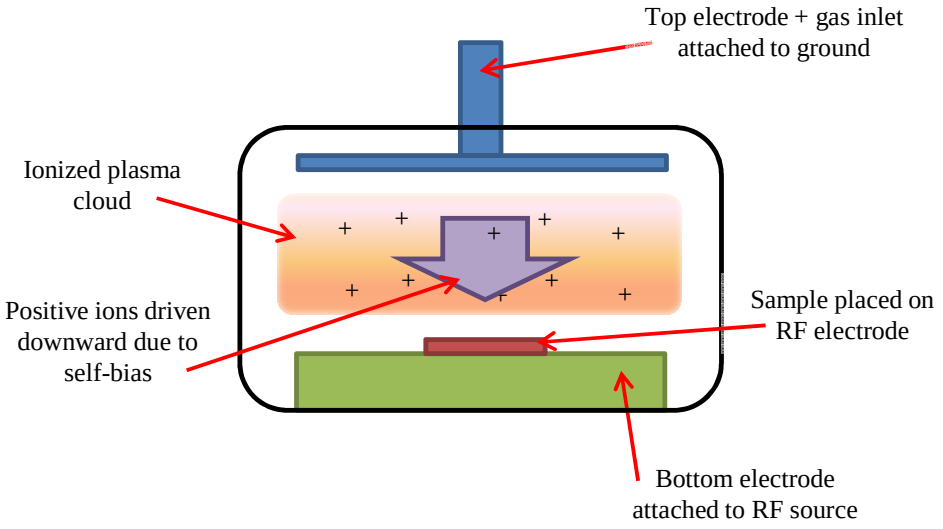


Figure 4.17. Schematic diagram of reactive ion etching (RIE) chamber.

Reactive ion etching (RIE) is a very common technique for material removal that utilizes ionized gasses to etch surfaces. Depending on the gas mixtures used and

the plasma power introduced to the chamber gasses, different materials can be targeted for removal. RIE operates by ionizing a mixture of gasses inside of a vacuum chamber with a pair of electrodes that have high frequencies induced on them, as shown in Figure 4.17. As the electrons are stripped from the atoms in the gas cloud, the cloud becomes positively charged. At the same time the electrons adsorb into the sample electrode, negatively charging it. This "self-bias" is generated, causing the positively charged ions to be accelerated towards the sample surface. The conditions of this ion acceleration, density, and species depend on any number of factors within the chamber, including: sample size, chamber pressure, gas flow ratios and species, RF power, and chamber cleanliness. As these ions strike the sample surface they both physically attack the surface, and react with the materials. These reactions produce chemical byproducts which are removed from the chamber via vacuum pumps, or are re-deposited on the sample and the chamber walls. These byproducts can be both harmful and helpful depending on the tuning of the process. Too many byproducts adsorbing to the sample surface can create micromasking effects or stop the etching process all-together, but well controlled adsorption can serve to protect sidewalls during the etch, increasing anisotropy of the etching process and creating more vertical etching profiles.

Due to the highly directional ion bombardment of the surface as a result of the self-bias, and the potential polymer byproducts, the resulting etch can be considered to be anisotropic when performing shallow etches. RIE is used extensively in the established process flow due to its convenience, material selectivity, anisotropic

etching of dielectrics, and effectiveness at cleaning off organic materials without attacking the underlying substrate.

4.1.3.1 SiO_2 pattern transfer (SiO2PT)

SiO_2 was used as a hardmask for later etches (discussed in section 4.1.4). A mixture of CHF_3 and O_2 gasses are used to perform this etch. The CHF_3 gas addition provides both fluorine radicals which chemically attack the SiO_2 material, F^+ ions which bombard the surface, and C compounds which provides a flouro-polymer generating passivation component. This polymer generation helps to increase the anisotropic qualities of this etch, passivating newly etched sidewalls during the etch process. The addition of O_2 assists in preventing buildup of this carbon containing passivation by etching it slightly while also increasing the F radical and F^+ density. Ion bombardment of the surface encourages the etching of horizontal surfaces while vertical sidewalls remain untouched, causing a marked increase in etching verticality. Verticality of this etch is of prime importance as the sidewall angle of the resulting etched surface directly impacts the future deep inductively coupled plasma (ICP) etch.

The developed baseline recipe provides a high quality, vertical etch provided the photoresist etch mask is also vertical. As mentioned in section 4.1.1, the transfer of the photoresist mask was verified using this RIE method (see Table 4.1 and Figure 4.18). Notably, the etch transfer was vertical for nearly all photoresist angles, excluding the extrema, meaning that the selectivity between SiO_2-Photoresist was very high. Details of the RIE etch recipe can be found in Appendix A.

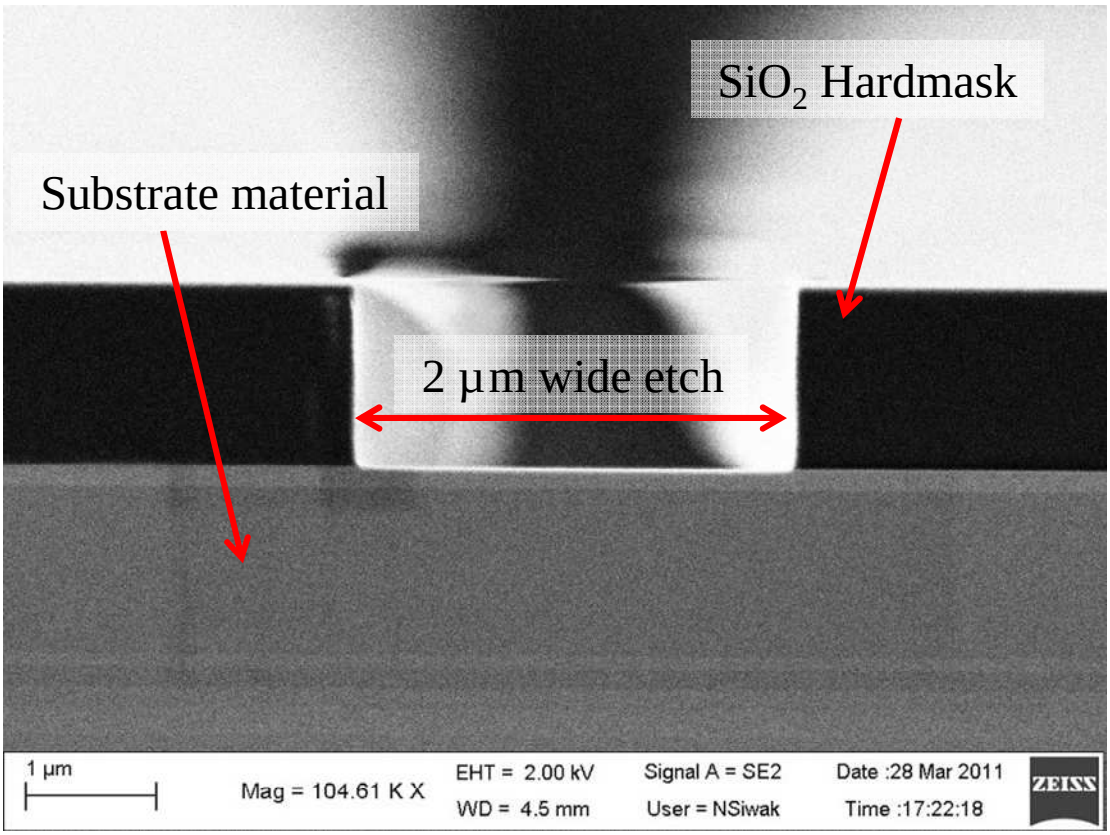


Figure 4.18. SEM image of a transferred SiO_2 oxide hardmask.

4.1.3.2 Si_3N_4 pattern transfer (DIELCUT)

Si_3N_4 was deposited on the substrate as a laser passivation layer to reduce parasitic surface currents and provide electrical isolation for the top ridge contact. SF_6-O_2 plasmas generate high F-radical densities and generally produce higher rate and more isotropic etches. Etching of this layer is less critical in terms of its sidewall angle, so a basic recipe utilizing SF_6-O_2 was employed for high-rate Si_3N_4 etching using the same RIE system. Details of this recipe can be found in Appendix A: Processing Recipes.

4.1.4 Inductively coupled plasma (ICP) etching

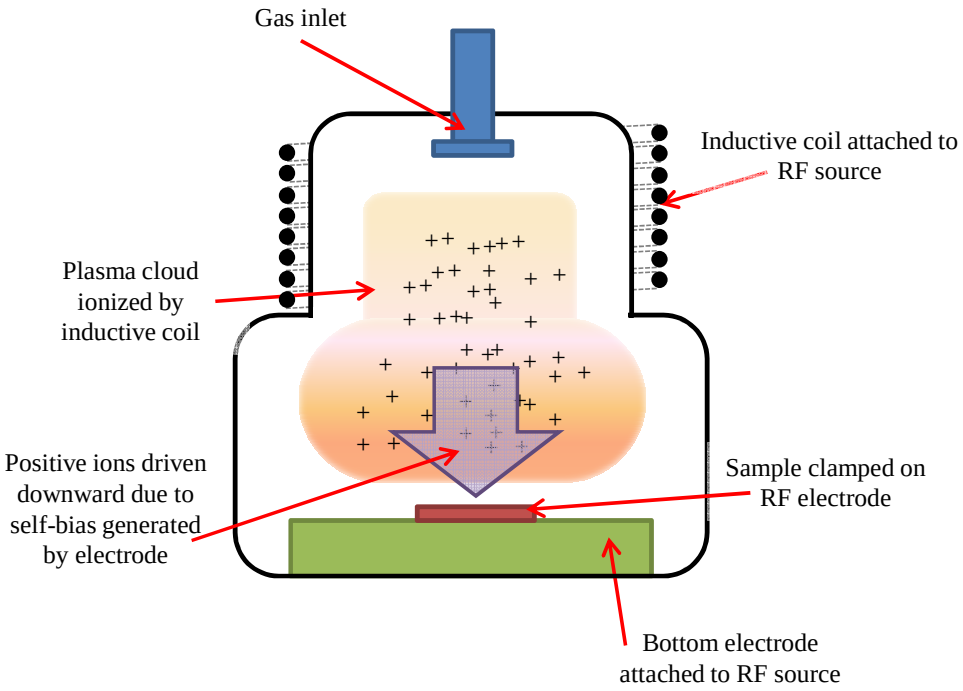


Figure 4.19. Schematic diagram of ICP etching chamber.

One of the primary etching mechanisms which enables the high aspect ratio, high sidewall smoothness, and high speed etches required in the fabrication of this microsystem is the use of inductively coupled plasma (ICP) etching. ICP etching is similar to the RIE process as mentioned in the previous section, with additional components in the reactor chamber that provide more control over the etching conditions. A schematic of the ICP chamber layout is shown in Figure 4.19. Two separate RF generators are utilized to ionize the reactor gasses, one upstream coil (ICP) from the sample controlling density of the plasma (ion current), and another which creates an RF bias at the substrate surface. By separating these two RF generation units, control of plasma density is decoupled from the plasma energy. In this way, very high ion currents can be applied during the etch while keeping the ion

energies relatively low, increasing chemical etch selectivity and reducing substrate damage due to high-energy ion bombardment.

An additional feature of the PlasmaTherm 770 ICP system used in this work is a heated sample chuck. Sample temperature is particularly important when etching InP-containing compounds with Cl_2- based plasma etches, since the byproducts of the Cl_2-based etch are volatile only at high temperatures (>175°C) and will redeposit on the sample surface during the etch if temperatures are not sufficiently elevated, roughening the etched surfaces and sidewalls [193].

Two etch chemistries were utilized in this work for fast and slow etching. The faster etch recipe consisted of Cl_2-Ar-O_2 gas chemistry, with most etching a result of the Cl^+ ions. The slower recipe consisted of a Cl_2-H_2-Ar etch chemistry with a mixture of Cl^+ and H^+ ions acting in the chemical etch. The high etch rate recipe was required in order to achieve the very deep and vertical (>7.1 µm) electrical isolation trenches. The slow etching recipe was chosen for its reduced etch rate and thus higher controllability in the final etch depth. All ICP etches are performed with a blank 3 inch silicon wafer as a carrier; 18×18 mm square samples are attached to the wafer with a very thin layer of silicon vacuum grease providing mechanical stability and thermal conductivity.

4.1.4.1 High rate ICP etch Cl_2-Ar-O_2

Ionized Cl_2 gas is well known to etch III-V materials, particularly InP [194, 195], in plasma reactors. The use of ICP increases the density of the reactive species and the addition of Ar in the plasma increases the bombardment energy seen by the horizontal surfaces of the sample, increasing the anisotropic nature of the etch, as

well as removing any non-volatile compounds which may not be desorbed during the etching process. To further assist this non-volatile removal, substrate temperature is set at 175°C via the heated chuck. Setting the sample stage to higher temperatures is preferable; however there is evidence that the high RF powers associated with this recipe may induce sufficient bombardment and self-heating of the substrate to lessen the effect of a heated substrate.

It has been demonstrated in a number of papers in literature [195-199] that the carrier wafer and chamber walls being used in the reactor contribute to the etching reaction by supplying ions and radicals to the etching surface, often beneficially, passivating etched sidewalls as they are created. In this case, the silicon carrier wafer contributes silicon atoms to SiO_2 formation on the sidewall surface.

In an attempt to improve the sidewall passivation effect, O_2 was added in the etch chemistry. A number of experiments with O_2 gas flows of 0.5-1.5 sccm were performed; the smallest flow of O_2 (0.5 sccm) produced the best sidewall quality as evidenced from SEM inspection of the etched surfaces in Figure 4.20.

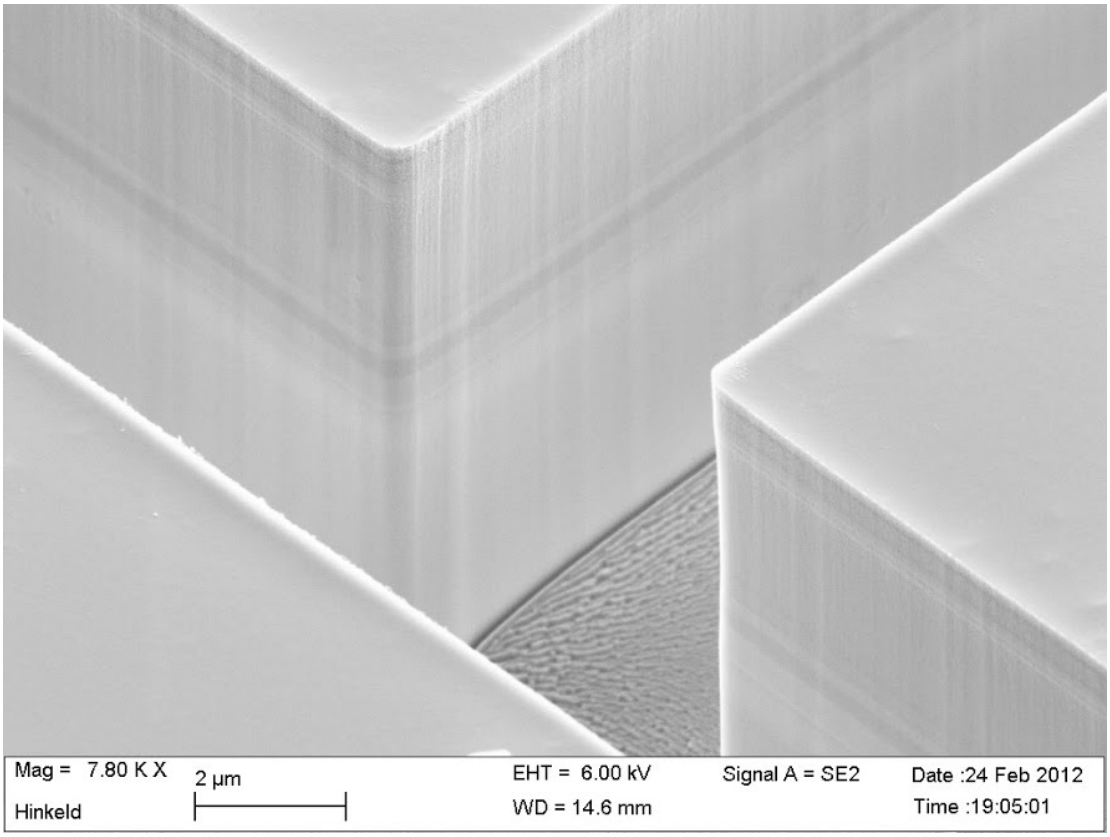


Figure 4.20. SEM of smooth deep-etched epitaxial sample.

Since etch quality and etch rate were sufficient for the work presented after these tests, no further recipe development was continued for this etch beyond etch rate measurement. The details of this "fast" etch recipe are included in Appendix A.

4.1.4.2 Slower rate ICP etch Cl_2-H_2-Ar

A slower etch rate was also pursued for this project in order to better control the etch depth of more critical steps in the process. The recipe was modeled upon the recipe reported by Rommel et al [196] consisting of a Cl_2-H_2-Ar gas chemistry plasma. This etch recipe has an increased sample temperature and reduced ICP/RF power. The result is an etch that is slightly less vertical, but still maintains very smooth sidewalls at a reduced etch rate (~50% slower). An SEM illustrating how

smooth the sidewalls are for this etch is shown in Figure 4.21. The details of the etch recipe are included in (Appendix A).

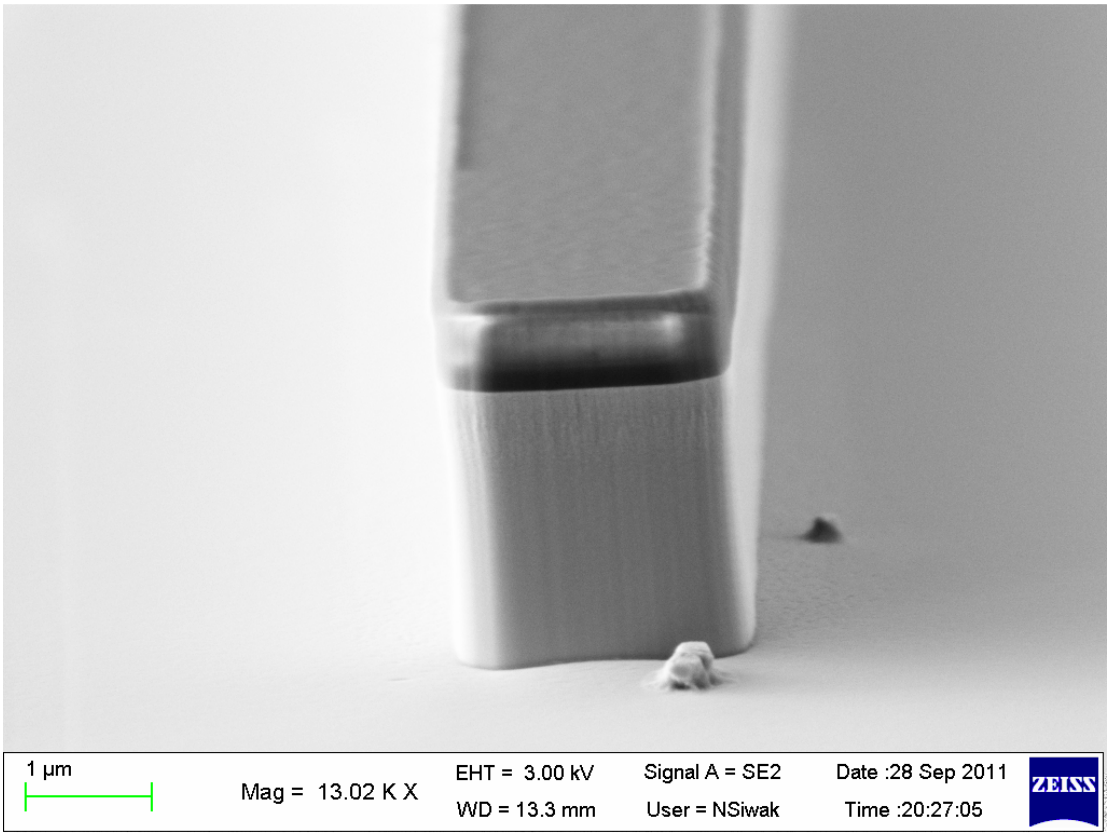


Figure 4.21. SEM image of slower etch rate with the laser ridge etch pattern. Oxide hardmask has not been removed.

4.1.4.3 ICP Etch chamber conditioning/cleaning

The ICP used for this work (PlasmaTherm 770 ICP) is a multi-user tool in which many different materials (GaAs, InAlAs, InAs, AlGaAs, InGaAs, InP, InGaAsP, InSb) at varying plate temperatures, with different etch gasses (BCl_3, H_2, Cl, CH_4) are all processed regularly. Byproducts from different etch gasses and substrate materials coat chamber walls and can affect the resulting etches negatively; introducing unwanted residues, sidewall sloping, and sidewall roughening. To compensate for this, a clean/conditioning step is performed before each of the etch sequences in order to return the chamber to a known state. The cleaning recipe

consists of a very high ICP/RF power CH_4 plasma etch and an additional O_2 plasma etch to remove any organics. The final step of the clean/condition is a standard BCl_3 based etch process run to condition the chamber walls. The details of this cleaning process are presented in (Appendix A).

Chamber condition is also closely related to how often the system is vented and manually cleaned. The etching chamber needed to be vented and opened occasionally to clean residues from the underside of the wafer clamping assembly not exposed to the chamber during the plasma clean/condition. It was observed that any chamber venting procedures occurring before etching greatly affected the drifting of etch rates, even after the standard plasma clean/condition procedure. This indicates that more or different chamber conditioning is needed after a manual venting/clean procedure. Critical etching steps are performed in light of this fact and were scheduled to be performed after extended usage periods from other users (i.e. no chamber venting/manual cleaning).

4.1.4.4 Timed etch procedure

The ICP etch tool used for this work has not been equipped with an endpoint detection system, and thus the etch depth is controlled only by the etch time. This introduces a number of uncertainties in the use of this recipe, as plasma strike and plasma stabilization times are not always consistent, onset of etching during the process is somewhat unknown (does etching begin at plasma strike time, or at plasma stabilization, etc.), and material composition strongly affects the sample etch rates. An arbitrary choice was made to use “plasma stabilization” as a measure of the onset of etching in relation to the timing of the etches. “Plasma stabilization” for these

processes is defined as the point at which the matching networks complete their tuning after plasma strike in the chamber.

It was observed that etch rates are variable through the epitaxial layer structure, with InP and GaAs containing layers etching at two different rates. This makes the targeting of various etch depths difficult via etch time only. Two look ahead travelers were used during a fabrication lot in order to compensate for any etch variability due to environmental variation, one sample of plain InP:Fe semiconductor material, and another die with the same epitaxial layer structure as the real die being fabricated. Both of these samples were the same size as a real die (18×18 mm) and were patterned along with each step of the fabrication process, so that loading and aspect-ratio dependence present in the etch will be consistent across every sample.

The procedure for establishing etch rates, and thus etch times, proceeds in a two-step process; the first step establishing the etch rate of InP-rich compounds, and the second InGaAs-like compounds (quaternary and ternary layers). The patterned InP:Fe sample is mounted on the carrier wafer using thermal grease as previously described, and etched for a fixed time. The resulting etched sample is measured with a stylus profilometer before and after the SiO_2 hardmask is removed. This allows for the measurement of the InP and the SiO_2 mask etch rates. The rates are compared with previous etch rates (if available) and the next sample is prepared for etching. The dummy epitaxial sample is mounted in the same manner as previously, the target depth is chosen based upon the current etching step to be performed. Throughout the depth of the etch, material compositions will vary depending on the layers in the epitaxial structure, the thicknesses of which are known and measured previously at

the time of growth completion. An estimated etching time is established based upon the InP etch rate calculated in the first dummy etching step and previously recorded etch rates. The etching step is then performed on the sample for this prescribed time. A stylus profilometer is used to measure the InP and the SiO_2 mask etch depth. An etch time is calculated for every layer etched throughout the measured depth, with the etch rate of InP compounds set to the value measured in the previous step and InGaAs/InGaAsP compounds both set as a single unknown value. It was found that the ternary and quaternary materials etched at similar rates to one another and thus a simplification was made to consider them as one material for etch rate calculations. This unknown is solved for and thus an approximate etch rate for the ternary and quaternary materials can be established. After each "real" die etch, the actual etch depth is measured along with the SiO_2 mask etch rate and compared with the previous value in order to monitor short-term drift of etch rates. Any corrections to the etch time are made at this stage before the next sample is etched. This initial rate determination step was found to be critical to the success of etching targeted depths to within ±200 nm through a complex epitaxial layer structure.

4.1.4.5 ICP nested etching

As previously described in section 0, the complete process flow for device fabrication consists of 4 separate ICP etching steps with varying depth requirements after one another. Step coverage of both photoresist and SiO_2 hardmasks becomes important as already discussed; however, the implications of remaining hardmask on the sidewalls of previously etched steps introduces an additional complication. After regular SiO_2 hardmask patterning, some SiO_2 overhanging material remains on the

corners of existing etch steps. This overhanging SiO_2 acts as a mask during the ICP etching step, creating unwanted overhanging material that resembles a "fence" around the perimeter of the etched steps (see Figure 4.22 and Figure 4.23).

It was found that an over-etch during the mask pattern of up to 30% was required in order to sufficiently remove overhanging material and minimize the appearance of this fence in resulting steps. This effect was observed for every hardmask patterning step after the first etch was completed.

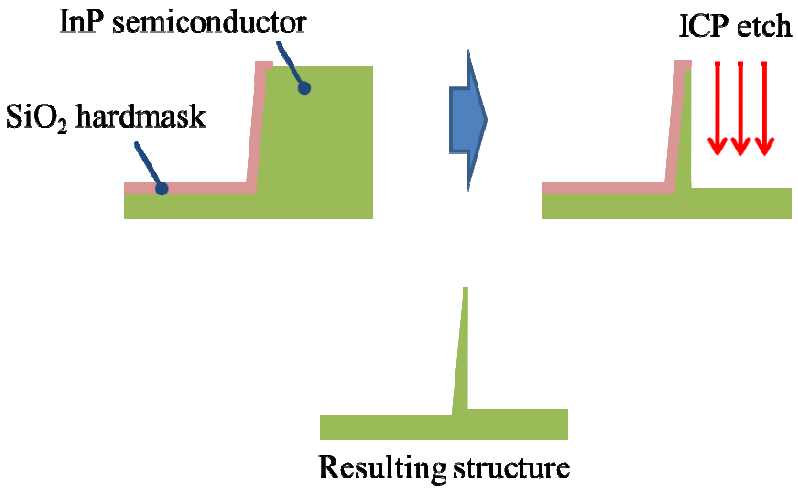


Figure 4.22. Diagram illustrating the effect of sidewall oxide hardmask on nested etching

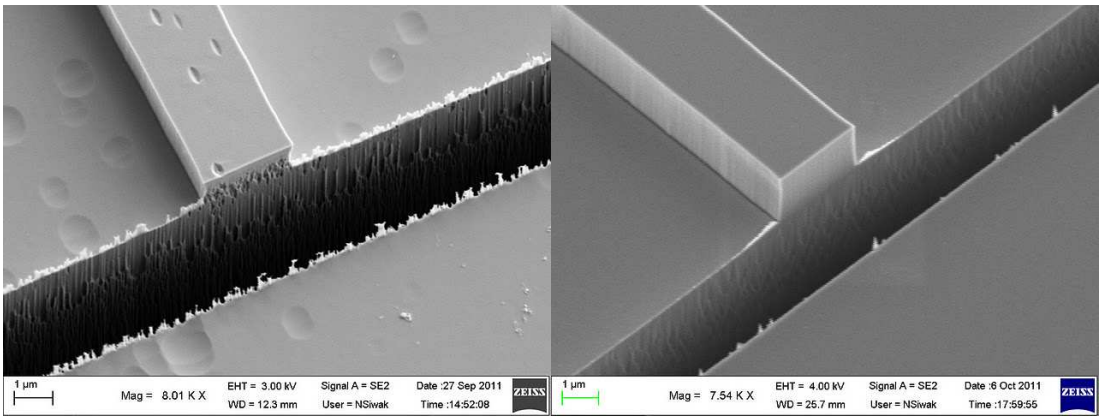


Figure 4.23. SEM images illustrating the fence structure Left: residues resulting from a poor overetch of the oxide hardmask, and Right: Cleaner edge due to proper hardmask overetch.

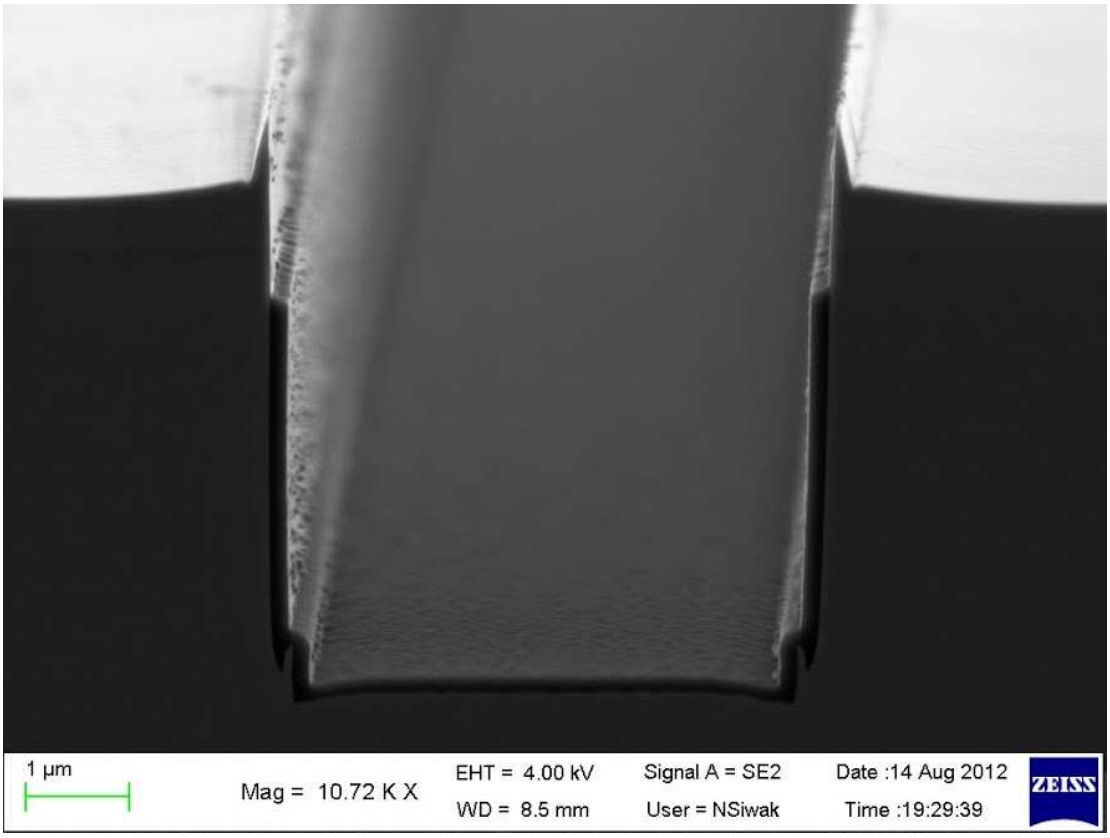


Figure 4.24. SEM image illustrating a crossection of fence residue.

4.1.4.6 Etching targets

The 4 etches needed in this fabrication process have varying depth requirements depending on the step. The required etch depths are illustrated schematically in Figure 4.25, and in tabular fashion in Table 4.2.

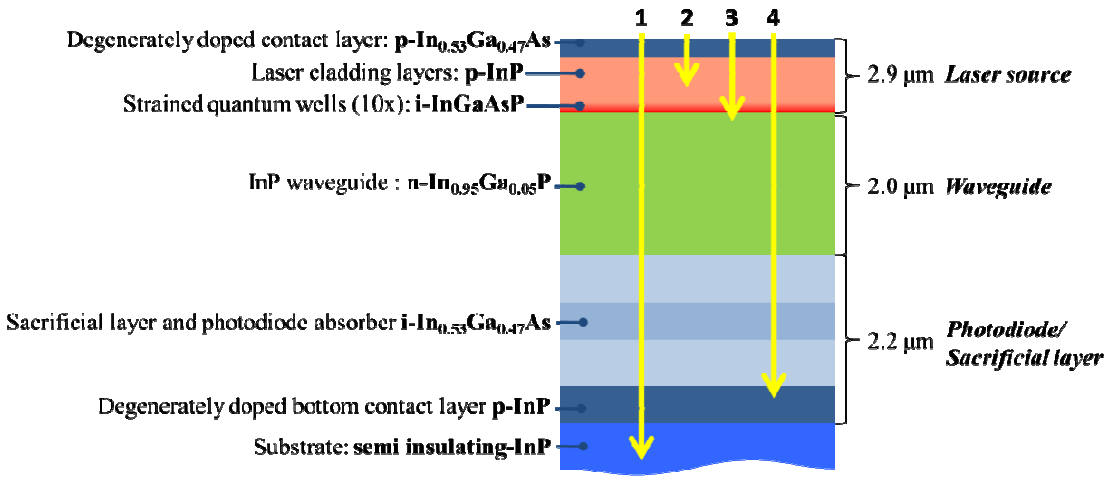


Figure 4.25. Diagram illustrating the 4 etches employed and their depth targets relative to the original epitaxial layer structure. 1) Trench etch, 2) Ridge etch, 3) Quantum well etch, 4) Waveguide etch.

Figure 4.26. Top-down colorized SEM of entire device, with color coated depth indication after each etching step. Red: Unetched depth, Yellow: Trench etch (#1), Purple: Ridge etch (#2), Blue: Quantum well etch (#3), Green: Waveguide etch (#4).

Table 4.2. Etch targets

Etch #	Mask layer	Target depth (µm)
1	Trench	7.1
2	Ridge	1.375
3	Quantum well	2.48
4	Waveguide	5.91

Etch 1 utilizes the high etch rate ICP etching step in order to achieve the deepest etch with the least amount of mask erosion possible as to achieve smooth etch sidewalls. This etch is slated to etch through the entire epitaxial material stack in order to create electrical isolation between the integrated components. Sidewall smoothness is critical for this etch since it also constitutes the etched laser facet and cantilever waveguide gap.

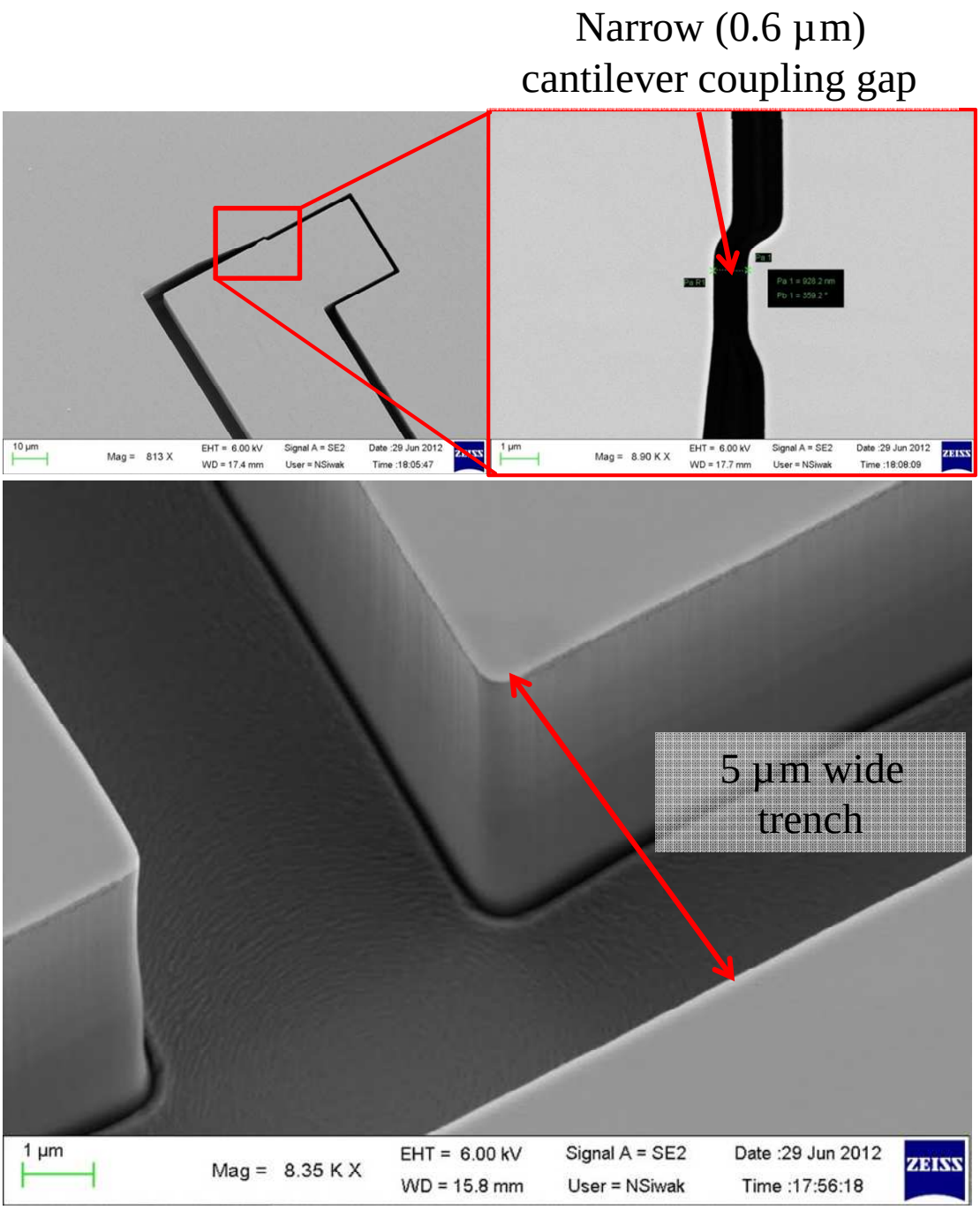


Figure 4.27. SEM images of the deep ICP trench etch.

Etch 2 utilizes the slower ICP etch and is used to create the ridge for the laser structure. This etch has less requirements on its depth and serves to create the lateral confinement of the laser optical mode. The sidewall smoothness of this etch is important to reduce the loss in the lasing mode.

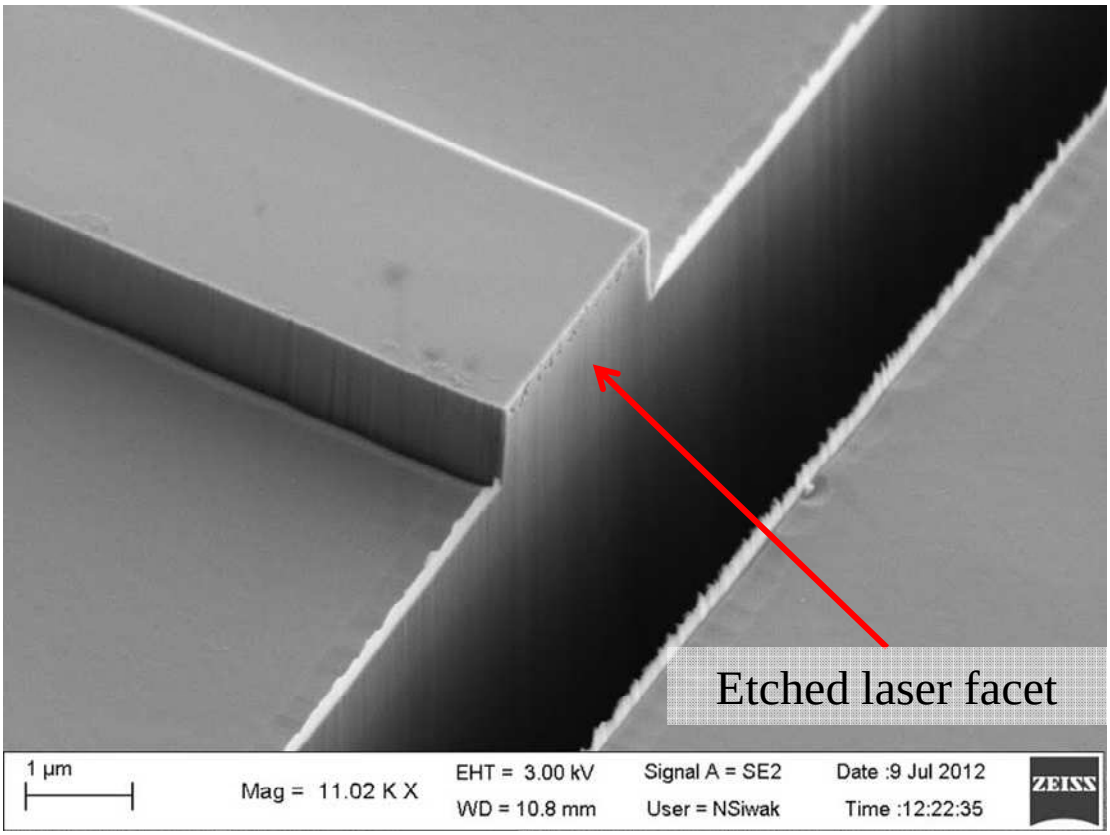


Figure 4.28. SEM image of laser facet with the defined laser ridge.

Etch 3 uses the slower etch recipe to remove the remaining active components of the laser region, removing the quantum wells across the die except in the active region, and opening the buried *n*-type laser contact. Since this layer is targeting a buried contact, its etch depth is critical. Sidewall roughness is less of a concern for this patterning step as the etched sidewall is far away from the laser gain region.

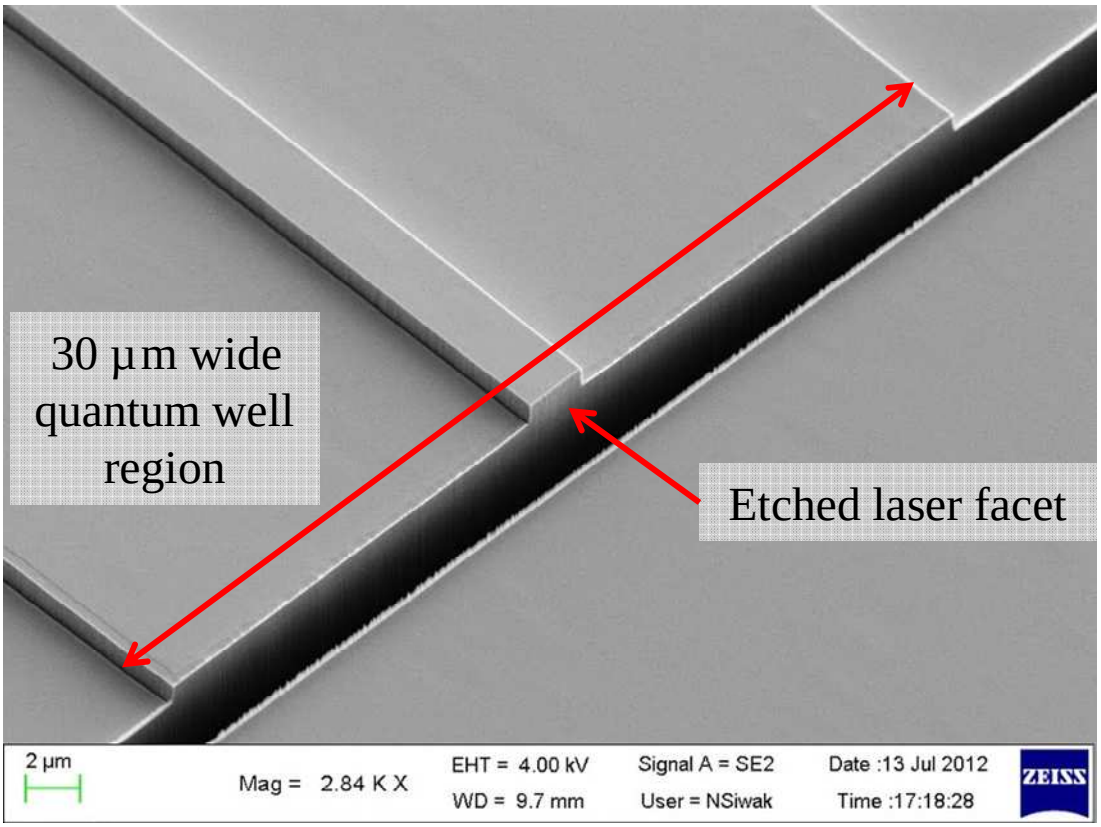


Figure 4.29. SEM image showing the quantum well etched region centered on the laser ridge.

Etch 4 again uses the slower etch to pattern all of the waveguide/photodetector structures. This etch also is meant to open the buried *p*-type contact for the photodiode components, and it also needs to completely etch through the waveguide and upper half of the sacrificial layers. Significant aspect-ratio-dependent etching (ARDE) is seen when performing this etch, making it difficult to realize. Large areas of 100's of microns square need to be etched in order to contact the buried contact layer, while trenches as narrow as 1 µm need to be etched as well. To address this issue, the large, open areas of the pattern are etched as deep as possible, allowing the very narrow regions to achieve sufficient depth. The depth of narrow regions is important for the success of this fabrication step in order to facilitate the undercut and release of movable structures; insufficient etch depth will lead to fixed cantilevers

that are still attached to the main bulk of the waveguide layer. Care must be taken however, to know the etch rates to a high degree of certainty as overetching the large areas will proceed beyond the buried contact.

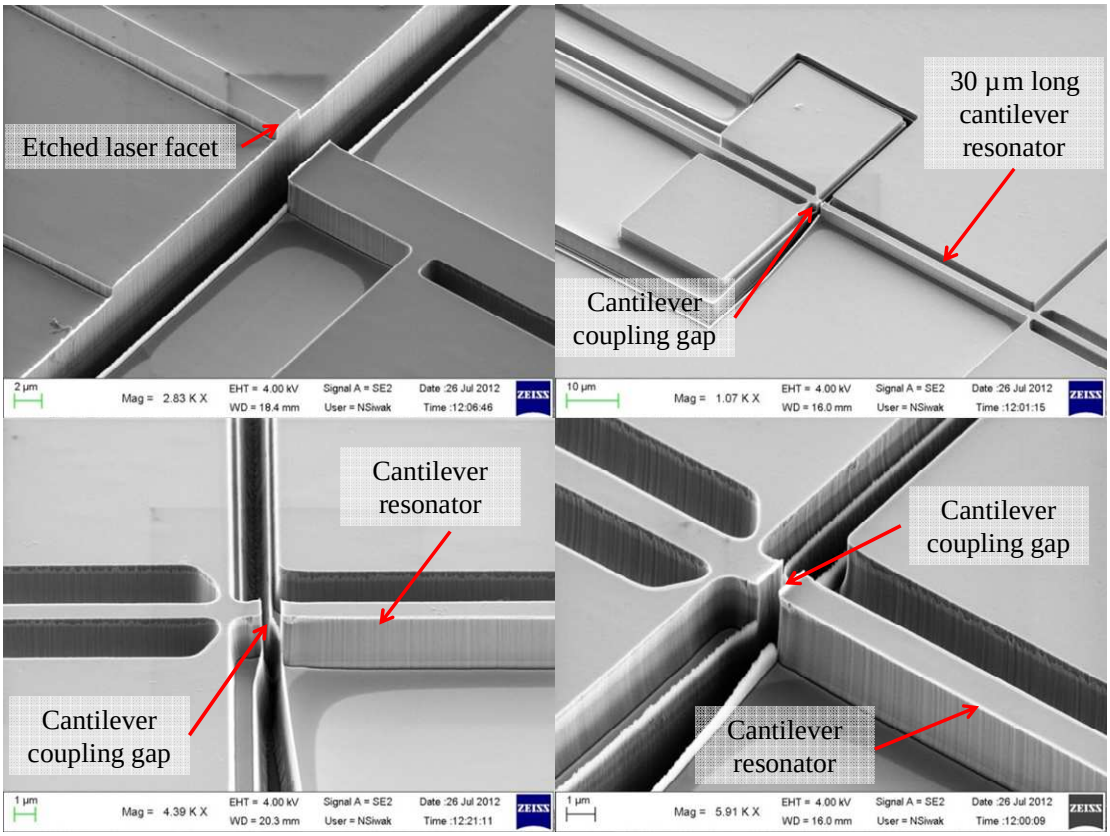


Figure 4.30. SEMs of waveguide etched patterns focusing on the laser facet and coupled waveguide areas (Top left), the cantilever structures (Top right), and around the cantilever gap defined by the first trench etch (Bottom row).

4.1.5 Metal contact deposition

Two metalizations were employed to create ohmic contacts to *n*-type and *p*-type semiconductor materials for this process flow. *P*-type metallization is a tri-layer of titanium – platinum – gold, and is un-annealed. *N*-type metallization is a 5-layer metal stack consisting of Nickel – Germanium – Gold – Nickel – Gold and is annealed to 400°C with a rapid thermal annealing system. Both techniques are

standardized metallization process, this work employed very particular surface preparations in order to achieve metal contacts which are ohmic, rather than Schottky.

4.1.5.1 *P*-type metallization

P-type metallization for InP-based semiconductors are made with a degenerately doped *p*-type layer of InGaAs, and a tri-layer of metals: titanium (500 Å), nickel (1200 Å), and gold (1.5 µm). Using a thin layer of InGaAs is effective in producing an ohmic contact even without annealing due to the narrow bandgap of the InGaAs material and the low barrier height between metals and the InGaAs compound semiconductor. In this metallization scheme, titanium acts as an adhesion layer for the remaining metal stack, the platinum acts as a diffusion barrier to prevent gold from diffusing into the underlying semiconductor, and the gold layer serves as a bulk current conductor and a non-oxidizing surface protection. All metal deposition is performed in a multi-pocket CHA industries Mark III (CHA) electron beam evaporator.

Practically, the *p*-type metallization is difficult for these samples due to the large and abrupt topography variations present in the samples, primarily when providing continuity from the top of a 3 µm wide and 1.2 µm tall ridge structure down to the surrounding substrate. To deposit metal up the sidewall more effectively, planetary sample holders are used in the CHA which rotate the sample at an angle during metal evaporation, coating sidewalls more effectively than a standard normal-incidence evaporation. Additionally, a very thick layer of gold is used to coat over this step more reliably. SEM images of the metal coating along a ridge structure are shown in Figure 4.31.

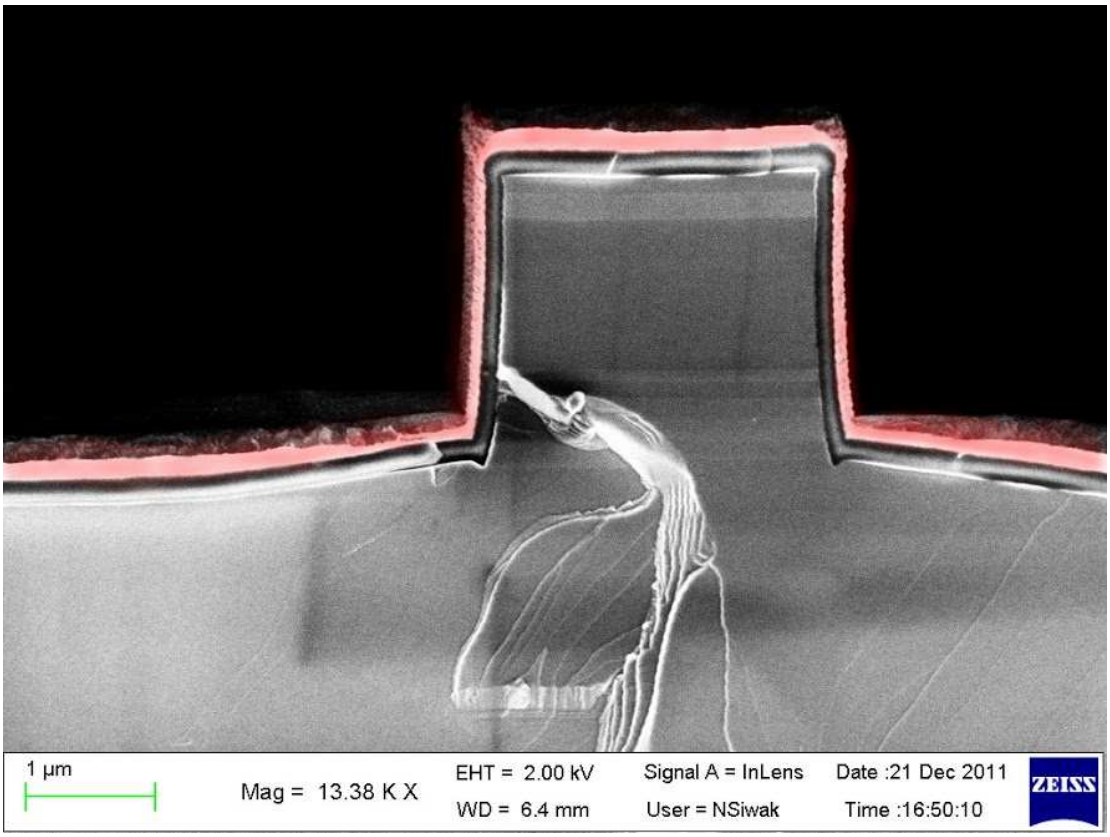


Figure 4.31. SEM image of metallization (tinted red) achieving continuity from the bottom to the top of the narrow laser ridge structure via planetary evaporation.

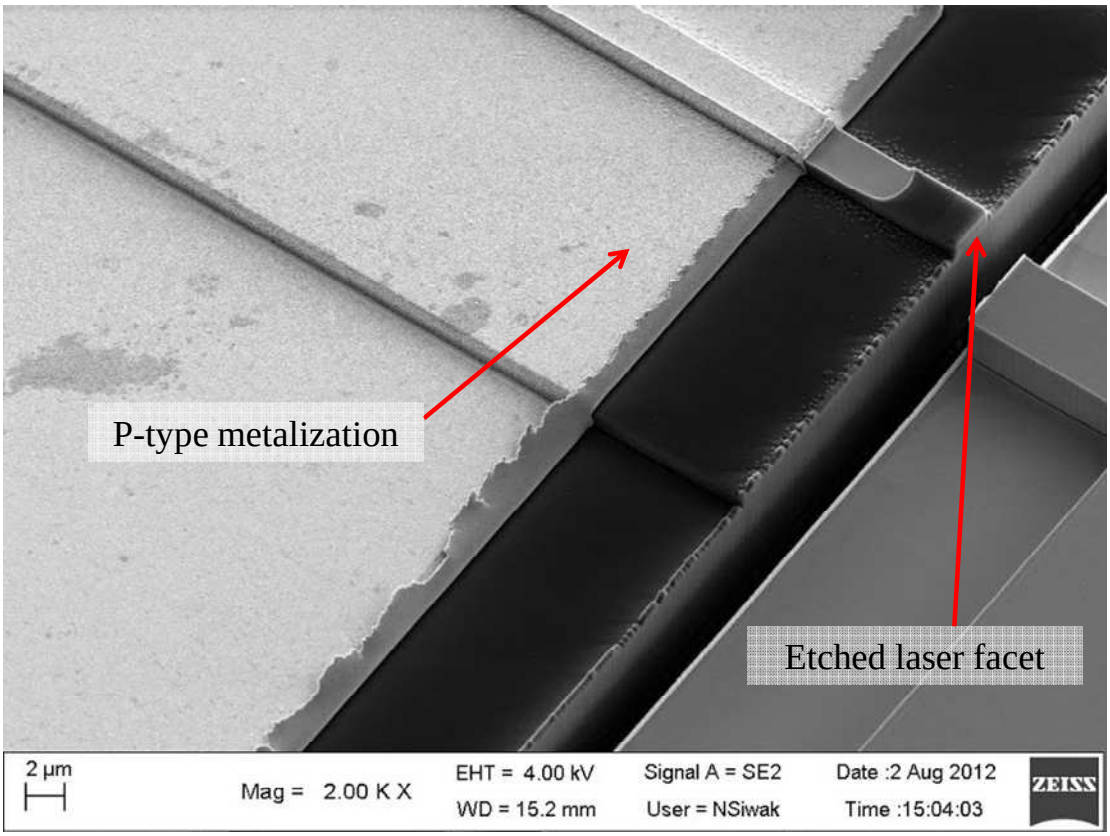


Figure 4.32. SEM of metallization on top of the Si_3N_4 passivation (dark region), and covering the laser ridge.

4.1.5.2 *N*-type metallization

The standard *n*-type metallization to InP materials is a mixture of Ni-Ge-Au materials annealed over 325°C, the nickel and germanium have been found to form complexes and alloys with the semiconductor material and reduce barrier heights present due to dangling bonds at the surface of the semiconductor [200]. The typical metallization consists of a dual layer of Ni and an AuGe alloy (88-11% by weight). Since all metalizations were performed in-house with an e-beam evaporator, metal alloys are not a preferred metal deposition due to the different evaporation/dissolution rates present in the metal alloys; instead a multi-layer stack is formed to approximate the use of an AuGe alloy. The final multilayer metal structure which is evaporated onto the degenerately doped ($n = 5\times10^{18}$ cm^{-3}) InP material is: nickel (50Å),

germanium (400Å), gold (300Å), nickel (800Å), gold (2000Å). The metal stack is then annealed in a rapid-thermal-annealing furnace (RTA), at 300°C for 60 seconds and then 400°C for 40 seconds. In this structure the nickel serves to assist in substrate adhesion, and also forms ternary compounds with the underlying substrate, likewise the next three gold and germanium layers in the metal stack form a eutectic and penetrate the underlying nickel and form ternary compounds with the doped InP material. The final gold layer is a thick capping layer to protect the surface and reduce metal oxidation. After annealing the surface roughness increases although this did not affect the performance of these contacts. Details of the process steps are available in Appendix A. This fabrication process is an established metallization scheme in literature and has been used for numerous published works [26, 30, 32, 165, 201].

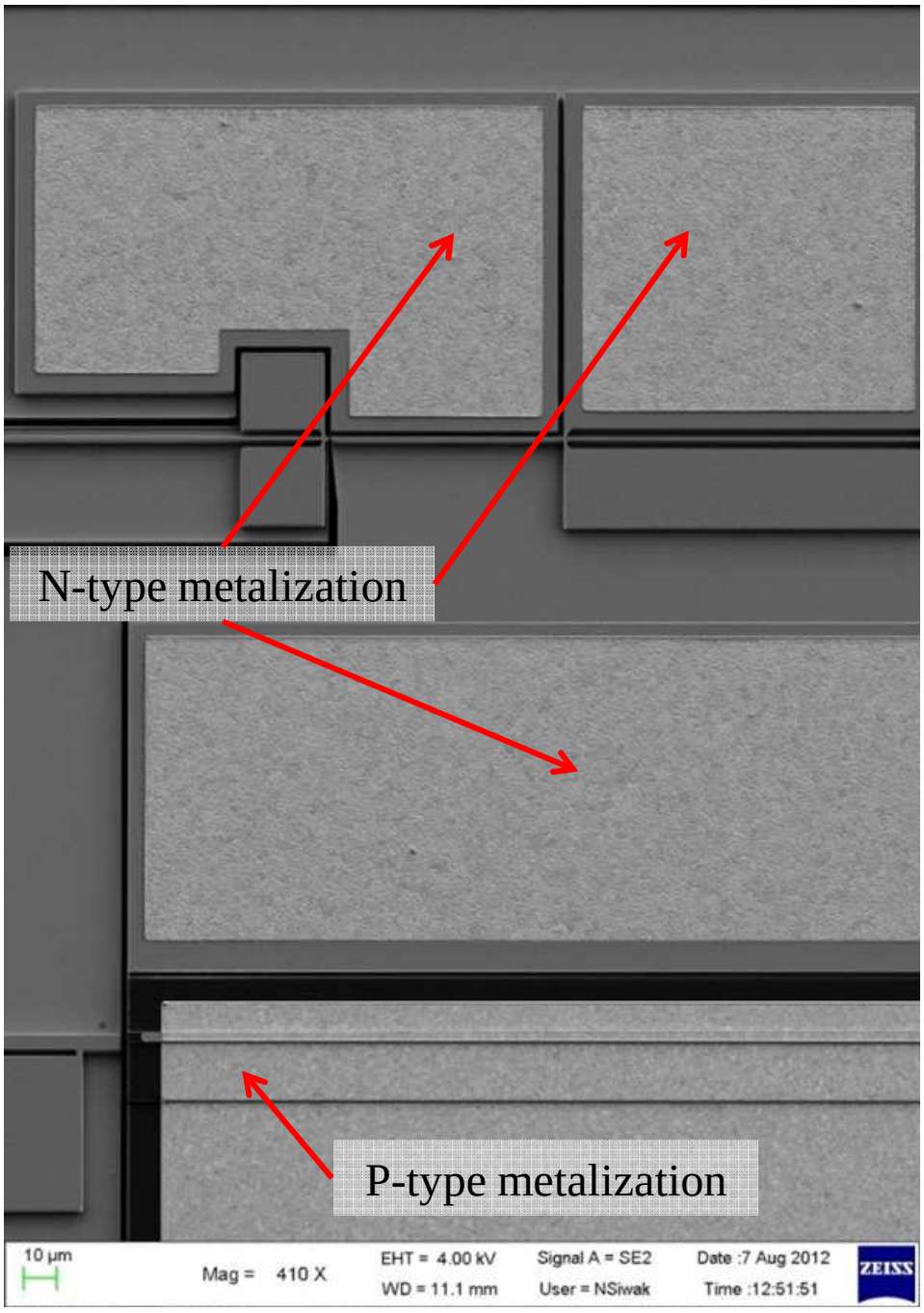


Figure 4.33. SEMs of *n*-metallization after annealing steps are completed. Left shows the rough morphology of the metal contact pads in the cantilever. Right shows the laser region with *p*-contacts over top of the dark Si_3N_4 passivation. Notice the difference in surface roughness between the *n* and *p* contact metals.

4.1.5.3 Metal lift-off

Patterning of all metal contacts is done via a lift-off process rather than a wet metal etch. This is due to the large number of metals and layers used in the contacts,

as well as the sensitivity of the underlying III-V semiconductors, many of which would be attacked by standard metal etches. The better solution over-all is the lift-off process.

The lift-off procedure is as follows:

1. Spin coat negative photoresist
2. Exposing and developing the resist
3. Performing a 30 second wet acid dip ($HCl:H_2O$ – 1:20) to remove surface oxides and impurities
4. Immediate insertion into electron beam metal evaporation chamber (CHA) and subsequent metal deposition (*n* or *p* type, as described above)
5. Remove from vacuum chamber
6. Overnight soak in 80°C Remover PG resist stripper (99% NMP solution)
7. Final sample cleaning with Acetone/Methanol/Isopropanol

4.1.5.4 Surface preparation

A key aspect of contact formation on semiconductor surfaces is the preparation and cleaning of these surfaces before metallization. If the surface is not clean of organic materials and surface oxides, metals may physically delaminate for the semiconductor surface, or a potential barrier may form between the metallization and the semiconductor surface.

A number of methods were explored in order to prepare sample surfaces before metallization. Tests of contact quality were performed using a circular transfer length measurement (CTLM) structure and measurement technique (see Figure 4.34).

This method has been used in previous literature to accurately determine contact resistance of the metallization and the sheet resistance of the underlying semiconductor surfaces [202-204] without the negative effects of current spreading which are often evident in the standard linear TLM measurement.

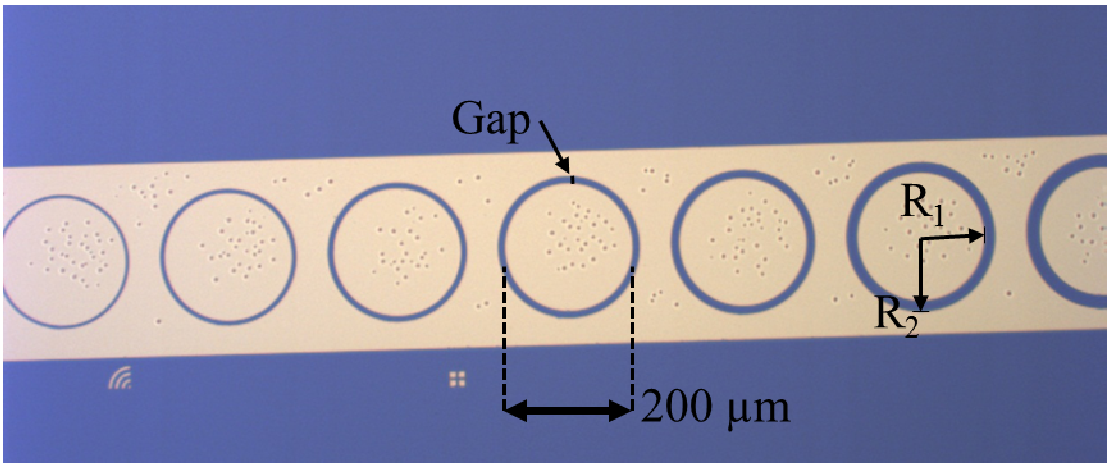


Figure 4.34. Optical micrograph showing CTLM metalized pattern used for contact resistance and sheet resistivity tests.

As in the standard linear TLM measurement, resistance is measured for various contact spacings and plotted versus the distance of the spacing. In this method, the resistance of a ring of semiconductor material, comprised of a 200 µm diameter circular center metal pad and a surrounding pad, is measured for varying gap lengths, 4, 8, 12, 16, 20, 24, 32, 40, and 48 µm. Resistance is determined via a standard 4-point probe measurement with an Agilent 4156B semiconductor parameter analyzer. I-V-curves of each contact pair are also considered for qualitative determination of non-linearity of each contact pair. Once resistance is determined, these values are plotted against the semiconductor gap dimensions.

The resistance of each circular contact pair can be represented approximately as [204, 205]:

$$R = \frac{R_{sh}}{2\pi}\left[\ln\frac{R_2}{R_2 - s} + L_T\left(\frac{1}{R_2 - s} + \frac{1}{R_2}\right)\right] \quad (4\text{-}1)$$

where R_{sh} is the sheet resistance of the semiconductor material, R_2 is the outer radius of the ring and s is the gap between the inner and outer rings (see Figure 4.34). L_T is the "transfer length" and is typically seen as a measure of the ohmic quality of the resulting contacts. A shorter L_T indicates a better ohmic contact. One can apply a linear correction term (see equation (4-3)) to each resistance value to linearize the data and make the extraction of parameters more simple; without these corrections, the specific contact resistance would be underestimated [204, 205]. The natural logarithm in equation (4-1) can be evaluated using a Taylor expansion in the limit that the inner radius (R_1) is much larger than s and $R_2 = R_1 + s$. Equation (4-1) then can be written as:

$$R = \frac{R_{sh}}{2\pi R_1}[s + 2L_T] \cdot c \quad (4\text{-}2)$$

where R_1 is the inner radius of the ring structure. The correction term, c, is then defined as:

$$c = \frac{R_1}{s} ln \frac{[R_1 + s]}{R_1} \quad (4\text{-}3)$$

Resistance data is then fit to a straight line by dividing each resistance measurement by this correction term and then plotting resistance versus gap length (see Figure 4.35). The values of the correction terms are shown below in Table 4.3. The resulting y-intercept and slope of the fitted line are used to calculate the transfer length, sheet resistance, and the specific contact resistance of the metallization following the form of equation (4-2). Each surface preparation sequence was carried out with this measurement following to determine the contact properties.

Table 4.3. Correction terms for linear fitting of CTLM data

Gap length (μm)	Correction term, *c*
4	0.990
8	0.981
12	0.971
16	0.962
20	0.953
24	0.944
32	0.928
40	0.912

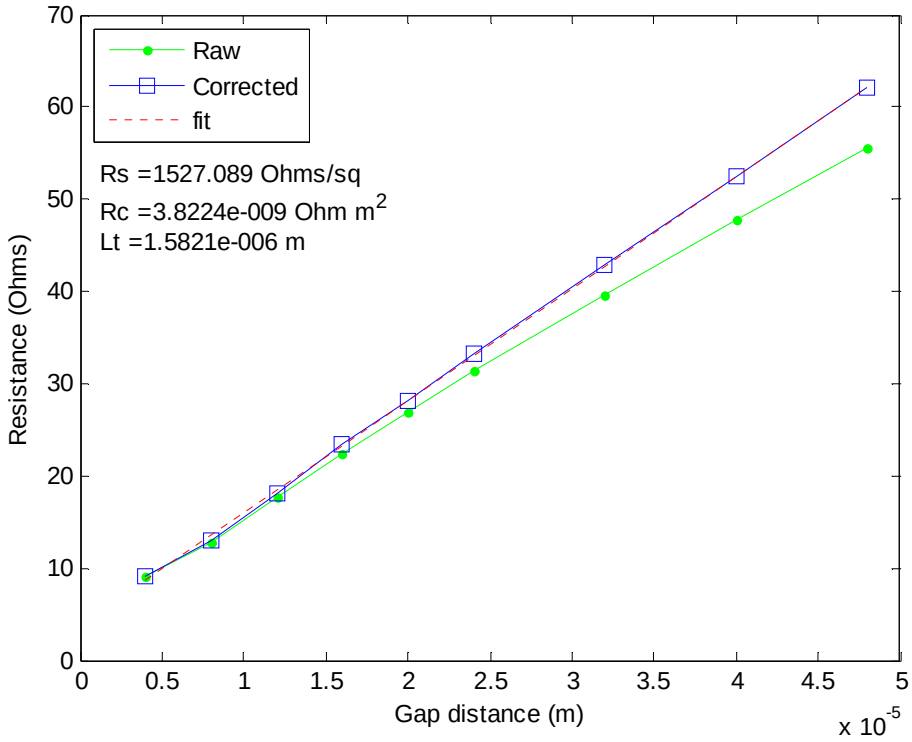


Figure 4.35. Example data from CTLM measurements showing raw and corrected data for a set of measurements.

Both plasma treatments and non-plasma treatments were used as surface preparations. The plasma treatments used were: O_2 plasma (for removal organics, photoresist), CHF_3 (traditional standard oxide etch, to remove native oxides), and Ar (physical sputtering to clean surfaces). Non-plasma treatments used were a dilute (1:20) solution of HCl:H_2O, and no treatment whatsoever. Test samples were

patterned with negative photoresist following the recipes outlined in section 4.1.1.6 for lift-off. Once the photoresist is patterned, the surfaces are treated with one of the above to ready them for *p* and *n*-type metallization in an e-beam evaporation chamber. A summary of these results are presented in Table 4.4.

Table 4.4. Tabulated results from contact resistance surface preparation testing.

Surface preparation	Contact resistance (Rc) ($\Omega \cdot m^2$)	Sheet resistance (Rs) ($\Omega/\square$)	Transfer length (Lt) (μm)
O2 plasma + HCL acid dip	1.11×10^{-7}	803.4	11.751
HCL acid dip	3.92×10^{-9}	455.4	2.9352
O2 plasma + Sio2PT oxide etch	1.99×10^{-6}	242.3	90.725
O2 plasma	8.23×10^{-7}	50.8	127.31
SiO2PT oxide etch	4.67×10^{-6}	158.4	171.76
Argon sputter	6.21×10^{-6}	156.2	199.34

Experiments indicated that any plasma processing steps used in an attempt to clean the surface for non-annealed metallization produced non-ohmic, Schottky contacts, with plasma processes other than an oxygen plasma clean producing worse contacts than oxygen plasma alone. The dilute HCL wet etch was the only successful technique to achieve ohmic, non-alloyed *p*-type contacts, with a contact resistance of 4×10^{-9} $\Omega \cdot m^2$. It was found that *n*-type metalizations were less sensitive to the surface preparation, as the alloying process in the RTA penetrates surface oxides and surface defects to establish ohmic contacts that did not vary between different surface preparations.

Literature indicates that hydrogen-containing plasmas passivate acceptors in nearly all semiconductors, including InGaAs. Moreover, papers reported passivation in the *p* (and *n*) type materials up to depths of 100's of nanometers [206-212]. In the case of InGaAs this passivation arises due to complexes that form between H and Be atoms in the semiconductor [213-215]. This creates effective doping densities an

order of magnitude less than the original doping density, and in low doping cases, complete type inversion. In addition to the interdiffusion of hydrogen species, there is also measurable lattice damage due to ion bombardment causing non-stoichiometric surfaces and additional defect states. Authors reported that in most cases high temperature anneals (>400°C for more than 60 seconds) were able to restore the semiconductor to its original state [216]. These high temperature annealing steps are not practical in the case of this work, or any work containing thin quantum wells for fear of interdiffusion of these abrupt interfaces.

4.1.6 Wet undercut etching and critical point drying

Wet semiconductor etches were employed in the fabrication process in order to create the overhanging MEMS cantilever structures. Material selectivity between InP and InGaAs containing materials was exploited to create a selectively etched sacrificial layer underneath the moveable devices. After the etch is performed, a critical point dry step is needed in order to dry the sample without the effects of stiction damaging the fragile released devices.

4.1.6.1 Wet etching chemistries

A number of wet etch chemistries are known for the InP-InGaAs material system, and in the case of an InGaAs sacrificial etch they are completely selective to InP, and only partially selective to InGaAsP compounds. Typically the solutions consist of an acid and hydrogen peroxide mixture diluted with water [217]. A number of wet etchants were tested for their ability to etch the as-grown materials; critical was the ability to etch InGaAs as well as InGaAsP materials, both of which

comprise the sacrificial layer for these devices (see section 0). Literature [217, 218] and anecdotal evidence shows that InGaAsP materials will etch significantly slower than InGaAs. It is important to not just find an etch which undercuts the InGaAs material fastest, but to find a wet etch chemistry which has the most balanced etch rate between InGaAs and InGaAsP materials to reduce the amount of sacrificial material without severely over etching the structures. In addition to this, the etchants cannot attack the existing materials on the die surface.

Three different acid/peroxide solutions were tested, $HF:H_2O_2:H_2O$, $H_2SO_4:H_2O_2:H_2O$, $H_3PO_4:H_2O_2:H_2O$, all mixed in a 1:1:8 ratio. These acids were chosen due to their availability and prevalence in literature. Previous work utilized the HF mixture, primarily due to its very high etch rate through InGaAs [26, 28, 30, 32, 165, 183]. Etches of a bulk sample were performed for 5 minutes, and then cleaved crossections were examined via SEM to investigate the undercut rate (see Figure 4.36).

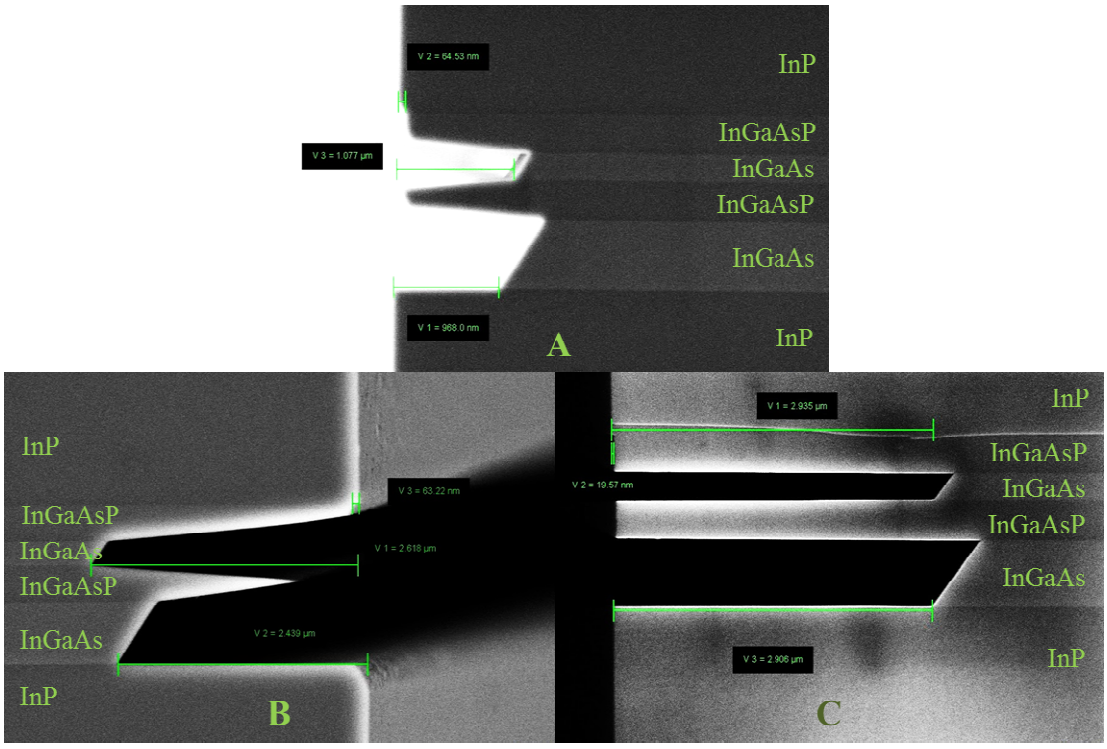


Figure 4.36. Cross-sectional SEM images of undercut samples with layers labeled A) H_3PO_4:H_2O_2:H_2O, B) H_2SO_4:H_2O_2:H_2O, C) HF:H_2O_2:H_2O

Table 4.5. Calculated undercut lateral etch rates for 5 minute etch tests of InGaAs and InGaAsP of epitaxial growth

Wet etchant:	**H_3PO_4:H_2O_2:H_2O**	**H_2SO_4:H_2O_2:H_2O**	**HF:H_2O_2:H_2O**
InGaAs etch rate (nm/min)	215.4	523.6	587
InGaAsP etch rate (nm/min)	12.906	12.644	4.084
Ratio	16.68991	41.41095	143.7316

The rates of each material for each etch are illustrated in Table 4.5. The three etched produced somewhat similar results, illustrating a crystalline anisotropy in the InGaAs materials. The results of this etch experiment indicate no dependence on the layer thickness to the undercut depth (see Figure 4.36), suggesting a mostly reaction-rate limited etching process, which is expected for the InP-InGaAs material system [18, 219, 220]. It is also of note to mention that the HF etch formulation, and to a lesser extend the H_2SO_4, aggressively attacks titanium delaminating *p*-type metal

pads on the sample surface which use a titanium adhesion layer (section 4.1.5.1). The H_2SO_4 and HF acid containing materials were found to etch InGaAs so quickly; they completely lifted off the patterns before a sufficient undercut of InGaAsP was achieved. From these results, the etchant which exhibits the lowest ratio of InGaAs/InGaAsP etch rates is the H_3PO_4 formulation, and thus was used for the undercut despite the overall slower etch rates. A side effect of this mismatched etch is that a thin membrane of InGaAsP remains beneath the released waveguides, increasing the possibility of stiction regardless of the CO_2 critical point dry (section 4.1.6.2). At the time of device fabrication the full impact of this un-etched membrane was unknown. A more complete discussion of this etching artifact will be discussed in section 5. This etching artifact is shown clearly in Figure 4.37.

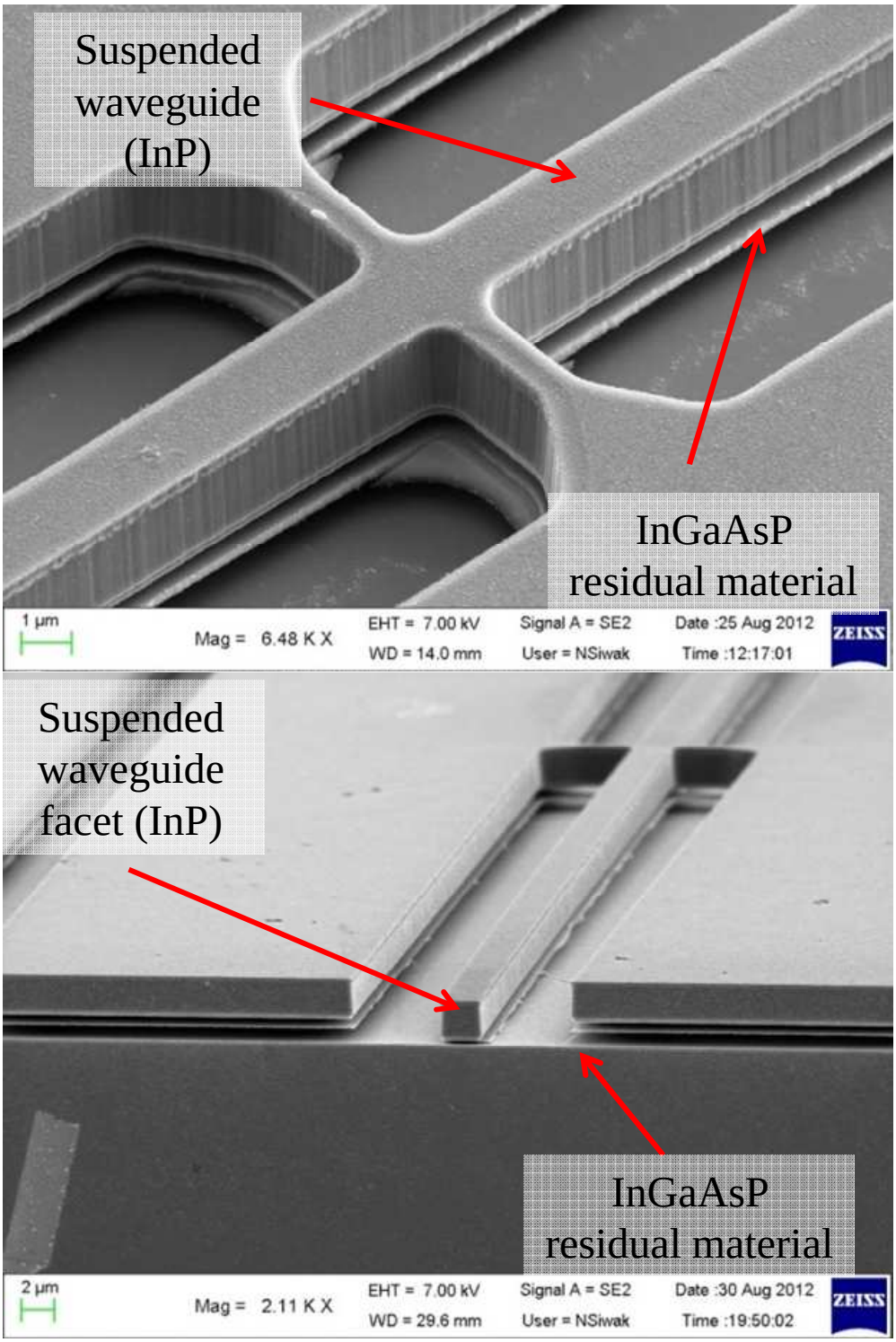


Figure 4.37. SEM images of undercut samples with the InGaAsP membrane clearly visible beneath the waveguides.

In order to gauge the amount of under etch practically when performing this fabrication step, a number of bars with varying widths (0.5 – 25 µm wide) are

included in the waveguide mask as “release bars.” As the undercutting etch is being performed the sample is periodically placed under a microscope to observe which release bars have lifted off completely. A completely released bar indicates a complete removal of the InGaAs and InGaAsP layers beneath, and thus can help gauge the degree of cantilever and waveguide release. Throughout this process, the sample is never removed from solution and dried to prevent surface tension forces from causing stiction of cantilevers and suspended waveguides against the substrate and sidewalls.

4.1.6.2 CO_2 critical point dry

The final fabrication process step is completed by using a critical point dryer (Tousimis Samdri®-795) to prevent stiction from occurring. A CO_2 critical point dryer takes liquid CO_2 through its critical point into a gaseous state, avoiding surface tension forces that are present under normal atmospheric evaporation which can cause destruction of free-standing structures.

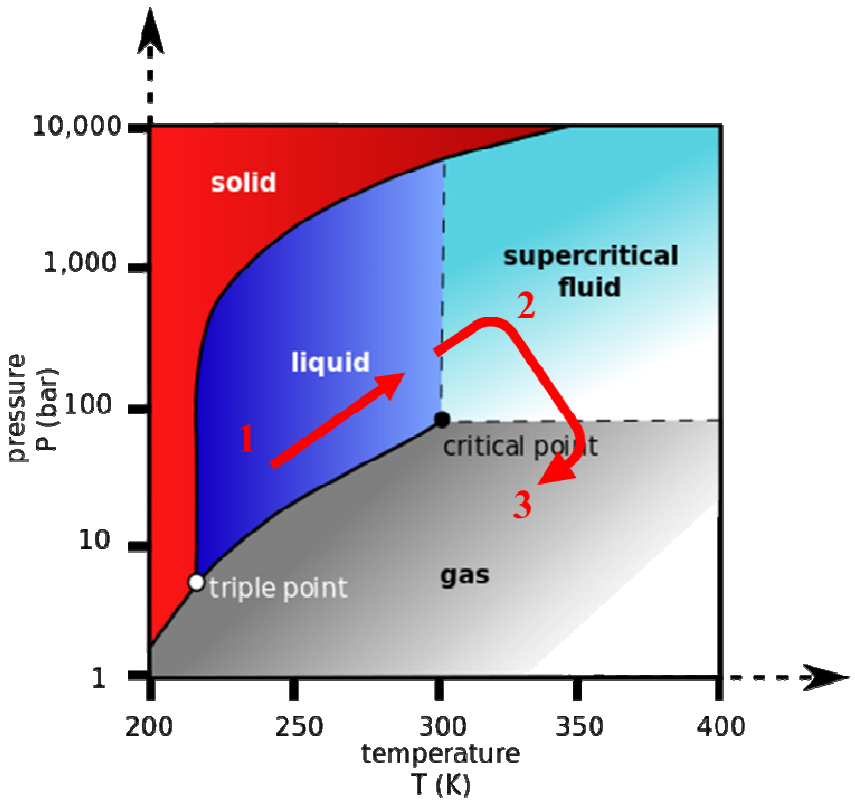


Figure 4.38. Phase diagram of CO_2 showing the critical point and the supercritical point dry process. 1) Liquid CO_2 is pumped into the chamber, the temperature and pressure increased beyond the critical point 2) once in the supercritical fluid phase, the pressure is reduced until the gas phase is achieved. Adapted from [221].

Released samples are transferred from deionized water into acetone and methanol subsequently in order to completely dehydrate the sample. Methanol is used to store the released sample before the sample is transferred to the CO_2 critical point dryer. The system is then automated to fill with liquid CO_2 and take the sample "around" the critical point of CO_2 (304.25 K, and 7.39 MPa) by raising the pressure and temperature beyond this point, and then reducing the pressure, avoiding the liquid-gas transition. This process negates the effect of the surface tension forces at the gas-liquid interface, and prevents the damage of fragile freestanding structures.

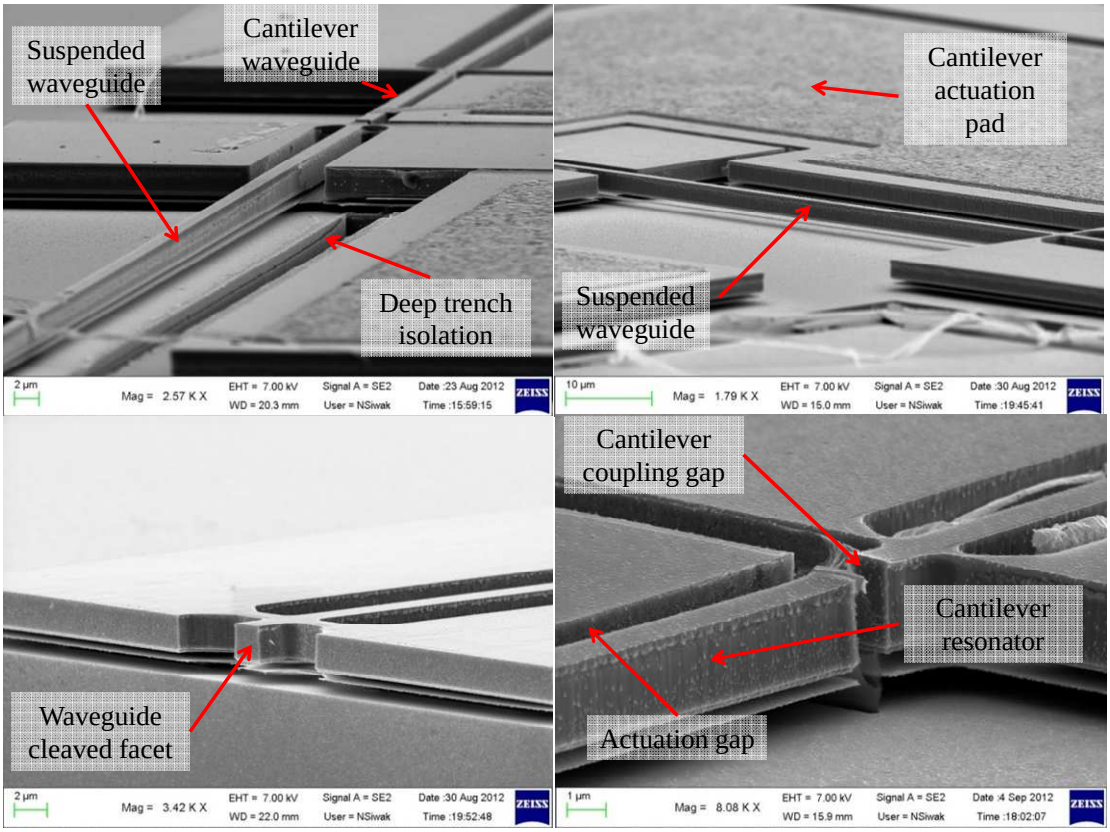


Figure 4.39. SEMs of various undercut and CO_2 critical point dried cantilevers and waveguides.

Fabricated device

In Figure 4.40 a completed, but yet un-thinned and un-cleaved die is shown alongside another thinned example which has been cleaved into the three chips. These images illustrate the scale and final form factor of the completed devices.

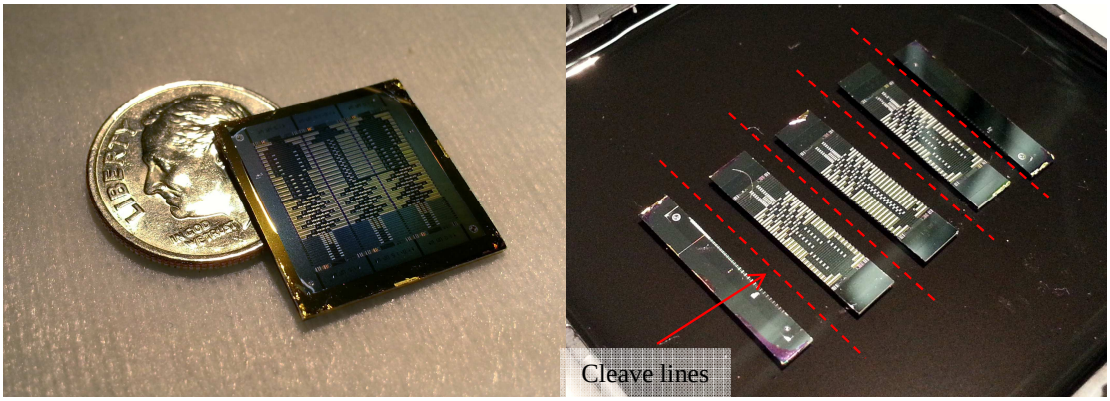


Figure 4.40. Photographs of completed die (left), and a thinned and cleaved die into the 3 chips (right).

Figure 4.41 presents a composite SEM image of the final completed device with each component notated and exploded in an inset image. Indication of the direction of light propagation along the waveguide is shown in the figure as well.

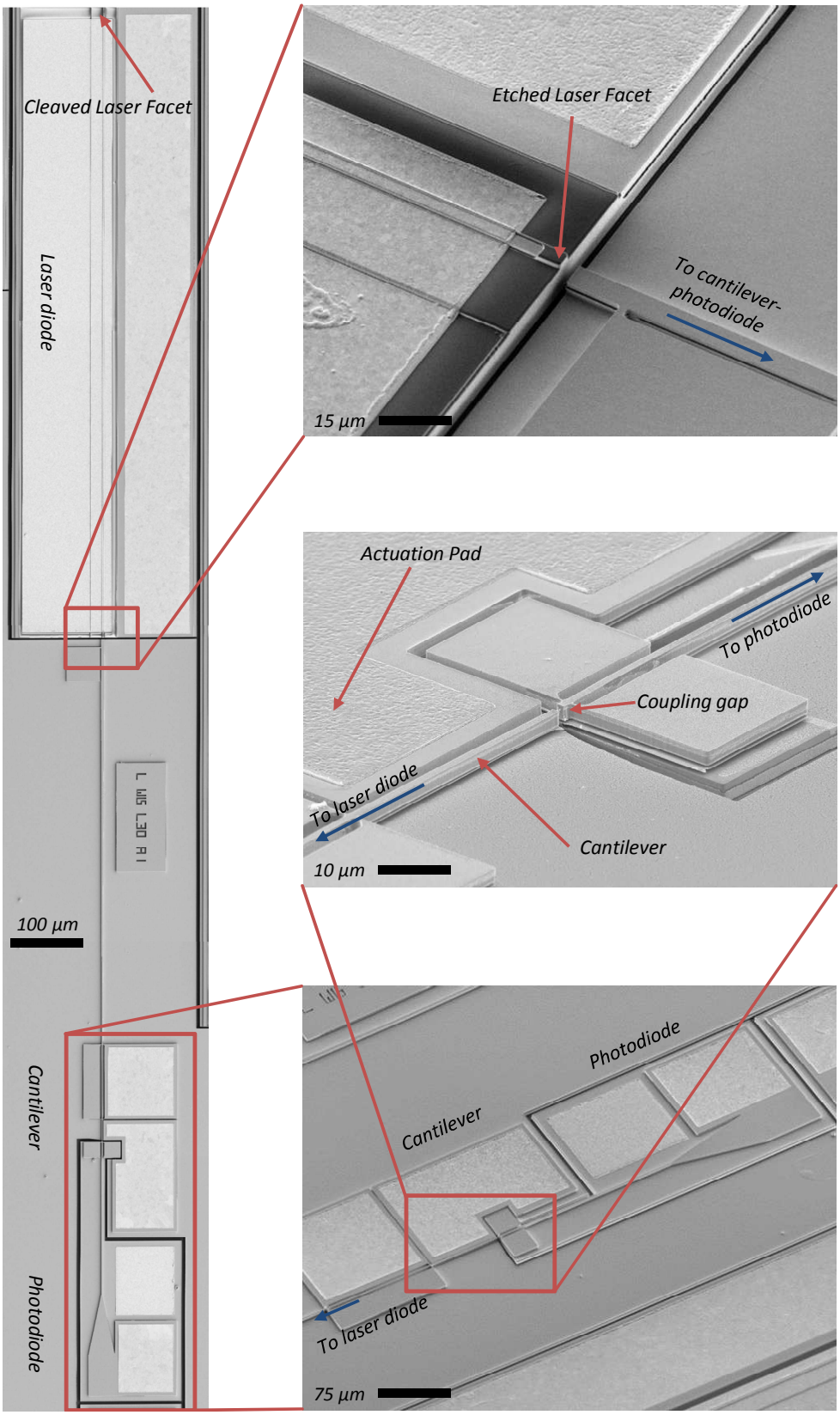


Figure 4.41. SEMs of completed device showing the relative locations of laser light source, cantilever waveguide, and photodiodes.

5 Device testing and analysis

Testing fabricated devices comprised the testing of separate components such as the lasers, cantilevers, and photodiodes independently. After this data was collected, the coupled components were intended to be tested together. The focus of this work was the demonstration of device integration, and thus a limited number of experiments were performed to verify the basic functionality of the devices under test in their different configurations. A complete fabrication run was performed successfully on an epitaxial sample and tested, however due to a processing oversight devices were rendered inoperable upon the last fabrication steps. Modifying the processing techniques slightly and acquiring a new material growth, a second improved fabrication run was then performed.

The following sections will outline the testing setups and procedures used in the testing of the two fabrication runs and present the raw data from the experiments. The majority of data taking and testing fixtures described in the following were initially constructed by Dr. Christopher Richardson and personally modified for the specific application to this work. The data which has been collected and analyzed is then discussed. Due to limited yield of fabrication run 1 and widespread device inoperability in fabrication run 2, much of the data analysis is focused on determining the failure mechanisms and shortcomings in the final device realization which contributed to the poor overall system performance. This section concludes with a discussion of the proposed failure mechanisms and how to address these in future work.

Fabrication run 1

Fabrication run 1 is completed after all of the fabrication optimizations as outlined in section 0. Testing is carried out in two phases, lasers and photodiodes tested before and after the device undercut waveguide/cantilever release outlined in section 4.1.6.

5.1.1 Testing setup and procedures

Laser diodes were tested in both pulsed and continuous wave (CW) modes of operation. Devices were fabricated and attached to a thin copper plate with indium solder (see Figure 5.1). This plate is then mounted to a copper block with thermal paste. Mounting the sample in this manner provides a thermal sink for the device. The device can be un-mounted simply by re-heating the copper plate and removing the sample with tweezers. This allows for the two-stage testing procedure before and after device release.

The whole system is cooled via a thermoelectric cooler element, an ILX Lightwave LDT-5412 temperature controller, and a feedback thermistor. All cooling is set to 10°C, estimated via the Steinhart/Hart method with provided manufacturer constants. Electrical contact was made to devices via micropositioner probes and connected to the current source used for electrically pumping the laser diodes. Measurement of light output was performed using a Newport Model 818-IR photodiode attached to a separately calibrated Newport 819-OPT integrating sphere used in order to capture the maximum crossection of output laser light. Figure 5.2 illustrates the components of this setup. This photodiode was then connected to a

Fempto DHPVA voltage amplifier characterized as high-impedance, low noise, and good low-frequency performance (bandwidth: DC – 200 MHz) in order to measure the diode photocurrent.

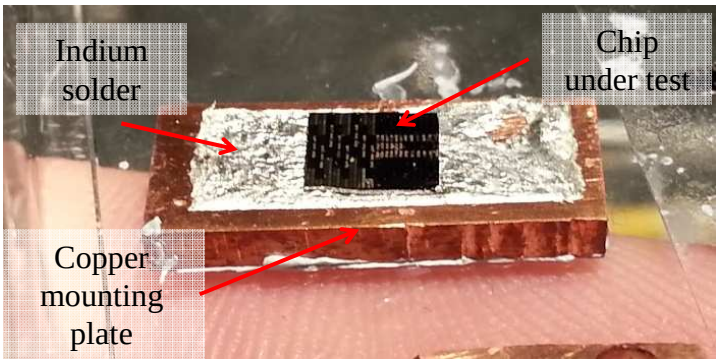


Figure 5.1. Standard sample mounting.

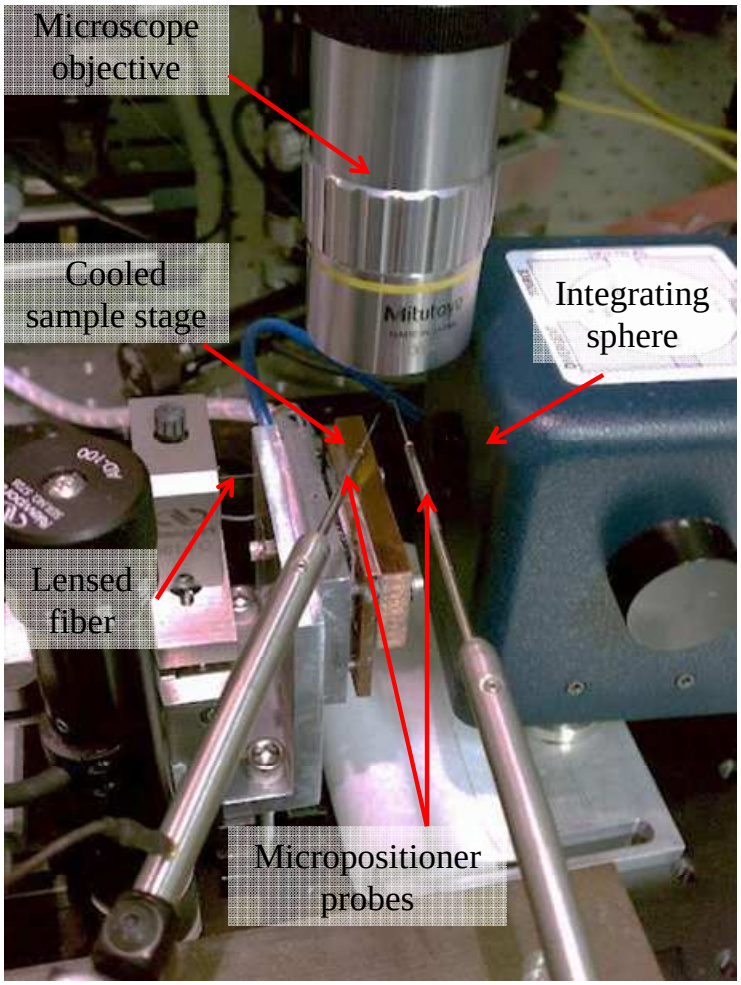


Figure 5.2 Standard testing setup.

5.1.1.1 Continuous wave testing

Continuous wave (CW) laser measurements are generally performed in order to measure the forward bias DC characteristics of the laser diodes. An initial current-voltage (I-V) sweep of the diode is performed utilizing an Agilent 4156B semiconductor parameter analyzer in order to establish diode-like forward and reverse bias behavior, as well as establish the diode turn-on voltage of the lasers.

A Newport modular controller (model 8008, or 5600 depending on required compliance voltage) laser diode driver is used to electrically pump the devices to achieve lasing operation. Output light is collected from the cleaved facet of the laser devices with the calibrated integrating sphere in order to increase the collection efficiency of the photodiode. The cleaved facet is used for collection due to its location at the edge of the wafer which makes it possible to place the integrating sphere and photodiode close to the source of emitted radiation.

5.1.1.2 Pulsed laser testing

Pulsed laser testing was performed in order to measure device current while minimizing the effect of resistive heating. A very low duty cycle (1%-0.001%) voltage pulse is created with a HP 0114A 100V/2A pulse generator and sent to the device via a voltage divider circuit which allows laser pumping and a direct measurement of device current and voltage. The circuit used for this measurement is presented below in Figure 5.3. Pulse widths were required to be larger than 5 µs due to the ~3-5 µs risetime of the Newport 819-OPT photodiode used in this experiment. A Tektronix TDS 3014B oscilloscope is used to capture the time-resolved laser diode voltage pulse as well as device current and device output light. Light – Current –

Voltage (LIV) are recorded simultaneously at varying stage temperatures (22°C and 10°C) and pulse widths (5-10 µs) to characterize fabricated laser diodes. A LABVIEW program (originally written by Dr. Chris Richardson and modified for this work) is used to automatically sweep the output voltage of the pulse source while recording the diode voltage and output light simultaneously.

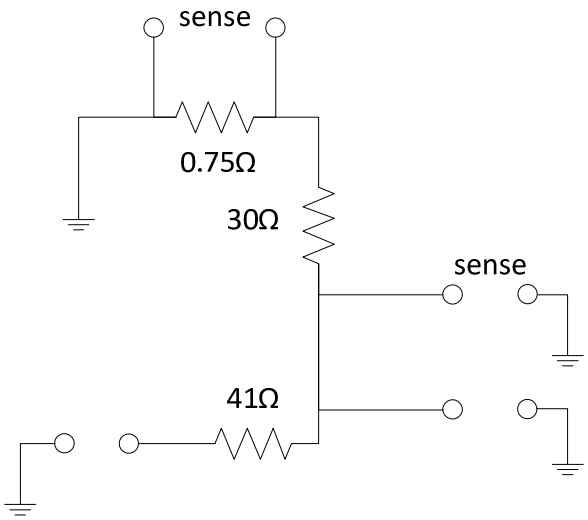


Figure 5.3. Circuit diagram illustrating connections for pulsed testing setup.

5.1.2 Laser testing results

Laser diodes were tested from each completed and cleaved devices before the undercut-release step, with varied success rates across various device runs. Figure 5.4 shows LIV curves typical of the first fabrication runs and corresponding to the three lengths of laser cavities (500, 1000, 1500 µm) tested with the pulsed current measurement configuration at two temperatures, actively cooled to 10°C and passively cooled to the copper heatsink (no cooling). Active cooling was used for every subsequent device test due to the lower threshold current exhibited in every device tested (as can be seen in Figure 5.4) and the reduced danger of device damage due to overheating. 10°C was observed as the temperature where condensation

begins to collect on the sample, and thus was selected as the lower limit of cooling. CW operation of the same laser diodes was observed for a single device only at the 10°C cooled conditions; however no parametric data was taken before device failure due to device breakdown and failure.

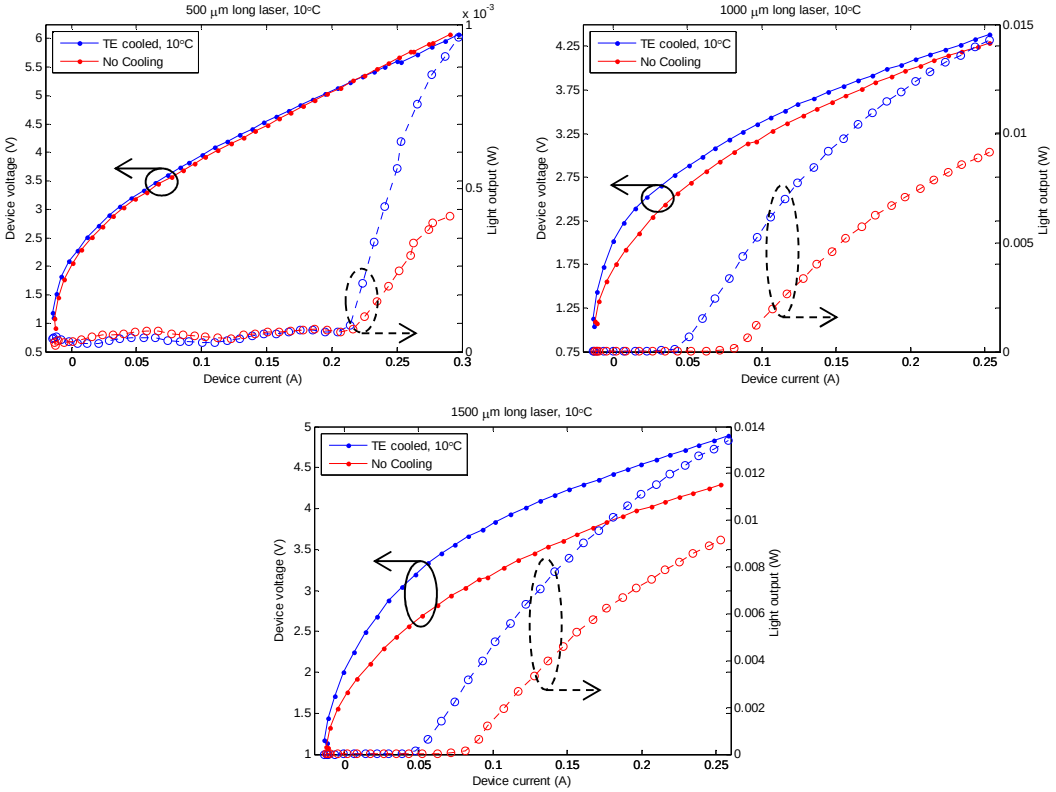


Figure 5.4. LIV measurements of working lasers with only passive cooling to the copper heatsink (no cooling) and actively cooled to 10°C. All three lengths are represented: 500, 1000, 1500 µm.

5.1.2.1 Laser diode analysis

The general device characteristics of each laser diode length (500, 1000, and 1500 µm) have been presented in Table 5.1 and Table 5.2, along with representative LIV curves at two temperatures in Figure 5.4. Due to the short lifetime of working devices, a complete spectral analysis was not able to be performed. To estimate the wavelength of the output laser light more accurately, the quantum well photoluminescence peak wavelength of 1517 nm determined at the time of the

epitaxial growth and measured by C. Richardson, was used for all wavelength values. All following calculations were performed with data taken under TE-cooling conditions unless indicated. Laser diode forward resistance was determined by fitting a straight line to the forward biased portion of the I-V curve. The slope of this line is then the inverse of the forward diode resistance (Ohm's law). Threshold current and slope efficiency are calculated by fitting a straight line to the Light-Current curve (L-I) near the laser diode threshold. The slope of this line is then taken as the slope efficiency, and the x-intercept is calculated to determine the threshold current. Table 5.1 and Table 5.2 present average values of the operating characteristics for 10°C cooled devices across the first functioning fabrication run from two chips on a single die. These two chips are functionally identical and were processed in parallel.

Table 5.1. Average values for tested lasers before undercut release (sample g1125a 3,4 2B)

Laser cavity length (μm)	**Threshold current density (A/m^2)**	**Forward resistance (Ohms)**	**Slope efficiency (W/A)**
500	$1.83\pm0.099\times10^8$	8.465±0.460	0.033±0.017
1000	$1.663\pm0.709\times10^8$	5.756±0.398	0.123±0.064
1500	$1.001\pm0.425\times10^8$	5.718±0.621	0.134±0.161

Table 5.2. Average values for tested lasers before undercut release (sample g1125a 3,4 3B)

Laser cavity length (μm)	**Threshold current density (A/m^2)**	**Forward resistance (Ohms)**	**Slope efficiency (W/A)**
500	$1.76\pm0.345\times10^8$	9.82±0.866	0.021±0.029
1000	$1.461\pm0.329\times10^8$	5.50±0.345	0.053±0.033
1500	$1.259\pm0.130\times10^8$	5.62±0.279	0.274±0.300

The goal of this experiment is to extract the internal parameters of the laser diodes: the internal loss $<\alpha_i>$, the internal quantum efficiency η_i, and the wall-plug

efficiency. These values can be determined by calculating the differential quantum efficiency, η_d, which can be expressed as [187]:

$$\eta_d = \left(\frac{q}{h\nu}\right)\frac{dP_o}{dI} \equiv \frac{\eta_i \alpha_{mirror}}{\langle \alpha_i \rangle + \alpha_{mirror}} \tag{5-1}$$

where q is the electron charge, h is Planck's constant, ν is the light frequency, P_o is the total output optical power from both facets, I is the laser diode forward current, η_i is the aforementioned internal quantum efficiency, and α_{mirror} is a lumped mirror loss term defined as [187]:

$$\alpha_{mirror} = \frac{1}{L}\ln\left[\frac{1}{r_1 r_2}\right] \tag{5-2}$$

where L is the length of the optical cavity, and $r_{1,2}$ are the mirror reflectivities. The differential resistance is easily calculated knowing the slope efficiency of the laser diode, and the diode lengths can be measured via SEM inspection. Equation (5-1) and (5-2) can thus be re-written as:

$$\frac{1}{\eta_d} = \frac{\langle \alpha_i \rangle}{\eta_i \ln[1/r_1 r_2]} L + \frac{1}{\eta_i} \tag{5-3}$$

The reciprocal of the differential quantum efficiency versus the length is plotted together for the varied lengths and fit a straight line. The slope and intercept is then used to calculate the internal loss and internal quantum efficiency.

Reflectance needs to be determined in order to complete the analysis. The reflectivity of the cleaved facet and the etched and coated facet will be very different and need to be calculated separately. The cleaved facet reflectivity is calculated by Fresnel's equation (equation (5-11)) using the effective index of refraction of the primary mode (n_{eff} = 3.23) and air and is found to be: r_1 = 27.8%. The reflectivity of

the etched facet is slightly more difficult to calculate since it is coated with a 400 nm thin film of silicon nitride (measured via SEM crossection) and is calculated by utilizing the transfer matrix method, generalized to plane incidence. In this method, each interface is represented by a 2x2 matrix, and each propagation medium is represented by a diagonalized 2x2 matrix:

$$Interface\ matrix = I_{12} = \begin{pmatrix} \frac{(k_1 + k_2)}{2k_1} & \frac{(k_1 - k_2)}{2k_1} \\ \frac{(k_1 - k_2)}{2k_1} & \frac{(k_1 + k_2)}{2k_1} \end{pmatrix} \quad (5\text{-}4)$$

$$Medium\ matrix = M_2 = \begin{pmatrix} e^{ik_2 d} & 0 \\ 0 & e^{-ik_2 d} \end{pmatrix} \quad (5\text{-}5)$$

where k_n is the wavevector corresponding to each medium, n, and d is the thickness of the Si_3N_4 coating. The matrices can then be constructed for the semiconductor (n_1 = 3.23) – silicon nitride (n_2 = 2) – air interface (n_3 = 1) and multiplied to yield the reflection and transmission coefficients of the material stack in question assuming a wavelength of 1517 nm.

$$\begin{bmatrix} \Gamma \\ \mathrm{P} \end{bmatrix} = I_{12} M_2 I_{23} \quad (5\text{-}6)$$

with reflectance and transmission defined as:

$$Reflectance = \left|\frac{\mathrm{P}}{\Gamma}\right|^2, \qquad Transmission = 1 - Reflectance \quad (5\text{-}7)$$

Using this method, the reflectance of the Si_3N_4 coated etched facet is: r_2 = 1.96%, low as expected since the thickness of the Si_3N_4 layer approaches the ¼ wavelength for 1517 nm light.

The slope efficiency is used to calculate the differential quantum efficiency from equation (5-1). Using these calculated values, the above calculated reflectance

of each facet, and measured values for laser cavity length, the curves shown in Figure 5.5 are generated. The extracted values for internal quantum efficiency and internal loss are shown in

Table 5.3.

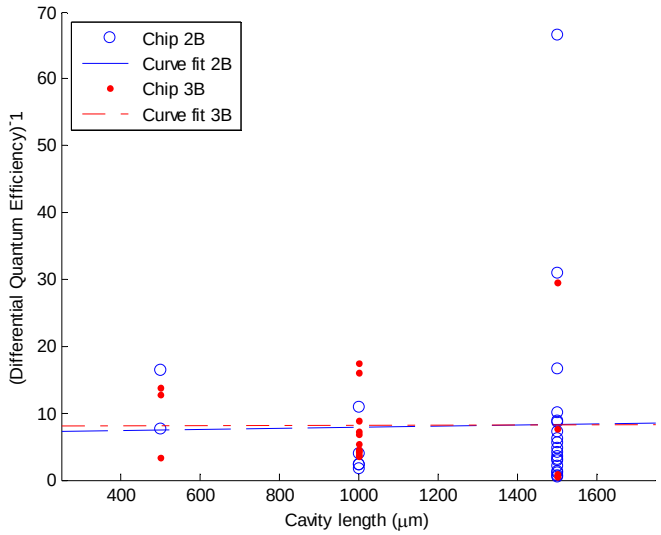


Figure 5.5. Plot of inverse differential quantum efficiency versus cavity length.

Table 5.3. Calculated internal laser parameters.

Chip	η_i (%)	$\langle\alpha_i\rangle$ (cm^{-1})
2B	13.92 ± 11.20	5.31 ± 29
3B	12.48 ± 4.9	1.07 ± 26

From Figure 5.5 and the variance in the calculated parameters from the fitted data it is evident that there is a large spread and uncertainty in the measured data, and these calculated values may not be very reliable in determining the loss mechanisms internally. This is a testament to the very sporadic lasing behavior exhibited by this first fabrication run of devices, and is an indicator of poor fabrication consistency that is a result of such a complicated fabrication scheme and die-level fabrication. It is

important to note that since the fabrication process was performed die-by-die, variation between samples even across a single 18×18 mm die due to alignment errors and edge effects was significant which contributed to the spread in this data.

Despite the large spread in the calculated parameters, it can be seen the calculated internal efficiency is small for both sets of devices, and may be an indication of high cavity loss or a high level of non-radiative recombination paths for the diode current through the active region, most likely dominated by Auger recombination, as with most InP-based lasers [187, 222, 223], and current leakage through the cladding and surface regions of the laser diode that is caused due to improperly passivated surfaces around the active regions. These non-radiative recombination paths may be due to internal material dislocations and impurities, as well as surface damage due to the ICP etching steps. Any defects directly within the quantum wells can also be significant contributors to this poor internal quantum efficiency. The very low values for internal quantum efficiency calculated here also show that these devices are very sensitive to any slight error in processing, particularly related to thermal cycling or sidewall roughness that further reduces etched facet reflectivity and propagating waveguide losses. The poor reflectance of the etched mirror coated with the Si_3N_4 passivation certainly plays a part in the overall loss, nearly doubling the mirror loss (α_{mirror}) compared with the ideal case of two cleaved facet boundaries with no coatings.

While there is some sidewall roughness along the laser ridge, this roughness is not expected to contribute heavily to the loss of the optical mode since a majority of the optical power is concentrated near the active region and not near the surface of the

semiconductor and is not expected to interact substantially [224-226]. In Figure 3.17 this is illustrated clearly by considering the simulations of the optical mode profile in the laser ridge region. Payne *et al* presents a generalized model for loss due to waveguide sidewall roughness, where the exponential loss coefficient can be expressed as [226]:

$$\alpha = \varphi^2(d)(n_1^2 - n_2^2)^2 \frac{k_o^3}{4\pi n_1} \int_0^{\pi} \mathcal{R}(\beta - n_2 k_o \cos\theta)\, d\theta \qquad (5\text{-}8)$$

where R is the spectral density function, related to the autocorrelation function that describes the sidewall roughness, and $\varphi(d)$ is the modal field at the surface of the ridge and the remainder of the variables take their normal definitions for a slab waveguide formulation. Integrating the modal field along the ridge surface in simulations shown in Figure 3.17, the normalized value of $\varphi(d)$ is calculated to be 9.8×10^{-6}, which would essentially negate this loss term due to the sidewall roughness.

From laser I-V characteristics taken at two temperatures (10°C and 25°C) the characteristic temperature for this range, T_o, was calculated from the relation [187]:

$$T_o = \frac{T_2 - T_1}{ln(I_{th2}/I_{th1})} \qquad (5\text{-}9)$$

where $T_{1,2}$ are the two temperatures, and $I_{th1,th2}$ are the calculated threshold currents at each temperature. The calculated values were found to be between 20-25K for devices tested, smaller than the expected values of 50-100K for strained quantum well lasers, indicative of the pulsed testing setup and the very poor temperature stability these devices. The low value may be due to the poor thermal properties of the laser device, which is isolated from the surrounding semiconductor material by an encompassing trench also meant to electrically isolate the laser diode. The values

calculated for internal losses loss, however, are near the expected value for these materials [187, 227]. The relatively low forward resistances of the devices also suggest good ohmic contact formation for both *n* and *p*-type materials for these particular components under significant bias, however, the turn on voltages are higher than expected, which may be an indication of a potential barrier in the metal-semiconductor interface.

The wall-plug efficiency was also calculated which is simply the optical power out versus the input electrical power. This should be constant assuming that the output optical power is linear after threshold; the instantaneous value will vary however. Below is a plot of the wall-plug efficiency of the three exemplary devices.

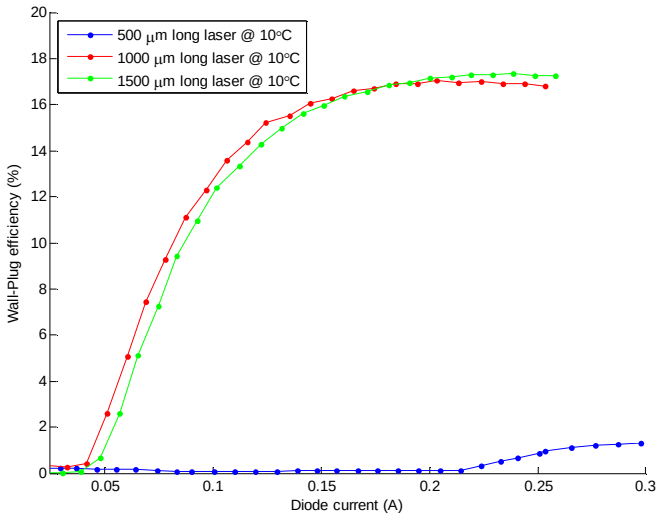


Figure 5.6. Plot of the wall plug efficiency versus the diode current.

Figure 5.6 shows that the maximum efficiency of the 1000 and 1500 µm long laser cavities are essentially the same, 17%, while the shortest cavity, 500 µm, has a maximum efficiency of 1.3%. This very large discrepancy indicates that the length of the 500 µm laser is not long enough for the device gain to overcome the internal losses in the laser material and mirror facets.

Not all devices in this first fabrication run exhibited laser characteristics, however it was directly attributed to poor cleaves which introduced cracked facets. Devices with these damaged facets did not lase at any temperature or input current, up to the catastrophic failure of the devices (~ 1 A of forward bias current). The poor cleaves were inspected via SEM imaging, an example of both cases is shown in Figure 5.7.

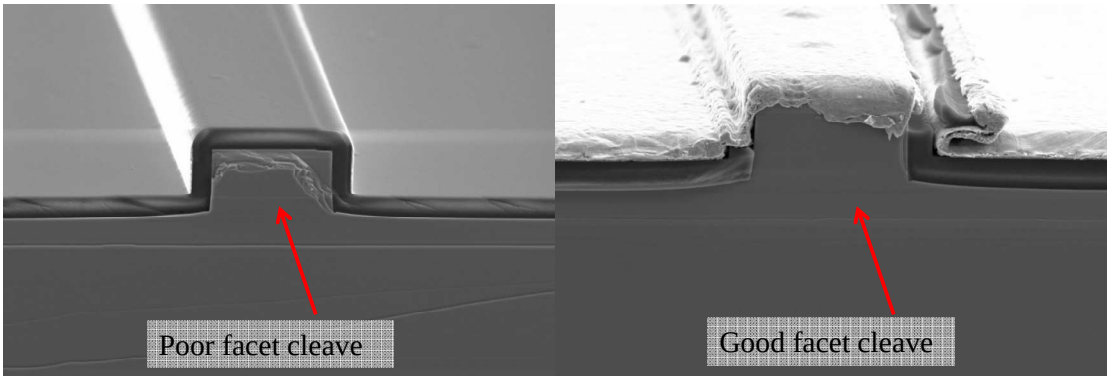


Figure 5.7. SEM images showing examples of a cracked facet and smooth facet after cleaving.

After these initial experiments were performed, the undercut and CO_2 critical point dry step (see section 4.1.6) was performed in order to release cantilever devices and suspended waveguides. This under-etching step inadvertently damaged the cleaved facets by etching away the Ga – and – As containing materials. All of the laser diodes were damaged in this way and exhibited no measurable lasing operation afterwards, with some devices exhibiting spontaneous emission at very high currents immediately before device failure. An SEM of a damaged cleaved facet is shown in Figure 5.8 along with a plot of before and after L-I-V characteristics.

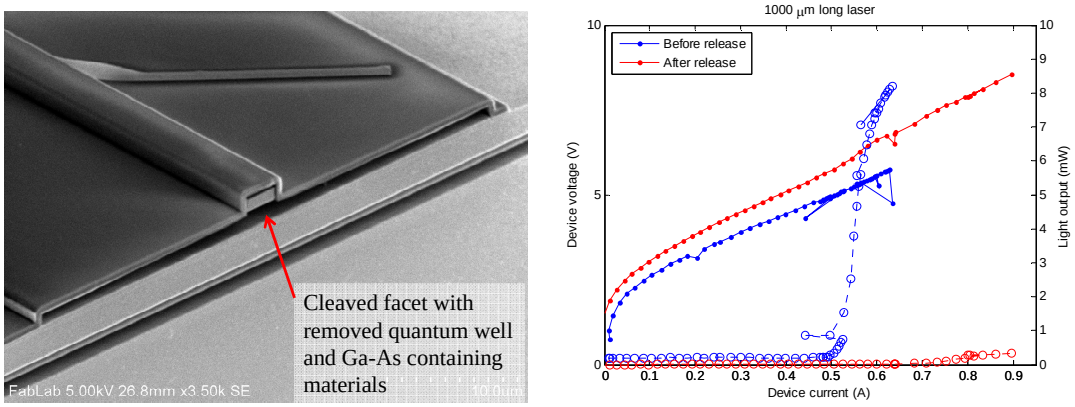


Figure 5.8. Left: SEM showing cleaved laser facet with completely removed InGaAsP quantum well regions. Right: L-I-V characteristics of the same laser diode before and after the undercut release.

5.1.3 Waveguide photodiodes

5.1.3.1 Testing setup and procedure

Waveguide integrated photodiodes were tested utilizing the same electrical probing and mounting schemes as listed for the laser testing, with contact being made to the photodiode *n* and *p* type contacts. The photodiode is illuminated with two methods: 1) a top-down out of plane approach with a closely placed, cleaved multimode optical fiber brought into proximity with the surface of the diode under test with a micropositioner stage. 2) An in-plane method utilizing a lensed fiber focused on a cleaved waveguide facet which directly couples to the photodiode via the integrated waveguide (see Figure 5.2). The first method is more convenient to measure without worry for waveguide quality or integrity since the waveguide propagation is bypassed; it does, however provide reduced absorption compared with the in-plane approach due to the very thin layer of absorber material.

The illumination source for these tests was a Photonetics Tunics PR wavelength tunable laser diode, set at the intended design wavelength of 1.55 µm. A

Stanford research systems (SRS) SR570 low noise current preamplifier is used as a high input impedance transimpedance amplifier to both reverse bias the PIN photodiode and measure its output photocurrent upon illumination. Laser intensity is controlled via an Eigenlight 420 in-line optical power monitor and variable attenuator. The semiconductor parameter analyzer is then used to sweep the applied voltage on the PIN diode and measure its I-V characteristics at varied illumination intensities. Throughout the testing procedure, the photodiodes are passively cooled via the copper heatsink and assumed to be at room temperature (25°C) during the experiments.

5.1.3.2 Photodiode testing results

The photodiodes were independently tested via top-down 1.55 μm illumination, as well as side illumination through the coupled waveguide. Incompletely undercut suspended waveguides caused total loss before the optical power reaches the waveguide photodiode due to the absorbing region below the waveguide when side illuminated tests were attempted. This loss rendered off-chip waveguide coupled photodiode measurements impossible. All photodiodes have identical dimensions and construction. Photodiodes showed dark currents of 47 nA (approximate current density of 1.1 $\mu A/cm^2$) and responsivity of 1.2 ± 0.16 mA/W at -2 V reverse bias. Figure 5.9 shows the dark as well as illuminated characteristic I-V plots of the photodiode structures.

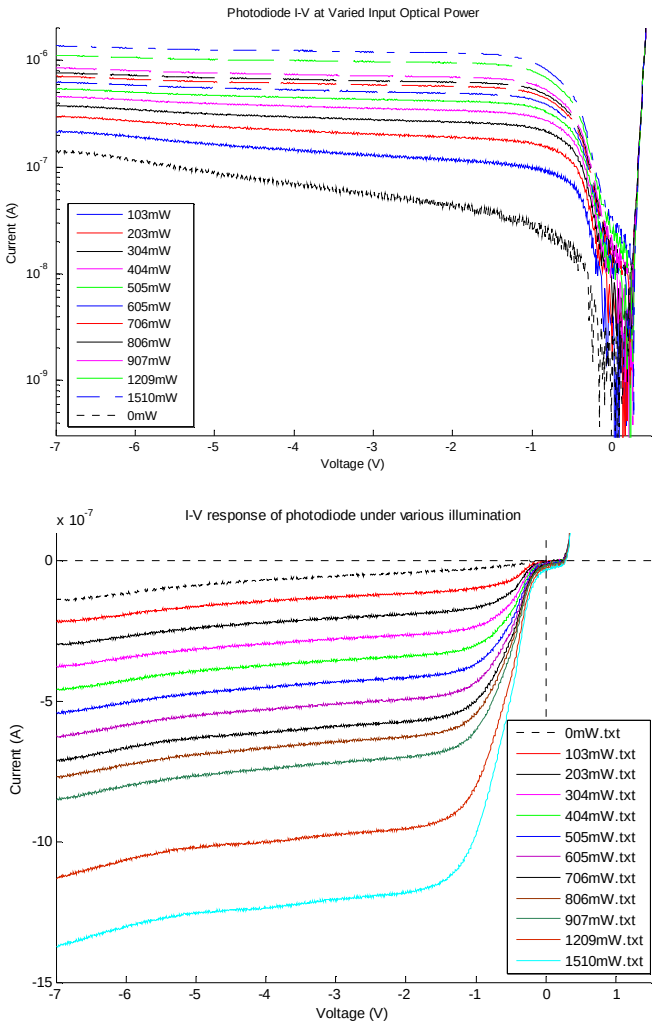


Figure 5.9. I-V curves of photodiode reverse bias characteristics under varied illumination intensities, top: semilog, bottom: linear.

5.1.3.3 Photodiode analysis

The photodiodes in this system were only tested via top illumination, not in the intended waveguide-coupled method due to a fabrication imperfection which did not allow for off-chip coupling. The area near the cleaved edge of the input waveguide did not get released by the wet under-cut etch, leaving the sacrificial and also absorbing material directly beneath the waveguides (see Figure 5.10). This caused significant optical loss and did not allow light to propagate through the waveguide. Testing with a cleaved multimode fiber suspended directly over top of

the photodiode region was instead used to independently test this component for photosensitive operation.

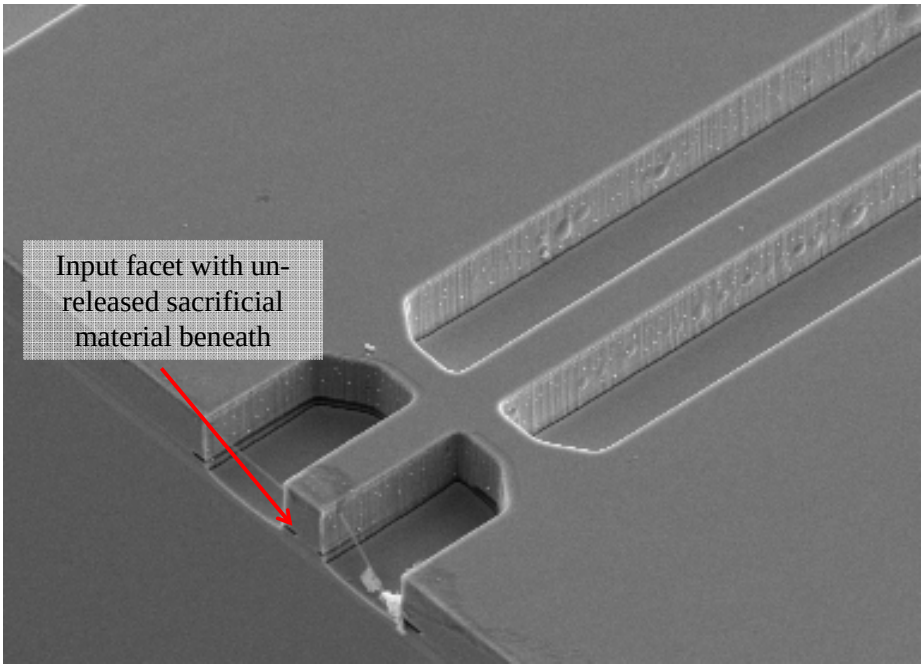


Figure 5.10. SEM of input waveguide facet showing un-released absorber at the input.

The internal quantum efficiency and responsivity were calculated for these devices under these illumination and test conditions. It was found that the output current of the photodiode "leveled off" at approximately -2 V of negative applied bias (see Figure 5.9), and this value was used for photocurrent calculations and voltage bias of the photodiode.

The primary photocurrent generated through the photodiode resulting from absorption in the depletion region, neglecting the minimal absorption in the quasi-neutral regions, can be expressed theoretically as:

$$I_{photo} = \frac{q}{h\nu} P_o (1 - e^{-\alpha t_{absorb}})(1 - R_{InP-Air}) \qquad (5\text{-}10)$$

where q is the electron charge, h is Planck's constant, v is the frequency of incident light, P_o is the input optical power, α is the absorption coefficient of InGaAs, t_{absorb} is the thickness of the absorbing region, and $R_{Inp\text{-}Air}$ is the reflection coefficient of the InP-Air interface, calculated in the usual way from Fresnel's equation:

$$R_{InP-Air} = \left(\frac{n_{InP} - n_{Air}}{n_{InP} + n_{Air}}\right)^2 \tag{5-11}$$

where n_{air} is taken as 1, and n_{InP} is taken as 3.1. Quantum efficiency is defined here as the number of electron hole pairs generated per absorbed input photon, and thus can be expressed as:

$$IQE = \eta = \frac{I_{photo}/q}{P_o/hv} \tag{5-12}$$

The responsivity is more general and can be seen as the total current versus the total input power incident, and can be expressed as:

$$Responsivity = \frac{I_{photo}}{P_o} = \eta\left(\frac{q}{hv}\right) \tag{5-13}$$

Considering equations (5-10) and (5-12), it can be seen that, theoretically, internal quantum efficiency should be independent of the input optical power. For this photodiode the InGaAs absorbing region is 250 nm thick, the incident optical radiation has a wavelength of 1.55 µm, and the absorption coefficient of InGaAs is taken as 2.3×10^3 cm^{-1} [188]. The theoretical upper-limit for the IQE for this illumination configuration is then calculated to be 4.12%. This very low value is due to the very thin absorbing region in this particular illumination configuration. Under side illumination the absorption thickness increases to 150 µm, increasing this theoretical value to a more typical 73.8%.

The output current versus the input optical power was very linear, as can be seen in Figure 5.11. The responsivity of the photodiode is calculated to be $1.065\pm0.038\times10^{-3}$ A/W from the linear fit to the plot in Figure 5.11. Equation (5-12) was used to calculate the measured quantum efficiency over the range of input powers shown in Figure 5.9, with an average IQE calculated to be 0.099±0.012%; an order of magnitude less than the theoretically calculated quantum efficiency. The poor quantum efficiency and the disparity between the measured values and theoretical can be attributed to a number of non-ideal testing conditions, such as the top-down illumination conditions of this testing setup, un-accounted for illumination spot size variation from the cleaved optical fiber, and any fluctuations in output optical power due to fiber kinks or downstream optical power measurement errors.

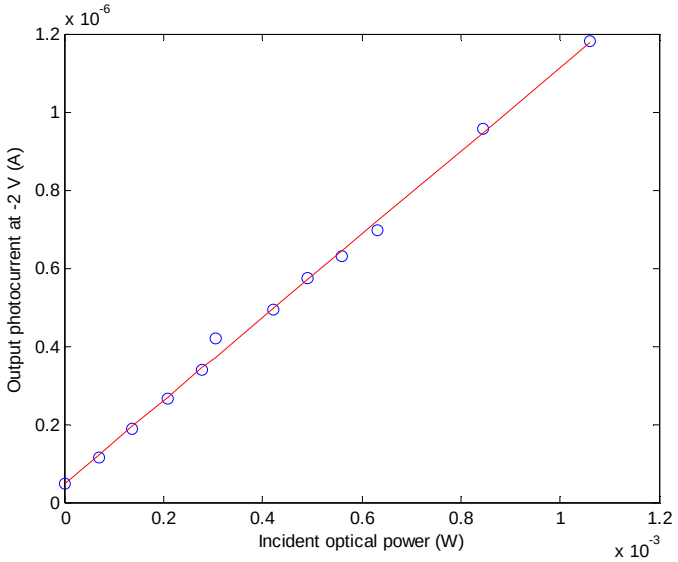


Figure 5.11. Output photocurrent at -2V revers bias versus input incident optical power.

Shunt resistance was measured by calculating the slope of the reverse bias current at -2 V, and was found to be inversely proportional with the input optical power and varied from 90 to 13 MΩ. Figure 5.12 shows this relationship. This

varying shunt resistance and relatively high dark current for this diode indicate the presence of bulk material or surface defects which contribute to leakage currents. Since no variation in diode geometry exist for this fabrication mask, determining the main contributor to this leakage current experimentally is difficult, however conceptually, it can be assumed that the likelihood of fabrication defects along the edge of the un-passivated photodiode are much higher than internal bulk defects.

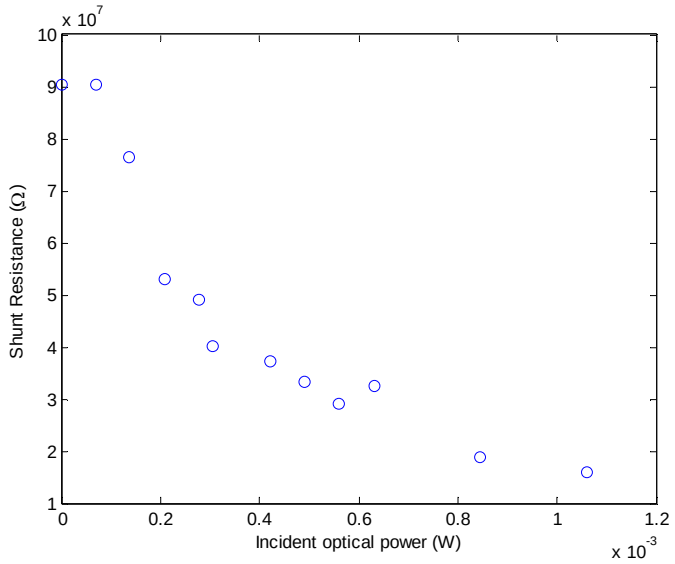


Figure 5.12. Shunt resistance versus the input optical power.

To calculate the minimum detectable power of this configuration we consider the RMS noise due to dark current and shunt resistance in the photodiode, expressed as:

$$\langle {i_{shot}}^2 \rangle = 2q(I_{dark})\Delta f \tag{5-14}$$

$$\langle {i_{Johnson}}^2 \rangle = \frac{4k_b \mathrm{T}\Delta f}{R_{shunt}} \tag{5-15}$$

where q is the electron charge, I_{dark} is the dark current, k_b is Boltzmann's constant, T is the temperature, R_{shunt} is the shunt resistance, and Δf is the measurement bandwidth. Since this device is operated in reverse bias mode, the shot noise will dominate and

the Johnson noise in the circuit will be minimal. The minimum detectable power can then be expressed as the sum of the two noise contributions divided by the responsivity:

$$P_{min} = \frac{\sqrt{\langle i_{shot}{}^2 \rangle + \langle i_{Johnson}{}^2 \rangle}}{Responsivity} \tag{5-16}$$

For this calculation we use the measured dark current 4.69×10^{-8} A and the bandwidth due to sampling measurement as 780 Hz, T as 293 K, and the responsivity as calculated above from the straight line fit in Figure 5.11. The minimum detectable input optical power with this illumination configuration and reverse bias condition is calculated then to be 3.24 nW.

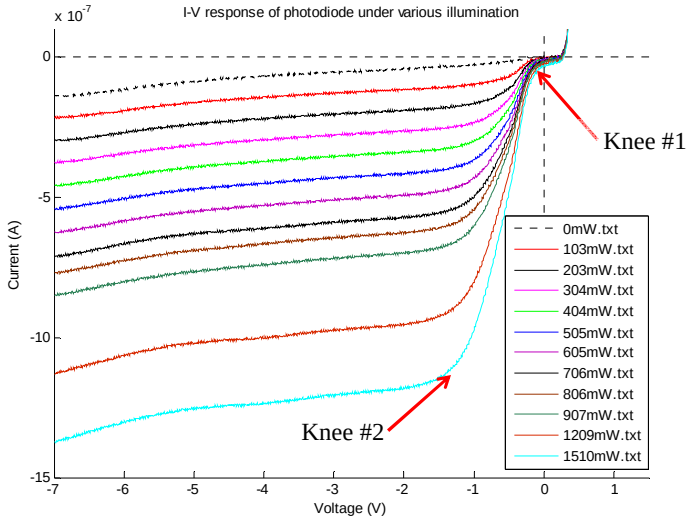


Figure 5.13. Linear I-V characteristics of the photodiode under various illumination powers.

Of note is that the reverse bias I-V characteristic in Figure 5.13 shows two "knees," with the primary photocurrent generated well into reverse applied bias rather than at 0 V bias as one might expect for a PIN photodiode operating in photovoltaic mode. The double knee reverse bias characteristics indicate that the active absorbing region is not fully depleted at 0 V reverse bias, due to a residual n-type doping in the

"undoped" sacrificial layers [228]. Once the core absorbing portion of the intrinsic region structure is fully depleted (after approximately -1 V of reverse bias) and the excess carriers swept away by this sufficiently large voltage, the photodiode produces substantial photocurrent in the typical fashion.

A Schottky barrier is also a possible cause of this additional knee. A crude approximation of the built-in voltage for a Schottky barrier diode can be taken as: $V_{bi} = (\varphi_{Metal} - \varphi_{Semi})/q$. From Figure 5.9 and this first knee appears at ≈-0.65-0.75 V, which is the estimated Schottky built-in-voltage of the *n*-type contact considering the work functions of nickel (5.15 eV) and InP (4.38 eV). This indicates a possible problem with the annealing of the *n*-type contact materials. No contact resistance measurement structures were included in the mask design in order to independently verify this, however the *n*-type region for the PIN diodes were exposed to a large number of plasma steps, which may have caused a degradation in the contact resistance of this specific contact [211, 229]. This was not observed in the laser diodes, however at the high forward bias voltages of the laser diodes we would expect any Schottky barriers to conduct and this effect would be less prominent and may not be apparent in the laser I-V characteristics.

As the device was not optimized for optimal photodiode performance and tradeoffs were made to facilitate the integration of this photodiode structure into the larger MEMS cantilever waveguide measurement scheme, the poor photocurrent and unintentional 0 V bias characteristic is understandable. The primary shortcoming in this experiment, however, lies in the testing and measurement setup where a photodiode not designed for top-down planar excitation was measured by such a

method due to the limitations imposed by the fabrication imperfections. This caused predictably low responsivity and quantum efficiency that would undoubtedly be improved by side-illumination.

5.1.4 Cantilever waveguides

5.1.4.1 Testing procedure

Separate cantilever devices are tested via micropositioner probes in contact with the topside bias and actuation electrodes. A potential difference is applied between the grounded bias electrode and the actuation electrode using a function generator in order to move the cantilever waveguides. Measurement of the motion of the cantilever waveguides was performed optically as described in section 3.1.6. 1.55 µm laser light from the aforementioned tunable laser source was coupled into a suspended on-chip waveguide with a lensed fiber (mode field diameter of 5 µm), and coupled off-chip with an identical lensed fiber in order to simplify the process of coupling on and off of the chip. This fiber was then coupled to a NewFocus 1811-FC high speed photodiode to measure the modulated optical power. Measurements of cantilever motion were limited to DC actuation due to substrate current leakage and capacitive losses which caused high frequency actuation to fail.

In addition to this standard measurement, attempts to visualize cantilever motion were performed via scanning electron microscopy imaging of a device under test. Cantilever waveguide contacts were wire bonded to a diamond submount and copper block package to provide for electrical connections through vacuum

feedthroughs. DC voltage was applied to the bias and actuation pads while inside of the SEM vacuum chamber and monitored via the SEM secondary electron detector.

5.1.4.2 Cantilever resonator testing results

Both fabrication runs tested produced no electrostatically actuatable cantilever waveguides. This was estimated to be caused by a combination of factors: incomplete undercut etching, residual sacrificial layer-induced stiction, and significant current leakage. Since the difficulties associated with the actuation of these cantilever devices are closely related to the other signals being applied to the integrated devices, cantilever actuation studies are lumped with a more generalized analysis and discussion in section 5.1.7 which covers the various efforts to measure the device actuation and the origins of the failure mechanisms.

5.1.5 Cantilever waveguide and PIN photodiode testing

Cantilever waveguides integrated with PIN photodiodes were tested separately from devices which also contained integrated laser diodes to validate their operation. The off-chip tunable 1.55 μm laser diode source was coupled onto the chip via a lensed optical fiber as with the PIN photodiode measurement previously (see section 5.1.3.1). Four micropositioner probes were used to make contact to the two cantilever bias and actuation electrodes and the *n* and *p* contacts for the PIN photodiodes. The cantilever contacts were connected to a function generator, while the PIN photodiode contacts were connected to the SRS transimpedance amplifier. The PIN photodiodes were operated in photovoltaic mode with 0 volts reverse bias applied across the *p* and *n* contacts with the *p*-type contact grounded to reduce

parasitic coupling between the photodiode and the cantilever actuation electrodes. An oscilloscope measured the actuation signal as well as the photodiode photocurrent during actuation. The function generator was set to provide a 0 volt minimum voltage at all times with varying amplitudes by introducing a DC offset in the signal. This assures that the actuation contact for the cantilever resonator remains the same polarity at all times during testing.

As with the cantilever waveguide resonators, devices were also tested while monitored by a SEM in order to visualize attempted cantilever actuation. All four contacts were wirebonded to the diamond-copper submount assembly to provide electrical connections via chamber feedthroughs.

5.1.6 Full system testing

The full system was tested in the same manner as the above subcomponents. The chip with the integrated devices was mounted on a diamond submount, and then mounted to a copper block. Six micropositioner probes provided electrical connection to the *n* and *p* laser diode contacts, the cantilever bias and actuation pads, and the *n* and *p* PIN diode contacts. The laser diode was attempted to be operated in CW mode in order to reduce parasitic capacitive coupling to other components in the system. The PIN photodiode was operated in photovoltaic mode once again, with 0 volt applied bias and the *p*-type contact grounded. Cantilever waveguides were actuated via a 0 volt minimum square wave signal provided by the function generator.

5.1.7 Results of coupled component testing

Due to fabrication imperfections and inoperable laser devices, the testing of all system components simultaneously was not successful. A number of issues that all traced back to deficiencies in the contact isolation became apparent through these failed experiments. The following section presents the data taken to analyze the contact isolation across the fabricated chip and the failure analysis of this aspect of the devices.

5.1.7.1 Contact and actuation pads current isolation and testing results

Unlike many conventional MEMS devices fabricated on top of insulating sacrificial layers and substrates, III-V MEMS devices are necessarily separated by semi-insulating or intrinsic compound semiconductors which can conduct if biased in the correct direction. The I-V characteristics between the device contact pads, isolated by epitaxial semiconductor junctions rather than insulators, were measured to establish the actuation voltage limitations whereby effective isolation is maintained and to discover potential parasitic paths in the final devices.

Figure 5.14 – Figure 5.21 contains diagrams illustrating the six contact points, and the I-V characteristics between each of the contact points on the device. Inset into each of these diagrams is the measured I-V characteristics of the specific configurations showing the theoretical current paths. Qualitatively it was observed that contact pairs with similar circuit pathways exhibited similar shaped I-V characteristics.

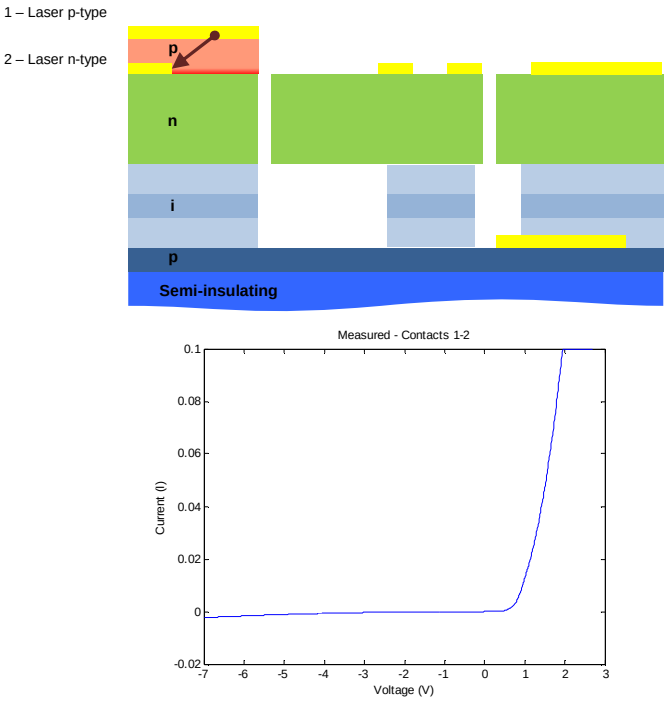


Figure 5.14. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

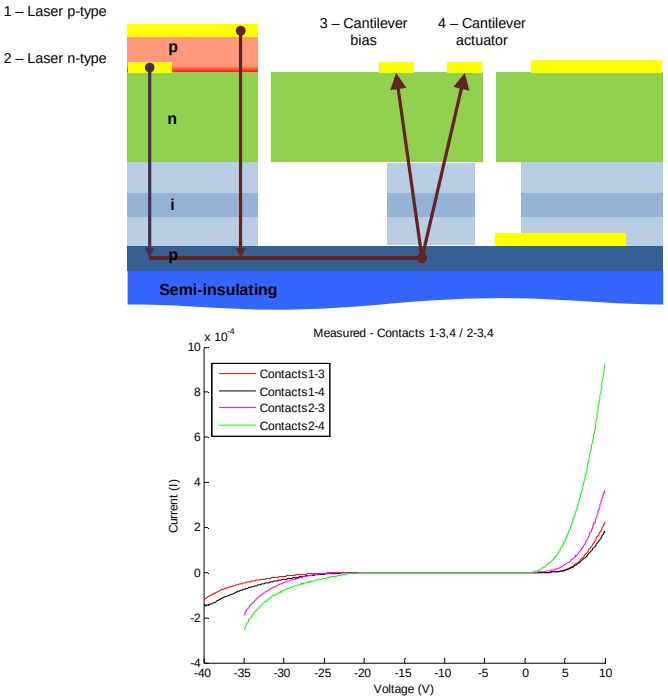


Figure 5.15. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

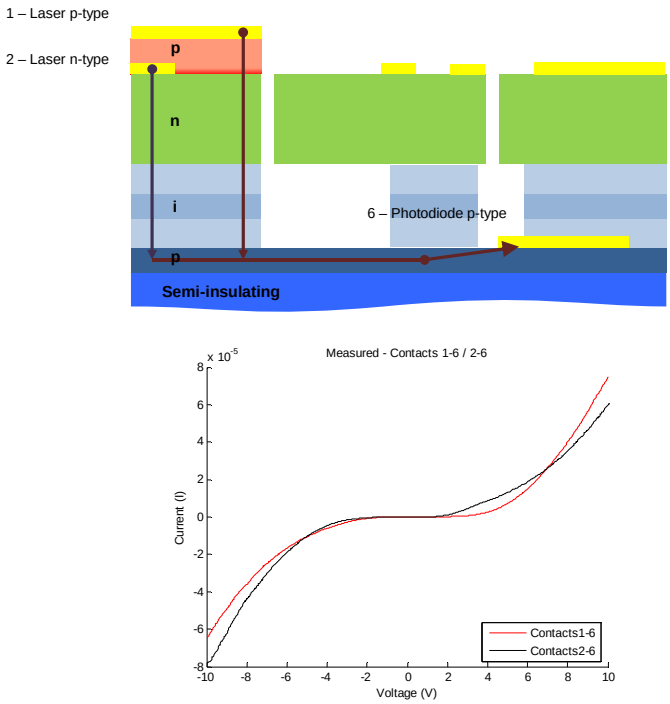


Figure 5.16. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

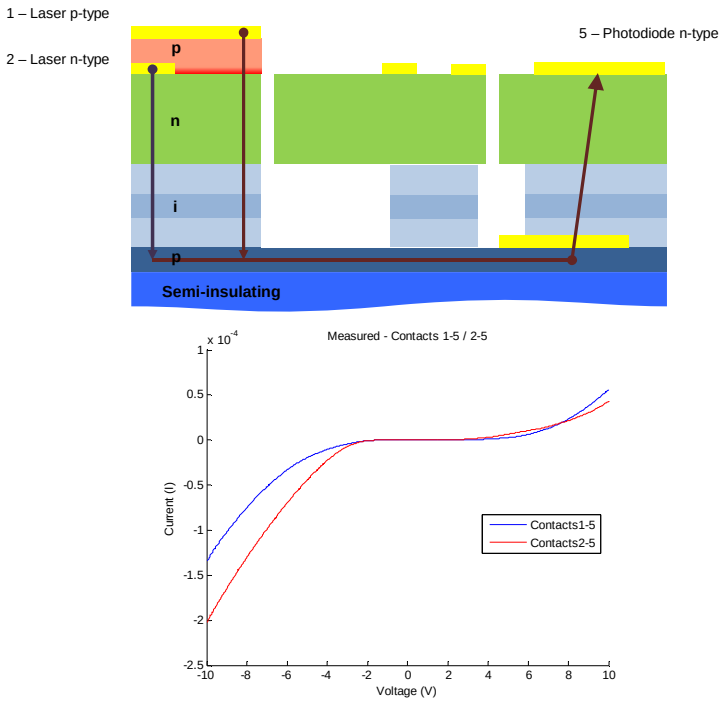


Figure 5.17. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

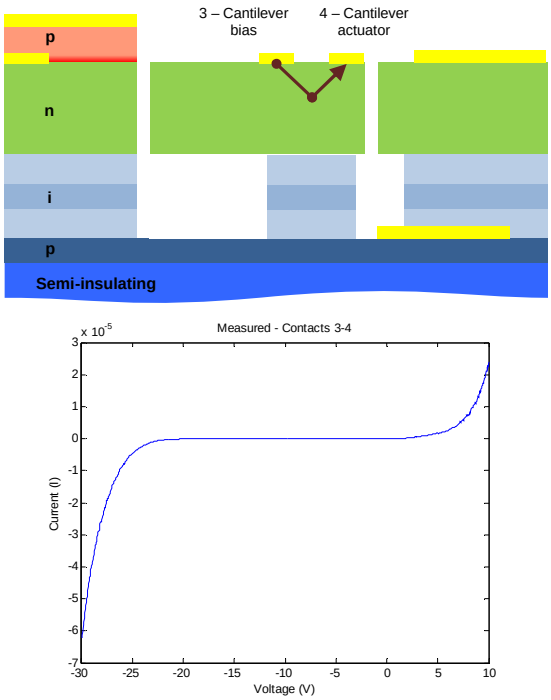


Figure 5.18. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

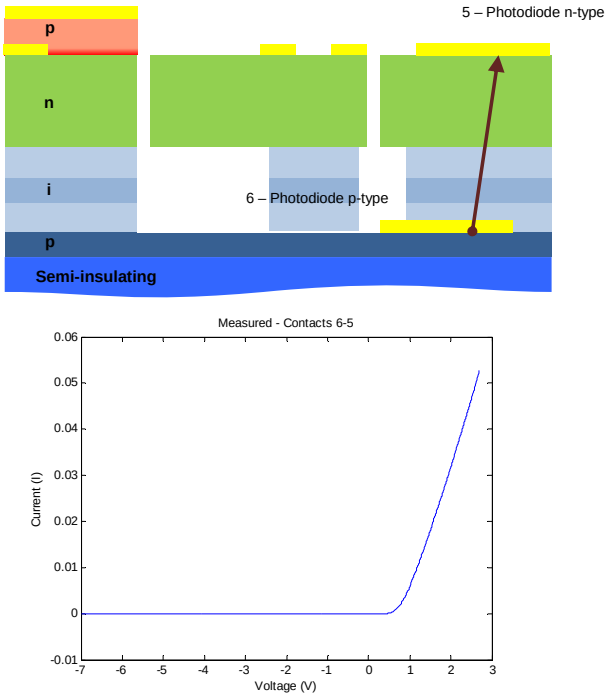


Figure 5.19. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

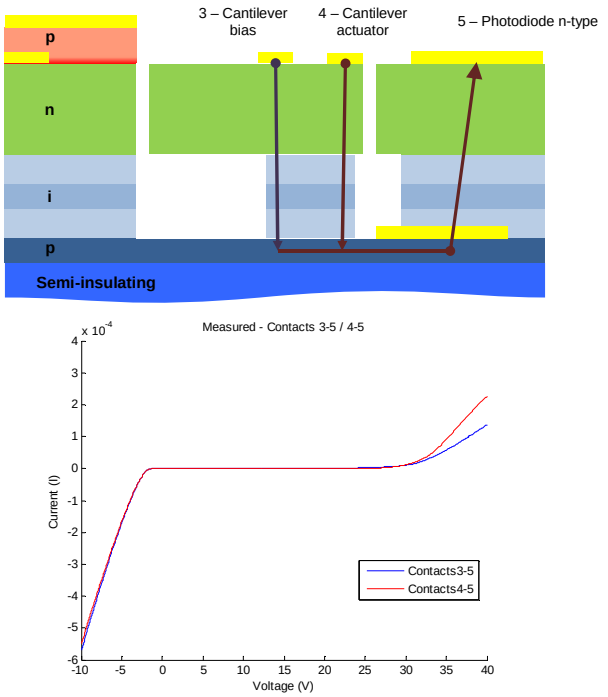


Figure 5.20. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

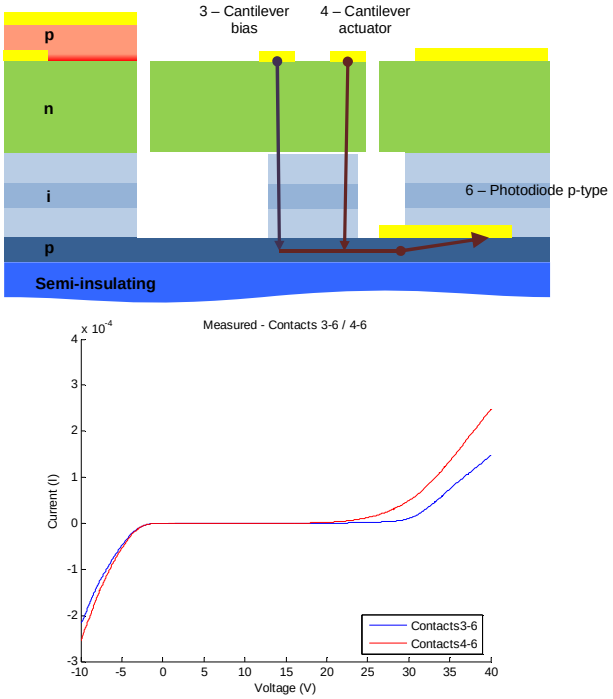


Figure 5.21. Device cross-section and numerated contact points. Numbers on cross-section coincide with labels on graphs. Red arrow indicates current path being measured.

5.1.7.2 Exploration of contact isolation and cantilever actuation failure

Contact isolation proved to be a pervasive flaw in nearly every component of the integrated system, particularly evident in the cantilever actuation scheme and the photodiode measurement.

The III-V MEMS devices fabricated in this work were separated and electrically isolated through deep trench isolation etches into a semi-insulating (Fe^+ counter-doped InP wafer) and reverse biased *p*-*n* junctions (See Figure 4.25 and Figure 5.14). Unfortunately, these junctions and current paths are not always non-conducting. As can be seen in Figure 5.15, there are clear current paths that are opened above ~5 V applied bias between actuation pads and photodiode contact pads. This proved to be detrimental in the measurement of cantilever motion with the integrated photodiodes, as the crosstalk between the actuation signal and the measurement signal became large enough to obscure any possible cantilever motion.

Independent verification of the cantilever waveguide motion via microscopy under a DC applied actuation signal was undertaken in an effort to decouple the effect of contact pad crosstalk. Cantilever motion is traditionally very small for low voltages, fractions of a micron (see Figure 3.9 for an example), and investigation under standard optical microscopes proved to be inconclusive during applied actuation. A SEM with feedthroughs for in-situ actuation of wire-bonded cantilever pads was used in an attempt to achieve higher resolution and precision in measuring cantilever motion. This measurement did not yield any measurable cantilever actuation, however did inadvertently provide information about parasitic current paths across the surface of the device via voltage-contrast SEM imaging. Voltage-contrast

SEM imaging “lights up” areas of negative voltage (repelling electrons and increasing the yield of electrons to the electron detectors) and darkening regions of positive voltage bias (attracting electrons reducing the electron yield in these regions). It was discovered that the trench isolation etch was not sufficient to completely isolate the laser diode, actuation pads, and photodiodes and followed a seemingly random pattern of leakage that was directly related to small fabrication imperfections resulting from aspect ratio dependent etching depths.

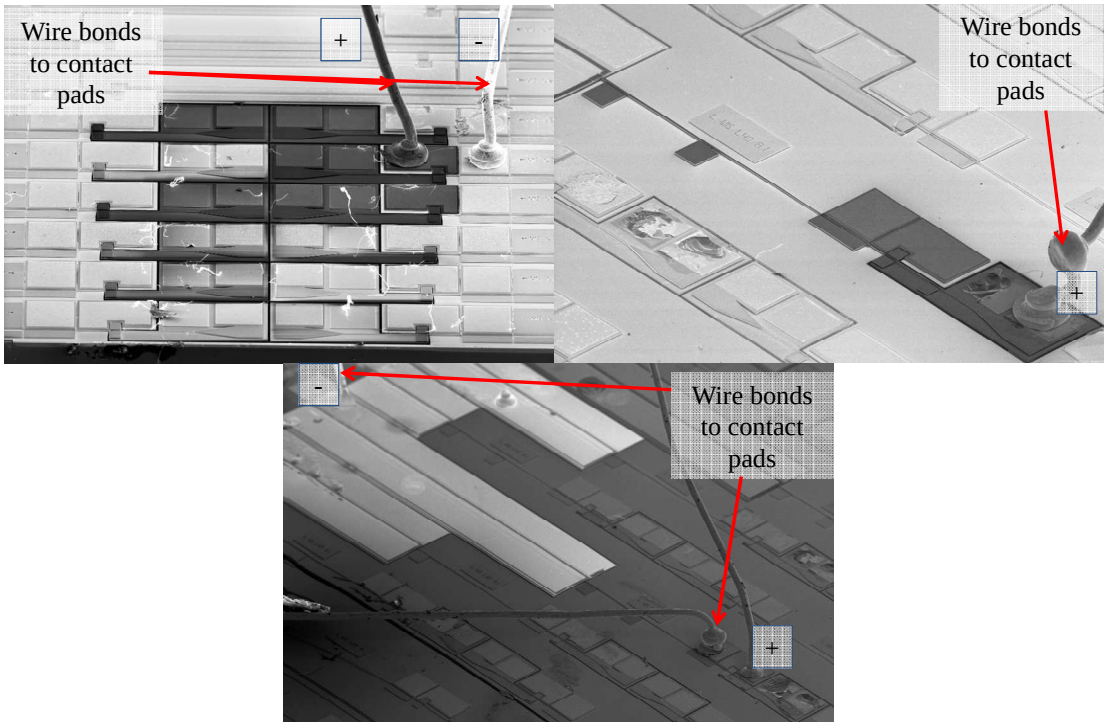


Figure 5.22. Voltage contrast SEM imaging of devices, showing current pathways through in-situ voltage application. Dark areas have positive voltage applied, and light areas have negative voltage applied.

The substrate resistance was estimated by fitting a straight line to the I-V curves in the forward and reverse biased conditions measured between the *n*-type cantilever actuation and bias pads and the bottom photodiode contact (3 and 4 contact pads, see Figure 5.14 and Figure 5.15). These particular contacts were chosen since they provide the most direct path through the substrate only 100 and 30 µm apart, to

reduce the measurement error due to current spreading. Through the laser and photodiode I-V curves, we see that forward resistances are very low, indicating that the contact resistance of each pad is negligible. In such a case, the forward bias slope is approximately equal to the resistance through the semi-insulating substrate. This was calculated to be only 58.8 kΩ-m; three orders of magnitude lower than the expected resistivity from the manufacturer specifications (30 MΩ-m). This indicates a number of additional pathways between the contacts that were not taken into account such as residual bottom-contact layer material (layers #1 and 2 in Table 3.1) not etched through during the deep trench etch and waveguide etch. Often, the undercut etching step does not completely remove the sacrificial layer during the wet undercut etch, providing an additional current path. Additionally, conduction paths can form across unpassivated sidewall and trench surfaces due to etch damage [211, 229].

Also discovered via SEM inspection was the incomplete removal of portions of the sacrificial undercut layer directly beneath the cantilever and in the surrounding structures, as indicated in Section 4.1.6. The aspect-ratio dependent etching in these narrow regions such as the cantilever actuation gap and the isolation trenches surrounding the cantilever actuation and bias pads (< 2 μm) reduced the overall etch depth to below this slower-etching layer, and thus they remained intact. With only 250 nm of spacing between this thin layer and the waveguide cantilever regions, stiction often occurred for free cantilevers preventing motion. SEM images illustrating this phenomenon are shown below in Figure 5.23. In addition to this, the thin membrane-like structure bridged the isolation gap between adjacent contact pads,

introducing other current paths (see Figure 5.24). These current paths may have prevented sufficient a sufficient voltage difference to be generated between the bias-actuation pads, which prohibited electrostatic actuation.

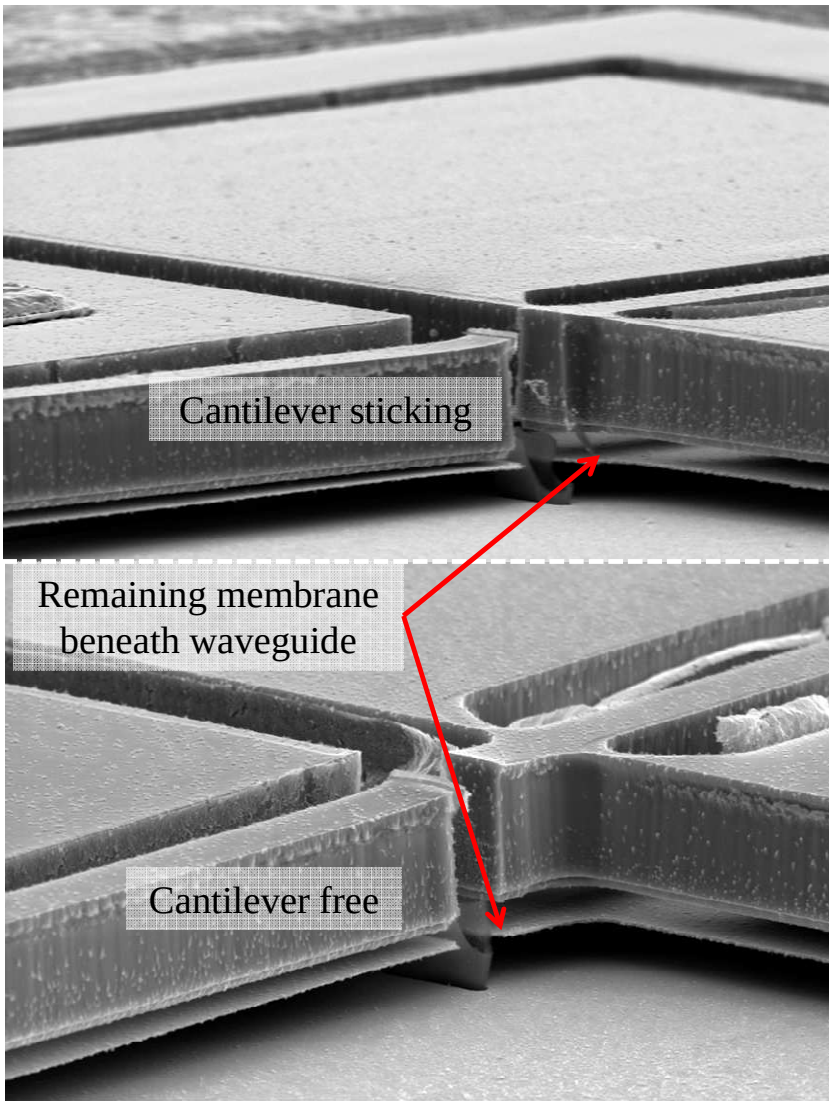


Figure 5.23. SEM images of released cantilever tips showing unetched layer beneath

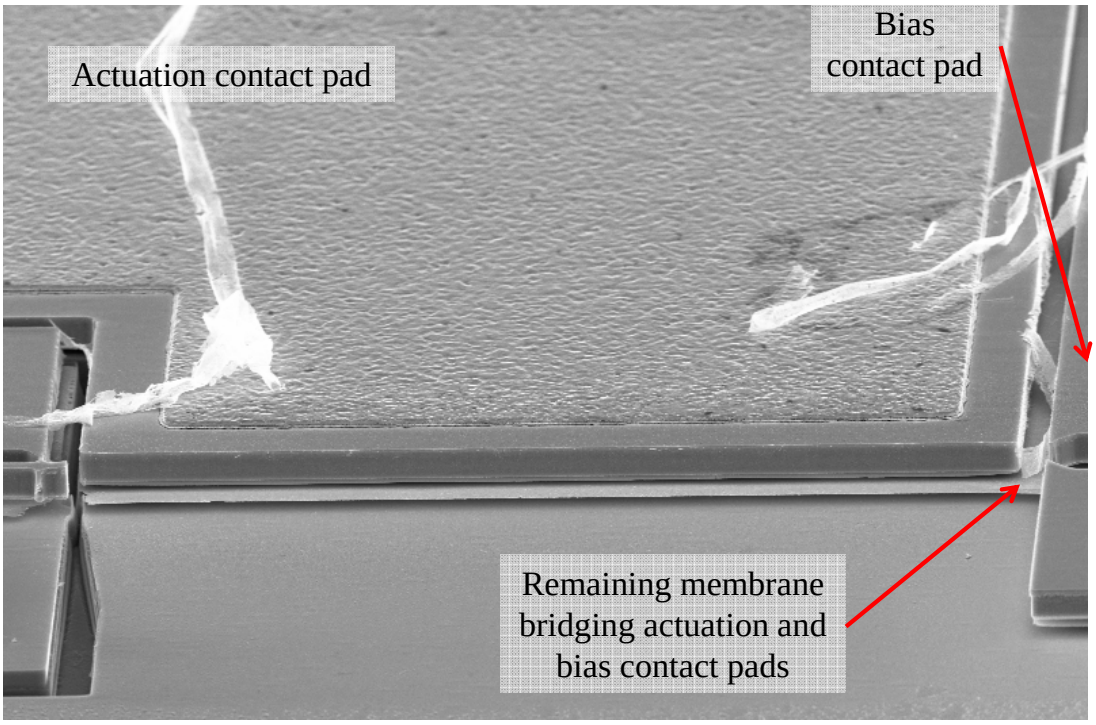


Figure 5.24. SEM of actuation-bias contact pad region with cantilever resonator removed, showing the underlying membrane and the bridging of the separation gap.

This thin membrane beneath the cantilever may have been biased along with the side-electrode, causing uneven actuation force and may have caused stiction early in the testing cycle. To test this hypothesis, simultaneous actuation of the cantilever beam was performed and measured by a KEYENCE VK-9700 laser-scanning non-contact profilometer. This tool scans a violet laser across the field of view of a microscope objective, measuring intensity of the reflected beam as the stage is moved in the z-direction. By tracking the maximum reflected power as the sample is translated through the z-direction, information about the topography of the sample can be determined. Comparison of cantilever vertical and in-plane displacement showed no appreciable difference at 0, 7, and 10 V of applied bias. Figure 5.25 shows a plot of the normalized height measured by the optical profilometer at these three applied voltage bias conditions. These results indicate that there is not

sufficient voltage bias between the cantilever and actuation pads in order to facilitate electrostatic actuation. The cantilever is already stuck in this experiment as can be seen via the downward bending of the profile, however from Figure 5.23, we see that a majority of the beam is free and should experience some sort of bending motion upon actuation.

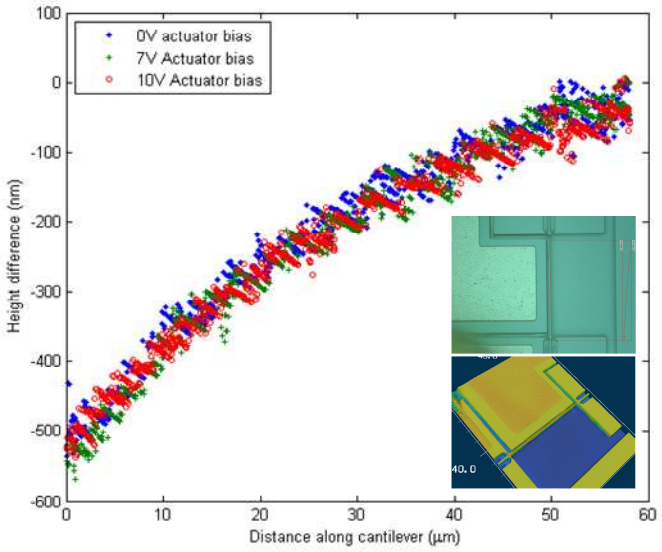


Figure 5.25. Plot of normalized height along the top of the cantilever during applied voltage. Right side is clamped portion of the cantilever. Inset shows microscope and false-color 3D image from optical profiler.

In the future, a different layer structure should be to be chosen without these thin cladding layers in the absorbing/sacrificial region regardless of the slight benefit they offer. These layers caused there to be physical stops to cantilever motion, poor undercut, as well as and enhanced current path between A more effective electrical isolation scheme needs to be employed for this particular cantilever actuation design. A method for achieving this is to obtain deeper isolation trenches facilitated by physically larger (> 2 µm) gaps between bias and actuation electrode islands to mitigate the aspect-ratio-dependent etch depth that occurs with very narrow trenches.

It was also found that attempting such a deep trench isolation etch with smooth sidewalls is impractical, and the implications of not etching deep enough through the epitaxial layer structure cause significant problems in the operation of the final devices. A re-design of the mask layers that incorporates larger trenches and gaps, along with re-ordering of the etching and patterning steps in order to reduce the stringent etching requirements can assure that the etch depths to achieve electrical isolation are met, alongside the other patterning requirements as discussed in sections 3 and 0.

Fabrication run 2

In order to proceed further with integrated testing of all three components and attempt to perform full-system testing, the laser diodes needed to be functional. In this manner, the laser diodes could be operated while the cantilever devices were moved in order to perform a measurement of the displacement via optical methods. A simplified solution was established to combat the undercutting of the active region during undercut and release in order to produce working laser diodes as well as released cantilevers and waveguide devices. The un-released cleaved facet edge was coated with photoresist in order to protect it during the wet etch release process. This solution was effective in protecting the facets from being under-etched, and was used to facilitate the completion of a second fabrication run. These devices were tested in the same manner as fabrication run 1, with the same setups for CW and pulsed laser testing being used.

5.1.8 Laser testing results

Upon testing these devices, the forward resistance and diode turn on characteristics were favorable, however no lasing operation was observed, as can be seen in Figure 5.26. A number of hypothesis were developed and tested via simulation and device testing in an attempt to explain the inoperability of all laser cavities on this device.

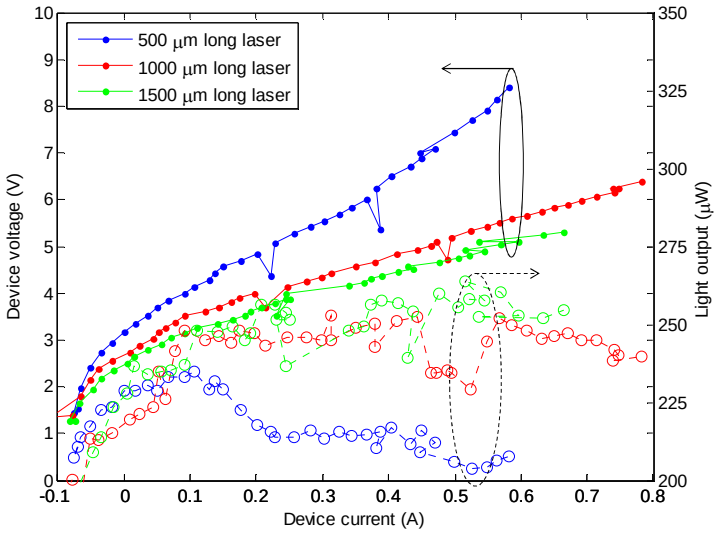


Figure 5.26. Example of LIV curves for second fabrication run devices.

The laser cavity facets were first considered as the source of excess loss that was preventing positive optical gain in the laser cavity. As previously, cracked or damaged cleaved facets will prevent reflection from a cavity mirror (see Figure 5.7). SEM was used to inspect the cleaved facets of the second fabrication run and to establish which devices to test. This device screening proved to produce no difference in optical output between devices with smooth cleaved facets and damaged facets.

The etched facet coated with Si_3N_4 was also considered, due to the low reflectivity from this mirror as a consequence of the dielectric coating. The already poor efficiency of the laser material may be compounded by this very low reflection from the etched laser facet. An attempt to remove this material was made in order to boost the reflectivity of this cavity mirror. Due to misalignment of the Si_3N_4 passivation mask, a number of laser cavities did not have Si_3N_4 coating this etched facet natively. These devices were selected for electrical and optical characterization as well as a number of samples which had the Si_3N_4 material removed from the etched facet sidewall with a RIE plasma etch. SEM images of both cases are shown in Figure 5.27 and Figure 5.28. Upon pulsed LIV testing of these selected laser cavities, the optical characteristics were again indiscernibly different between natively Si_3N_4-free, Si_3N_4 removed via RIE, and normal coated facets. Figure 5.29 shows the output optical power from each of the facets, cleaved and the etched facet as well as a trace with the photodiode input blocked, or "blanked."

Figure 5.27. SEM of before and after Si_3N_4 removal via RIE etching. Residual dielectric can be seen deep in the trench, indicating removal of the coating.

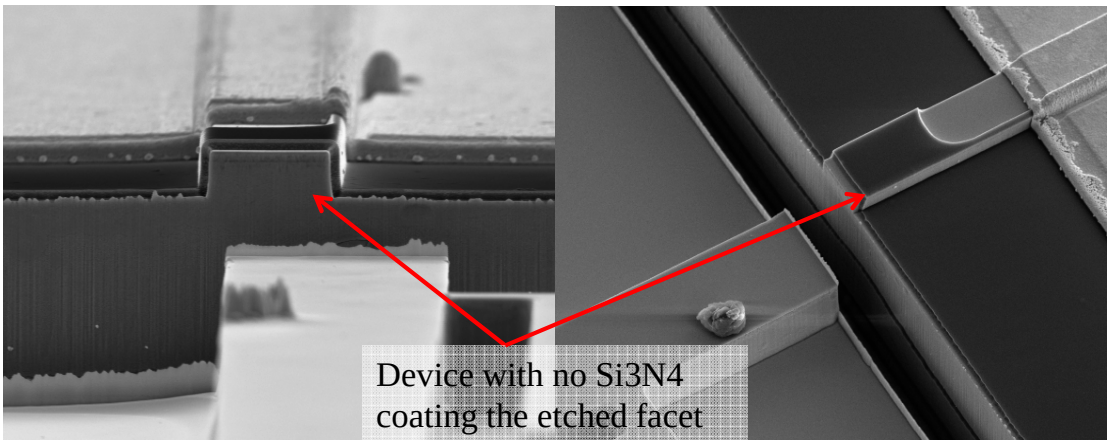


Figure 5.28. SEM of device with misalignment errors that left it natively un-coated.

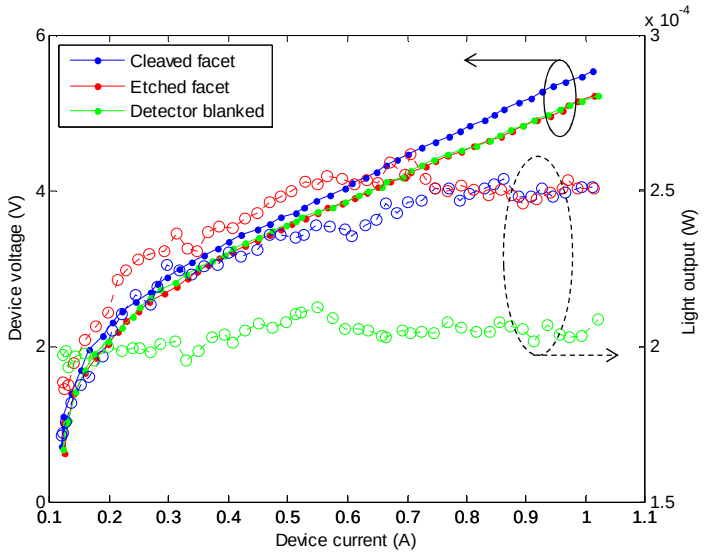


Figure 5.29. LIV curves of a device that has had the nitride removed, measured at each facet and with the detector blanked.

The SEM images in Figure 5.27 and Figure 5.28 show that the etched laser facets appear slightly rough due to the ICP etching procedure. Facet reflectivity will be affected due to this surface roughness. We can estimate the facet reflectance (R) due to a RMS surface roughness (Δd) compared to that of a perfectly smooth facet (R_o) with the following relation derived from Huygens's diffraction [230]:

$$\frac{\mathrm{R}}{R_o} = e^{-(4\pi n \Delta d/\lambda)^2} \tag{5-17}$$

A plot of this reduced reflection versus the RMS roughness of the facet is shown in Figure 5.30 for the specific case here with the laser wavelength, λ=1570 nm and effective index of the primary laser mode as n=3.23.

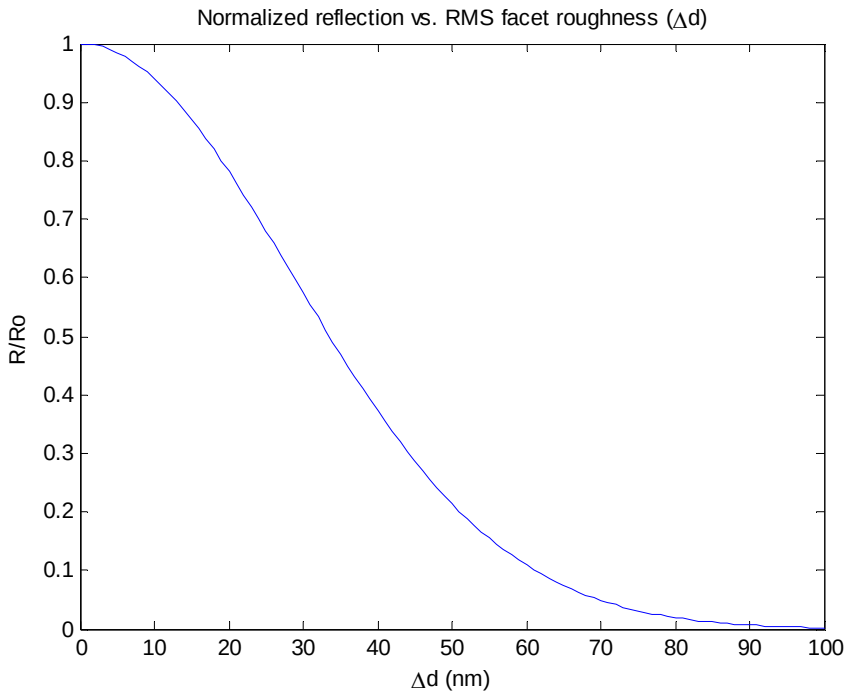


Figure 5.30. Facet reflectance versus the RMS roughness of the laser facet for the case of the fabricated laser diodes.

From the SEM's we see that for much of the area underneath the ridge it is very difficult to make out any surface roughness whatsoever. We can place an estimate of the roughness to be between 10-20 nm, which is near the minimum resolvable feature with our SEM. From equation (5-18) we see that this would introduce an approximately 6%-20% reduction in the reflectance compared to a perfectly smooth surface, reducing the reflectivity from 27.85% to 26.14% or 22.28% for the best and worst case roughness scenarios. Although this is a gross estimate since no AFM measurement of the facet roughness was performed, Figure 5.30 and

equation (5-18) indicate that for these specific devices the facet roughness is an unlikely source of reflection loss as far as the observed facets are able to show in SEM inspection. Much larger (closer to 35 nm in order to reduce reflection by 50%) and more obvious defects are required to obtain appreciable loss due to the facet roughness.

As demonstrated in section 5.1.2.1, the sidewall roughness of the laser ridge should not produce significant loss compared to other factors. Furthermore, it will be shown in section 5.1.10 that the surfaces of the ridge play even less of a part in the propagation of the primary lasing mode from this second fabrication run due to the more shallow ridge compared with the first fabrication run and thus this aspect was not considered in the loss considerations.

The final attempt to increase the reflectivity of this laser facet was taken by attempting to re-cleave the device near the etched facet edge. This will shorten the laser cavity, but will provide for a laser cavity that has two cleaved facets as is traditionally done for laser bar fabrication. This cleaving process was practically difficult due to the very narrow sample width, but was successful in producing lasers with a cavity length of 750 µm long after the second cleaving step. Once again, the standard pulsed LIV testing of these laser diodes at 10°C yielded no stimulated emission and no substantial difference in the I-V characteristics beyond a slight change in the device forward resistance. This change is expected since the electrical contact area was changed. What is observed is a possible measure of spontaneous LED-like emission; however it is likely that this is due to radiated heat from the laser diode. See Figure 5.31 for a visualization of the location of this new cleave. Figure

5.32 shows a plot of the LIV characteristics with optical power measured from both facets, as well as the background noise when the photodetector input is blanked.

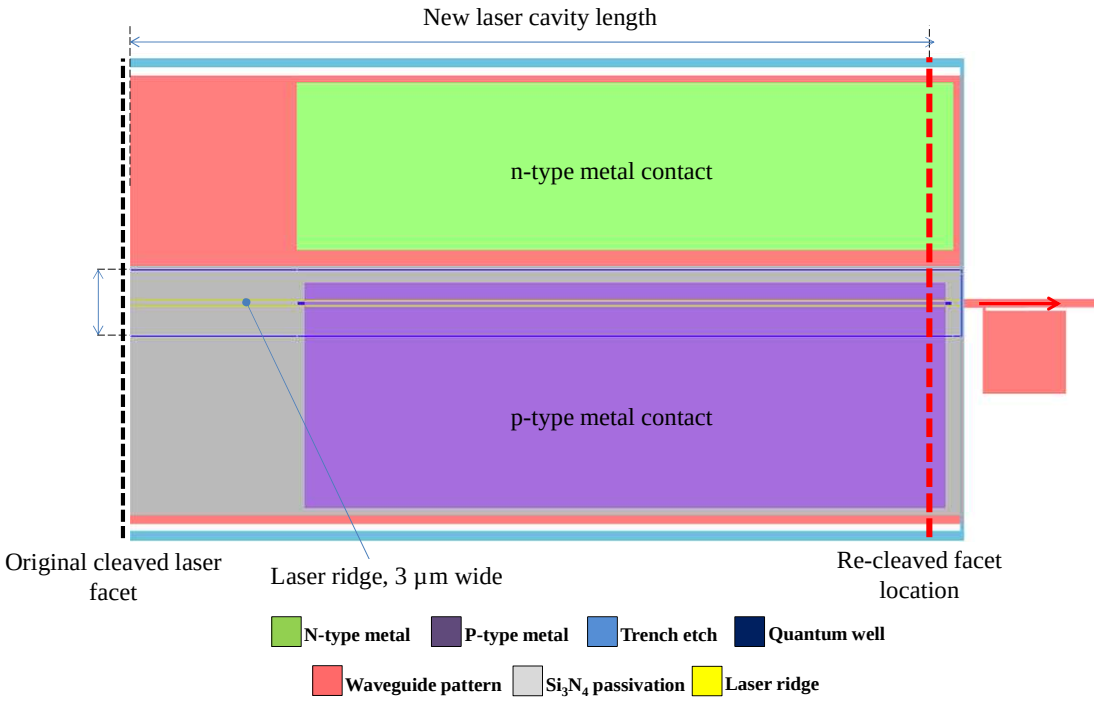


Figure 5.31. Top down diagram illustrating the location of the re-cleaved laser facet (not to scale).

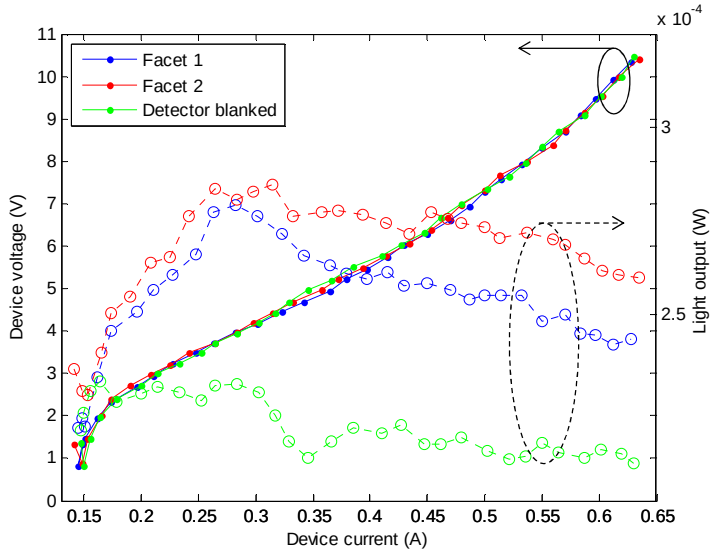


Figure 5.32. LIV curves for a device that has two cleaved facets. Output power shown from both sides of the laser, as well as a plot of the detector input blanked.

5.1.9 Cryogenic testing setup

It is well understood that InGaAsP-based laser gain is very sensitive to temperature variation [187, 223, 227], and it was thought that by mounting these samples within a cryostat and cooling the devices down to 11K, this gain could be recovered and the devices would be able to lase.

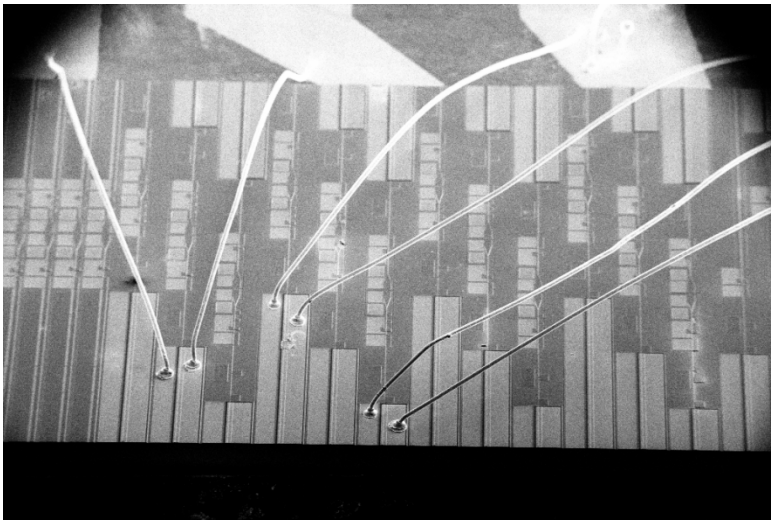


Figure 5.33. SEM showing three devices connected via wire bonding, notice one of each laser length is connected for cryo-testing.

The laser characterization was performed at cryogenic temperatures with an APD Cryogenics Expander 202 6.5 K helium cryostat. In order to interface samples inside of the vacuum chamber, the fabricated devices were mounted to a diamond sub-mount where wire-bonding was performed to the topside contacts for the laser diodes in order to achieve electrical contact (see Figure 5.34 and Figure 5.33).. Diamond is chosen as the submount substrate for cryogenic testing for its high thermal conductivity, and low electrical conductivity. The submount can then be connected to wire feedthroughs and used without micropositioner probes. A sapphire window with a 90% transmission at 1.55 µm is placed at the end of the vacuum

chamber, allowing the generated light from the cleaved laser diode to escape the cryostat assembly and be collected by the same integrating sphere.

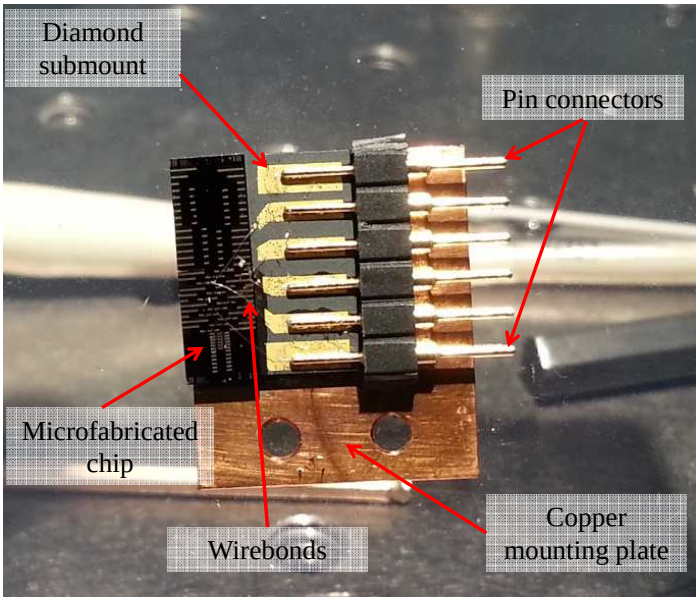


Figure 5.34. Sample mount for cryogenic and vacuum testing.

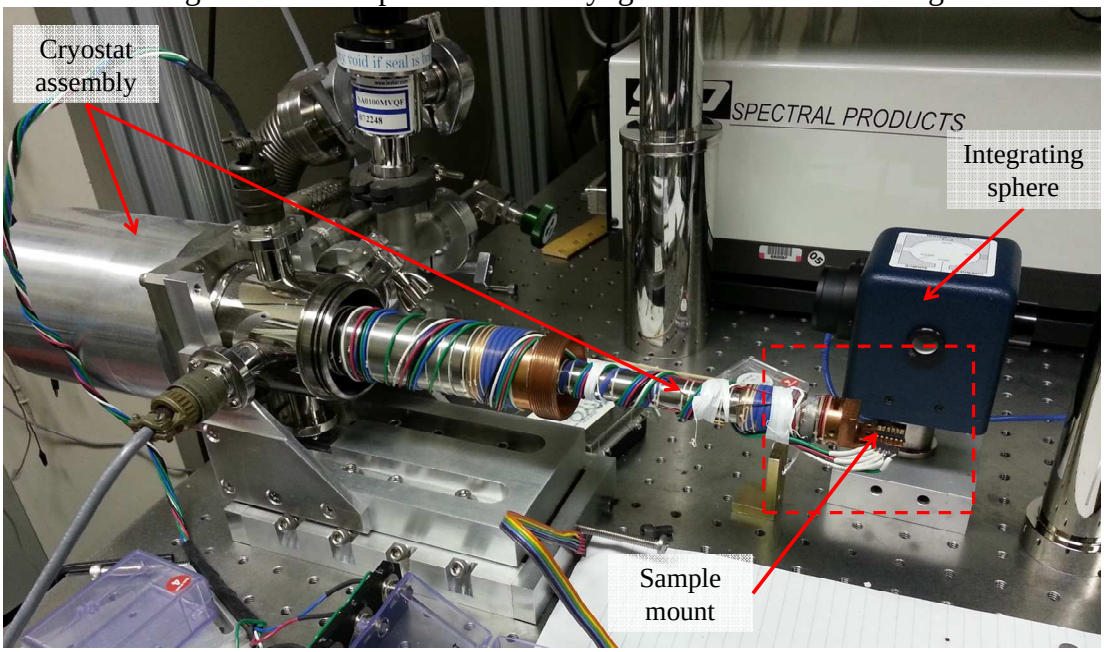


Figure 5.35. Full cryogenic testing setup, dotted line references close up of the coldhead in Figure 5.36.

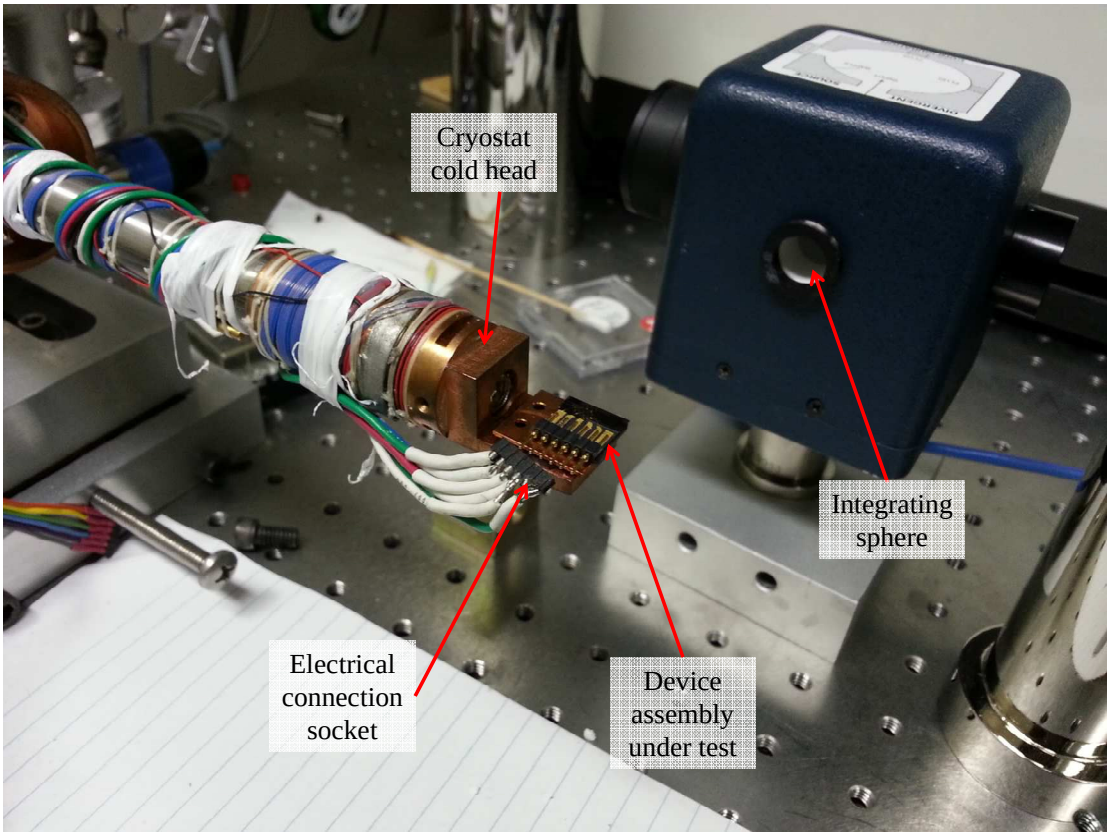


Figure 5.36. Close-up image of the coldhead assembly with sample attached.

A total of 6 feedthroughs were available on the cryostat, allowing 3 devices to be tested in one cool-down cycle. Samples were placed in the chamber at 8 mT vacuum, and the cryostat was run to its base temperature of approximately 11 K. Bringing the sample temperature this low causes negative self-heating effects to be drastically reduced. The same LIV measurements are performed using the pulsed-excitation measurement scheme.

5.1.10 Cryogenic testing results and further analysis

Devices were tested at room temperature with no active cooling beyond the thermal heatsink, and also at 11K, with no lasing behavior observed at either temperature condition. The turn-on voltage of the diode curves increases as is

expected for cryogenic testing of *p-n* junctions. Data from these measurements for all three laser diode cavity lengths is presented below in Figure 5.37.

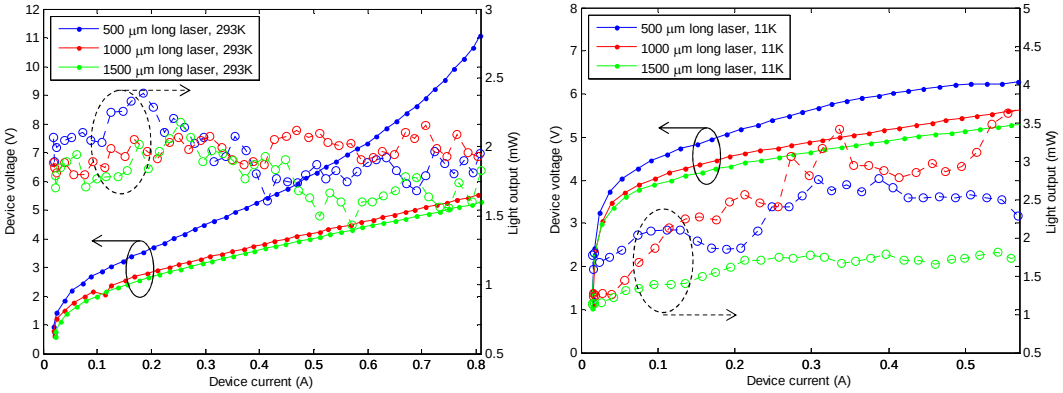


Figure 5.37. LIV plots of three laser cavities at room temperature (Left) and cryogenically cooled to 11K (Right).

After performing each of these permutations in the testing conditions of the laser diodes from the second fabrication run, output light due to lasing action was not observed. From SEM inspection and simple I-V curve measurements it would be expected for these devices to work as designed.

All of these experiments establish that the internal gain of the laser medium is not able to overcome the losses within the laser cavity or at the laser cavity mirrors. Beyond internal losses due to dislocations and material defects and mirror facet reflectivity loss, loss can be experienced through surface leakage of the optical mode. This is brought on by surface roughness and metal covering the laser ridge in close proximity to the guided laser mode. This particular fabrication run differed slightly compared to the previous working fabrication run, particularly in the height of the laser ridge. Fabrication run 1 yielded a laser ridge height of 1.5 μm tall with a nitride coating of 400 nm while fabrication run 2 produced a laser ridge height of 1.2 μm tall with a nitride coating of 175 nm. These changes may have put the metal contacts

closer to the optical mode due to the thinner passivation coating for the fabrication run 2 devices.

In order to test this hypothesis, simulations were performed using the same finite difference modesolver used previously to calculate the loss in the primary guided mode due to the underlying sacrificial region. In this case, the introduction of the Si_3N_4 coating and gold metallization were included in the simulation. These mode simulations were used to calculate the loss in the primary TE mode via the effective index of the guided mode as per equation (3-35). The two fabrication run geometries were simulated and compared. Figure 5.38 shows the two cases and the primary guided mode.

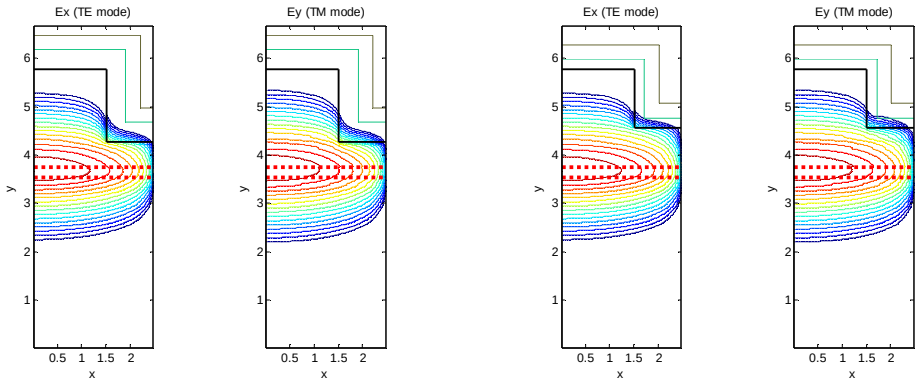


Figure 5.38. Output of modesolver simulations for (left) Fabrication run 1 and (right) Fabrication run 2. Dotted lines indicate the location of the quantum well gain region, green lines indicate the Si_3N_4 coating, and the brown lines on top indicate the gold contact material.

The simulated loss *only* due to absorption from the lossy layers (sacrificial region and gold metal contact which blankets the ridge) was found to be: 0.00555 dB/cm for fabrication run 1 and 0.00522 dB/cm for fabrication run 2. The simulations indicate that there is little difference between the two fabrication runs; in fact the fabrication run 2 should perform marginally better. The reason for this relative insensitivity is largely due to an error in the growth thickness of the upper SCH layer

(layer #29 in Table 3.1) which makes it double the thickness of the bottom SCH layer. This discrepancy does not affect the propagation of an optical mode; however it does push the active gain region of the quantum wells even further away from the surface, reducing any interaction of the mode with the surface, increasing the confinement.

The shallower ridge in fabrication run 2 may have additional consequences in the overall laser device effectiveness due to the lack of current confinement which can arise due to lateral current spreading. Figure 5.39 shows a diagram which illustrates this effect. Since the ridge etch was shallower in run 2 than run 1, there is a region of doped material above the quantum wells, called "underetch," which allows current to spread out more readily as soon as it leaves the physical confinement of the ridge. This effectively increases the volume which the current passes through, reducing the overlap of the current flow with the optical mode, and decreasing the effective current density, yielding higher required threshold currents to achieve lasing. This phenomena also has an effect on the mode discrimination in the gain region and the single or multimode operation of the laser.

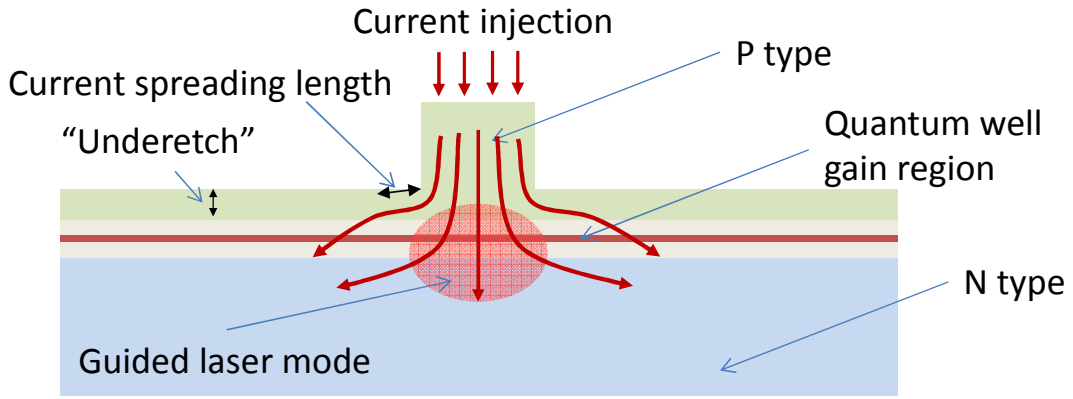


Figure 5.39. Diagram illustrating the effect of ridge underetch on the current through the guided laser mode in the gain region.

Achtenhagen *et al.* have developed a model to simulate the lateral current spreading in the "y" direction (away from the ridge) [231, 232]. This lateral current can be described as:

$$J(y) = \begin{cases} J_s\left(1 + \dfrac{|y| - w/2}{l_s}\right) & for\ |y| > w/2 \\ J_s & for\ |y| < w/2 \end{cases} \tag{5-18}$$

where J_s is defined as:

$$J_s = J_T\left(1 + \frac{2l_s}{w}\right)^{-1} \tag{5-19}$$

and J_T represents the total injected current density. From these equations, we can solve for l_s, the spreading length:

$$l_s = \sqrt{\frac{4k_B T d}{q\rho J_s}} \tag{5-20}$$

where k_B is Boltzmann's constant, T is the temperature, d is the underetch thickness, q is the elementary charge, w is the width of the laser ridge, and ρ is the resistivity of the material in which the current spreads. We take these equations and solve for our system with a ridge width of 3 µm at room temperature and the cryogenic temperatures attempted (11K), and pick bounds for the maximum and minimum current densities encountered for threshold. The resulting simulations show an approximate maximum and minimum range of expected current spreading length as a function of the overetch thickness. These plots are shown in Figure 5.40.

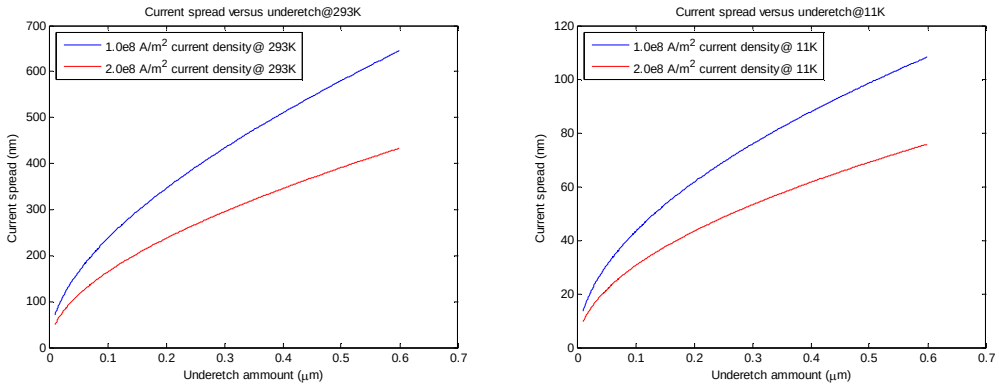


Figure 5.40. Plots of simulated current spreading versus underetch amount at multiple temperatures.

From these simulations, it is found that the current spreading length is about 300-500 nm for fabrication run 2 devices (with a 0.400 um underetch value experimentally determined). This spreading length is even less when the devices are cryogenically cooled to 11K with a current spreading length of 60-80 nm. These spreading lengths are very small in comparison with the ridge width, indicating that this effect is probably not a contributor to the final device effectiveness.

While not directly tested for these two fabrication runs, the processing steps used in order to fabricate the devices may have contributed to the overall poor performance of the laser devices. Of particular importance are the processes which introduce thermal cycling such as ICP etching, electron beam metal evaporation, and contact annealing. Each of these steps could cause aggregation of defects within the quantum well regions, or intermixing of the quantum wells themselves, increasing the loss within this active region. ICP and RIE etching are also aggressive processes known to introduce damage and surface modification to epitaxial structures after plasma exposure [233], and may have caused additional surface current paths, intermixing effects, or propagated defects within the active region. The wafer thinning process used in order to better cleave the devices into chips is a physically

aggressive grinding process which may also cause there to be propagated crystalline defects through the substrate into the epitaxially grown layers.

Ultimately the root cause for lack of stimulated emission in the second fabrication run was not definitively determined. It is possible that while one of these factors discussed here in this section may not single-handedly cause the failure of the laser devices, any combination or permutation of the possible flaws may increase the likelihood for failure. It was deemed beyond the scope of the objectives of the research presented here to further explore the failure mechanisms for these devices.

Conclusions and future work

Through two full fabrication runs that yielded multiple die and chips for testing and characterization, the testing of the full system with all three components together was not possible within the time and resource constraints of this program. Significant effort was undertaken to understand the devices separately as their discrete components, as well as the interdependence of each. It is this interdependence which provides the largest challenge when attempting to integrate these components into a monolithic system. This is evident in the previous work published by the author, and others in our group [26, 32, 169, 181], which demonstrated the stand-alone MEMS cantilever and photodiode components operating successfully in the absence of an integrated laser source. The results presented in this dissertation are invaluable in the investigation of the interdependence between optical and MEMS components. Approaching this system

from the design, fabrication, and testing perspectives simultaneously was a primary goal of this work and has shed much light on the practical limitations of this system.

Contact isolation was investigated, photodiodes were characterized as discrete components, and the measurement and characterization of the laser diodes was undertaken. It was found that laser diodes performed poorly due to what may be a myriad of effects from Auger recombination, surface current leakage paths, low mirror facet reflectivity, or temperature instability. Without sufficient contact isolation cantilever actuation was not possible, and system-wide testing was impossible due to crosstalk between the laser diode, photodiode, and cantilever waveguide actuation which obscured the photodiode readout. This contact isolation proved to be the largest impediment to the system operation and is likely caused due to a combination of effects: incomplete sacrificial layer removal, insufficient isolation trench etching depth, and unpassivated trench surfaces.

A second fabrication run with an inexplicable 0% device yield indicates that the complexity and interdependence of the epitaxial layer structure, the mask layout, and the fabrication process flow is not fully understood. Many more iterations in the design of the epitaxial layer structure, components, layout, and processing steps are needed in order to successfully realize a fully integrated optical MEMS system in these III-V materials.

A number of changes in the design of this system from a device layout and process flow perspective need to be made when considering future work related to these devices. A more effective and reliable method for contact isolation between photodiodes, actuation pads, and the laser diodes is required if all of the components

of the system are to be operated simultaneously. Much of this isolation scheme depends on the ordering of process steps that allow for physical deep isolation trench etching. The design presented in this work attempted to streamline the fabrication process by combining the creation of the trench isolation etches with the laser mirror facets, marginalizing the importance of the etch depth in favor of etch smoothness. This caused for much of the electrical isolation trenches to miss their depth requirements and negating their function. To better address the design of the system as a whole, these fabrication steps should be de-coupled into two separate etches which can be optimized for depth and smoothness independently.

Simplifying the conceptual design of the active regions of this MEMS interrogation scheme would also be beneficial as opposed to the two completely separate laser and photodiode active regions as in the design presented here. A side effect of this design choice is an unnecessarily thick epitaxial growth and extra fabrication steps. The very thick growth required complicates the MBE growth and makes the realization of high-quality material more difficult to achieve. It also impacts the fabrication scheme by increasing the required depths and numbers of the etches (much more of an issue in III-V MEMS devices as opposed to silicon-based MEMS devices which have very mature high-aspect ratio etching schemes available). Deeper etches are much less ideal than a more shallow version of the same, and suffer more from aspect ratio dependent etching. Deeper etching causes the die surface to be highly non-planar, while the demands of other in-plane fabrication tolerances remain the same. Non-planar surfaces are notoriously harder to pattern with high resolution and fidelity. The separation of both active regions (photodiode and laser)

in the layer structure also introduces more patterning steps which introduce more sources of alignment error, fabrication imperfections, or additional effects which will damage the device surfaces. Collectively this integration scheme makes wet etching, photolithography, dielectric material deposition, and metallization much more challenging, reducing device yield.

Furthermore a more traditional design similar to that performed with CMOS MEMS integration can be employed where photonic and MEMS based components are isolated from each other via encapsulation using a polymer such as BCB or dielectric coatings like Si_3N_4 or SiO_2. This approach can serve to increase the yield of devices and lessen the interdependence of non-standard MEMS processing techniques which can damage or destroy the photonic devices. Clever arrangement of these encapsulated sections can also make the interfacing of the MEMS resonant sensor with the external environment easier.

If a re-design of the integration scheme is to be pursued, a more efficient approach would be having only one active region in the layer structure through utilizing the active region of the laser diode operated in reverse bias mode as the absorbing region of the photodiodes. This would reduce the overall thickness of the epitaxial growth, improve the optical and presumably thermal performance of the laser diode region by removing unnecessary absorbing regions, and would ultimately require fewer masks to layout the discrete components of the integrated system. The photodiode design in this scheme would not be dictated by the sacrificial region as well, which allows for a separate optimization of the sacrificial and absorbing region. In this way, an ideal sacrificial layer can be grown which would provide more reliable

device release for MEMS device fabrication, without any need to optimize its optical qualities.

The specific design of the laser devices need to be reconsidered and re-prioritized as the most complicated and sensitive portion of the entire integrated system. The impact of fabrication processes being used to fabricate the other components of this MEMS system on the laser diode operation need to be better understood and accounted for in the device protection and design, as was evident in the damage to laser facets due to the undercutting etch and the low reflectivity exhibited by the passivation coating on laser facets. Mirror facet reflectivity was taken for granted in this current design, and the laser cavities would benefit greatly by the implementation of high-reflectivity facet coatings on the etched laser facets in order to both protect these facets and reduce the cavity losses. Additionally it may be beneficial to use the very smooth ICP etching techniques developed in this work to establish both mirror facets in order to precisely control the laser cavity length and the quality of both facets independent of the highly variable mechanical cleaving process which greatly reduced the overall device yield. It is believed that the importance of the thermal sinking requirements of the laser diode cavity was greatly underestimated, and a targeted design to better conduct away excess thermal energy from the laser diode gain region would significantly improve the performance of the laser devices.

Furthermore a more radical approach may need to be taken for future integrated elements using this particular integration scheme, which may involve the usage of static MEMS optical elements such as evanescent waveguide sensors and ring resonators. These un-released structures can provide sensing capabilities without

the more demanding and destructive undercut and release MEMS fabrication steps which damage and reduce the effectiveness of the optical elements. This change would have the effect of making the whole system more robust. The increase robustness can be taken advantage of in order to better optimize the optical components before attempting another moveable MEMS device design.

This work presents the first attempt to develop a fully integrated MEMS sensor platform in the InP III-V material system. Many practical design requirements of such a MEMS system were uncovered in the areas of fundamental device design, electrical performance, optical performance, and fabrication process flow optimization. It is this first-hand discovery which is critical to the understanding of these type of new monolithically integrated III-V MEMS systems and often cannot be modeled or predicted aside from exploratory experimentation. The research performed here has performed this function and served to establish a baseline for future MEMS designs in InP materials, as well as other III-V material systems not explicitly explored here such as GaAs, AlGaAs, GaN, and even hybrid silicon-III-V approaches.

6 Conclusions

Summary of dissertation accomplishments

1. A vertically offset monolithic integration scheme was designed for the integration of a multiple quantum well laser source, an optical MEMS cantilever resonator sensor, and a waveguide integrated PIN photodiode within a single epitaxial growth. Optimization of the optical performance of each component was performed via numerical simulations of the optical characteristics in order to design a 36 layer, 7.1 µm thick epitaxial layer structure that contains all of the necessary functionality to implement a novel all-optical resonator readout scheme. The primary driver in this design was an attempt to maintain the simplicity and ease of integration of each component.
2. Fabrication processes were developed and characterized in order to realize the first physical implementation of a fully integrated optical MEMS microsystem. The fabrication process flow utilized 7-projection lithography masks, 4 nested ICP etches, and over 60 discrete process steps. Focus was placed on the optimization of the following:
    a. Photolithography processing techniques to repeatedly achieve high resolution (< 1 µm) and pattern alignment fidelity.
    b. Inductively coupled plasma (ICP) etching to achieve high aspect ratio (7:1) and damage free vertical sidewalls for the definition of laser facets, waveguides and deep electrical isolation trenches.

c. Reactive ion etching (RIE) recipes for SiO_2 and Si_3N_4 in order to realize highly vertical patterns in order to create highly vertical ICP etching masks and laser passivation regions.

d. The deposition of very thick (>1.5 µm), highly conformal SiO_2 and Si_3N_4 dielectrics via plasma enhanced chemical vapor deposition (PECVD) for ICP etching masks and device passivation coatings.

e. *P* and *N* –type metallization material stacks and annealing steps characterized with the circular transverse length method (CTLM) in order to achieve low resistance ohmic contacts for electrical contacts to active optical components.

f. The undercutting of a sacrificial layer and the subsequent CO_2 critical point drying procedure to create moveable MEMS structures and suspended waveguides.

g. Full-fabrication process flow optimization and compatibility was considered in order to assure the compatibility and discover the interdependence of all fabrication steps.

3. Each component of the fabricated microsystem was tested separately and characterized.

   a. Photodiodes were characterized in the negative bias region of operation, showing expected operation with respect to the illumination scheme employed.

   b. Laser diodes were tested via a pulsed LIV excitation technique at room temperature, thermoelectrically cooled, and in a cryogenically cooled

system. Devices performed with varied levels of success, showing optical performance limited by both intrinsic material losses and fabrication imperfections.

c. A number of failure mechanisms for non-functional cantilever actuators and laser diodes were explored in detail.

Conclusions and final comments

This dissertation aimed to explore the monolithic integration of optical sources and photodetectors with passive MEMS devices. Specifically the work presented the conceptualization, design, and fabrication of such a system with Indium Phosphide (InP), and other lattice matched III-V semiconductor materials. A novel design for an all-optical readout MEMS resonator utilizing suspended dielectric waveguides was developed along with the active optical components needed to interrogate and measure the sensor. A focus on the development of unit fabrication processes and the integration of each procedure into a complete fabrication process flow allowed for the first realization of such an integrated MEMS system. The fabricated devices were tested and characterized and the design and performance of the integrated system was evaluated.

In the spirit of early work by Kelly *et al.* [28], Pruessner *et al.* [25, 26, 30, 165, 181, 183, 234], and Siwak *et al.* [32] focusing on the early development of InP-based MEMS technology, this dissertation provided the logical conclusion to these works by accomplishing the monolithic integration of a MEMS sensor system in these materials. I have shown that a number of unforeseen challenges arise when

integrating these well-established stand-alone MEMS structures with a complete optical system. A fabrication "toolbox" and design methodology has been developed for a brand new class of III-V MEMS devices, incorporating standard semiconductor processing, specialized III-V design schemes, and MEMS fabrication techniques into a single unified design process.

This work presents the first attempt to develop a fully integrated MEMS sensor platform in the InP III-V material system. Many practical design requirements of such a MEMS system were uncovered both in fundamental device design, electrical performance, optical performance, and fabrication process flow optimization. The research performed here has served to establish the baseline for future MEMS designs in InP materials, as well as other III-V material systems not explicitly explored here such as GaAs and InAs. Through the successes and failures of the resulting system, material and device specific design criteria have been established that will allow for new and exciting designs of III-V MEMS to be realized in the future.

Appendix A: Processing Recipes

A.1 Photoresist recipes used

- **Fujifilm OiR 906-10 (I line resist, recipe for 1.05um thick film)**
  - Dehydrate (60s @ 120C+)
  - Spin HMDS if using silicon-based substrate (60s @ 3000 RPM w 500 RPM/s ramp)
  - Pipette resist onto sample surface, cover with spinner lid
  - Spin resist (60s @ 3200 RPM w 500 RPM/s ramp)
  - Softbake (60s @ 90C)
  - Expose (stepper = 0.7s / LPS Karl SUSS contact aligner 12s)
  - Hardbake (60s @ 120C)
  - Cool sample on metal surface (table/plate 60s)
  - Develop (60s with OPD 4262)
  - Dry sample / inspect

- **Fujifilm OiR 908-35 (I line resist, recipe for 3.3um thick film)**
  - Dehydrate (60s @ 120C+)
  - Spin HMDS if using silicon-based substrate (60s @ 4000 RPM w 500 RPM/s ramp)
  - Pipette resist onto sample surface, cover with spinner lid
  - Spin resist (60s @ 4000 RPM w 500 RPM/s ramp)
  - Softbake (60s @ 120C)
  - Expose (stepper = 1.0s / LPS Karl SUSS contact aligner 15s)
  - Leave resist in ambient for 15-30 min
  - Hardbake (60s @ 120C)
  - Cool sample on metal surface (table/plate 60s)
  - Develop (60s with OPD 4262)
  - Dry sample / inspect

- **AZ-nLOF 2020 Negative photoresist (recipe for 1.6um thick film, if for liftoff use REMOVERPG @80C to dissolve)**
    - Dehydrate (60s @ 120C+)
    - Pipette resist onto sample surface, cover with spinner lid
    - Spin resist (60s @ 3000 RPM w 500 RPM/s ramp)
    - Softbake (60s @ 110C)
    - Expose (stepper = 0.5s)
    - Hardbake (60s @ 110C)
    - Cool sample on metal surface (table/plate 60s)
    - Develop (30s with AZ 3000 MIF)
    - Dry sample / inspect

- **AZ-nLOF 2035 Negative photoresist (recipe for 3.6 µm thick film, if for liftoff use REMOVERPG @80C to dissolve)**
    - Dehydrate (60s @ 120C+)
    - Pipette resist onto sample surface, cover with spinner lid
    - Spin resist (60s @ 3000 RPM w 500 RPM/s ramp)
    - Softbake (60s @ 110C)
    - Expose (stepper =1.15 s)
    - Hardbake (60s @ 110C)
    - Cool sample on metal surface (table/plate 60s)
    - Develop (120s with AZ 3000 MIF)
    - Dry sample / inspect

A.2 RIE recipes used

- **SiO_2 etch (SIO2PT) provides high anisotropy in etch – typical rate = 330 Angstroms/min**
    - CHF_3 20sccm
    - O_2 20sccm
    - RF power 175W
    - Pressure 40mT

- **Si_3N_4 etch (DIELCUT) etches nitride dielectrics – typical rate = 1360 Angstroms/min**
    - SF_6 19.86sccm
    - DC bias set point 170V
    - Pressure 20mT

- **O_2 plasma descum (DESCUMRG) etch removes organic materials**
    - O_2 16sccm
    - RF power 175W
    - Pressure 175mT

- **Argon sputter (ARsample) physical etch cleans surfaces**
    - Ar 40sccm
    - RF power 300W
    - Pressure 100mT

A.3 PECVD recipes used (NOVELLUS PECVD Concept One deposition tool)

- **SiO_2 deposition recipe (1npsoxide) typical rate = 73 Angstroms/sec**
  - Temperature 300°C
  - SiH_4 0.3sccm
  - N_2 1.5sccm
  - N_2O 9.5sccm
  - HF RF power 1100W
  - LF RF power 0W
  - Pressure 2.4T

- **Si_3N_4 deposition recipe (1npsnitride300c) typical rate = 24 Angstroms/sec**
  - Temperature 300°C
  - SiH_4 0.5sccm
  - N_2 1.6sccm
  - NH_3 4sccm
  - HF RF power 570W
  - LF RF power 430W
  - Pressure 2.6T

A.4 ICP etch recipes used (PlasmaTherm 770 ICP)

- **"Fast Etch" – typical rate = 460 Angstroms/sec**
  - Temperature 175°C
  - Cl_2 4sccm
  - Ar 6sccm
  - O_2 0.5sccm
  - ICP power 900W
  - RF power 210W
  - Pressure 2mT
  - Typical DC bias 250-255V

- **"Slow Etch" – typical rate = 100 Angstroms/sec**
  - Temperature 225°C
  - Cl_2 2sccm
  - Ar 3sccm
  - H_2 2sccm
  - ICP power 900W
  - RF power 110W
  - Pressure 1.5mT
  - Typical DC bias 165-175V

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