

## ABSTRACT

Title of Dissertation: NANO-ENGINEERING AND SIMULATING  
ELECTROSTATIC CAPACITORS FOR ELECTRICAL  
ENERGY STORAGE

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Electrical energy storage solutions with significantly higher gravimetric and volumetric energy densities and rapid response rates are needed to balance the highly dynamic, time-variant supply and demand for power. Nanoengineering can provide useful structures for electrical energy storage because it offers the potential to increase efficiency, reduce size/weight, and improve performance. While several nanostructured devices have shown improvements in energy and/or power densities, this dissertation focuses on the nanoengineering of electrostatic capacitors (ESC) and application of these high-power electrostatic capacitors in electrical energy storage systems.

A porous nano-template with significant area enhancement per planar unit area coated with ultra-thin metal-insulator-metal (MIM) layers has shown significant improvements in areal capacitance. However, sharp asperities inherent to the initial nano-template localized electric fields and caused premature (low field) breakdown, limiting the possible energy density ( $E = \frac{1}{2} CV^2/m$ ). A nanoengineering strategy was

identified for rounding the template asperities, and this showed a significant increase in the electrical breakdown strength of the device, providing rapid charging and discharging and an energy density of 1.5 W-h/kg – which compares favorably with the best state-of-the-art devices that provide 0.7 W-h/kg.

The combination of the high-power ESC with a complementary high-energy-density electrochemical capacitor (ECC) was modeled to evaluate methods resulting in the combined power-energy storage capabilities. While significant improvements in the ESC's energy density were reported, the nanodevices display nonlinear leakage resistance, which directly relates to charge retention. The ECC has distinctly different nonlinearities, but can retain a greater density of charge for significantly longer, albeit with slower inherent charging and discharging rates than the ESC. The experimentally derived dynamic model simulating the nonlinear performance of the ESC and ECC devices indicated this hybrid-circuit reduces the time required to charge the ECC to near-maximum capacity by a factor of up to  $\sim 12$ .

NANO-ENGINEERING AND SIMULATING ELECTROSTATIC CAPACITORS FOR  
ELECTRICAL ENERGY STORAGE

by

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## Dedication

To my father and mother  
*Dr. J. Kent and Karen Haspert*

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# Chapter 1: Introduction

## 1.1 Background and Motivation

Electrical energy storage solutions incorporated within power grids offer the ability to balance electricity generation from conventional sources (*i.e.*, coal, gas, oil) and renewable energy sources (*i.e.*, wind and solar) with electricity consumption and distribution for meeting instantaneous load demands.<sup>1,2</sup> Strong fluctuations in renewable energy generation have a vastly dynamic, time-variant profile.<sup>1</sup> Integrating energy storage systems into power grids can capture energy fluctuations to smooth the renewable energy generation profile and/or release the energy to supply additional power as needed.<sup>1,3</sup> Therefore, effective and efficient electrical energy storage solutions must be able to capture, store, and release energy quickly and in large quantities.

Energy storage devices and systems for managing energy supply and demands on the power grid should have the ability to respond quickly to abrupt fluctuations (high power density) and supply large amount of energy under abrupt or extended dips in source generation (high energy density). Conventional energy storage devices each rely on fundamentally different charging mechanisms (batteries, electrochemical capacitors and electrostatic capacitors shown in Figure 1.1). Batteries store electrical energy through faradaic chemical reactions occurring at electrode surfaces, providing very large charge capacities (high energy) but the response time is limited by the redox reaction rates (low power). Batteries are commonly used for storing energy as they have very large capacities but in applications where spurts of high power (fast discharging of the

battery) are needed, large currents are drawn increasing the temperature, degrading the capacity and reducing lifetime. For higher power applications, electrochemical capacitors can be used. In electrochemical capacitors (moderate energy, power) ionic charges build on the solid-electrolyte interface forming an electrical double layer capacitance, which responds faster than batteries.<sup>4</sup> However, electrochemical capacitors also experience some capacity degradation over their lifetime and their cost versus energy capacity make them a less competitive option to batteries.<sup>5</sup> Electrostatic capacitors are ideal for high power applications and find various uses in modern electronics<sup>4</sup> – ranging from trench capacitors in dynamic access memories for storing binary information,<sup>6,7</sup> integrated circuits for filtering out noise, micro-electro-mechanical systems driving sensors or actuators,<sup>8</sup> to power applications for power smoothing or conditioning. Electrostatic capacitors do not experience capacity fade and can rapidly transfer the equal and opposite non-faradaic surface charge stored at metal-insulator interfaces (high power) but the amount of charge stored is limited by the geometric and materials properties (low energy) and are typically not used for storing large amounts of energy.

Continuing research focuses on the development of innovative solutions for energy storage solutions that are affordable, efficient, compact/portable, have large gravimetric and volumetric energy densities and are able to respond quickly for balancing energy supply and demand. This proves to be a challenge as Figure 1.1 shows power and energy densities in conventional devices are often a trade-off. Nanostructured devices offer the potential to greatly improve the performance of electrical energy storage devices.<sup>9</sup> The ability to control the dimensionality and morphology of heterogeneous nanostructures can result in faster charging rates by optimizing electronic and/or ionic



conduction pathways and diffusion lengths.<sup>10</sup> Additionally, nanostructures have high surface-to-volume ratios increasing the active surface area per unit volume for charge storage. Devices built on nanostructured foundations can be more efficient, reduce the overall system weight and size and with demonstrate improved performance (refer to Figure 1.1).<sup>11</sup> This dissertation focuses on nanostructuring electrostatic capacitors for increasing energy density for energy storage applications.

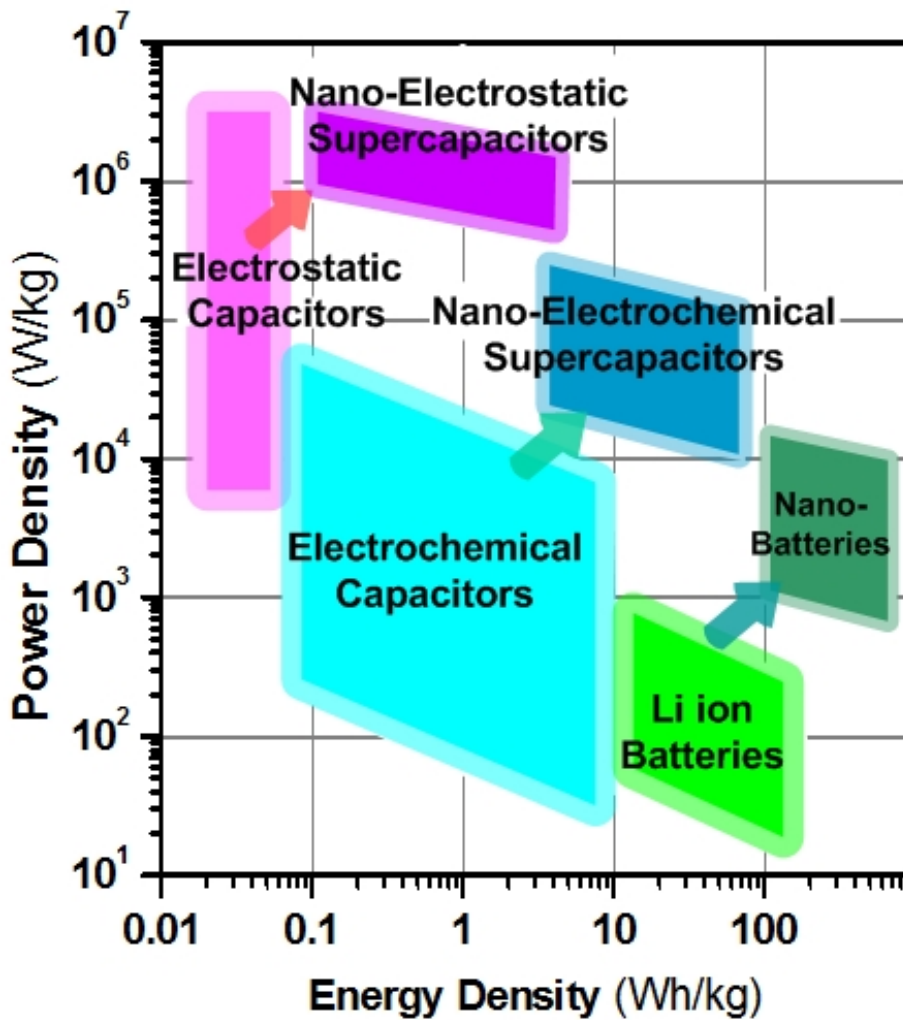


Figure 1.1 Ragone plot showing the power density and energy density of electrostatic capacitors, electrochemical capacitors and Li ion batteries. Nanostructures have shown improvements in the energy density and/or energy density.

## 1.2 Electrostatic capacitors for electrical energy storage

Material and geometric properties determine the capacitance of the electrostatic capacitor. In parallel plate electrostatic capacitors the capacitance,  $C$ , is given by  $C = \epsilon_0 \kappa A/d$ , where  $\epsilon_0$  is the permittivity of free space,  $\kappa$  is the dielectric constant of the insulator,  $A$  is the cross-sectional metal-insulator interface, and  $d$  is the thickness of the insulator. Methods of increasing the capacitance include reducing the thickness of the insulator, using a high- $\kappa$  insulating material, and increasing the surface area for charge storage. While these methods of increasing the capacitance are intended to increase the energy density, the methods should not limit or effect the maximum voltage that can be applied since energy,  $E$ , is given by  $E = \frac{1}{2} CV^2$ .

### 1.2.1 Methods of increasing charge storage capacity

An insulating material of some nominal thickness ( $\geq 5$  nm) should be used to maintain an adequate energetic barrier to charge tunneling, otherwise, reducing the barrier thickness increases the probability for direct electron tunneling (*i.e.*, leakage currents) reducing the ability to retain charge over time.<sup>6,12,13</sup> An insulating material with a higher dielectric constant,  $\kappa$ , can be used but these materials often have higher leakage currents as a result of reduced Schottky barrier height<sup>14</sup> and catastrophic failure (breakdown) occurs at lower fields.<sup>15-17</sup> An alternative method of increasing capacitance is to increase the cross-sectional area,  $A$ , but for planar capacitors this does not satisfy the electronics miniaturization trend.<sup>18</sup> Instead, the challenge in increasing device capacity (while maintaining some nominal insulator thickness and reducing footprints) can be met with 3D substrate geometries to increase the surface area for charge storage per planar unit area. Roozeboom *et al.*<sup>19</sup> reported capacitors for radio frequency microelectronics in

an etched Si template (trenches 1.5  $\mu\text{m}$  in diameter, spaced 3.5  $\mu\text{m}$  apart, 150  $\mu\text{m}$  deep using 30 nm oxide-nitride-oxide dielectric material) had 100 $\times$  increase in capacitance over planar devices. Templates with higher aspect ratios and closer pore spacing (higher array density) have shown further improvements in areal capacitance, however, this can be a challenge using conventional lithography and etching techniques. Other templating fabrication techniques have relied on self-assembly processes for, potentially offering time and cost advantages over conventional lithographic techniques.<sup>20,21</sup> For example, anodic aluminum oxide (AAO) templates are fabricated electrochemically and result in a self-aligned, highly periodic porous structure with few processing steps.<sup>21</sup> A top-view scanning electron microscopy (SEM) image of an AAO template and cross-section SEM image of the pore base are shown in Figure 1.2(a) and Figure 1.2(b), respectively. Pores are hexagonally self-organized from the pore opening to pore base.

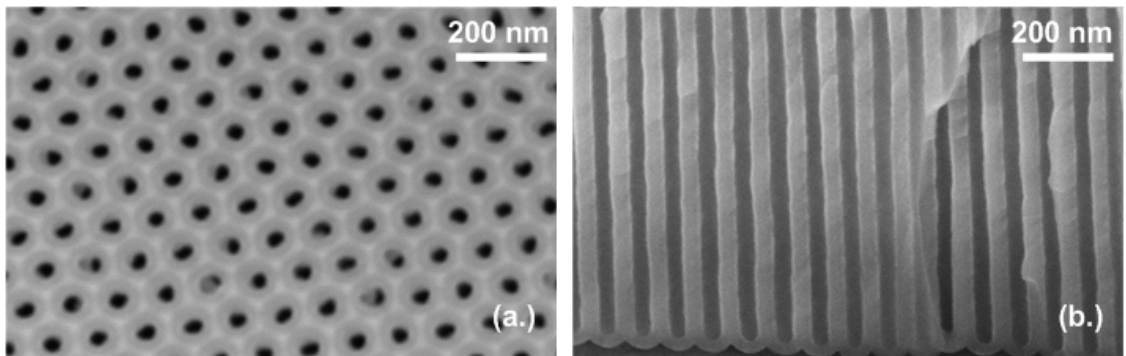


Figure 1.2 (a) Top-view SEM image of a porous anodic aluminum oxide template with hexagonally periodically spaced pores and (b) cross-section of the pore base showing highly aligned, vertical pore growth.

Shelimov *et al.*<sup>22</sup> reported electrostatic capacitors in an open-ended template with a  $\sim 250$  aspect ratio had an areal capacitance of  $\sim 2.5 \mu\text{F}/\text{cm}^2$  using carbon as the top and bottom electrodes and boron nitride as the insulator ( $d = 70 \text{ nm}$ ,  $\kappa \approx 2.5$ ).<sup>22</sup> Other reports

have documented increased capacity using the porous oxide template as part of the insulating material.<sup>23-26</sup> Lee *et al.*,<sup>27</sup> reported coating a  $\sim 400$  aspect ratio AAO template with  $\text{TiO}_2$  resulted in a capacity  $\sim 480 \mu\text{F}/\text{cm}^2$ . While all showed an increase in the areal capacity, none reported leakage current or breakdown field measurements or described these as performance shortcomings.<sup>22-27</sup>

Leakage currents and breakdown fields of metal-insulator-metal (MIM) electrostatic capacitors in an AAO template were reported by Banerjee *et al.*<sup>28,29</sup> Figure 1.3(a)-(b) shows MIM electrostatic capacitors at the bottom and top regions of the AAO template, respectively.<sup>28</sup> The areal capacitance was found to be dependent on template thickness ( $\sim 10 \mu\text{F}/\text{cm}^2$  in a  $1 \mu\text{m}$  thick template to  $\sim 100 \mu\text{F}/\text{cm}^2$  in a  $10 \mu\text{m}$  thick template), while the leakage current densities ( $5 \times 10^{-9} \text{ A}/\text{cm}^2$  at  $3 \text{ MV}/\text{cm}$ ) and breakdown fields ( $\sim 4 \text{ MV}/\text{cm}$ ) were independent of template thickness.<sup>28</sup> Even though the breakdown field was  $\sim 3 \times$  lower than the expected strength of the insulator an order of magnitude increase in the energy density ( $\sim 0.7 \text{ Wh}/\text{kg}$ ) over conventional electrostatic devices was reported.<sup>28</sup>

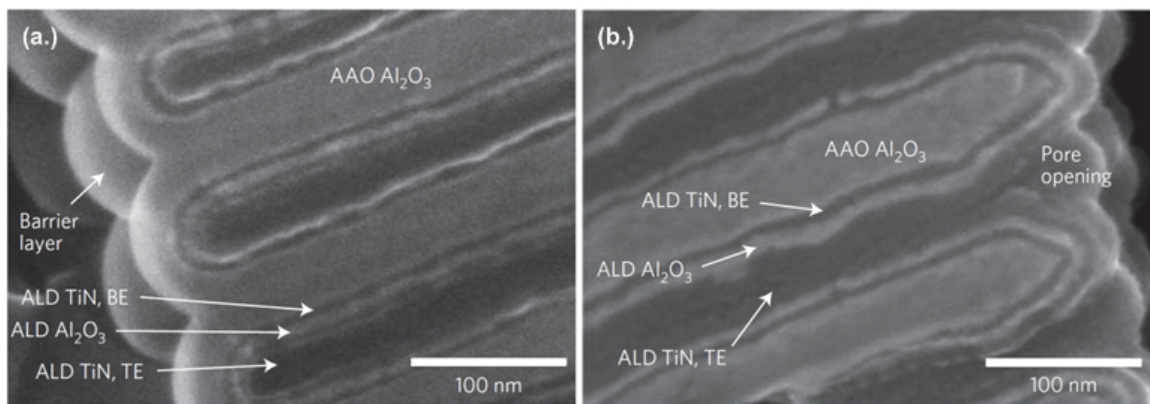


Figure 1.3 (a) SEM images of MIM capacitor fabricated in AAO template at the pore base and (b) at the pore opening show conformal deposition of the  $\text{TiN}-\text{Al}_2\text{O}_3-\text{TiN}$  metal-insulator-metal layers. [Reprinted from Banerjee *et al.*<sup>28</sup>].

### 1.2.2 Influence of nano-template on electrical performance

The premature breakdown reported by Banerjee *et al.*<sup>28,29</sup> was attributed to the interpore sharp asperities located at the pore opening (refer to Figure 1.3(b)). These asperities are locations with very small radii of curvature, which cause localization of an enhanced electric field and result in premature (low field) electrical breakdown. This significantly restricts the maximum voltage and field usable for energy storage. An effective technique able to smooth the regular interpore peaks is necessary to improve the overall performance. Breakdown fields near the strength of the insulator could further improve the energy density close to an additional order of magnitude.

In the work reported by Banerjee *et al.*,<sup>28,29</sup> a 15 nm passivation layer coated the porous template (reducing the initial available 80 nm pore diameter to 50 nm) prior to the MIM deposition to act as a passivation layer and to smooth the inherently sharp asperities. This smoothing effect was reported by Cleveland *et al.*,<sup>30</sup> where a surface consisting of sharp ridges (height  $\sim 42$  nm) resembling the interpore peaks shown in Figure 4.2(a) could be smoothed after coating the rough surface with an atomic layer deposition (ALD) film shown in Figure 1.4(b).<sup>30</sup> A dramatic reduction in the estimated surface area to the planar equivalent area was not found until after a film  $\sim 3\times$  thicker than the one deposited by Banerjee *et al.*<sup>29-31</sup> Introducing a thicker passivation layer to smooth the nanoroughness on the template would introduce design constraints and complexities on the subsequent MIM layers.

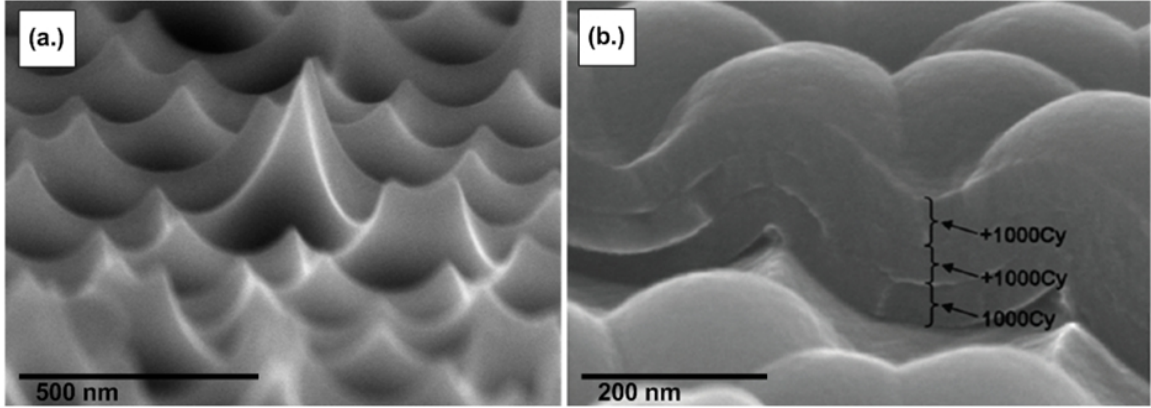


Figure 1.4 (a) Peak asperities on a rough surface resembling the interpore peaks on the AAO template and (b) introducing several layers of ALD on top of a non-planar surface smooths the surface. [Reprinted from Cleveland *et al.*<sup>30</sup>].

### 1.2.3 Ultra-thin metal-insulator-metal layers

The pore radius defines the maximum thickness of the MIM layer stack for fabricating the full device within each pore, where the total thickness of the three active layers should not exceed the radius of the pore. Thin metallic layers ( $\sim 10$  nm) can be deposited having the same low-resistivity of the bulk material but decreasing the thickness of the metallic layers ( $< 10$  nm) may reduce the conductivity of the film.<sup>32</sup> Introducing significant electrode series resistance limits the power,  $P$ , since  $P = V^2/R_e$ , where  $R_e$  is series resistance. Therefore, not only does the insulator layer need to be of some nominal thickness, the conducting layers must also be of some nominal thickness in order to maintain the high power capability inherent to the electrostatic capacitors. Furthermore, process capability is very important since few approaches have the thickness control and conformality needed to produce ultrathin uniform layers inside very high aspect ratio nanopores.

While the insulator will be of some nominal thickness, some reduction in its leakage resistance is expected with increasing the applied voltage. As charge

accumulates the energy bands shift, causing the insulating energetic barrier to become trapezoidal and increasing the probability for electron tunneling at these thinner barrier regions, referred to as Schottky tunneling. As template nanoengineering extends the voltage threshold of the device to higher potentials, the charge retention as affected by reduced leakage resistance should be analyzed. Using the electrostatic capacitor for charge capture and transferring charge to an alternative energy storage device for long-term charge storage may provide an electrical energy storage hybrid solution with fast response time and large charge storage.

#### *1.2.4 Basic processing sequence of fabricating nano-electrostatic capacitors*

The basic processing sequence of the MIM electrostatic capacitor devices is shown in Figure 1.5(a). Anodizing high-purity aluminum fabricates the porous template. The top conducting layer (*i.e.*, top electrode) is patterned by conventional photolithography methods to create 250  $\mu\text{m}$  diameter electrode pads, creating several hundred devices per sample and each device wires more than 5 million nanocapacitors together in parallel per microcapacitor device. Devices are characterized (Figure 1.5(b)) with current-voltage (IV) sweeps were measured with a HP 4145B for determining leakage currents and breakdown fields and capacitance-voltage (CV) measurements to determine the capacitance per planar unit area with an Agilent 4980A LCR meter at 20 Hz applying 100 mV (AC). Analytic SEM was performed with a Hitachi SU-70 to verify the structure the device.

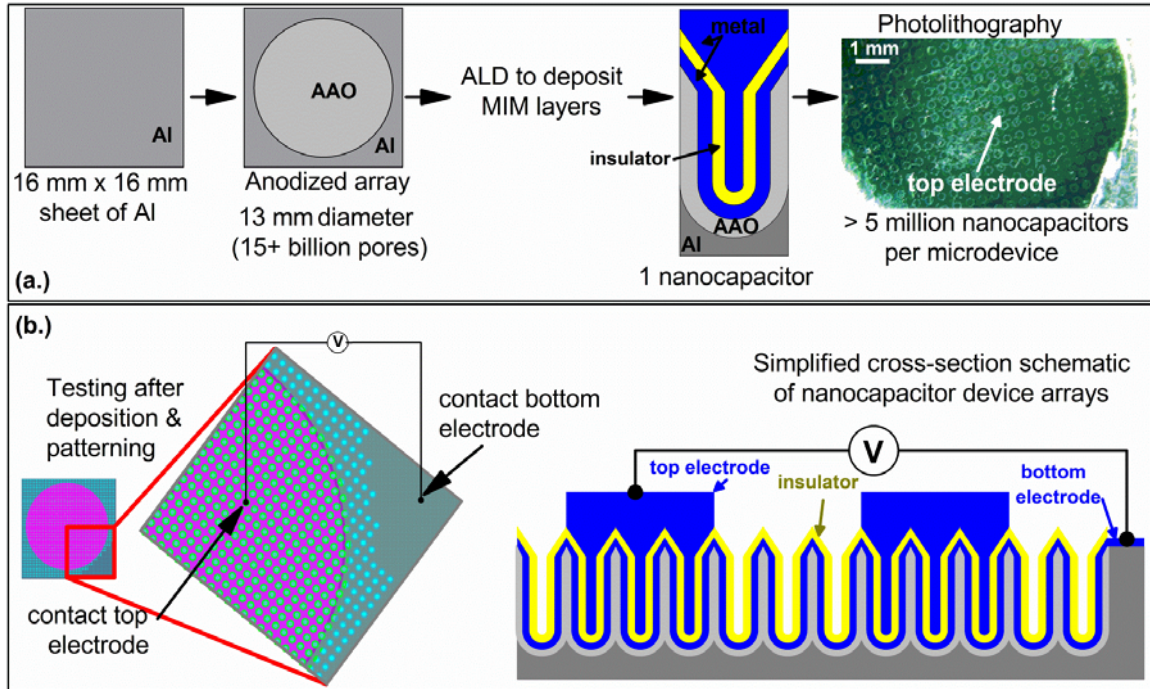


Figure 1.5 (a) Left to right: shows process flow of anodizing the sheet of the aluminum for creating a massive porous array. Within a 13 mm diameter window more than 5 billion pores are available for use as nanocapacitors. A photograph shows the AZO electrodes that have been patterned for electrical characterization and testing. (b). Schematic of the AAO template on Al with patterned AZO top electrodes (green) are individually contacted when probing the top electrode (left). A simplified schematic shows how contact is made to the bottom and top electrodes (right).

### 1.3 Overview of Dissertation

#### 1.3.1 Objectives

The following objectives focus on improving the energy density of electrostatic capacitors (ESC) and the role of this device in energy storage applications.

1. Identify effective nano-engineering strategies for modifying the nanotopography of the porous anodic aluminum oxide (AAO) template, increasing breakdown fields to the strength of the insulator,  $E = \frac{1}{2} CV^2$ .



2. Develop and simulate a dynamic, experimentally derived ESC model that depicts the nonlinearities of the ESC and determine its application in energy storage systems.
3. Expand the model to simulate an ESC-electrochemical capacitor hybrid circuit. Determine methods for efficiently capturing, transferring and storing charge and demonstrate high-energy high-power capability.

### *1.3.2 Outline*

Chapter 2 discusses the anodic aluminum oxide fabrication process, the various properties of the template and methods in which these properties may be modified, along with widely accepted theoretical formation and ordering mechanisms. The atomic layer deposition (ALD) process used to deposit the MIM layers is discussed in Chapter 3. The basic processing sequence and various examples of nanostructures fabricated using ALD in literature are presented. Combining these two key technologies to fabricate electrostatic capacitors, Chapter 4 will discuss optimization of the electrostatic device configuration and the template nanoengineering strategy significantly increasing the breakdown field, and thus improving the energy density to 1.5 Wh/kg. The practical applications of the nano-electrostatic device are presented in Chapter 5, focusing on the combination of an electrostatic capacitor with an electrochemical capacitor to create a nano-hybrid circuit able to achieve both high power and high energy. Chapter 6 will summarize the major research findings and provide discussion on future work and challenges.

## Chapter 2: Anodic Aluminum Oxide (AAO)

### 2.1 Introduction

Anodization of aluminum for protective coatings has been known since the early 1920s.<sup>33</sup> In the past decades, research has focused on creating a highly-regular, highly-ordered porous alumina oxide membrane because it can serve as a template for creating a very high density array of nanotubes, nanowires or nanorods for applications including photovoltaics,<sup>34,35</sup> catalysts,<sup>34,36</sup> sensors,<sup>34,37</sup> chemical and biological separation,<sup>37-39</sup> and electronic and magnetic devices.<sup>40,41</sup> The aspect ratio of the pores is determined by the anodization conditions and the length of the anodization. The top-view and cross-section schematics shown in Figure 2.1(a) and Figure 2.1(b), respectively, indicate the pore diameter,  $D_p$ , interpore spacing,  $D_{int}$ , and thickness also referred to as the pore depth,  $L$ . The self-aligning, self-assembly formation process results in uniform hexagonally spaced nanopores that can range from 50 – 500 nm.<sup>40</sup> Figure 2.1(c)-(e) shows transmission electron microscopy (TEM) images of various templates all having similar symmetry with  $D_p$  and  $D_{int}$  increasing from Figure 2.1(c) to Figure 2.1(e).<sup>42</sup>

The electrochemical process for fabricating anodic alumina oxide (AAO) templates requires few processing steps, whereas conventional template fabrication techniques require several complex and challenging lithographic processes and/or etching chemistries for fabricating high aspect ratio features.<sup>42-44</sup> Additionally, the array size of the AAO membrane can be scaled without the need to additional equipment or sensitive measurements for extended template uniformity.

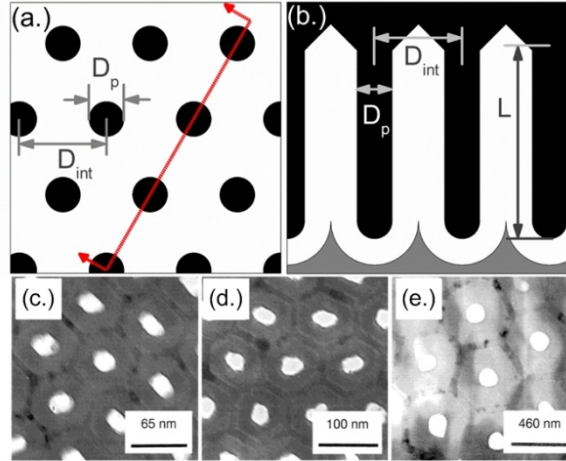


Figure 2.1 (a) Top-view schematic of ordered AAO and (b) cross-section schematic of AAO template, where  $D_{int}$  is the interpore spacing,  $D_p$  is the pore diameter and  $L$  is the pore depth. Top-view TEM images of AAO templates anodized under various anodization chemistries, resulting in different  $D_{int}$  and  $D_p$  of (c) 66.3 nm and 24 nm, (d) 105 nm and 31 nm, and (e) 501 nm and 158.4 nm, respectively. [c-e are reprinted from Nielsch *et al.*<sup>42</sup>]

## 2.2 Structure properties of AAO

Porous AAO can be formed under either galvanostatic (constant current) or potentiostatic (constant voltage) conditions. Potentiostatic conditions provide more control over template dimensions and are the focus of the discussion below.<sup>45</sup>

The discrete ordering regimes in which the highly-ordered template is formed depends largely on the electrolytic solution and the anodizing potential,  $V_{anod}$ .<sup>45</sup> Commonly used anodization chemistries are as follows: sulfuric acid with  $V_{anod}$  between 19-25 V,<sup>42,46,47</sup> oxalic acid with  $V_{anod}$  at 40 V,<sup>20,42</sup> and phosphoric acid with  $V_{anod}$  between 160-195 V.<sup>21,42,46</sup> Figure 2.2(a) shows a linear relationship between anodization potential and interpore spacing,  $D_{int}$ , can be estimated by  $V_{anod}[\text{V}] \approx 2.5 \times D_{int}[\text{nm}]$ .<sup>40</sup> Given this relationship the pore density of the hexagonally spaced arranged cells can be calculated by  $2/(3^{1/2} \times (D_{int}[\text{nm}] \times 10^{-7})^2)$ .<sup>40</sup> Figure 2.2(b) plots the pore density as a

function of anodization voltage and interpore spacing, where the inset schematics represent the relative spacing for each anodization condition.

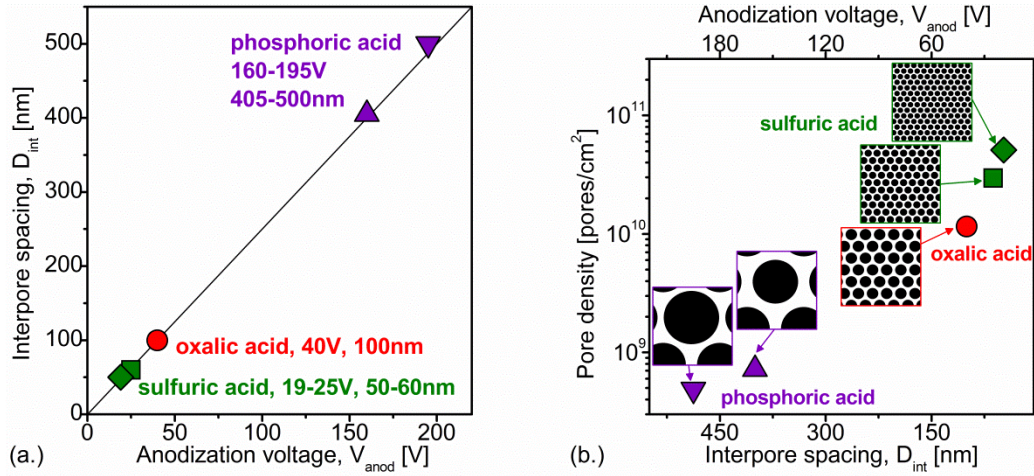
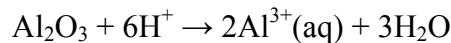


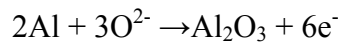
Figure 2.2 (a) Dependence of anodization voltage on interpore spacing,  $D_{int}$ , for various ordering regimes (as indicated by acids). [Adapted from Lee *et al.*<sup>40</sup>] (b) The effect  $D_{int}$  on the pore density (shown for mild anodization conditions) has an inverse relationship, bottom axis. The associated  $V_{anod}$  is shown on the top axis. Insets represent the relative interpore spacing.

### 2.3 Fabrication a highly ordered porous AAO nanotemplate

Two reaction mechanisms are necessary for the formation of porous AAO: (1) ejection of mobile  $Al^{3+}$  ions at the oxide-electrolyte interface into the electrolyte solution and (2) migration of  $OH^-/O^{2-}$  ions towards the metal-oxide interface, represented in the schematic in Figure 2.3. The ejection of  $Al^{3+}$  is associated with the dissolution of the oxide at the oxide-electrolyte interface where the following reaction occurs:



The migration of  $OH^-/O^{2-}$  is associated with oxide formation at the metal-oxide interface, where the following reaction takes place:



During steady-state pore formation, these reactions are balanced, resulting in equal dissolution and oxidation rates.

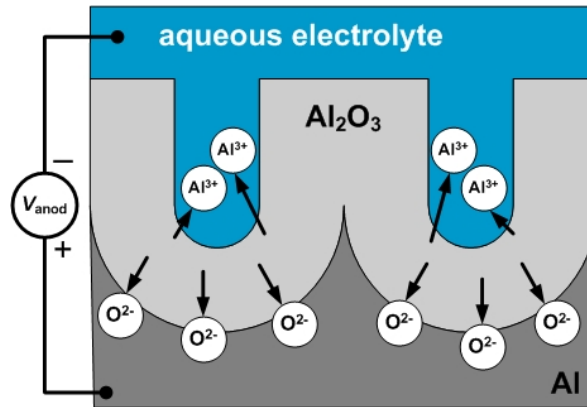


Figure 2.3 Schematic representing the ionic movement responsible for the dissolution of Al<sub>2</sub>O<sub>3</sub> by ejecting Al<sup>3+</sup>(aq) into solution and oxidation of Al through the migration of OH/O<sup>2-</sup> to the metal-oxide interface.

The anodization process for pore formation can be divided into 4 stages as reflected in the shape of the current density versus time plot. Figure 2.4(a) shows the current density as a function of time (stages a, b, c and d)<sup>45,48</sup> and Figure 2.4(b) schematically represents the structure of the oxide at each stage.<sup>45</sup> Initially (stage a), the ionic OH/O<sup>2-</sup> conduction is very high and results in the formation of an oxide barrier layer. The oxide formation current dominates the total current and decreases as the oxide layer thickens. During the second stage (stage b), cracks randomly propagate through the oxide barrier layer. Localized current flows to repair the crack, enhancing dissolution and oxide formation through this point. During stage b, the oxide formation current continues to decrease while the pore formation current begins to rise, resulting in a minimum total current, where stage c begins. The enhanced ionic conduction causes the pore formation current to create the pore cells and breakdown the initial oxide barrier. At the final stage (stage d), pore formation and growth begins as the current at the pore bases becomes uniform. Steady-state pore growth results in balanced and continued dissolution of the oxide near the oxide-electrolyte interface and formation of the oxide near the metal-oxide interface.

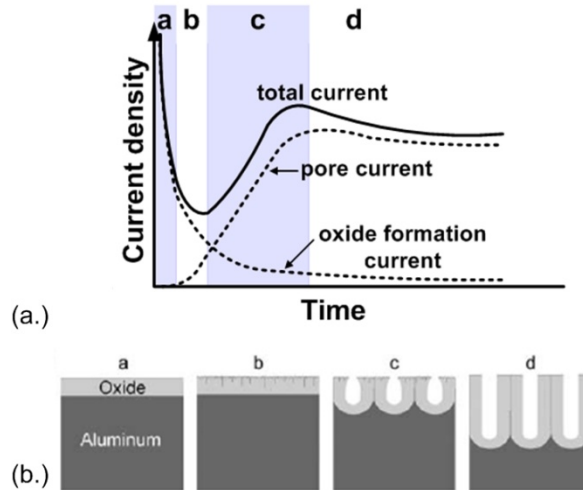


Figure 2.4 (a) Current density versus time profile for potentiostatic anodization of Al, showing the current contribution from oxide formation and pore formation. [Adapted from Hoar *et al.*<sup>48</sup> and Eftekhari *et al.*<sup>45</sup>] (b) Oxide formation at various stages. Stage a: forms an oxide barrier coating on the Al surface. Stage b: cracks propagate through oxide barrier. Stage c: pore cells form and break down barrier oxide. Stage d: lateral and steady-state pore growth. [Reprinted from Eftekhari *et al.*<sup>45</sup>]

Because pore initiation is random and as some pores continue to propagate while others are hindered by more dominating pores and the top of the porous membrane is random but the pores align near the base with continued anodization. Highly ordered templates (aligned pores from the top to the pore base) can be fabricated following a two-step anodization procedure.<sup>20</sup> Figure 2.5(a) shows the first anodization oxide. It generally requires that the first anodization forms 30-40  $\mu\text{m}$  of the porous oxide before optimum and uniform ordering is achieved at the pore base. Removing the oxide formed during first anodization leaves the Al surface with a scalloped texture (Figure 2.5(b)). This texturized surface results in highly ordered pores from the top to the base with subsequent anodization (Figure 2.5c).

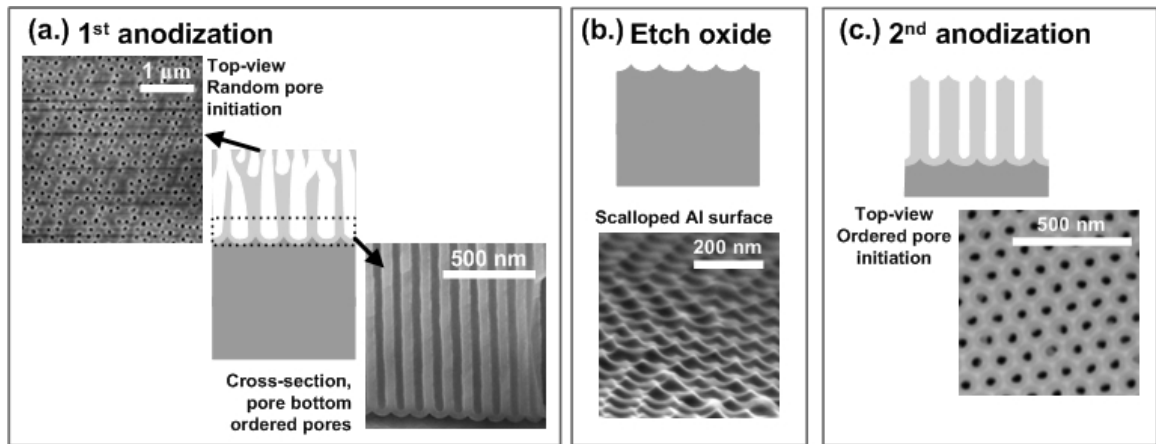


Figure 2.5 Schematics of AAO processing sequence for ordered AAO templates: (a) first anodization has random pore spacing at pore top (SEM, top left) and ordered pores at pore bottom (SEM, bottom right), (b) etch oxide for scalloped Al surface (SEM bottom), and (c) second anodization for ordered template.

Pre-texturing the surface with the scalloped texture is necessary for creating an ordered template from top to bottom. Upon second anodization the current initially localizes at the ridges forming a non-uniform barrier oxide – oxide is thicker at the ridges and flattens the metal-oxide interface. Shimizu *et al.*<sup>49</sup> and Thompson *et al.*<sup>50</sup> reported the growth of non-uniform oxide introduces stress within the oxide material between the thinner and thicker oxide regions, causing successive crack-and-heal events until the current concentrates at the (bottom) thinner oxide locations, where dissolution and oxidation continue and lateral pore formation begins.<sup>49,50</sup>

During the formation of the oxide anions from the electrolytic solution get trapped within the porous oxide sidewalls. Figure 2.6(a) shows the variety and movement of ions present during anodization in sulfuric acid.<sup>45,51</sup> The depth and concentration of anion incorporation depends on the mobility and conductivity of the species. Figure 2.6(b) shows the relative incorporation of various electrolytic ion species incorporations within the pore base.<sup>45</sup> Sulfate ions are nearly equally distributed through the entire oxide layer, while phosphate and oxalate anion concentrations remain equally distributed through

about  $\frac{3}{4}$  of the oxide layer and rise sharply near the oxide-electrolyte interface. Chromate ions reach a maximum concentration about  $\frac{1}{4}$  through the oxide formation layer from the electrolyte-oxide interface.

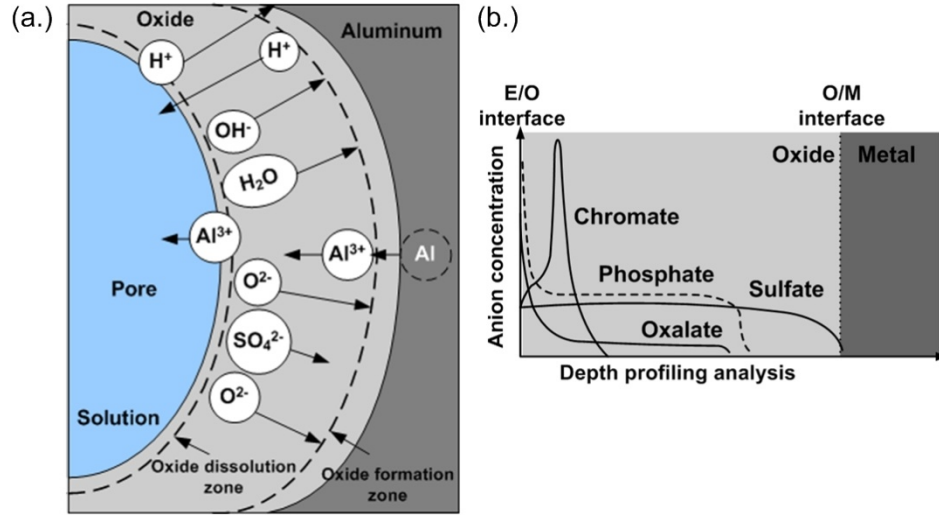


Figure 2.6 (a) Schematic representing the ionic conduction during steady-state pore growth and mobility of electrolytic anions through the cross-sectional barrier layer. [Adapted from Patermarakis *et al.*<sup>51</sup> and Eftekhari *et al.*<sup>45</sup>] (b) Anion incorporation as a result of electrolytic solution at pore base. [Adapted from Eftekhari *et al.*<sup>45</sup>]

## 2.4 Theories for self-alignment and ordering mechanisms of AAO

Two well accepted theories which explain the self-alignment phenomenon are the enhanced field-assisted mechanism and the volume expansion between alumina and aluminum are presented below. Several theories on the lateral growth of self-aligned pores have been proposed, and can be found elsewhere.<sup>45</sup>

### 2.4.1 Enhanced field-assisted mechanism

Chen *et al.*<sup>52</sup> proposed lateral pore growth mechanism occurs from the enhanced field at the scalloped pore base. Figure 2.7 represents the electric field and pore geometry of the pore base, showing the angle of the pore base,  $\omega$ , the radius of curvature



of the pore base at the metal-oxide interface,  $r$ , and the radius curvature of the pore base at the electrolyte-oxide interface,  $r_a$ , and the thickness of the barrier layer,  $b$ .

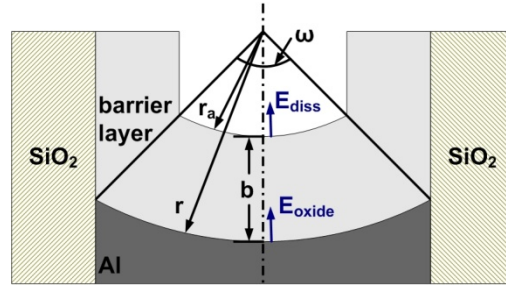


Figure 2.7 Schematic for the field-enhanced pore formation mechanism. The field at the oxide-electrolyte interface,  $E_1$ , and the field at the metal-oxide interface,  $E_2$ , are shown. [Adapted from Chen *et al.*<sup>52</sup>]

This theory suggests the self-alignment is a result of the shape of the barrier oxide layer determining the local electric fields responsible for porous oxide formation – the local electric field at oxide-electrolyte interface ( $r = r_a$ ) is responsible for dissolution and the local field at the oxide-metal interface ( $r = r_a + b$ ) is responsible for oxidation. The field across the barrier layer,  $E(r)$ , can be expressed as  $E(r) = J/\sigma$  where  $J$  is the current density ( $J = I/[\omega r^2]$ , and  $I$  is current,  $\omega$  is the angle of the scalloped barrier region). Solving for the constant voltage across the oxide,  $V$ , which is equal to the integral of  $E(r)$  with limits from  $r_a+b$  to  $r_a$  and where  $E(r) = I/(\sigma \omega r^2)$ , puts the electric field in terms of  $r$ ,  $r_a$  and  $b$  is given by the following equation:

$$E(r) = \frac{r_a \cdot (r_a + b) V}{r^2 b}$$

The local electric field at the top of the pore base (oxide-electrolyte interface) proportional to the rate of oxide dissolution where  $r = r_a$ ,  $E_{diss}(r = r_a)$  is given by

$$E_{diss}(r_a) = \frac{(r_a + b) V}{r_a b}$$

The local field at the bottom of the pore base (oxide-metal interface) proportional to the rate of oxide formation where  $r = r_a + b$ ,  $E_{\text{oxide}}(r = r_a + b)$  is given by

$$E_{\text{oxide}}(r_a + b) = \frac{r_a}{(r_a + b)} \frac{V}{b}$$

Under steady-state conditions, the rate of dissolution and rate of oxidation are equal. Therefore, the dimensions of the  $r_a$ ,  $b$  and  $r$  should remain constant under steady-state formation. If, however,  $r_a$  decreases (decreasing radius of curvature at electrolyte-oxide interface),  $E_{\text{diss}}(r_a)$  will increase to speed the rate of dissolution. If  $r_a$  increases (increasing the radius of curvature at the at the electrolyte-oxide interface),  $E_{\text{diss}}(r_a)$  will decrease to slow the dissolution of the oxide. A similar effect is observed for non-equilibrium values of  $b$ . If  $b$  becomes large,  $E_{\text{oxide}}(r_a + b)$  will decrease to slow the rate of oxidation at the oxide-metal interface. Conversely, if  $b$  becomes small,  $E_{\text{oxide}}(r_a + b)$  will increase and the rate of oxidation increases.

Chen *et al.*<sup>52</sup> also described the self-correcting nature of uniform porous dimension growth by the angle of the scalloped barrier region,  $\omega$ . Because  $E(r)$  is inversely proportional to  $\omega$ , if  $\omega$  is less than the equilibrium value (small cell size), then  $E(r)$  must increase until the value of  $\omega$  is restored to its larger equilibrium value, causing the size of the pore cell to increase. In a scenario where  $\omega$  is small and a competing neighboring pore cell has a maximum  $\omega$ , ( $\omega = 180^\circ$  flat pore base) then  $E(r)$  in the flat base cell will be smaller than  $E(r)$  in the cell base with  $\omega \neq 180^\circ$ . Lateral pore growth will stop in the flat bottom base cell where  $\omega = 180^\circ$  and continue in the cell where  $\omega \neq 180^\circ$ .

#### 2.4.2 Mechanical forces by volume expansion

Jessensky *et al.*<sup>53</sup> and Nielsch *et al.*<sup>42</sup> reported hexagonally, self-organized pores occur from the moderate volume expansion during the conversion of aluminum to alumina leading to mechanical stresses which provide repulsive forces between neighboring cells, forcing the lateral upward growth of the pore sidewalls. A schematic of this mechanism is shown in Figure 2.8.<sup>53</sup>

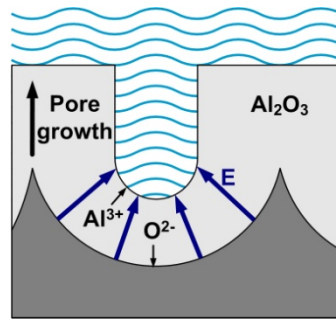


Figure 2.8 Schematic for the volume-expansion formation mechanism. The electric field is concentrated at the base of the pore, causing the sidewalls to move upward. [Adapted from Jessensky *et al.*<sup>53</sup>]

The volume expansion,  $\Delta$ , (also known as the Pilling-Bedworth Ratio) is defined as the ratio of volume of the oxide produced during anodization,  $V_{\text{oxide}}$ , to the volume of the aluminum consumed during oxidation,  $V_{\text{Al}}$ . The volume of the oxide,  $V_{\text{oxide}} = M_{\text{oxide}} / \rho_{\text{oxide}}$ , where  $M_{\text{oxide}}$  is the molar mass of the oxide, and  $\rho_{\text{oxide}}$  is the density of the oxide ( $\rho_{\text{oxide}} = 3.2 \text{ g/cm}^3$ ).<sup>42</sup> The volume of the total aluminum consumed  $V_{\text{Al}} = (2\text{-Al atoms}/\text{Al}_2\text{O}_3)M_{\text{Al}} / \rho_{\text{Al}}$ , where  $M_{\text{total}}$  is the molar mass of the oxide, and  $\rho_{\text{Al}}$  is the density of the oxide ( $\rho_{\text{Al}} = 2.7 \text{ g/cm}^3$ ).<sup>42</sup> Therefore, the volume expansion can be determined by

$$\Delta = \frac{M_{\text{oxide}} \cdot \rho_{\text{Al}}}{2M_{\text{Al}} \cdot \rho_{\text{oxide}}} f$$

The factor  $f$  takes into account the fraction of  $\text{Al}^{3+}$  ions contributing to the oxide formation, equal to  $[1 - (\# \text{Al}^{3+} \text{ ions})/(\text{total Al atoms})]$  since the formation process requires dissolution of the oxide by ejecting mobile  $\text{Al}^{3+}$  ions into the electrolytic solution. If all of the aluminum consumed is converted to oxide  $f \approx 1$  and a maximum volume expansion ratio will occur ( $\Delta \approx 1.6$ ). It was shown that  $f \approx 0.77$  (meaning 23% Al atoms are ejected into the electrolytic solution as  $\text{Al}^{3+}$ ), results in the optimum hexagonally, self-ordered structure with large ordering domain size, and thus  $\Delta \approx 1.2$ . If  $1.6 > \Delta > 1.2$ , the volume expansion is large and results in irregular growth, structural defects, and reduced ordering domain size.<sup>42,45,53</sup> If a greater amount of  $\text{Al}^{3+}$  ions are ejected into solution during anodization  $\Delta < 1.2$ , repulsive forces between neighboring cells is not large enough to promote ordering creating disordered pore arrays.

## 2.5 Formation of non-porous anodic alumina

The formation of non-porous anodic alumina referred to as barrier anodic alumina, BAA, occurs when aluminum is anodized in a neutral electrolytic solution. This is different to the formation of porous AAO, which occurs from anodizing in an acidic solution. The key difference in non-porous oxide formation mechanism is that  $\text{Al}^{3+}$  ions are not outwardly ejected into the electrolytic solution. Rather, mobile  $\text{Al}^{3+}$  ions heal any cracks at the oxide-electrolyte interface.<sup>33</sup> In a neutral solution there are more deprotonated species *i.e.*, anions, which can react with mobile  $\text{Al}^{3+}$  ions at the oxide-electrolyte interface and can form a complex oxide.<sup>54</sup> The oxide formation that forms is uniform, unlike the initial barrier layer formed for fabricating the porous oxide.<sup>49,50</sup> A schematic in Figure 2.9 represents the barrier layer formation on an aluminum surface

containing ridges for porous and non-porous anodization conditions. The barrier layer formed in the non-porous structure is uniform maintaining a non-flattened profile at the metal-oxide interface, unlike the barrier oxide layer formed during porous AAO anodization is non-uniform and flattens the metal-oxide interface.

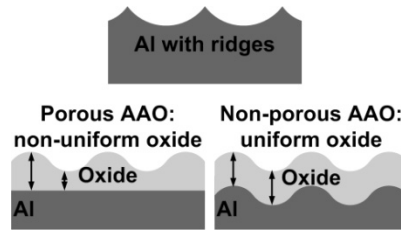


Figure 2.9 Schematic representing the difference in oxide growth during initial Al anodization for porous AAO and non-porous AAO when ridges in Al surface are present. The oxide growth formed prior to porous AAO growth is non-uniform (left), while the oxide formed with an anodization chemistry for creating non-porous films, barrier anodic aluminum (BAA), is uniform.

During anodization of a non-porous layer, the current versus time continues to exponentially decay with time<sup>55</sup> because the ionic conduction decreases with barrier film thickness. Figure 2.10 shows current-time curves for the formation of BAA on aluminum at various  $V_{\text{anod}}$ . Increasing  $V_{\text{anod}}$  increases the ionic conduction corresponding to the formation of a thicker oxide layer.

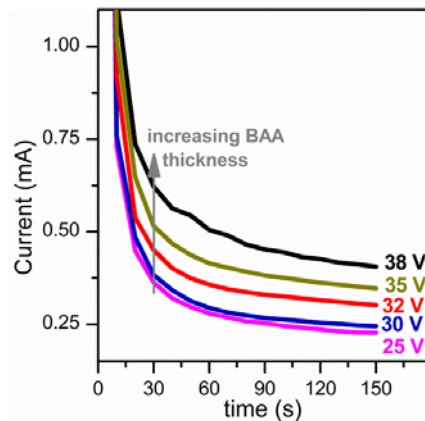


Figure 2.10 Current versus time for forming a BAA layer in an aqueous neutral electrolytic solution for 150 s. Increasing  $V_{\text{anod}}$  increases the current and thus, increases the thickness of the barrier anodic aluminum (BAA), or non-porous oxide film thickness. For all current-time curves, the continual decrease in current with time indicates no porous oxide formation.

## 2.6 Methods for fabricating AAO templates

Template preparation starts with electropolishing high purity 99.99% Alfa-Aesar Al sheets in 1:5 perchloric acid to ethanol solution. Porous AAO templates were fabricated following a two-step anodization procedure in 0.3 M oxalic acid at 40 V. Templates were highly ordered, with hexagonally spaced pores ( $D_{\text{int}} \sim 100$  nm and  $D_p \sim 40$  nm), resulting in pore densities of  $\sim 1.15 \times 10^{10}$  pores/cm<sup>2</sup>. Initial pore diameters were widened to  $D_p \sim 80$  nm in a 1:1 NH<sub>4</sub>OH:H<sub>2</sub>O solution. The final pore diameter can be controlled as a function of pore depth, L, and etching time, t. It was found that the pore depth does not contribute largely to the etching rate (assuming  $L \leq 10$  μm) and the final pore diameter can be estimated more simply by  $D_p$  [nm]  $\approx 2.5$  [nm/min]  $\times t$  [min].

The non-porous oxide, BAA was formed by anodizing an Al surface in a 2:1 KOH:oxalic acid electrolytic solution. Forming BAA on a first anodized Al surface altered the surface texture. (see Chapter 4.) ,

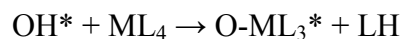
## Chapter 3: Atomic Layer Deposition (ALD)

### 3.1 Introduction

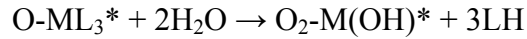
Atomic Layer Deposition (ALD) was developed as a method for depositing thin, defect-free, high-purity films.<sup>56</sup> It has become a key processing technique in the display and microelectronics industries where miniaturization has required precise atomic control of film thickness and conformal deposition.<sup>57</sup> Unlike Chemical Vapor Deposition (CVD), where precursors react in the gas-phase, ALD is a cyclic and self-limiting process based on sequential binary surface reactions.<sup>30,58-61</sup> ALD can be used to coat a variety of substrate materials (with typically amorphous) films because it is a low temperature process. Various recipes can be deposited consecutively since each precursor is introduced separately and many recipes have a wide deposition temperature window. Furthermore, this process is scalable, able to coat large and/or multiple substrates.<sup>61</sup>

#### 3.1.1 Processing sequence

Figure 3.1 shows an example of an ALD sequence for depositing a binary metal-oxide compound,  $\text{MO}_2$  (M represents a metal and O is oxygen), onto a hydroxyl functionalized surface. The basic deposition sequence includes the 4 following basic steps, also referred to as two half-cycles: (1) Exposure of the first precursor,  $\text{ML}_4$  (L represents a ligand group, *e.g.*  $\text{N}(\text{CH}_3)_2$ ), fully saturating the surface by reacting with all available surface sites and forming byproducts. The following surface reaction occurs:



Where \* indicates the surface group. The reaction results in a  $-ML_3$  terminated surface and with LH as the byproduct. (2) A system purge removes remaining unreacted precursor and LH byproducts, completing the first half-cycle. (3) Exposure of a second oxidizing precursor,  $H_2O$ , reacts at the remaining metal-ligand sites and the following reaction occurs:



(4) A second purge removes remaining unreacted precursor and byproducts from the system, completing the second half-cycle and one full cycle. The surface is  $-OH$  terminated (same to initial surface). The 4 basic steps are repeated with subsequent cycling, adding one monolayer of  $MO_2$  film per cycle.

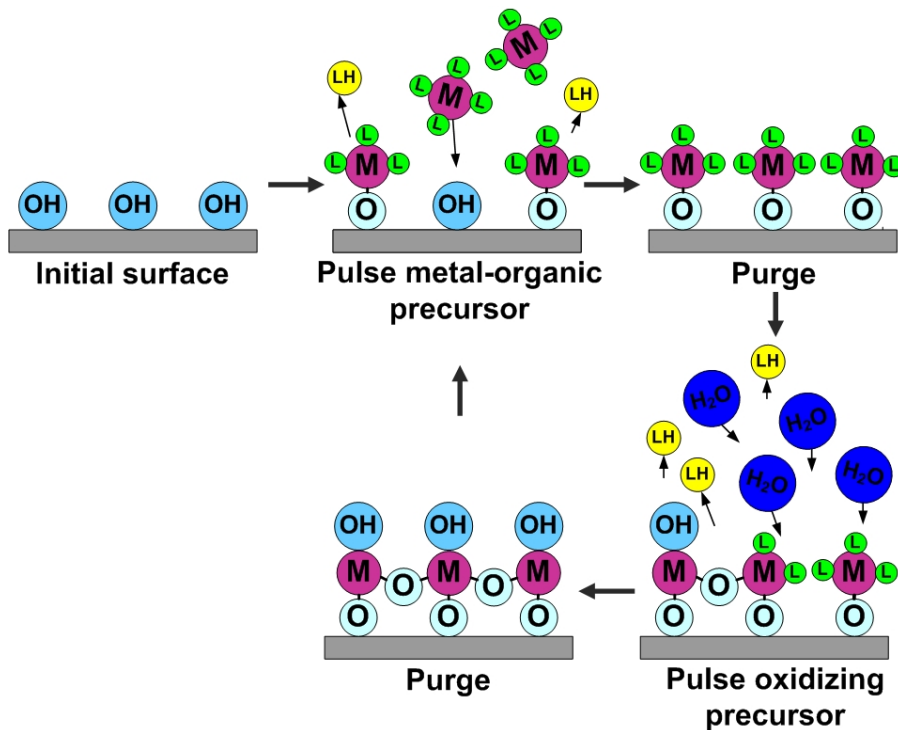


Figure 3.1 Schematic of one complete metal-oxide ALD cycle (clockwise): initial hydroxyl functionalized surface, pulsing a metal-organic precursor ( $ML_4$ ) reacts with surface sites, purge removes unreacted precursor and byproducts,  $H_2O$  pulse reacts with remaining ligands attached to metal site, final purge removes any unreacted precursor and byproducts. At the end of one cycle, one monolayer of material  $MO_2$  uniformly and conformal coats the entire surface.



The pulse-purge half-cycles must be optimized to ensure conformal coating of the substrate surface. The following example shows optimized pulse-purge half-cycles for deposition of  $\text{Al}_2\text{O}_3$  with trimethylaluminum (TMA) and  $\text{H}_2\text{O}$  precursors, resulting in a growth rate per cycle (GPC) of 0.084 nm.<sup>62</sup> Figure 3.2(a) shows the effect of the first half cycle pulse-purge lengths on deposition thickness per cycle (TMA precursor).<sup>62</sup> Increasing the TMA pulse increases GPC until  $\sim 100$  ms and then GPC plateaus indicating full saturation of the substrate surface and that the half-cycle is self-limiting. Increasing TMA purge time, however, causes GPC to fall before it plateaus where there is sufficient time for removing excess molecules (high GPC indicates somewhat of a CVD reaction). Figure 3.2(b) shows similar trends of the pulse and purge time on the GPC for the  $\text{H}_2\text{O}$  half-cycle with GPC plateauing at longer pulse-purge lengths than for the TMA half-cycle.<sup>62</sup> Recipes with self-limiting pulse-purge half-cycles result in linear monolayer growth with cycle number, as shown in Figure 3.2(c) for a  $\text{ZrO}_2$  film thickness as a function of cycle number.

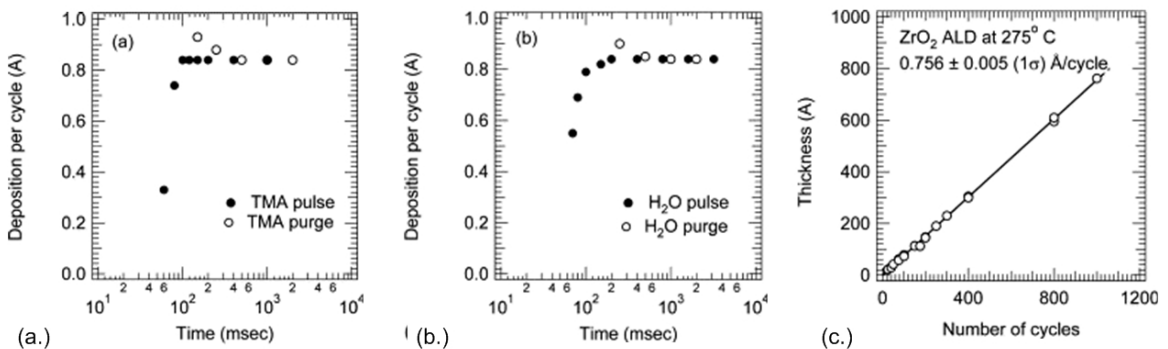


Figure 3.2 The effect of pulse and purge time on deposition per cycle of an  $\text{Al}_2\text{O}_3$  film (tri-methyl aluminum, TMA, and  $\text{H}_2\text{O}$  precursors). (a) Effect of TMA pulse and purge time and (b) effect on  $\text{H}_2\text{O}$  pulse and purge time. Saturation and self-limiting behavior occurs when GPC is 0.084 nm. (c) The thickness for a  $\text{ZrO}_2$  film increases linearly with the number of cycles. [Reprinted from Sneh *et al.*<sup>62</sup>]

### 3.1.2 Applications

A variety of materials can be deposited using ALD such as  $\text{HfO}_2$ ,  $\text{ZrO}_2$ ,  $\text{TiO}_2$  dielectrics for high- $\kappa$  applications,<sup>58,60</sup> transition metal nitrides like  $\text{TiN}$  and  $\text{TaN}$  for metallization barriers and gate metals,<sup>60,63,64</sup> and continuing development of precursors and recipes for depositing metals, like  $\text{W}$  and  $\text{Ru}$ .<sup>61,65</sup> The range of materials that can be deposited by ALD makes this a versatile deposition process in the semiconductor industry creating devices like dynamic access memory (DRAM), field-effect transistors (FET) and non-volatile memory (NVM) devices.<sup>58</sup> ALD is also used in the fabrication of transparent thin film transistors, sensitivity sensors, photovoltaics, biological implants,<sup>61</sup> micro- MEMS devices and protective coatings.<sup>60</sup>

### 3.2 ALD coatings on complex nanostructures

ALD is not a line-of-sight process because precursors diffuse to available surface sites resulting in conformal films on 2D and nano-3D geometries. Compared to other deposition techniques, the ALD processing temperature is relatively low around 100-200 °C<sup>66-69</sup> and a deposition temperature as low as 33 °C has been reported for  $\text{Al}_2\text{O}_3$ .<sup>66</sup> Therefore, a variety of materials can be used as substrates that would otherwise decompose at higher temperature processes, like many organic materials such as polymers, fibers and aerogels.<sup>58</sup> Deposition onto organic materials (*i.e.*, a disordered network of tangled fiber strands or a porous polymer sheet) coats the internal structure as precursors diffuse through voids/pores and adsorb onto available surface sites if the surface is not functionalized.<sup>61</sup> The binary reaction with the adsorbed precursor during the second half-cycle and continued cycling forms clusters that coalesce, eventually

coating the entire surfaces and a continuous film is deposited.<sup>61,70</sup> Thus, ALD is used for encapsulating such materials. Figure 3.3(a) shows an SEM of carbon aerogel coated with Ru<sup>71</sup> and Figure 3.3(b) shows Al<sub>2</sub>O<sub>3</sub> nanotubes coated on sacrificial polyvinyl alcohol fibers.<sup>72</sup>

ALD is also used to create very thin protective coatings on nanoparticles to maintain their inherent and enhanced thermal, optical, electrical, and mechanical properties that are otherwise degraded with continued load cycling or surface contamination.<sup>73-79</sup> ALD coatings can be used to make a negative mold of self-assembled nanoparticles. Figure 3.3(c) shows an array of nanobowls created from a 2D array of self-assembled spheres for large scale nanolithography applications.<sup>80</sup> Figure 3.3(d) is a field emission SEM (FESEM) image of a 3D array of self-assembled, hexagonally packed spheres were used for fabricating an inverse opal structure applicable for photonic crystals, optoelectronics, electromagnetic, or chemical/biological sensors.<sup>81</sup>

ALD is ideal for coating high aspect ratio structures uniformly and conformally, but the precursor flow mechanism is no longer diffusion-driven, but is molecular-driven within capillary pores only a few nanometers in diameter.<sup>61</sup> Elam *et al.*<sup>59</sup> showed that conformal coatings within a high aspect ratio structure containing ~65 nm diameter pores and ~50 μm in length required an exposure time up to ~ 30 s – ALD reactions were no longer diffusion limited.<sup>59</sup> Conformal deposition within high aspect ratio structures are shown in Figure 3.3(e) where ZrO<sub>2</sub> nanotubes were formed within a sacrificial polycarbonate template<sup>82</sup> and in Figure 3.3(f) where 100% conformal deposition of ZrO<sub>2</sub> into SiO<sub>2</sub> trenches.<sup>62</sup> Additional examples are listed in Table 3.1, including deposition

onto fibrous and porous networks, nanoparticles and ordered nanoparticle arrays, and high aspect ratio structures. 28,59,70,83-91

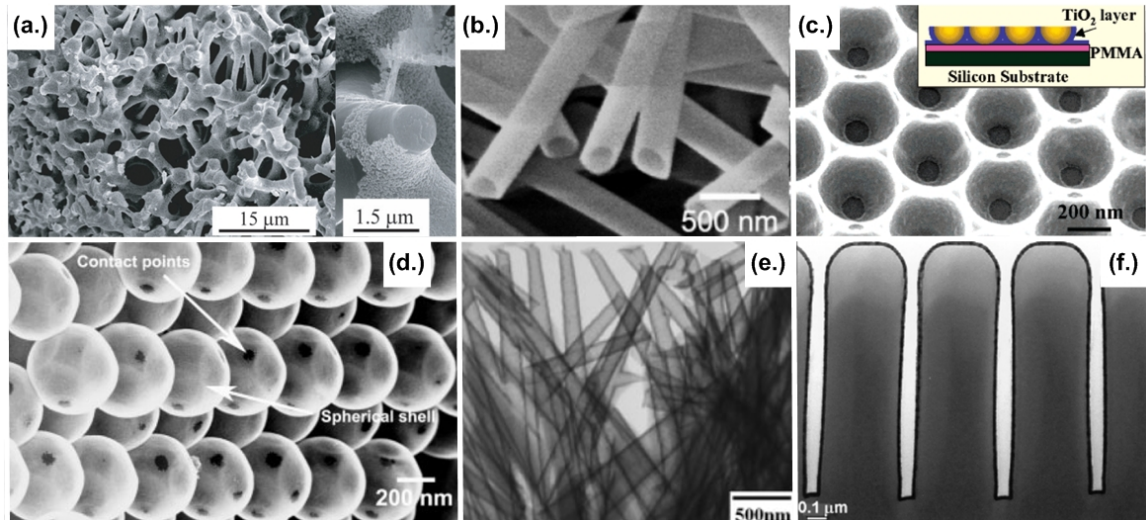


Figure 3.3 ALD coating on various 3D nano-structures. (a) SEM carbon aerogel coated with Ru (left) and a closer image (right) shows the broken carbon ligament and nucleation clusters of Ru. [Reprinted from Biener *et al.*<sup>71</sup>] (b) SEM image of Al<sub>2</sub>O<sub>3</sub> nanotubes created after deposition onto polyvinyl alcohol fibers and subsequent removal of fibers, inset shows hollow center of nanotubes. [Reprinted from Peng *et al.*<sup>72</sup>] (c) SEM image of nanobowls fabricated using polystyrene spheres on PMMA, ion milling and etching of the spheres. [Reprinted from Wang *et al.*<sup>80</sup>] (d) FESEM image of inverse opal structure fabricated by depositing TiO<sub>2</sub> onto silica spheres. [Reprinted from King *et al.*<sup>81</sup>] (e) TEM image of ZrO<sub>2</sub> nanotubes fabricated with a polycarbonate carbonate template. [Reprinted from Shin *et al.*<sup>82</sup>] (f) TEM image of high aspect ratio SiO<sub>2</sub> coated with 20 nm ZrO<sub>2</sub> shows 100% conformality. [Reprinted from Sneh *et al.*<sup>62</sup>]

	Substrate	ALD coating	Application	Reference
Polymers, fibers and nanoporous materials	SiO <sub>2</sub> aerogel	ZnO	Sensing	Kucheyev <i>et al.</i> <sup>83</sup>
	Aerogel	TiO <sub>2</sub>	Photovoltaics	Hamann <i>et al.</i> <sup>84</sup>
	C aerogel	W	Metal functionalization	Elam <i>et al.</i> <sup>85</sup>
	Nanocellulose and nano-fibrillar aerogel	TiO <sub>2</sub> , ZnO, Al <sub>2</sub> O <sub>3</sub>	Sensing, drug-release, encapsulation	Korhonen <i>et al.</i> <sup>86</sup>
	PVC, PS, PC, PP, PMMA *	W	Flexible optical mirror, gas diffusion barrier	Wilson <i>et al.</i> <sup>70</sup>
Nano particles	ZnO nanorods	Al <sub>2</sub> O <sub>3</sub>	Protective coating	Min <i>et al.</i> <sup>73</sup>
	ZrO <sub>2</sub> nanoparticles (62 nm diameter)	Al <sub>2</sub> O <sub>3</sub>	Protective coating	McCormick <i>et al.</i> <sup>74</sup>
	BN nanoparticles	Al <sub>2</sub> O <sub>3</sub>	Microelectronics	Wank <i>et al.</i> <sup>75</sup>
	Multi-walled carbon nanotube (MWCNT)	Al <sub>2</sub> O <sub>3</sub>	Microelectronics, chemical sensors	Lee <i>et al.</i> <sup>76</sup>
	MWCNT	Al <sub>2</sub> O <sub>3</sub> -W-Al <sub>2</sub> O <sub>3</sub>	Electronics (coaxial cable)	Hermann <i>et al.</i> <sup>77</sup>
	Single-walled (SW) CNT	HfO <sub>2</sub> and Al <sub>2</sub> O <sub>3</sub>	Electronics encapsulation	Farmer <i>et al.</i> <sup>78</sup>
	SWCNT	Al <sub>2</sub> O <sub>3</sub>	Electronics encapsulation	Farmer <i>et al.</i> <sup>79</sup>
High aspect ratios	Si trenches	Ir-Pt	Metal functionalization	Christensen <i>et al.</i> <sup>87</sup>
	Si and glassy C	HfO <sub>2</sub> and ZrO <sub>2</sub>	High-κ	Hausmann <i>et al.</i> <sup>88</sup>
	SiO <sub>2</sub> capillary tube	WN	Interconnects	Becker <i>et al.</i> <sup>89</sup>
	Si trenches	Cu	Interconnects	Solanki <i>et al.</i> <sup>90</sup>
	AAO	Al <sub>2</sub> O <sub>3</sub>	Conformality study	Elam <i>et al.</i> <sup>59</sup>
	AAO	HfO <sub>2</sub>	Conformality study	Perez <i>et al.</i> <sup>91</sup>
	AAO	TiN-Al <sub>2</sub> O <sub>3</sub> -TiN	Electronic devices	Banerjee <i>et al.</i> <sup>28</sup>

Table 3.1 A list of examples in literature of ALD coatings on various nanostructures and their applications. \*PVC: Polyvinyl chloride, PS: polystyrene, PC: polycarbonate, PP: polypropylene, PMMA: polymethylmethacrylate

### 3.3 Nanolaminate ALD films

ALD is ideal for creating nanolayered or nanolaminate films because: (1) the stacking sequence and multi-layer thicknesses sequence can be precisely controlled, (2) the saturating, self-limiting nature provides very sharp multilayer interfaces (as shown in Figure 3.4(a) with  $\text{Al}_2\text{O}_3$ - $\text{TiO}_2$  alternating stack for antireflection of optical mirror applications),<sup>92,93</sup> (3) various chemistries have large and overlapping temperature windows so consecutive deposition does not require temperature adjustment and (4) reactors equipped with multiple valves for various precursor sources enables alternating material deposition to occur without the to bring chamber to atmosphere (Figure 3.4(b),  $\text{W-Al}_2\text{O}_3$  stack repeated 16 times for Bragg reflectivity applications).<sup>94</sup>

Nanolaminate films are desirable because electrical, optical, mechanical or magnetic properties are different from either material used independently.<sup>95</sup> For example,  $\text{W/Al}_2\text{O}_3$  multilayer stacks have also been shown to reduce the thermal conductivity of thermal barrier coatings<sup>96</sup> since interfaces increase phonon scattering.<sup>97</sup> Nanolaminates have also shown improved performance for high- $\kappa$  dielectric applications, maintaining a relatively large  $\kappa$  value while having high leakage resistance. Figure 3.4(c) shows a high resolution TEM (HRTEM) image reported by Kim *et al.*<sup>98</sup> of a  $\text{HfO}_2/\text{ZrO}_2$  nanolaminate film with high- $\kappa$  and low leakage currents. Additional examples of nanolaminate structures are listed in Table 3.2.<sup>62,93,96,98-102</sup>

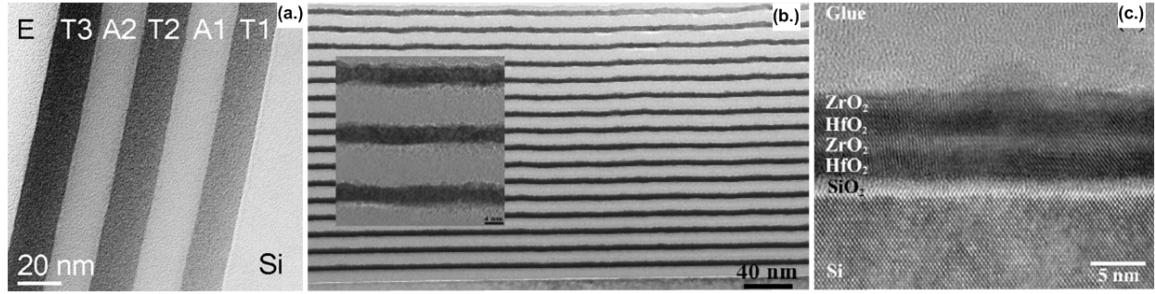


Figure 3.4 (a) TEM image showing a stack of alternating  $\text{TiO}_2$  and  $\text{Al}_2\text{O}_3$  on Si, where T1-3 indicates  $\text{TiO}_2$  and A1-2 indicates  $\text{Al}_2\text{O}_3$  layers, and sharp interfaces are observed. [Reprinted from Mitchell *et al.*<sup>92</sup>] (b) SEM image of W/ $\text{Al}_2\text{O}_3$  stack on Si(100) (dark layers are W and lighter layers are  $\text{Al}_2\text{O}_3$ ), repeated 16 times and inset of TEM image showing a higher resolution image of the stack and the sharp bilayer interfaces. [Reprinted from Fabreguette *et al.*<sup>94</sup>] (c) HRTEM image of a nano-laminate structure on  $\text{SiO}_2$  containing  $\text{HfO}_2$  and  $\text{ZrO}_2$  layers shows no significant intermixing of the two materials. Subsequent deposition of  $\text{ZrO}_2$  induces crystallization of the previous  $\text{HfO}_2$  layer and epitaxial growth of subsequent layers follows. [Reprinted from Kim *et al.*<sup>98</sup>]

ALD nanolaminate stack	General results	Application	Reference
AlP / GaP	Smooths substrate surface roughness	Multi-layer mirrors	Ishii <i>et al.</i> <sup>99</sup>
$\text{Ta}_2\text{O}_5 / \text{Al}_2\text{O}_3$	Increased leakage resistance over $\text{Ta}_2\text{O}_5$	High- $\kappa$	Kukli <i>et al.</i> <sup>100</sup>
$\text{ZrO}_2 / \text{Al}_2\text{O}_3$	Increased leakage resistance over $\text{ZrO}_2$ and $\text{Ta}_2\text{O}_5$	High- $\kappa$	Kukli <i>et al.</i> <sup>100</sup>
$\text{HfO}_2 / \text{Al}_2\text{O}_3$	Improved dielectric	High- $\kappa$	Cho <i>et al.</i> <sup>101</sup>
$\text{Al}_2\text{O}_3 / \text{Hf}_x\text{Al}_y\text{O}_z$ (varying Hf Al O composition)	Higher thermal stability	Gate dielectrics	Sneh <i>et al.</i> <sup>62</sup>
W / $\text{Al}_2\text{O}_3$	Reduced thermal conductivity	Barrier coating	Costescu <i>et al.</i> <sup>96</sup>
$\text{ZrO}_2 / \text{HfO}_2$	Stacking sequence and roughness/morphology	High- $\kappa$	Kim <i>et al.</i> <sup>98</sup>
$\text{Al}_2\text{O}_3 / \text{TiO}_2$	Tailoring refractive index	Optical films	Zaitso <i>et al.</i> <sup>93</sup>
Hf-La oxide alloy	Increased breakdown strength over $\text{HfO}_2$	High- $\kappa$	Tang <i>et al.</i> <sup>102</sup>

Table 3.2. A list of some examples in literature using ALD nanolaminates for improved performance properties.

### 3.4 Doping ALD films to improve electrical performance

Doped films with highly repeatable doping concentrations can be fabricated with ALD. For example, a metal-oxide,  $MO_x$ , can be doped with element D (D-doped  $MO_x$ ) by depositing  $n$  cycles of  $MO_x$  followed by 1 cycle of D-oxide (molecular formula  $D_yO_z$ ). This ratio is called a supercycle, which is repeated until the desired thickness is reached. Assuming the deposition of  $MO_x$  onto  $D_yO_z$  is not energetically hindered and vice versus<sup>103</sup> the growth rate per cycle, GPC, will not deviate from the case where  $MO_x$  is deposited directly onto  $MO_x$  ( $GPC_{MO_x}$ ) and where  $D_yO_z$  is deposited directly onto  $D_yO_z$  ( $GPC_{D_yO_z}$ ). The atomic percent of D, at.% D, is the number of D atoms per total number of atoms in one supercycle is given by,

$$\text{at.\% D} = \frac{\frac{\# \text{ D atoms}}{D_y O_z} \times \frac{GPC_{D_y O_z}}{V_{m, D_y O_z}}}{\left( \frac{\# \text{ D atoms}}{D_y O_z} \times \frac{GPC_{D_y O_z}}{V_{m, D_y O_z}} \right) + \left( n \text{ cycles} \times \frac{\# \text{ M atoms}}{MO_x} \times \frac{GPC_{MO_x}}{V_{m, MO_x}} \right)}$$

where  $V_{m, MO_x}$  is the molar volume of  $MO_x$ , defined as the density of  $MO_x$  divided by the molar mass of  $MO_x$  and  $V_{m, D_y O_z}$  is the molar volume of  $D_y O_z$ , defined as the density of  $D_y O_z$  divided by the molar mass of  $D_y O_z$ . Thus, increasing  $n$  cycles reduces the at.% of D in  $MO_x$ . Two examples of Al-doped metal oxides are discussed below.

#### 3.4.1 Improving dielectric performance of $TiO_2$ with Al-doping (ATO)

Thin films of  $TiO_2$  have been investigated for their dielectric properties as replacements for insulators in microelectronic devices such as field effect transistors (FETs) and dynamic access memory (DRAM) capacitors.<sup>104-106</sup> Maximizing the dielectric constant,  $\kappa$ , and hence capacitance and minimizing intrinsically high leakage



current is required to improve performance and speed while reducing power consumption in modern microelectronics. To achieve high- $\kappa$  and low leakage, two methods are commonly used: (1) thermal annealing to enhance crystallinity, thereby enhancing  $\kappa$ ,<sup>107</sup> which can be as high as 80 for crystalline TiO<sub>2</sub> (rutile phase)<sup>16</sup> and (2) adding modest amounts of substitutionally doped elements to TiO<sub>2</sub> to tailor nucleation and growth rates during annealing.<sup>15,108,109</sup> Past work studied both effects with increasing the at.% Al and anneal time.<sup>110</sup> Sample compositions evaluated were 1 cycle Al<sub>2</sub>O<sub>3</sub> to 50 cycles TiO<sub>2</sub> (1.7 at.% Al) referred to as 1:50ATO, 1 cycle Al<sub>2</sub>O<sub>3</sub> to 20 cycles TiO<sub>2</sub> (4.1 at.% Al) referred to as 1:20ATO and purely TiO<sub>2</sub> films are referred to as 0:1ATO. All ATO as-deposited films were ~25 nm thick and increased ~1-2 nm in thickness after 300 s of annealing. Changes in the ATO film and/or growth of an interfacial oxide layer between the film and substrate surface are expected with annealing.<sup>111</sup> The crystalline phase detected after annealing was anatase, increasing with anneal time and with decreasing at.% Al.

The effect of Al-doping on leakage current is shown in Figure 3.5(a). As-deposited films all have high leakage, however, leakage for as-deposited films decreases by a factor of 4 and 5 for 1:50ATO and 1:20ATO films, respectively, as compared to the 0:1ATO film. This reduction in leakage is attributed to the slight increase in Schottky barrier height for contacts to TiO<sub>2</sub> with Al-doping.<sup>14,106</sup> Leakage currents for 0:1ATO remain high with annealing. Annealing the 1:50ATO and 1:20ATO films dramatically reduces leakage currents ( $10^3\times$ ) even with brief annealing, after which the leakage remains low for all extended anneal conditions. While an increase in Schottky barrier height is also expected for annealed 1:50ATO and 1:20ATO films, the Al-doping is not expected to increase the ATO barrier height enough to explain such a profound effect on

leakage currents. Rather, this dramatic effect is attributed to effect of Al-doping on the microstructure, that Al-doping reduced grain growth which reduces percolation pathways within the film.

Figure 3.5(b) shows the dielectric constant,  $\kappa$ , measured at 10 kHz as a function of annealing time.  $\kappa$  of the as-deposited films could not be measured due to high leakage. The  $\kappa$  decreases with Al-doping, as this is expected since  $\kappa$  of  $\text{TiO}_2$  (anatase) is 30-40<sup>104,112</sup> versus 9 for  $\text{Al}_2\text{O}_3$ .<sup>16</sup> Since the ATO films have a high  $\kappa$  even thin layers of an interfacial oxide can significantly decrease  $\kappa$ . For example, growth of even a 1.6 nm interfacial oxide layer with  $\kappa = 4$  next to a 25 nm ATO layer with  $\kappa = 40$  will result in a net series capacitance with  $\kappa$  value of only 24. The interfacial oxide growth during annealing is attributed to the decrease in  $\kappa$  with annealing. While this interfacial oxide supports the trend of  $\kappa$ , it does not account for the reduction in leakage current since the interfacial oxide growth for ATO compositions is expected to be relatively equal.

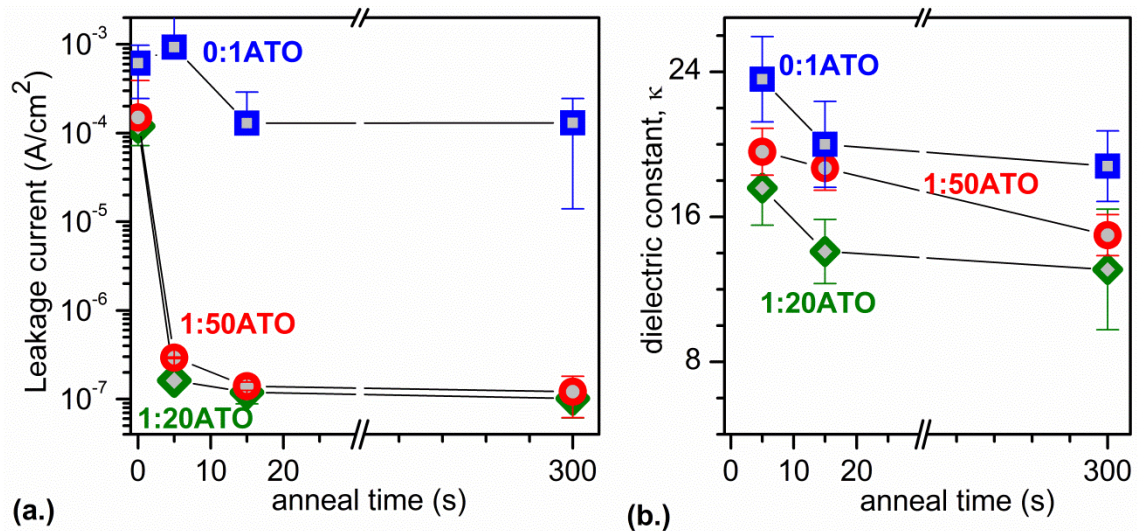


Figure 3.5 Improving the performance of dielectric films with ALD. (a) Effect of doping as a function of annealing time on leakage current densities at 1 MV/cm. Dramatic decrease in leakage currents after 5 s of annealing at 600°C for 1:50ATO and 1:20ATO (1:50 and 1:20 represent the supercycle ratio). (b) The dielectric constant for the films shown in (a) measured at 10 kHz.

The considerable drop in leakage for Al-doped samples ( $10^4\times$ ) compared to the undoped ( $10\times$ ) demonstrates that a more important leakage current reduction mechanism is generated by low-level Al-doping with ALD. These doped films showed significant reduction in leakage currents, while maintaining a  $\kappa$  about  $2.5\times$  larger than that of  $\text{Al}_2\text{O}_3$ .

### 3.4.2 Optimizing conduction of transparent Al-doped ZnO (AZO)

Transparent conducting oxides can be used in a variety of technologies including solar cells,<sup>113,114</sup> displays,<sup>113-115</sup> organic light emitting diodes,<sup>115,116</sup> transparent thin film transistors<sup>113,114</sup> and energy saving windows.<sup>113,114</sup> Al-doped ZnO (AZO) is an attractive transparent conducting oxide because transmits over a wide range of the visible spectrum,<sup>117,118</sup> it is non-toxic, abundant and cheap.<sup>113</sup> ZnO is conductive, but introducing  $\text{Al}^{3+}$  dopant ions provide extra electronic charge carriers, making AZO an n-type conductor.<sup>69</sup>

Elam *et al.*<sup>119</sup> reported that ALD AZO films could reduce the crystallinity within the film, having a smoother surface texture with increased Al-doping. Reduced surface roughness improves the performance of the material because high surface roughness will reduce electronic conduction and introduce contact resistance.<sup>114</sup> Later, it was reported that varying the Al-dopant concentration (from conducting at 0% to insulating at 100%) changed the resistivity 18 orders of magnitude, with a minimum resistivity  $\sim 10^{-3}$   $\Omega\text{-cm}$  for 98% Zn content.<sup>69</sup>

Banerjee *et al.*<sup>118</sup> reported the structural, optical and electrical properties of AZO films with low-level doping. Similar to results reported by Elam *et al.*<sup>119</sup> the surface roughness decreased with increasing Al concentration.<sup>118</sup> Optical transmission of AZO reached as high as  $\sim 80\text{-}90\%$  the visible spectrum and increasing Al concentration

widened the visible transmission window with a blue-shift of the absorption edge.<sup>117,118</sup> With low-level Al concentration, the Al<sup>3+</sup> ions substitutionally-doped Zn<sup>2+</sup> sites resulting in the n-type conduction and the films becomes as more conductive as the Al<sup>3+</sup> donor ions elevate the Fermi level above the conduction band (becoming degenerate, decreasing AZO resistivity).<sup>69,118</sup> However, an decrease in the conductivity is observed beyond ~3 at.% Al-doping, which was attributed to increased defects (scattering events) and the formation of a non-conducting or meta-stable phase clusters.<sup>69,117,120</sup>

Figure 3.6 shows the electrical properties taken by Hall measurements at room temperature.<sup>118</sup> The supercycle ratios of 40 ZnO cycles:1 Al<sub>2</sub>O<sub>3</sub> cycle and 5 ZnO cycles:1 Al<sub>2</sub>O<sub>3</sub> cycle correspond to the doping concentration at 1.5 at.% and 24.6 at.%, respectively.<sup>118</sup> The carrier concentration reaches a broad maximum. The drop in carrier concentration with increased Al-doping was attributed to the number of Al<sup>3+</sup> ions exceeding the maximum amount of substitutionally-doped Al<sup>3+</sup> ions within the ZnO structure where the Al<sup>3+</sup> ions do not act as donors and contribute to the segregation or formation of some meta-stable phase. The reduced mobility of carriers is attributed to the reduced crystallinity of the films with increasing Al<sup>3+</sup> and the maxima of resistivity (inversely proportional to conductivity, related to mobility and carrier concentration) reaches a minimum at 3.0 at.%.<sup>118</sup> Low-levels of Al<sup>3+</sup> doping can improve the conductive properties of ZnO and transparent conducting AZO can be deposited with repeatable doping concentrations using ALD.

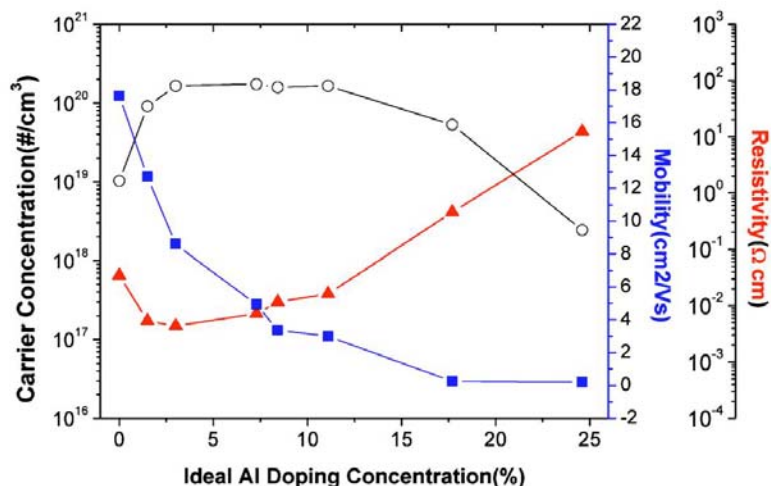


Figure 3.6 Electrical characterization of AZO with various Al-doping concentrations, showing low-level doping by ALD has improved electrical performance. Doping level ~2.5% has largest carrier concentration (-o-), increased mobility (-□-) and lowest resistivity (-Δ-). [Reprinted from Banerjee *et al.*<sup>118</sup>]

### 3.5 Deposition recipes for MIM trilayers

The chamber was held at 175 °C, while the tetrakis (dimethylamido) titanium (TDMAT) precursor as kept at 34 °C and the NH<sub>3</sub> precursor was maintained at 25 °C. 40 cycles were deposited at a rate of ~0.1 nm/cycle, in line with reported values.<sup>121</sup> For all samples, MIM layers were deposited in the same reactor. The chamber was set to 150 °C and all precursors were maintained at 25 °C. The top and bottom electrode were made from Al-doped ZnO (AZO). The bottom electrode was deposited by alternating 1 Al<sub>2</sub>O<sub>3</sub> cycle (trimethyl aluminum (TMA) and H<sub>2</sub>O precursors) after 10 ZnO cycles (diethyl zinc (DEZ) and H<sub>2</sub>O precursors) 5 times. This provided a target thickness of 10.5 nm AZO, given the growth rates of an Al<sub>2</sub>O<sub>3</sub> and ZnO cycle are ~0.1 nm/cycle and ~0.2 nm/cycle, respectively.<sup>118</sup> 80 cycles of Al<sub>2</sub>O<sub>3</sub> deposited the 8 nm insulator layer. The 102.5 nm top electrode was deposited by alternating 1 Al<sub>2</sub>O<sub>3</sub> cycle to 20 ZnO cycles 25 times.

## Chapter 4: Nanoengineering strategies for metal-insulator-metal electrostatic capacitors

### 4.1 Abstract

Nanostructures can improve the performance of electrical energy storage devices. Metal-insulator-metal (MIM) electrostatic capacitors fabricated in a three-dimensional cylindrical nanotemplate of anodized aluminum oxide (AAO) porous film have shown profound increase in device capacitance (100X or more) over planar structures. However, inherent asperities at the top of the nanostructure template cause locally high field strengths and lead to low breakdown voltage. This severely limits the usable voltage, the associated energy density ( $\frac{1}{2}CV^2$ ), and thus the operational charge-discharge window of the device. An electrochemical technique, complementary to the self-assembled template pore formation process in AAO film, has been developed that provides nanoengineered topographies with significantly reduced local electric field concentrations, enabling breakdown fields up to 2.5× higher (to > 10 MV/cm) while reducing leakage current densities by one order of magnitude (to  $\sim 10^{-10}$  A/cm<sup>2</sup>). In addition, methods of optimizing the AAO template and nanopore dimensions are investigated for increasing the capacitance per planar unit area by another 20%. As a result, the MIM nano capacitor devices achieve an energy density of  $\sim 1.5$  Wh/kg — the highest reported.

## 4.2 Introduction

Past work has shown that nanostructured designs of three-dimensional (3D) solid state metal-insulator-metal (MIM) electrostatic capacitors can achieve major advances in energy density (effective planar capacitance, EPC) compared to planar devices.<sup>19,28,29,122</sup> Recently, Bof Bufon *et al.* demonstrated a self-assembly technique for fabricating ultracompact capacitors with areal capacitance of up to  $\sim 200 \mu\text{F}/\text{cm}^2$ .<sup>122</sup> Beginning with a planar device (large footprint, relatively low areal capacitance), the inherent differential multi-layer stresses transformed the planar structure into self-wound 3D ultracompact capacitor (reduced footprint, thus increased areal capacitance).<sup>122</sup> However, scaling to fill the remaining surface area with additional rolled-up capacitors seems a major challenge. Earlier, Banerjee *et al.* demonstrated an EPC of  $\sim 100 \mu\text{F}/\text{cm}^2$  with  $> 10\text{X}$  increase in energy density for nanostructured electrostatic capacitors<sup>28,29</sup> by combining a 3D nanopore template of anodic aluminum oxide (AAO) with multilayer film deposition into the nanopores using atomic layer deposition (ALD).<sup>7</sup> AAO fabrication exploits natural, self-assembly during the anodization process, resulting in a highly-regular, highly-ordered network of pores with high aspect ratios.<sup>20</sup> The self-limiting nature of ALD provides precise monolayer thickness control, which translates into exceptional conformality for inserting ultrathin multilayer coatings uniformly into the nanopores to form the MIM devices.<sup>58,59</sup>

While the nanostructured AAO template provides substantial area enhancement resulting in significantly higher effective planar capacitance densities compared to conventional planar thin film arrangements,<sup>22,26,27</sup> the associated AAO nanotopography introduces several technical challenges, depicted in Figure 4.1, that can substantially limit

critical performance metrics. Nanoroughness and trapped impurities at the AAO sidewalls, resulting from the anodization process, can increase leakage current densities, thereby decreasing charge retention time.<sup>28,29</sup> More dramatically, are the sharp inter-pore asperities that result from the self-assembly nanopore ordering phenomenon. Arrays of parallel storage nanodevices formed over these asperities experience local high electric fields, leading to premature (low field) breakdown). (see Chapter 1) Means to bypass these inherent defect sources are needed to develop viable energy nanotechnologies based on AAO templates.

Despite these considerations, nanostructured AAO-based MIM devices<sup>28,118</sup> have shown dramatic increases in energy density (> 10X), employing (1) AAO pore widening to remove impurity-contaminated regions and (2) deposition of an ALD passivation layer under the MIM structure to smooth the nano-topography.<sup>30</sup> While significantly reducing leakage current, these techniques did not avoid low field breakdown in the range 4 MV/cm, well below the 12 MV/cm breakdown field reported for Al<sub>2</sub>O<sub>3</sub> dielectrics in DRAM structures.<sup>28</sup> Since the gravimetric energy density  $E$  of electrostatic capacitors is a strong function of voltage ( $E = \frac{1}{2}CV^2$ , where  $C$  is capacitance and  $V$  is applied voltage), significant increases in energy density can only be reached if the operating voltage window is extended well beyond the low field breakdown regime caused by inherent asperities in the AAO nanotopography.

This Chapter considers key aspects of process optimization for AAO template formation, ALD layer parameters, and the resulting performance metrics for AAO-ALD based electrostatic nanocapacitors, all important considerations in nanodevice design. Here, an electrochemical nanoengineering technique is described, complementary to the



AAO fabrication process that effectively tailors the nanotopography by transforming sharp interpore peak asperities into smooth, rounded peaks that diminish local electric fields. Microcapacitor devices are fabricated on these nanoengineered templates, each consisting of more than 5 million nanocapacitors wired together in parallel. As a result, the electrical performance is significantly improved, achieving energy densities of  $\sim 1.5$  Wh/kg (compared to 0.7 Wh/kg reported by Banerjee *et al.*<sup>28</sup>). Breakdown occurs at much higher fields, around 10 MV/cm, significantly increasing the operating voltage window and approaching intrinsic breakdown fields of the  $\text{Al}_2\text{O}_3$  insulator. Finally, the projected performance benefits that can be expected from this advance are assessed.

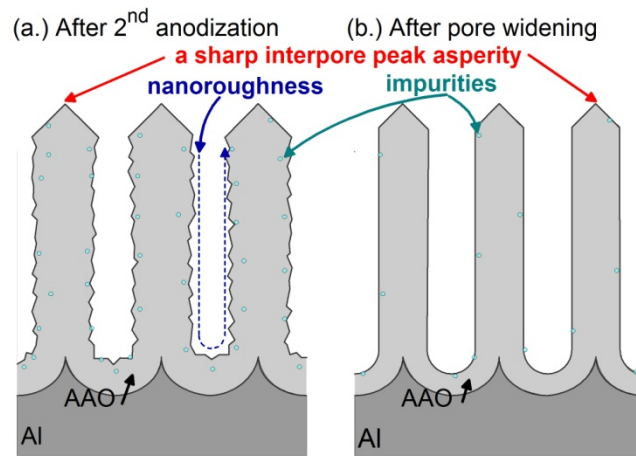


Figure 4.1 Schematic of AAO cross-section depicting the challenges of using AAO as a template for MIM capacitors. (a) Inherent interpore peak asperities cause premature breakdown, while nanoroughness of sidewalls and trapped impurities increase leakage current densities. (b) Pore widening smoothes sidewalls removes impurities but does not blunt interpore peak asperities and does not reduce interpore asperities.

### 4.3 Theory and Results

#### 4.3.1 Geometric modeling and Optimization of Nanocapacitors and Arrays

AAO template design is addressed to maximize equivalent planar capacitance (EPC) – *i.e.*, energy density per unit planar surface area - within the constraints of

available electrochemical processes for AAO formation, nanopore modification, and embedding of typical MIM nanocapacitor layers within the nanopores.

Prior to MIM layer deposition and after the nanopore template is established, pore widening techniques can be used to enlarge pore diameters independent of  $D_{\text{int}}$ . Figure 4.2 schematically represents increasing pore diameters for a given inter pore spacing. To convey the message of this work, the discussion is simplified by choosing a restricted parameter space – design guidelines limited the pore diameter ( $D_p$ ) to not exceed  $0.8 \times$  the inter pore spacing  $D_{\text{int}}$  and selected pore lengths (or AAO thicknesses,  $L$ ) of  $1 \mu\text{m}$ .

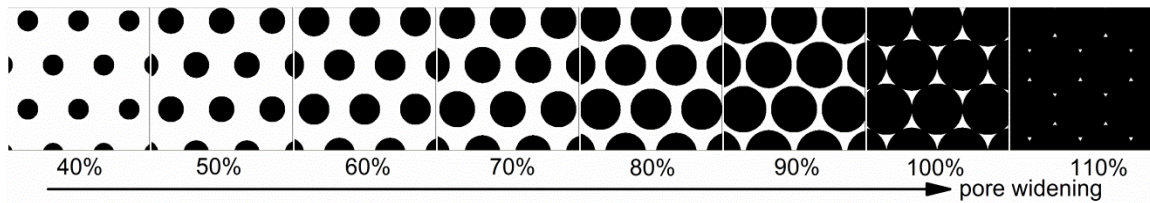


Figure 4.2 Schematic top-view of AAO template, where white regions indicate oxide and black regions indicate the pore openings. Pore widening increases the sidewall surface area, but widening beyond 100% degrades template integrity and stability.

AAO template top-view and cross-section schematics for various anodization chemistries are shown in Figure 4.3(a) to illustrate how pore density influences the surface area available in the template. For deep pores with high aspect ratio AR (defined as pore depth/pore width), the presence of the pores dramatically increases the available surface area relative to that for a flat, planar surface. Accordingly, the enhancement factor (AEF) is defined as the total surface area (including pore sidewalls, pore bottom, and template top region between pores) per unit planar surface area. Figure 4.3(a) clearly shows that smaller inter pore spacings results in greater pore densities and larger AEF.

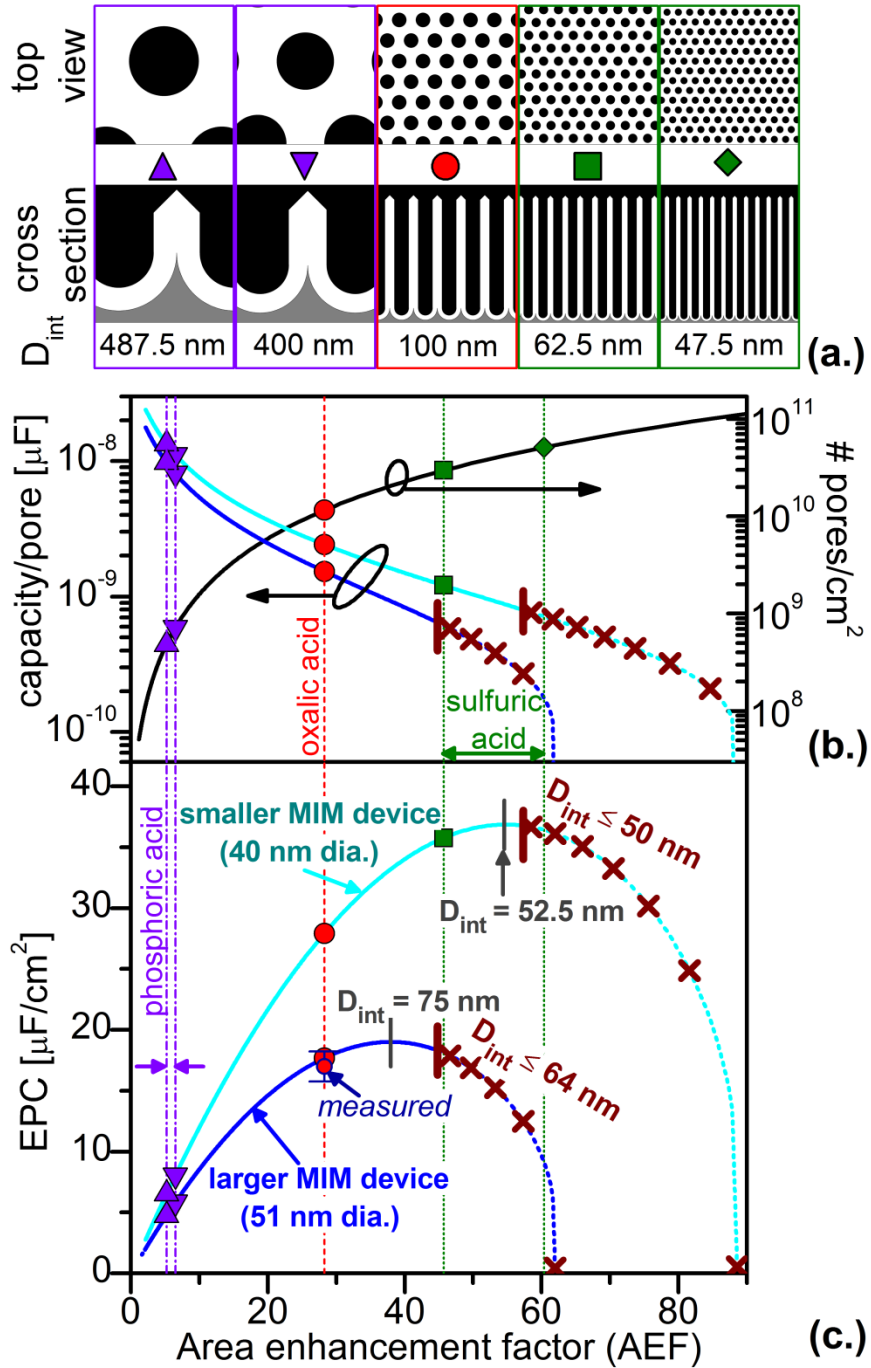


Figure 4.3 (a) Schematics of various anodization chemistries. Anodization voltages from left to right: 195, 160, 40, 25, and 19 V, where purple, red, and green symbols indicate phosphoric, oxalic, and sulfuric chemistries. (b) Increasing nanopore density (i.e., reduced  $D_{int}$ ) increases the area enhancement factor (AEF) but narrower pores reduce the capacity of each nanocapacitor. (c) Effective planar capacitance (EPC) for various anodization chemistries and AEFs for  $L = 1 \mu\text{m}$ ,  $D_p = 0.8D_{int}$ , dielectric constant,  $\kappa = 9$ . The times symbols ( $\times$ ) indicate where the specified finite MIM layers no longer fit within the pore diameters.

MIM device layer configurations are based on Al-Zn-oxide (AZO)<sup>69,118,123</sup> as the conducting top electrode (TE) and bottom electrode (BE), with Al<sub>2</sub>O<sub>3</sub> as the dielectric. Two specific parameter sets are considered, denoted by TE-dielectric-BE. One, referred to as the “larger MIM device” has a 51 nm diameter and is specifically a 10.5 nm AZO-8 nm Al<sub>2</sub>O<sub>3</sub>-7 nm AZO configuration, while the “smaller MIM device” has a 40 nm diameter and is 7 nm AZO-6 nm Al<sub>2</sub>O<sub>3</sub>-7 nm AZO. The choice of MIM layer thicknesses defines a minimum pore diameter required to accommodate the full MIM structure within the pore, although the resulting pore diameter may or may not be accessible by known chemistries for nanoporous AAO formation.

The capacitance for a device within a single nanopore (*i.e.*, an individual nanocapacitor) and the areal density of nanocapacitors (or nanopores) are plotted as a function of AEF in Figure 4.3(b) (top). For increasing AEF (*i.e.* smaller  $D_{\text{int}}$ ) the nanocapacitor areal density increases (right axis, Figure 4.3(b)). However, the capacity per nanocapacitor (left axis, Figure 4.3(b)) decreases with AEF, as higher AEF values imply smaller nanopore and MIM device diameters.

For high aspect ratio nanocapacitors the capacitance of each is dominated by the sidewalls, which is proportional to  $1/\ln(b/a)$ , where  $b$  and  $a$  are the outside and inside diameter respectively of the dielectric layer separating the outer conducting layer (bottom electrode) from the inner conducting electrode (top electrode). The ratio of these radii varies as function of active layer thicknesses, consistent with pore diameters, and two generalities can be made.

First, for a given MIM device layer structure, wider pores have a higher capacity per nanocapacitor, thus preferring phosphoric > oxalic > sulfuric. For example, for the larger MIM device within a phosphoric acid template (pore radius,  $R = 160$  nm,  $b = 149.5$  nm and  $a = 141.5$  nm)  $b/a$  is  $\sim 1.05$ . For the same layer structure within an oxalic acid template ( $R = 40$  nm,  $b = 29.5$  nm and  $a = 21.5$  nm)  $b/a$  is  $\sim 1.37$ . Since capacitance is related to the inverse of the  $b$  to  $a$  ratio, the same layer structure in a wider pore ( $R = 160$  nm) yields higher capacitance than in a narrower pore ( $R = 40$  nm). Similarly, the smaller MIM device shows decreasing capacitance per nanocapacitor as the pore diameter narrows.

A second observation from Figure 4.3(b) is that for a given template, thinner bottom electrode ( $t_{be} = R - b$ ) as well as thinner insulators ( $t_{ins} = b - a$ ) provide higher capacitance (assuming the top electrode fills the remaining portion of the pore). Comparing the two device layer structures within an oxalic acid pore ( $R = 40$  nm), the larger MIM device ( $b = 29.5$  nm,  $a = 21.5$  nm,  $b/a \approx 1.37$ ) has a lower capacitance than does the smaller MIM device ( $b = 33$  nm,  $a = 27$  nm,  $b/a \approx 1.22$ ). As in a parallel plate capacitor, decreasing the  $t_{ins}$  increases the device capacitance. However, unlike a parallel plate capacitor, the value of  $t_{be}$  in a porous nanocapacitor influences the capacity since this determines  $b$ . Thus, a thinner bottom electrode shifts  $b$  and  $a$  to larger values, which results in smaller  $b/a$  and higher capacitance.

An important consideration is the design constraint that the MIM device must fit within the pore diameter, which in turn is constrained by the mechanical stability of the AAO template (*e.g.*, as suggested in the guideline that  $D_p \leq 0.8D_{int}$ ). This limits the usable AEF to  $\sim 45$  and  $\sim 57$  for the two examples considered, a feature which is depicted

in Figure 4.3(b) by the vertical bars at these values and the ‘×’ symbols at higher AEF values, indicating that the device is no longer able to fit within the constraints of the template. For the larger MIM device the 51 nm diameter fully fills the pore diameter when  $D_{\text{int}} \sim 64$  nm (at AEF  $\sim 45$ ), while the smaller MIM device’s small diameter (40 nm) enables its use at higher AEF values corresponding to  $D_{\text{int}} \sim 50$  nm (at AEF  $\sim 57$ ).

#### 4.3.2 *Device and Template Optimization*

Given that a very large number of nanocapacitors will be wired together in parallel for use as a storage device, the capacitance per unit planar area is shown in Figure 4.3(c) as the equivalent planar capacitance (EPC). EPC depends on the product of areal density of MIM devices (or nanopores) and the capacitance per device, which respectively increase and decrease with AEF (Figure 4.3(b)). Accordingly the theoretical EPC first increases with AEF, then decreases at higher AEF, as shown by the smooth curves in Figure 4.3(c). For the larger and smaller MIM device examples shown, EPC maxima occur in the range of AEF = 35-50, somewhat before the MIM size constraint (to fit into the nanopore) takes over (again shown by vertical bars and “×” symbols in Figure 4.3(c)). This modeling is validated by experiment, illustrated by an experimental EPC (“measured”) value for an oxalic acid template shown in Figure 4.3(c), in good agreement with the model.

As seen in Figure 4.3(c), the model suggests that, on net, larger EPC’s are achieved with smaller pores and MIM devices within them. Within the suggested design guidelines, sulfuric and oxalic acid templates provide significant EPC gain compared to phosphoric. While the benefit of sulfuric over oxalic is notable, the thinner layers required pose more challenging process control constraints. The maximum EPC for the

larger MIM device occurs near  $D_{\text{int}} = 75$  nm compared to  $D_{\text{int}} = 52.5$  nm for the smaller MIM device. The benefit of moving from the larger MIM device (51 nm dia) to the smaller MIM device (40 nm dia) is greater for oxalic cf. phosphoric templates, increasing EPC by ~60% for oxalic cf. only by ~20% for phosphoric.

These results demonstrate that the realistic imposition of finite-size MIM devices within the nanopore templates adds geometric constraints to the optimization problem. Optimized templates for reaching near-maximum EPC must consider the density of nanocapacitors, their detailed geometric specifications and material properties, and the precision with which the designs can be realized on a massive integration scale.

While thinner active layers are beneficial for increasing EPC, this may introduce limitations on other critical performance metrics. For example, the dielectric must be thick enough to avoid excessive leakage current from Fowler-Nordheim tunneling, direct tunneling, and leakage or low-field breakdown associated with defects. Additionally, the electrode must be thick enough to achieve sufficiently low series resistance. Electrodes that are very thin may have low conductivity,<sup>32</sup> which would increase the RC time constant, limiting the capacitor's ability to rapidly charge and discharge for providing high bursts of power.

For the experimental component of this work, oxalic acid templates were selected as the MIM capacitor platform because these yield substantially higher EPC as compared to planar devices and provide adequate space for depositing adequate MIM layer thicknesses along with a passivation layer. The remainder of this Chapter describes the experimental method of nanoengineering the oxalic acid template topography and the significant effect this has for reducing leakage currents and increasing breakdown fields.

### 4.3.3 *Smoothing Template Nanotopography*

Fabricating a highly uniform, ordered porous AAO template is typically achieved with a two-step anodization process (see Chapter 2).<sup>20</sup> The scalloped texture on the Al surface essential for creating the ordered porous structure during subsequent anodization is shown in Figure 4.4(a). However, the sharp peaks in the Al surface have a small radius of curvature ( $7.8 \pm 0.8$  nm) which directly produce corresponding sharp interpore peak asperities upon growth of the final AAO template during the second anodization step (Figure 4.1).

Before forming the final nanopore AAO template by the normal second anodization, an intermediate electrochemical anodization process was carried out in neutral solution to form a non-porous oxide film, referred to as barrier anodic alumina (BAA). (see Chapter 2.) Figure 4.4(b) shows the results of this intermediate processing step, which transforms the sharp peaks into smoother nanoengineered domes without degrading the ordering of the dimpled texture required for pore ordering during the second anodization. A higher resolution cross-sectional SEM image of this BAA layer on the scalloped Al surface, shown in Figure 4.4(c), indicates the radius of curvature at the top of the BAA layer is significantly increased to  $20.0 \pm 2.5$  nm from  $9.0 \pm 1.2$  nm at the BAA/Al interface, with a BAA film thickness of  $45.0 \pm 3.3$  nm at the dimple minima. Even though the peaks at the BAA-Al interface (Figure 4.4(c)) have a radius of curvature (9.0 nm) only slightly larger than that (7.8 nm) of the peaks on the Al scalloped BAA-free surface (Figure 4.4(a)), the rounded nanotopography (radius of curvature 20.0 nm) of the BAA top surface (Figure 4.4(c)) is retained during subsequent second anodization to form the final AAO nanopore template.



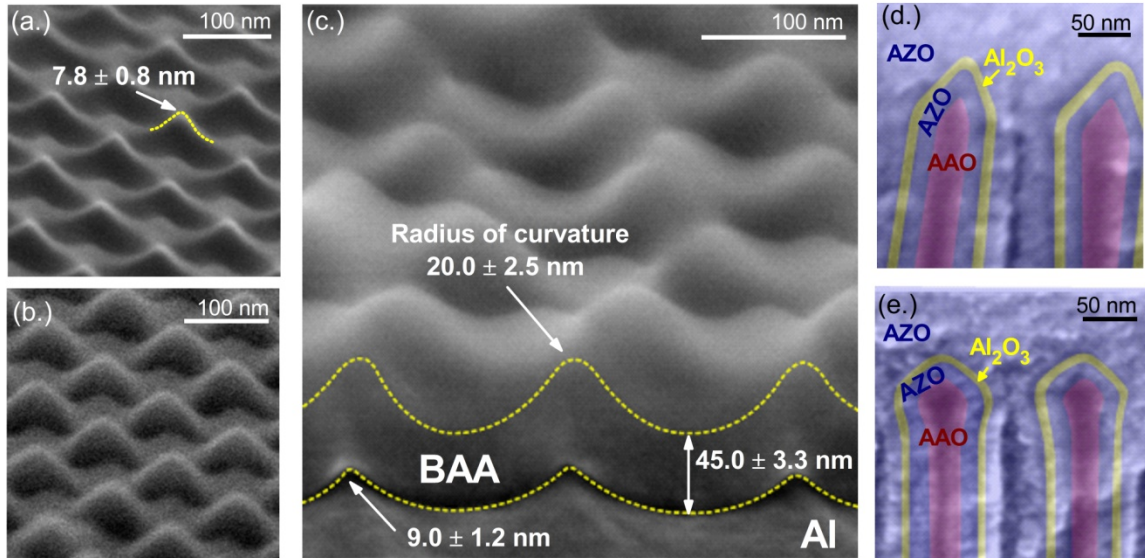


Figure 4.4 (a) SEM image of first anodized Al surface shows scalloped texture. (b) Formation of a BAA layer (40 V) on the first anodized surface smooths scallop asperities. (c) Cross-section of the BAA shows the radius of curvature above and below the BAA layer. (d) Cross-sectional SEM for MIM capacitor fabricated without BAA intermediate step, resulting in sharp inter-pore asperities. (e) SEM for MIM capacitor fabricated with BAA intermediate step, resulting in rounded inter-pore peaks.

Cross-sectional SEM images show MIM nanocapacitors fabricated on an AAO template following a normal two-step anodization process without an intermediate BAA step (Figure 4.4(d)) and with an intermediate BAA step (Figure 4.4(e)). With transparent colors overlaying the SEM cross-section images to guide the eye, it is clear that the curvatures are less sharp at the inter-pore peaks because of the BAA step (Figure 4.4(e)). MIM layers (AZO-Al<sub>2</sub>O<sub>3</sub>-AZO) on the normal two-step anodized BAA-free template appear to be stretching over sharp peak asperities (Figure 4.4(d)), while the MIM layers appear to have much gentler bending when built on a BAA-AAO template (Figure 4.4(e)).

#### 4.3.4 Electrical Consequences of BAA Smoothing Layer

To evaluate resulting electrical properties, MIM layers were deposited within AAO templates with varying BAA voltage and pore depth. Actual thicknesses are very near the targeted thicknesses:  $10.2 \pm 1.0$  nm Al-doped ZnO (AZO) bottom electrode and  $7.3 \pm 0.9$  nm of  $\text{Al}_2\text{O}_3$  insulator. Unlike past work which used TiN as the electrode material,<sup>28</sup> this work used AZO to explore broader conducting layers and to determine if this material system is suitable to transparent optical devices.

Figure 4.5(a) shows representative current-voltage (IV) curves of selected devices. Electrode series resistance was measured with an additional IV sweep after catastrophic failure that caused shorting of the MIM capacitors. Reported electric fields have been adjusted to compensate for series resistance in order to accurately determine the actual breakdown fields and leakage currents. Even though AZO film resistivity is low as measured in planar thin films,<sup>118</sup> it was expected the thin-film 3D nanoelectrodes would introduce consequential resistance ( $\sim 10$  k $\Omega$ ). These measured values are in good agreement with the expected resistance of thin-film AZO.

The nanoengineered templates show dramatic electrical performance improvements. Devices on the BAA-free 1.5  $\mu\text{m}$  thick AAO (representative sample shown in Figure 4.5(a)) has very high leakage current densities at low fields ( $>10^{-4}$  A/cm<sup>2</sup>). Devices built on nanoengineered templates using the BAA smoothing step, including 1  $\mu\text{m}$  thick AAO with BAA formed at 40 V, and 1.5  $\mu\text{m}$  thick AAO with BAA formed at 10, 20, 30, and 40 V (referred to in text as 40BAA-1 $\mu\text{m}$ , 10BAA-1.5 $\mu\text{m}$ , 20BAA-1.5 $\mu\text{m}$ , 30BAA-1.5 $\mu\text{m}$  and 40BAA-1.5 $\mu\text{m}$ , respectively), all showed similar dramatic reduction of leakage current, illustrated by the 40BAA-1 $\mu\text{m}$  and 30BAA-1.5 $\mu\text{m}$

IV curves in Figure 4.5(a). Leakage currents are reduced by  $10^5\times$  for all templates by a BAA intermediate processing step. At 1 MV/cm field, leakage currents are on the order of  $10^{-9}$  A/cm<sup>2</sup>. Increasing AAO template thickness from 1  $\mu\text{m}$  to 1.5  $\mu\text{m}$  did not change leakage currents.

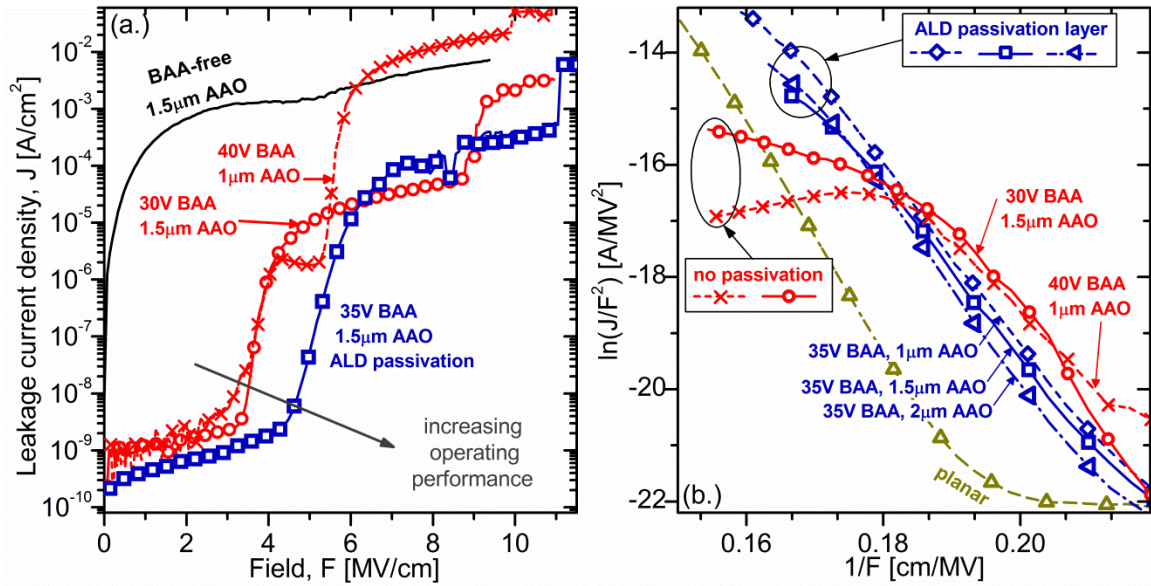


Figure 4.5 (a) Representative IV curves for AZO-Al<sub>2</sub>O<sub>3</sub>-AZO capacitors fabricated in AAO templates showing influence of BAA smoothing layer and ALD TiN passivation layer. (b) Linear segment indicate FN tunneling regime, which occurs for wider ranges and higher fields with the introduction of an ALD TiN passivation layer.

Additionally, significant increases in breakdown fields were observed from nanoengineered templates that included the BAA layer, including breakdown fields of  $9.0 \pm 1.4$  MV/cm for 10BAA-1.5 $\mu\text{m}$ ,  $9.6 \pm 0.8$  MV/cm for 20BAA-1.5 $\mu\text{m}$ ,  $9.5 \pm 0.8$  MV/cm for 30BAA-1.5 $\mu\text{m}$ , and  $9.5 \pm 0.7$  MV/cm for 40BAA-1.5 $\mu\text{m}$ . Breakdown fields for 40BAA-1 $\mu\text{m}$  ( $9.5 \pm 1.5$  MV/cm) are nearly identical to 40BAA-1.5 $\mu\text{m}$ , indicating breakdown fields are also independent of AAO thickness.

These results demonstrate major improvements in leakage current and breakdown field due to the BAA smoothing layer. The improved breakdown characteristics are

attributed to the rounding of the interpore asperities inherent in AAO templating and the lower leakage current to the lower fields present (hence lower Fowler-Nordheim currents at asperities).

#### 4.3.5 ALD Passivation Layers to Suppress Impurity Diffusion

Electrical performance was further improved by introducing a thin titanium nitride (TiN) ALD passivation layer prior to MIM layer deposition.<sup>63,64</sup> All samples with a passivation layer were fabricated using AAO thicknesses of 1, 1.5 and 2  $\mu\text{m}$  with BAA formed at 35 V (referred to as 35BAA-1 $\mu\text{m}$ -p, 35BAA-1.5 $\mu\text{m}$ -p and 35BAA-2 $\mu\text{m}$ -p in the text, respectively). Of the samples with a passivation layer, for clarity only 35BAA-1.5 $\mu\text{m}$ -p is shown on Figure 4.5(a). Low-field leakage current densities at 1 MV/cm were substantially further reduced from about  $1.13 \times 10^{-9}$  A/cm<sup>2</sup> to  $4.7 \times 10^{-10}$  A/cm<sup>2</sup> for 35BAA-1 $\mu\text{m}$ -p,  $4.6 \times 10^{-10}$  A/cm<sup>2</sup> for 35BAA-1.5 $\mu\text{m}$ -p, and  $4.3 \times 10^{-10}$  A/cm<sup>2</sup> for 35BAA-2 $\mu\text{m}$ -p. In addition, breakdown fields were also further increased to  $10.2 \pm 1.5$  MV/cm for 35BAA-1 $\mu\text{m}$ -p, 35BAA-1.5 $\mu\text{m}$ -p, and 35BAA-2 $\mu\text{m}$ -p. More importantly, these fields are well within the range of theoretical and experimental breakdown fields of Al<sub>2</sub>O<sub>3</sub>.<sup>17,124,125</sup> These results suggest that the passivation layer suppresses diffusion of impurities from the AAO surface into the MIM device, improving leakage current and breakdown field, and confirming that 3D nanotemplates, initially intended to increase capacitance densities, have been effectively nanoengineered to meet critical electrical performance metrics. The nanoengineered template no longer introduces an intrinsic mechanism for low-field catastrophic failure, and allows significantly higher operating electric fields (near the strength of the insulator) to be used, with accompanying benefit to energy density  $\frac{1}{2}CV^2$ .

Leakage currents in MIM structures are typically dominated by electron tunneling over a barrier, *i.e.* Fowler-Nordheim (FN) tunneling. (see Chapter 1.) FN analysis of current-voltage behavior is shown in Figure 4.5(b) for AZO-Al<sub>2</sub>O<sub>3</sub>-AZO MIM nanocapacitor devices with BAA layers and ALD TiN passivation, in comparison to corresponding planar MIM on a SiO<sub>2</sub> wafer. These curves exhibit a classic FN-tunneling regime governed by  $J = AF^2 \exp(B/F)$ , where  $J$  is the leakage current density,  $F$  is the applied field, and  $A$  and  $B$  are constants.<sup>126</sup> The linear region indicates the regime where FN-tunneling dominates charge transport across the capacitor dielectric. 40BAA-1 $\mu$ m and 30BAA-1 $\mu$ m display FN tunneling over a narrow range, 0.20 to 0.22 cm/MV in Figure 4.5(b), from which a barrier height of  $\sim$ 1.3-1.4 eV is derived. 35BAA-1 $\mu$ m-p, 35BAA-1.5 $\mu$ m-p, and 35BAA-2 $\mu$ m-p, and the planar device show characteristic FN-tunneling over a broader range in Figure 4.5(b), 0.16-0.21 cm/MV and an increased barrier height of  $\sim$ 1.8 eV.

Unexpected IV behavior is observed for 40BAA-1 $\mu$ m between  $\sim$ 4 and 6 MV/cm in Figure 4.5(a), where the slope is no longer positive, suggesting negative resistance. Although the representative IV curve for 30BAA-1.5 $\mu$ m does not display uncharacteristic behavior, many devices on this sample (and on many devices on 10BAA-1.5 $\mu$ m, 20BAA-1.5 $\mu$ m, and 40BAA-1.5 $\mu$ m samples), showed uncharacteristic behavior in this range. One possible explanation is that these templates involve a dominating, counter-acting leakage mechanism to conventional FN tunneling, which could result from foreign ionic species as impurities. During anodization for oxide formation, electrolytic solutions dissociate, negatively charged ions move towards the oxide-Al interface, and positively charged ions move towards the oxide-electrolyte interface, both likely remaining trapped

in the oxide membrane.<sup>127-129</sup> Under an electric field, these ions could become mobile and enter active layers, possibly causing this anomalous behavior. The introduction of a TiN passivation layer, like the Al<sub>2</sub>O<sub>3</sub> example noted previously,<sup>28,29</sup> seems to diminish or eliminate the uncharacteristic behavior, suggesting the role of these layers as diffusion barriers that prevent migration of impurities from the AAO material into the nanodevice.

Capacitance measurements of all devices were in good agreement with the theoretical estimates provided by the geometrical calculations. The EPC of  $11.6 \pm 0.5 \mu\text{F}/\text{cm}^2$  for 35BAA-1 $\mu\text{m}$ -p,  $20.6 \pm 0.4 \mu\text{F}/\text{cm}^2$  for 35BAA-1.5 $\mu\text{m}$ -p, and  $26.2 \pm 1.5 \mu\text{F}/\text{cm}^2$  for 35BAA-2 $\mu\text{m}$ -p scales with increasing AAO template thickness (or pore depth). Comparing these EPC values with those reported by Banerjee *et al.* for thicker AAO templates,<sup>28</sup> a ~20% increase in EPC per unit AAO thickness can be projected. The IV curves (Figure 4.5(a)) show that nanotopography smoothing of interpore peak asperities by BAA-AAO is highly effective for nanoengineering the topography and increasing energy density. This BAA-AAO technique combined with a thin 4 nm TiN passivation layer (compared to thicker, 15 nm of Al<sub>2</sub>O<sub>3</sub><sup>28</sup>), adds to the performance improvement by providing more space within the template, and resulting in larger AEF and EPC (refer to Figure 4.3). As a result, projecting the EPC for devices fabricated on thicker AAO templates, significantly higher EPC should be attainable with greater AAO thicknesses.

#### 4.4 Discussion

The results described above illustrate the importance of detailed nanoengineering of energy storage nanostructures, and the challenges involved. Taken together, the 20%

increase in EPC per unit AAO thickness and  $2.5\times$  improvement in breakdown field ( $6.25\times$  increase in energy density  $\frac{1}{2} CV^2$ ) suggest a total areal energy density increase by a factor of  $7.5\times$ . As compared to Banerjee *et al.*,<sup>28</sup> the devices characterized in this work had a much thinner passivation layer, which resulted in greater values of  $b$  and  $a$ . Assuming material densities of  $5.62 \text{ g/cm}^3$  for ZnO,<sup>69</sup>  $3.0 \text{ g/cm}^3$  for  $\text{Al}_2\text{O}_3$ ,<sup>66</sup> and  $3.0 \text{ g/cm}^3$  for TiN,<sup>130 4</sup> the active material mass per nanocapacitor is increased by a factor of about  $3.7\times$ . Therefore, the experimental parameters used here result in larger mass, reducing the energy density increase expected from  $7.5\times$  to about  $2\times$ . Nevertheless this represents a significant increase in energy density from  $0.7 \text{ Wh/kg}$  in previous work<sup>28</sup> to  $1.5 \text{ Wh/kg}$ .

Further improvements in electrostatic nanocapacitor performance can be foreseen. Some of these reside in the materials aspects of the design. The use of high- $\kappa$  dielectrics (cf.  $\text{Al}_2\text{O}_3$ ) offers benefits in energy storage density (linear in  $\kappa$ ), but can encounter problems with leakage current and breakdown field.<sup>17</sup> Engineered nanomaterials can address some of these challenges, *e.g.* by introducing Al dopant into high- $\kappa$  ALD  $\text{TiO}_2$ .<sup>110</sup> Lower resistivity, ultrathin electrodes can be achieved by ALD, illustrated by the example of Ru,<sup>65</sup> which has potential to reduce series resistance by  $\sim 10^3\times$  compared to the AZO employed here. (see Chapter 1.)

Another source of opportunity lies in modeling and optimization of the MIM structure itself for electrical performance. While the examples considered in Figure 4.3 assumed a specific set of layer thicknesses, these parameters may be varied and optimized as well, leading to a broader picture than Figure 4.3. The geometry as well as the resistivity of the metal electrodes will affect power capability of the electrostatic

nanocapacitor, functioning as a distributed resistance network whose power handling capability is improved by thicker, shorter nanoelectrodes. If higher  $\kappa$  dielectrics are employed, or larger area enhancement factor geometries used, leakage currents will likely increase, degrading the retention time during which the energy is stored for transfer to other circuitry.

#### 4.5 Conclusion

Detailed nanoengineering of AAO-ALD electrostatic MIM nanocapacitors has enabled significant performance improvements. By electrochemically shaping and smoothing AAO nanotopography using an intermediate BAA smoothing layer, breakdown fields for MIM layers over this topography have increased by 2.5 $\times$ , from about 4 MV/cm to about 10 MV/cm (approaching intrinsic dielectric strength of the  $\text{Al}_2\text{O}_3$  insulator), with benefit to energy density that scales with  $V^2$ . In general, devices based on self-assembly techniques are likely to offer a more affordable solution, but without nanoengineering techniques, like BAA, the notion of replacing traditional expensive templating techniques would not be feasible, since cost is not necessarily an equal tradeoff to performance. AAO template nanoengineering combined with a thin metallic material is as effective at passivating ions as a thick dielectric material used by Banerjee *et al.*<sup>28</sup> An ultrathin TiN passivation layer under the MIM structure reduces leakage current densities to the  $10^{-10}$  A/cm<sup>2</sup> range, serving as a diffusion barrier to prevent impurities from the AAO material entering the active MIM structure. Modeling and optimization of the template geometry increases capacitance density by 20% due to more efficient utilization of nanopore volume. As a result of these improvements,



expected energy densities are 1.5 Wh/kg. This work also illustrated the numerous factors of device design, materials choice, process engineering, and multi-parameter optimization that critically influence achievable performance of such energy storage nanostructures.

## Chapter 5: Hybrid Circuits to Exploit Electrostatic and Electrochemical Energy Storage Nanostructures

### 5.1 Abstract

Time-varying energy profiles of renewable sources, electric vehicles, end user demands, and grid fluctuations require high power as well as energy density in storage systems. Nanostructured storage devices present new opportunities, including batteries, electrochemical capacitors (ECC's), and recently electrostatic capacitors (ESC's) with profiles ranging from high energy/low power to its inverse. Hybrid circuits have previously been considered to combine batteries and electrochemical supercapacitors. This Chapter discussed a hybrid simulation model combining ESC and ECC devices, based on experimental response surface models for corresponding nanostructured devices and including the distinctly different nonlinearity mechanisms in each. Results suggest that power-energy combinations can be enhanced by the contrasting yet synergistic mechanisms by which ESC and ECC operate. While design tradeoffs exist between total energy captured and the efficiency of such capture/storage, the addition of ESC enables faster charging rates and better use of power transients as needed for power leveling applications across the domains of electrical energy storage.

## 5.2 Introduction

The trend towards incorporating renewable sources of energy into the power grid has stimulated much interest in the development of efficient, affordable and compact energy storage devices.<sup>2,131</sup> Renewables like wind and solar energy have dramatically time-variant profiles where fluctuations in the amount of energy available and harvested depends on many conditions, including time of day, weather conditions, and time of year.<sup>132</sup> Moreover, grid and transportation applications also have correspondingly dynamic profiles.<sup>133</sup> To effectively use the energy available, energy storage solutions are needed which efficiently capture, store and distribute the electrical energy until needed by the end-user. Therefore, energy storage devices should be capable of holding large amounts of energy (high energy density) and have the ability to respond quickly, *i.e.*, capture energy as generated and quickly distribute energy as needed (high power density).

### 5.2.1 Trade-off between energy density and power density

Engineering a single energy storage device with both high energy density and high power density is a major challenge, since the charge transfer and storage mechanisms in traditional energy storage devices vary from one device category to the other (see Chapter 1). Electrochemical capacitors have higher cyclability as well as rates than do batteries because the ions do not change the chemical structure of the material.<sup>134,135</sup> These characteristics have made electrochemical capacitors suitable for many applications such as electric vehicles<sup>5,136,137</sup> and metro trains,<sup>134,138</sup> regenerative braking,<sup>135,138-140</sup> emergency door opening,<sup>134</sup> cordless power tools,<sup>134,141,142</sup> and back-up memory.<sup>5,138,142</sup> While electrochemical capacitors are gaining popularity, their cost

versus energy performance and operating requirements sets them back from their competitors.<sup>138</sup> The voltage window is limited by the electrolyte electrochemical stability (1 - 3 V),<sup>134,141</sup> placing limits on energy density ( $E \sim V^2$ ) as well.

### 5.2.2 *Opportunities and limitations of nanostructures*

Significant research has focused on nanostructured nano-energy storage devices for achieving greater performance improvements over conventional storage technologies because the reduced dimensions provide higher surface areas and have the potential to improve efficiencies.<sup>9</sup> (see Chapter 1) For example, replacing the solid material in an electrochemical capacitor (ECC) with a highly porous material increases the available surface area significantly. The improvement in charge storage is so large that these devices are often referred to as supercapacitors.<sup>4,143</sup>

Electrostatic capacitors (ESC's) at the nanoscale are of interest because the advantage of ESC's is that their power levels are substantially higher than those of ECC's and batteries.<sup>144-149</sup> (see Chapter 1). With nanostructuring to dramatically increase surface area, the ESC's present very high power capability at low energy density, complementing the characteristics of electrochemical devices (ECC's and batteries) but opening the question of how best to exploit ESC's in an electrical energy storage system that delivers both high power and high energy. Specific challenges in this effort include how best to use the higher voltage capability of the ESC c.f. ECC, and how to manage the short charge retention time of the ESC caused by dielectric leakage.

Prior work has identified and addressed the use of hybrid electrical storage circuits comprised of electrochemical devices, particularly batteries (for high energy) and electrochemical supercapacitors (for high power).<sup>150-162</sup> Physical and electrochemical

mechanisms involved in their charge/discharge operation are similar for these devices; indeed, the demarcation between supercapacitors and batteries can be vague.

In this Chapter hybrid circuit configurations are considered which combine ESC's to achieve exceptionally high power along with ECC's to obtain reasonably high energy. A simple simulation model has been developed for the hybrid ESC-ECC circuit employing response surface models for their individual behavior that are extracted from experimental data for nanostructured ESC's<sup>149</sup> and ECC's<sup>163</sup>. The completely different mechanisms involved in ESC vs. ECC operation provide a challenge in itself – different voltage windows, charge retention, charge storage species, and nonlinearities associated tunneling, breakdown, and cycling. Results indicate the contrasting yet complementary ESC and ECC storage mechanisms can be combined to advantage in a hybrid system, with a variety of tradeoffs to be made in system design. By actively switching connections between source, ESC, ECC and load, charge captured on the ESC can be efficiently transferred to the ECC for longer term retention. The intrinsic leakage of the ESC, at first glance a disadvantage, also means that the front-end ESC device is typically discharged at the next voltage pulse to arrive, making it ready to accept a full charge on that pulse – a significant advantage.

### 5.3 Devices overview

#### 5.3.1 *Electrostatic capacitors (ESC)*

Nanotechnology has opened the door to dramatic increases in surface area for electrostatic capacitors (ESC's), leading to significantly increased (up to ~1-200X) capacitance per unit planar area.<sup>7,22,28,149,164</sup> (see Chapter 1.) Furthermore, because they

store strictly electronic charge on conducting surfaces, ESC's have exceptional power handling capability, far better than that of electrochemical storage devices (supercapacitors or batteries). Nanosynthesis practice has enabled such parallel arrays of nanocapacitors to perform effectively as ESC's, an accomplishment in itself.<sup>28,149</sup> Here a single ESC device is used as a simple representation of the actual devices, since it reflects the fundamental behavior, challenges, and nonlinearities, which are all qualitatively different from those of electrochemical devices as described below.

Figure 5.1(a) shows a single ESC used to capture energy from a source, then store and finally transfer it to an external load. While in principle its capacitance  $C_{\text{ESC}}$  is linear ( $Q = C_{\text{ESC}} V$ , with  $Q$  charge and  $V$  voltage), in practice its behavior is nonlinear, as depicted in Fig. 5.1(b). Direct and Fowler-Nordheim tunneling dramatically change the leakage current as a function of applied electric field, while high field breakdown sets in at even higher field to limit the working field and voltage range of the device. Figure 5.1(b) (top) shows a representative current-voltage curve reported by Haspert *et al.* for a device having an insulator thickness of  $\sim 7.2$  nm.<sup>149</sup> (see Chapter 4.) Low applied voltages ( $V_{\text{in}} \leq 4$  V) produce minimal leakage current by direct tunneling. Higher voltages ( $V_{\text{in}} > 4$  V) cause a rapid increase in leakage current associated with Fowler-Nordheim tunneling, i.e. field-enhanced tunneling over a barrier. At still higher  $V_{\text{in}}$  ( $\sim 8$  V) catastrophic breakdown of the device occurs, as shown by the jump in leakage current. Figure 5.1(b) (bottom) shows the corresponding electrical resistance ( $R_{\text{ESC}}$ ) across the insulator layer as a function of  $V_{\text{in}}$ . Fowler-Nordheim tunneling at  $V_{\text{in}} > 4$  V produces a substantial decrease in  $R_{\text{ESC}}$ , followed by a sharp drop in  $R_{\text{ESC}}$  at  $\sim 8$  V corresponding to breakdown.

The voltage at which these mechanisms occur is dependent on the insulator thickness so that it is common to report leakage currents as a function of electric field (top axis in Fig. 5.1(b)). Therefore, these leakage mechanisms are expected to occur at the same fields for an insulator twice as thick, but the corresponding voltages should be  $2\times$  higher. Energy storage in an ESC scales as  $E = \frac{1}{2} CV^2$ . Since  $C = \epsilon A/d$  (with  $\epsilon =$  insulator dielectric constant,  $A =$  ESC area, and  $d =$  insulator thickness), energy density depends on  $AV^2/d$ . While this suggests energy density benefits for constant field achieved at higher voltages and insulator thicknesses, nanostructured designs deliver high surface areas  $A$  per unit volume that ultimately weighs in favor of such designs even though dimensions for the MIM layers are constrained by nanopore dimensions.

Leakage currents in the thin insulator layers in the MIM ESC structure are represented by a nonlinear internal resistance  $R_{ESC}$  in Fig. 5.1(a), which causes self-discharge of the voltage and charge on the ESC even without connection to an external load  $R_{load}$ . The high power of the ESC derives from the configuration in which a modest series resistance ( $R_{series}$  in Fig. 5.1(a)) enables ultrafast charge transfer onto the ESC. While this makes the ESC ideal for capturing high power bursts, the retention times are much too short to retain essentially all of the charge on the ESC for use later. As shown in Fig. 5.1(c) at time  $t_2$ , after charging  $V_{ESC}$  decays quickly when the applied input voltage  $V_{in}$  is removed.  $V_{ESC}$  then stabilizes and decreases much more slowly when it reaches lower values where leakage currents are far smaller and leakage resistance much higher (Fig. 5.1b). Details of the simulations shown are given below.

Where ESC's are used to store information as charge on DRAM capacitors, a similar self-discharge occurs. In this memory application, the information is refreshed by

active circuitry faster than the low retention time of the ESC, but this is of course unworkable in energy storage applications. A different solution to the short retention time is needed. This challenge, together with the opportunity posed by the very high power capability of the ESC, motivates the present study of hybrid circuits involving electrostatic and electrochemical capacitors (ECC's) which may capture charge in sharp transients or voltage spikes and rapidly transfer it to electrochemical devices for longer-term storage. The reverse behavior of the hybrid circuit would apply to delivering high power levels for short bursts of demand.

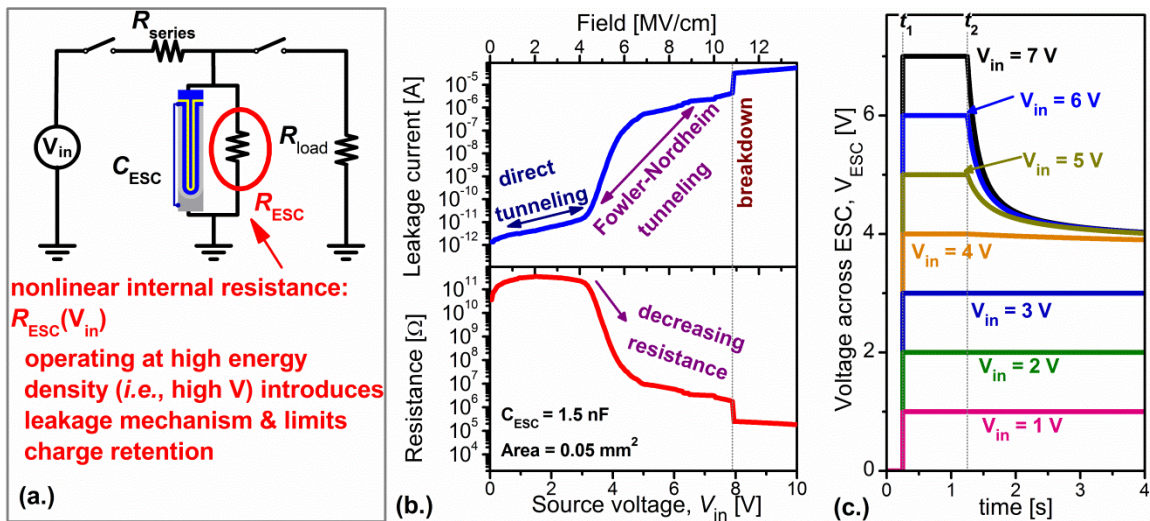


Figure 5.1 **Electrostatic capacitor (ESC)**. (a) ESC as stand-alone device for supplying power/energy to an external load ( $R_{load}$ ) is not ideal for storing large amounts of energy for significant time. (b) Nonlinear leakage current as a function of  $V_{in}$  due to various leakage mechanisms (top). Leakage is low with  $V_{in} \leq 4$  V but rises  $> 4$  V. The sharp rise in current ( $\sim 8$  V) indicates catastrophic breakdown. Nonlinear resistance as a function of  $V_{in}$  shows drop in resistance  $> 4$  V (bottom). (c) After  $t_2$ , the voltage across the capacitor,  $V_{ESC}$ , for  $V_{in} = 5-7$  V drops rapidly until  $V_{ESC}$  drops to  $\sim 4$  V, where the discharge rate,  $R_{ESC}C_{ESC}$ , becomes much slower as the internal resistance is larger. ( $R_{ESC}C_{ESC}$  for  $V_{in} = 5-7$  V is very fast then very slow.)

### 5.3.2 Electrochemical capacitor (ECC)

Electrochemical capacitors store charge as ions both in the electrical double layer which forms at electrode/electrolyte interfaces and as Faradic charge within the electrodes. Ion transport through the electrolyte between electrodes is accompanied by



electron transport through the external circuit, thus storing or delivering electrical energy and power. Slower transport of ions translates to higher energy storage capability, longer charge retention times, and lower power handling capability for ECC's in comparison to ESC's. Material, chemical, and structural changes which accompany ion transport produce significant hysteresis in current-voltage response of ECC's, accompanied by drifts in properties with charge cycling and limited voltage regimes within which electrolytes are sufficiently stable. Clearly these ECC phenomena differ profoundly - qualitatively and quantitatively - from the behavior of ESC's.

As a representative ECC the poly(3,4-ethylenedioxythiophene) (referred to as PEDOT) nanotube structure is considered.<sup>163</sup> The base of a highly porous anodic aluminum oxide (AAO) template is coated with gold and PEDOT is electrochemically deposited within the AAO pores. The AAO template is then dissolved away, leaving a dense array of high aspect ratio PEDOT nanotubular structures.

Figure 5.2(a) shows a simple circuit for using an ECC to capture energy from a source, then store and finally transfer it to an external load. The schematic represents a symmetric single nanotubular electrochemical capacitor, adapted from Liu *et al.*,<sup>163</sup> where the regions colored white outlined by a broken line represent the sacrificial AAO pore sidewalls, blue represents the PEDOT, and yellow represents the base gold contact. Here, open-circuit charge dissipation resistance ( $R_{ECC}$ ) is assumed to be significantly high, like an ideal capacitor, so that the charge stored across the ECC is stable over time,<sup>136,139</sup> especially compared to the behavior of the ESC described above. However, the capacitance  $C_{ECC}$  is inversely proportional to scan rate, or change in potential with time, since at fast scan rates not all the ionic charge can move fast enough to contribute to

the capacitance. Figure 5.2(b) shows cyclic voltammograms simulated by the MatLab/Simulink ECC model component with parameters adjusted to nearly replicate the experimental data reported by Liu *et al.*<sup>163</sup> From this data, it is possible to determine the capacitance of single device (relationship shown in lower right corner of Fig. 5.2(b)). Figure 5.2(c) shows that the capacitance decreases nonlinearly with increasing scan rate, behavior qualitatively different from that of the ESC. Slower scan rates provide higher capacitances because the kinetics of charge transport accommodates a larger fraction of available charge. The maximum specific capacitance reported was calculated using the 50 mV/s scan rate.<sup>163</sup> For a single electrode with an electrode mass,  $m_{\text{electrode}}$ , of  $5.72 \times 10^{-2}$  mg, this which provides a specific capacitance of  $\sim 140$  F/g and translates into a maximum capacitance of  $\sim 4$  mF for a symmetric capacitor device.<sup>163</sup>

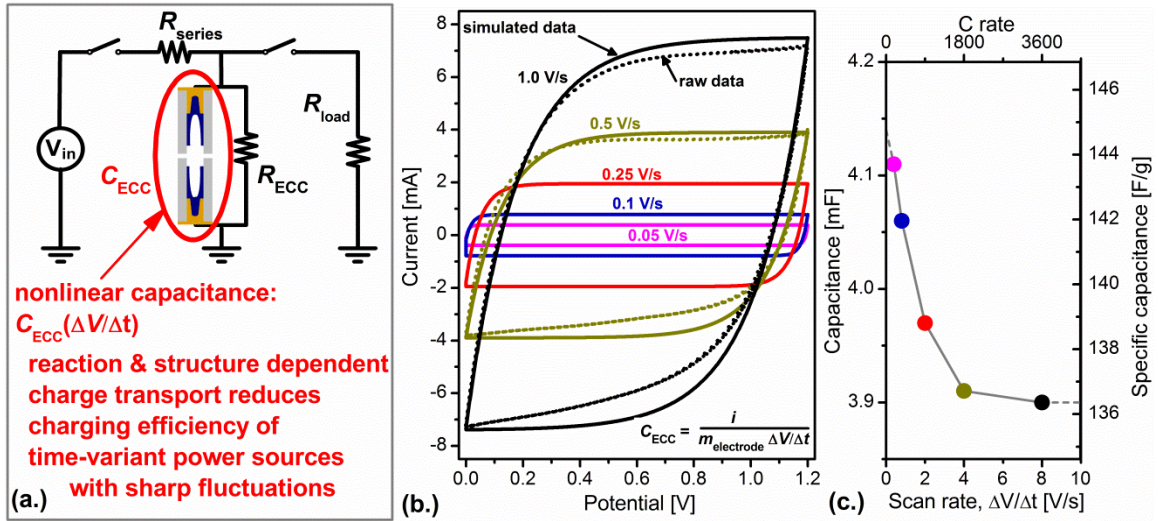


Figure 5.2 Electrochemical capacitor (ECC) (a) ECC as stand-alone device for supplying power to an external load ( $R_{\text{load}}$ ) is not ideal when time-varying power sources, e.g., step-wave power sources drop ECC charging efficiency to 93% (capacitance at infinite rise in potential assumed to be 7.68 mF.) (b) Simulated cyclic voltammograms of one electrode ECC (top) from which the capacitance can be calculated, where  $\Delta V/\Delta t$  is the scan rate,  $i$  is the current, and  $m_e$  is the mass. Dotted lines show raw data for 1 V/s and 0.5 V/s. (c) The capacitance (left) and specific capacitance (right,  $m_{\text{electrode}} = 5.72 \times 10^{-2}$  mg) as a function of the  $\Delta V/\Delta t$  for a symmetric capacitor shows ECC has higher capacity with slower  $\Delta V/\Delta t$ .

Using the ECC device alone is not ideal in scenarios with abrupt time-variant power sources and loads because of its limited power handling capability (c.f. ESC). Furthermore, the electrochemistry of the electrolyte limits the voltage range through which the system can be cycled. Both these limitations may be countered by a hybrid configuration of ECC with high power ESC, investigated and described below.

### 5.3.3 *Creating a hybrid system*

The incorporation of different storage devices into a hybrid system has been considered previously, particularly combining supercapacitors and batteries for the high power of the former and high energy density of the latter.<sup>154,158</sup> In these cases the mechanisms of ion and electron charge transport are rather similar, leading to parallel questions of ion diffusion rates in the storage materials, voltage stability range of the electrolyte, etc. Advances in electrostatic capacitors (ESC's), described above, pose analogous motivation for a hybrid system, in this case integrating ESC and ECC (or potentially, battery) into a hybrid circuit configuration.

The challenge is addressed here through a dynamic MatLab/Simulink model for the hybrid circuit configuration. The ESC-ECC hybrid differs from previous work on supercapacitor-battery hybrids in that – as emphasized above – the physical and electrochemical mechanisms by which the two device types operate are very different, accompanied by contrasts in usable voltage range, vastly different charge retention times, and differing materials sets. The primary goal of this study is to see how the ESC's high power capability can be exploited for power leveling of fast power excursions from renewable sources (e.g., solar, wind) and power demand surges (e.g., electric vehicle acceleration/deceleration), using hybrid configurations to compensate for short retention

times of ESC's and to balance voltage and charge storage between ESC and ECC components of the system.

The dynamic model developed here utilizes step-function voltage sources at the input to the ESC, programmable switches to connect/disconnect both ESC and ECC devices to each other and to input source and load, and the inherent nonlinearities of both ESC and ECC devices. Hybrid configurations are considered with varying total capacity of ESC vs ECC components, various parameters for each type of device, and timing considerations for switching connections. The object is to capture on the ESC as much of an input power burst as possible, then transfer that charge to the ECC components, and finally to be able to deliver that charge at high power to a load by reversing the pathway. Besides these optimization issues a key constraint is that efficiency requires that the rate of ESC discharge must be faster than the rate in which the ESC would self-discharge if it stored the charge directly.

The dynamic MatLab/Simulink model uses behavior of ESC and ECC storage nanodevices built and experimentally measured to connect with the growing interest and opportunities in nanostructures for electrical energy storage. Nevertheless the concepts and trends are general for ESC-ECC hybrids, and could be extended to more complex hybrid systems. Furthermore the results should be relevant whether the hybrid system is comprised of discrete devices wired into a circuit, or alternatively nanostructured device arrays that may even be integrated ESC-ECC combinations at the micro or nano aggregation level.

## 5.4 Modeling dynamic behavior

Using MatLab/Simulink to simulate the dynamic charge transfer processes, a basic circuit in which switches transfer charge from an input voltage to an ESC, and subsequently that charge is transferred from the ESC to an ECC, as depicted in Fig. 5.3(a) through three stages – capture, transfer, and store. At this stage the behavior of the two devices are linear and set the capacitance ratio  $CR = C_{ECC} / C_{ESC} = 10$ , since it will turn out that circuit optimization requires larger  $C_{ECC}$  than  $C_{ESC}$ . Since leakage resistance of the ESC is a major motivation for the hybrid circuit configuration, substantially different values of  $R_{ESC}$  are considered, either 10 k $\Omega$  or 0.01 k $\Omega$ , while  $R_{ECC}$  is kept at 10 k $\Omega$ . At time,  $t$ , equal to  $t_0$ , the circuit is initially at steady-state so that  $V_{ESC} = V_{ECC} = 0$ .

Charge capture begins at  $t_1$  when the first switch S1 closes, which allows charge to build up on  $C_{ESC}$ . Figure 5.3(b) (left) shows the rise in voltage and saturation at the value of  $V_{in}$  across  $C_{ESC}$ , indicating that the capacitor is fully charged and that the amount of charge,  $Q_{ESC}(\text{capture})$ , should be equal to  $C_{ESC} \times V_{in}$ . For  $R_{ESC} = 10 \text{ k}\Omega$   $V_{ESC}$  rapidly reaches the full input voltage  $V_{in} = 4 \text{ V}$ , since  $R_{series}$  is negligible ( $R_{series} = 1 \Omega$ ). However, for  $R_{ESC} = 0.01 \text{ k}\Omega$ ,  $V_{ESC} < V_{in}$  since the lower leakage resistance prevents complete charging of the capacitor, forming a voltage divider for  $V_{in}$  with  $R_{series}$ . This also accounts for the notable current through the ESC during the charge capture phase, as seen in Figure 5.3(c) (left) for  $R_{ESC} = 0.01 \text{ k}\Omega$ . This leakage of charge, is clearly wasted energy that should be minimized in an energy storage system, hence the motivation for the present study.

In the transfer phase, the input source is disconnected from the ESC, and the ESC is connected to the ECC to transfer its charge there, the negative ESC current producing a

positive ECC current. Since the two devices are electrically connected in this phase, their voltages must become equal, and so finite charge remains on both devices, determined by their relative capacitance values. The remaining charge on the ESC is thus not transferred, and is subject to degradation associated with the leakage resistance  $R_{\text{ESC}}$ . This is reflected in the decrease in ESC voltage with time during the transfer and store phases in Fig. 5.3(b) (left) for low  $R_{\text{ESC}}$ , and also in the decrease in ECC voltage during the transfer phase. The ECC voltage remains constant in the store phase since it is disconnected from the ESC and thus unaffected by ESC leakage current, while ECC leakage is much smaller.

In addition to these simple considerations about the dynamics of a hybrid combination of linear ESC and ECC devices, the physical and electrochemical mechanisms that account for nonlinearities described above must be accommodated into a model, for these play a significant role in overall system behavior and dynamics. Prime factors include voltage-dependent ESC leakage, ESC dielectric breakdown threshold, ECC hysteresis and again, and electrolyte stability limits for ECC cycling.

The input voltage profile was constructed as a square wave using a DC source (1-7.5V) modulated by simulation-controlled switches (whose energy cost are assumed negligible for this analysis). The ESC capacitance  $C_{\text{ESC}}$  is fixed, while its leakage current is determined as a function of  $V_{\text{ESC}}$  by using an experimentally determined look-up table. For the ECC component, a lookup table determines the  $C_{\text{ECC}}$  (output) as a function of  $V_{\text{ECC}}$  and its rate of change, using experimental data based on a symmetric capacitor with maximum capacity  $\sim 4$  mF. As in the previous example, the time-dependent behavior of

the system through capture, transfer, and store phases, is analyzed but now including the nonlinearities of the ESC and ECC devices.

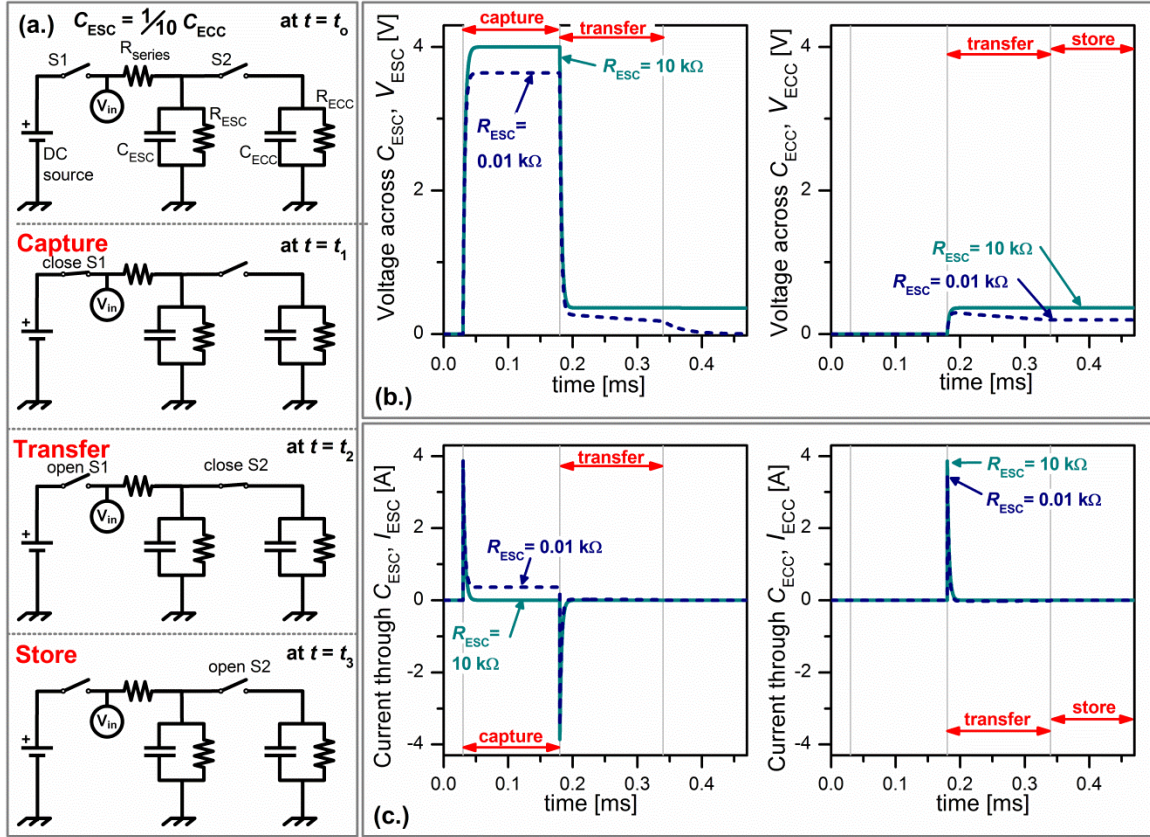


Figure 5.3 **Simple hybrid ESC-ECC circuit operation (linear devices)**. (a) Circuit design of two capacitors with switching scheme and time (top to bottom) shown.  $R_{ECC}$  remains relatively large while  $R_{ESC}$  is either  $10 \text{ k}\Omega$  (solid) or  $0.01 \text{ k}\Omega$  (dashed). (b) The voltage across  $C_{ESC}$  (left) and voltage across  $C_{ECC}$  (right) during transfer and store stages ( $V_{in} = 4 \text{ V}$ ). The potentials at from  $t \approx 0.2 \text{ ms}$  to  $t_3$  are equal ( $V_{eq}$ ) and its value largely depends on the ratio of  $C_{ESC}$  to  $C_{ECC}$ . Reducing  $R_{ESC}$  results reduces voltage across ESC during capture and leaks away charge remaining on ESC during and after transfer. (c) Current through  $C_{ESC}$  spikes and exponentially decays upon charging and reverses when charge is transferred to  $C_{ECC}$  (left) where current through  $C_{ECC}$  spikes at  $t_2$  (right).

## 5.5 Results

### 5.5.1 Charge capture and transfer efficiencies

Figure 5.4(a) depicts the efficiency with which charge is captured by the ESC within the hybrid circuit as a function of  $C_{ESC}$  for fixed  $C_{ECC}$ , i.e., changing capacitance ratio of  $C_{ECC}$  to  $C_{ESC}$ . This charge capture efficiency is given by the total charge captured

by the ESC, namely  $Q_{\text{ESC}}(\text{capture}) (= C_{\text{ESC}} \times V_{\text{ESC}}(\text{capture}))$  versus the total amount of charge that flowed through  $C_{\text{ESC}}$  while charging,  $Q_{\text{in}} (= \int I_{\text{ESC}}(\text{capture}) dt)$ . The charge capture efficiencies for all circuits are  $\sim 100\%$  when  $V_{\text{in}} \leq 4$  V. As the source voltage level increases to about 4 V, corresponding to electric field about 4 MV/cm, the capture efficiency drops substantially, a consequence of the increasing leakage current (or decreasing leakage resistance) as the field enters the Fowler-Nordheim regime (Fig. 5.1(b)). The effect of Fowler-Nordheim tunneling increases with  $C_{\text{ESC}}$  (with  $V_{\text{in}} > 4$  V) because while capacitance increases proportionally with device total area the leakage resistance,  $R_{\text{ESC}}(V_{\text{in}})$ , decreases (inversely) with area, resulting in the dramatic reduction of capture efficiency at  $V_{\text{in}} > 4$  V with increasing  $C_{\text{ESC}}$  (refer to Figure 5.3). The charge lost to this internal resistance at high field may be reduced by optimizing the length of time the circuit is in the capture state, i.e., making it only long enough to achieve nearly the input voltage level, and not more.

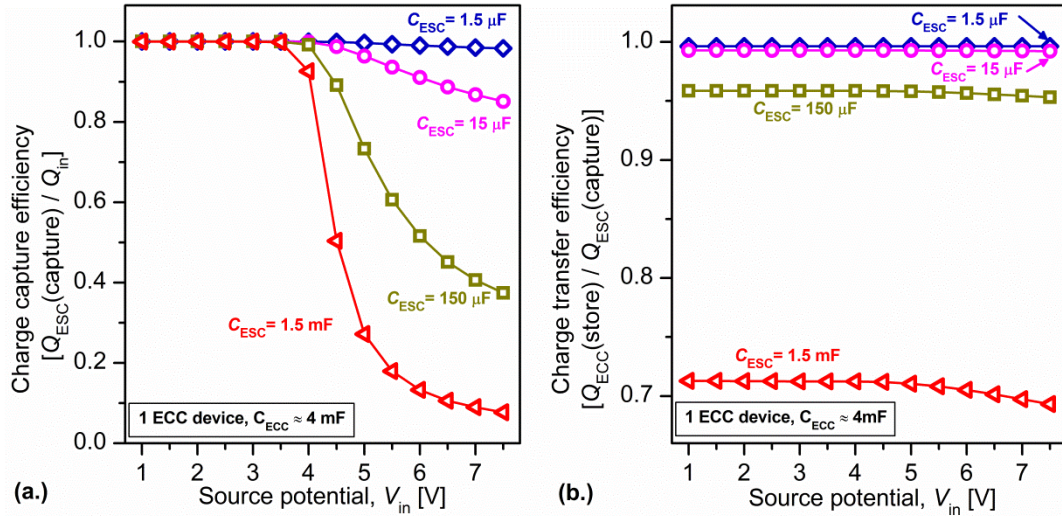


Figure 5.4 **Hybrid circuit performance (nonlinear devices)**. (a) Charge capture efficiency for various hybrid ESC-ECC circuits keeping  $C_{\text{ECC}}$  fixed and varying  $C_{\text{ESC}}$  as a function of  $V_{\text{in}}$ . Capture efficiency increases with increasing  $CR$  ( $C_{\text{ESC}} \ll C_{\text{ECC}}$ ) since the  $R_{\text{ESC}}$  scales as  $R_{\text{ESC}}/N$  and is relatively constant at  $V_{\text{in}} \leq 4$  V but drops with increasing  $V_{\text{in}}$  for all designs. (b) Charge transfer efficiency as a function of  $V_{\text{in}}$  for the various circuits shown in (a). Transfer efficiency drops with increasing  $N$  and with  $V_{\text{in}} > 4$  V.



The ratio of the charge stored on the ECC,  $Q_{\text{ECC}(\text{store})}$ , to the charge captured by  $C_{\text{ESC}}$ ,  $Q_{\text{ESC}(\text{capture})}$ , provides a measurement of the charge transfer efficiency of the hybrid circuit (i.e., ignoring charge left on the ESC in the store phase, which will likely disappear through leakage current losses anyway). Charge transfer efficiencies of the hybrid circuits are shown in Figure 5.4(b). For small  $C_{\text{ESC}}$  the charge transfer efficiency is high, even at higher  $V_{\text{in}}$ , because more charge is transferred from the ESC in the capture phase to the ECC in the transfer phase, hence leaving less charge on ESC to drain away through leakage currents. As shown in Fig. 5.4(b), increasing  $C_{\text{ESC}}$  causes reduced charge transfer efficiency to the ECC, as the capacitance ratio leaves more charge on the ESC from the transfer phase.

The simulation enables exploration of how key parameters of the hybrid circuit affect where charge ultimately goes in the energy capture and store function of the hybrid circuit. Trends are indicated in Figure 5.5 as a function of ECC and ESC capacitance values, the shaded areas depicting the distribution of charge. It should be noted that the vertical charge axes are different from row to row, increasing by  $10\times$  from top to middle and then by  $10\times$  again from middle to bottom.

The simulation accounts for charge conservation as follows:

$Q_{\text{in}} = Q_{\text{ECC}(\text{store})} + Q_{\text{ESC}(\text{store})} + Q_{\text{loss}(\text{xfer})} + Q_{\text{loss}(\text{capture})}$  is the total charge supplied to the ESC during capture stage where

$Q_{\text{ECC}(\text{store})} = \int I_{\text{ECC}(\text{xfer})} dt$  is the charge left on the ECC in the store state ( $I_{\text{ECC}(\text{xfer})}$  is the current through the ECC during charge transfer),

$Q_{\text{ESC}(\text{store})} = C_{\text{ESC}} \times V_{\text{ESC}(\text{capture})} + \int I_{\text{ESC}(\text{xfer})} dt$  is the charge left on the ESC in the store state (which may be subsequently lost over time to leakage currents,  $I_{\text{ESC}(\text{xfer})}$  is

the current through the ESC during transfer stage and  $V_{ESC}(\text{capture})$  is the maximum potential across  $V_{ESC}$  during capture stage)

$Q_{\text{loss}}(\text{xfer}) = C_{ESC} \times V_{ESC}(\text{capture}) - Q_{ESC}(\text{store}) - Q_{ECC}(\text{store})$  is the charge lost during the transfer phase from ESC to ECC and

$Q_{\text{loss}}(\text{capture}) = \int I_{ESC}(\text{capture}) dt - C_{ESC} \times V_{ESC}(\text{capture})$  is the charge lost during the capture phase for charging the ESC.

A major goal is to capture maximum charge  $Q_{ECC}(\text{store})$  on the ECC, where it can be stored for extended periods until needed. This parameter is indicated by the blue regions labeled as such in Fig. 5.5. Clearly a first step toward this goal is to maximize the initial charge capture from the input signal, i.e. increasing  $C_{ESC}$  (moving from top to bottom row of Fig. 5.5). Noting, again, the  $10\times$  increase in vertical charge axes in Fig. 5.5 from top to bottom, increasing the capacitance of the ESC  $C_{ESC}$  does increase the charge stored on the ECC,  $Q_{ECC}$ , substantially.

However, this increase is somewhat less than proportional, because other factors enter the picture. The larger  $C_{ESC}$  brings with it larger charge losses in the capture phase, associated with leakage current in the ESC, as shown by the green components  $Q_{\text{loss}}(\text{capture})$  in the middle and more prominently in the bottom row, and by the decreasing efficiency values  $\eta = Q_{ECC}/Q_{in}$  at  $V_{in} = 7 \text{ V}$  (upper right of each plot) with larger  $C_{ESC}$ .

With increasing  $C_{ESC}$  more charge is left on the ESC (red areas) and less on the ECC (blue areas), an undesirable result since a long duty cycle (with switch S1 open) would ultimately lose the charge on the ESC through the leakage resistance  $R_{ESC}$ . However, this effect can be compensated by also increasing  $C_{ECC}$  as shown in the middle

and bottom rows of Fig. 5.5. Larger values of  $C_{\text{ESC}}$  also increase the charge losses associated with capture by the ESC, depicted by the green regions and consistent with Fig. 5.4(a). Charge loss during transfer from the ESC to the ECC in the transfer phase is small.

The division of charge between ESC and ECC that happens during the transfer phase produces the same steady state voltage across both devices. It is important that the voltages not be too high, for the ECC to prevent electrolyte degradation and for the ESC to prevent dielectric breakdown. As CR increases – i.e.,  $C_{\text{ECC}}$  increases at constant  $C_{\text{ESC}}$  – the ECC is able to absorb relatively more charge from the ESC without increasing its voltage, and larger  $C_{\text{ECC}}$  for a fixed  $Q_{\text{ESC}}$  means that the final ECC voltage will be lower.

The results in Fig. 5.5 also illustrate a particularly important message – the tradeoff between charge capture and energy efficiency. Charge capture and storage on the ECC is maximized by large ECC and large ESC (bottom right of Fig. 5.5). However, this domain has a relatively low energy efficiency, in that a substantial amount of charge is lost during the capture phase to leakage currents in the ESC. The desirable balance between charge capture and energy efficiency depends on the application, involving multiple metrics specific to that application. Furthermore, the quantitative tradeoffs depend as well on materials, device structure, and electrical and electrochemical behavior, features which may change with ongoing research.

There are numerous other ways to depict the multivariate behavior of this simple system, but space limitations preclude a more extensive discussion. Nevertheless, this discussion illustrates that models such as that employed here have the capability to reflect the nuances and nonlinearities of real physical systems, enabling rapid assessment and

optimization of key metrics, revealing important trends, and providing feedback on where improvement in physical or electrochemical parameters would best enhance system performance.

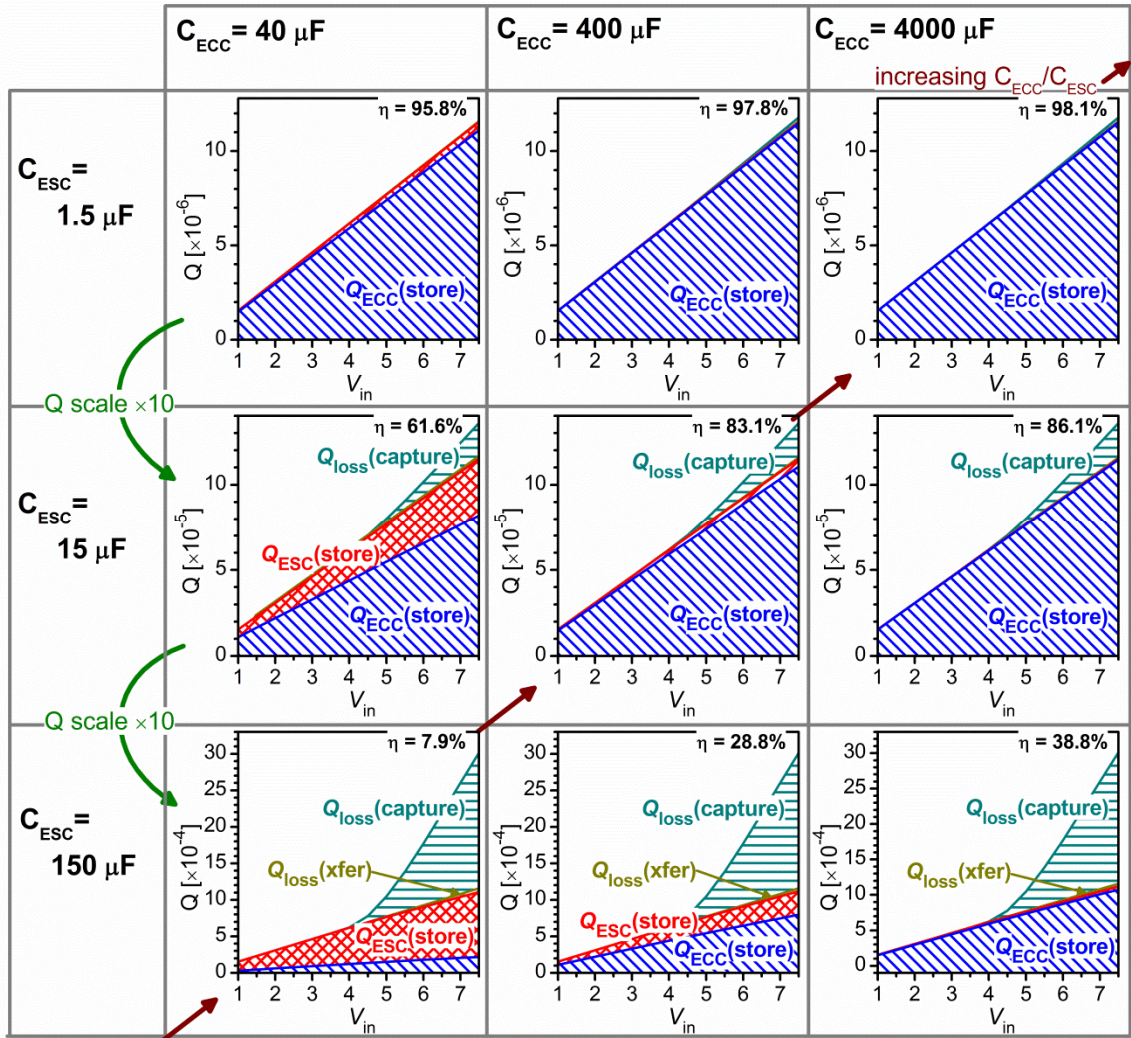


Figure 5.5 Charge distribution in hybrid circuit (nonlinear devices). The collective charge distribution of various hybrid circuits with regions indicating the amount of charge stored on ECC after transfer,  $Q_{ECC}(\text{store})$ , charge remaining on ESC after transfer,  $Q_{ESC}(\text{store})$ , charge lost during transfer,  $Q_{\text{loss}}(\text{xfer})$ , and charge lost during ESC capture,  $Q_{\text{loss}}(\text{capture})$ , respectively). Rows have same  $C_{ESC}$  value, columns have same  $C_{ECC}$  value.  $\eta$  indicates the ratio of  $Q_{ECC}/Q_{\text{in}}$  at  $V_{\text{in}} = 7\text{V}$ .

### 5.5.2 Hybrid charging rates and energy efficiencies

Next, the charging rate and energy efficiency of the hybrid ESC-ECC circuit in comparison to using the ECC alone is considered, using square wave input voltage waveforms with a low duty cycle (pulse width vs. pulse period) as a simplified representation of the transient power excursions (as found in renewable sources, transportation, and grid switching environments). In these situations it is desirable to have a system capability for power leveling in addition to high energy density storage (e.g. batteries).

The energy of an ECC-only circuit is compared to two different hybrid ESC-ECC circuit configurations, using  $C_{\text{ECC}} = 4 \text{ mF}$  and  $C_{\text{ESC}} = 1.5 \text{ or } 15 \text{ }\mu\text{F}$ , for a pulse period of  $0.1 \text{ ms}$ , and duty cycle of  $1.0\%$ . Figure 5.6(a) shows the cumulative amount of energy stored on one unit ECC ( $C_{\text{ECC}} \approx 4 \text{ mF}$ ) as a function of increasing pulse number. For the ECC-only circuit,  $V_{\text{in}}$  is set to  $2.4 \text{ V}$  to stay within the electrochemical stability of the electrolyte ( $1.2 \text{ V}$  gradient across each symmetric electrode and  $1 \text{ }\Omega$  series resistance between the ESC and ECC prevents overvoltage across ECC electrolyte). The charge and energy for the ECC-only circuit requires several thousand cycles to approach saturation, or full charge, whereas longer pulse widths would reduce the time (i.e. number of pulses) required to fully charge the ECC. Experimental data is extrapolated (Figure 5.2(c)) to estimate the ECC capacitance values for the abrupt rise in voltage at the introduction of the square pulse and the constant voltage during the pulse length.

A larger  $V_{\text{in}}$  can be applied by introducing the  $C_{\text{ESC}}$  into the circuit because it experiences catastrophic breakdown at a higher voltage. A  $V_{\text{in}}$  of  $7 \text{ V}$  is chosen to operate the ESC near its maximum energy density to supply, capture and transfer more energy to

the ECC with each pulse. Here, the period and pulse width of  $V_{in}$  is the same as for the ECC-only circuit. The difference is that when  $V_{in}$  is in its off or zero-state, the ESC transfers the  $Q_{ESC}(\text{capture})$  to the ECC.

Figure 5.6(a) shows the enhancement in charging rates using the hybrid circuit, the number of pulses required to increase  $E_{ECC}(\text{store})$  above 10.4 mWs is used for comparison to the ECC-only circuit. The rate of charging becomes  $\sim 8.9\times$  faster with the hybrid with  $C_{ESC} = 1.5 \mu\text{F}$  and increases further to  $\sim 12.2\times$  with the hybrid of  $C_{ESC} = 15 \mu\text{F}$ . The charging rates of the ESC are dependent on the value of  $C_{ESC}$  and the pulse width because the time-dependence of voltage across the ESC depends on the RC time constant of the input circuit, with  $V_{ESC}$  varying as  $(1 - \exp(-t/R_{series}C_{ESC}))$ , with risetime faster for small  $C_{ESC}$ . This value of  $V_{ESC}(\text{capture})$  and the capacitance ratio of  $C_{ECC}$  to  $C_{ESC}$  determines  $V_{eq}$ . Even though  $V_{ESC}(\text{capture})$  is lower with a larger  $C_{ESC}$ ,  $V_{eq}$  is slightly larger when  $C_{ESC}$  is larger. Additionally, the amount of charge captured is larger for large  $C_{ESC}$  (see Figure 5.5), providing more charge for transfer and resulting in greater  $Q_{ECC}(\text{store})$  for larger  $C_{ESC}$ . Since  $E = \frac{1}{2} Q_{ECC}(\text{store}) \times V_{eq}$ , more energy is supplied to the ECC with the each pulse when  $C_{ESC} = 15 \mu\text{F}$ . Reducing  $V_{in}$  to 4 V where the internal resistance sufficiently large reduces charging rates (shown in Figure 5.6(a)). Compared to the ECC-only circuit, the hybrid circuit supplied with 4 V charges 4.1 and  $5.6\times$  faster with the hybrid with  $C_{ESC}$  of 1.5 and 15  $\mu\text{F}$ , respectively. The reduced charging rates are expected since the amount of energy that can be captured by the ESC is limited by the reduced  $V_{in}$ .

Figure 5.6(b) shows the energy efficiency of charging the ECC-only circuit and the hybrid circuits from Figure 5.6(a). Energy efficiency here is calculated by taking the

cumulative sum of the power transferred (power transfer =  $I_{ECC}(xfer) \times V_{ECC}(xfer) \times dt$ ) with each pulse divided by the cumulative sum of the incoming power of the pulses (incoming power =  $I_{ECC}(capture) \times V_{in} \times dt$ ), where  $dt$  is the computational time interval,  $10^{-8}$  s. The following summarizes the energy efficiency calculation:

$$\text{Energy Efficiency} = \frac{\sum_{n=1}^{\text{pulses}} \sum_{t=t_2}^{t_3} (I_{ECC}(xfer) \times V_{ECC}(xfer) \times dt)}{\sum_{n=1}^{\text{pulses}} \sum_{t=t_1}^{t_2} (I_{ECC}(capture) \times V_{in} \times dt)}$$

Figure 5.6(b) shows the energy efficiency of the ECC-only circuit charged to 99% capacity is ~49.3% (limits in numerator of Equation 1 for ECC-only are same as denominator). Introducing the ESC component increases the charging rates (as shown in Figure 5.6(a)) and its energy efficiency at the pulse number required to obtain 99% capacity provides a 5% and 37% larger efficiency for  $C_{ESC}$  of 1.5 and 15  $\mu\text{F}$ , respectively, with  $V_{in} = 7$  V over that pulse number for the ECC-only circuit. For  $V_{in} = 4$  V, the efficiency trajectories for a  $C_{ESC}$  appear to be aligned with that for  $V_{in} = 7$  V, suggesting the leakage resistance does significantly influence loss. Because  $V_{in} = 4$  V requires additional pulses before the ECC is charged, the energy efficiencies are improved by 34.5% and 35.1% for  $C_{ESC}$  of 1.5 and 15  $\mu\text{F}$ , respectively, over that for the ECC-only circuit. Reducing  $V_{in}$  by 75% shows an increase in the charging efficiencies of the hybrid circuits by ~75%. Figure 5.6(a)-(b) shows the hybrid circuit can be used to charge the ECC to 99% capacity significantly faster with a pulsed square wave and that higher efficiencies at these reduced charging time scales are possible. Additionally, the

amplitude of  $V_{in}$  can be modulated to provide rapid charging rates and/or improvements in energy efficiency.

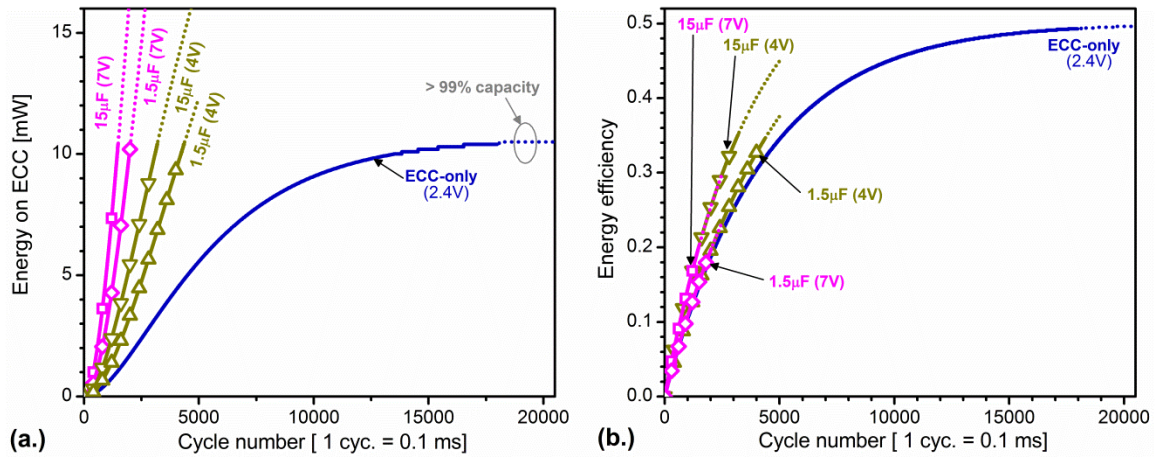


Figure 5.6 **Performance during charging.** Energy and energy efficiencies for charging the ECC component to 99% efficiency with 1.0% duty cycle. (a) For the same pulsing sequence, hybrid circuits charge significantly faster - 4.1 and 8.9x faster for 1.5µF with  $V_{in} = 4V$ , and 5.6 and 12.2x faster for 15µF with  $V_{in} = 7V$ . (b) Efficiencies at those maximum  $E_{ECC}(\text{store})$  are increased. Efficiencies of charging are increased by 75% for  $V_{in} = 4V$  as compared to  $V_{in} = 7V$ .

## 5.6 Discussion

The results presented here have been generated by a very simple MatLab/Simulink model of a hybrid ESC-ECC circuit under idealized conditions, using a limited set of parameters. Nevertheless, the model takes into account important physical realities, including nonlinearities of different origins for the ESC and ECC devices, and their representation in empirically-determined response surface models (through lookup tables). Not included in the model is the fading of capacitance with charge/discharge cycling of electrochemical storage devices, a feature which should be addressed in subsequent models.

The mismatch of voltage limitations for the ESC and ECC devices derives from their inherently different mechanisms of charge storage. In the hybrid circuit here, charge redistribution from the ESC causing its higher voltage capability to be distributed



at lower voltage to ECC devices with higher capacitance, thus lowering the ECC voltage when charge redistribution between the ESC and ECC during the transfer phase is completed. As noted above, some wire resistance ( $1 \Omega$ ) is required for using the higher input voltage allowed by the ESC to prevent sufficiently short burst of overvoltage to the ECC when the ESC and ECC are connected in the transfer phase will not substantially degrade the electrolyte.

An implicit assumption in building the model has been that the design should attempt to use the quite different voltage ranges compatible with the ESC and ECC devices, suggesting active switching circuitry in the hybrid system as described above. Since in the primary interest was to gather an understanding whether there is potential benefit from the hybrid ESC-ECC circuit (as found in other hybrid electrochemical circuits<sup>154,158,165-168</sup>), the model does not account for the energy or power costs of this switching circuitry. This issue is important to address in the future. Indeed this would be but a first step in a larger system design analysis. Since the time profiles of power fluctuations are not regular, and can be widely varying, an active circuit may well benefit from onboard intelligence to adapt switching algorithms to incoming power profiles, a question far beyond the scope of the present work. Such capability could also play a useful role in monitoring device degradation and anticipating safety concerns.

While the results presented here reflect only a limited set of examples, the model can be expanded for broader investigation. One area is to assess new permutations of component parameters and the additional mechanisms (e.g. ECC capacitance fading) important to application. Another is to accommodate a variety of time-varying input (and output) voltage and power profiles. As a simulation model this is a natural next step, and

it is important because the switching algorithms and device parameters should be developed for the anticipated application. One can imagine the simulation model employed to handle a random input power profile, exercised by changing the model to see how energy capture/storage and efficiency change.

Finally, the model presents opportunities for research prioritization in enabling a prediction of how much performance would improve if certain material, structural, or electrochemical modifications could be made or discovered. For example, the impact of a lower leakage insulator in the ESC can be directly predicted from the simulation model, providing feedback on the potential value of such efforts before they are pursued.

## 5.7 Conclusions

This investigation of hybrid ESC-ECC circuits was initiated to see whether the high power of the ESC could be incorporated and employed to extend the power-energy capability of an electrochemical storage system. Analysis based on the simulation model shows clear benefits of the hybrid ESC-ECC circuit in enhancing the power capability over that of an ECC-only system, since the high power capability of the ESC complements the higher energy density of the ECC. Indeed, the notion of hybrid circuits to function with both high power and high energy is important, and well known within the electrochemical storage device arena.

The simulation model incorporates most (though not all) important aspects of the distinctly different ESC and ECC devices, particularly their nonlinearities associated with different physical mechanisms. Indeed, the simulation results indicate faster charging/discharging is possible in the hybrid system, but it incurs other constraints,

particularly lower charge capture efficiency associated with the inherent leakage current of the ESC device around which the dynamic switching of the hybrid circuit must be designed. In the end this leads to a tradeoff between maximum energy/charge capture and energy efficiency, a design preference which is dependent on other factors (cost, space, weight) specific to the application.

Besides its benefit in high power, the ESC suffers from intrinsic leakage currents that deplete its charge in times short compared to those needed for energy storage. The ESC-ECC hybrid resolves this dilemma, albeit with a penalty in terms of energy efficiency. On the other hand, the ESC's charge leakage problem proves beneficial for capturing intermittent power bursts, in that the ESC is typically partially discharged when a power burst appears at the input, so it can capture much of the energy in that burst. Thus the ESC-ECC hybrid is particularly attractive for power leveling applications<sup>169-172</sup> in conjunction with high energy density storage schemes (e.g. batteries).

In some sense the hybrid circuit is a demonstration that the quite different ESC and ECC devices can work synergistically together, each compensating for the limitations of the other. Energy captured by ESC can be transferred to the ECC at a rate which is faster than the ESC's self-discharge but slower than the abrupt voltage bursts, so that more of the input charge is stored. The energy held on the ECC can then be stored for significantly longer lengths of time. The versatility of the ESC-ECC combination – in power and energy – makes it attractive for a variety of energy storage applications, most notably in adding power leveling capability aimed at time-varying power of renewables (e.g. wind bursts, solar fluctuations due to clouds); acceleration, deceleration, and fast charging for electric vehicles; and demand spikes on the grid.

## Chapter 6: Conclusions and Outlook

### 6.1 Summary

The overall goal of this dissertation was to fabricate, characterize and simulate the optimized performance of the nano-electrostatic capacitor to evaluate its role in energy storage. The main findings of this work are as follows:

- 1) A nanoengineering strategy has been developed which effectively modifies the surface topography of the ESC's nanotemplate resulting in a  $2\times$  improvement in energy density, 1.5 Wh/kg.
- 2) A dynamic, experimentally derived model for characterizing the ESC has been built to determine the role of the ESC device in electrical energy storage.
- 3) Modeling a hybrid circuit (ESC acting as a front-end component to the higher energy density ECC) has shown the high power density of the ESC can be combined with the high energy of the ECC - charging the ECC to near-maximum capacity up to  $12\times$  faster than using an ECC-only circuit.

The first finding focused on nanoengineering the AAO template nanotopography for increasing the applied voltage range and thus energy density since  $E = \frac{1}{2} CV^2$ . Without template modification, inherent interpore asperities located at the pore openings caused localization of the electric field and resulted in premature (low field) breakdown. The asperities were effectively smoothed by introducing a non-porous BAA film on the first anodized Al surface prior to subsequent anodization. As a result, the

nanoengineering strategy blunted these asperities and increased the field range up to  $2.5\times$ , near the breakdown strength of the insulator, providing the marked improvement in energy density. Methods of further improving the energy density were discussed.

The second finding used experimentally derived data to build an accurate and dynamic model for depicting the performance characteristics of the nanoengineered ESC device. The model was built in MatLab/Simulink to study the effect of the nonlinear internal resistance on the charge retention as a function of source potential. Charge retention studies indicated that for the ESC to be used at its higher energy density, i.e., high operating voltages, the charge would have to be transferred to an external load or alternative component within ms before significant self-discharge occurred.

The last finding demonstrated the feasibility of the ESC for energy storage. The ESC's ability to rapidly capture and release energy is an attractive characteristic for energy storage devices, as it can instantaneously meet load demands. Even though the energy density was improved with template nanoengineering, its nonlinear internal resistance provides poor charge retention especially when higher potentials are applied. Rather, simulations demonstrated that the ESC could act as a front-end component for capturing charge and transfer its charge to a higher energy density component, like the ECC. Results showed that by selecting the appropriate capacitance ratios, the ESC and ECC worked together efficiently as a hybrid circuit. The ESC is able to capture the charge from sharp transients and transfer it to the ECC. The energy capacity of the ECC could be reached up to  $12\times$  faster using the ESC as a front-end component.

## 6.2 Outlook

Nanostructures are promising foundations for energy storage devices, offering the ability to improve efficiency, energy capacity, charge/discharge rates, and with reduced size/weight. Several nanostructures have shown marked improvements in energy density and/or power density. Specifically, this dissertation has shown that template nanoengineering resulted in higher ESC energy densities. However, there is not yet a single device that is able to provide the lifetime, stability and both the energy and power capability desired from electrical energy storage devices. Continued identification and exploration of effective nanoengineering methods which modify material and/or structure properties be studied for developing more efficient, higher performance nanostructures for electrical energy storage.

While nanoengineering may open the application space for nanodevices, nonlinearities may be present that were otherwise masked by the performance limitations or these nonlinearities may not be apparent when ranking in terms of energy density and power density. The nonlinearities must be considered in regards to how the device stores energy. Additionally, it must be understood how the nonlinearities affect efficiency and may dominate the performance under various load and source profiles/conditions.

Device modeling of the charge, retention and discharge dynamics is an integral part of overall nanoengineering design strategies for electrical energy storage devices. Accurate experimentally derived models of nanodevices are necessary to identify: (1) methods for effectively mitigating the nonlinearities, (2) physical properties that introduce performance constraints, (3) factors that cause device degradation/aging over its lifetime, and/or (4) materials properties that limit performance.

A parallel strategy to the optimization of a single device is combining different electrical energy storage devices into a hybrid circuit configuration to understand if and how the devices complement each other for achieving both high energy and power capabilities. Specifically, the nanohybrid circuit discussed in Chapter 5 showed the electrostatic capacitor acting as a front-end component to an ECC, improving the charging rate of the ECC up to a factor of 12. Other basic circuit models, like electrostatic-battery hybrid circuits and multi-device circuits, can provide further insights into the versatility and potential opportunities offered from various hybrid circuits. Basic models should be refined to account for the effect of various periodic and random source and load profiles, effects of degradation and aging on storage capacity, and energy loss associated with active or inactive circuitry components. Lastly, experimental verification and characterization should be performed in parallel to identify suspecting or unsuspecting cause-and-effect relationships and to identify methods for improved process controls and materials optimization.

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